Design and Analysis of Mem-elements Emulator using Analog Building Blocks

Thesis

Submitted for the Award of the Degree of

Doctor of Philosophy

by

Nisha

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CERTIFICATE

I, **Nisha**, hereby certify that the research work presented in the thesis entitled "**Design and Analysis of Mem-elements Emulator using Analog Building Blocks**" being submitted by me with **Registration No. 901806018** to the Department of Electronics and Communication Engineering,Thapar Institute of Engineering and Technology, Patiala, India in the fulfillment of the requirements for the award of the degree of "**Doctor of Philosophy**". It is an authentic record of bonafide research work carried out under the guidance and supervision of **Dr. Shireesh Kumar Rai**, Assistant Professor, DECE, TIET, Patiala, and **Dr. Rishikesh Pandey**, Assistant Professor, DECE, TIET, Patiala.

The matter presented in this has not been submitted either in part or full to any other university or institute for the award of any other degree.

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NISHA

Dedicated to
LORD KRISHNA

ABSTRACT

The evolution of electronic components has led to the discovery of various mem-elements, including memristors, memcapacitors, and meminductors, which exhibit memory-dependent behavior. These elements are poised to revolutionize many fields of science and engineering. However, fabricating these devices at the nanoscale remains a significant challenge, thereby creating a demand for mem-element emulators to facilitate experimental research and circuit design. Earlier, electronic systems relied on fundamental components like resistors, capacitors, and inductors alongside semiconductor devices. Even while these conventional components are essential, they are not very flexible in responding to changing environmental conditions. Mem-elements overcome these limitations and potentially revolutionize the industry by enhancing circuit design, functionality, and efficiency. Therefore, researchers and practicing engineers use emulation techniques to replicate mem-element functionality, allowing engineers to study their behavior without needing physical prototypes. This thesis presents the development of a versatile mem-element emulator capable of reproducing mem-elements' behavior, including memristors and meminductors. This work lays the groundwork for further exploration of mem-elements in future electronic systems and provides a platform for simulating their diverse functionalities.

In the thesis, six designs of mem-element emulators have been presented, including three for memristors and another three for meminductors. These circuits utilize analog building blocks such as operational transconductance amplifiers (OTAs), current differencing buffered amplifiers (CDBAs), voltage differencing gain amplifiers (VDGAs), fully-balanced voltage differencing buffered amplifiers (FB-VDBAs), and voltage differencing transconductance amplifiers (VDTAs). The first memristor emulator is designed using OTA and CDBA. The second memristor emulator employs VDGA, whereas the third memristor emulator is designed using FB-VDBA. These designs feature a grounded capacitor as a memory element and achieve grounded and floating configurations with incremental and decremental topologies. In addition, the first meminductor emulator is designed using two OTAs. The second meminductor emulator has been designed using VDGA, while the third meminductor emulator is designed using a VDTA. In all designs of meminductor emulators, CDBA has been utilized to obtain incremental and decremental topologies. One of the capacitors is used as a memory element, while the other is used to form the inductance.

The emulator's performance is thoroughly analyzed through pinched hysteresis loops, non-volatility tests, temperature analyses, Monte Carlo analyses, etc. These analyses confirm the

efficacy of proposed emulator designs in natural environments. The emulators also offer the feature of electronic tunability, often required to adjust the internal parameters of the circuit. These emulators display pinched hysteresis loops across a broad frequency range (hundreds of Hz to MHz). Both memristor and meminductor emulators present promising results that offer a wide range of memristances and meminductances. The memristor emulators have been used in the design of analog filters, while meminductor emulators are used in adaptive learning and chaotic circuits, demonstrating satisfactory performance. Non-ideal analyses have also been conducted to verify their performance in the natural environment. The simulation results have been obtained using Eldo simulation tools for 180 nm CMOS technology parameters.

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ABBREVIATIONS

ASK	Amplitude-shift keying
ABB	Analog building block
ADC	Analog to digital converter
AM	Analog multiplier
BPSK	Binary phase-shift keying
BFSK	Binary frequency-shift keying
BJT	Bipolar junction transistor
BOCCII	Balanced output second generation current
CCII+/-	Second generation current conveyor
CCCDTA	Current-controlled current differencing transconductance amplifier
CFOA	Current feedback operational amplifier
CBTA	Current backward transconductance amplifier
CDBA	Current differencing buffered amplifier
CMOS	Complementary metal oxide semiconductor
CFTA	Current follower transconductance amplifier
CDTA	Current differencing transconductance amplifier
CCTA	Current conveyor transconductance amplifier
CC-CCTA	Current-controlled current conveyor transconductance amplifier
CNFET	Carbon nanotube field effect transistor
CCIITA	Current conveyor transconductance amplifier
DDCC	Differential difference current conveyor
DVCCTA	Differential voltage current conveyor transconductance amplifier
DTMOS	Dynamic threshold voltage MOSFET
DVCC	Differential voltage current conveyor
DO-OTA	Dual-output operational transconductance amplifier
DO-CCII	Dual-output second-generation current conveyor
DXCCDITA	Dual-X current conveyor differential input

	transconductance amplifier
ECCII	Electronically tunable second-generation current conveyor
EDDCC	Electronically tunable differential different current conveyor
FB-VDBA	Fully-balanced voltage differencing buffered amplifier
FDCCII	Fully-differential second-generation current conveyor
FSK	Frequency-shift keying
FPGA	Field programmable gate arrays
FCS	Floating current source
FPAA	Field programmable analog array
F-MRE	Floating memristor emulator
G-MRE	Grounded memristor emulator
IAC	Inverter adder circuit
ICCTA	Inverting current conveyor transconductance amplifier
IoT	Internet of things
LDR	Light dependent resistor
MO-OTA	Multi-output operational transconductance amplifier
MDVCCTA	Modified differential voltage current conveyor transconductance amplifier
MVDCC	Modified voltage differencing current conveyor
MO-VDTA	Multi-output voltage differencing transconductance amplifier
MRE	Memristor emulator
MIE	Meminductor emulator
OTA	Operational transconductance amplifier
PHL	Pinched hysteresis loop
STDP	Spike timing dependent plasticity
TOA	Transimpedance operational amplifier

TG	Transmission gate
VDCC	Voltage differencing current conveyor
VDTA	Voltage differencing transconductance amplifier
VDGA	Voltage differencing gain amplifier
VDIBA	Voltage differencing inverted buffered amplifier

CHAPTER 1
INTRODUCTION

1.1 Introduction

The electronics circuits rely heavily on fundamental components like resistors, capacitors, and inductors along with semiconductor devices to create all sorts of electronic gadgets and systems. Resistors control the flow of electricity, capacitors store or release electrical energy, and inductors create a magnetic field which are crucial for making electronic circuits but their limitations hinder the full potential of electronic technology. These components are not very good at changing their behavior based on what is happening around them. This makes it hard to deal with the changing needs of modern electronics. Therefore, while resistors, capacitors, and inductors are essential for building electronic circuits, their static nature restricts adaptability to new environmental conditions. This limits their use in the ever-changing demands of today's electronic devices. With the rising power consumption of electronic devices, power efficiency emerged as a pressing concern. Traditional electronic components struggled to achieve optimal energy efficiency while maintaining performance, posing significant hurdles in the pursuit of sustainable and eco-friendly electronics. The resistors, capacitors, and inductors faced challenges in integration and scaling issues to fulfil the demand for miniaturization and energy-efficient computing. To overcome the above-mentioned issues, a new passive element namely memristor is under investigation which was presented by Prof. Leon Chua in 1971 as a fundamental element alongside resistors, capacitors, and inductors [1, 2]. The proposition arose from recognizing a balance between charge and flux, indicating the existence of a fourth fundamental component defined by the association between charge and flux. Professor Chua's theory opened the door for the development and eventual realization of the memristor as a practical device, which came to fruition several decades later in 2008 through advancements in nanotechnology and material science by Stanley William and his collaborators at Hewlett Packard Lab [3]. Following the widespread applications of the memristor, two additional passive components, known as meminductor and memcapacitor, were also identified using the same theoretical outline. The memristor, meminductor, and memcapacitor are together known as mem-elements. The mem-elements are crucial in VLSI systems due to their distinctive characteristics. The stable and long-term retention of stored values to maintain the integrity of analog signals over time

makes them suitable for applications like data converters. The low leakage current is essential to minimize power consumption in circuits. Therefore, mem-elements retain their stored values without excessive power dissipation and ensure energy efficiency [4-5]. The high-speed applications require mem-elements because of their capability of fast read and write operations to meet the speed requirements. Before the mem-elements came along, electronic engineering mainly relied on fundamental components like resistors, capacitors, and inductors along with semiconductors. These components did their job, but they had limitations. They couldn't store much data, weren't very energy-efficient, and weren't powerful for computing tasks. Despite being somewhat effective, these old methods held back electronic systems from reaching their full potential. Therefore, the role of mem-elements is now viewed as the future of the electronics industry. It brought a whole new way of doing things to electronics. Unlike the old components, the mem-elements could tackle many of the problems encountered by traditional technologies. Its introduction marked the start of a fresh era in electronics, where memory technology, computing power, and energy efficiency all took big leaps forward. The mem-elements opened doors to exciting new possibilities in electronic engineering, promising better performance, reliability, and eco-friendliness in electronic systems. The introduction of mem-elements has the potential to bring significant changes to the analog industry, particularly in terms of circuit design, functionality, and efficiency. The mem-elements offer more efficient and versatile analog circuits. Engineers can incorporate mem-elements into circuit designs to optimize performance, reduce power consumption, and enhance functionality. It has the potential to revolutionize memory technology in the analog industry. It contributes to increased energy efficiency in analog systems and enables new possibilities in signal processing applications. Since memristor, meminductor, and memcapacitor modify resistance, inductance, and capacitance based on the signal characteristics respectively that allows their usage in adaptive and dynamic signal processing, leading to improved performance and versatility. The mem-element is essential for the progress of neuromorphic computing [6-7], which aims to mimic the brain's structure and functionality. In the analog industry, it could lead to the creation of intelligent systems capable of learning, adaptation, and pattern recognition, [8-9], creating new opportunities for applications in fields like artificial intelligence, robotics, security, autonomous systems, and neurocomputing. Mem-elements are key to creating systems designed to emulate the human brain's architecture and operations so that the systems achieve energy-efficient and parallel processing, enabling tasks such as cognitive

computing, sensory processing, and decision-making. It is used in security applications to implement physical unclonable functions [10-13] which are physical structures in integrated circuits that generate unique identifiers based on manufacturing variations. These identifiers serve as cryptographic keys for device authentication and secure communication. It can also be used in biomedical applications [14-18] such as neural interfaces, brain-machine interfaces, and implantable devices. Mem-element-based neural interfaces can record and stimulate neural activity with high precision and efficiency, enabling advancements in neuroscience research and medical treatments [19-21]. Mem-elements can be integrated into energy harvesting systems to improve efficiency and power management. Devices using memristor technology can capture energy from various sources, including solar, thermal, and vibrational, supporting the functionality of self-powered sensors, IoT devices, and wearable electronics [22-25]. Overall, mem-elements are driving innovation across multiple disciplines, offering new opportunities for advancements in computing, memory storage, security, adaptive electronics, energy harvesting, non-volatile memory devices and biomedical engineering [26-27]. As research and development in mem-element technology continue to progress, we can expect to see even more diverse and impactful applications in the future.

Despite having so many applications, it has some arguments to be worked on such as its physical implementation and integration into electronic circuits, the transition from research prototypes to commercial mem-elements-based products is a significant goal. Companies like Hewlett-Packard, Intel, and others are working on bringing mem-elements technologies to the market. The researchers find a unique way to work with the mem-element in the form of emulators. The emulators are hardware implementations that duplicate the behavior of definite electronic components, devices, or systems. They allow engineers, researchers, and developers to test, validate, and experiment with electronic designs without using the actual physical components. Emulators have been a fundamental part of electronics development, helping reduce costs, speed up prototyping, and facilitate testing.

1.2 Mem-element emulators

Mem-element emulators have gained importance for a decade. The first commercial memristor was developed by Knowm in 2015 but it was quite expensive for commercial use as it operates in a very severe environment and it is difficult to follow its datasheets [28]. The meminductors and memcapacitors have physically developed but are not commercially

available and the researchers are exploring various ways to develop these mem-elements. Knowing the need to simplify mem-elements-based circuit design, researchers began developing mem-element emulators. These hardware circuits emulate the behavior of mem-elements, enabling engineers to test the performance of circuits. As mem-elements-based technologies continue to evolve and expand their applications, mem-element emulators will play an increasingly crucial role. These emulator circuits will become essential tools for scientists, engineers, and students involved in the field that leverage the unique properties of mem-elements, driving the development of innovative electronic systems and devices.

1.3 History of mem-elements

Over the years, the three general components of electronic circuits such as inductors, capacitors, and resistors were ruling to form any electrical circuit. Ewald Georg von Kleist first discovered the capacitor in 1745, while Georg Simon Ohm made his discovery of the resistor in 1827, and lastly, the inductor was discovered by Michael Faraday in 1831. These three components remained the fundamental circuit elements until 1971, when Prof. Leon Chua acknowledged the fourth circuit element [2]. The theory of Prof. Chua represents that the key circuit variables in electronics are current (i), voltage (v), charge (q), and magnetic flux (ϕ). Each component forms a relationship between these variables. Previously, only five relationships had been identified. The behavior of the three essential circuit elements resistors, capacitors, and inductors are defined by linear relationships between key electrical variables. Resistance arises from the association between voltage (v) and current (i), capacitance connects voltage (v) with charge (q), and inductance links current (i) with magnetic flux (ϕ). However, the potential connection between flux (ϕ) and electric charge (q) remain unexplored. Therefore, the idea of symmetricity from Aristotle's theory of matter [1] was taken by Prof. Chua to establish a connection between charge (q) and magnetic flux (ϕ). The Chua designated this theoretical non-linear element as the memristor which is the conjunction of memory and resistor. The hysteresis loop which is the fingerprint of the memristor represents the property of memory and the resistor indicates the dissipation feature. The resistance of a memristor is affected by the past voltage applied to it. It means the resistance increases and decreases as per the current flow in one direction and opposite direction respectively. If the current flow halts, the memristor retains the value of resistance which has been previously stored. It means, it remembers the last flowed current in the device in terms of resistance. That's why it is called a memory resistor or memristor.

In 1976, Prof. Leon Chua and S.M. Kang extensively explored system and devices of memristor [29]. The titanium dioxide-based memristor possesses a pinched hysteresis loop (PHL) in the voltage-current plane under bipolar input sources. Thereafter, memristors became popular worldwide in academia and industry. The memristor plays an important role in various application fields, such as adaptive learning circuits, neural networks, digital arithmetic circuits, analog programmable circuits, logic gates arrays, crossbar latch memories, chaotic circuits, adaptive filters, and non-volatile memories.

After the successful implementation of the memristor, M. D. Ventra, Y.V. Pershin, and Leon Chua detected remembrance property in memcapacitors and meminductors whose behavior was the same as the memristor. They linked Chua's theory by extending ideas for the inductor and capacitor to explore the other memory elements namely memcapacitor and meminductor as shown in Fig. 1.1 [30]. Memristors, meminductors, and memcapacitors establish relationships between the time integrals of fundamental electrical quantities. Specifically, memristors link voltage (represented by flux linkage, ϕ) and current (charge, q), meminductors connect magnetic flux (ρ) and charge (q), and memcapacitors relate charge (ρ) and magnetic flux (ϕ). The mem-element can remember its properties after powering off. The discovery of new elements approaches various applications.

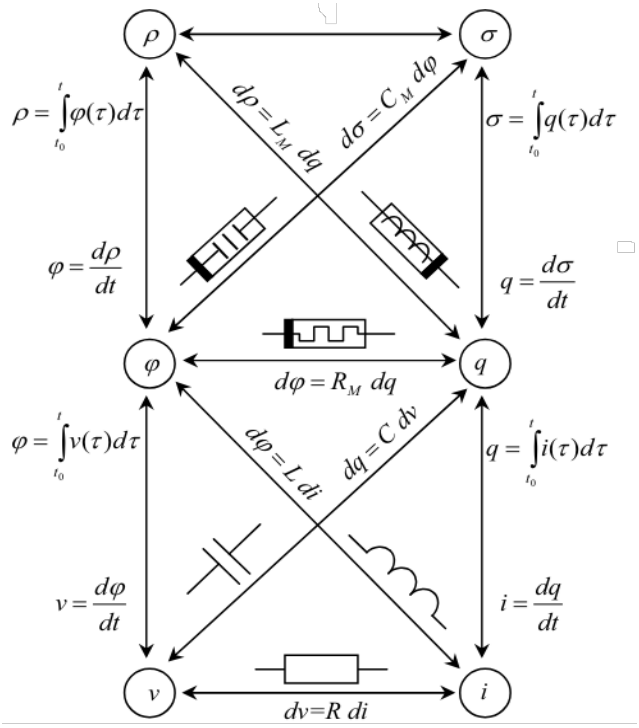

Fig.1.1 Relationships between circuit components and mem-elements [30].

Prior to 2009, memory devices primarily focused on memristive systems. However, the concept was broadened to encompass memcapacitive and meminductive systems, leading to the collective term mem-elements for these memory devices, which have since found diverse applications.

1.4 Characteristics of mem-elements

In this section, characteristics of mem-elements are discussed in detail following their mathematical relations. A memristor is a two-terminal device that alters its resistance based on the current that passes through it. The memristor retains information about the total charge that has flowed before. It can retain the state where the charge has stopped flowing even when the power is disabled. Being a passive device, the memristor has a memory capability that distinguishes it from other passive components. The memristor symbol is depicted in Fig. 1.2. Its behavior is described by the constitutive relationship $f_M(\phi, q) = 0$ which represents a curve or its attributes in the ϕ-q plane. If f_M is linear, the memristor shows linearity, represented by a straight line through the origin, with the expression $\phi = M(q)$, wherever M is constant termed as memristance. The reciprocal of memristance i.e. $W = M^{-1}$ is represented by memductance. After differentiating the relation $f_M(\phi, q) = 0$, it gives the links between voltage (v) and current (i).

In a memristive system, memristance (M_R) demonstrates a nonlinear relationship between the time integrals of current (q) and voltage (v) as shown in Equations (1.1) and (1.2).

$$\phi(t) = \int_{-\infty}^{t} v(t)\, dt. \tag{1.1}$$

$$q(t) = \int_{-\infty}^{t} I(t)\, dt. \tag{1.2}$$

The memristive system can be defined by the Equation:

$$d\phi = M_R dq \tag{1.3}$$

where M_R represents the memristance of the system.

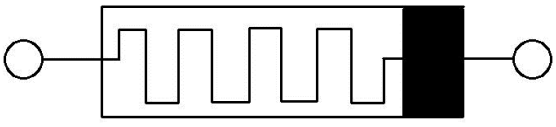

Fig. 1.2 Symbol of memristor.

We can also define Equation (1.3) in the form given in Equation (1.4) by differentiating Equation. (1.3) w.r.t. time

$$v(t) = M_R(q)i(t) \tag{1.4}$$

Memristive systems, characterized by a PHL between voltage v(t), and current i(t) exhibit distinct behaviors based on the flux-charge relationship. A charge-dependent relationship defines a charge-controlled memristor, while a flux-dependent relationship signifies a flux-controlled based memristor.

In the case of a charge-controlled based memristor, the flux is given by:

$$\phi = f(q) \tag{1.5}$$

Differentiating Equation (1.5) w.r.t time yields:

$$\frac{d\phi}{dt} = \frac{df(q)}{dq}\frac{dq}{dt} \tag{1.6}$$

Substituting voltage as $v(t) = \frac{d\phi}{dt}$ and current as $i(t) = \frac{dq}{dt}$, Equation (1.6) can be rewritten as:

$$v(t) = M(q)i(t) \tag{1.7}$$

Similarly, in the case of a flux-controlled based memristor, the charge can be defined as:

$$q = f(\phi) \tag{1.8}$$

Differentiating Equation (1.8) yields

$$\frac{dq}{dt} = \frac{df(\phi)}{d\phi}\frac{d\phi}{dt} \tag{1.9}$$

Substituting current as $i(t) = \frac{dq}{dt}$ and voltage $v(t) = \frac{d\phi}{dt}$ in Equation (1.9) which results in

$$i(t) = W(q)v(t) \tag{1.10}$$

A meminductor is a passive two-terminal component that can be considered as a combination of a memory and an inductor with the specialty of both inductance and memory. It stores the past state and retains it even when the power is off. The symbol of a meminductor is shown in Fig. 1.3. It is defined by the constitutive relation $f_{ML}(\rho, q) = 0$ which represents a curve or its attributes in the ρ-q plane.

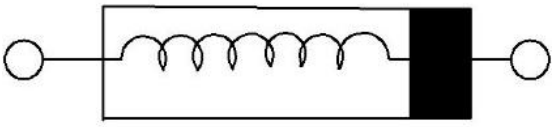

Fig. 1.3 Symbol of meminductor.

Meminductance (M_L) characterizes a meminductive system that establishes a nonlinear relationship between the integral of current over time (q) and the integral of flux over time (ρ), as illustrated in Equations (1.11) and (1.12)

$$\rho(t) = \int_{-\infty}^{t} \phi(t)\, dt \tag{1.11}$$

$$q(t) = \int_{-\infty}^{t} i(t)\, dt \tag{1.12}$$

The meminductive system can also be described as

$$d\rho = M_L dq \tag{1.13}$$

where M_L he meminductance of the system.

The Equation (1.13) can be expressed as given in Equation (1.14) by differentiating it w.r.t time

$$\phi(t) = M_L i(t) \tag{1.14}$$

$$i(t) = M_L^{-1} \phi(t) \tag{1.15}$$

In these Equations, ϕ(t) and i(t) denote the flux and current in the meminductive system, respectively. The meminductive system exhibits pinched hysteresis behavior between ϕ(t) and i(t).

The meminductor is current-controlled if the input is dependent on current and is called flux-controlled if the input is dependent on flux as mentioned in Equations (1.16) and (1.17).

$$\phi(t) = M_L \left[\int_{t_0}^{t} I(\tau) d\tau \right] . I(t) \tag{1.16}$$

$$I(t) = M_L^{-1} \left[\int_{t_0}^{t} \phi(\tau) d\tau \right] . \phi(t) \tag{1.17}$$

where the initial time t_0 is chosen to ensure that $\int_{-\infty}^{t_0} i\,(\tau)d\tau = 0$ and $\int_{-\infty}^{t_0} \phi(\tau)d\tau = 0$. Therefore, the meminductance of meminductors varies depending on whether they are current-controlled or flux-controlled.

A memcapacitor is a two-terminal passive component with special features such as storing and retaining. It is considered as a combination of memory and capacitor. It stores the electrical state and retains the past state similar to memristors and meminductors. The symbol of a mmemcapacitor is shown in Fig. 1.4. It is defined by the constitutive relation f_{MC} (σ, ϕ) = 0, which represents a curve or its attributes in the σ-ϕ plane. Memcapacitance (M_C) is defined as a property of a memcapacitive system, which establishes a nonlinear relationship between the time integral of charge (σ) and the time integral of voltage (ϕ), as indicated by Equations (1.18) and (1.19):

$$\sigma(\mathrm{t}) = \int_{-\infty}^{\mathrm{t}} \mathrm{q}(\mathrm{t})\,\mathrm{dt} \tag{1.18}$$

$$\phi(\mathrm{t}) = \int_{-\infty}^{\mathrm{t}} \mathrm{v}(\mathrm{t})\,\mathrm{dt} \tag{1.19}$$

A memcapacitive system can also be expressed as

$$\mathrm{d}\sigma = M_C \mathrm{d}\phi \tag{1.20}$$

where, $\mathrm{M_C}$ represents the memcapacitance of the system.

Equation (1.20) can be rewritten as Equation (1.21) by differentiating it w.r.t time

$$q(\mathrm{t}) = M_C \mathrm{v}(\mathrm{t}) \tag{1.21}$$

$$V(\mathrm{t}) = M_C^{-1} \mathrm{q}(\mathrm{t}) \tag{1.22}$$

In these Equations, q(t) and v(t) denote the charge and voltage in the memcapacitive system, respectively. The system's pinched hysteresis behavior is observed between q(t) and v(t).

Fig 1.4 Symbol of memcapacitor.

The memcapacitor is voltage-controlled if the input is dependent on voltage v (t) and is called charge-controlled if the input is dependent on charge q(t) as mentioned in Equations (1.23) and (1.24).

$$q(t) = M_C \left[\int_{t_0}^{t} V(\tau) d\tau \right] . \mathrm{V}(t) \tag{1.23}$$

$$V(t) = M_C^{-1} \left[\int_{t_0}^{t} q(\tau) d\tau \right] . \mathrm{q}(t) \tag{1.24}$$

The initial time t_0 , is selected such that $\int_{-\infty}^{t_0} V(\tau) d\tau = 0$ and $\int_{-\infty}^{t_0} q(\tau) d\tau = 0$. Thus, the memcapacitance of a memcapacitor depends on either the charge or the voltage, depending on whether the device is voltage-controlled or charge-controlled.

1.5 Structure of thesis

The thesis is organized into six chapters. The outline of the thesis is are as follows:

Chapter 1 introduces the basics of mem-elements, their importance, history, and potential applications.

Chapter 2 presents the literature survey of mem-element emulators based on multiplier and multiplier-less realizations.

Chapter 3 explores the development of memristor emulator designs employing analog building blocks. These designs leverage operational transconductance amplifiers, current differencing buffered amplifiers, voltage differencing gain amplifiers, and fully-balanced voltage differencing buffered amplifiers. The chapter details the core design principles and presents a comprehensive mathematical analysis of each proposed memristor emulators (MREs) configuration.

The proposed meminductor emulators (MIEs) using operational transconductance amplifiers (OTA), current differencing buffered amplifier (CDBA), voltage differencing gain amplifier (VDGA), and voltage differencing transconductance amplifier (VDTA) have been presented in Chapter 4. The working principles of these emulators, their mathematical equation, and the core ideas behind these circuits are discussed in detail.

In Chapter 5, simulation results of proposed MREs and MIEs have been included and

discussed in detail. The design parameters, values of different components, and all details of the circuits have been given to obtain the simulation results. Monte Carlo analyses of the emulator circuits have been conducted to assess the robustness of the proposed designs. Comparative analyses of the proposed mem-elements emulator against existing mem-elements emulator designs have also been performed.

Chapter 6 provides the concluding remarks and outlines the future scope of the work.

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CHAPTER 2

LITERATURE SURVEY

This chapter offers a comprehensive literature review on emulators designed for mem-elements such as memristors, meminductors, and memcapacitors. The reported emulators are categorized into two groups: emulators with analog multipliers (AM) and emulators without analog multipliers. Before discussing the designs of memristor emulators (MREs) without multipliers, a review of MREs that incorporate them is presented. The same approach is followed for meminductor emulators (MIEs) and memcapacitors (MCEs).

2.1 Realization of memristor emulators using multipliers

The first MRE was reported using off-the-shelf components by Hyongsuk Kim *et al.* [31] in which the behavior of a TiO_2 based memristor has been replicated using three operational amplifiers (op-amps), an analog multiplier (AM), seven resistors, and one capacitor. Memristor fingerprints are confirmed for a single memristor, its hybrid, series, and parallel connections. Both simulations and experimental results have confirmed the effectiveness of the proposed emulator.

Later, a floating memristor emulator (F-MRE) utilizing four second-generation current conveyors (CCII+s), an AM, five resistors, and a capacitor was reported by C. Sanchez-Lopez *et al.* [32]. Up to 20 kHz frequency, the pinched hysteresis loops (PHLs) have been preserved. The presentation of both the simulation and experimental results validated the memristor's behavior.

The expanded concept of the work is done in [32] with a thorough mathematical derivation by the same group, C. Sanchez-Lopez *et al.* [33]. The F-MRE used four CCII+s, an AM, five resistors, and a variable capacitor. The PHL was sustained up to 20.2 kHz frequency.

Subsequently, Abdullah Yeşil *et al.* [34] used one differential difference current conveyor (DDCC), an AM, a capacitor and two resistors to realize decremental and incremental MREs. It has been confirmed that the behavior of a single memristor, its series and parallel topologies, in conjunction with other passive components is consistent. The PHLs were obtained for the frequency range of of 100 kHz to 1 MHz.

Dongsheng Yu *et al.* [35] introduced the first universal mutator circuit designed for

transformations between memristors, meminductors, and memcapacitors. Along with a few passive components, three AD844 operational amplifiers were employed to construct the mutator circuit. Memristors were further transformed into meminductors and memcapacitors using the mutator circuit. The transient and PHLs were generated by applying a frequency range of 15 Hz to 60 Hz. The four AD844s, one op-amp, one multiplier, one capacitor, and numerous resistors are all used to realize the MRE.

Changju Yang *et al.* [36] presented an incremental MRE in which six op-amps, a current conveyor, a multiplier, a diode, eight MOS transistors, eleven resistors, and a capacitor were utilized. A current conveyor and a few resistors transfer the same input current to the output port of the reported MRE, ensuring its connectivity with other devices. To confirm the emulator performance satisfactorily, transient response, and PHLs were obtained for the frequency range of 5 Hz to 1 kHz.

Next, Abdullah G. Alharbi *et al.* [37] reported the exponential model of decremental memristor to realize a current-controlled MRE. The MRE circuit was realized using two CCs, a wave-shaping function circuit, a multiplier, two transistors, a capacitor, and four resistors. The fingerprints of the memristor were verified up to 3 kHz frequency.

Subsequently, Montree Kumngern and Phichet Moungnoul realized an MRE circuit in both decremental and incremental configurations using electronically tunable DDCC, six OTAs, a multiplier, two resistors, and a capacitor. The PHL was not deformed up to 1.5 kHz [38].

C. Sánchez-López *et al.* [39] reported a decremental and incremental MRE in which used two dual-output CCII+, a resistor, a multiplier and a capacitor was used. The PHLs were obtained for the frequency range of 16 Hz to 160 kHz.

Montree Kumngern used two OTAs, a multiplier, four resistors, and a capacitor to realize a floating decremental MRE [40]. The PHL remains unaltered up to 5 kHz.

Manu Chilukuri and Sungyong Jung reported a decremental MRE using an integrator, a summing amplifier, a multiplier, five resistors, and a capacitor [41]. The PHLs were achieved for frequencies between 8 kHz to 16 kHz.

Liu Wei *et al.* [42] designed a decremental F-MRE for the decremental configuration only. It utilizes a multiplier, an integrator, an adder-subtraction circuit, an exponential circuit, twenty-one resistors, and two capacitors. The PHLs are sustained up to 50 Hz.

The incremental and decremental MRE were realized by Yongjin Kim *et al.* [43]. The design

included six op-amps, a multiplier, a diode, twelve MOSFETs, seven resistors, and a capacitor. The PHLs were obtained for the frequency range of 100 Hz to 200 Hz.

A decremental MRE was presented by Hyuncheol Choi and Hyongsuk Kim, utilizing seven op-amps, a multiplier, ten MOS transistors, nine resistors, a variable resistor, a diode, a switch, and a capacitor [44]. The PHLs were obtained for the frequency range of 5 Hz to 250 Hz.

Zehra Gulru Cam and Herman Sedef realized the decremental and incremental MREs [45] with the help of four current conveyors (CCs), an AM, three resistors, and a capacitor. The PHLs were achieved for frequencies between 1 Hz to 40 kHz.

The decremental and incremental MREs was reported utilizing a MO-OTA, a resistor, a capacitor and a multiplier by Yunus Babacan *et al.* [46]. The PHLs were obtained for the frequency range of 100 Hz to 1 kHz.

C. Sánchez-López and L.E. Aguila-Cuapio demonstrated the decremental and incremental G-MRE [47] utilizing a CCII+, a resistor, a capacitor, and a multiplier. The frequency range of MRE is found to be from 16 Hz to 860 kHz.

The grounded decremental and incremental MREs were achieved by Umut Engin Ayten *et al.* [48] with the aid of a multiplier, two resistors, a capacitor, and a current backward transconductance amplifier (CBTA). The PHL was not deformed up to 100 kHz.

Somia H. Rashad *et al.* [49] realized a fractional order MRE using two CCII+, a multiplier, three resistors, and a fractional order capacitor. The PHLs were acquired for the frequency range of 1 kHz to 10 kHz.

Zhijun Li *et al.* [50] reported the floating decremental and incremental MRE using two CFOA, two AMs, two capacitors, and three resistors. The frequency range of MRE is found to be from 1 kHz to 10 kHz.

The inductive coupling of two configurations of MRE that employs three CCIIs+, a multiplier, a summer, five resistors, two capacitors, and an inductor was reported by Dongsheng Yu *et al.* [51]. The memristor is operating in the frequency range of 60 kHz to 150 kHz.

Zhi Zhou *et al.* [52] reported a decremental MRE using three op-amps, four current feedback op-amps, an analog multiplier, thirteen resistors, and two capacitors.

C. Sánchez-López *et al.* [53] reported a flux-controlled fractional-order memristor emulators using four CCII+s, a multiplier, four resistors, and two capacitors. In contrast, a charge-controlled fractional-order memristor was realized using two CCII+s, two capacitors, three resistors, and a multiplier.

Predrag B. Petrovic [54] developed a flux-controlled floating memristor emulator (F-MRE) that includes thirty-two MOS transistors, two resistors, a capacitor, a multiplier, and a voltage differencing transconductance amplifier (VDTA). The PHLs were maintained for frequencies up to 2 MHz. The frequency to amplitude demodulator using the proposed MRE was also suggested.

Another MRE was reported by Fadhil Rahma Tahir and Saif Muneam Ramadhan using field programmable analog arrays (FPAA), such as adder, sample and hold circuit, integrator, and multiplier [55]. The PHLs were not deformed for the frequency range of 1 kHz to 20 kHz.

Bo Dang *et al.* [56] reported a decremental MRE using two op-amps, an AM, a capacitor and six resistors. The PHL remained unaltered up to 3 kHz.

Ahmed M. Hassanein *et al.* [57] realized MRE using three CCII+s, a multiplier, three resistors, and a capacitor. The memristor is said to function acceptably in the frequency range of 500 Hz to 200 kHz.

Yan Liang *et al.* [58] presented F-MRE using off-the-shelf components such as two op-amps, a multiplier, two CCII+s, sixteen resistors, two diodes, and a capacitor. The PHL has been obtained for the frequency range of 5 kHz to 60 kHz.

Qing Zhao *et al.* [59] designed G-MREs and F-MREs, realized using an AM, three resistors, a capacitor, and three CCII+s. The proposed MREs were able to attain the frequency range of 500 Hz to 5 kHz.

Xudong Xie *et al.* [60] presented a holistic logarithmic MRE circuit using five op-amps, two multipliers, a capacitor and ten resistors. The frequency range for which the PHLs are acquired is 5 Hz to 100 Hz.

An OTA based MRE circuit was realized by Aphichata Thongrak *et al.* [61]. The circuit employs an ECCII, two OTAs, a multiplier, a capacitor and two resistors. The PHLs are plotted for frequencies up to 1.5 kHz.

Aphichata Thongrak *et al.* [62] presented an electronically tunable differential difference

current conveyor (EDDCC) based MRE. One EDDCC block, two resistors, a capacitor, and a multiplier were utilized to configure the MRE. The PHL was not deformed up to 1.5 kHz.

Nariman A. Khalil *et al.* [63] reported a fractional order mem-element emulator using two CCII+s, a multiplier, an adder, a multiplier/divider block, five resistors, and two switches. The frequency range for which the PHLs are acquired is 1 kHz to 2 kHz.

Vipin Kumar Sharma *et al.* [64] reported a decremental MRE using two CFOAs, a multiplier, two PMOS transistors, three resistors, and a capacitor. The frequency range for which the PHLs are acquired is 100 Hz to 1 kHz.

A decremental MRE was realized using three multipliers, four resistors, a capacitor, and six OTAs by Melih Yildirim and Firat Kacar [65]. The MRE was reported to have operated effectively within the frequency range of 400 Hz to 1200 Hz.

Indrajit Pal *et al.* [66] developed the MRE using two VDTAs, a four-quadrant multiplier, a capacitor and two resistors. The MRE was reported to have operated effectively within the frequency range of 800 Hz to 1 kHz.

Nilay Aishwarya *et al.* [67] reported a carbon nanotube field effect transistor (CNFET) based MRE. The CNFET was created using a VDTA and a four-quadrant multiplier. The MRE circuit was implemented using two VDTAs, two resistors, a four-quadrant multiplier, and a capacitor. The PHL of proposed MRE was not deformed up to 500 kHz.

Haneen G. Hezayyin *et al.* [68] developed an inverse MRE using two CCII+s, a multiplier, a capacitor and three resistors. The PHL of proposed MRE was not deformed up to 500 kHz.

2.2 Realization of multiplier-less memristor emulators

Y. V. Pershin and M. Di Ventra [30] reported the MRE employing a microcontroller, an analog-to-digital converter, and a potentiometer.

V. Biolková *et al.* [69] introduced a mutator-based MRE utilizing an operational trans-impedance amplifier. The PHLs are plotted for frequencies up to 100 Hz only.

I. Hussein and M. E. Fouda [70] presented a current-controlled MRE employing a CCII+ and a voltage-controlled resistor. The PHL is plotted for the frequency range of 100 kHz to 1 MHz.

Zhang Xuliang *et al.* [71] reported MRE using two varactor diodes, two inductors, and a

resistor. The operating frequency range of proposed MRE is 1 kHz.

SangHak Shin *et al.* [72] designed MRE utilizing transmission gates (TG), comparators, voltage control resistors (VCR), diodes, capacitors, and current mirrors. The memristor was reported to have operated effectively within the frequency range of 10 kHz to 40 kHz.

Jun-Myung Choi *et al.* [73] realized another MRE circuit using TG, CMOS transistors, comparators, diodes, and resistors with the functionality verified through a programmable gain amplifier. The PHL is not deformed up to 50 Hz frequency.

M. T. Abuelma'atti and Z. J. Khalifa presented the circuit of MRE in both incremental and decremental arrangements using three CFOAs, four resistors, two capacitors, and a diode, with functionality verified through ASK, FSK, and BPSK circuits The PHLs were plotted for frequency up to 500 Hz [74].

Dongsheng Yu *et al.* [75] reported a flux-controlled MRE utilizing four CCs, a multiplier, ten resistors, a capacitor, and an inverting adder circuit (IAC). Further, they employed the MRE in the relaxation oscillator design. The proposed MRE achieves satisfactory performance throughout the frequency range of 17 Hz to 120 Hz.

M.T Abuelma'atti and Z. J. Khalifa [76] reported a continuous-level MRE utilizing a CFOA, an OTA, two capacitors and three resistors The suggested design of the MRE is used in the multivibrator circuit to demonstrate its workability. The PHL has been obtained up to 600 Hz frequency.

Abdullah G. Alharbi *et al.* [77] realized the circuit of MRE utilizing a CCII+, two op-amps, two transistors configured as diodes, two resistors, and a capacitor. The PHL is not deformed up to 20 kHz frequency.

Hasan Sözen and Uğur Çam reported the MRE circuit using four CCII+s, three OTAs, six resistors, and a capacitor. The proposed MRE circuit achieves satisfactory performance throughout the frequency range of 10 Hz to 5 kHz [78].

Dalibor Biolek *et al.* [79] realized a memristive system using a MOSFET transistor, a capacitor and two resistors. It was observed that the MRE circuit performed well in the frequency band of 10 Hz to 10 kHz.

Hasan Sözen and Uğur Çam [80] designed the MRE circuit using four CCII+s, three OTAs, a capacitor and six resistors. The measured PHLs of the reported MRE span for a frequency

range of 100 Hz to 10 kHz.

Another MRE was realized using four CFOAs, five resistors, four capacitors, and two diodes by M. Taher Abuelma'atti and Z. Jamal Khalifa [81]. The proposed MREs were utilized in frequency to amplitude modulation converter. The PHL of reported MRE was not deformed up to 2.9 kHz to 6 kHz.

Abdullah G. Alharbi *et al.* [82] realized the MRE circuit using two CCIIs+, a voltage amplifier, three resistors, and a capacitor. The PHLs have been obtained for 200 Hz to 5 kHz frequency range.

A field programmable gate array-based MRE using a serial-to-parallel converter, parallel-to-serial converter, 10-bit ADC, and resistor arrays has been realized by Rajeev Ranjan *et al.* [83]. It has been reported that the MRE functions effectively within the frequency range of 20 Hz to 400 Hz.

John Kalomiros *et al.* [84] reported the MRE circuit using two NPN transistors, three resistors, two diodes, and two capacitors. The measured PHLs of the reported MRE span over a frequency range of 100 Hz to 500 kHz.

Yunus Babacan and Fırat Kacar reported the floating decremental and incremental MREs working in the subthreshold region using an OTA, two MOS transistors, and a capacitor [85]. The proposed MRE achieves satisfactory performance throughout the frequency range of 10 Hz to 30 Hz.

Yunus Babacan and Fırat Kaçar reported a decremental/incremental MRE using leaky integrators, a capacitor and four MOS transistors[86].

A DVCCTA, a capacitor and three resistors were used by Rajeev Kumar Ranjan *et al*. [87] to realise the incremental and decremental configurations of the MRE. A high pass filter is realized using the reported MRE. The MRE was reported to have operated effectively within the frequency range of 500 kHz to 1 MHz.

Another decremental/incremental MRE using a current conveyor transconductance amplifier (CCTA), three resistors, and a capacitor has been realized by Rajeev Kumar Ranjan *et al.* [88]. The PHL was not deformed up to 100 kHz frequency.

Olufemi Akindele Olumodeji and Massimo Gottardia *et al.* realized the MRE model using a digital potentiometer and Arduino microcontroller. The standard mathematical Equations of

the HP model were used to program the Arduino board, and the value of the digital potentiometer was set through serial peripheral interface ports [89]. The PHL was obtained for the frequency range of 200 Hz to 500 Hz.

Yunus Babacan and Firat Kacar reported a floating current source-based decremental/incremental MRE that consumed very little power [90]. The circuit is simpler as no multiplier has been used to achieve the non-linear behavior of the memristor. It uses dynamic threshold MOS-based floating current sources, two transistors, and a capacitor in the design of emulator. The PHLs were plotted for the frequency range of 1Hz to 10 Hz.

A very simple grounded MRE was presented by Yunus Babacan *et al.* using an OTA, two MOS transistors, a multiplier and two capacitors [91]. The PHLs were plotted for the frequency range of 1 kHz to 12 kHz.

Abdullah Yesil reported another grounded MRE in which a capacitor and seven MOS transistors have been employed. The fingerprints of the MRE have been obtained by both simulation and experimental setups [92]. The PHL was not deformed up to 50 MHz frequency.

Another MRE was presented by Vishal Saxena using an OTA and a grounded capacitor. The OTA uses four MOS transistors, while one MOS is used for a switch, and another MOS is used to design a grounded capacitor [93]. The MRE is found to be working satisfactorily up to 1 MHz frequency.

A floating incremental/decremental MRE was reported by Predrag B. Petrovic using a VDTA, two resistors, a multiplier, and a capacitor. The frequency to amplitude demodulator is also reported to verify the proposed MRE. Simulation and experimental setups have been given for the reported MRE [94]. The PHLs were plotted for the frequency range upto 1MHz.

Rajeev Kumar Ranjan *et al.* presented an op-amp-based MRE using four MO-OTAs, a capacitor and three resistors [95]. In order to confirm the effectiveness of the suggested MRE, incremental and decremental realisations of the memristor-capacitor filter have been built. The center frequency of the filter is varied using a memristor-capacitor filter. The PHL of reported MRE was not deformed up to 150 kHz.

Yunus Babacan *et al.* presented a Zinc oxide (ZnO) based MRE using five MOS transistors. The PHLs are obtained by simulation and experimental setup [96]. The PHL was not deformed up to 100 MHz frequency.

Dong-Sheng Yu *et al.* realized a MRE using three CFOA, an op-amp, five resistors, a capacitor, and a varactor diode [97]. The PHL was not deformed up to 9 kHz.

Incremental/decremental G-MREs and F-MREs were reported by Gaurav Kanyal *et al.* using two OTAs and a capacitor [98]. The amplitude modulator and demodulator circuits are also designed to show the workability of the reported MRE. The PHL was obtained for the frequency range of 400 kHz.

A MRE using digital components was reported by Oscar Camps *et al.* [99]. The MRE is realized using a field-programmable gate array by Altera that results in less than 100 gates. Therefore, the possibility of discovering more than 50k memristors has been emphasized using modern field programmable gate array boards. The PHL of reported MRE was not deformed up to 5 Hz.

Fatih Gul and Yunus Babacan reported a ZnO-based floating MRE using an OTA, two capacitors and three transistors [100]. The frequency range of reported MRE is found to be 8 Hz to 24 Hz.

A floating MRE is presented using a multiple-output OTA and a grounded capacitor by Abdullah Yesil [101]. The PHLs have been plotted for series and parallel connections of memristors. The PHL of reported MRE was not deformed up to 50 Hz.

Abdullah Yesil *et al.* [102] reported a floating MRE using a current backward transconductance amplifier (CBTA) and two capacitors. The workability of reported MREs is verified by realizing single, series, and parallel combinations of MREs. The PHL of reported MRE was not deformed up to 1 MHz.

The VDTA based MRE was reported by Abdullah Yesil *et al.* [103]. One MOS capacitor is used to retain the state of the memristor. The simulation and experimental setup were used to obtain the non-volatility test and PHLs. The PHL was obtained for the frequency range of 15 MHz to 50 MHz.

Another MRE was realized using a voltage differencing current conveyor (VDCC), resistor, and a capacitor by Abdullah Yesil *et al.* [104] for which hardware implementation is also suggested. The PHL of MRE was not deformed for frequency lying in between 500 kHz to 2 MHz.

John Vista and Ashish Ranjan reported a MOS transistor-based MRE [105]. Three MOS transistors and a capacitor are used in the design. Further, the reported MRE has been used

in the design of Schmitt trigger, amplitude modulator, frequency demodulator, and associative learning circuits. The PHL was obtained for the frequency range of 100 kHz to 1 MHz.

A bipolar junction transistor-based inverse MRE was reported by Nariman A. Khalil *et al.* [106]. Two BJTs, a resistor, and a capacitor are used in the design. A chaotic oscillator is also realized using a reported inverse MRE. The MRE was reported to operate effectively within frequency range of 10 Hz to 200 Hz.

Niranjan Raj *et al.* introduced the MRE circuit in which a CCII+, an OTA, a capacitor, and a resistor have been utilized [107]. This emulator was employed to create a chaotic oscillator and a high-pass filter. The MRE was reported to operate effectively within frequency range of 16 MHz to 25 MHz.

Pushkar Srivastava *et al.* reported the MRE circuit based on MOS transistors [108]. The floating memristor emulator (F-MRE) is realized using three MOS transistors while the grounded memristor emulator (G-MRE) is realized using two MOS transistors. Two additional buffers have been used in the experimental setups of reported MREs. The PHLs of reported MRE were achieved for frequencies lying in between 500 kHz and 30 MHz.

Abdullah Yesil *et al.* designed the circuit of F-MRE based on dual-output OTA, a DVCC, an electronic resistor realized by two MOSFETs, and a capacitor [109]. Simulations and experimental results have been shown for the reported MRE. The PHLs of reported MRE were achieved for frequencies lying in between 500 kHz and 1.5 MHz.

The F-MRE and G-MRE were reported by S. Gupta *et al.* using an OTA and a current differencing transconductance amplifier (CDTA) [110]. The memristor-based Tow-Thomas biquad has also been reported. The PHLs were obtained up to 1 MHz frequency.

Hacer Atar Yildiz and Serdar Ozoguz realized the MRE circuit using three MOS transistors without any external capacitor [111]. Despite the external capacitor, the transistor's internal capacitance has been utilized in the design. The overall size of emulator circuit is decreased while its frequency range of operation is increased. The emulator circuit has been modified further to make it locally active to design a chaotic oscillator. The reported MRE demonstrates effective performance up to 4 MHz frequency.

Sagar Surendra Prasad *et al.* realized the MRE circuit utilizing a current follower transconductance amplifier (CFTA) and a capacitor. The experimental results of the

reported emulator and chaotic oscillator are realized using the suggested MRE [112]. The PHL was not deformed up to 5 MHz frequency.

Vipin Kumar Sharma *et al.* reported the four-quadrant analog multiplier-based MRE [113]. Two NMOS transistors, an inverting buffer, and a capacitor are used in addition to the CDTA based analog multiplier. Schmitt trigger and high pass filters are also implemented using the reported MRE. The emulator circuit is also modified to realize a capacitor-less MRE. The PHL of proposed MRE was obtained up to 1 MHz frequency.

The CMOS transistor-based MRE circuit was realized by Naheem Olakunle Adesina *et al.* using only four MOS transistors [114]. The reported MRE demonstrates effective performance at 1 kHz frequency.

Another MRE was reported by Hacer Atar Yildiz using a single active element and intrinsic capacitance of MOSFET [115]. Two circuits of MREs are realized, one of which is a CFOA based MRE, while another is based on an OTA. The reported MRE operates effectively up to 60 MHz frequency.

The VDTA-based MRE is reported by Kapil Bhardwaj and Mayank Srivastava [116]. The MRE is implemented by means of a resistor, two VDTAs and a capacitor. The proposed configuration of the MRE is used in an associative learning circuit. The reported MRE demonstrates effective performance at 1.5 MHz frequency.

The three cross-over points in PHLs of the MRE circuit have been obtained by Kapil Bhardwaj and Mayank Srivastava [117]. The emulator circuit consists of five OTAs, three resistors, and a grounded capacitor. The performance of reported MRE is found to be satisfactorily at 2 MHz frequency.

Another MRE was reported by Kapil Bhardwaj and Mayank Srivastava [118] using an OTA, a VDCC, two resistors, and a capacitor. The same analog building blocks are also utilized to realize MCE and MIE configurations. The PHLs were obtained up to 1 MHz frequency for the proposed MRE.

A triple-crossing MRE circuit that can find specific applications in multilevel memory and chaotic generators is realized using two VDTAs, two resistors, and a grounded capacitor by Kapil Bhardwaj and Mayank Srivastava [119]. The PHL was not deformed up to 300 kHz for the reported MRE.

Anamika Raj *et al.* [120] reported a grounded memristor emulator (G-MRE) using an OTA,

a DVCC, a resistor, and a capacitor. The PHL was obtained up to 1 MHz frequency.

Another MRE was designed using a PMOS transistor, a CCII+ and a resistor by Prashant Kumar *et al.* [121]. The reported MRE is utilized in read-write operations to demonstrate its practical feasibility. The PHLs of reported MRE are obtained for frequency up to 40 kHz.

Pankaj Kumar Sharma *et al.* designed the MRE using a DVCC, an OTA, a resistor, and a capacitor. The experimental set-up of a MRE with application in a high pass filter, Chaotic oscillator, and neuromorphic circuit was reported [122]. It has been claimed that the performance of reported MRE is satisfactory up to 30 MHz.

Lei Zhou *et al.* reported the MOS-only MRE using two MOSFETs only. No external capacitor or power supply is required in the design [123]. Four logic circuits have also been implemented using the reported MRE. The PHL of reported MRE was obtained up to 300 MHz frequency.

Another MRE was reported by Yesil *et al*. that uses four MOS transistors to control fixed and variable parts electronically. Incremental and decremental MREs have been realized [116]. The PHLs were obtained up to 1 MHz frequency.

The two transistors-based F-MRE was reported by Navnit Kumar *et al.* [125]. The circuit consists of a current source and two transistors. The conventional passive capacitor is replaced by the intrinsic parasitic capacitance of MOSFET. The functionality of the circuit has been verified through the Wien Bridge oscillator and Schmitt trigger. The frequency range of 1 MHz was attained for the reported MRE.

A flux-controlled MRE using a single inverting current conveyor transconductance amplifier (ICCTA) was designed by Navnit Kumar *et al.* [126]. The incremental and decremental configurations using ICCTA, a capacitor, and a grounded resistor have been utilized in the design. PHLs are available in single, double, and triple versions. A high pass filter is designed using a decremental and incremental MRE. The frequency range of suggested MRE was found to be 4MHz.

Pankaj Kumar Sharma *et al.* reported the MRE circuit using a voltage differencing inverted buffered amplifier (VDIBA) and a CCII+ [127]. The PHLs are obtained for single and parallel combinations of memristor up to 4 MHz frequency.

A conventional and dynamic threshold MOSFET-based MRE was reported by Ananda Y. R. *et al.* [128]. Four transistors, including three MOSFETs, a DTMOS, and a capacitor are

used in the design of the MRE. A high pass filter, inverter, adaptive learning circuit, and Chua's chaotic oscillator were realized using the reported MRE. The PHL was not deformed up to 1.5 MHz frequency.

The VDIBA based MRE is designed by Sagar *et al.* using two VDIBAs and a grounded capacitor [129]. This circuit utilized two blocks of VDIBA and a capacitor. The PHLs are obtained up to 12.7 MHz frequency. The PHLs are obtained for a single and parallel configuration of the MRE.

Prosenjit Kumar Ghosh *et al.* reported a CMOS-based MRE [130]. The MRE circuit was designed using nine MOSFETs. The PHL was not deformed up to 10 MHz frequency.

A G-MRE using a DVCCTA, two resistors, and a grounded capacitor is reported by S. S. Prasad *et al.* [131]. The PHLs are obtained for a high frequency range (in MHz) for a single and parallel configuration of the MRE.

The inverse frequency characteristics of the memristor are obtained using two conventional and two dynamic threshold-based MOSFETs along with a grounded capacitor. The PHLs have been obtained up to 1 MHz frequency, and series and parallel configurations of memristors have been utilized for performance verification [132]. A chaotic oscillator is also realized by embedding a MOS-DTMOS-based emulator.

A current-controlled CDTA (CCCDTA) based MRE is reported in [133] using a CCCDTA and a capacitor. The PHLs are obtained for frequency range of 750 kHz to 1.5 MHz. The reported MRE offers electronic tunability.

Another F-MRE was realized using four n-type MOSFETs by Mourina Ghosh *et al.* [134]. One of the MOSFETs is used as a grounded capacitor. The PHLs are obtained for 50 MHz frequencies. A BFSK circuit is designed after embedding the reported MRE.

Sagar *et al.* [135] realized a G-MRE and a floating memristor emulator (F-MRE) using an OTA, a VDCC, and a capacitor. The PHLs are obtained up to 8 MHz frequency.

The OTA and VDIBA based MRE is reported by M. Ghosh *et al.* [136]. The PHL is obtained up to 5 MHz frequency. The performance of the reported MRE is verified through a BFSK modulator-demodulator circuit.

The MRE circuit has been reported recently by R. Gupta *et al*. using a MOSFET, a resistor, and a capacitor. The PHL is obtained up to 80 MHz frequency. The reported MRE is used

in the design of Schmitt trigger and chaotic oscillator [137].

Kapil Bharadwaj *et al.* reported an OTA and CCII+ based universal mem-elements emulator [138]. A capacitor and three OTAs are used to implement the MRE circuit. The MIE circuit is realized using two capacitors and four OTAs. In contrast, the MCE circuit is realized using a CCII+, two capacitors, three OTAs, and a resistor. A relaxation oscillator is designed using mem-elements emulator. The operating frequency of reported mem-element emulator is found to be 1.5 MHz.

A DVCC based MRE circuit is reported by Sadaf Tasneem *et al.* [139]. The emulator's design utilizes a DVCC, three PMOS transistors, and a grounded capacitor. The emulator's performance is verified through an adaptive learning circuit. The PHL of reported MRE was obtained up to 5 MHz frequency.

Another MRE was presented by Sagar *et al.* and is based on a CCTA. The emulator operates with a ±1 V DC supply, a capacitor and two resistors. Incremental and decremental arrangements can be achieved by placing the capacitor either at the ZC+ terminal or the ZC- terminal of the CCTA. The designed MRE has been used in applications including adaptive learning circuits and chaotic oscillators [140]. It has been claimed that the performance of reported MRE is satisfactory up to 1.75 kHz frequency.

A current-controlled CCTA (CC-CCTA) based MRE was reported in [141]. The floating configuration of reported emulator utilizes a capacitor, an OTA and a CC-CCTA. The implemented MRE has been embedded in the design of a chaotic oscillator to check the performance. The PHL was not deformed up to 100 kHz frequency.

An op-amp based MRE was realized by B. Suresha *et al.* [142]. The implementation utilizes a floating capacitor, an op-amp, a transistor and three resistors. The operating freuency was found to be 20 kHz. The implemented MRE has been used to design a Schmitt trigger.

The MRE based on ICCTA has been presented by Navnit Kumar *et al.* The flux-controlled emulator uses one ICCTA, one resistor, and one capacitor, whereas the charge-controlled emulator uses one ICCTA and three resistors [143]. The PHL was not deformed up to 5 kHz.

A charge-controlled MRE has been developed using a DVCCTA with one capacitor and two resistors by Nidhee Bhuwal *et al.* [144]. This circuit can switch between grounded and floating configurations with a single switch and operate in incremental or decremental modes with an additional switch. Thus, the same circuit can function as a F-MRE and G-MRE in

either mode using just two switches. The PHL has been obtained for the high frequency range up to several hundreds of MHz.

2.3 Realization of meminductor/memcapacitor emulators with multipliers

Maheshwar Pd reported a mutator-based meminductor emulator (MIE) that utilizes a CCII+, along with three operational amplifiers, resistors, a memristor, and a capacitor. Two dependent current sources, a multiplier, resistors, capacitors, and an op-amp are used in the realization of reported MIE design. Series, parallel, and hybrid connections of meminductors are used to verify the reported emulator's performance [145]. The hysteresis loop retains its shape over a frequency range of 0.5 kHz to 1 kHz.

A floating memristor-less MIE has been realized by Y. Liang *et al.* using four CCII+s, two op-amps, an AM, a buffer, a few resistors, and two grounded capacitors [146]. The PHLs are obtained in the frequency range of a few tens' Hz.

Maheshwar Pd. Sah *et al.* [147] reported a charge-controlled MIE using three op-amps, six NMOS transistors, six PMOS transistors, a multiplier, an inductor, two resistors, a capacitor, and a switch. It has been claimed that the performance of reported MIE is satisfactory up to 300 Hz frequency.

Mohammed E. Fouda and Ahmed G. Radwan designed a current-controlled MIE using three CCII+s, three resistors, a multiplier, an adder, and two capacitors. In contrast, a voltage-controlled MIE was realized using three CCII+s, an adder, a divider, three grounded resistors, and two capacitors [148]. The PHL has been obtained for the frequency of 0.2 Hz.

Another MIE was reported by Fang Yuan *et al.* for chaos generation using four op-amps, two analog multipliers, two capacitors and nine resistors, [149]. A chaotic oscillator was also realized using a MIE to verify the performance. The PHLs are obtained at 180 Hz.

Yang Ling *et al.* designed a flux-controlled MIE using two capacitors, eight op-amps, an AM and nine resistors. A hardware implementation and simulation were conducted to confirm the functionality of the stated emulator circuit [150]. The frequency range was found to be 400 Hz to 800 Hz.

John Vista and Ashish Ranjan presented the two designs of VDTA-based MIEs [151]. In the first design, two VDTAs, a multiplier, and two grounded capacitors were used, whereas in the second design, two VDTAs and two grounded capacitors were used. The second design

does not employ a multiplier. A neuromorphic circuit simulating the behavior of amoeba is presented to demonstrate the functionality of the reported emulator. The PHL is achieved up to 1.5 MHz.

Fang Yuan *et al.* reported the op-amp based MIE [152]. Seven op-amps, a multiplier, thirteen resistors, and a capacitor were used in the design. The chaotic circuit utilizing the op-amp-based MIE was also reported. The PHL was not deformed up to 300 Hz for the reported MIE.

Dongsheng Yu *et al.* realized a floating universal mutator circuit for MREs, MCEs and MIEs [153]. The mutator was realized using four CCII+s, a multiplier, four resistors, a capacitor, and two devices connected to the 'z' and 'x' terminals of the fourth current conveyor. The capacitor and varactor diode, resistor and varactor diode, and varactor diode and resistor are utilized for the realizations of MREs, MCEs and MIEs, respectively. The operating frequency range of reported mutator is 8 kHz.

Yuan and Yuxia Li reported another op-amp-based MREs, MCEs and MIEs [154]. The MRE was reported using four multipliers, five op-amps, capacitors, and a few resistors. The MIE circuit was designed using a multiplier, seven op-amps, a capacitor, and a few resistors. In contrast, three op-amps, a multiplier, a few resistors, and two capacitors were used to realize the MCE circuit. These three emulators were connected in parallel to configure a chaotic oscillator.The PHL was not deformed up to 400 Hz for the reported MIE.

Hasan Sozen and Ugur Cam designed the grounded and floating MIEs using a multiplier, two capacitors, two resistors, an OTA, two CCII+s, and a CFOA [155]. The PHLs are achieved for the frequency range of 500 Hz to 5 kHz.

Mustafa Konal *et al.* realized a MIE using a dual-output OTA, a MO-OTA, an AM, two resistors, and two capacitors [156]. To show the workability of the proposed MIE, PHLs have been plotted for single, parallel, and composite meminductors. The experimental setup has also been suggested for a meminductor. The operating frequency range of reported MIE is spanning from 1 Hz to 10 kHz.

Fang Yuan *et al.* realized a local active multistable MIE based on a mathematical formulation. The coexisting metastable PHLs have been formed for the reported MIE. It was realized with the help of seven op-amps, two analog multipliers, fourteen resistors, two capacitors, and a switch [157]. The PHL was not deformed in the frequency range of 0.5

kHz to 1.5 kHz for the reported MIE.

Another MIE was realized using three multipliers, fourteen resistors, two capacitors, and six op-amps by D. D. Zhai, F. Q. Wang *et al.* [158]. A simple double-scroll chaotic oscillator circuit is implemented using the reported MIE. The hysteresis loop was found to be undistorted across frequencies spanning from 1.8 kHz to 3 kHz.

Farbod Setoudeh and Massoud Dousti designed a flux-controlled MIE using ten resistors, two capacitors, multiplier and five op-amps. A Colpitt oscillator was realized using the reported MIE [159]. The hysteresis loop was found to be undistorted across frequencies spanning from 50 Hz to 200 Hz.

The charge-controlled MIE is realized by Muhammet Oguz Korkmaz *et al.* using a dual input second-generation current conveyor, a CCII+, a multiplier, two resistors, two capacitors, and an inductor [160]. The hysteresis loop was found to be undistorted across frequencies starting from 300 Hz to 700 Hz.

Another MIE is realized by Durmus Ersoy and Firat Kaçar in [161] using an OTA, a multiple-output OTA, a multiplier, a resistor, and two capacitors. The chaotic oscillator and neuromorphic circuit are realized by embedding the reported MIE. The hysteresis loops are obtained at 1 MHz for the reported MIE.

A mutator circuit that converts the MRE into MCE and MIE was suggested by Yu Dong-Sheng *et al.* [162]. Two CCII+s, a MRE, a capacitor, and a resistor are used to construct the MCE circuit. The MIE circuit was also suggested using one resistor, a memristor, a capacitor, and two CCII+. The MRE was realized using two op-amps, two CCII+s, a capacitor, an AM, and seven resistors. The operating frequency of reported emulator is 80 Hz.

A mem-element emulator is reported by Yue Liu *et al.* [163] that can emulate memristor, memcapacitor, and meminductor. The generalized emulator is realized using three CCII+s, two-op-amps and multipliers with two capacitors and six resistors. The ports P1, P2, and P3 are chosen appropriately to get the three types of mem-elements. The hysteresis loop was found to be undistorted for frequencies starting from 1 kHz to 10 kHz.

2.4 Realization of multiplier-less meminductor/memcapacitor emulators

Yuriy V. Pershin and Massimiliano Di Ventra reported the op-amp-based MIEs and MCEs

[164]. An op-amp, memristor, and capacitor were used to design these emulators. The MCEs and MIEs and vice versa are realized by interchanging the memristor and capacitor positions. The MRE circuit is also suggested with the help of a microcontroller, A to D converter, and potentiometer. The mem-element was reported to work satisfactorily within the frequency range of 10 kHz.

Yunus Babacan reported an op-amp-based MIEs and MCEs [165]. The MCE was reported using an OTA, two grounded capacitors, and a voltage source. In contrast, the MIE has been reported using an inductor, a capacitor, a resistor, an OTA, and a voltage source. The PHLs were successfully obtained within the frequency of 100 to 300 Hz for the MCE. In contrast, the PHLs have been obtained within the frequency range of 100 Hz to 300 Hz for the MIE.

Antoniou's gyrator-based MIE was reported by Francisco J. Romero *et al.* [166] using five op-amps, seven resistors, and two capacitors. The hardware implementation is also suggested using off-the-shelf components. The hysteresis loop was found to be undistorted in the frequency range of 1kHz to 10kHz for the suggested MIE.

The mathematical formulation of the MIE and its field programmable analog array (FPAA)-based realization is suggested by Preecha Thongdit *et al.* [167]. Two integrators, a multiplier, an adder, and two inverting gain amplifiers of FPAA were used. The PHLs have been formed for 5 kHz, 10 kHz, and 20 kHz frequencies.

The VDCC based MIEs and MCEs are suggested by Aneet Singh and Shireesh Kumar Rai [168] using a VDCC, a resistor, and a capacitor. The MCE and MIE realization are obtained by switching the positions of the memristor and capacitor. The SPICE model of memristor and MRE were both utilized to verify the responses of MCE and MIEs. An adaptive learning circuit is also realized using MCEs and MIEs. The operating frequency range was achieved from 0.3 Hz to 0.7 MHz for the reported MCE and MIE.

Francisco J. Romero *et al.* realized a floating MIE using Riordan gyrator [169]. The design of a MIE was suggested using three op-amps, five resistors and a capacitor. The PHLs were observed in between 1 kHz to 10 kHz.

The characteristics of self and mutual meminductance are analyzed between two MIEs by D.S. Yu *et al.* [170]. The four CCs, three op-amps, a multiplier, nine resistors, and two capacitors have been utilized in the design of MIEs. The operating frequency of MIE is found to be in the range of 10 Hz to 15 Hz.

Zehra Gülru Çam Taskıran *et al.* reported the MCEs and MIEs using a CBTA, a memristor, and a capacitor [171]. In the reported design, the position of the memristor and capacitor can be interchanged to convert the circuit into MCE and MIE. The operating frequency is found to be within 100 kHz.

The OTA, VDTA, and a grounded capacitor were utilized by Keshab Kumar and Bal Chand Nagar to realize the MIE [172]. The PHL has been maintained up to 3 MHz frequency. A bandpass filter using a MIE is realized to demonstrate its application.

Hacer Atar Yildiz and Serdar Ozoguz reported a MIE using two integrators realized by CCII+ and two buffers. The internal capacitance of MOSFET is utilized rather than any external capacitor. The design also uses one additional current conveyor circuit [173]. The pinched hysteresis were observed between 20 MHz to 70 MHz.

Another grounded decremental/incremental MIE was realized using three OTAs and two grounded capacitors by Ankur Singh *et al.* [174]. The operating frequency range is achieved from 100 Hz to 100 kHz.

The second-generation current conveyor transconductance amplifier (CCIITA) based MIE was reported by Anmol Verma *et al.* [175]. One memristor and a capacitor are used along with a single CCIITA. The PHLs are plotted for the high range of frequencies. A neuromorphic circuit using a CCIITA-based MIE is also realized. The hysteresis loop was found to be undistorted within a frequency range of 20 MHz to 200 MHz.

Aneet Singh and Shireesh Kumar Rai realized the op-amp-based MIE circuits [176] using a capacitor, two op-amps, and three resistors. The hardware implementation is also suggested for the reported MIE. The chaotic oscillator is also realized using suggested MIE. The PHLs were observed up to 2 MHz frequency for the reported MIE.

Anamika Raj *et al.* realized a grounded MIE using a resistor, two OTAs, a DVCC, and two capacitors. [177]. The non-volatility test and temperature analysis are reported for the MIE. The PHLs are not distorted up to 1.75 kHz frequency for the proposed MIE.

Another tunable MIE was reported by Anamika Raj *et al.* using three OTAs, and two grounded capacitors [178]. The performance and robustness of the circuit are checked using process and temperature variations. The operating frequency is found to be 10 MHz.

A multiple-output VDTA (MOVDTA) based MIE was reported by Predrag B. Petrovic *et al.* [179]. The MOVDTA and two capacitors are utilized in the design of the MIE. The PHLs

are obtained up to 3 MHz frequency. A neuromorphic circuit is also realized to demonstrate the functionality of the reported MIE.

Aneet Singh and Shireesh Kumar Rai reported single op-amp-based circuits of MIEs [180]. The op-amp, memristor, a few resistors, and two capacitors are used in the design of the MIE. The chaotic oscillator is also realized to demonstrate the application of the reported emulator. The PHLs are not distorted up to 128 kHz frequency for the suggested MIE.

The modified voltage differencing current conveyor (MVDCC) and OTA are used in the configuration of memristor and MIEs by Kapil Bhardwaj and Mayank Srivastava [181]. Two resistors and a capacitor are used to realize a memristor, whereas two grounded capacitors and a resistor are used to create a MIE. A neuromorphic circuit is realized using a reported MIE. The PHLs are found to be undistorted for the frequency range of 100 kHz to 300 kHz.

Next, the MRE and MIE are realized by Kapil Bhardwaj and Mayank Srivastava using a VDTA and a dual output CCII+. The passive components used to realize a memristor are two resistors and a capacitor, whereas a resistor and two capacitors were used for the MIE [182]. The reported mem-elements emulator is used in the design of neuromorphic circuits. The PHLs are not distorted up to 200kHz frequency for the proposed MIE.

The memristor-less and resistor-less MIE is reported using a multi-output OTA, an OTA, and two grounded capacitors by Bhawana Aggarwal *et al.* The workability of the reported MIE is verified through a chaotic oscillator [183]. The PHLs are found to be undistorted for the frequency range of 600 kHz to 900 kHz.

A flux-controlled MIE has been designed using three OTAs and two grounded capacitors by Kapil Bhardwaj and Mayank Srivastava. In contrast, the MCE emulator is realized using an OTA, a CCII+, a resistor, and two capacitors [184]. The PHLs are not distorted up to 1.2 MHz frequency for the proposed MIE.

Another MIE is realized using two OTAs and two CCs along with two capacitors and a resistor by Garima Shukla *et al.* [185]. The reported MIE is employed in the design of the amplitude modulation circuit. The PHLs are found to be undistorted for the frequency range of 100 kHz to 500 kHz.

The CDTA based MIE is realized using two CDTAs and two grounded capacitors by Harsh Jain *et al.* The chaotic oscillator and neuromorphic circuit are used for the verification [186]. The operating frequency range of suggested MIE is 300 kHz to 500 kHz.

Vikas Singroha *et al.* reported a MIE using a voltage differencing buffered amplifier, a memristor, a resistor, and a capacitor [187]. The frequency range of suggested MIE is found to be 4.3 Hz to 4.9 Hz.

The voltage differencing current conveyor (VDCC) based MRE, MIE and MCE are implemented by Predrag B. Petrovic [188]. The MIE is realized using two VDCCs, two capacitors, and two PMOS transistors. The MCE is also realized using the same analog building blocks and components, but the configuration differs from the MIE. The MRE is realized using two VDCCs and a grounded capacitor. The hysteresis loop are found to be undistorted for frequencies range upto 1 MHz to 10 MHz.

Harsh Jain *et al.* realized the modified voltage differencing voltage transconductance amplifier (MVDVTA) based MIE [189]. The PHLs are obtained up to 500 kHz frequency. The design of the reported MIE utilizes an MVDVTA, two capacitors, and a resistor. The design's functionality has been confirmed through a chaotic oscillator and a neuromorphic circuit.

A dual mem-element MRE and MIE are reported using a VDIBA, an OTA, two MOS transistors, a resistor, and a capacitor by Kapil Bhardwaj and Mayank Srivastava [190]. The PHLs are obtained for both the mem-elements at 2 MHz frequency.

Another mem-element emulator is reported by Kapil Bhardwaj and Mayank Srivastava using a VDCC, an OTA, a capacitor, a resistor, and a generalized impedance (Z). If the capacitor is used in place of Z, it behaves as a memcapacitor, and if 'Z' is replaced as a resistor, it behaves as a memristor. The performance verification is done through an adaptive learning circuit [191]. The mem-element was reported to work satisfactorily within the frequency of 250 kHz.

Ansh Goel *et al.* implemented a MIE using an OTA, a CCII+, a CDBA, a capacitor, and a resistor [192]. The PHLs are obtained at 1 MHz frequency. The reported MIE is embedded in the design of the chaotic oscillator for performance verification.

Anshul Gupta *et al.* reported a fractional-order MIE in [193]. The realization uses a fractional capacitor, two OTAs, a CDBA and a capacitor. The performance verification is done through an adaptive learning circuit. The PHLs were observed at a frequency of 3 MHz for the suggested fractional-order meminductor.

Rupam Das *et al.* designed a MIE based on the modified differential voltage current

conveyor transconductance amplifier (MDVCCTA), two capacitors and a resistor [194]. The circuit's validation was demonstrated in neuromorphic application and a chaotic oscillator. The hysteresis loop are found to be undistorted at high frequency but use of passive resistor makes the realization less attractive.

B. Suresha *et al.* presented a G-MIE using a dual-output CCII+ (DO-CCII), an OTA, along with three resistors, an inductor, and two capacitors [195]. The neuromorphic circuit was demonstrated to validate the effectiveness of MIE. The performance of reported MIE is found to be satisfactory within the range of 100 Hz to 700 Hz.

2.5 Identified research gaps

After reviewing the literature, it has been noted that several designs utilize analog multipliers to achieve the non-linear behavior of mem-elements, resulting in complex circuitry. Other designs that do not employ analog multipliers only achieve PHL formation at frequencies up to a few kHz or MHzs. The MOS-based design of emulators provides a restricted range of transconductance, which in turn limits the range of values for mem-elements. Using active building blocks in the design of memelement emulators offers several advantages over compact MOS-based designs, stemming from the inherent flexibility and functionality of active components. Active building blocks enable precise control over the emulator's behavior, such as adjustable resistance ranges and tunable nonlinearity or dynamic response. This makes them particularly valuable in applications like analog computing, adaptive circuits, and neuromorphic systems, where customizable parameters are essential. They also provide excellent linearity and predictable behavior, ensuring accurate emulation of memelement characteristics. In contrast, MOS-based designs often suffer from non-idealities such as threshold voltage mismatch, process variations, and nonlinearity. Moreover, active building blocks can operate over a broader range of voltages and currents, making them suitable for diverse applications. MOS-based emulators, constrained by the operating range of MOSFETs, lack this flexibility. Analog systems such as filters, oscillators, and learning circuits benefit significantly from the high precision and accuracy of active building blocks, which minimize errors caused by parameter drift or variability common issues in MOS-based designs. Memelement characteristics like hysteresis or non-linear switching are easier to replicate using active building blocks, as feedback and control circuits can be designed to emulate these behaviors closely. In contrast, compact MOS-based

designs require complex arrangements and additional transistors to approximate such characteristics. Furthermore, active building blocks are less sensitive to process variations, especially in scaled-down technology nodes, ensuring consistent performance across different fabrication runs. They also simplify impedance matching in analog and mixed-signal applications, which is critical for maintaining signal integrity. Another significant advantage of active building blocks is their adaptability. Designers can easily modify the circuit topology or feedback configuration to tailor memelement emulators for various applications. MOS-based designs, on the other hand, tend to be more rigid and require substantial redesign to meet new requirements. Additionally, active building blocks can incorporate elements to model memelement non-idealities, such as frequency-dependent behavior or parasitics, without adding significant circuit complexity. Achieving similar functionality in MOS-based designs often demands more transistors and intricate configurations. While MOS-based designs do offer benefits such as compactness, simplicity, and compatibility with CMOS technology important for highly integrated systems and digital applications their performance may be limited in high-precision analog circuits, where active building blocks excel.

Thus, based on the literature survey, it is concluded that the mem-elements emulator reported in the literature have one or more drawbacks, as follows: (i) the circuit is very complex and requires multiplier in many designs (ii) only one configuration of incremental/decremental is reported in several designs (iii) Many designs of mem-elements emulator reported only grounded type configuration (iv) limited frequency range (v) usage of memristor for the realization of meminductor emulators. Based on the drawbacks mentioned above, the following research gaps have been identified:

1. Resistor-less grounded and floating incremental/decremental mem-elements emulators need to be investigated using a minimum number of active and passive components.
2. Realization of mem-element emulators without using analog multipliers for an improved range of memristance and meminductance is needed.
3. Mem-element emulators which work well over a wide range of frequencies (MHz) are required for high-frequency applications.

2.6 Objectives of the proposed work

The objectives of the thesis have been predefined as

1. To design grounded and floating mem-elements emulator using minimum number of active and passive components.
2. To enhance the performance of designed emulators in terms of mem-elements value and range of operating frequency.
3. To validate the performance of proposed mem-elements emulator by demonstrating their different applications.

2.7 Research methodology

The objectives of the research are achieved by following methodologies:

1. The specifications have been defined for designing of mem-element emulator circuits and based on these specifications, the proposed circuits of mem-element have been realized using the Mentor Graphics Eldo simulation tool.

2. The performance of proposed mem-element emulators have been verified on the basis of several parameters such as non-volatility test, transient analysis, Monte Carlo analysis, temperature analysis, supply voltage variations, formation of PHLs for a wide range of frequencies, mem-element's value, etc. The performances of proposed mem-element emulators have been compared with performances of existing mem-element emulators.
3. Three applications namely analog filters, adaptive learning circuits, and chaotic oscillators have been used to demonstrate the performance of proposed designs of mem-element emulators.

CHAPTER 3

PROPOSED MEMRISTOR EMULATORS USING ANALOG BUILDING BLOCKS

3.1 Introduction

The evolution of mem-element technology has sparked interest due to its advanced features compared to other conventional components in VLSI. Researchers have identified numerous applications for mem-elements, including neuromorphic computing [6-7, 122, 153, 183, 186, 188, 189], digital memories [119], logic circuits [123], communication systems [54, 81, 94, 98, 105, 136, 187], analog filter applications [87, 95, 107, 123, 113, 128, 174], programmable logics [55, 73, 83, 99, 174], physical unclonable functions (PUFs) [9, 11-12], oscillator circuits [183, 186, 190, 193], and pattern recognition [8]. Memristors, in particular, have become the cornerstone for new analog circuits that mimic the brain's functionality, with potential applications in IoT, controllers and sensors [22-25], biomedical applications [14-18], instrumentation and robotics [6], and memory systems [22-23].

The initial discovery of the memristor existed before Prof. Leon Chua's prediction in 1971. Stanford University professor Bernard Widrow introduced the memristor in 1960 as a ground-breaking three-terminal device. This device skilfully controls resistance by utilizing the time integral of the current to manipulate the charge in the third terminal, consequently maintaining the conductance between the two terminals. Additionally, in 1968, F. Argall's findings were reported in [196] akin to the memristor model that Stanley Williams and his colleagues introduced. In 1976, Leon Chua and his associates expounded upon the concept of memristors and memristive systems by introducing a pinched hysteresis curve, thus further illustrating the behavior of current versus voltage.

IBM's Zurich research laboratory researchers reported reproducible resistance-switching effects in thin oxide films [197]. Despite numerous devices exhibiting behavior akin to the memristor between 1994 and 2008, HP scientists successfully linked their work to Chua's memristor postulation. The memristor was fabricated as a device in 2008 by Stanley Williams and colleagues at HP Lab, marking a significant milestone in electronics history with potential applications spanning memory technology to neuromorphic computing.

However, manufacturing and scalability challenges limit physical memristors' availability for research and experimentation. Consequently, memristor emulators have emerged as substitutes, designed to simulate memristor behavior in a controlled and reproducible manner. These emulators enable the exploration of memristor-based applications, even when physical memristors are scarce or expensive. Various SPICE macro models, such as those developed by Zdenek Biolek *et al.* [198] in June 2009, have been used to imitate memristor behavior. Other researchers have proposed SPICE macro models and CMOS emulators for memristors, verifying their performance against mathematical models and experimental data.

In conclusion, memristor emulators (MREs) play a crucial role in investigating the dynamic behavior of memristors experimentally, with designs often utilizing analog multipliers to simulate memristor characteristics effectively.

The complexity associated with analog multipliers has been noted as a limitation in the literature. To address this issue, proposed MREs have been designed to simplify the overall design process. The research also covers the analysis of various analog building blocks, including OTA [199], CDBA [200], VDGA [201], FB-VDBA [202], and VDTA [203-204]. Unlike previous structures that relied heavily on several analog building blocks and passive components, the proposed emulators utilize only one or two analog building blocks, resulting in a more straightforward design.

In existing designs, many resistors have been used as passive components, contributing to power dissipation. To mitigate this, the proposed MREs have been developed without resistors, reducing power consumption. Additionally, many existing circuits have been designed with higher power supply, while some have limitations in their frequency range, operating only in the Hz or kHz range. The proposed emulators aim to address these drawbacks of the MREs reported in the literature, offering simplified structures and improved performance.

This chapter presents three proposed MRE circuits that use one or two analog analog building blocks and one grounded capacitor. The first proposed circuit for a MRE uses an operational transconductance amplifier (OTA), a current differencing buffered amplifier (CDBA), and a grounded capacitor. The second proposed MRE circuit has been realized using a voltage differencing gain amplifier (VDGA), and a grounded capacitor. The third proposed MRE has been designed using a fully-balanced voltage differencing buffered

amplifier (FB-VDBA), and a grounded capacitor. The minimal passive components, such as a capacitor and a low-voltage supply, are used to realize the three proposed MREs.

The proposed MREs offer various improved performance parameters such as wide frequency range, high memristance range, and low supply voltage requirement. Additionally, multiple applications have been used to validate the proposed MRE's performances. The chapter is organized as follows: Section 3.2 goes over the circuit description of OTA and CDBA. It also covers the operation of the proposed grounded and floating MREs using OTA and CDBA and the mathematical analysis of these emulators. In section 3.3, the focus shifts to the circuit description of VDGA. The functioning of the proposed grounded and floating MREs with VDGA is described, along with mathematical analysis. Following that, section 3.4 delves into the description of FB-VDBA. It investigates the ideas underlying the proposed grounded and floating MREs utilizing FB-VDBA. It also covers mathematical analysis. Section 3.5 marks the conclusion section of the chapter.

3.2 Proposed memristor emulators using OTA and CDBA

In this section, proposed grounded and floating memristor emulators (G-MREs and F-MREs) using OTA and CDBA have been discussed. The terminal characteristics of analog building blocks (OTA and CDBA) are presented first. The working principle of proposed MREs with mathematical derivations is discussed thereafter. The configurations of both incremental and decremental modes have been presented.

3.2.1 Description of operational transconductance amplifier

The operational transconductance amplifier (OTA) is one of the analog building blocks that is being used in varieties of applications in analog signal processing. It comprises five terminals, two of which are used for voltage input, another two are used for current output, and the remaining one is used for the tuning of the transconductance gain (Gm) of OTA with the help of bias voltage (V_B). The OTA has a very high input impedance. Its high input impedance terminals, '+ 'and '-,' respectively, receive two voltages, Vin+ and Vin-. Equation. (3.1) indicates how its transconductance gain (Gm) transforms these voltages into two currents, Io+ and Io-. The transconductance gain (Gm) of OTA is given in Equation (3.2)

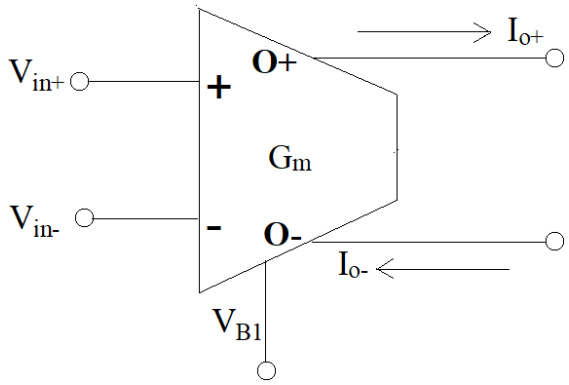


Fig.3.1 Symbolic representation of voltage-tunable OTA [98].

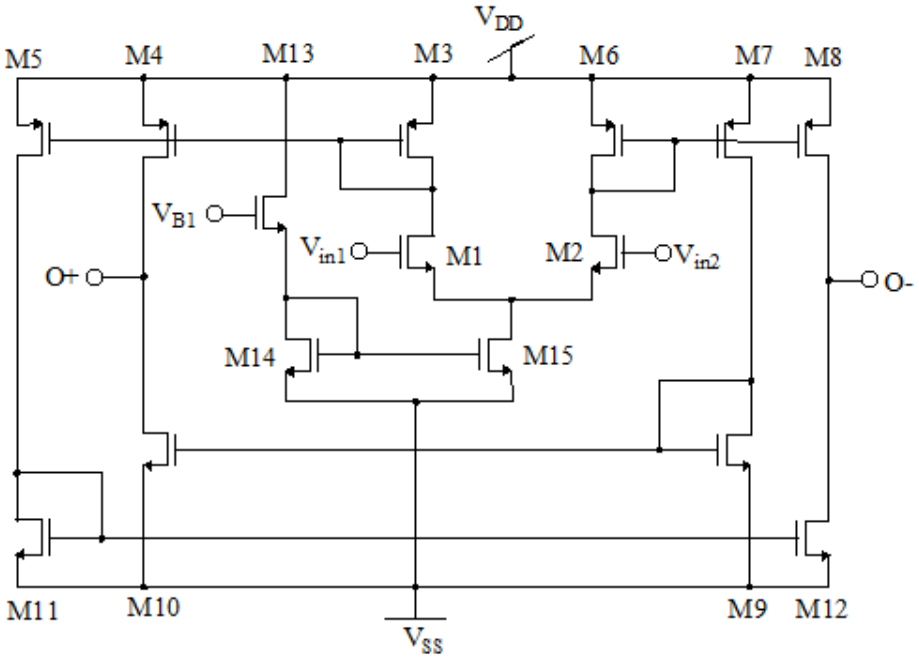


Fig. 3.2 CMOS implementation of voltage-tunable OTA.

$$I_{0+} = \pm G_m V_{\text{in}} \text{ where } V_{\text{in}} = V_{\text{in}+} - V_{\text{in}-} \tag{3.1}$$

$$G_m = \frac{K}{\sqrt{2}}(V_{B1} - V_{SS} - 2V_{th}) \tag{3.2}$$

$$K = \mu_n C_{ox} \frac{W}{L} \tag{3.3}$$

The value of bias voltage (V_{B1}) can be changed to alter the transconductance gain (Gm) of voltage-tunable OTA in Equation. (3.3) provides the value of K, which is dependent upon the gate-oxide capacitance (C_{ox}), mobility (μ_n) of the charge carrier, and aspect ratio (W/L) of the MOSFETs. In Fig. 3.1, the symbol of voltage-tunable OTA is presented. The non-ideal behaviour of OTA has been described in appendix A.2. Fig. 3.2 shows the CMOS implementation of voltage-tunable OTA.

3.2.2 Description of the current differencing buffered amplifier

As illustrated in Fig. 3.3, the current differencing buffered amplifier (CDBA) is an analog building block of four terminals I_P and I_N are currents applied to low-impedance input terminals P and N.

$$V_P = V_N = 0, \quad I_Z = I_P - I_N, \quad V_W = V_Z \tag{3.4}$$

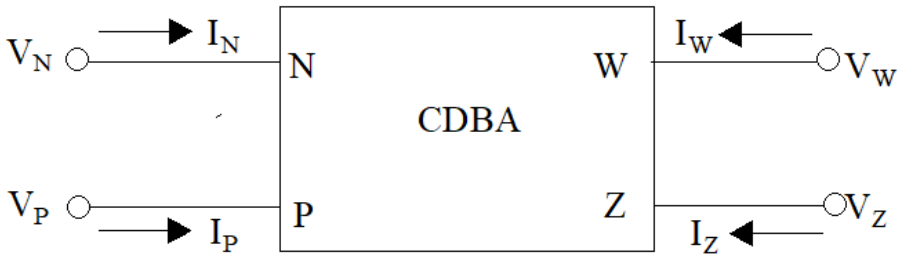


Fig. 3.3 Symbolic notation of CDBA.

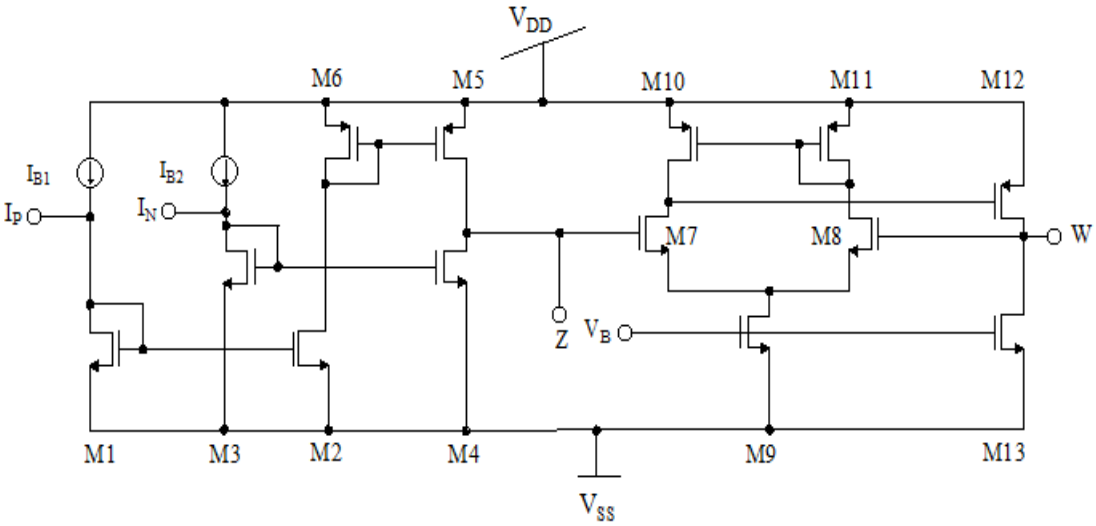
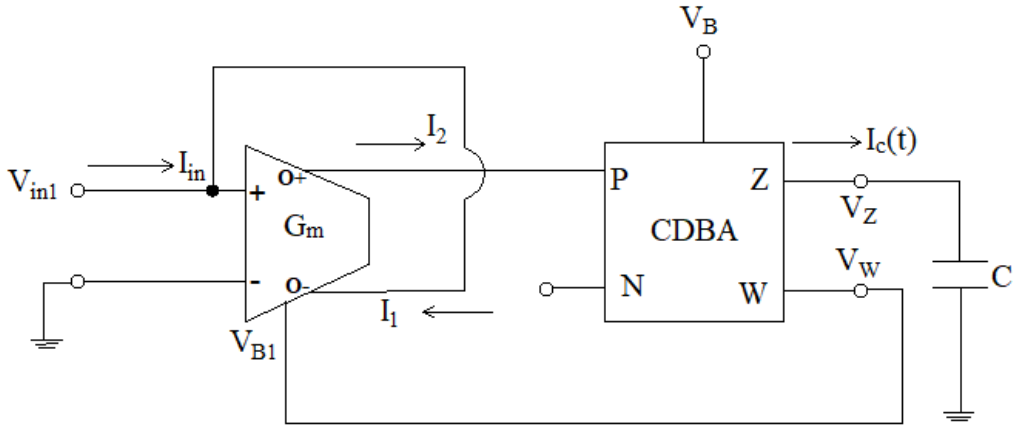


Fig. 3.4 CMOS implementation of CDBA [205].

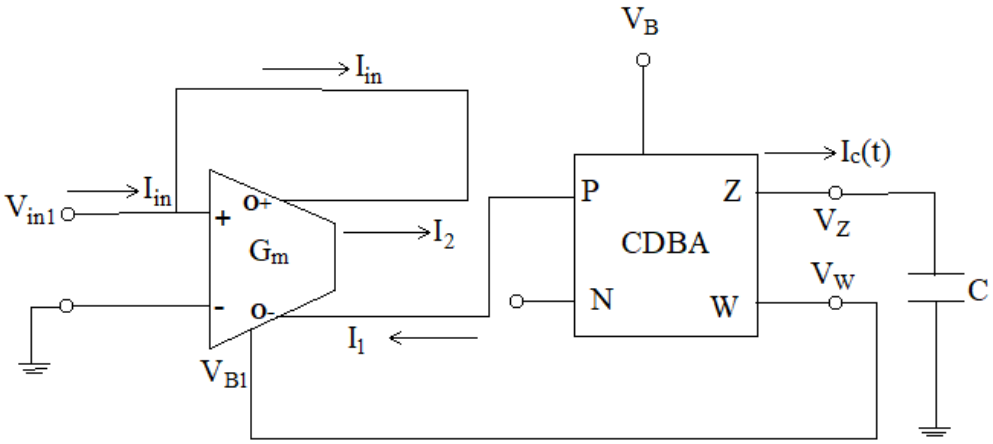
The current (I_Z) is transformed to voltage (V_Z) by connecting the impedance to the 'Z' terminal. An inbuilt buffer copies voltage V_Z from 'Z' terminal to voltage V_W at 'W' terminal. Equation. (3.4) describes the terminal Equations of the ideal CDBA. The non-ideal behaviour of CDBA has been described in appendix. Fig. 3.4 displays the CMOS implementation of CDBA [205], which is utilized with OTA to design the proposed MRE.

3.2.3 Working principle of proposed memristor emulators

This section presents the proposed memristor emulators (MREs) designed using OTA and CDBA. A comprehensive discussion on G-MREs and F-MREs is provided. Additionally, the G-MREs and F-MREs are modified into incremental and decremental configurations by slightly altering the connections in the proposed design.

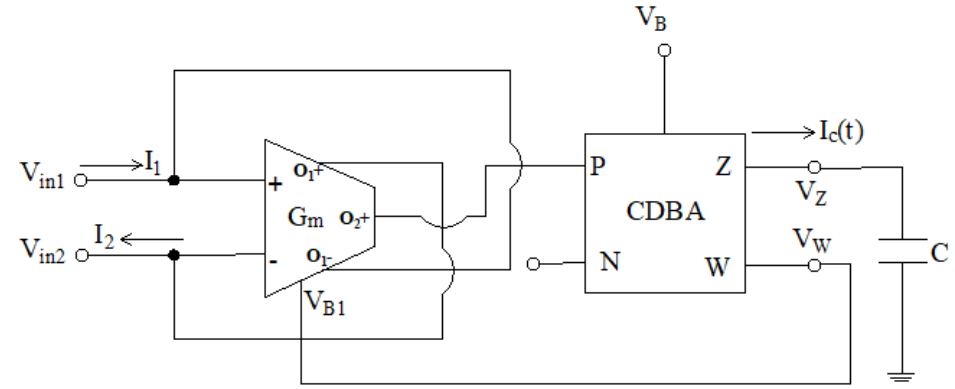


(a)

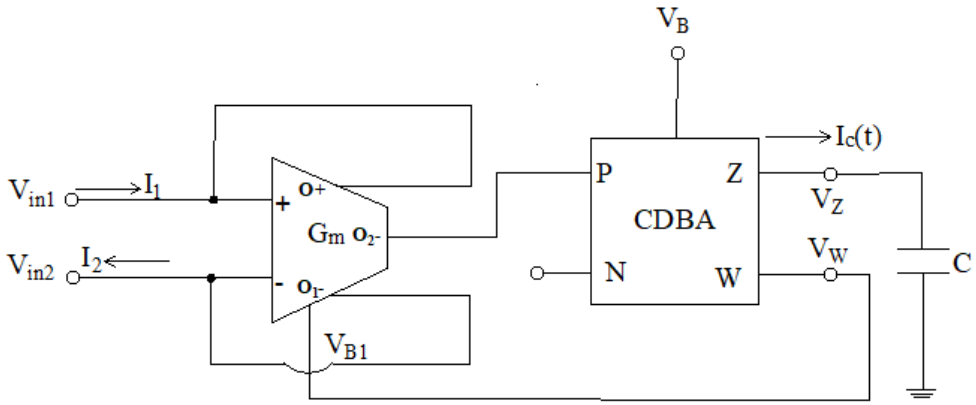


(b)

Fig. 3.5 Proposed G-MRE based on OTA and CDBA (a) decremental (b) incremental.



(a)



(b)

Fig. 3.6. Proposed F-MREs based on OTA and CDBA (a) decremental (b) incremental.

The memristor, known as a resistor with memory, is implemented in the proposed designs shown in Figs. 3.5 (a) and (b) using an electronically tunable resistor realized through OTA. In these figures, the resistor is realized by connecting one of the OTA's input terminals '+' to one of its output terminals 'o-' (or 'o+'). To realize the G-MREs, the other OTA input terminal '-' is connected to the ground, as depicted in Figs. 3.5 (a) and (b).

The output current of the OTA (I_{O+} or I_{O-}) is directed to the input terminal 'P' of the CDBA, with the terminal 'N' left open. The capacitor C, functioning as a memory element, is linked to the 'Z' terminal of the CDBA. The capacitor C gets charged due to the current (I_P) flowing through the 'P' terminal of the CDBA, as both currents I_P and I_Z are equal. The voltage (Vz) developed across the capacitor C is transferred to the 'W' terminal of the CDBA using an inbuilt buffer. The voltage (Vw) is linked to the bias voltage (V_{B1}) of the OTA, which modulates the transconductance gain (Gm) of the voltage tunable OTA. For the proposed decremental MRE configuration, the output terminal 'o-' is connected to the OTA's input

terminal '+', while for the incremental MRE configuration, the output terminal 'o+' is linked to the same input terminal '+' of the OTA.

In the F-MRE, both terminals ('o+' and 'o-') of the OTA are maintained at different voltages, V_{in1} and V_{in2}, as illustrated in Fig. 3.6 (a) and (b). The OTA output terminals 'o_{1+}' and 'o_{1-}' are connected to input terminals '-' and '+' to establish a floating resistor, as shown in Fig. 3.6 (a). The capacitor C serves as the memory element in this configuration. The OTA output terminal 'o_{1-}'is connected to the CDBA's input terminal 'P'. The floating resistor's output current is then passed through the CDBA to charge the capacitor C at the 'Z' terminal of the CDBA. The voltage Vz across the capacitor C is copied to the 'W' terminal of the CDBA and eventually to the bias terminal (V_{B1}) of the OTA. Through this feedback mechanism, the transconductance (Gm) and indirectly the resistance (R = 1/Gm) are controlled. The resistance is influenced by the previous state stored in the capacitor, regulating the resistance of the proposed MRE. The suggested floating incremental MRE is shown in Fig. 3.6(b). The decremental (or incremental) configurations can be achieved by modifying the connection of the OTA output terminals ('o_{1+}' and 'o_{1-}) to the 'P' terminal of the CDBA.

3.2.4 Mathematical analysis of proposed memristor emulators

This section presents the numerical analysis of the proposed memristor emulator (MRE) using OTA and CDBA. The numerical analysis of non-ideal behaviour of the proposed MRE has discussed in appendix B.2. The following Equations are obtained by the routine analysis of the proposed MRE circuit shown in Fig. 3.6 (a).

$$I_1(t) = G_m[V_{in1}(t) - V_{in2}(t)] = G_m V_{in}(t) \tag{3.5}$$

where, $V_{in}(t) = V_{\text{in}1}(t) - V_{\text{in}2}(t)$

The current I_C is obtained as

$$I_Z = -I_C(t) = -G_m V_{in}(t) \tag{3.6}$$

$$V_Z = I_Z \times \frac{1}{sC} = -\frac{1}{C}\int I_c\,(t)dt = -\frac{1}{C}\int G_m\, V_{in}(t)dt \tag{3.7}$$

$$V_W = V_{B1} = V_Z \tag{3.8}$$

Bias voltage V_{B1} is given by

$$V_{B1} = -\frac{1}{C}\int I_c\,(t)dt = -\frac{1}{C}\int G_m V_{in}\,(t)dt = -G_m\frac{\phi_{in}}{C} \tag{3.9}$$

where, $\phi_{in} = \int V_{in}\,(t)dt$ is the total flux obtained by the memristor.

Substituting the value of V_{B1} from Equation (3.9) to Equation (3.2), the value of transconductance (Gm) is obtained as

$$G_m = \frac{K}{\sqrt{2}}\left(-G_m\frac{\phi_{in}}{C} - V_{SS} - 2V_{th}\right) \tag{3.10}$$

The Equation (3.10) can be rearranged as

$$G_m = -\frac{\frac{K}{\sqrt{2}}(V_{SS} + 2V_{th})}{(1 + \frac{K}{\sqrt{2}}\frac{\phi_{in}}{C})} \tag{3.11}$$

Hence, the memristance of the proposed decremental F-MREs is obtained with the help of Equations (3.5) and (3.11).

$$M(\phi_m) = \frac{V_{in}}{I_{in}} = \frac{1}{G_m} = -\frac{(1 + \frac{k}{\sqrt{2}}\frac{\phi_{in}}{C})}{\frac{K}{\sqrt{2}}(V_{SS} + 2V_{th})} \tag{3.12}$$

The Equation. (3.12) can be rearranged as

$$M(\phi_m) = \frac{1}{\frac{K}{\sqrt{2}}(V_{SS} + 2V_{th})} - \frac{\phi_{in}}{C(V_{SS} + 2V_{th})} \tag{3.13}$$

$\leftarrow$ Fixed part $\rightarrow$ $\leftarrow$ Variable part $\rightarrow$

Similarly, by changing the connections as shown in Fig. 3.6 (b), the polarity of the variable part of Equation. (3.13) will be changed and result in incremental memristance as

$$M(\phi_m) = -\frac{1}{\frac{K}{\sqrt{2}}(V_{SS} + 2V_{th})} + \frac{\phi_{in}}{C(V_{SS} + 2V_{th})} \tag{3.14}$$

$\leftarrow$ Fixed part $\rightarrow\leftarrow$ Variable part $\rightarrow$

For the sinusoidal input signal, ϕ_{in} (t) can be written as

$$\phi_{in}(t) = \frac{A_m}{\omega}\sin\left(\omega t - \frac{\pi}{2}\right) \tag{3.15}$$

where, Am is the voltage amplitude and ω is the angular frequency of the input signal.

By substituting the value of ϕ(t) from (3.15) in Equations (3.13) and (3.14), the value of memristance can be expressed as

$$M(\phi_m) = -\frac{1}{\frac{K}{\sqrt{2}}(V_{SS} + 2V_{th})} \pm \frac{\frac{A_m}{\omega}\sin\left(\omega t - \frac{\pi}{2}\right)}{C(V_{SS} + 2V_{th})} \tag{3.16}$$

where '-' represents the decremental configuration and '+' indicates the incremental configuration. From Equation (3.16), it can be concluded that the memristance $M(\phi_m)$ of the proposed F-MREs consists of two components: one fixed and one variable. The fixed component remains constant for a given technology, while the variable component is influenced by the amplitude (Am) and frequency (ω) of the input signal. Additionally, it is dependent on the capacitance value used in the design. The non-ideal analysis of proposed MRE using OTA and CDBA is given in appendix B.2.

3.3 Proposed memristor emulator using VDGA

This section discusses the design of a memristor emulator (MRE) that utilizes a voltage differencing gain amplifier (VDGA). The key advantage of incorporating VDGA in the MRE design, compared to previous designs using OTA and CDBA, lies in its inherent gain, which can be adjusted by modifying the transconductance gains. The characteristics of the MRE can be effectively controlled by leveraging the gain control feature of the VDGA. To clarify the working principle of the proposed MRE design, the terminal characteristics of the VDGA are explained first. Subsequently, the operation of G-MREs and F-MREs, along with their mathematical analysis, is presented. These MREs (both grounded and floating) can be easily converted into incremental and decremental configurations with slight modifications to the circuit.

3.3.1 Description of voltage differencing gain amplifier

The voltage tunable voltage differencing gain amplifier (VDGA) is a seven-terminal active component, featuring two input terminals, P and N, three intermediate terminals, Z_{1+}, Z_{2+},

and Z-, one output terminal, W, and an additional terminal, V_B, for transconductance control. The symbol for the voltage tunable VDGA is shown in Fig. 3.7. VDGA has a very high input impedance, which makes the input currents I_P and I_N nearly zero. Voltages V_P and V_N are applied to the input terminals 'P' and 'N' of the VDGA. The difference in voltage between the 'P' and 'N' terminals is converted into current I_Z by transconductance (Gm) at the 'Z' terminal, as indicated in Equation. (3.17). The non-ideal behavior of VDGA has discussed in appendix A.4. The transconductance gain (Gm) is modulated by adjusting the bias voltage V_B, allowing for voltage tunability as detailed in Equation. (3.18). The current I_z is transformed into voltage V_z using impedance Zz, as specified in Equation. (3.19). The voltage V_w is given by β times V_z, as shown in Equation (3.20), where the voltage transfer

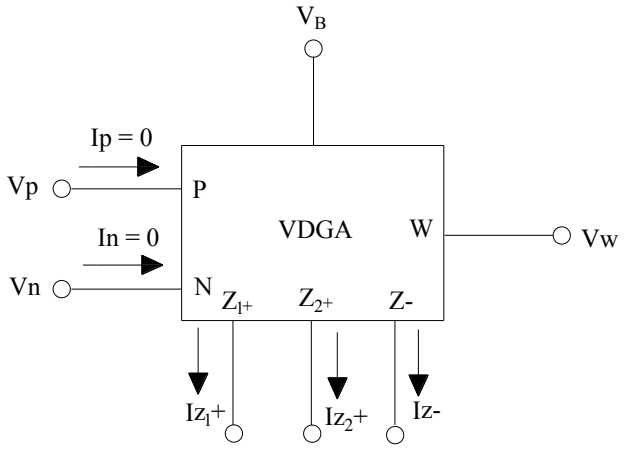


Fig. 3.7 Symbol of voltage-tunable VDGA [206]

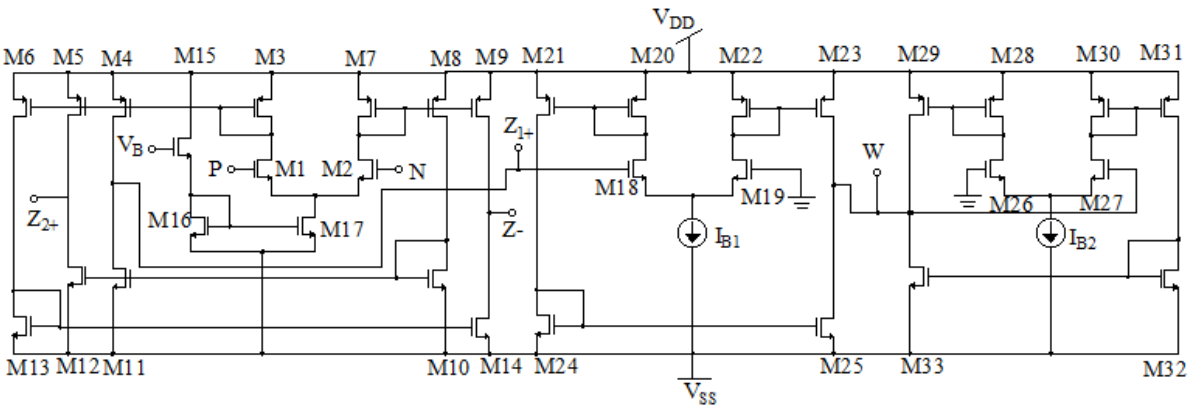


Fig. 3.8 Modified CMOS implementation of VDGA.

gain (β) is regulated through the biasing currents I_{B1} and I_{B2}. The VDGA implemented using CMOS technology is given Fig. 3.8. The terminal characteristics of the VDGA are described as follows:

$$I_P = I_N = 0, I_{Z+} = G_m(V_P - V_N), I_{Z-} = -G_m(V_P - V_N) \tag{3.17}$$

$$G_m = \frac{K}{\sqrt{2}}(V_B - V_{SS} - 2V_{th}) \tag{3.18}$$

$$V_Z = I_Z.Z_Z \tag{3.19}$$

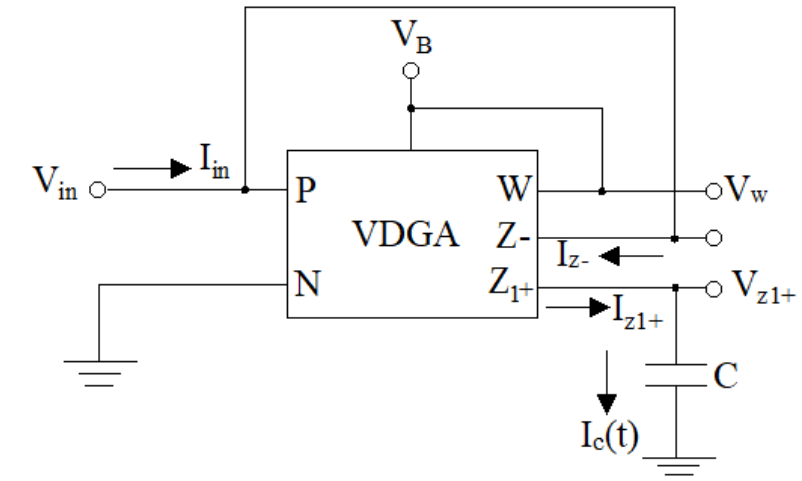
$$V_W = \beta V_Z \tag{3.20}$$

where $K = \mu_n C_{ox} \frac{W}{L}$ that depends on technology parameters, and β is the gain.
The VDGA implemented using CMOS technology can be seen in Fig. 3.8.

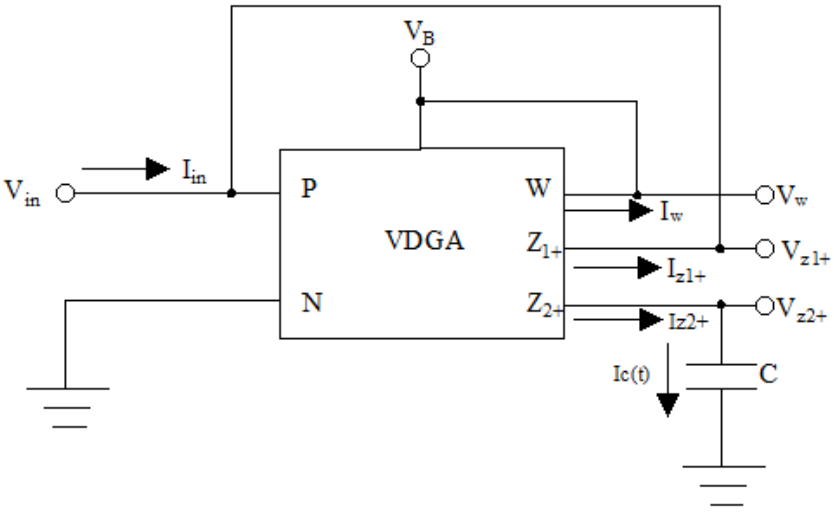
3.3.2 Working principle of proposed memristor emulators

In the proposed configurations of the memristor emulator (MRE) utilizing VDGA, the resistor is realized through the VDGA's input terminals 'P' and 'N' and output terminals 'Z+' and 'Z-'. A capacitor, functioning as a memory element, is connected to one of the output terminals and the voltage across the capacitor is transferred to the 'W' terminal of the VDGA. This 'W' terminal is then connected to the bias terminal (V_B) of the VDGA, thereby adjusting the memristance of the MRE.

The proposed electronically tunable G-MREs and F-MREs are implemented in both decremental and incremental configurations, as depicted in Figs. 3.9 (a) and (b), with the input terminal 'N' grounded. In the decremental configuration shown in Fig. 3.9 (a), the 'P' terminal is connected to the 'Z-' terminal, while the capacitor is connected to the 'Z_{1+}' terminal of the VDGA. In contrast, in the incremental configuration illustrated in Fig. 3.9 (b), the 'P' terminal is connected to the 'Z_{1+}' terminal, and the capacitor is connected to the 'Z_{2+}' terminal of the VDGA. In both cases, the voltage 'Vw' modulates the bias voltage (V_B) of the VDGA, which in turn controls the transconductance gain of the VDGA.



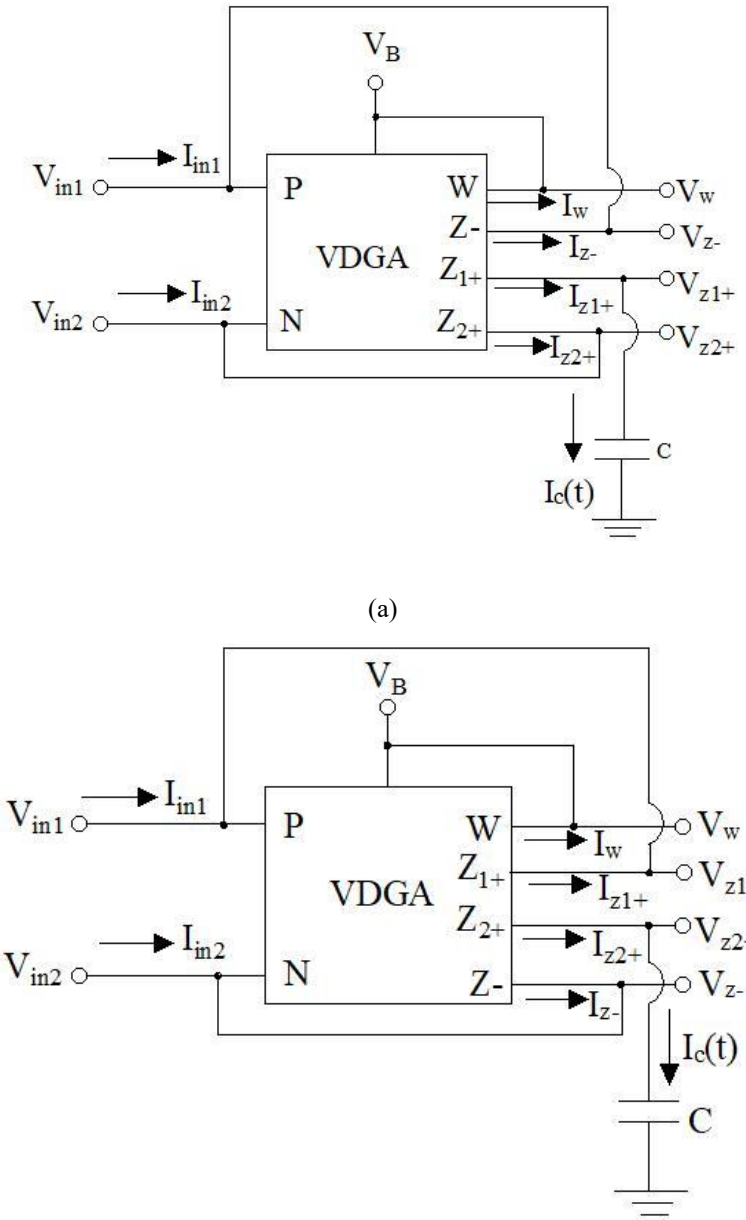
(a)



(b)

Fig. 3.9 Proposed G-MREs based on VDGA (a) decremental (b) incremental.

As shown in the Figs. 3.10 (a) and (b), the proposed F-MREs have been realized in decremental and incremental arrangements. In these arrangements, different voltages (V_{in1} and V_{in2}) are applied to the VDGA's input terminals 'P' and 'N', with a capacitor connected to the 'Z_{1+}' terminal of the VDGA. The voltage 'V_w' regulates the bias voltage 'V_B' in both configurations. In the decremental configuration shown in Fig. 3.10 (a), the 'Z-' terminal is connected to the 'P' terminal, and the 'Z_{2+}' terminal is connected to the 'N' terminal of the VDGA. Conversely, in the incremental configuration depicted in Fig. 3.10 (b), the 'Z_{2+}' terminal is connected to the 'P' terminal, and the 'Z-' terminal is connected to the 'N' terminal of the VDGA.



(a)

(b)

Fig. 3.10 Proposed F-MREs based on VDGA (a) decremental (b) incremental.

3.3.3 Mathematical analysis of proposed memristor emulators

This section includes the mathematical analysis of the suggested MRE using VDGA. Analyzing the proposed MRE of Fig. 3.9 (a), the following Equations are obtained.

$$I_{in}(t) = I_{z-} = G_m V_{in}(t) \tag{3.21}$$

$$I_C(t) = I_{z+} = G_m V_{in}(t) \tag{3.22}$$

$$V_{z+} = I_{Z+} \times \frac{1}{sC} = \frac{1}{C}\int I_c\,(t)dt = \frac{1}{C}\int G_m\, V_{in}(t)dt \tag{3.23}$$

The bias voltage V_B is given

$$V_B = \frac{1}{C}\int I_c\,(t)dt = \frac{1}{C}\int G_m V_{in}\,(t)dt = G_m\frac{\phi_{in}}{C} \tag{3.24}$$

where, $\phi_{in} = \int V_{in}\,(t)dt$ is the total flux obtained by the memristor.

The transconductance gain (Gm) can be determined by considering Equations (3.19) and (3.24) as

$$G_m = -\frac{\frac{K}{\sqrt{2}}(V_{SS} + 2V_{th})}{(1 - \frac{K}{\sqrt{2}}\frac{\phi_{in}}{C})} \tag{3.25}$$

From Equations (3.21) and (3.25), we get the value of memristance as

$$M(\phi_m) = \frac{V_{in}(t)}{I_{in}(t)} = \frac{1}{G_m} = -\frac{(1 - \frac{k}{\sqrt{2}}\frac{\phi_{in}}{C})}{\frac{K}{\sqrt{2}}(V_{SS} + 2V_{th})} \tag{3.26}$$

The expression for memristance of Equation. (3.26) can be rearranged as

$$M(\phi_m) = -\frac{1}{\frac{K}{\sqrt{2}}(V_{SS} + 2V_{th})} + \frac{\phi_{in}}{C(V_{SS} + 2V_{th})} \tag{3.27}$$

The memristance of incremental configuration as seen in Fig. 3.9(b) can be obtained as

$$M(\phi_m) = -\frac{1}{\frac{K}{\sqrt{2}}(V_{SS} + 2V_{th})} - \frac{\phi_{in}}{C(V_{SS} + 2V_{th})} \tag{3.28}$$

$\longleftarrow$ Fixed part $\longrightarrow\!\!\longleftarrow$ Variable part $\longrightarrow$

When sinusoidal signal $A_m \sin\omega t$ is applied to the proposed electronically tunable MREs of Fig. 3.9 (a) and (b), the expression of flux (ϕ) is obtained by the relation $\phi_{in} = \int V_{in}\,(t)dt$ as

$$\phi_{in}(t) = \frac{A_m}{\omega}\cos\left(\omega t - \frac{\pi}{2}\right) \tag{3.29}$$

where, A_m is amplitude and ω is the angular frequency.

Replacing the value of ϕ_{in} from Equation. (3.29) to Equation. (3.27) and (3.28), the value of memristance is obtained as

$$M(\phi_m) = -\frac{1}{\frac{K}{\sqrt{2}}(V_{SS} + 2V_{th})} \pm \frac{A_m \cos\left(\omega t - \frac{\pi}{2}\right)}{\omega C(V_{SS} + 2V_{th})} \tag{3.30}$$

where negative and positive signs in the variable parts of Equation. (3.30) refer to the memristances of decremental and incremental MRE configurations, respectively that can be varied by changing the amplitude and frequency of the input signal. The non-ideal analysis of proposed MRE using VDGA has been discussed in appendix B.5.

3.4 Proposed memristor emulators using FB-VDBA

The proposed designs of memristor emulators (MREs) using a fully-balanced voltage differencing buffered amplifier (FB-VDBA) are discussed in this section. The proposed G-MREs and F-MREs have been realized using a FB-VDBA and a grounded capacitor. The decremental and incremental configurations of G-MREs and F-MREs have been obtained by slightly modifying the circuit. In the subsequent subsection, the terminal characteristics of FB-VDBA and its CMOS circuit diagram is given.

3.4.1 Description of fully balanced voltage differencing buffered amplifier

The fully balanced voltage differencing buffered amplifier (FB-VDBA) is a six-terminal analog building block, out of which two are input terminals, two are intermediate terminals, and the remaining two are output terminals, as depicted in Fig. 3.11. Input voltages V_P and V_N are applied to terminals ‘p’ and ‘n’. The transconductance amplifier converts these voltages into currents (I_{z+} and I_{z-}) at z+ and z- terminals, respectively, as given in Equation (3.31). The voltages V_{z+} and V_{z-} are obtained by connecting z_{z+} and z_{z-} impedances to the terminals ‘z+’ and ‘z-’ respectively as given in Equation (3.32). Two inverted buffers copy these voltages to ‘w-’ and ‘w+’ terminals of FB-VDBA as given in Equation (3.33). Using Equation. (3.34), the transconductance gain (Gm) of FB-VDBA can be adjusted by adjusting the bias voltage (V_B). Fig. 3.12 depicts the internal circuit of the voltage-tunable FB-VDBA which has been obtained by modifying the conventional design of FB-VDBA [207]. The non-ideal description of FB-VDBA has been presented in appendix A.5.

The terminal characteristics of FB-VDBA are given as

$$I_{z+} = G_m(V_P - V_N), \quad I_{z-} = -G_m(V_P - V_N), \tag{3.31}$$

$$V_{z+} = I_{z+}.Z_{z+}, V_{z-} = -I_{z-}.Z_{z-} \tag{3.32}$$

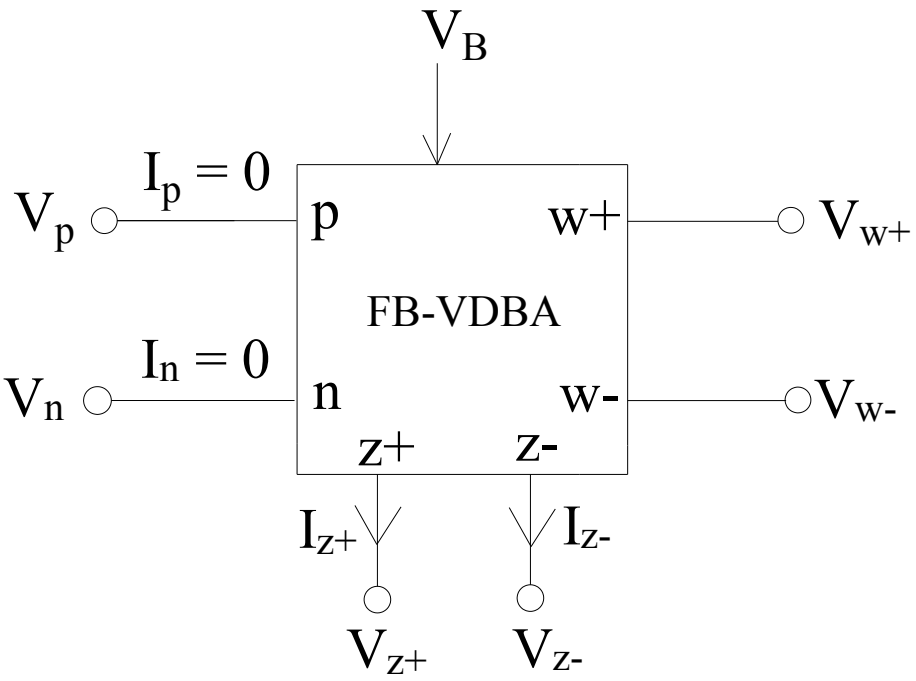


Fig. 3.11 Symbol of voltage-tunable FB-VDBA [207].

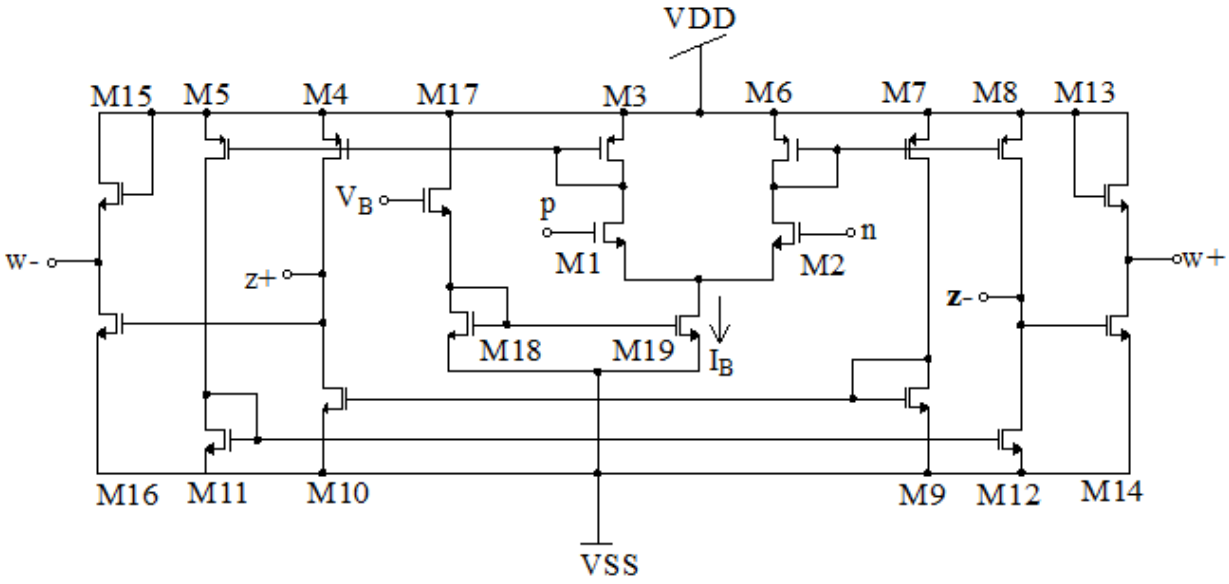


Fig. 3.12 Modified CMOS implementation of voltage-tunable FB-VDBA.

$$V_{w-} = -V_{z+} \ , V_{w+} = -V_{z-} \tag{3.33}$$

$$G_m = \frac{k}{\sqrt{2}}\left(V_B - V_{SS} - 2V_{th}\right) \tag{3.34}$$

3.4.2 Working of proposed memristor emulators

In memristor emulator (MRE), the resistance is changed according to the past history of the system. In FB-VDBA based G-MREs, resistor has been formed by connecting the output terminal 'Z-' of FB-VDBA to its input terminal 'p' while the other input terminal 'n' is grounded as shown in Fig. 3.13. By following the similar approach, resistor has been formed by connecting the output terminals 'z_{2+}' and 'z_{-}' of FB-VDBA to its input terminals 'n' and 'p' respectively as shown in Fig. 3.14. The capacitor C is connected to one of the 'Z' terminals of FB-VDBA which acts as a memory element. The voltage across capacitor (C) is copied to the 'w-' terminal of FB-VDBA.

The terminal 'w-' is connected to the bias terminal V_B which finally controls the transconductance (Gm) of FB-VDBA. Therefore, the memristance (M_R) of proposed MRE is controlled by changing the transconductance (Gm) of the FB-VDBA. The incremental configuration of G-MREs is obtained when terminals 'a' and 'c' are connected to terminals 'd' and 'b', respectively, while decremental G-MREs is obtained when terminals 'a' and 'c' are connected to terminals 'b' and 'd', respectively as shown in Fig. 3.13.

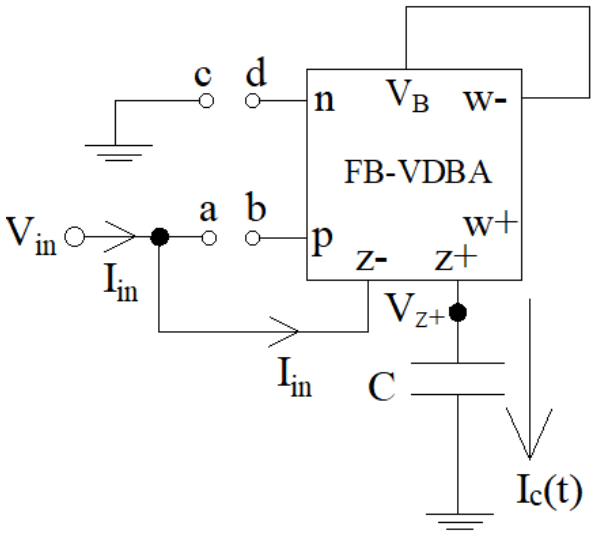


Fig. 3.13 Proposed decremental and incremental G-MREs s based on FB-VDBA.

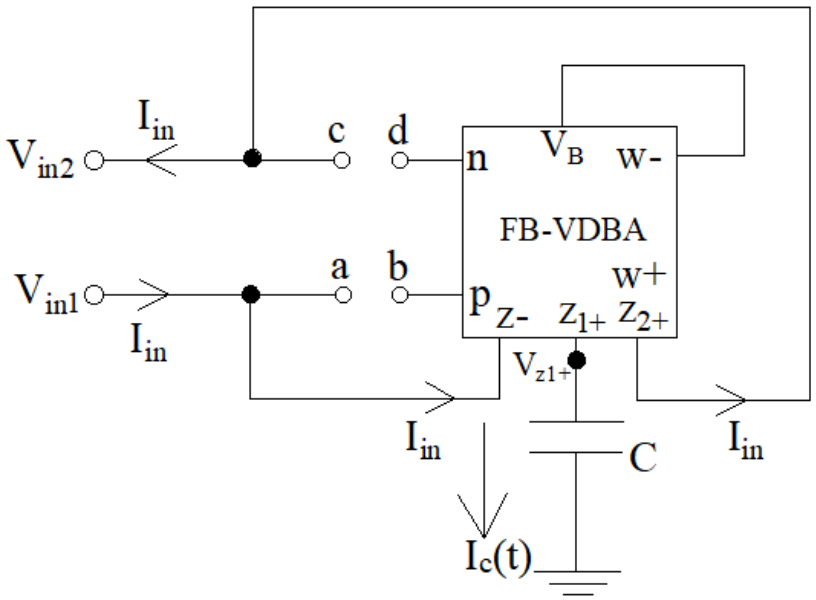


Fig. 3.14 Proposed decremental and incremental F-MREs based on FB-VDBA.

Fig. 3.14 depicts the realization of decremental/incremental F-MREs using FB-VDBA. When terminals 'a' and 'c' are connected to terminals 'b' and 'd', respectively, the decremental MRE circuit is realized. Conversely, the incremental F-MREs circuit is realized when terminals 'a' and 'c' are connected to terminals 'd' and 'b' respectively. Different voltages V_{in1} and V_{in2} are applied to decremental and incremental F-MREs circuits.

3.4.3 Mathematical analysis of proposed memristor emulators

The routine analysis of Fig. 3.14 yields the following equations:

$$I_{in} = I_{z-} = G_m(V_{in1} - V_{in2}) = G_m V_{in} \tag{3.35}$$

$$I_c(t) = I_{z1+} = G_m V_{in} \tag{3.36}$$

$$V_{w-} = -V_{z+} = V_B = -\frac{1}{C}\int I_c(t)dt \tag{3.37}$$

Using Equations. (3.36) and (3.37), we obtain

$$V_{w-} = V_B = -\frac{1}{C}\int G_m V_{in}(t)dt = -\frac{G_m \phi_{in}}{C} \tag{3.38}$$

where ϕin is the total flux measured in the proposed MRE circuit.

Equation (3.39) provides the flux (ϕ) of the proposed MRE circuit.

$$\phi_{in} = \int V_{in}(t)dt \tag{3.39}$$

The transconductance (Gm) is obtained after solving Equations (3.34) and (3.38) as

$$G_m = -\frac{\frac{k}{\sqrt{2}}(V_{ss} + 2V_{th})}{1 + \frac{k}{\sqrt{2}}\frac{\phi_{in}}{C}} \tag{3.40}$$

The memristance M (ϕ) is achieved after replacing the value of Equation (3.40) into Equation (3.35) as

$$M(\phi) = \frac{V_{in}}{I_{in}} = \frac{1}{G_m} = -\frac{1}{\frac{k}{\sqrt{2}}(V_{ss} + 2V_{th})} - \frac{\phi_{in}}{C(V_{ss} + 2V_{th})} \tag{3.41}$$

$\leftarrow$ Fixed part $\rightarrow\leftarrow$ Variable part $\rightarrow$

It is observed from Equation (3.41) that the memristanace has two parts: fixed and variable. The variable part gets subtracted from the fixed part, and therefore, it represents the memristance of the decremental G-MREs (FB-VDBA) circuit. The value of memristance depends on the amount of flux (ϕ) and capacitor value. Similarly, the memristance of the incremental MRE circuit is represented by Equation (3.42), in which a variable part is added to the fixed part.

$$M(\phi) = \frac{V_{in}}{I_{in}} = \frac{1}{G_m} = -\frac{1}{\frac{k}{\sqrt{2}}(V_{ss} + 2V_{th})} + \frac{\phi_{in}}{C(V_{ss} + 2V_{th})} \tag{3.42}$$

$\leftarrow$ Fixed part $\rightarrow\leftarrow$ Variable part $\rightarrow$

After applying a sinusoidal signal $V_m \sin \omega t$ to the input terminal of the G-MREs flux (ϕ) is obtained as

$$\phi_{in} = \frac{V_m}{\omega}\cos\left(\omega t - \frac{\pi}{2}\right) \tag{3.43}$$

where V_m is the amplitude of the sinusoidal input signal, and ω represents the frequency. The value of flux (ϕ) obtained from Equation (3.43) is substituted into Equations (3.41) and (3.42), which leads to

$$M(\phi) = \frac{V_{in2} - V_{in1}}{I_{in}} = \frac{1}{G_m} = -\frac{1}{\frac{k}{\sqrt{2}}(V_{ss} + 2V_{th})} \mp \frac{V_m \cos\left(\omega t - \frac{\pi}{2}\right)}{\omega C(V_{ss} + 2V_{th})} \tag{3.44}$$

$\leftarrow$ Fixed part $\rightarrow\leftarrow$ Variable part $\rightarrow$

From Equation (3.44), it is observed that the value of memristance varies with a change in amplitude and frequency for the applied signal of proposed decremental and incremental F-MREs (FB-VDBA) circuits. It is also controlled by changing the value of capacitors. The non-ideal analysis of proposed MREs using FB-VDBA has been presented in appendix A.4.

3.5 Conclusions

Three MRE circuits have been proposed in this chapter. The first MRE circuit is realized using operational transconductance amplifier (OTA) and current differencing buffered amplifier (CDBA). In the second MRE, voltage differencing gain amplifier (VDGA) has been employed whereas third MRE has been realized using fully balanced voltage differencing buffered amplifier (FB-VDBA). In all configurations of MRE, a grounded capacitor is used. The mathematical analysis of three emulators have been presented. The grounded and floating configurations of MREs in incremental and decremental modes have been suggested. The OTA and CDBA based MRE provide smooth control over the parameters of memristor due to usage of buffer in the design. The VDGA based MRE provides an additional feature of adjusting the gain while FB-VDBA based MRE is compact in design and also offers the smooth control over the parameters of memristor.

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CHAPTER 4

PROPOSED MEMINDUCTOR EMULATORS USING ANALOG BUILDING BLOCKS

4.1 Introduction

The memristor, memcapacitor, and meminductor are novel fundamental circuit elements whose characteristics are determined by the past conditions of the devices. The first element of mem-element family is the memristor. It became popular due to its unique feature and a wide range of applications spanning from memory to neuromorphic computing. The researchers and engineers got motivated to explore the realm of mem-elements further. Inspired by the memristor, they expanded their investigation to include the memcapacitor and meminductor. These elements are considered as extensions of memristor. They discovered that the behavior of the memcapacitor is associated with the charge and voltage whereas the behaviour of meminductor is related to the flux and current. Researchers successfully demonstrated the presence of a pinched hysteresis curve in the meminductor and memcapacitors, indicating its mem-state or memory-like nature. This observation aligns with the definition applied to the realization of memristors. Like memristive devices, memcapacitive and meminductive devices also have information storage capabilities. This feature can reduce power usage in large-scale energy-efficient neuromorphic computing systems, which imitate the brain's operation. Because of their memory-like behavior, these devices can help to create effective and adaptable neural networks. Furthermore, they can find applications in signal processing tasks where their ability to remember past signals can be helpful. This includes functions like filtering, amplification, and modulation. In summary, meminductors and memcapacitors offer a wide range of potential usage across various fields. Their distinct functionalities can potentially improve electronic systems' performance and efficiency. Following the initial development of SPICE models for meminductors and memcapacitors, subsequent efforts focused on creating meminductor emulator (MIE) and memcapacitor emulator (MCE) circuits. The first SPICE model of a mem-element system was developed by Dalibor Biolek et al. in 2009 [208]. In 2011, Dalibor Biolek et al. advanced this work by implementing a PSPICE model for flux-controlled and current-controlled MIE [209]. Additionally, Hui Wang et al. in 2013 reported a MIE using memristor [210]. Various

MIEs/ MCEs have been discussed in the literature survey. In conclusion, MIEs and MCEs play a crucial role in investigating meminductors' possible applications in many extents of science and engineering. However, the complexity associated with the design of MIE has been acknowledged as a limitation in the literature. To mitigate this issue, proposed MIEs have been designed to simplify the overall design process. Unlike previous structures that heavily relied on many analog building blocks and passive elements, the suggested emulators utilize only two or three analog building blocks, resulting in a more straightforward design. Moreover, electronic tunability is provided in the proposed design of MIEs whereas many existing designs lack this feature. Although some designs in the literature have utilized memristors, the proposed MIEs does not incorporate them. Additionally, while many existing circuits have been designed with high-power supply, and others have limitations in their frequency range (operating only in the Hz or kHz range), the proposed emulators aim to address these drawbacks observed in the literature survey. In summary, the proposed MIEs have been customized to overcome the challenges identified in the existing designs, offering simplified structures and improved performance.

In this chapter, three distinct circuits of MIE utilizing two analog building blocks and two grounded capacitors have been introduced. The operational transconductance amplifier (OTA) and current differencing buffered amplifier (CDBA) have been used to design the first MIE circuit. The second MIE circuit is designed using voltage differencing gain amplifier (VDGA) and CDBA, whereas the third MIE is designed using voltage differencing transconductance amplifier (VDTA) and CDBA. The CDBA block has been used in all three configurations of MIEs to manage incremental/decremental mode of operation. All three MIEs were designed with minimal passive components and typically two grounded capacitors. These proposed MIEs offer several improved performance parameters, including a more comprehensive wide frequency range and low supply voltage requirement. Furthermore, the performance of the proposed MIEs has been validated through various applications. The chapter is organized as follows: Section 4.2 delves into the circuit description of the MIE using OTA and CDBA. The mathematical analysis and functioning of the proposed G-MIEs and F-MIEs using OTA and CDBA are also covered in the same section. Moving on to Section 4.3, the circuit description of the MIE based on VDGA and CDBA is explained. This section also covers the operation of the proposed G-MIEs and F-MIEs using VDGA and CDBA. In Section 4.4, the circuit description of the MIE using VDTA and CDBA is explored. The working principle of the proposed G-MIEs and F-MIEs

based on VDTA & CDBA, and the mathematical analysis of the circuit are covered. Finally, the chapter concludes with Section 4.5, summarizing the essential findings and implications discussed.

4.2 Proposed meminductor emulators using OTA and CDBA

This section examines the proposed meminductor emulators (MIEs) that utilize operational transconductance amplifiers (OTAs), a current differencing buffered amplifier (CDBA), and two grounded capacitors. It provides an overview of the operation and mathematical analysis of these MIEs. The design allows for both grounded and floating implementations, which are suitable for incremental and decremental arrangements. In the proposed MIE that employs OTAs and CDBA, the voltage-tunable inductor is realized using two OTAs with transconductance gains Gm_1 and Gm_2, along with a capacitor C_1, as illustrated in Fig. 4.1. An additional capacitor C_2 functions as a memory element by storing charge. The combination of the two transconductances (Gm_1 and Gm_2) with capacitor C_1 forms a gyrator circuit. The output current from the gyrator is directed to either the 'P' or 'N' terminal of the CDBA. Capacitor C_2 accumulates charge from this output current, and the voltage across C_2 is used to adjust the transconductances (Gm_1 and Gm_2) of the gyrator circuit. Consequently, the inductance of the gyrator varies based on the previous state (the voltage across C_2) of the circuit, implementing the memory effect in the proposed MIE circuit.

Fig. 4.1 depicts the grounded configuration for decremental and incremental MIEs. The output terminals 'X_{2-}' and 'X_{2+}' of OTA-2 are connected to the input terminals '+' and '-' of OTA-1. One output terminal of OTA-1 is linked to the 'P' or 'N' terminals of the CDBA, while another terminal (X_{1-}) connects to one of the input terminals '+' of OTA-2. Capacitor C_1 is placed between the transconductors to form the gyrator circuit. Capacitor C_2 is connected to the 'z' terminal of the CDBA. The CDBA's terminal characteristics allow current to flow to the 'z' terminal, which charges capacitor C_2. The voltage across C_2 is then transferred to the 'w' terminal of the CDBA, which is linked to the bias voltage (V_B) of the transconductors. This process changes the meminductance (M_L) based on the device's historical state. The decremental and incremental configurations are achieved by switching the 'P' and 'N' terminals of the CDBA. Fig. 4.2 illustrates a floating MIE based on OTA and CDBA, designed for both decremental and incremental operations.

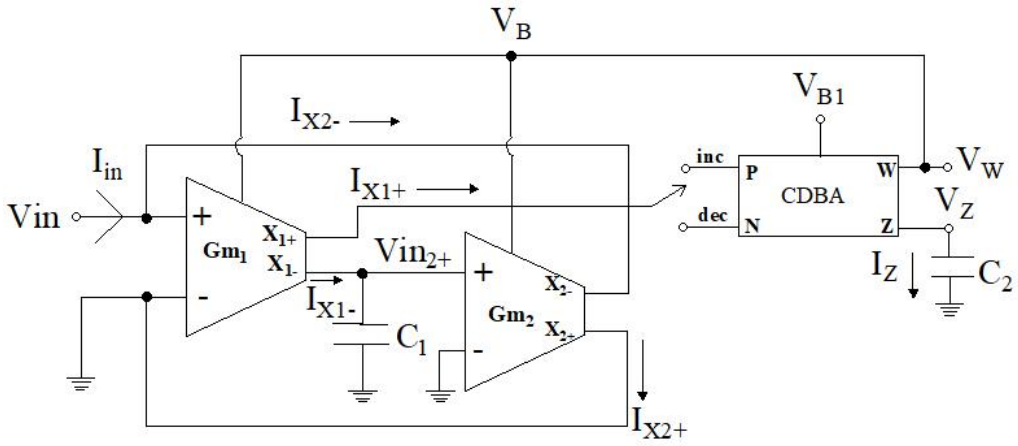

Fig. 4.1 Proposed G-MIE using OTA and CDBA.

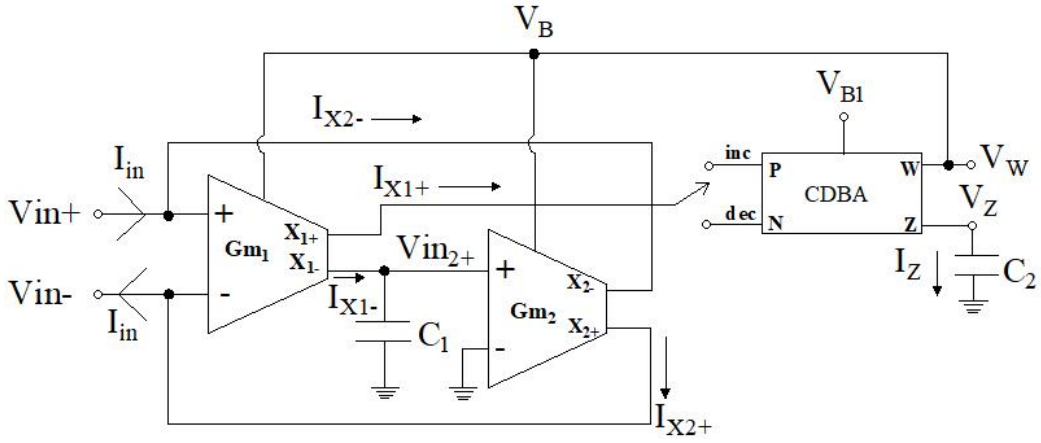

Fig. 4.2 Proposed F-MIE using OTA and CDBA.

The setup shown in Fig. 4.2 is similar to the one in Fig. 4.1, with the primary difference being the voltages applied at the OTAs' positive and negative terminals, denoted as 'V_{in+}' and 'V_{in-}', respectively. In the emulator design presented in Fig. 4.1, the negative terminal of OTA-1 is grounded. Conversely, in Fig. 4.2, which illustrates the proposed floating MIE (F-MIE), the negative terminal of OTA-1 is connected to the voltage 'V_{in-}'.

4.2.1 Mathematical analysis of proposed meminductor emulators

This section introduces the numerical analysis of the proposed meminductor emulators (MIEs) based on OTA and CDBA. Theoretical investigation of the circuit illustrated in Fig. 4.2 results in deriving the following Equations.

$$I_{X+} = G_m(V_{in+} - V_{in-}) \text{ and } I_{X-} = -G_m(V_{in+} - V_{in-}) \tag{4.1}$$

$$I_{X1+} = G_{m1}V_{in} \tag{4.2}$$

$$I_{X1-} = -G_{m1}V_{in} \tag{4.3}$$

$$I_{X2-} = I_{in} = G_{m2}V_{in2+} \tag{4.4}$$

The voltage V_{in2+} represents the voltage across capacitor C_1, and may be expressed as

$$V_{in2+} = \frac{1}{C_1}\int I_{X1-}\, dt \tag{4.5}$$

Finding the value of I_{X1-} from Equation (4.3) and substituting it in Equation (4.5) yields

$$V_{in2+} = \frac{1}{C_1}\int -G_{m1}V_{in}dt \tag{4.6}$$

$$V_{in2+} = -\frac{1}{C_1}G_{m1}\phi(t) \tag{4.7}$$

where $\int V_{in}dt = \phi(t)$ is the flux of proposed MIE.

The input current (I_{in}) is obtained in Equation (4.8) with the help of Equations (4.4) and (4.7).

$$I_{in} = -\frac{G_{m1}G_{m2}}{C_1}\,\phi(t) \tag{4.8}$$

Both OTAs' bias voltages (V_B) are the same, as seen in Fig. 4.1. Therefore, the transconductances (Gm_1 and Gm_2) of both OTAs are equal. Substituting $Gm_1 = Gm_2 = Gm$ into Equation (4.8) results into

$$I_{in} = -\frac{G_m^2}{C_1}\,\phi(t) \tag{4.9}$$

The current I (t) and flux ϕ (t) are corelated with inverse meminductance (M_L^{-1}) as

$$I(t) = M_L^{-1}\phi(t) \tag{4.10}$$

Thus, by comparing Equation (4.9) and (4.10), the value of inverse meminductance is obtained as

$$M_L^{-1} = -\frac{G_m^2}{C_1} \tag{4.11}$$

Rearranging Equation (4.11) will cause the meminductance value to be

$$M_L = -\frac{C_1}{G_m^2} \tag{4.12}$$

The voltage across capacitor (C_2) is obtained as

$$V_Z = \frac{1}{C_2}\int I_z\,(t)dt \tag{4.13}$$

It is simple to determine the value of current (Iz) using the CDBA terminal equations as

$$I_Z(t) = I_P = I_{X1+} = G_m V_{in} \tag{4.14}$$

The result of swapping in the value of current Iz (t) from Equation (4.13) into Equation (4.14), we get

$$V_Z = \frac{1}{C_2}\int G_m V_{in}\,dt \tag{4.15}$$

The voltage Vz is replicated to the CDBA's 'W' terminal using an internal buffer. Thus, the voltage Vw can be written as

$$V_W = V_B = \frac{1}{C_2}\int G_m V_{in}\,dt = \frac{G_m}{C_2}\phi_{in} \tag{4.16}$$

After inserting value of bias voltage V_B from Equation (4.16) to Equation (3.10), the transconductance (Gm) value is obtained as

$$G_m = \frac{-\frac{\mu_n C_{ox}}{\sqrt{2}}(V_{SS} + 2V_{th})}{1 - \frac{\mu_n C_{ox}}{\sqrt{2}}\frac{\phi_{in}}{C_2}} \tag{4.17}$$

Equation (4.11) is obtained by inserting the value of Gm from Equation (4.17).

$$M_L^{-1} = -\frac{\left[\frac{-\frac{\mu_n C_{ox}}{\sqrt{2}}(V_{SS} + 2V_{th})}{1 - \frac{\mu_n C_{ox}}{\sqrt{2}}\frac{\phi_{in}}{C_2}}\right]^2}{C_1} \tag{4.18}$$

Upon decomposing Equation (4.18), the value of meminductance (M_L) can be acquired as

$$M_L = -\frac{C_1\left[1-\frac{\mu_n C_{ox}}{\sqrt{2}}\frac{\phi_{in}}{C_2}\right]^2}{\frac{(\mu_n C_{ox})^2}{2}(V_{SS}+2V_{th})^2} \tag{4.19}$$

The value of meminductance (M_L) for a decremental meminductor can be obtained by rearranging the terms in Equation (4.19).

$$M_L = -\frac{2C_1}{(\mu_n C_{ox})^2(V_{SS}+2V_{th})^2} - \frac{2C_1\phi_{in}\left[\frac{\mu_n C_{ox}\phi_{in}}{2C_2}-\sqrt{2}\right]}{\mu_n C_{ox}C_2(V_{SS}+2V_{th})^2} \tag{4.20}$$

←Fixed part→ ←Variable part→

Similarly, the value of meminductance (M_L) for an incremental meminductor is determined as follows after switching the connections at the CDBA's input terminals from 'P' to 'N'.

$$M_L = \frac{2C_1}{(\mu_n C_{ox})^2(V_{SS}+2V_{th})^2} + \frac{2C_1\phi_{in}\left[\frac{\mu_n C_{ox}\phi_{in}}{2C_2}-\sqrt{2}\right]}{\mu_n C_{ox}C_2(V_{SS}+2V_{th})^2} \tag{4.21}$$

←Fixed part→ ←Variable part→

It is clear from Equations (4.20) and (4.21) that the first term of meminductance is constant, but the second term varies since it depends on flux. The terms in Equation (4.20) and Equation (4.21) indicate the meminductances (M_L) of incremental and decremental MIEs, respectively. The non-ideal analysis of proposed MIE using OTA and CDBA is presented in appendix B.5.

4.3 Proposed meminductor emulators using VDGA and CDBA

This section delves into the proposed meminductor emulators (MIEs) employing VDGA and CDBA. Furthermore, it discusses the functioning and mathematical analysis of the proposed MIEs. Moreover, the circuitry facilitates the realization of grounded and floating implementations, which are easily achieved for incremental and decremental configurations. In the proposed configuration of MIE, the VDGA and capacitor (C_1) are used to realize an inductor circuit while capacitor (C_2) acts as a memory element. The voltage across capacitor (C_2) is used to regulate the bias voltage (V_B) of the VDGA. This bias voltage (V_B) in turn

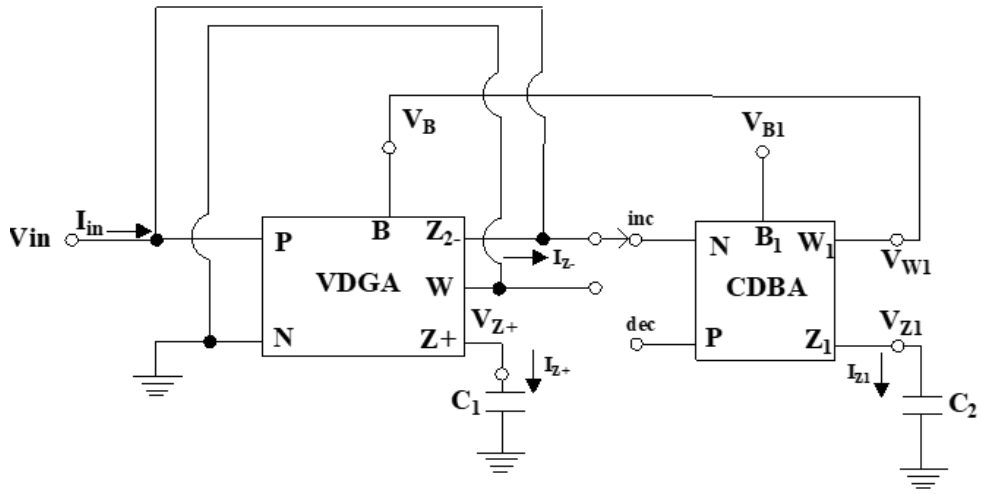

Fig. 4.3 Proposed G-MIE using VDGA and CDBA.

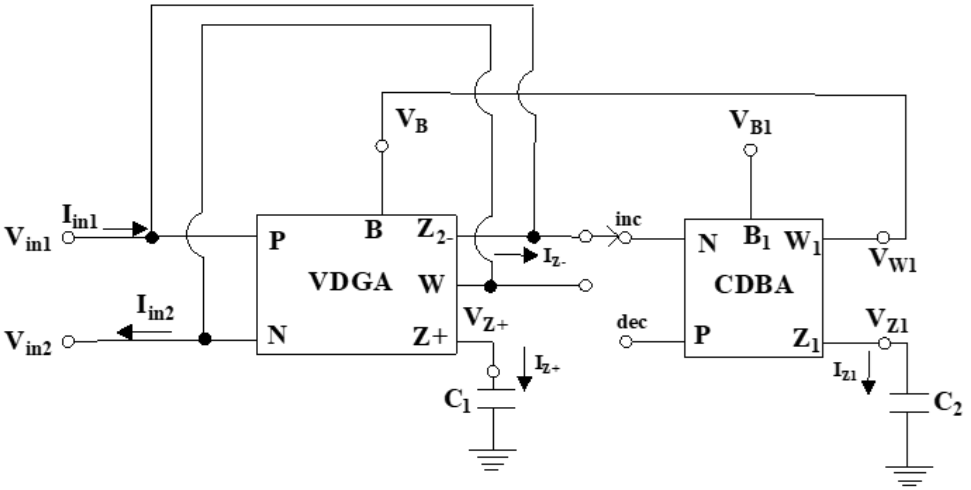

Fig. 4.4 Proposed F-MIE using VDGA and CDBA.

adjusts the transconductance (Gm_1). By varying the transconductance within the circuit, the inductance can be modified. As a result, the inductance of the circuit is influenced by its prior state, which is why this variation in inductance is termed meminductance (M_L).

In the grounded decremental MIE suggested in Fig. 4.3, intermediate terminal 'Z_{2-}' of the VDGA is associated to the input terminal 'P. The input voltage (Vin) is applied to 'P' terminal of VDGA while the 'N' terminal is kept at ground. The capacitor, C_1 is attached to the intermediate terminal 'Z+' of VDGA, while the other capacitor (C_2) is connected to the "Z_1" terminal of CDBA. Notably, the system's previous charge is stored in capacitor C_2 and voltage developed across capacitor is utilized to change the transconductance of VDGA

which results in change of meminductance (M_L) of proposed MIE. The voltage across the 'Z_1' terminal of CDBA is copied to the 'W_1' terminal, which is directly connected to the 'B' terminal of VDGA. The voltage 'V_B' at the 'B' terminal adjusts the transconductance gain (Gm_1) of VDGA. The summation of input currents (I_{in} + I_{z2-}) traverses through the input terminals 'P' or 'N' of CDBA, thereby realizing either incremental or decremental MIEs, respectively. This current subsequently flows through the 'Z_1' terminal of CDBA, leading to the charging of capacitor C_2. Fig. 4.4 shows the design of proposed floating incremental/decremental MIE that uses VDGA and CDBA. The input voltages V_{in1} and V_{in2} are applied to 'P' and 'N' terminals of VDGA. The capacitor C_1 is connected to the intermediate terminal 'Z+' of VDGA while capacitor C_2 is connected to 'Z_1' terminal of CDBA. The decremental and incremental MIEs are easily realized by connecting the input terminals 'P' or 'N' of CDBA to the intermediate terminal 'Z_{2-}' of VDGA.

4.3.1 Mathematical analysis of proposed meminductor emulators

This section presents the numerical analysis of proposed MIE based on VDGA and CDBA. The following equations have been derived on the basis of terminal characteristics of VDGA and CDBA.

$$V_{Z+} = \frac{1}{C_1}\int I_{Z+}dt = \frac{1}{C_1}\int G_{m1}V_{in}\,dt \tag{4.22}$$

where, $\int V_{in}dt = \phi_{in}(t)$, hence, Equation (4.22) can be rewritten as

$$V_{Z+} = \frac{G_{m1}}{C_1}\phi_{in}(t) \tag{4.23}$$

Equation (4.24) provides the input current (I_P) of CDBA if the 'Z_{2-}' terminal of VDGA is connected to the 'P' terminal of CDBA as depicted in Fig. 4.3. The value of current 'I_{z1}' is equal to the current 'Ip'. The values of these currents are obtained as

$$I_P = I_{Z2-} + I_{in} = I_{z1} \tag{4.24}$$

The voltage across 'Z_1' terminal of CDBA is calculated as

$$V_{Z1} = \frac{1}{C_2}\int I_{Z1}\,dt = \frac{1}{C_2}\int (I_{Z2-} + I_{in})dt \tag{4.25}$$

Substituting the value of 'I_{Z2-}' from Equation (3.17) results in

$$V_{Z1} = \frac{1}{C_2}\int (-G_{m2}V_{Z+} + I_{in})\,dt \tag{4.26}$$

Substituting the value of 'V_{Z+}' from Equation (4.23) in Equation (4.26), we get

$$V_{Z1} = \frac{1}{C_2}\int \left(-G_{m2}\frac{G_{m1}}{C_1}\phi_{in}(t) + I_{in}\right)dt \tag{4.27}$$

where, $\int \phi_{in}dt = \rho(t)$ and $\int I_{in}dt = q(t)$.

Hence, Equation (4.27) can be rewritten as Equation (4.28)

$$V_{Z1} = -\frac{G_{m1}G_{m2}}{C_1C_2}\rho(t) + \frac{q(t)}{C_2} \tag{4.28}$$

The voltages V_B, V_{W1}, and V_{z1} are obtained as

$$V_B = V_{W1} = V_{Z1} = -\frac{G_{m1}G_{m2}}{C_1C_2}\rho(t) + \frac{q(t)}{C_2} \tag{4.29}$$

Substituting the value of V_B from Equation (4.29) to Equation (3.10), we get

$$G_{m1} = K_1\left[-\frac{G_{m1}G_{m2}}{C_1C_2}\rho(t) + \frac{q(t)}{C_2} - V_{SS} - V_{th}\right] \tag{4.30}$$

From Equation (3.17) and Equation (4.23), we get

$$I_{Z-} = -G_{m2}V_{Z+} = -\frac{G_{m1}G_{m2}}{C_1}\phi_{in}(t) \tag{4.31}$$

Upon substituting the value of Gm_1 from Equation (4.30) into Equation (4.31), we obtain

$$I_{z-} = -K_1\frac{G_{m2}}{C_1}\left[-V_{SS} - V_{th} - \frac{G_{m1}G_{m2}}{C_1C_2}\rho(t) + \frac{q(t)}{C_2}\right]\phi_{in}(t) \tag{4.32}$$

The flux and current are correlated as given in Equation (4.33)

$$\phi(t) = M_L I(t) \text{ or } I(t) = M_L^{-1}\phi(t) \tag{4.33}$$

By comparing Equation (4.32) and Equation (4.33), we get

$$M_L^{-1} = K_1 \frac{G_{m2}}{C_1}\left[V_{SS} + V_{th} + \frac{G_{m1}G_{m2}}{C_1C_2}\rho(t) - \frac{q(t)}{C_2}\right] \tag{4.34}$$

The Equation (4.34) can be rearranged as

$$M_L^{-1} = K_1 \frac{G_{m2}}{C_1}(V_{SS} + V_{th}) - K_1 \frac{G_{m2}}{C_1}\left[-\frac{G_{m1}G_{m2}}{C_1C_2}\rho(t) + \frac{q(t)}{C_2}\right] \tag{4.35}$$

$$\longleftarrow \text{Fixed Term} \longrightarrow \quad \longleftarrow \text{Variable Term} \longrightarrow$$

The expression for the inverse meminductance of the grounded decremental MIE is given by Equation (4.35). The suggested MIE functions as a grounded incremental MIE when the 'Z_2-' terminal of VDGA is connected to the 'N' terminal of CDBA in Fig. (4.3). The inverse meminductance expression is modified as follows.

$$M_L^{-1} = K_1 \frac{G_{m2}}{C_1}(V_{SS} + V_{th}) + K_1 \frac{G_{m2}}{C_1}\left[-\frac{G_{m1}G_{m2}}{C_1C_2}\rho(t) + \frac{q(t)}{C_2}\right] \tag{4.36}$$

$$\longleftarrow \text{Fixed Term} \longrightarrow \longleftarrow \text{Variable Term} \longrightarrow$$

The values of meminductance obtained from Equations (4.35) and (4.36) indicate that the first term is fixed because Gm_2 of VDGA is controlled by a fixed biasing current, I_{B1}, and G_{m1} of VDGA is variable based on the bias voltage (V_B), which is connected to the voltage at capacitor C_2. The Equations (4.35) and (4.36) are combined into a single expression as given in Equation (4.37)

$$M_L = \frac{1}{K_1 \frac{G_{m2}}{C_1}(V_{SS} + V_{th})} \pm \frac{1}{K_1 \frac{G_{m2}}{C_1}\left[-\frac{G_{m1}G_{m2}}{C_1C_2}\rho(t) + \frac{q(t)}{C_2}\right]} \tag{4.37}$$

$$\longleftarrow \text{Fixed Term} \longrightarrow \longleftarrow \text{Variable Term} \longrightarrow$$

The '+' and '-' signs of Equation (4.37) indicate the expressions for grounded incremental and decremental configurations of MIE respectively. The non-ideal analysis of proposed meminductor emulator using VDGA and CDBA is presented in appendix B.6.

4.4 Proposed meminductor emulators using VDTA and CDBA

This section explores the design of proposed meminductor emulators (MIEs) employing voltage differencing transconductance amplifier (VDTA) and current differencing transconductance amplifier (CDBA). It covers the discussion and analysis of proposed MIEs. The working principle and operation of the proposed MIEs are also described. The proposed configuration allows the grounded and floating configurations in both incremental and decremental modes.

4.4.1 Description of voltage differencing transconductance amplifier

The symbol of voltage differencing transconductance amplifier **(**VDTA) is depicted in Fig. 4.5. There are seven terminals out of which 'P' and 'N' are input terminals, two are output terminals namely 'X+' and 'X-', one 'Z' terminal is the intermediate terminal, and other two terminals are 'V_B' and 'V_{B1}' for adjusting the transconductance gains g_{m1} and g_{m2} of the VDTA. According to Equation (4.38), the input terminals' high impedances cause them to draw nearly no current. Applying the differential voltage V_P -V_N between the input terminals 'P' and 'N', the first transconductor with transconductance gain 'g_{m1}' transforms it into current 'I_Z' at the 'Z' terminal, as per Equation (4.39). The voltage 'Vz' is converted into current 'Iz' by the second transconductor of the VDTA as given by Equation (4.40). Fig. 4.6 displays the CMOS circuit diagram of VDTA.

$$I_P = I_N = 0 \tag{4.38}$$

$$I_Z = g_{m1}(V_P - V_N) \tag{4.39}$$

$$I_{X\pm} = \pm g_{m2} V_Z \tag{4.40}$$

The architecture of VDTA [230] has been slightly modified making it suitable for the design of MIEs. The transconductance gains (g_{m1} and g_{m2}) of the modified architecture of VDTA can be obtained as

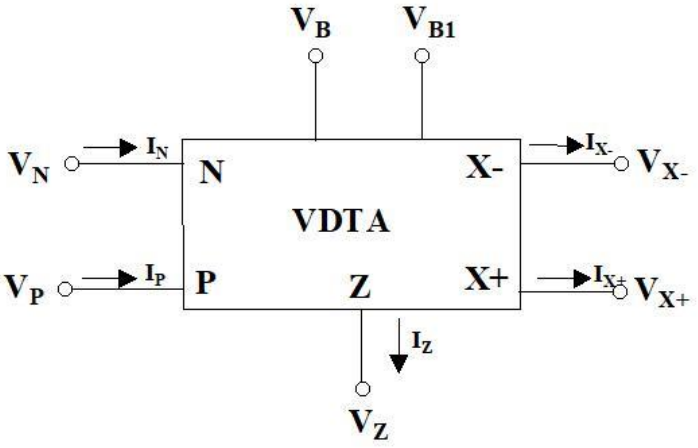

Fig. 4.5 Symbolic notation of VDTA [211].

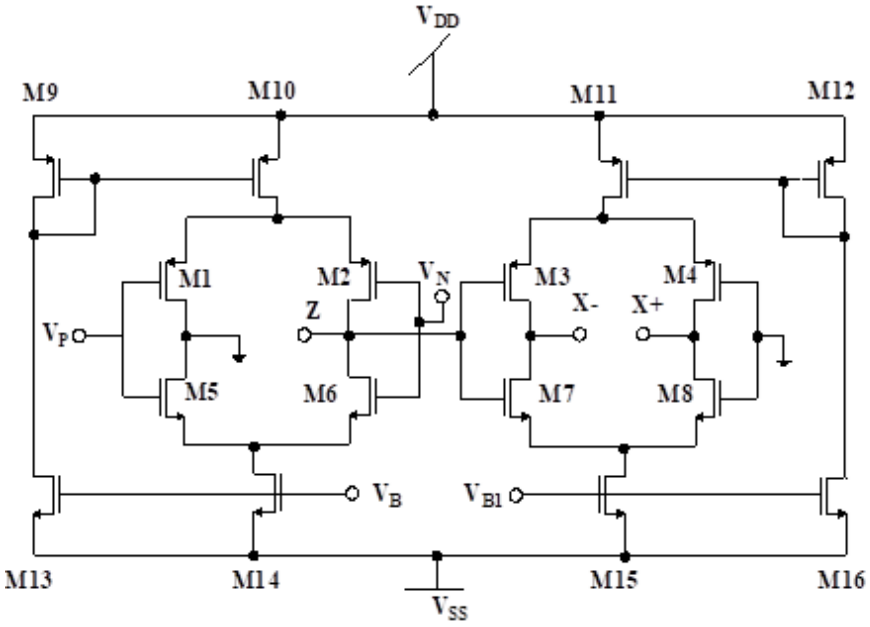

Fig. 4.6 Modified CMOS implementation of VDTA.

$$g_{m1} = \frac{g_1 g_2}{g_1 + g_2} + \frac{g_5 g_6}{g_5 + g_6} \tag{4.41}$$

$$g_{m2} = \frac{g_3 g_4}{g_3 + g_4} + \frac{g_7 g_8}{g_7 + g_8} \tag{4.42}$$

where g_i is the output transconductances of respective MOSFET and is defined as

$$g_i = \sqrt{2\mu C_{ox}\left(\frac{W}{L}\right)_i I_D} \tag{4.43}$$

The aspect ratios of MOSFET pairs (M1, M2) and (M5, M6) are assumed to be exactly equal. Therefore, their respective transconductance gains (g_1, g_2) and (g_5, g_6) are the same and thus the Equation (4.41) reduces to

$$g_{m1} = \frac{g_2 + g_5}{2} \tag{4.44}$$

Similarly, the aspect ratios of MOSFET pairs (M3, M4) and (M7, M8) are assumed to be exactly equal, and thus, their respective transconductances (g_3, g_4) & (g_7, g_8) are the same. Therefore, Equation (4.42) reduces to

$$g_{m2} = \frac{g_4 + g_7}{2} \tag{4.45}$$

From Equation (4.43), the respective transconductance gains (g_2 and g_5) of MOSFETs M2 and M5 can be written as

$$g_2 = \sqrt{2\mu C_{ox}\left(\frac{W}{L}\right)_2 I_{D2}} \tag{4.46}$$

$$g_5 = \sqrt{2\mu C_{ox}\left(\frac{W}{L}\right)_5 I_{D5}} \tag{4.47}$$

The drain current drawn by MOSFET M14 is the summation of drain currents I_{D2} and I_{D5}. Due to the symmetrical structure, the drain currents I_{D2} and I_{D5} are equally divided, and hence it leads to Equation (4.48)

$$I_{D2} = I_{D5} = \frac{I_{D14}}{2} \tag{4.48}$$

Substituting the value of Equation (4.48) into Equations (4.46) and (4.47) lead to

$$g_2 = \sqrt{\mu C_{ox}\left(\frac{W}{L}\right)_2 I_{D14}} \tag{4.49}$$

$$g_5 = \sqrt{\mu C_{ox}\left(\frac{W}{L}\right)_5 I_{D14}} \tag{4.50}$$

Substituting the values from Equations (4.49) and (4.50) into Equation (4.41) results in value of transconductance (g_{m1}) as

$$g_{m1} = \frac{\sqrt{\mu C_{ox}\left(\frac{W}{L}\right)_2} + \sqrt{\mu C_{ox}\left(\frac{W}{L}\right)_5}}{2}\sqrt{I_{D14}} \tag{4.51}$$

The drain current of MOSFET M14 operating in saturation region can be written as

$$I_{D14} = \frac{1}{2}\mu C_{ox}\left(\frac{W}{L}\right)_{14}(V_B - V_{SS} - V_{th})^2 \tag{4.52}$$

From Equations (4.51) and (4.52), the value of transconductance (g_{m1}) is obtained as

$$g_{m1} = K_1(V_B - V_{SS} - 2V_{th}) \tag{4.53}$$

$$\text{where } K_1 = \frac{\sqrt{\mu C_{ox}\left(\frac{W}{L}\right)_2} + \sqrt{\mu C_{ox}\left(\frac{W}{L}\right)_5}}{2\sqrt{2}}\sqrt{\mu C_{ox}\left(\frac{W}{L}\right)_{14}}$$

Similarly, the transconductance gain (g_{m2}) of the modified VDTA can be derived as

$$g_{m2} = K_2(V_{B1} - V_{SS} - 2V_{th}) \tag{4.54}$$

$$\text{where } K_2 = \frac{\sqrt{\mu C_{ox}\left(\frac{W}{L}\right)_4} + \sqrt{\mu C_{ox}\left(\frac{W}{L}\right)_7}}{2\sqrt{2}}\sqrt{\mu C_{ox}\left(\frac{W}{L}\right)_{15}}$$

4.4.2 Working principle of proposed meminductor emulators

Fig. 4.7 illustrates the proposed design of a decremental and incremental G-MIEs based on VDTA and CDBA. The inductor is realized using VDTA and capacitor C_1 while capacitor C_2 is used to store the charge and acts as a memory element. The CDBA is used to achieve the incremental and decremental configurations using its 'N' and 'P' terminals. For G-MIE, the 'N' terminal of VDTA is grounded while the output terminals 'X+' and 'X-' of the VDTA are connected to the input terminals 'N' and 'P', respectively. Capacitor C_1 is connected to intermediate terminal 'Z' of VDTA. Incremental or decremental MIEs can be realised by connecting the 'X-' terminal of VDTA to the 'P' or 'N' terminals of CDBA, respectively. The capacitor C_2 is connected to the 'Z_1' terminal of the CDBA which retains the charge. The 'P' or 'N' terminal of CDBA receives the current (I_{in} + I_{x-}) from VDTA. The capacitor C_2 is

charged by the input current ($I_P = I_{in} + Ix-$ or $I_N = I_{in} + Ix-$) of CDBA which also flows through its 'Z_1' terminal. The voltage developed across 'Z_1' terminal is replicated to the 'W' terminal of CDBA, which is attached to the 'V_B' terminal of VDTA. The transconductance gain (g_{m1}) of the VDTA is controlled by the voltage 'Vw'. Therefore, the meminductance of the proposed G-MIE is controlled by controlling the transconductance (g_{m1}) of VDTA.

Fig. 4.8 shows the suggested F-MIE based on VDTA and CDBA for both incremental and decremental configurations. In floating configuration, two input voltages V_{in1} and V_{in2} are applied to input terminals of VDTA while rest of the circuit remains same as in Fig 4.7.

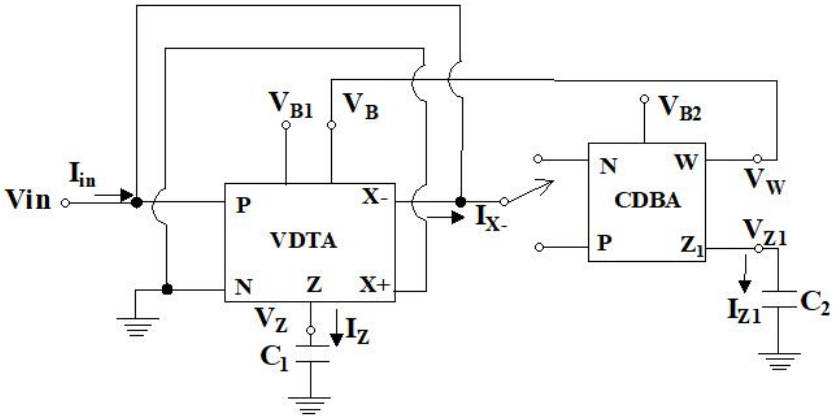

Fig.4.7 Proposed G-MIE based on VDTA and CDBA.

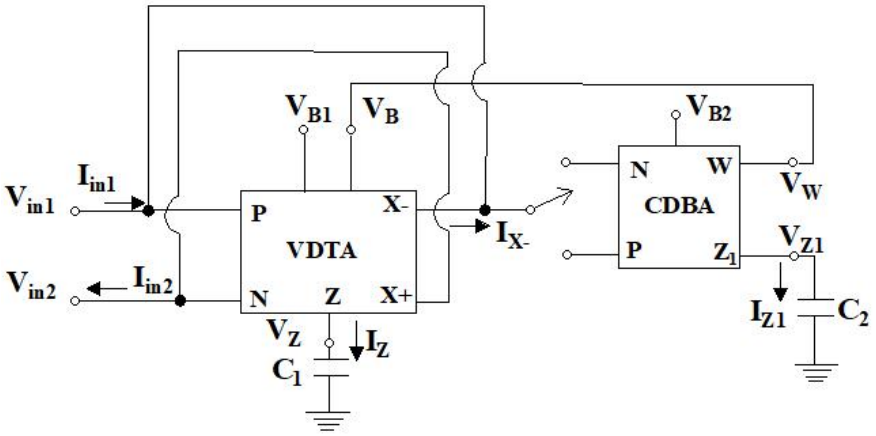

Fig. 4.8 Proposed F-MIE based on VDTA and CDBA.

4.4.3 Mathematical analysis of proposed meminductor emulators

This section covers the numerical analysis of proposed MIE based on VDTA and CDBA. The following equation have been derived for the G-MIE of Fig. 4.7 with the help of terminal characteristics of VDTA and CDBA.

$$V_Z = \frac{g_{m1}}{C_1}\phi_{in}(t) \tag{4.55}$$

$$V_Z = \frac{1}{C_1}\int I_Z dt = \frac{1}{C_1}\int g_{m1}V_{in}\,dt \tag{4.56}$$

$$V_Z = \frac{g_{m1}}{C_1}\phi_{in}(t) \tag{4.57}$$

whereas $\int V_{in}dt = \phi_{in}(t)$, Therefore, Equation (4.56) can be written as

When terminal 'X-' of VDTA is connected to the 'P' terminal of CDBA in Fig. 4.7, the current "I_{z1}" at the intermediate terminal of CDBA can be written as

$$I_{Z1} = I_P = I_{X-} + I_{in} \tag{4.58}$$

The voltage across the 'Z_1' terminal of CDBA can be written as

$$V_{Z1} = \frac{1}{C_2}\int I_{Z1}\,dt = \frac{1}{C_2}\int (I_{X-} + I_{in})dt \tag{4.59}$$

Substituting the values of current 'Ix-' and voltage 'Vz' from Equations (4.56) and (4.57) into Equation (4.59) leads to

$$V_{Z1} = \frac{1}{C_2}\int (-g_{m2}V_Z + I_{in})\,dt = \frac{1}{C_2}\int \left(-g_{m2}\frac{g_{m1}}{C_1}\phi_{in}(t) + I_{in}\right)dt \tag{4.60}$$

whereas $\int \phi_{in}dt = \rho(t)$ and $\int I_{in}dt = q(t)$.

Therefore, Equation (4.60) gets modified into Equation (4.61)

$$V_{Z1} = -\frac{g_{m1}g_{m2}}{C_1C_2}\rho(t) + \frac{q(t)}{C_2} \tag{4.61}$$

A buffer inside the CDBA copies the voltage 'V_{z1}' to the 'W' terminal. Therefore, voltage 'V_{z1}' is equal to the voltage 'Vw' as given in Equation (4.62)

$$V_B = V_W = V_{Z1} = -\frac{g_{m1}g_{m2}}{C_1C_2}\rho(t) + \frac{q(t)}{C_2} \tag{4.62}$$

After substituting the value of V_B from Equation (4.62) to Equation (3.10), we get

$$g_{m1} = K_1\left[-\frac{g_{m1}g_{m2}}{C_1C_2}\rho(t) + \frac{q(t)}{C_2} - V_{SS} - V_{th}\right] \tag{4.63}$$

With the help of Equations (4.40) and (4.57), we get

$$I_{X-} = -g_{m2}V_Z = -\frac{g_{m1}g_{m2}}{C_1}\phi_{in}(t) \tag{4.64}$$

$$I_{X-} = K_1\frac{g_{m2}}{C_1}\left[V_{SS} + V_{th} + \frac{g_{m1}g_{m2}}{C_1C_2}\rho(t) - \frac{q(t)}{C_2}\right]\phi_{in}(t) \tag{4.65}$$

The well-known relation among meminductance (M_L), current I(t), and flux ϕ (t) is given as

$$\phi(t) = M_L I(t) \tag{4.66}$$

The Equation (4.66) can be rearranged as

$$I(t) = M_L^{-1}\phi(t) \tag{4.67}$$

Comparing Equations (4.65) and (4.67) leads to the value of inverse meminductance as

$$M_L^{-1} = K_1\frac{g_{m2}}{C_1}\left[V_{SS} + V_{th} + \frac{g_{m1}g_{m2}}{C_1C_2}\rho(t) - \frac{q(t)}{C_2}\right] \tag{4.68}$$

The Equation (4.68) can be rearranged as

$$M_L^{-1} = K_1 \frac{g_{m2}}{C_1}(V_{SS} + V_{th}) + K_1 \frac{g_{m2}}{C_1}\left[\frac{g_{m1}g_{m2}}{C_1C_2}\rho(t) - \frac{q(t)}{C_2}\right] \quad (4.69)$$

When terminal 'X-' of VDTA is connected to the 'N' terminal of CDBA in Fig. (4.8), the expression for inverse meminductance is obtained as

$$M_L^{-1} = -K_1 \frac{g_{m2}}{C_1}(V_{SS} + V_{th}) - K_1 \frac{g_{m2}}{C_1}\left[\frac{g_{m1}g_{m2}}{C_1C_2}\rho(t) - \frac{q(t)}{C_2}\right] \quad (4.70)$$

It can be concluded from Equations (4.69) and (4.70) that the first term is fixed as transconductance (g_{m2}) of VDTA is controlled by a fixed bias voltage (V_{B1}), whereas transconductance (g_{m1}) is controlled by the bias voltage (V_B) that is connected to the voltage developed across capacitor C_2 (history of the system). The values of meminductances for incremental and decremental MIEs are obtained as

$$M_L = \pm\frac{1}{K_1 \frac{g_{m2}}{C_1}(V_{SS} + V_{th})} \pm \frac{1}{K_1 \frac{g_{m2}}{C_1}\left[\frac{g_{m1}g_{m2}}{C_1C_2}\rho(t) - \frac{q(t)}{C_2}\right]} \quad (4.71)$$

It is observed from Equation (4.71) that the meminductance of incremental MIE attains positive values (both fixed and variable terms are positive). In contrast, the meminductance of the decremental MIE attains negative values (both fixed and variable terms are negative). The non-ideal analysis of proposed MIE using VDTA and CDBA is presented in appendix B.7.

4.5 Conclusions

In this chapter, three distinct MIEs based on OTA-CDBA, VDGA-CDBA, and VDTA-CDBA have been realized. Each proposed MIE has undergone simulation in both grounded and floating configurations, considering both incremental and decremental modes of operation. The first MIE employs two operational transconductance amplifiers, a current differencing buffered amplifier, and two grounded capacitors. The second and third MIEs require two analog building blocks utilizing VDGA-CDBA and VDTA-CDBA along with two grounded capacitors. The connections of the proposed MIEs are straightforward as compared to the structures available in the literature. Mathematical analysis has been done to verify the proposed MIEs. Furthermore, the effectiveness of the proposed MIEs has been demonstrated through adaptive learning circuit and chaotic circuit. applications.

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CHAPTER 5

SIMULATION RESULTS OF PROPOSED MEM-ELEMENTS EMULATORS

5.1 Introduction

In this chapter, the simulation results of proposed memristor emulators (MREs) based on operational transconductance amplifier (OTA) and current differencing buffered amplifier (CDBA), voltage differencing gain amplifier (VDGA), and fully-balanced voltage differencing buffered amplifier (FB-VDBA) have been discussed. The detailed analysis of these MREs have already been covered in Chapter 3. In addition, the simulation results of proposed meminductor emulators (MIEs) based on OTA and CDBA, VDGA and CDBA, and voltage differencing transconductance amplifier (VDTA) and CDBA have also been included. The working principle and mathematical analysis of these MIEs have already been discussed in Chapter 4. The Mentor Graphics Eldo simulation tool using 180nm CMOS technology parameters has been used for simulation.

The performances of proposed mem-element emulators have been compared with existing mem-element emulators based on parameters such as range of frequency, number of analog building blocks and passive components, feature of electronic tunability, grounded/floating configurations, incremental/decremental types, memristor/memristor-less configuration, resistor/resistor-less configuration, multiplier/multiplier-less configuration, power supply, etc.

To attain the initial objective of minimizing analog building blocks (ABBs) and passive components, the proposed mem-elements have been designed with the least possible ABBs and passive components. Utilizing minimal active and passive components in a circuit provides several advantages such as cost efficiency, where reducing the component count generally results in lower manufacturing costs. Active and passive components contribute significantly to a circuit's overall cost, and minimizing their usage can be economically advantageous. Another advantage is reduced complexity; simplifying a circuit by minimizing components leads to a less intricate design, making it easier to comprehend, troubleshoot, and maintain. This approach also lowers the likelihood of errors during the design and manufacturing processes.

Furthermore, minimizing the number of components enhances reliability by reducing the potential points of failure or degradation over time. Additionally, circuits with fewer components often exhibit lower power consumption, crucial in power-sensitive applications, such as battery-powered devices or energy-efficient systems. Space savings are another benefit, as minimizing components usually results in a more compact circuit layout. This is especially important in applications with limited space, such as portable electronic devices or miniaturized systems. Moreover, circuits with fewer components are generally easier to integrate into larger systems, simplifying the overall system design and integration process. This ease of integration makes it more straightforward to incorporate the circuit into a broader electronic system. Finally, reducing the number of components can improve overall performance in some cases. This is particularly true when optimizing for speed, as a lower component count may minimize signal propagation delays and enhance the circuit's response time. The crucial aspect of mem-elements lies in analysing the pinched hysteresis loop (PHL), acting as a vital characteristic that exposes the behaviour of the mem-elements. This loop illustrates the maximum frequency range within which a mem-element circuit operates satisfactorily, aligning with the secondary objective to enhance the performance of the designed emulators in terms of the operating frequency range. The operating dynamic range of active building blocks refers to the range of input or output signals (voltage, current, or power) over which the component operates linearly and effectively, without significant distortion. This range directly impacts the performance of circuits, including memelement emulators. The pinched hysteresis loop, a defining characteristic of memelements (e.g., memristors, memcapacitors, and meminductors), represents the relationship between voltage and current (or other quantities) under periodic signals. If the input signal amplitude exceeds the active building block's dynamic range, clipping occurs, distorting the loop. For instance, in an OTA-based emulator, transconductance may saturate for large input voltages, leading to a flattened or asymmetrical loop.

A wide dynamic range ensures the memelement emulator operates within the linear region of the active building block, maintaining an accurate and continuous hysteresis loop. In contrast, a narrow dynamic range leads to nonlinear distortions, altering the loop's width and compromising the fidelity of the emulated memelement behavior. The width of the hysteresis loop, which represents energy dissipation, depends on the building block's ability to handle the input signal range accurately. A small dynamic range can limit the memelement's resistance or impedance range, compressing the loop's area and reducing its effectiveness in

applications. At high frequencies, the active building block's bandwidth may also limit its dynamic range, causing phase shifts and amplitude reductions that distort the loop and degrade emulator performance. High noise levels can blur the "pinched" region (the crossing point at the loop's origin), diminishing precision.

To ensure faithful reproduction of hysteresis loops across a broad input signal range, active building block circuits must be designed with an adequate dynamic range. This may involve using higher supply voltages, improving linearity through feedback, or selecting low-noise components. However, increasing the dynamic range may come at the expense of power consumption, area, or speed, particularly in scaled technologies with lower supply voltages. For applications like neuromorphic computing or analog circuits, maintaining loop fidelity is critical for functionality, requiring careful alignment of the input signal range with the dynamic range of the building blocks.

In summary, the dynamic range of active building blocks is essential for preserving the accuracy, symmetry, and scaling of the pinched hysteresis loop in memelement emulators. Ensuring a wide dynamic range and operating within it is crucial for reliable, distortion-free emulation. The active building blocks used in this thesis to design memelement emulators provide a dynamic range between 50mV and 200mV, making them suitable for most applications. A comparative analysis with other mem-element emulators has also been emphasized to prove it.

Evaluating the performance of the proposed mem-elements emulator involved conducting a range of analyses, including frequency analysis, transient analysis, temperature analysis, non-volatility tests, and Monte Carlo analysis. Each of the analyses assures the performance and robust design of the proposed circuit.

The layout of this chapter is as follows: The simulation results of proposed OTA and CDBA-based MRE are shown in section 5.2 whereas simulation results of proposed VDGA-based MRE simulation results are presented in section 5.3. The simulation results of the proposed FB-VDBA-based MRE are depicted in section 5.4. The comparison between proposed MREs and reported MREs are presented in section 5.5. The Section 5.6 presents various applications of the proposed MREs. The simulation results of the suggested MIE based on OTA and CDBA are shown in section 5.7, and the simulation results of the suggested MIE based on VDGA and CDBA are covered in section 5.8. The simulation results of the suggested MIE based on VDTA and CDBA are discussed in section 5.9. The comparison between proposed MIEs and reported MIEs are described in section 5.10. The section 5.11

covers various applications of the proposed MIEs, highlighting their versatility and potential usage. The chapter has been concluded in section 5.12.

5.2 Simulation results of proposed memristor emulators using OTA and CDBA

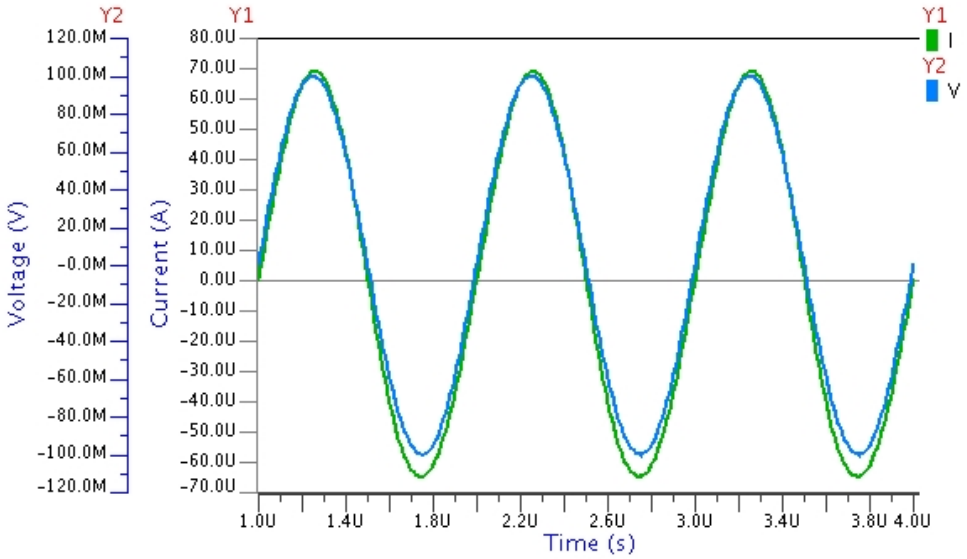
The simulation results of proposed memristor emulators (MREs) employing OTA and CDBA are presented in this section.

5.2.1 Transient analysis

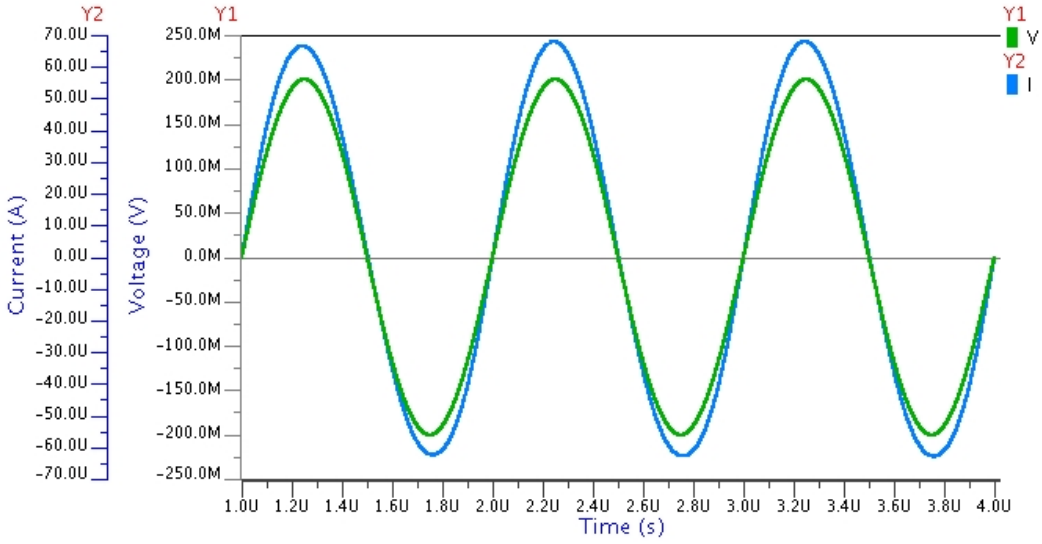
The transient analysis and PHLs have been obtained for the proposed MREs using OTA and CDBA. The OTA and CDBA have been designed using MOS transistors. The aspect ratios (W/L) of MOS transistors used in the proposed MREs having OTA and CDBA are listed in Table 5.1.

Table 5.1. Sizes of MOSFETs for OTA and CDBA used in proposed MRE.

OTA			**CDBA**		
MOSFETs	**W(µm)**	**L(µm)**	**MOSFETs**	**W(µm)**	**L(µm)**
M_1-M_2	16	1	M_1-M_4	32	2
M_3-M_8	9	1	M_5, M_6	42.5	0.36
M_9-M_{12}	4	1	M_7, M_8	0.8	0.5
M_{13}	15	0.36	M_9, M_{12}, M_{13}	10	0.5
M_{14}-M_{15}	14	0.36	M_{10}, M_{11}	4	0.5



(a)

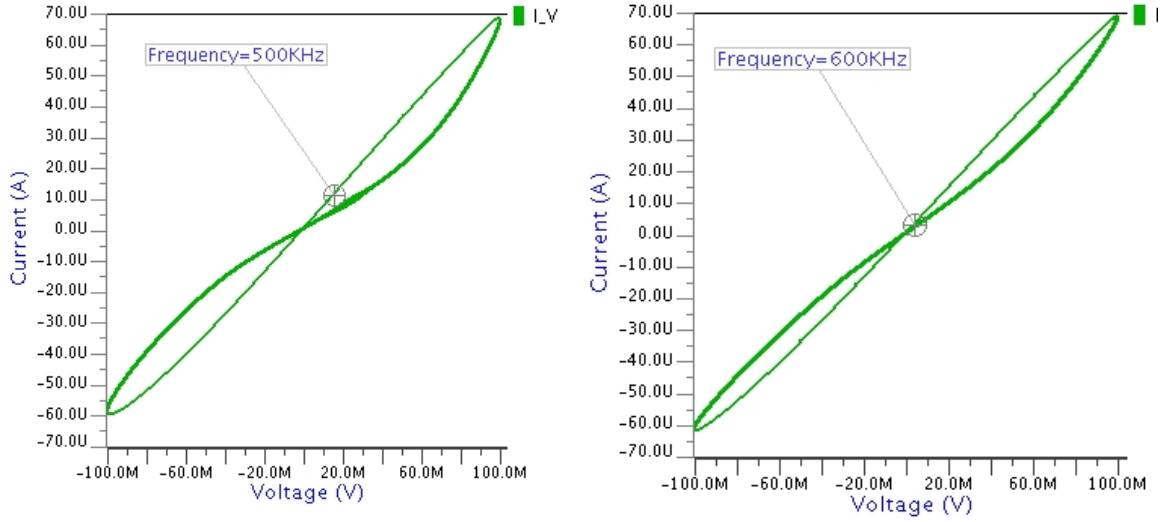


(b)

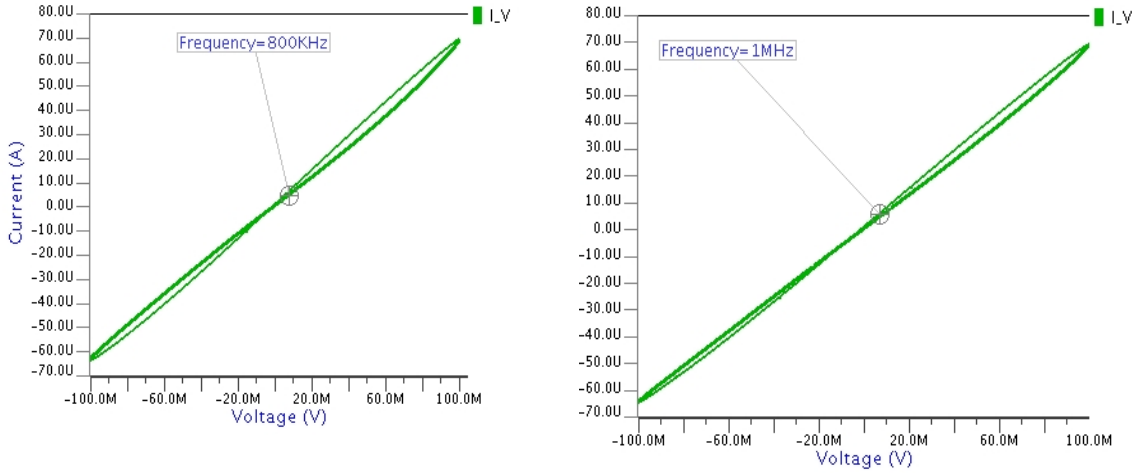
Fig. 5.1 Transient analysis of proposed MRE based on OTA and CDBA (a) grounded (b) floating.

The supply voltage V_{DD} = -V_{SS} = 0.9V is used, whereas the bias voltage V_B is set to -0.1V. The value of capacitance is selected as 40 pF. The current sources I_{B1} and I_{B2} are chosen as 20 µA for CDBA. All MOS transistors are operating in the saturation region.

Fig. 5.1 (a) and (b) display the transient responses of OTA and CDBA-based G-MREs and F-MREs. The sinusoidal voltage signal having an amplitude of 100 mV and a frequency of 800 kHz is applied to proposed G-MREs and F-MREs. In contrast, a sinusoidal input signal with an amplitude of 200 mV and a frequency of 500 kHz is applied to the F-MREs.

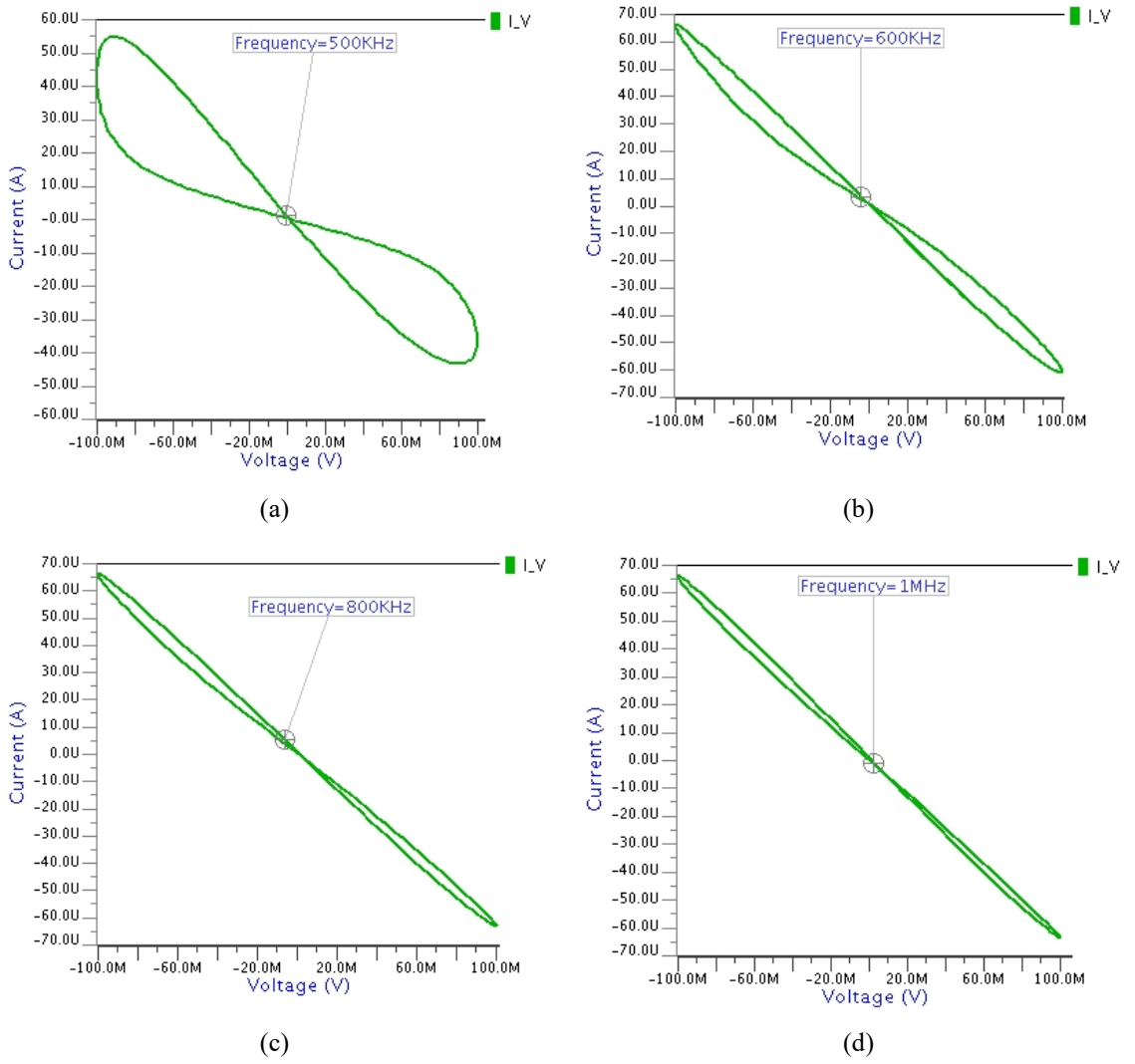


(a) (b)



(c) (d)

Fig. 5.2 PHLs of proposed decremental G-MREs based on OTA and CDBA.



(a) (b)

(c) (d)

Fig. 5.3 PHLs of proposed incremental G-MREs based on OTA and CDBA.

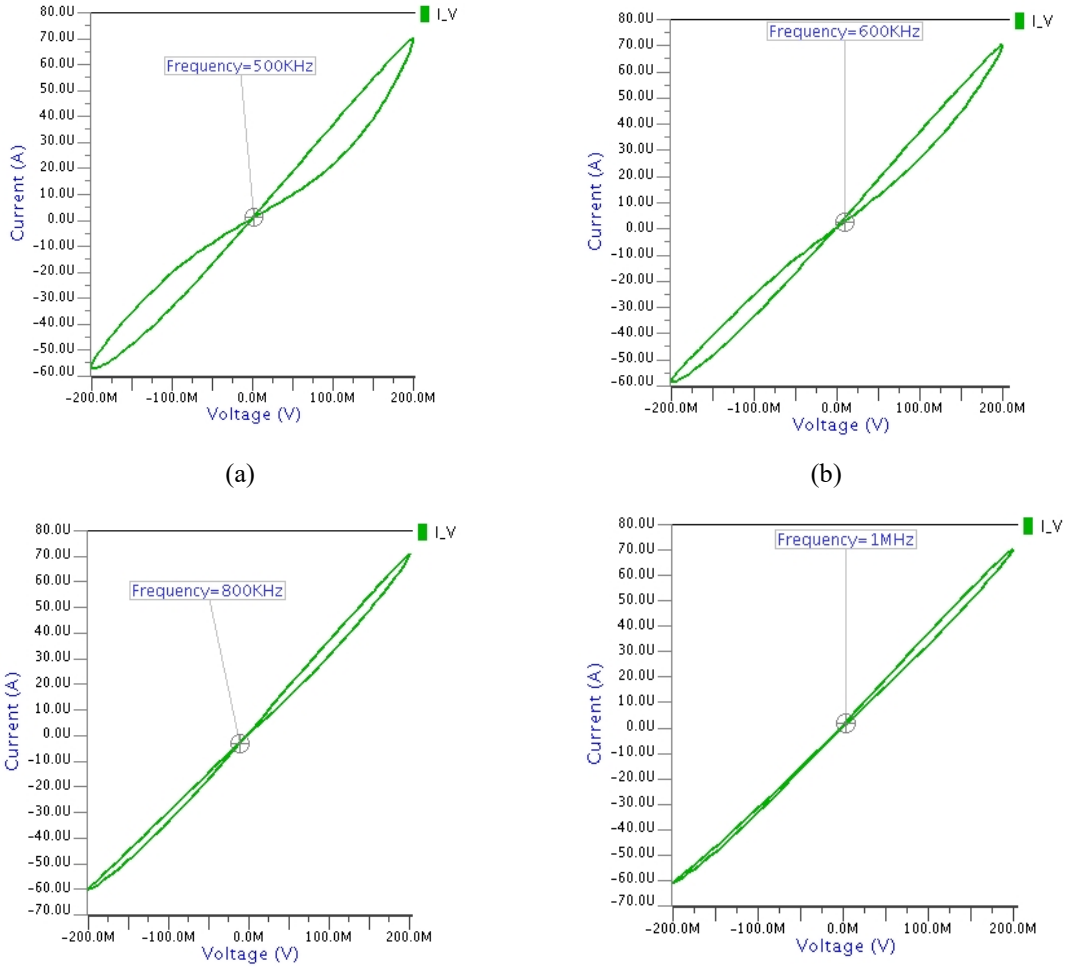
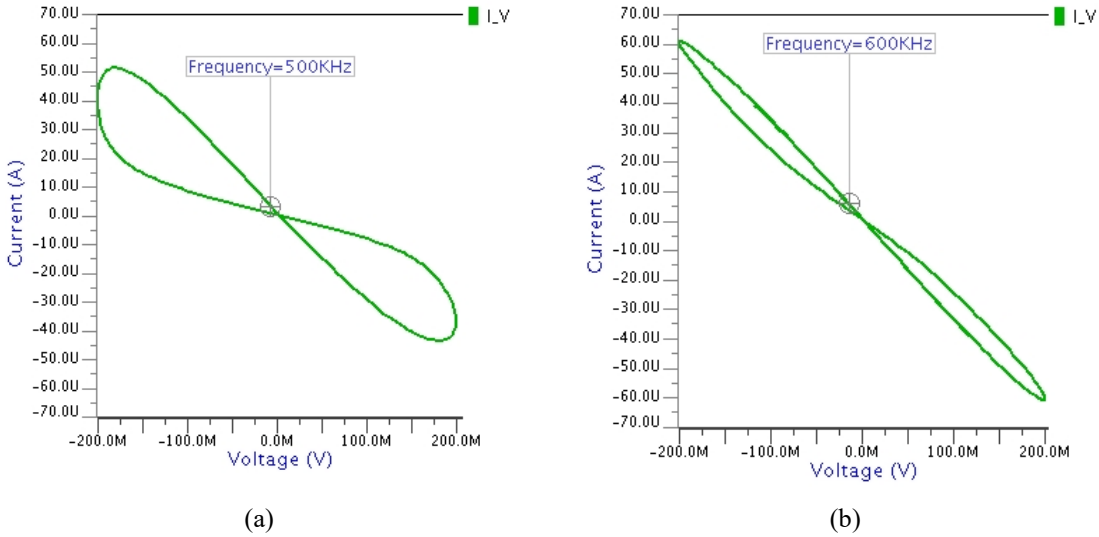
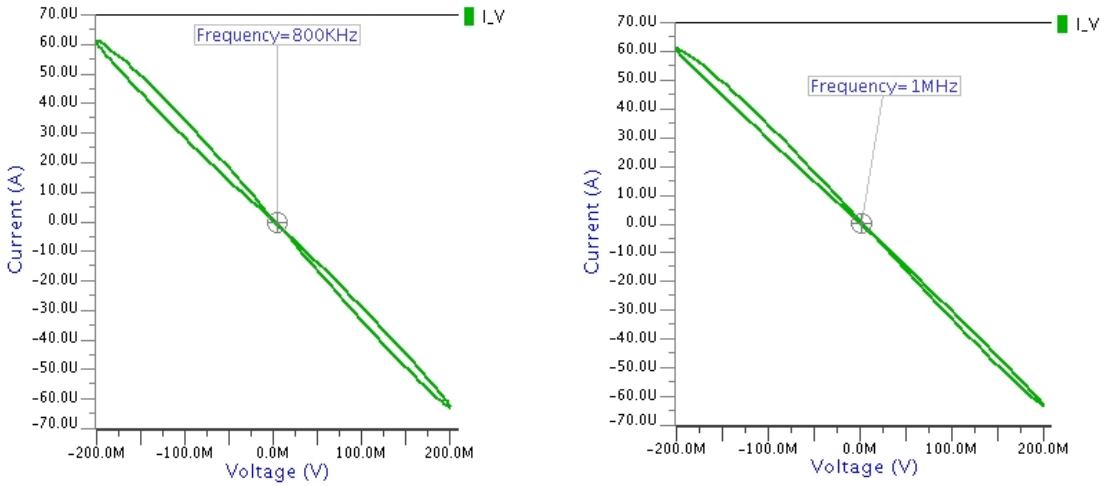


Fig. 5.4 PHLs of proposed decremental F-MREs based on OTA and CDBA.





(c) (d)

Fig. 5.5 PHLs of proposed incremental F-MREs based on OTA and CDBA.

The main characteristic of OTA and CDBA-based MRE is the PHL which is obtained for the frequency range of 500 kHz to 1 MHz as shown in Figs. 5.2 (a)-(d) and Figs. 5.3 (a)-(d) for the sinusoidal signal of amplitude 100 mV.

The performance of MRE is found to be satisfactory up to a frequency of 1 MHz. It is evident from the Figs. 5.3 and 5.4 that the PHLs get contracted when the frequency of input sinusoidal signal is raised.

The PHLs for decremental and incremental F-MREs s are shown Figs. 5.4 and 5.5 for the frequency range of 500 kHz to 1 MHz. The PHL is undistorted throughout the entire frequency range and contracts as the frequency increases.

5.2.2 Temperature analysis

The temperature analysis helps to assess how temperature variations impact the reliability and performance of the proposed MRE. This is crucial for ensuring the longevity and stable operation of devices, especially in harsh or varying environmental conditions. It helps identify temperature-sensitive components and design strategies to maintain or enhance performance under different conditions. Therefore, the PHLs for G-MREs and F-MREs for different temperatures is shown in Figs. 5.6. and 5.7. It is evident from Figs. 5.6 and 5.7 that the proposed MREs deliver acceptable performance within the temperature range of -55°C to +125°C.

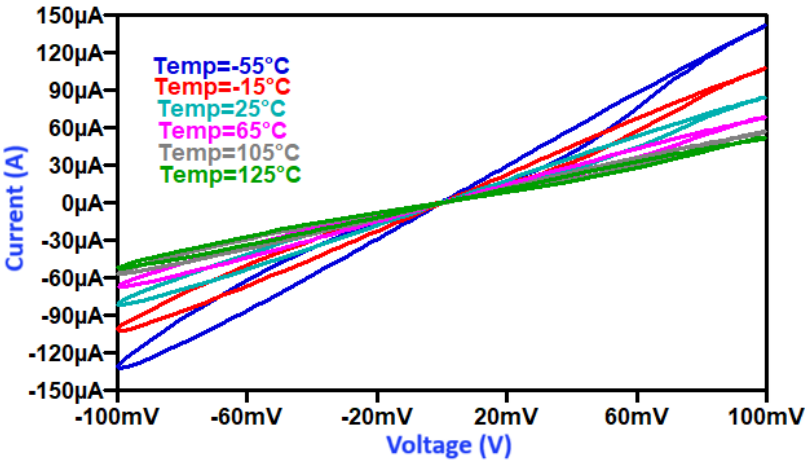


Fig. 5.6 PHLs of decremental G-MREs based on OTA and CDBA for different temperatures.

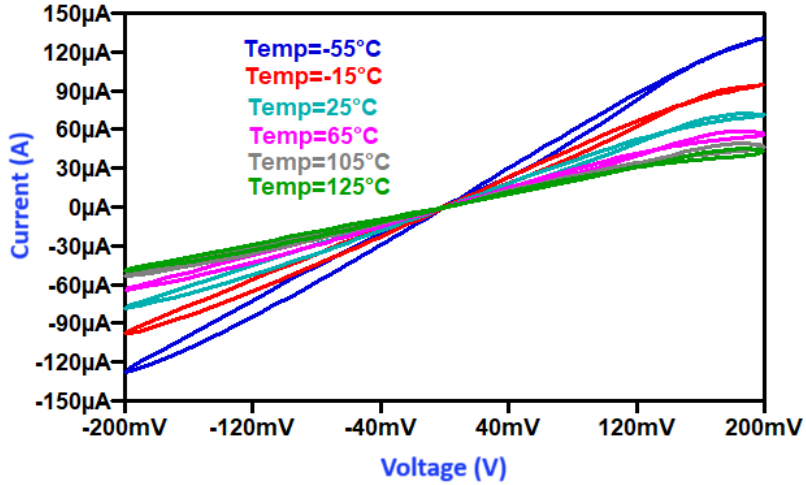


Fig 5.7 PHLs of decremental F-MREs based on OTA and CDBA for different temperatures.

5.2.3 Non-volatility test

The non-volatility test assesses a circuit's ability to maintain information or its state without power. It determines if the circuit retains operational characteristics or stored data even when disconnected from the power source. This form of testing is especially pertinent for circuits or electronic components designed for persistent information storage, such as non-volatile memory devices, specific storage elements like memristors or mem-elements, and other non-volatile components. The non-volatility tests are conducted for all proposed emulators using an input pulse with a frequency of 1 MHz. Fig. 5.8 shows the result of the non-volatility test performed for the suggested decremental and incremental G-MREs. The memristance of decremental MRE decreases during the on-period of input pulse while maintaining its value

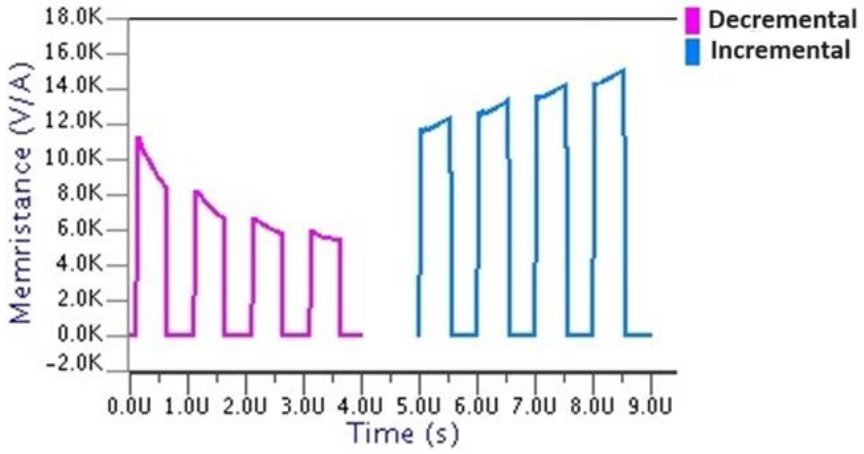


Fig. 5.8 Non-volatility test for decremental/incremental G-MREs using OTA and CDBA.

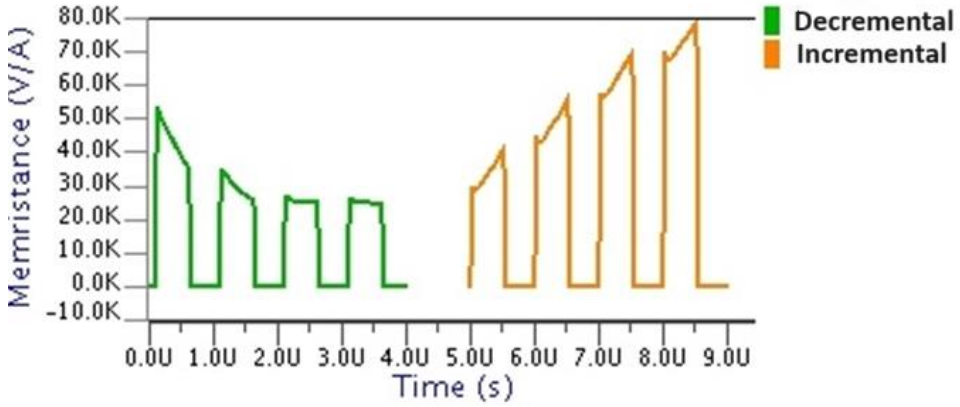
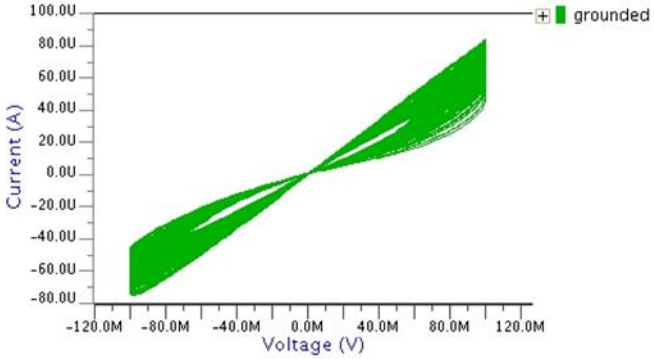


Fig. 5.9 Non-volatility test for decremental/incremental F-MREs using OTA and CDBA.

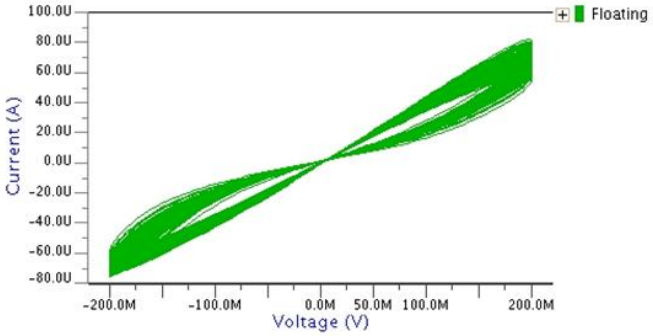
during the off-period. The memristance of incremental MRE increases during the on-period while maintaining its value during the off-period. The non-volatility test across five cycles of input pulses is shown in Fig. 5.9 for the proposed decremental/incremental F-MREs at the input frequency of 1 MHz. The non-volatility test for the F-MREs also demonstrates satisfactory performance.

5.2.4 Monte Carlo analysis

Monte Carlo analysis is conducted by systematically varying MOSFETs' threshold voltage (V_{TH}). This involved running multiple simulation runs, each with a randomly chosen values for V_{TH}. The purpose of this analysis is to evaluate the sensitivity of the emulator to the variations in the threshold voltage and to understand how these variations affect the overall performance of the MRE based on OTA and CDBA. The simulations incorporated Gaussian random variations in the threshold voltage, reflecting the statistical distribution of this



(a)



(b)

Fig. 5.10 Monte Carlo analysis of proposed MRE based on OTA and CDBA (a) grounded (b) floating.

parameter. By generating multiple sets of simulation results with different V_{TH} values, the analysis aimed to provide insights into the range of possible outcomes, the likelihood of specific scenarios, and the overall robustness to variations in the threshold voltage. For the proposed MREs based on OTA and CDBA, Monte Carlo (MC) analysis is carried out at a frequency of 500 kHz with 200 runs. Gaussian random fluctuations were given to standard device characteristics such as threshold voltage (V_{TH}), aspect ratios (W/L), and different device capacitances. Figs. 5.10 (a) and (b) show the PHLs of the suggested MREs in the MC analysis. The simulation results indicate that the PHLs of the proposed MREs based on OTA and CDBA consistently remain pinched at the origin, demonstrating a well-preserved characteristic.

5.3 Simulation results of proposed memristor emulators using VDGA

The simulation results of the proposed MRE based on voltage differencing gain amplifier (VDGA) are shown in this section.

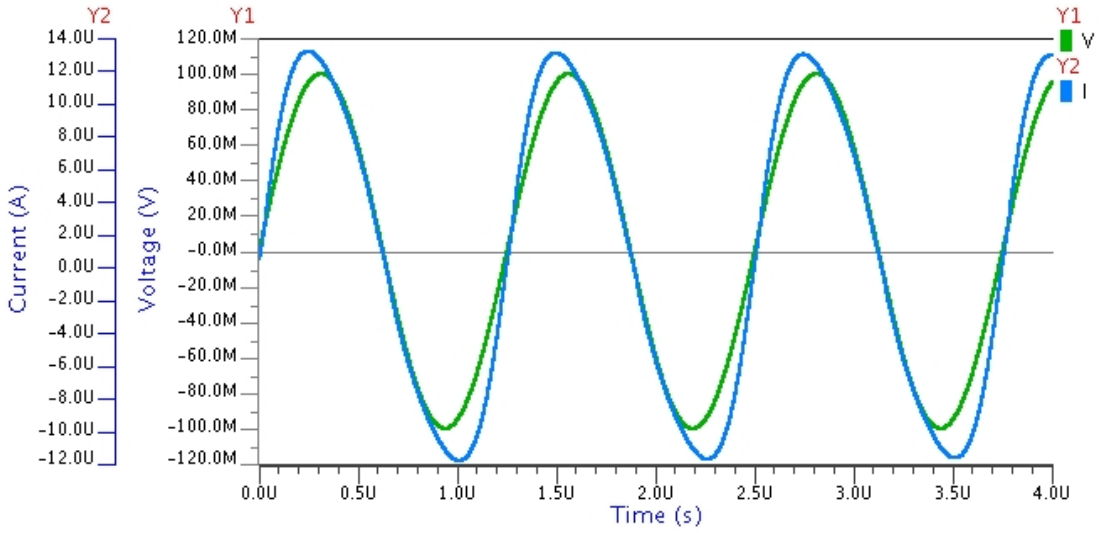
5.3.1 Transient analysis

The transient analysis and PHLs have been obtained for the proposed MRE using VDGA. The VDGA has been designed using MOS transistors. Table 5.2 provides the aspect ratios (W/L) for the MOS transistors used in the VDGA based MRE design. A power supply $V_{DD} = -V_{SS} = 0.9V$ and bias currents (I_{B1} & I_{B2}) of 100 µA are used. The capacitor is chosen to have a value of 40 pF.

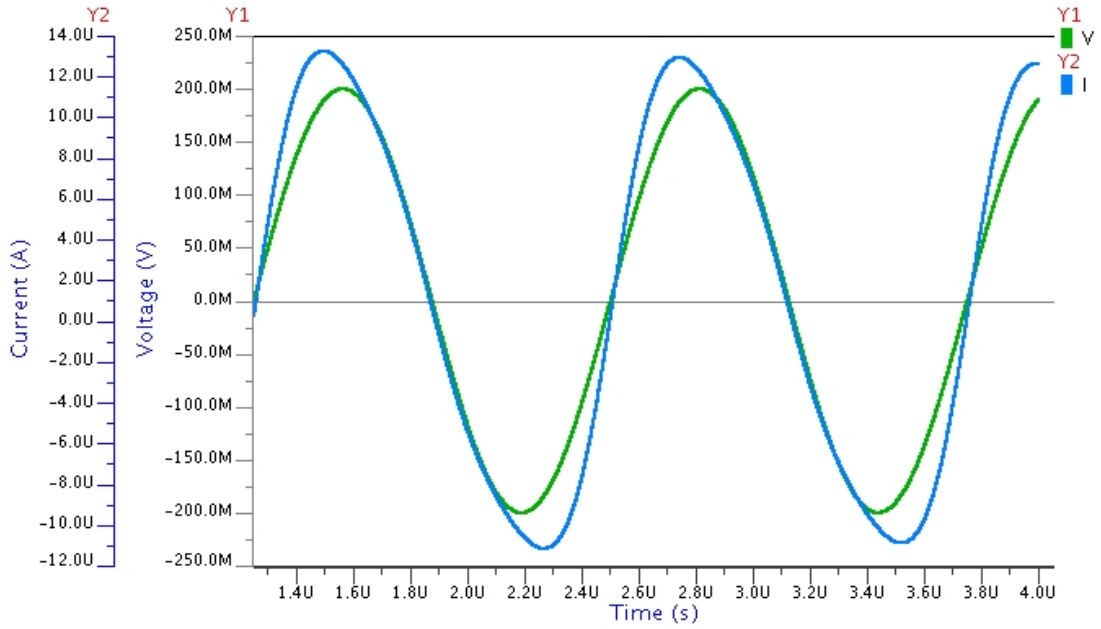
Table 5.2 Sizes of MOSFETs for VDGA.

MOSFETs	W(µm)	L(µm)
M_1, M_2, M_{18}, M_{19}, M_{26}, M_{27}	16	1
M_3 –M_9, M_{20}-M_{23}, M_{28}-M_{31}	9	1
M_{10} -M_{14}, M_{24}, M_{25}, M_{32}, M_{33}	4	1
M_{15}	15	0.36
M_{16}, M_{17}	14	0.36

This section details the transient analysis of the VDGA based G-MREs and F-MREs in their incremental and decremental configurations. For the G-MREs, a sinusoidal signal with a 100 mV amplitude and 800 kHz frequency is applied, while a 200 mV amplitude and 800 kHz frequency sinusoidal signal is used for the F-MREs. The results of these analyses are depicted in Figs. 5.11 (a) and (b).

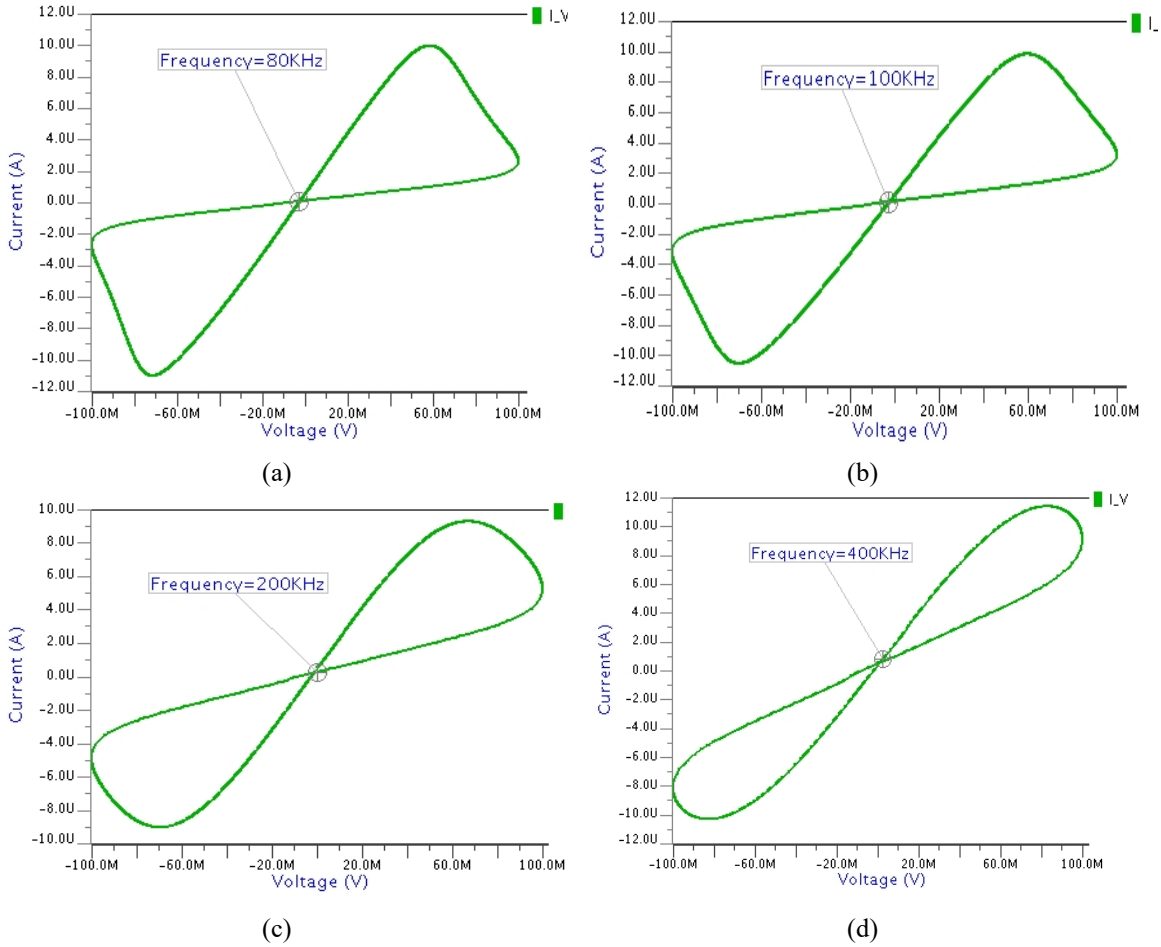


(a)



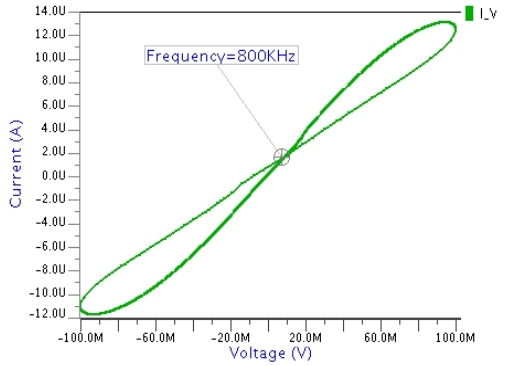
(b)

Fig. 5.11 Transient analysis of proposed MRE based on VDGA (a) grounded (b) floating.

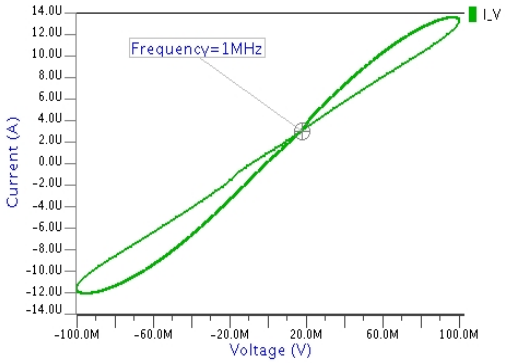


(a) (b)

(c) (d)

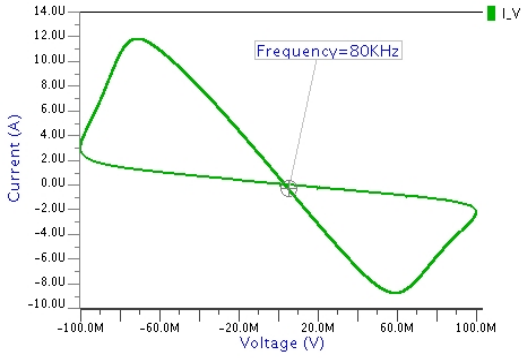


(e)

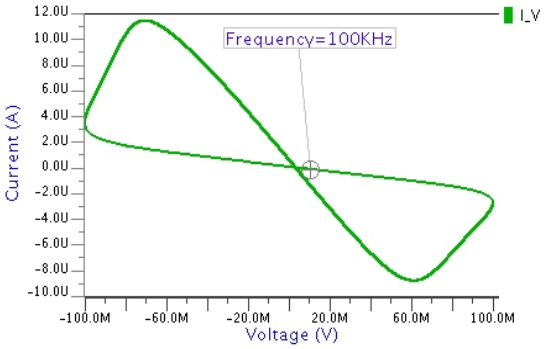


(f)

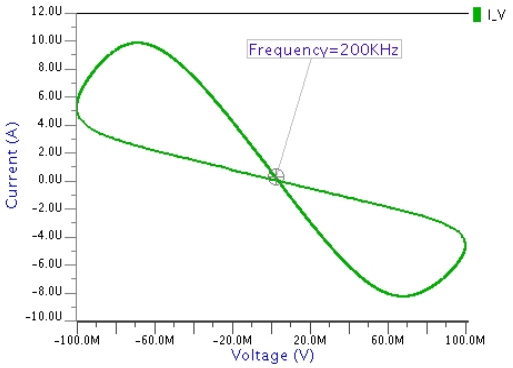
Fig. 5.12 PHLs of proposed decremental G-MREs based on VDGA.



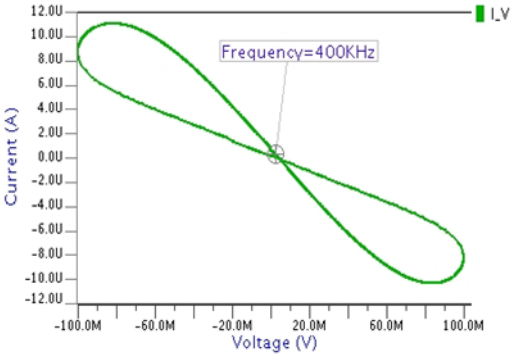
(a)



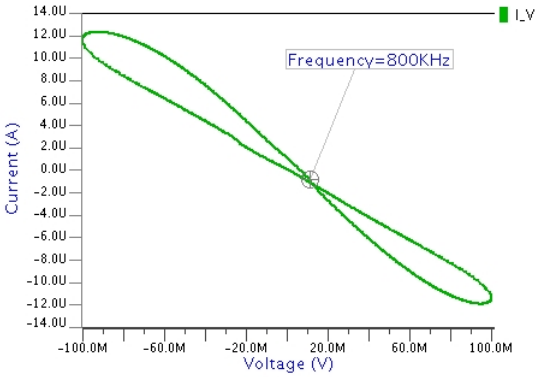
(b)



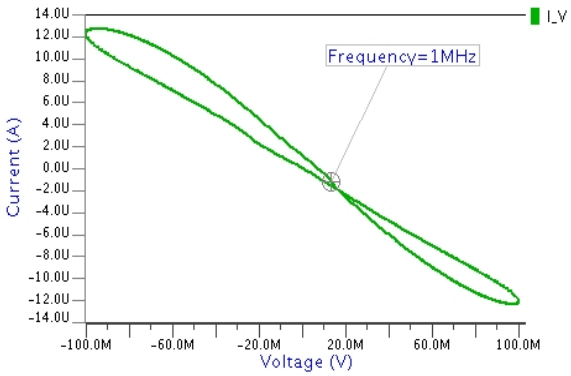
(c)



(d)



(e)



(f)

Fig. 5.13 PHLs of proposed incremental G-MREs based on VDGA.

Figs. 5.12 (a)-(f) and 5.13 (a)-(f) illustrate the PHLs for both incremental and decremental MREs based on VDGA across various frequencies from kHz to 1 MHz, using a 40 pF capacitor. The results demonstrate that the PHLs become more confined as the frequency increases. The formations of PHL for decremental and incremental F-MREs for frequencies between 80 kHz and 1 MHz are shown in Figs. 5.14 (a)-(f) and 5.15 (a)-(f) respectively. The area under the PHL curves get reduced at higher frequencies. As a result, the proposed F-MREs demonstrate satisfactory performance across a broad frequency range.

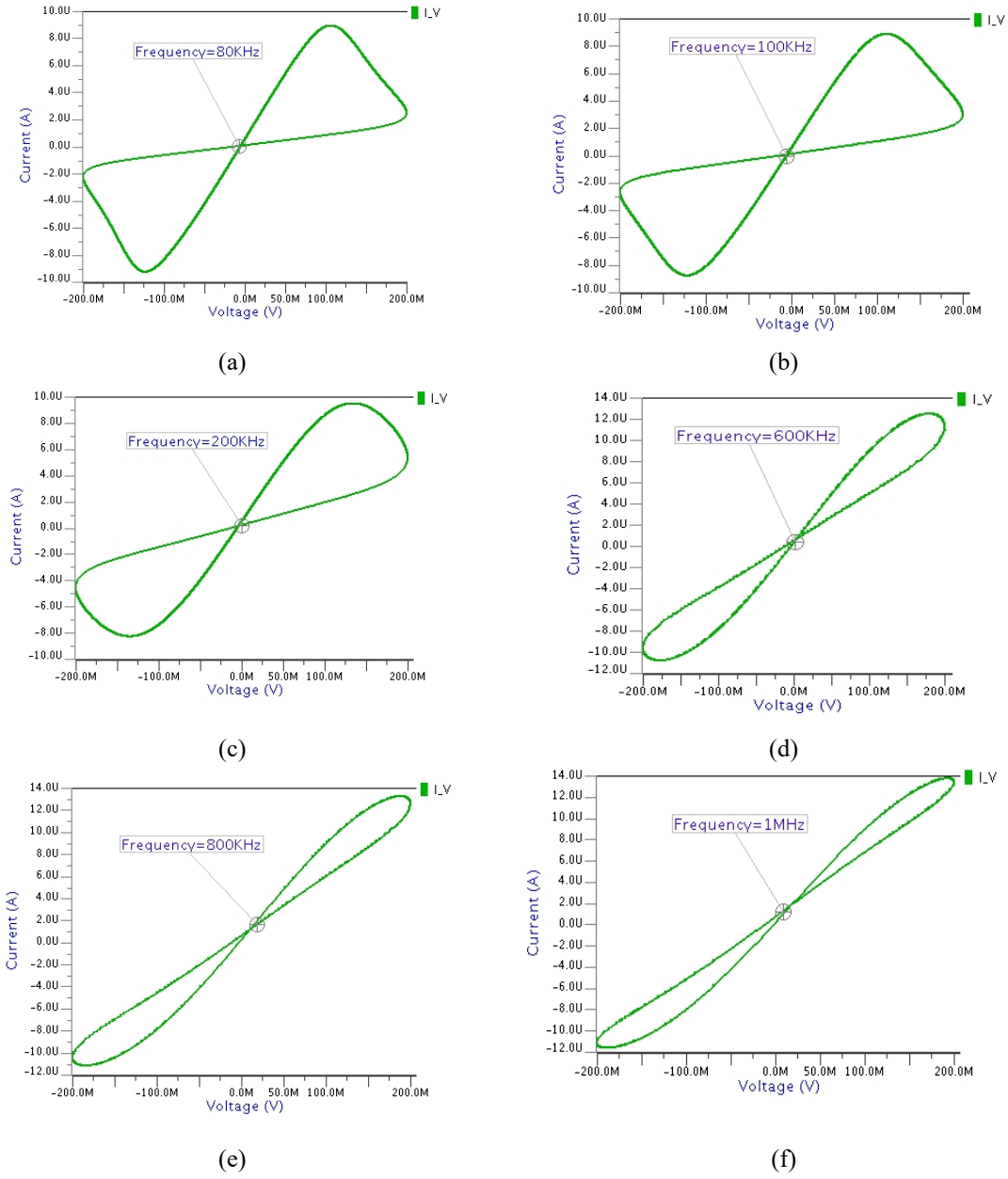


Fig. 5.14 PHLs of proposed decremental F-MREs based on VDGA.

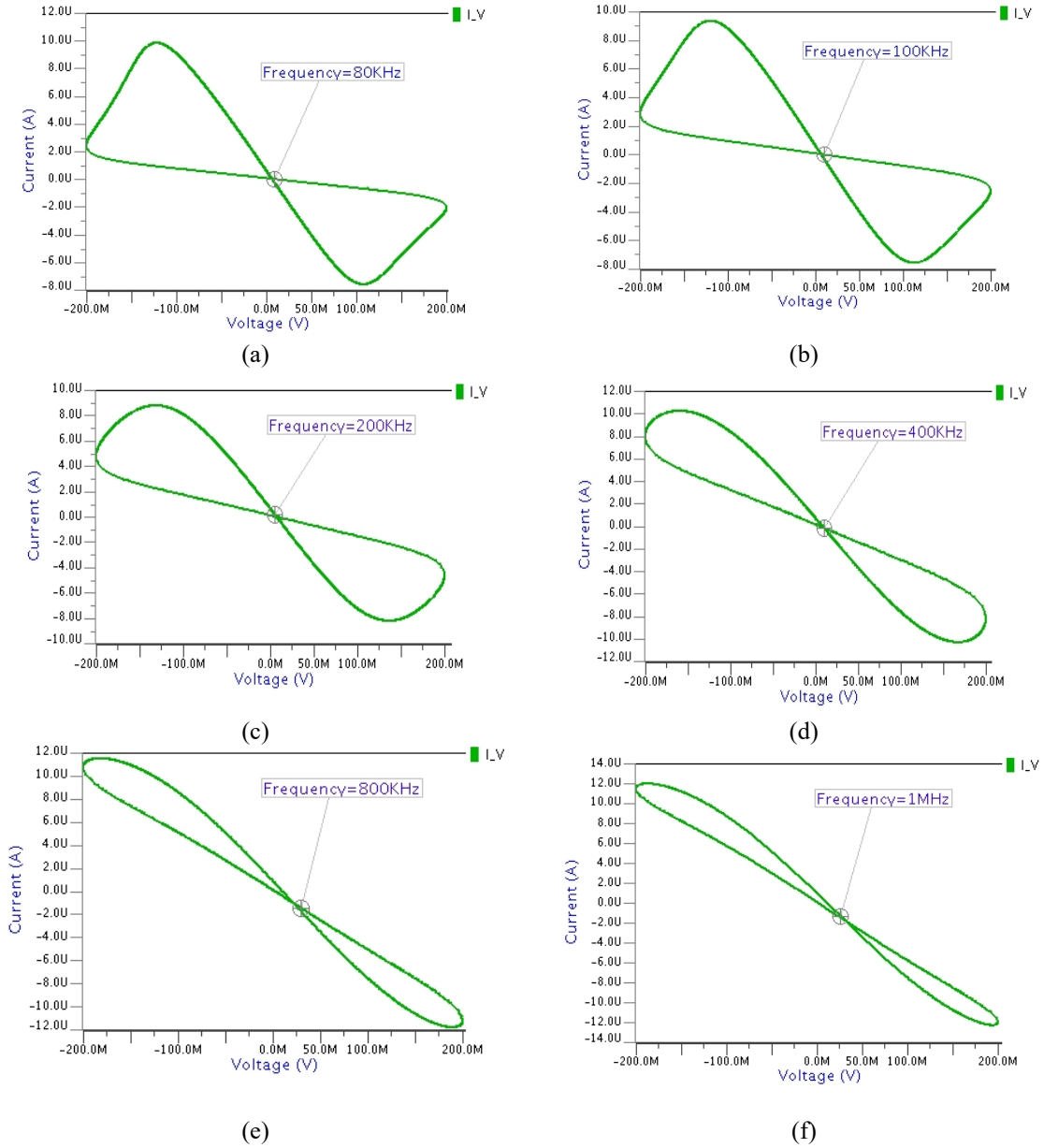


Fig. 5.15 PHLs of proposed incremental F-MREs based on VDGA.

5.3.2 Temperature analysis

The temperature analyses of proposed G-MREs and F-MREs based on VDGA are depicted in Figs. 5.16 and 5.17, respectively. These figures show the PHLs of the VDGA based incremental G-MREs and F-MREs as a function of temperature change from -55°C to +125°C. When examining Figs. 5.16 and 5.17 closely, it is clear that the hysteresis loop of the incremental G-MREs and F-MREs based on VDGA is not deformed in the temperature

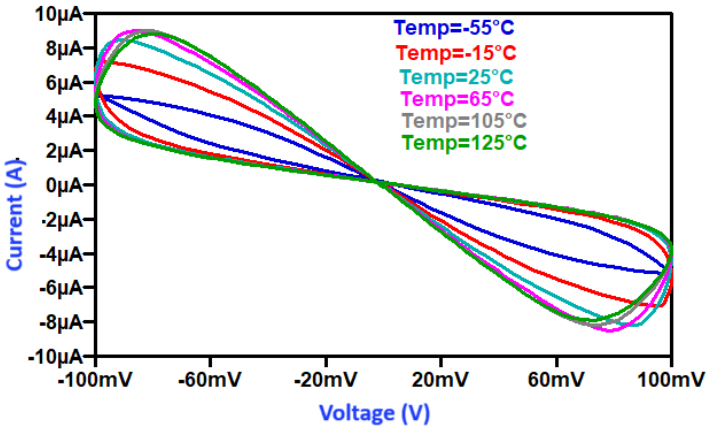


Fig. 5.16 PHLs of incremental G-MREs based on VDGA for different temperatures.

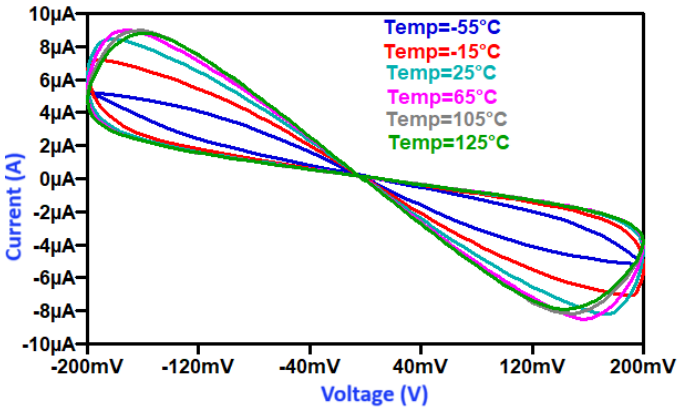
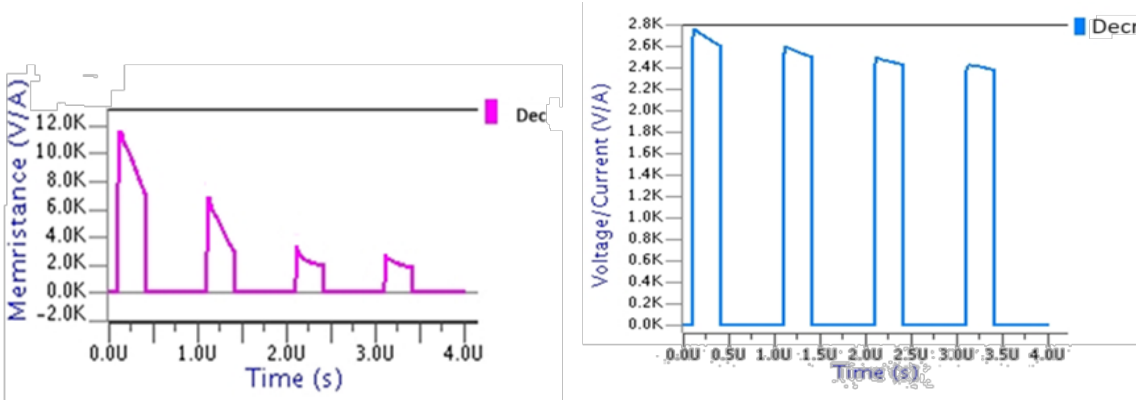


Fig. 5.17 PHLs of incremental F-MREs based on VDGA for different temperatures.

range of -55°C to +125°C. It demonstrates the circuit's robustness and stability throughout an extensive temperature range.

5.3.3 Non-volatility test

A voltage pulse with a frequency of 1 MHz is applied to the input terminals of the proposed decremental G-MREs and F-MREs circuits to validate their non-volatility characteristics. Figs 5.18 (a) and (b) present the non-volatility test results for these circuits. For a grounded memristor, the memristance (M_R) decreases from 11 kΩ to 7 kΩ during the 'on' phase of the input pulse. It remains at that value for the entire 'off' phase of the input pulse, as shown in Fig. 5.18 (a). During the subsequent 'on' phase of the next cycle, the memristance reduces from 7 kΩ to 3 kΩ and holds this value for the following 'off' phase. These results confirm that the MRE circuit retains the previous memristance value during the 'off' phase of the input pulse. Similarly, in the F-MREs circuits, as depicted in Fig. 5.18 (b), the memristance



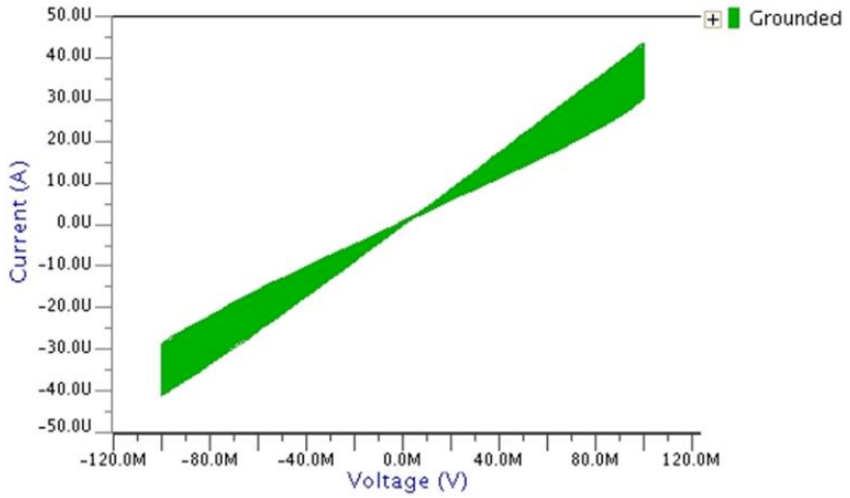
(a) (b)

Fig. 5.18. Non-volatility tests for decremental MRE based on VDGA(a) grounded (b) floating.

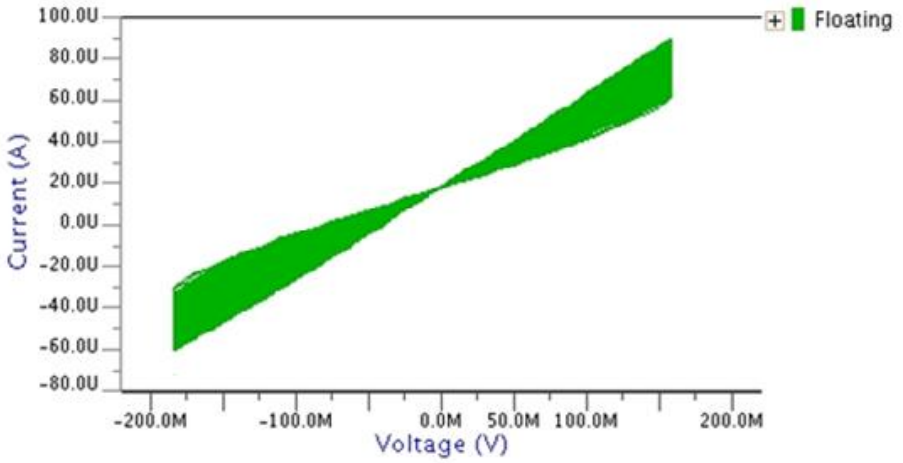
(M_R) decreases from 2.8 kΩ to 2.6 kΩ during the 'on' phase of the input pulse and remains at that level throughout the following 'off' phase. In the next cycle, the memristance drops further from 2.6 kΩ to 2.5 kΩ during the 'on' phase and stabilizes at this value in the 'off' phase. Therefore, the MRE circuit preserves the previous memristance value during the 'off' phase.

5.3.4 Monte Carlo analysis

The proposed MRE design based on VDGA exhibits resilience in the Monte Carlo analysis. This analysis, performed over 200 runs with Gaussian random variations in device parameters such as threshold voltage and MOSFET aspect ratios, demonstrates the robustness of the incremental and decremental MRE circuits. Despite variations in these



(a)



(b)

Fig. 5.19 Monte Carlo analysis of proposed MRE based on VDGA (a) grounded (b) floating

parameters, the pinched hysteresis curves remain consistent, as illustrated in Fig. 5.19 (a) and (b).

5.4 Simulation results of proposed memristor emulators using FB-VDBA

This section presents the simulation results of memristor emulator (MRE) using fully-balanced voltage differencing buffered amplifier (FB-VDBA).

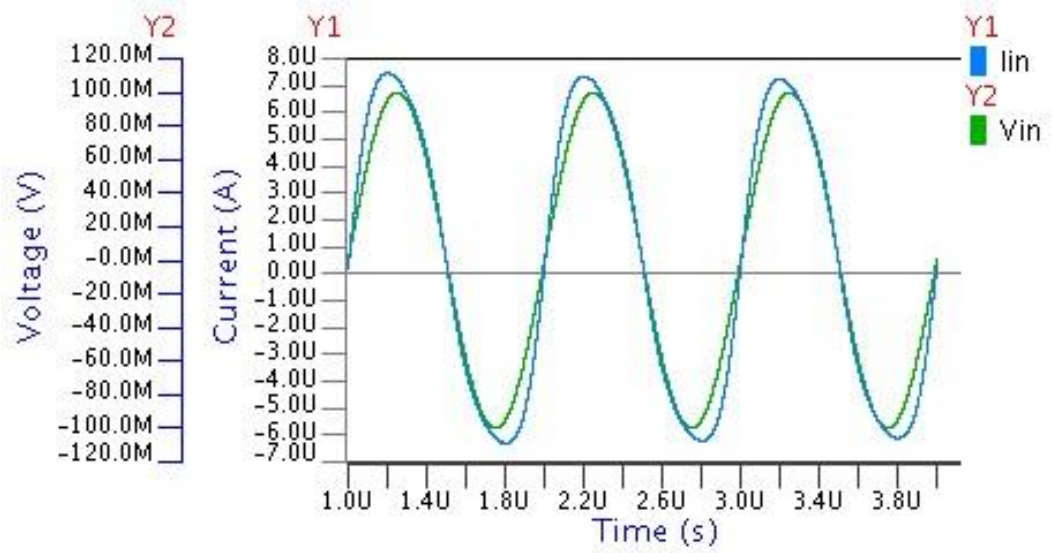
5.4.1 Transient analysis

The transient analysis and PHLs have been obtained for the proposed FB-VDBA-based MRE using Eldo simulation tool for 180 nm CMOS technology parameters. The supply voltage is used as $V_{DD} = -V_{SS} = 0.9$ V. The value of capacitor is selected as 40 pF.

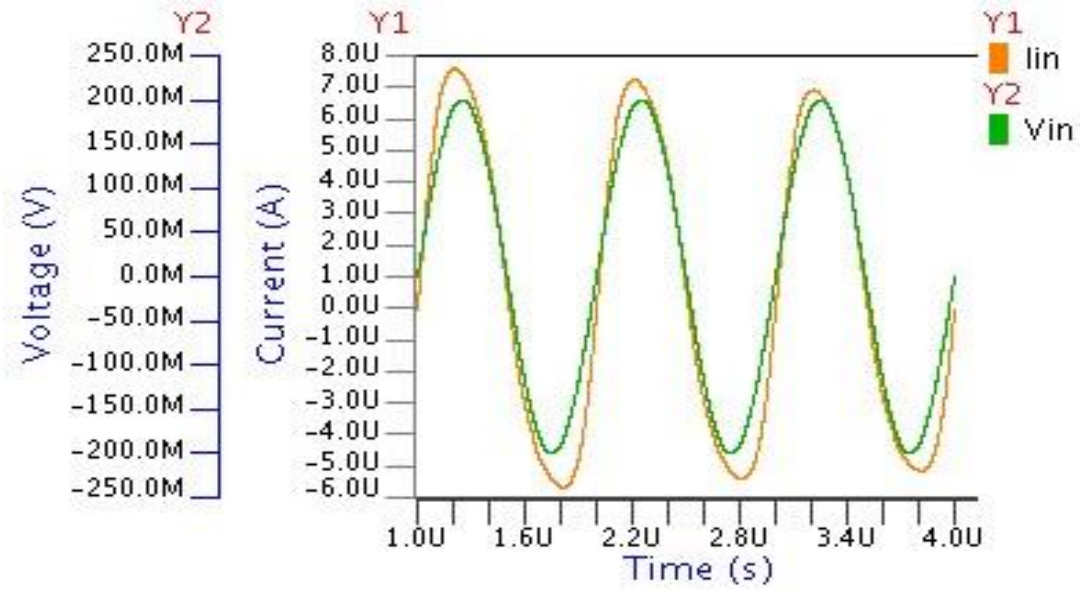
Table 5.3 Sizes of MOSFETs for FB-VDBA.

MOSFETs	W(µm)	L(µm)
M_1-M_2	16	1
M_3-M_8	9	1
M_9-M_{12}	4	1
M_{13}-M_{16}	54	0.18
M_{17}	15	0.18
M_{18}-M_{19}	14	0.18

The Table 5.3 lists the aspect ratios (W/L) of the MOS transistors utilized in the suggested MRE based on FB-VDBA. The decremental G-MREs and F-MREs circuits based on FB-VDBA are subjected to a sinusoidal signal with a 100 mV amplitude and a frequency of 1 MHz. The resulting current- voltage response over time is illustrated in Fig. 5.20 for G-MREs and F-MREs based on FB-VDBA.



(a)



(b)

Fig. 5.20 Transient analysis of proposed MRE based on FB-VDBA (a) grounded (b) floating.

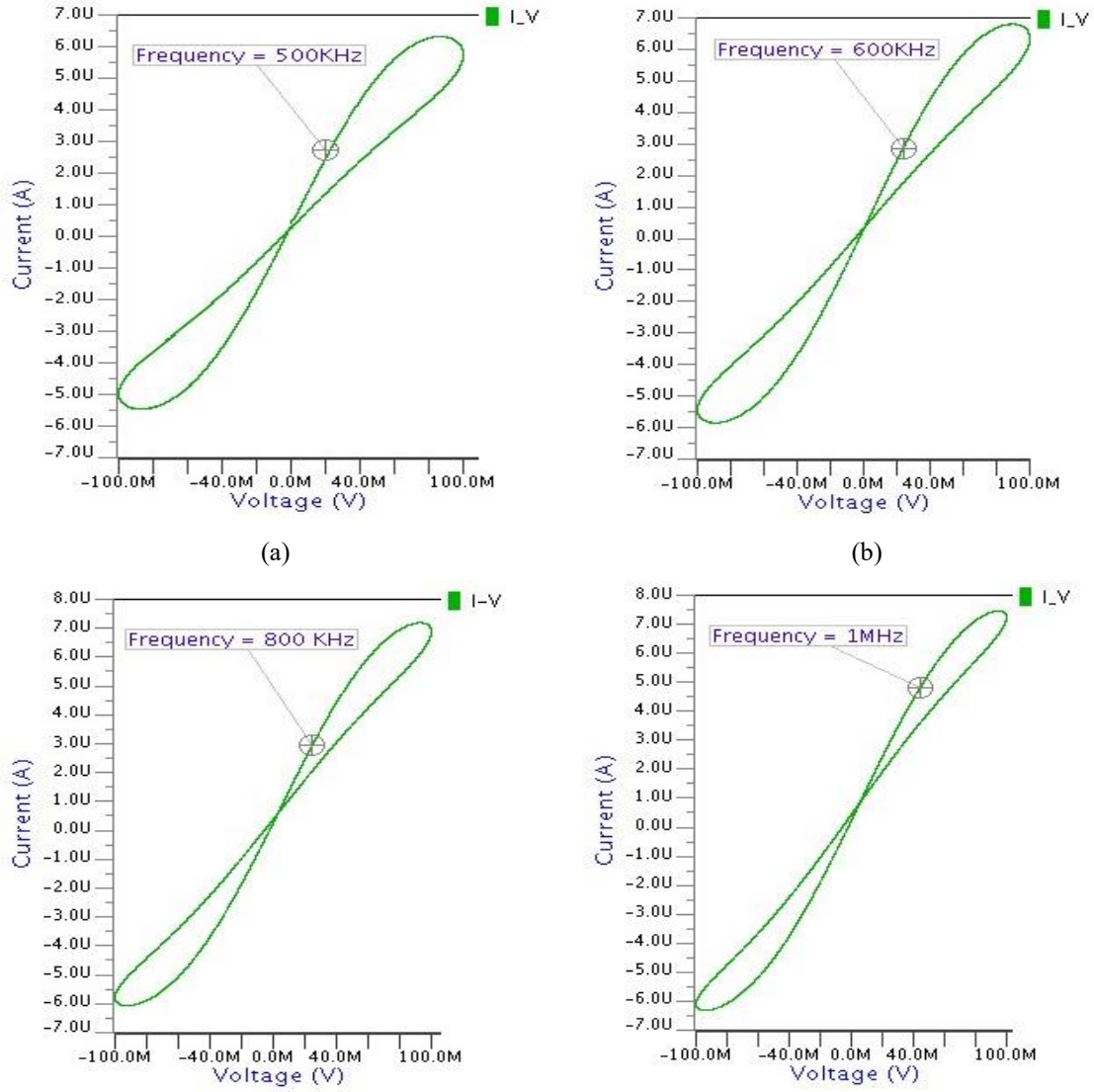
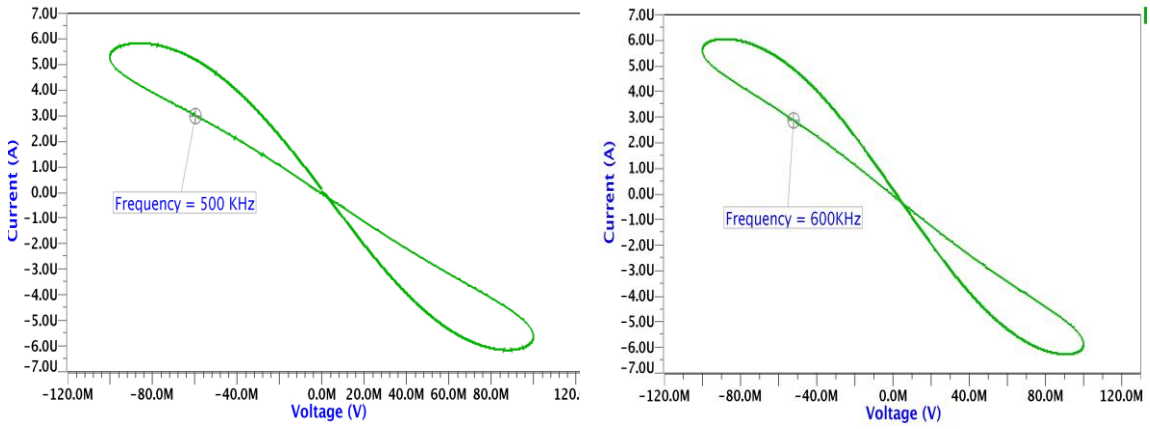
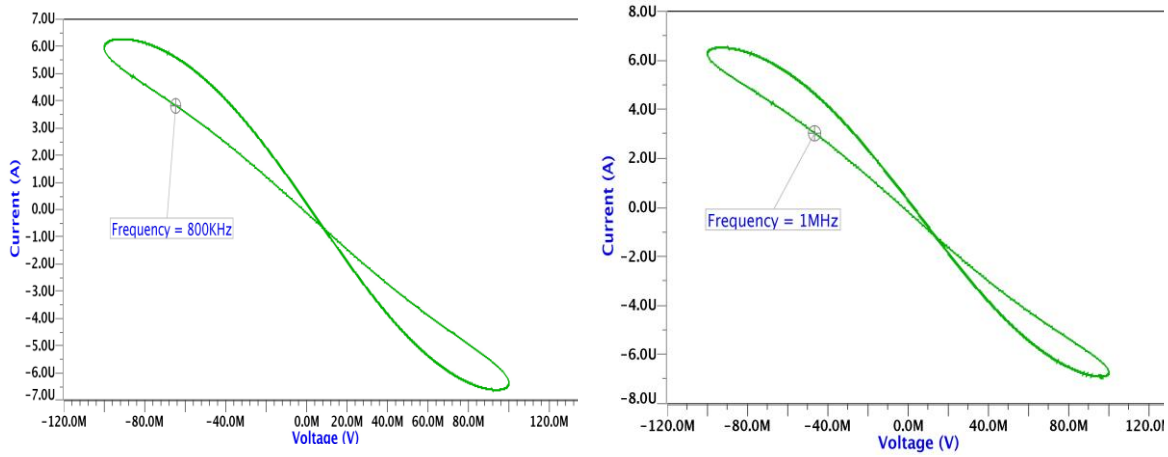


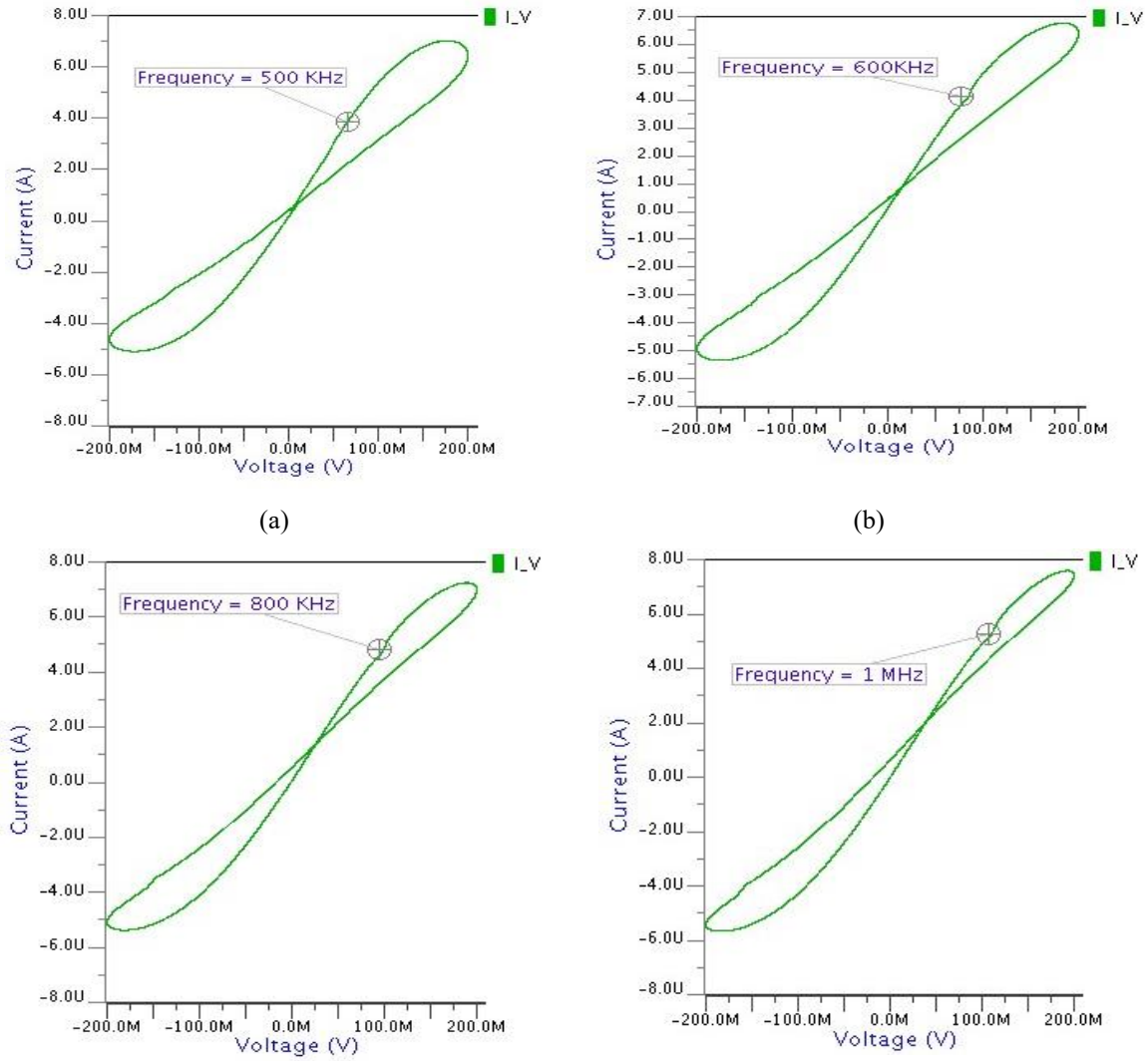
Fig. 5.21 PHLs of proposed decremental G-MREs based on FB-VDBA.





(c) (d)

Fig. 5.22 PHLs of proposed incremental G-MREs based on FB-VDBA.



(a) (b)

(c) (d)

Fig 5.23 PHLs of proposed decremental F-MREs circuits based on FB-VDBA.

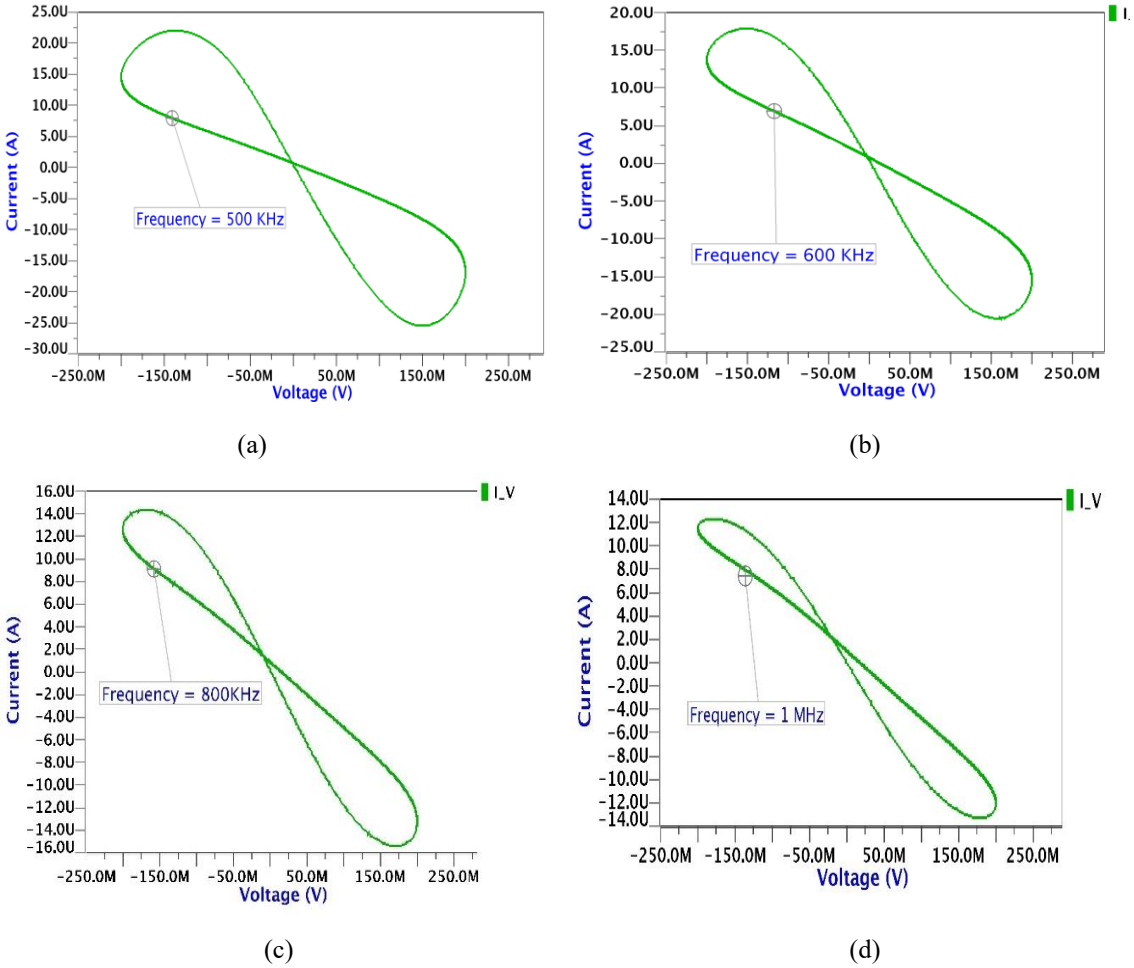


Fig. 5.24 PHLs of proposed incremental F-MREs circuits based on FB-VDBA.

The sinusoidal voltages V_{in1} and V_{in2} having 100 mV amplitude and 1 MHz frequency are applied to the input terminals of the decremental F-MREs. Figs. 5.23 (a) to (d) and Figs. 5.24 (a) to (d) show PHLs of the decremental and incremental F-MREs circuits corresponding to different frequencies. It is evident that the PHL contracts when the frequency is increased within a suitable range.

5.4.2 Temperature analysis

The temperature analysis of the proposed G-MREs and F-MREs based on FB-VDBA is presented in Figs. 5.25 and 5.26, respectively. The performance of the proposed incremental G-MREs and F-MREs based on FB-VDBA is found to be satisfactory in the temperature range from -55°C to +125°C. Upon careful examination of Figs. 5.25 and 5.26, it becomes evident that the hysteresis loop of the proposed decremental G-MREs and F-MREs does not undergo deformation throughout the temperature range from -55°C to +125°C.

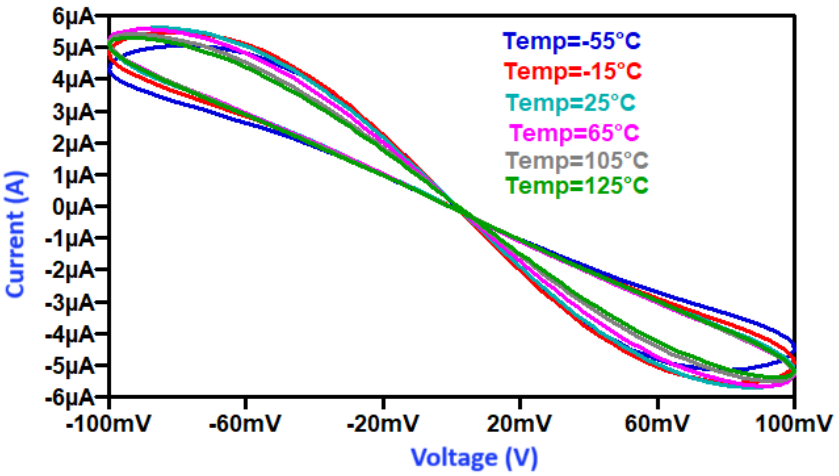


Fig. 5.25 PHLs of incremental G-MREs based on FB-VDBA for different temperatures.

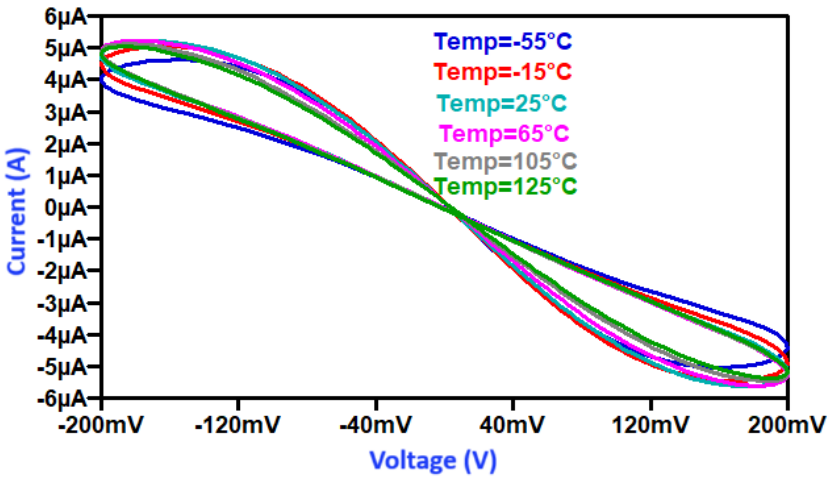


Fig. 5.26 PHLs of incremental F-MREs based on FB-VDBA for different temperatures.

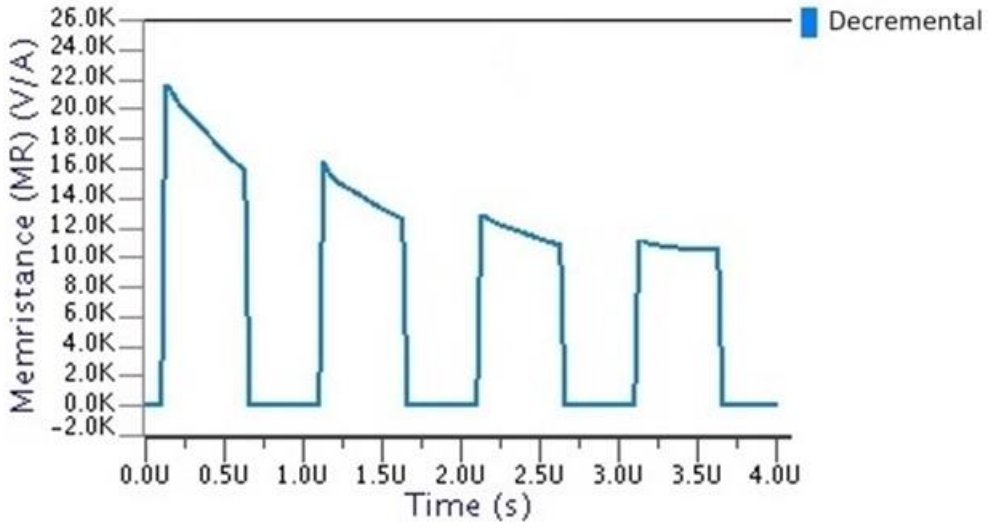
This consistent behaviour reflects the robustness of the MRE circuit across a wide temperature range, highlighting its reliability under varying thermal conditions.

5.4.3 Non-volatility test

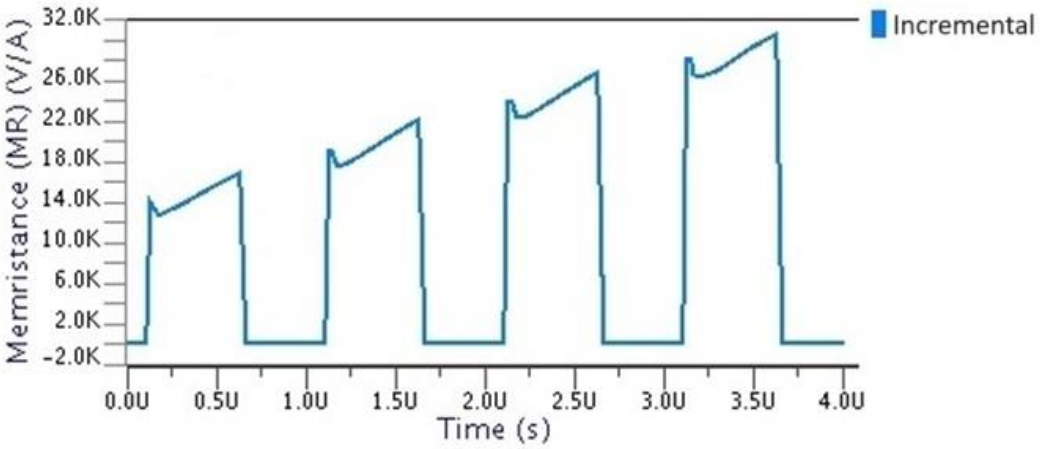
A voltage pulse having frequency of 1 MHz is applied to the input terminals of the proposed decremental/incremental G-MREs and F-MREs based on FB-VDBA for the validation of the non-volatility characteristic. Figs. 5.27 (a) and (b) display the non-volatility test of the proposed decremental/incremental G-MREs based on FB-VDBA. The memristance (M_R) shows a drop from 22 kΩ to 16 kΩ in the 'on' phase of the input pulse as shown in Fig. 5.27 (a) and it stays at this value in the 'off' period. The memristance drops from 16 kΩ to 13 kΩ

in the ‘on’ phase of next cycle and stays at that value in the ‘off’ period. This cyclic behaviour continues suggesting that the MRE circuit preserves the previous memristance value during the ‘off’ time of the input pulse.

Comparably, in the case of the incremental G-MREs and F-MREs circuits, the memristance rises from 14 kΩ to 18 kΩ during the ‘on’ phase of first cycle and stays unchanged during the ‘off’ phase as shown in Fig. 5.27 (b). Once again, in the next cycle, the memristance increases from 18 kΩ to 22 kΩ during the ‘on’ phase staying at that amount in the following ‘off’ phase. It follows that the suggested incremental and decremental memristor emulators based on FB-VDBA circuits successfully follows the non-volatility property.

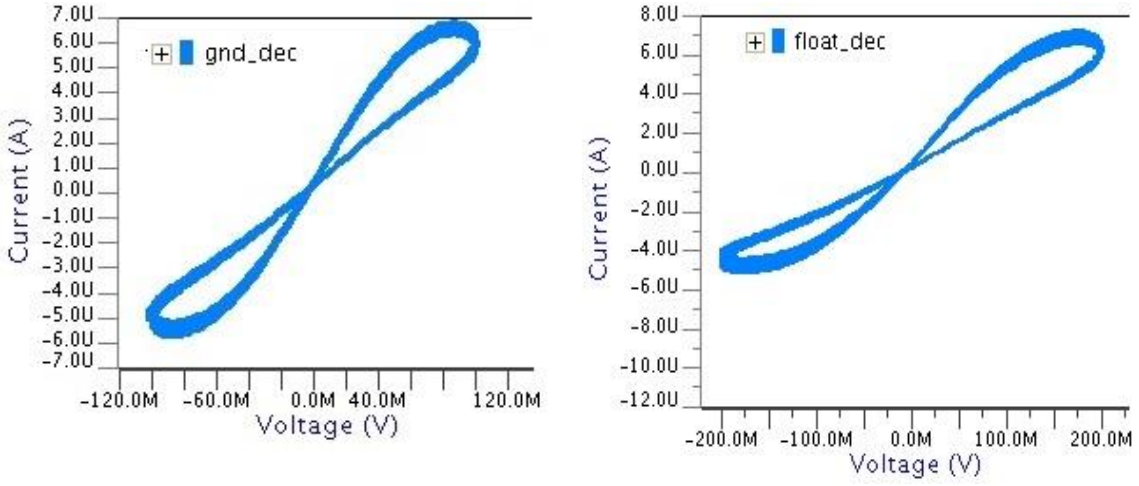


(a)



(b)

Fig. 5.27. Non-volatility tests for MRE based on FB-VDBA (a) decremental (b) incremental.



(a) (b)

Fig. 5.28 Monte Carlo analysis of proposed MRE based on FB-VDBA (a) grounded (b) floating.

5.4.4 Monte Carlo analysis

The robustness of the proposed MRE based on FB-VDBA has been comprehensively examined via meticulous Monte Carlo analysis. This analysis, involving 200 runs, incorporated Gaussian random variations to modify essential device parameters, encompassing the device's MOSFET aspect ratios, and threshold voltage. The outcomes of Monte Carlo analysis are depicted in Fig. 5.28 (a) and (b). The pinched hysteresis curves are obtained through the Monte Carlo analysis. This indicates that the incremental and decremental MRE designs are sturdy. Their steady performance in various conditions proves that these circuits are reliable and stable making them suitable for many applications that must endure and tolerate different changes.

5.5 Comparison of proposed MREs with reported MREs

The proposed MREs based on OTA and CDBA, VDGA, and FB-VDBA are compared with existing designs, as shown in Table 5.4. Unlike existing emulators that rely on analog multipliers [31-37, 39, 43, 45, 46, 48, 50, 59, 61, 75], the proposed designs using OTA and CDBA, VDGA, and FB-VDBA circumvent this complexity. It spans a broader frequency range, extending up to 1 MHz, contrasting with the frequency range of Hz [31, 35, 43, 45, 50, 75, 85 and 119] and kHz [32, 33, 36, 37, 39, 46, 48, 59, 61, 70, 76, 77, 78, 80 and 98] ranges. Our emulator simplifies circuitry by employing only one passive component, unlike the multiple components in existing designs [31-37, 39, 43, 45, 46, 48, 50, 59, 61, 75, 76, 78, 79, 87, 94, 107, 116, 117, 118, 119, 126 and 127]. Furthermore, while existing designs

are restricted to grounded configurations [31, 35, 37, 39, 46, 48, 61, 76, 77, 85, 107, 113, 115, 117, 118, 126, 127, 133 and 138] the proposed designs of MRE supports both grounded and floating setups.

Table 5.4 Comparison of proposed MREs with other reported MREs in the literature.

Ref.	No. of active elements	No. of passive elements	Power supply	Output range	Decremental (D) /Incremental (I)	Memristance Range	Floating(F) / grounded(G)	Electronic Tunability
[31]	1 buffer, 1 integrator, & 1 multiplier	3R,1C	±5V	400Hz	D	15.45Ω-2.58kΩ	G	No
[32]	4 CCIIs, & 1multiplier	5R, 1C	±10V	2 kHz	D	0Ω-15.148Ω	F	No
[33]	4CCII, & 1 multiplier	5R,1C	±10V	20.2 kHz	D	----	F	No
[24]	1DDCC, & 1multiplier	2R, 1C	±1.5V	1MHz	Both	6Ω-22Ω	F	No
[36]	4op-amps, 1 multiplier, & 3 current dependent sources.	9R,1C	±2V	20.3 kHz	D	0-4kΩ	F	No
[37]	2 CCII, multiplier, & current shaping circuits.	4R, 1C	±1V	1kHz	D	----	G	No
[39]	2CCIIs, & 1multiplier	4R, 3C	±10V	27kHz	D	----	G	No
[43]	6 op-amp, 1 multiplier, 1 diode, & 12 MOSFETs,	7R, 1C	±15V	800Hz	Both	0-37.5kΩ	F	No
[45]	4 CCIIs, & 1 multiplier	3R, 1C	±10V	120Hz	Both	----	F	No
[46]	1 MO-OTA, & 1multiplier	1R, 1C	±5V/ 1.2V	1kHz	Both	----	G	Yes
[48]	1 CBTA, & 1multiplier	2R, 1C	±0.9V	1kHz	D	0-25Ω	G	No
[50]	2op-amp, & 2multipliers	3R, 2C	----	10Hz	Both	----	F	No
[59]	3 CCII+s, & 1analog multiplier	3R, 1C	±10V	5 kHz	D	----	Both	No
[61]	1 ECCII, 2 OTAs, & multiplier	2R, 1C	±10V	1.5 kHz	Dl	----	G	No
[69]	1VCR, & 1 CCII	----	±1.5V	2 kHz		7kΩ-35kΩ	F	No
[75]	4 CCIIs,1op-Amp & 1multiplier	10R, 1C	±15V	160Hz	D	----	F	No
[76]	2CFOAs, & 1OTA	3R, 2C	±12V	2 kHz	D	----	G	No
[77]	1 CCII, 1AD633, 2 transistors PN3565, & 1amplifier	5R, 1C	±1V	3 kHz	D	1.6kΩ-3.45kΩ	G	No

[78]	3OTAs, & CCII+	6R,1C	±5V, ±15V	5 kHz	D	----	F	No
[80]	4CCIIs, & 3OTAs	5R, 1C	±15V	1kHz	D	0.3kΩ-1.8kΩ	F	----
[85]	1OTA, & 2PMOS	1C	±1V	30Hz	Both	5GΩ-25GΩ	F	No
[87]	1 DVCCTA	3R, 1C	±0.9V	2MHz	Both	0℧-4℧	F	----
[94]	VDTA, & 1multiplier	2R,1C	±0.9V	2 MHz	Both	0℧-5℧	F	Yes
[98]	2 OTAs	1C	±1.2V	4kHz/ 8MHz	Both	----	Both	Yes
[102]	1CBTA	1C	±1.25V	1MHz	D	8kΩ-30kΩ	F	Yes
[105]	3MOS transistor	1C	±1V	13MHz	Both	----	G	No
[107]	1 CCII+, & 1 OTA	1R, 1C	±1.2V	25MHz	Both	0-1kΩ	G	------
[109]	1 OTA, 1 DVCC, & 2 MOS	1C	±0.9V	1.5MHz	D	----	F	No
[113]	1CDTA & 2 transistors	1C	±1.2V	10MHz	D	4kΩ-5.5kΩ	G	No
[115]	1CCCII, buffer, & 1 transistor	1C	±1.2V	10MHz	D	1.44kΩ	G	No
[116]	2 VDTA	1R ,1C	±0.9V	1MHz	Both	----	F	Yes
[117]	5OTA	3R, 1C	±11V	2MHz	D	0.5kΩ-2kΩ	G	No
[118]	1OTA & 1VDCC	2R, 1C	±10V	1MHz	D	----	G	No
[119]	2VDTA	2R, 1C	±0.9V	5 kHz	D	0kΩ-15.2kΩ	F	No
[126]	1CCTA	1R, 1C	±1.2V	1MHz	Both	----	G	Yes
[127]	1CCII+ & VDIBA	1R, 1C	±0.9V	25MHz	D	----	G	Yes
[128]	4DTMOS	1C	±1V	1MHz	D	0Ω-120Ω	F	No
[132]	4NMOS transistor	1C	±1V	1MHz	D	1.2kΩ-2.4kΩ	F	No
[133]	CCCDTA	1C	±0.9V	1.5MHz	I	1MΩ-2.6MΩ	G	No
[138]	4 OTAs & 1CCII+s	2C	±0.9V	1.5MHz	I	0Ω-10kΩ	G	No
Proposed MRE-I	1OTA & 1CDBA	1C	±0.9V	1MHz	Both	1.19kΩ-1.45 MΩ	Both	Yes
Proposed MRE-II	1VDGA	1C	±0.9V	1MHz	Both	0.59kΩ-59kΩ	Both	Yes
Proposed MRE-III	1FB-VDBA	1C	±0.9V	1MHz	Both	42.6kΩ-1.5MΩ	Both	Yes

The memristance range of proposed emulators is higher than the range of memristance of reported emulators [31, 32, 34, 36, 43, 48, 70, 77, 79, 87, 94, 102, 107, 113, 115, 117, 128, 132 and 138]. It eliminates resistors present in existing emulators and operates at lower

power supply voltages. The proposed design offers the feature of electronic tunability, largely absent in existing MREs except for a few instances [46, 94, 98, 102, 109, 116, and 128].

5.6 Applications of proposed memristor emulators

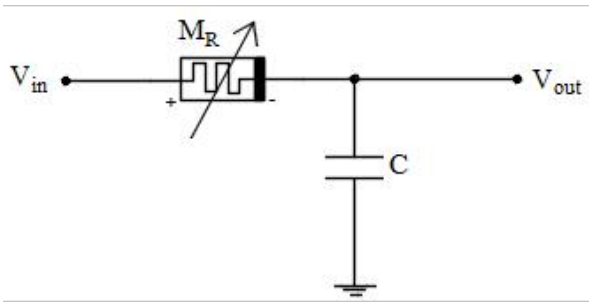
This section covers the application of memristor emulators (MREs) realized using OTA-CDBA, VDGA, and FB-VDBA. Applications of MREs in analog filters are demonstrated using the proposed emulators. The performance of proposed MREs has been verified by embedding it in the design of analog filter circuits. The performance of grounded and floating configurations of MREs realized using OTA-CDBA, VDGA, and FB-VDBA are found to be satisfactory.

5.6.1 Realization of analog filters using proposed memristor emulators

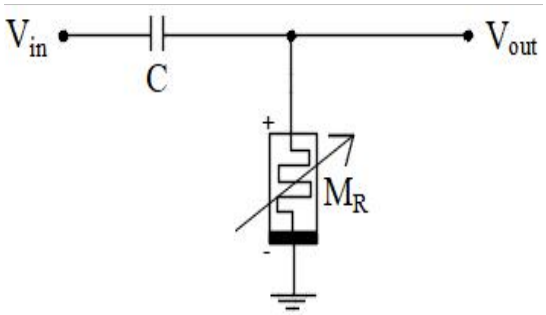
Using analog filters, the effectiveness of the proposed MREs utilizing OTA-CDBA and VDGA was confirmed. The low pass, band pass, and high pass filters are realized as illustrated in Fig. 5.29 (a), (b), and (c), respectively. The bandpass filter is realized by cascading the low pass and high pass filters. The center frequency of filters is given as

$$f_0 = \frac{1}{2\pi M_{Ravg} C} \tag{5.1}$$

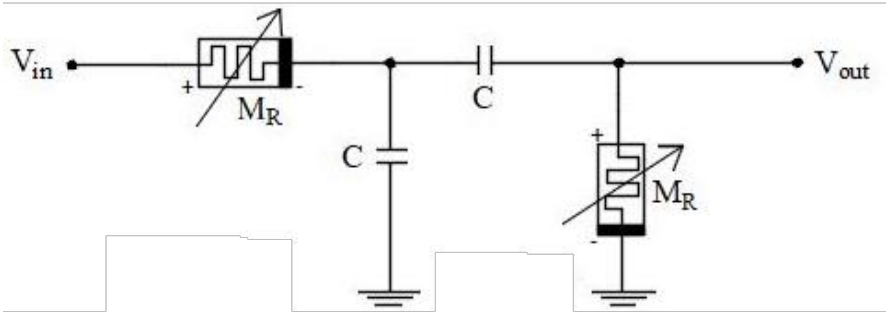
where f_0, M_{Ravg}, and C represent the center frequency, the average memristance, and the capacitor, respectively. As shown in Equation (5.1), the center frequencies of the designed filters can be substantially adjusted by altering the value of memristance (M_{Ravg}) given that the capacitor value is fixed at 1 nF for the proposed MRE.



(a)



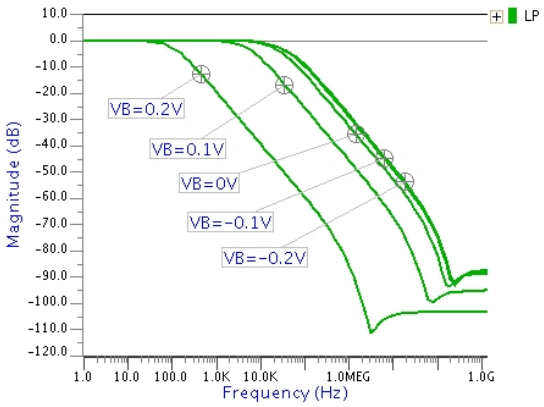
(b)



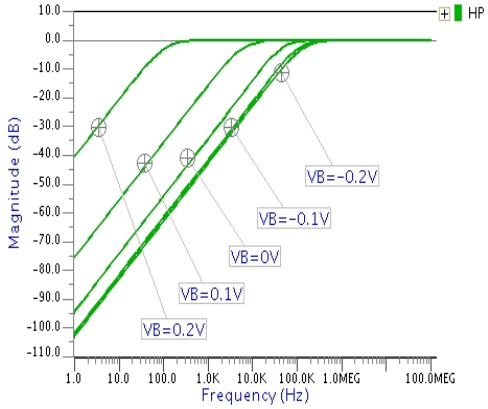
(c)

Fig. 5.29 Realization of analog filters using proposed MRE (a) low pass (b) high pass (c) band pass.

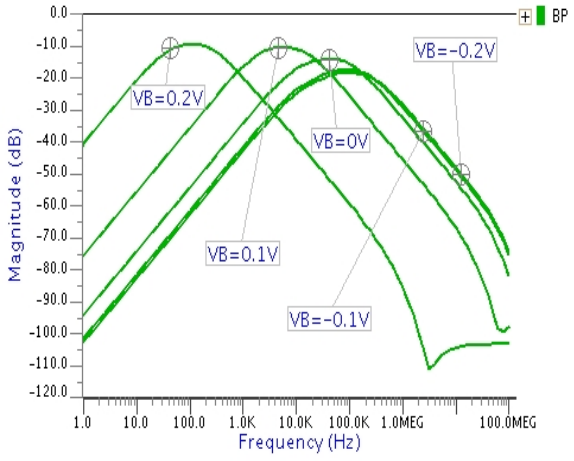
Figs. 5.30 (a) to (c) display the low pass, high pass, and band pass filter simulation results for the proposed MRE realized using OTA and CDBA, respectively.



(a)



(b)



(c)

Fig 5.30 Responses of analog filters using proposed MRE based on OTA and CDBA (a) low pass (b) high pass and (c) band pass.

It is seen from the simulation results that the center frequencies of filters are varied over a wide range of frequencies. These variations are obtained by changing the value of memristance M_R. Variation in the value of memristance (M_R) with change in the amplitude of input sinusoidal signal for biasing voltage (V_B) of -0.1 V.Bias voltages can be changed to obtain the different values of memristance (M_R). The memristance (M_R) varies from 1.54 – 2.72 kΩ for (V_B) of -0.1 V. The values of memristance (M_R) ranging from 1.19 kΩ to 1.45 MΩ are obtained by changing the bias voltage (V_B) from -0.2 V to 0.2 V. The center frequency is varied from 138 kHz to 108.6 Hz as shown in Table 5.5. The obtained results agree well with the theoretical results.

Table 5.5 Memristance range and center frequency of filters using proposed MRE based on OTA and CDBA.

Bias Voltage (V_B)	**Average value of Memristance (M_{Ravg})**	**Range of Memristance**	**Center frequency (f_0)**
-0.2V	1.19 kΩ	0.875 – 1.49 kΩ	138 kHz
-0.1V	2.06 kΩ	1.54 – 2.72 kΩ	76.95 kHz
0V	3.87 kΩ	2.76 – 5.27 kΩ	45.28 kHz
0.1V	26.82 kΩ	15.41 – 39.43 kΩ	6.08 kHz
0.2V	1.45 MΩ	1.023 - 1.884 kΩ	108.6 Hz

Simulation results of the analog filters realized by the proposed VDGA-based MRE have been obtained for various capacitor values, has shown in Table 5.6 including 10 pF, 50 pF, 100 pF, and 1000 pF.

Table 5.6 Memristance range and center frequency of filters using proposed MRE based on VDGA.

Capacitor(C)	**Average memristance (M_{Ravg})**	**Center frequency (f_0)**
10 pF	59.150 kΩ	275 .4228 kHz
50 pF	11.830 kΩ	55.8041 kHz
100 pF	5.9 kΩ	27.96834 kHz
1000 pF	0.59 kΩ	2.79683 kHz

The values of memristances (M_R) are obtained in the range of 59.150 kΩ to 0.59 kΩ. This leads to a centre frequency of 2.79683 kHz to 275.4228 kHz as indicated in Table 5.6. Fig.

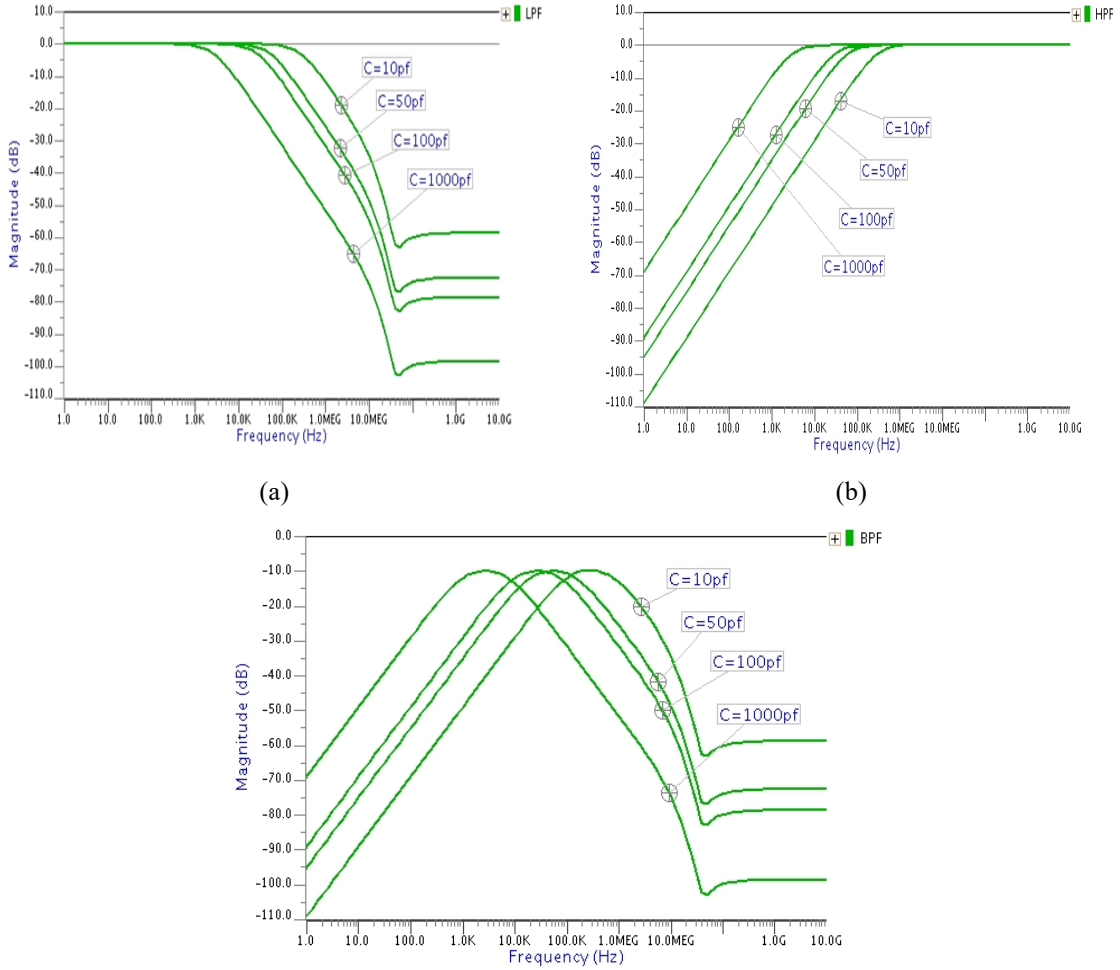


Fig 5.31 Responses of analog filters using proposed MRE based on VDGA (a) low pass (b) high pass and (c) band pass.

5.31 (a) to (c) makes it clear that average value of memristance and the value of capacitor affect the center frequencies of the filters. The obtained outcomes closely resemble the theoretical outcomes.

5.6.2 Realization of biquad filter using proposed memristor emulator

The proposed MRE based on FB-VDBA is embedded in a universal biquad filter as seen in Fig. 5.32. To evaluate its performance at high frequency, the floating resistor (R) in the universal biquad filter has been replaced with a proposed floating MRE based on FB-VDBA (M_R). The average value of memristance (M_R) is set to 1kΩ. The bias current (I_B) of voltage differencing inverted buffered amplifier (VDIBA) is selected as 100 µA whereas the values of the capacitors are selected as $C_1 = C_2 = 20$ pF.

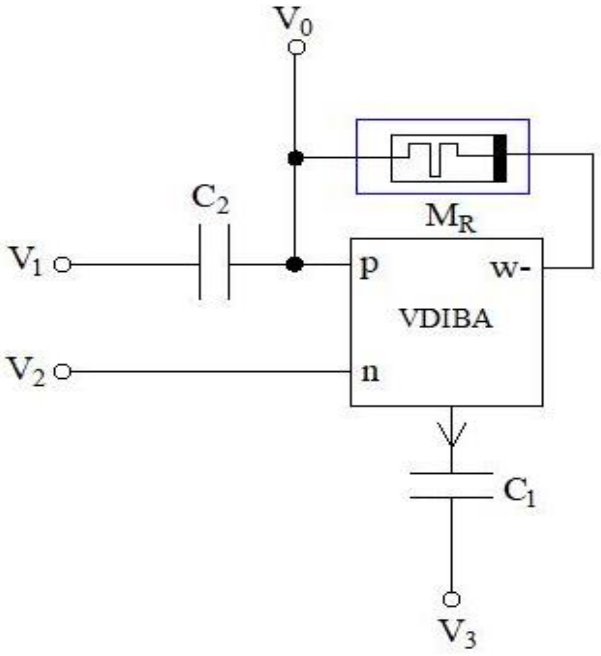


Fig. 5.32 Universal biquad filter using MRE based on FB-VDBA [212].

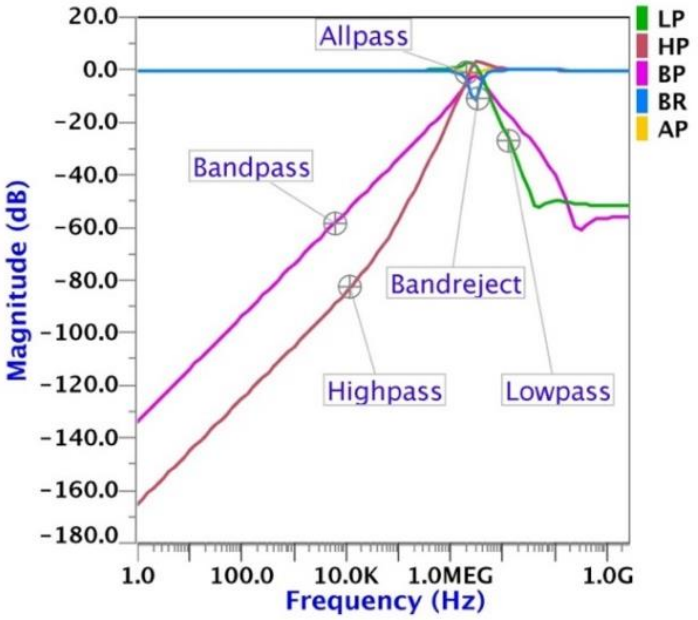


Fig. 5.33 Responses of universal biquad using memristor M_R.

The VDIBA-based universal filter's center frequency (f_0) is provided as

$$f_0 = \frac{1}{2\pi}\sqrt{\frac{g_m}{R_0 C_1 C_2}} \tag{5.2}$$

When the frequency of the sinusoidal input is raised over a specific frequency, the PHL of the MRE contracts and becomes a single-valued function. A resistor is used to represent this one-valued function. The memristor (M_R) has been used to realize universal biquad filter demonstrating the performance of proposed decremental floating memristor emulator (F-MREs). The resulting simulation results, which are shown in Fig. 5.33 exhibit behavior confirming the memristor's ability to function as a resistor at high frequencies. The center frequency (f_0) is found to be 5.7 MHz

5.7 Simulation results of proposed meminductor emulator using OTA and CDBA

This section details the simulation results of the proposed meminductor emulator (MIE), which incorporates two operational transconductance amplifiers (OTAs) and a current differencing buffered amplifier (CDBA).

5.7.1 Transient analysis

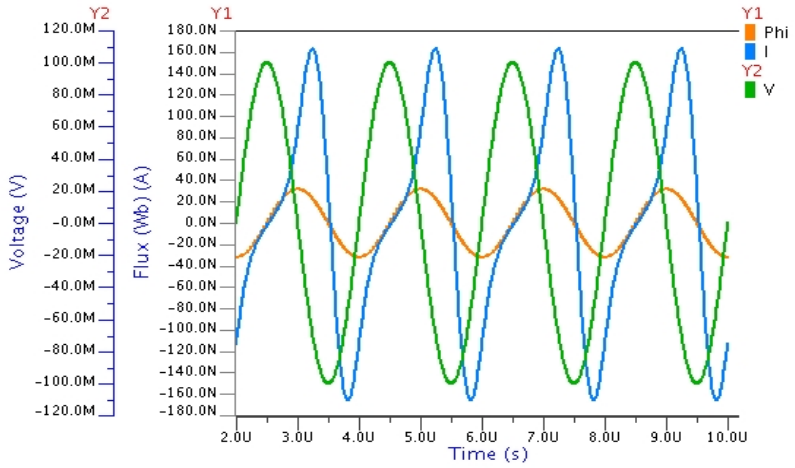
The transient analysis and PHLs have been obtained for the proposed MIE using OTA and CDBA. The OTA and CDBA has been designed using CMOS transistors. A ±0.9V voltage supply is used whereas the bias currents of CDBA are set to $I_{B1} = I_{B2} = 20$ µA. The bias voltage (VB1) for the CDBA is configured to -0.1 V.

Table 5.7 Sizes of MOSFETs for OTA and CDBA used in proposed MIE.

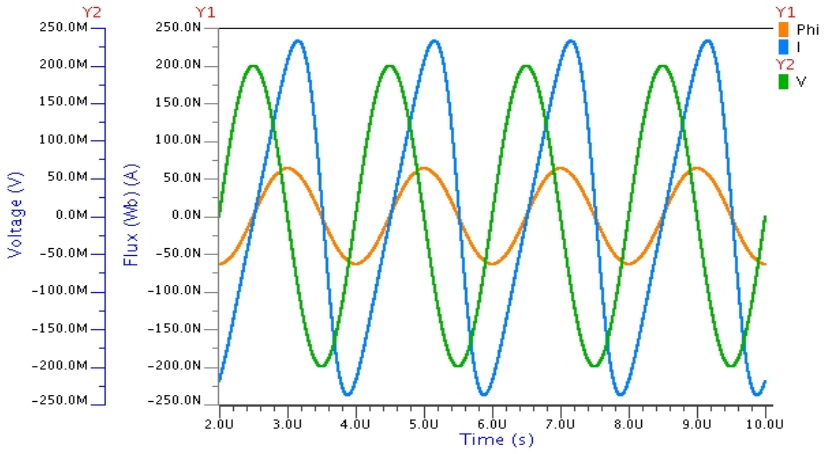
OTA			**CDBA**		
MOSFETs	**W(µm)**	**L(µm)**	**MOSFETs**	**W(µm)**	**L(µm)**
M_1-M_2	14	0.9	M_1-M_4	14.4	0.9
M_3-M_8	9	0.9	M_5-M_6	45	0.54
M_9-M_{12}	3.6	0.9	M_7-M_8	0.9	0.54
M_{13}	15	0.36	M_9-M_{10}	4.32	0.54
M_{14}-M_{15}	14	0.36	M_{11}-M_{13}	10.8	0.54
			M_{14}-M_{15}	2	0.9

The capacitors (C_1 and C_2) are set to values of 20 pF and 40 pF, respectively. These capacitor values can be fine-tuned at higher frequencies to achieve the desired pinched hysteresis

curves. The aspect ratios of the MOSFETs used in the OTA and CDBA circuit diagrams are listed in Table 5.7.

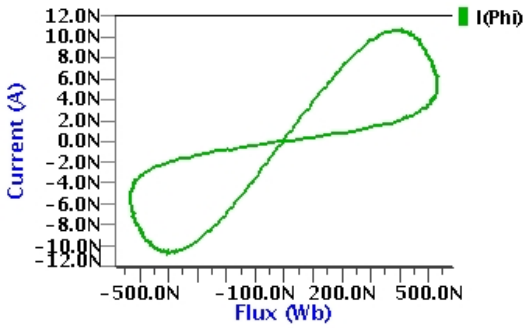


(a)

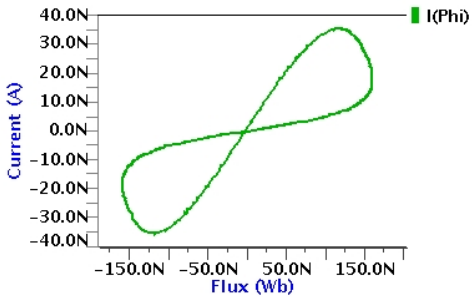


(b)

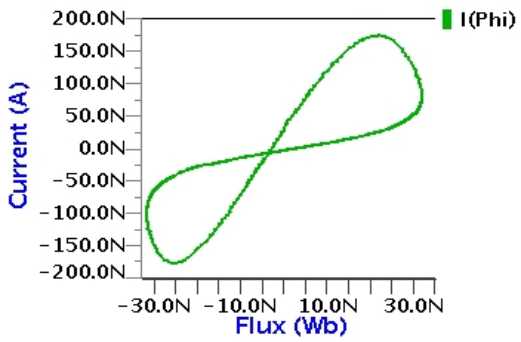
Fig. 5.34 Transient analysis of proposed MIE based on OTA and CDBA (a) grounded (b) floating.



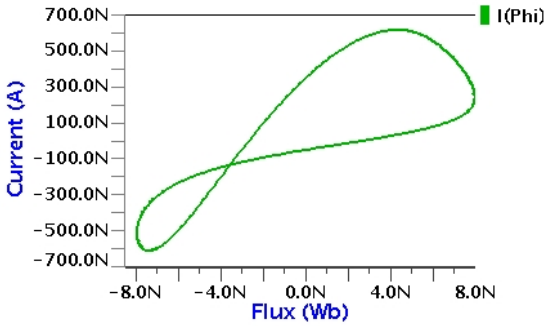
(a) 30 kHz



(b) 100 kHz

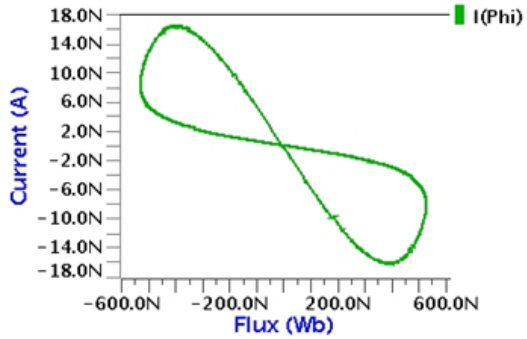


(c) 500 kHz

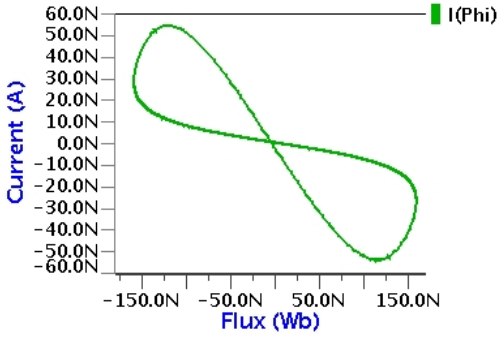


(d) 2MHz

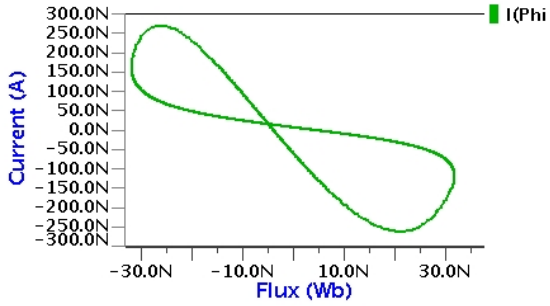
Fig. 5.35. PHLs of proposed decremental G-MIE based on OTA and CDBA.



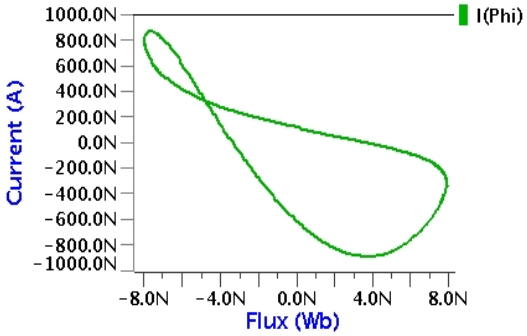
(a) 30 kHz



(b) 100 kHz

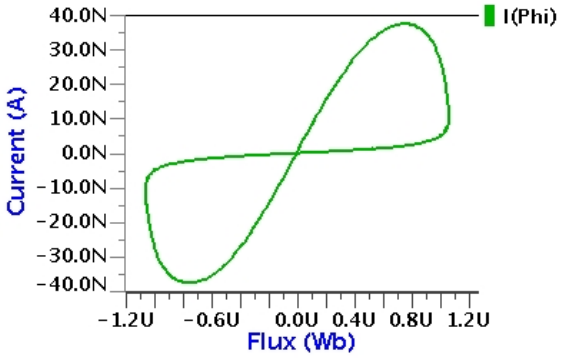


(c) 500 kHz

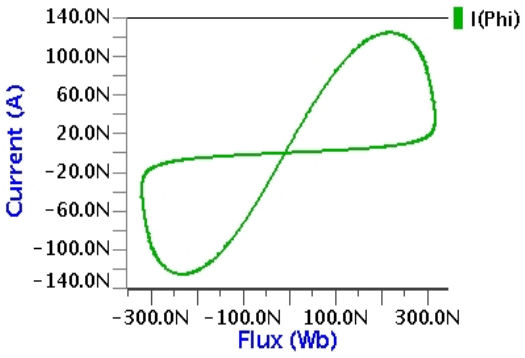


(d) 2MHz

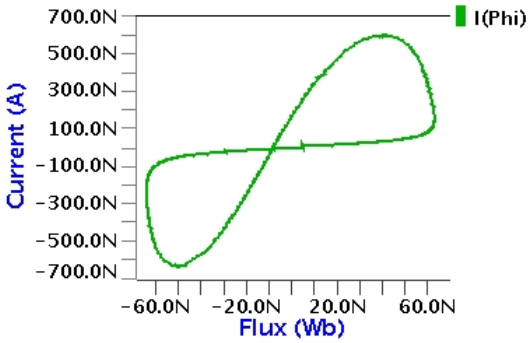
Fig. 5.36. PHLs of proposed incremental G-MIE based on OTA and CDBA.



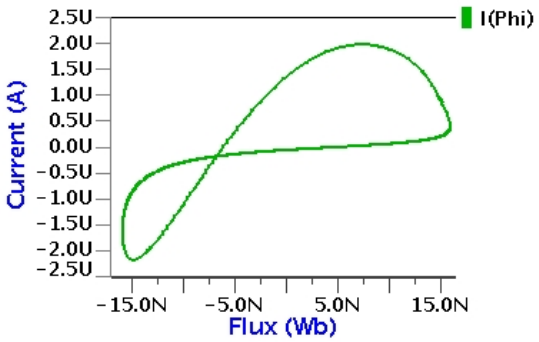
(a) 30 kHz



(b) 100 kHz

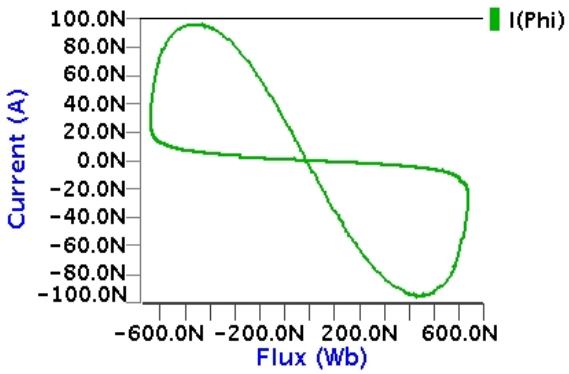


(c) 500 kHz

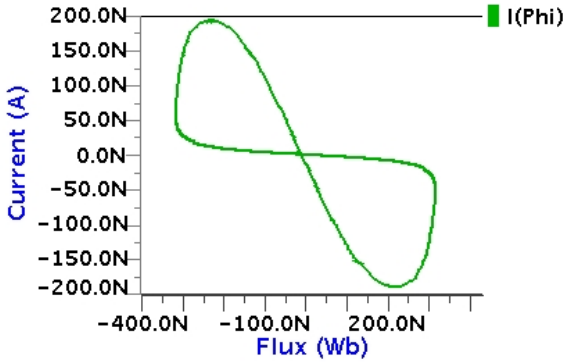


(d) 2MHz

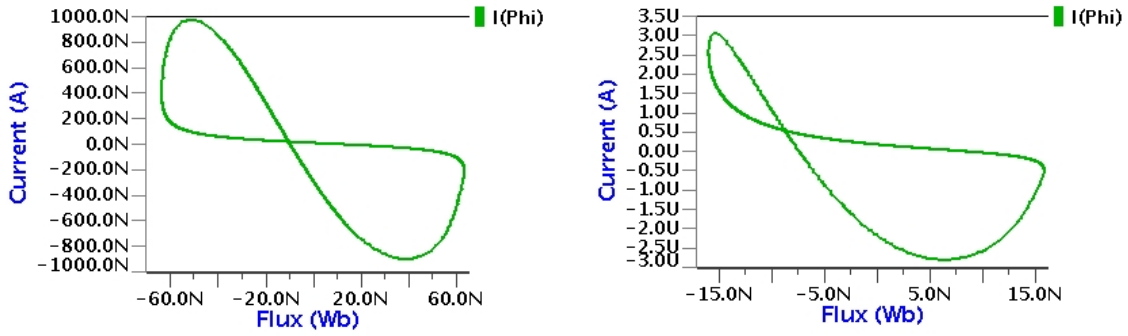
Fig. 5.37. PHLs of proposed decremental F-MIE based on OTA and CDBA.



(a) 30 kHz



(b) 100 kHz



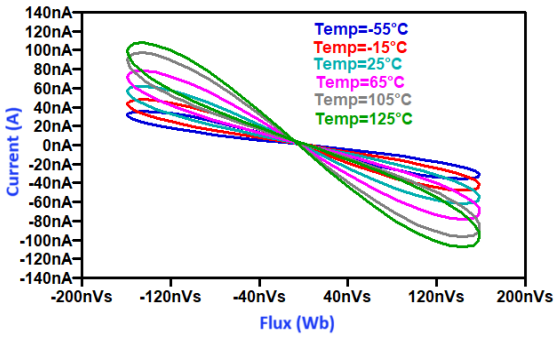
(c) 500 kHz (d) 2MHz

Fig. 5.38. PHLs of proposed incremental F-MIE based on OTA and CDBA.

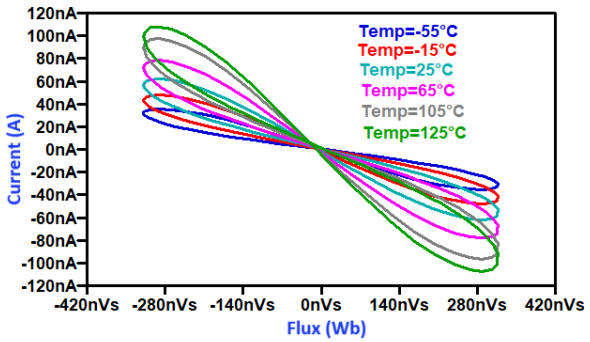
The proposed G-MIE using OTA and CDBA is analyzed with a 100 mV amplitude sinusoidal signal at a frequency of 100 kHz, as shown in Fig. 5.34 (a). The transient analysis of the proposed F-MIE using OTA and CDBA is conducted with a sinusoidal voltage of 200 mV amplitude and 100 kHz frequency, as depicted in Fig. 5.34 (b). Additionally, the PHLs between flux and current for the decremental and incremental G-MIEs using OTA and CDBA are measured by applying a 100 mV amplitude sinusoidal signal across various frequencies from 30 kHz to 2 MHz, as illustrated in Figs. 5.35 (a) to (d) and 5.36 (a) to (d), respectively. In addition, the PHL is assessed over a frequency range from 30 kHz to 2 MHz, as depicted in Figs. 5.37 and 5.38 for the decremental and incremental F-MIEs using OTA and CDBA.

5.7.2 Temperature analysis

The temperature analysis of the proposed decremental G-MIES and F-MIES using OTA and CDBA was conducted by applying a 100 mV amplitude sinusoidal input signal at a



(a)



(b)

Fig. 5.39 Temperature analysis of proposed MIE using OTA and CDBA. (a) grounded and (b) floating.

frequency of 50 kHz while varying the temperature from -55°C to 125°C.The results of this temperature analysis are presented in Fig. 5.39. It is observed that the PHL remains undistorted despite of the temperature variations. It can be concluded from the results of MIEs that the proposed circuits can function satisfactorily over a wide temperature range.

5.7.3 Non-volatility test

The non-volatility test of proposed G-MREs and F-MREs using OTA and CDBA are assessed by applying an input pulse with an amplitude of 5V and a frequency of 500 kHz. The responses which are the currents through capacitor C_1 of the proposed decremental G-MREs and F-MREs to the pulse input are illustrated in Figs. 5.40 and 5.41. Both responses confirm the presence of memory in the MIEs as they retain their values during the 'OFF' periods of the input pulses which are obtained during the 'ON' periods.

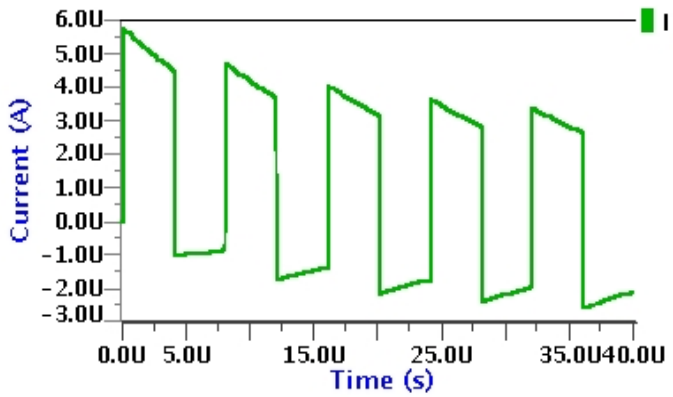


Fig. 5.40 Non-volatility test of proposed G-MIE based on OTA and CDBA.

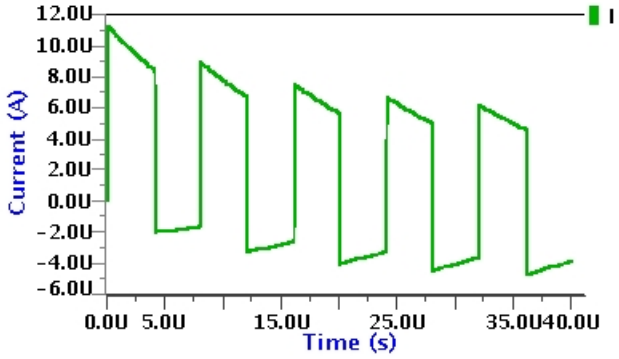
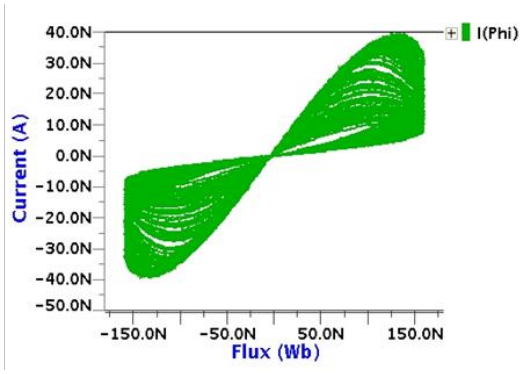


Fig. 5.41 Non-volatility test of proposed F-MIE based on OTA and CDBA.

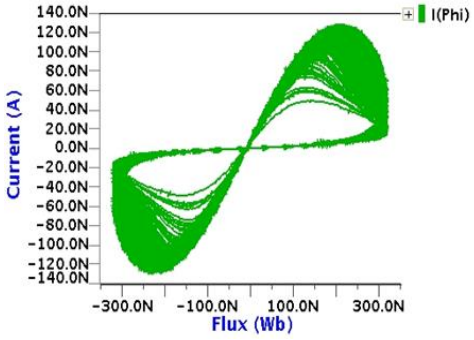
In the subsequent pulses, the values decrease or increase for the decremental or incremental G-MREs and F-MREs.

5.7.4 Monte Carlo analysis

A Monte Carlo analysis has been carried out using a frequency of 50 kHz for 200 runs to assess the performance of the proposed MIEs using OTA and CDBA after variations in device parameters.



(a)



(b)

Fig. 5.42 Monte Carlo analysis of proposed MIE based on OTA and CDBA (a) grounded (b) floating.

The purpose of this investigation is to find out how reliable the proposed designs are after Gaussian random variations in the aspect ratios of MOSFET and threshold voltages. Fig. 5.42 (a) and (b) show the PHLs for the proposed MIE using OTA and CDBA. These findings consistently validate that the PHLs maintain for various cycles.

5.8 Simulation results of the proposed meminductor emulators using VDGA and CDBA

In this section, the simulation results of the proposed meminductor emulator (MIE) employing a voltage differencing gain amplifier (VDGA) and a current differencing buffered amplifier (CDBA) has been discussed.

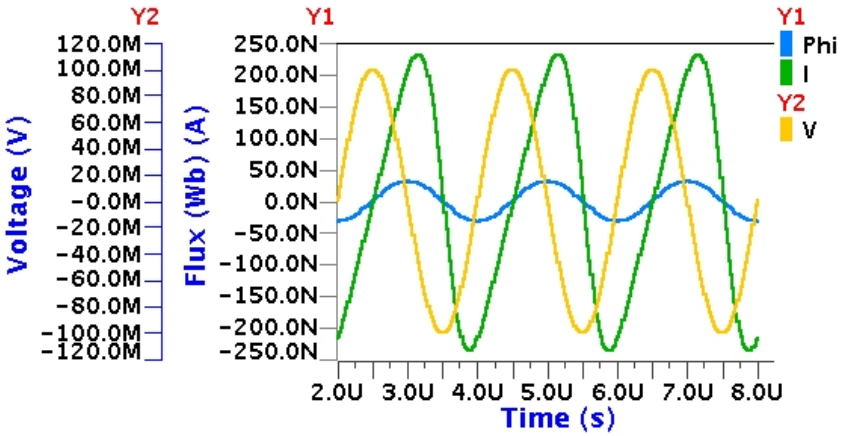
5.8.1 Transient analysis

The transient analysis and PHLs for the proposed MIE using VDGA and CDBA were conducted with a supply voltage of ±0.9V for both VDGA and CDBA. Table 5.8 lists the aspect ratios of the MOSFETs used in these circuits. The bias currents are 80 µA for I_{B1}, 100 µA for I_{B2}, and 20 µA for I_{B3}-I_{B4}. Capacitors C_1 and C_2 are set at 10 pF and 40 pF, respectively, and the bias voltage V_{B1} is -0.1V.

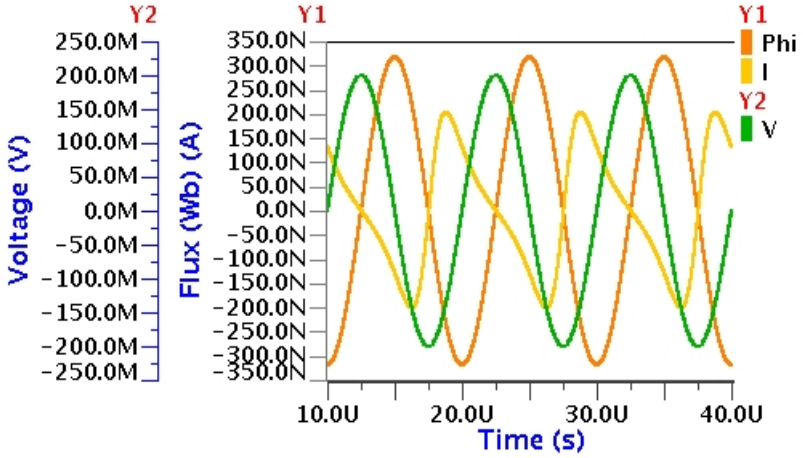
Table 5.8. Sizes of MOSFETs for VDGA and CDBA.

VDGA			CDBA		
MOSFETs	**W(µm)**	**L(µm)**	**MOSFETs**	**W(µm)**	**L(µm)**
M_1, M_2, M_{12}, M_{13}, M_{24}, M_{25}	16	1	M_1-M_2	0.8	0.5
M_6-M_9, M_{14}-M_{19}, M_{26}-M_{29}	9	1	M_3-M_5	10	0.5
M_{10}, M_{11}, M_{20}, M_{21}, M_{22}, M_{23}, M_{30}, M_{31}	4	1	M_6-M_7	4	0.5
M_3, M_4	14	0.36	M_8-M_9	42.5	0.36
M_5	15	0.36	M_{10}-M_{13}	32	2

To perform the transient analysis, a sinusoidal signal with an amplitude of 120 mV and a frequency of 100 kHz is applied to the input terminal of the proposed G-MIEs and F-MIEs, as shown in Figs. 5.43(a) and (b). The PHLs of these G-MIEs and F-MIEs are depicted in Figs. 5.44 and 5.45 for frequencies ranging from 10 kHz to 2 MHz. In Figs. 5.44 (a)-(d), it is observed that the loop area diminishes as the frequency increases. The proposed MIE operates effectively up to 2 MHz, beyond which the PHLs start to distort. Fig. 5.45 (a)-(d) displays the PHLs of the proposed incremental MIE for frequencies between 10 kHz and 2 MHz, using a sinusoidal signal with a 100 mV amplitude The PHLs are obtained for



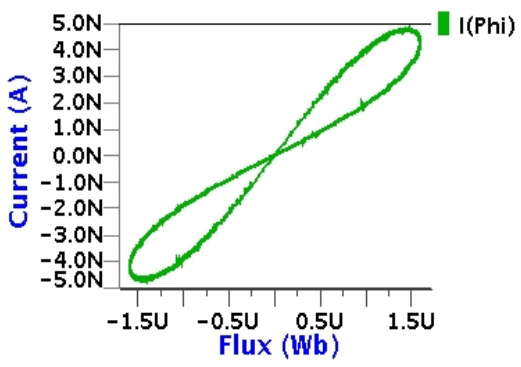
(a)



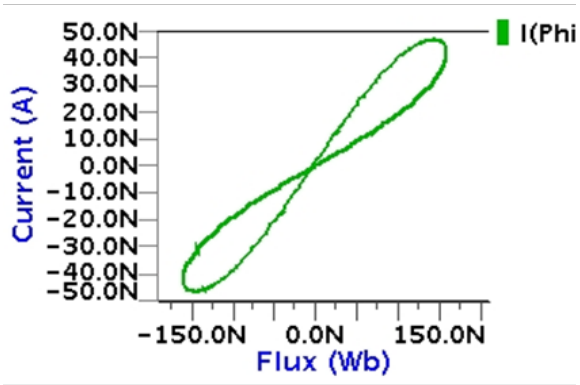
(b)

Fig. 5.43. Transient analysis of proposed MIE based on VDGA and CDBA(a) grounded (b) floating.

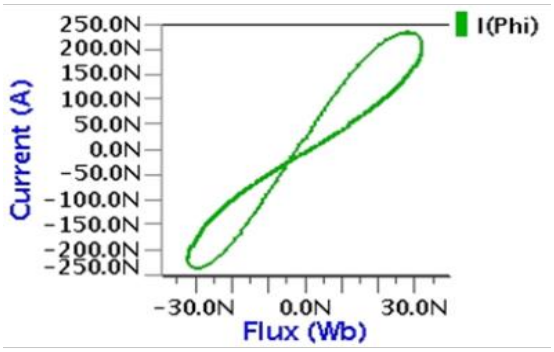
frequencies between 30 kHz and 2 MHz for the decremental and incremental F-MIE as shown in Figs. 5.46 (a) to (d) and 5.47 (a) to (d), respectively.



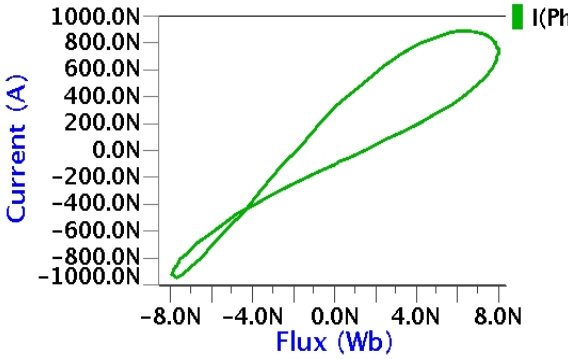
(a) 10 kHz



(b) 100 kHz

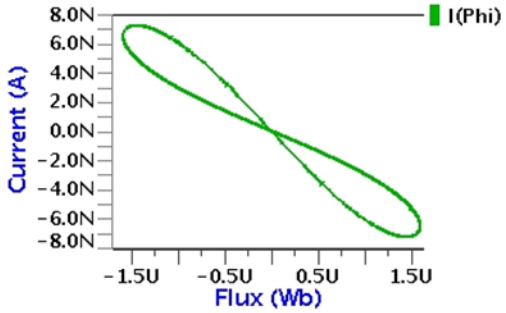


(c) 500 kHz

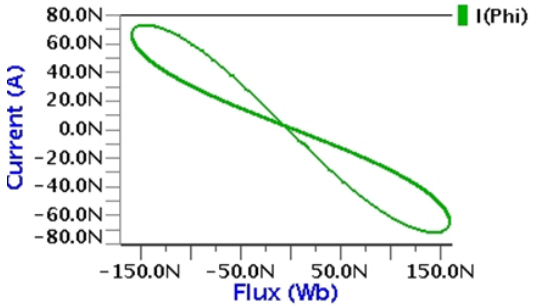


(d) 2MHz

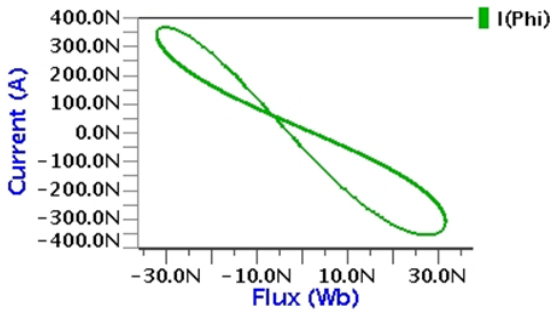
Fig. 5.44. PHLs of proposed decremental G-MIE based on VDGA and CDBA.



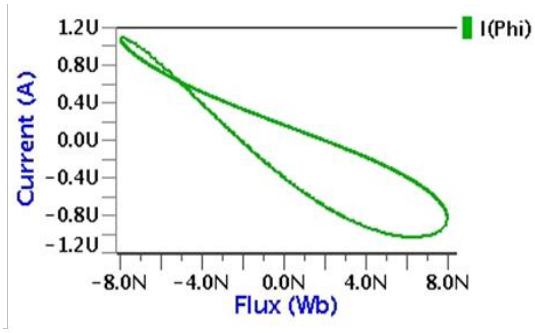
(a) 10 kHz



(b) 100 kHz

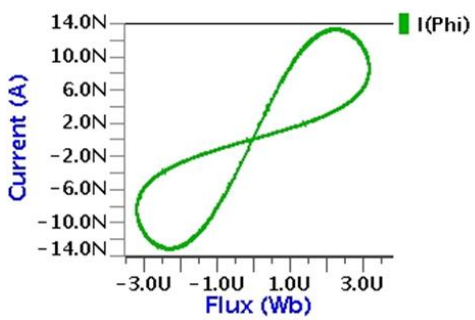


(c) 500 kHz

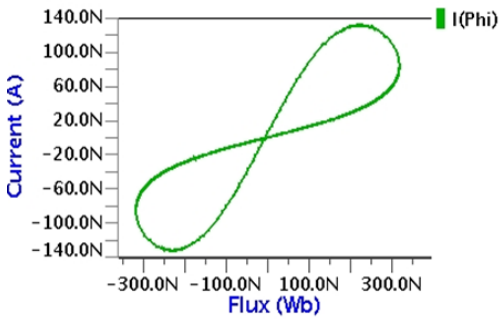


(d) 2 MHz

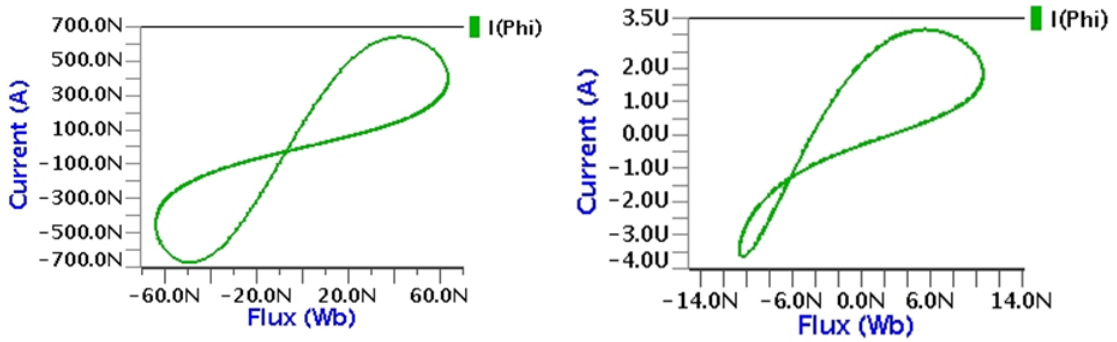
Fig. 5.45. PHLs of proposed incremental G-MIE based on VDGA and CDBA.



(a) 10 kHz

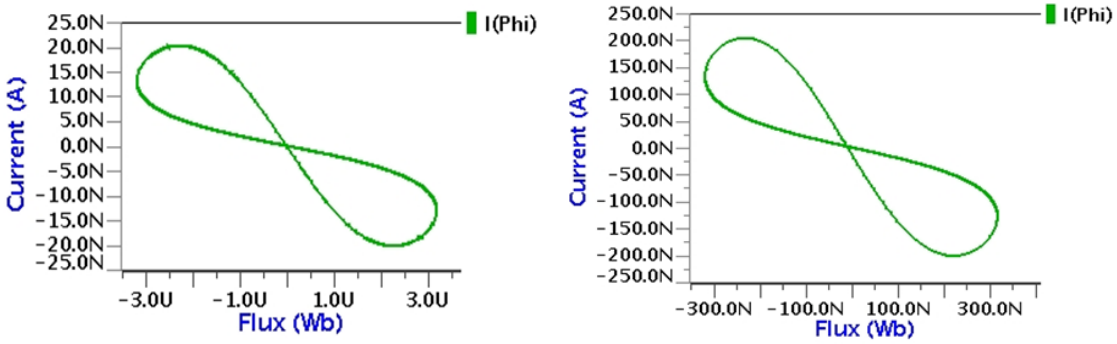


(b) 100 kHz

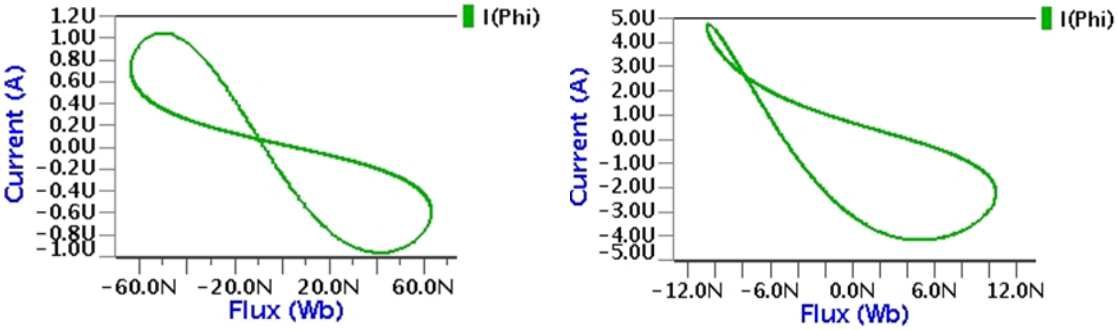


(c) 500 kHz (d) 3 MHz

Fig. 5.46. PHLs of proposed decremental F-MIE based on VDGA and CDBA.



(a) 10 kHz (b) 100 kHz

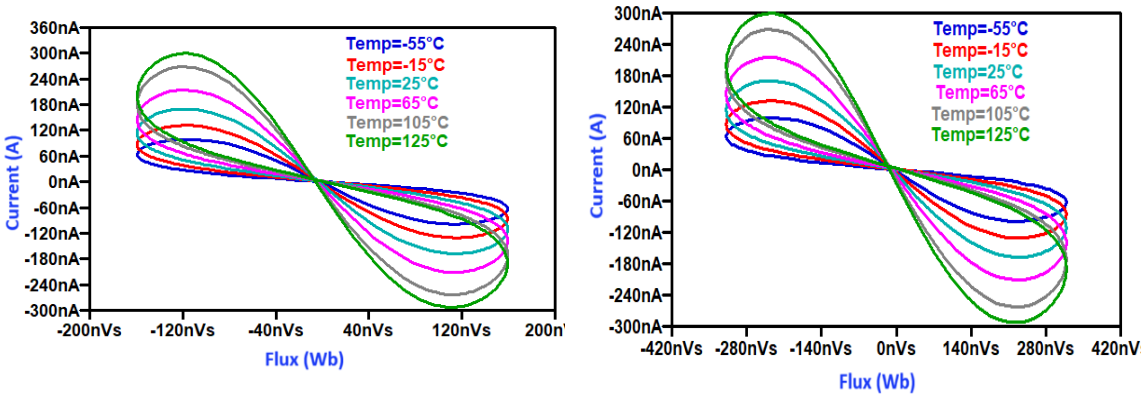


(c) 500 kHz (d) 3 MHz

Fig. 5.47. PHLs of proposed incremental F-MIE based on VDGA and CDBA.

5.8.2 Temperature analysis

Generally, the threshold voltage (V_{TH}), carrier mobility (μ), and velocity saturation get changed with temperature variations. As a result, the emulators must operate effectively with very negligible effect on these variations. A sinusoidal signal characterized by a 100 mV amplitude and a 100 kHz frequency is employed in temperature analysis. Fig. 5.48 illustrates the satisfactory performance of the proposed G-MIE utilizing VDGA and CDBA across



(a) (b)

Fig. 5.48 Temperature analysis of proposed MIE based on VDGA and CDBA (a) grounded and (b) floating.

temperatures ranging from -55ºC to 125ºC. Notably, the pinched hysteresis is maintained over a spectrum of temperature variations.

5.8.3 Non-volatility test

The operational characteristics of the proposed MIE in its non-volatile state have been investigated. Fig. 5.49 demonstrates a reduction in the output current through capacitor C_2 when the signal is 'ON' while it remains relatively constant when the signal is 'OFF'. This behaviour suggests its ability to retain memory during the 'OFF' phase, substantiating its non-volatile attributes. A comparable trend is evident in Fig. 5.50 further validating the memory-preserving properties of the proposed G-MIE and F-MIE.

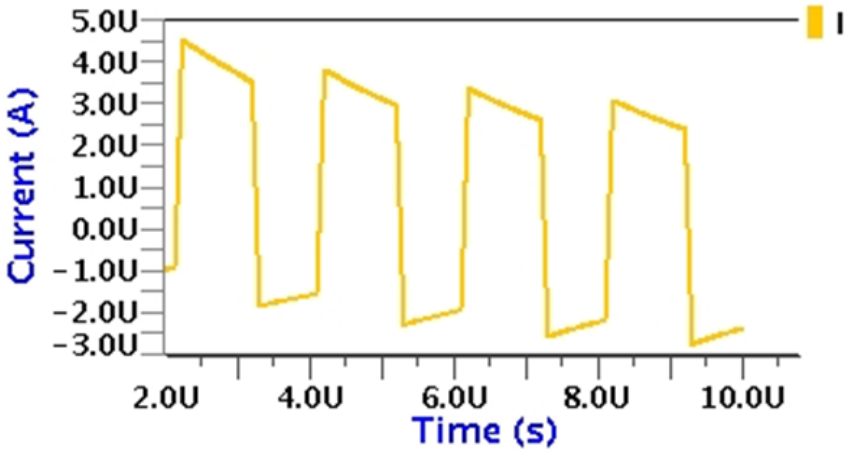


Fig. 5.49. Non-volatility test of proposed G-MIE based on VDGA and CDBA.

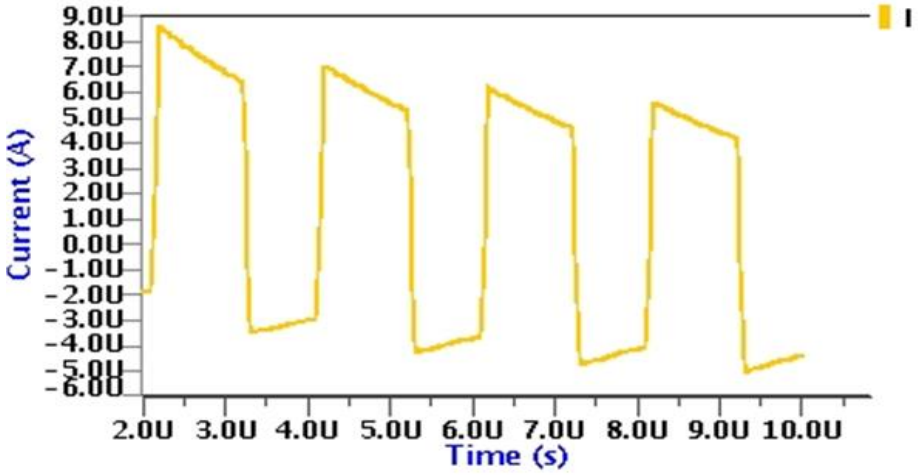
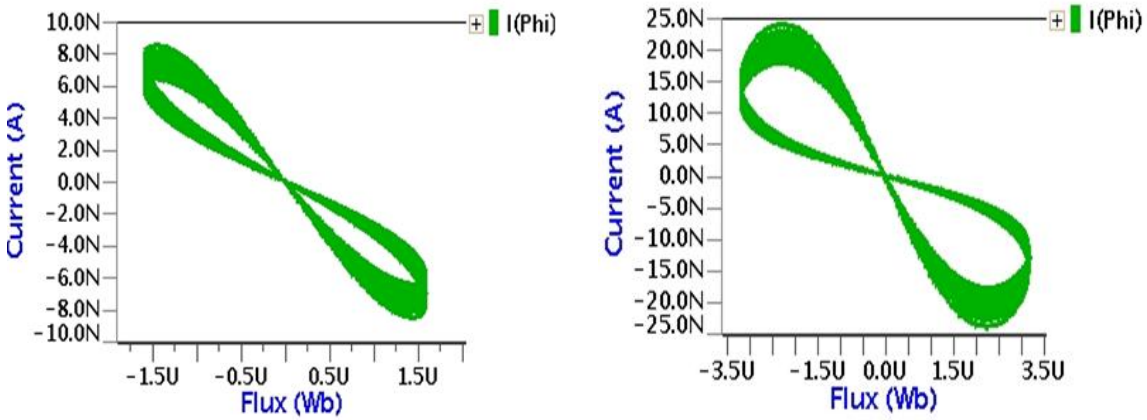


Fig. 5.50. Non-volatility test of proposed F-MIE based on VDGA and CDBA.

5.8.4 Monte Carlo analysis

The robustness of the proposed MIE using VDGA and CDBA is assessed through Monte Carlo analysis, as shown in Fig. 5.51 (a) and (b). This analysis includes 200 runs with 10 kHz frequency and 100 mV amplitude signals. The results indicate that the meminductor's hysteresis loop is pinched at the origin, confirming the satisfactory performance of the proposed meminductor. Additionally, with a 200 mV input signal at a frequency of 100 kHz, both the decremental and incremental F-MIEs show satisfactory performance, as illustrated in Fig. 5.51.



(a) (b)

Fig. 5.51 Monte Carlo analysis of proposed MIE based on VDGA and CDBA (a) grounded (b) floating.

5.9 Simulation results of the proposed meminductor emulator using VDTA and CDBA

This section presents the simulation results of the proposed MIE employing a voltage differencing transconductance amplifier (VDTA) and a current differencing buffered amplifier (CDBA).

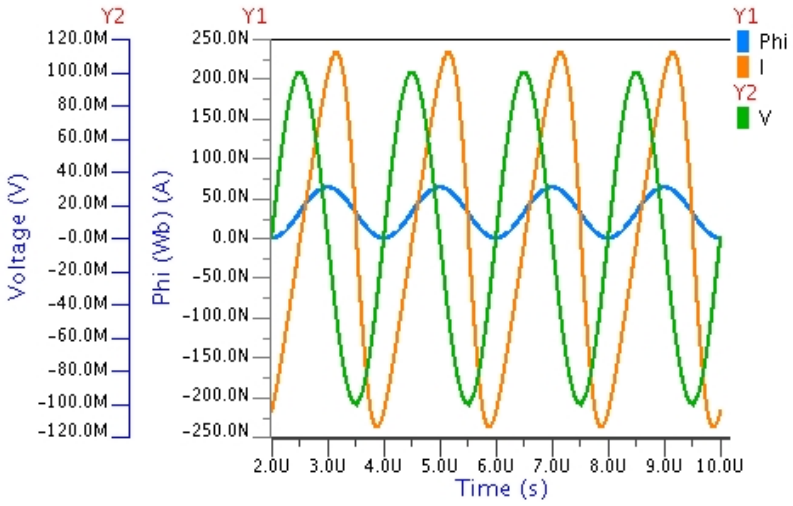
5.9.1 Transient analysis

The transient analysis and PHLs for the proposed MIE using VDTA and CDBA have been conducted. A supply voltage of ±0.9V is employed for implementing the proposed MIEs with VDTA and CDBA. The bias currents for the CDBA are set at I_{B1} = I_{B2} = 20 µA, with the bias voltages (V_{B1}) and (V_{B2}) adjusted to -0.1 V for VDTA and CDBA, respectively.

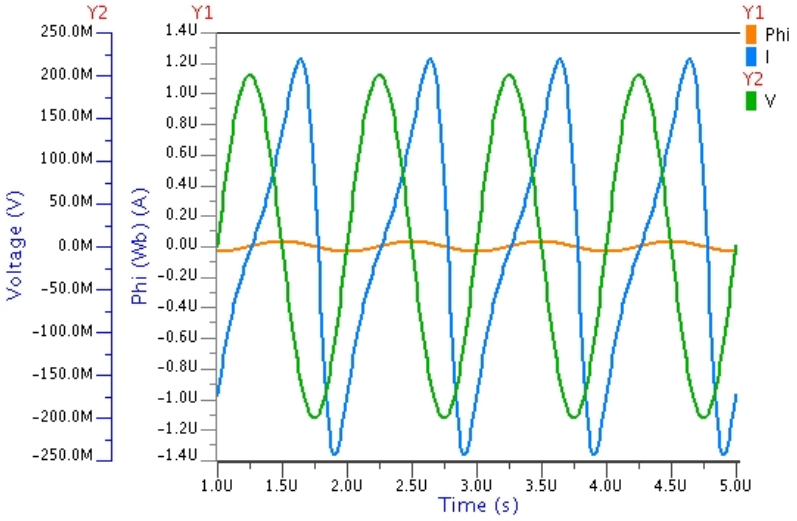
Table 5.9 Sizes of MOSFETs for VDTA and CDBA.

VDTA			CDBA		
MOSFETs	**W(µm)**	**L(µm)**	**MOSFETs**	**W(µm)**	**L(µm)**
M_1-M_4	52.4	1.4	M_1, M_2	0.8	0.5
M_5-M_8	32.2	1.4	M_3, M_4	4	0.5
M_9-M_{12}	42	1.4	M_5-M_7	10	0.5
M_{13}-M_{16}	17.5	1.4	M_{11}, M_8	42.5	0.36
			M_9, M_{10}, M_{12}, M_{13}	32	2

Capacitor values C_1 and C_2 are chosen as 20 pF and 40 pF, respectively, and can be fine-tuned at higher frequencies to achieve pinched hysteresis curves. The aspect ratios of the MOSFETs used in the VDTA and CDBA designs are listed in Table 5.9.



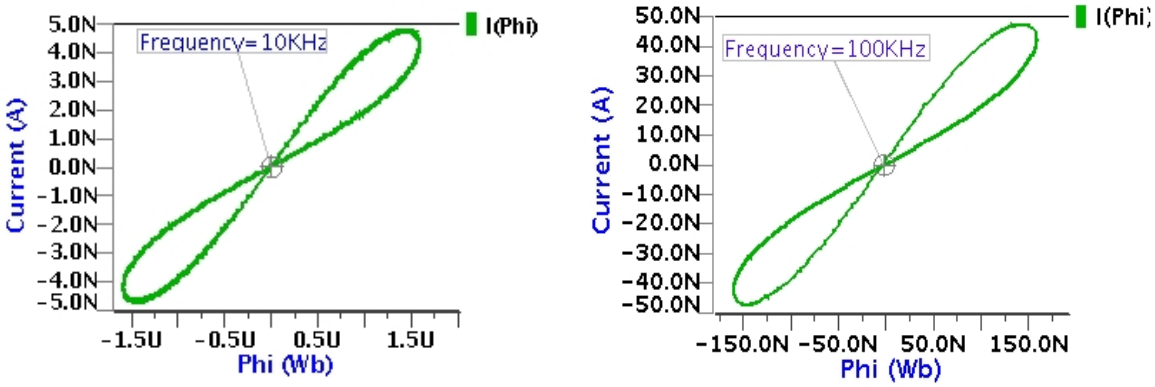
(a)



(b)

Fig. 5.52 Transient analysis of proposed MIE based on VDTA and CDBA (a) grounded (b) floating.

The proposed decremental and incremental G-MIEs are analyzed with a sinusoidal input signal of 120 mV amplitude at 500 kHz. The resulting transient waveforms for the input voltage, flux, and current are shown in Fig. 5.52 (a). Additionally, the transient analysis of the proposed F-MIE is performed with a 250 mV amplitude sinusoidal voltage at 500 kHz,as depicted in Fig. 5.52 (b).Pinched hysteresis loops (PHL) are obtained by applying a sinusoidal signal with an amplitude of 120 mV for the range of frequencies varies from 10 kHz to 2 MHz for the suggested decremental and incremental G-MIEs. The obtained PHLs for decremental and incremental G-MIEs are shown in Figs. 5.53 (a)-(e) and 5.54 (a)-(e), respectively. Figs. 5.53 (a)-(e) and 5.54 (a)-(e) reveals the reduction in the loop area when frequency is increased.



(a) (b)

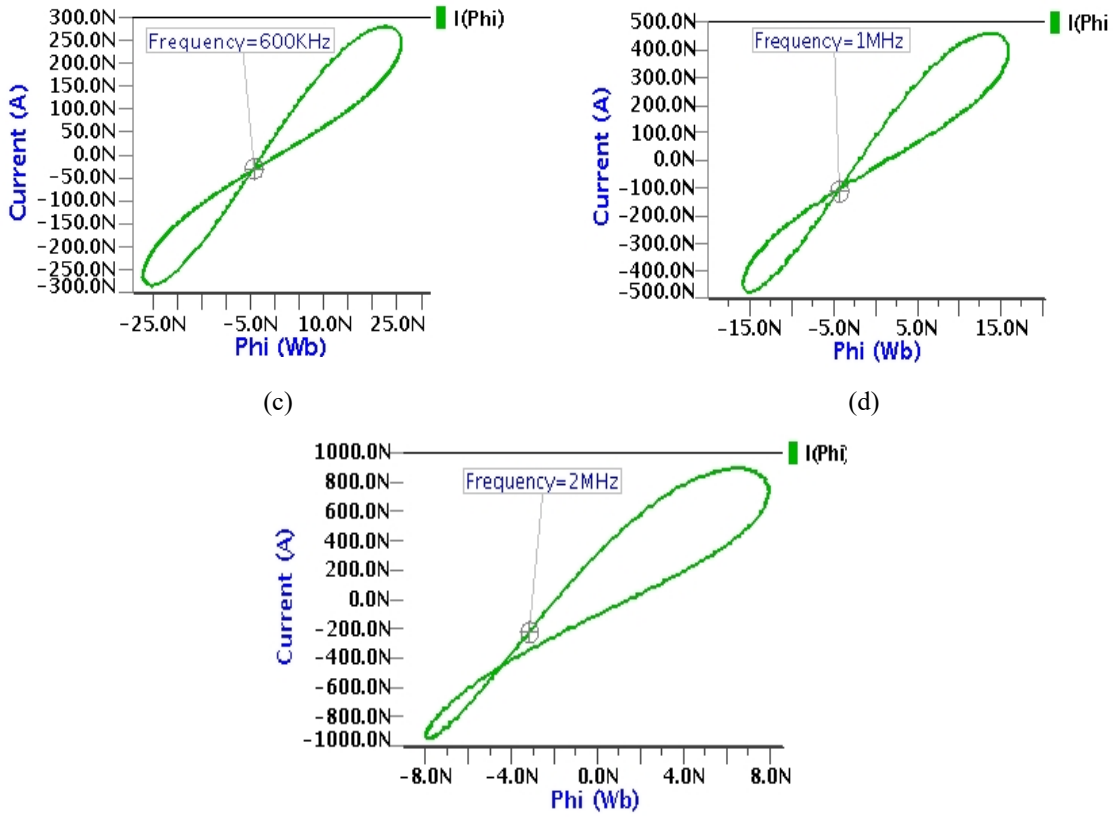
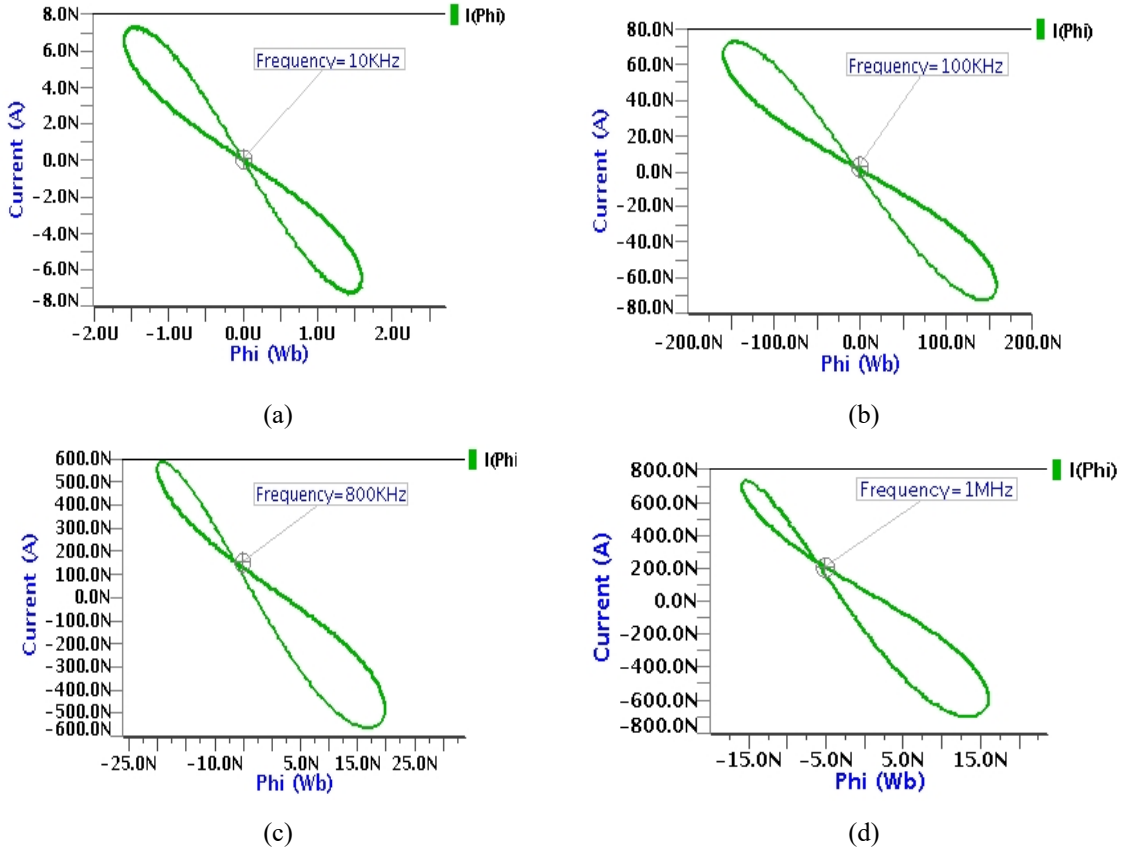
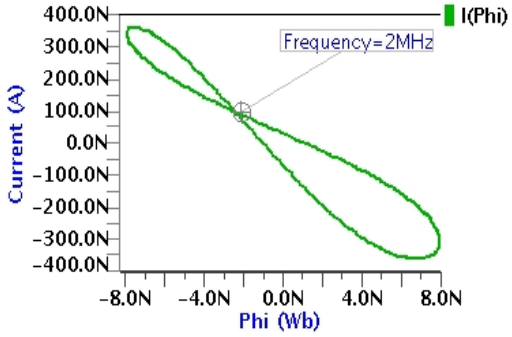


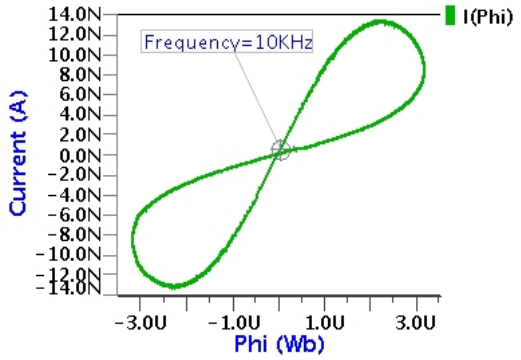
Fig. 5.53. PHLs of proposed decremental G-MIE based on VDTA and CDBA.



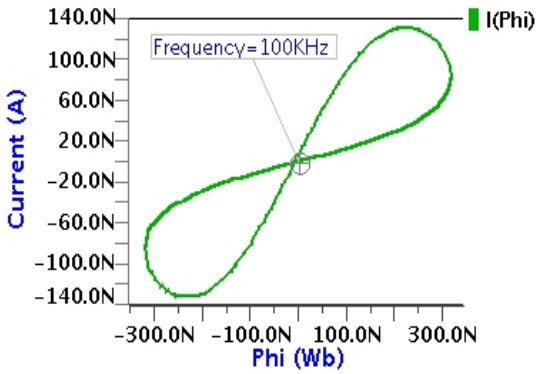


(e)

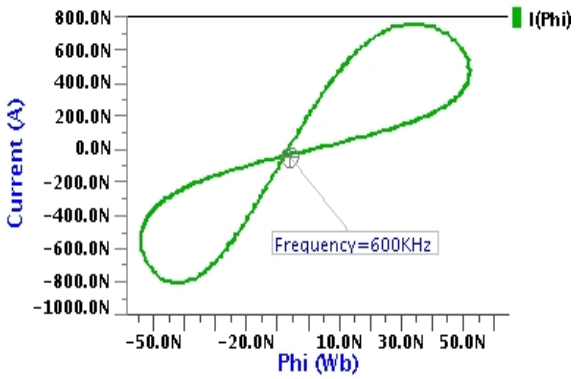
Fig. 5.54 PHLs of proposed incremental G-MIE based on VDTA and CDBA.



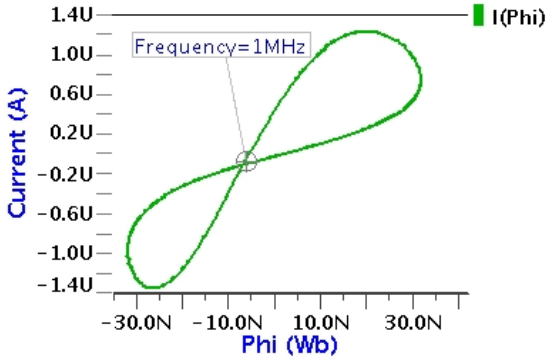
(a)



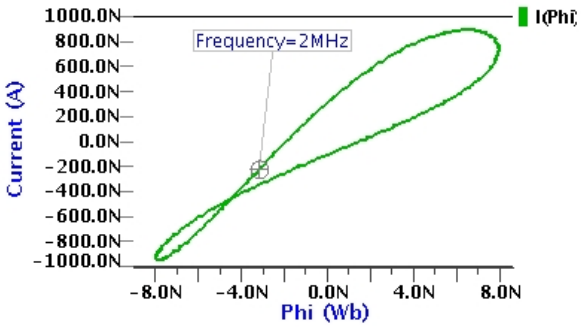
(b)



(c)



(d)



(e)

Fig. 5.55 PHLs of proposed decremental F-MIE based on VDTA and CDBA.

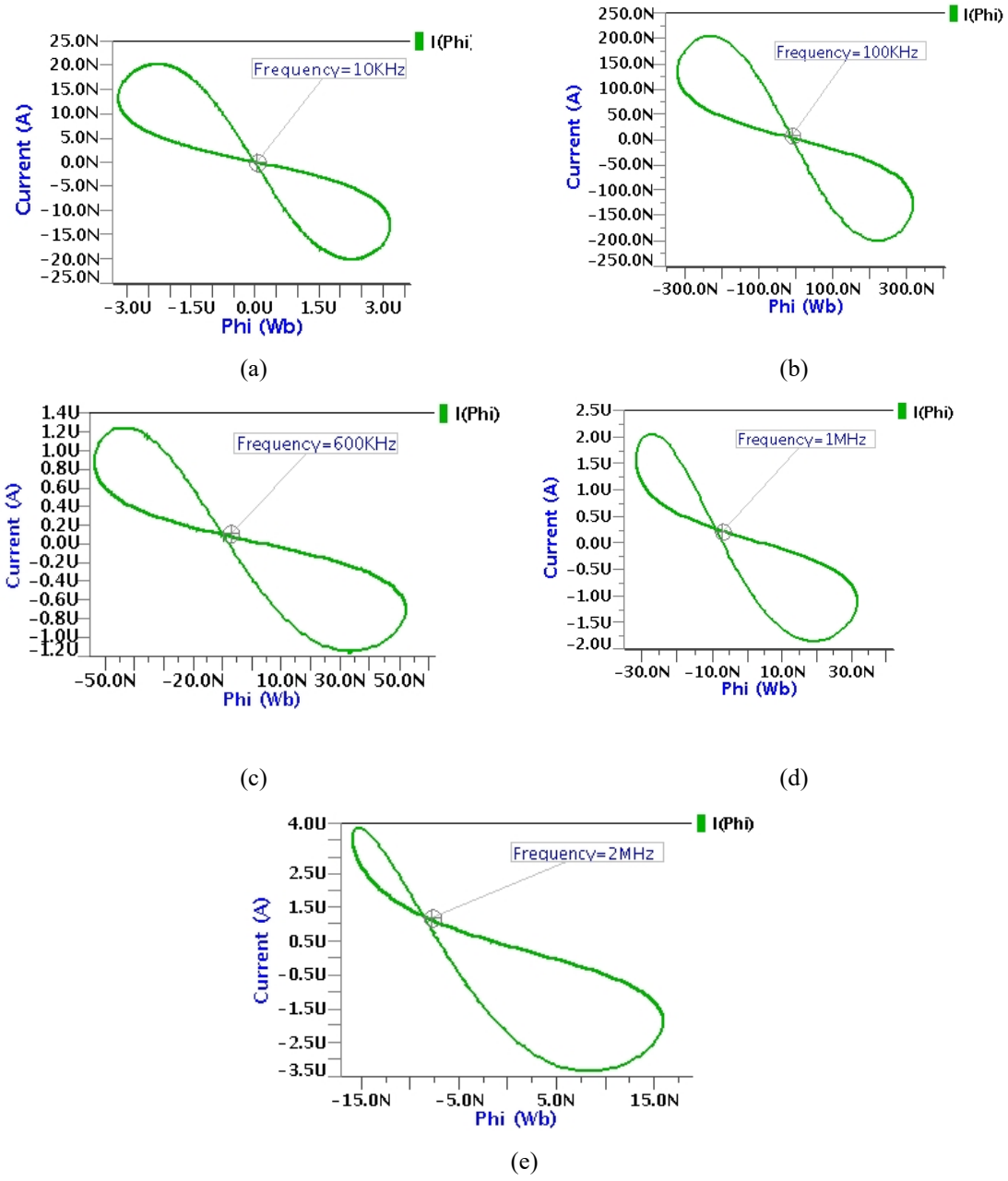
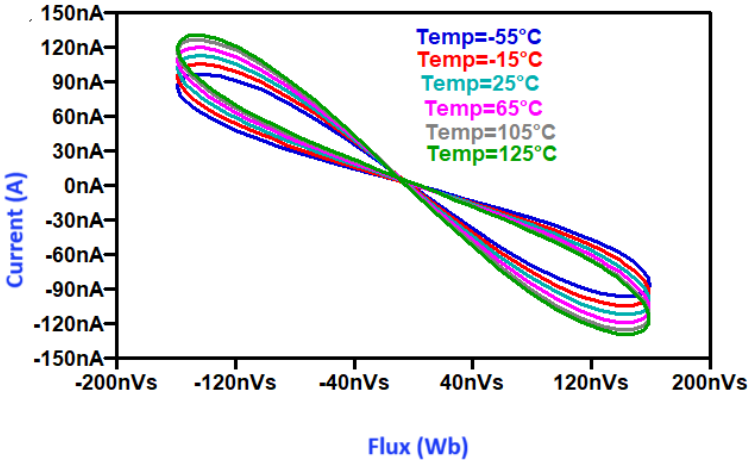
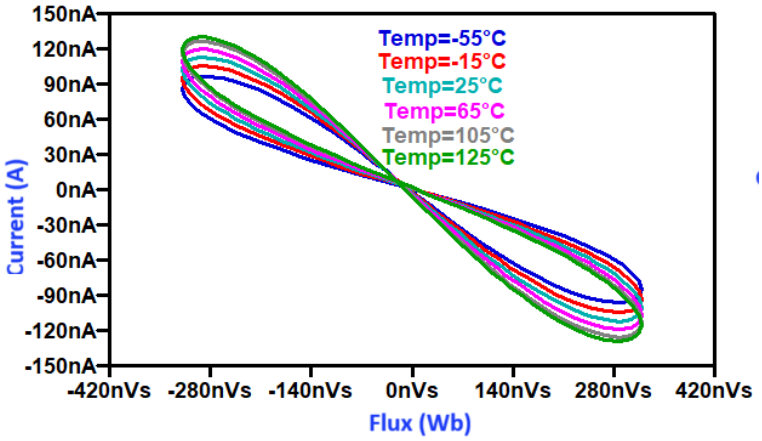


Fig. 5.56. PHLs of proposed incremental F-MIE based on VDTA and CDBA.

The PHL is sustained up to 2 MHz, albeit the pinched point is shifted at higher frequencies and the loop deforms at frequencies higher than 2 MHz. The resulting PHLs of the F-MIE are shown in Figs. 5.55 (a) to (e) and 5.56 (a) to (e). The loop areas decrease as the frequency increases. It can be observed by examining the data on the x-axis of Figs. 5.55 (a) to (e) and 5.56 (a) to (e). The loops display non-symmetrical characteristics because the pinched point is shifted away from the midpoint. Consequently, the loops become distorted for frequencies exceeding 2 MHz, as depicted in Fig. 5.56 (e).



(a)



(b)

Fig. 5.57 PHLs of proposed decremental MIE based on VDTA and CDBA for different temperatures (a) grounded (b) floating.

5.9.2 Temperature analysis

A temperature analysis is carried out to evaluate the performances of G-MIEs and F-MIEs performance at different temperatures by applying an input sinusoidal signal with V_m = 100 mV and frequency = 100 kHz while temperature is varied between -55°C and +125°C. The obtained results are shown in Fig. 5.57 (a).

It shows that the pinched hysteresis curves are not deformed after variation in the temperature. As a result, the temperature analysis is found to be satisfactory for the suggested decremental G-MIEs. The temperature analysis is also carried out for the proposed G-MREs and F-MREs, spanning a temperature range from -55°C to +125°C. The simulation results

depicted in Fig. 5.57 (b) demonstrate the satisfactory performance of the proposed decremental F-MIEs across varying temperatures.

5.9.3 Non-volatility test

The performances of the proposed G-MIEs and F-MIEs are assessed by applying an input pulse with an amplitude of 5V and a frequency of 500 kHz.

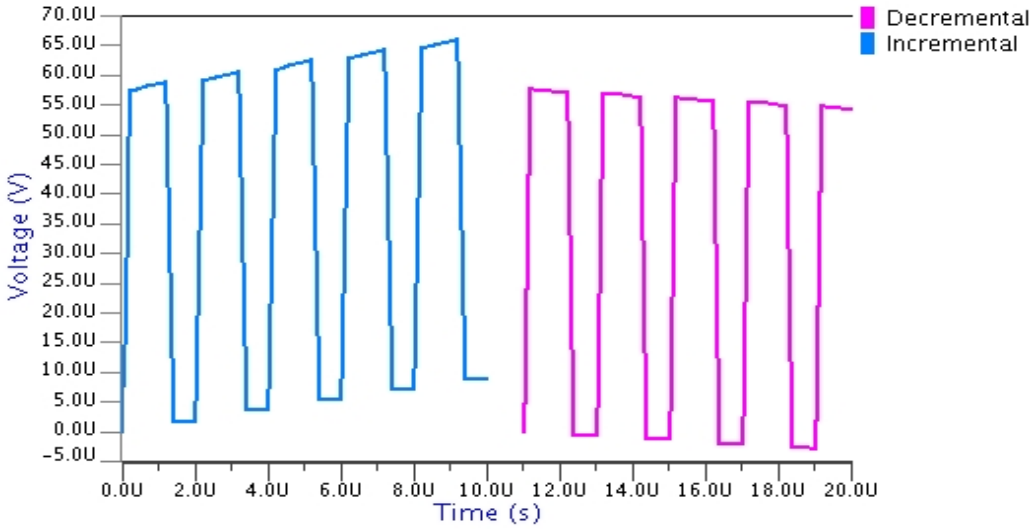


Fig. 5.58. Non-volatility test of proposed G-MIE based on VDTA and CDBA.

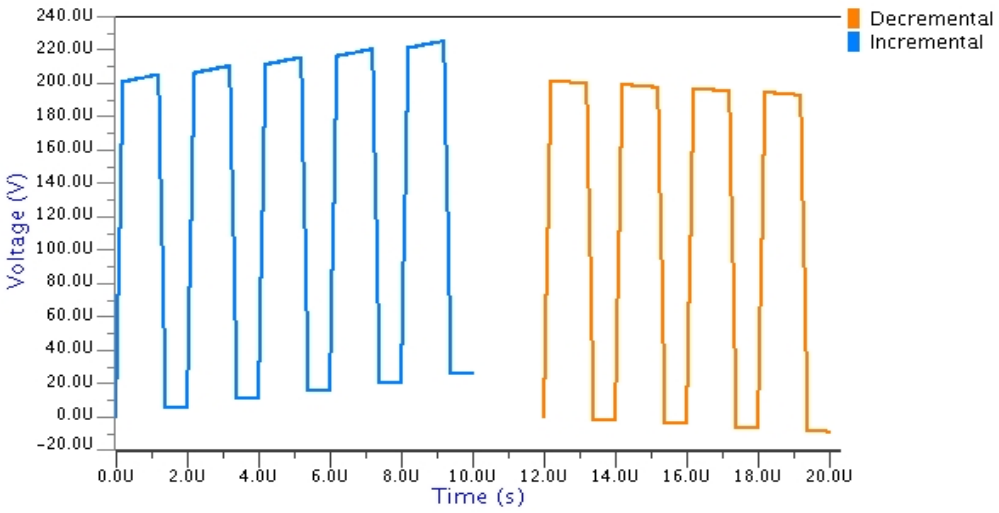
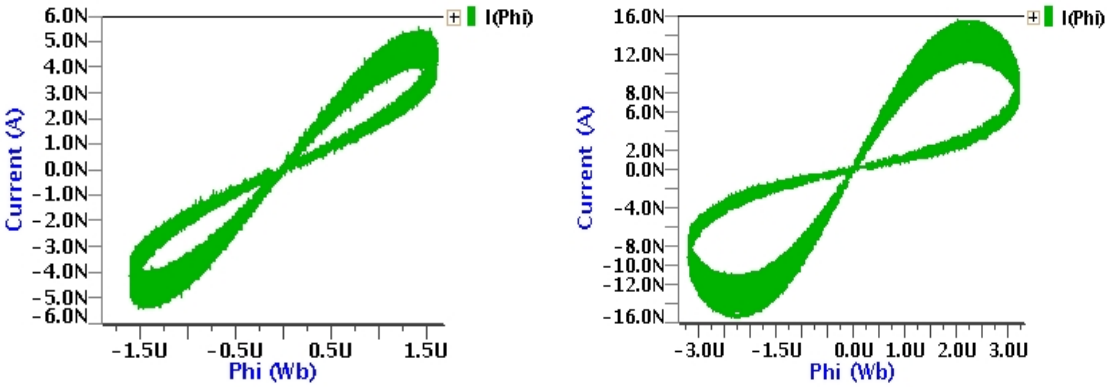


Fig. 5.59. Non-volatility test of proposed F-MIE based on VDTA and CDBA.



(a) (b)

Fig. 5.60 Monte Carlo analysis of proposed MIE based on VDTA and CDBA (a) grounded (b) floating

Figs. 5.58 and 5.59 display the responses (voltages across capacitor C_1) of the proposed grounded and floating decremental/incremental MIEs to the pulse input. Both responses confirm the presence of memory in the MIEs, as they maintain their values during the 'OFF' periods of the input pulses, which were acquired during the 'ON' periods. Subsequently, the values start decreasing/increasing in the subsequent pulses for the decremental/incremental G-MIEs and F-MIEs

5.9.4 Monte Carlo analysis

To assess the robustness of the proposed MIEs, a Monte Carlo analysis has been conducted by applying a sinusoidal signal with an amplitude of 120 mV and a frequency of 500 kHz for 500 simulation runs. Gaussian random variations are applied to modify the threshold voltage, aspect ratios, and capacitances. The PHLs obtained by the Monte Carlo analysis are depicted in Figs. 5.60 (a) and (b). It is evident from these Figs. that all hysteresis loops remain consistent and unchanged.

5.10 Comparison of proposed meminductor emulators with reported meminductor emulators

The proposed MIEs are contrasted with existing designs of MIEs listed in references, as shown in Table 5.10. Unlike existing emulators relying on analog multipliers [151, 152, 155-162 and 172], the proposed MIEs overcome the complexity of the design.

Table 5.10 Comparison of proposed MIEs with existing MIEs.

Ref.	No. of active elements	No. of passive elements	Power supply	Output range	Memristor-less	Meminductance Range	Floating (F) & grounded (G)	Electronic Tunability
[151]	4 CCII+s, two op-amps & buffer	11R, 2C	±15V	36.9Hz	Yes	28.3mH-36.9mH	G	No
[152]	Three op-amps, 6 NMOS transistors, 6 PMOS transistors, & multiplier,	2R, 1C, 1L	±5V	300Hz	Yes	----		No
[155]	8 op-amps & multiplier	9R, 2C	----	4Hz	Yes	----	G	No
[156]	2 VDTAs, & multiplier	2C	±0.9V	1MHz	Yes	----	F	Yes
[157]	7 op-amps, & multiplier	13R, 1C	----	1Hz	Yes		G	No
[158]	4 CCII+s, & multiplier	4R, 1C	±3V	14kHz	Yes	2kH	F	No
[159]	7 op-amps, & multiplier	5R, 1C	----	200Hz	Yes	----	G	No
[160]	1OTA, 1 CFOA, 2 CCII+s, & multiplier	2R, 2C	----	5 kHz	Yes	----	Both	No
[161]	1DO-OTA, 1 MO-OTA & multiplier	2R, 2C	±1.25V	1kHz	Yes	----	G	Yes
[162]	7 op-amps, 2 multipliers & 1switch	14R, 2C	±12V	1kHz	Yes	----	G	No
[169]	1 DO-CCII+, 1 CCII, & multiplier	10R, 2C, 1L	±12V	700Hz	Yes	----	G	No
[172]	2 integrators,1 multiplier, 1 adder & FPAA	----	±0.9V	2 kHz	Yes	3.5mH-4mH	F	Yes
[173]	VDCC	1R, 1C	±0.9V	7kHz	No	----	F	Yes
[176]	CBTA	1C	---	15Hz	No	0.09375mH -0.5mH	Both	Yes
[177]	1OTA & 1VDTA	1C	±1.25V	3MHz	No	0-100µH	G	Yes
[179]	3 OTAs	2C	±1.2V	1kHz	No	----	G	No
[182]	1 OTA & 1 DVCC	1R, 2C	±0.9V	10MHz	Yes	0-40µH	G	No
[185]	1 Op-amp	3R, 2C	±15V	107kHz	No	----	G	No
[186]	MVDCC & OTA	2R, 1C	±0.9V	3 kHz	No	----	F	Yes
[187]	VDTA & DO-CCII	2R, 1C	±10V	3 kHz	Yes	----	F	Yes
[194]	MVDTA	1R, 2C	±0.9V	5 kHz	Yes	----	Both	No
Proposed MIE-I	2OTAs & 1 CDBA	2C	±0.9V	2MHz	Yes	0-565.46mH	Both	Yes
Proposed MIE-II	VDGA & CDBA	2C	±0.9V	3MHz	Yes	0-342.63mH	Both	Yes
Proposed MIE-III	VDTA & CDBA	2C	±0.9V	2MHz	Yes	0-834mH	Both	Yes

It achieves a broader frequency spectrum reaching up to 2 to 3 MHz as opposed to the existing emulators in Hz and kHz ranges. Unlike multiple components in existing designs of MIEs the proposed emulators are realized by utilizing only one passive component. The range of meminductance of proposed MIEs is higher than the existing MIEs as shown in Table 5.10. Moreover, while some of the existing designs are exclusively grounded the proposed MIEs accommodates grounded and floating configurations. The proposed MIEs are resistor-less while in many existing designs of MIEs resistors have been employed. Additionally, the proposed design of MIEs distinguish itself with electronic tunability, a feature primarily absents in many proposed MIEs except for a few cases [156, 161, 172, 173, 176, 186, and 187]. The proposed MIE is also resistor-less and memristor-less; while many designs use a memristor.

5.11 Applications of proposed meminductor emulators

In this section, the proposed MIEs utilizing OTA-CDBA, VDGA-CDBA, and VDTA-CDBA have been used in the adaptive learning and chaotic circuits to demonstrate their applications. The performances of both grounded and floating configurations have been verified through these applications.

5.11.1 Realization of adaptive learning circuit using proposed meminductor emulators

The application area of mem-element is very large such as computational neural network (CNN) due to their unique ability to combine memory and computation in a single device [201]. The Fig. 5.61 shows the adaptive learning circuit [170-172] that is realized to evaluate the performance of the proposed MIE. The proposed MIE circuits have been embedded in the design of adaptive learning circuit. The proposed MIE can retain past events and thereby influencing its performance based on the historical context of the circuit. A piecewise linear (PWL) signal as shown in Fig. 5.62, is applied to the adaptive learning circuit to validate its memory characteristic. Initially, the circuit familiarizes itself with the PWL pattern, effectively memorizing past inputs and swiftly predicting subsequent patterns. This adaptive behavior is evident from the output (V_{out}) depicted in Figs. 5.63 to 5.65, where it initially takes slightly longer to track the first pulse. However, after learning the input pulse behavior, it quickly adapts to follow the second and third pulses. To confirm its memory retention

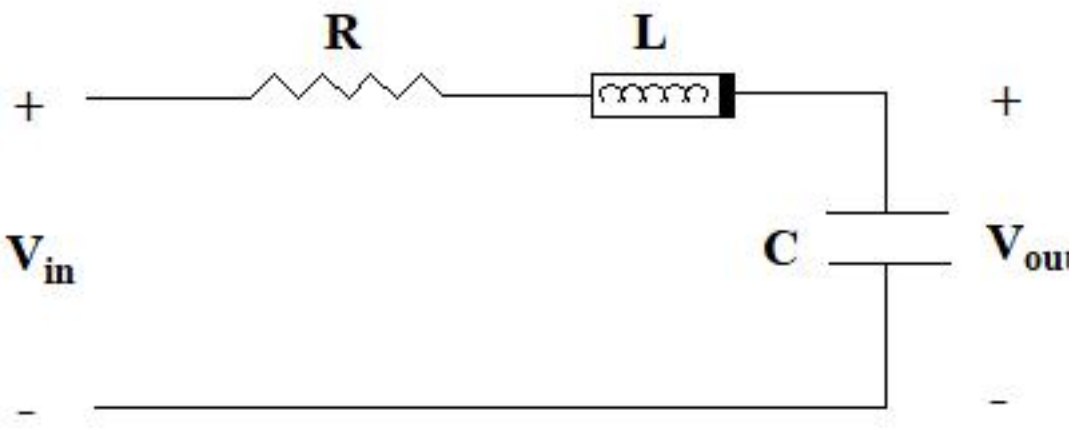


Fig. 5.61 Adaptive learning circuit using proposed MIEs.

capability, a fourth pulse is applied after an interval, affirming that the circuit, realizing using MIEs using OTA-CDBA, VDGA-CDBA, and VDTA-CDBA, can successfully track this pulse even after an irregular interval. The behavior of this circuit draws an analogy to the learning process of an amoeba, which assimilates past events before initiating action. To elucidate this analogy further, consider the input voltage (V_{in}) as analogous to temperature, dictating the motion of the amoeba. The locomotive speed of the amoeba in reaction to temperature variations is represented by the output voltage (V_{out}) across the capacitor. As a result, environmental changes (V_{in}) correlate with variations in locomotive speed (V_{out}). It is evident that a decrease in temperature, analogous to V_{in}, leads to a reduction in locomotive speed, reflecting the adaptive response of an amoeba to changes in its surroundings. This process validates the steps of the adaptive learning process observed in amoebas, where future temperature changes are anticipated based on past occurrences. Fig. 5.62 shows the input response of the adaptive learning circuit. Figs. 5.63 to 5.65, depict the outputs of adaptive learning circuits of proposed MIEs based on OTA-CDBA, VDGA-CDBA, and VDTA-CDBA. The response of the MIE based on OTA and CDBA is illustrated in Fig. 5.63. The component values for adaptive learning circuit based on OTA and CDBA are selected as R = 2 kΩ, C = 50 nF whereas internal capacitors of meminductor is selected as C_1 = 20 pF, and C_2 = 40 pF. Similarly, the component values for adaptive learning circuits based on MIEs using VDGA and CDBA are R= 1 kΩ, C=10 nF whereas the values of internal capacitors are given as C_1 = 20 pF, and C_2 = 40 pF. The component values for adaptive learning circuit based on VDTA and CDBA are R= 0.5 kΩ, C = 50nF whereas the values of internal capacitors are given as C_1 = 20 pF, and C_2 = 40 pF, respectively. The responses of

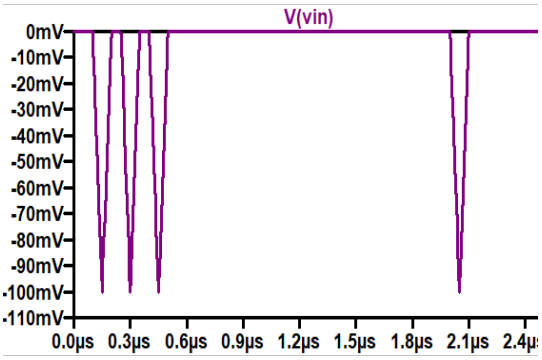


Fig. 5.62 Input waveform of adaptive learning circuit.

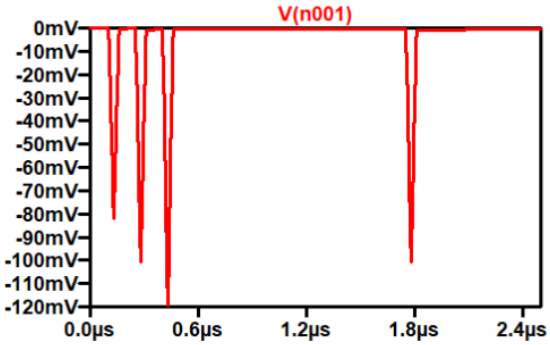


Fig. 5.63 Response of adaptive learning circuit using OTA and CDBA based MIE.

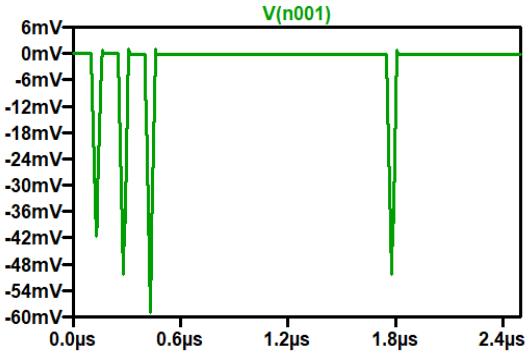


Fig. 5.64 Response of adaptive learning circuit using VDGA and CDBA based MIE.

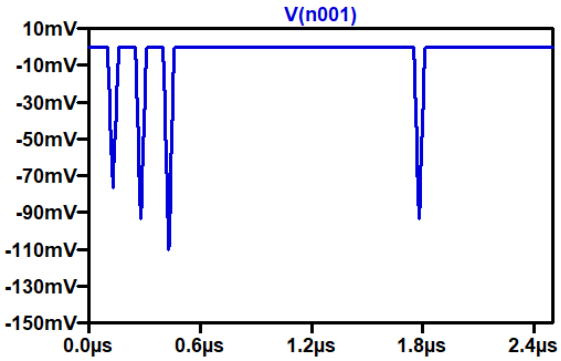


Fig. 5.65 Response of adaptive learning circuit using VDTA and CDBA based MIE.

adaptive learning circuits using proposed MIE based on VDGA-CDBA and VDTA-CDBA have been presented in Figs. 5.64 and 5.65.

5.11.2 Realization of chaotic circuits using proposed meminductor emulators

Another application incorporating the proposed MIEs based on OTA-CDBA, and VDGA-CDBA is shown in Fig. 5.66. The values of passive components are chosen as $R_a = 2k\Omega$, and $R_b = 9k\Omega$, L = 120mH, $R_1 = 50\Omega$, $C_1 = 28nF$, and $C_2 = 70nF$ for the adaptive learning circuit realized with MIE using OTA and CDBA whereas the values of passive components are chosen as $R_a = 2k\Omega$, and Rb = 9kΩ, L = 120mH, $R_1 = 150\Omega$, $C_1 = 18.2nF$, and $C_2 = 65nF$ for the adaptive learning circuit realized with MIE using VDGA and CDBA. The AD711 operational amplifier has been used. The 2-D projection plots illustrating the relationship between voltages V_1 and V_2, and current I_{L1} and voltage V_1 are presented in Fig. 5.67 (a) and

(b), respectively for the adaptive learning circuit embedded with the MIE using OTA and CDBA. These graphical representations offer insights into the dynamic behavior of the chaotic circuit, revealing its intricate patterns and behaviours.

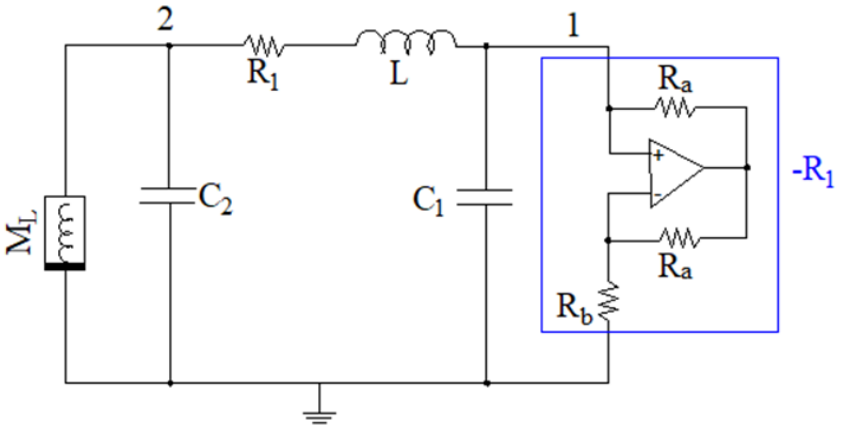
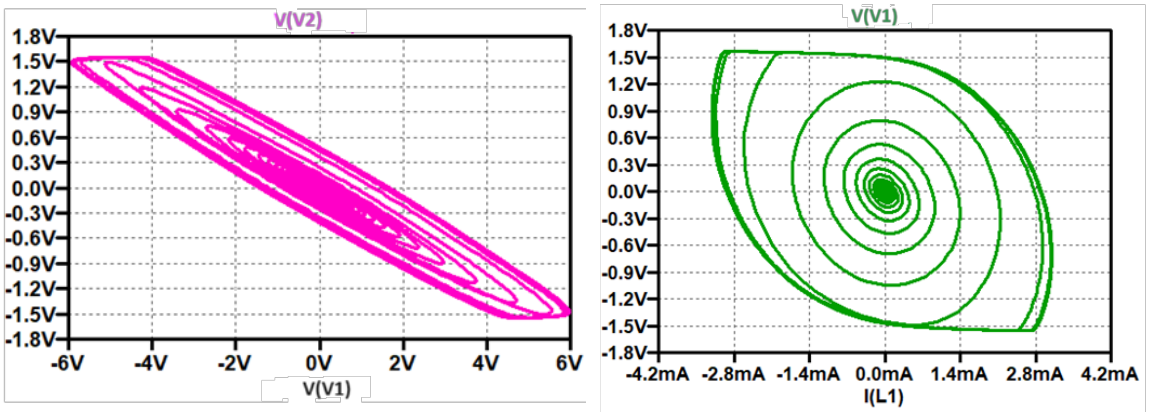
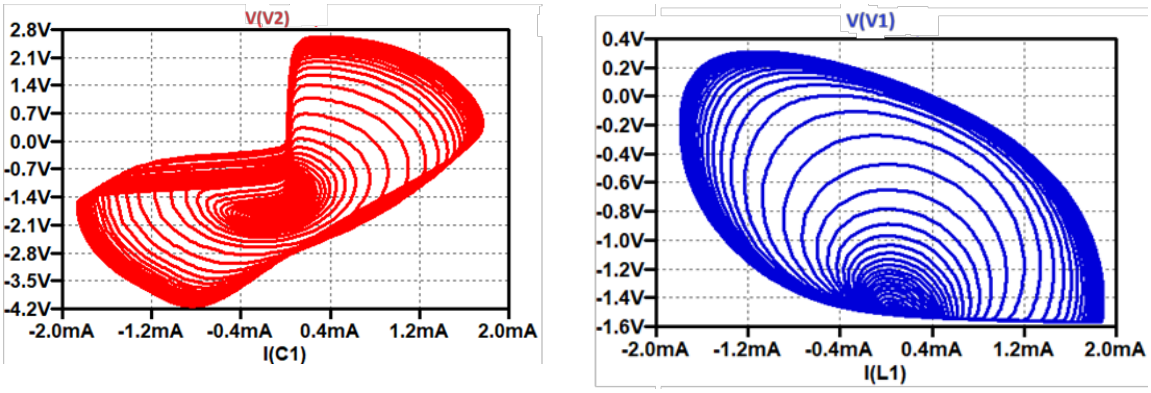


Fig. 5.66 Chaotic circuit using OTA and CDBA and VDGA and CDBA based MIEs.



(a) (b)

Fig. 5.67 2-D projection plots of chaotic oscillators using OTA and CDBA based MIE.



(a) (b)

Fig. 5.68 2-D projection plots of chaotic oscillators using VDGA and CDBA based MIE.

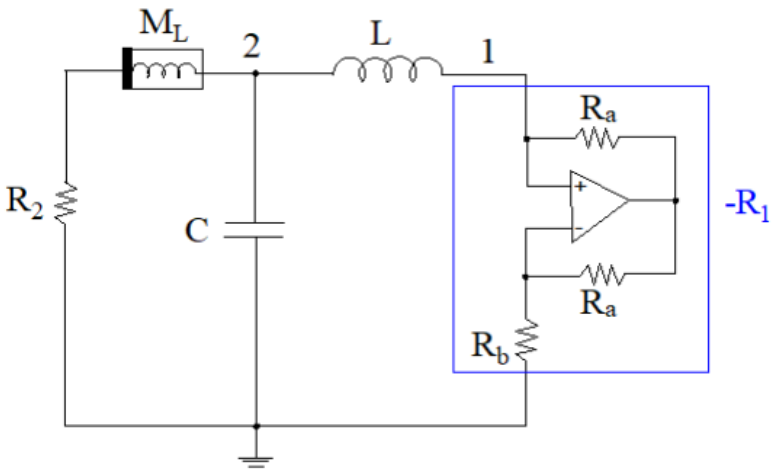
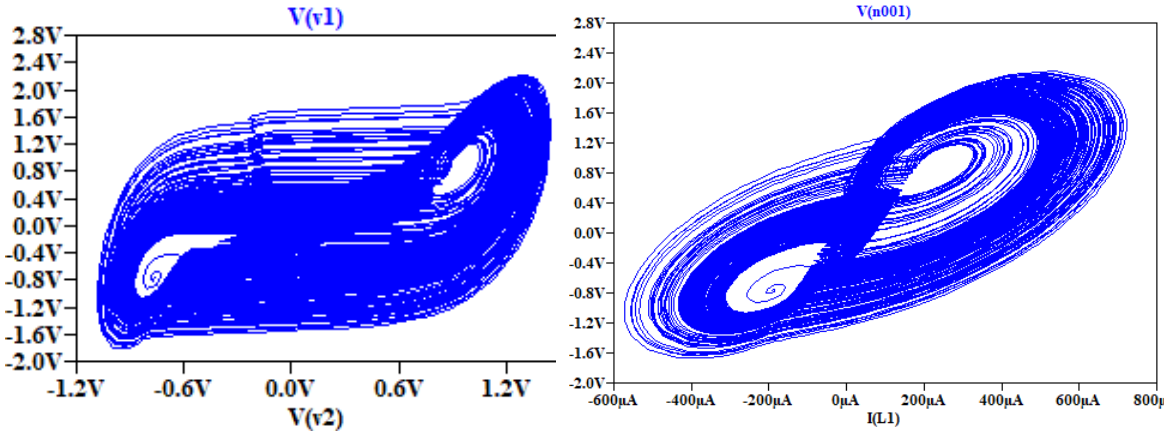


Fig. 5.69 Chaotic circuit using proposed VDTA and CDBA based MIE.



(a) (b)

Fig. 5.70 2-D projections of chaotic oscillator using VDTA and CDBA based MIE.

The 2-D projection plots illustrating the relationship between voltages V_1 and $I(C_1)$, and current (I_{L1}) and voltage (V_1) are presented in Fig. 5.68 (a) and (b) for the adaptive learning circuit embedded with the MIE using VDGA and CDBA.

The chaotic circuit embedding the proposed MIE using VDTA and CDBA is shown in Fig. 5.69. The values of passive components are chosen as $R_a = 2k\Omega$, and Rb = 9kΩ, L = 120mH, $R_1 = 50\Omega$, $C_1 = 28nF$, and $C_2 = 70nF$. The 2-D projection plots illustrating the relationship between voltages V_1 & V_2, and current (I_{L1}) & voltage (V_1) are presented in Fig. 5.70 (a) and (b), respectively.

5.12 Conclusions

In this chapter, the simulation results of proposed emulators have been presented including MREs using OTA and CDBA, VDGA, and FB-VDBA. In addition, the simulation results of MIEs have also been included using OTA and CDBA, VDGA and CDBA, and VDTA and CDBA, respectively. The MRE employing OTA and CDBA achieves a high-frequency range in MHz but requires two analog building blocks and a grounded capacitor whereas VDGA and FB-VDBA based MREs use only a single analog building block with a grounded capacitor and the frequency range is also found to be in MHz range. The range of memristance of proposed MRE using OTA and CDBA is found to be higher than the range of memristance of proposed MRE using VDGA. In contrast, memristance of OTA and CDBA based memristor is less than the MRE using FB-VDBA. All emulators facilitate both the decremental and incremental configurations. In the proposed MIEs, the PHLs are found to be satisfactory in the range of kHz to MHz. The range of meminductance is higher in VDTA and CDBA based MIE than the OTA and CDBA, and VDGA and CDBA based MIEs. The transient analysis, PHLs, temperature analysis, Monte Carlo analysis, etc. are found to be satisfactory for the proposed mem-element emulator.

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CHAPTER 6

CONCLUSION AND FUTURE SCOPE

6.1 Conclusion

The mem-elements are indispensable in analog circuits due to their unique ability to retain and process analog signals, facilitating the development of adaptive and efficient circuitry. Their unique properties enable the development of innovative solutions for various applications in electronic systems. Therefore, the thesis mainly focuses on designing of new memristor emulators (MREs) and meminductor emulators (MIEs). In the thesis, six circuits of mem-element emulators have been reported consisting of three MREs and three MIEs emulators. These MREs have been proposed using operational transconductance amplifier (OTA) and current differencing transconductance amplifier (CDBA), a voltage differencing gain amplifier (VDGA), and a fully-balanced voltage differencing buffered amplifier (FB-VDBA). A grounded capacitor has also been used as a passive component in each MRE circuit. On the other hand, the three MIE circuits have been suggested using OTA & CDBA, VDGA & CDBA, and VDTA & CDBA. Two grounded capacitors have been used in each MIE circuits The performances of MREs and MIEs are found to be satisfactory up to a few MHz frequencies. Their values of memristances and meminductances are found to be significant and therefore these emulators can be used in varieties of applications. The proposed MREs have been embedded in the design of analog filters to demonstrate the application of proposed MREs and validate their workability, while the MIEs have been employed to demonstrate their versatility in chaotic oscillators, and adaptive learning circuits. It means that the practical uses of MREs and MIE demonstrate their ability to push technological boundaries. By improving efficiency, performance, and adaptability in electronics, these components are shown to be essential for advancing current and future technologies.

6.2 Future Scope

In the thesis, analog building blocks and a few passive components are utilized in the design of mem-elements emulator. In the future scope of work, MOSFET-only mem-element emulators can be realized without using passive components. The required passive

components can be realized using MOSFETs. In the thesis, three applications have been explored using mem-elements namely analog filters, adaptive learning circuits, and chaotic oscillators. Mem-elements can be used in varieties of applications ranging from memory to neuromorphic computing. The usage of mem-elements in neuromorphic computing and bionic circuits can be explored.

List of Publications

SCI Journal Papers

1. Nisha Yadav, Shireesh Kumar Rai, and Rishikesh Pandey, "New grounded and floating memristor emulators using OTA and CDBA", *International Journal of Circuit Theory and Application*, 48 (7), 2020, 1154-1179. (SCI Journal, **Impact Factor: 1.8, Publisher: Wiley**)

2. Nisha Yadav, Shireesh Kumar Rai, and Rishikesh Pandey, "Novel memristor emulators using fully balanced VDBA and grounded capacitor", *Iranian Journal of Science and Technology, Transactions of Electrical Engineering*, 45, 2021, 229-245. (SCI Journal**, Impact Factor: 1.5, Publisher: Springer**)

3. Nisha Yadav, Shireesh Kumar Rai, and Rishikesh Pandey, "High frequency electronically tunable floating memristor emulators employing VDGA and grounded capacitor", *Wireless Personal Communications*, 121 (4), 2021, 3185-3211. (SCI Journal**, Impact Factor: 1.9, Publisher: Springer**)

4. Nisha Yadav, Shireesh Kumar Rai, and Rishikesh Pandey, "New grounded and floating memristor-less meminductor emulators using VDTA and CDBA", *Journal of Circuits, Systems and Computers*, 30 (15), 2021, 2150283-1-31. (SCI Journal**, Impact Factor: 0.9, Publisher: World Scientific**)

5. Nisha Yadav, Shireesh Kumar Rai, and Rishikesh Pandey, "New high frequency memristorless and resistorless meminductor emulators using OTA and CDBA", *Sādhanā,* 47 (1), 2022, 1-18. (SCI Journal**, Impact Factor: 1.4, Publisher: Springer**)

6. Nisha Yadav, Shireesh Kumar Rai, and Rishikesh Pandey, "Simple grounded and floating meminductor emulators based on VDGA and CDBA with application in adaptive learning circuit", Journal *of Computational Electronics*, 22 (1), 2023, 531-548. (SCI Journal**, Impact Factor: 2.2, Publisher: Springer**)

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Appendix A: Non-ideal behavior of analog building blocks

A.1 Introduction

This appendix delves into the specific non-ideal behaviors exhibited by the analog building blocks analyzed in this thesis. These components, including resistors, capacitors, and inductors, often deviate from their idealized models due to various practical factors such as parasitic effects, temperature variations, and finite gain.

A.2 Non-ideal behavior of operational transconductance amplifier (OTA)

The non-ideal OTA is shown in Fig. A.1, in which parasitic resistance R_{in+} is connected in parallel with parasitic capacitance C_{in+} at input terminal "+" of OTA. In contrast, parasitic resistance R_{in-} is connected in parallel with parasitic capacitance C_{in-} at another input terminal "-" of OTA. The parasitic resistance R_{0+} and parasitic capacitance C_{0+} appear in parallel at the output "O+" terminal of OTA. Similarly, parasitic resistance R_{0-} and parasitic capacitance C_{0-} are connected in parallel at another output terminal, "O-" of OTA. The transconductance gain (G_m) of OTA also depends on the frequency of operation and can be represented by G_m (s). Thus, the non-ideal equations of OTA are given by

$$I_{0+} = \pm G_m(s) V_{in} \tag{A.1}$$

The transconductance gain G_m(s) can be expressed as

$$G_m(s) = \frac{G_{m0}}{1 + \frac{s}{\omega_{gm}}} \tag{A.2}$$

where G_{m0} is the transconductance value at low frequency, and ω is the pole frequency

The value of transconductance gain G_m (s) is controlled by the bias voltage (V_{B1}) and is given by

$$G_m(s) = \frac{\mu_n C_{ox} \frac{W}{L}}{\sqrt{2}} (V_{B1} - V_{SS} - 2V_{th}) \tag{A.3}$$

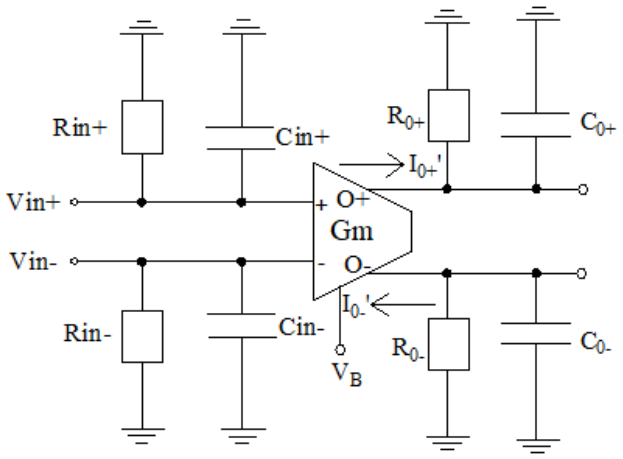

Fig. A.1 Non-ideal model of OTA.

It is seen that the transconductance gain G_m (s) depends on both the frequency of operation and the process parameters which are likely to be changed due to process variation. Therefore, in non-ideal conditions, the transconductance gain G_m (s) cannot be assumed to maintain a constant value for all frequencies of operation

A.3 Non-ideal behavior of current differencing buffered amplifier (CDBA)

The non-ideal CDBA is shown in Fig. A.2, in which R_P and R_N are parasitic resistances of P and N terminals, respectively. Parasitic resistance Rz and parasitic capacitance C_Z appear in parallel at Z terminal whereas parasitic inductance L_W and parasitic resistance R_W appear in series at W terminal. The current transfer ratios from P to Z and from N to Z terminals are given as α_P and α_N, respectively. The voltage transfer ratio from Z terminal to W terminal is defined by β which depends on the frequency of operation. Thus, the voltage gain β is given by β (s). After including these non-ideal conditions, the terminal equations of non-ideal CDBA are given in Equations (A.4), (A.5), and (A.6).

$$V_P' = I_P'^{R_P}, V_N' = I_N'^{R_N} \tag{A.4}$$

$$I_Z' = \alpha_P I_P' - \alpha_N I_N' \tag{A.5}$$

$$V_W' = \beta(s) V_Z' + I_W R_W \tag{A.6}$$

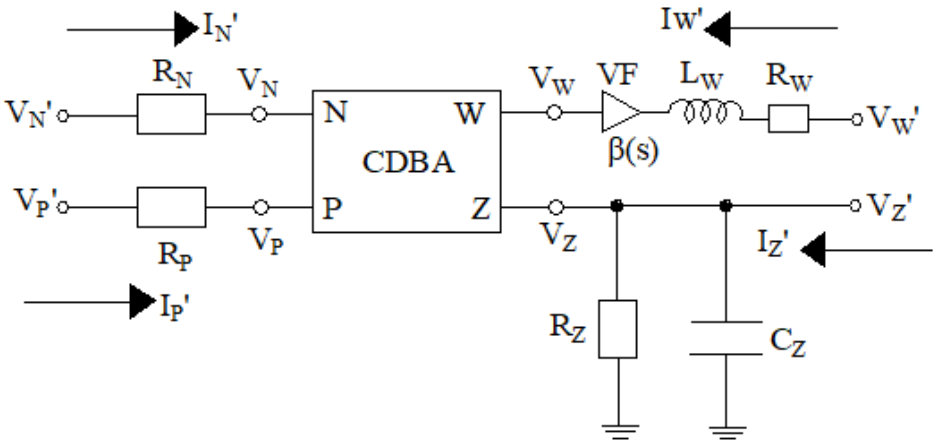

Fig. A.2 Non-ideal model of CDBA.

For ideal CDBA, parasitic resistances (R_P, R_N, R_W) are assumed to be zero, while current and voltage transfer ratios (α_P, α_N, β) are assumed to be one. Thus, the resulting equations lead to ideal equations of CDBA as given in Equation (3.4).

A.4 Non-ideal behavior of VDGA

A non-ideal model of VDGA [206], including parasitic resistances and capacitances of different terminals, is shown in Fig. A.3. The parasitic resistances are represented by Rp, Rn, Rz-, Rz1+, Rz2+ and Rw at terminals p, n, z-, z1+, z2+ and w respectively whereas parasitic capacitances are shown by Cp, Cn, Cz-, Cz1+ and Cz2+ at terminals p, n, z-, z1+ and z2+, respectively. The parasitic resistances Rp, Rn, Rz1+, Rz2+ and Rz- appear in parallel with parasitic capacitances Cp, Cn, Cz1+, Cz2+ and Cz- at terminals p, n, z1+, z2+ and z- respectively. In ideal case, transconductance gain (gm) of VDGA is assumed to be constant for all frequencies of operation whereas in the non-ideal case, transconductance gain (gm) is the function of frequency and is represented by gm (s).

$$I_p = \frac{V_p}{Z_p}, \qquad I_n = \frac{V_n}{Z_n} \tag{A.7}$$

$$I_{z+} = g_m(s).(V_p - V_n) + \frac{V_{z+}}{Z_{z+}}, \; I_{z-} = -g_m(s).(V_p - V_n) + \frac{V_{z-}}{Z_{z-}} \tag{A.8}$$

$$V_w = [\beta(s).V_z + I_w R_w] \tag{A.9}$$

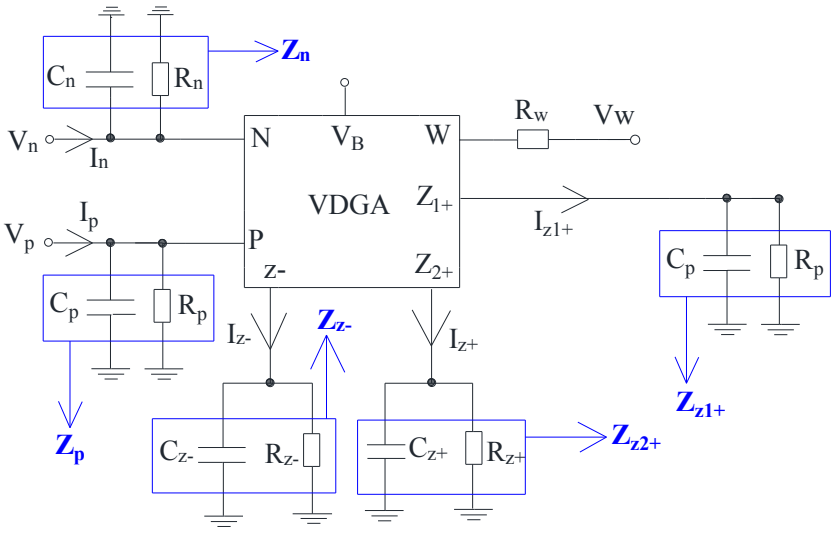

Fig. A.3 Non-ideal model of VDGA.

where Z_p, Z_n, Z_{z-}, Z_{z1+}, Z_{z2+} and Z_w are parasitic impedances of p, n, z-, z1+, z2+ and w terminals of VDGA.

The transconductance gm(s) can be given as

$$g_m(s) = \frac{g_{m0}}{1 + \frac{s}{\omega_{gm}}} \tag{A.10}$$

where gm0 is the transconductance gain at lower frequencies of operation and ω is the pole frequency.

A.5 Non-ideal behaviour of Fully-balanced voltage differencing buffered amplifier (FB-VDBA)

Non-ideal model of FB-VDBA [207] including parasitic resistances and capacitances of different terminals is shown in Fig. A.4. The parasitic resistances are represented by Rp, Rn, Rz-, Rz+, Rw- and Rw+ at terminals p, n, z-, z+, w- and w+ respectively whereas parasitic capacitances are shown by Cp, Cn, Cz- and Cz+ at terminals p, n, z- and z+, respectively. Parasitic inductances are presented by Lw+ and Lw- at terminals w+ and w-, respectively. The parasitic resistances Rp, Rn, Rz+ and Rz- appear in parallel with parasitic capacitances Cp, Cn, Cz+ and Cz- at terminals p, n, z+ and z- respectively. The parasitic resistances Rw+ and Rw- appear in series with parasitic inductances Lw+ and Lw- at w+ and w- terminals of FB-VDBA, respectively.

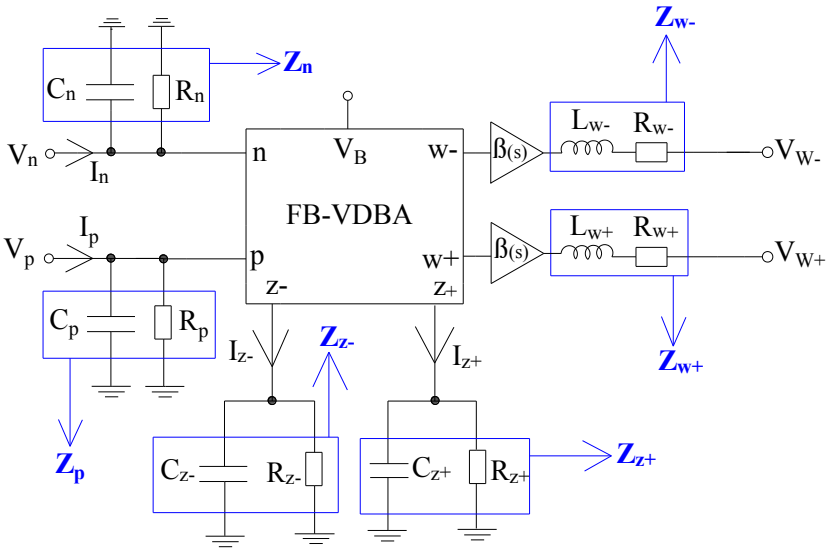

Fig. A.4 Non-ideal model of FB-VDBA.

In the ideal case, transconductance gain (g_m) and gain (β) of FB-VDBA are assumed to be constant for all frequencies of operation whereas in the non-ideal case, transconductance gain (gm) and gain (β) both are the function of frequency and are represented by g_m (s) and β(s). Therefore, the terminal characteristics of non-ideal FB-VDBA is given as

$$I_p = \frac{V_p}{Z_p}, \qquad I_n = \frac{V_n}{Z_n} \tag{A.11}$$

$$I_{z+} = g_m(s).(V_p - V_n) + \frac{V_{z+}}{Z_{z+}}, \qquad I_{z-} = -g_m(s).(V_p - V_n) + \frac{V_{z-}}{Z_{z-}} \tag{A.12}$$

$$V_{w+} = -[\beta(s).V_{z-} + I_{w+}Z_{w+}], \qquad V_{w-} = -[\beta(s).V_{z+} - I_{W-}Z_{w-}] \tag{A.13}$$

where Zp, Zn, Zz-, Zz+, Zw- and Zw+ are parasitic impedances of p, n, z+, z-, w+ and w- terminals of FB-VDBA.

The transconductance gm(s) can be given as

$$g_m(s) = \frac{g_{m0}}{1 + \frac{s}{\omega_{gm}}} \tag{A.14}$$

where gm0 is the transconductance gain at lower frequencies of operation and ω is the pole frequency.

The gain of buffer amplifier of FB-VDBA can be given as

$$\beta(s) = \frac{\beta(0)}{1 + \frac{s}{\omega_\beta}} \tag{A.15}$$

where, β (0) is the gain at lower frequencies and ω_β is the corresponding pole frequency.

A.6 Description of non-ideal voltage differencing transconductance amplifier (VDTA)

The non-ideal model of VDTA [204] including parasitic resistances and capacitances of different terminals is shown in Fig. A.5. The parasitic resistances are represented by Rp, Rn, Rx+, Rx- and Rz for terminals p, n, x+, x- and z respectively whereas parasitic capacitances are shown by Cp, Cn, Cx+, Cx- and Cz for terminals p, n, x-, x+ and z, respectively. The parasitic resistances Rp, Rn, Rx+, Rx- and Rz appear in parallel with parasitic capacitances Cp, Cn, Cx+, Cx- and Cz at terminals p, n, x+, x- and z respectively. In ideal case, transconductance gain (gm) of VDTA are assumed to be constant for all frequencies of operation whereas in the non-ideal case, transconductance (gm) is the

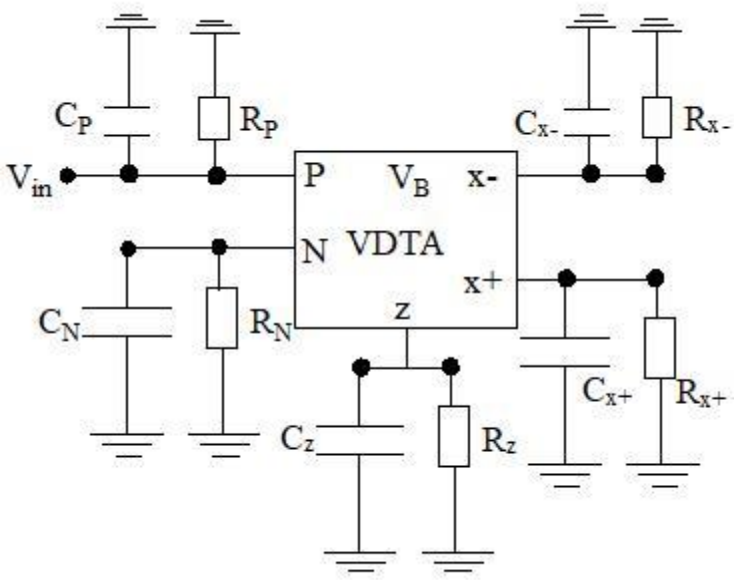

Fig. A.5 Non-ideal model of VDTA.

function of frequency and is represented by gm (s). The non-ideal terminal equations have been defined in matrix form as equation (A.16)

$$\begin{bmatrix} I_Z \\ I_{X+} \\ I_{X-} \end{bmatrix} = \begin{bmatrix} \beta_F g_{mF} & -\beta_F g_{mF} & 0 \\ 0 & 0 & \beta_S g_{mS} \\ 0 & 0 & -\beta_S g_{mS} \end{bmatrix} \begin{bmatrix} V_P \\ V_N \\ V_Z \end{bmatrix} \quad \text{(A.16)}$$

In the context of voltage differential transconductance amplifiers (VDTAs), the terms β_F and β_S refer to the respective tracking errors of voltages associated with the first and second stages. In the proposed circuits, it is crucial to account for the influence of parasitic resistances and capacitances that manifest in parallel at the high-impedance ports of the VDTA. These parasitic elements are illustrated in Fig. A.5, highlighting their significance in circuit design and performance.

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Appendix B: Non-ideal behavior of proposed mem-element emulators circuits

B.1 Introduction

In this appendix, the circuit designs of the proposed non-ideal mem-element emulators are presented, complementing the ideal behaviors discussed in Chapters 3 and 4. Specifically, this section includes the designs and mathematical analyses of three memristor emulators based on OTA-CDBA, VDGA, FB-VDBA, and three meminductor emulators circuits utilizing OTA-CDBA, VDGA-CDBA, and VDBA-CDBA configurations. These designs are analyzed to highlight the non-ideal characteristics that may arise in practical implementations.

B.2 Non-ideal analysis of proposed memristor emulator using OTA and CDBA

After considering the non-ideal effects of CDBA and OTA, the proposed non-ideal equivalent model of grounded decremental memristor emulator is shown in Fig. B.1.

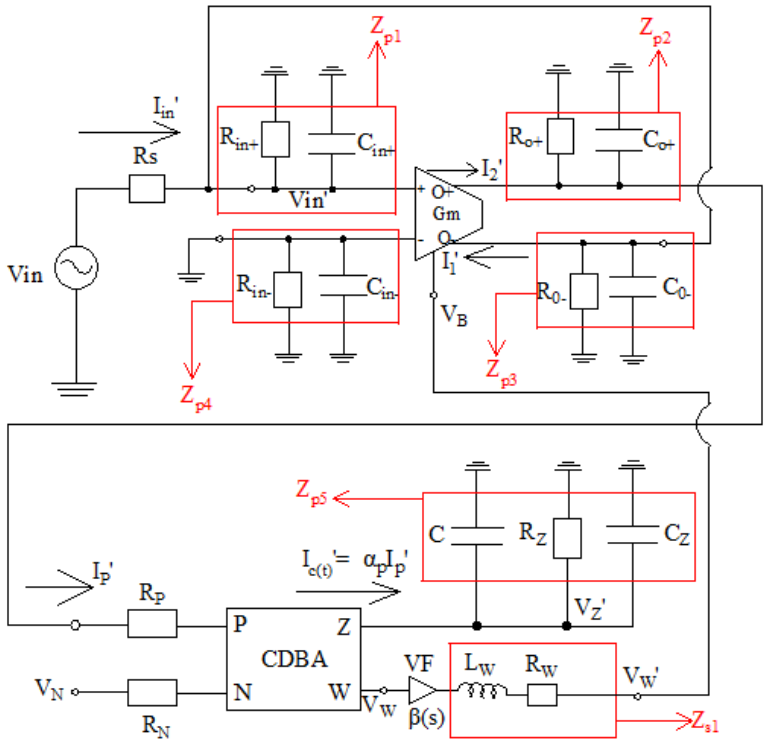

Fig B.1 Non-ideal equivalent model of proposed decremental G-MRE based on OTA and CDBA.

Parallel combinations of parasitic resistances and parasitic capacitances $\left(R_{\text{in}+}||\frac{1}{\text{sC}_{\text{in}+}},\right.$ $\text{R}_{\text{in}-}||\frac{1}{\text{sC}_{\text{in}-}}$,$\text{R}_{o+}||\frac{1}{\text{sC}_{o+}}$,$\text{R}_{o-}||\frac{1}{\text{sC}_{o-}}$, $\left.R_z||\frac{1}{s(C+C_z)}\right)$ at different terminals of OTA and CDBA are represented by impedances Z_{p1}, Z_{p2}, Z_{p3}, Z_{p4} and Z_{p5}, respectively. The series combination of inductor (L_w) and resistance (R_w) is represented by Z_{s1}.

The output current I_1'(t) at output terminal "o-"of OTA is given as

$$I_1'(t) = G_m(s)V_{in}'(t) = G_m(s)V_{in}(t) \times \frac{1}{1 + G_m(s)R_s + \frac{R_s}{Z_{p1}||Z_{p3}}} \tag{B.1}$$

where $G_m(s) = \frac{g_{\text{m0}}}{1+\frac{s}{\omega_{\text{gm}}}}$,$\text{Z}_{\text{p1}} = \frac{1}{\text{sC}_{\text{in}+}+\frac{1}{R_{\text{in}+}}}$, $\text{Z}_{\text{p3}} = \frac{1}{sC_{0-}+\frac{1}{R_{o-}}}$, g_{m0} is the value of transconductance at low frequency, ω represents corresponding pole frequency and Rs is the internal resistance of voltage source V_{in}.

The current at Z terminal of CDBA is expressed as

$$I_C'(t) = \alpha_P I_P' = \alpha_P I_1'(t) \times \frac{Z_{p2}}{R_p + Z_{p2}} \tag{B.2}$$

where α_P is the current transfer ratio from P terminal to Z terminal, R_P is the parasitic resistance at input P terminal of CDBA and $Z_{\text{p2}} = \frac{1}{sC_{o+}+\frac{1}{R_{o+}}}$.

Substituting the value of I_1' (t) from Equation (B.1) to Equation (B.2) results in

$$I_C'(t) = \alpha_P I_P' = \alpha_P G_m(s)V_{in}(t) \times \frac{1}{1 + G_m(s)R_s + \frac{R_s}{Z_{p1}||Z_{p3}}} \times \frac{Z_{p2}}{R_p + Z_{p2}} \tag{B.3}$$

The voltage Vz' can be easily obtained from Fig. B.1 as

$$V_z' = I_C'(t) \times Z_{p5} = I_C'(t) \times \frac{1}{s(C + C_Z) + \frac{1}{R_Z}} \tag{B.4}$$

Substituting the value of Ic' (t) from Equation (B.3) in Equation (B.4), the value of Vz' is given as

$$V_z' = \alpha_P G_m(s)V_{in}(t) \times \frac{1}{1+G_m(s)R_s+\frac{R_S}{Z_{p1}||Z_{p3}}} \times \frac{Z_{p2}}{R_p+Z_{p2}} \times \frac{1}{s(C+C_Z)+\frac{1}{R_Z}} \tag{B.5}$$

As the value of 1/Rz << s(C+C_z), the Equation (B.5) can be approximated as

$$V_z' \cong \alpha_P G_m(s) V_{in}(t) \times \frac{1}{1+G_m(s)R_s+\frac{R_s}{Z_{p1}||Z_{p3}}} \times \frac{Z_{p2}}{R_p+Z_{p2}} \times \frac{1}{s(C+C_Z)} \tag{B.6}$$

The Equation (B.6) can be easily rewritten as

$$V_z' \cong \alpha_P \times \frac{1}{(C+C_Z)} \times \frac{1}{1+G_m(s)R_s+\frac{R_s}{Z_{p1}||Z_{p3}}} \times \frac{Z_{p2}}{R_p+Z_{p2}} \int G_m(s) V_{in}(t) dt \tag{B.7}$$

The voltage V_W' at W terminal of CDBA can be expressed as

$$V_w' = \beta(s) V_Z' + I_W R_W \tag{B.8}$$

The voltage transfer ratio of Z terminal and W terminal (gain of buffer amplifier) of CDBA can be defined as

$$\beta(s) = \frac{\beta(0)}{1+\frac{s}{\omega_\beta}} \tag{B.9}$$

where, β (0) is the value of gain of buffer amplifier of CDBA at low frequency and ω_β represents the corresponding pole frequency.

The voltage V_W' at W terminal of CDBA can be written as

$$V_w' \cong \beta(s)\alpha_P G_m(s) V_{in}(t) \times \frac{1}{1+G_m(s)R_s+\frac{R_s}{Z_{p1}||Z_{p3}}} \times \frac{Z_{p2}}{R_p+Z_{p2}} \times \frac{1}{s(C+C_Z)} + I_W R_W \tag{B.10}$$

The biasing voltage V_B is equal to V_W' and can be expressed as

$$V_B \cong \beta(s)\alpha_P G_m(s) V_{in}(t) \times \frac{1}{1+G_m(s)R_s+\frac{R_s}{Z_{p1}||Z_{p3}}} \times \frac{Z_{p2}}{R_p+Z_{p2}} \times \frac{1}{s(C+C_Z)} + I_W R_W \tag{B.11}$$

Similarly, Equation (B.11) can be rewritten as

$$V_B \cong \beta(s)\alpha_P . \frac{1}{(C+C_Z)} . \frac{1}{1+G_m(s)R_s+\frac{R_s}{Z_{p1}||Z_{p3}}} . \frac{Z_{p2}}{R_p+Z_{p2}} \int G_m(s) V_{in}(t) dt + I_W R_W \tag{B.12}$$

In Equation (B.12), $\int V_{in}(t)dt$ is the total flux obtained by the memristor and can be represented by flux ϕ_{in}. Therefore, Equation (B.12) is now modifying as

$$V_B \cong G_m(s).\beta(s)\alpha_P.\frac{1}{(C+C_Z)}.\frac{1}{1+G_m(s)R_s+\frac{R_S}{Z_{p1}||Z_{p3}}}.\frac{Z_{p2}}{R_p+Z_{p2}}.\phi_{in}+I_WR_W \tag{B.13}$$

Now, substituting the value of V_B in Equation (3.2), results in

$$G_m(s)=\frac{\mu_nC_{ox}\frac{W}{L}}{\sqrt{2}}\left[\left(G_m(s).\beta(s)\alpha_P.\frac{1}{(C+C_Z)}.\frac{1}{1+G_m(s)R_s+\frac{R_S}{Z_{p1}||Z_{p3}}}.\frac{Z_{p2}}{R_p+Z_{p2}}.\phi_{in}+I_WR_W\right)-V_{SS}-2V_{th}\right] \tag{B.14}$$

The Equation (B.14) can be rearranged as

$$G_m(s)=-\frac{\frac{\mu_nC_{ox}\frac{W}{L}}{\sqrt{2}}(V_{SS}+2V_{th})}{1-\frac{\mu_nC_{ox}\frac{W}{L}}{\sqrt{2}}\left[\beta(s)\alpha_P.\frac{1}{(C+C_Z)}.\frac{1}{1+G_m(s)R_s+\frac{R_S}{Z_{p1}||Z_{p3}}}.\frac{Z_{p2}}{R_p+Z_{p2}}.\phi_{in}+I_WR_W\right]} \tag{B.15}$$

The value of input current I_{in}' (t) can be obtained from Fig. B.1 as

$$I'_{in}(t)=I'_1(t)\left[1+\frac{R_o}{Z_{p1}||Z_{p3}}\right] \tag{B.16}$$

where R_0 is the output resistance of OTA.
Substituting the value of I_1'(t) from Equation (B.1) to Equation (B.16) results in

$$I'_{in}(t)=G_m(s)V'_{in}(t)\left[1+\frac{R_o}{Z_{p1}||Z_{p3}}\right] \tag{B.17}$$

The value of memristance $M(\phi_m)$ for the non-ideal grounded decremental memristor emulator is obtained from Equation (B.17) as

$$M(\phi_m) = \frac{V'_{in}(t)}{I'_{in}(t)} = \frac{1}{G_m(s)} \times \frac{1}{1 + \frac{R_o}{Z_{p1}||Z_{p3}}} \tag{B.18}$$

Substituting the value of G_m (s) from Equation (B.15) into Equation (B.18), the value of memristance $M(\phi_m)$ is given as

$$M(\phi_m) = \frac{V'_{in}(t)}{I'_{in}(t)} = -\frac{1}{\frac{\mu_n C_{ox}\frac{W}{L}}{\sqrt{2}}(V_{SS}+2V_{th})} \times \frac{1}{1-\frac{\mu_n C_{ox}\frac{W}{L}}{\sqrt{2}}\left[\beta(s)\alpha_P.\frac{1}{(C+C_Z)}.\frac{1}{1+G_m(s)R_S+\frac{R_S}{Z_{p1}||Z_{p3}}}.\frac{Z_{p2}}{R_p+Z_{p2}}.\phi_{in}+I_W R_W\right]} \times \frac{1}{1+\frac{R_o}{Z_{p1}||Z_{p3}}} \tag{B.19}$$

Rearranging the terms of Equation (B.19) results in

$$M(\phi_m) = \frac{V'_{in}(t)}{I'_{in}(t)} = -\frac{1-\frac{\mu_n C_{ox}\frac{W}{L}}{\sqrt{2}}\left[\beta(s)\alpha_P.\frac{1}{(C+C_Z)}.\frac{1}{1+G_m(s)R_S+\frac{R_S}{Z_{p1}||Z_{p3}}}.\frac{Z_{p2}}{R_p+Z_{p2}}.\phi_{in}+I_W R_W\right]}{\frac{\mu_n C_{ox}\frac{W}{L}}{\sqrt{2}}(V_{SS}+2V_{th})} \times \frac{1}{1+\frac{R_o}{Z_{p1}||Z_{p3}}} \tag{B.20}$$

The value of $Z_{p1}||Z_{p3}$ is very high as compare to R_0, which reduces the Equation (B.20) as

$$M(\phi_m) = \frac{V'_{in}(t)}{I'_{in}(t)} = -\frac{1-\frac{\mu_n C_{ox}\frac{W}{L}}{\sqrt{2}}\left[\beta(s)\alpha_P.\frac{1}{(C+C_Z)}.\frac{1}{1+G_m(s)R_S+\frac{R_S}{Z_{p1}||Z_{p3}}}.\frac{Z_{p2}}{R_p+Z_{p2}}.\phi_{in}+I_W R_W\right]}{\frac{\mu_n C_{ox}\frac{W}{L}}{\sqrt{2}}(V_{SS}+2V_{th})} \tag{B.21}$$

Rearranging the terms of Equation (B.21) leads to

$$M(\phi_m) = \frac{V'_{in}(t)}{I'_{in}(t)} = -\frac{1}{\frac{\mu_n C_{ox}\frac{W}{L}}{\sqrt{2}}(V_{SS}+2V_{th})} + \frac{\beta(s)\alpha_P.\frac{1}{(C+C_Z)}.\frac{1}{1+G_m(s)R_S+\frac{R_S}{Z_{p1}||Z_{p3}}}.\frac{Z_{p2}}{R_p+Z_{p2}}.\phi_{in}+I_W R_W}{(V_{SS}+2V_{th})} \tag{B.22}$$

The values of current gain and voltage gain are measured and found to be $\alpha_P = 1.01$ and $\beta = 0.99$ for the frequency range of 0 to 1 MHz. The parasitic capacitance C_z is found to be 1.084 pF. The value of source resistance (Rs) is very low. The values of parasitic resistances R_{o+} and R_{o-} are found to be as 19.12 KΩ. The values of R_P and Rw is measured and found to be approximately 1KΩ and 77 Ω, respectively. After substituting these values in Equation (B.22), the value of memristance $M(\phi_m)$ is found to be very close to the ideal value of memristance $M(\phi_m)$. Therefore, it is concluded that the performance of memristor emulator is found to be satisfactory after taking the non-ideal conditions in to consideration.

B.3 Non-ideal analysis of proposed memristor emulator using VDGA

Non-ideal equivalent model of proposed grounded memristor emulator circuit is shown in Fig. B.2 which includes the effect of parasitic impedances. The parasitic resistance and capacitance (Rp and Cp) appear in parallel at "P" terminal of VDGA and is represented by parasitic impedance Zp. Similarly, parasitic resistance and capacitance (Rn and Cn) are connected in parallel at "N" terminal of VDGA and is represented by parasitic impedance Zn.

Parasitic resistance and capacitance (Rz- and Cz-) appear in parallel at "z-" terminal and is represented by parasitic impedance Zz-. Similarly, parasitic resistance and capacitance (Rz1+ and Cz1+) are connected in parallel at "Z1+" terminal and is represented by parasitic impedance Zz1+. The voltages (Vz1+ and Vz-) at z1+ and z- terminals are copied with the help of internal buffer of VDGA. The parasitic resistance Rw are in series at "W" terminal.

The values of parasitic impedances Zp, Zn, Zz-, Zz1+ and Zw are given by

$$Z_p = \frac{1}{sC_p + \frac{1}{R_p}}, \qquad Z_n = \frac{1}{sC_n + \frac{1}{R_n}} \tag{B.23}$$

$$Z_{z1+} = \frac{1}{sC_{z1+} + \frac{1}{R_{z1+}}}, \qquad Z_{z-} = \frac{1}{sC_{z-} + \frac{1}{R_{z-}}} \tag{B.24}$$

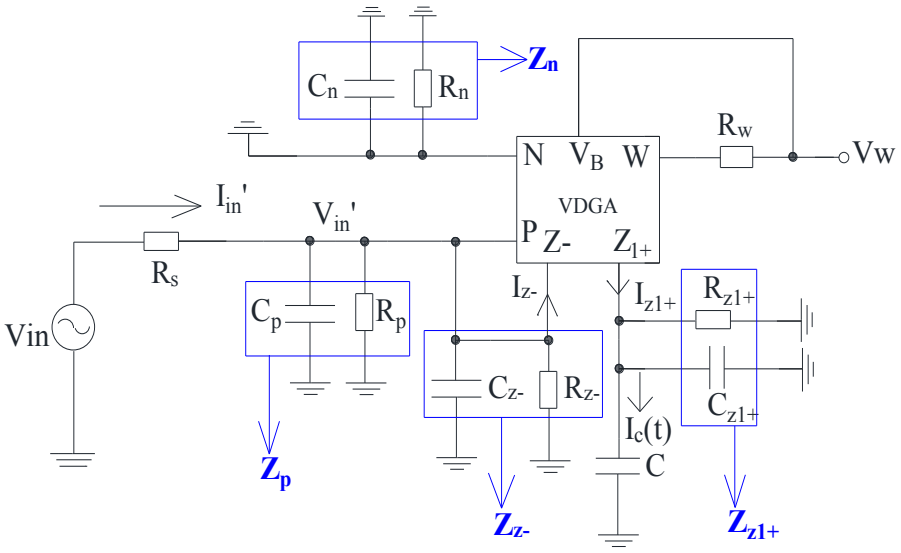

Fig. B.2 Non-ideal equivalent model of proposed decremental G-MRE based on VDGA.

The routine analysis of Fig. B.2 yields the value of current Iz- at intermediate terminal "Z-"of VDGA as

$$I_{z-} = G_m(s)V'_{in} = G_m(s)V_{in} \times \frac{1}{1 + G_m(s)R_s + \frac{R_s}{Z_p||Z_{z-}}} \tag{B.25}$$

where Rs is the source resistance of input voltage Vin.

The current I_{z1+} of FB-VDBA is the same as obtained in Equation (B.25).

$$I_{z1+} = G_m(s)V_{in} \times \frac{1}{1 + G_m(s)R_s + \frac{R_s}{Z_p||Z_{z-}}} \tag{B.26}$$

The voltage V_{z1+} is obtained at Z_{1+} terminal of VDGA as

$$V_{z1+} = I_{z1+} \times \frac{1}{s(C + C_{Z1+}) + \frac{1}{R_{z1+}}} \tag{B.27}$$

The value of Vz1+ is obtained with help of Equations. (B.26) and (B.27) as given in Equation (B.28).

$$V_{z1+} = G_m(s)V_{in} \times \frac{1}{1 + G_m(s)R_s + \frac{R_s}{Z_p||Z_{z-}}} \times \frac{1}{s(C + C_{z1+}) + \frac{1}{R_{z1+}}} \quad \text{(B.28)}$$

Since the value of 1/Rz+ << s(C+Cz+), the Equation (B.28) can be modified as

$$V_{z1+} \cong G_m(s)V_{in} \times \frac{1}{1 + G_m(s)R_s + \frac{R_s}{Z_p||Z_{z-}}} \times \frac{1}{s(C + C_{z1+})} \quad \text{(B.29)}$$

The Equation (B.29) can be rewritten as

$$V_{z1+} \cong \frac{1}{(C + C_{z1+})} \times \frac{1}{1 + G_m(s)R_s + \frac{R_s}{Z_p||Z_{z-}}} \int G_m(s)V_{in}(t)dt \quad \text{(B.30)}$$

Replacing the voltage Vz1+ from Equation (B.30) into Equation (A.9), the voltage V_W can be written as

$$V_w' \cong \left(\beta(s) \frac{1}{(C+C_{Z+})} \times \frac{1}{1+G_m(s)R_s+\frac{R_s}{Z_p||Z_{z-}}} \int G_m(s)V_{in}(t)dt + I_w.R_w \right) \quad \text{(B.31)}$$

The biasing voltage V_B is directly connected to V_W in Fig. B.2 and can be expressed as

$$V_B \cong \left(\beta(s) \frac{1}{(C+C_{Z+})} \times \frac{1}{1+G_m(s)R_s+\frac{R_s}{Z_p||Z_{z-}}} \int G_m(s)V_{in}(t)dt + V_w \right) \quad \text{(B.32)}$$

The term $\int V_{in}(t)dt$ can be represented by flux (ϕ) and thereby Equation (B.32) is now changed to

$$V_B \cong \left(G_m(s)\beta(s) \frac{1}{(C + C_{Z+})} \times \frac{1}{1 + G_m(s)R_s + \frac{R_s}{Z_p||Z_{z-}}} . \phi_{in} + V_w \right) \quad \text{(B.33)}$$

After replacing the voltage V_B from Equation (B.33) into Equation (3.10), we get

$$G_m(s) = \frac{k}{\sqrt{2}}\left[\left(G_m(s).\beta(s).\frac{1}{(C+C_Z)}.\frac{1}{1+G_m(s)R_s+\frac{R_s}{Z_p||Z_{z-}}}.\phi_{in} + V_w\right) - V_{SS} - 2V_{th}\right] \quad \text{(B.34)}$$

The Equation (B.34) can be rearranged as

$$G_m(s) = \frac{\frac{k}{\sqrt{2}}(V_{SS} + 2V_{th})}{1 + \frac{k}{\sqrt{2}}\left[\beta(s).\frac{1}{(C + C_{Z1+})}.\frac{1}{1 + G_m(s)R_s + \frac{R_s}{Z_p||Z_{z-}}}.\phi_{in} + V_w\right]} \quad \text{(B.35)}$$

The value of input current Iin' (t) can be obtained from Fig B.2 as

$$I'_{in}(t) = I_{z-} \times \left[1 + \frac{R_o}{Z_p||Z_{z-}}\right] \quad \text{(B.36)}$$

where R0 is the output resistance of Z- terminal of VDGA.

After replacing the current Iz- from Equation (B.25) to Equation (B.36), we get

$$I'_{in}(t) = G_m(s)V'_{in}(t)\left[1 + \frac{R_o}{Z_p||Z_{z-}}\right] \quad \text{(B.37)}$$

The value of memristance $M(\phi_m)$ for the non-ideal decremental grounded memristor emulator circuit is obtained from Equation (B.37) as

$$M(\phi_m) = \frac{V'_{in}(t)}{I'_{in}(t)} = \frac{1}{G_m(s)} \times \frac{1}{1 + \frac{R_o}{Z_p||Z_{z-}}} \quad \text{(B.38)}$$

When the value of Gm (s) is substituted from Equation (B.35) into Equation (B.38), we get the value of memristance $M(\phi_m)$ as

$$M(\phi_m) = \frac{V'_{in}(t)}{I'_{in}(t)} = -\frac{1}{\frac{k}{\sqrt{2}}(V_{SS}+2V_{th})} - \frac{\beta(s).\frac{1}{(C+C_{Z1+})}.\frac{1}{1+G_m(s)R_S+\frac{R_s}{Z_p||Z_{z-}}}.\phi_{in}+V_w}{(V_{SS}+2V_{th})} \quad \text{(B.39)}$$

The fixed part of memristance remains same for ideal and non-ideal grounded decremental memristor emulator circuit whereas variable part is changed due to parasitic impedances at various terminals of VDGA. The value of parasitic capacitance Cz1+ is very low and therefore the effect of Cz1+ on the performance of memristor emulator circuit will be negligible. The source resistance value Rs is very low and therefore the effect of parasitic impedance Zz- becomes negligible. The voltage transfer gain (β) is approximately equal to 1. The parasitic resistance Rw appears in series and has neglible effect on the performance of memristor emulator circuits. It is observed from Equation (B.39) that the effects of parasitic impedances on the performance of memristor emulator circuits are negligible and thereby its performance are found to be satisfactory in non-ideal conditions.

B.4 Non-ideal analysis of proposed memristor emulator using FB-VDBA

Non-ideal equivalent model of proposed grounded memristor emulator circuit is shown in Fig. B.3 which includes the effect of parasitic impedances. The parasitic resistance and capacitance (Rp and Cp) appear in parallel at "p" terminal of FB-VDBA and is presented by parasitic impedance Zp. Similarly, parasitic resistance and capacitance (Rn and Cn) are connected in parallel at "n" terminal of FB-VDBA and is presented by parasitic impedance Zn.

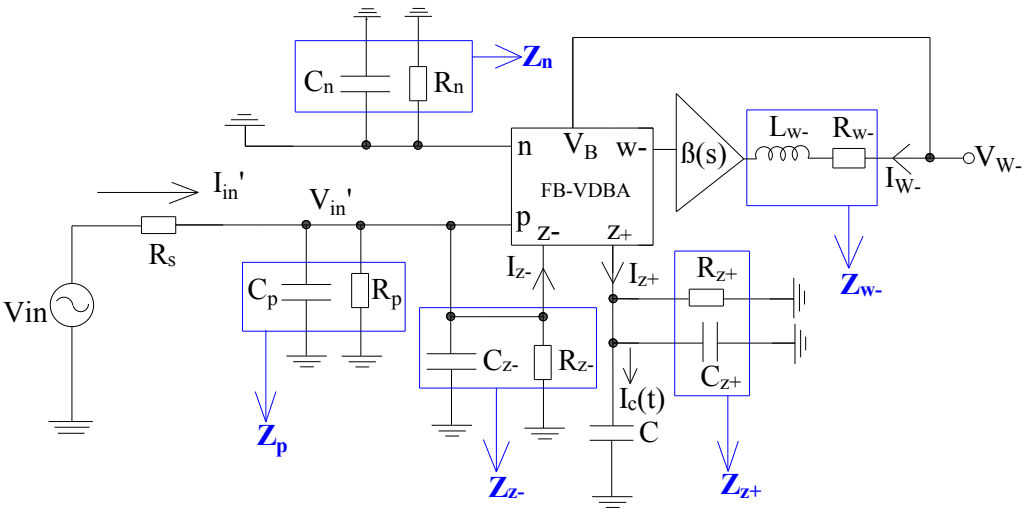

Fig.B.3 Non-ideal equivalent model of proposed decremental G-MRE based on FB-VDBA.

Parasitic resistance and capacitance (Rz- and Cz-) appear in parallel at "z-" terminal and is presented by parasitic impedance Zz-. Similarly, parasitic resistance and capacitance (Rz+ and Cz+) are connected in parallel at "z+" terminal and is presented by parasitic impedance Zz+. The voltages (Vz+ and Vz-) at z+ and z- terminals are copied with the help of internal buffer of FB-VDBA. The parasitic resistance and inductance (Rw- and Lw-) appear in series at "w-" terminal and is presented by parasitic impedance Zw-.
The values of parasitic impedances Zp, Zn, Zz-, Zz+ and Zw- are given by

$$Z_p = \frac{1}{sC_p + \frac{1}{R_p}}, \qquad Z_n = \frac{1}{sC_n + \frac{1}{R_n}} \tag{B.40}$$

$$Z_{z+} = \frac{1}{sC_{z+} + \frac{1}{R_{z+}}}, \qquad Z_{z-} = \frac{1}{sC_{z-} + \frac{1}{R_{z-}}} \tag{B.41}$$

$$Z_{w-} = R_{w-} + sL_{w-} \tag{B.42}$$

The routine analysis of Fig. B.3 yields the value of current Iz- at intermediate terminal "z-" of FB-VDBA as

$$I_{z-} = G_m(s)V_{in}' = G_m(s)V_{in} \times \frac{1}{1 + G_m(s)R_s + \frac{R_s}{Z_p \parallel Z_{z-}}} \tag{B.43}$$

where Rs is the source resistance of input voltage Vin.
The current Iz+ of FB-VDBA is the same as obtained in Equation (B.43).

$$I_{z+} = G_m(s)V_{in} \times \frac{1}{1 + G_m(s)R_s + \frac{R_s}{Z_p \parallel Z_{z-}}} \tag{B.44}$$

The voltage Vz+ is obtained at z+ terminal of FB-VDBA as

$$V_{z+} = I_{z+} \times \frac{1}{s(C + C_{Z+}) + \frac{1}{R_{z+}}} \tag{B.45}$$

The value of Vz+ is obtained with help of Eqations. (B.44) and (B.45) as given in Equation (B.46).

$$V_{z+} = G_m(s)V_{in} \times \frac{1}{1 + G_m(s)R_s + \dfrac{R_s}{Z_p \parallel Z_{z-}}} \times \frac{1}{s(C + C_{z+}) + \dfrac{1}{R_{z+}}} \tag{B.46}$$

Since the value of 1/Rz+ << s(C+Cz+), the Equation (B.46) can be modified as

$$V_{z+} \cong G_m(s)V_{in} \times \frac{1}{1 + G_m(s)R_s + \dfrac{R_s}{Z_p \parallel Z_{z-}}} \times \frac{1}{s(C + C_{z+})} \tag{B.47}$$

The Equation (B.47) can be rewritten as

$$V_{z+} \cong \frac{1}{(C + C_{Z+})} \times \frac{1}{1 + G_m(s)R_s + \dfrac{R_s}{Z_p \parallel Z_{z-}}} \int G_m(s)V_{in}(t)dt \tag{B.48}$$

The voltage Vw- can be expressed as given in Equation (B.49) after considering the parasitic impedance Zw- of FB-VDBA.

$$V_{w-} = -[\beta(s)V_{z+} - I_{w-}Z_{w-}] \tag{B.49}$$

The voltage transfer ratio between z+ and w- terminals of FB-VDBA can be defined as

$$\beta(s) = \frac{\beta(0)}{1 + \dfrac{s}{\omega_\beta}} \tag{B.50}$$

where, β (0) is the voltage transfer ratio between z+ and w- terminals of FB-VDBA at dc and ω_β is the corresponding pole frequency.

Replacing the voltage V_{z+} from Equation (B.48) into Equation (B.49), the voltage V_{W-} can be written as

$$V_w' \cong -\left(\beta(s) \frac{1}{(C + C_{Z+})} \times \frac{1}{1 + G_m(s)R_s + \dfrac{R_s}{Z_p \parallel Z_{z-}}} \int G_m(s)V_{in}(t)dt - I_{w-}.Z_{w-} \right) \tag{B.51}$$

The biasing voltage V_B is directly connected to V_{W-} in Fig. B.3 and can be expressed as

$$V_B \cong -\left(\beta(s) \frac{1}{(C + C_{Z+})} \times \frac{1}{1 + G_m(s) R_s + \frac{R_s}{Z_p \parallel Z_{z-}}} \int G_m(s) V_{in}(t) dt - I_{w-}.Z_{w-} \right) \tag{B.52}$$

The term $\int V_{in}(t)dt$ can be represented by flux (ϕ) and thereby Equation (B.52) is now changed to

$$V_B \cong -\left(G_m(s)\beta(s) \frac{1}{(C + C_{Z+})} \times \frac{1}{1 + G_m(s) R_s + \frac{R_s}{Z_p \parallel Z_{z-}}} .\phi_{in} - I_{w-}.Z_{w-} \right) \tag{B.53}$$

After replacing the voltage V_B from Equation (B.53) into Equation (3.2), we get

$$G_m(s) = \frac{k}{\sqrt{2}} \left[-\left(G_m(s).\beta(s).\frac{1}{(C + C_Z)}.\frac{1}{1 + G_m(s) R_s + \frac{R_s}{Z_p \parallel Z_{z-}}} .\phi_{in} - I_{W-}.Z_{w-} \right) - V_{SS} - 2V_{th} \right] \tag{B.54}$$

The Equation (B.54) can be rearranged as

$$G_m(s) = -\frac{\frac{k}{\sqrt{2}}(V_{SS} + 2V_{th})}{1 + \frac{k}{\sqrt{2}} \left[\beta(s).\frac{1}{(C + C_Z)}.\frac{1}{1 + G_m(s) R_s + \frac{R_s}{Z_p \parallel Z_{z-}}} .\phi_{in} - I_{W-}.Z_{w-} \right]} \tag{B.55}$$

The value of input current Iin' (t) can be obtained from Fig B.3 as

$$I_{in}'(t) = I_{z-} \times \left[1 + \frac{R_o}{Z_p \parallel Z_{z-}} \right] \tag{B.56}$$

where R_0 is the output resistance of z- terminal of FB-VDBA.

After replacing the current Iz- from Equation (B.43) to Equation (B.56), we get

$$I_{in}'(t) = G_m(s) V_{in}'(t) \left[1 + \frac{R_o}{Z_p \parallel Z_{z-}} \right] \tag{B.57}$$

The value of memristance $M(\phi_m)$ for the non-ideal decremental grounded memristor emulator circuit is obtained from Equation (B.57) as

$$M(\phi_m) = \frac{V_{in}'(t)}{I_{in}'(t)} = \frac{1}{G_m(s)} \times \frac{1}{1 + \frac{R_o}{Z_p \parallel Z_{z-}}} \tag{B.58}$$

When the value of Gm (s) is substituted from Equation (B.54) into Equation (B.58), we get the value of memristance $M(\phi_m)$ as

$$M(\phi_m) = \frac{V_{in}'(t)}{I_{in}'(t)} = -\frac{1}{\frac{k}{\sqrt{2}}(V_{SS} + 2V_{th})} - \frac{\beta(s).\frac{1}{(C + C_{Z+})}.\frac{1}{1 + G_m(s)R_s + \frac{R_s}{Z_p \parallel Z_{z-}}}.\phi_{in} - I_{W-}.Z_{w-}}{(V_{SS} + 2V_{th})} \tag{B.59}$$

The fixed part of memristance remains same for ideal and non-ideal grounded decremental memristor emulator circuit whereas variable part is changed due to parasitic impedances at various terminals of FB-VDBA. The value of parasitic capacitance Cz+ is very low and therefore the effect of Cz+ on the performance of memristor emulator circuit will be negligible. The source resistance value Rs is very low and therefore the effect of parasitic impedance Zz- becomes negligible. The voltage gain (β) is very close to one and it remains in acceptable range upto 1 MHz frequency. The parasitic impedance Zw- appears in series and has neglible effect on the performance of memristor emulator circuits. It is observed from Equation (B.59) that the effects of parasitic impedances on the performance of memristor emulator circuits are negligible and thereby its performance are found to be satisfactory in non-ideal conditions

B.5 Non-ideal analysis of proposed meminductor emulator using OTA and CDBA

After considering the non-ideal effects of OTA and CDBA, the proposed non-ideal equivalent model of grounded decremental meminductor emulator is shown in Fig. B.4. Parallel combinations of parasitic resistances and parasitic capacitances $R_{in1+} \parallel \frac{1}{sC_{in+}}$, $R_{x2+} \parallel \frac{1}{sC_{x2+}}$, $R_{x1+} \parallel \frac{1}{sC_{x1+}}$, $R_{x1-} \parallel \frac{1}{s(C_{x1-}+C_1)}$, $R_{in2+} \parallel \frac{1}{sC_{in2+}}$, $R_{x2-} \parallel \frac{1}{sC_{x2-}}$, $R_{in1-} \parallel \frac{1}{sC_{in-}}$, $R_{in2-} \parallel \frac{1}{sC_{in-}}$ and $R_z \parallel \frac{1}{s(C_z+C_2)}$ at different terminals of OTA and CDBA are represented by

impedances Z_{p1}, Z_{p2}, Z_{p3}, Z_{p4}, Z_{p5}, Z_{p6}, Z_{p7}, Z_{p8} and Z_{p9} respectively. The series combination of inductor (L_w) and resistance (R_w) is represented by Z_{s1}.

The following equations representing the non-ideality of the proposed grounded meminductor using OTA and CDBA.

The output current at "X_2-"terminal is equivalent to "I_{in}" which can be expressed as

$$I_{in} = I_{x2-} = gm_2(s)V'_{in2}(t) \tag{B.60}$$

The equation (B.61), represents the output current at "X_2-"terminal

$$I_{x2-} = gm_2(s)V'_{in2}(t) \times \frac{1}{gm_2(s)R_s + \frac{R_s}{Z_{p1}||Z_{p2}}} \tag{B.61}$$

The voltage at V_{in2+} terminal is

$$V'_{in2}(t) = \frac{I_{x1-}}{s(C_1 + C_{o-} + C_{in+}) + \frac{1}{R_{o-} + R_{in2+}}} \tag{B.62}$$

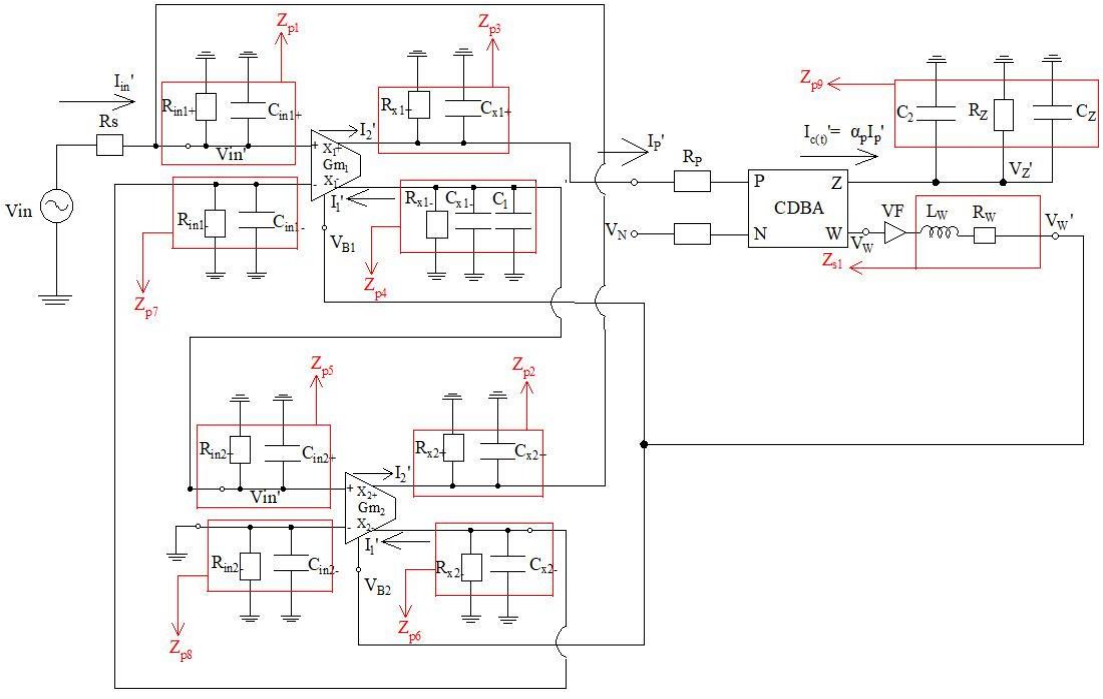

Fig B.4 Non-ideal equivalent model of proposed decremental G-MIE based on OTA and CDBA

$$\frac{1}{R_{o-}+R_{in2+}} \ll C_1 + C_{o-} + C_{in+}$$

Therefore,

$$V'_{in2}(t) = -\frac{I_{x1-}}{s(C_1 + C_{o-} + C_{in+})} \tag{B.63}$$

Assume $C_1 + C_{o-} + C_{in+} = C_{eq}$

The equation (B.63) can be rewritten as,

$$V'_{in2}(t) = -\frac{1}{C_{eq}} \int gm_1(s) V'_{in1}(t) \tag{B.64}$$

The equation (B.64) can be evaluated as

$$V'_{in2}(t) = -\frac{1}{C_{eq}} gm_1(s) \phi'_1(t) \tag{B.65}$$

Substitute the $V'_{in2}(t)$ of equation (B.65) in equation (B.61)

$$I_{in} = I_{x2-} = -\frac{gm_1(s)gm_2(s)}{C_{eq}} \times \frac{\phi'_1(t)}{gm_2(s)R_s + \frac{R_s}{Z_{p1}||Z_{p2}}} \tag{B.66}$$

The current at Z terminal of CDBA is expressed as

$$I'_z(t) = \alpha_P I'_P = \alpha_P [I'_{x1+}(t)] \times \frac{Z_{p3}}{R_p + Z_{p3}} \tag{B.67}$$

The equation (B.67) can be evaluated as

$$I'_z(t) = \alpha_P gm_1(s) V_{in1}(t) \times \frac{1}{1 + gm_2(s)R_s + \frac{R_s}{Z_{p1}||Z_{p2}}} \times \frac{Z_{p3}}{R_p + Z_{p3}} \tag{B.68}$$

where α_P is the current transfer ratio from P terminal to Z terminal, R_P is the parasitic resistance at input P terminal of CDBA and $Z_{p1} = \frac{1}{sC_p + \frac{1}{R_p}}$ and $Z_{p3} = \frac{1}{sC_{z-} + \frac{1}{R_{z-}}}$

The voltage at "Z" terminal of CDBA is

$$V'_z(t) = I'_{x1}(t) \times Z_{p9} \tag{B.69}$$

Where, $Z_{p9} = \frac{1}{s(C_2 + C_z) + \frac{1}{R_z}}$ and $\frac{1}{R_z} \ll C_2 + C_z$

By comparing equation (B.67) and equation (B.68), we get

$$V_z'(t) = \alpha_P gm_1(s)V_{in1}(t) \times \frac{1}{1 + gm_2(s)R_s + \frac{R_s}{Z_{p1}||Z_{p2}}} \times \frac{Z_{p3}}{R_p + Z_{p3}} \times \frac{1}{s(C_2 + C_z)} \tag{B.70}$$

After evaluating $V_z'(t)$ we get

$$V_z'(t) = \frac{1}{(C_2 + C_z)} \times \frac{\alpha_P}{1 + gm_2(s)R_s + \frac{R_s}{Z_{p1}||Z_{p2}}} \times \frac{Z_{p3}}{R_p + Z_{p3}} \int gm_1(s)V_{in1}(t) \tag{B.71}$$

The performance of the calculations using equation (B.71) results in

$$V_z'(t) = \frac{gm_1(s)}{(C_2 + C_z)} \times \frac{\alpha_P}{1 + gm_2(s)R_s + \frac{R_s}{Z_{p1}||Z_{p2}}} \times \frac{Z_{p3}}{R_p + Z_{p3}} \phi_{in}(t) \tag{B.72}$$

The voltage V_W' at W terminal of CDBA can be expressed as

$$V_w' = \beta(s)V_z' + I_w R_w \tag{B.73}$$

The voltage transfer ratio of Z terminal and W terminal (gain of buffer amplifier) of CDBA can be defined as

$$\beta(s) = \frac{\beta(0)}{1 + \frac{s}{\omega_\beta}} \tag{B.74}$$

where, β (0) is the value of gain of buffer amplifier of CDBA at low frequency and ω_β represents the corresponding pole frequency

After substituting of equation (B.72) in equation (B.73). The voltage V_W' at W terminal of CDBA is obtained and can be written as

$$V_w' = \beta(s)\frac{gm_1(s)}{(C_2 + C_z)} \times \frac{\alpha_P}{1 + gm_2(s)R_s + \frac{R_s}{Z_{p1}||Z_{p2}}} \times \frac{Z_{p3}}{R_p + Z_{p3}} \phi_{in}(t) + I_w R_w \tag{B.75}$$

The biasing voltage V_B is equal to V_W' and can be expressed as

$$V_B = V_w' \tag{B.76}$$

Therefore, V_B can be written as

$$V_B = \beta(s)\frac{gm_1(s)}{(C_2+C_z)} \times \frac{\alpha_P}{1+gm_2(s)R_s+\frac{R_s}{Z_{p1}||Z_{p2}}} \times \frac{Z_{p3}}{R_p+Z_{p3}}\phi_{in}(t) + I_w R_w \tag{B.77}$$

Now, substituting the value of V_B in Equation (3.2), results in

$$g_{m1}(s) = \frac{K}{\sqrt{2}}\left[\left(\beta(s)\frac{gm_1(s)}{(C_2+C_z)} \times \frac{\alpha_P}{1+gm_2(s)R_s+\frac{R_s}{Z_{p1}||Z_{p2}}} \times \frac{Z_{p3}}{R_p+Z_{p3}}\phi_{in}(t) + I_w R_w\right) - V_{SS} - 2V_{TH}\right] \tag{B.78}$$

By rearranging the equation (B.78), we get

$$g_{m1}(s) = \frac{\frac{K}{\sqrt{2}}(V_{SS}+2V_{TH})}{1-\frac{K}{\sqrt{2}}\left[\beta(s)\frac{\alpha_P}{(C_2+C_z)}\frac{1}{1+g_m(s)R_s+\frac{R_s}{Z_{p1}||Z_{p2}}} \times \frac{Z_{p3}}{R_p+Z_{p3}}\phi_{in}(t)+I_w R_w\right]} \tag{B.79}$$

The relation between flux ϕ (t) and current I (t) is given by

$$I(t) = M_L^{-1}\phi(t) \tag{B.80}$$

Therefore, by comparing equation (B.66) and equation (B.80) results comes in

$$I_{in}(t) = -\frac{gm_1(s)gm_2(s)}{C_{eq}} \times \frac{\phi'_1(t)}{1+g_m(s)R_s+\frac{R_s}{Z_{p1}||Z_{p2}}} \tag{B.81}$$

Bias voltages (V_B) of both OTAs are the same as can be seen from the Fig. B.4 Therefore, the transconductances (G_{m1} and G_{m2}) of both OTAs are equal. Substituting $G_{m1} = G_{m2} = G_m$ into equation (B.81) result into

$$I_{in}(t) = -\frac{g_m^2(s)}{C_{eq}} \times \frac{\phi'_1(t)}{1+g_m(s)R_s+\frac{R_s}{Z_{p1}||Z_{p2}}} \tag{B.82}$$

By comparing equation (B.80) and equation (B.82),

$$M_L^{-1} = -\frac{g_m^2(s)}{C_{eq}} \times \frac{1}{1 + g_m(s)R_s + \frac{R_s}{Z_{p1}||Z_{p2}}} \tag{B.83}$$

Where, $M_L^{-1}$is inverse meminductance.

$$M_L = \frac{C_{eq}}{gm^2} \times \left(1 + g_m(s)R_s + \frac{R_s}{Z_{p1}||Z_{p2}}\right) \tag{B.84}$$

Substitute $gm(s)$ value from equation (B.81) in equation (B.84), results

$$M_L = \frac{C_{eq} \times \left(1 + g_m(s)R_s + \frac{R_s}{Z_{p1}||Z_{p2}}\right)}{\left(\frac{\frac{K}{\sqrt{2}}(V_{SS}+2V_{TH})}{1 - \frac{K}{\sqrt{2}}\left[\beta(s)\frac{\alpha_P}{(C_2+C_z)}\frac{1}{1+g_m(s)R_s+\frac{R_s}{Z_{p1}||Z_{p2}}} \times \frac{Z_{p3}}{R_p+Z_{p3}}\phi_{in}(t)+I_W R_W\right]}\right)^2} \tag{B.85}$$

After evaluation equation (B.84), the meminductance of grounded meminductor emulator will be

$$M_L = \frac{C_{eq} \times (1 + g_m(s)R_s + \frac{R_s}{Z_{p1}||Z_{p2}})}{K^2(V_{SS}+2V_{TH})^2} \times \left[1 - \frac{K}{\sqrt{2}}\left(\beta(s)\frac{\alpha_P}{(C_2+C_z)}\frac{1}{1+g_m(s)R_s+\frac{R_s}{Z_{p1}||Z_{p2}}} \times \frac{Z_{p3}}{R_p+Z_{p3}}\phi_{in}(t) + I_w R_w\right)\right]^2 \tag{B.86}$$

Rearrange equation (B.86), the equation (B.87) results as

$$M_L = \frac{2C_{eq} \times (1 + g_m(s)R_s + \frac{R_s}{Z_{p1}||Z_{p2}}}{K^2(V_{SS}+2V_{TH})^2} - \frac{2C_{eq} \times (1 + g_m(s)R_s + \frac{R_s}{Z_{p1}||Z_{p2}}\phi_{in}\left[\frac{K}{2}\beta(s)\frac{\alpha_P}{(C_2+C_z)}\frac{1}{1+g_m(s)R_s+\frac{R_s}{Z_{p1}||Z_{p2}}}\frac{Z_{p3}}{Rp+Z_{p3}}\phi_{in}(t)+I_W R_W - \sqrt{2}\right]}{K(C_2+C_z)(V_{SS}+2V_{TH})^2} \tag{B.87}$$

The first part in equation is fixed and the other part is variable in the equation (B.87)

$$M_L = \frac{2C_{eq}\times(1+g_m(s)R_s+\frac{R_s}{Z_{p1}||Z_{p2}}}{K^2(V_{SS}+2V_{TH})^2} \pm \frac{2C_{eq}\times(1+g_m(s)R_s+\frac{R_s}{Z_{p1}||Z_{p2}}\phi_{in}\left[\frac{K}{2}\beta(s)\frac{\alpha_P}{(C_2+C_z)}\frac{1}{1+g_m(s)R_s+\frac{R_s}{Z_{p1}||Z_{p2}}}\frac{Z_{p3}}{Rp+Z_{p3}}\phi_{in}(t)+I_wR_w-\sqrt{2}\right]}{K(C_2+C_z)(V_{SS}+2V_{TH})^2} \quad \text{(B.88)}$$

The equation (B.88) shows the incremental and decremental expression for grounded meminductor emulator using OTA and CDBA.

B.6 Non-ideal analysis of proposed meminductor emulators using VDGA and CDBA

After considering the non-ideal effects of VDGA and CDBA, the proposed non-ideal equivalent model of grounded decremental meminductor emulator is shown in Fig. B.5 Parallel combinations of parasitic resistances and parasitic capacitances. $R_p||\frac{1}{sC_p}$, $R_{Z-}||\frac{1}{sC_{Z-}}$, $R_w||\frac{1}{sC_W}$, $R_{Z+}||\frac{1}{s\,(C_{Z+}+C_1)}$ and $R_z||\frac{1}{s\,(C_z+C_2)}$, at different terminals of VDGA and CDBA are represented by impedances Z_{p1}, Z_{p2}, Z_{p3}, Z_{p4} and Z_{p5} respectively. The series combination of inductor (L_w) and resistance (R_w) is represented by Z_{s1}.

The following equations representing the non-ideality of the proposed grounded meminductor using VDGA and CDBA.

The voltage at "Z" terminal of VDGA is

$$V'_{z+}(t) = \frac{I'_{z+}(t)}{s(C_1 + C_{z+})} \quad \text{(B.89)}$$

After evaluating equation (B.89),

$$V'_{z+}(t) = \frac{1}{(C_1 + C_{z+})}\int I'_{z+}(t) \quad \text{(B.90)}$$

The current at the output of "Z" terminal of VDGA is

$$I_{Z+} = gm_1(V_P - V_N) = gm_1V_{in} \quad \text{(B.91)}$$

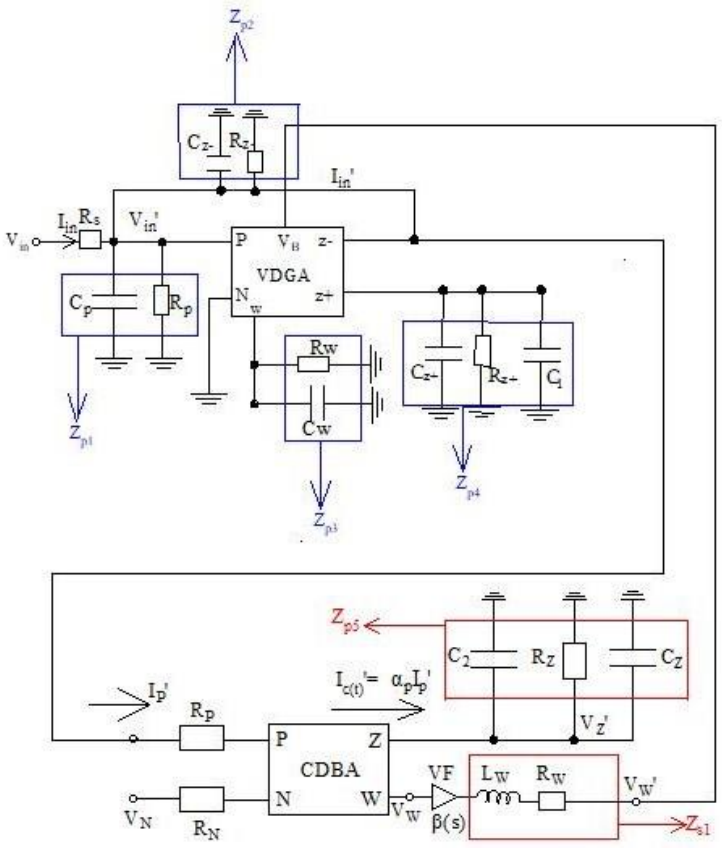

Fig. B.5 Non-ideal equivalent model of proposed decremental G-MIE based on VDGA and CDBA.

The current at the output of "Z" terminal of VDGA while including parasitic is

$$I'_{z+}(t) = gm_1(s)V'_{in}(t) \times \frac{1}{gm_1(s)R_s + \frac{R_s}{Z_{p1}||Z_{p2}}} \tag{B.92}$$

Substituting the value of $I'_z(t)$ from equation (B.92) in equation (B.90)

$$V'_{z+}(t) = \frac{1}{(C_1 + C_{z+})} \times \frac{gm_1}{1 + gm_1(s)R_s + \frac{R_s}{Z_{p1}||Z_{p2}}} \int V'_{in}(t) \tag{B.93}$$

After evaluating the equation (B.93), results

$$V'_{z+}(t) = \frac{1}{(C_1 + C_{z+})} \times \frac{gm_1}{1 + gm_1(s)R_s + \frac{R_s}{Z_{p1}||Z_{p2}}} \phi_{in}(t) \tag{B.94}$$

The current at Z terminal of CDBA is expressed as

$$I'_z(t) = \alpha_P I'_P = \alpha_P[I'_{in}(t) + I'_{z2-}(t)] \times \frac{Z_{p5}}{R_p + Z_{p1}||Z_{p2}} \tag{B.95}$$

whereas,

$$I'_{z2-}(t) = gm_2 V'_{z+}(t) \tag{B.96}$$

Substituting the value of $I'_{z2-}(t)$ from equation (B.96) in equation (B.95). The equation (B.96) can be evaluated as

$$I'_z(t) = \alpha_P I'_P = \alpha_P[I'_{in}(t) + gm_2 V'_{z+}(t)] \times \frac{Z_{p5}}{R_p + Z_{p1}||Z_{p2}} \tag{B.97}$$

where α_P is the current transfer ratio from P terminal to Z terminal, R_P is the parasitic resistance at input P terminal of CDBA.

Replace the value of $V'_{z+}(t)$ from equation (B.94) in equation (B.98)

$$I'_z(t) = \alpha_P \left[I'_{in}(t) + gm_2 \frac{1}{(C_1+C_{z+})} \times \frac{gm_1}{1+gm_1(s)R_s+\frac{R_s}{Z_{p1}||Z_{p2}}} \phi_{in}(t) \right] \times \frac{Z_{p5}}{R_p+Z_{p1}||Z_{p2}} \tag{B.98}$$

The voltage at "Z" terminal of CDBA is

$$V'_z(t) = -\frac{1}{s\left(C_2 + C_z + \frac{1}{R_z}\right)} I'_z(t) \tag{B.99}$$

As, $\frac{1}{R_z} \ll C_2 + C_z$

Substituting the value of $I'_z(t)$ from equation (B.98) in equation (B.99)

$$V'_z(t) = -\frac{1}{s(C_2+C_z)} \times \alpha_P \left[I'_{in}(t) + \frac{gm_2}{(C_1+C_{z+})} \times \frac{gm_1}{1+gm_1(s)R_s+\frac{R_s}{Z_{p1}||Z_{p2}}} \phi_{in}(t) \right] \times \frac{Z_{p5}}{R_p+Z_{p1}||Z_{p2}} \tag{B.100}$$

The evaluating equation (B.100) results in

$$V_z'(t) = -\frac{1}{(C_2+C_z)} \times \frac{Z_{p5}}{R_p+Z_{p1}||Z_{p2}} \int \alpha_P \left[I_{in}'(t) + \frac{gm_2}{(C_1+C_{z+})} \times \frac{gm_1}{1+gm_1(s)R_s+\frac{R_s}{Z_{p1}||Z_{p2}}} \phi_{in}(t) \right] \quad \text{(B.101)}$$

Rearranging equation (B.101), we get

$$V_z'(t) = -\frac{1}{(C_2+C_z)} \times \frac{Z_{p5}}{R_p+Z_{p1}||Z_{p2}} \times \alpha_P \left[q_{in}(t) + \frac{gm_2}{(C_1+C_{z+})} \times \frac{gm_1}{1+gm_1(s)R_s+\frac{R_s}{Z_{p1}||Z_{p2}}} \rho_{in}(t) \right] \quad \text{(B.102)}$$

The voltage V_W' at W terminal of CDBA can be expressed as

$$V_w' = \beta(s)V_z' + I_w R_w \quad \text{(B.103)}$$

The voltage transfer ratio of Z terminal and W terminal (gain of buffer amplifier) of CDBA can be defined as

$$\beta(s) = \frac{\beta(0)}{1+\frac{s}{\omega_\beta}} \quad \text{(B.104)}$$

where, β (0) is the value of gain of buffer amplifier of CDBA at low frequency and ω_β represents the corresponding pole frequency

After substituting of equation (B.102) into equation (B.103), the voltage V_W' at W terminal of CDBA is obtained as

$$V_w' = -\beta(s) \times \frac{1}{(C_2+C_z)} \times \frac{Z_{p5}}{R_p+Z_{p1}||Z_{p2}} \times \alpha_P \left[q_{in}(t) + \frac{gm_2}{(C_1+C_{z+})} \times \frac{gm_1}{1+gm_1(s)R_s+\frac{R_s}{Z_{p1}||Z_{p2}}} \rho_{in}(t) \right] + I_w R_w \quad \text{(B.105)}$$

The biasing voltage V_B is equal to V_W' and can be expressed as

$$V_B = V_w' \quad \text{(B.106)}$$

Therefore, V_B can be written as

$$V_B = -\beta(s) \times \frac{1}{(C_2 + C_z)} \times \frac{Z_{p5}}{R_p + Z_{p1}||Z_{p2}} \times \alpha_P \left[q_{in}(t) + \frac{gm_2}{(C_1 + C_{z+})} \times \frac{gm_1}{1 + gm_1(s)R_s + \frac{R_s}{Z_{p1}||Z_{p2}}} \rho_{in}(t) \right] + I_w R_w \tag{B.107}$$

Now, substituting the value of V_B in Equation (3.2), results in

$$g_{m1}(s) = -\frac{K}{\sqrt{2}} \left[\left(\beta(s) \times \frac{1}{(C_2+C_z)} \times \frac{Z_{p5}}{R_p+Z_{p1}||Z_{p2}} \times \alpha_P \left[q_{in}(t) + \frac{gm_2}{(C_1+C_{z+})} \times \frac{gm_1}{1+gm_1(s)R_s+\frac{R_s}{Z_{p1}||Z_{p2}}} \rho_{in}(t) \right] + I_w R_w \right) - V_{SS} - 2V_{TH} \right] \tag{B.108}$$

By rearranging the equation (B.108), we get

$$g_{m1}(s) = -\frac{\frac{K}{\sqrt{2}}(V_{SS}+2V_{TH})}{1-\frac{K}{\sqrt{2}} \left[\beta(s) \times \frac{1}{(C_2+C_z)} \times \frac{Z_{p5}}{R_p+Z_{p1}||Z_{p2}} \times \alpha_P [q_{in}(t) + \frac{gm_2}{(C_1+C_{z+})} \times \frac{gm_1}{1+gm_1(s)R_s+\frac{R_s}{Z_{p1}||Z_{p2}}} \rho_{in}(t)] + I_w R_w \right]} \tag{B.109}$$

As we know,

$$I_{z-} = -gm_2(s) V'_{z+}(t) \tag{B.110}$$

Substitute $V'_{z+}(t)$ value from equation (B.93) in equation (B.101)

$$I_{z-} = -gm_2(s) \times \frac{1}{s(C_1 + C_{z+})} \times \frac{gm_1(s)}{1 + gm_1(s)R_s + \frac{R_s}{Z_{p1}||Z_{p2}}} \phi_{in}(t) \tag{B.111}$$

Replace the $g_{m1}(s)$ value in equation (B.111)

$$I_{z-} = -\frac{gm_2(s)K}{(C_1+C_{z+})} \times \frac{\phi(t)}{1+gm_1(s)R_s+\frac{R_s}{Z_{p1}||Z_{p2}}} \left[K \left\{ -\frac{\alpha_P}{(C_2+C_z)} \times \frac{gm_1(s)gm_2(s)}{(C_1+C_{z+}) \times 1+gm_1(s)R_s+\frac{R_s}{Z_{p1}||Z_{p2}}} + \frac{q_{in}(t)}{(C_2+C_z)} \right\} \times \frac{Z_{p5}}{R_p+Z_{p1}||Z_{p2}} \right] - V_{SS} - 2V_{TH} \tag{B.112}$$

The relation between flux ϕ (t) and current I (t) is given by

$$I(t) = M_L^{-1}\phi(t) \tag{B.113}$$

Therefore, by comparing equation (B.113) and equation (B.94), the value of inverse meminductance is obtained as

$$M_L^{-1} = \frac{gm_2(s)K}{(C_1+C_{z+})} \times \frac{1}{1+gm_1(s)R_s+\frac{R_s}{Z_{p1}||Z_{p2}}}\left[K\left\{-\frac{\alpha_P}{(C_2+C_z)} \times \frac{gm_1(s)gm_2(s)}{(C_1+C_{z+})\times 1+gm_1(s)R_s+\frac{R_s}{Z_{p1}||Z_{p2}}} + \frac{q_{in}(t)}{(C_2+C_z)}\right\} \times \frac{Z_{p5}}{R_p+Z_{p1}||Z_{p2}}\right] - V_{SS} - 2V_{TH} \tag{B.114}$$

The equation (B.114) can be rearranged as

$$M_L^{-1} = \frac{gm_2(s)K}{(C_1+C_{z+})} \times \frac{1}{1+gm_1(s)R_s+\frac{R_s}{Z_{p1}||Z_{p2}}} \times \frac{Z_{p5}}{R_p+Z_{p1}||Z_{p2}}(V_{SS}+2V_{TH}) + \frac{gm_2(s)K}{(C_1+C_{z+})} \times \frac{1}{1+gm_1(s)R_s+\frac{R_s}{Z_{p1}||Z_{p2}}} \times \frac{Z_{p5}}{R_p+Z_{p1}||Z_{p2}}\left(-\frac{\alpha_P}{(C_2+C_z)} \times \frac{gm_1(s)gm_2(s)}{(C_1+C_{z+})\times 1+gm_1(s)R_s+\frac{R_s}{Z_{p1}||Z_{p2}}} + \frac{q_{in}(t)}{(C_2+C_z)}\right) \tag{B.115}$$

It can be concluded from Equation (B.115) and Equation (B.116) of meminductance that the first term is fixed as G_{m2} of VDGA is controlled by fixed biasing current I_{B1} and transconductance (G_{m1}) of VDGA it changed according to the bias voltage (V_B) which is indirectly proportional to the potential at capacitor C_2.

$$M_L = \frac{1}{\frac{gm_2(s)K}{(C_1+C_{z+})}\times\frac{1}{1+gm_1(s)R_s+\frac{R_s}{Z_{p1}||Z_{p2}}}\times\frac{Z_{p5}}{R_p+Z_{p1}||Z_{p2}}(V_{SS}+2V_{TH})} \pm \frac{1}{\frac{gm_2(s)K}{(C_1+C_{z+})}\times\frac{1}{1+gm_1(s)R_s+\frac{R_s}{Z_{p1}||Z_{p2}}}\times\frac{Z_{p5}}{R_p+Z_{p1}||Z_{p2}}\left(-\frac{\alpha_P}{(C_2+C_z)}\times\frac{gm_1(s)gm_2(s)}{(C_1+C_{z+})\times 1+gm_1(s)R_s+\frac{R_s}{Z_{p1}||Z_{p2}}}+\frac{q_{in}(t)}{(C_2+C_z)}\right)} \tag{B.116}$$

Equation (B.116) represents the expression for meminductance, where the "+" sign indicates expression for grounded incremental configuration and the "-“sign indicates expression for grounded decremental configuration.

B.7 Non-ideal analysis of proposed meminductor emulators using VDTA and CDBA

After considering the non-ideal effects of VDTA and CDBA, the proposed non-ideal equivalent model of grounded decremental meminductor emulator is shown in Fig. B.6. Parallel combinations of parasitic resistances and parasitic capacitances. $R_N||\frac{1}{s(C_p+C_{x-})}$, $R_{x+}||\frac{1}{sC_{x+}}$ $R_{z+}||\frac{1}{s(C_{z+}+C_1)}$ and $R_z||\frac{1}{s(C_z+C_2)}$, at different terminals of VDTA and CDBA are represented by impedances Z_{p1}, Z_{p2}, Z_{p3}, Z_{p4} and Z_{p5} respectively. The series combination of inductor (L_w) and resistance (R_w) is represented by Z_{s1}.

The following equations representing the non-ideality of the proposed grounded meminductor using VDTA and CDBA.

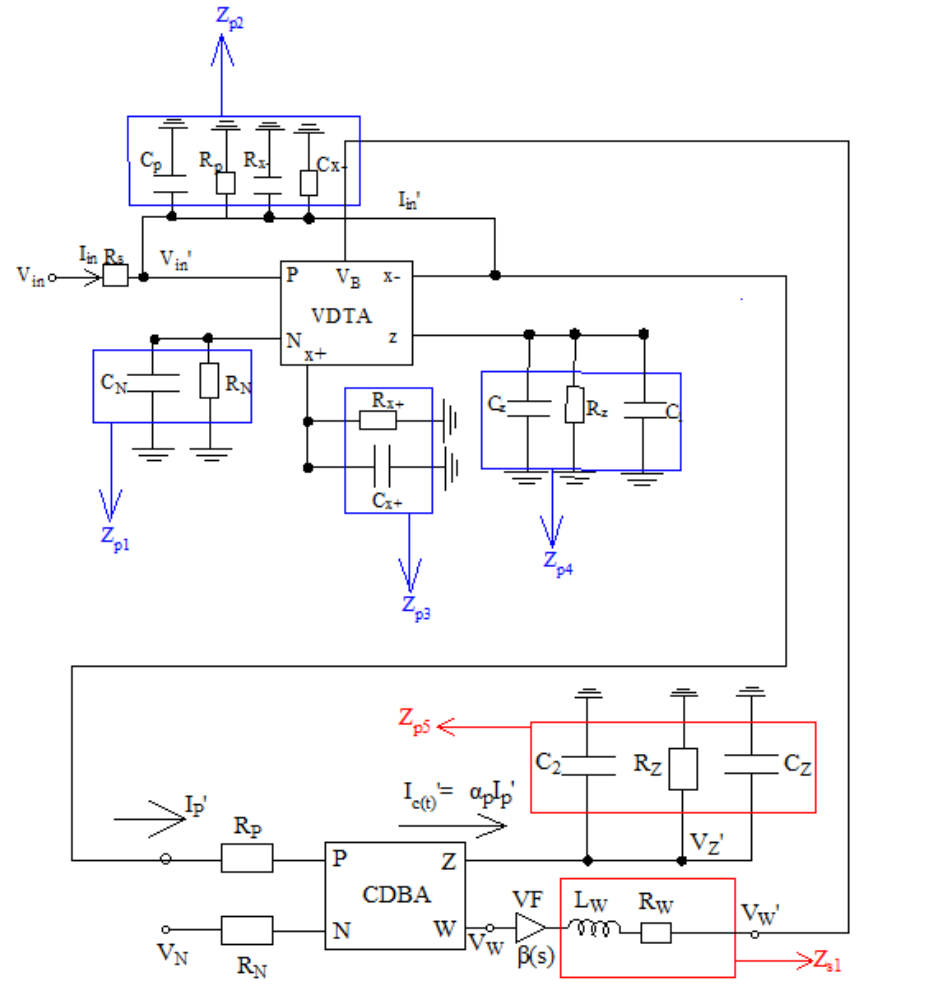

Fig B.6 Non-ideal equivalent model of proposed decremental G-MRE based on VDTA and CDBA

$$V'_{z+}(t) = \frac{I'_{z+}(t)}{s(C_1 + C_{z+})} \tag{B.117}$$

After evaluating equation (B.117),

$$V'_{z+}(t) = \frac{1}{(C_1 + C_{z+})} \int I'_{z+}(t) \tag{B.118}$$

The current at the output of "Z" terminal of VDGA is

$$I_{Z+} = gm_1(V_P - V_N) = gm_1 V_{in} \tag{B.119}$$

The current at the output of "Z" terminal of VDGA while including parasitic is

$$I'_z(t) = gm_1(s)V'_{in}(t) \times \frac{1}{gm_1(s)R_s + \frac{R_s}{Z_{p2}}} \tag{B.120}$$

Substituting the value of $I'_z(t)$ from equation (B.120) in equation (B.118)

$$V'_{z+}(t) = \frac{1}{(C_1 + C_{z+})} \times \frac{gm_1}{1 + gm_1(s)R_s + \frac{R_s}{Z_{p2}}} \int V'_{in}(t) \tag{B.121}$$

After evaluating the equation (B.121) results

$$V'_{z+}(t) = \frac{1}{(C_1 + C_{z+})} \times \frac{gm_1}{1 + gm_1(s)R_s + \frac{R_s}{Z_{p2}}} \phi_{in}(t) \tag{B.122}$$

The current at Z terminal of CDBA is expressed as

$$I'_z(t) = \alpha_P I'_P = \alpha_P [I'_{in}(t) + I'_{x-}(t)] \times \frac{Z_{p5}}{R_p + Z_{p2}} \tag{B.123}$$

where,

$$I'_{x-}(t) = gm_2 V'_{z+}(t) \tag{B.124}$$

Substituting the value of $I'_{x-}(t)$ from equation (B.124) in equation (B.123). The equation (B.125) can be evaluated as

$$I_z'(t) = \alpha_P I_P' = \alpha_P [I_{in}'(t) + gm_2 V_{z+}'(t)] \times \frac{Z_{p5}}{R_p + Z_{p2}} \tag{B.125}$$

where α_P is the current transfer ratio from P terminal to Z terminal, R_P is the parasitic resistance at input P terminal of CDBA.

Replace the value of $V_{z+}'(t)$ from equation (B.122) in equation (B.125)

$$I_z'(t) = \alpha_P \left[I_{in}'(t) + gm_2 \frac{1}{(C_1 + C_{z+})} \times \frac{gm_1}{1 + gm_1(s)R_s + \frac{R_s}{Z_{p2}}} \phi_{in}(t) \right] \times \frac{Z_{p5}}{R_p + Z_{p2}} \tag{B.126}$$

Rearrange equation (B.126), results in

$$I_z'(t) = \alpha_P \left[I_{in}'(t) + \frac{gm_2}{(C_1 + C_{z+})} \times \frac{gm_1}{1 + gm_1(s)R_s + \frac{R_s}{Z_{p2}}} \phi_{in}(t) \right] \times \frac{Z_{p5}}{R_p + Z_{p2}} \tag{B.127}$$

The voltage at "Z" terminal of CDBA is

$$V_z'(t) = -\frac{1}{s\left(C_2 + C_z + \frac{1}{R_z}\right)} I_z'(t) \tag{B.128}$$

As, $\frac{1}{R_z} \ll C_2 + C_z$

Substituting the value of $I_z'(t)$ from equation (B.127) in equation (B.128), we get

$$V_z'(t) = -\frac{1}{s(C_2 + C_z)} \times \alpha_P \left[I_{in}'(t) + \frac{gm_2}{(C_1 + C_{z+})} \times \frac{gm_1}{1 + gm_1(s)R_s + \frac{R_s}{Z_{p2}}} \phi_{in}(t) \right] \times \frac{Z_{p5}}{R_p + Z_{p2}} \tag{B.129}$$

The equation (B.129) can be rearranged into equation (B.130)

$$V_z'(t) = -\frac{1}{(C_2 + C_z)} \times \frac{Z_{p5}}{R_p + Z_{p2}} \int \alpha_P \left[I_{in}'(t) + \frac{gm_2}{(C_1 + C_{z+})} \times \frac{gm_1}{1 + gm_1(s)R_s + \frac{R_s}{Z_{p2}}} \phi_{in}(t) \right] \tag{B.130}$$

Rearranging equation (B.130), the result gets as (B.131)

$$V_z'(t) = -\frac{1}{(C_2+C_z)} \times \frac{Z_{p5}}{R_p+Z_{p1}||Z_{p2}} \times \alpha_P \left[q_{in}(t) + \frac{gm_2}{(C_1+C_{z+})} \times \frac{gm_1}{1+gm_1(s)R_s+\frac{R_s}{Z_{p2}}} \rho_{in}(t) \right] \quad \text{(B.131)}$$

The voltage V_W' at W terminal of CDBA can be expressed as

$$V_w' = \beta(s)V_z' + I_w R_w \quad \text{(B.132)}$$

The voltage transfer ratio of Z terminal and W terminal (gain of buffer amplifier) of CDBA can be defined as

$$\beta(s) = \frac{\beta(0)}{1+\frac{s}{\omega_\beta}} \quad \text{(B.133)}$$

where, β (0) is the value of gain of buffer amplifier of CDBA at low frequency and ω_β represents the corresponding pole frequency

After substituting the values obtained in equation (B.131) into equation (B.132). The voltage V_W' at W terminal of CDBA can be obtained as

$$V_w' = -\beta(s) \times \frac{1}{(C_2+C_z)} \times \frac{Z_{p5}}{R_p+ Z_{p2}} \times \alpha_P \left[q_{in}(t) + \frac{gm_2}{(C_1+C_{z+})} \times \frac{gm_1}{1+gm_1(s)R_s+\frac{R_s}{Z_{p2}}} \rho_{in}(t) \right] + I_w R_w \quad \text{(B.134)}$$

The biasing voltage V_B is equal to V_W' and can be expressed as

$$V_B = V_w' \quad \text{(B.135)}$$

Therefore, V_B can be written as

$$V_B = -\beta(s) \times \frac{1}{(C_2+C_z)} \times \frac{Z_{p5}}{R_p+Z_{p2}} \times \alpha_P \left[q_{in}(t) + \frac{gm_2}{(C_1+C_{z+})} \times \frac{gm_1}{1+gm_1(s)R_s+\frac{R_s}{Z_{p2}}} \rho_{in}(t) \right] + I_w R_w \quad \text{(B.136)}$$

Now, substituting the value of V_B in Equation (3.2), results in

$$g_{m1}(s) = -\frac{K}{\sqrt{2}} \left[\left(\beta(s) \times \frac{1}{(C_2+C_z)} \times \frac{Z_{p5}}{R_p+Z_{p2}} \times \alpha_P \left[q_{in}(t) + \frac{gm_2}{(C_1+C_{z+})} \times \frac{gm_1}{1+gm_1(s)R_s+\frac{R_s}{Z_{p2}}} \rho_{in}(t) \right] + I_w R_w \right) - V_{SS} - 2V_{TH} \right] \quad \text{(B.137)}$$

By rearranging the equation (B.137), we get

$$g_{m1}(s) = -\frac{\frac{K}{\sqrt{2}}(V_{SS}+2V_{TH})}{1-\frac{K}{\sqrt{2}} \left[\beta(s) \times \frac{1}{(C_2+C_z)} \times \frac{Z_{p5}}{R_p+Z_{p2}} \times \alpha_P [q_{in}(t) + \frac{gm_2}{(C_1+C_{z+})} \times \frac{gm_1}{1+gm_1(s)R_s+\frac{R_s}{Z_{p2}}} \rho_{in}(t)] + I_w R_w \right]} \quad \text{(B.138)}$$

As we know,

$$I_{z-} = -gm_2(s) V'_{z+}(t) \quad \text{(B.139)}$$

Substitute $V'_{z+}(t)$ value from equation (B.122) into equation (B.139)

$$I_{z-} = -gm_2(s) \times \frac{1}{s(C_1+C_{z+})} \times \frac{gm_1(s)}{1+gm_1(s)R_s+\frac{R_s}{Z_{p2}}} \phi_{in}(t) \quad \text{(B.140)}$$

Replacing the $g_{m1}(s)$ from (B.138) value in equation (B.140)

$$I_{z-} = -\frac{gm_2(s)K}{(C_1+C_{z+})} \times \frac{\phi(t)}{1+gm_1(s)R_s+\frac{R_s}{Z_{p2}}} \left[K \left\{ -\frac{\alpha_P}{(C_2+C_z)} \times \frac{gm_1(s)gm_2(s)}{(C_1+C_{z+})\times 1+gm_1(s)R_s+\frac{R_s}{Z_{p2}}} + \frac{q_{in}(t)}{(C_2+C_z)} \right\} \times \frac{Z_{p5}}{R_p+Z_{p2}} \right] - V_{SS} - 2V_{TH} \quad \text{(B.141)}$$

The relation between flux ϕ (t) and current I (t) is given by

$$I(t) = M_L^{-1}\phi(t) \tag{B.142}$$

Therefore, by comparing equation (B.141) and equation (B.142) results in

$$M_L^{-1} = \frac{gm_2(s)K}{(C_1+C_{z+})} \times \frac{1}{1+gm_1(s)R_s+\frac{R_s}{Z_{p2}}}\left[K\left\{-\frac{\alpha_P}{(C_2+C_z)} \times \frac{gm_1(s)gm_2(s)}{(C_1+C_{z+})\times 1+gm_1(s)R_s+\frac{R_s}{Z_{p2}}} + \frac{q_{in}(t)}{(C_2+C_z)}\right\} \times \frac{Z_{p5}}{R_p+Z_{p2}}\right] - V_{SS} - 2V_{TH} \tag{B.143}$$

The equation (B.143) can be rearranged as

$$M_L^{-1} = \frac{gm_2(s)K}{(C_1+C_{z+})} \times \frac{1}{1+gm_1(s)R_s+\frac{R_s}{Z_{p2}}} \times \frac{Z_{p5}}{R_p+Z_{p2}}(V_{SS}+2V_{TH}) + \frac{gm_2(s)K}{(C_1+C_{z+})} \times \frac{1}{1+gm_1(s)R_s+\frac{R_s}{Z_{p2}}} \times \frac{Z_{p5}}{R_p+Z_{p2}}\left(-\frac{\alpha_P}{(C_2+C_z)} \times \frac{gm_1(s)gm_2(s)}{(C_1+C_{z+})\times 1+gm_1(s)R_s+\frac{R_s}{Z_{p2}}} + \frac{q_{in}(t)}{(C_2+C_z)}\right) \tag{B.144}$$

It can be concluded from Equations (B.143) and (B.144) of meminductance that the first term is fixed as transconductance gain (G_{m2}) of VDGA is controlled by fixed biasing current I_{B1} and the transconductance gain (G_{m1}) of VDGA is changed according to the bias voltage (V_B) which is connected to the voltage across capFacitor C_2.

$$M_L = \frac{1}{\frac{gm_2(s)K}{(C_1+C_{z+})}\times\frac{1}{1+gm_1(s)R_s+\frac{R_s}{Z_{p2}}}\times\frac{Z_{p5}}{R_p+Z_{p2}}(V_{SS}+2V_{TH})} \pm \frac{1}{\frac{gm_2(s)K}{(C_1+C_{z+})}\times\frac{1}{1+gm_1(s)R_s+\frac{R_s}{Z_{p2}}}\times\frac{Z_{p5}}{R_p+Z_{p2}}\left(-\frac{\alpha_P}{(C_2+C_z)}\times\frac{gm_1(s)gm_2(s)}{(C_1+C_{z+})\times 1+gm_1(s)R_s+\frac{R_s}{Z_{p2}}}+\frac{q_{in}(t)}{(C_2+C_z)}\right)} \tag{B.145}$$

Equation (B.145) represents the expression for meminductance, where the "+" sign indicates expression for grounded incremental configuration and the "-“ sign indicates expression for grounded decremental configuration of meminductor emulator.

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Appendix C: 180 nm CMOS parameter file for Mentor Graphics Eldo

This section provides the full 180 nm CMOS process file used in the Mentor Graphics Eldo simulation tool. This file includes the necessary parameters to model the behavior of NMOS and PMOS transistors, as well as other circuit components, under the 180 nm technology node.

```
*--------------------------------------------------

* 180 nm CMOS Process Model for Eldo Simulation Tool

*--------------------------------------------------


* NMOS 180 nm Model
. MODEL NMOS_180NM NMOS (
   LEVEL = 53                    ;BSIM4 model level
   TOX = 2.5e-9                  ;Gate oxide thickness (m)
   VTH0 = 0.45                   ;Threshold voltage (V)
   U0 = 450                      ;Surface mobility (cm^2/V/s)
   LINT = 2.0e-8                 ;Effective channel length reduction (m)
   WINT = 2.0e-8                 ;Effective channel width reduction (m)
   K1 = 0.8                      ;Bulk threshold parameter
   K2 = 0.02                     ;Body effect coefficient
   NDEP = 2.2e17                 ;Channel doping concentration (cm^-3)
   NSUB = 5.0e17                 ;Substrate doping concentration (cm^-3)
   XT = 1.55e-7                  ;Cross-term coefficient (m)
   VBM = -3.0                    ;Maximum depletion width (V)
   ETA0 = 0.08                   ;Drain-induced barrier lowering coefficient
   DVT0 = 1.0                    ;First-order DIBL coefficient
   DVT1 = 0.2                    ;Second-order DIBL coefficient
   DVT2 = -0.1                   ;Body-bias coefficient
   MOBMOD = 1                    ;Mobility model selector
   CJ = 2.2e-4                   ;Zero-bias junction capacitance per unit area (F/m^2)
```

```
   MJ = 0.5                    ;Junction grading coefficient
   CJSW = 2.2e-10              ;Zero-bias sidewall junction capacitance (F/m)
   MJSW = 0.33                 ;Sidewall junction grading coefficient
   PB = 0.8                    ;Junction potential (V)
   CGSO = 2.2e-10              ;Gate-source overlap capacitance (F/m)
   CGDO = 2.2e-10               ;Gate-drain overlap capacitance (F/m)
   RSH = 7.5                    ;Source/drain sheet resistance (ohm/sq))

* PMOS 180 nm Model
. MODEL PMOS_180NM PMOS (
   LEVEL = 53          ;BSIM4 model level
   TOX = 2.5e-9        ;Gate oxide thickness (m)
   VTH0 = -0.5         ;Threshold voltage (V)
   U0 = 150            ;Surface mobility (cm^2/V/s)
   LINT = 2.0e-8       ;Effective channel length reduction (m)
   WINT = 2.0e-8       ;Effective channel width reduction (m)
   K1 = 0.8            ;Bulk threshold parameter
   K2 = 0.02           ;Body effect coefficient
   NDEP = 2.2e17       ;Channel doping concentration (cm^-3)
   NSUB = 5.0e17       ;Substrate doping concentration (cm^-3)
   XT = 1.55e-7        ;Cross-term coefficient (m)
   VBM = -3.0          ;Maximum depletion width (V)
   ETA0 = 0.08         ;Drain-induced barrier lowering coefficient
   DVT0 = 1.0          ;First-order DIBL coefficient
   DVT1 = 0.2          ;Second-order DIBL coefficient
   DVT2 = -0.1         ;Body-bias coefficient
   MOBMOD = 1          ;Mobility model selector
   CJ = 2.2e-4         ;Zero-bias junction capacitance per unit area (F/m^2)
   MJ = 0.5            Junction grading coefficient
   CJSW = 2.2e-10      ;Zero-bias sidewall junction capacitance (F/m)
```

```
    MJSW = 0.33             ;Sidewall junction grading coefficient
    PB = 0.8                ;Junction potential (V)
    CGSO = 2.2e-10          ;Gate-source overlap capacitance (F/m)
    CGDO = 2.2e-10          ;Gate-drain overlap capacitance (F/m)
    RSH = 7.5               ;Source/drain sheet resistance (ohm/sq))

* Parasitic Capacitances
. PARAM CGB0 = 1.0e-10          ;Gate-bulk capacitance (F)
. PARAM CJD = 1.0e-12           ;Junction depletion capacitance (F)
. PARAM CJS = 1.0e-12           ;Junction sidewall capacitance (F)

* Process Corner Definitions
. PARAM CORNER = 'TT'    ; Typical-Typical (TT) corner as default
. PARAM TT = 'TOX=2.5e-9 VTH0=0.45'
. PARAM FF = 'TOX=2.4e-9 VTH0=0.4'
. PARAM SS = 'TOX=2.6e-9 VTH0=0.5'

* Subthreshold Parameters
. PARAM NFACTOR = 2.0           ; Subthreshold slope factor
. PARAM VOFF = -0.1             ; Offset voltage (V)
. PARAM DSUB = 0.2              ; Subthreshold slope factor

* Noise Parameters
. PARAM NOIA = 1.0e-24          ; Flicker noise coefficient (A^2)
. PARAM NOIB = 1.0e-24          ; White noise coefficient (A^2)

* Temperature Coefficients
. PARAM TEMP = 25               ; Default simulation temperature (°C)
. PARAM TCVTH = -2.0e-3    ; Threshold voltage temperature coefficient (V/°C)
. PARAM TCU0 = -2.0e-4      ; Mobility temperature coefficient (1/°C)
```