DESIGN, ANALYSIS AND SIMULATION OF SINGLE AND MULTIFIN TRIGATE FinFET STRUCTURE AND CMOS IMPLEMENTATION OF FinFETs

Dissertation submitted in partial fulfillment of the requirements
for the award of the degree of

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In

VLSI Design

Submitted by

Shivam Shrivastava

Roll. No. 601261025

Under the supervision of

Mr. Arun Kumar Chatterjee

Assistant Professor, ECED

Department of Electronics & Communication Engineering

Thapar University, Patiala

INDIA

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CERTIFICATE

I hereby declare that the work which is being presented in the dissertation entitled, **"Design, Analysis and Simulation of Single and MultiFin TRIGATE FinFET Structure and CMOS implementation of FinFETs"** in partial fulfillment of the requirement for the award of degree of Master of Technology (VLSI Design) at the department of Electronics and Communication Engineering, Thapar University, Patiala, is an authentic record of my own work carried out under the supervision of Mr. Arun Kumar Chatterjee, Assistant Professor, ECED.

The matter presented in this dissertation has not been submitted in any other University/Institute for the award of any other degree.

Shivam

Date: 07/07/14

Shivam Shrivastava
Roll.No.601261025

It is certified that the above statement made by the student is correct to the best of my knowledge and belief.

Arun Kumar Chatterjee. 7/7/14

Mr. Arun Kumar Chatterjee
Assistant Professor
ECED,Thapar University

Counter signed by:

Dr. Sanjay Sharma
Professor & Head
ECED, Thapar University
Patiala-147004

Dr. S. K. Mahapatra
Dean of Academic Affairs
Thapar University
Patiala-147004

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This work is dedicated to my father ,mother and my uncle who shaped much of the way I think, instilled my confidence and technical desire, and unknowingly coined many of phrases by which I live my life.

ABSTRACT

According to Moore's law scaling of CMOS technologies beyond 22nm is limited by factors like excessive power consumption, process variation effects and other short channel effects(SCEs) like Drain Induce Barrier Lowering(DIBL), Gate Induce Drain Leakage(GIDL) and V_{th} roll off. Double Gate MOSFETs(DG MOSFET) are one of the solution to these SCEs but due to fabrication difficulties like misalignment of top and bottom gates etc. DG MOSFETs are replaced by FinFET. FinFET device have reduced SCEs due to their 3D structures like Double Gate FinFET(DG FinFET) and TG FinFET(TG FinFET). In this dissertation the current flow in DG MOSFETs, DG FinFETs and TG FinFETs has been analyzed.

For the simulation of modelled and designed structure Matlab R2007b and Cogenda Visual TCAD 1.8.0.2 tool has been used

The 3D effects due to active top gate in TG FinFET has also been analyzed and a depletion charge based current model considering 3D effects has been proposed. The agreement between the simulated and modeled results of current , supports the good accuracy of the proposed model. Further the most leaky path in subthreshold region and strong inversion region has been studied along with corner effects in TG FinFET and multi fin FinFET.

Analysis of the impact of silicon body thickness over short channel effects and the comparison of multi fins and single fin FinFETs has been done. Next a CMOS inverter has been designed by using single fin n-channel FinFET and Double fin p-channel FinFET. A ring oscillator has been designed using these CMOS inverter.

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ABBREVIATIONS

MOS	Metal Oxide Semiconductor
MOSFET	Metal Oxide Semiconductor Field Effect Transistor
SCE	Short Channel Effect
SS	Subthreshold Slope
SOI	Silicon On Insulator
FD SOI MOSFET	Fully Depleted Silicon On Insulator MOSFET
PD SOI MOSFET	Partially Depleted Silicon On Insulator MOSFET
AR	Aspect Ratio
DIBL	Drain Induced Barrier Lowering
GIDL	Gate Induce Drain Leakage
DG MOSFET	DG MOSFET
TG FinFET	Tri Gate FinFET
DG FinFET	DG FinFET

CHAPTER-1

INTRODUCTION

The journey of the modern MOSFETs has been started in 1959 when Dawon Kahng and Martin M. John invented the MOSFET at Bell Labs. Metal-Oxide-Semiconductor field-effect transistor(MOSFET) is a four terminal device i.e. source(S), gate(G), drain(D) and body(B) as shown in fig.1, it is used for amplifying or switching the electronic signals. MOSFET can be differentiated into two types n channel MOSFET in which channel contains electrons and p channel MOSFET containing holes in channel. MOSFET have two modes enhancement mode in which the conductivity increases by increasing the carriers in the channel and depletion mode in which conductivity decreases by decreasing carriers in channel when the gate voltage is applied. Commonly we uses n channel enhancement type MOSFET.

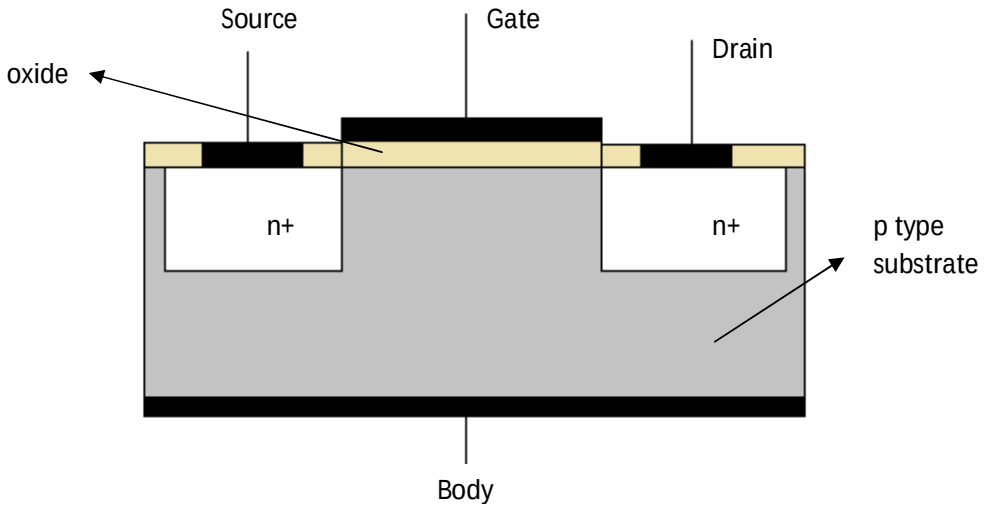


fig.1 Schematic view of MOSFET

1.1 MOORE's Law

According to the law the number of transistors in chips doubles in every 18 months[1].

Limits of Law

On 13 April 2005, Gordon Moore says that law can't be extended. He notice that the transistors miniaturisation limit reaches to the atomic levels. The basic barrier for the law is that the transistors size are approaching to the size of atoms.

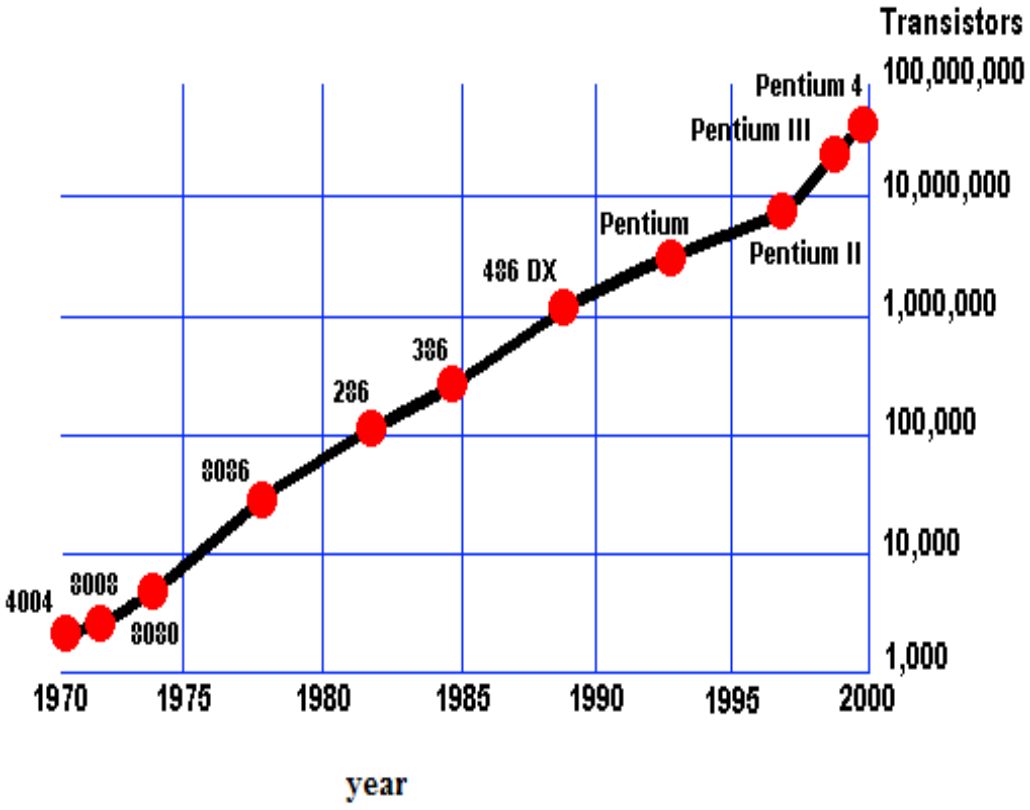


fig 1.1 Transistor count increase in microprocessors

1.2 Scaling of MOSFET

In order to decrease the power consumption, delay and to follow the Moore's law, scaling of the MOSFET is to be done. Scaling basically means the reduction of the dimensions of MOSFET's. There are three types of scaling strategies : *full scaling* (also known as constant field scaling) in which all dimensions are reduced by factor S but magnitude of the internal electric field is preserved and second is *constant voltage scaling* in which all dimensions are reduced by factor S but power supply and the terminal voltages are remain unchanged in this type of scaling[30] and third is *generalised scaling*.

1.3 Short Channel Effects

When the channel length is of the same order of depletion layer width of source and drain the MOSFET is said to be short. As the channel length becomes shorter and enters into the deep submicron regime, many effects came into light which are so called short channel effects[3][11][30] which are as follows

- **PN Junction Reverse Bias Current**

In MOSFET the drain and source to well junctions are reverse biased forming the pn junction diode due to which the leakage current flows. There are mainly two components of pn junction leakage : one is due to the presence of high electric field in the depletion region due to which electron hole pairs are generated; the second one is due to the drift/diffusion of minority carriers near the depletion region edge[3][11] .

- **Subthreshold Leakage**

In order to reduce the internal electric field and power consumption lower power supply is required, hence the lower threshold voltage is desirable. The current flows when gate voltage is below the threshold voltage is known as subthreshold or weak inversion current. The equation of subthreshold current is[3][11],

$$I_{ds} = \mu_o c_{ox} \left(\frac{W}{l}\right) * (m-1) * v_t^2 * \left[e^{\left(v_g - v_{th}/mv_t\right)}\right] * \left[1 - e^{(-v_{ds}/v_t)}\right]$$

where,

$m=1+C_{dm}/C_{ox}=1+3t_{ox}/\ w_{dm}$

V_{th} : threshold voltage

V_t : KT/q (thermal voltage)

C_{ox} : gate oxide capacitance

μ_0 : zero bias mobility

m : subthreshold swing

w_{dm} : maximum depletion layer width

- **Drain Induced Barrier Lowering (DIBL)**

When the drain voltage is increased the depletion region below the drain increases and starts contributing with the gate voltage to form the channel results in decrease of threshold voltage. DIBL is mainly due to the contribution of drain electric field over the channel. The effect of drain electric field is less is long channel devices but when the channel length becomes shorter the effect of the drain electric field increases lowering the barrier height, resulting in further decrease of threshold voltage. DIBL occurs at higher drain voltage and short channel lengths. DIBL can be reduced by higher channel doping and shallow source/drain junctions[3][11].

- **Punchthrough**

When drain voltage increases the depletion region below the drain and well junction also increases and at one drain voltage the source and drain depletion regions interacts and the current starts flowing and increases drastically with no potential barrier. The current is so high that it is impossible to turn off the device[3] . This is punchthrough and it is of two types

- Surface punchthrough : When the punchthrough occurs on the surface and current flows through surface is known as surface punchthrough.
- Bulk punchthrough : When non-uniform doping is done due to ion implantation the region under the surface is heavily doped in order to control the threshold voltage due to which the depletion region starts extending in the bulk and the punchtrough occurs in the bulk that is called bulk punchthrough.

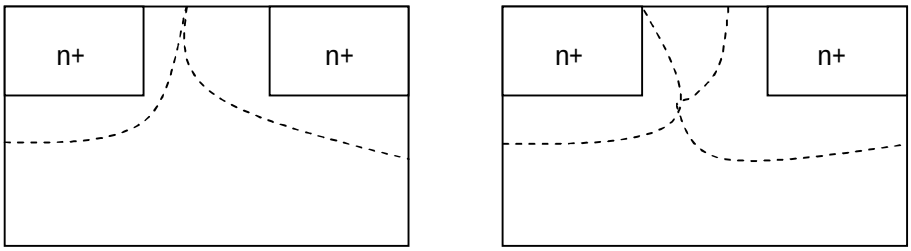


fig.1.3(a) surface and bulk punchthrough

- **Injection of Hot carriers from Substarte to Gate oxide**

The electrons or holes near the Si/SiO_2 interface gains sufficient energy due to the higher electric field and crossed the interface potential barrier and enters the oxide layer. This effect is known as hot carrier injection[3].

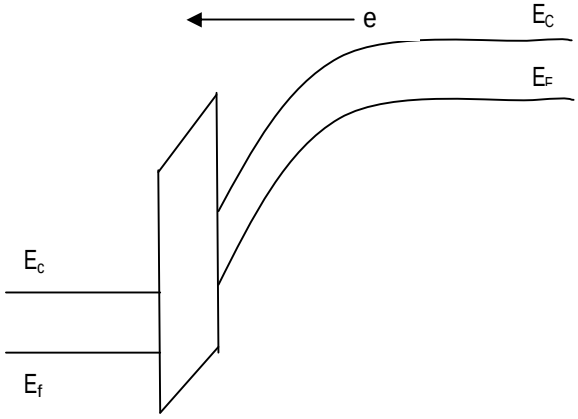


fig.1.3(b) injection of hot carrier from substrate to oxide

- **Tunnelling into Gate Oxide**

Due to scaling of the gate oxide thickness the electric field strength across the oxide, which results in tunnelling of electrons from substrate through gate oxide known as gate tunnelling current[3].

- **Gate Induced Drain Leakage (GIDL)**

When a negative bias is applied to the gate, there is accumulation of holes at the surface due to which the surface behaves like a p region more heavily doped than the substrate due to which the depletion layer here is much narrower and as a result the electric field increases. An even larger negative bias causes the n+ drain region under the gate to be depleted and even inverted due to which the electric field strength increases led to band to band tunnelling and electron hole pair generations . Hence the holes are swept to the lower potential and electron towards the positive potential as a result a leakage current flows and this effect is known as GIDL[3].

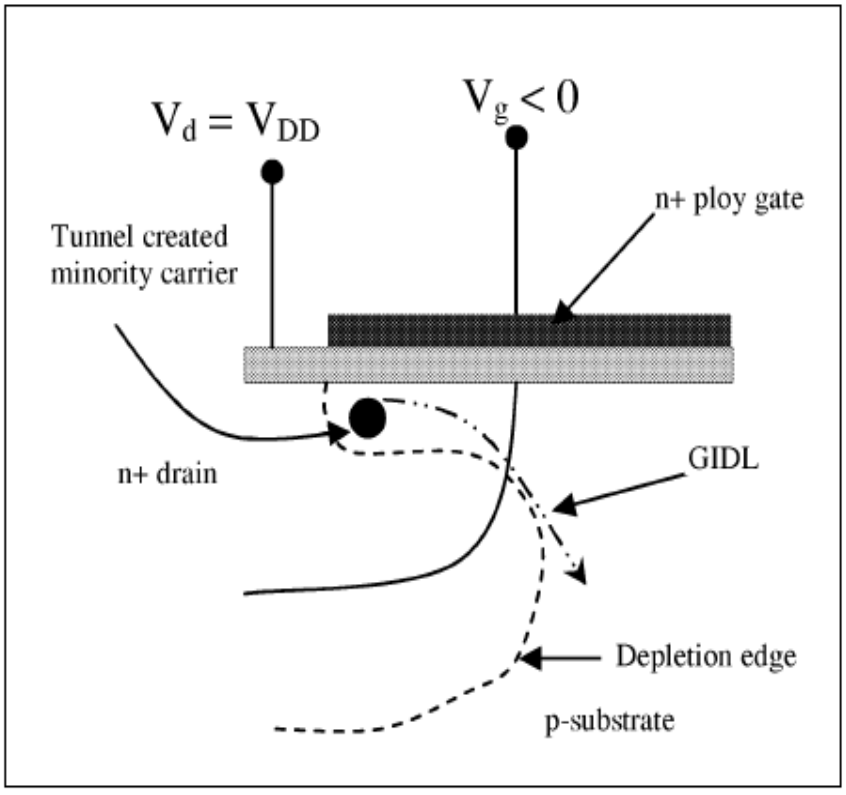


fig. 1.3(c) Gate Induced Drain Leakage

1.4 Advanced Nano Scale MOSFET

Due to scaling the contribution of drain electric field over the channel increases due to which many short channel effects came into light and due to limitation of miniaturisation new device structures came into picture[2].

- **Silicon on Insulators MOSFET's (SOI MOSFET's)[32],[5]**

In SOI MOSFET's a buried oxide is introduces as shown in fig.1.4(a)

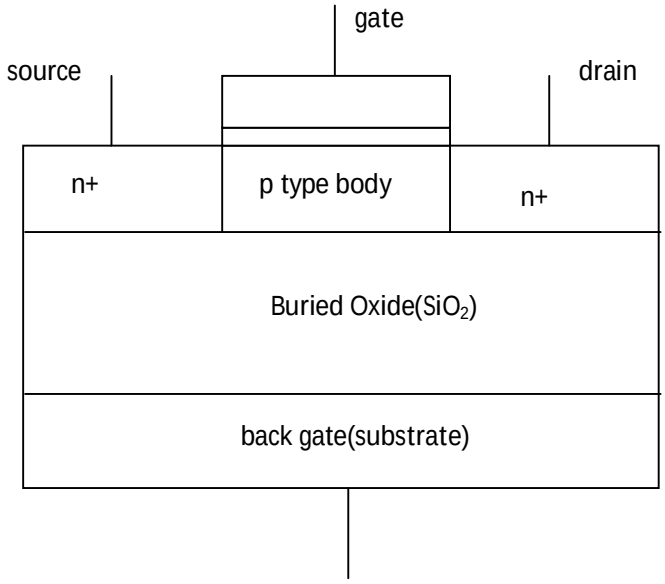


fig 1.4(a) Schematic view of SOI MOSFET

SOI MOSFET have smaller parasitic capacitances due to the introduction of buried oxide, smaller source/drain leakage as compare to bulk MOSFET.

SOI MOSFETs are of two types

- Partially Depleted SOI MOSFET(PD SOI MOSFET)

In this type of MOSFET the silicon film thickness is larger than the sum of width of depletion region from back to front end. Hence there is no interaction between source/drain and buried oxide due to which a neutral piece remains beneath the depletion region. If this piece will connected to the ground or body contact it will work as a bulk MOSFET. If this piece remains neutral or not connected to any contact than it becomes floating giving rise to Kink effect , degrading the characteristics of device.

➢ Fully Depleted SOI MOSFET(FD SOI MOSFET)

In this type of MOSFET the source/drain are buried oxide interacts and hence no neutral piece exists and hence kink effect is eliminated. This type of MOSFET is made by extremely thin SOI substrate.

- **Double Gate MOSFET's**

The concept of DGMOSFET came by the concept of back gate biasing in bulk MOSFET as the threshold voltage is controlled by back gate biasing. Basic structure of DGMOSFET is shown in fig.1.4(b) . It has two gates front and the back gate simultaneously controlling the charges at silicon and oxide interface and hence current. The advantages of DGMOSFET are less short channel effects i.e. DIBL ,better sub threshold slope, volume inversion , better gate control over the channel[7] .

There are mainly two types of DGMOSFET :

1) *a symmetric* type with both gates having same work function so that both surface channels turn on at same gate voltage.

2) *an asymmetric* type with different work functions for the gates and only one channel turns on at threshold voltage..

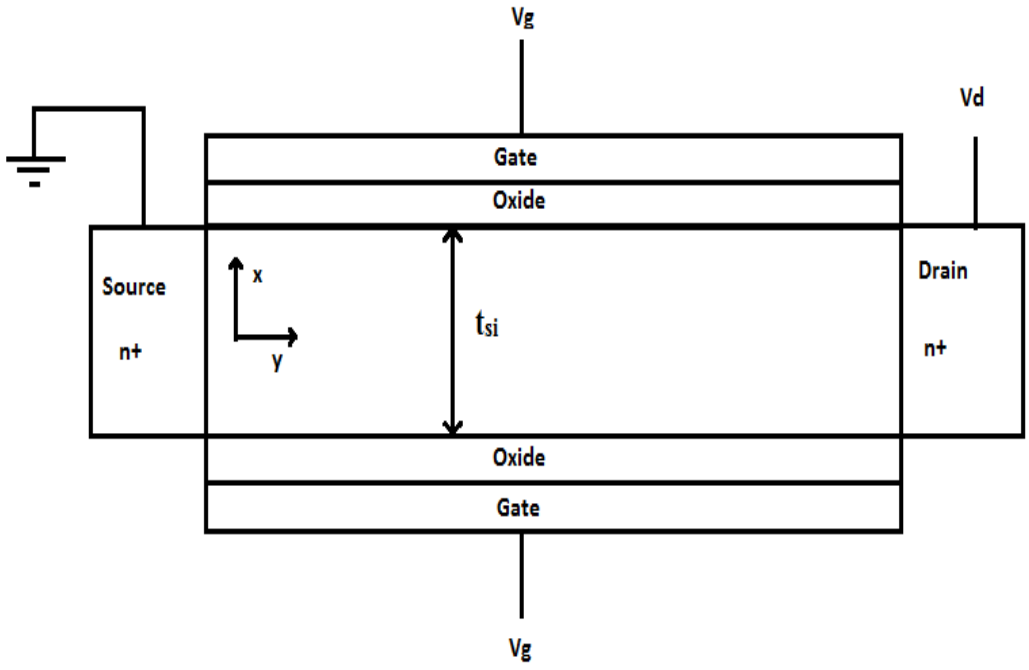


fig.1.4(b) Schematic view of Double gate MOSFET

- **FinFET**

The FinFET is a non-planar, double-gate transistor which is built on an SOI substrate. The main distinguishing characteristic of the FinFET is that the conducting channel is wrapped by a thin silicon "fin", which forms the body of the device[11][13]. The effective channel length of the device is determined by the thickness of the fin (measured in the direction from source to drain).

1.5 Literature Survey

Kaushik Roy et al. ,2003 [3]

The continuous scaling of channel length, gate oxide thickness, and threshold voltage in the deep-submicrometer regime leads to high leakage current which is becoming a serious concern because of the high power dissipation it leads to. Consequently, it is necessary to identify different leakage components and to carefully model them so as to reduce the leakage power. This paper reviews the different transistor intrinsic leakage mechanisms, including sub-threshold leakage, drain-induced barrier lowering, punchthrough, gate-induced drain leakage, hot carrier injection into the oxide, and gate oxide tunnelling. The paper also discusses channel engineering techniques including halo doping and retrograde doping as a means to ameliorate short-channel effects for continuous scaling down of CMOS devices. Finally, the paper explains various circuit-level techniques to reduce leakage power.

Vishwas Jaju ,2004[5]

This paper explains the issues related to silicon-on-insulator technology. SOI technology gives a good alternative to bulk CMOS processes which are reaching their limits in terms of device miniaturization and fabrication. Firstly, the paper discusses the various SOI wafer fabrication techniques including hetro-epitaxy, homo-epitaxy, recrystallization, SIMOX, wafer boding and unibonding. SIMOX and UNIBOND techniques are viewed as future industrially scaled processes. Next, the paper presents the different types of SOI MOSFETs and evaluates the related physical concepts. Finally, the properties of double gate MOSFET's and its pros and cons over bulk CMOS technology are explained. This paper successfully discusses advantages of SOI MOSFETs with the stress on Double Gate MOSFETs. The technological challenges in realizing this new device structure are also presented in this paper. Double Gate MOSFETs provide excellent short channel effect immunity and exhibit a near ideal sub-threshold slope which make them the ultimate scalable device structure.

Anurag Chaudhry , M.Jagadesh Kumar ,2004[4]

This paper examines the degradation in performance of a MOS device fabricated on a silicon-on-insulator (SOI) wafer due to the undesirable short-channel effects (SCE) such as Drain Induced Barrier Lowering , short channel effects arising due to back-gate biasing dependence

,short channel effects arising due to structural dependence on thin-film thickness, thin film doping density ,thickness of buried oxide, as the channel length is scaled down. This paper presents different structures such as Thin Body FD SOI with raised source and drain, Halo Doped SOI MOSFET ,Ground Plane FDSOI MOSFET, MULTIPLE GATE SOI MOSFET to circumvent the SCE in SOI MOSFETs and also discusses the strengths and weaknesses specific to each attempt.

Ran-Hong Yan, Abbas Ourmazd and Kwing F. Lee, 1992[6]

This paper shows the scaling theory of Si MOSFET from bulk to SOI devices and explores the effect of horizontal electric field and vertical electric field due to scaling of bulk MOSFET. It shows the concept of natural length and its extraction through the use of vertical and horizontal potential. At last it derives the minimum potential in the channel and gives its relation with natural length and tells that minimum potential of channel should be less and for this the natural length should be less.

Kunihiro Suzuki et al. , 1993[7]

This paper shows the advantage of double gate MOSFET over bulk MOSFET and establishes the scaling theory for double gate MOSFET relevant to natural length, giving guidance to extract the parameters like oxide thickness , silicon thickness to get ideal characteristics of device.

Yaun Taur et al. , 2004[8]

In this letter a continuous current-voltage model has been derived through the use of poisson's equation for long channel DG MOSFET. All regions of device operation i.e. linear, subthreshold and saturation region has been covered in this letter and current-voltage model has been derived for all regions. In this letter poisson's equation is solved in term of potential in the channel.

Jin He et al. , 2004[10]

In this paper a non charge sheet based analytical model has been derived for undoped double gate MOSFET in terms of electron concentration. The difference of this model with other models derived until that time is that in this paper the poisson's equation is solved in term electron concentration rather than the surface potential. In this paper the electron and

potential distribution, surface potential and inversion charge carriers, effect of volume inversion on characteristics of double gate MOSFET has also shown.

Marc Swinnen, Ron Duncan, 2012[11]

In this paper the effect of scaling on bulk MOSFET and the various short channel effetcs like drain induced barrier lowering, threshold voltage roll off, charge mobility degradation and variations of threshold voltage has been explained. Alternative transistors design like FinFET ,its structural parameter ,its working, its fabrication steps and comparision of FinFET with fully depleted MOSFET has been shown. At last strengths and weakness of FinFET and fully depleted SOI MOSFET has been shown.

Digh Hisamoto et al. , 2000[13]

In this paper a novel self aligned double gate FinFET has been proposed and its effect over short channel effects has been shown. Fabrication process flow of FinFET has been explained and shows that the resultant device is quasiplanar. Main features of FinFET that is shown in this paper is that this device can suppress short channel effects upto 17nm channel length, alignment problem of gates in double gate MOSFET is eliminated in FinFET .

A. Kaneko et al. , 2005[15]

The fabrication process flow of FinFET using new improved sidewall trnasfer process and selective gate sidewall spacer formation technology for sub-15 nm FinFET with elevated source/drain extension has been explained in this paper. The resistance of source/drain has been reduced through this process flow is also shown.

Jakub Kedzierski et al. , 2003[16]

Challenges in the fabrication process of FinFET such as parasitic series resistance and how this resistance can be reduced during the fabrication time has been explained. The series resistance can be minimised by using angled implants so that the irregularity of dopants doped during diffusion process can be minimised and can be diffused deeply. Due to the less fin thickness the resistance increases hence by increasing the fin thickness outside the gate region called raised source/drain the resistance can be decreased. By using the silicide contacts resistance also decreased. Hence the FinFET with angled implants, raised source/drain and silicide contacts parasitic series resistance can be reduced.

Yongxun Liu et al. , 2003[18]

This paper shows the influence of crystal orientation of soi wafer and fin of FinFET over the characteristics of device. In this paper to make the silicon fin smooth <111> crystal oriented fin has been growth over the <110> oriented silicon wafer due to which higher drive current and excellent subthreshold characteristics are demonstrated.

Yaun Taur, Jooyoung Song, Bo Yu, 2008[20]

This paper shows the compact model of different multigate MOSFETs. Firstly, a core model based on analytical potential solutions for symmetric DGMOSFET and surrounding gate MOSFET has been derived and with addition of short channel effects, capacitance the derived core model is extended to other multigate MOSFET i.e. trigate MOSFET, Quadruple gate MOSFET, pi gate MOSFET.

F.Dauge et al. , 2004[19]

The coupling effects between front and back gate in the trigate FinFET has been shown in this paper. Transport properties has also experimentally studied. Impact of fin thickness on device characteristics of short channel with coupling effect has been emphasized. In this paper it has shown that the mobility of channel is higher in front and back gate as compare to lateral channel mobility due to difference in crystal orientation and degradation of sidewalls .

Alexander Kloes, Michaela Weidemann, Mike Schwarz, 2009[21]

This paper describes the operation of FinFET and shows the flow of drain current with 3D effect. The most leaky path in subthreshold region which is at bottom corner and most leaky path at strong inversion which is at corners of FinFET has been shown through experimentally. Analytical model in undoped FinFET for threshold conditions and subthreshold slope at different positions in the channel has been derived. A model for current equation constituting the 3D effects has been derived in this paper.

N.Fasarakis et al. , 2011[23]

In this paper an analytical model for threshold voltage for double gate FinFET has been derived and this model has been extended to trigate FinFET using the electrostatic behaviour of top gate.

Nikolaos Fasarakis et al. , 2012[27]

An analytical current model for lightly doped trigate FinFET has been derived. The quantum mechanical effect and the short channel effects such as velocity saturation and channel length modulation has been considered to derive the current model and then this model has been compared with experimental results.

CHAPTER-2

BASIC CONCEPTS

2.1 FinFET

In order to reduce the short channel effects in bulk MOSFET and SOI MOSFETs[3][4], DGMOSFET has been introduced. Though DGMOSFET suppress many of the short channel effects, but the difficulty in fabrication of DGMOSFET has been encountered due to the misalignment of top gate and the back gate[7]. Hence to overcome the shortcomings of DGMOSFET the FinFET architecture is introduced[11][13].

In the FinFET the conducting channel is raised up into a 'fin' with the gate wrapped around it in a 3dimensional structure as shown in fig.2.1(a), H_{fin} the height of fin , L_g is the gate length and W_{fin} is width of the fin . The fundamental advantage of a FinFET is that no part of the channel is not too far from the influence of the gate hence the controllability of gate over channel increases and the device can be switch on-off quickly[11][13].

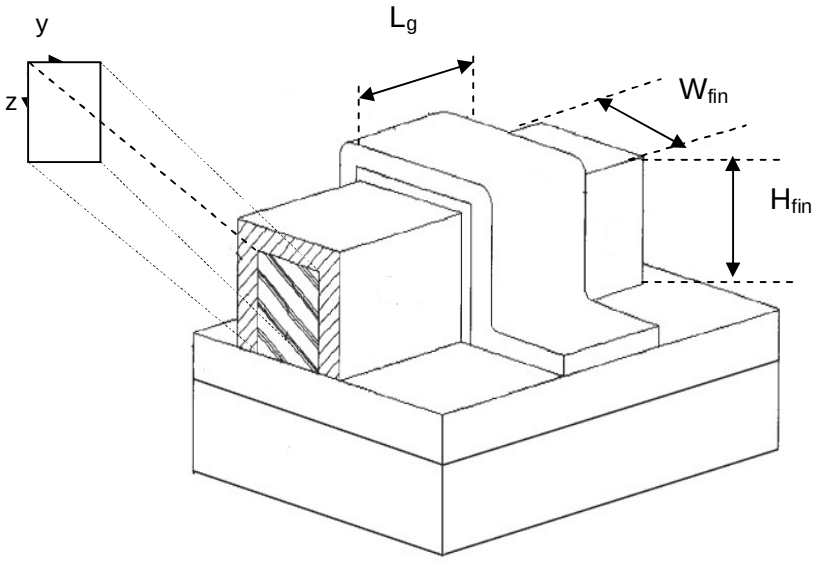


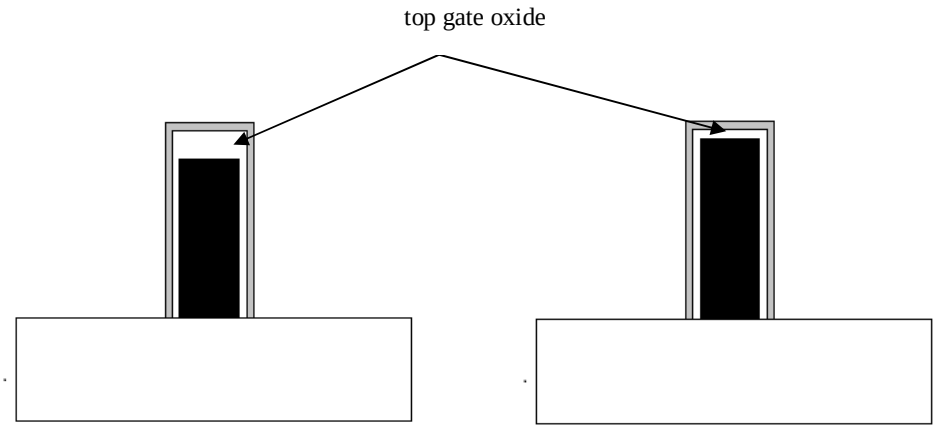
fig.2.1(a) Schematic view of FinFET

There are two types of FinFET

a) DGFinFET (Double gate FinFET)

b) TGFinFET (Tri gate FinFET)

The difference between the DGFinFET and the TGFinFET is thickness of the oxide at the top gate . In the DGFinFET the gate oxide thickness of top gate and the side gates are different as shown in fig 2.2(b)a ,



(a) (b)

fig.2.2(b) side view of DGFinFET (a) and TGFinFET (b)

thickness of the top gate is more enough so that the top gate will become electrically isolated and the gate oxide thickness of side gates are equal therefore only two gate (side gates) contributes in forming channel . Hence the effective conduction width of DGFinFET is [33]

$W_{effdg} = 2 \times n \times H_{fin}$

while in TGFinFET the gate oxide thickness of side gates and top gate are equal and all three gates contributes in forming channel as shown in fig1.4(d)b , hence the drive current is more in TGFinFET as compare to DGFinFET Thus the effective width of TGFinFET is [33]

$W_{efftg} = n \times (2 \times H_{fin} + W_{fin})$

n is number of fins, and n=1 for single fin FinFET , the main drawback of single fin FinFET is lower drive current as compare to other architecture due to thinner fins and if the thickness of fins are increased than the SCE increases ,hence multi fins are introduced by increasing the number of fins on the same substrate as shown in fig 2.2(c) ,hence the effective width increases without increasing the width of single fin and thus the drive current increases.

The fin pitch (P_{fin}) is also the the essential figure of merit.The P_{fin} is the sum of of spacing between two fins with width of the single fin (W_{fin}).

Acoording to [33]

$P_{fin} < 2 \times H_{fin}$

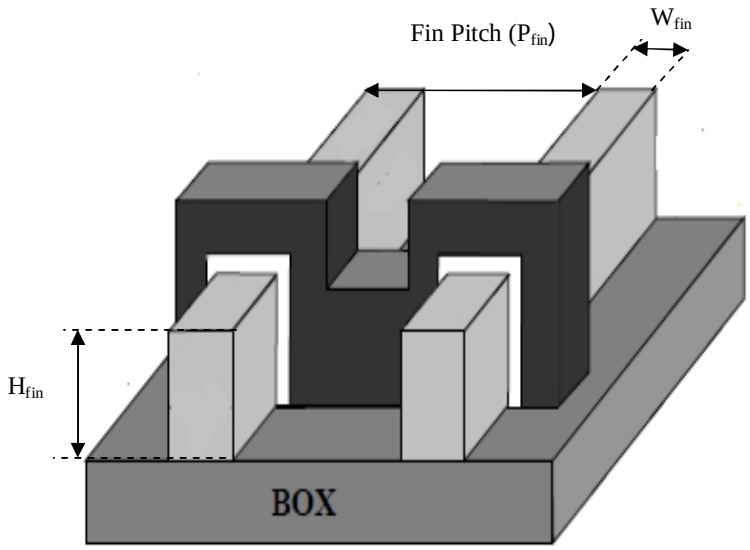


fig.2.2(c) Schematic view of multifin FinFET

2.2 Fabrication of FinFET

There are different methods or process flow for fabricating the FinFET. Here one of them has been shown[14][15][16].

- Substractive method

Step 1 : Grow silicon nitride as capping layer of silicon layer and then a hardmask which is of amorphous silicon.

Step 2 : Now photoresist material and then spacers are grown.

Step 3: Then the photoresist material is removed and the device remained with nitride as spacers.

Step 4 : Now the nitride is etched so that the hardmask remains which protects the silicon below it.

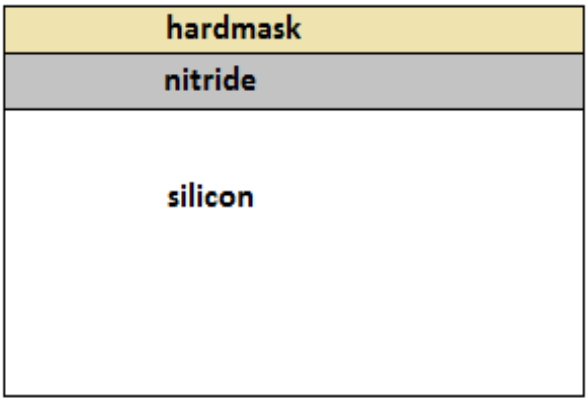
Step 5 : Now etching has been done so that area below hardmask remains uneched and this step forms the fin.

Step 6 : Remaining hardmask is then echted and now fin and nitride remains. (This step defines whether the fabricate device is double gate or trigate FinFET , if the nitride remains at the top the top gate can't be access at DGFinFET is fabricated and if nitride is etched than the top gate can be accessed and trigate FinFET has been fabricated)

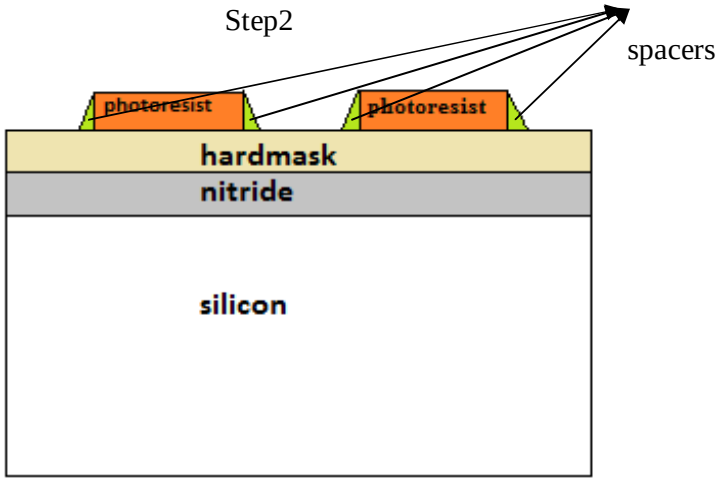
Step 7 : Then trenching (gap between fins) has been filled with oxide and then top portion is planarised.

Step 8 : Then oxide is etched according to the height of fin (hence this step defines the height of fin).

Step 1



Step2



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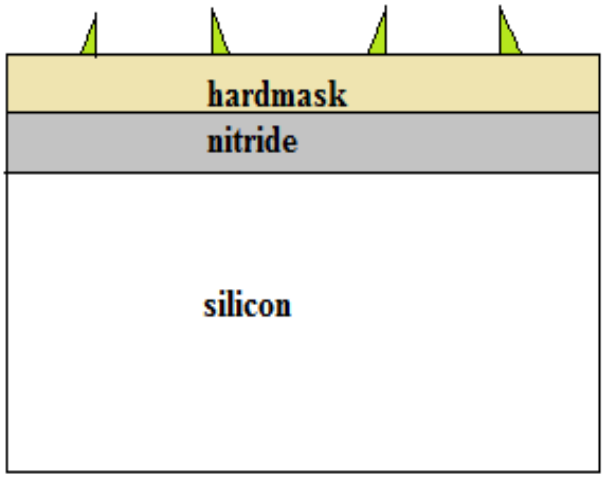
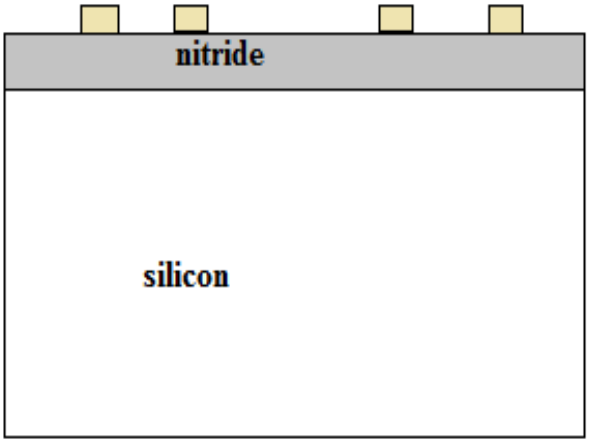
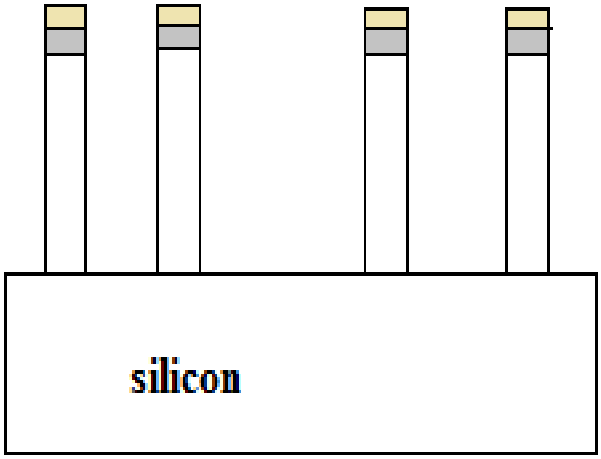


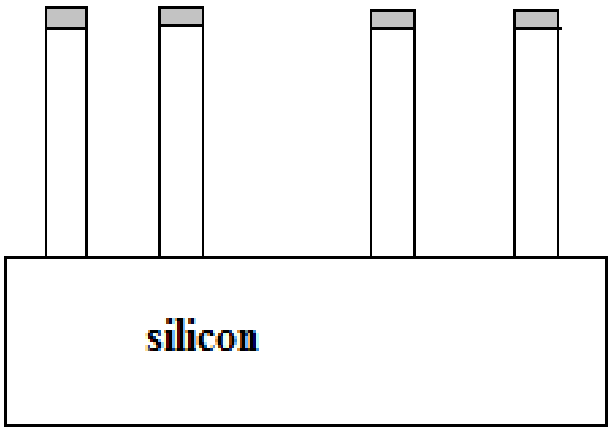
Step 4



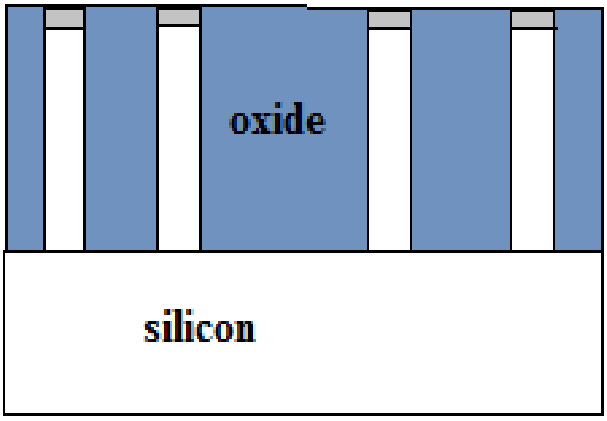
Step 5



Step 6



Step 7



Step 8

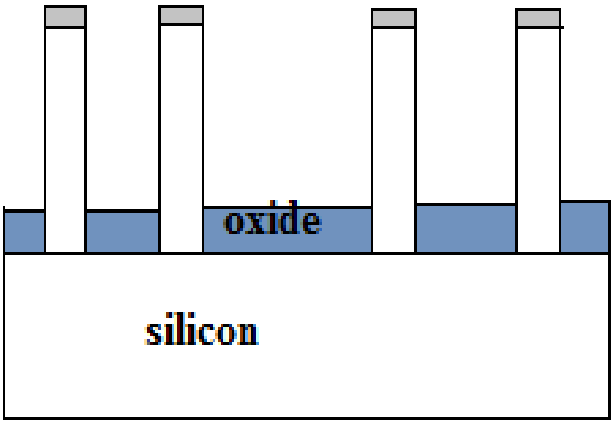


fig 2.3 fabrication steps of FinFET

CHAPTER 3

ANALYSIS OF CURRENT FLOW AND CURRENT MODEL FOR TRIGATE FinFET

In TGFinFET, in weak inversion the most leaky path exists in the bottom centre of the channel[21][22] because for lower gate voltage the effect of the gate decreases as one goes away from the gate. gate covers channel through three sides, thus the most leaky path exists at bottom centre which is far from all three gates and the effect of drain potential is higher at that point as shown in fig3.1 and fig.3.2 due to which the channel first forms at bottom centre of the channel. Fig 3.1 shows that potential increases along the width of fin and maximizes at bottom and fig.3.2 shows that potential increases along the fin height and maximizes at bottom, hence from both graphs it is clear that the most leaky path exists at bottom centre of the fin. By increasing the gate voltage the channel starts moving from bottom centre to silicon-oxide interface. In TGFinFET when height of the fin is greater than width of fin each half of the top gate width contributes to channel formation with the side gates. Thus the effective width becomes $W_{eff} = H_{fin} + W_{fin}/2$ [23].

The overall current of TGFinFET with channel length modulation given in[23] is

$$I_d = \mu_0 2W_{eff}\frac{\varepsilon_{ox}}{t_{ox}}(2V_{th})^2\left[\frac{(q_{is}-q_{id})}{L}+\frac{1}{2}\frac{({q_{is}}^2-{q_{id}}^2)}{L-\Delta L}\right] \quad (1)$$

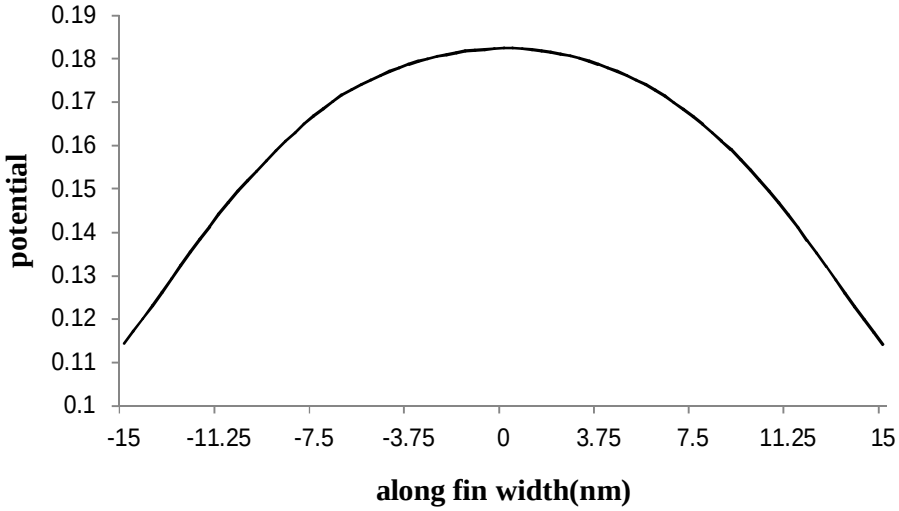


fig.3.1 potential graph at weak inversion along the fin width (y direction) showing that the maximum potential at the middle of the fin

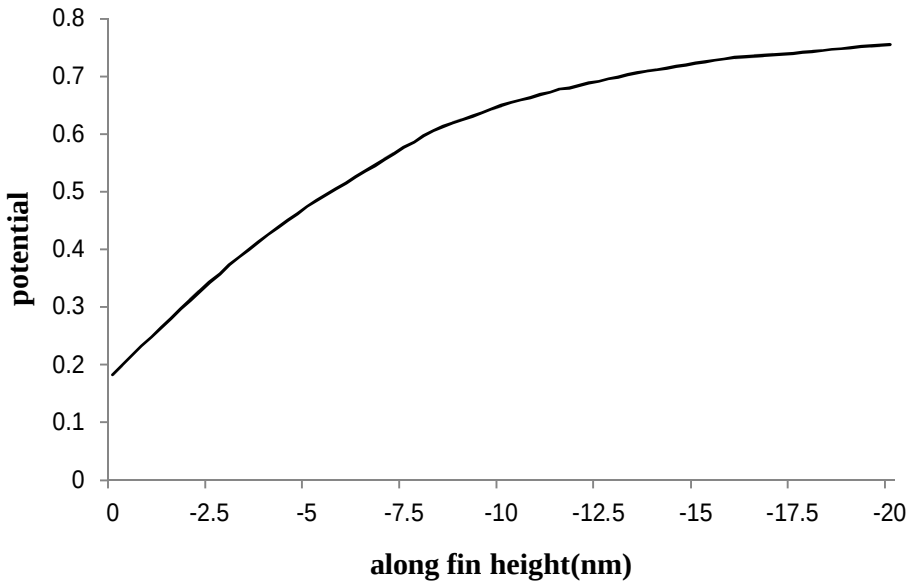


fig.3.2 potential graph at weak inversion along the fin height (z direction) showing that the maximum potential at the bottom of the fin

Here ΔL is gap between L and channel pinchoff, μ_0 is the low field electron mobility, ε_{ox} is permitivity of oxide and t_{ox} is thickness of oxide, q_{is} and q_{id} are normalized inversion sheet charge density which is given as

$$q_{ix} = Lambert\ W\left(e^{\frac{(V_g - V_t - V_x)}{2V_{th}}} \frac{e^{\frac{(V_g - V_t - V_x)}{2\eta'_{TG} V_{th}}}}{A + e^{\frac{(V_g - V_t - V_x)}{2\eta'_{TG} V_{th}}}} \right) \quad (2)$$

A is given as :

$$A = 4e^{\frac{V_t + V_{fb}}{Vo}} \quad (3)$$

where V_o is 1v, V_x is the channel voltage at source it is 0 and at drain it is V_d ,V_{th} is thermal voltage which is KT/q ,V_t is threshold voltage $\eta'_{TG} = \eta_{TG}/(\eta_{TG}-1)$ is the subthreshold switch coefficient , given in [27]. The threshold voltage given in [23] is

$$V_t = V_{fb} - \frac{A_{1,TG}(V_{bi}+V_d)+A_{2,TG}V_{bi}}{1-(A_{1,TG}-A_{2,TG})} + \frac{V_{th}}{1-(A_{1,TG}-A_{2,TG})} \ln\left(\frac{Q_{th}N_a}{n_i{}^2 W_{fin}}\right) \quad (4)$$

where $V_{fb} = \Phi_{ms} - V_{th} \ln(N_a/n_i)$ is flat band voltage, Φ_{ms} is the work function difference between metal and silicon, V_{bi} is built in potential given as $V_{bi} = V_{th} \times \ln(N_d/n_i)$. In this model

the effect of depletion charges has been neglected. If the substrate is highly doped than the effect of depletion charges came into effect which affects the built in potential as well as threshold voltage ,thus these has to be modified .

The modified V_t and V_{bi} are :

$$V_t = V_{fb} - \frac{A_{1,TG}(V_{bi}+V_d)+A_{2,TG}V_{bi}}{1-(A_{1,TG}-A_{2,TG})} + \frac{V_{th}}{1-(A_{1,TG}-A_{2,TG})} + Q_d \quad (5)$$

$$V_{bi} = V_{th} \ln\left[\frac{N_a N_d}{{n_i}^2}\right] \quad (6)$$

N_a and N_d are acceptor and donor charge densities and n_i is intrinsic silicon charge concentration, Q_d is the depletion charges given as:

$$Q_d = .5 \times qN_aW_{fin} \quad (7)$$

$A_{1,TG}$, $A_{2,TG}$ are the parameters which are the functions of natural length and channel length given in [24] and it has finite values for short channel devices but for long channel devices values there values are 0.

Therefore threshold voltage for long channel devices is

$$V_{tlong} = V_{fb} + V_{th} \ln\left(\frac{Q_{th}N_a}{{n_i}^2 W_{fin}}\right) + Q_d \quad (8)$$

Q_{th} is the minimum sheet charge density, required to achieve turn on of strong inversion is given as:

$$Q_{th} = \frac{2V_{th}}{q} \times \frac{{C^2}_{ox}}{C_{si}} \quad (9)$$

where C_{ox} and C_{si} is capacitance of oxide and silicon respectively which is given as:

$$C_{ox} = \varepsilon_{ox}/t_{ox} \text{ and } C_{si} = \varepsilon_{si}/W_{fin} \quad (10)$$

In the above model of current the switching parameter should be use to get the correct graph when the device is switching from strong to weak inversion .The switching parameter given in [24] for DGMOSFET is modified and given as :

$$iss_{tg} = c1 \times \tanh\left(c2 \times (V_g + \Delta V_t - V_t)\right) \quad (11)$$

c1 and c2 are the fitting parameters,

$$\Delta V_t = V_t - V_{tlong} \quad (12)$$

Hence the new drain current equation proposed is :

$$I_d = \mu_0 2W_{eff} \frac{\varepsilon_{ox}}{t_{ox}} (2V_{th})^2 \left[\frac{(q_{is} - q_{id})}{L} + \frac{1}{2} \frac{(issTG)({q_{is}}^2 - {q_{id}}^2)}{L - \Delta L} \right] \quad (13)$$

The comparison of new drain current equation given in (12) and the simulation results is shown in fig.3.3. From the simulation c1 and c2 is found .01 and .5 and Q_{th} should be in order of 10^{17} .Here the mid gap metal gate is used.

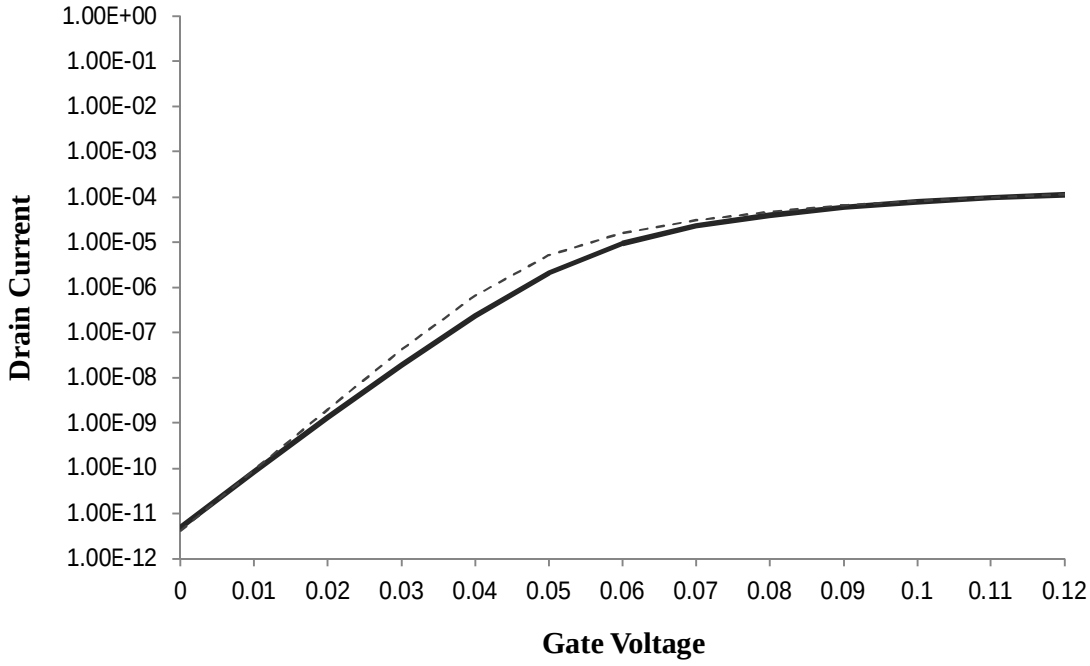


fig.3.3 drain current versus gate voltage at V_d=.6,t_{ox}=2nm dash line representing simulation results and solid line represents model result.

In order to increase the drive current multifin FinFET is used. The current equation given in (13) can be extended to multifin FinFET by changing $W_{eff} = n(H_{fin} + W_{fin}/2)$. The simulation results for the multifin FinFET with current model is shown in fig.3.4 , two fins are used for simulation and hence n=2.

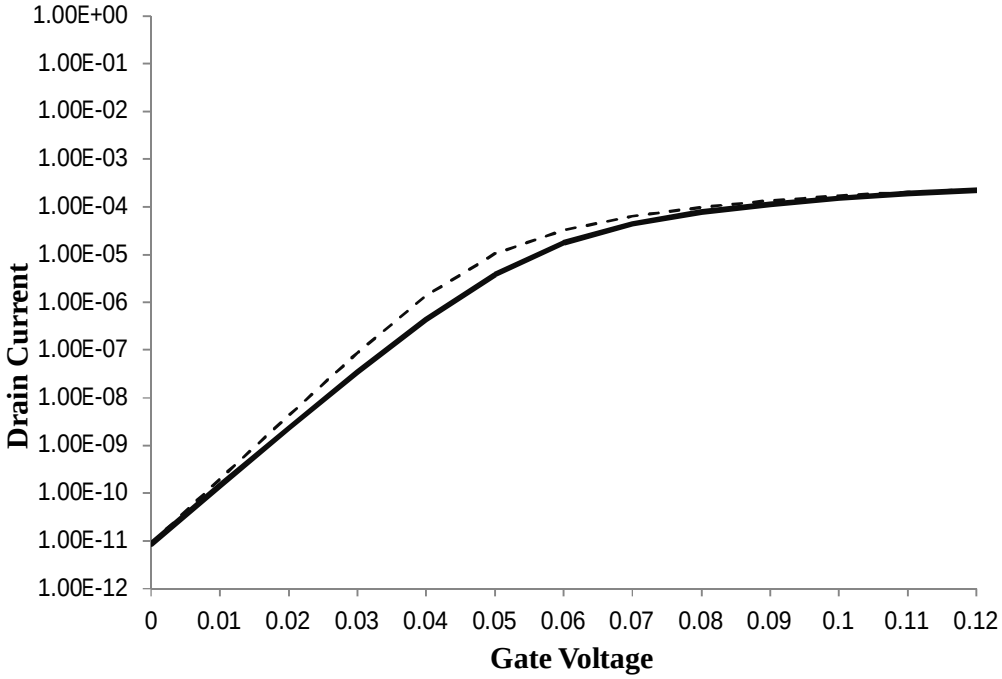


fig.3.4 drain current versus gate voltage of double fin FinFET at V_d=.6,t_{ox}=2nm dash line representing simulation results and solid represents model result.

CHAPTER 4

RESULTS AND DISCUSSION

4.1 Double Gate MOSFET

- **Impact of silicon thickness**

As the dimensions of device are scaled down the oxide thickness is also been scaled but due to scaling of oxide tunneling current increases and hence a concept of natural length (λ) evolved which represents the distance of penetration of drain electric field in the channel t_{ox}[6][7],

$$\lambda = \sqrt{\frac{\epsilon_{si} t_{si} t_{ox}}{2\epsilon_{ox}}}$$

λ is proportional to square root of product of device body thickness and gate oxide thickness , therefore by decreasing the substrate thickness we can decrease the short channel effects[32] . The comparision of results is shown below at two different t_{si} in table 4.1(a) and graphs in fig 4.1(a)

Parameters	**t_{si} at 20nm**	**t_{si} at 10nm**
I_{on}	3 mA	2.9 mA
I_{off}	3.9×10^{-11} A	2.8×10^{-12} A
V_t	.2 V	.27 V
DIBL	.15	.1

table 4.1(a) comparision of results at two different silicon thickness

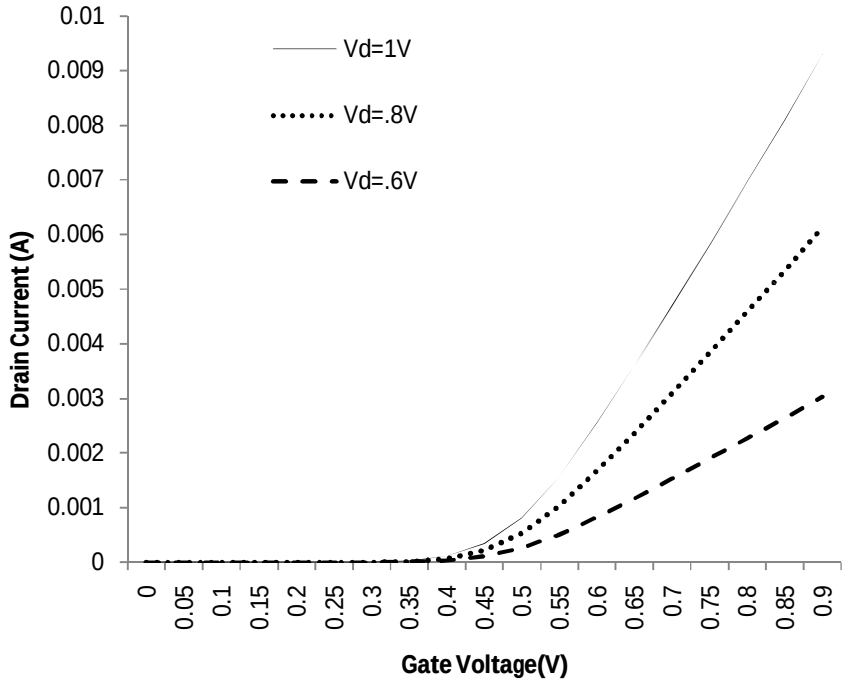


fig. 4.1(a) Linear graph of gate voltage versus drain current at different drain voltage at t_{si} = 20nm

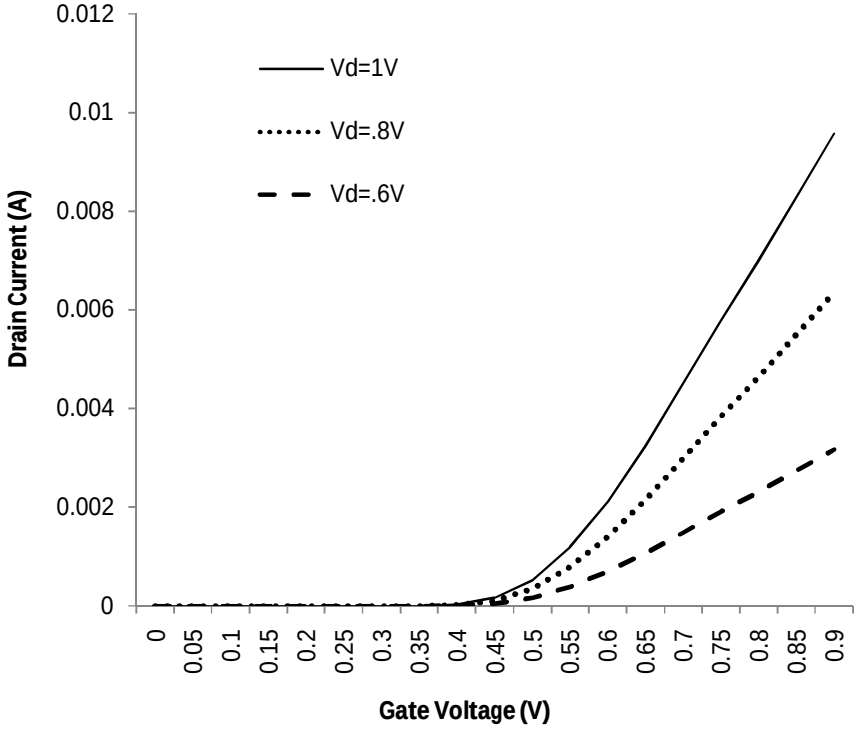


fig. 4.1(b) Linear graph of gate voltage versus drain current at different drain voltage at t_{si} = 10nm

From the above graphs it is clear that by decreasing the thickness of silicon substrate sub threshold current decreases , drain induced barrier lowering decreases and on current does not decreases as off current decreases , therefore I_{on}/ I_{off} ratio increases.

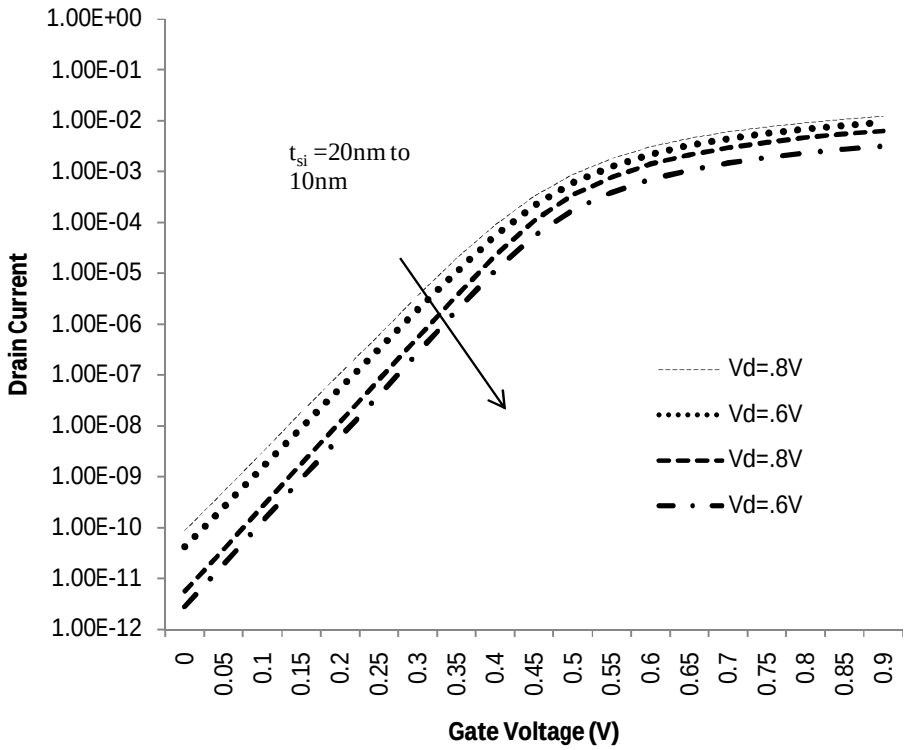


fig. 4.1(c) Log graph of gate voltage versus drain current at different drain voltage at t_{si} = 20nm and 10nm .

- **Potential with respect to substrate thickness**

Taking the top silicon-silicon oxide interface as reference zero point and going towards back gate the distribution of potential at different gate voltage and different substrate thickness is shown in fig. 4.1(d) From the graph , when the substrate thickness is more here it is 20nm than the potential is almost constant at low gate voltage[8][9][10]. Therefore potential at silicon-oxide interface is same as at the middle of substrate ,but as we increases the gate voltage the potential at the interface increases and potential at the middle of the substrate goes on decreasing and the difference between surface potential and the potential at the middle of the substrate increases more , but when the substrate thickness is less here it is 10nm ,at lower gate voltage the potential is distributed all over the substrate and as we increase the gate voltage the potential difference is created between the potential at interface

and the potential at the middle of the substrate , but this potential difference is very less as compare to the potential difference created between surface potential and at the middle of substrate in higher thickness substrate .

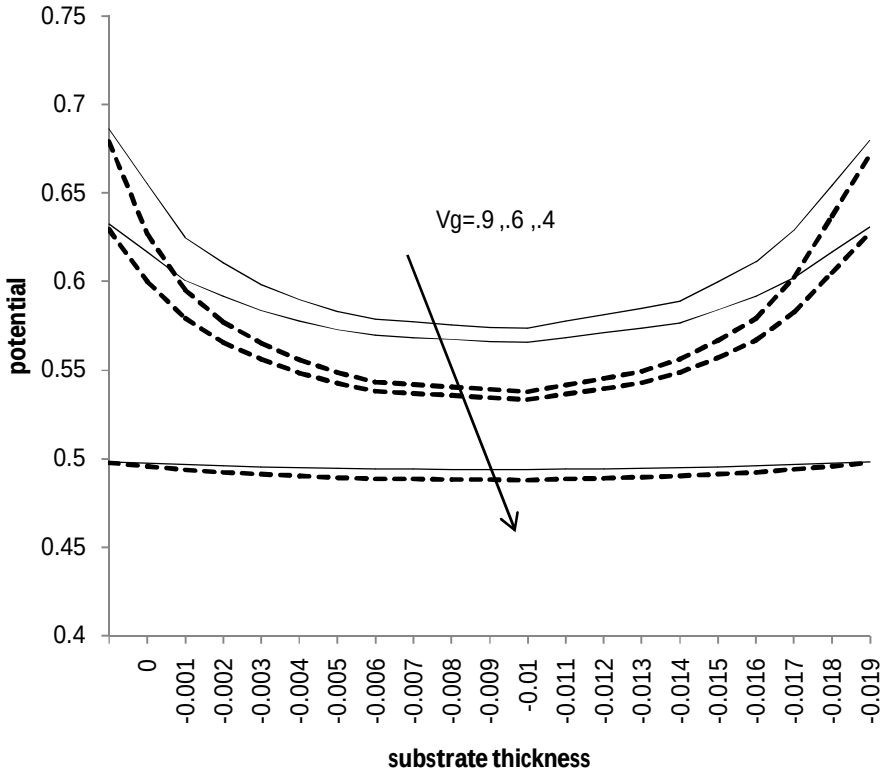


fig.4.1(d) Potential graph versus substrate thickness at different gate voltage dash line showing graph at t_{si}=20nm and solid line showing graph at t_{si} =10nm

- **Volume Inversion**

From the fig 4.1(d) it is clear that at lower gate voltage the potential is distributed throughout the substrate and the electron are also distributed uniformly throughout the substrate and hence the volume inversion occurs and the difference in potential and electron distribution at interface and mid of the substrate increases as we increase the gate voltage and this difference is more in the substrate having more thickness [10]. Hence the volume inversion is more in the substrate having less thickness and contributes in giving high current because here whole substrate is contributing in the current. Electron distribution with respect to thickness of substrate is shown in fig 4.1(e)

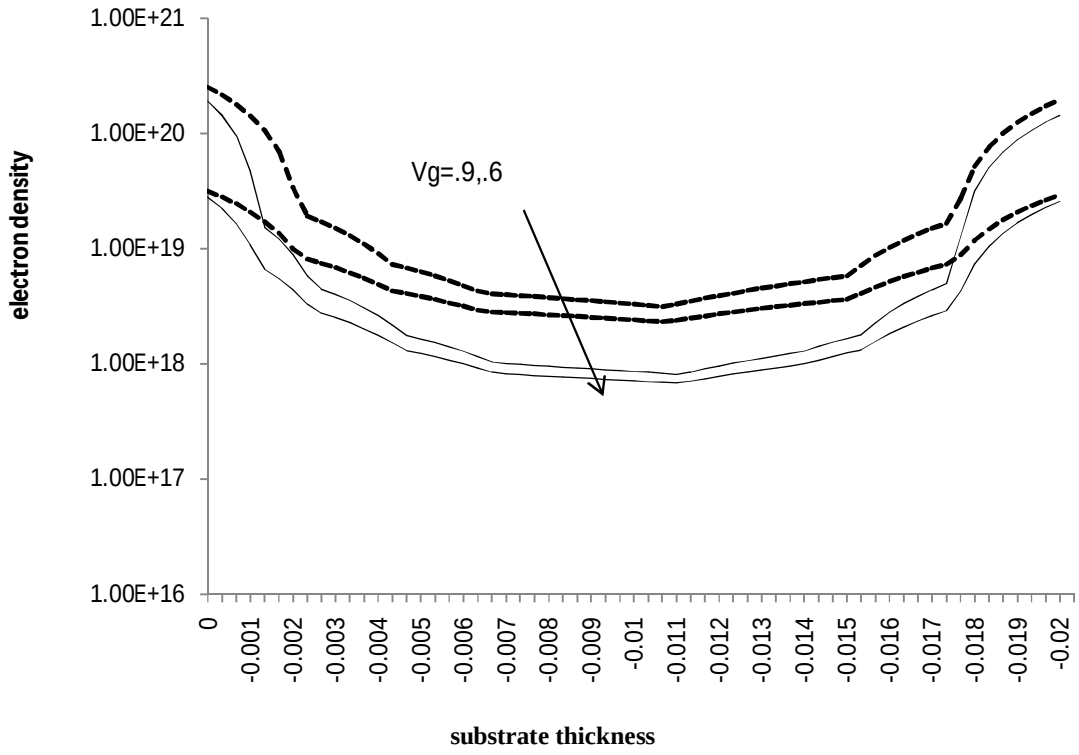


fig.4.1(e) electron density graph versus substrate thickness at different gate voltage dash line showing graph at t_{si}=20nm and solid line showing graph at t_{si} =10nm

4.2 FinFET

4.2.1 Single fin FinFET

- **Layout of FinFET**

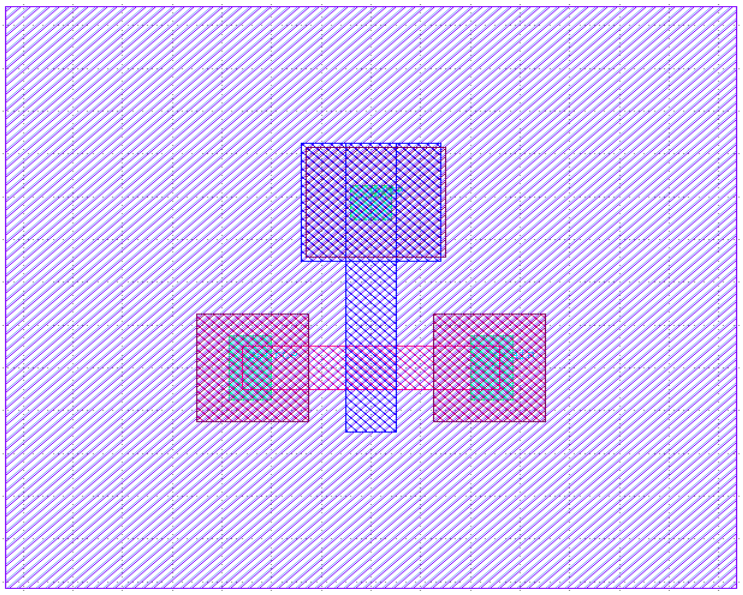


fig. 4.2.1(a) Layout of FinFET

- **3D view of FinFET**

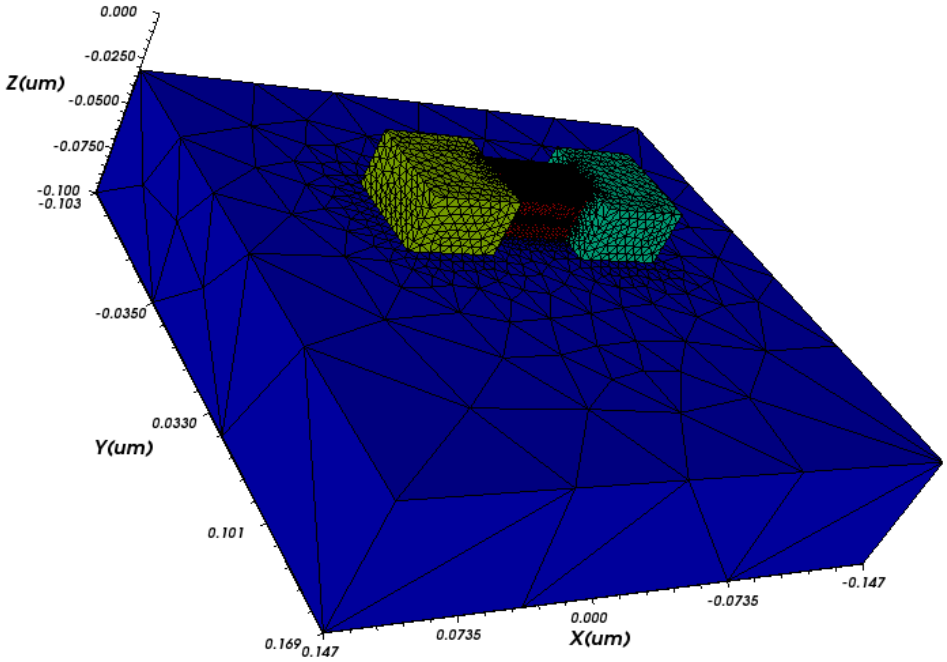


fig 4.2.1(b) 3D mesh of single fin FinFET

- **Impact of Fin thickness**

The comparison of results is shown below at two different t_{si} at table 4.2.1(a) and 4.2.1(b) and fig.4.2.1(c) and 4.2.1(d)

TABLE 4.2.1(a) ,Results at V_d =.6V and t_{si} =10nm

I_{ON}	1.23×10^{-5} A
I_{OFF}	1.7×10^{-13} A
DIBL	.08
V_t	.32 V

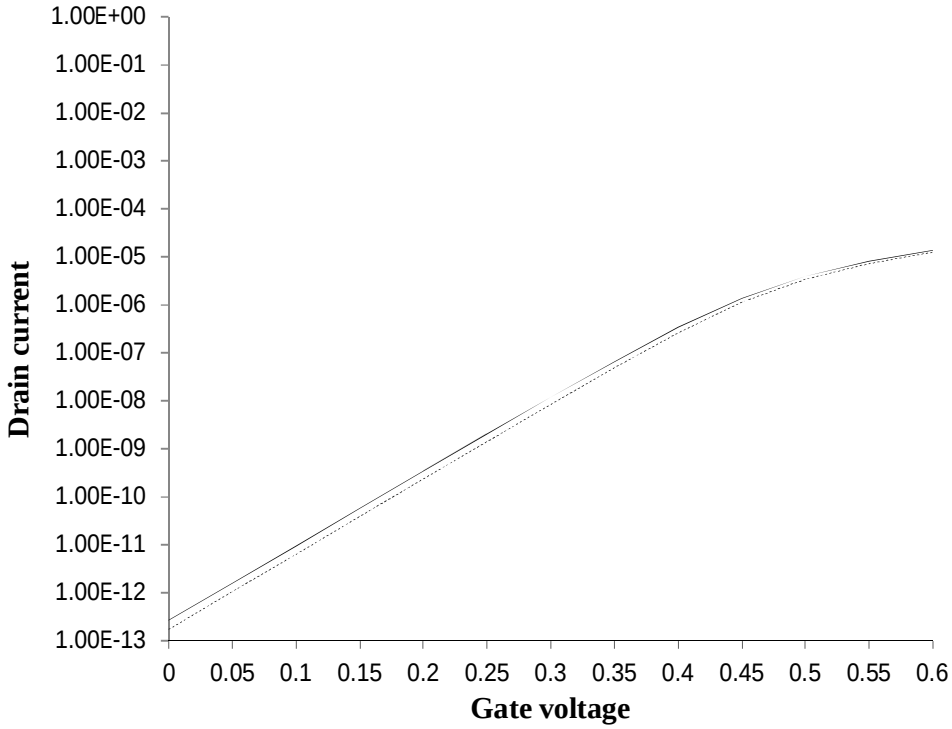


fig.4.2.1(c) drain current versus gate voltage at different drain voltages at tsi=10nm ,dash line representing drain current at drain voltage =1.2V and solid line representing drain current at drain voltage =.6V

TABLE 4.2.1(b) Results at V_d =.6V and t_{si} =30nm

I_{ON}	1.72×10^{-5} A
I_{OFF}	5.12×10^{-9} A
DIBL	.33
V_t	.18 V

From the results it is clear that by increasing the fin thickness the drain current increases but short channel effects increases more ,in fig.4.2(e) it can be easily understood.

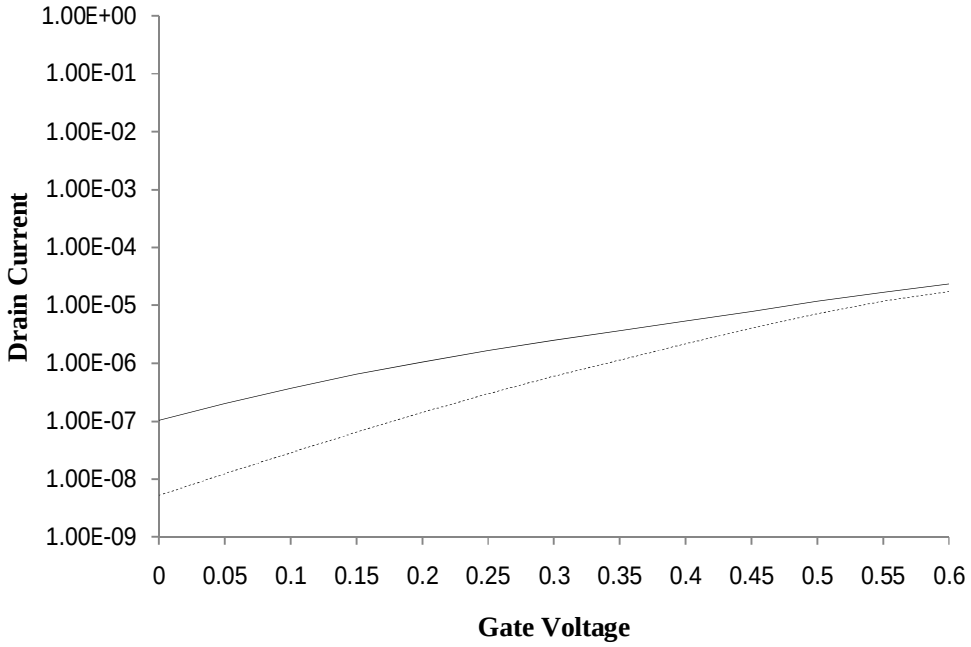


fig.4.2.1(d) drain current versus gate voltage at different drain voltages at tsi=30nm ,dash line representing drain current at drain voltage =1.2V and solid line representing drain current at drain voltage =.6V

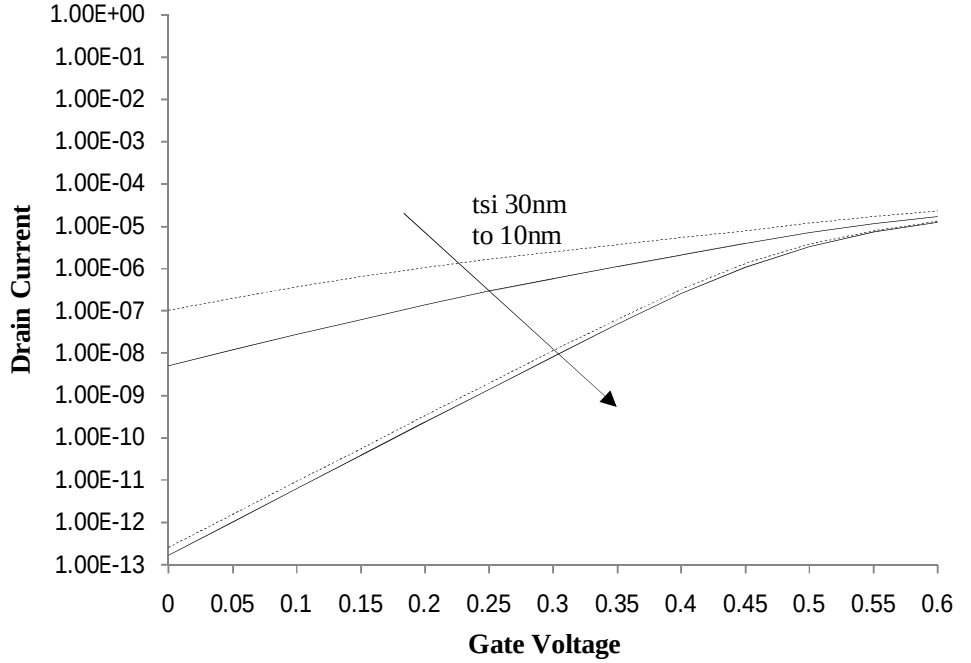


fig.4.2.1(e) drain current versus gate voltage at different drain voltages at tsi=30nm and 10nm, dash line representing drain current at drain voltage =1.2V and solid line representing drain current at drain voltage =.6V

4.2.2 Multi fin FinFET

- **Layout of double fin Finfet**

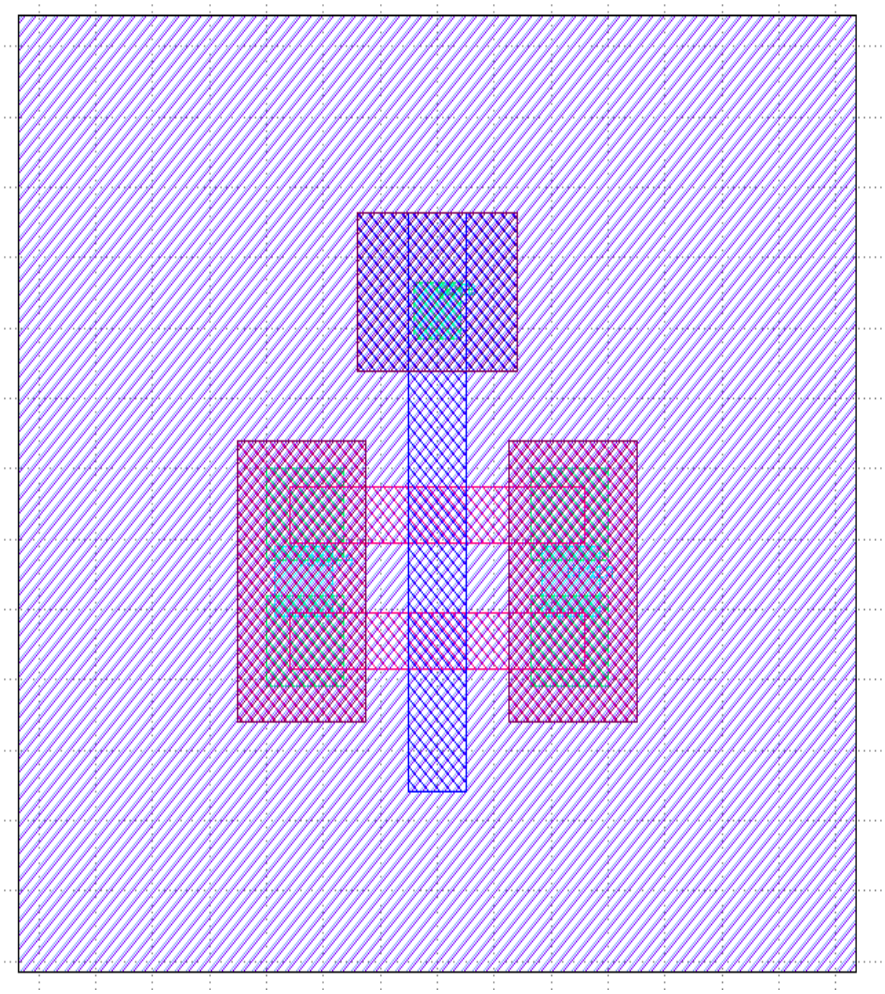


fig.4.2.2(a) Layout of double fin FinFET

The layout of double fin FinFET is given in above fig. and the advantage of increasing fin on the single substrate is to increase the drive current without increasing short channel effects because by increasing fin the effective width increases but the fin thickness of every fin remains same and short channel effect only depends on increasing fin thickness, if the fin thickness of single fin is increase than the short channel effects increases, that's why we mostly prefer to increase number of fins to increase the drive current.

- **3D view of double fin FinFET**

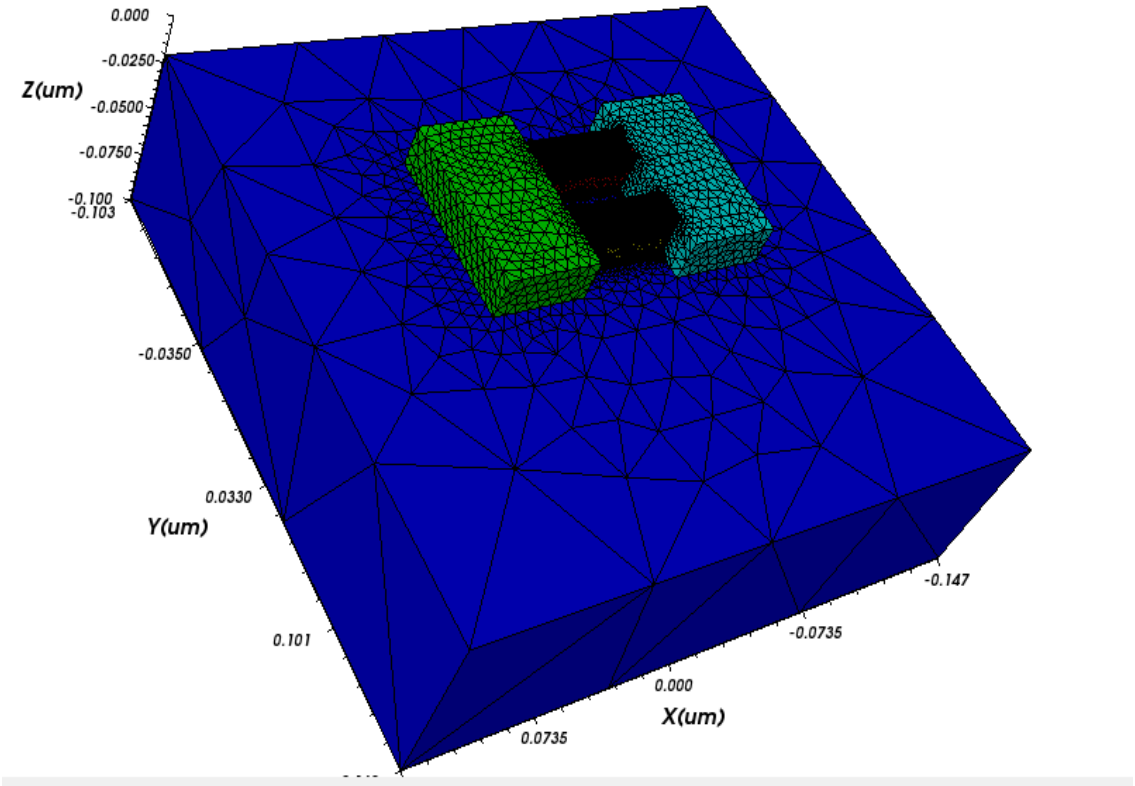


fig 4.2.2(b)3D mesh of double fin FinFET

- **Comparision of single fin and multi fin FinFET**

The TGFinFET is the best structure in submicron technology due to reduce short channel effects and its compatibility for fabrication steps . But the main disadvantage of single fin TGFinFET is reduce drive current because of thinner fins due to which number of charge carriers participating in current is less[28]. This problem can be solved by increasing the number of fins on the same substrate so that the width of the device increases and hence number of charge carriers increases thus the current increases as shown in fig.4.2.2(c)

From the graph it is seen that drive current has been increased by increasing fins.

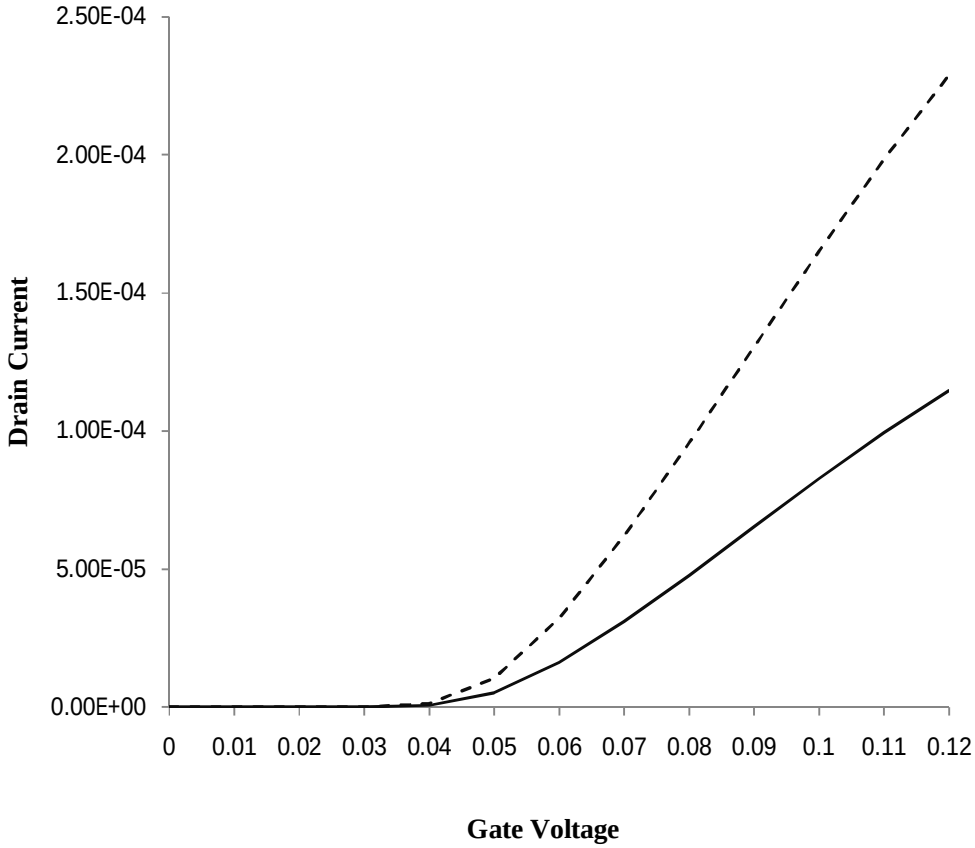


fig.4.2.2(c) drain current versus gate voltage of double fin and single fin TGFinFET at drain voltage =.6, where dash line represents double fin TGFinFET and continuous represents single fin FinFET.

- **Corner effect**

In strong inversion region in doped TGFinFET the most leaky path is shifted to the corners where maximum gate voltage is observed because of electric field fringing due to coupling of the top gate and the side gates hence higher potential and electron density is observed at the corners as shown in fig.4.2.2(d) and fig.4.2.2(e)

From the graphs shown below it is clear that the potential and electron density is more at the corners due to which corners offer lower threshold voltage as compare to the channel threshold voltage due to which leakage occurs. This problem has become severe as we go more to submicron technologies.

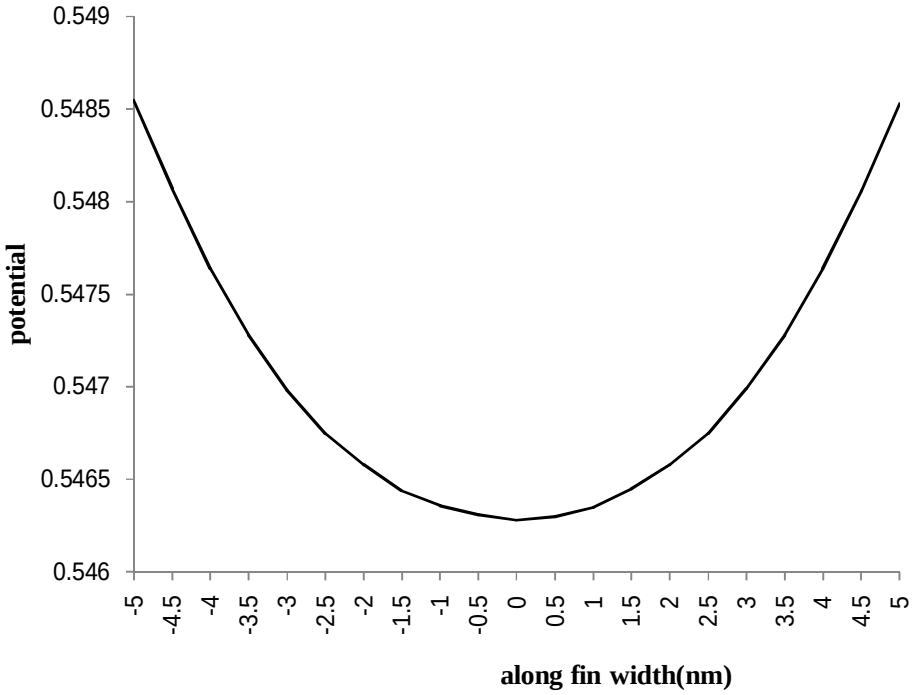


fig.4.2.2(d) potential graph at strong inversion along the fin width (y direction) showing that the maximum potential at the corner of fin

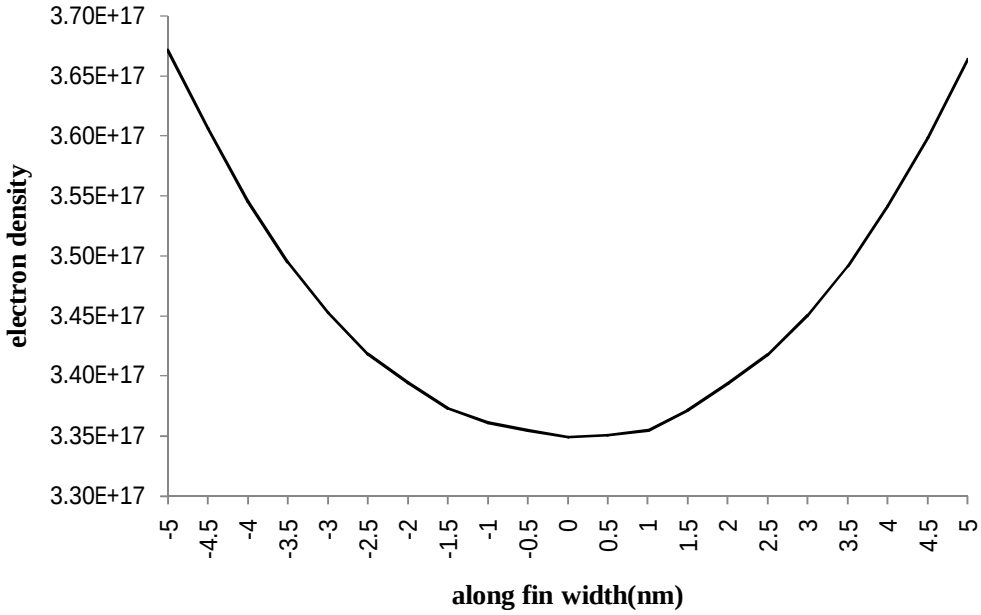


fig4.2.2(e) electron density graph at strong inversion along the fin width (y direction) showing that the maximum electron density at the corner of fin

This problem can be solved by making the corner rounds[11][12] as shown in fig.4.7, due to which the electric field at the corners are cancelled out which are responsible for pulling the electron at the corners and hence the electron density and potential becomes almost constant throughout the width.

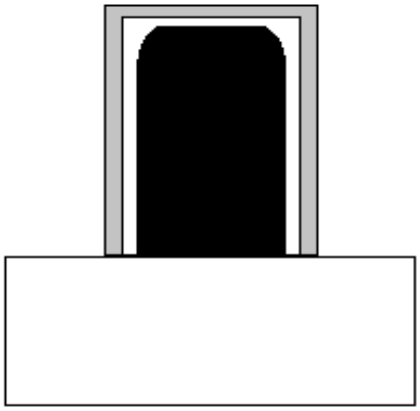


fig.4.2.2(f) schematic view of TGFinFET having its corner round

Comparison of electron density and potential along the fin width in TGFinFET is shown in fig.4.2.2(g) and 4.2.2(h)

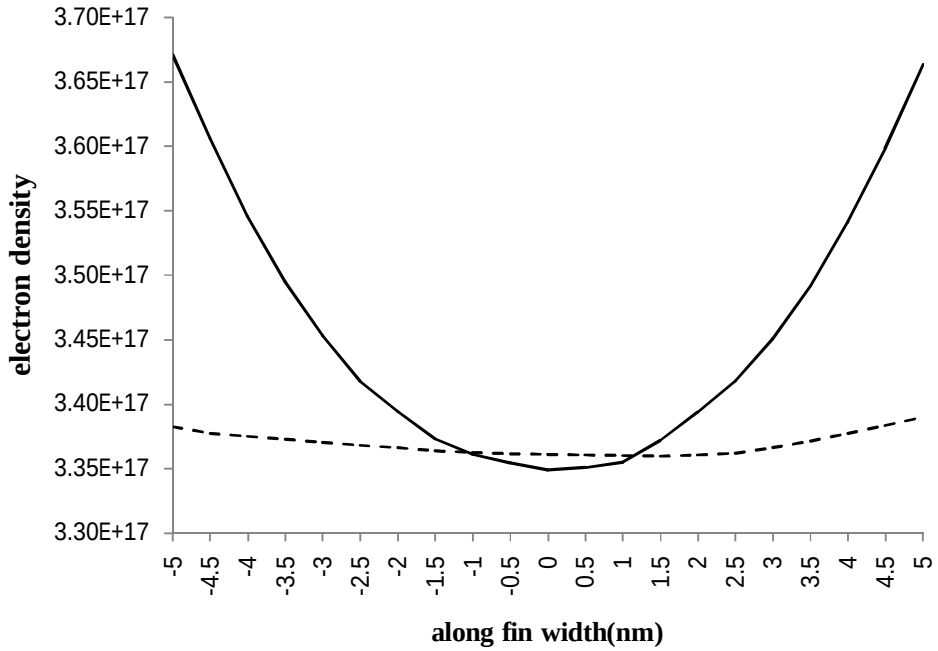


fig.4.2.2(g) electron density graph at strong inversion along the fin width (y direction) ,dash line representing electron density of TGFinFET with round corners and continuous representing electron density of TGFinFET without round corners

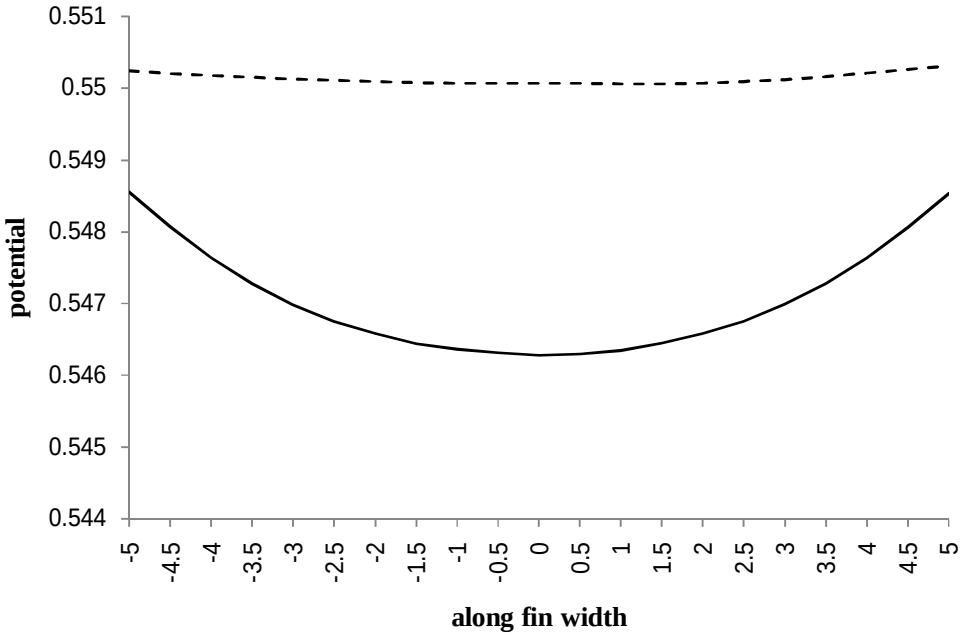


fig.4.2.2(h) potential graph at strong inversion along the fin width (y direction) ,dash line representing potential of TGFinFET with round corners and continuous representing potential of TGFinFET without round corners

From the fig.4.2.2(g) and 4.2.2(h) it can be concluded that by making the corner rounds of the fin the potential and the electron density will become almost equal along the width due to which the leakage due to extra channel formed at the corners will reduce.

4.2.3 CMOS Inverter

- **Layout of CMOS Inverter with single fin**

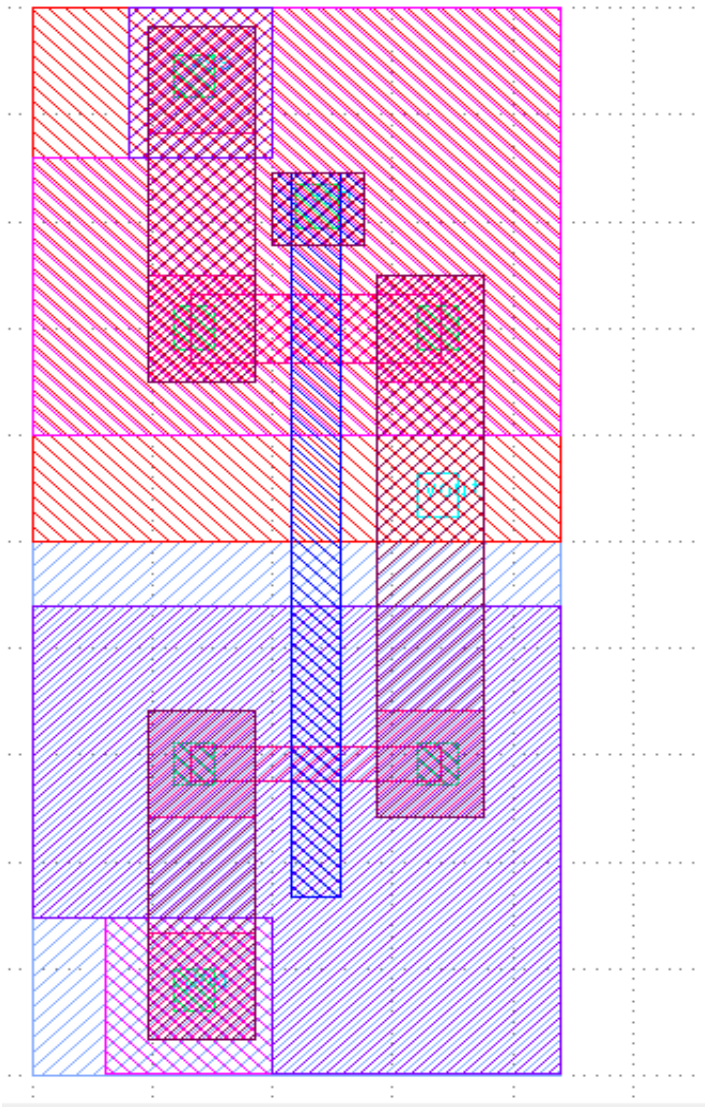


fig.4.2.3(a) layout of CMOS inverter

fig4.2.3(a) shows the layout of CMOS inverter in which the pull up network fin thickness(PMOS fin thickness) has been increased to equalize the mobility of pull down network. But from fig.4.2.1(e) it has identified that by increasing the thickness of fin short channel effect increases, hence a new structure has been developed with the use of double fin FinFET for pull up network and single fin FinFET for pull down network as shown in fig. 4.2.3(b)

- **Layout of new structure of CMOS inverter**

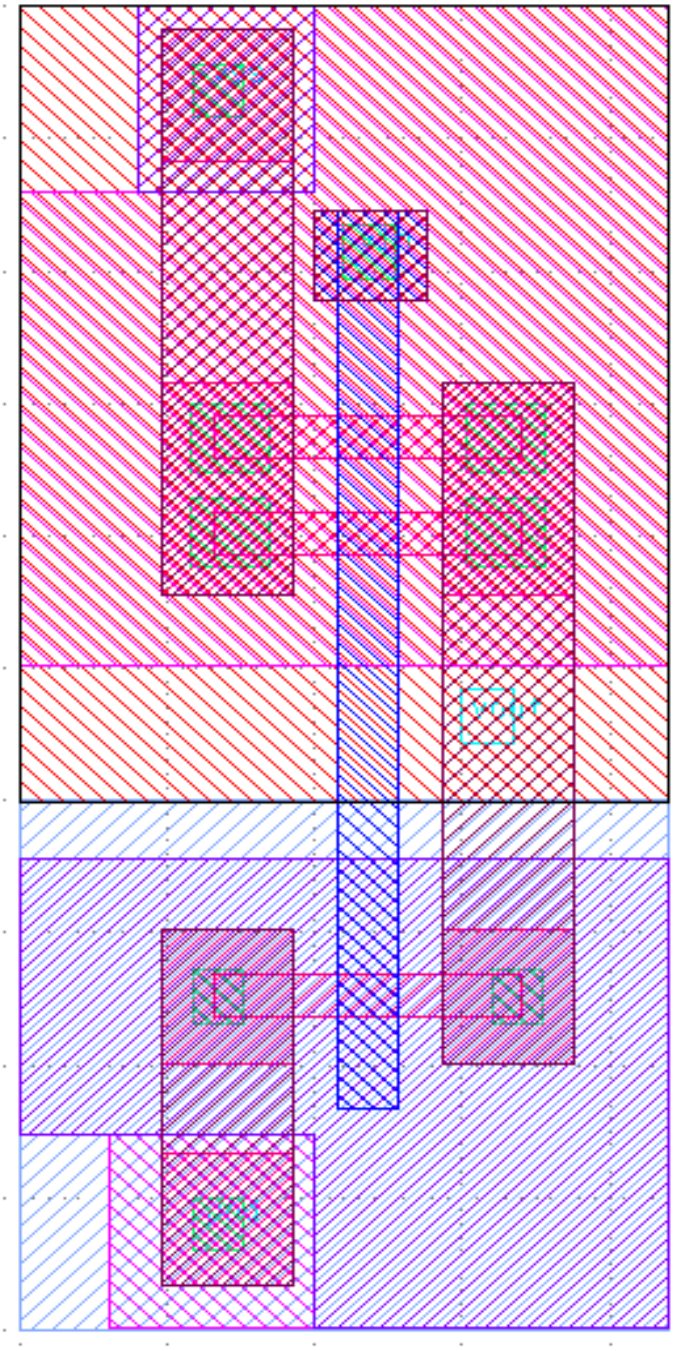


fig 4.2.3(b) layout of new structure of CMOS inverter

By using this structure the effective width of the pull up network has been increased , while the thickness of single fin remains same as in pull down network. Hence the short channel effects remains the same as in pull down network which is very less due to less thick fin.

- **3D view of new CMOS inverter**

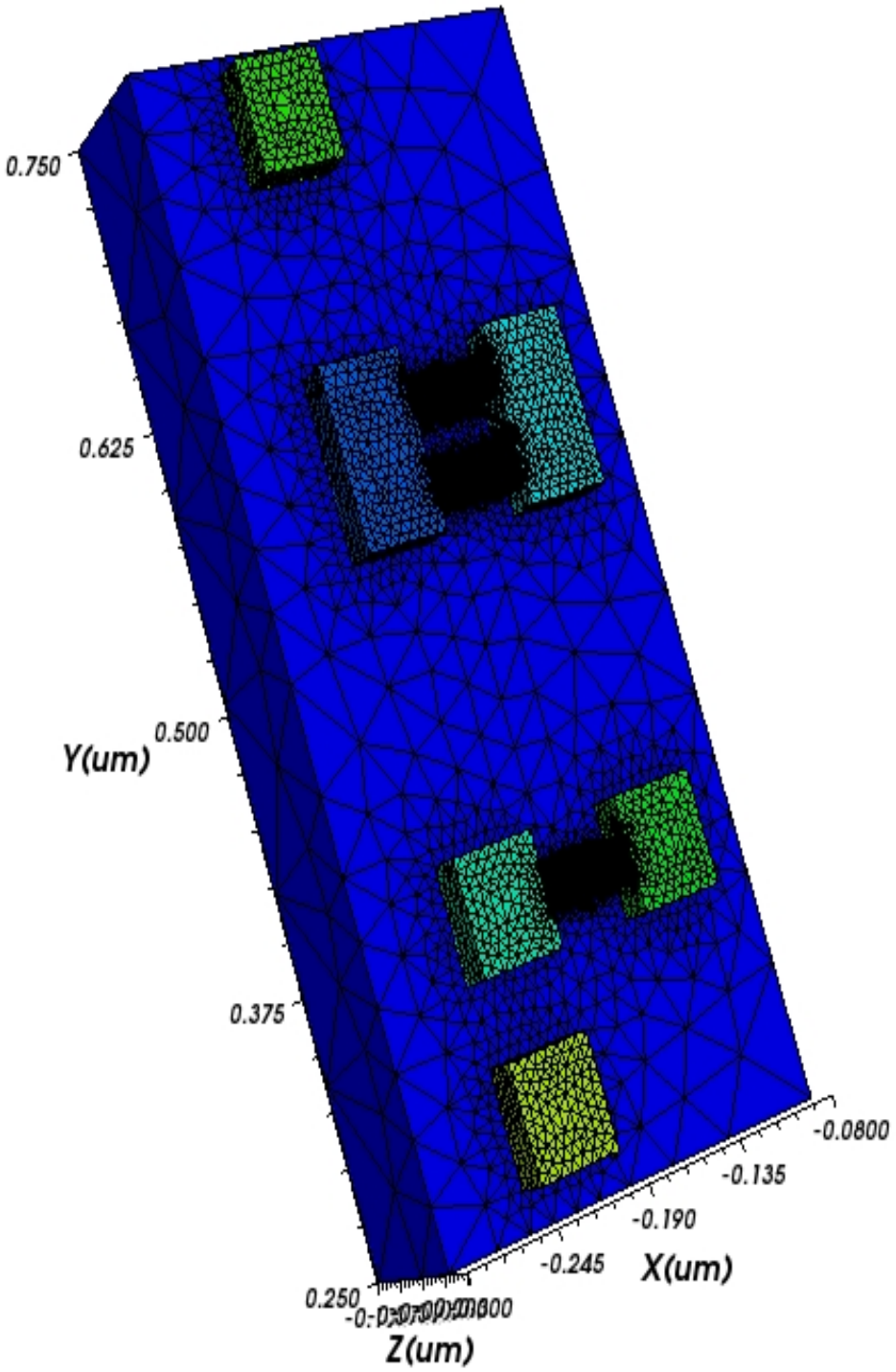


fig4.2.3(c) 3D mesh of new structure of CMOS inverter

- **DC analysis of new structure of CMOS inverter**

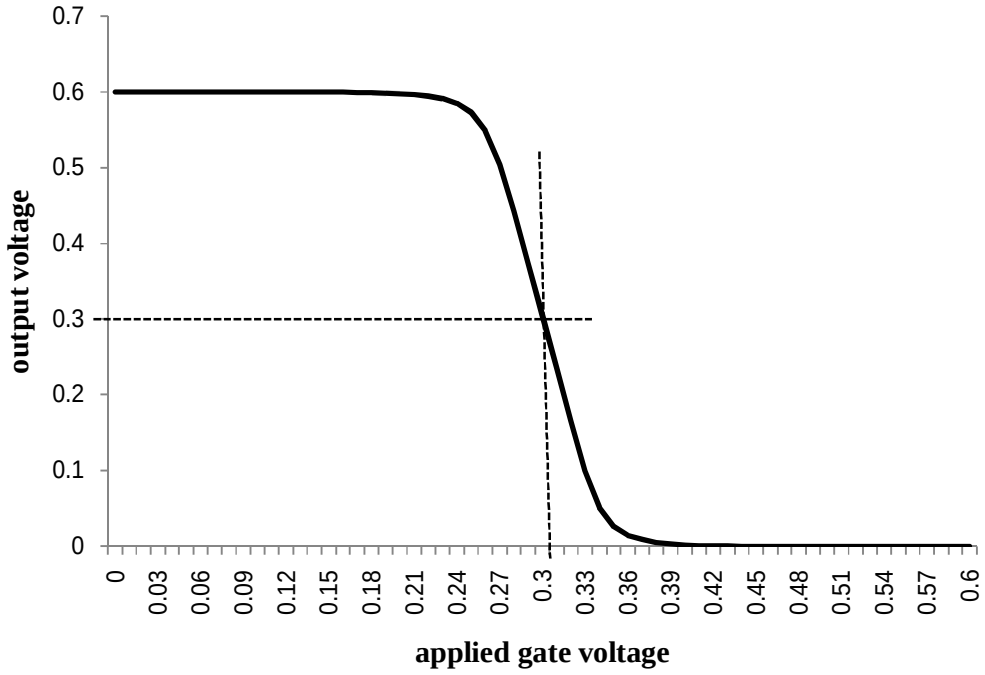


fig.4.2.3(d) DC analysis of CMOS inverter

- **Transient analysis of new structure CMOS inverter**

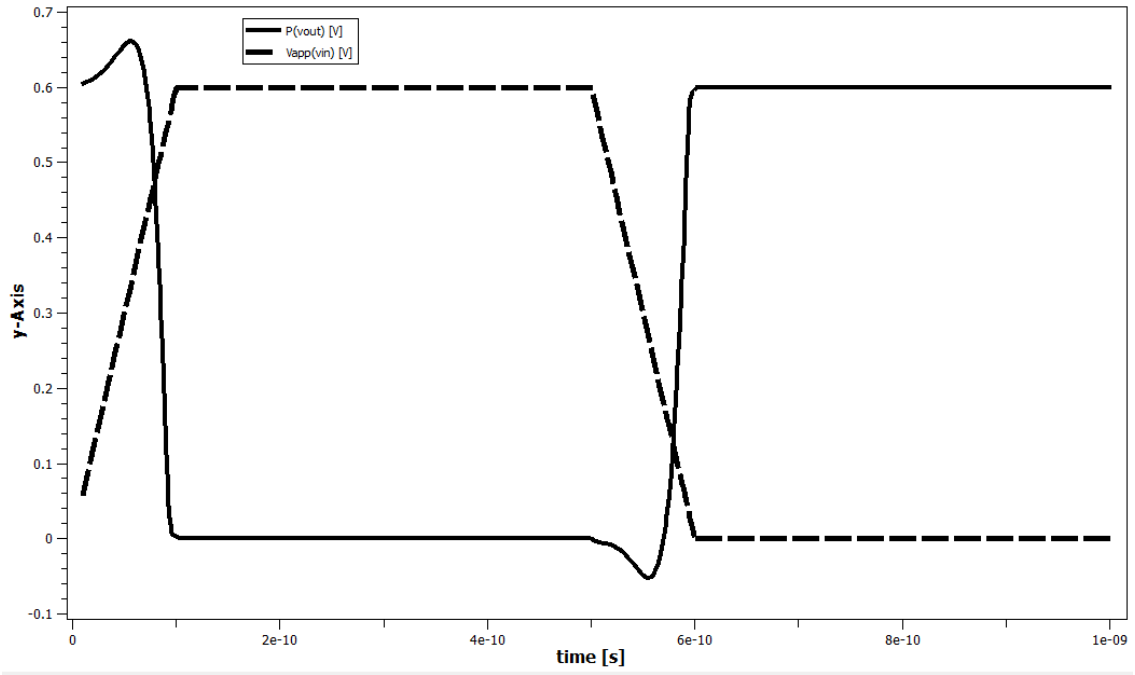


fig4.2.4(e) Transient analysis of CMOS inverter

Comparision of CMOS inverter designed by DGMOSFET and TG FinFET has been shown in the figure. From the figure it can be analyzed that FinFET CMOS inverter shows better agreement than DGMOSFET.

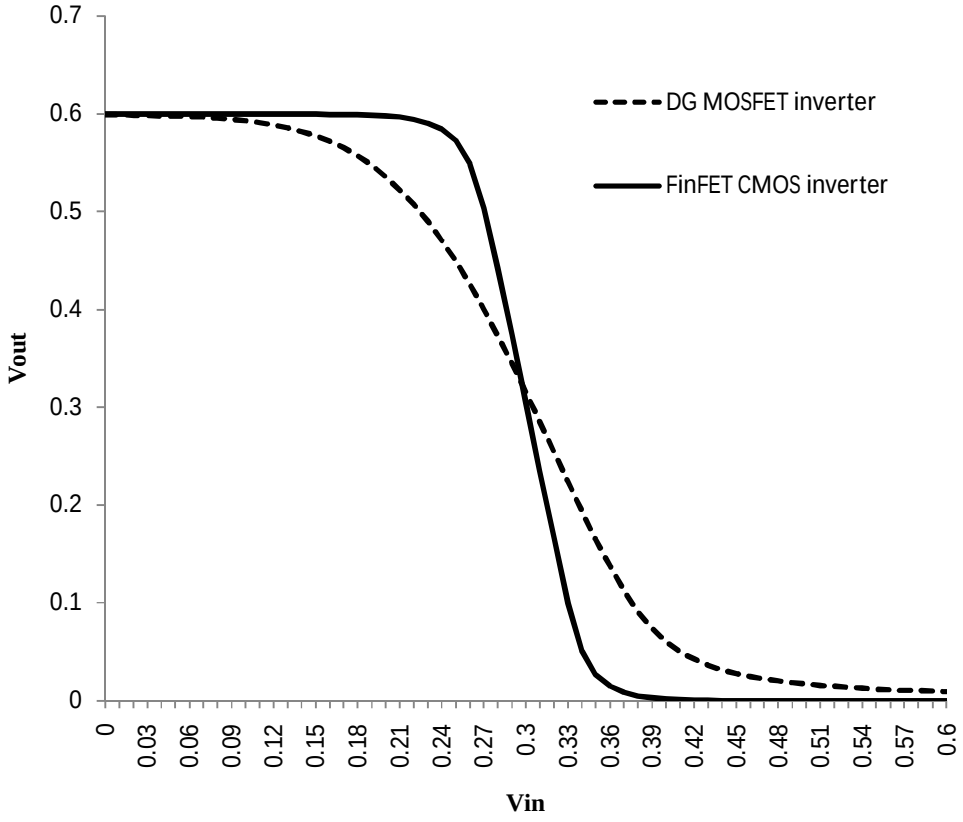


fig.4.2.4(f) comparison of CMOS inverter designed with TGFinFET and with DG MOSFET

4.2.4 Ring Oscillator

Ring oscillator is a device having odd number of not gates (CMOS inverters) , whose output oscillates between two levels 1 or 0. In ring oscillator no input is required but the output comes .It is mainly used as a delay element.

- **Layout of ring oscillator**

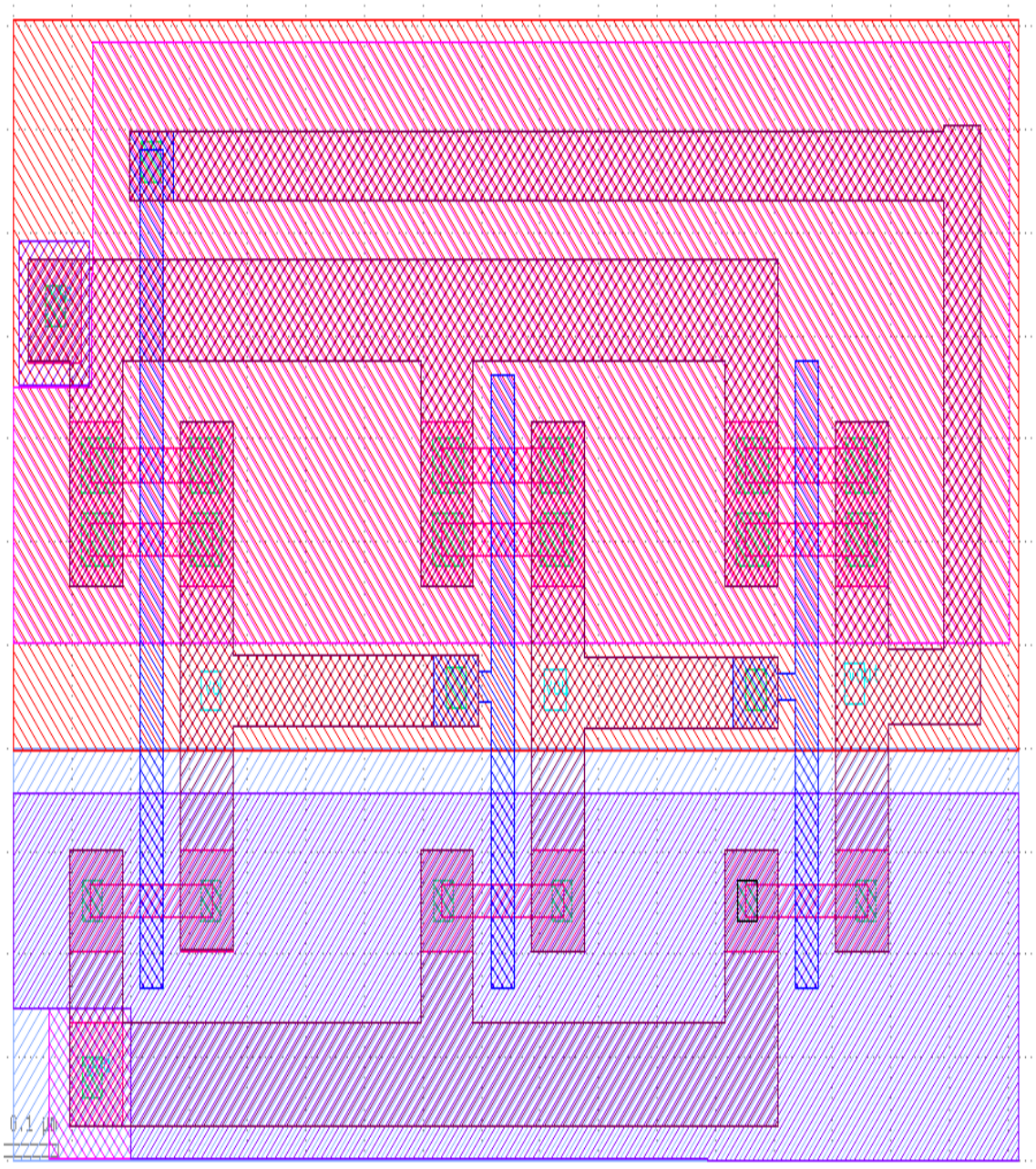


fig.4.2.4(a) Layout of ring oscillator

- **3D view of Ring Oscillator**

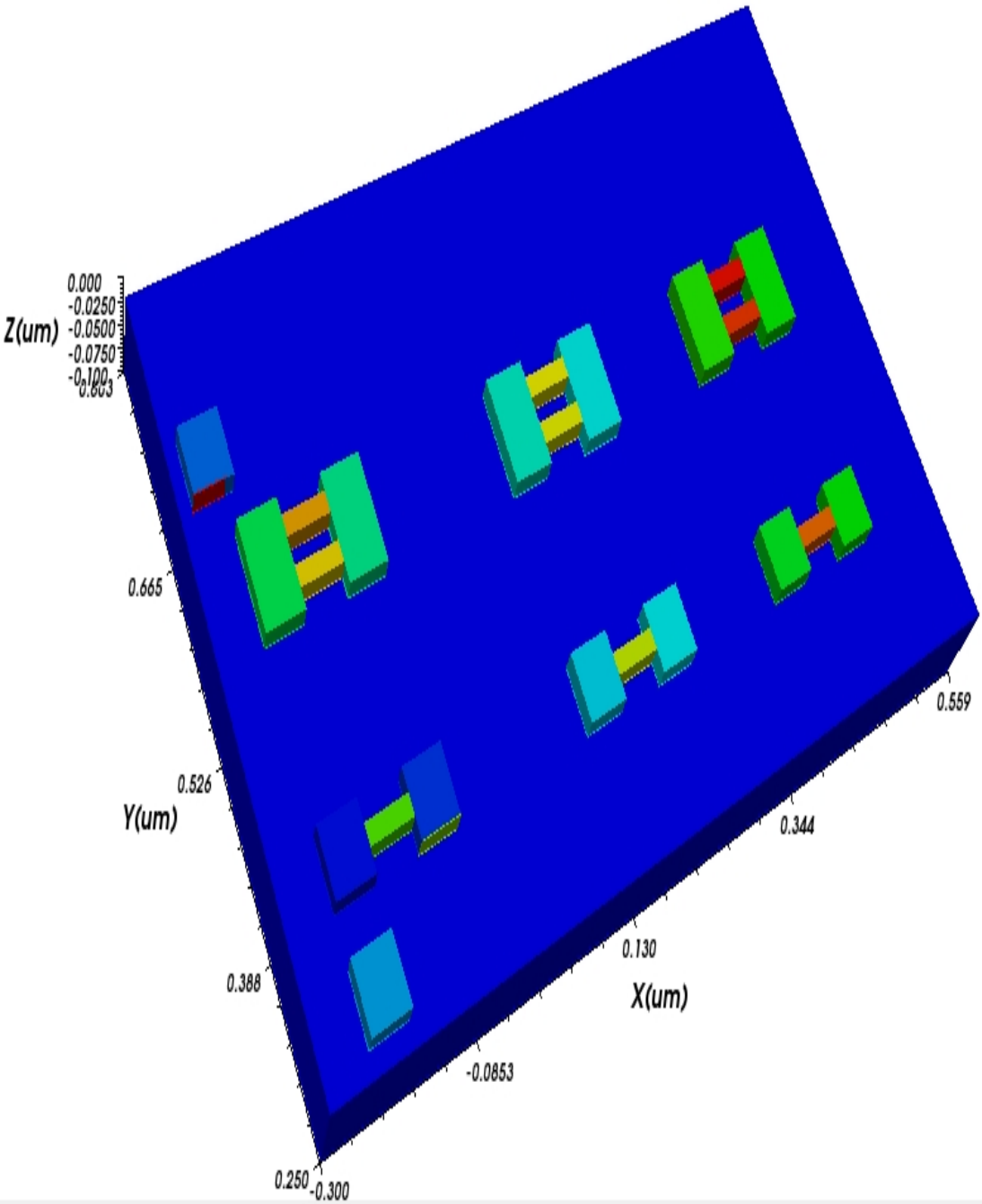


fig.4.2.4(b) 3D view of ring oscillator

- **Transient analysis of ring oscillator**

fig 4.2.4 shows the graph between time and output of the ring oscillator which oscillates between zero and one and Vss is the voltage given at source which is becoming constant after some time.

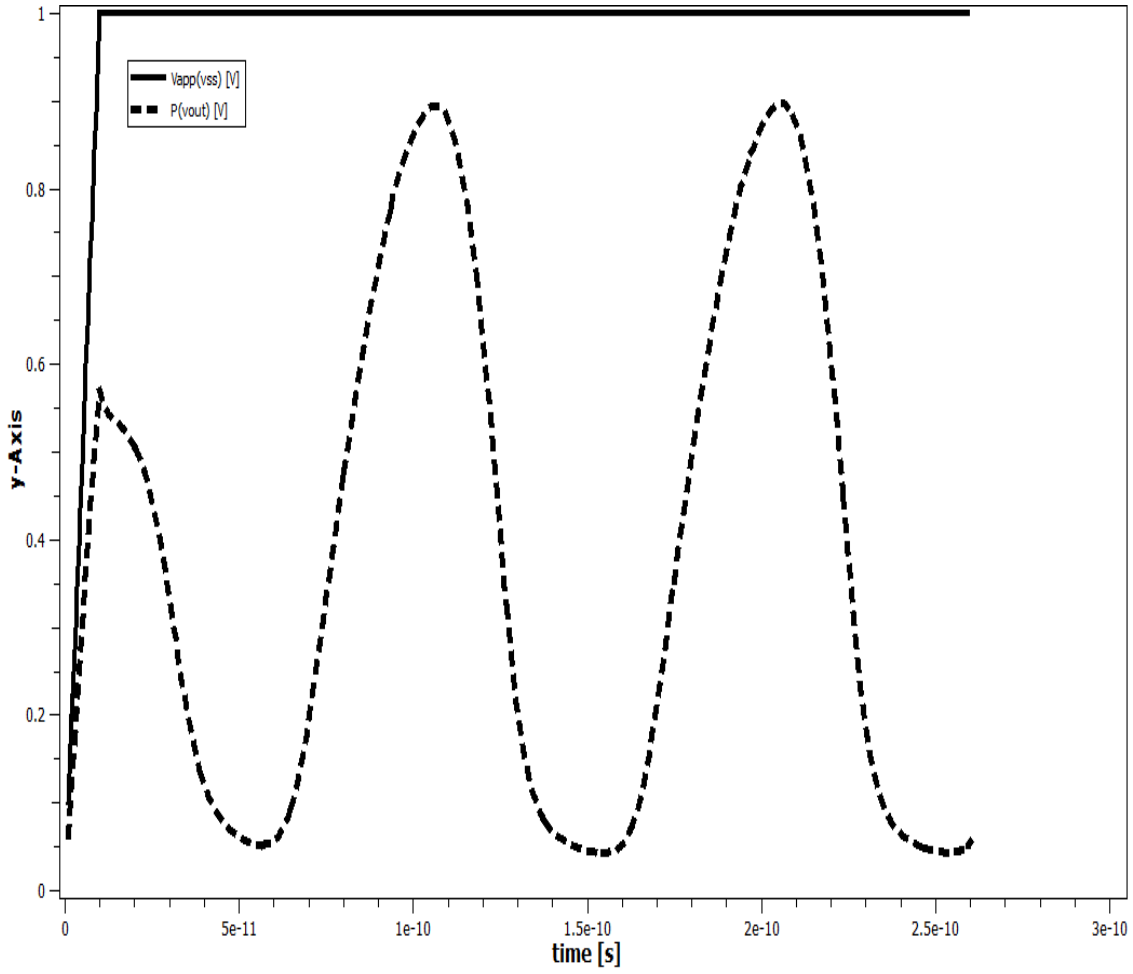


fig.4.2.4(c) transient analysis of CMOS inverter

The ring oscillator mainly works as a not gate with delay. Delay is because the use of odd number of not gates or CMOS inverter. The output of one CMOS inverter goes to the input of other CMOS inverter and some delay is occurred at every stage of the inverter. Hence main use of ring oscillator is as a delay element.

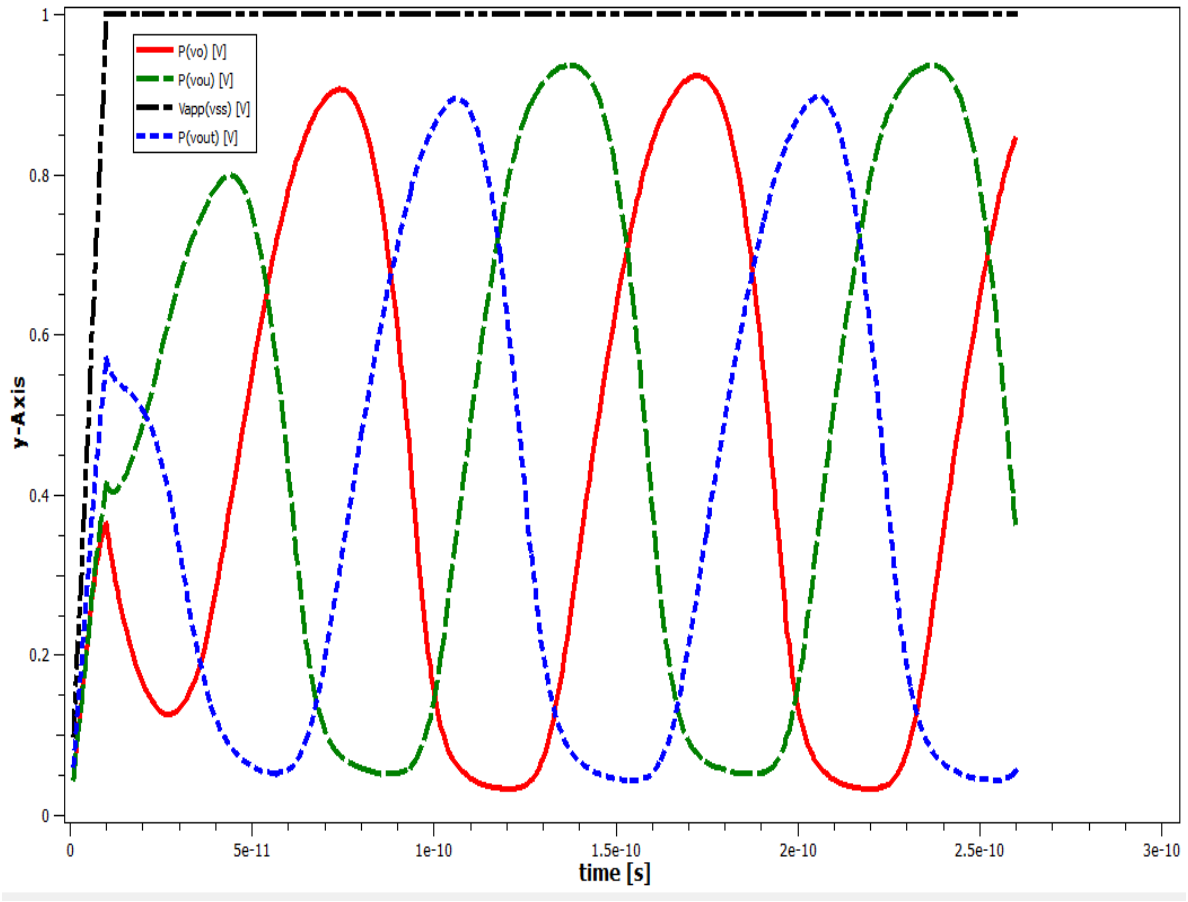


fig 4.2.4(d) result of every CMOS inverter output of ring oscillator

CHAPTER 5
Conclusion and Future scope

A current model for single and multifin TGFinFET has been designed by introducing the effect of depletion charges. It is found that depletion charges affect the threshold voltage when the fin is lightly doped. An inversion region-switching parameter has also been introduced to get better agreement of the model with the simulated results.

Comparison of drive current for single fin FinFET and double fin FinFET has been done and it is observed that by increasing the number of fins the drive current increases and short channel effects remains almost same as in single fin FinFET. By increasing the number of fins the effective width of the device increases but the width of individual fins remains same and hence the short channel effects in multi fin FinFET in comparision of wider single fin FinFET is reduced.

Impact of silicon body thickness for double gate MOSFET has been analyzed. Decreasing the silicon thickness reduces the short channel effects, as it increases the control of gate over channel. The drive current should also decrease due to the reduction in Si thickness but it is somewhat overcome by the volume inversion of the channel.

Impact of fin thickness for TGFinFET has been shown and found that by decreasing fin thickness the short channel effects decreases.

The most leaky path in the subthreshold region and strong inversion region has been identified at bottom centre and at corner of the fins respectively. This suggests that lesser the fin thickness, more will the control of gate on the channel and hence less subthreshold leakage. Also rounding the corners will decrease the leakage due to corner effect.

CMOS inverter has been designed by using single fin n-channel FinFET for pull down circuit and double fin p-channel FinFET for pull up circuit. To equalise the strength of n-channel FinFET, the width of p-channel FinFET should be increased but by increasing the individual width of fin the short channel effects increases as discuss above. Hence the number of fins of p-channel FinFET has been increased to increase the effective fin width only and not the short channel effects.

DC analysis and transient analysis of CMOS inverter using designed using FinFETs has been done and a better agreement of characteristics with conventional CMOS inverter has been found. A ring oscillator using FinFET CMOS inverter has also been designed and simulated.

TG FinFET controls the channel through three sides. The controllability of gate over the channel can be further increased by using surrounding gate MOSFETs, which covers the channel through four sides. By the use of different gate stacks the performance of the TG FinFET can be improved.

Further the channel length is reduced upto atomic levels for which carbon nano tubes and silicon nano wires are used.

The current model proposed here for FinFET shows the good agreement with the simulated results but still the model is insufficient for the higher technology MOSFETs. For the sub 10nm technology the electron behaviour changes from particle to wave. To model the transport of electron for these small atomic level dimensions quantum models are needed.

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