ANALYTICAL MODELING OF THRESHOLD VOLTAGE AND SUB-THRESHOLD DRAIN CURRENT FOR DOUBLE-GATE JUNCTIONLESS MOSFET

A Thesis Submitted in Partial Fulfillment of the Requirement for the Award of the Degree of

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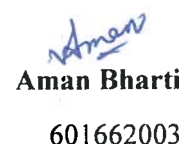
JULY, 2018

DECLARATION

I, Aman Bharti hereby declare that the work presented in this thesis entitled "**Analytical modeling of threshold voltage and sub-threshold drain current for double-gate junctionless MOSFET**" in fulfilment of the requirement for the award of degree of Master of Technology submitted at Electronics and Communication Engineering department, Thapar Institute of Engineering & Technology (Deemed to be University), Patiala is an authentic record of work carried out under supervision of Mr. Arun Kumar Chatterjee (Professor, ECED, Thapar Institute of Engineering & Technology) from January 2017 to July 2018. The matter presented in this has not been submitted either in part or full to any other university or institute for the award of any other degree.



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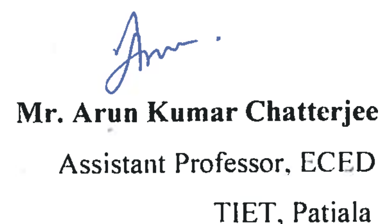

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ABSTRACT

A Junctionless Transistor (JL) is a uniformly doped device without any source and drain junction. It allows full depletion of charge carriers when the device is turned off. The fabricated junctionless device with a high content of impurity concentration within the channel and source/drain regions requires no junctions. It exhibits many advantages, such as simplified and flexible fabrication process, nearly ideal subthreshold slope (SS ≈ 60 mV/decade), high ON–OFF current ratio ($I_{ON}/I_{OFF} > 10^7$), low source/drain series resistance, and small drain induced barrier lowering. Within the bulk, channel is formed when a small bias is applied to the gate and current starts flowing. The channel becomes neutral under the flat band condition.

In this dissertation, an analytical drain current model has been obtained in the subthreshold region for a symmetrical Double Gate junctionless MOSFET. A two Dimensional analytical solution for Poisson's equation has been derived by using the surface potential based charge model considering only the mobile charge carriers. The effect of hot carrier injection is also considered by including interface charges at the junction of silicon dioxide and silicon film. Using this surface potential, the mobile charge density in the channel region has been evaluated which is used in the Pao-Sah integral in order to obtain the drain current in the subthreshold region. The developed drain current model and threshold voltage model for a device damaged due to localized charges is shown and it has been found that the developed model has better ON current by OFF current ratio and subthreshold slope.

Further, for 40 nm technologies the characteristics of drain current model in subthreshold region for DG JL MOSFET are compared with the numerically simulated results obtained from ATLAS module of SILVACO TCAD tool. The developed model is in good agreement with that of the simulation results.

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LIST OF ABBREVIATIONS

IC	Integrated Circuit
MOSFET	Metal-Oxide-Semiconductor Field Effect Transistor
CMOS	Complementary Metal-Oxide-Semiconductor
ITRS	International Technology Roadmap for Semiconductors
SCE	Short Channel Effect
SOI	Silicon-On-Insulator
FET	Field Effect Transistor
DIBL	Drain-Induced Barrier Lowering
SS	Subthreshold Slope
PD-SOI	Partially Depleted SOI
FD-SOI	Fully Depleted SOI
DG JL MOSFET	Double Gate Junctionless MOSFET
DG MOSFET	Double Gate MOSFET

CHAPTER 1

INTRODUCTION

1.1 BACKGROUND

In the early years of the development of integrated electronics, Integrated Circuits (ICs) contained only a few transistors. With the ever increasing complexity in the circuits, the number of components in these circuits increased steadily. To meet this growing demand of increasing components in a chip, scaling of components started. Metal Oxide Semiconductor Field Effect Transistors (MOSFETs) use Metal Insulator Semiconductor (MIS) as their main component, are now majorly used for IC development over the past two decades. With the advancing technology, silicon based MOSFETs have continually delivered performance gain with reduction in the cost of manufacturing. Moore's law states that the number of transistors in an integrated circuit will double every eighteen months. Semiconductor industry has kept up with this law with tremendous advancements in the field of device scaling. The dimensional scaling of CMOS has been one of the key driving forces behind the evolution of semiconductor electronics. Today, CMOS based semiconductor electronics can be found everywhere around us, ranging from portable electronics to the telecommunications sector.

A lot of research and tremendous amounts of resources have gone into device design over the past thirty years. The evolution of scaling technologies has brought a lot of new opportunities, however, a lot of new obstacles have also come forward as the device size has gone down. As the CMOS technology enters the nanometer ranges, short channel effects come into the picture. These effects are primarily due to the small geometry of the devices under consideration. Short Channel effects can be reduced to an extent by reducing the gate oxide thickness. This reduction in gate oxide thickness results in gate leakage currents which in turn increase the power consumption in the chip, which is completely undesirable. Other than short channel effects, quantum effects also result from device scaling which affect the device behavior.

1.2 TECHNOLOGY SCALING

Scaling results in reduced dimensions of the devices and increases the device density as well as the functional capacity of the chip. [1] Over the past few decades, the typical channel lengths in MOSFETs have been scaled down from several micrometers to as short as tens of nanometers. As a consequence, the number of transistors that can be fabricated on an IC has increased significantly in the past few decades. There are several reasons behind the desirability of smaller size of MOSFETs.

The primary reason is that smaller the size of the device that is being fabricated, more will be the number of devices that can be incorporated in a given area.

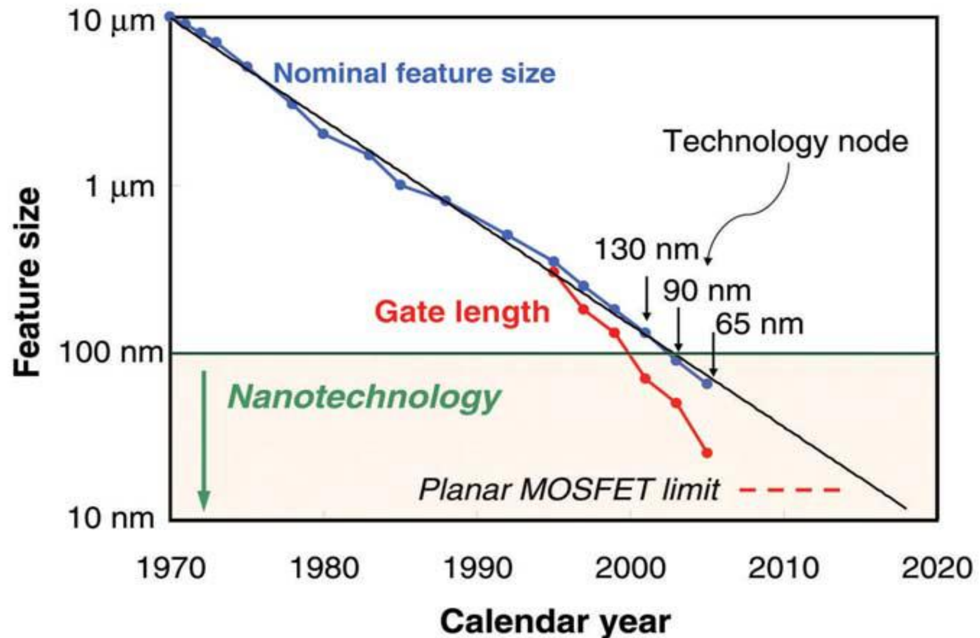


Figure 1.1 Gate length and technology node size of transistor versus calendar year [1].

As a result, the chips have more functionality in a relatively smaller area, or it can also be viewed as an increase in the functionality of the chip in the same area. The cost of fabrication remains fairly constant, so decrease in the size of devices results in the possibility of manufacture of more number of chips on the wafer. This in turn reduces the cost per chip. Hence the number of transistors per chip increases with every new technology node. The number of MOSFETs fabricated in a 45 nm technology node might as well be double the number fabricated in a 65 nm chip. This trend was first observed by Gordon Moore in the year 1965 and came to be known as the Moore's Law. Moore's Law is an appropriate description of the rapid trend of miniaturization. Whenever the minimum line width is reduced, a new technology node, or technology generation is introduced.

Smaller transistors are also expected to have higher switching rates. One of the approaches that are used to scale down transistors is to reduce all the device dimensions in a proportional manner. These dimensions include channel length, channel width and oxide thickness. When these dimensions are scaled down proportionally, that is, with same factors, the resistance in the channel does not change, but the gate capacitance gets scaled down. This results in the reduction of the RC delay and the device is expected to have a shorter switching time. However, with the present trend in scaling of MOSFETs, reduced transistor dimensions do not necessarily translate to increased speed because of delay caused by the interconnects becomes more significant.

Since 1965, the cost of one bit of memory has dropped about 100 million times. The primary factor behind this significant reduction in cost has been the scaling of MOSFETs. Device miniaturization has also been responsible for the improvement in the speed and power consumption in ICs.

With the CMOS technology scaling, packaging technology is also required to progress at a consistent rate with sustainable cost and performance levels. Advances in I/O density, heat extraction, bandwidth, power distribution and system architecture are required.

1.3 TYPES OF SCALING

Scaling can be classified into the following two categories:

1. Constant Field Scaling
2. Generalized Scaling

1. Constant Field Scaling: This type of scaling results from reduction in device dimensions and supply voltage of the transistor and an increase in the doping density by a constant factor, called the scaling factor. The supply voltage is scaled by this factor, but the electric field remains constant, hence the name constant field scaling.

2. Generalized Scaling: At sub micrometer levels, the electric field of the device does not remain constant due to the presence of short channel effects. Gradual field approximation fails at such small device dimensions and the electric field changes. This was addressed by Brews et. al. [2] and they have proposed a minimum channel length that can be maintained so as to maintain the same subthreshold characteristics.

$$L_{min} = A\,[x_j t_{ox}(W_s + W_d{}^2)]^{1/3}$$

Where L_{min} is the minimum channel length, W_s and W_d are the depletion widths of source and drain regions, x_j is the junction depth t_{ox} is the oxide thickness and A is the proportionality constant. This approach of scaling has many advantages over constant field scaling [3]. One of the major advantages is that all the dimensions are not required to be scaled down by the same factor. Only three factors were suggested by Brews, but later it was found that MOSFET scaling depends on five factors, L_G, t_{ox}, V_{DD}, N_A, x_j. Under Short Channel Effects (SCE), the device behavior depends on these five parameters.

1.4 SHORT CHANNEL EFFECTS:

Device scaling results in several Short Channel Effects. [4] These are defined below:

1. Drain Induced Barrier Lowering (DIBL) and Punch through: Punch through occurs when the depletion regions surrounding the drain extend to the source due to reverse bias and merge. It can be minimized with larger substrate doping, thinner oxides, shallower junctions. Current flows in a MOSFET through an inversion layer. This inversion layer is formed by applying gate bias that is greater than the threshold voltage. If the gate voltage applied is less than the threshold voltage, there is a potential barrier to the flow of the charge carriers. When the gate voltage is increased, this potential barrier reduces and the charge carriers flow under the influence of this electric field. In small geometry MOSFETs, the drain voltage also influences this flow of charge carriers. At higher drain voltages, this potential barrier is reduced, and the carriers can move from source to drain even at low gate voltages. Thus, even when the gate voltage has not increased beyond the threshold voltage, sub-threshold current flows in the device. This phenomenon of the reduction in the potential barrier because of drain voltage is known as Drain Induced Barrier Lowering (DIBL).

2. PN Junction Leakage Currents: Source and Drain to well junctions are reverse biased and there is a reverse biased current associated with this biasing. This reverse bias current is comprised of two components, minority carrier current and current due to recombination of charges. The minority carrier current flows due to drift/diffusion in the depletion region. This reverse bias current mainly depends on the junction area and doping. With the increase in the concentration of PN junction doping with halo implants, then band to band tunneling current dominates reverse bias current.

3. Hot Electrons: Hot electrons result from the high electric field in the device due to small geometry. Electrons present inside the substrate region gain sufficient energy to overcome the potential barrier enter the oxide region. The accumulation of these electrons in the oxide region result in the increase of threshold voltage and thus affect the reliability of solid state devices greatly. It adversely affects the gate’s control over the drain current. These electrons cause leakage currents within the device and result in larger power dissipation. Figure 1.2 shows hot electron effect in a region of high longitudinal electric field in inversion channel of a MOSFET.

4. Impact Ionization: Due to the high velocity of electrons in the presence of longitudinal fields that are capable of generating electron hole pairs by impacting the silicon atoms and ionizing them, an undesirable short channel effect occurs. With the proper biasing, electrons are attracted towards drain and the holes substitute the parasitic current by entering the substrate. The region between the source and the drain acts like the base of n-p-n transistor, with the source and the drain acting as emitter and

collector respectively. The hole current formed by the holes collected by the source, a voltage drop is created and the previously reverse biased substrate source junction begins to conduct appreciably. This situation can also get worse if the electrons that are generated through the high fields enter the substrate and affect the nearby devices.

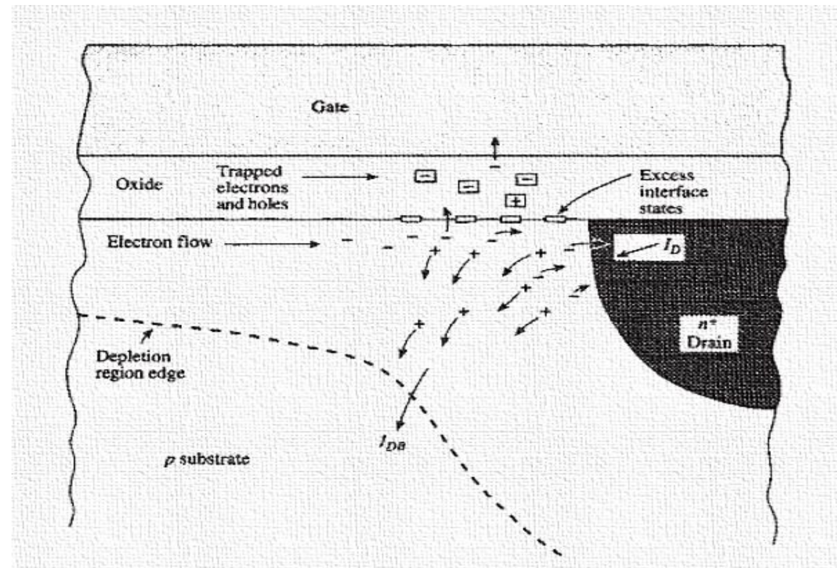


Figure 1.2 Hot electron carrier effect in a region of high longitudinal electric field in inversion channel of a MOSFET [5].

5. Surface Scattering: With the lateral expansion of the depletion layer into the channel region, the channel becomes smaller and the longitudinal electric field component increases, and as a result surface mobility becomes field dependent. Surface scattering results from the collisions suffered by the electrons that are attracted towards the interface. This phenomenon causes reduction in mobility and the carriers face difficulty in moving parallel to the interface and so the surface mobility is almost half of that of the bulk mobility.

6. Velocity Saturation: In the saturation mode of operation, the transconductance is reduced, affecting the performance of short channel devices due to velocity saturation. At low electric field, the electron drift velocity in the channel varies linearly with electric field intensity. However, after a certain point, it increases more slowly and then attains saturation. The drain current in the MOSFET is limited by velocity saturation, instead of pinch off. This is a result of device scaling wherein the device dimensions are scaled down without decreasing the bias voltages.

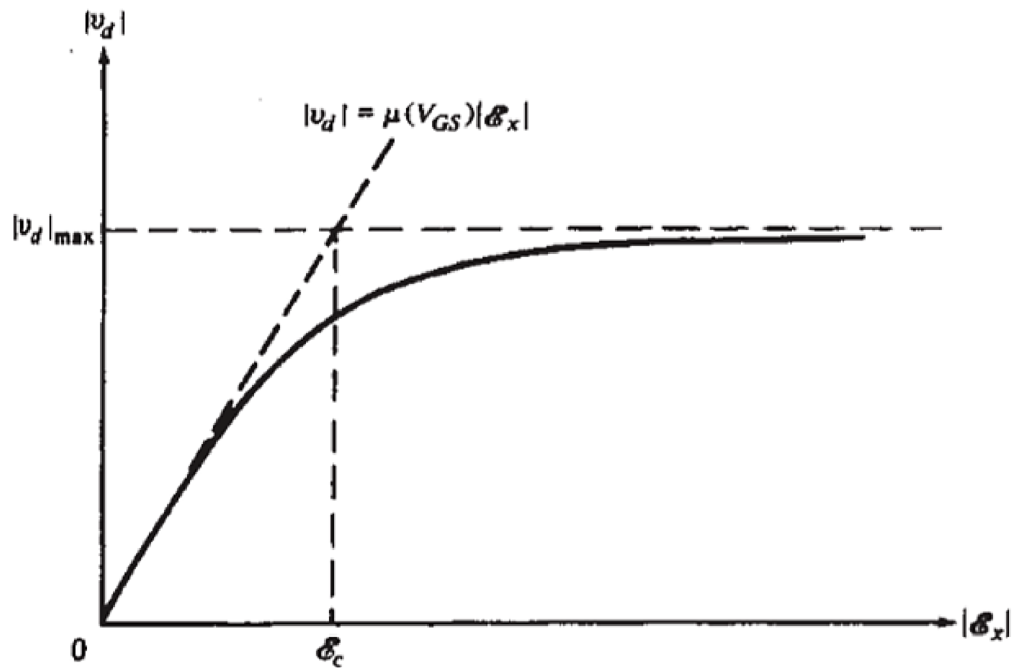


Figure 1.3 Magnitude of carrier velocity in inversion layer vs. magnitude of longitudinal component of electric field [5].

7. Oxide Leakages: These are caused within the device through gate to the substrate due to reduced gate oxide thickness. If oxide thickness is reduced up to 2nm then the effect is more prominent. Electrons start tunneling through the gate to substrate. Oxide leakages results in higher power dissipation in the device. These leakages can be reduced by using high k dielectric material for gate terminal.

8. Gate Induced Drain Leakage (GIDL): With the scaling and increased voltages, electric field at drain overlap becomes extremely high [4]. This increased electric field results in depletion of carriers into drain overlap region. The valence band of gate and conduction band of drain region overlaps. This overlapping results in band to band tunneling of electrons from gate to drain.

1.5 TECHNOLOGY TO OVERCOME CHALLENGES IMPOSED DUE TO SCALING

To overcome challenges imposed by scaling the complexity in fabrication of conventional MOSFET is increased due to incorporation of techniques called strained silicon, epitaxial layer formation, isolation techniques etc. Alternate approaches such as SOI MOSFETs, tunnel FETs, FINFETs, and many other unconventional techniques are used to overcome scaling issues. Among all junctionless field effect transistors can be used in place of conventional MOSFETs.

1.5.1 JUNCTIONLESS TRANSISTORS

The active elements in a conventional bulk-silicon circuit, the devices are separated by the depletion layer formed in between them. This depletion layer is formed due to the presence of PN junction and it results in leakage currents in the device. These temperature dependent leakage currents and thus increase exponentially with temperature. This is responsible for giving serious reliability issues to the device. Excessive leakage currents result in high power dissipation and thus limit the operation of these devices at high temperatures. Latch up conditions caused in the insulating tubes of the neighboring transistors due to formation of parasitic transistors significantly degrade the performance of these devices. To reduce these short channel effects to significant extent, a new device structure called a Junctionless (JL) Transistor has been introduced.

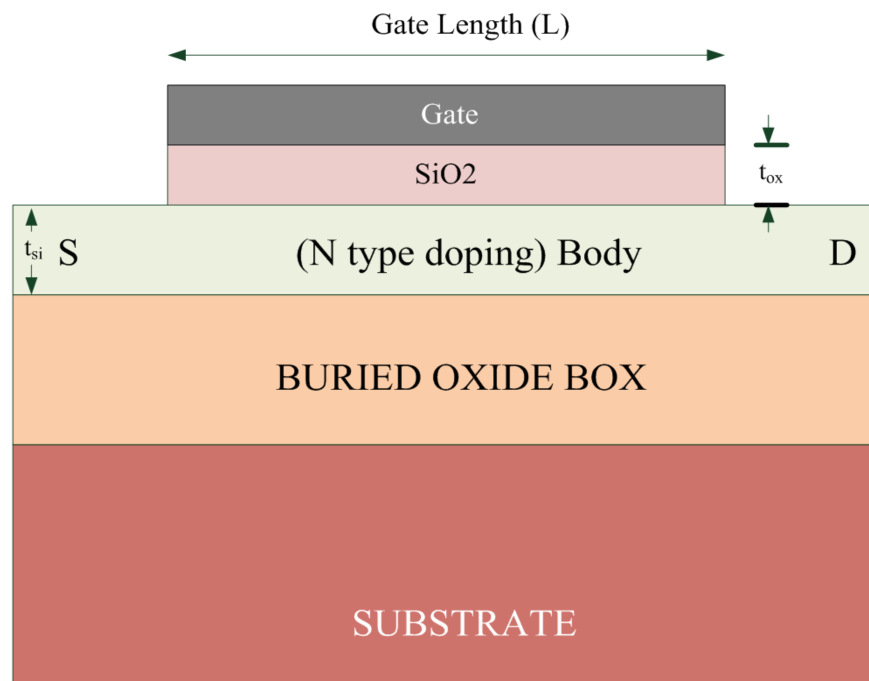


Figure 1.4 Schematic of an SOI junctionless transistor.

A junctionless device with uniform doping concentration and type throughout the channel and source/drain extensions overcomes the challenges faced by conventional nano-devices [**6**]. Junctionless Transistors (JLTs) have high doping in the channel region because of which they are completely depleted in the OFF state. In JLTs a gate metal with high work function difference to that of the channel is required. Biasing needs to be done on gate so as to bring the channel out of depletion such that there is conduction between the source and the drain. A single semiconducting bar with uniform doping is present between the source and the channel. It can be modelled as a resistor whose resistance can be controlled by the gate. The doping of the semiconductor bar needs to be very high to ensure reasonable conductance between the source and the drain. The depletion width in a JLT is very small as the doping is very high, an ultra-thin silicon body is required for JLT.

The schematic representation of junctionless transistor is shown in figure 1.7. It can be seen that for an n-channel operation, the source, channel and drain are of n-type doping and the gate is of a p-type work function (5.1eV). Since the workfunction difference between the n-type channel and the p-type gate is of 1eV, which results in depletion of the channel, where the depletion is decided by the doping of the channel region (thin depletion width for high doping and vice-versa). Channel can be made fully depleted by choosing an extremely thin channel and channel doping in the range of 10 nm and 10^{19} cm^{-3} respectively.

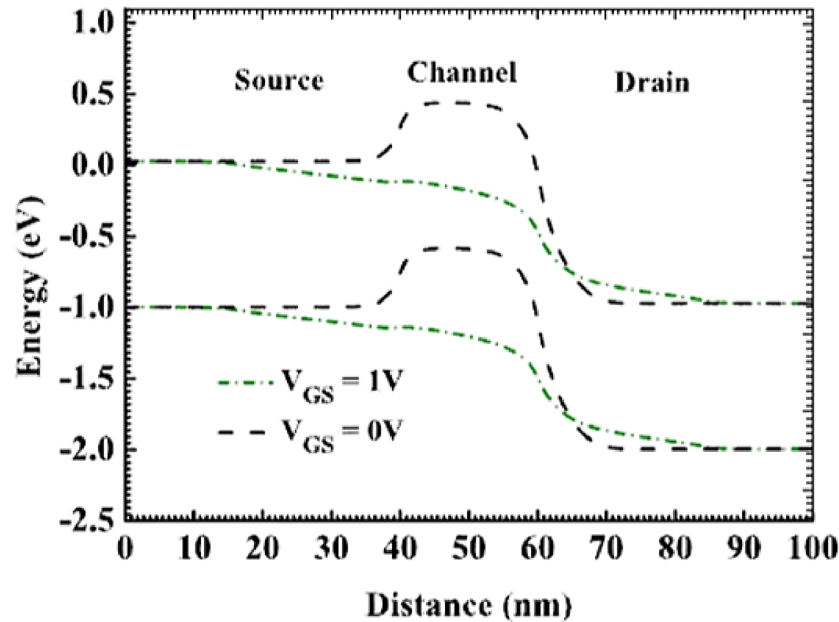


Figure 1.5 Lateral band diagram on JLT both for the ON and OFF states.

Once the channel is fully depleted, the current between the source and drain becomes very small. The current is very small when the gate is at 0V. Also, it can be seen in the band diagram (Figure 1.8) for V_{GS} =0V [14], that there exists a barrier between the source and the channel due to depletion of carriers in the channel. There exists a similar barrier between the source and channel, even in the conventional MOSFET. Once a positive gate bias is applied (note this is for an n-channel operation), the channel is now brought out of depletion and the barrier between the source and channel is reduced. This results in a high drain current for a non-zero drain bias. When the voltage applied at the gate is approximately equal to the workfunction difference between the gate and channel, the device is brought into the flat-band condition and the transistor is said to be turned ON. However, all this is valid when the channel thickness is less than its depletion width, else, the device will not be turn OFF at zero gate bias. For example, if the depletion width calculated is a10nm and the channel thickness is 20nm, the device will conduct due to the drain to source bias, even for a zero gate bias, i.e., the device

cannot be turned OFF. Hence it is important to maintain a very thin semiconductor thickness in junctionless transistors to have proper switching characteristics.

1.5.2 DOUBLE GATE JUNCTIONLESS TRANSISTOR:

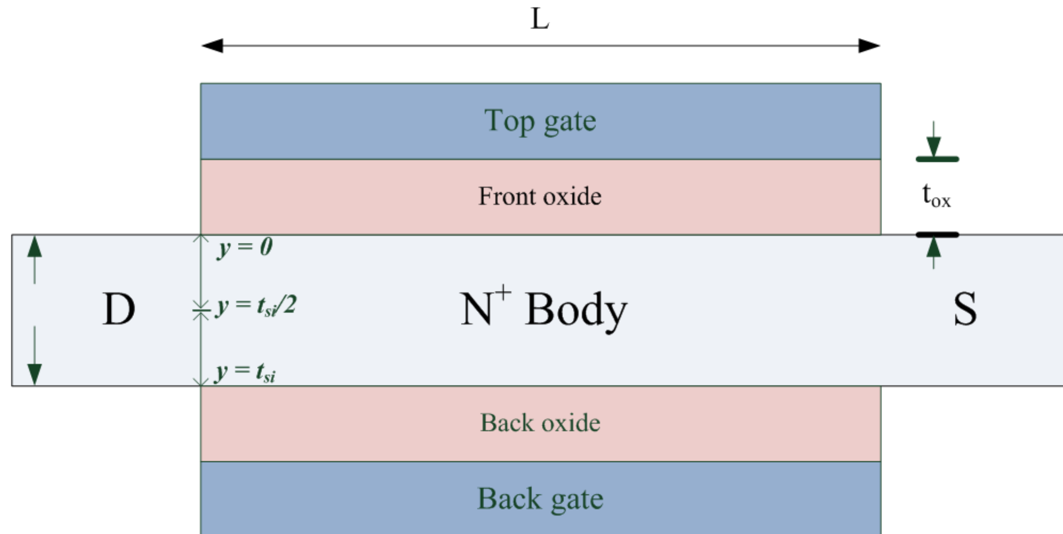


Figure 1.6 Structural view of double gate junctionless MOSFET.

The down scaling of the channel length in MOSFETs poses increasingly difficult challenges as leakage current and short-channel effects increase due to the decreasing control efficiency of the gate on the channel. In a Mu-GFET, the gate electrode is wrapped around a silicon nanowire, forming a multigate structure with excellent control of the channel potential, which allows one to fully deplete the channel region. In very short-channel devices, the formation of ultra-sharp source and drain junctions is quite a challenge and imposes drastic conditions on doping techniques and thermal budget. The JL transistor is a resistor with uniform doping. The doping concentration is constant through the source, channel, and drain. The absence of doping concentration gradient eliminates diffusion of impurities and the problem of sharp doping profile formation altogether. Any increase of temperature induces variations of the electrical parameters of MOS devices (e.g., threshold voltage shift, increase of leakage current, and reduction of mobility). Recently, a double-gate (DG) junctionless (JL) field effect transistor (DG JL FET) has been reported as a promising candidate for future technology nodes. Technically, all undoped or lightly counter-doped DG MOSFETs are junctionless if the doping in the channel is of the same type as the source and the drain. What distinguishes the recently developed junctionless MOSFET is that the channel is heavily doped of the same type and to a similar magnitude of concentration as the source and the drain. The fabricated junctionless device with a high content of impurity concentration within the channel and source/drain (S/D) regions requires no junctions and exhibits many advantages, such as the simplified flexible fabrication process, nearly ideal subthreshold slope ($SS \approx 60$ mV/decade), high ON–OFF current ratio

($I_{ON}/I_{OFF} > 10^7$), low S/D series resistance, and small drain induced barrier lowering. Moreover, the JL transistor shows many interesting characteristics, like conductance oscillations at low temperature and high temperature behavior.

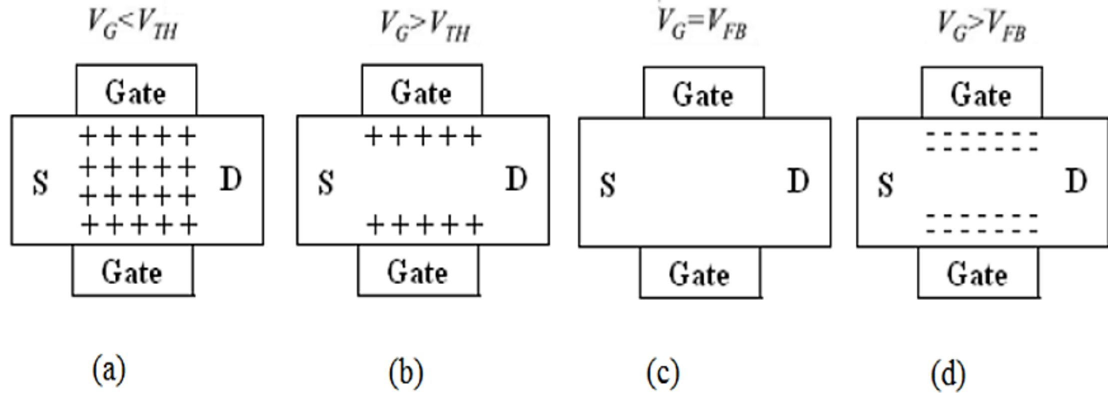


Figure 1.7 a) Fully depleted channel in subthreshold regime, b) semi depleted channel in bulk conduction mode, c) Flat band mode, d) Accumulation mode.

The junctionless transistor (JLT) is a heavily-doped SOI resistor with an MOS gate that controls current flow. Doping concentration is constant and uniform throughout the device and typically ranges from 10^{19} and 10^{20} cm-3.aThe device features bulk conduction instead of surface channel conduction. Figure 1.9 shows the device structure of the double gate junctionless MOSFET. The operational principle of an n-channel DG JL FET is different from that of a standard n-channel DG FET. In the subthreshold region [see Figure 1.7 (a)], a highly doped channel is fully depleted; hence, it can hold a large electric field. By increasing gate voltage, the electric field in the channel reduces until a neutral region is created in the center of the channel. At this point, it is possible to define threshold voltage because bulk current starts to flow through the center of the channel [see Figure 1.7 (b)]. Then, by further increasing the gate voltage, depletion width reduces until a completely neutral channel is created [see Figure 1.7 (c)]. This occurs when the gate voltage equals flat band voltage. At the onset of this condition, the bulk current reaches its maximum value. Thereafter, by increasing the gate voltage further, negative charges accumulate on the surfaces of the channel [see Figure 1.7 (d)]. These charges result in surface current, which is similar to the current in a standard n-channel DG FET. However, the surface current lows at a gate voltage that is much higher than the threshold voltage for the bulk current. Hence, the bulk current drives the total current in the JL transistors.

Additionally, in contrast to the regular junction-based devices, the principle of operation of junctionless DG MOSFETs is based on a current flow in the volume of the silicon layer instead of at the Si–SiO_2 interface. Ideally, the channel doping density of DG JL MOSFETs should be quite high to drive high current densities. On the other hand, turning OFF the device also needs to fully deplete

the channel of mobile charges, which can be difficult if the doping concentration is exceedingly large. (Recently, such an argument regarding full depletion is also used to justify that SiO2 scaling in DG JL MOSFETs should follow almost the same trend as in bulk DG MOSFETs). For instance, considering an n-type doped channel, if the silicon layer is too highly doped and/or too thick, it may be unfeasible to fully deplete the channel from electrons, even for the lowest gate voltage that the device can bear. Depending on the technological parameters, a hole inversion layer can also build up at the channel interface, further screening the gate electric field and preventing depletion of electrons at the center of the channel. Recently, this hypo dissertation is experimentally verified. Therefore, above a certain doping density and silicon thickness, what ultimately limits channel depletion and OFF-state current density is the inherent inverted hole layer at the Si– SiO_2 interface. Preliminary studies are attempted to evaluate the performance of DG JL MOSFET integrated on bulk substrate; however, key relationships to investigate the design space of DG JL MOSFETs are still missing today.

1.6 INTRODUCTION TO DEVICE MODELLING:

There has been rapid development in the field of device modelling in the last two decades. For better performance, the operation and optimization of semiconductor circuits needs to be understood. Device modelling helps in understanding the device behavior to improve the performance on a larger scale. With the decreasing device dimensions, the device behavior starts drifting away from the expected behavior. Device modelling then plays a crucial role in identifying the device behavior of such devices. Device modelling can be broadly classified into two types, physical model and equivalent circuit model. Physical model is based on the physics of the device operation whereas circuit model incorporates the electrical characteristics of the device. The analysis requirements for physical models are normally satisfied using numerical techniques implemented on computers. Physical device models are solved using either bulk carrier transport equations (the semiconductor equations), solutions to the Boltzmann transport equation or quantum transport concepts. Historically, bulk transport solutions have satisfied most device models, whilst Boltzmann and quantum transport solutions have provided a strong insight into the detailed device physics. However, the trend towards very small geometry devices, operating in the hot electron range, means that non-equilibrium transport conditions must be accounted for and the importance of the latter two techniques has become more significant.

1.6.1 STANDARD MOSFET MODELS

Some semiconductor industry standard compact models, such as charge, potential and conductance based models are given below:

1. Charge based MOSFET model: The charge based modeling approach is one of the basic and primitive modeling approaches. It is based on the computation of the inversion charge density in the MOSFET channel in terms of the terminal voltages, i.e. gate and drain voltages. This model is a regional model because it explains the behavior of the MOSFET separately in all regions of its operation. So, these models require smoothing parameters, they are somewhat empirical in the interfacing regions and, thus the device is not described accurately. The prominent charge based models are level 1, level 2, and level 3, BSIM 1, HSPICE level 28, BSIM 2, BSIM 3, BSIM 4, and BSIM 5. BSIM 5 is used for sub100nm CMOS circuit simulation. This model is applicable to deep sub-micron region, and attempts have been made to include the modeling of strained silicon technology in the latest spice models. BSIM 4 considers the influence of stress of mobility, velocity saturation, threshold voltage, body effect and DIBL effect. But the equations expressed are mostly empirical and no analytical models have been given.

2. Potential based MOSFET model: This model approach is more accurate than the charge based models. It is based on the calculation of the potential in the channel of a MOSFET to determine the I-V and C-V characteristics. Some of the models based on the approach are SP models by Penn-state University, USA, HISIM (Hiroshima-University, STARC IGFET model) valid down to sub-100nm MOSFETs. This model is applicable to the sub-micron region and attempts have been made to include the modeling of strained silicon technology.

3. Conductance based MOSFET model: This modeling approach is suitable for low power, short channel applications for analog design. It is known as the EKV (Enz-Krummenachar-Vittoz) model, which has been developed by the Swiss Federal Institute of Technology, Switzerland. This model keeps the substrate as the reference rather than the source, as observed in the potential based and charge based models. Due to its complexity, it is much less used for modeling purposes. Moreover, no stress modeling has been done in this model. In all the approaches mentioned above, attempts have been made to model MOSFETs. But most of the models that have been developed are either empirical in nature. Therefore, there is a need for a more physics based approach to accurately explain the behavior of the device [7].

1.7 ORGANIZATION OF THE DISSERTATION WORK

CHAPTER-1 INTRODUCTION: -

This chapter starts from Moore's law and then discusses about scaling in bulk MOSFETs, its challenges and their solution in the form of advance MOSFETs. Then it looks upon the major SCEs in conventional short channel devices.

CHAPTER-2 LITERATURE SURVEY: -

This chapter starts with small introduction about need of DG JL MOSFETs devices and then tells about DG JL MOSFETs, its advantages.

CHAPTER-3 ANALYTICAL MODELLING OF JUNCTIONLESS DOUBLE-GATE MOSFET : -

In this chapter 2D potential function is derived and then a relation between surface potential and gate voltage is obtained for the DG JL MOSFETs in terms of Lambert-W function. Next, these derived expressions are used to model drain current in the subthreshold region.

CHAPTER-4 RESULTS AND DISCUSSION: -

This chapter contains the comparison of the device simulation results of the DG JL MOSFETs from ATLAS tool of silvaco TCAD with the model results.

CHAPTER-5 CONCLUSION AND FUTURE SCOPE: -

A brief conclusion and possible improvements have been discussed in this chapter.

CHAPTER 2

LITERATURE SURVEY

2.1 MOTIVATION

In the following section to get insight about junctionless devices a rigorous literature survey is performed. While analyzing its structure it is clear that there is a significant simplicity when compared to conventional MOSFETs. The fabrication cost is reduced to a much extent due to its single doping profile. Single doping also results in reduced layout design complexity. More over in the absence of junction the short channel effects such as reverse saturation currents, latch up, punch through etc, are diminished to a significant amount. The comparison between junctionless transistor and inversion mode devices shows advantages of junctionless transistors in terms of subthreshold slope and ON/OFF current ratio. Unlike conventional field effect transistors the junctionless transistor's conduction mechanism is based on bulk conduction mode. Further literature study shows that interface charges due to hot carrier injection can modulate threshold voltage in junctionless transistors. Despite of all the advantages over conventional metal oxide field effect transistors, the high doping profile in junctionless transistors can result in lower transconductance (g_m) and lower drive current due to reduction in carrier mobility.

2.2 LITERATURE REVIEW

Jean-Pierrie Colinge (2012), [8] in this paper tells us about the conduction mechanism in different types of FETs such as inversion mode, accumulation mode and junctionless FETs. The short-channel effects in junctionless transistors are reduced due to non-availability of NP, NN^+ and PP^+ junctions. This paper also shows comparison between junctionless and inversion mode transistors. Architecture of junctionless FETs is very simple as compared to conventional FETs.

Table 2.1 Comparison of junctionless FET with inversion mode FET.

Parameters	Junctionless FET	Inversion Mode FET
Subthreshold slope (SS)	92 mV/decade	75 mV/decade
Drain Induced Barrier Lowering (DIBL)	78 mV/V	10 mV/V
ON Current (I_{ON})	1000 μA/μm	1000 μA/μm
Ratio of ON and OFF Currents (I_{ON} /I_{OFF})	5×10^6	5×10^6

Jong-Ho Woo *et al.* (2013), [9] tells us about the effects of hot carrier injection in junctionless FET's threshold voltage. The analytical threshold voltage model is presented for JL double-gate MOSFETs.

This analytical model includes the effect of localized charges. The model is proposed with the help of 2-D Poisson's equation. Gate length is divided into three regions such as i=1,2 and 3. The region 2 is supposed to have interface charges at silicon-oxide interface. A separate threshold voltage equations for all three regions is derived in this work.

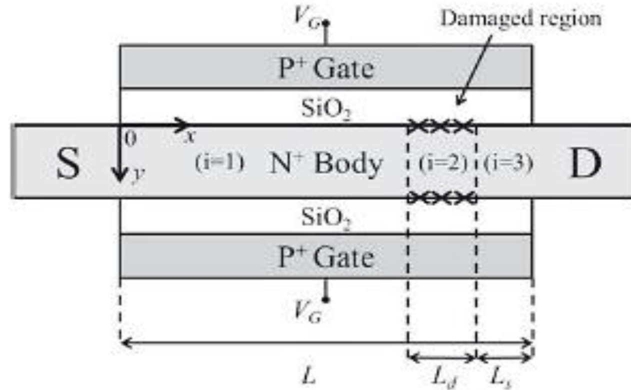


Figure 2.1 Schematic of double gate junctionless field effect transistor [9].

In figure 2.1 schematic of double gate junctionless field effect transistor which is proposed in this paper. L is equal to total gate length, L_d is the damaged region and i=1,2 and 3 represents three regions where i=2 represents damaged region or region with interface charges are present due to hot carrier injection. Atlas 2-D simulation tool is used to verify the proposed model. The parabolic approximation of potential helps us to find the surface potential and body potential and the relationship between them. They have also stated that when there has been minimum surface potential the depletion width at that point has to be maximum i.e $t_{si}/2$.

The boundary conditions used are:

1. The central potential is represented by V_c.

2. Electric flux is continuous between top/bottom and silicon.

3. Electric filed at the centre of body must be equal to zero.

The device is simulated for different lengths of interface charges i.e from 0 to 40 micro meters. Depletion width along the channel is also inspected and difference in the values of damaged and undamaged FET's threshold voltages is investigated for different oxide thickness and different body thickness. The variation in threshold voltage can differ for type of localized charges. Negative charges are more probable to be induced by hot-carrier injection so it can be seen that thin devices are affected more. This work can be used to inspect the effect on threshold voltage caused by localized charges induced by hot-carrier injection.

J.P Colinge *et al.* (2010), [10] present a device which is made using silicon nanowire. This device shows best results when it comes to short channel effect. It has less subthreshold slope, and very low leakage currents. Voltage applied to gate and variation in temperature can cause degradation in mobility of carriers in conventional FETs. Whereas in JNT these degradations are negligible and carriers have ideal mobility. They referred this device as gated resistor as there is no junction and have an either regular doping of N^+ or P^+. The simulation results show nearly ideal CMOS operation by proposed device. Current-Voltage characteristics and output characteristics have been shown in this work which tells that gated resistor is a promising candidate for future CMOS devices in VLSI industry.

Chan-Hoon Park *et al.* (2011), [11] in this work fabricated junctionless nanowire FETs and conventional inversion mode FETs. Then the characteristics at low-frequency for noise and DC analysis are performed on both the devices. The device have gate length 20nm, width=15nm and oxide thickness=5nm.

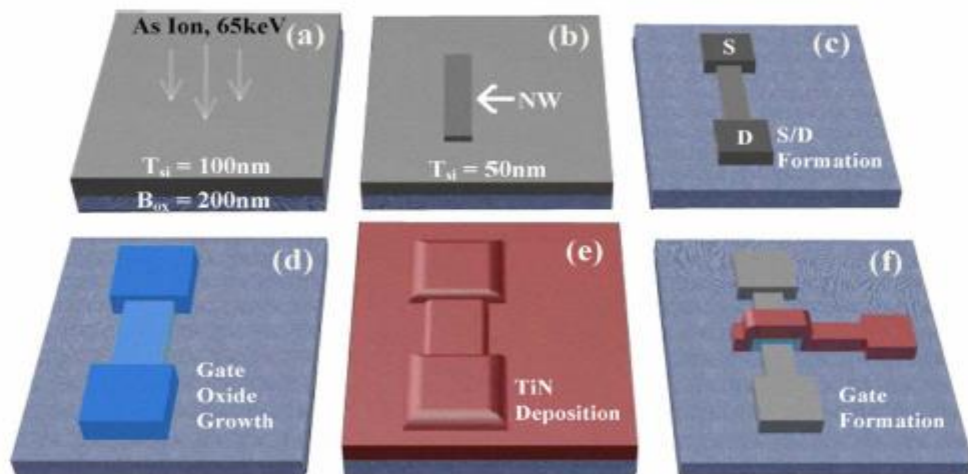


Figure 2.2 Process flow schematic for Junctionless nano-wire transistors [11].

The low-frequency noise characteristics shows that due to higher traps at the interface the junctionless FET shows higher power spectral density as compared to other devices. The author concluded by considering junctionless nanowire FET as a device for future generation. This device at 20nm gate length showed best electrical characteristics and excellent short channel effects and as junction is not required it has a simpler fabrication process. Table 2.2 compares current, subthreshold slope, ON current by OFF current ratio and drain induced barrier lowering in both junctionless nano wire and conventional MOSFETs.

Table 2.2 Comparison of junctionless nanowire FETs with inversion mode FETs

Parameters	Junctionless nanowire FET	Inversion mode FET
I_{ON}	1mA/μm	1mA/μm
I_{ON}/I_{OFF}	$>10^6$	$>10^6$
DIBL	10mV/V	10mV/V
Subthreshold Slope	75m/dec	92mv/dec

J.P Colinge *et al.* (2010), [12] tell us about difference in intensity of vertical electric field in case of junctionless FETs as compared to conventional one. In junctionless transistor the electric-field perpendicular to the flow of carriers is significantly less as compared to conventional MOSFETs. Unlike conventional FETs this reduced vertical field in junctionless transistors doesn't affect the mobility of charged carriers and hence giving them edge in terms of current drive in sub-atomic regime for their complementary MOSFET operations and applications.

Te-Kuang Chiang (2012), [13] in this work author have derived threshold voltage for shot channel junctionless FET based on quasi-2-D scaling equation on bulk conduction mode. Also extended his work to model accumulation operation mode for junctionless FET and inversion operation mode for junction based FET. Junctionless device have shown better performance than junction based device in terms of decreased Drain induced barrier lowering, threshold voltage roll-off and have a decreased sub-threshold swing. When channel length is reduced in order to reduce V_T roll-off, the oxide thickness reduction is best possible option for both junctionless and junction based devices. The threshold voltage can be easily explored using this model and have been verified using 2-D device simulation for double gate junctionless FET due its computation efficiency and simple formulae.

K. Konrad Young (1989), [14] have shown a 2 dimensional analytical model for short channel effects in fully depleted silicon-on-insulator MOSFETs. The lateral field across source and drain is strongly influenced by the vertical field through the depleted film. Further this work shows that by decreasing silicon film thickness the short channel effects can be significantly reduced. The model values and PISCES results are in in accordance with each other. The paper was concluded by saying that the short channel induced threshold voltage reduction in silicon-on-insulator MOSFETs is better than bulk MOSFETs.

Yuh-Sheng Jean *et al.* (1997), [15] have presented an analytical model for threshold voltage of MOSFET in presence of localized charges in silicon and oxide interface. To obtain a simple threshold voltage model, author divided damaged device in three portions. Region 2 is the damaged area with concentration $10^{12}/cm^2$ charges at the interface. Also surface potential is calculated by solving poisson's equation in two dimensions. Analytical surface model is defined by calculating the

minimum surface potential. This model also included substrate bias and DIBL effects. Threshold voltage shift is dominated by the damaged region because this zone is out of influence of screening effect. In conclusion the author claims that 2-D numerical results verified the calculated results of model and they are in quit good agreement.

A. Kranti *et al* (2011), [16] has demonstrated that junctionless FET as compared to conventional FETs have very different physical phenomenon. Here bulk conduction is responsible for flow of carriers in ON state. It acts as variable resistor controlled and modulated by gate electrode. Device is turned OFF by completely depleting the silicon channel heavily doped nanowire. Physics of device is explained which shows how junctionless transistor's electrical characteristics are similar to conventional MOSFETs. The energy band diagram of n-channel junctionless FET in ON state and flat band condition is shown. While describing the conduction mechanism it shows that it works in either full depletion or partial depletion and not in inversion or accumulation. It also shows that width, thickness and doping of nanowire can affect threshold voltage. In Figure 2.3 Electron concentration contour plots in an n-type junctionless transistor. A: V_D = 50 mV, B: V_D = 200 mV; C: V_D = 400 mV, D: V_D = 600 mV where $V_G > V_{TH}$. Device parameters are: L = 40 nm, W_{si} = 20 nm, t_{si} = 10 nm, t_{ox} = 2 nm, $N_D = 10^{19}$ cm^{-3}. Simulation was carried out by solving drift–diffusion, continuity and Poisson's equations.

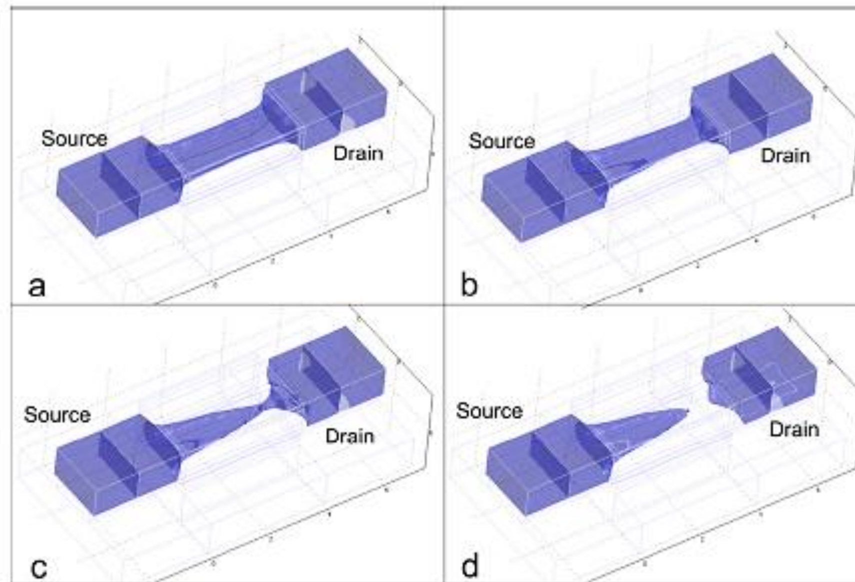


Figure 2.3 Electron concentration contour plots in an n-type junctionless transistor [16].

A. Ortiz-Conde *et al.* (2002), [17] explained different methods of extracting threshold voltage in MOSFETs. Approximately fourteen different methods have been proposed in this paper to extract threshold voltage, eleven of which are measured on linear transfer characteristics, two methods based

on saturation mode operation and one precisely for non-crystalline thin film FETs. The figure 2.4 shows the method known as GMLE which means linear extrapolation of the gm–Vg characteristics at its maximum first derivative (slope) point of the gate voltage axis intercept which give threshold voltage of device in TCAD simulation.

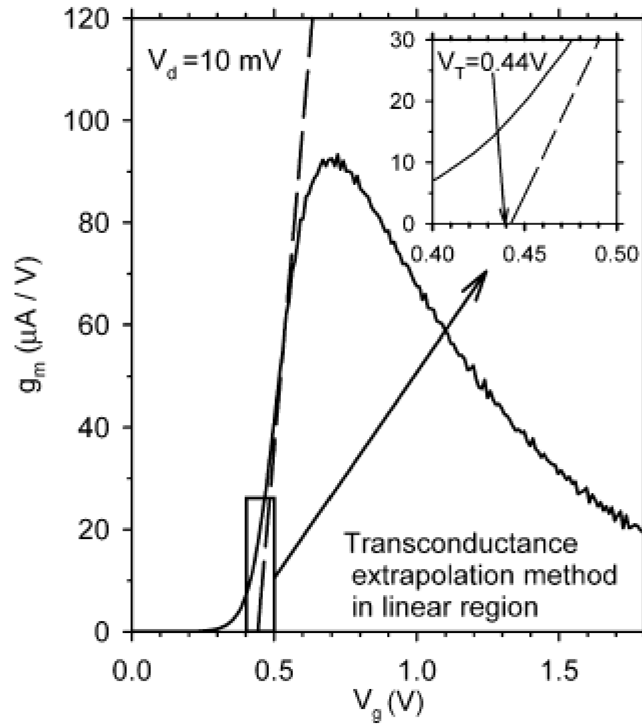


Figure 2.4 Method of calculating threshold voltage by transconductance extrapolation (GMLE) [17].

Zer-Ming Lin *et al.* (2014), [18] talked about subthreshold current and subthreshold swing in double-gated fully-depleted junctionless field effect transistors. In this study by solving two dimensional poisson's equation he derived a model analytically for electric potential. This model can even help in deducing the extent of threshold-voltage roll off. Further the author has shown graphically that how the sub-threshold slope can change with change in gate length. Comparison of analytical model and technology aided simulation results is extensively done for threshold voltage calculation, drain current for different gate voltages, sub-threshold slope and threshold voltage roll-off with drain voltage is done and these comparisons have shown that model is very much in accordance with simulation results.

F. Jazaeri *et al.* (2013), [19] has almost presented a deep insight into junctionless double gate field effect transistor sub-threshold regime. The electrostatic model of FET is presented by solving two dimensional poisson's equation. Further the surface potential differential equation is obtained. Then a relationship between surface potential and central potential is being formulated. Author further added

the detailed analysis of subthreshold slope and its modelling. In figure 2.5 on the left the surface potential and body center potential profile is shown gate length 20nm, whereas on the right these profiles are for gate length equal to 50nm. Considering all voltages zero and doping concentration equal to 10^{19} cm^{-3}.

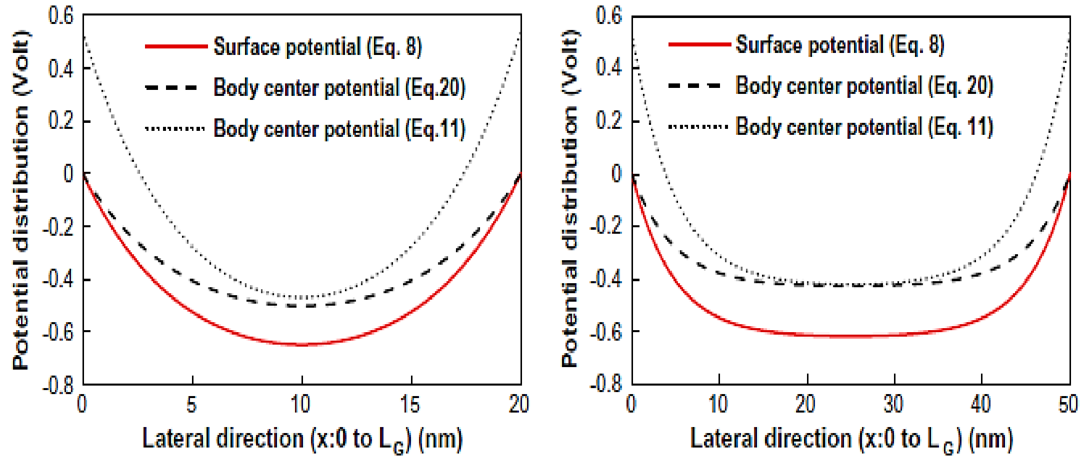


Figure 2.5 Surface potential and central potential along channel [19].

Hongki Kang *et al.* (2008), [20] proposed analytical threshold voltage model with localized-trapped charges for double gate metal-oxide semiconductor. Parabolic potential approximations and two dimensional poisson's equation is used to find threshold voltage. This model is then verified for different device dimensions by using two dimensional device simulations. In figure 2.6 three regions are shown where region1 and region 2 are undamaged whereas region 2 is damaged region due hot-carrier injection.

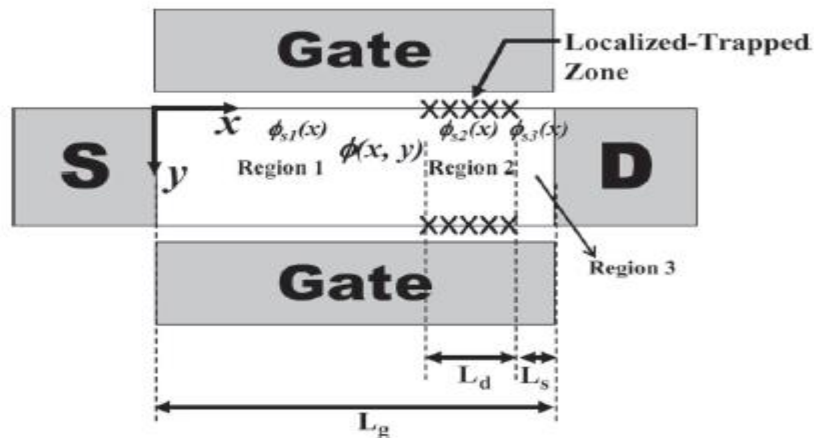


Figure 2.6 Schematic of double-gate metal oxide field effect transistors [20].

Xiaoshi Jin *et al.* (2013), [21] proposed a model which uses variable separable technique to solve two dimensional poisson's equation. Nano-scale double gate device characteristics for sub-threshold operation has been presented in this paper. Asymmetric double gate structures of junctionless transistor's models have been described for nano-scale channel. The front gate back gate differently biased and varying oxide thickness for asymmetric geometry and then behaviour in subthreshold region is plotted. Various parameters like length of channel, thickness of body and body doping are considered.

Renan D. Trevisoli *et al.* (2013), [22] presented tri-gate junctionless field effect transistors. The modelling of tri-gate FET is addressed, while focusing on effects of short channel. Sub-threshold slope, threshold voltage roll-off and DIBL effects are analytically observed. All these effects and characteristics are verified using three dimensional technology aided software. Two dimensional poisson's equation is used to model drain current for tri-gate nano wire junctionless FET. Author have shown and assured that the simulation results and models go hand in hand with each other.

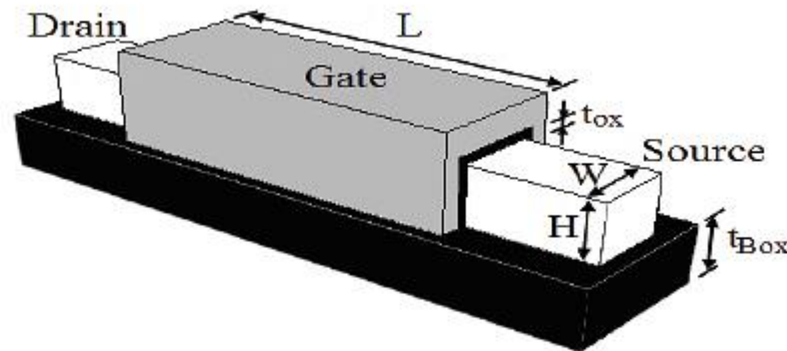


Figure 2.7 The tri-gate junctionless field effect transistor's schematic is shown [22].

Chun-Yu Chen *et al.* (2017), [23] presented a detailed analysis using device simulation on variation in junctionless double gate transistors. When channel length is shrinking less than or up to ten nano meters the threshold voltage is greatly affected. And effect on threshold voltage is very much influenced by its thickness even in the presence of random dopant fluctuation. But further reduction in silicon thickness up to four nano meters or less the effect on threshold voltage is less susceptible on film thickness. Effective film thickness is used to predict the impact on threshold voltage due to variation of film thickness. And reason for less sensitivity on thickness of film may be due to quantum confinement. After presenting the models, the author have shown different characteristics which show relationship between change in threshold voltage with respect to silicon thickness and also on oxide thickness. Threshold voltage contour plot which is having channel thickness in the x axis and channel length in the y axis is shown with drain to source voltage kept at 50mV.

Balraj Singh ***et al.*** **(2017), [24]** presented analytical model in two dimensional poisson's expression of double gate junctionless field effect transistor which is ion implanted for subthreshold swing and subthreshold current. The device shows vertical Gaussian- like doping profile. The effect of all these parameters such as thickness of channel, thickness of oxide, length of channel and peak concentration of doping on subthreshold swing and subthreshold current is shown in detail. In figure 2.8 the result of two dimensional atlas mixed mode simulation for ion implanted double gate junctionless field effect transistor with different straggle parameter at length 30 nm, oxide thickness equal to 1.5 nm and silicon thickness equal to 10nm. On the left the inverter is shown with M1 as load and M2 as driver transistor, whereas on the right the transfer characteristic of inverter is shown.

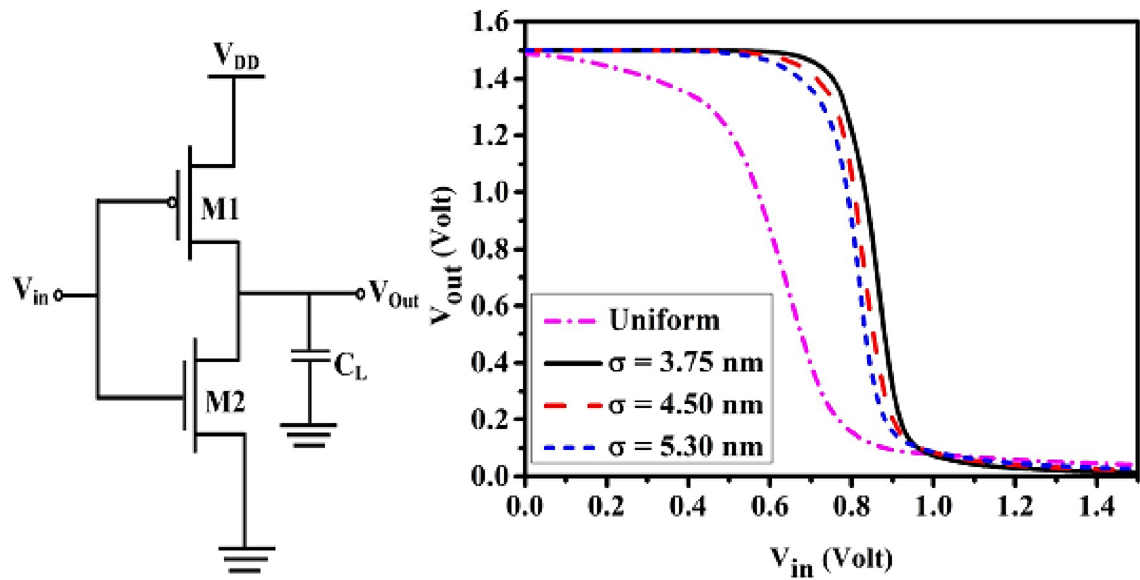


Figure 2.8 Shows the result of two dimensional atlas mixed mode simulation for ion implanted double gate junctionless field effect transistor [24].

Abhinav ***et al.*** **(2017), [25]** at first focused on advantages of junctionless transistors over conventional ones. He then proceeded to say that bulk conduction mechanism is one of the reasons for significantly reduced short channel effects in junctionless devices. The emphasis then shifted to reliability issues of junctionless device. These issues comprised of thermal stability and misalignment effects. The temperature varied from 200k to 500k to test thermal stability. Reduction in current of device is one of the major reliability issue caused by gate misalignments. Back gate and front gate when not properly aligned can produce misalignment effects and hence affecting the performance of device. Shift towards source or drain side in the back gate can cause performance degradation. The radio frequency or analog parameters checked and distortion in linearity has been investigated for different misalignments of gate in junctionless device. Finally results prove that there exists a thermally stable point and device should operate around it for stable operation.

Te-Kuang Chiang *et al.* (2011), [26] has performed three dimensional device simulation to verify the model of surrounding-gate MOSFETs which is comprised of interface charges trapped in silicon and oxide interface. Method used in model is perimeter-weighted-sum and scaling theory for metal oxide semiconductor with gate all around while considering the effects of charges at interface on flat-band voltage. Effects of negative or positive localized charges, thickness of oxide, thickness of silicon and length of channel on threshold voltage is shown.

20. Vikkee *et al.* (2015), [27] presented variable separation method to derive analytical model of JLT. Two dimensional poisson's equation is solved in silicon as well as oxide region to get potential of surface, DIBL and threshold voltage in DGJLT. Sentaurus TCAD is used to verify results of derived equations. Even analytical models are compared with derived model behavior.

2.3 PROBLEM FORMATION & OBJECTIVES

- Formulating analytical model for subthreshold drain current with hot carrier injection for double gate junctionless field effect transistor.

- Analyze effect of doping concentration on subthreshold slope and threshold voltage for oxide thickness less than 2nm.

- Discussion on circuit behavior of double gate junctionless filed effect transistor using mixed-mode simulation.

CHAPTER 3

ANALYTICAL MODELLING OF JUNCTIONLESS DOUBLE-GATE MOSFET

3.1 INTRODUCTION

In long channel MOSFETs the source and drain are very far away from each other due to which the horizontal electric field component can be neglected and only vertical electric field is assumed to be present and hence forth reducing the work to one dimension. Short channel devices on other hand require two dimensional analyses, due to very short spacing between source and drain the effect of lateral electric field component is also significant and should be analyzed while solving poisson's equation. Recently proposed junctionless transistor is one of the worthy candidates to be incorporated in circuits when it comes to short channel device applications. Double-gate junctionless MOSFET are very similar to double-gate conventional MOSFETs except they have same doping profile in source, drain and channel region. In the recent past many advantages of junctionless FETs over inversion-mode FETs have been revealed in many studies. But in spite of all these advantages and better performances the hot carrier effects in junctionless FETs are also associated and analysis on HCE's is required.

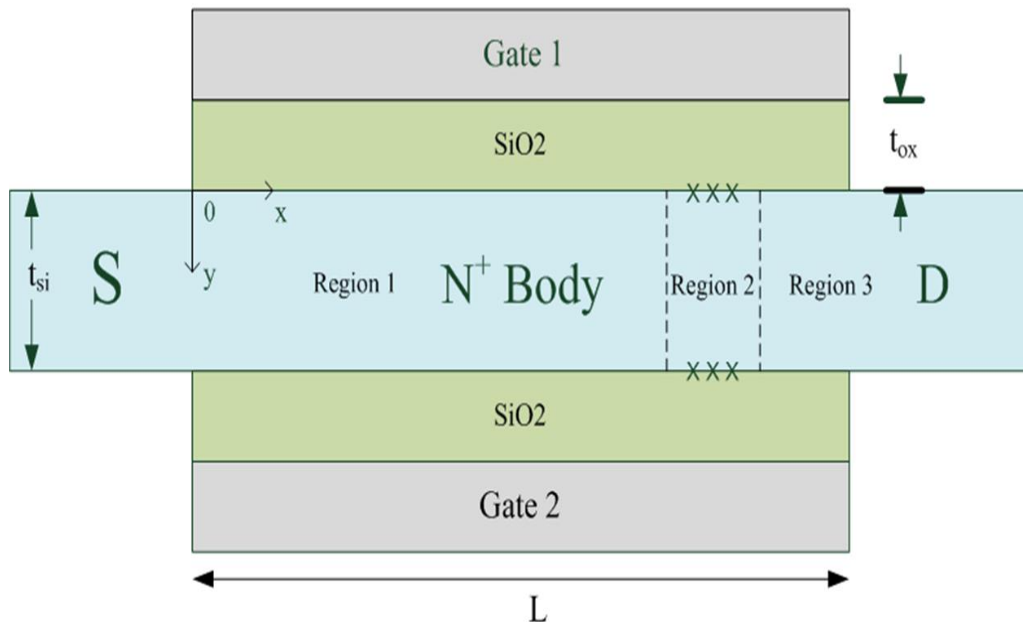


Figure 3.1 Structure and cross-section view of a double-gate JLT with interface charges where 'i' symbolizes damaged or undamaged region.

3.2 DOUBLE-GATE JUNCTIONLESS MOSFET STRUCTURE

Potential distribution in any device could be analyzed and an accurate potential based model could be derived, only if structure of device is thoroughly discussed and studied. In figure 3.1 the structure of double-gate junctionless MOSFET is shown where 'i' symbolizes three regions. Where 'i=1' and 'i=3' represents undamaged regions or regions not affected by hot carrier injection. Whereas 'i=2' represents damaged region or region affected by hot carrier injection or region with interface charges at silicon and dioxide interface. The axis along channel from source to drain is termed as 'x' axis while vertical axis from gate 1 to gate 2 is 'y' axis. The origin of axis is taken at interface point of top oxide and silicon substrate. Gate 1 and gate 2 are two gates top and bottom gates respectively of double-gate junctionless MOSFET. The materials used for making gates of junctionless FETs are usually high work function materials. The P^+ doped polysilicon can also be used as a gate material in these MOSFETs. Reason for using high work function material is the strength of these materials to deplete silicon substrate of its charge carriers due to work function difference. 'L' in the figure 3.1 signifies gate length, 'L_d' the length of damaged region and 'L_s' is the leftover undamaged region at the drain side. The body thickness and oxide thickness is represented by 't_{si}' and 't_{ox}' respectively. Also 'N_D' is the doping concentration of channel, drain and source region.

3.3 POISSON'S EQUATION

Modelling physical behavior of symmetrical double-gate junctionless field effect transistor at sub-nanometer regime, distribution of potential in thin silicon film with respect to different gate and drain bias condition must be analyzed. Unlike single gate MOSFETs, due to presence of two gates the double-gate MOSFETs have very different potential distribution. Maximum potential is at some depth and not at the surface of film. Among many other approaches the depletion approximation for solving poisson's equation is one to determine the potential in double-gate MOSFET silicon film. In the following model description the two dimensional poisson's equation have been used to determine potential distribution. The two dimensional analysis means applying partial double derivative in two dimensions, in this model we have taken 'x' and 'y' directions for describing our model. Poisson's equation is a partial differential equation named after the French mathematician and physicist Simeon-Denis Poisson. Derived from Coulomb's law and Gauss's law, it is a second-order partial differential equation used for solving problems, such as finding the electric potential for a given charge distribution.

$$\nabla^2(V) = \left(\frac{\partial^2 V}{\partial x^2} + \frac{\partial^2 V}{\partial y^2}\right) = -\frac{\rho}{\varepsilon_{si}} \tag{3.1}$$

Where ‘v’ represents potential, ‘x’ and ‘y’ representing two dimensions, ‘ρ’ is the total charge density and ‘ε_{si}’ is the silicon permittivity. Equation (1) is poisson’s equation which describes relationship between charge distribution and double differential of potential distribution.

3.4 CALCULATION OF THRESHOLD VOLTAGE

In figure 3.1 the cross section view of double-gate junctionless MOSFET with interface charges at gate oxide and channel junction. We can also see that silicon film is divided into three regions named i=1, 2 and 3. Region 2 is the one with hot carrier injected localized interface charges.

Approximation says that body potential (represented by Ψ(x, y)) is parabolic along y-axis, i.e

$$\Psi(x, y) = \Psi_s + a_1(x)y + a_2(x)y^2 \tag{3.2}$$

where ‘Ψ_s’ is the surface potential.

Now applying 2-D poisson’s equation in (3.2) we get,

$$\frac{\partial^2 \Psi_s}{\partial x^2} + \frac{\partial^2 a_1}{\partial x^2} y_d + \frac{\partial^2 a_2}{\partial x^2} y_d^2 + 2a_2 = -\frac{qN_D}{\varepsilon_{si}} \tag{3.3}$$

where ‘N_D’ is the silicon film doping concentration and ‘y_d’ is the width of depletion in y-axis. Now applying different boundary conditions such as continuity of electric flux at the interface and applying gauss’s law to the center of the thin silicon film.

1. $\Psi(x, y_d) = V_C$.
2. $\partial\Psi(\mathrm{x},\mathrm{y}) / \partial y|_{y=0} = \frac{C_{ox}}{\varepsilon_{si}}(\Psi_s - V_G + V_{FB})$.
3. $\partial\Psi(\mathrm{x},\mathrm{y}) / \partial y|_{y=tsi/2} = 0.$

After applying these boundary conditions we want ‘a_1’ and ‘a_2’ as functions of ‘y_d’ and ‘Ψ_s’, and where V_C is the potential at the center. By applying first boundary condition in (3.2) we get

$$\Psi_s + a_1(x)y_d + a_2(x)y_d^2 = V_C \tag{3.4}$$

Second boundary condition gives

$$a_1(x) = \frac{C_{ox}}{\varepsilon_{si}}(\Psi_s - V_G + V_{FB}) \tag{3.5}$$

Third boundary condition gives

$$a_2(x) = \frac{-C_{ox}}{t_{si}\varepsilon_{si}}(\Psi_s - V_G + V_{FB}) \tag{3.6}$$

Now substituting (3.4), (3.5), (3.6) in (3.2) we get,

$$\Psi(x,y) = \Psi_s + \left[\frac{C_{ox}}{\varepsilon_{si}}(\Psi_s - V_G + V_{FB})\right] y + \left[\frac{-C_{ox}}{t_{si}\varepsilon_{si}}(\Psi_s - V_G + V_{FB})\right] y^2 \tag{3.7}$$

Applying 2-D poisson's equation in (3.7),

$$\frac{\partial^2 \Psi_s}{\partial x^2} + \frac{\partial^2\left[\frac{C_{ox}}{\varepsilon_{si}}(\Psi_s - V_G + V_{FB})\right]}{\partial x^2} y_d + \frac{\partial^2\left[\frac{-C_{ox}}{t_{si}\varepsilon_{si}}(\Psi_s - V_G + V_{FB})\right]}{\partial x^2} y_d^2 + 2\left[\frac{-C_{ox}}{t_{si}\varepsilon_{si}}(\Psi_s - V_G + V_{FB})\right] = -\frac{qN_D}{\varepsilon_{si}} \tag{3.8}$$

Put $y_d = t_{si}/2$ and differentiating we get

$$\frac{\partial^2 \Psi_s}{\partial x^2}\left[1 + \frac{C_{ox}t_{si}}{4\varepsilon_{si}}\right] = -\frac{qN_D}{\varepsilon_{si}} + \frac{2C_{ox}}{C_{ox}t_{si}}[\Psi_s - V_G + V_{FB}] \tag{3.9}$$

After rearranging the terms in (9)

$$\frac{\partial^2 \Psi_s}{\partial x^2} - \frac{8C_{OX}\Psi_s}{t_{si}(4\varepsilon_{si} + C_{OX}t_{si})} = -\frac{8C_{OX}}{t_{si}(4\varepsilon_{si} + C_{OX}t_{si})}\left[V_G + \frac{qN_D t_{si}}{2C_{OX}} - V_{FBi}\right] \tag{3.10}$$

Assigning symbols and simplifying (3.10) to a standard differential equation

$$\frac{\partial^2 \Psi_s}{\partial x^2} - k^2\Psi_s = -k^2\Psi_i \tag{3.11}$$

where values of k^2 and Ψ_i are as following,

$$\Psi_i = V_G + \frac{qN_D t_{si}}{2C_{OX}} - V_{FBi} \ (i = 1, 2 \text{ and } 3) \tag{3.12}$$

$$k^2 = \frac{8C_{OX}}{t_{si}(4\varepsilon_{si} + C_{OX}t_{si})} \tag{3.13}$$

As we know that three regions are denoted by i = 1, 2 and 3. But for i = 2 flat band voltage,

$$V_{FBi} = V_{FB0} - \frac{qN_x}{C_{ox}} \tag{3.14}$$

Where 'N_x' is the density of trapped charge's at the interface of oxide and silicon film in damaged region. $V_{FBi} = V_{FB0}$ is the flat band voltage for rest two regions i.e. i =1 and 3. It shows how interface trapped charges or localized charges at interface affect threshold voltage of device. The general solution of threshold voltage should include this factor in simplified manner. The general solution of (3.11) is

$$\Psi_{s,i}(x) = b_i e^{kx} + c_i e^{-kx} + \Psi_i \tag{3.15}$$

Now for calculating the values of b_i and c_i we need to apply a boundary condition. We know that electric flux should be continuous at the lateral boundaries in x-axis. These lateral boundaries are source to region 1 (undamaged), region 1 (undamaged) to region 2 (damaged), region 2 (damaged) to region 3 (undamaged) and region 3 (undamaged) to drain region.

$$b_1 = \frac{V_D + \Psi_1(e^{-kL} - 1) + (\Psi_1 - \Psi_2)[\cosh k(L - L_2) - \cosh k(L - L_1)]}{2 \sinh kL} \tag{S1}$$

$$b_2 = \frac{V_D + \Psi_1(e^{-kL} - 1) + (\Psi_1 - \Psi_2)[\cosh k(L - L_2) - e^{-kL} \cosh kL_1]}{2 \sinh kL} \tag{S2}$$

$$b_3 = \frac{V_D + \Psi_1(e^{-kL} - 1) + (\Psi_1 - \Psi_2)e^{-kL}[\cosh kL_2 - \cosh kL_1]}{2 \sinh kL} \tag{S3}$$

$$c_1 = \frac{-V_D - \Psi_1(e^{kL} - 1) - (\Psi_1 - \Psi_2)[\cosh k(L - L_2) - \cosh k(L - L_1)]}{2 \sinh kL} \tag{S4}$$

$$c_2 = \frac{-V_D - \Psi_1(e^{kL} - 1) - (\Psi_1 - \Psi_2)[\cosh k(L - L_2) - e^{kL} \cosh kL_1]}{2 \sinh kL} \tag{S5}$$

$$c_3 = \frac{-V_D - \Psi_1(e^{kL} - 1) - (\Psi_1 - \Psi_2)e^{kL}[\cosh kL_2 - \cosh kL_1]}{2 \sinh kL} \tag{S6}$$

Equation ($S_1 - S_6$) are derived values of b_i and c_i for all values of i = 1, 2 and 3 with the help of above mentioned boundary conditions. Body being heavily doped by n-type doping means our threshold voltage condition will be achieved only when surface potential (Ψ_s) reaches its minimum value and depletion depth (y_d) reaches its maximum value. When surface potential (Ψ_s) is at its minimum value, the channel potential (Ψ_c) is also minimum at $t_{si}/2$ depletion width. Even further, when gate voltage is equal to threshold voltage the minimum channel potential is equal to zero value. In addition, $\frac{\partial \Psi_s}{\partial x} = 0$ when surface potential is at its minimum value and $\Psi_{s,min}$ is calculated by differentiating (3.15) with respect to 'x' gives

$$kb_i e^{kx} - kc_i e^{-kx} = 0$$

Rearranging previous equation gives,

$$\frac{b_i}{c_i} = \frac{e^{kx}}{e^{-kx}} = e^{2kx}$$

Taking natural logarithm to both sides,

$$x = \frac{1}{2k} ln\left(\frac{b_i}{c_i}\right)$$

After inserting the value of x in (3.15) we get,

$$\Psi_{s,\min} = 2\sqrt{b_i c_i} + \Psi_i \tag{3.16}$$

The electric field$(\partial\Psi/\partial y)$ according to gauss law is

$$-\frac{\partial \Psi}{\partial y} = -\frac{qN_D y}{t_{si}\varepsilon_{si}}$$

Integrating Ψ from Ψ_s to V_c and y from 0 to $t_{si}/2$ we get

$$\Psi_{s,\min} = V_C - \frac{qN_D t_{si}^2}{8\varepsilon_{si}} \tag{3.17}$$

By solving (3.12) with (3.16) and (3.17), we obtain an equation for threshold voltage,

$$V_{Ti} = V_{T0} - 2\sqrt{b_i c_i} - \frac{qN_x}{C_{OX}}\delta(i-2) \tag{3.18}$$

$$V_{T0} = V_{FB0} + V_C - \frac{qN_D t_{si}}{2C_{OX}} - \frac{qN_D t_{si}^2}{8\varepsilon_{si}} \tag{3.19}$$

Where $\delta(i-2)$ in (3.18) is an impulse function and its value is 1 for region i=2 and zero for other two regions. Also from (S1) to (S6) it can be seen that b_i and c_i are quadratic functions of threshold voltage Vt_i. We can directly figure out that Ψ_1-Ψ_2 is equivalent to $-\frac{qN_x}{C_{ox}}$ and Ψ_1 is direct sum of V_T with some constants. Therefore following linear equation can be framed

$$\begin{cases} b_1 = \alpha V_T + \beta_1 \\ b_2 = \alpha V_T + \beta_2 \\ b_3 = \alpha V_T + \beta_3 \\ c_1 = \alpha^* V_T + \beta_1^* \\ c_2 = \alpha^* V_T + \beta_1^* \\ c_3 = \alpha^* V_T + \beta_3^* \end{cases} \tag{S7}$$

Comparing (S1) to (S7) we get constants shown in (S7)

$$\begin{bmatrix} \alpha = \dfrac{e^{-kL}-1}{2\sinh kL} \\ \alpha^* = \dfrac{1-e^{kL}}{2\sinh kL} \end{bmatrix} \tag{S8}$$

$$\begin{bmatrix} \beta_1 = \dfrac{V_D + \left(\frac{qN_D t_{si}}{2C_{ox}} - V_{FB0}\right)(e^{-kL}-1) - \frac{qN_x}{C_{ox}}[\cosh k(L-L_2) - \cosh k(L-L_1)]}{2\sinh kL} \\ \beta_2 = \dfrac{V_D + (\frac{qN_D t_{si}}{2C_{ox}} - V_{FB0})(e^{-kL}-1) - \frac{qN_x}{C_{ox}}[\cosh k(L-L_2) - e^{-kL}\cosh kL_1]}{2\sinh kL} \\ \beta_3 = \dfrac{V_D + (\frac{qN_D t_{si}}{2C_{ox}} - V_{FB0})(e^{-kL}-1) - \frac{qN_x}{C_{ox}} e^{-kL}[\cosh kL_2 - \cosh kL_1]}{2\sinh kL} \end{bmatrix} \tag{S9}$$

$$\begin{bmatrix} \beta_1^* = -\left[\dfrac{V_D + \left(\frac{qN_D t_{si}}{2C_{ox}} - V_{FB0}\right)(e^{kL}-1) - \frac{qN_x}{C_{ox}}[\cosh k(L-L_2) - \cosh k(L-L_1)]}{2\sinh kL}\right] \\ \beta_2^* = -\left[\dfrac{V_D + \left(\frac{qN_D t_{si}}{2C_{ox}} - V_{FB0}\right)(e^{kL}-1) - \frac{qN_x}{C_{ox}}[\cosh k(L-L_2) - e^{kL}\cosh kL_1]}{2\sinh kL}\right] \\ \beta_3^* = -\left[\dfrac{V_D + \left(\frac{qN_D t_{si}}{2C_{ox}} - V_{FB0}\right)(e^{kL}-1) - \frac{qN_x}{C_{ox}} e^{kL}[\cosh kL_2 - \cosh kL_1]}{2\sinh kL}\right] \end{bmatrix} \tag{S10}$$

Where L_1 and L_2 are L-L_d-L_s and L-L_s respectively and constant with asterisk sign (*) are obtained by just replacing k with $-k$.

Now after getting all these expressions and their respective constants, we can obtain three quadratic equations for threshold voltage. Maximum value of V_T among three expressions is our device threshold voltage for given device geometry and condition.

$$V_{T1} = \frac{V_{T0} + 2(\alpha\beta_1^* + \alpha^*\beta_1) - \sqrt{[V_{T0} + 2(\alpha\beta_1^* + \alpha^*\beta_1)]^2 - (4\alpha\alpha^* - 1)(4\beta_1\beta_1^* - V_{T0}^2)}}{(1 - 4\alpha\alpha^*)} \qquad (3.20)$$

$$V_{T2} = \frac{V_{T0} - \frac{qN_x}{c_{ox}} + 2(\alpha\beta_2^* + \alpha^*\beta_2) - \sqrt{[V_{T0} - \frac{qN_x}{c_{ox}} + 2(\alpha\beta_2^* + \alpha^*\beta_2)]^2 - (4\alpha\alpha^* - 1)[4\beta_2\beta_2^* - (V_{T0} - \frac{qN_x}{c_{ox}})^2]}}{(1 - 4\alpha\alpha^*)} \qquad (3.21)$$

$$V_{T3} = \frac{V_{T0} + 2(\alpha\beta_3^* + \alpha^*\beta_3) - \sqrt{[V_{T0} + 2(\alpha\beta_3^* + \alpha^*\beta_3)]^2 - (4\alpha\alpha^* - 1)(4\beta_3\beta_3^* - V_{T0}^2)}}{(1 - 4\alpha\alpha^*)} \qquad (3.22)$$

Equation (3.20), (3.21) and (3.22) are threshold voltages of our double-gate junctionless metal oxide semiconductor field effect transistor with hot carrier injected trap charges. The maximum value among these three 'V_T' is threshold voltage at the given conditions.

3.5 SUB-THRESHOLD DRAIN CURRENT MODEL

Considering only the mobile charges, according to the classical model, the Poisson's equation in the channel region of Figure 3.1 is given by:-

$$\frac{d^2\Psi}{dy^2} = \frac{qN_{si}}{\mathcal{E}_{si}}\left[\exp\left(\frac{\Psi - V}{v_{thermal}}\right) - 1\right] \qquad ...(3.23)$$

where Ψ is the electrostatic channel potential, $\mathcal{E}_{si}$ is the silicon permittivity, $v_{thermal}$ is the thermal voltage whose value is given by (kT/q) is approximately equal to 26 mV, V is the quasi-Fermi potential of the electron and q is the electronic charge.

DG JL MOSFET being a majority carrier device, the hole concentration is considered to be negligible compared to that of electrons in the channel with the boundary condition to be considered as

$$\left.\frac{\partial\Psi}{\partial y}\right|_{y=tsi/2} = 0 \tag{3.24}$$

The electric potential at y=0 is given by termed as surface potential (Ψ_s) and the potential at the centre of the film at y = $t_{si}/2$ is denoted by $\Psi_{tsi/2}$.

Integrating (3.23) from $\Psi_{tsi/2}$ to Ψ_s give

$$\frac{\partial\Psi}{\partial y} = \sqrt{\frac{2qN_D v_{thermal}}{\mathcal{E}_{si}}\left[e^{\left(\frac{\Psi_s - V}{v_{thermal}}\right)} - e^{\left(\frac{\Psi_{tsi/2} - V}{v_{thermal}}\right)} - \left(\frac{\Psi_s - \Psi_{tsi/2}}{v_{thermal}}\right)\right]} \tag{3.25}$$

Now using Gauss's law, the relation between the surface potential and the gate voltage can be obtained by

$$Q_0 = 2\mathcal{E}_{si}\left.\frac{\partial\Psi}{\partial y}\right|_{y=0,\ tsi} \tag{3.26}$$

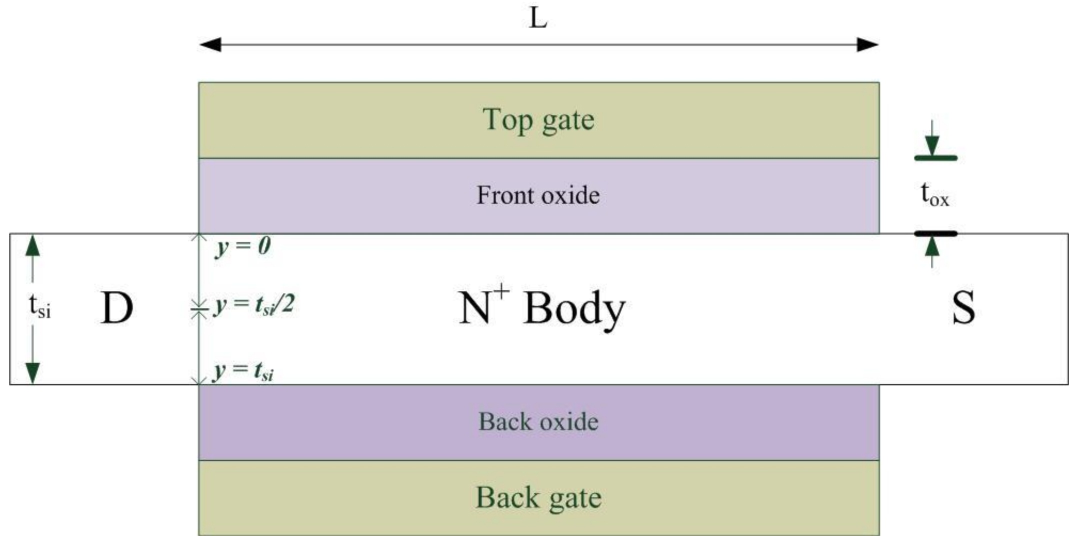


Figure 3.2 Schematic representation of DGJLT.

Where Q_o, the space charge density within limits ($\Psi_{tsi/2}$ to Ψ_s) is given by:

$$Q_0 = -2\mathcal{E}_{si}\frac{\partial\Psi}{\partial y} = -2C_{ox}(V_G - V_{FB} - \Psi_s) \tag{3.27}$$

Where C_{ox} is oxide capacitance, V_G is the gate voltage, V_{FB} is the flat band voltage (V_{FB} is approximately equal to Φ_{ms} the work function difference).

Solving (3.25) and (3.27) we obtain,

$$V_G - V_{FB} - \Psi_s = -\sqrt{\frac{2qN_D\mathcal{E}_{si}\xi v_{thermal}}{C_{ox}^2}\left[1 - \left(e^{\left(\frac{\Psi_{\frac{tsi}{2}}-V}{v_{thermal}}\right)}\right)\left(\frac{1-e^{(-\xi)}}{\xi}\right)\right]} \tag{3.28}$$

Where $\xi = -\left(\frac{\Psi_s - \Psi_{\frac{tsi}{2}}}{v_{thermal}}\right)$, for subthreshold region the term inside the square root $\left(\frac{1-e^{(-\xi)}}{\xi}\right)$ approximately equal to '1',

$$V_G - V_{FB} - \Psi_s = -\sqrt{\frac{2qN_D\mathcal{E}_{si}\xi v_{thermal}}{C_{ox}^2}\left[1 - e^{\left(\frac{\Psi_{\frac{tsi}{2}}-V}{v_{thermal}}\right)}\right]} \tag{3.29}$$

Applying binomial expansion

$$V_G - V_{FB} - \Psi_s = -\sqrt{\frac{2qN_D\mathcal{E}_{si}\xi v_{thermal}}{C_{ox}^2}}\left(1 - \frac{e^{\left(\frac{\Psi_{\frac{tsi}{2}}-V}{v_{thermal}}\right)}}{2}\right) \tag{3.29}$$

Putting the value of ξ in (3.29),

$$V_G - V_{FB} - \Psi_s = -\sqrt{\frac{2qN_D\mathcal{E}_{si}\left(\Psi_{\frac{tsi}{2}} - \Psi_s\right)}{C_{ox}^2}}\left(1 - \frac{e^{\left(\frac{\Psi_{\frac{tsi}{2}}-V}{v_{thermal}}\right)}}{2}\right) \tag{3.30}$$

We know

$$\Psi_{tsi/2} - \Psi_s = \frac{qN_D t_{si}^2}{8\varepsilon_{si}} \tag{3.31}$$

Putting (3.31) in (3.30), we get

$$V_G - V_{FB} - \Psi_s = -\frac{qN_D t_{si}}{2C_{ox}}\left[1 - \frac{e^{\left(\frac{\Psi_{\frac{tsi}{2}}-V}{v_{thermal}}\right)}}{2}\right] \tag{3.32}$$

Also from (3.19),

$$V_{T0} = V_{FB} + V_C - \frac{qN_D t_{si}}{2C_{OX}} - \frac{qN_D t_{si}^2}{8\varepsilon_{si}}$$

$$V_{FB0} = V_{T0} - V_C + \frac{qN_D t_{si}}{2C_{OX}} + \frac{qN_D t_{si}^2}{8\varepsilon_{si}} \tag{3.33}$$

From (3.32) and (3.33) we get the relation between the surface potential and gate voltage for DG JL MOSFET. Expression is further simplified with the help of Lambert-W function.

$$\Psi_s = V_G - V_{T0} - \frac{qN_D t_{si}^2}{8\varepsilon_{si}} - v_{thermal} W[x] \tag{3.34}$$

Where x= $\frac{qN_D t_{si}}{4v_{thermal}C_{ox}}\left(e^{\left(\frac{V_g - V - V_{th}}{v_{thermal}}\right)}\right)$ and W is the Lambert-W function which is defined as the inverse function of $y = xe^x$ [28].

For making relation between current and mobile charges we need to use the gradual channel approximation, the drain current equation can be expressed by Pao-Sah integral as:

$$I_D = -\mu\frac{W}{L}\int_0^{V_D} Q_{mobile}\, dV \tag{3.35}$$

Where $Q_{mobile} = Q_0 - Q_D$ is the mobile charge density, $Q_D = qN_{si}t_{si}$ being the fixed charge density, μ is the carrier mobility which is constant along the channel, W is the width of the DG JL MOSFET and L being the channel length. V_D is the drain voltage with the source voltage assumed to be 0.

Replacing Q_0 from (3.27)

$$I_D = \mu\frac{W}{L}\int_0^{V_D} [2C_{ox}(V_G - V_{FB} - \Psi_s) + Q_D]\, dV \tag{3.36}$$

A compact analytical model for the subthreshold drain current model is developed using the surface potential equation in (3.33).For subthreshold region($V_G < V_{FB}$), the channel of DG JL MOSFET is fully depleted. Differentiating (3.33) with respect to Ψ leads to

$$\frac{dV}{d\Psi} = \left[\frac{1 + W[x]}{W[x]}\right] \tag{3.37}$$

Solving (3.36) we obtain

$$I_D = \mu\frac{W}{L}2C_{ox}v_{thermal}\int_{0}^{V_D} W[x]\, dV \tag{3.38}$$

Using (3.37) in (3.38) we get the subthreshold drain current as:-

$$I_D = \mu\frac{W}{L}2C_{ox}v_{thermal}\int_{\Psi_0}^{\Psi_L} [1 + W[x]\,]d\Psi \tag{3.39}$$

where Ψ_0 and Ψ_L being the surface potential at x=0 and L respectively.

Putting the limits, finally the subthreshold drain current of DG JL MOSFET is obtained as

$$I_D = \mu\frac{W}{L}2C_{ox}(v_{thermal})^2(1 + A)(A - Z) \tag{3.40}$$

where $A = W\left[\frac{qN_D t_{si}}{4v_{thermal}C_{ox}}\left(e^{\left(\frac{V_g - V_{th}}{v_{thermal}}\right)}\right)\right]$ and $Z = W\left[\frac{qN_D t_{si}}{4v_{thermal}C_{ox}}\left(e^{\left(\frac{V_g - V_{th} - V_D}{v_{thermal}}\right)}\right)\right]$

With device dimension scaling, the subthreshold drain current is affected by the short channel effects such as DIBL (Drain Induced Barrier Lowering) and channel length modulation. Some parameters have been incorporated in the drain current model to account for these effects.

A drain voltage dependent parameter αV_D accounting for DIBL is being included in the exponential term of the current model which was previously only gate voltage dependent parameter [29]. The value α of as developed by Meindl and Swanson [30] for bulk MOSFET is being modified for the case of double gate structure by adding an empirical parameter H, thereby modifying the value of α as

$$\alpha = \frac{\mathcal{E}_{si}H}{C_{ox}L} \tag{3.41}$$

The channel length modulation parameter [31] is represented as:-

$$CM = 1 + \left(\frac{\lambda}{L}\right)^{\beta - \sqrt{\frac{\lambda}{L}}}\left(\frac{V_{def}}{V_{gef} - V_{th}}\right) \tag{3.42}$$

Where 'β' is the empirical fitting parameter and $\lambda = \sqrt{\frac{\mathcal{E}_{si}t_{si}}{2C_{ox}}\left(1 + \frac{t_{si}C_{ox}}{4\mathcal{E}_{si}} - \frac{t_{si}C_{ox}}{16\mathcal{E}_{si}}\right)}$ is the natural length [32].

Thus, the modified subthreshold drain current model for DG JL MOSFET is modeled as

$$I_D = \mu \frac{W}{L} 2C_{ox}(v_{thermal})^2(1 + A_1)(A_1 - Z_1)(CM) \tag{3.43}$$

Where $$A_1 = W\left[\frac{qN_D t_{si}}{4v_{thermal}C_{ox}}\left(e^{\left(\frac{\alpha V_D + V_g - V_{th}}{v_{thermal}}\right)}\right)\right]$$

And $$Z_1 = W\left[\frac{qN_D t_{si}}{4v_{thermal}C_{ox}}\left(e^{\left(\frac{\alpha V_D + V_g - V_{th} - V_D}{v_{thermal}}\right)}\right)\right]$$

CHAPTER 4

RESULTS AND DISCUSSION

The results obtained from the modelling of Junctionless double gate MOSFET are being verified using SILVACO TCAD simulation tool. Numerical simulation using ATLAS tool has been performed to validate modelling results for same device. Since we developed a short channel device with thin oxide, due to high electric field density auger recombination model has been used along with Shockley-read hall (SRH) model. CONMOB and Bandgap narrowing (BGN) models have been used for mobility and carrier statistics respectively. The Bohm Quantum Potential (BQP.N) model has also been used to monitor quantum effects of electrons. The FNORD and HEI (HHI) models has been incorporated for modelling gate current and hot electron injection (hot hole injection). Block Newton method solves the equations and parameters associated with these algorithms. The transfer characteristics of the developed device is obtained for channel length L = 40 nm and width as W = 50 nm. The effective mobility for simplicity is considered to be 500 cm2/Vs with the assumption that the carrier mobility is constant throughout the channel and the velocity saturation effect is neglected. The gate work function is considered to be 5.4 eV. An n-type uniform channel doping for the DG JL MOSFET is considered as $N_{si} = 10^{19}$ cm^{-3} and other device parameters such as oxide thickness and

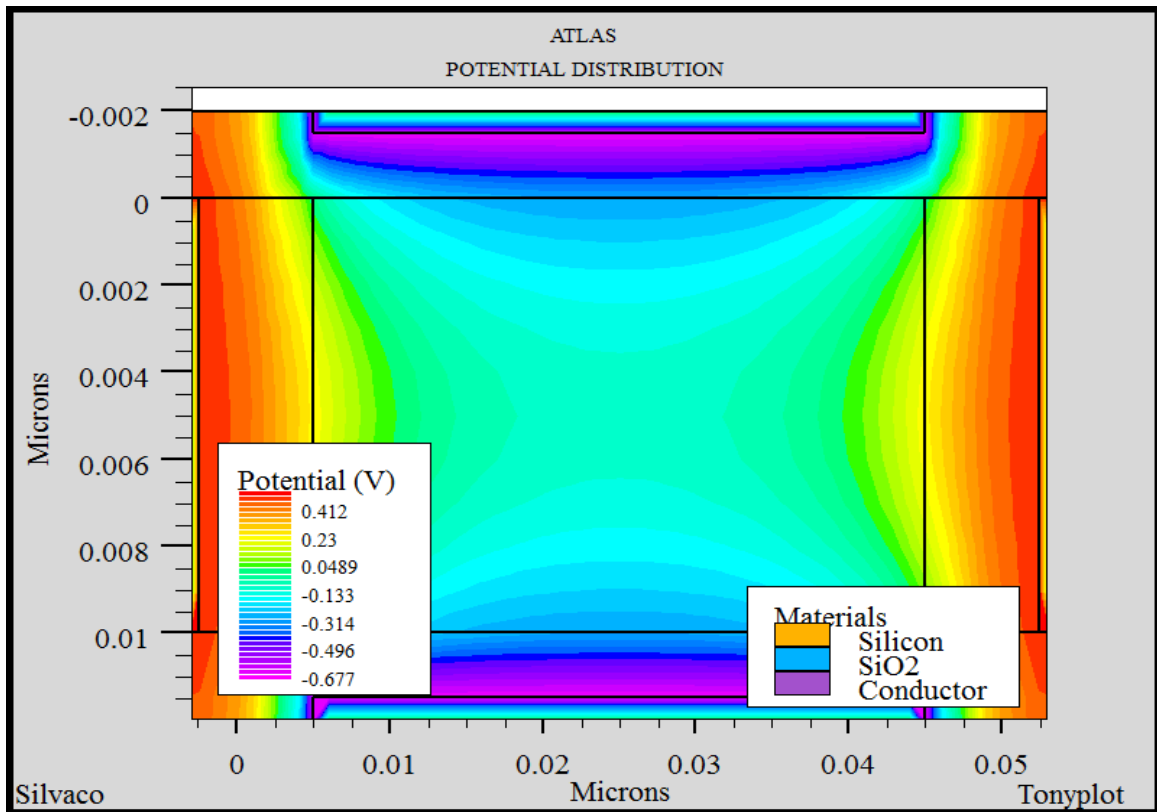


Figure 4.1 Structure with Potential profile of DG JLT MOSFET with L=40nm.

silicon film thickness is considered as t_{ox} = 1.5 nm and t_{si} = 10 nm respectively. These device parameters are considered throughout the simulation process for DG JL MOSFET.

4.1 POTENTIAL DISTRIBUTION

Figure 4.1 shows structure and potential distribution of proposed device. The doping profile of proposed structure is similar in drain, source and channel region which is represented by N_D (N_D=10^{19}).

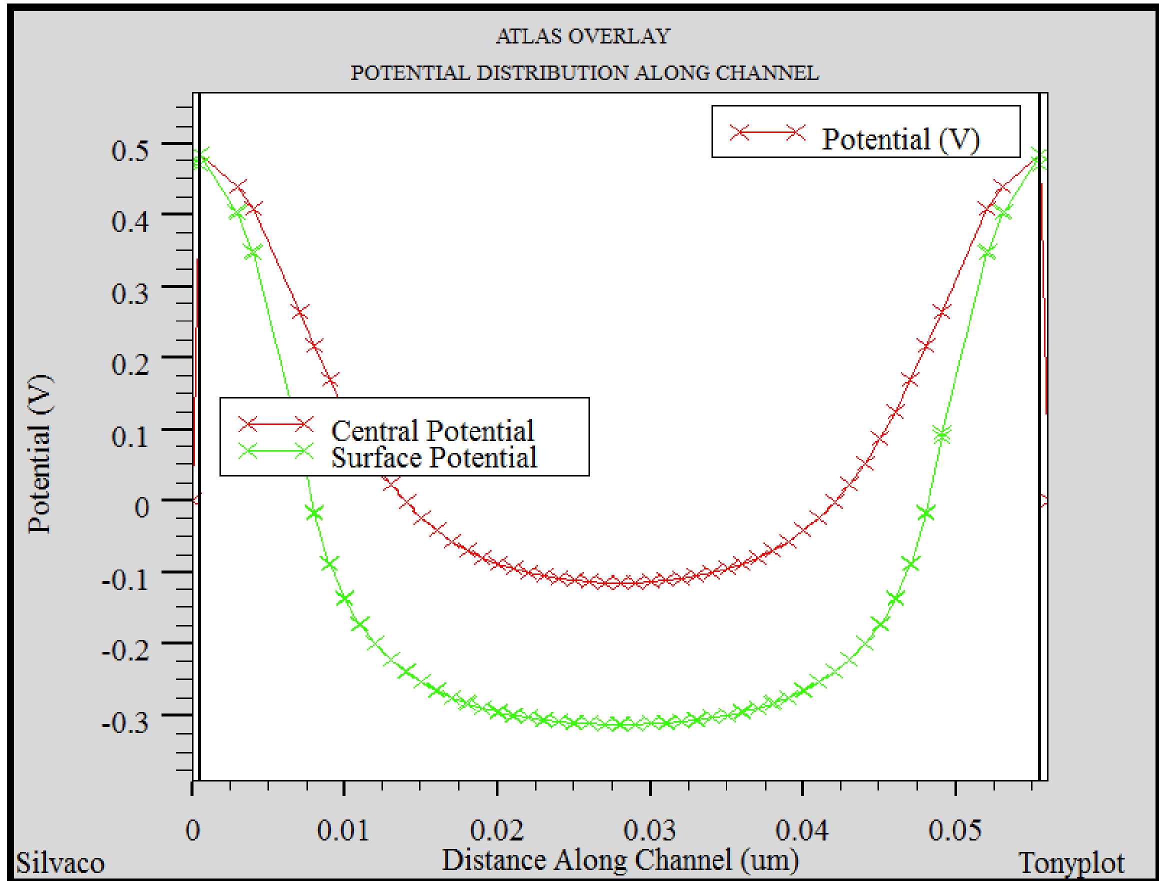


Figure 4.2 Potential distribution along channel for DG JLT MOSFET for bias voltages kept at 0V.

The central potential and surface potential with respect to channel length is represented in figure 4.3. With the help of cutline at the center and surface along channel of device structure, we get potential distribution curve. Bias voltages are kept at ‘0’ volts to plot potential distribution curve in figure 4.2.

4.2 SURFACE POTENTIAL VARIATION WITH GATE VOLTAGE

Figure 4.3 shows the relationship between surface potential and gate voltage gate voltage for JL MOSFET with quasi-Fermi potential V = 0. The model is found to be in good agreement with the TCAD simulation results.

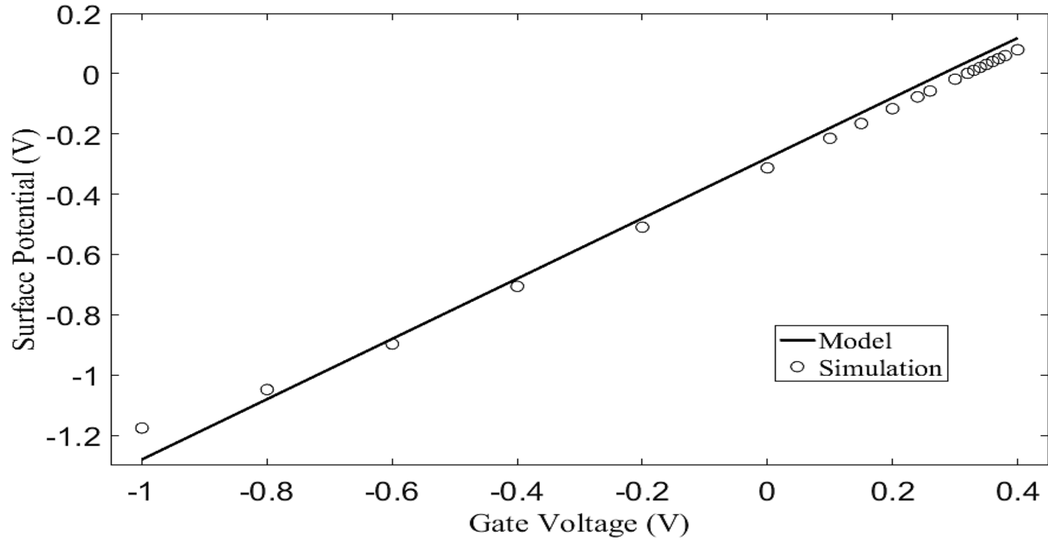


Figure 4.3 Surface potential variation with gate voltage for DG JL MOSFET for quasi- Fermi potential V = 0.

4.3 THRESHOLD VOLTAGE

Figure 4.4 represents change in threshold voltage caused by localized charges dispersed in length L_D with concentration of localized charges N_x ($N_x = \pm 10^{12}$ cm^{-2}).

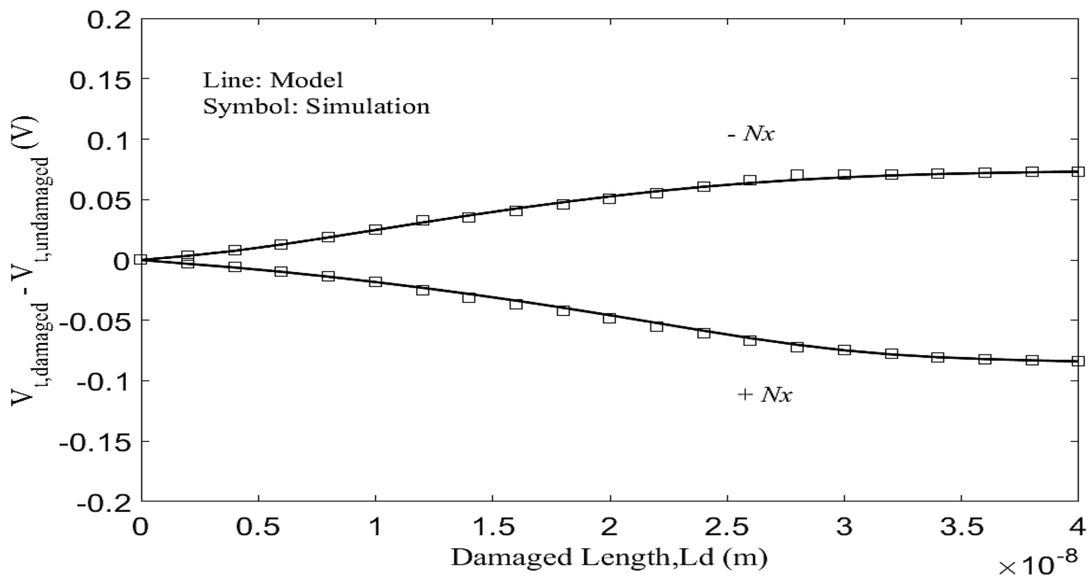


Figure 4.4 Threshold voltage difference for the damaged lengths.

The channel thickness t_{si} =10 nm, doping concentration N_D = 10^{19} cm^{-3}, oxide thickness t_{ox} =1.5 nm and channel length L = 40 nm. These localized charges are formed due to hot carrier injection at silicon film and oxide interface. When interface charges constitute of electrons then concentration of interface charges N_x is taken as -10^{12} cm^{-2}, similarly for holes N_x is equivalent to 10^{12} cm^{-2}. From figure 4.5 it can be seen that $-N_x$ will increase the threshold voltage while $+N_x$ will decrease threshold voltage. The effect of interface charges in TCAD simulation has been monitored by using the following command where, 'QF' represents concentration of trap charges. Different values of threshold voltage are obtained by changing value of 'x.min' in each simulation. Equation (3.21), (3.22) and (3.23) gives three threshold voltages and largest among them represents threshold voltage of device. Figure 4.4 clearly shows that model and simulation results are in accordance with each other.

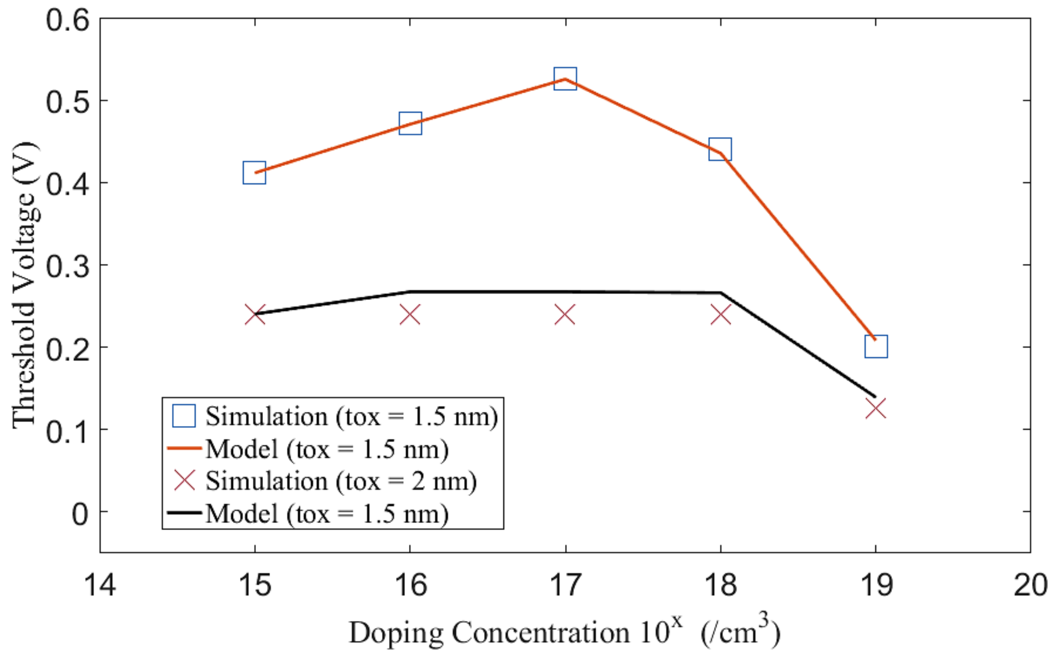


Figure 4.5 Variation of threshold voltage with change in doping concentration of silicon film in DG-JLT for t_{ox}= 1.5 and 2 nm.

Figure 4.5 shows change in threshold voltage when doping concentration of DG-JLT is varied from 10^{15} cm^{-3} to 10^{19} cm^{-3}. The fitting parameter used in figure 4.5 is represented by 'D'. Where, 'D' can be varied from 0.563574 to 0.732664 in the case of different oxide thickness.

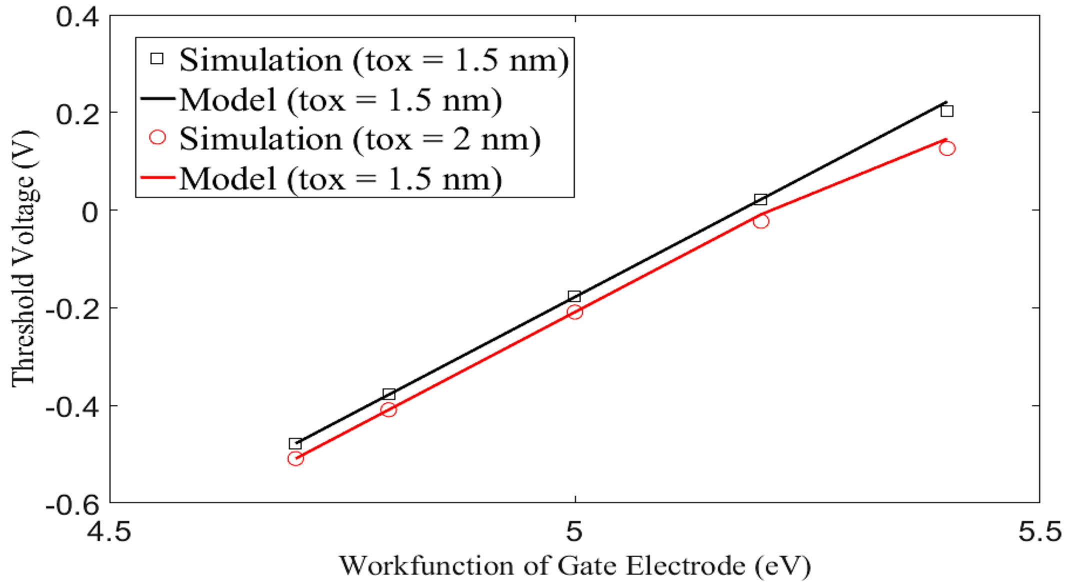


Figure 4.6 Variation of threshold voltage with change in workfunction of gate electrode material in DG-JLT for t_{ox}= 1.5 and 2 nm.

In figure 4.6 the impact of workfunction difference on threshold voltage is shown for work function varied from 4.7 eV to 5.4 eV. The fitting parameter used in figure 4.6 is represented by 'X'. Where, 'X' can be varied from 0.36 to 0.44 to make model in accordance with simulation results for different oxide thickness.

4.4 SUBTHRESHOLD DRAIN CURRENT

Figure 4.7 (a) and 4.7 (b) represents the transfer characteristics of the DG JL MOSFET in the subthreshold region for V_D = 1 V and V_S = 0 V. The fitting parameter values considered for the drain

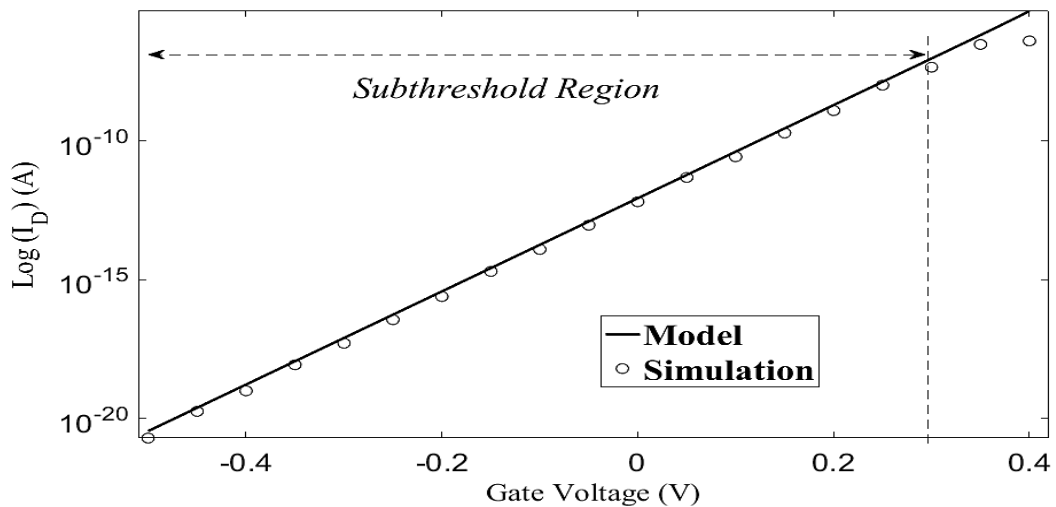


Figure 4.7 (a) Transfer characteristics for symmetrical DG JL MOSFET in logarithmic scale for the developed model compared with simulation (symbols) results.

current model are H = 0.4 and β = 1 where the value of can be any value from 0.6 to 1.2. The figures represent the subthreshold region drain current in both logarithmic and linear scale respectively. From both the figures it is clearly observable that the developed model and the simulation results are in good agreement with each other for the subthreshold region ($V_G < V_{th}$) and deviates after that.

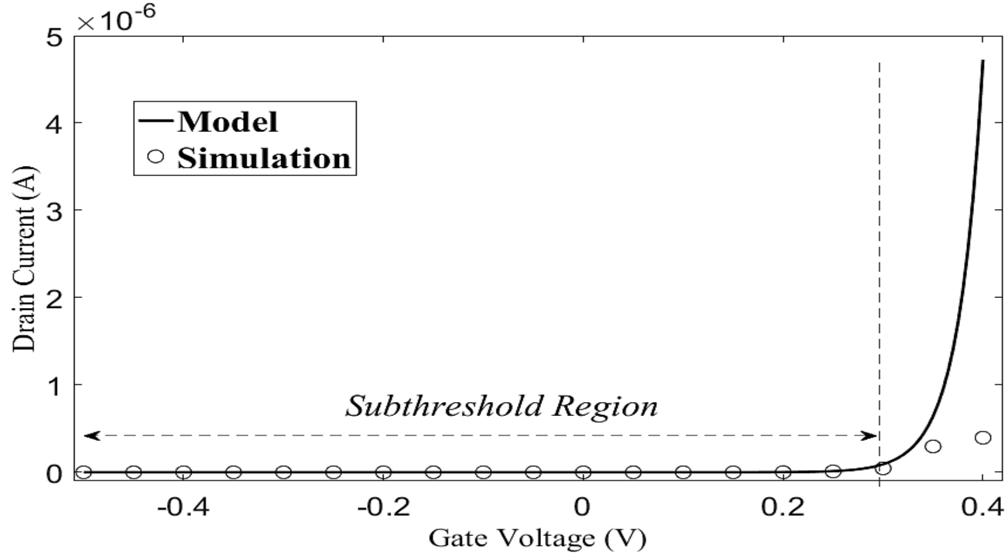


Figure 4.7 (b) Transfer characteristics for symmetrical DG JL MOSFET in linear scale for the developed model compared with simulation (symbols) results.

From figure 4.7(a) we can get the value of I_{ON} / I_{OFF} approximately more than or equal to 10^{10}. This ratio of on current and off current is favorable for device application in low power design for short channel devices.

4.5 SUBTHRESHOLD SLOPE

In table 4.1(a) and 4.1(b) subthreshold slope of double gate junctionless metal oxide semiconductor is shown with change in workfunction and doping concentration.

Table 4.1 (a) Variation of subthreshold slope due to change in workfunction of gate material

Workfunction of Gate Electrode (eV)	Subthreshold Slope (mV/decade) for Oxide Thickness, ‘t_{ox}’ = 1.5 nm	Subthreshold Slope (mV/decade) for Oxide Thickness, ‘t_{ox}’ = 2 nm
4.7	244.512	418.597
4.8	131.317	280.875
5.0	65.669	88.6573
5.2	63.4922	64.2934
5.4	63.17	63.0884

Table 4.1 (b) Variation of subthreshold slope due to changes in doping concentration of DG-JLT

Doping Concentration, N_D (cm^{-3})	Subthreshold Slope (mV/decade) for Oxide Thickness, 't_{ox}' = 1.5 nm	Subthreshold Slope (mV/decade) for Oxide Thickness, 't_{ox}' = 2 nm
10^{15}	60.0989	62.3097
10^{16}	60.5944	62.1779
10^{17}	61.1623	62.1879
10^{18}	62.4188	62.4468
10^{19}	63.17	63.0884

From table 4.1(a) it is clear that with increase in workfunction of gate material the subthreshold slope of DG-JLT decreases for both 1.5 nm and 2 nm oxide thickness. So, these results show that we should prefer higher workfunction materials for junctionless FETs in order to reduce static power dissipation. Table 4.1(b) shows that with the increase in doping concentration of DG-JLT the subthreshold slope increases.

4.6 OUTPUT CHARACTERISTICS OF DG-JLT

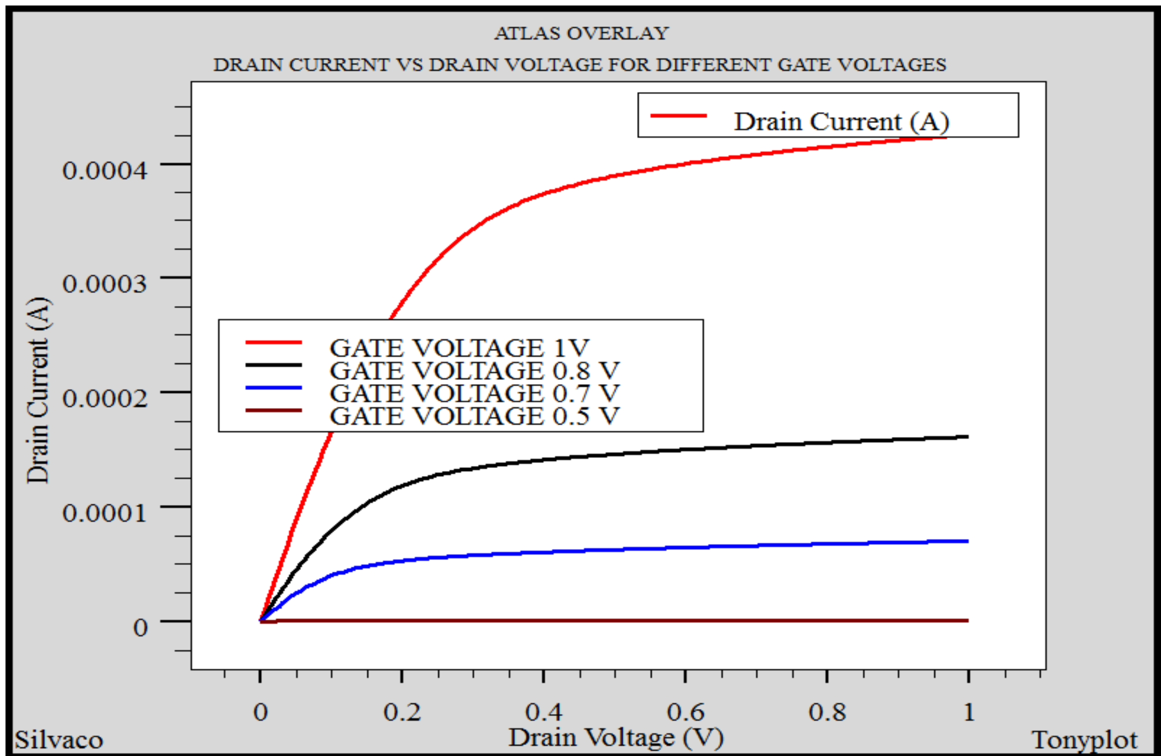


Figure 4.8 Output characteristics of DG-JLT for different values of gate voltage.

Figure 4.8 shows change in drain current for different values of drain voltage by keeping gate voltage at some constant value. These characteristics are obtained with the help of Atlas TCAD simulation by overlaying four plots of four different gate voltages.

4.7 MIXED-MODE CIRCUIT SIMULATION

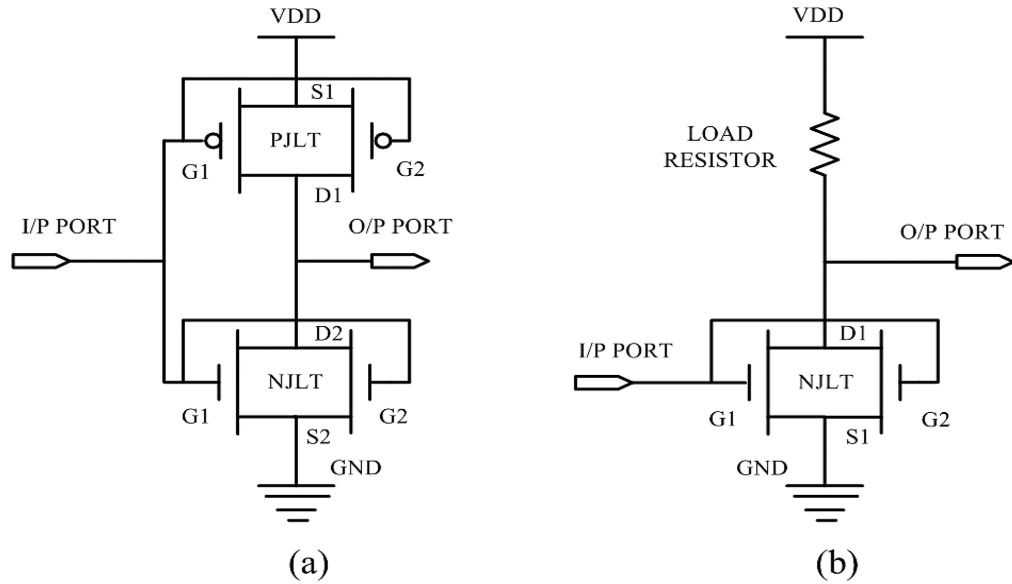


Figure 4.9 Schematic of (a) DG-JLT CMOS and (b) DG-JLT NMOS inverter.

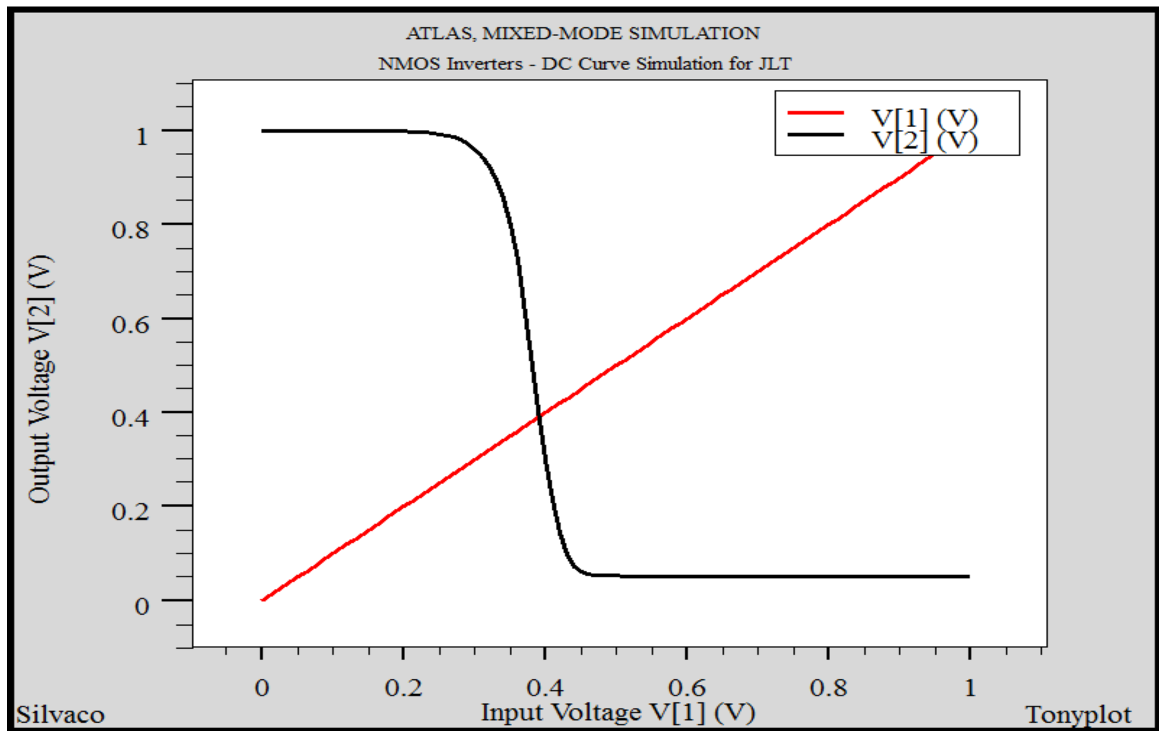


Figure 4.10 DC Curve Simulation for DG-JLT NMOS inverter.

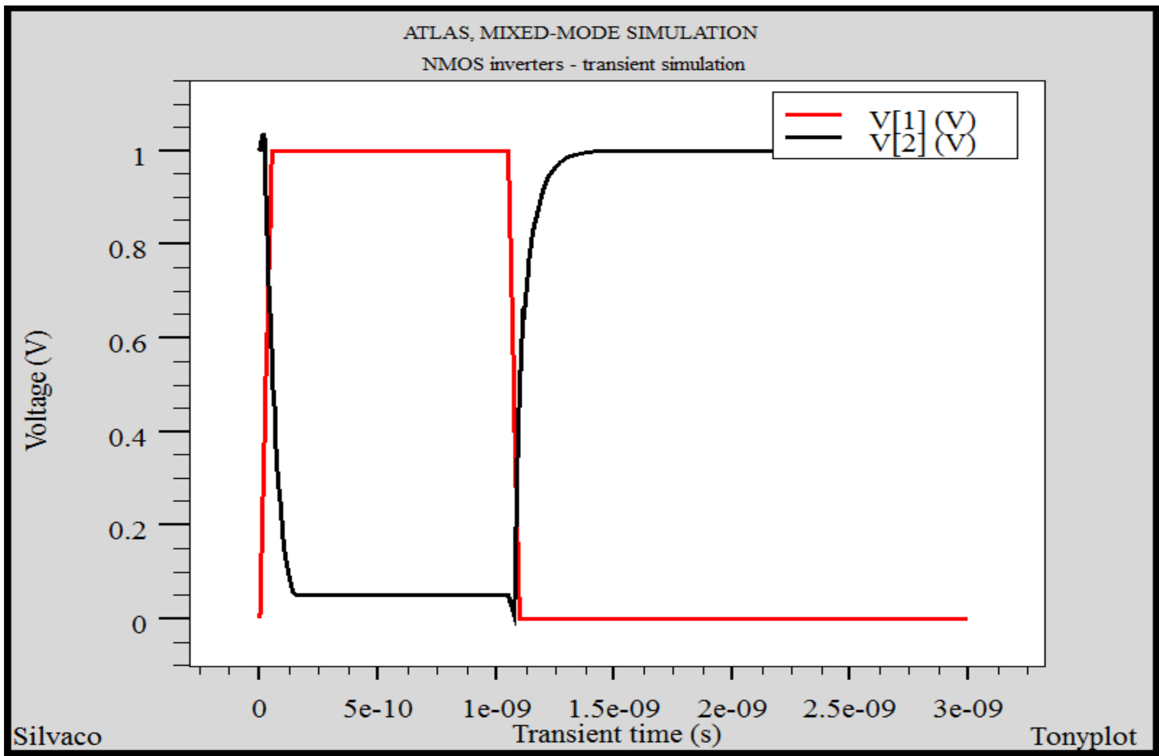


Figure 4.11 Transient Analyses for DG-JLT NMOS Inverter.

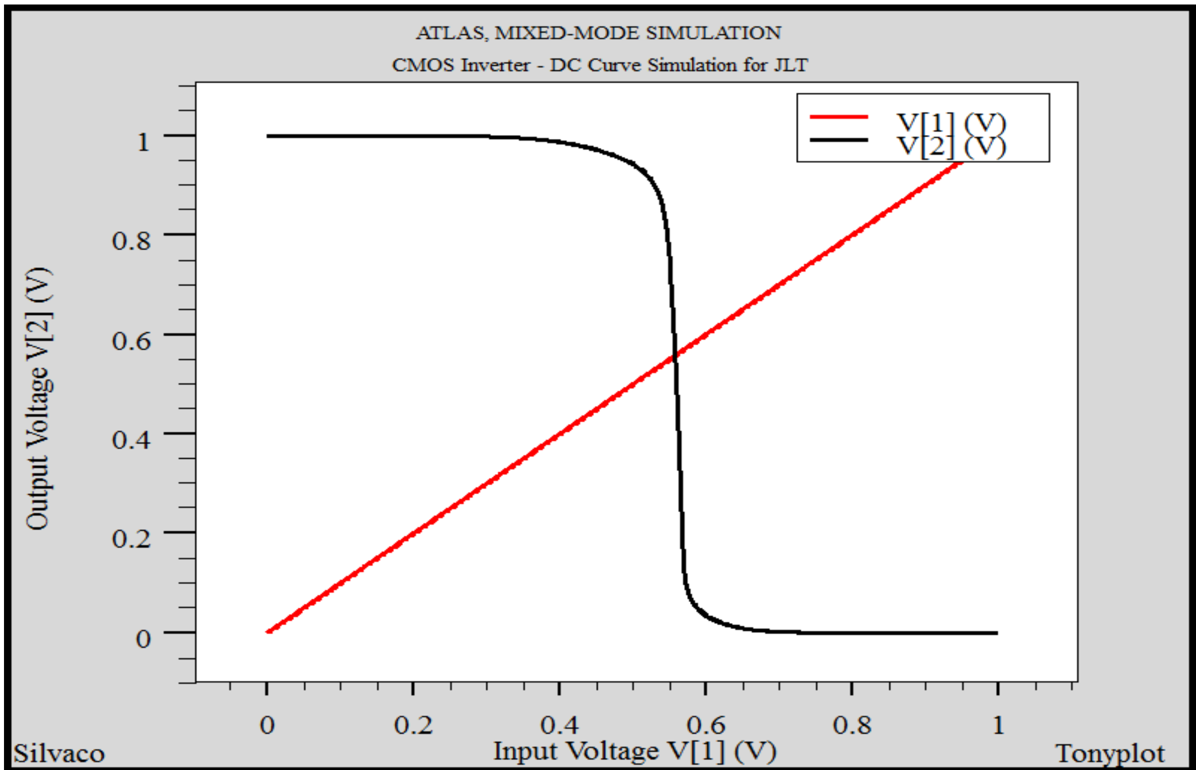


Figure 4.12 DC Curve Simulation for DG-JLT CMOS.

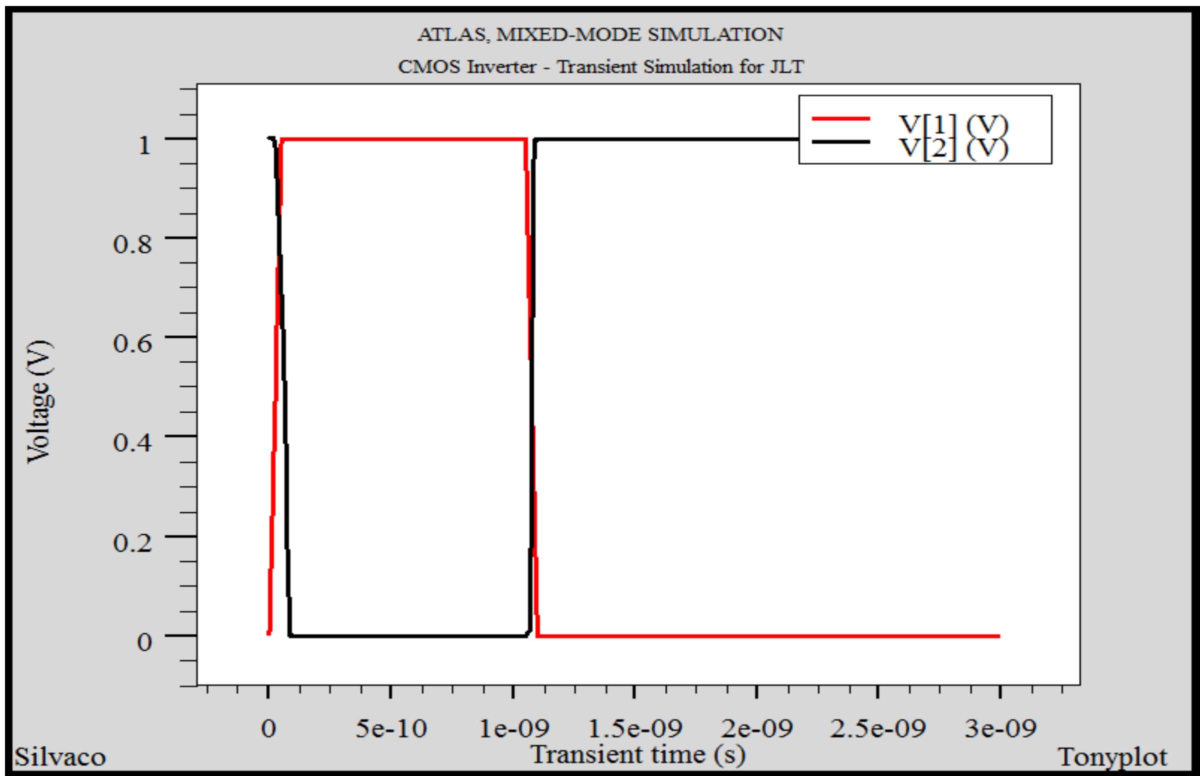


Figure 4.13 Transient Analyses for DG-JLT CMOS Inverter.

In figure 4.9 (a) the schematic representation of CMOS inverter using N channel JFET and P channel JFET is shown. Similarly figure 4.9 (b) shows resistive load inverter with N channel JFET is depicted. In ATLAS tool we have a privilege of performing circuit simulation with circuit components. This mixed mode simulation approach provides spice level simulation along with device level simulation so that behavior of new device at circuit level could be analyzed. In figure 4.10 DC curve simulation of N channel JFET is shown. Where V[1] is the input applied voltage and V[2] is the output voltage at the output terminal of inverter. Similarly figure 4.12 shows DC curve simulation for CMOS inverter.

Figure 4.11 and 4.13 show transient simulation of NMOS inverter and CMOS inverter designed using JFET. Where V[1] is the input applied voltage and V[2] is the output voltage at the output terminal of inverter. It is clearly visible that CMOS inverter is showing promising results in comparison to NMOS inverter. After analyzing mixed mode results we can conclude with a positive note on our proposed device's circuit application. The TCAD script for mixed-mode simulation has been presented in Appendix.

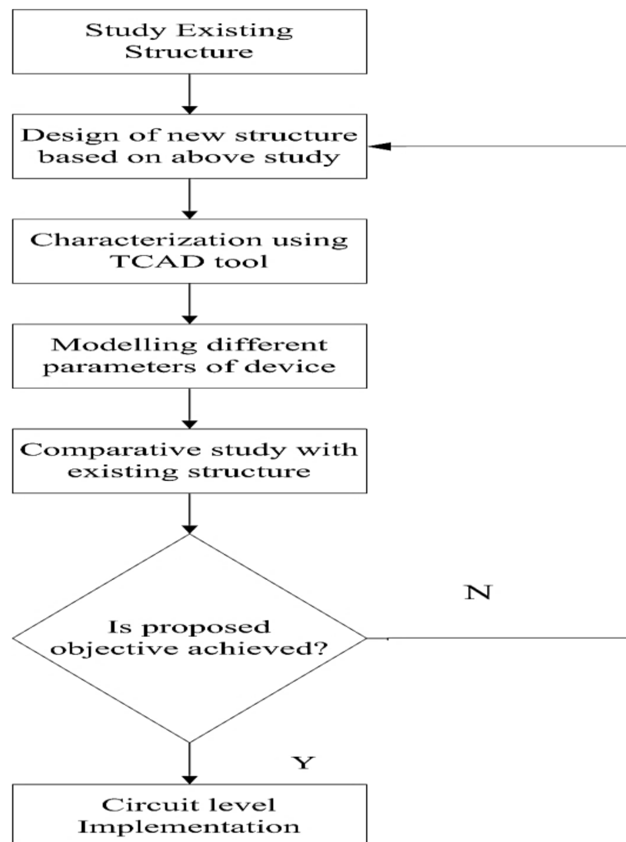
CHAPTER 5

CONCLUSION AND FUTURE WORK

5.1 CONCLUSION

With the scaling of device dimensions, a need to suppress the short channel effects was felt and DG JL MOSFET is one of the promising future candidates in the field of device technology. In this chapter n-type DG JL MOSFET was explored to study its behaviour. An analytical compact drain current model and threshold voltage model in the presence of interface charges in subthreshold region was developed and the model was validated with the simulation results and was found to be in good agreement. The developed model characteristics was compared to the ATLAS simulation results was found that the developed model follows all the characteristics of a short channel device and has a beer subthreshold slope. Developed model is showing high drain current values (high ON-OFF current ratio) which shows better feasibility of our device. Other than the performance advantages, our device offers simple fabrication and cost effectiveness.

5.2 METHODOLOGY



5.3 SCOPE FOR FUTURE WORK

The developed model has several possible extensions that could be attempted as ongoing research work. Some specific recommendations based on the present work are as follows:

1. The developed drain current model for the subthreshold region can be extended for a full drain current model by considering the current in depletion and accumulation region using proper boundary conditions

2. Present study can be well extended by adding other SCEs, which were not considered such as mobility degradation and velocity saturation into consideration.

3. The present model follows classical drift-diffusion approach and can be studied for semi-classical modeling as well.

4. Quantum effects such as quantum confinement and nanoscale effects can also be incorporated into the model so that a more précised results are obtained.

5. Model of relation between central potential and surface potential could be studied in deep for precise calculation of threshold voltage.

6. Gate current model can also be obtained for oxide thickness 1.5 nm, which would help in modelling leakage current in a precise manner.

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APPENDIX

1. ATLAS SILVACO Script for DG-JLT with oxide thickness 1.5 nm

```
go atlas
mesh

x.m l=-0.003 s=0.01
x.m l=-0.0025 s=0.01
x.m l=0 s=0.01
x.m l=0.001 s=0.01
x.m l=0.004 s=0.01
x.m l=0.005 s=0.001
x.m l=0.04 s=0.001
x.m l=.045 s=0.001
x.m l=0.046 s=0.01
x.m l=0.049 s=0.01
x.m l=0.05 s=0.01
x.m l=0.0525 s=0.01
x.m l=0.053 s=0.01

y.m l=-0.002  s=0.01
y.m l=-0.0015  s=0.001
y.m l=0.0      s=0.001
y.m l=0.005    s=0.001
y.m l=0.010    s=0.001
y.m l=0.0115    s=0.001
y.m l=0.012    s=0.01

#Defing regions
region num=1 x.min=-0.005 x.max=0.045 y.min=0 y.max=0.010 silicon
region num=2 x.min=-0.0025 x.max=0.005 y.min=0 y.max=0.010 silicon
region num=3 x.min=0.045 x.max=0.0525 y.min=0 y.max=0.010 silicon
region num=4 x.min=0.005 x.max=0.045 y.min=-0.0015 y.max=0 sio2
region num=4  x.min=-0.003 x.max=0.005 y.min=-0.002 y.max=0 sio2
region num=4  x.min=0.045 x.max=0.053 y.min=-0.002 y.max=0 sio2
```

```
region num=5 x.min=0.005 x.max=0.045 y.min=0.010 y.max=0.0115 sio2
region num=5 x.min=-0.003 x.max=0.005 y.min=0.010 y.max=0.012 sio2
region num=5 x.min=0.045 x.max=0.053 y.min=0.010 y.max=0.012 sio2

#Defining Electrodes
electrode   num=1 name=gate x.min=0.005 x.max=0.045 y.min=-0.002 y.max=-0.0015
electrode   num=2 name=drain  x.min=-0.003 x.max=-0.0025 y.min=0 y.max=0.01
electrode   num=3 name=source x.min=0.0525 x.max=0.053 y.min=0 y.max=0.01
electrode   num=4 name=gate2 x.min=0.005 x.max=0.045 y.min=0.0115 y.max=0.012

#Doping Concentration
doping region=1 n.type uniform conc=1e19
doping region=2 n.type uniform conc=1e19
doping region=3 n.type uniform conc=1e19

#Defining interface trap charge
#INTERFACE QF=1e12 x.min=0.040 x.max=0.045 y.min=0 y.max=0
#INTERFACE QF=1e12 x.min=0.040 x.max=0.045 y.min=0.01 y.max=0.01

contact name=source
contact name=drain
contact name=gate   workfunction=5.4
contact name=gate2   workfunction=5.4 common=gate

# select models
models conmob srh auger bgn fldmob print
#models HEI HHI N.CONCAN P.CONCAN BQP.N fnord print
#output band.par con.band val.band t.quantum qfn qfp e.lines e.field j.electron
j.hole

#Calculation
solve init
method block newton
solve vsource=0
#solve vdrain=0
#solve vgate=1
```

```
#solve vgate=0.7

solve vdrain=1

log outf=DG_JLT_MOSFET_Lg=40nm_Tox=1.5nm.log master

solve vgate=0 vstep=0.005 name=gate vfinal=1

log off

save outf=DG_JLT_MOSFET_Lg=40nm_Tox=1.5nm.str


#extract device parameters......

extract init inf="DG_JLT_MOSFET_Lg=40nm_Tox=1.5nm.log"

extract name="vt" (xintercept(maxslope(curve(abs(v."gate"),abs(i."drain"))))-
abs(ave(v."drain"))/2.0)


#extract device parameters......

extract init inf="DG_JLT_MOSFET_Lg=40nm_Tox=1.5nm.log"

extract name="vt" (xintercept(maxslope(curve(abs(v."gate"),abs(i."drain"))))-
abs(ave(v."drain"))/2.0)


#extract the device parameter SubVt...

extract init inf="DG_JLT_MOSFET_Lg=40nm_Tox=1.5nm.log"

extract name="subvt"
1.0/slope(maxslope(curve(abs(v."gate"),log10(abs(i."drain")))))


tonyplot DG_JLT_MOSFET_Lg=40nm_Tox=1.5nm.log

tonyplot DG_JLT_MOSFET_Lg=40nm_Tox=1.5nm.str

quit
```

2. Mixed-Mode ATLAS script for resistive load NJLT Inverter

```
go atlas


mesh    outf=jltformixedmode.str master.out


x.m l=0 s=0.01

x.m l=0.001 s=0.01

x.m l=0.004 s=0.01

x.m l=0.005 s=0.001
```

```
x.m l=0.04 s=0.0001

x.m l=.045 s=0.0001

x.m l=0.046 s=0.01

x.m l=0.049 s=0.01

x.m l=0.05 s=0.01


y.m l=-0.003  s=0.01

y.m l=-0.002  s=0.001

y.m l=0.0      s=0.001

y.m l=0.005   s=0.001

y.m l=0.010   s=0.001

y.m l=0.012   s=0.001

y.m l=0.013   s=0.01


region num=1 x.min=0.001 x.max=0.049 y.min=0 y.max=0.010 silicon

region num=2 x.min=0.005 x.max=0.045 y.min=-0.002 y.max=0 sio2

region num=2  x.min=0.00 x.max=0.005 y.min=-0.003 y.max=0 sio2

region num=2  x.min=0.045 x.max=0.05 y.min=-0.003 y.max=0 sio2

region num=3 x.min=0.005 x.max=0.045 y.min=0.010 y.max=0.012 sio2

region num=3 x.min=0 x.max=0.005 y.min=0.010 y.max=0.013 sio2

region num=3 x.min=0.045 x.max=0.05 y.min=0.010 y.max=0.013 sio2


electrode   num=1 name=gate x.min=0.005 x.max=0.045 y.min=-0.003 y.max=-0.002

electrode   num=2 name=drain  x.min=0 x.max=0.001 y.min=0 y.max=0.01

electrode   num=3 name=source x.min=0.049 x.max=0.05 y.min=0 y.max=0.01

electrode   num=4 name=gate2 x.min=0.005 x.max=0.045 y.min=0.012 y.max=0.013


doping region=1 n.type uniform conc=1.5e17


save outf=jltformixedmode.str master


go atlas


.begin

vin 1 0 0

an 2=drain 1=gate 1=gate2 0=source infile=jltformixedmode.str width=1.
```

```
mn 3 2 0 0 simple L=.05u W=1u
r1 2 4 50k
r2 3 4 10k
vcc 4 0 1.
c1 3 0 1ff
#
#     End of circuit description
#
.model simple nmos ( tox=0.002e-6 vt0=0.5 )
#
.numeric vchange=1.
.options print m2ln noshift
#
.save outfile=nmos
.end

#  Define physical models for ATLAS device
#
contact device=an name=gate   workfun=4.7
contact device=an name=gate2   workfun=4.7 common=gate
model   device=an reg=1 conmob fldmob bgn

go atlas
.begin
#
#     NMOS inverters - DC curve simulation

#
#     Circuit description
#
vin 1 0 0
an 2=drain 1=gate 0=source 1=gate2  infile=jltformixedmode.str width=1.
mn 3 2 0 0 simple L=.05u W=1u
r1 2 4 50k
r2 3 4 10k
vcc 4 0 1.
```

```
c1 3 0 1ff
#
#     End of circuit description
#
.model simple nmos ( tox=0.002e-6 vt0=0.5 )
#
.options print fulln noshift
#
.load infile=nmos
.log outfile= jltformixedmode
.dc vin 0. 1. 0.01
#
.end
#
#  Define physical models for ATLAS device
#
contact device=an name=gate   workfun=4.7
contact device=an name=gate2   workfun=4.7 common=gate
model   device=an reg=1 conmob fldmob bgn

go atlas

tonyplot  jltformixedmode_dc_1.log -set  jltformixedmode_dc_1.set

go atlas
.begin
#
#     NMOS inverters - transient simulation
#
#     Circuit description
#
vin 1 0 0. PULSE 0 1 0 50ps 50ps 1000ps 10
an 2=drain 1=gate 0=source 1=gate2  infile= jltformixedmode.str width=1.
mn 3 2 0 0 simple L=0.05u W=1u
r1 2 4 50k
r2 3 4 10k
```

```
vcc 4 0 1.
c1 3 0 1ff
#
#     End of circuit description
#
.model simple nmos ( tox=.002e-6 vt0=0.5 )
#
.numeric lte=0.05 dtmin=1e-15
.options print noshift
#
.load infile=nmos
.log outfile= jltformixedmode_t
#
.tran 0.0001ps 3ns
#
.end
#
#    ATLAS device models and parameters
#
contact device=an name=gate   workfun=4.7
contact device=an name=gate2   workfun=4.7 common=gate
model   device=an reg=1 conmob fldmob bgn

go atlas
tonyplot  jltformixedmode_t_tr.log -set  jltformixedmode_t_tr.set
quit
```

3. Mixed-Mode ATLAS script for CMOS Inverter with NJLT and PJLT.

```
go atlas

mesh    outf=jltnmos_operation.str master.out

x.m l=0 s=0.01
x.m l=0.001 s=0.01
x.m l=0.004 s=0.01
```

```
x.m l=0.005 s=0.001

x.m l=0.04 s=0.0001

x.m l=.045 s=0.0001

x.m l=0.046 s=0.01

x.m l=0.049 s=0.01

x.m l=0.05 s=0.01


y.m l=-0.003  s=0.01

y.m l=-0.002  s=0.001

y.m l=0.0      s=0.001

y.m l=0.005   s=0.001

y.m l=0.010   s=0.001

y.m l=0.012   s=0.001

y.m l=0.013   s=0.01


region num=1 x.min=0.001 x.max=0.049 y.min=0 y.max=0.010 silicon

region num=2 x.min=0.005 x.max=0.045 y.min=-0.002 y.max=0 sio2

region num=2  x.min=0.00 x.max=0.005 y.min=-0.003 y.max=0 sio2

region num=2  x.min=0.045 x.max=0.05 y.min=-0.003 y.max=0 sio2

region num=3 x.min=0.005 x.max=0.045 y.min=0.010 y.max=0.012 sio2

region num=3 x.min=0 x.max=0.005 y.min=0.010 y.max=0.013 sio2

region num=3 x.min=0.045 x.max=0.05 y.min=0.010 y.max=0.013 sio2



electrode   num=1 name=gate x.min=0.005 x.max=0.045 y.min=-0.003 y.max=-0.002

electrode   num=2 name=drain  x.min=0 x.max=0.001 y.min=0 y.max=0.01

electrode   num=3 name=source x.min=0.049 x.max=0.05 y.min=0 y.max=0.01

electrode   num=4 name=gate2 x.min=0.005 x.max=0.045 y.min=0.012 y.max=0.013


doping region=1 n.type uniform conc=1.5e18


#Defining interface trap charge

INTERFACE QF=-1e12 x.min=0.001 x.max=0.045 y.min=0 y.max=0

INTERFACE QF=-1e12 x.min=0.001 x.max=0.045 y.min=0.01 y.max=0.01


save outf=jltnmos_operation.str master
```

```
#tonyplot  jltnmos_operation.str -jltnmos_operation.set

go atlas

mesh    outf=jltpmos_operation.str master.out

x.m l=0 s=0.01
x.m l=0.001 s=0.01
x.m l=0.004 s=0.01
x.m l=0.005 s=0.001
x.m l=0.04 s=0.0001
x.m l=.045 s=0.0001
x.m l=0.046 s=0.01
x.m l=0.049 s=0.01
x.m l=0.05 s=0.01

y.m l=-0.003  s=0.01
y.m l=-0.002  s=0.001
y.m l=0.0      s=0.001
y.m l=0.005   s=0.001
y.m l=0.010   s=0.001
y.m l=0.012   s=0.001
y.m l=0.013   s=0.01

region num=1 x.min=0.001 x.max=0.049 y.min=0 y.max=0.010 silicon
region num=2 x.min=0.005 x.max=0.045 y.min=-0.002 y.max=0 sio2
region num=2  x.min=0.00 x.max=0.005 y.min=-0.003 y.max=0 sio2
region num=2  x.min=0.045 x.max=0.05 y.min=-0.003 y.max=0 sio2
region num=3 x.min=0.005 x.max=0.045 y.min=0.010 y.max=0.012 sio2
region num=3 x.min=0 x.max=0.005 y.min=0.010 y.max=0.013 sio2
region num=3 x.min=0.045 x.max=0.05 y.min=0.010 y.max=0.013 sio2

electrode   num=1 name=gate x.min=0.005 x.max=0.045 y.min=-0.003 y.max=-0.002
electrode   num=2 name=drain  x.min=0 x.max=0.001 y.min=0 y.max=0.01
electrode   num=3 name=source x.min=0.049 x.max=0.05 y.min=0 y.max=0.01
```

```
electrode   num=4 name=gate2 x.min=0.005 x.max=0.045 y.min=0.012 y.max=0.013

doping region=1 p.type uniform conc=1.5e18

#Defining interface trap charge
INTERFACE QF=-1e12 x.min=0.001 x.max=0.045 y.min=0 y.max=0
INTERFACE QF=-1e12 x.min=0.001 x.max=0.045 y.min=0.01 y.max=0.01

save outf=jltpmos_operation.str master

go atlas

.begin
vin 1 0 0
an1 2=drain 1=gate 1=gate2 0=source infile=jltnmos_operation.str width=0.05.
an2 2=drain 1=gate 1=gate2 3=source infile=jltpmos_operation.str width=0.1.
mp 4 2 0 0 simple L=.05u W=1u
r1 4 0 10k
#r2 3 4 1k
vcc 3 0 1.
c1 4 0 1ff

#
#     End of circuit description
#
.model simple nmos ( tox=0.002e-6 vt0=0.5 )
#
.numeric vchange=1.
.options print m2ln noshift
#
.save outfile=nmos
.end
#  Define physical models for ATLAS device
#
contact device=an1 name=gate   workfun=4.7
contact device=an1 name=gate2   workfun=4.7 common=gate
```

```
model   device=an1 reg=1 conmob fldmob bgn
contact device=an2 name=gate workfun=4.7
contact device=an2 name=gate2 workfun=4.7 common=gate
model   device=an2 reg=2 conmob fldmob bgn
go atlas
.begin
#
#     CMOS inverters - DC curve simulation
#
#     Circuit description
#
vin 1 0 0
an1 2=drain 1=gate 0=source 1=gate2  infile=jltcmos_operation.str width=0.05.
an2 2=drain 1=gate 3=source 1=gate2 infile=jltpmos_operation.str width=0.1.
mp 4 2 0 0 simple L=.05u W=1u
r1 4 3 10k
#r2 3 4 0.1k
vcc 3 0 1.
c1 4 0 1ff
#
#     End of circuit description
#
.model simple nmos ( tox=0.002e-6 vt0=0.5 )
#
.options print fulln noshift
#
.load infile=nmos
.log outfile= jltcmos_operation
.dc vin 0. 1. 0.001
#
.end
#
#  Define physical models for ATLAS device
#
contact device=an1 name=gate   workfun=4.7
contact device=an1 name=gate2   workfun=4.7 common=gate
```

```
model   device=an1 reg=1 conmob fldmob bgn
contact device=an2 name=gate workfun=4.7
contact device=an2 name=gate2 workfun=4.7 common=gate
model   device=an2 reg=2 conmob fldmob bgn
go atlas
tonyplot  jltcmos_operation_dc_1.log -set  jltcmos_operation_dc_1.set

go atlas
.begin
#

#     CMOS inverters - transient simulation
#
#     Circuit description
#
vin 1 0 0. PULSE 0 1 0 50ps 50ps 1000ps 10
an1 2=drain 1=gate 0=source 1=gate2  infile= jltcmos_operation.str width=0.05.
an2 2=drain 1=gate 3=source 1=gate2  infile=jltpmos_operation.str width=0.1.
mp 4 2 0 0 simple L=.05u W=1u
r1 4 3 10k
#r2 3 4 1k
vcc 3 0 1.
c1 4 0 1ff
#

#     End of circuit description
#
.model simple nmos ( tox=.002e-6 vt0=0.5 )
#
.numeric lte=0.05 dtmin=1e-15
.options print noshift
#
.load infile=nmos
.log outfile= jltcmos_operation_t
#
.tran 0.001ps 3ns
```

```
#
.end
#

#    ATLAS device models and parameters
#
contact device=an1 name=gate   workfun=4.7
contact device=an1 name=gate2   workfun=4.7 common=gate
model   device=an1 reg=1 conmob fldmob bgn
contact device=an2 name=gate workfun=4.7
contact device=an2 name=gate2 workfun=4.7 common=gate
model   device=an2 reg=2 conmob fldmob bgn
go atlas
tonyplot  jltcmos_operation_t_tr.log -set  jltcmos_operation_t_tr.set
quit
```