An Analytical Study of 6H-SiC Schottky Barrier Diode (SBD) using Complementary Error Function profile for Breakdown Voltages and Depletion Region Width

A Thesis submitted in partial fulfillment of the requirements for the award of degree of

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CERTIFICATE

I hereby certify that the work, which is being presented in the thesis, entitled "**An analytical study of 6H-SiC Schottky Barrier Diode (SBD) using complementary error function profile for Breakdown Voltages and Depletion Region width**" in partial fulfillment of the requirements for the award of degree of Master of Technology in VLSI Design & CAD at Electronics and Communication Engineering Department of Thapar University, Patiala, is an authentic record of my own work carried out under the guidance of Dr. A.K.Chatterjee.

I have not submitted the matter presented in the thesis for the award of any other degree of this or any other university.

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This is to certify that the above statement made by the candidate is correct and true to best of my knowledge.

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ABSTRACT

Silicon carbide is a wide band gap semiconductor material for high temperature, high-power and high-frequency device applications.The fact that wide band gap semiconductors are capable of electronic functionality at much higher temperatures than silicon. Because of its wide band gap, the leakage current of SiC is many orders of magnitude lower than that of silicon.

There are number of possible crystal structure. These are 2H, 3C, 4H and 6H; but the most important are 3C, 4H and 6H.These structures differ by band gap energy, carrier mobility and breakdown field. Silicon Carbide is the only chemical compound of carbon and silicon. It was originally produced by a high temperature electro-chemical reaction of sand and carbon. Schottky barrier diodes (SBDs) have many benefits compared to other rectifying devices, such as fast switching speeds and relatively easy fabrication.

The present work aims at the design of high breakdown voltage 7 kV 6H-SiC Schottky barrier diode with complementary error function doping profile in drift region .Firstly, the device equation for calculating breakdown voltages (Punch through and Avalanche both) is derived. After that the drift region depletion width is calculated at doping concentration $N_d = 1*10^{15}$ /cm^3 for different breakdown voltages from 1 to 10 kV

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LIST OF USED ACRONYM

CVD : Chemical Vapor Deposition

eV : Electron Volt

HTCVD : High Temperature Chemical Vapor Deposition

LPE : Liquid Phase Epitaxy

MESFET : Metal-Semiconductor Field Effect Transistor

MOSFET : Metal-Oxide Semiconductor Field Effect Transistor

SBD : Schottky Barrier Diode

SBH : Schottky Barrier Height

SiC : Silicon Carbide

SiO_2 : Silicon dioxide

VPE : Vapor Phase Epitaxy

E_g : Energy bandgap

E_C : Energy Conduction Band

E_{fm} : Metal Fermi Level

ϕ_m : Metal Work Function

ϕ_S : Semiconductor Work Function

E_{fs} : Semiconductor Fermi Level

E_0 : Vacuum Level

ϕ_{Bn} : Barrier height of n-type semiconductor

ϕ_{Bp} : Barrier height of p-type semiconductor

ϕ_B : Barrier height

V_{bi} : Built in voltage

χ_S : Electron affinity of semiconductor

$\in_S$: Permittivity of semiconductor

$\in_0$: Permittivity of free space

V_a : Applied voltage to Schottky Contact

N_d : Doping concentration of semiconductor

J : Current Density

J_F : Forward Current Density

V_F : Forward Voltage Drop

η : Ideality Factor

A^* : Richardson's constant

k : Boltzmn constant

T : Temperature

q : Electronics Charge

$\Delta\phi_b$: Potential lowering

n_i : Intrinsic Carrier Concentration

A : Schottky Contact Area

V_n : Potential between conduction band and Fermi level under flat band Conditions

δ : Interfacial film width

R_S : Series Resistance

V_B : Breakdown Voltage

$\in_{cr}$: Critical electric field

R_{on-sp} : Specific on-resistance

μ_n : Electron mobility

W_d : Depletion width

J_L : Leakage Current Density

E_m : Maximum Electric Field

V_R : Reverse Bias Voltage

P_d : Power Dissipation

α : Gradient

CHAPTER 1

INTRODUCTION

1.1. Brief History of SiC

It is a wide band gap semiconductor with an energy gap wider than 2 eV and possesses extremely high power, high voltage switching characteristics and high thermal, chemical and mechanical stability. The unique thermal and electronic properties of silicon carbide provide multiplicative combination of attributes which lead to one of the highest figure of merit for any semiconductor material for use in high-power,-speed,- temperature,-frequency and radiation hard environment. Silicon Carbide (SiC) was discovered in 1824 by the Swedish scientist Jons Jacob Berzelius [1], who received part of his education at Linkoping. SiC is also known as carborundum or moissanite, in natural form it is found in meteorites [2]. SiC is a hard and stable compound maintaining its mechanical properties above 1000ºC. In the Mohs scale of hardness SiC is placed with a number 9, while diamond is 10 and corundum 8. The interest in SiC began to grow from its excellent mechanical properties. In the Acheson process [3] SiC was manufactured by the electrochemical reaction of sand and carbon at high temperatures (up to 2550ºC). As an abrasive material it has found its application for cutting, grinding and polishing. SiC is a very promising wide bandgap semiconductor due to its physical and electrical properties. The first electroluminescence has been reported in 1907 [4], when a SiC light emitting diode was made.

The limitations in material properties of silicon have further increased the interest in SiC and in the last decade it has been growing rapidly. While most of the present semiconductor applications are using Si based devices, there are some for which silicon will never be applicable due to its Physical limitations.

Silicon is limited to maximum operating temperature of 150ºC. It cannot be used in optoelectronics and operate at very high voltages. In comparison, silicon carbide has an excellent material property which makes it superior to Si in a wide range of applications. One method for growing high quality SiC crystals was presented by J.A. Lely in 1955 [5]. The

method was based on sublimation and enabled growth of α-SiC platelets. This invention has initiated a lot of research on SiC electronic applications. The breakthrough was made in 1978. The modified Lely method was reported by Tairov and Tsvetkov [6]. The method uses a seeded sublimation process and reduces the problems with yield and polytype control, even though crystalline quality was low. The method is commonly termed physical vapor transport (PVT). The new technique brought new problems in the form of high defect density in the grown crystals. The most severe is the so-called micropipe, a hollow core penetrating through the crystal. It can degrade the electrical properties of devices and became an obstacle for successful commercialization of SiC for electronic applications.

1.2 Introduction to SiC

Device processing, as well as micro machining in SiC, is under development which will make it possible to combine sensors with e.g. electronics, heating, temperature sensors on the same chip in future. However the successive development of any material for semiconductor applications depends to a large degree on the capability of producing high quality single crystals of that material with controlled electronic properties.

The development of SiC had long been hindered by a lack of suitable crystal growth technology. Two significant factors in SiC's crystal growth problems are its ability to grow in many different crystal structures, called polytypes, and its inability to be melted at a reasonable pressure. There are number of possible crystal structure. These are 2H, 3C,4H and 6H;but the most important are 3C,4H and 6H.These structures differ by band gap energy, carrier mobility and breakdown field.

Silicon Carbide is the only chemical compound of carbon and silicon. It was originally produced by a high temperature electro-chemical reaction of sand and carbon. Silicon carbide is an excellent abrasive and has been produced and made into grinding wheels and other abrasive products for over one hundred years. Today the material has been developed into a high quality technical grade ceramic with very good mechanical properties. It is used in abrasives, refractories, ceramics, and numerous high-performance applications. The material can also be made an electrical conductor and has applications in resistance heating, flame

igniters and electronic components. Structural and wear applications are constantly developing.

Silicon carbide is composed of tetrahedral of carbon and silicon atoms with strong bonds in the crystal lattice. This produces a very hard and strong material. Silicon carbide is not attacked by any acids or alkalis or molten salts up to 800°C. In air, SiC forms a protective silicon oxide coating at 1200°C and is able to be used up to 1600°C. The high thermal conductivity coupled with low thermal expansion and high strength give this material exceptional thermal shock resistant qualities.

Silicon carbide ceramics with little or no grain boundary impurities maintain their strength to very high temperatures, approaching 1600°C with no strength loss. Chemical purity, resistance to chemical attack at temperature, and strength retention at high temperatures has made this material very popular as wafer tray supports and paddles in semiconductor furnaces. The electrical conduction of the material has lead to its use in resistance heating elements for electric furnaces, and as a key component in thermistors (temperature variable resistors) and in varistors (voltage variable resistors).

Silicon carbide has been regarded as a wide band gap semiconductor material for visible light- emitting devices, since electro luminescence was observed for the first time in 1907, and a light emitting diode was fabricated for the first time in 1923. Generally 3C-SiC is stable in the low-temperature region below 1800^0C, and 6H-SiC is stable in the higher temperature region above 1800^0C. Although 4H-SiC also sometimes occurs in the high temperature region, the probability is very lower compared to 6H-SiC. Each polytype has unique electrical and physical properties. The stable characteristics of SiC have caused difficulty in producing high quality layers and large single crystal growth, and thus the development of semiconductor technology in SiC has been delayed.

1.3 SiC Semiconductor Electrical Properties

Some of the more important semiconductor electrical properties of the 3C, 4H, and 6H silicon carbide polytypes are given in Table 1.1 [6]. Even within a given polytype, some important electrical properties are non-isotropic, in that they are a strong functions of crystallographic direction of current flow and applied electric field. Dopants in SiC can incorporate into energetically inequivalent quasi-hexagonal (*h*) C-sites or Si-sites, or quasi-cubic (*k*) C-sites or Si-sites. While all dopant ionization energies associated with various dopant incorporation sites should normally be considered for utmost accuracy. Silicon is the semiconductor employed in most commercial solid-state electronics; it is the yardstick by which other semiconductor materials must be evaluated against. To varying degrees the major SiC polytypes exhibit advantages and disadvantages in basic material properties compared to silicon. The most beneficial inherent material superiorities of SiC over silicon are its exceptionally high breakdown electric field, wide band gap energy, high thermal conductivity, and high carrier saturation velocity.

Table 1.1 Properties of common semiconductors in comparison to SiC [6]

material	E_g at 300 K [eV]	μ_n [$cm^2 (Vs)^{-1}$]	E_c [$x10^6$ Vcm^{-1}]	v_{sat} [$x10^7 cm\ s^{-1}$]	λ [$W\ (cm\ K)^{-1}$]
Si	1.1	1350	0.3	1.0	1.5
GaAs	1.4	8500	0.4	2.0	0.5
3C-GaN	3.27	1000	1	2.5	1.3
2H-GaN	3.29	900	3.3	2.5	1.3
3C-SiC	2.3	900	1.2	2.0	4.5
4H-SiC	3.26	720	2.0	2.0	4.5
6H-SiC	3.0	370	2.4	2.0	4.5
AIN	6.1	1100	11.7	1.8	2.5
Diamond	5.45	1900	5.6	2.7	2.0

1.4 SiC Semiconductor Crystal Growth

1.4.1 Seeded Sublimation Growth

The main SiC bulk growth method is the seeded sublimation growth method also known as physical vapor transport (PVT), and often referred to as modified Lely method. This is the most successful SiC bulk growth method and now a day's widely used in the industry to grow monocrystalline 4H and 6H-SiC boules [6]. In the method, a SiC source and a SiC seed are placed inside quasi-closed graphite or TaC crucible.

To prevent contamination from falling particles the seed is placed at the top of the crucible. Lely platelets or modified Lely grown wafers of high quality are used as a seed. It is important to obtain a high quality material with reduced defect and micropipe densities. By selecting the best wafers it is possible gradually to eliminate the micropipes.

The driving force in the process is provided by applying a temperature difference between the sources (higher temperature T2) and the seed (lower temperature T1) in a low pressure of inert gas (argon at 5-30 mbar), see Fig.1.1.The temperature is obtained by applying induction (frequency of 10-100 kHz) heating on the crucible. Since graphite has good heat and electrical conductivity, the crucible design contributes to temperature control of the crystal growth. The temperatures are measured with two pyrometers at the top and the bottom of the crucible. Both SiC powder and polycrystalline boules were used as a source material, usually purified and sintered before growth to reduce contamination of the crystal from impurities and obtain more stable growth behavior.

The source material sublimes at applied high temperature (1800-2600ºC) and at low inert gas (argon) pressure. The Si and C bearing species (of which Si, SiC2, Si2C are the main ones) are transported to the growing surface. A long source-to-seed distance (5-30mm) is required to grow long boules and there will be an interaction of Si containing species in the vapor with the graphite walls. This makes the growth process difficult to control. In the vapor equilibrium the total pressure is determined by the highest partial pressure of one of the components. Silicon has the highest vapor pressure in the regime of the used growth temperatures.

In the sublimation growth performed in the quasi-closed crucible Si losses might easily occur, especially if growth is conducted in vacuum ambient. This results in graphitization of the source and causes undesired growth conditions. There are two ways to control Si vapor behaviour a) introduce excess Si to powder or b) getter C. The former option may lead to extreme excess of Si, especially at the initial stage of growth when Si liquid drops are formed at the seed substrate and cause growth disturbances. The latter option using refractory metal, which absorbs carbon and forms stable carbides at the growth temperatures. A tantalum as a carbon getter has been utilized in this work.

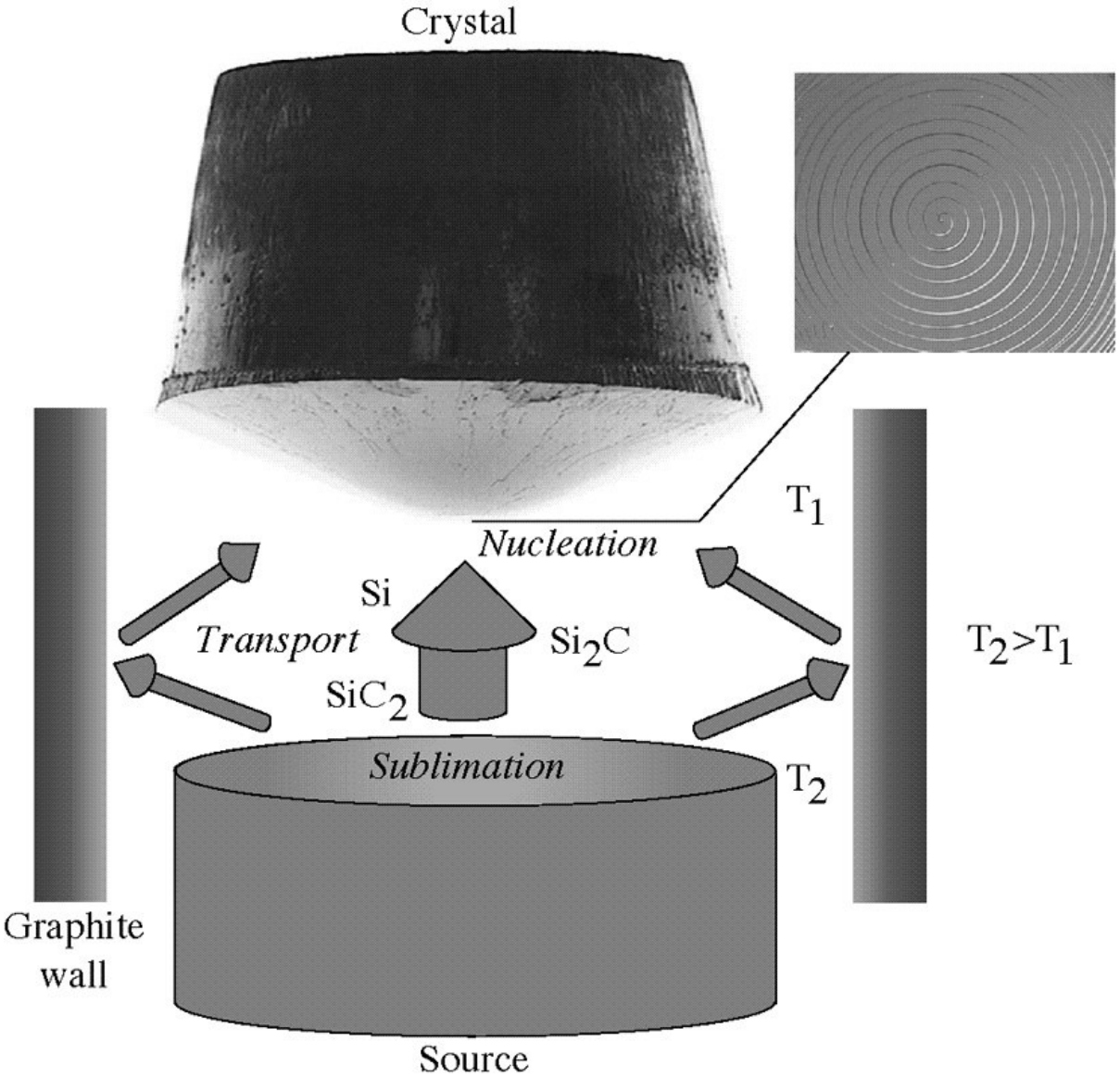

Fig.1.1 SiC sublimation bulk growth method in schematic picture [7]

The shielding was introduced for growth in vacuum, which is one way to decrease impurity incorporation in bulk crystals. The activation energies for a growth in vacuum above 2075^{o}C are of same order as typically reported for sublimation growth whereas significantly smaller activation energies for growth temperatures below 2075^{o}C are observed. Thus the low super saturation may be kept constant.

The next important issue in the SiC growth is the polytype occurrence with respect to the temperature [8] . The formation of 4H polytype is more probable at lower temperature, while 6H is found to be more stable at higher temperatures. The 3C polytype is metastable and it can form at non-equilibrium during crystal growth, e.g. excess silicon is known to increase the probability of the 3C occurrence.

1.4.2 Sublimation Epitaxial Growth

The principle of sublimation epitaxy also known as PVT epitaxy is similar to that of sublimation bulk, i.e. the driving force in the process is provided by applying a temperature difference between the source (higher temperature) and the seed (lower temperature), which are spaced with short distance, usually 1 mm.

However, the growth is in vacuum and the interaction of subliming species with the walls of the crucible is diminished in difference to sublimation bulk growth. Sublimation epitaxy has proven to be a suitable technique for growth of thick (up to100 μm) epitaxial layers with smooth as-grown surfaces. The structural quality of the epilayer improves compared with the substrate.

A detailed study of the technique was presented in Ref. [7].The remaining issue necessary for epi-fabrication using sublimation epitaxy is growth of high-purity layers. At high temperatures, residual impurities in the epilayers are introduced from the growth environment, mainly the SiC source material, graphite and tantalum. The temperature gradient is controlled and can be adjusted by movable RF coil. To prevent absorption of nitrogen in the graphite and also nitrogen diffusion from ambient into the growth chamber

during loading, argon flushed glove box as a loading chamber was implemented. By varying growth parameters such as growth rate, tantalum environment, heating ramp and Si/C ratio, the relative incorporation of the impurities can be changed.

One interesting finding is that selecting the growth conditions can change the preferred occupation of boron in the shallow or deep level. The electrical activation of acceptors has been studied. The interplay between nitrogen, aluminum and boron is a subject for continued investigations for further understanding of the compensation mechanism. Availability of more pure source material is expected to decrease the residual doping and degree of compensation in the sublimation grown epilayers. Devices such as Schottky diodes and Metal-oxide-semiconductor capacitors were processed on sublimation grown epilayers.

1.5 Structural Defects in SiC

There is no perfect crystal. Even in the thermodynamic equilibrium a crystal structure contains point defects by the absence of atoms or presence of extra atoms. These defects may alter the electrical and optical properties. If a host atom is removed from the lattice, a vacancy is formed. This results in four unsaturated bonds, which have impact on electrical properties of the crystal. If the atom is inserted (either host or impurity atom) into an interstitial site, Schottky interstitial is formed. In the case of the interstitial atom staying in the vicinity of the vacancy, the Frenkel interstitial is formed. The distortion energy associated with the interstitials is reduced.

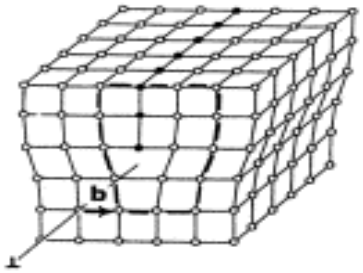

Fig.1.2 Edge dislocation

Dislocations are one-dimensional line defects and they extend through the entire lattice. There are two main types of dislocations, with screw and edge character. The dislocation is a local distortion of the crystal and due to stress. It is required to move by one lattice constant. An edge dislocation is formed by removing from the crystal a half of atoms plane terminating on the dislocation line and then joining the two planes in the way to restore order in the crystal, see Fig.1.2.

A screw dislocation can be explained in the following manner. The crystal has been slipped above the dislocation line by a lattice vector parallel to the line and then rejoined to the part below the dislocation line to restore crystalline order, see Fig.1.3.A structural defect, which has attracted most attention in the SiC research, is the micropipe. It is a hollow core propagating along the [0001] direction. The diameter of the micropipe is several or tens of micrometers.

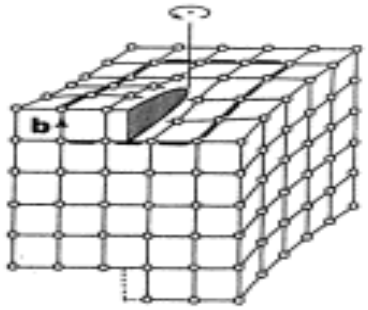

Fig.1.3 Screw dislocation

The usual density in the bulk crystals varies between 10-100/cm^2. The recent scientific reports show a tremendous decrease in the micropipe density to as low as 1.1/cm ^{2} in 2 inch wafers [9]. The micropipes are known to degrade the device performance and yield, e.g. they reduce the breakdown voltage of Schottky diodes [7, 10].

The effect was obtained by applying growth conditions at which the source powder was gradually approaching graphitization and the vapor becoming C-rich. Micropipes

propagating in the single crystal area and facing the misoriented grain have been studied, and it is shown that they may either be terminated at the grain or their propagation is altered to be parallel with the grain boundary. The polytype of the grains may switch from 6H to 4H, which is explained by the change of the Si/C ratio in the vapour.

The defects initially formed as small prismatic platelets and with continued growth the defect formation became more dominating. Grains with high misorientation extended on the surfaces and became the preferred nucleation centre rather than the single crystal material. This demonstrates that defect formation, which could be local appearances, may severely degrade the whole crystals. In the course of the crystal growth the vapour composition, i.e. Si/C ratio change towards C-rich conditions, which in turn promote switching of the polytype.

1.6 Impurities and Intrinsic Levels in SiC.

Doped semiconductors contain impurities. These impurities can either be unintentional or they can be added on purpose to provide free carriers in the semiconductor. The generation of free carriers requires not only the presence of impurities, but also that the impurities are ionized to provide electrons to the conduction band (donors) or that they provide holes to the valence band (acceptors) by effectively accepting an electron from the filled valence band. A semiconductor doped with impurities, which are ionized (meaning that the impurity atoms either have donated or accepted an electron), will therefore contain free carriers. Shallow impurities are impurities, which require little energy – typically around the thermal energy at room temperature or less - to be ionized. Deep impurities require energies higher than the thermal energy at room temperature to be ionized so that in practice only a fraction of the impurities present in the semiconductor contribute to free carriers. Such deep impurities are also called traps.

A semiconductor in which ionized donors provide free electrons, is called n-type, while a semiconductor in which ionized acceptors provide free holes, is referred as a p-type semiconductor. The ionization of the impurities is dependent on the thermal energy and the position of the impurity level within the energy band gap. Statistical thermodynamics can be

used to obtain the probability that the impurity is ionized. The resulting expression is similar to the Fermi-Dirac probability function except for a factor that accounts for the fact that the impurity can only provide one hole or one electron and also accounts for the degeneracy of the valence band [11].

Ionized shallow impurities provide free carriers that equal the impurity concentration for complete ionization. In the case of SiC the most common donors are nitrogen and phosphorus. Both substitute on carbon sites in the lattice. The most common acceptors are aluminum, boron and titanium. They all substitute on silicon sites with some specification for boron. The site is not polytype dependent, but the energy level depends on the particular polytype [12]. Nitrogen and aluminium are the most common dopants.
The impurities may be introduced during the growth, via ion implantation technique or by diffusion. Diffusion is a common doping method of the active layer; however, the diffusion coefficients of impurities in SiC are small. Ion implantation is frequently used in SiC device fabrication. The main drawbacks are the lattice damage caused during the ion bombardment and the occurrence of amorphous material of the ion implanted volume. Nitrogen incorporation decreases exponentially, while aluminum increases exponentially with the growth temperature [13]. The incorporation depends also on the vapor pressure. In the case of nitrogen it increases with the square root of the nitrogen partial pressure in the growth cell, while for aluminum the relation is linear [13,14].

1.7 Advantages of SiC compared with Si

As mentioned earlier, SiC is a wide-bandgap semiconductor, and this property of SiC is expected to yield greatly superior power electronics devices once processing and fabrication issues with this material are solved. Some of the advantages of SiC compared with Si based power devices are as follows:

1. SiC-based power devices have higher breakdown voltages (5 to 30 times higher than those of Si) because of their higher electric breakdown field.

2. SiC devices are thinner, and they have lower on resistances. The substantially higher breakdown voltage for SiC allows higher concentrations of doping and consequently

a lower series resistance. For low breakdown voltage devices (~50V), SiC unipolar device on-resistances are around 100 times less; and at higher breakdown voltages (~5000V), they are up to 300 times less [15]. With lower R_{on}, SiC unipolar power devices have lower conduction losses and therefore higher overall efficiency.

3. SiC has a higher thermal conductivity and thus a lower junction-to-case thermal resistance. This means heat is more easily conducted away from the device junction, and thus the device temperature increase is slower.

4. SiC can operate at high temperatures because of its wider bandgap. SiC device operation at up to 600°C is mentioned in the literature [16]. Most Si devices, on the other hand, can operate at a maximum junction temperature of only 150°C.

5. Forward and reverse characteristics of SiC power devices vary only slightly with temperature and time; therefore, SiC devices are more reliable.

6. SiC-based devices have excellent reverse recovery characteristics [17]. With less reverse recovery current, the switching losses and electromagnetic interference (EMI) are reduced and there is less or no need for snubbers.

7. SiC is extremely radiation hard; i.e., radiation does not degrade the electronic properties of SiC.

1.8 Polytypes of SiC

SiC has equal parts silicon and carbon, both of which are group IV elements. The distance between neighbouring silicon (a) or carbon atom is approximately 3.08 Å for all polytypes. The carbon atom is situated at the centre of mass of the tetragonal structure outlined by the four neighbouring Si atoms (see Figure 1.4). The distance between the C atom and each of the Si atoms is approximately 2.52 Å. The height of the unit cell, called c, varies between the different polytypes. Therefore, the ratio of c/a differs from polytype to polytype. This ratio is 1.641, 3.271, and 4.908 for the 2H, 4H, and 6H-SiC polytypes respectively.

The polytype is a variation of crystalline material in which the stacking order of planes in the unit cell is different. Each SiC bilayer, while maintaining the tetrahedral binding scheme of the crystal, can be situated in one of three possible positions with respect to the lattice (A, B, or C).

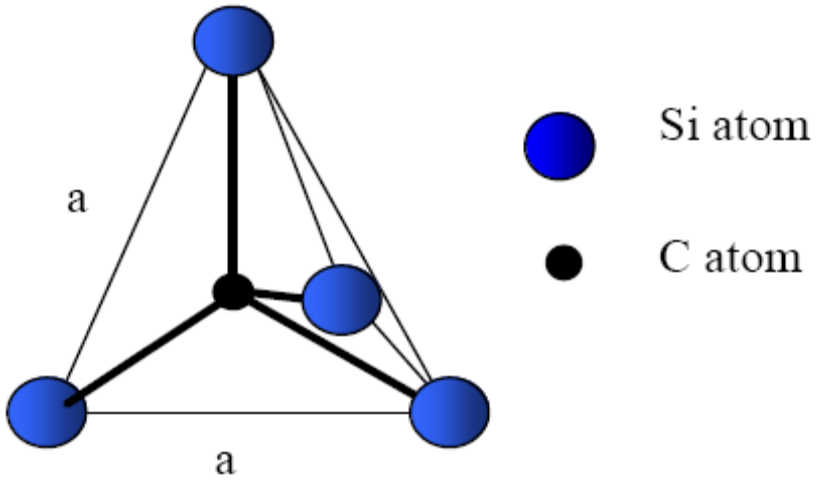

Figure 1.4 The tetragonal bonding of a carbon atom with the four nearest silicon [31].

The bonding between Si and C atoms in adjacent bilayer planes is either of a Zinc-blende (Cubic) or Wurtzite (Hexagonal) nature depending on the stacking order[31]. If the stacking is ABCABC...the cubic polytype commonly abbreviated as 3C-SiC, is realized.

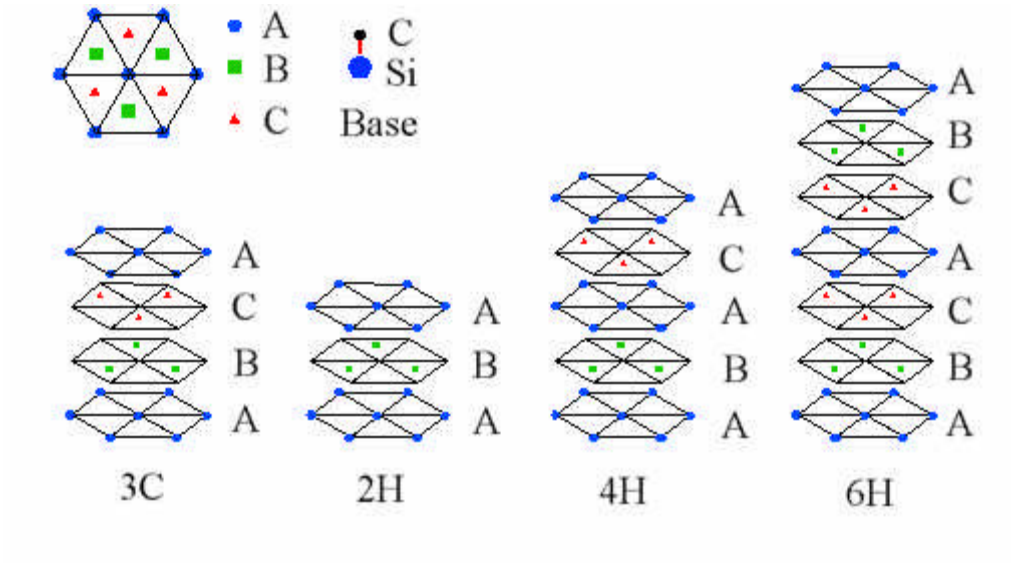

Figure 1.5 The staking sequence of common 3C-, 2H-, 4H-, and 6H-silicon carbide (after ref. [17]).

The purely Wurtzite ABAB... stacking sequence is called 2H-SiC. The 4H-SiC (ABAC...) and 6H-SiC (ABCACB...) are also shown in Figure 1.5[17]. These two types of SiC are the most common hexagonal polytypes [32]. 4H-SiC consists of equal amounts cubic and hexagonal bonds, while 6H-SiC is two-thirds cubic. All the polytypes of SiC are referred to in a hexagonal coordinate system consisting of three a plane coordinates a1, a2, and a3, and a c-axis coordinate. The c-axis is the direction of the stacking of hexagonally close packed layers, and the three a-plane axes are all in the plane perpendicular to c-axis (see Figure 1.6), with 120-degree angle between a planes. Commercially available SiC bulk material is generally cut and polished 3~8 degrees off-axis towards <11 2 0> for avoiding the growth of 3C inclusions in the epitaxial layers of 4H, called step-controlled epitaxy by Matusunami et al. [33]. Two different faces perpendicular to the c-axis (Si 0001 and C 000 1) exist in commonly used SiC. SiC with the silicon face is commonly used for device applications since the quality of epitaxial growth is better than that on the carbon face.

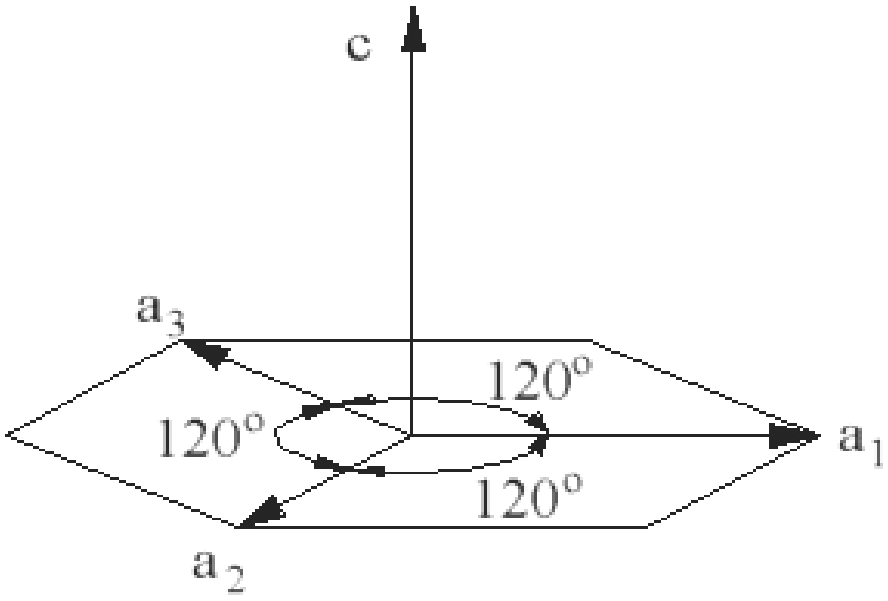

Figure 1.6 The Miller indices describing the hexagonal structure.

CHAPTER 2

SCHOTTKY BARRIER DIODES

2.1 Device Introduction

Schottky barrier diodes (SBDs) have many benefits compared to other rectifying devices, such as fast switching speeds and relatively easy fabrication. Couple this with the large amount of data that can be extracted through measurements and SBDs provide a great research platform. However, it is first necessary to understand the physics behind what makes a SBD work. Once this is established, then useful data can be taken and device characteristics extracted.

2.2 Ideal Electrostatics of Schottky Barrier Diodes

The formation of an ideal Schottky contact depends on the work functions of the two materials being brought into intimate contact with each other. When a metal and a semiconductor are brought together two outcomes are possible: either a Schottky contact or an ohmic contact can form. Both types of contacts are extremely important to solid state research.

A metal's work function is determined by the energy required to knock a valence electron from the metal into free space, or "vacuum". This measurement is often done through use of the photoelectric effect. The metal work function, Φ_m, is an intrinsic property of the metal and is constant assuming there is no worry of depleting the valence electrons; in other words, there are a lot of metal atoms. Thus, the metal work function,Φ_m, can be described as the vacuum level, E_o, subtracted from the energy level where the valence electrons sit, which is known as the metal's Fermi level, E_{fm}.

$$\Phi_m = E_0 - E_{fm} \tag{2.1}$$

A work function for the semiconductor, Φ_s, can also be defined using the steps as those for a metal. This concept can be seen in figure 2.1 with

$$\Phi_s = \chi + \left(E_C - E_{fs}\right)_{FB} \tag{2.2}$$

Where χ is known as the electron affinity and is an invariant property of the semiconductor. $(E_c - E_{fs})_{FB}$ is the difference between conduction band and semiconductor Fermi level under flatband conditions. Note that the equilibrium position of the Fermi level in the semiconductor is not an invariant value. It is positioned based on conductivity type and doping concentration meaning that $(E_c - E_{fs})_{FB}$ can be varied. This means that unlike the metal work function, the semiconductor's work function can be varied.

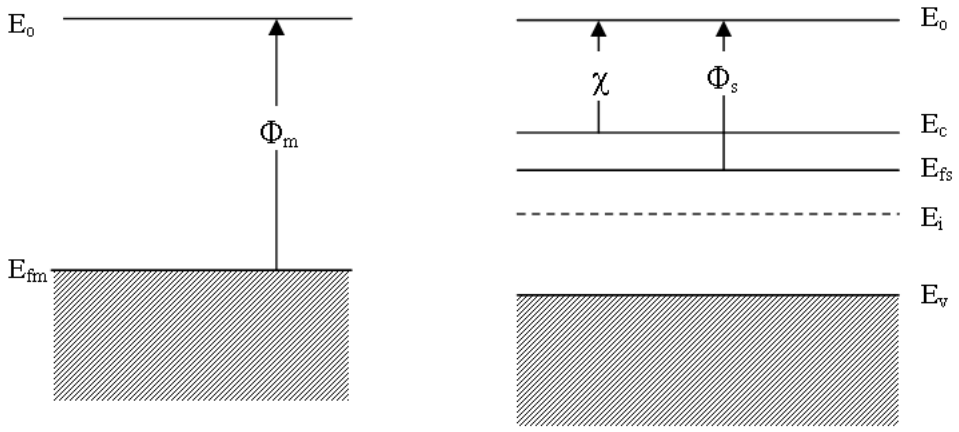

Figure 2.1 Separate equilibrium band diagrams of a metal (on the left) and n-type semiconductor (on the right)

Utilizing figure 2.1 as a visual guide, the Fermi levels of the two dissimilar materials do not match when the two material's vacuum levels are set equal. The instant the metal and semiconductor are brought together, their Fermi levels still do not equal.

However, a splitting in Fermi levels signifies non-equilibrium conditions exist. This is obviously not the case since no external perturbation is being applied. Therefore, to get to equilibrium conditions, transference of electrons between the semiconductor and the metal will occur. This will create a depletion region at the interface of the metal and

semiconductor. Under equilibrium conditions, the Fermi level is invariant with position as shown in figure 2.2.

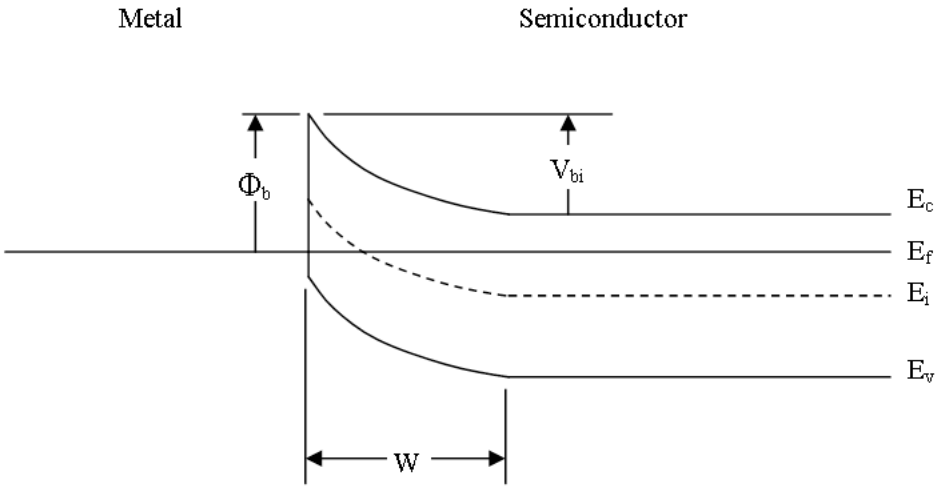

Figure 2.2 Equilibrium band diagram of rectifying Schottky contact on an n-type semiconductor

Depending on the difference in work function between the metal and semiconductor, an ideal metal-semiconductor contact can either be ohmic or rectifying. The rectifying contact as shown in figure 2.2 has a built-in voltage, V_{bi} that can be equated from the Schottky barrier height and semiconductor doping level as

$$V_{bi} = \frac{1}{q}\left[\Phi_b - \left(E_c - E_{fs}\right)_{FB}\right] \tag{2.3}$$

Where the Schottky barrier height $\Phi_b = \Phi_m - \chi$ and q is the charge on an electron. Using one-sided abrupt junction electrostatics, such as those used for p^+n junctions, the usual electrostatic variables can be obtained for non-punch through devices

Electric Field, $$E(x) = \frac{-qN_D}{K_s\varepsilon_0}\left(W - x\right) \tag{2.4}$$

Voltage, $$V(x) = \frac{-qN_D}{2K_s\varepsilon_0}\left(W - x\right)^2 \tag{2.5}$$

Depletion Width , $$W = \sqrt{\frac{2K_s\varepsilon_0}{qN_D}(V_{bi} - V_a)} \quad (2.6)$$

With the preceding variables defined as follows:

N_D is the doping of the semiconductor (in contact with the metal),

K_s is the permittivity of the semiconductor,

ε_o is the permittivity of free space,

V_a is the applied voltage to the Schottky contact,

x is distance from the metal-semiconductor interface

2.3 Forward and Reverse Bias

Now that the electrostatics of a SBD has been discussed, enough insight has been provided to look at the current flow of a forward biased SBD. Unlike its bipolar cousin, the pn-junction, a SBD is a unipolar device. In other words, the current flow is dominated by only one flavor of carrier; in this case it is the majority carrier.

Operation of a metal-semiconductor junction under forward and reverse bias is illustrated with Fig. 2.3 As a positive bias is applied to the metal (Fig. 2.3 (a)), the Fermi energy of the metal is lowered with respect to the Fermi energy in the semiconductor. This results in a smaller potential drop across the semiconductor. The balance between diffusion and drift is disturbed and more electrons will diffuse towards the metal than the number drifting into the semiconductor. This leads to a positive current through the junction at a voltage comparable to the built-in potential. As a negative voltage is applied (Fig. 2.3 (b)), the Fermi energy of the metal is raised with respect to the Fermi energy in the semiconductor. The potential across the semiconductor now increases, yielding a larger depletion region and a larger electric field at the interface.

The barrier, which restricts the electrons to the metal, is unchanged so that that barrier, independent of the applied voltage, limits the flow of electrons. The metal-semiconductor junction with positive barrier height has therefore a pronounced rectifying behavior. A large current exists under forward bias, while almost no current exists under reverse bias. The

potential across the semiconductor therefore equals the built-in potential minus the applied voltage, V_a.

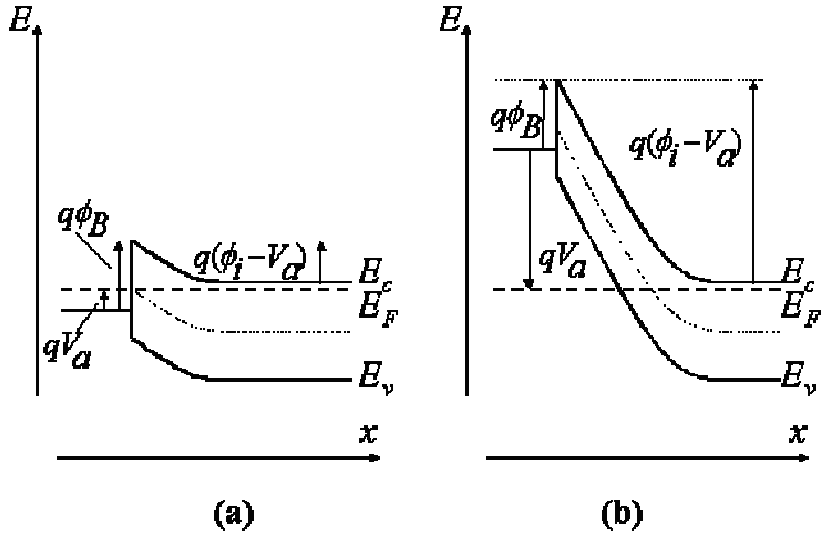

Figure 2.3 Energy band diagram of a metal-semiconductor junction under (a) forward and (b) reverse bias [19].

The current density, J, through the SBD can be given by the equation [4]:

$$J = A^{*}T^{2}e^{\frac{-q\Phi_b}{kT}}\left[e^{\frac{qV_a}{\eta kT}}-1\right] \tag{2.7}$$

where

Richardson's constant,

$$A^{*}=\frac{4\pi qm^{*}k^{2}}{h^{3}}=120\frac{m^{*}}{m}$$

T is the temperature,

V_a is the applied gate bias,

k is Boltzmann's constant and

n is the ideality factor.

To describe the current flow in a reverse biased SBD the following equation is used:

$$J = A^{*}T^{2}e^{\frac{-q\Phi_b}{kT}}\left[e^{\frac{qV_a}{\eta kT}}-1\right] \approx A^{*}T^{2}e^{\frac{-q\Phi_b}{kT}} \tag{2.8}$$

The approximation is made based on the exponentially decreasing effect of applied gate bias due to the negative applied bias, V_a. As can be seen from the reverse current equation 2.8, the barrier height, Φ_b, is an important variable to know as precisely as possible. As such, it is important to consider the image-force barrier lowering that occurs in a Schottky contact. This lowering of the potential barrier for carrier emission is known as the Schottky effect.

2.4 Capacitance in a Schottky Barrier Diode

A useful technique for determining not only barrier height, but also the average ionized doping concentration profile is measuring the capacitance, C, of a deeply depleted Schottky barrier diode.

To perform the measurement, a small a.c. signal is superimposed on top of a d.c. bias. The a.c. signal provides a measurable charge fluctuation at the edge of the depletion region. The d.c. bias is used to sweep the SBD further and further into reverse bias. This increasing depletion width reduces capacitance as given by

$$C = \frac{K_s \varepsilon_0 A}{W} \tag{2.9}$$

Where C is the measured capacitance and A is the area of the contact. Knowing the width of the depletion region as a function of applied bias from equation 2.6, a doping profile can be extracted from this measurement.

2.5 Breakdown Voltage in a Schottky Barrier Diode

An important characteristic of power devices is the blocking voltage that the device can handle before "breaking down". The breakdown of a device is characterized by the impact ionization of carriers within the depletion region. Applying larger reverse biases leads to an increase in the peak electric field inside the device as established by equation 2.4.

As the electric field grows, the acceleration of the carriers being swept through the depletion region is increased. The acceleration will increase to the point where the carrier has enough energy to ionize an atom in the semiconductor lattice, in other words, create an electron-hole pair. This is known as impact ionization. Impact ionization can begin to occur unbounded if the electron-hole pair that is originally created through impact ionization gains enough energy to impact ionize another lattice site, and the newly created electron-hole pair causes impact ionization at another site, and so on.

As newly created electron-hole pairs create their own new electron-hole pairs, an avalanche of electron-hole pair creation begins. This exponentially increasing avalanching causes the current to quickly tend towards negative infinity. As such, this snowball effect of electron-hole pair creation is aptly named avalanche breakdown. This occurs at the breakdown voltage, V_{bd}, which can be found as

$$V_{bd} = \frac{K_s \varepsilon_0 \varepsilon_{cr}^2}{2qN_D} \tag{2.10}$$

Where $\mathcal{E}_{cr}$ is the critical electric field and N_D is the doping of the substrate or epi-layer, provided the epilayer is not punched-through. This is the simplest definition of breakdown. For a more rigorous derivation, the reader is referred to [18].

2.6 Thermal Equilibrium of Schottky Barrier Diode

Electrons in the *n*-type semiconductor can lower their energy by traversing the junction. As the electrons leave the semiconductor, a positive charge, due to the ionized donor atoms, stays behind. This charge creates a negative field and lowers the band edges of the semiconductor.Electrons flow into the metal until equilibrium is reached between the diffusion of electrons from the semiconductor into the metal and the drift of electrons caused by the field created by the ionized impurity atoms. This equilibrium is characterized by a constant Fermi energy throughout the structure.

In thermal equilibrium, i.e. with no external voltage applied, there is a region in the semiconductor close to the junction which is depleted of mobile carriers and is called depletion region. The potential across the semiconductor equals the built-in potential.

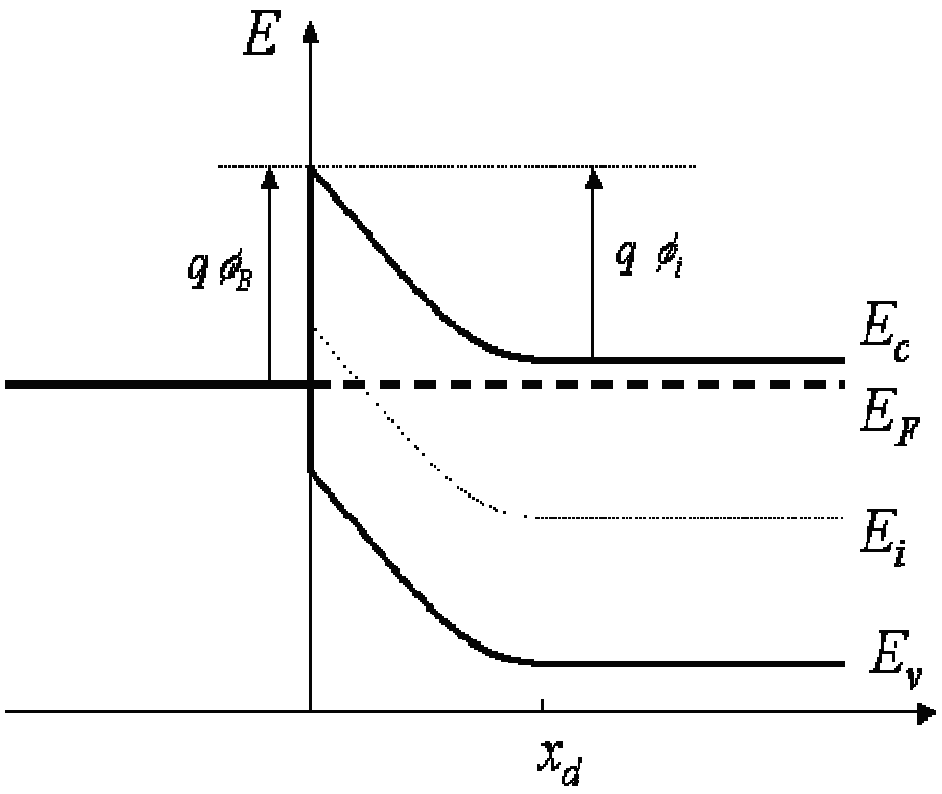

Figure 2.4 Energy band diagram of a metal-semiconductor contact in thermal equilibrium [19].

2.7 Survey of Schottky Diodes Structures

Many techniques have been tested in trying to improve Schottky contact diode characteristics. Based on layered nature of the photolithographic process most Schottky contacts are of a planar design. One of the problems encountered while utilizing planar contact geometries is the effects that occur at edge terminations.

A common technique to prevent electric field stress at edge terminals is buffering the edges of the metal contact with insulator. Research conducted by Ravi Chilukuri and B.J. Baliga at North Carolina State University implemented the usage of low energy Argon (Ar) implantation into the 4H SiC epilayer for planar edge termination[34]. An illustration of the design for the Schottky diode is shown in Figure 2.5. The Argon ion implantations can be seen to the left and right of the Schottky diode contact.

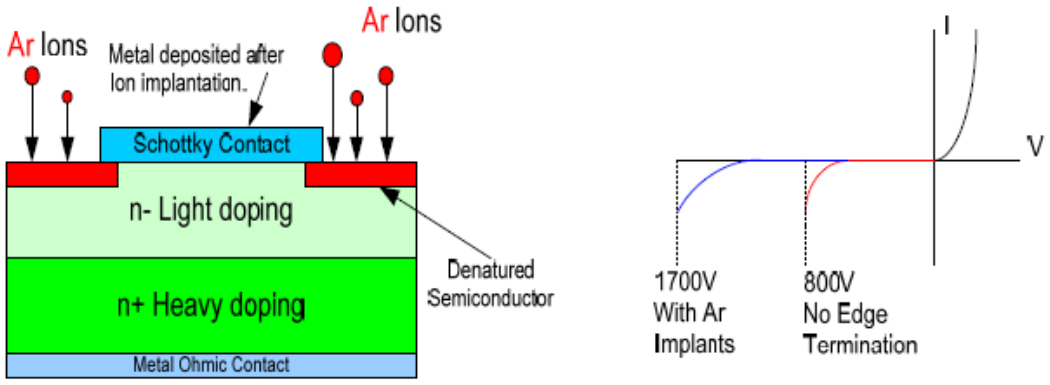

Figure 2.5 Nickel on SiC Schottky contact diode and I-V curve sketch of the performance difference obtainable by adding argon implantation edge termination to the diode design.

The diodes without edge termination were found to have a leakage current proportional to the diode diameter indicating a dominance of perimeter leakage where barrier height lowering occurred due to electric field crowding at the edge terminal.

The Schottky diodes constructed with the use of low energy argon implantation for planar edge termination were found to result in breakdown voltages above 1 kV. This technique

created a thin highly resistive layer at the edges of the planar metal contact where the doses of argon ions were implanted.

The quality of a Schottky contact and successful edge termination is measured by how closely the device can approach its theoretical breakdown voltage. The method discussed previously is a technique of buffering the edges with a highly resistive layer of denatured semiconductor. Another technique is to deposit a field plate insulator (typically a layer of oxide) over the semiconductor so that a Schottky contacts edge terminal may be protected by the field plate. This way fringing effects at the edge terminals are directed through the insulator field plate and not the semiconductor. Research conducted by M.C. Tarplee, V.P. Madangalri, Q. Zhang, and T.Sudarshan developed design rules for optimizing field plate thickness and metal contact overlap [35].

The computer simulation preformed by the group also showed that breakdown occurred directly underneath the corner of the unguarded Schottky contact. Electric field stress computer simulations allowed the team to make predictions as to what ratio of field plate thickness to metal contact overlap would be optimal. Figure 2.6 contrasts the diodes to show the benefit of oxide field plate termination. The concepts discussed in “Design Rules for Field Plate Edge Termination in SiC Schottky Diodes” provide a 4 step design process that may be used to optimize the oxide layer thickness and field plate overlap (Xo) when fabricating Schottky diodes [35].

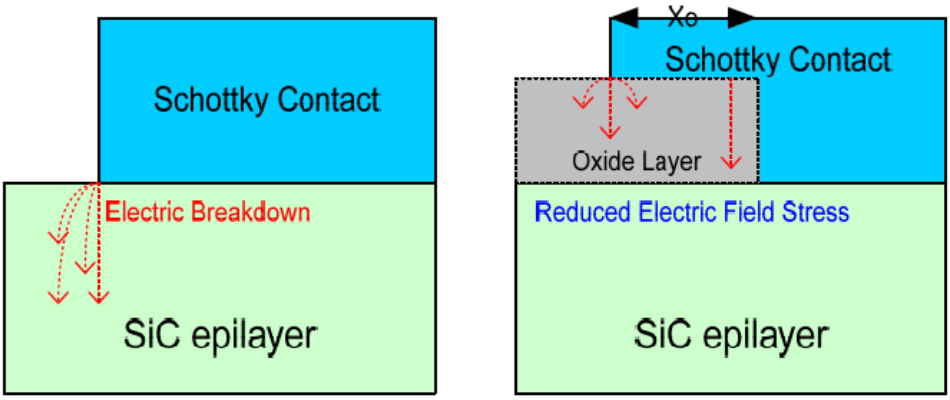

Figure 2.6 Schottky contact with and without oxide layer edge guard.

Another common technique to prevent electric field stress at edge terminations is guard rings. The importance of electric field distribution around a geometric design plays a major role in the development of ring guard terminations also referred to as field limiting rings FLR. Research performed by Seong-Jin Kim at Woosuk University studied the improvement of high voltage reverse breakdown characteristics of Schottky barrier diodes with ring guard terminations [36].

In this study no ring guard protection, a single guard ring protector, and multiple guarding protectors made from aluminium (Al) were deposited by using electron beam deposition and thermal treatment upon the SiC substrate. The aluminium oxidized and formed Al silicide at the deposited locations becoming an insulator.

The findings confirmed that the breakdown voltage characteristics were greatly dependant on the FLR width and spacing. When I-V curve analysis was performed on the device it was shown that the absence of ring guards had no effect on the forward conduction current. However the reverse leakage currents where greatly affected by the ring guard edge termination structure. Figure 10 illustrates the concept of ring guard termination similar to those discussed. Multiple ring guards could achieve breakdowns higher than -1.2 kV.

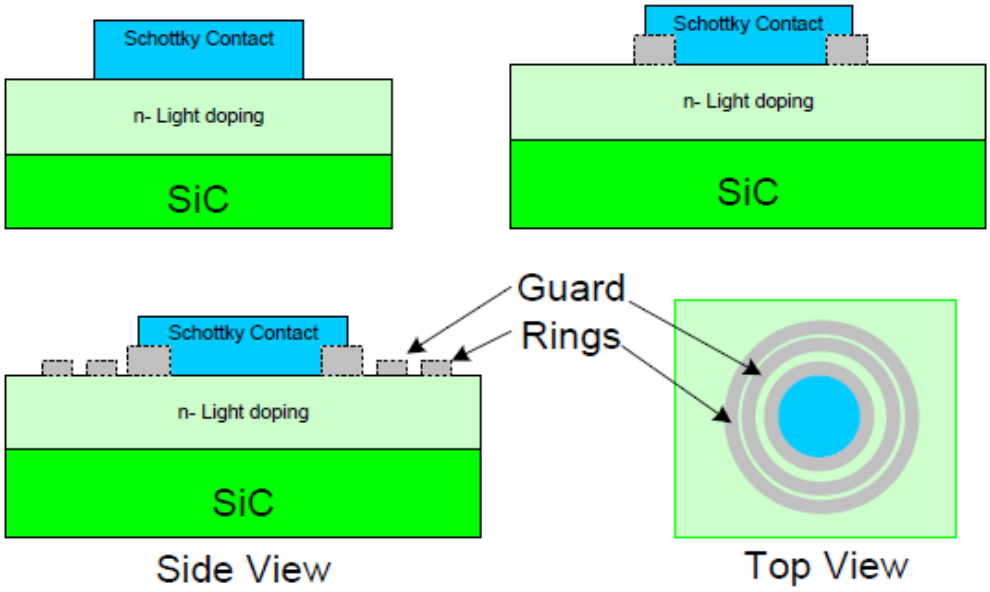

Figure 2.7 Diodes with different guard ring configurations for improved VRB, one with no ring guard, a single guard ring, and multiple guard rings for improved breakdown characteristics

CHAPTER 3

SiC SCHOTTKY BARRIER DIODE

3.1 General Introduction

Silicon carbide (SiC) power devices receive increasing attention in application fields of high voltage engineering and power transmission. Superior material properties make silicon carbide (SiC) a very promising candidate for high-power and high frequency devices [20]. For power device applications, SiC's large bandgap translates into a high critical field [21]. However, due to the difficulty in the formation of well-controlled metal/SiC interface, the reverse leakage current of Schottky barrier diodes can be significantly increased prior to junction breakdown [22]. An increase in reverse leakage current of SBDs leads to higher power loss and premature breakdown. It is therefore important to reduce reverse leakage current of Schottky barrier diodes.

Schottky barrier diodes (SBD) are unipolar devices, i.e. they do not inject minority carriers into a neutral region as do PN diodes. Since there is no minority charge storage, the turn of event is fast and the transient reverse current is small. As a result, the switching energy dissipated during turn-off is minimal. Hence, Schottky diodes eliminate the switching losses. SiC Schottky barrier diodes are attractive because the breakdown field of SiC is 8 to 10 times higher than for silicon. Hence, these are capable of operation at much higher temperatures than silicon devices.

Purdue University fabricated the 1700V 4H-SiC Schottky barrier diode using both Ni and Ti as Schottky metals. Figure 3.1 shows the cross section of SBD. The N-layer is 10-13 microns thick. The semiconductor under the edges of the Schottky contact is implanted with boron. Under reverse bias this produces a region containing a large density of deep levels that serve as charge trapping centres and accumulate a distributed charge that reduces the electric field crowding at the edges of Schottky contact [23].

The Schottky metal is covered with 1 micron of gold metallisation to reduce spreading resistance of the Schottky contact and the backside ohmic contact is formed by annealed nickel.

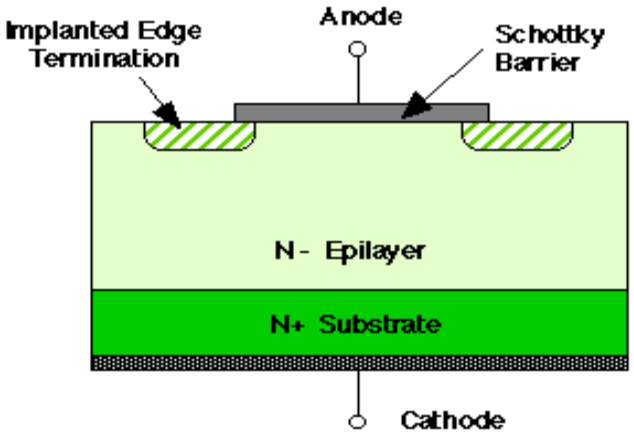

Figure 3.1 Cross section of SBD (After A. Itoh et al., Ref. 9)

The barrier heights for Ti and Ni on 4H-SiC at room temperature are 0.8 eV and 1.3 eV respectively and the lower barrier Ti gives lower forward voltage drop but higher leakage current as compared to the Ni barrier. The reverse blocking voltages are 1500 and 1720 volts respectively. In 1996, 4H-SiC Schottky barrier diodes having 1400 V with forward current densities over 700 A/cm2 at 2 V were demonstrated [24].

In 2001, the static and dynamic characteristics of large-area, high-voltage 4H-SiC Schottky barrier diodes were presented [25]. This device achieved the breakdown voltage greater than 1200 V and a forward current of 6 A, and enabled the use of SiC Schottky diodes in practical switching circuits.

3.1.1 Schottky Barrier Formation

When a metal and a semiconductor are brought in contact, the respective Fermi-levels must coincide in thermal equilibrium as shown in Figure 3.2 (b). There are two limiting cases such as the ideal case (referred to as Schottky-Mott limit [26]) and a practical case (known as the Bardeen limit [27]) to describe the relationship between a metal and a semiconductor. Figure 3.2 shows the energy band diagram for the ideal case (Schottky-Mott limit) with the absence of surface states.

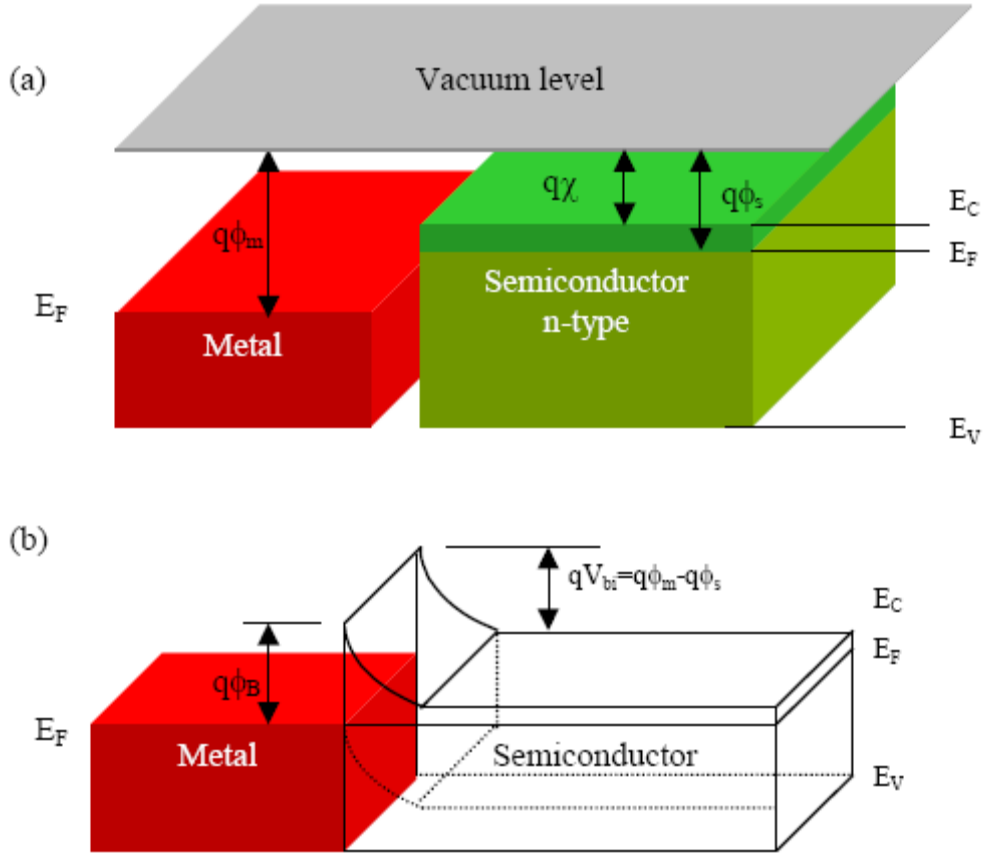

Figure 3.2 The formation of a barrier between the metal and the semiconductor when (a) neutral and isolated and (b) in perfect contact without any oxide between them (SchottkyMott limit) [26].

In this case the barrier height for n-type semiconductor can simply be determined to be the difference between the metal work function (ϕ_m) and electron affinity (χ_S) of the semiconductor;

$$q\Phi_{Bn} = q\left(\Phi_m - \chi_s\right) \tag{3.1}$$

For a given semiconductor and a metal, the sum of the barrier height on n- and p-type semiconductor is expected to be equal to the energy bandgap

$$q\left(\Phi_{Bn} + \Phi_{Bp}\right) = E_g \tag{3.2}$$

This relationship for Schottky-Mott limit implies that the control of the barrier height is achieved by the choice of the metal. The second limiting case is the Bardeen limit [27] where a large density of states is present at the semiconductor to metal interface. In the Bardeen limit the barrier height ϕ_B is completely independent of the metal work function ϕ_m in contrast to the Schottky-Mott limit and the Fermi level is said to be pinned by the high density of interface states.

3.1.2 Flow of Current

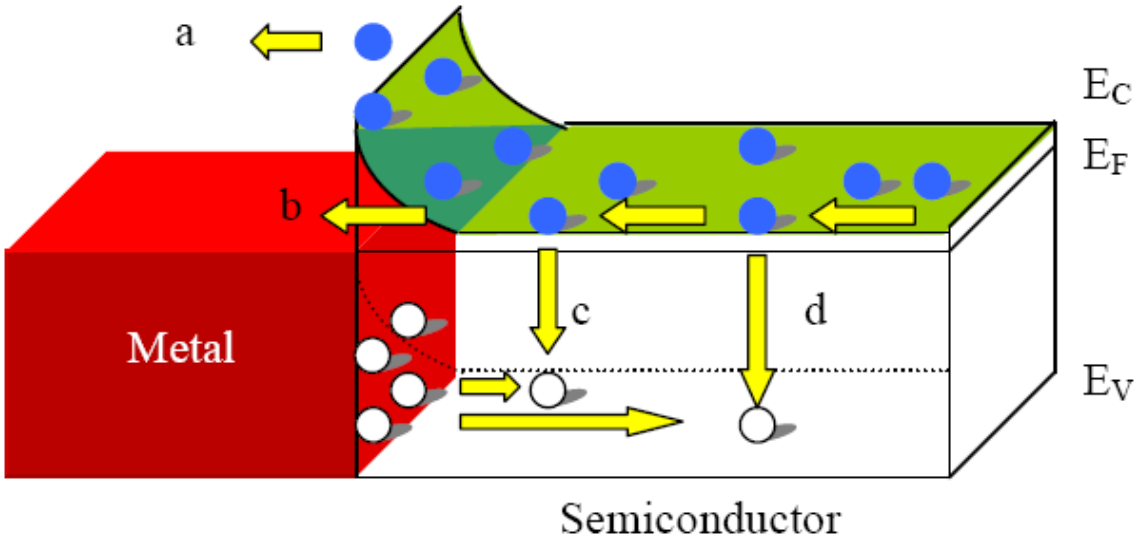

Figure 3.3 Current transport processes in a forward-biased Schottky barrier [28].

Figure 3.3 shows four basic transport processes for n-type semiconductors under forward bias [28]. The four processes are a) emission of electrons from the semiconductor over the top of the barrier into the metal, b) quantum mechanical tunnelling through the barrier, c) recombination in the space-charge region, and d) recombination in the neutral region (called hole injection). For the lowly doped semiconductor the current flows as a result of thermionic emission (TE) [29] as shown

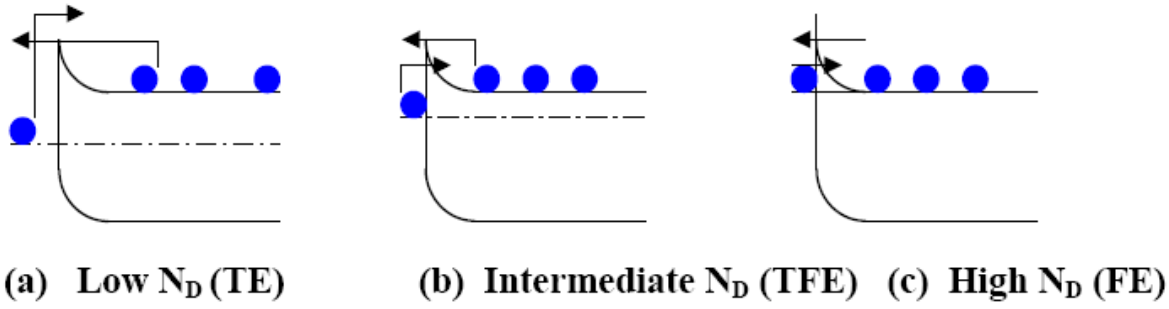

Figure 3.4 Energy band diagram for (a) low doped, (b) intermediate doped, and (c) high doped n-type semiconductor. The arrow indicates the electron flow.

in Figure 3.4 (a) with electrons thermally excited over the barrier. In the intermediate doping range, thermionic field emission (TFE) [30] dominates as shown in Figure 3.4 (b). For high doping, the barrier is sufficiently narrow at or near the bottom of the conduction band for the electrons to tunnel directly, known as field emission (FE).

3.2 Schottky Diode Performances

Schottky diodes are of interest for high-power devices because they are majority carrier devices and consequently have very fast switching times and no reverse recovery current. Here, some important properties of Schottky barrier diodes for power rectifiers will be described.

3.2.1 Specific on-Resistance

The specific on-resistance should be as low as possible for high power device operation.The specific on-resistance is given by

$$R_{on-sp} = \frac{W}{q\mu_n N_D} = \frac{4V_B^2}{e\mu_n E_C^3} \tag{3.3}$$

$$= \left(\frac{W}{q\mu_n N_D}\right)_{Epi-layer} + \left(\frac{W}{q\mu_n N_D}\right)_{substrate} \tag{3.4}$$

Where W is the thickness of epilayer and substrate, V_B is the breakdown voltage, q charge of electron, μ_n is electron mobility, N_D is doping, E_C is critical electric field.

3.2.2 Forward Voltage Drop

Forward voltage drop is given by the equation

$$V_F = \frac{\eta kT}{q} \ln\left(\frac{J_F}{A^* T^2}\right) + \eta\phi_B + R_{on-sp} J_F \tag{3.5}$$

Where η is the ideality factor, k is the Boltzman's constant, J_F is the forward current density, ϕ_B is barrier height, R_{on-sp} is specific on resistance and A^* is the Richardson's constant. The forward voltage drop (V_F) is a function of the temperature, Schottky barrier height, and specific on resistance.

3.2.3 Breakdown Voltage and Reverse Leakage Current

The breakdown is given by

$$V_B = \frac{\varepsilon_S E_C^2}{2qN_D} \tag{3.6}$$

The breakdown voltage depends on the critical field, epilayer doping and thickness, and edge termination. For a given epilayer thickness, a decrease in epilayer doping does not necessarily increase the breakdown voltage since the decrease in doping may correspondingly decrease the critical field. The reverse leakage current is given by the equation

$$J_L = -A^* T^2 \exp\left(\frac{-q\phi_B}{kT}\right) \tag{3.7}$$

The reverse leakage current is affected by Schottky barrier height, temperature, and image force barrier height lowering. The leakage current density of the Schottky rectifier increases rapidly with the temperature. Using equation 3.6, a plot of the leakage current of a Schottky rectifier as a function of the temperature and Schottky barrier height is shown in Figure 3.5. As shown in Figure 3-9, the leakage current density of the Schottky rectifier increases rapidly with the temperature.

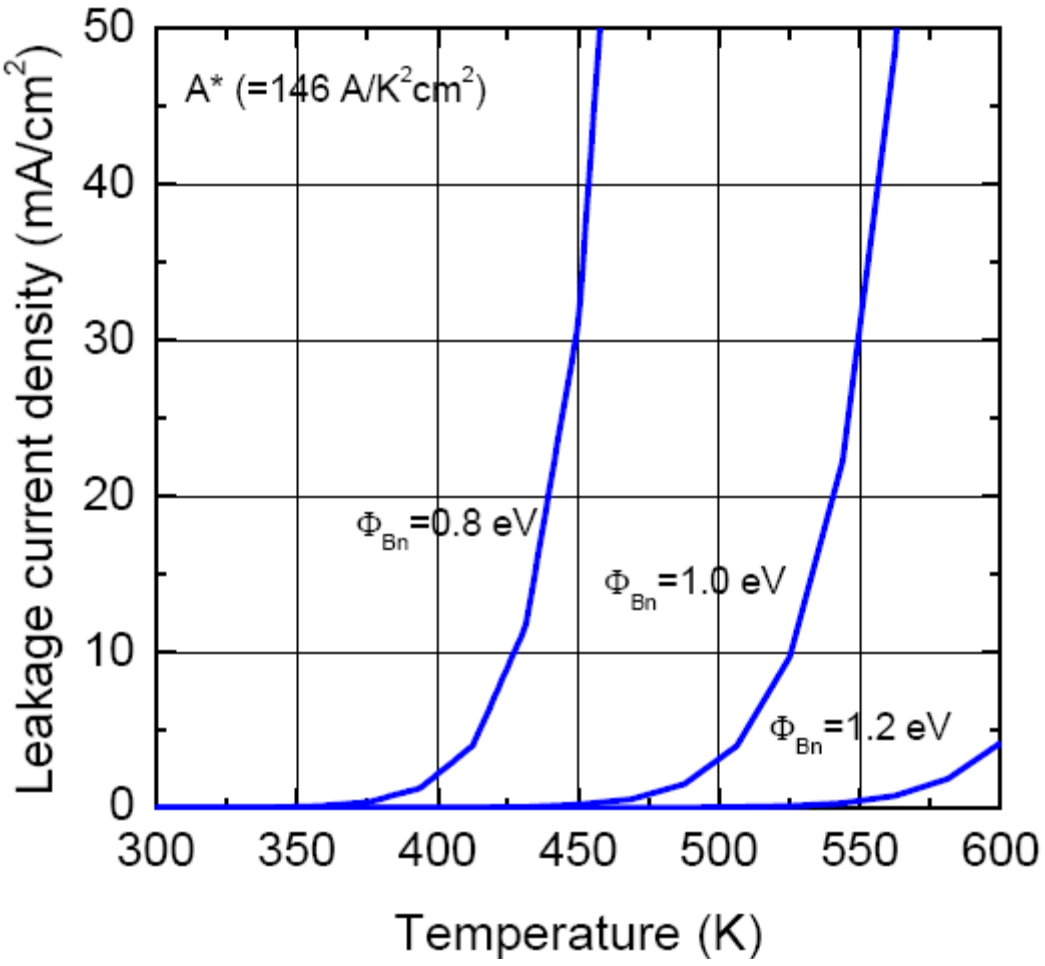

Figure 3.5 Reverse leakage current versus temperature and Schottky barrier Heights [30].

3.2.4 Schottky Barrier Lowering

There is a reduction of the Schottky barrier height due to the image force lowering, under reverse bias voltage. When an electron approach a metal, the requirement that the electric field must be perpendicular to the surface enables the electric field to be calculated as if there is a positive charge of magnitude q located at the mirror-image of the electron with respect to the surface of the metal.The barrier height reduction due to the image force lowering is given by [28].

$$\Delta\phi_B = \sqrt{\frac{qE_m}{4\pi\varepsilon_S}} \tag{3.8}$$

Where E_m is the maximum electric field given by

$$E_m = \sqrt{\frac{2qN_D}{\varepsilon_S}(V_R + V_{bi})} \tag{3.9}$$

Where V_R is the reverse bias voltage and V_{bi} is the built-in voltage for SiC. The leakage current density including the image force barrier height lowering can be given by

$$J_L = -A^* T^2 \exp\left(\frac{-\phi_B}{kT}\right)\exp\left(\frac{\Delta\phi_B}{kT}\right) \tag{3.10}$$

Figure 3.6 shows the calculated Schottky barrier height reduction due to the image force lowering effect as a function of the reverse bias voltage up to 10 kV.

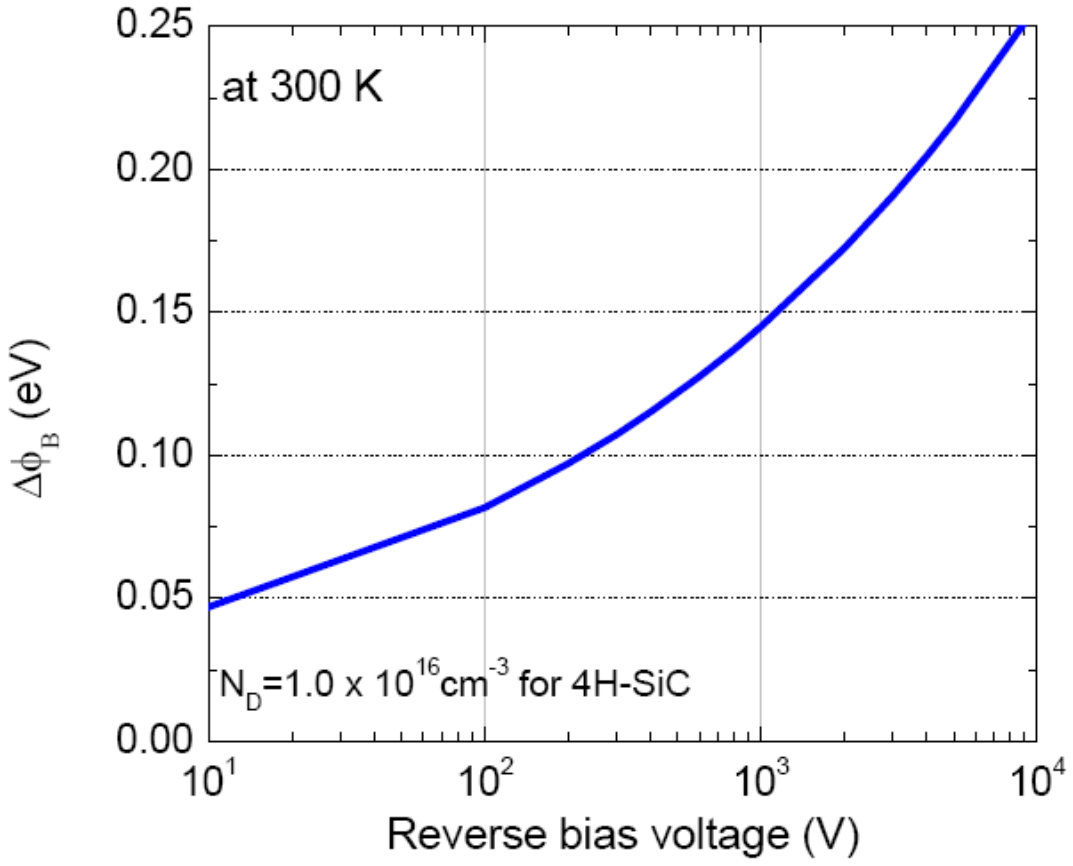

Figure 3.6 The calculated Schottky barrier height reduction at room temperature due image force lowering versus reverse bias voltage [28].

3.3 Other rectifiers

In order to achieve better reverse blocking characteristics while maintaining Schottky like forward conduction characteristics several modern rectifiers such as JBS, MPS, DMT, and TMBS have been developed and presented in the literature. The most common advantages and disadvantages of each device are presented in this section.

3.3.1 Junction Barrier Schottky (JBS) diodes

The junction barrier Schottky diode is a device which has the advantage of a low forward voltage drop while keeping a low leakage current at high blocking voltage. It is normally a Schottky structure with a normally implanted P+ grid into its drift region [38]. The schematic structure of a JBS diode is shown in Figure 3.7. The unipolar current flows through the conductive channels under the Schottky metal with a voltage drop that is normally determined by the Schottky barrier height like the Schottky diode in forward mode. In reverse conduction mode the p^+n junctions become reverse biased and the depletion layers spread into the channel and pinch-off the Schottky barrier. The spacing, width, and thickness of the p^+ grid are important design factors to optimize its performance. The total resistance which is a large contribution of an increasing voltage drop in JBS is the sum of the resistance in grid (R_{grid}), in drift (R_{drift}), and at backside Ohmic contacts ($R_{cathode}$) as shown in Figure 3.7. The contribution of backside Ohmic contacts to the voltage drop might be small and can be ignored. Because the contact resistance of annealed n-type Ni contacts is in the range of below 10^{-5} Ω cm^2, the voltage drop is in the range of 1 mV at 100 A/cm^2 [39].

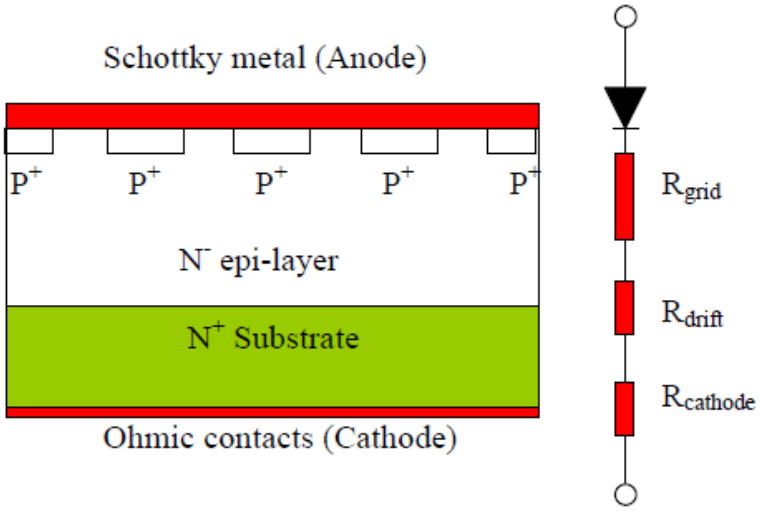

Figure 3.7 Schematic JBS diode structure and its equivalent circuit.

3.3.2 Merged P-i-N / Schottky (MPS) diodes

The MPS [38] is an attractive approach to reducing the switching losses in high voltage power rectification without increasing the on-state voltage drop. Figure 3.8 shows the schematic view of the MPS structure. The MPS is a similar approach as JBS rectifier. However, the operating mode of two rectifiers is different.

In the MPS rectifier, the PN junction becomes forward biased in the on-state, unlike the case of the JBS, because the drift region has a very high resistance due to its design for supporting high voltage during the reverse blocking. Reverse leakage current and breakdown voltage can be achieved by employing this MPS even though the performance of the reverse recovery behavior of the diodes does not reduce.

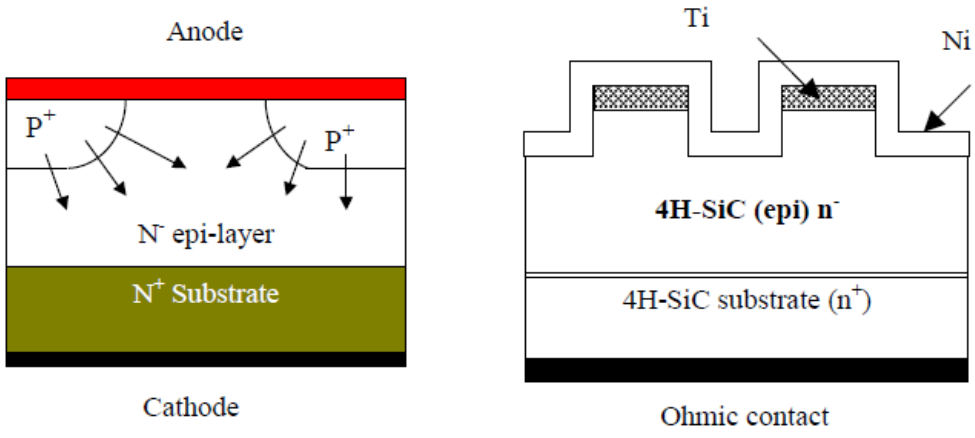

Figure 3.8 Schematic structure of MPS rectifier. Figure 3.9. Device structure of Ti/Ni dual metal-trench rectifier.

3.3.3 DMT (Dual metal trench) diodes

Recently, Schoen et al. [40] reported the DMT diode utilizing metals with two different barrier heights to achieve similar performance as conventional Schottky diode (see Figure 3.9). The DMT rectifier has advantages such as a simple structure (self aligned structure), simple process flow, and does not need an ion implantation process.

The DMT device had Ti deposited to achieve a low barrier height on top of the mesa followed by conformal deposition of Ni over the entire device to achieve high barrier height at the bottom of the trenches. The forward and reverse current reported for this device was between Ti and Ni Schottky barrier diode. In particular, a forward voltage drop close to that of Ti SBD but with leakage current two order of magnitude lower than that of Ti SBD and about a factor of two higher than Ni SBD. The DMT diode can be applied for applications such as lower voltage drop and lower leakage current.

3.3.4 TMBS (Trench MOS Barrier Schottky) diodes

Khemka et al. [41] reported that embedding a UMOS trench like grid instead of a pn junction grid as in the JBS/MPS rectifier yields a structure known as the TMBS rectifiers shown in Figure 3.10. The forward and reverse characteristics of a polysilicon planarized Ni-TMBS in 4H-SiC for two different Schottky areas (40% or 57%) were compared to that of simultaneously fabricated Ni SBD and a pin diode. A forward voltage drop of 1.75 V at 60 A/cm^2 and the reverse leakage current density of $6*10^{-6}$ A/cm^2 were obtained from this TMBS rectifiers.

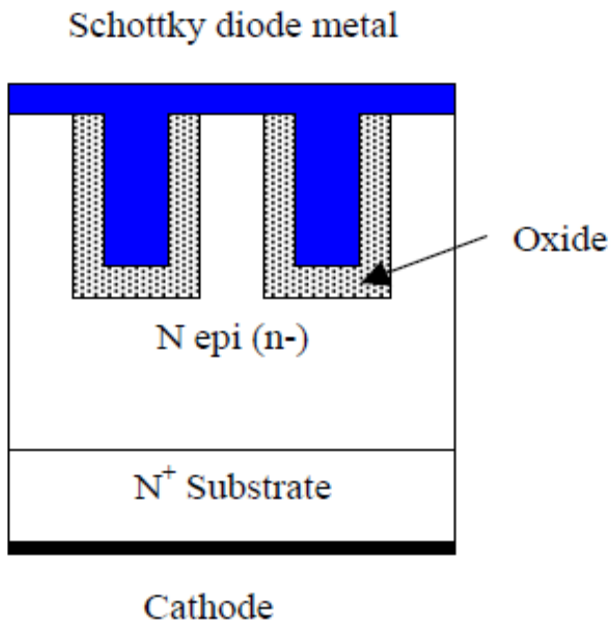

Figure 3.10 Schematic cross-section of a trench MOS barrier Schottky (TMBS) rectifier.

3.3.5 Schottky Rectifiers

The main advantage of wide band gap semiconductors for power device applications is the very low resistance of the drift region even when it is designed to support large voltages. This favours the development of high voltage unipolar devices which have much superior switching speed than bipolar structures. The Schottky rectifier, formed by making a rectifying contact been a metal and the semiconductor drift region, is an attractive unipolar device for power applications. In the case of silicon, the maximum breakdown voltage of Schottky rectifiers has been limited by the increase in the resistance of the drift region1. Commercially available devices are generally rated at breakdown voltages of less than 100 volts.

Many applications described above require fast switching rectifiers with low on-state voltage drop that can also support over 500 volts. The much lower resistance of the drift region for silicon carbide enables development of such Schottky rectifiers with very high breakdown voltages. These devices not only offer fast switching speed but also eliminate the large reverse recovery current observed in high voltage silicon rectifiers.

3.3.6 Shielded Schottky Rectifiers

In the case of silicon Schottky rectifiers, it has been traditional to trade-off the on-state (or conduction) power loss against the reverse blocking power loss by optimizing the Schottky barrier height. As the Schottky barrier height is reduced, the on-state voltage drop decreases producing a smaller conduction power loss. At the same time, the smaller barrier height produces an increase in the leakage current leading to larger reverse blocking power loss. It has been demonstrated that the power loss can be minimized by reducing the Schottky barrier height at the expense of a reduced maximum operating temperature. This optimization process is exacerbated by the rapid increase in the leakage current with increasing reverse bias voltage due to the Schottky barrier lowering phenomenon.

The first method proposed to ameliorate the barrier lowering effect in vertical silicon Schottky rectifiers utilized shielding by incorporation of a P-N junction. Since the basic concept was to create a potential barrier to shield the Schottky contact against high electric

fields generated in the semiconductor by using closely spaced P^+ regions around the contact, this structure was named the *'Junction-Barrier controlled Schottky (JBS) rectifier'*.

Subsequently, a novel silicon structure that utilizes the charge coupling concept was proposed to reduce the resistance in the drift region. Since these structures utilized an electrode embedded within an oxide coated trench region that surrounds the metal-semiconductor contact, this structure was named the *'Trench MOS Barrier controlled Schottky (TMBS) rectifier'*. The performance of this structure was further enhanced by using a graded doping profile to create a device named the *'Graded-Doped Trench MOS Barrier controlled Schottky (GD-TMBS) rectifier'*. This has allowed extending the breakdown voltage of silicon Schottky rectifiers to the 200 volt range. Yet another method proposed to create a potential barrier under the Schottky contact was the utilization of a second metal-semiconductor contact with large barrier height surrounding the main Schottky contact with a low barrier height. Since a stronger potential barrier could be created by locating the high barrier metal with a trench, this structure was named the *'Trench Schottky Barrier controlled Schottky (TSBS) rectifier'*.

CHAPTER 4

ANALYSIS OF 6H-SiC SCHOTTKY BARRIER DIODE

Si Schottky devices are severely limited to systems operating up to 200V due to their low critical field and high leakage current. Unlike Si devices, SiC SBDs can operate at breakdown voltages in excess of 5kV and junction temperatures over 400^0C.

In recent years there has been increasing interest and research into silicon carbide (SiC) as a semiconductor for use in high-temperature, high Power, and/or high radiation operating conditions under which silicon and conventional 111 V semiconductors can not adequately function. Of the two most common SiC polytypes investigated to date (6H-SiC and 3C-SiC),the 6H polytype has clearly yielded far superior electrical device results.

The barrier heights for Ti and Ni on 4H-SiC at room temperature are 0.8 eV and 1.3 eV respectively and the lower barrier Ti gives lower forward voltage drop but higher leakage current as compared to the Ni barrier. The reverse blocking voltages are 1500 and 1720 volts respectively. [37]

4.1 DERIVATION OF BASIC DEVICE EQUATION

For complementary error function carrier concentration is given by,

$$N(x) = N_0 erfc(h-x) \tag{4.1}$$

But we know that

$$erfc(h-x) = 1 - erf(h-x) \tag{4.2}$$

And

$$erf(h-x) = \frac{2}{\sqrt{\pi}} \int_0^{h-x} e^{-y^2} dy \tag{4.3}$$

On solving we get

$$erf(h-x) = \frac{2}{\sqrt{\pi}} \left[(h-x) - \frac{(h-x)^3}{3} + \frac{(h-x)^5}{10} \right] \tag{4.4}$$

Putting equation (4.4) into (4. 2),

$$erfc(h-x) = 1 - \frac{2}{\sqrt{\pi}}\left[(h-x) - \frac{(h-x)^3}{3} + \frac{(h-x)^5}{10}\right] \tag{4.5}$$

Now using Poisson's equation

$$-\frac{\partial^2 v}{\partial x^2} = \frac{\rho}{\varepsilon} \tag{4.6}$$

Where ε permittivity of semiconductor, ρ electric charge density and v is potential developed in the drift region.

We know that

$$\rho = eN(x) \tag{4.7}$$

Where $N(x)$ is the doping distribution

Put equation (4. 7) into (4.6)

$$-\frac{\partial^2 v}{\partial x^2} = \frac{eN(x)}{\varepsilon} \tag{4.8}$$

Put the value of $N(x)$ from (4.1) into (4.8),

$$-\frac{\partial^2 v}{\partial x^2} = \frac{e}{\varepsilon} N_0 erfc(h-x) \tag{4.9}$$

Put the value of $erfc(h-x)$ from (4.5) into (4.9),

$$-\frac{\partial^2 v}{\partial x^2} = \frac{e}{\varepsilon} N_0 \left[1 - \frac{2}{\sqrt{\pi}}\left\{(h-x) - \frac{(h-x)^3}{3} + ...\right\}\right] \tag{4.10}$$

After expanding $(h-x)^3$,

$$-\frac{\partial^2 v}{\partial x^2} = \frac{e}{\varepsilon} N_0 \left[1 - \frac{2}{\sqrt{\pi}}\left\{(h-x) - \frac{1}{3}\left(h^3 - x^3 - 3xh^2 + 3x^2 h\right) + ...\right\}\right] \tag{4.11}$$

Integrating equation (4.11),

$$-\frac{\partial v}{\partial x} = \frac{e}{\varepsilon} N_0 \left[x - \frac{2}{\sqrt{\pi}}\left\{\left(hx - \frac{x^2}{2}\right) - \frac{1}{3}\left(h^3 x - \frac{x^4}{4} - 3\frac{x^2}{2}h^2 + 3\frac{x^3}{3}h\right) + ...\right\}\right] + C_1 \tag{4.12}$$

We know that,

$$-\frac{\partial v}{\partial x} = E \tag{4.13}$$

Where E is the electric field in the drift region.

Now using boundary condition at x=h, E=0, then we get,

$$C_1 = -\frac{e}{\varepsilon} N_0 \left[h - \frac{2}{\sqrt{\pi}} \left\{ h - \frac{2}{\pi} \left(\frac{h^2}{2} - \frac{1}{3} \left(\frac{h^4}{4} \right) \right) + ... \right\} \right] \tag{4.14}$$

Putting value of C_1 into equation (12),

$$-\frac{\partial v}{\partial x} = \frac{e}{\varepsilon} N_0 \left[x - \frac{2}{\sqrt{\pi}} \left\{ \left(hx - \frac{x^2}{2} \right) - \frac{1}{3} \left(h^3 x - \frac{x^4}{4} - 3\frac{x^2}{2} h^2 + 3\frac{x^3}{3} h \right) + ... \right\} \right]$$
$$- \frac{e}{\varepsilon} N_0 \left[h - \frac{2}{\sqrt{\pi}} \left\{ h - \frac{2}{\pi} \left(\frac{h^2}{2} - \frac{1}{3} \left(\frac{h^4}{4} \right) \right) + ... \right\} \right] \tag{4.15}$$

Integrating equation (4.15) we get,

$$-v = \frac{e}{\varepsilon} N_0 \left[\frac{x^2}{2} - \frac{2}{\sqrt{\pi}} \left\{ \frac{x^2}{2} h - \frac{x^3}{6} - \frac{1}{3} \left(\frac{x^2}{2} h^3 - \frac{x^5}{20} - \frac{x^3}{2} h^2 + \frac{x^4}{4} h \right) \right\} \right]$$
$$- \frac{e}{\varepsilon} N_0 \left[hx - \frac{2}{\sqrt{\pi}} \left(\frac{x^2}{2} h - \frac{x}{12} h^4 \right) \right] + C_2 \tag{4.16}$$

Now using boundary condition at x=0 ,v=0 so that we can obtain C_2=0,

Again using boundary condition that x=w, v=v_{bi} , where w is the depletion region width and v_{bi} is the built in potential.

Putting x=w into equation (4.16),

$$-v_{bi} = \frac{e}{\varepsilon} N_0 \left[\frac{w^2}{2} - \frac{2}{\sqrt{\pi}} \left\{ \frac{w^2}{2} h - \frac{w^3}{6} - \frac{1}{3} \left(\frac{w^2}{2} h^3 - \frac{w^5}{20} - \frac{w^3}{2} h^2 + \frac{w^4}{4} h \right) \right\} \right] -$$
$$\frac{e}{\varepsilon} N_0 \left[hw - \frac{2}{\sqrt{\pi}} \left(\frac{w^2}{2} h - \frac{w}{12} h^4 \right) \right] \tag{4.17}$$

Rearranging above equation,

$$\frac{v_{bi} \varepsilon}{e N_0} = \left[\frac{W^5}{30\sqrt{\pi}} - \frac{W^4}{6\sqrt{\pi}} h + w^3 \left(\frac{h^2}{3\sqrt{\pi}} - \frac{1}{3\sqrt{\pi}} \right) - w^2 \left(\frac{1}{2} - \frac{h}{\sqrt{\pi}} + \frac{1}{3\sqrt{\pi}} h \right) + w \left(h - \frac{h^2}{\sqrt{\pi}} + \frac{h^4}{6\sqrt{\pi}} \right) \right] \tag{4.18}$$

In reverse bias condition above equation becomes,

$$\frac{\varepsilon\left(v_{rev}+v_{bi}\right)}{eN_0}=\left[\frac{W^5}{30\sqrt{\pi}}-\frac{W^4}{6\sqrt{\pi}}h+w^3\left(\frac{h^2}{3\sqrt{\pi}}-\frac{1}{3\sqrt{\pi}}\right)-w^2\left(\frac{1}{2}-\frac{h}{\sqrt{\pi}}+\frac{1}{3\sqrt{\pi}}h\right)+w\left(h-\frac{h^2}{\sqrt{\pi}}+\frac{h^4}{6\sqrt{\pi}}\right)\right] \tag{4.19}$$

But,

$$v_{rev} >> v_{bi}$$

So that we can write above equation,

$$v_{rev}\frac{\varepsilon}{eN_0}=\left[\frac{W^5}{30\sqrt{\pi}}-\frac{W^4}{6\sqrt{\pi}}h+w^3\left(\frac{h^2}{3\sqrt{\pi}}-\frac{1}{3\sqrt{\pi}}\right)-w^2\left(\frac{1}{2}-\frac{h}{\sqrt{\pi}}+\frac{1}{3\sqrt{\pi}}h\right)+w\left(h-\frac{h^2}{\sqrt{\pi}}+\frac{h^4}{6\sqrt{\pi}}\right)\right] \tag{4.20}$$

When breakdown condition occurs then,

$$v_{rev}=v_{bd}$$

Where v_{bd} is the breakdown voltage ,

$$v_{bd}\frac{\varepsilon}{eN_0}=\left[\frac{W^5}{30\sqrt{\pi}}-\frac{W^4}{6\sqrt{\pi}}h+w^3\left(\frac{h^2}{3\sqrt{\pi}}-\frac{1}{3\sqrt{\pi}}\right)-w^2\left(\frac{1}{2}-\frac{h}{\sqrt{\pi}}+\frac{1}{3\sqrt{\pi}}h\right)+w\left(h-\frac{h^2}{\sqrt{\pi}}+\frac{h^4}{6\sqrt{\pi}}\right)\right] \tag{4.21}$$

CHAPTER 5

CALCULATION AND RESULTS

Now calculation:

For calculation, we have used the following parameters with the value quoted against each of them:

Doping concentration $N_0 = 1\times10^{14} / cm^3$

Permittivity of free space $\varepsilon_0 = 8.85\times10^{-14}\left(\Omega - cm\right)^{-1}$ sec

Permittivity of SiC semiconductor $\varepsilon_s = 9.7\varepsilon_0$

Electron charge $e = 1.6\times10^{-16} Coulomb$

First we have to calculate device height by using equation of uniform doping profile

which is given below:

$$w = h = \sqrt{\frac{3\varepsilon_s v_{bd}}{e\Delta N_d}} \tag{5.1}$$

Taking breakdown voltage v_{bd} = 10 kV

After simplifying we get

h = 400μm

Now taking critical electric field on the basis of our complementary error function profile

$$E_c = \left(\frac{e\alpha w^2}{8\varepsilon_s}\right) \tag{5.2}$$

Where α impurity gradient and is given by equation,

$$\alpha = \frac{dN}{dx} \tag{5.3}$$

Based on the above equation avalanche breakdown is given by,

$$v_b = \frac{2}{3} E_c w \qquad (5.4)$$

Table 5.1 Variation of depletion region width with breakdown voltage h=330(μm)

S.N.	Breakdown Voltage v_{bd} (volt)	Depletion region width w(μm)	$v_b = \frac{2}{3} E_c w$ (volt)
1	1000	17	60
2	2000	35	166
3	3000	54	611
4	4000	74	1570
5	5000	97	3542
6	6000	121	6800
7	7000	149	12000
8	8000	182	23000
9	9000	225	44000
10	10000	330	

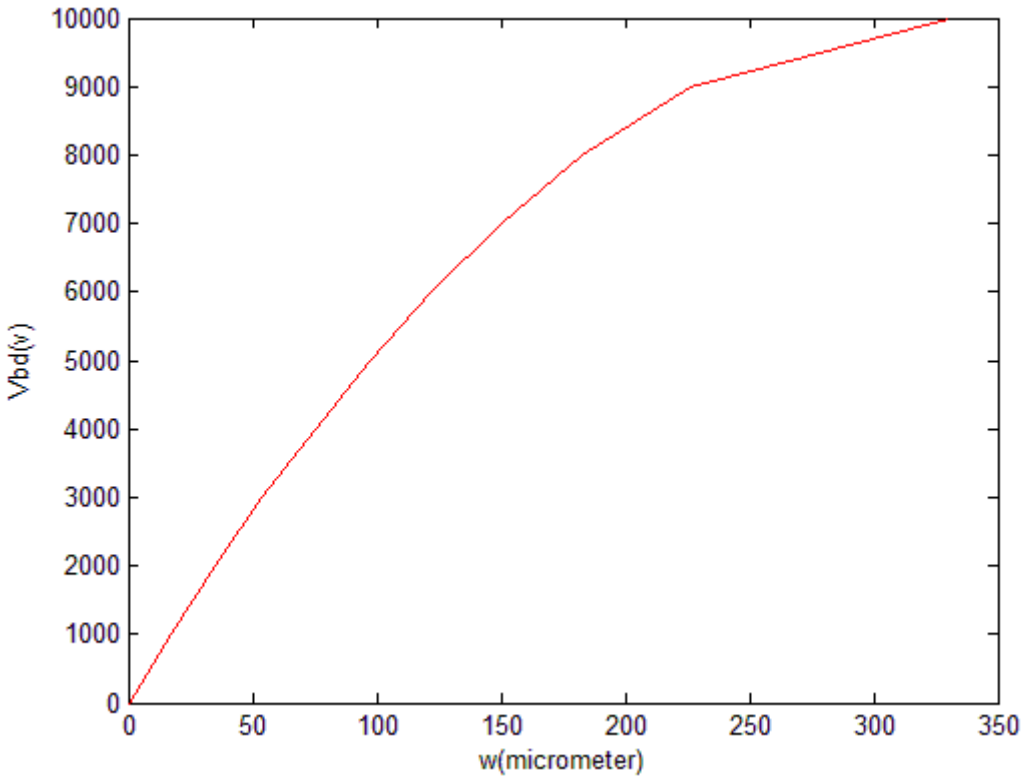

Figure 5.1 Plot of breakdown voltage with variation of depletion width

Table 5.2 Variation of breakdown voltage with depletion region width (w) for different values of h

S.N.	v_{bd} (volts)	h=330(μm) w (μm)	h=350(μm) w (μm)	h= 400(μm) w (μm)
1	1000	17	16	14
2	2000	35	33	28
3	3000	54	50	43
4	4000	74	69	59
5	5000	97	89	76
6	6000	121	111	93
7	7000	149	135	111
8	8000	182	162	131
9	9000	225	193	152
10	10000	311	295	175

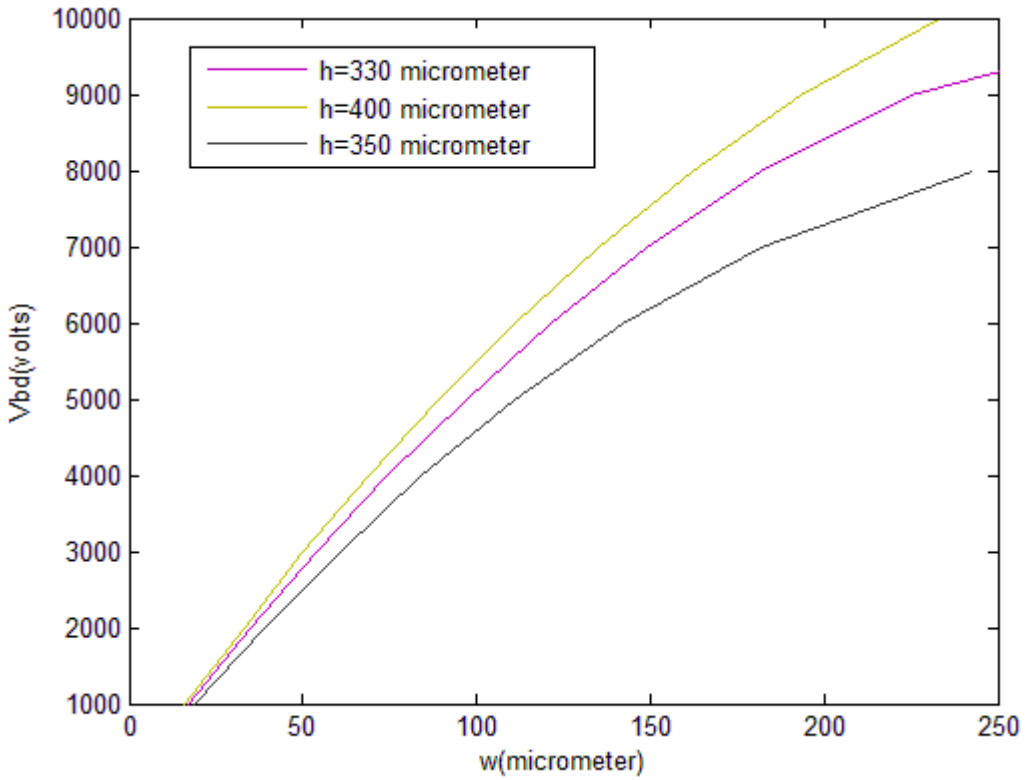

Figure 5.2 Plot of breakdown voltage with depletion region width (w) for different values of h

Table 5.3 Variation of breakdown voltage with height (h) for w=100 μm

S.N.	Height (h) (μm)	Breakdown voltage v_{bd} (volts)
1	100	929.3273
2	150	1854.3
3	200	2774
4	250	3688.4

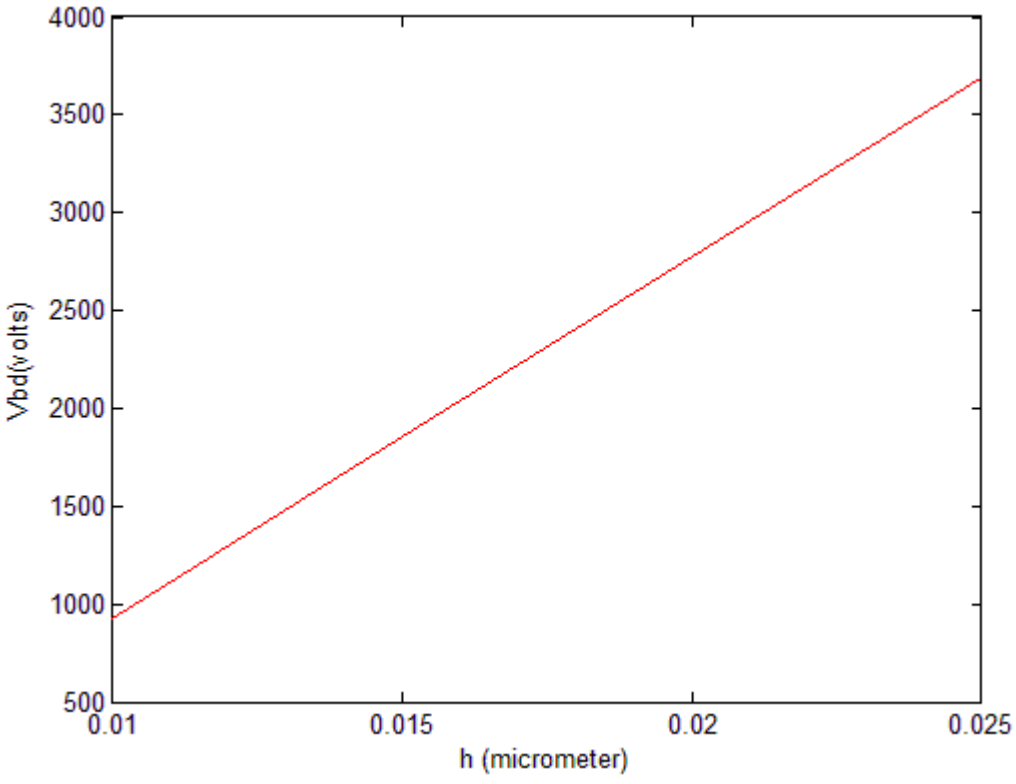

Figure 5.3 Plot of variation of breakdown voltage with height

Table 5.4 Variation of breakdown voltage with different doping levels (N_0)

S.N.	N_0/cm^3	For h=100 µm Breakdown voltage (volts)	For h=200 µm Breakdown voltage (volts)	For h=250 µm Breakdown voltage (volts)
1	1e14	929.3273	2774	3688.4
2	1e15	9293.273	27740	36884
3	1e16	92932.73	277400	368840
4	1e17	929327.3	2774000	3688400

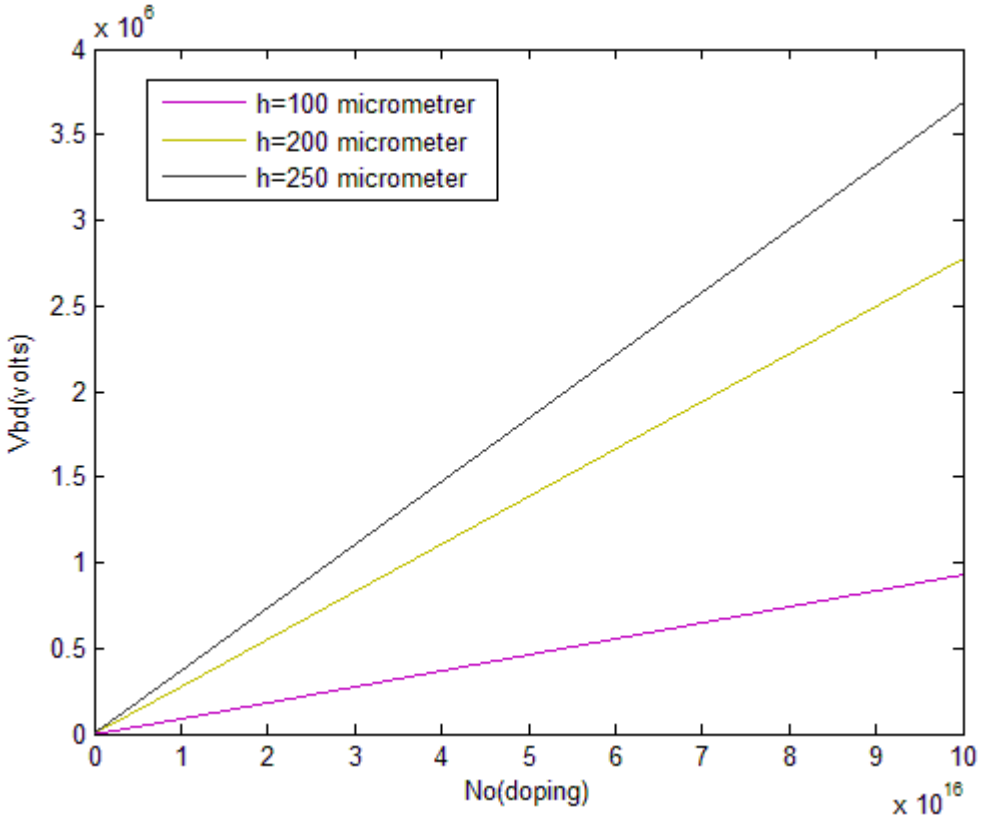

Figure 5.4 Plot of variation of breakdown voltage with different doping levels (N_0)

Table 5.5 Variation of breakdown voltage (v_{bd}) with drift region height (h) for different values of doping (N_0)

S.N.	Height (h) μm	Breakdown voltage (volts) For N_0=1e14	Breakdown voltage (volts) For N_0=1e15	Breakdown voltage (volts) For N_0=1e16
1	100	929.33	9293.3	92933
2	150	1854.3	18543	185430
3	200	2774	27740	277400
4	250	3688.4	36884	368840

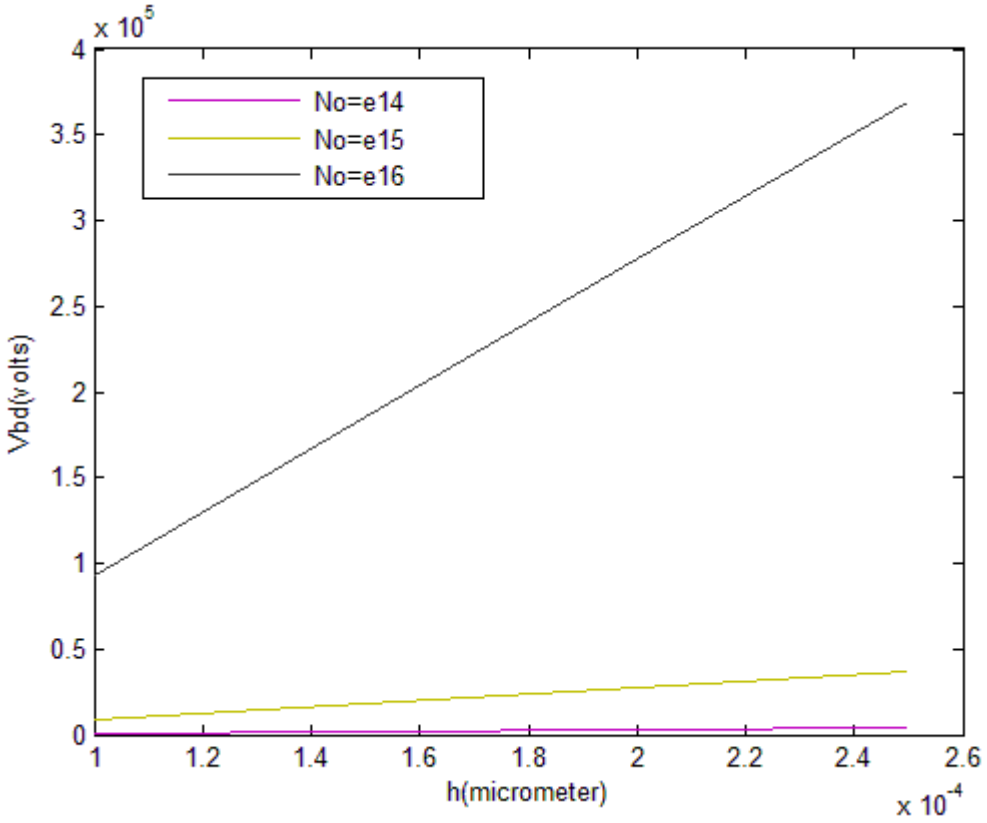

Figure 5.5 Plot of variation of breakdown voltage (v_{bd}) with drift region height (h) for different values of doping (N_0)

Table 5.6 Variation of breakdown voltage with depletion region width (w)

S.N.	Depletion region width w(μm)	Breakdow n voltage (volts) For N_0=1e14 N_0/cm^3
1	100	3688.4
2	120	4206.6
3	140	4651.4
4	160	5022.4
5	180	5319.5
6	200	5542.6
7	220	5691.6
8	240	5766.1
9	260	5766.1

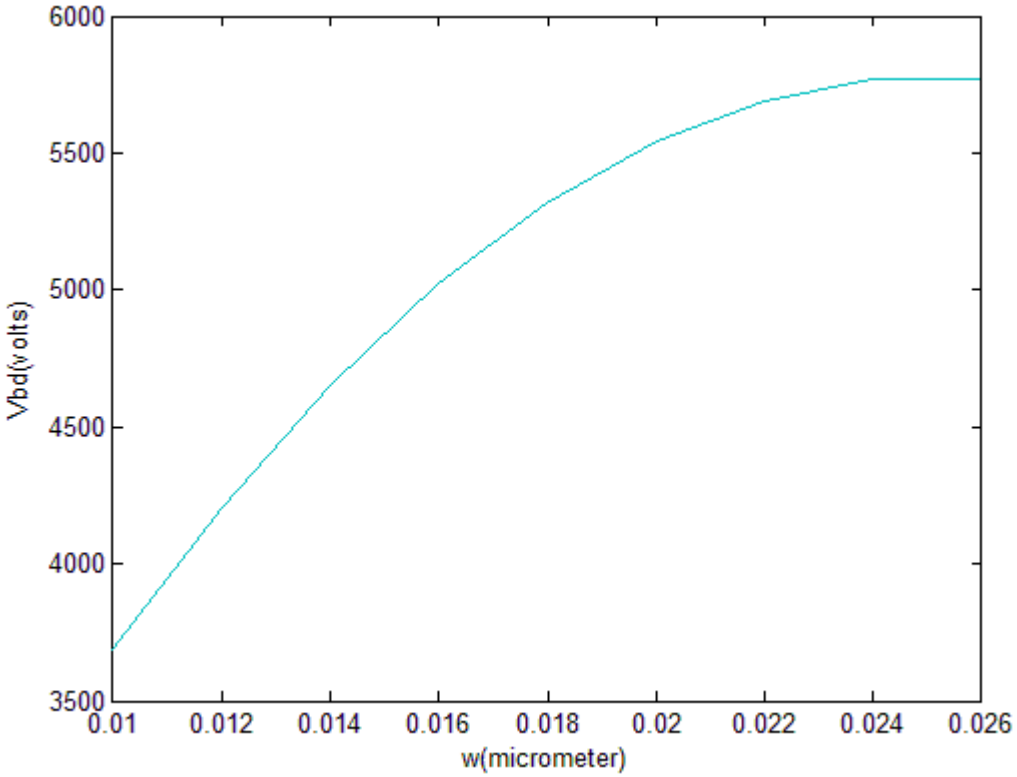

Figure 5.6 Plot of variation of breakdown voltage with depletion region width (w)

CHAPTER 6

CONCLUSION

SiC Schottky barrier diodes are attractive because the breakdown field of SiC is 8 to 10 times higher than for silicon. Hence, these are capable of operation at much higher temperatures than silicon devices.

The equation for breakdown voltage for 6H-SiC Schottky Barrier Diode, using complementary error function doping profile in drift region, was derived. Equation showed that the value of Breakdown voltage depends on height (h) of drift region and doping level.

For different values of height (h), breakdown voltages (Punch through and Avalanche) and its corresponding depletion region width was calculated and was plotted in Figure 5.2.For drift region height h= 330 μm, $N_0 = 10^{14}$ cm^{-3}, we got drift region width w= 121 μm at the breakdown voltage of 6 kV and at the breakdown voltage of 6 kV Avalanche breakdown voltage was 6.8 kV. Hence punch through breakdown will occur before Avalanche breakdown. It was seen from figure 5.3 that by with increase in drift region height, breakdown voltage was found to increases. For different values of doping level, the breakdown voltage was calculated and plotted in Figure 5.5. For larger drift region height, depletion region width is very small even for higher breakdown voltages and it could be improved further.

For the same height, breakdown voltage for other doping profiles like uniform, linearly graded could be calculated and could be compared with the complementary error function profile results given in this work.

REFERENCES

[1] J.J. Berzelius, Ann. Phys. Lpz., 1 (1824) 169-230.

[2] H. Moissan, C.R. Acad. Sci. Paris, 140,405, (1905).

[3] E.G.Acheson, Engl..Pat. 17911 (1892).

[4] H.J. Round, Electric World, 19 (1907) 309.

[5] J.A. Lely, Ber.Deut. Keram. Ges., 32 (1955) 229.

[6] Y.M. Tairov, V.F. Tsvetskov, J. Cryst. Growth, 43, 209, (1978).

[7] M. Syväjärvi, PhD thesis, Linköping University (1999).

[8] W. F. Knippenberg, Philips Res. Rep. 18. (1963).

[9] C. Carter, Jr., R. Glass, M. Brady, D. Malta, D. Henshall, S. Mueller, V.Tsvetkov,

[10] P.G. Neudeck, IEEE Electron Device Lett. 15 (1994) 63.

[11] N.W.Ashcroft, N.D. Mermin, "Solid State Physics", chap.28.

[12] An-Ben Chen, P. Srichaikul, Phys. Stat. Sol. (b) 202 (1997) 81-106.

[13] H.M. Hobgood, D.L. Barrett, J.P. McHugh, R.C. Clarke, S. Sriram, A.A. Burk, J. Greggi, C.D. Brandt, R.H. Hopkins, W.J. Choyke, J. Crystal Growth 137 (1994) 181-186.

[14] T. Troffer, C. Hassler, G. Pensl, K.Holzlein, H. Mitlehner, J. Volkl, Inst. Phys. Conf. Ser. 142, (1996) 281-4.

[15]. M. Bhatnagar and B. J. Baliga, "Comparison of 6H-SiC, 3C-SiC, and Si for power devices," IEEE Trans. On Electron Devices, 40 (3), pp. 645-655, March 1993.

[16]. K. Shenai, R. S. Scott, B. J. Baliga, "Optimum semiconductors for high-power electronics," IEEE Transactions on Electron Devices, 43(9), pp. 1811-1823, Sept. 1989.

[17]. A Elasser, M. Kheraluwala, M. Ghezzo, R. Steigerwald, N. Krishnamurthy, J. Kretchmer, and T. P. Chow, "A comparative evaluation of new silicon carbide diodes and state-of-the-art silicon diodes for power electronic applications," IEEE IAS Annual Meeting Conference Proceedings, pp. 341-345, 1999.

[18] S. Sze, Physics of Semiconductor Devices. Wiley-Interscience, 2nd ed., 1986.

[19] Bart Van Zeghbroeck "Principles of Semiconductor Devices",2007

[20] H. J. Na , H. J. Kim et al: Mater. Sci. Forum Vol. 389-3 (2002), p. 1383

[21] Schoen, K.P., Woodall, J.M., Cooper, J.A., Melloch, M.R. : IEEE Trans. Electron Devices, Vol.45 (1998), p. 1595.

[22] Crofton, J., Sriram, S.: IEEE Trans. Electron Devices, Vol.43 (1996), p. 2305.

[23]. A. Itoh, T. Kimoto, and H. Matsunami, "Excellent reverse blocking characteristics of high-voltage 4H-SiC Schottky rectifiers with boron-implanted edge termination", IEEE Electron Device Lett., 1996, 17, 139-141.

[24]. C. Weitzel, J. Palmour, C. Carter, K. Moore, K. Nordquist, S. Allen, C. Thero, and M. Bhatnagar, "Silicon carbide high-power devices", IEEE Trans. Electron Devices, 1996, 43, 1732-1741.

[25]. D. T. Morisette, J. A. Cooper, Jr., M. R. Melloch, G. M. Dolny, P. M. Shenoy, M. Zafrani, and J. Gladish, "Static and dynamic characterization of large area high-current-density SiC Schottky diodes", IEEE Trans. Electron Devices, 2001, 48, 349-352.

[26] N. F. Mott, *Proc. Cambr. Phil. Soc.* vol. 34, 1938.

[27] J. Bardeen, *Phys. Rev.* vol. 71, pp. 717, 1947.

[28] E. H. Rhoderick and R. H. Williams, *Metal-Semiconductor Contacts*, vol. 19, 2nd ed. Oxford: Clarendon Press, 1988.

[29] H. A. Bethe, *MIT Radiat. Lab. Rep.* vol. 43-12, 1942.

[30] F. A. Padovani and R. Stratton, *Solid-State Electron.* vol. 9, pp. 695, 1966.

[31] H. Morkoc, S. Strite, G. B. Gao, M. E. Lin, B. Sverdlov, and M. Burns, *J. Appl. Phys.* vol. 76, pp. 1363, 1994.

[32] CREE Research Inc., N.C., U.S.A.

[33] T. Kimoto, H. Nishino, W. S. Yoo, and H. Matsunami, *J. App. Phys.* vol. 73, pp. 726, 1993.

[34] Ravi K. Chilukuri and B. Jayant Balagia, "High Voltage Ni/4H-SiC Schottky Rectifiers" North Carloina State University. pg. 161-164 IEEE article 1999

[35] Marc C. Tarplee "Design Rules for Field Plate Edge Termination in SiC Schottky Diodes" IEEE Transactions on Electron Devices Vol 48. No. 12, pg. 2659-2654 December 2001

[36] Seong- Jin Kim "Breakdown Voltage Characteristics of SiC Schottky Barrier Diode with Aluminum Deposition Edge Termination" Woosuk University Jounel of the Korean Physical Society pp. S768 – S773 Vol 49 December 2006

[37] Maejo international journal of science and technology 2008.

[38] B. J. Baliga, *Modern Power Devices*. New York: Wiley, 1987.

[39] J. Crofton, P. G. McMullin, J. R. Williams, and M. J. Bozack, *J. Appl. Phys.*, vol. 77, pp. 1317, 1995.

[40] K. J. Schoen, J. P. Henning, J. M. Woodall, J. A. Cooper Jr., and M. R. Melloch, *IEEE Electron Device Lett.* vol. 19, pp. 97, 1998.

[41] V. Khemka, V. Ananthan, and T. P. Chow, *IEEE Electron Device Lett.*, vol. 21, pp. 286, 2000.