Performance
of
Multistage Interconnection Networks
for
Multiprocessor Systems

A Thesis
submitted for the award of the degree of
DOCTOR OF PHILOSOPHY
by

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September 2010

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CERTIFICATE

I hereby certify that the work which is being presented in this thesis, "Performance of Multistage Interconnection Networks for Multiprocessor Systems", for the award of degree of "Doctor of Philosophy", submitted to the Department of Computer Science and Engineering, Thapar University, Patiala, is an authentic record of my own work, carried out under the supervision of Dr. P. K. Bansal and Dr. Seema Bawa. It refers to other researchers' works, which have been duly listed in the reference section.

The matter presented in this thesis has not been submitted in part or full to any other institute or university, for the award of any other degree.

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This is to certify that the above statement made by the candidate is correct and true to the best of my knowledge.

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Abstract

Multistage Interconnection Network (MIN) is one of the major components of a multiprocessor system. MIN provides an interconnection either between processor to processor or between processor and memory modules. MINs meet the communication needs in multiprocessor systems in a cost-effective manner. The performance of the multiprocessor system depends largely on the MIN that enables multiple processors to communicate among themselves or with memory modules. In this thesis, four new fault-tolerant MINs have been proposed for multiprocessor systems. Here, four new fault-tolerant MINs have been proposed namely M_ASEN, M_FDOT, Hybrid and M_QUAD. M_ASEN belongs to Regular category and the rest three are of Irregular in category. These MINs make use of multiple path feature to incorporate fault-tolerance. Each of the designed MIN making use of Chaining of SEs within each stage and an extra fault-tolerant subnetwork. The design procedure, mathematical function for routing algorithm for each of the proposed MINs has been presented along with the evaluation of various performance parameters. Each of the designed MIN has been analyzed in terms of the performance parameters - probabality of acceptance, bandwidth, fault-tolerance, reliability, path length, hardware complexity and cost, and permutations passable. Finally, the performance of the proposed MINs has been compared with the existing MINs of similar type and it turns out that the designed MINs are better in terms of most of the performance parameters.

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Chapter 1

Introduction

Interconnection Network (IN) is one of the major components of a multiprocessor system that enables the processors to communicate among themselves or with memory modules.

1.1 Multiprocessor System

Principle characteristic of a multiprocessor system is the ability of each of its processors to share access to common sets of main memory modules and peripheral devices. An IN structure is used between the memories and processors (and between memories and input-output channels, if needed) in multiprocessor systems as shown in Figure 1.1.

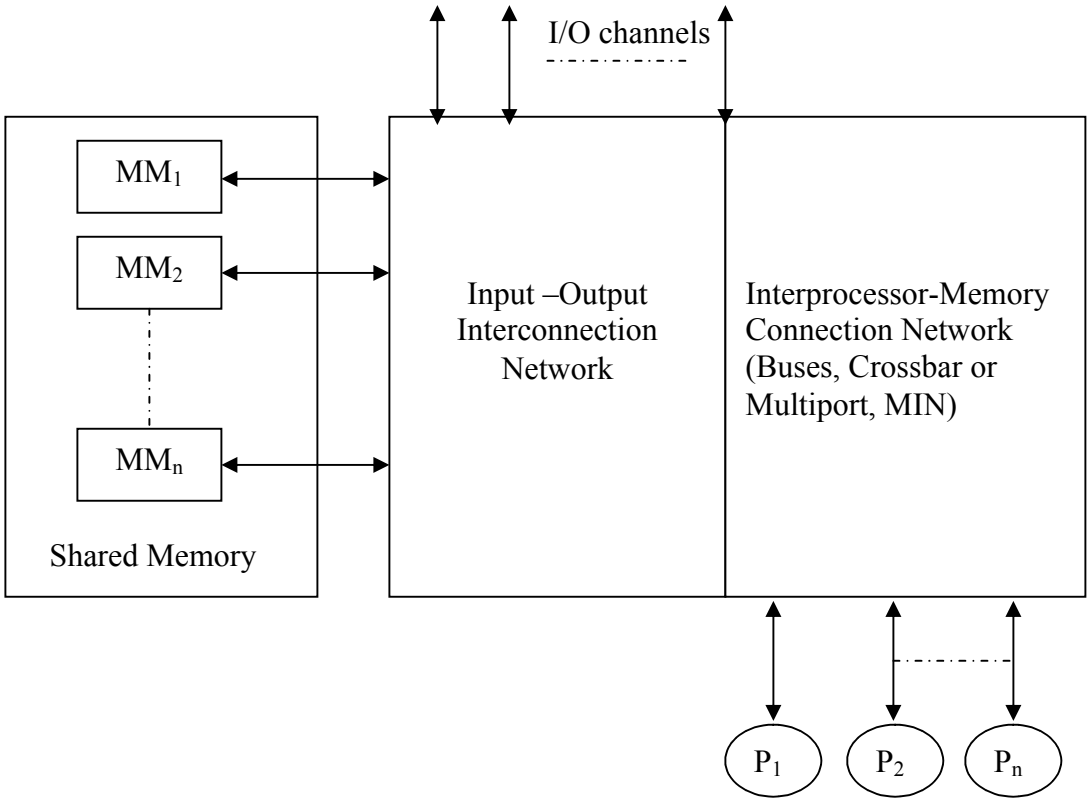

Figure 1.1 : Multiprocessor System

INs are the backbone for multiprocessor systems. As sequential computers are reaching their limits, the common approach to enhancing the performance is to design multiprocessor systems. Basically, there are two architectures of shared memory multiprocessor systems : the Uniform Memory Access (UMA) and the Non-Uniform-Memory-Access (NUMA). In the UMA model, multiple processors share a set of memory modules and an interconnection network provides interaction between them. In the NUMA model, each processor is associated with its local memory and the IN provides an interconnection between processors. Research in the area of INs has been active world-wide for several decades. The milestone represented by non-blocking IN by Clos is dated 1953. Since then a lot of progress has taken place in the general theory of INs. In the late 60's and in the 70's interest in the INs kept growing and was addressed towards INs built out of very simple SEs, generally 2×2, structured in multiple stages. The driving force was the interest in multiprocessor systems. Till now, hundreds of INs have been proposed. Some networks are better than others in some aspects but lag behind others in other aspects. Thus, there is no one ultimate network which is better than all others in all aspects. As such, designing new networks remains a topic for intensive investigation because there is no clear winner among existing ones. Researchers in the past have focused on two types of network models : circuit switched, packet switched and packet switched with buffers [28-30,53,64-67,113-114]. Study of circuit switched networks has gradually diminished since various packet switching techniques have been more prevalent. Recent research effort is directed towards design and analysis of buffered networks to avoid packet discarding during heavy traffic loads. In this thesis, the design and analysis of fault-tolerant, regular and irregular dynamic networks have been carried out with evaluation and optimization of the buffer requirement.

1.2 Classification of Interconnection Networks (INs)

Based on evolution, INs can be classified as shown in Figure 1.2

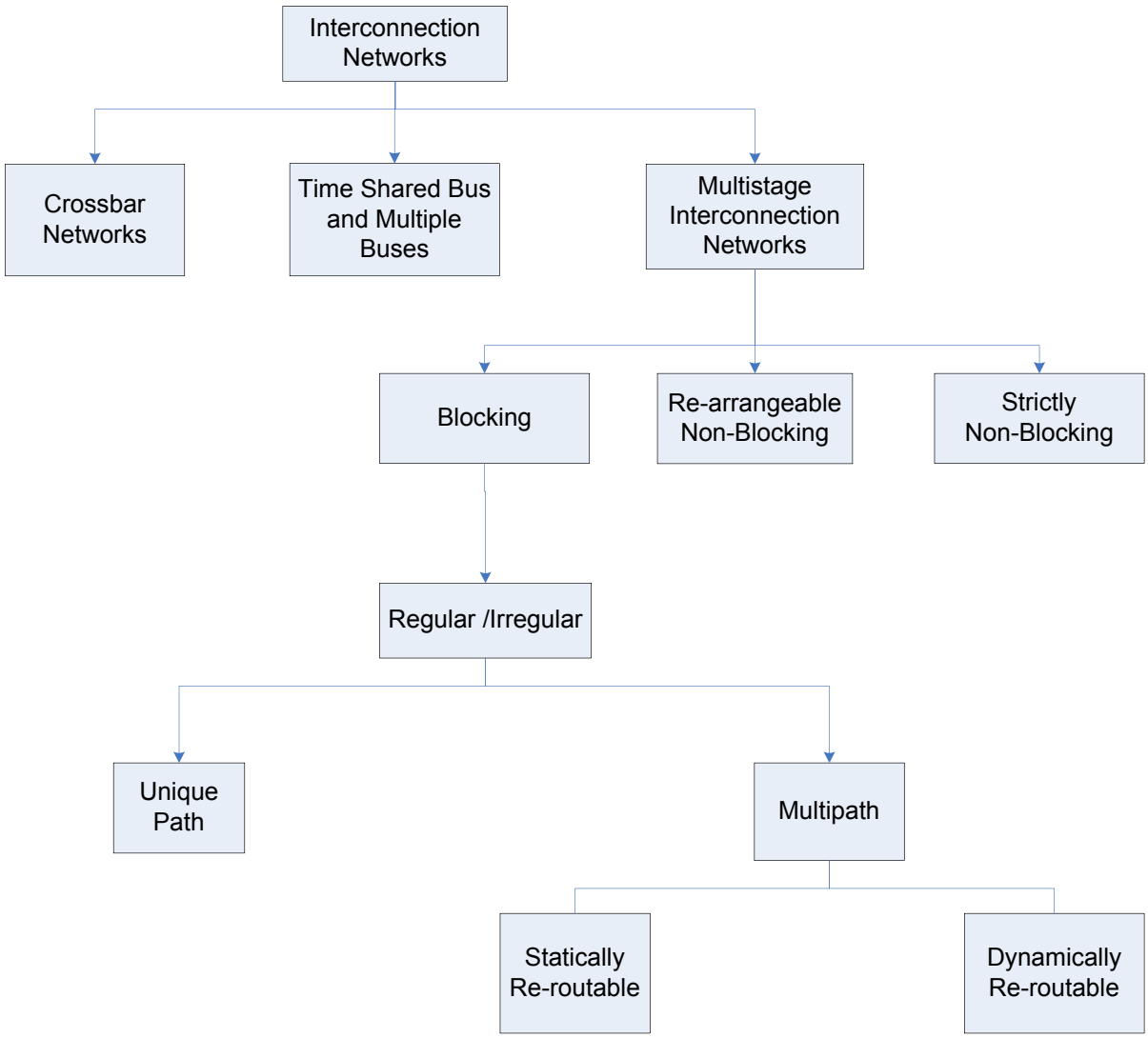

Figure 1.2 : Classification of Interconnection Networks

Crossbar Networks provide a fast means of interconnecting the resources in a multiprocessor system. A crossbar network is shown in Figure 1.3 below. In a crossbar network, a separate path is available for each memory unit. Every processor is connected to each memory module through a crosspoint switch. All processors can send memory requests independently and asynchronously. Each crosspoint switch in a crossbar network can be set open or closed, providing a point to point connection between the source and the

destination. On each row of the crossbar mesh, multiple switches can be connected simultaneously. In each column of crossbar mesh, only one switch can be

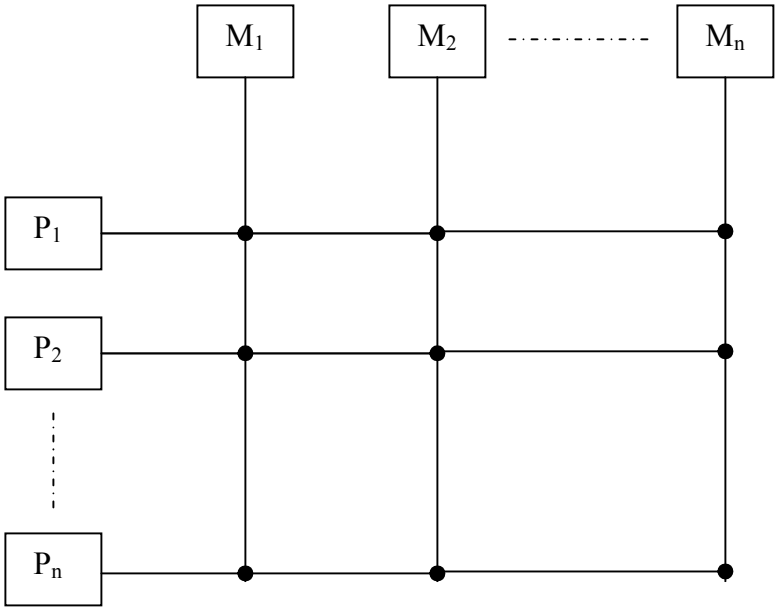

Figure 1.3 : Crossbar Network

connected at a time. Problem arises when multiple requests are destined for same memory module at the same time. In such cases, only one of the requests is serviced at a time (since in column of crossbar mesh only one switch can be connected).

To resolve the contention for each memory module, each crosspoint switch must be designed with extra hardware. All necessary switching and conflict resolution logics are built into the crosspoint switch. The hardware required to implement the crossbar switch is quite large and complex. For N inputs (processors) and N outputs (processors or memories) they require N^2 crosspoints and thus become prohibitively expensive for large values of N. On the other hand, time shared buses are inexpensive but do not permit simultaneous communication between distinct processor/processor or processor/memory pairs. Thus they are inefficient and become quite slow for even a moderate number of processors. Use of multiple buses can be an efficient technique for improved performance

but it becomes economically expensive. As a compromise between time shared buses and the crossbar networks, a class of networks called Multistage Interconnection Networks (MINs) have been proposed.

MINs are constructed from cascaded stages to divide the task of permutation in the network into several sub-tasks of lower complexity. When all the inputs of an interconnection network are connected to the outputs in a one-to-one fashion, a permutation on the inputs is said to be realized. Each stage consists of a set of basic switching elements (SEs), each SE is a small crossbar network. The outputs of the SEs of each stage are routed to the inputs of the next stage SEs through some inter-stage wiring pattern that defines the network topology. These SEs can connect any of the input lines to any of the output lines with the restriction that two or more input lines cannot be connected to the same output line at the same time. When two or more input lines have requests that attempt to pass through the SE to the same output line, a conflict is produced. In this case, one of the requests is equiprobably selected and passed while the other waits to the next cycle. The SEs can store a fixed number of waiting requests in queues. As such, the network is able to work in a packet communication environment. Packet communication reduces the blocking probability and hence improves performance.

A MIN is said to be strictly non-blocking if it is able to connect an input to an output which is not already connected to any other input, regardless of the state of the network. A non-blocking network can realize any permutation on its inputs and have hardware complexity $O(N(\log_2 N)^2)$ and are thus considered unsuitable for multiprocessor systems. A MIN is said to be rearrangeable non-blocking if it is possible to connect a source to a non-busy output, by rearranging existing connections if necessary[68]. It is possible to realize any permutation on the inputs of a rearrangeable non-blocking network. They have hardware complexity $O(N\log_2 N)$ but their routing algorithms have time complexity $O(N\log_2 N)$ which is not acceptable for reasonably sized multiprocessor systems [68]. A MIN is said to be a blocking network if some simultaneous connections between distinct input-output pairs are not possible because of conflicts for common communication links required for the connections. MINs can be further classified as regular/irregular on the basis of number of SEs per stage. If the number of SEs is same in

each stage, then the MIN is specified as regular otherwise irregular. In a unique path MIN, there always exists a unique path from any input to any output. Since there is a unique path between any input-output pair, the failure of any SE or link in the MIN disconnects at least one input from at least one output. In fact, if a SE fails then no paths can be routed through that SE and as such several permutations are lost. In a multipath MIN, there exist multiple paths between every input-output pair. If a multipath MIN allows re-routing to be made only at the source or at some fixed points in the network where the alternate paths exist, then it is statically re-routable. In case of dynamically re-routable MINs, there exists a fork at every stage and thus re-routing decisions can be made by the SEs at any stage.

1.3 Performance of MINs for Multiprocessor Systems

In this thesis, dynamic regular/irregular MINs have been designed and evaluated for their performance. The performance of a multiprocessor system depends largely upon the performance of MIN [13-15,16,21,29,43-44,51,54-55,57,64,76,112]. The various parameters that have been evaluated for performance analysis are probability of acceptance (PA), bandwidth (BW), fault-tolerance (FT), reliability, permutations passable, hardware complexity and cost. Probability of acceptance[76] is defined as the ratio of the average number of requests accepted by the destination to the average number of requests submitted by the sources per network cycle**.** Bandwidth of the MIN is defined as the average number of requests accepted per network cycle [76]. Terminal reliability [83,104] is defined as the probability that a given source-destination pair has at least one fault free path between them given that each SE has a certain reliability (the reliability of a SE is the probability that it is fault free). Fault-tolerance of MINs is concerned with finding alternate paths between a source and destination so that faulty paths can be avoided. Three fault models are used for MINs : the stuck-at fault model [4,32], the link fault model, and the switch fault model. In the stuck-at fault model, a failure causes a SE to remain in a particular stage regardless of the control inputs given to it, thus affecting its ability to set up proper connections. In the link fault model, a failure affects an individual link of a SE, leaving the remaining part of the SE operational. In the switch fault model, the strongest

of the three, a failure makes a SE totally unusable [2,56,108]. In this thesis, the switch fault model is being considered. Here, *Chaining technique* has been used to incorporate fault-tolerance. In chaining, some specific SEs in each stage are connected by means of auxiliary links to form loops. In case of any SE fault or conflict for output ports of SE, the traffic gets steered via auxiliary link towards associated SE in the loop thus bypassing the fault. The hardware complexity of a MIN can be determined by evaluating SE complexity and link complexity. The hardware complexity in turn is a measure of the cost of the MIN. The SE complexity of a regular MIN is equal to the complexity of the individual SE times the number of SEs per stage times the number of stages. However, in case of irregular MIN, the SE complexity needs to be evaluated stage by stage as the number of SEs in each stage may not be equal. The complexity of an individual SE is estimated by the number of crosspoints necessary to implement it. An m×m SE implemented as full crossbar has complexity m^2. An m×1 multiplexer and an 1×m demultiplexer each has complexity m. Link complexity is specified by three components : the number of stages, the number of inter-stage links and the number of intra-stage links.

A good IN should be should be fault-tolerant, reliable, fast, cost effective, maintain good performance (i.e. high values of probability of acceptance and bandwidth even in the presence of faults). It should have lower values of path length. Permutations Passable should not get effected under faulty scenarios other than critical faults. It should be on-line repairable. If some faults develop in any SE/subnetwork, and the faulty SE/subnetwork can be simply replaced by the new one without causing a breakdown in the system then the system is on-line repairable.

The above characteristics have to be achieved avoiding exorbitant additonal cost. As an outcome of this thesis, four networks namely M_ASEN, M_FDOT, Hybrid and QUAD have been proposed. An effort has been mode to improve upon the existing MINs in the literature. Permutations passable for each of the proposed MINs have been investigated analytically. Most of the existing MINs show degradation in the performance parameters i.e. PA and BW during faulty scenarios. The MINs proposed in this thesis have been so designed to eliminate this limitation as well as to provide improvement in other performance parameters also.

1.4 Objectives

To study the existing MINs, to incorporate modifications in the existing MINs and to design new MINs leading to better performance than the existing ones. To evaluate the performance of the proposed MINs in terms of parameters such as probability of acceptance, bandwidth, reliability, fault-tolerance, permutations passable and hardware complexity.

1.5 Organization of the Thesis

Thesis has been organized as follows :

Chapter 1: Introduction

Chapter 2: Literature Survey

Chapter 3 : Design and Analysis of the proposed Regular MIN

Chapter 4 : Design and Analysis of the proposed Irregular MINs

Chapter 5 : Comparative Performance of the Proposed MINs

Chapter 6 : Conclusions and Future Scope

In Chapter 2, literature survey has been carried out. The various static and dynamic fault-tolerant MINs proposed and analyzed by various researchers have been presented. Chapter 3 deals with the design and analysis of the proposed regular MIN i.e. M_ASEN. A 16×16 network is drawn, followed by discussion on its construction procedure, routing algorithm and fault-tolerance. The other performance parameters that have been evaluated/analyzed are PA, BW, terminal reliability, permutations passable and hardware complexity. In Chapter 4, the three proposed irregular MINs : M_FDOT, Hybrid and M_QUAD have been presented. A 16×16 sized network corresponding to each proposed design has been drawn followed by its construction procedure, routing algorithm and fault-tolerance abilities. Thereafter, the terminal reliability feature of each proposed irregular

MIN has been evaluated followed by tabulation of permutations passable feature for each network. Lastly, hardware complexity evaluation (effecting cost) for each of the proposed irregular network has been carried out. Chapter 5 presents the comparison of the proposed regular and irregular MINs with networks of similar type and also presents the comparative analysis of the proposed MINs among themselves. Lastly, the concluding part of the work along with suggestions for further scope in this area are presented in Chapter 6.

Chapter 2

Literature Survey

In this chapter, various existing unique path and multipath (static and dynamic) MINs with regular and irregular topologies have been examined and presented. The various fault-tolerant techniques that have been used in various existing multipath MINs have been studied. The various existing fault-tolerant MINs have been categorized under four headings – static regular MINs, static irregular MINs, dynamic regular MINs and dynamic irregular MINs.

2.1 Multistage Interconnection Networks

MINs provide cost-effective, high bandwidth communication in multiprocessor systems [33,36,76,110]. These networks possess the property of full access, allowing data from any source to any destination in a single pass through the network. MINs differ in the interconnection pattern between stages, the type and operation of individual SEs, and the control scheme for setting up the SEs. Examples include the Flip [20], Baseline [110], Banyan [36], Delta [76] networks etc. Within the class of Banyan networks in which only one path exists between an input and output, the delta networks raised a lot of interest. These MINs are characterized by two very important properties : the digit routability and the high parallelism attained within the network. Digit routability is the process of routing a packet from any source to any destination using a n-digit routing tag. The operations of SEs in each stage are mutually independent so that the processing capability of each stage of an N×N MIN is N/2 times the processing capability of a single SE. The minimum requirement of any of these networks is to provide full access capability, which means that any source should be able to access any destination in one pass through the network.

The various unique path MINs reported in the literature are Omega Network [61], Shuffle Exchange Network [73], Delta Network [76], Reverse Baseline Network [110] etc. The various statically routed MINs reported in the literature are Extra Stage Cube [1], Modified Omega Network [71] , INDRA[80] etc. A large number of multi-path dynamically re-routable MINs have been proposed by the researchers [26,61,70,71, 74,78,82]. Dynamic MINs can be further classified as regular/irregular on the basis of number of SEs per stage. If the number of SEs is same in each stage, then the MIN is specified as regular and if the number of SEs in each stage of MIN are not equal then the MIN is specified as irregular. The various regular dynamic MINs existing in the literature are Augmented Shuffled Exchange Network (ASEN) [57] and its variations, Augmented Baseline Network (ABN) [9] etc. The various irregular dynamic MINs existing in the literature are Fault-tolerant Double Tree Network (FDOT) [10], QUAD Tree Network [12], ALN [86], PHN [86], etc. Dynamic regular/irregular MINs can be designed as buffered/non-buffered. In case of non-buffered MINs, whenever there is a conflict between packets for the same port, only one packet is provided the port and the other is discarded. But in case of buffered MINs, the packet which is not provided the port is stored in the buffer instead of being discarded and when the required port becomes available, it is provided to the packet in the buffer. Researchers in the past have analyzed the performance of a number of buffered MINs [28,29,34,51,65,99,113]. The various MINs – Unique path, Multipath (Static Regular, Static Irregular, Dynamic Regular and Dynamic Irregular) are described as under

2.2 Unique Path MINs

In a unique path MIN, there is a single path from any source to any destination. The unique-path property of a MIN facilitates the use of simple routing algorithms for setting up connections through the network. However, the presence of a single fault among the SEs or the connecting links of these networks destroys the full access property.

2.2.1 Omega Network

Omega Network is shown in Figure 2.1

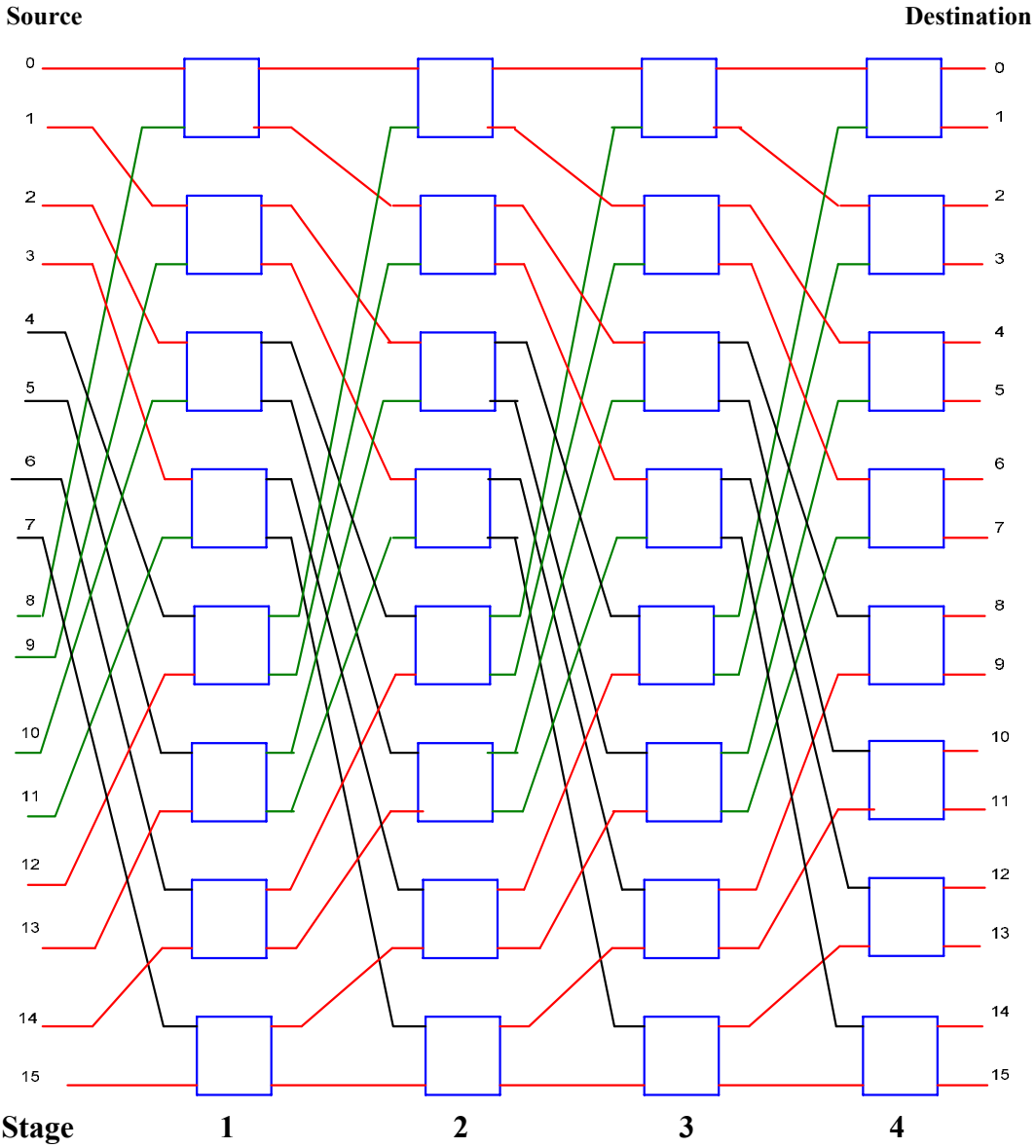

Figure 2.1 : Omega Network [60]

Omega Network maintains a uniform connection pattern between stages. Every source has a unique path to every destination. Routing is performed in a distributed manner using destination address as the "routing tag". A 16×16 network is shown in Figure 2.1. There are $\log_2 N$ stages, each stage comprising of N/2 SEs where N is the size of the Network.

2.2.2 Baseline Network

The Baseline Network is shown in Figure 2.2(a) below :

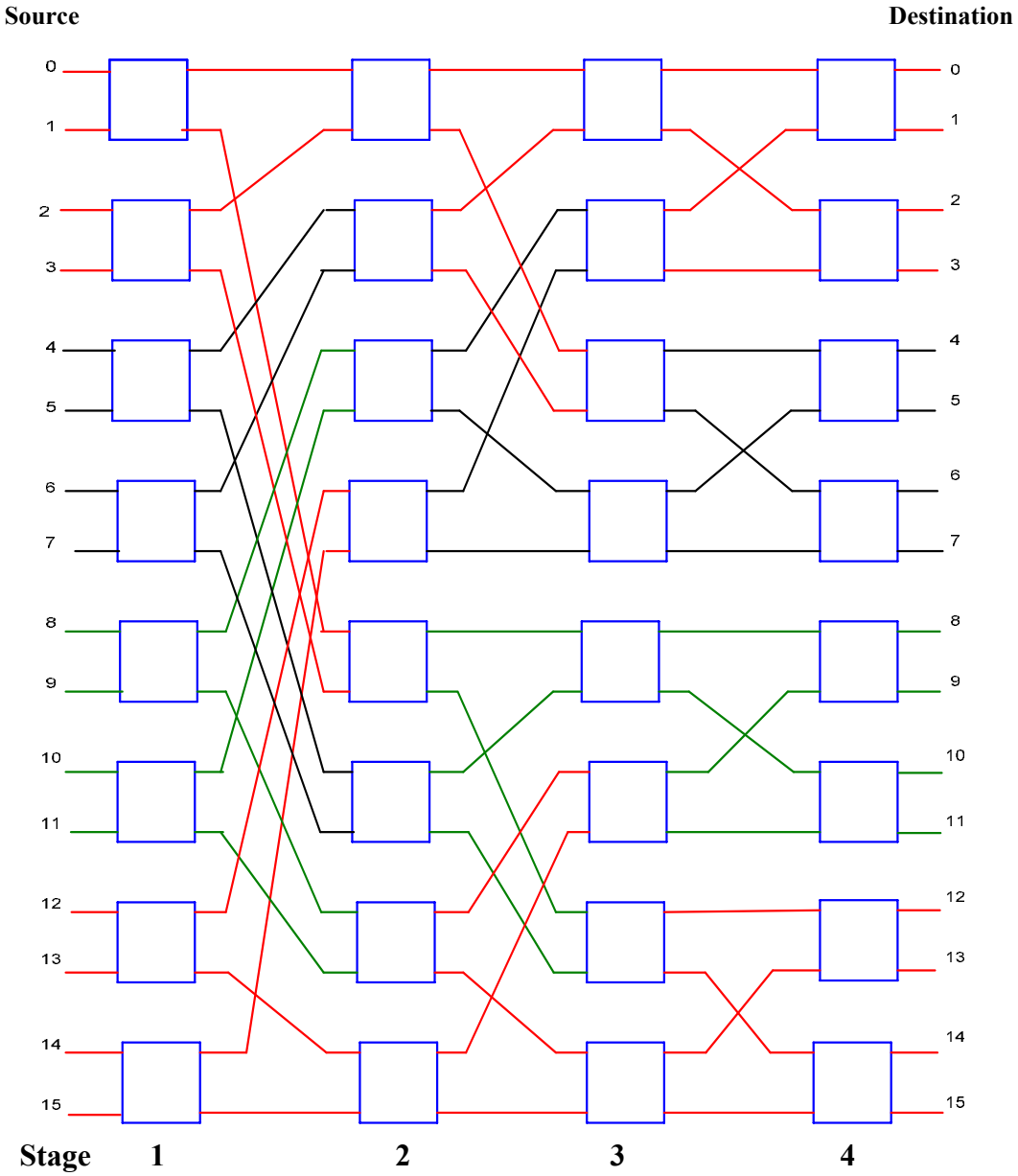

Figure 2.2(a) : Baseline Network [110]

Baseline Network maintains a uniform connection pattern between stages. The connection pattern is inverse perfect shuffle. There are $\log_2 N$ stages, each stage comprising of N/2 SEs where N is the size of the Network.

2.2.3 Reverse Baseline Network

It is unique path network. All the SEs are identical in size. The network has the self routing property requiring $\log_b N$ (where N is the number of inputs and b is the size of SE) digits to route a packet from an input to output.

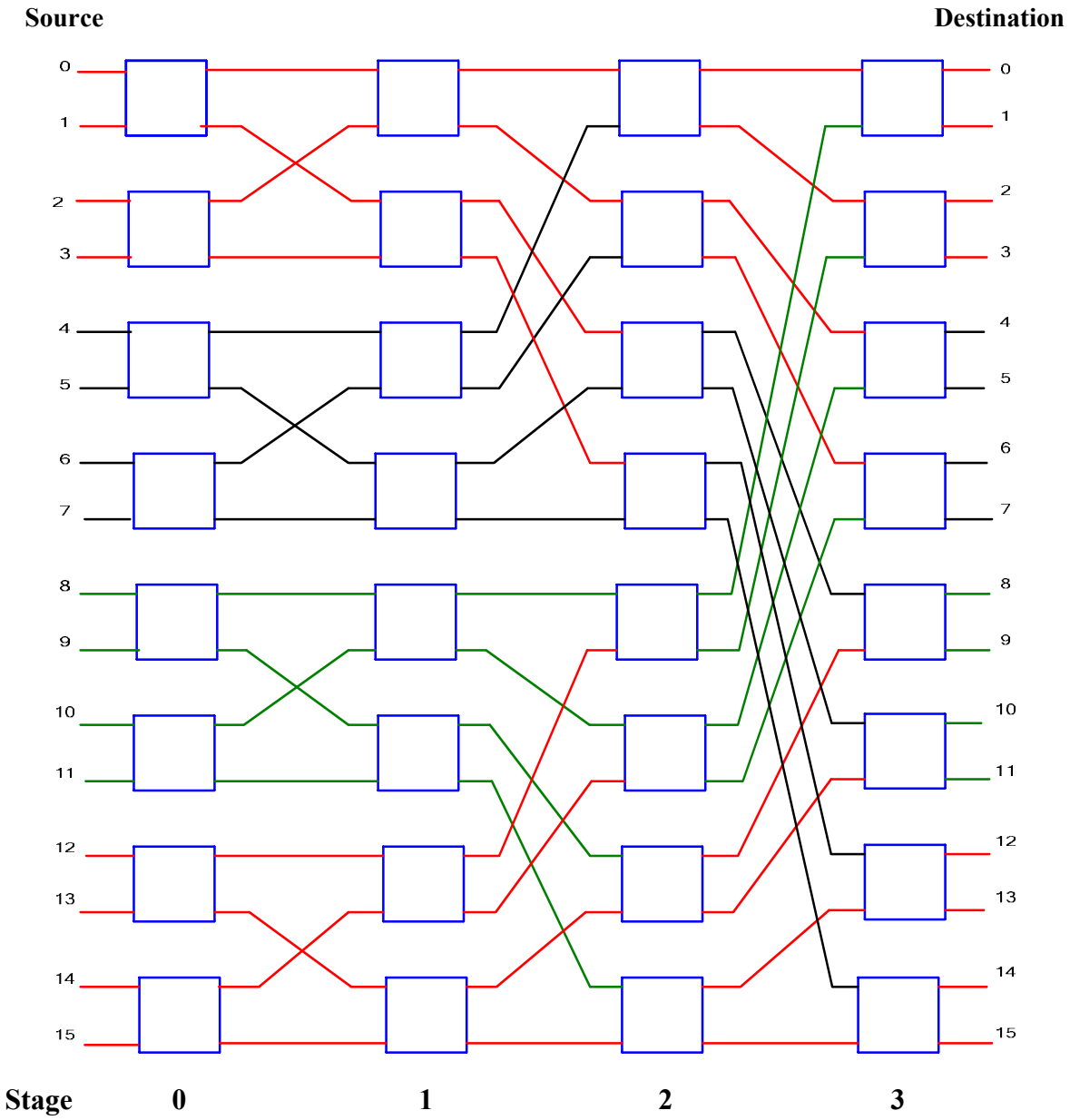

Figure 2.2(b) : Reverse Baseline Network

2.2.4 Delta Network

The Delta Network is shown in Figure 2.3

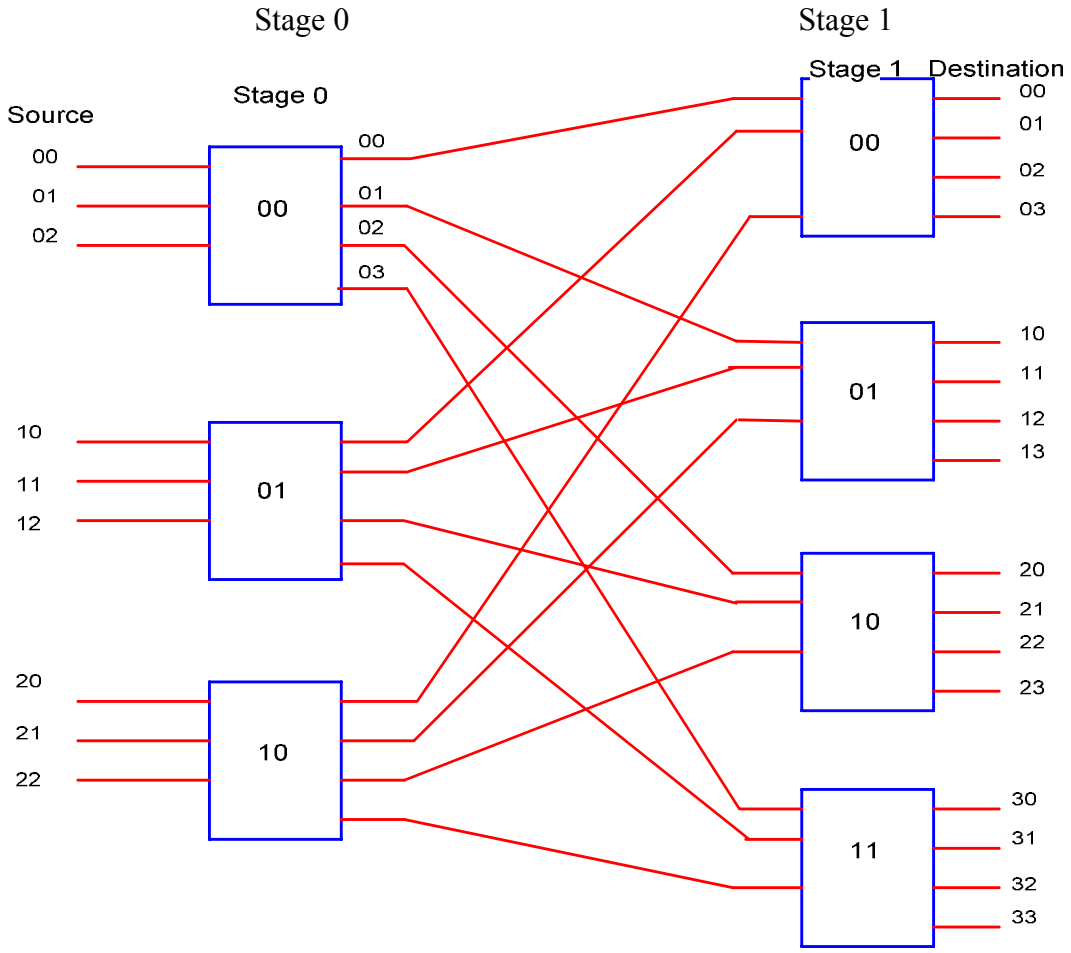

Figure 2.3 : Delta Network [76]

Delta Networks also have the property of digit controlled routing, which means that a path can be setup through the network in a distributed manner by using individual bits of the destination address. The sources and destinations are numbered 0 through N-1. The stages are numbered from 0 to n-1 from the input side. This network has m stages of SEs sized a×b, have a^m sources and b^m destinations. The i^{th} stage has $a^{m-i}b^{i-1}$ SEs controlled by the i^{th} digit of the destination address. It is a blocking network. Suppose that the source 01 needs a connection with the destination 10 and the source 02 needs to be connected to the destination 11. Both the connections require the output port 02 of switch 00 in stage 0. This leads to blocking of one request. One of the two requests is equiprobably selected.

2.2.5 Indirect Binary n-cube Network

The binary n-cube network of size 16×16 is shown below

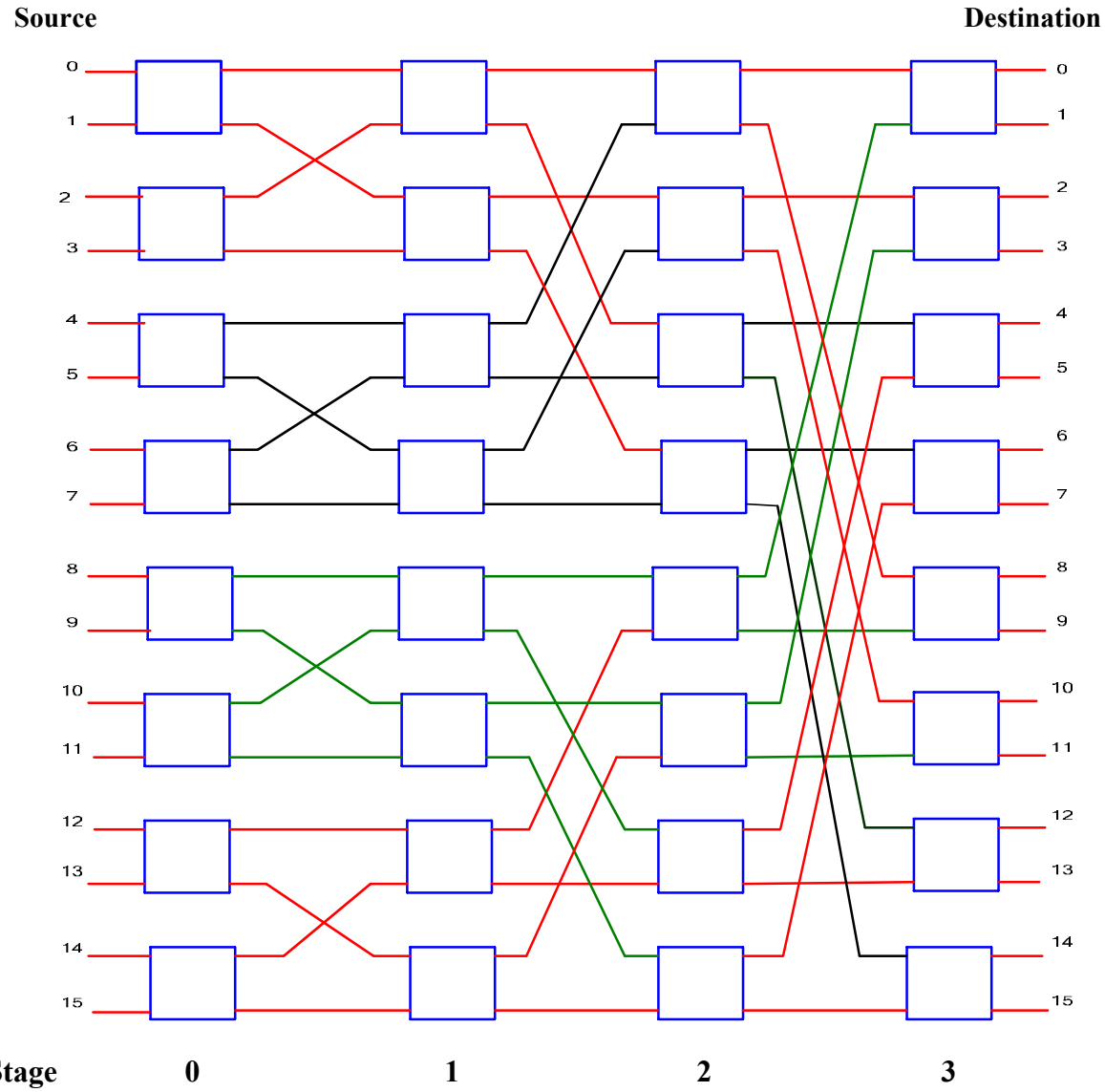

Figure 2.4 : Indirect Binary n-cube Network [77]

The network consists of m stages of N/2 SEs with independent control. The structure of the network is defined such that the two input links to a SE in stage i differ only in the i^{th} bit position, $0 \leq i < m$. The ordering of the stages, from network input to output is stage 0, stage 1, ……, stage m-1. It is unique path network. The size of each SE is 2×2.

2.2.6 Modified Data Manipulator Network

It is unique path network. All the SEs are identical in size. The network has the self routing property requiring $\log_b N$ (where N is the number of inputs and b is the size of SE) digits to route a packet from an input to output.

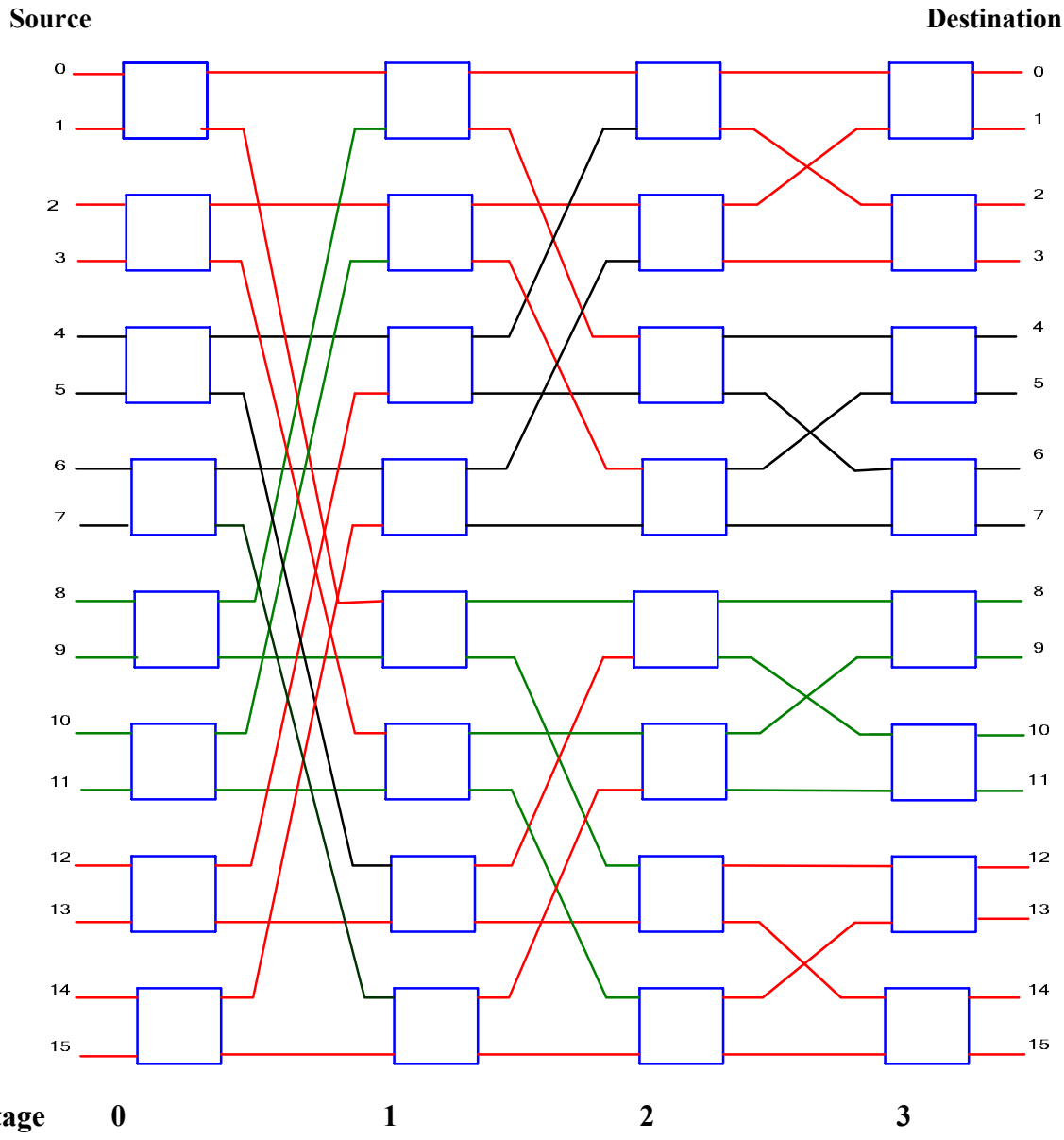

Figure 2.5 : Modified Data Manipulator Network[92]

2.3 Fault-Tolerant MINs

Fault-tolerance of MINs is concerned with finding alternate paths between a source and a destination so that faulty paths can be avoided. In other words, fault-tolerance techniques are aimed at maintaining full access in the presence of one or more component failures. Fault-tolerance can be achieved using redundancy at the network level, extra stage(s) in the network and by means of Chaining technique. The technique where fault-tolerant networks are designed using multiple copies of the basic network is called redundancy at the network level. MINs making use of this technique are INDRA [80] Network, Fault-tolerant Double Tree Network (FDOT) [12] etc. INDRA is of regular topology whereas topology of FDOT is irregular. INDRA and FDOT have been shown in Figures 2.7 and 2.9 respectively. Another method to incorporate fault-tolerance into the network is through the use of one or more extra stages of SEs[1,71]. The technique of using extra SE stages provides multiple disjoint paths between source-destination pairs at a relatively lesser cost as compared to network level redundancy. MINs making use of this technique are Extra Stage Cube Network [1], Extra Shuffle Exchange Network [37], Extra Stage Omega Network [108] etc. Extra Stage Cube Network has been shown in Figure 2.6. In Chaining technique, some specific SEs in each stage are connected by means of auxiliary links to form loops to provide fault-tolerance and distribution of traffic under high packet generation rates. The number of SEs in each loop are usually kept equal in number. In case of detection of any fault/blocking, packets are steered via auxiliary link towards associated SE in the loop. In the recent past, this technique has been extensively used by the researchers[7-12,56,86]. Examples of various existing MINs making use of this technique are Augmented Shuffle Exchange Network (ASEN-2) , ASEN-MAX [57], Augmented Baseline Network (ABN) [9], QUAD Tree (QT) Network [11], Alpha Network (ALN), PHI Network (PHN) [86], Irregular Augmented Shuffle Exchange Network (IASEN) [3]. ASEN-2, ASEN-MAX and ABN have been shown in Figures 2.10(a), 2.10(b) and 2.11 respectively. QT, ALN, PHN and IASEN have been shown in Figures 2.12 to 2.15 respectively.

2.4 Fault-Tolerant Static Regular MINs

In fault-tolerant static regular MINs, fork is available only at some selected single/multiple stages. Static MINs have a fixed connection pattern and the presence of a fault disconnects the path through which that faulty element is present.

2.4.1 Extra Stage Cube Network (ESC)

The extra stage cube network of size 8×8 is shown in Figure 2.6

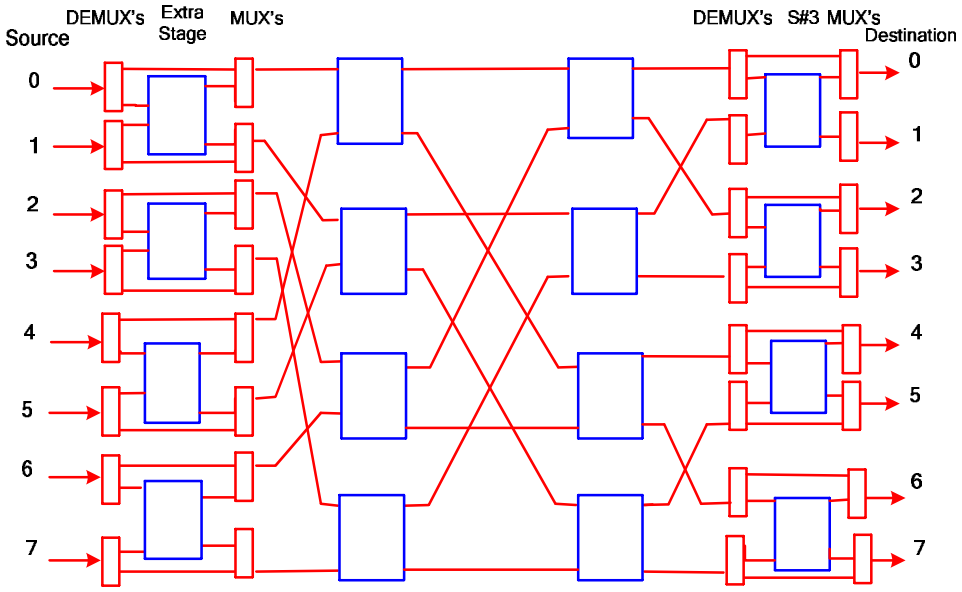

Figure 2.6 : Extra Stage Cube Network[1]

The extra stage cube is the modified form of generalized cube MIN . The extra stage cube is constructed from the generalized cube network by adding an extra stage at the input side of the MIN. (The Generalized Cube network has $n = \log_2 N+1$ stages where N is the size of the network and $N = 2^{n-1}$. The size of each SE is 2×2. The connections are based on the cube interconnection functions [44]). ESC is single SE fault tolerant in any stage. The SEs in this extra stage and in the final stage are equipped with demultiplexers at the inputs and multiplexers at the outputs respectively. Stage n and stage 0 can each be

enabled or disabled. A stage is enabled when its SEs can be used to provide interconnection capability. It is disabled when its SEs are being bypassed. Enabling and disabling of stages n and 0 is accomplished by a demultiplexer at each SE input and a multiplexer at each output. One demultiplexer output goes to a SE input, the other to an input of its corresponding multiplexer. The remaining multiplexer input is from the matching SE output. The demultiplexer and multiplexer are configured such that they either both connect to their SE (enable) or both bypass it (disable). All multiplexers and demultiplexers for stage n share a common control signal. All demultiplexers and multiplexers for stage 0 also share a common control signal. Enabling and disabling of stages n and 0 is performed by a system control unit. Normally, the network will be set so that stage n is disabled and stage 0 is enabled. If the fault is in stage 0, stage n is enabled and stage 0 is disabled. For a fault in link or SE in stages n-1 to 1, both stages n and 0 will be enabled. The switch complexity of the ESC is $2N(\log_2 N + 1) + 8N$. There are $(\log_2 N + 1)$ stages and N links between adjacent stages. Since the communication links are common for various source-destination pairs, hence ESC is a blocking type of MIN. ESC allows only static rerouting. Under normal conditions, the extra stage is disabled and there is only one path between any source-destination pair. Thus the fault-free performance of the ESC is the same as that of a unique path MIN. If a faulty SE is present in the ESC, at least two passes are required to realize a permutation realizable by the fault-free generalized cube in one pass.

2.4.2 INDRA Network

The Interconnection Networks Designed for Reliable Architectures (INDRA) Network is shown in Figure 2.7. INDRA Network can be viewed as a union of L parallel copies of a basic network with an initial distribution stage: each basic network is a delta network constructed from N×N SEs. The SE size N and the redundancy L determine the fault-tolerance capability of the network. The interconnection pattern between stages of each sub-network is the generalized shuffle [76]. The initial distribution stage consists of N SEs, each having a crossbar of size N×L. On the input side, each source is connected to

N different SEs. The outputs of each SE in the distribution stage are connected to L different sub-networks. On the output side, the output terminals of the L sub-networks converge on the N destinations. There are N.L paths between any source and any destination. The INDRA network can be visualized as a shuffle-exchange MIN of size N×N with each of the N sources connected to a specified set of N SEs in the first stage and each destination receiving connections from N specified SEs in the last stage.

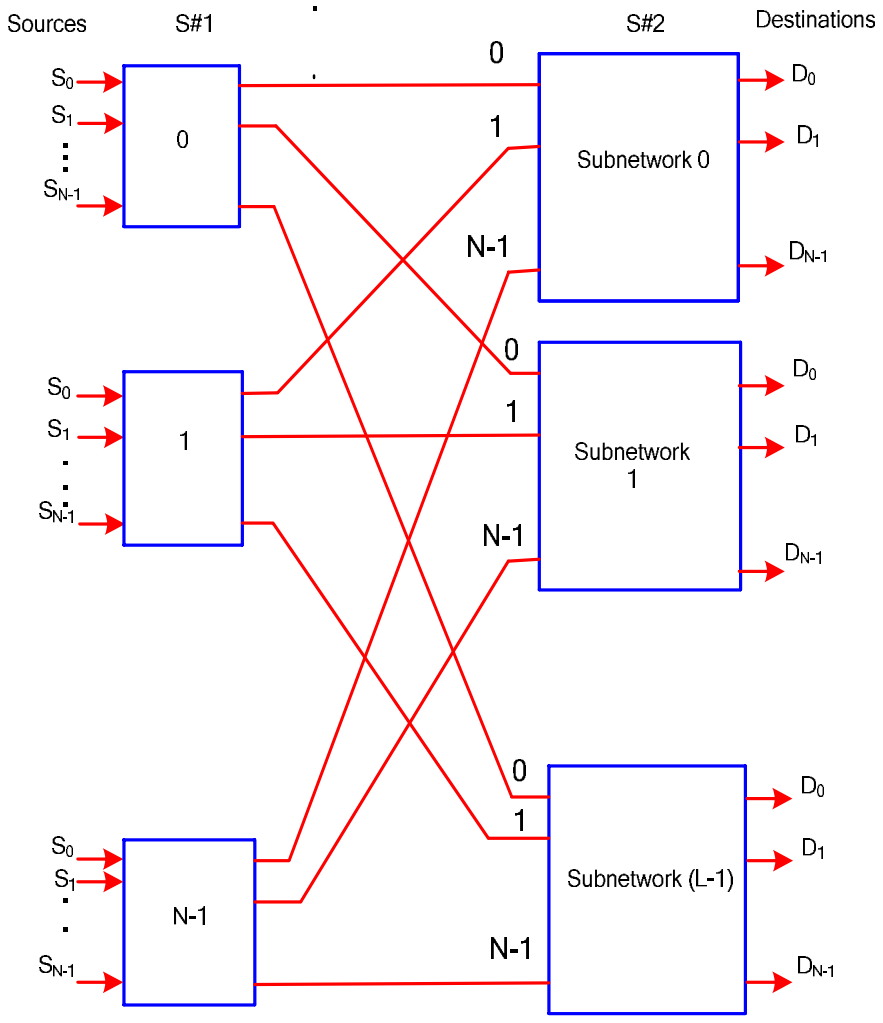

Figure 2.7 : INDRA Network[80]

2.5 Fault-tolerant Static Irregular Networks

In fault-tolerant static irregular networks, the number of SEs may not be same in each stage and fork exists only at some fixed stages. Although static MINs also provide fault-tolerance but may not be as efficient as dynamic MINs.

2.5.1 DOT Network

An 8×8 sized DOT network is shown in Figure 2.8. A DOT Network consists of a right and a left half. Each half of the network resembles a binary tree, with the left half and right half being mirror images of each other. A DOT Network of size N×N has N sources and N destinations, comprising of (2n-1) number of stages with $(2^{n+1} - 3)$ SEs. An i^{th} and $(2n-i)^{th}$ stage has 2^{n-i} SEs of size 2×2 for i=1,2,…n. Although it is a redundant network but it is not fault-tolerant.

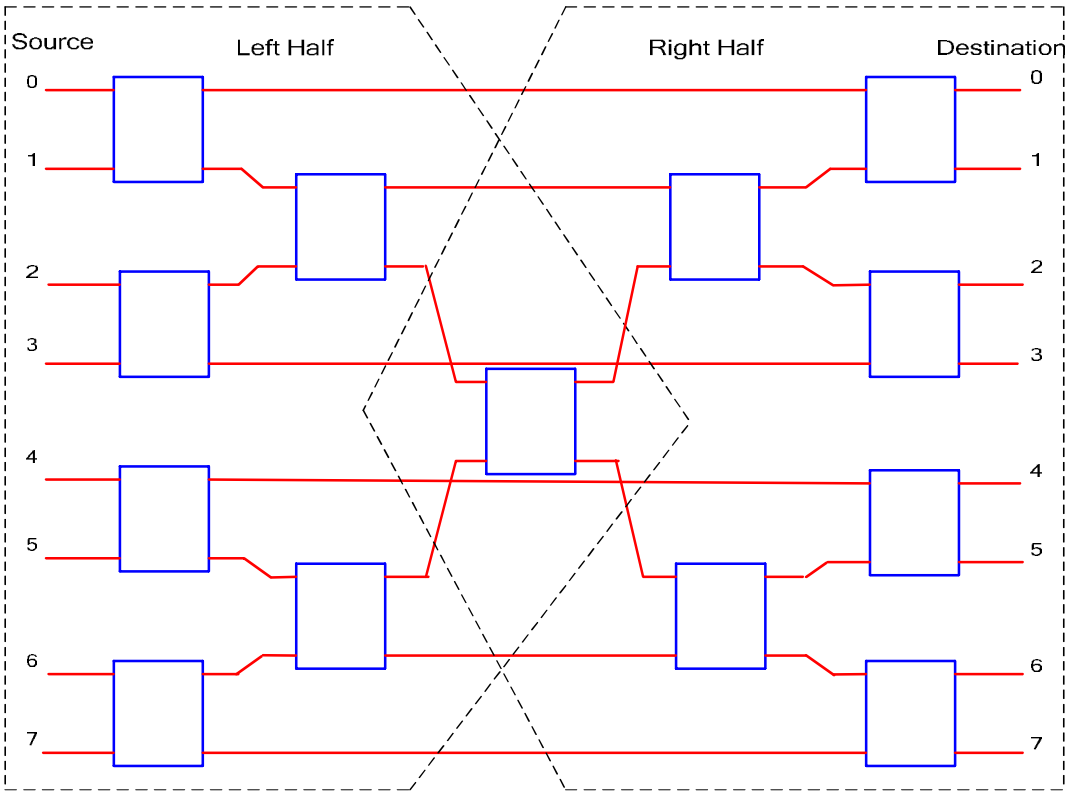

Figure 2.8 : DOT Network [61]

2.5.2 Fault-Tolerant Double Tree Network (FDOT)

The Fault-tolerant Double Tree Network (FDOT) is shown in Figure 2.9.

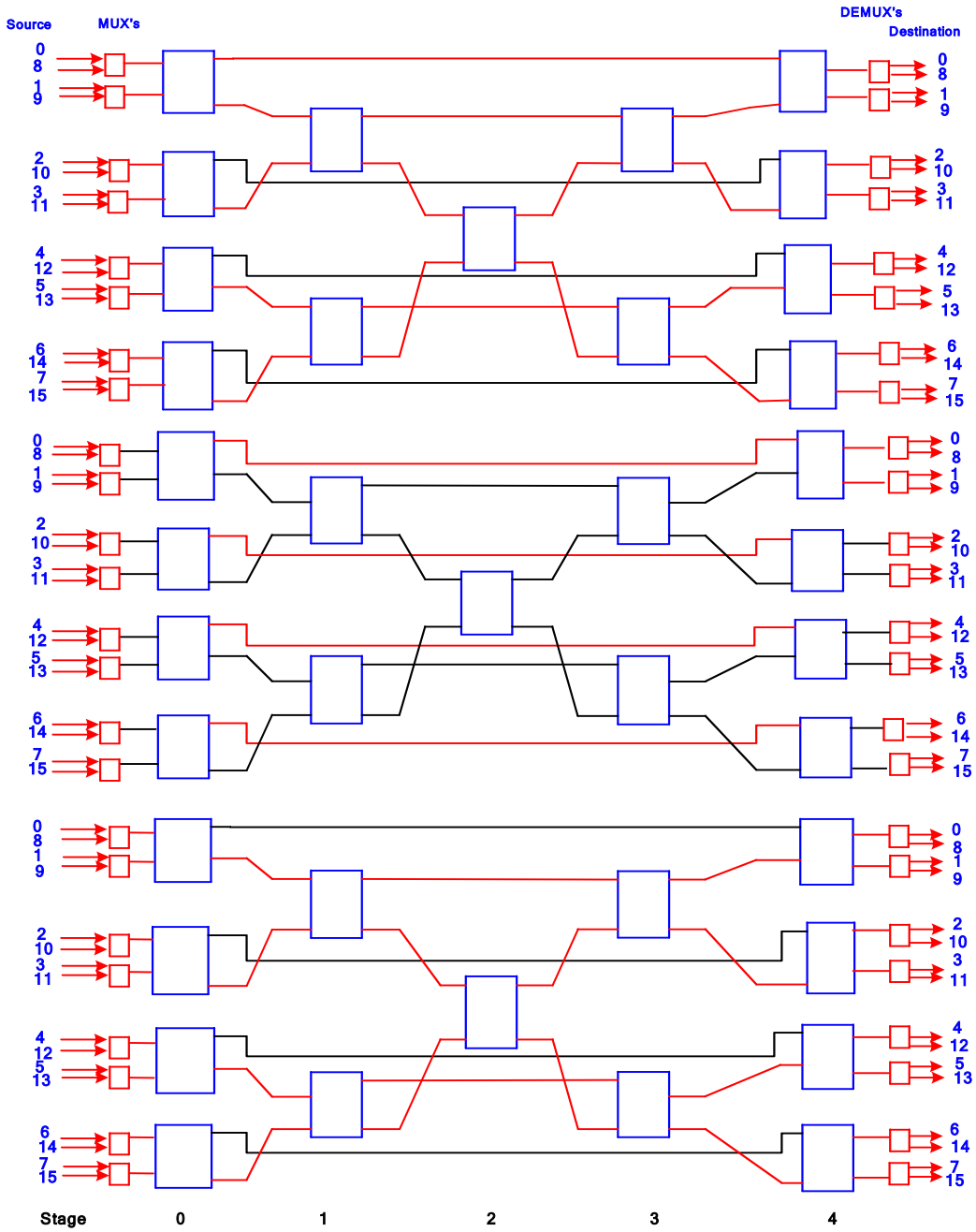

Figure 2.9 : Fault-tolerant Double Tree (FDOT) Network [10]

The FDOT is a fault-tolerant irregular dynamic Network. An FDOT-k network[10] of size N×N is designed by dividing N inputs and N outputs into k disjoint partition of N/k sources and N/k destinations where k (≥2) and N (>k) are powers of 2. There are k independent sub-networks, and an extra one, such that a connection path between each source-destination pair can be established via any one of the subnetwork. As such, it is k switch fault tolerant. All the (k+1) subnetworks are of identical type : a DOT network of size N/k × N/k. The number of favorite destinations is increased from 2 to 2k as compared to DOT network of similar size. The extra subnetwork helps to enhance fault-tolerance capability. The network consists of (2n-1) number of stages and $(k+1)(2^{n+1}-3)$ number of SEs where $n=\log_2 N/k$. It consists of $N\times(1+1/k)$ number of k×1 multiplexers and an equal number of 1×k demultiplexers. Each of the stage i and 2(n-1)-i have exactly $(k+1)\times 2^{n-i-1}$ SEs for i=0,1,……..,(n-1). The cost of this network is computed by the formula $(k + 1)(2^{n+3}+ 2N -12)$. The cost gets evaluated to 108 units for 8×8 FDOT, 252 units for 16×16 sized FDOT, 540 units for 32 × 32 sized network.

2.6 Fault-Tolerant Dynamic Regular MINs

In a dynamic MIN, the interconnection pattern among the SEs can be varied dynamically. The number of SEs in each stage are equal. Fork exists at every SE in every stage. In the last two decades, fault-tolerance for dynamic MINs has been an active area of research [69,99,100]. Three distinct fault-tolerance criteria have been used in the design and evaluation of these networks – full access, dynamic full access and partial connectivity. Full-access refers to the ability of the network to provide connection between any source-destination pair. Partial connectivity is the availability of a set of K ≤ N SEs with full access among them. Dynamic full-access (DFA) is less stringent requirement of fault-tolerance than full-access. DFA is the ability of the network to route data between any pair of source and destination in a finite number of passes, routing the data through one or more intermediate SEs. DFA is achieved by the use of chaining technique. In chaining, additional links are provided between SEs belonging to the same stage for routing the data through some fault-free path in the

presence of a single/multiple SE faults. In fault-tolerant dynamic regular MINs, there are equal number of SEs in each stage and fork is available in every SE at every stage. Some of the fault-tolerant dynamic regular MINs are presented in the following sections :

2.6.1 Augmented Shuffle Exchange Network

ASEN is constructed from a shuffle exchange MIN by adding a stage of 2×1 multiplexer switches at the input side (for making multiple connections from the sources to the MIN), replacing the last stage SEs by 1×2 demultiplexer SEs (for providing multiple connections from the MIN to each destination) and by adding auxiliary links to connect certain groups of SEs within each stage to form loops (to provide an alternate way of routing in each stage). An ASEN-2 for N=16 is shown in Figure 2.10(a). There are several versions of ASEN depending upon the number of SEs in each loop e.g. In ASEN-2, there are exactly two SEs in each loop. ASEN-2 has (n-1) stages where $n=\log_2 N$. Before stage 1, there is a stage 0 of multiplexers with two inputs and one output, stages 1 through (n-2) consist of N/2 SEs of size 3×3; stage (n-1) consists of N/2 SEs of size 2×2 and after stage (n-1), there is a stage of demultiplexers with one input and two outputs.

The inter-stage and intra-stage interconnection pattern is designed as under :

i) $S_m(i)$, the set of multiplexers connected to source i, $0 \le i \le N$ is $\{(0,i), (0,i+N/2 \bmod N)\}$.

ii) The multiplexer (0,i) , $0 \le i < N$ is connected to the SE $(1, \lfloor i/2 \rfloor)$.

iii) The connection pattern between SEs in stages i and (i+1), for $1 \le i \le n-2$ is the perfect shuffle permutation. In addition, there exist intrastage links in stage i, $1 \le i \le n-2$, which connect SEs whose binary representations differ in the second bit from the left.

iv) The SE (n-1,i), $0 \le i < N/2$ is connected to the SEs $(n, 2i \bmod N/2)$, $(n, 2i+1 \bmod N/2)$.

v) $S_L(i)$, the set of demultiplexers are connected to destinations i, $0 \le i < N$ is $\{(n, , \lfloor i/2 \rfloor, (n, \lfloor i/2 \rfloor + N/2)\}$.

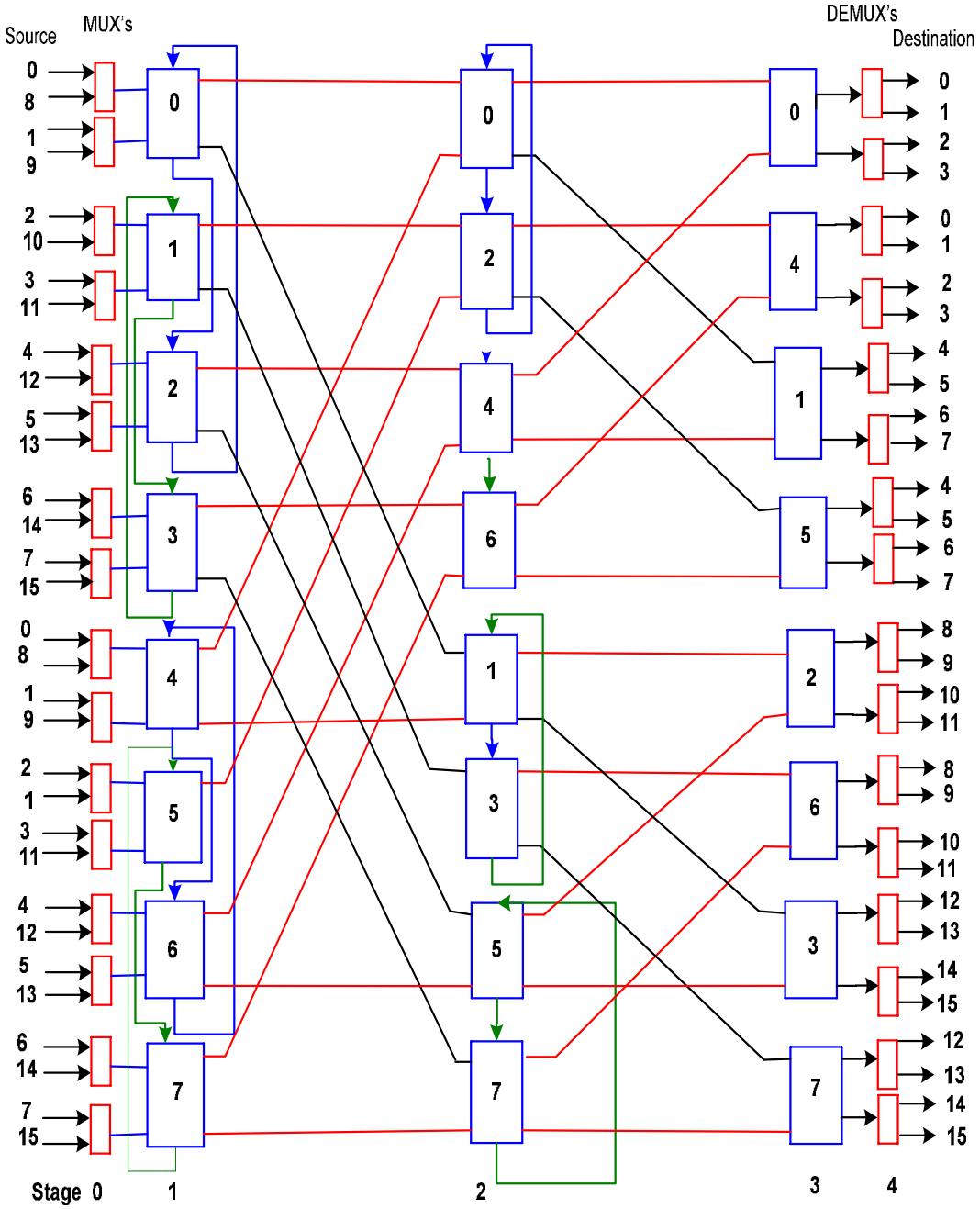

Figure 2.10(a) : Augmented Shuffle Exchange Network (ASEN-2) [57]

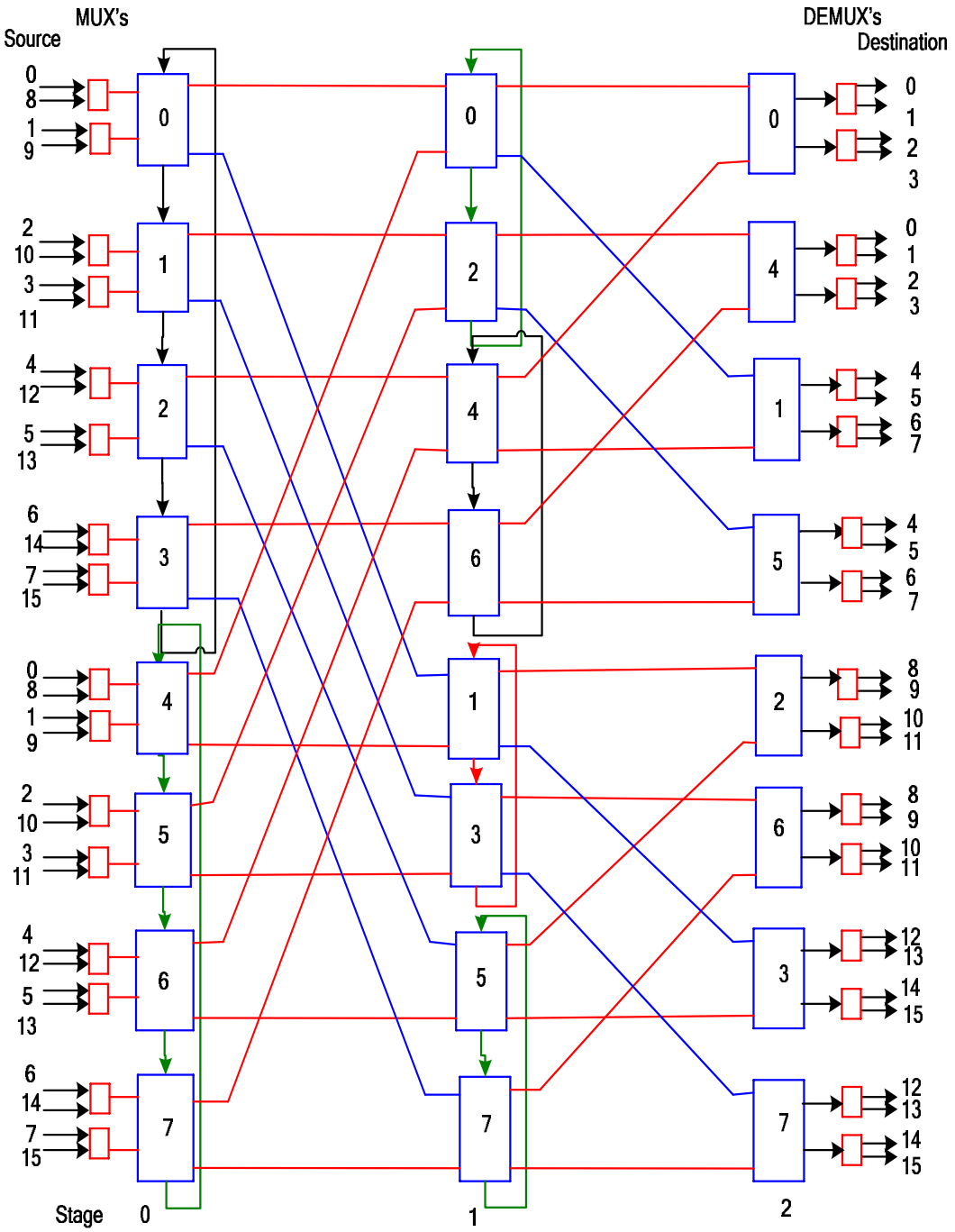

Figure 2.10(b) : ASEN-MAX [57]

The existing Augmented Shuffle Exchange Network(ASEN) [57] is a fault-tolerant regular type of MIN. In the ASEN, no single SE fault causes any source to be disconnected from any destination although the bandwidth of the network may get reduced [57]. Moreover, the ASEN tolerates several multiple SE faults while maintaining the ability to connect any source to any destination. ASEN is obtained by making certain intra-stage connections between specific SEs in shuffle exchange MINs . ASEN- and ASEN-4 are shown in Figure 2.10(a) and Figure 2.10(b) respectively.

The SEs that are connected by means of intra stage connections forming a loop must satisfy the following two conditions :

i) They must belong to the same conjugate subset. All the SEs in a given stage which have output paths leading to the same subset of destinations comprise a conjugate subset of SEs.

ii) No two SEs in a loop must form a conjugate pair. In each conjugate subset, there exist several pairs of SEs called conjugate pair of SEs. The SEs in such a pair are connected to the same SEs in the next stage.

Routing in ASEN is adaptive and is based upon the destination based routing tag. Each SE will sense a specific bit in the routing tag and depending upon the value of the sensed bit, it will steer the packet either towards the upper or lower port. If the bit sensed is 0, the bit is steered towards the upper output port and if the bit sensed turns out to be one, the packet is steered towards the lower output port.

2.6.2 Augmented Baseline Network (ABN)

The Augmented Baseline Network is shown in Figure 2.11. It is a baseline network with one less stage. The SEs in the last stage are of size 2×2 and the remaining SEs in stage 1 through (n-3) ($n=\log_2 N$) are of size 3×3. In each stage, the SEs can be grouped into conjugate pairs i.e. each SE in such a pair has the same successor SEs in the next stage. These conjugate pairs can then be grouped into conjugate subsets, where each conjugate subset is composed of all SEs in a particular stage that lead to the same subset of destinations.

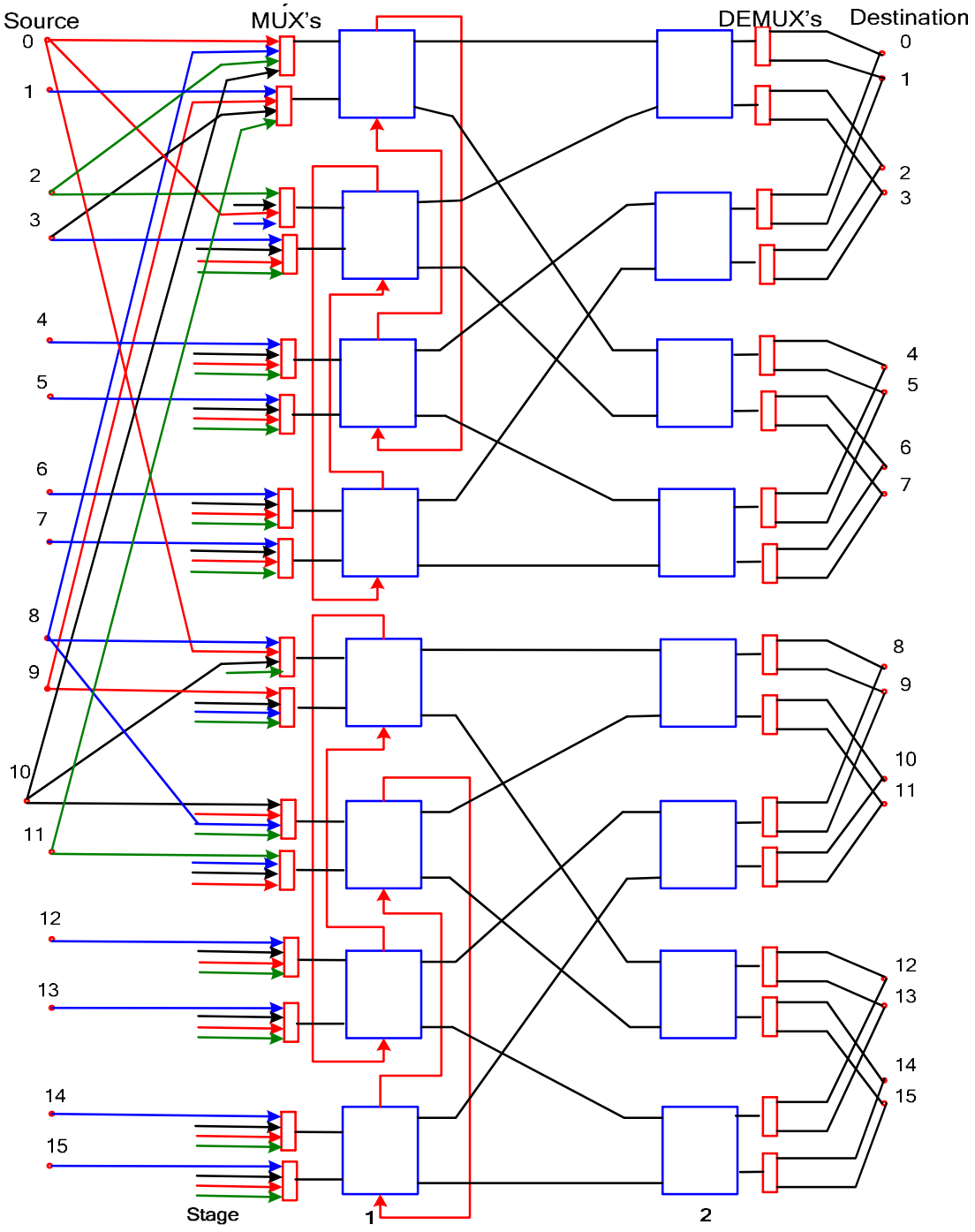

Figure 2.11 : Augmented Baseline Network [9]

The network achieves the multiple path property by permitting two SEs in the same conjugate subset, that are not a conjugate pair, to communicate through auxiliary links. The SEs that communicate through the use of auxiliary links are called a conjugate loop. An ABN of size N consists of N multiplexers of size 4×1, N demultiplexers of size 1×2 and (n-2) stages of N/2 SEs each. The network can tolerate the failure of any SE in the network. The topology of the network is such that it provides on line reparability and maintainability. The ABN cost is N/2*(9*n -11).

2.7 Fault-Tolerant Dynamic Irregular MINs

Fault-tolerant dynamic MINs are irregular in topology i.e. the SEs may not be same in each stage and fork exists at each SE in every stage making them more efficient performance with respect to static irregular MINs.

2.7.1 QUAD Tree Network (QT)

Quad Tree network [11] shown in Figure 2.12 is an irregular type of multistage dynamic network of size $2^n \times 2^n$. Because of irregular architecture, for a given source-destination pair there are multiple paths of different path lengths. It is single switch fault tolerant in every stage. For a connection to a favorite destination, the path length is always 2 irrespective of the size of the network.

2.7.2 ALPHA NETWORK (ALN)

The ALN is shown in Figure 2.13. ALN network of size $2^n \times 2^n$ ($n = \log_2 N$) consists of (2m-1) stages of SEs and in total ($2^{m+2} - 4$) SEs where $m = \log_2(N/2)$. Of these, 2^{n-1} SEs are of size 2×2 and the rest of size 3×3. There are 2^n multiplexers and same number of demultiplexers. The network is single SE fault-tolerant in all the stages. The cost of the network turns out to be $N/2*[17+9\log_2(N/2)]$.

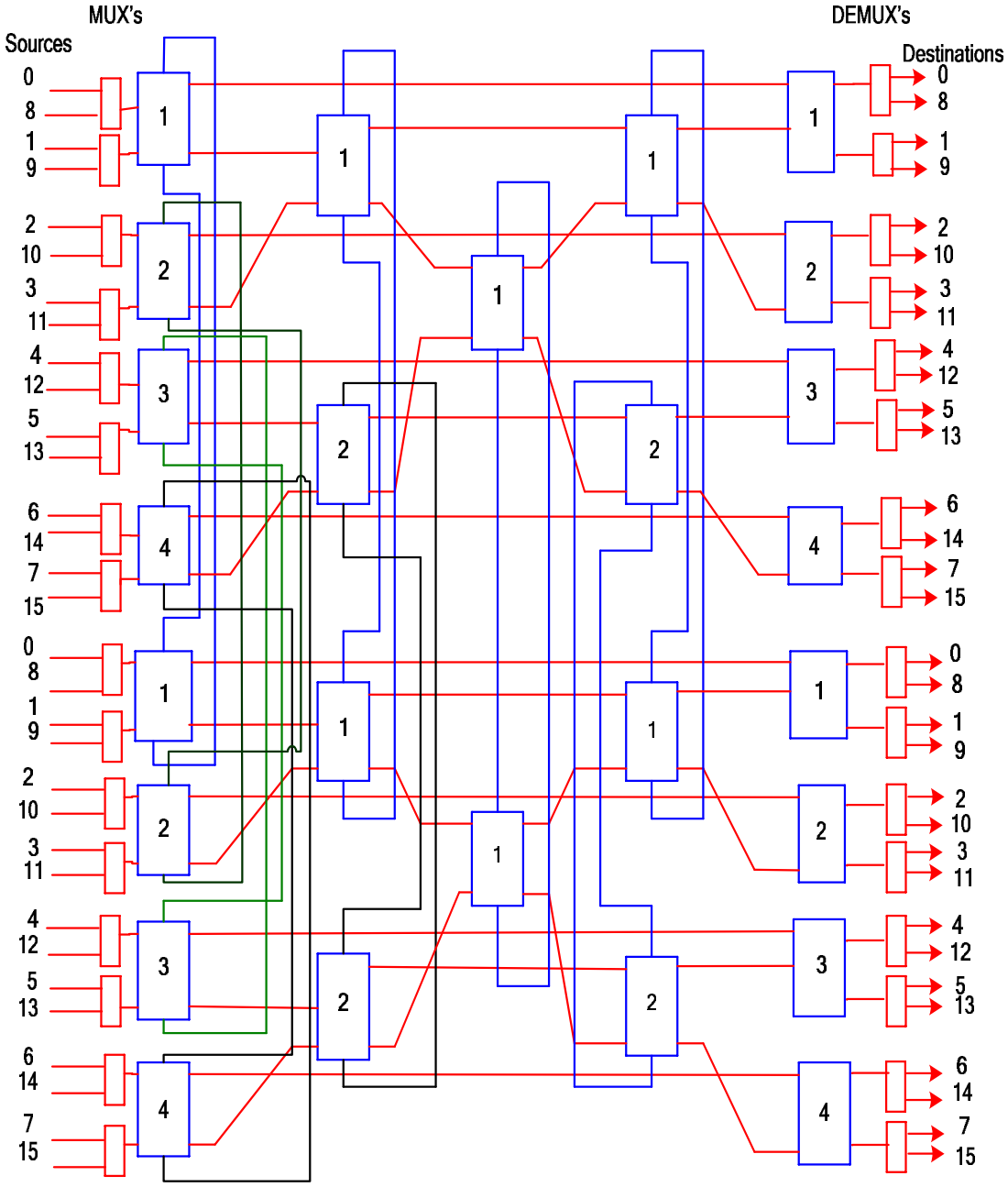

Figure 2.12 : Quad Tree Network [11]

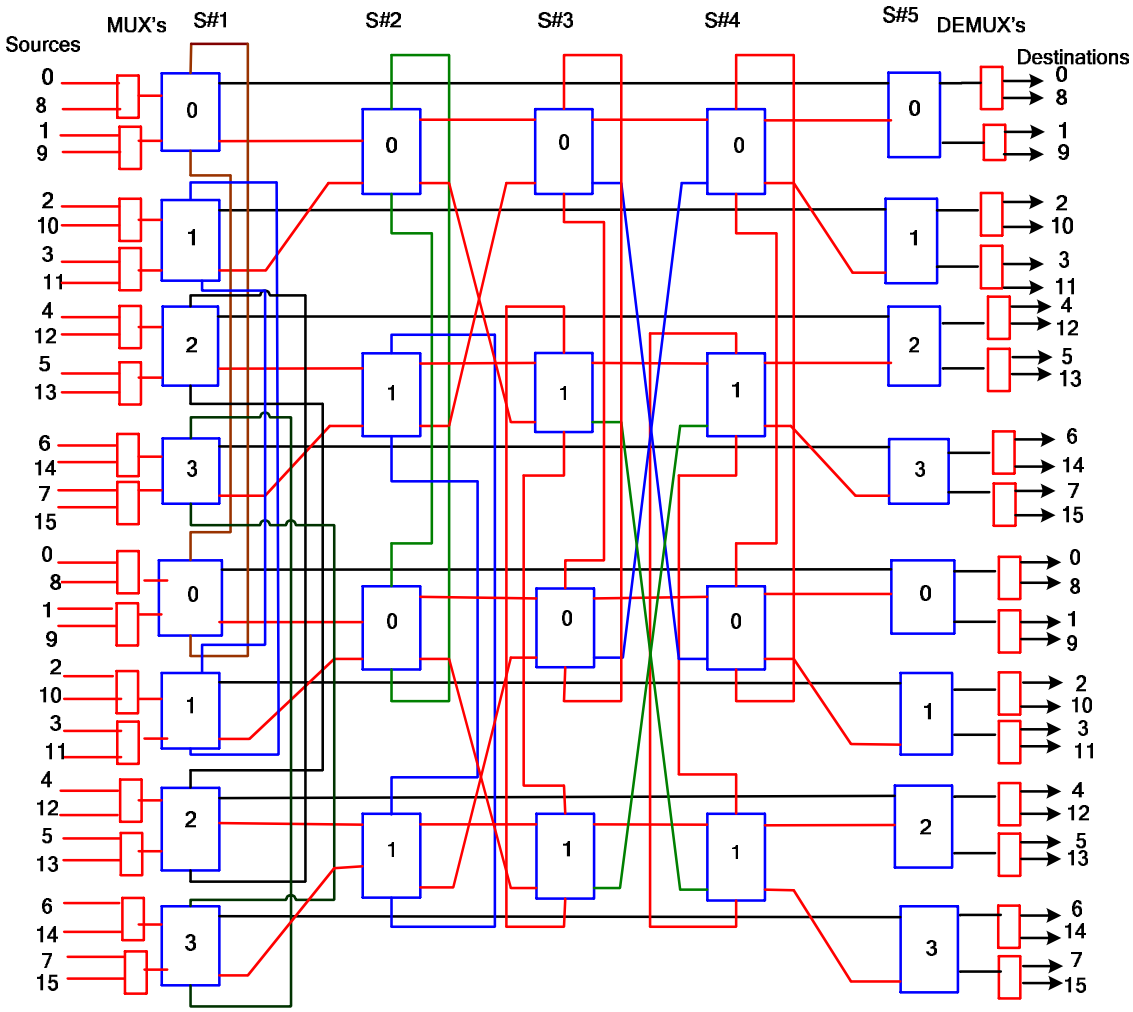

Figure 2.13 : ALN Network[86]

2.7.3 PHI Network (PHN)

The PHN network is shown in Figure 2.14. PHN network of size N×N consists of n stages(n=$\log_2$ N). The input stage has N/2 2×2 SEs, while intermediary (n-2) stages have varying number of 3×3 SEs. Minimum path length of 2 is provided for the favorite memory modules in half of the requests generated at the input. Remaining requests use path length of $\log_2$N. The cost function for PHN is 3N [2 + 3Σ$1/2^i$].

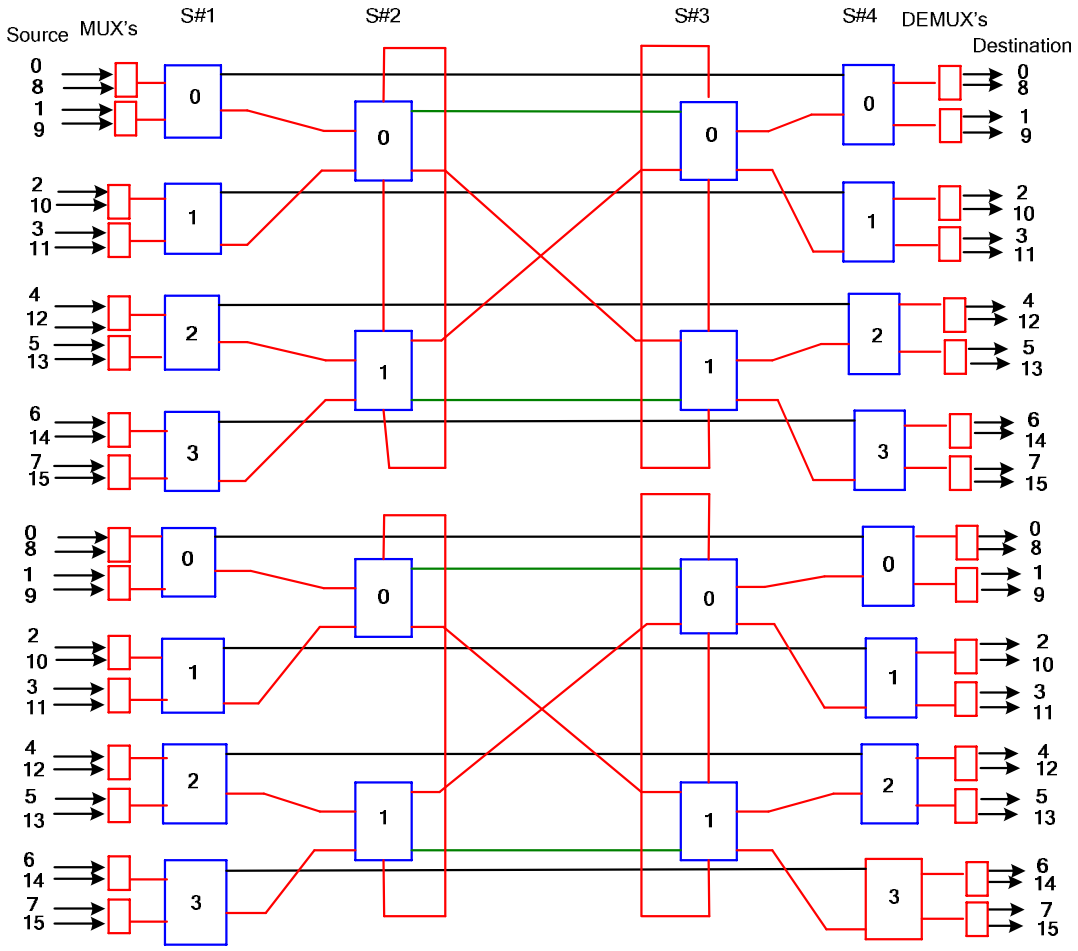

Figure 2.14 : PHN Network [86]

2.7.4 Irregular Augmented Shuffle Exchange Network (IASEN)

Irregular Augmented Shuffle Exchange Network (IASEN) shown in Figure 2.15 is derived from ASEN-2 MIN. The SEs in the first stage form a loop to provide multiple paths if a fault occurs in the next stage. Each source is connected to two different SEs in each group with the help of multiplexer and each destination is connected with demultiplexer.

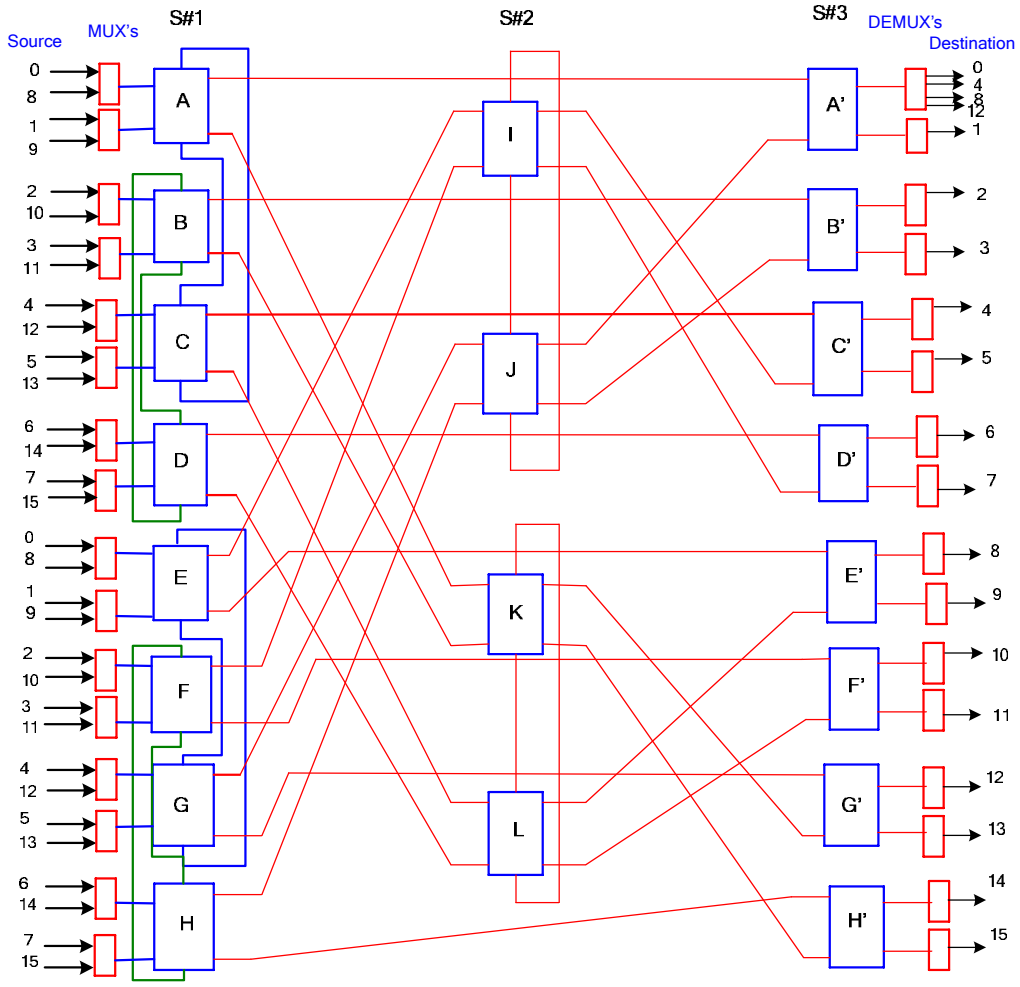

Figure 2.15 : Figure Irregular Augmented Shuffle Exchange Network(IASEN) [3]

2.87 Conclusions

In this chapter, various existing unique path, static and dynamic fault-tolerant MINs, having regular or irregular topology were examined. The study of the existing MINs helps the designer in designing new MINs with better performance or incorporating modifications in the existing MINs so as to improve performance.

In the next chapter, a regular fault-tolerant dynamic MIN namely M_ASEN has been proposed and analyzed for its performance.

Chapter 3

Design and Analysis of the Proposed Regular MIN

This chapter deals with the design, analysis and parametric evaluation of the proposed regular MIN named M_ASEN. The network of size 16×16 is drawn, with its routing algorithm and followed by discussion on fault-tolerance. The routing algorithm is in generalized form applicable for M_ASEN of any arbitrary size. The parameters that have been evaluated for the proposed M_ASEN are : probability of acceptance, bandwidth, reliability, permutations passable and cost. Probability of acceptance and bandwidth have been evaluated for different packet generation rates for fault-free as well as for faulty scenarios.

3.1 Modified Augmented Shuffle Exchange Network (M_ASEN)

The M_ASEN is a dynamic regular fault-tolerant MIN. It is the modification of the existing ASEN [57]. Four techniques have been incorporated in an integrated manner to make it better fault-tolerant and having better performance than the existing ASEN. The techniques are : Chaining , an additional fault-tolerant sub-network, three SEs per loop, change in the location of multiplexers and variation in the number of multiplexers and demultiplexers.

3.1.1 Design of M_ASEN

The proposed MIN is shown in Figure 3.1. The designed MIN corresponds to size 16×16. M_ASEN is a regular type of network as the number of switching elements (SEs) in each stage are equal i.e twelve. There are three stages of SEs labeled as S#1, S#2

and S#3 starting from inputs side. The entire network is comprised of two sub-networks – normal ASEN (N_ASEN) and fault-tolerant ASEN (F_ASEN).

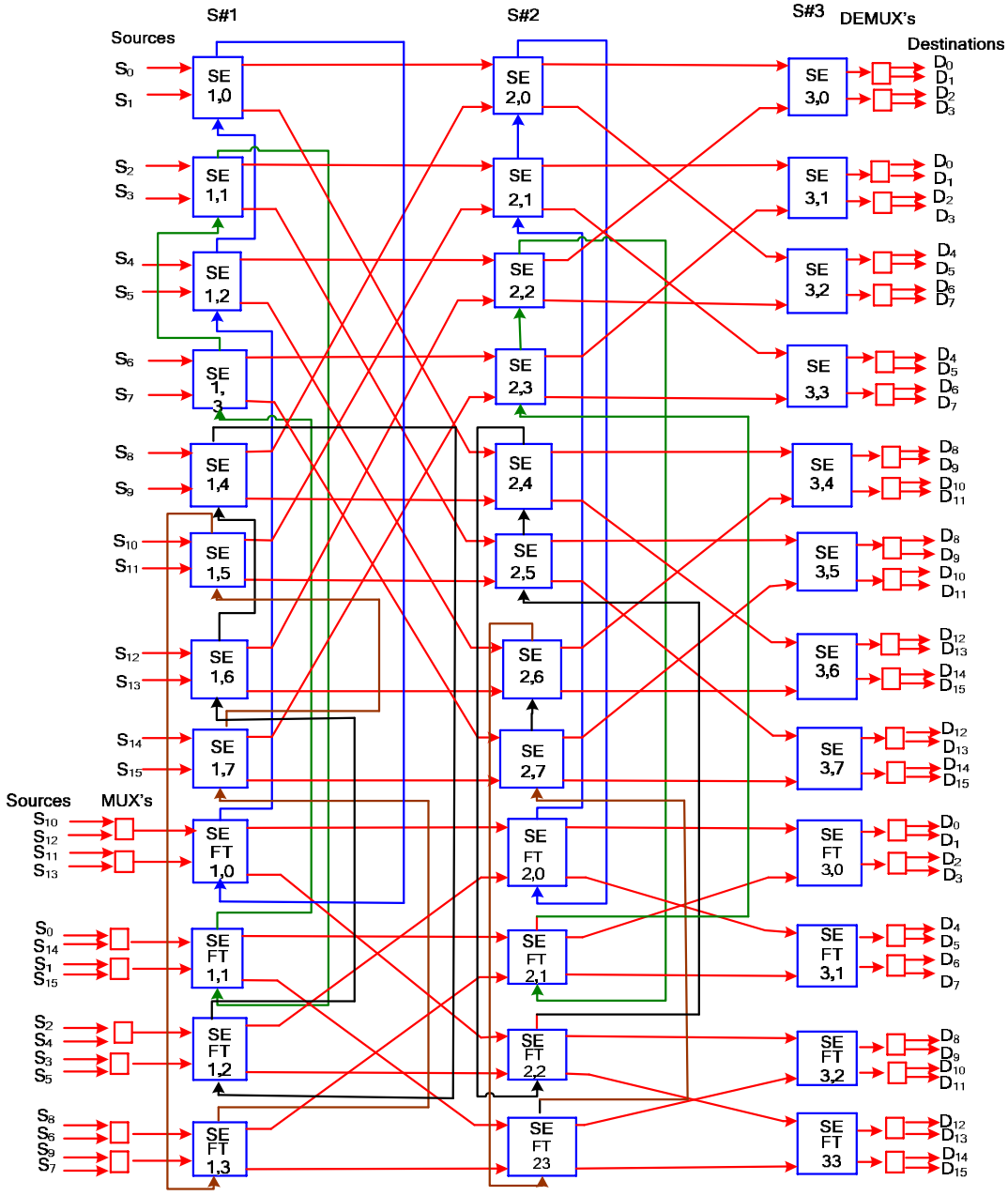

Figure 3.1 : M_ASEN with N=16

These two sub-networks (i.e N_ASEN and F_ASEN) together constitute Modified ASEN (M_ASEN). In N_ASEN, there are twenty four SEs in all, eight SEs per stage. In

F_ASEN, there are twelve SEs in all, four SEs per stage. These SEs are being termed as fault-tolerant (FT) SEs. SEs have been marked as SE# and FT#. The # consists of two digits – the left digit is the label for stage and the right digit stands for the relative position of the SE in that stage from the top starting from zero. The inter-stage connections are as per ASEN [56] network. In general, each subnetwork of M_ASEN consists of $N=m^n$ inputs and N outputs. N is the size of the network. There are (n-1) stages in all. The size of SEs, in all stages, is $(m+1)\times(m+1)$ except in the stage adjacent to outputs where the SEs are of size $m\times m$. Out of (m+1) links, m links are of inter-stage type and one link corresponds to intra-stage auxiliary link. The stages are numbered from 1 to (n-1) starting from input side. In the designed M_ASEN, each stage of N_ASEN consists of m^{n-1} SEs numbered from 0 to $(m^{n-1} – 1)$. Each stage of F_ASEN consists of $m^{n-1}/2$ SEs. Prior to the first stage of SEs in F_ASEN is the stage of multiplexers (each of size 2×1) and after the third stage of SEs in M_ASEN, there is a stage of demultiplexers (each of size 1×2). The $S_0, S_1, \ldots S_{15}$ denote the sources and the $D_0, D_1 \ldots D_{15}$ denote destinations. In addition to inter-stage links, there are intra-stage connections also in the first and the second stage leading to C*haining*. Chaining leads to the formation of loops. In the designed M_ASEN, there are four loops each in first and second stage, each loop comprising of three SEs. Chaining contributes towards fault-tolerance as well as distribution of traffic either during heavy load conditions or during conflicts between packets for the same port.

The designed M_ASEN is better than the existing ASEN (and its variations) in terms of fault-tolerance, probability of acceptance and bandwidth. Moreover, the bandwidth does not degrade under faulty scenarios whereas in case of existing ASEN it degrades. The way the sources are connected to MUX's (in the secondary paths) eliminates the chances of conflict between generated packets in the multiplexers in case of single loop faults in the first stage. This design also supports on-line repairability in case of single loop faults. On-line repairability means that the faulty subnetwork can be simply replaced by the new one without causing a breakdown in the system.

3.1.2 Routing Tag and Routing Algorithm

The proposed architecture makes use of distributed routing strategy i.e. each SE contributes towards routing of packets. Whenever a packet gets generated at a source, a destination address field is always there where the packet has to reach. Each source, as per stored routing algorithm, evaluates and attaches one more field in the packet called routing tag field. The routing scheme assumes that the sources and SEs have the ability to detect faults in the SEs to which they are connected. There are two links (i.e. primary and secondary) for each source. The primary link connects each source to N_ASEN and the secondary link connects the same source to F_ASEN to incorporate fault-tolerance. Each source attempts entry into the MIN via its primary link along with the evaluated routing tag. If the source detects that the primary link led SE has become faulty, then the source steers the packet towards the secondary link. If the first stage SE/MUX at the termination of secondary link is also detected faulty then the MIN loses its dynamic full access capability. For each SE in first/second stage, if the regular output link is busy or if the successor SE in the next stage is faulty, then the packet is steered towards the auxiliary output port of the SE. If at any time there is a conflict for a particular port among three packets (i.e. two at the regular input ports and one coming via auxiliary input port) then any one packet is provided regular output port on random basis, another packet (of the remaining two packets) is provided auxiliary output port again on random basis and the left over packet is buffered.

The algorithm for evaluating routing tag from destination address tag is as follows.
Let $d_{n-1}d_{n-2}\ldots\ldots d_0$ denote the destination address tag and $s_{n-1}s_{n-2}\ldots\ldots..s_0$ be the source address tag within each packet. The destination tag is the address where the packet has to reach and source tag is the source address that has generated the packet.
Let the routing tag be denoted as $t_m t_{n-2} t_{n-3}\ldots..t_0 t_{dm}$.

In the routing tag, the significance of the various bits are as under :

t_m = denotes the multiplexer control bit.

t_{n-2} = denotes the bit that will be sensed by first stage SEs.

t_{n-3} = denotes the bit that will be sensed by the second stage SEs.

……

t_0 = denotes the bit that will be sensed by the last (third)stage SEs.

t_{dm} = denotes the demultiplexer control bit.

Mathematical Function for Routing Procedure

$t_{n-2-i} = d_{n-1-i}$ (for $0 \le i \le n-2$) where $n = \log_2 N$ and N is the size of the Network

$t_m = s_{n-2}$

$t_{dm} = d_0$

For example, let the source address is 0000 and the destination address is 1010. Then, as per mathematical function, the routing tag bits are as follows :

$t_2 = d_3 \quad \Rightarrow \quad t_2 = 1$

$t_1 = d_2 \quad \Rightarrow \quad t_1 = 0$

$t_0 = d_1 \quad \Rightarrow \quad t_0 = 1$

$t_m = s_2 \quad \Rightarrow \quad t_m = 0$

$t_{dm} = d_0 \quad \Rightarrow \quad t_{dm} = 0$

Hence, the routing tag becomes

$t_m t_2 t_1 t_0 t_{dm} = 01010$

3.1.3 Fault Tolerance

We first characterize the SE faults that M_ASEN is guaranteed to survive, and the faults that will always cause the network to fail. It is clear that if both the SEs that a source or destination is connected to become faulty, then that source or destination becomes disconnected from the rest of the network. However, if such critical faults do not occur, several SE faults can be tolerated.

Lemma 1 : If the faults occurring are such that they effect SEs in at most one loop in any stage and there is at least one SE surviving in that loop, then there exists at least one path from every source to every destination of the network.

Consider the loop comprising of SEs SE2,0, FT2,0 and SE2,1 in the second stage. Suppose the SEs SE2,0 and FT2,0 become faulty i.e. SE2,1 is the only surviving SE in the loop. Let the packet generated by the source S_0 has to reach destination D_2. The routing tag becomes 00010. In the absence of the faults, the path would have been

$$S_0 \rightarrow SE1,0 \rightarrow SE2,0 \rightarrow SE3,0 \rightarrow D_2$$

When SE1,0 detects fault in SE2,0, it steers the packet towards SE FT1,0 through its auxiliary port. FT1,0 also detects fault in FT2,0. As such the packet is steered towards SE1,2 via auxiliary port. SE1,2 forwards the packet to SE2,2. Since SE2,2 belongs to another loop (it can't be faulty as per lemma), the path adopted by the packet becomes

$$S_0 \rightarrow SE1,0 \rightarrow FT1,0 \rightarrow SE1,2 \rightarrow SE2,2 \rightarrow SE3,0 \rightarrow D_2$$

The above lemma is applicable to first stage also since the secondary path SE in the fault-tolerant subnetwork belongs to different loop.

The above lemma can also be verified from the redundancy graph of M_ASEN shown in Figure 3.3.

Lemma 2*: *If the faults occurring in M_ASEN are such that they effect SEs in the N_ASEN subnetwork, then there exists atleast one path from every source to every destination of the network i.e. the sub-network F_ASEN of M_ASEN provides full dynamic access capability.

Suppose the packet has to go from source S_{10} to destination D_0. Suppose the SEs SE1,5; SE2,1 and SE3,0 become faulty. The routing tag becomes 00000. The following route is adopted which is totally through F_ASEN.

$$S_{10} \rightarrow FT1,0 \rightarrow FT2,0 \rightarrow FT3,0 \rightarrow D_0$$

The lemma can also be verified from the redundancy graph of M_ASEN shown in Figure 3.3.

Lemma 3 : If the faults occurring in M_ASEN are such that they effect two conjugate SEs (out of three) in the final stage (i.e stage closest to the outputs), then there exists atleast one path from each source to every destination.

Conjugate SEs are the ones that lead to the same set of destinations through demultiplexers e.g. SE3,0; SE3,1 and FT3,0 is one such set. There are in all four sets of conjugate SEs in the stage S#3 in the example network.

Let SE3,0 and SE3,1 become faulty simultaneously. Suppose the packet has to get routed from source S_4 to destination D_0. In the absence of any fault, the route would have been

$$S_4 \rightarrow SE1,2 \rightarrow SE2,2 \rightarrow SE3,0 \rightarrow D_0$$

When the switching element SE2,2 detects fault in SE3,0 it steers the packet to FT2,1 through its auxiliary output port. As such the route adopted by the packet becomes

$$S_4 \rightarrow SE1,2 \rightarrow SE2,2 \rightarrow FT2,1 \rightarrow FT3,0 \rightarrow D_0$$

The lemma can be verified from the redundancy graph of M_ASEN shown in Figure 3.4. The primary routes from all sources to all destinations for M_ASEN are shown in Table A1.1(a) and all secondary routes in Table 1.1(b) [Annexure 1].

3.2 Generalized Analysis of Packet Availability at Ports

In the analysis, the probability of a packet being present at the output port and auxiliary input port of each SE is being calculated. This probability analysis leads to the evaluation of average queue length in each SE and hence the buffer requirement to avoid packet discarding. This probability distribution will also be used in the next chapter for the evaluation of probability of acceptance and bandwidth for the proposed irregular MINs

The following assumptions are being considered in the analysis :

i) Each source generates a packet at the beginning of a network cycle with probability p_0.

ii) The packets generated are mutually independent and distributed uniformly overall the destinations.

iii) If there is a conflict between the two packets arriving at a SE at the beginning of a network cycle for the same output port then any one packet is selected at random and is provided the output port.

iv) All the packets that are passed by the SEs in any stage (say k) are submitted simultaneously to the SEs in the next stage (k+1), irrespective of the number of intra-stage links used by them [55]. This implies that the network cycle time has to be kept proportional to the number of SEs in the loop.

v) A destination can accept upto three packets per network cycle, since each destination is connected to three separate SEs [55].

vi) In the analysis carried out here, non-priority routing is considered i.e. if there is a conflict between two packets (one on any of the input ports and the other on the auxiliary link), then any one of the two packets is provided output port on a random basis.

There are two aspects that need to be discussed before going for bandwidth analysis. A SE is said to *generate* a packet if the packet routed to an auxiliary port is the result of the conflict between the two packets arriving at the input ports of that SE. And a SE is said to *propagate* a request if the packet arriving at its auxiliary port is in conflict with the packet arriving at one of its input ports.

The following notations are in use for performing *probability of acceptance* and *bandwidth* evaluation :

SE# = SE stands for a particular switching element labeled "#". "#" denotes the position of the SE from the top in a particular stage. "#" comprises of two digits, the first digit denotes the stage and the second digit denotes the position of the SE in that stage from the top.

p_0 = Probability that a source submits a packet at the beginning of a network cycle.

$p_{gen\_SE\#}$ = Probability that a particular SE labeled "#" *generates* a packet for its auxiliary port.

$p_{prop\_SE\#}$ = Probability that a specific SE labeled "#" *propagates* a packet on its auxiliary port.

$p_{aux\_SE\#}$ = Probability that a particular SE labeled "#" receives a packet on its auxiliary port, which is independent of the request sent out on its auxiliary port.

$p_{out\_SE\#}$ = Probability of a packet being present on any output port of a SE

$p_{in\_SE\#}$ = Probability of a packet being present on any input port of a SE

To evaluate $p_{aux\_SE\#}$ for a particular SE of a loop, disconnect a loop in stage k contain L_k SEs in such a way that the particular SE under consideration is the last one in the sequence. As per the reference [55], the formula for evaluating $p_{aux,SE\#}$ is :

$p_{aux\_SE\#} = p_{gen,SE\#}$

$p_{gen\_SE\#}$, $p_{prop\_SE\#}$ and $p_{out\_SE\#}$ are evaluated using equations (3.1) to (3.10) .

To calculate $p_{gen\_SE\#}$, the only way a request is not generated for the a-out link is if all the packets on the regular input links are mapped into the b output links in a one-to-one fashion. The probability that no two packets conflict for an output link, given that there are i requests at the inputs of the SE, is given by

$$p_{gen\_SE\#} = 1 - \sum_{i=0}^{b} {}^{b}C_i p_{in\_SE\#}^{i} (1 - p_{in\_SE\#})^{b-i} * (NC(i)) \qquad (3.1)$$

$$\text{where } NC(i) = b!/(b-i)! * 1/ b^{i} \qquad (3.2)$$

As per reference [55], the formulae to evaluate $p_{prop\_SE\#}$ and $p_{out\_SE\#}$ become as under:

In case of fault-free scenario, then none of the packets are steered towards fault tolerant subnetwork.

As such

$$p_{gen\_FT11} = p_{gen\_FT12} = p_{gen\_FT13} = p_{gen\_FT14} = 0 \qquad (3.3)$$

$$p_{prop\_SE\#} = \sum_{i=0}^{b} {}^{b}C_i * p^{i}_{in\_SE\#} * (1 - p_{in\_SE\#})^{b-i} * NC(i) * i/b \qquad (3.4)$$

$$p_{out\_SE\#} = 1 - [(1-p_{in\_SE\#}/b)^{a} * (1-p_{aux\_SE\#}/b)] \qquad (3.5)$$

To evaluate $P_{aux\_SE\#}$ for a particular SE of a loop, disconnect the loop in such a way that the particular SE is in the last (bottom) one in the sequence diagram as shown in Figure 3.2. The sequence diagram, in general, is shown in Figure 3.2 and the corresponding generalized equations are as under (3.6a) to (3.6c)

$$P_{aux\_SE\_Z} = P_{gen\_SE\_Y} + P_{gen\_FT\_X} * P_{prop\_SE\_Y} \quad (3.6a)$$

or

$$P_{aux\_SE\_Z} = P_{gen\_FT\_Y} + P_{gen\_SE\_X} * P_{prop\_FT\_Y} \quad (3.6b)$$

or

$$P_{aux\_FT\_Z} = P_{gen\_SE\_Y} + P_{gen\_SE\_X} * P_{prop\_SE\_Y} \quad (3.6c)$$

The equations corresponding to the sequence diagram 3.3 are shown in appendix 1.

Since the arrival rates at the two inputs of a SE of second stage may be different, then mean arrival rate is taken into consideration. Consider the following notations:

p_{in1_SE21} = Probability of a packet being present at the upper regular input port of SE2,1

p_{in2_SE21} = Probability of a packet being present at the lower regular input port of SE2,1

In general,

$p_{in\_SE\#}$ = Probability of a packet being present at the upper/lower input port of a specific SE of a specific stage(mentioned in the subscript in place of #).

$$p_{in\_SE\#} \text{ (second stage)} = p_{out\_SE\#} \text{ (first stage)} \quad (3.7)$$

For evaluating p_{gen_SE} and p_{prop_SE} of second stage SEs, mean value of packet arrival probability is used and is given as :

$$p_{in\_SE\#} = (p_{in1\_SE\#} + p_{in2\_SE\#})/2.0 \quad (3.8)$$

The set of equations getting generated from equation (3.6) can be altered as per loops of second and third stages to evaluate p_{aux_SE} for respective stage SEs. The $p_{out\_SE\#}$ for SEs of second stage as per reference [55] is

$$p_{out\_SE\#} = 1 - (1-p_{in1\_SE\#}/b)(1-p_{in2\_SE\#}/b)*(1-p_{aux\_SE\#}/b) \quad (3.9)$$

Let us now consider SEs of final (stage closest to outputs) stage. Here also, the probability of a packet at the two inputs of a SE may be different. Since no chaining is being used in

the last stage, as such on the basis of work done by Patel [76], the output of a SE is evaluated and is given as :

$$p_{in\#\_SE\#} \text{ (final stage)} = p_{out\_SE\#} \text{ (previous stage)} \quad (3.10)$$

$$p_{out\_SE\#} = 1 - (1 - p_{in1\_SE\#}/b)*(1 - p_{in2\_SE\#}/b) \quad (3.11)$$

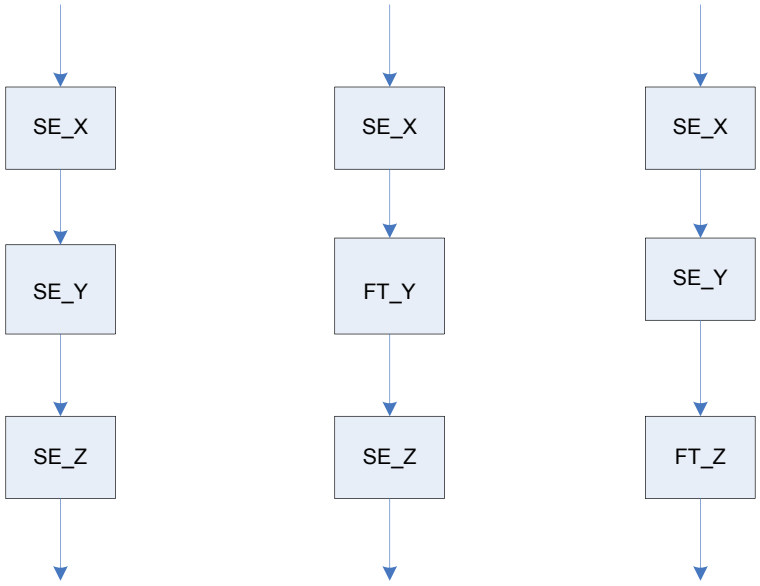

Figure 3.2 : Sequence Diagram in General

3.3 Analysis of Modified ASEN (M_ASEN)

In this section, first of all, the proposed M_ASEN has been analyzed for the probability of packet availability at the output and auxiliary port of each SE under fault-free as well as faulty scenarios. This probability analysis has been used subsequently for the evaluation of probability of acceptance and bandwidth, again for faulty-free and faulty scenarios. This probability analysis also leads to the evaluation of average queue length in each SE and hence the optimal buffer requirement to avoid packet discarding. Thereafter, terminal reliability has been evaluated for favorite as well as for non-favorite destinations followed by cost evaluation.

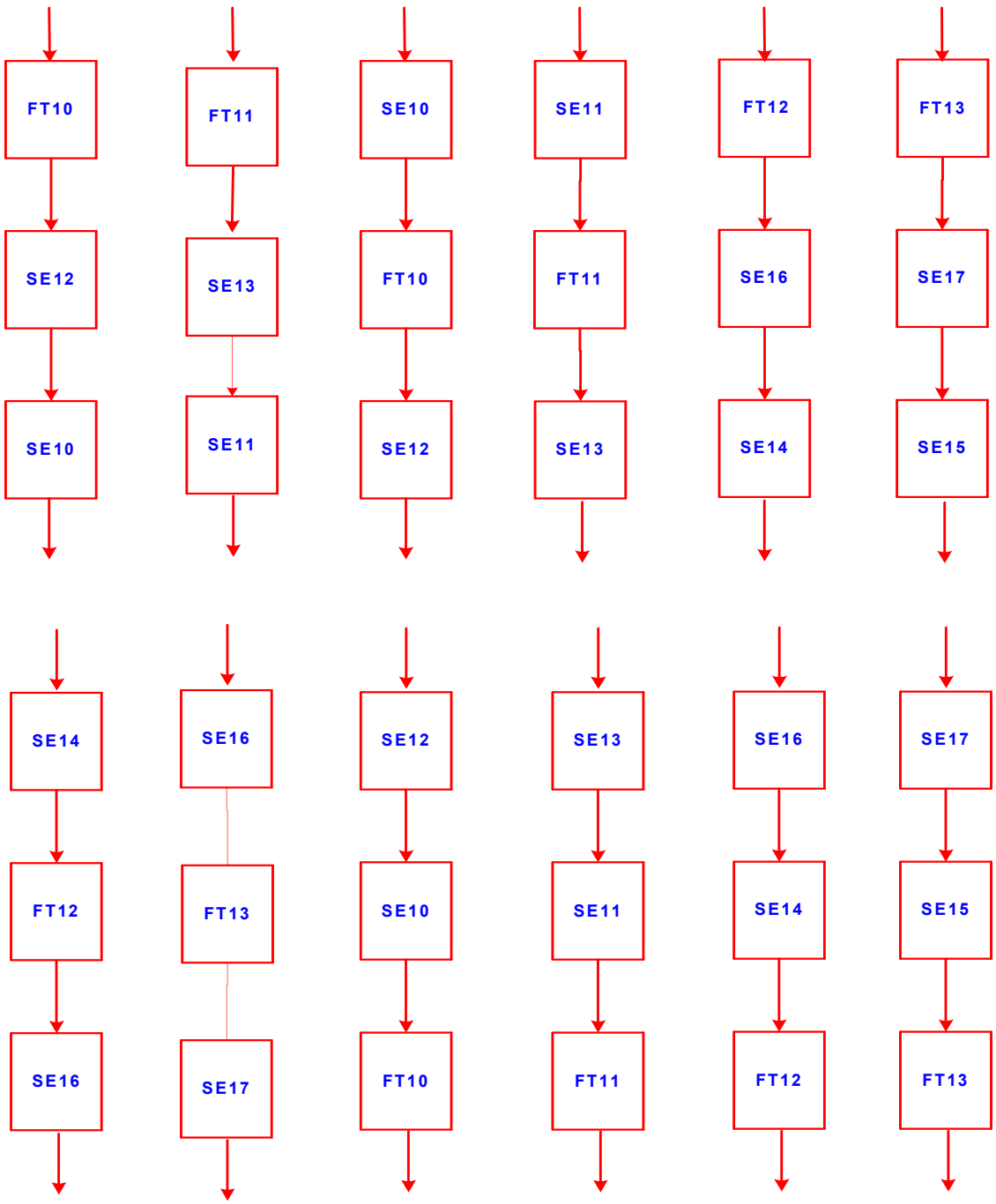

Figure 3.3 : Sequence Diagram of SEs in first stage

3.3.1 Probability of Packet Availability at ports

The equations for evaluating the probability of a packet being present at the auxiliary ports of first and second stage, at the input and output ports of second stage, at the output ports of third stage SEs are given in Tables labeled A1.2(a) to A1.2(e) (Appendix 1).

3.3.2 Probability of Acceptance and Bandwidth

Probability of acceptance, as defined in chapter 1, is the ratio of the average number of requests accepted by the destination to the average number of requests submitted by the sources per network cycle and bandwidth is defined as the average number of requests accepted per network cycle. In the Tables 3.1(a)-3.1(b), the probability of acceptance and bandwidth parameter values of M_ASEN have been evaluated for fault-free and single loop fault in the first stage respectively.

Table 3.1(a)

Prob. of acceptance and Bandwidth values for M_ASEN under fault-free conditions

Pkt. gen. rate	Bandwidth	Prob. of acceptance	Pkt. gen. rate	Bandwidth	Prob. of acceptance
0.1	1.5668	0.9793	0.6	8.4851	0.8839
0.2	3.0729	0.9603	0.7	9.6435	0.8610
0.3	4.5223	0.9422	0.8	10.7025	0.8361
0.4	5.9131	0.9239	0.9	11.6549	0.8094
0.5	7.2377	0.9047	1.0	12.4976	0.7811

Table 3.1(b)

Prob. of acceptance and Bandwidth values for M_ASEN when single loop fault in first stage

Pkt. gen. rate	Bandwidth	Prob. of acceptance	Pkt. gen. rate	Bandwidth	Prob. of acceptance
0.1	1.5796	0.9873	0.6	8.4615	0.8814
0.2	3.1133	0.9729	0.7	9.5167	0.8497
0.3	4.5871	0.9556	0.8	10.4393	0.8156
0.4	5.9823	0.9347	0.9	11.2297	0.7798
0.5	7.2794	0.9099	1.0	11.8936	0.7434

3.3.3 Average Queue Length and Optimal Buffer Requirement

It has been recognized that buffers in MINs can increase the MIN performance significantly. They also prevent a packet from being lost when a path conflict occurs. When buffers are kept in each SE, then a packet can leave its buffer only when the destination buffer at the succeeding stage is able to accept it.

Table 3.2
Optimal Buffer Requirement in M_ASEN

SE#	Avg. queue length at O/Ports	Min no. of buffers at O/ Ports	Avg queue length at aux ports	Min no. of buffers at aux ports	SE#	Avg queue length at O/Ports	Min no. of buffers at O/Ports	Avg queue length at aux ports	Min no. of buffers at aux ports
SE1,0	3.5211	4	0.5	1	SE2,6	1.1363	2	0.0288	1
SE1,1	3.5211	4	0.5	1	SE2,7	1.1363	2	0.0288	1
SE1,2	2.25	3	0.0	0	FT2,0	0.5042	1	0.0	0
SE1,3	2.25	3	0.0	0	FT2,1	0.5042	1	0.0	0
SE1,4	3.5211	4	0.0	0	FT2,2	0.4330	1	0.0	0
SE1,5	3.5211	4	0.5	1	FT2,3	0.4330	1	0.0	0
SE1,6	2.25	3	0.0	0	SE3,0	0.7641	1	-	-
SE1,7	2.25	3	0.0	0	SE3,1	0.7641	1	-	-
FT1,0	0.225	1	2.25	3	SE3,2	0.7909	1	-	-
FT1,1	0.225	1	2.25	3	SE3,3	0.7909	1	-	-
FT1,2	0.225	1	2.25	3	SE3,4	0.6733	1	-	-
FT1,3	0.225	1	2.25	3	SE3,5	0.6733	1	-	-
SE2,0	1.7559	2	0.2083	1	SE3,6	0.7391	1	-	-
SE2,1	1.9686	2	0.4062	1	SE3,7	0.7391	1	-	-
SE2,2	1.4240	2	0.0352	1	FT3,0	0.3225	1	-	-
SE2,3	1.9028	2	0.3371	1	FT3,1	0.3225	1	-	-
SE2,4	1.3660	2	0.1439	1	FT3,2	0.3225	1	-	-
SE2,5	1.3660	2	0.1439	1	FT3,3	0.3225	1	-	-

The Table 3.2 gives the average queue length of packets and optimal buffer requirement at the output ports and auxiliary input port of each SE at every stage corresponding to request generation rate of 1.0. Since in the first network cycle, the packets that have arrived in the first stage get distributed from the normal subnetwork into fault-tolerant subnetwork that is why more buffers are required in the first stage as compared to in the subsequent

stages. Since there are no auxiliary links in the last (third stage), as such hypen has been shown in the columns in the a above Table.

3.3.4 Terminal Reliability

Terminal Reliability is the probability that a given source-destination pair has at least one fault-free path between them, given that each SE has a certain reliability (the reliability of a SE is the probability that it is fault-free). In case of interconnection networks having regular topology, the terminal reliability is independent of the relative position of the source and destination pair considered. The terminal reliability of a MIN can be evaluated by considering its redundancy graph.

The redundancy graph for M_ASEN is shown in Figure 3.4

Consider the loop formed by the SE1,0; SE1,2 and FT1,0 in the first stage. Let r denote the reliability of SE. Atleast, one of the three SEs must be fault free. The probability that atleast one of the SEs in the first stage is fault free is

$$R_{S\#1} = \left[1 - (1- r)^3\right]$$

In second stage, atleast one of the three SEs namely SE2,0; SE2,2 and FT2,0 must survive

$$R_{S\#2} = \left[1 - (1- r)^3\right]$$

For the entire path, one specific SE should survive from the last stage.

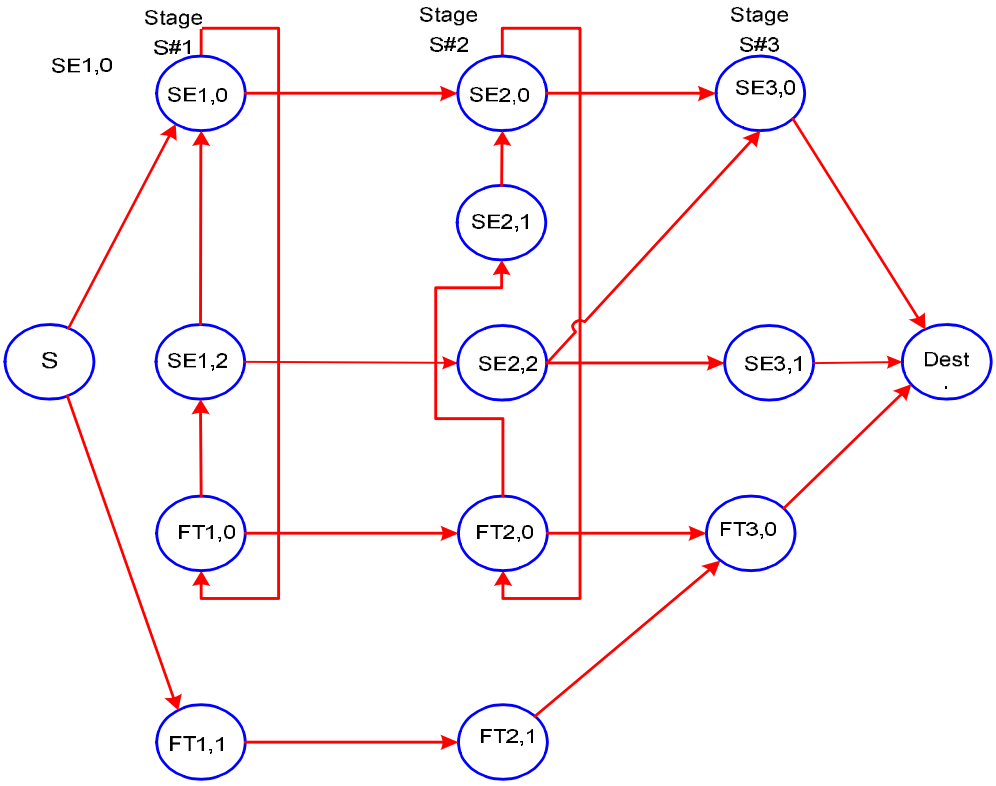

Figure 3.4: Redundancy Graph for M_ASEN

Hence the reliability of the path (comprising of loop in first and second stage) becomes

$R_{path\_1} = R_{S\#1} \times R_{S\#2} \times r$

Reliability of path comprising of FT1,1; FT2,2 and FT3,0

$R_{path\_2} = r^3$

The probability that

Path_1 fails = $1 - R_{path\_1}$

Path_2 fails = $1 - R_{path\_2}$

The probability that path_1 and path_2 both fail together is $(1 - R_{path\_1}) \times (1 - R_{path\_2})$

Probability that, atleast, one path survives

$R_{term} = [\ 1 - (1 - R_{path\_1}) \times (1 - R_{path\_2})\ ]$

Table 3.3
Terminal Reliability of M_ASEN

SE Reliability	Terminal Reliability
0.90	0.9724
0.92	0.9821
0.94	0.9898
0.96	0.9954

The terminal reliability values when compared with the corresponding SE reliability values in Table 3.3 reveal that terminal reliability values are higher than assumed values of SE reliabities. Hence, the proposed design is worthwhile considering the terminal reliability aspect.

3.3.5 Hardware Complexity and Cost

However, here only SE complexity is being used for the evaluation of cost.

To estimate the cost of a network, one common method is to calculate the switch complexity with an assumption that the cost of a SE is proportional to the number of crosspoints involved. For example, a 2×2 SE has 4 units of cost and a 3×3 SE has 9 units of cost. For multiplexers and de-multiplexers, it is assumed that each of k×1 and 1×k has k units of cost.

Total number of stages = (n-1)

Total number of SEs $= (n-1)\times\left(m^{n-1}+\frac{m^{n-1}}{2}\right)$

Total number of links = $(n-2)\left(\frac{N}{2}*2+\frac{N}{4}*2\right)$

$$= (n-2)\left(N+\frac{N}{2}\right)$$

$$= \frac{3N}{2}(n-2)$$

Cost = $9*(n-1)\left(m^{n-1}+\frac{m^{n-1}}{2}\right)-9*\left(m^{n-1}+\frac{m^{n-1}}{2}\right)+4\left(m^{n-1}+\frac{m^{n-1}}{2}\right)$

$$= (9n-14)*\left(m^{n-1}+\frac{m^{n-1}}{2}\right)$$

Total number of multiplexers and demultiplexers = $4m^{n-1}$

Total cost of multiplexers and demultiplexers = $2 * 4m^{n-1}$

Total cost of M_ASEN = $(9n-14)*\left(m^{n-1}+\frac{m^{n-1}}{2}\right)+2*4m^{n-1}$

The cost of various sizes of M_ASEN has been evaluated and is given below :

Table 3.4
Cost of different size M_ASEN

Size of M_ASEN	Cost
16 × 16	328
32 × 32	872
64 × 64	2176
128 × 128	5216
256 × 256	12160
512 × 512	27776
1024 × 1024	62464

3.3.6 Permutation Passable in M_ASEN

A permutation for a network is a pairing of its sources and destinations such that each source appears in exactly one pair and each destination appears also in exactly one pair. In other words, a permutation is a full one-to-one mapping between the network sources and destinations.

The sixteen tables labeled as A1.3(a) to A1.4(p) (Annexure 1) are the basic ones, each table representing two permutations (the first two columns representing one permutation and the last two columns representing the second permutation). Corresponding to each basic table, there are fourteen sub-tables (i.e. seven pairs of sub-tables) e.g sub-tables A1.3(a)-i and A1.3(a)-ii constitute one pair of sub-table corresponding to the basic table A1.3(a) (Annexure 1). Similarly, sub-tables A1.3(a)-iii and A1.3(a)-iv constitute another pair of sub-tables corresponding to the basic table A1.3(b) and so on. The basic table is shown included in each pair of sub-tables. Each pair of sub-tables represents 16 permutations (excluding two permutations of basic table).

As such, number of permutations represented by seven pairs of sub-tables = 7 * 16 = 112

Number of permutations as represented by the basic table = 2

Thus, total number of permutations by a single basic table and its associated set of pair of sub-tables = 112 + 2 = 114

Number of basic tables = 16 [A.4 (a) to A.4(p) in Annexure 1]

Hence, total number of possible permutations passable in M_ASEN = 16*114

= 1824

A prominent feature of the proposed M_ASEN is that it retains the above mentioned permutations passability feature even in the presence of first stage non-critical faults which is an edge over the existing ASEN.

3.4 Conclusions

In this chapter, the design of a dynamic regular MIN namely M_ASEN has been proposed along with routing tag evaluation and also analyzed for parametric evaluation. A prominent feature of the designed MIN is that it is highly fault-tolerant. It can survive and retain the property of dynamic full access on the basis of fault-tolerant sub-network only. The sources have been connected to the multiplexers of fault-tolerant sub-network in such a way that blocking in multiplexers is avoided during faulty scenarios. In the analysis of the proposed MIN, the probability of a packet being present at the regular output port as well as at the auxiliary port of each SE has been evaluated followed by parametric evaluation. The packet traffic distribution that has been tabulated corresponds to packet generation rate of 0.5, 0.8 and 1.0. The parameters that have been evaluated are probability of acceptance, bandwidth, fault-tolerance, reliability, permutations passable and cost. The M/M/1 queuing model along with the results of packet traffic distribution leads to the evaluation of average queue length and optimal buffer requirement. The probability of acceptance and bandwidth values in M_ASEN corresponding to packet generation rate of 1.0 are 0.7811 and 12.4976 which are higher than that of existing ASEN-2 and ASEN-4 (The probability of acceptance and bandwidth values in ASEN-2 are 0.5812 and 9.2986 respectively. In ASEN-4, the corresponding values are 0.5998 and 9.5970 respectively). Regarding fault-tolerance, the proposed M_ASEN can tolerate two SE faults in each loop every stage whereas ASEN-2 is single SE fault-tolerant. The terminal reliability, path length and permutations passable are comparable with the existing ASEN. The terminal

reliability of M_ASEN has been evaluated as 0.9724 whereas that of existing ASEN-2 is 0.953 and that of ASEN-MAX (ASEN-4) is 0.960. The path length feature remains same i.e 3. The permutations passable in M_ASEN are 1824 and the same are possible in existing ASEN.

The next chapter presents the designs, routing tag evaluation algorithms, detailed analysis and performance parametric evaluations of three proposed dynamic irregular MINs namely M_FDOT, Hybrid and M_QUAD. In the detailed analysis, the probability of a packet being present at the output port and auxiliary port of each SE is being evaluated for each of the designed MIN for different packet generation rates under normal as well as faulty conditions.

Chapter 4

Design and Analysis of the Proposed Irregular MINs

MINs can be designed either with regular or irregular topology. Irregular MINs have an edge over regular networks considering path length feature for favorite destinations. The path length for favorite destinations usually remains constant in irregular networks leading to reduced network latency especially for larger sized MINs. This chapter deals with the design and analysis of the proposed irregular MINs. Three irregular MINs namely M_FDOT, Hybrid and M_QUAD have been proposed. Corresponding to each proposed MIN, a 16×16 sized network has been drawn, followed by its routing tag evaluation algorithm and discussion on fault-tolerance. Although, the networks shown in various Figures are of size 16×16, but with the given construction procedure, any sized network can be designed. The routing algorithms are in generalized form applicable to network of any arbitrary size. In the analysis of the proposed MINs, the probability has been evaluated for packet availability at each port in all SEs for fault free as well as for faulty scenarios. The other parameters that have been evaluated are – probability of acceptance, bandwidth, terminal reliability, hardware complexity and cost, permutations passable and optimal buffer requirement in the SEs. Probability of acceptance and bandwidth have been evaluated for different packet generation rates for fault-free as well as for faulty scenarios.

4.1 Modified FDOT Network (M_FDOT)

The existing FDOT MIN has been modified and named as M_FDOT. The M_FDOT is a dynamic irregular fault-tolerant MIN. The techniques that have been incorporated to make it highly fault-tolerant and efficient in performance are : *Chaining* and an *additional fault-tolerant sub-network.* The following section discusses the design of this MIN.

4.1.1 Design of M_FDOT

The design is shown in Figure 4.1. The designed MIN corresponds to size 16×16.

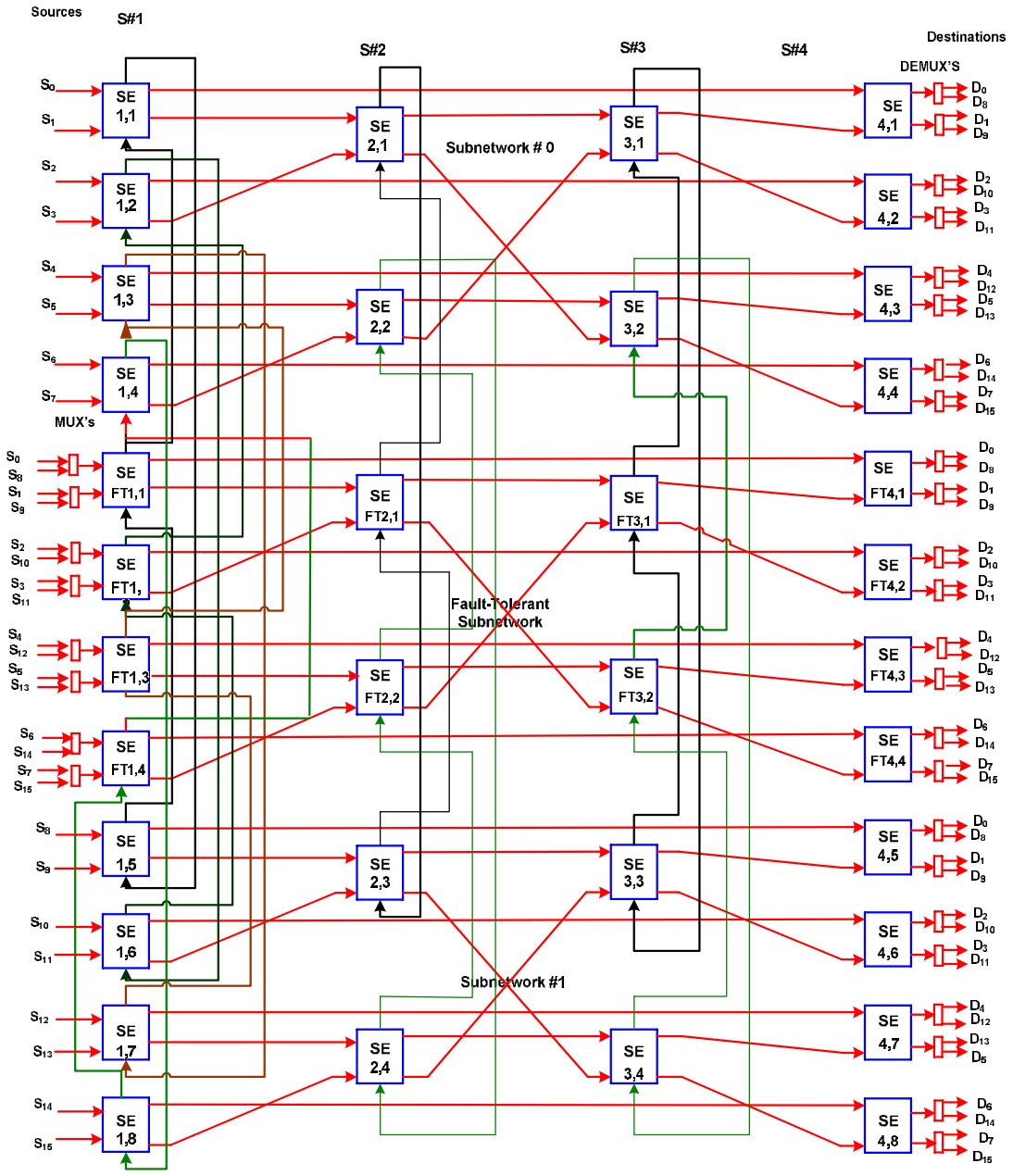

Figure 4.1: M_FDOT Network with N=16

The M_FDOT shown in Figure 4.1 corresponds to the size 16×16. The entire network is comprised of two sub-networks – *normal sub-network* (comprising of sub-network#0 and sub-network#1) and *fault-tolerant sub-network*. The entire network can be looked upon in two ways. The first one is in terms of sub-networks. Normal sub-network comprises of twenty-four switching elements (SEs): eight SEs in first stage, followed by four SEs each in second and third stage and eight SEs in the last (fourth) stage. Fault-tolerant sub-network comprises of twelve SEs four SEs in the first stage, followed by two SEs each in the second and third stage and four SEs in the last stage. The second way of looking at the network is in terms of stages. There are four stages of SEs marked S#1, S#2, S#3 and S#4. In the first stage, there are twelve SEs (four SEs belonging to sub-network#0, four SEs belonging to fault-tolerant sub-network and four SEs of sub-network#1), the second and third stage each has six SEs (two SEs belonging to sub-network#0, two SEs belonging to fault-tolerant sub-network and two SEs belonging to sub-network #1) and the last stage has again twelve SEs. The size of each SE in the first, second and third stage is 3×3 and the size of each SE in the last(fourth) stage is 2×2. The numbers written prior to multiplexers denote the sources which are attached to that specific multiplexer e.g. the numbers (0,8) written prior to multiplexer attached with FT1,1 indicates that sources 0 and 8 are connected with this particular MUX. As such, each source is connected to two sub-networks: primary sub-network directly and to the fault-tolerant sub-network via multiplexer. The size of each de-multiplexer is 1×2. There are four loops in the first stage, each loop comprising of three SEs. Whenever, a fault is detected in the next stage or blocking is encountered in any SE, the packet is steered intra-stage via auxiliary output port of the SE. In the second stage, there are two loops each having three SEs. Same is the status of third stage. Loops of SEs provide fault-tolerance by providing multiple paths and bypassing the faulty SE. Loops in the first stage provide fault-tolerance in case of faulty SEs in the second and last stage. Loops of stage S#2 account for fault-tolerance in third stage and loops in third stage take care of fault-tolerance in last stage. If all the SEs of a loop (of any stage) become faulty at the same time, then the MIN loses its DFA capability. In M_FDOT, there are n stages where $N = 2^n$, N is the size of the network and n is even. There are $N/2^j$ and $((N/2^j)/2)$ number of SEs

in any stage of normal and fault-tolerant sub-network respectively where j is the label of the stage and the value of j varies from 1 to n/2. Stage j and (n+1-j) have the equal number of SEs. The inter-stage connections are to be made as under :

Mark the input and output ports of each SE starting with 0 from top to bottom in each stage. Connect the even numbered output ports of each stage (except stage n/2) with the same even numbered input ports of SEs of associated stage. The stages which are equidistant from left and right are being termed as associated stages. Connect the odd numbered output ports of two adjacent SEs with the input ports of SE in the next stage, for stages 1,2…….. n/2. Label the output ports of each set of SEs (of stage n/2) from top to bottom as 0,1,2,3. Similarly, label the input ports of each set of SEs (of stage n/2 +1) as 0,1,2,3. Connect the even labeled output ports of stage n/2 with the same even number input ports of stage (n/2+1) and cross connect the odd numbered output ports of stage n/2 with input ports of stage (n/2+1).

4.1.2 Routing Tag and Routing Algorithm

The switching scheme assumes that the sources and SEs have the ability to detect faults in the SEs to which they are connected [7-10]. There are two paths (i.e. primary and secondary) between each source-destination pair. The packet from each source attempts entry into the MIN through primary path along with the evaluated routing tag. If, in the primary path, the SE of first stage is faulty then the source steers the packet towards the secondary path. The secondary path leads the packet into the fault-tolerant sub-network. A faulty multiplexer is considered as a failure of its associated SE.

Considering network of size 16×16 as shown in Figure 4.1, the routing tag comprises of six bits. Let the bits in the routing tag be denoted as $t_m.t_3.t_2.t_1.t_0.t_{dm.}$ Let the destination address be represented as $d_3.d_2.d_1.d_0$. The sources marked S_0 to S_7 transmit via subnetwork #0 and sources marked S_8 to S_{15} transmit via sub-network #1 under normal conditions (no faults). The bit t_3 in the routing tag is sensed by concerned SE of the stage S#1 and if it is 0, the packet is steered towards the upper output port of the SE and if it is 1, the packet is steered towards the lower output port. The SEs of stage S#2 sense the bit t_2 and depending

on its value (0 or 1), the packet is steered either towards the upper or lower output port respectively. The SEs of stage S#3 take steering decision based on routing tag bit t_1 and SEs of last stage i.e. S#4 consider tag bit t_0 for forwarding the packet.

Chaining of SEs in each stage provides multiple paths leading to fault-tolerance. In the designed MIN, chaining has been done in the first, second and third stages. The routing tag bit t_m serves as the control signal for the multiplexer. The switching mechanism within the fault-tolerant sub-network remains the same. The bit t_{dm} is the control signal for the de-multiplexer.

Routing Tag Algorithm

The algorithm for evaluating routing tag from destination address is as follows.

Let $d_{n-1}d_{n-2}\ldots\ldots d_0$ denote the destination address

Let $s_{n-1}s_{n-2}\ldots\ldots..s_0$ be the source address.

The destination address is the address where the packet has to reach and source address is the source address that has generated the packet. Let the routing tag be denoted as

$t_m t_{n-1} t_{n-2}\ldots..t_0 t_{dm}$.

In the routing tag, the significance of the various bits is as under :

t_m = denotes the multiplexer control bit.

t_{n-1} = denotes the bit that will be sensed by SEs of first stage i.e. S#1

t_{n-2} = denotes the bit that will be sensed by SEs of second stage i.e. S#2.

……

t_0 = denotes the bit that will be sensed by the last stage SEs.

t_{dm} = denotes the demultiplexer control bit.

Mathematical Function for Routing in M_FDOT

$t_i = d_i$ for all ($0 \le i \le n/2$) where $n = \log_2 N$ and N is the size of the network

$ti = \{(s_{n-1} \oplus d_{n-1}) + (s_{n-2} \oplus d_{n-2}) + \ldots\ldots\ldots\ldots + (s_{n-i} \oplus d_{n-i})\}$ for all $\{(n/2+1) \le i \le (n-1)\}$

$t_m = s_{n-1}$

$t_{dm} = d_{n-1}$

4.1.3 Fault Tolerance and Routing

Lemma 1 : If the faults occuring are such that they effect any number of SEs in the normal subnetwork of M_FDOT, then there exists atleast one path from every source to every destination through the fault-tolerant subnetwork of the M_FDOT.

Suppose the packet has to go from source S0 to destination D7. The routing tag gets evaluated to 011110. Under fault-free conditions, the path becomes

$S_0 \rightarrow$ SE2,1 $\rightarrow$ SE3,2 $\rightarrow$ SE4,4 $\rightarrow D_7$

Suppose the SEs SE2,1; SE2,3 and SE3,2 become faulty. When SE1,1 detects that SE2,1 is faulty, it steers the packet towards SE1,5 via auxiliary link. SE1,5 also detects SE2,3 faulty. The packet is then steered towards FT1,1. Finally, the route taken by the packet becomes

$S_0 \rightarrow$ SE1,1 $\rightarrow$ SE1,5 $\rightarrow$ FT1,1 $\rightarrow$ FT2,1 $\rightarrow$ FT3,2 $\rightarrow$ FT4,4 $\rightarrow D_7$

Lemma 2 : The designed MIN can sustain two faulty SEs in any single loop in the intermediate stages. However, in case of first stage, the designed MIN can tolerate the faults in those two SEs in a loop which are connected to different sources. Multiple occurences of this type of fault, pertaining to the same stage, are tolerable.

Let the packet generated by source S_0 be destined for D_2 and suppose that SE2,1 and SE2,3 become faulty simultaneously. In the absence of fault, the path would have been (as per the routing tag which is 010100)

$S_0 \rightarrow$ SE1,1 $\rightarrow$ SE2,1 $\rightarrow$ SE3,1 $\rightarrow$ SE4,2 $\rightarrow D_2$.

When SE1,1 detects the fault, it steers the packets to its auxiliary output port. The packet reaches SE1,5. SE15 has also detected fault in the SE of the following stage to which it is connected i.e SE2,3. As such, it also steers the packet on its auxiliary output port. The packet reaches FT1,1. It then follows the route

$S_0 \rightarrow$ SE1,1 $\rightarrow$ SE1,5 $\rightarrow$ FT1,1 $\rightarrow$ FT2,1 $\rightarrow$ FT3,1 $\rightarrow$ FT4,2 $\rightarrow D_2$

Lemma 3 : If the faults occuring in M_FDOT are such that they effect two conjugate SEs (out of three) in the final/last stage (stage closest to outputs), then there exists atleast one path from every source to every destination of the network.

Conjugate SEs, as defined earlier, are the ones that lead to the same set of destinations. Suppose the packet has to get routed from source S_0 has to be routed to destination D_7. The routing tag gets evaluated to 011110. Let the SEs SE4,4 and SE4,8 become faulty. In the absence of any fault, the path would have been

$$S_0 \rightarrow SE1,1 \rightarrow SE2,1 \rightarrow SE3,2 \rightarrow SE4,4 \rightarrow D_7$$

When SE4,4 is detected faulty by the preceeding SE SE3,2, it steers the packet towards SE3,4. SE3,4 allows detects the following SE SE4,8 faulty. As such, the packet gets steered towards FT3,2 via auxiliary link. Finally, the path adopted by the packet becomes

$$S_0 \rightarrow SE1,1 \rightarrow SE2,1 \rightarrow SE3,2 \rightarrow SE3,4 \rightarrow FT3,2 \rightarrow FT4,4 \rightarrow D_7$$

4.2 Analysis of M_FDOT

In this section, first of all, the proposed M_FDOT has been analyzed for the probability of packet availability at the output and auxiliary port of each SE under fault-free as well as faulty scenarios. Then probability analysis has been used subsequently for the evaluation of probability of acceptance and bandwidth, again for faulty-free and faulty scenarios. This probability analysis also leads to the evaluation of average queue length in each SE and hence the optimal buffer requirement to avoid packet discarding. Thereafter, terminal reliability has been evaluated for favorite as well as for non-favorite destinations and followed by cost evaluation.

The assumptions being considered in the analysis are exactly the same that have been discussed in section 3.3 of Chapter 3. The notations being used and analysis for performing *probability of acceptance* and *bandwidth* evaluation are identical to that discussed in section 3.3.

4.2.1 Probability of Packet Availability at ports

As per the SE loop sequences, the equations for evaluating $p_{aux,SE\#}$ [55] for various SEs of first stage of M_FDOT are given in Table 2.2(a). Equations 3.1 to 3.10 in previous Chapter 3 can be used to evaluate $p_{gen\_SE\#}$, $p_{prop\_SE\#}$ and $p_{out\_SE\#.}$ For second stage, the equations have been tabulated in A2.2(b). The equations for calculating the probability at the input ports of second stage are given in Table A2.2(c). The equations for the probability of a packet being generated at output ports of various SEs of second stage are given in Table A2.2(d). The equations for calculating the probability at the auxiliary ports and the input ports of third stage are in Tables A2.2(e) and A2.2(f) respectively. The equations for evaluating packet probability at the outputs of the third stage are given in Table A2.2(g). The equations for calculating the probability at the input ports of fourth stage have been presented in Table 2.2(h). The outputs of the final (fourth) stage [76] are in Table A2.2(i). The Tables A2.2(a) to A2.2(i) are in Annexure 2. On the basis of the equations tabulated in A2.2(a) – A2.2(i), the probability values for packet availability at ports of SEs have been presented in the following Tables 4.1(a) to 4.1(c), 4.2(a) to 4.2(c), 4.3(a) to 4.3(c) and 4.4(a) to 4.4(c) for fault-free and different faulty scenarios corresponding to different packet generation rates.

Table 4.1(a)

Prob. of packet availability at O/Ports of SEs corresponding to packet generation rate of 0.5 (M_FDOT)

First Stage			Second Stage			Third Stage			Fourth Stage	
SE#	P_{out}	$P_{aux\ in}$	SE#	P_{out}	$P_{aux\ in}$	SE#	P_{out}	$P_{aux\ in}$	SE#	P_{out}
SE1,1	0.4375	0.0000	SE2,1	0.3936	0.0129	SE3,1	0.3630	0.0252	SE4,1	0.3605
SE1,2	0.4375	0.0000							SE4,2	0.3605
SE1,3	0.4375	0.0000	SE2,2	0.3936	0.0129	SE3,2	0.3630	0.0252	SE4,3	0.3605
SE1,4	0.4375	0.0000							SE4,4	0.3605
SE1,5	0.4727	0.1250	SE2,3	0.4451	0.0970	SE3,3	0.4201	0.0811	SE4,5	0.3967
SE1,6	0.4727	0.1250							SE4,6	0.3967
SE1,7	0.4727	0.1250	SE2,4	0.4451	0.0970	SE3,4	0.4201	0.0811	SE4,7	0.3967
SE1,8	0.4727	0.1250							SE4,8	0.3967
FT1,1	0.0859	0.1719	FT2,1	0.1511	0.1462	FT3,1	0.1991	0.1258	FT4,1	0.1383
FT1,2	0.0859	0.1719							FT4,2	0.1383
FT1,3	0.0859	0.1719	FT2,2	0.1511	0.1462	FT3,2	0.1991	0.1258	FT4,3	0.1383
FT1,4	0.0859	0.1719							FT4,4	0.1383

Table 4.1(b)

Prob. of packet availability at O/Ports of SEs corresponding to packet generation rate of 0.8 (M_FDOT)

First Stage			Second Stage			Third Stage			Fourth Stage	
SE#	P_{out}	$P_{aux\ in}$	SE#	P_{out}	$P_{aux\ in}$	SE#	P_{out}	$P_{aux\ in}$	SE#	P_{out}
SE1,1	0.6400	0.0000	SE2,1	0.5588	0.0788	SE3,1	0.5096	0.1188	SE4,1	0.4932
SE1,2	0.6400	0.0000							SE4,2	0.4932
SE1,3	0.6400	0.0000	SE2,2	0.5588	0.0788	SE3,2	0.5096	0.1188	SE4,3	0.4932
SE1,4	0.6400	0.0000							SE4,4	0.4932
SE1,5	0.6976	0.3200	SE2,3	0.6219	0.2170	SE3,3	0.5679	0.1795	SE4,5	0.5337
SE1,6	0.6976	0.3200							SE4,6	0.5337
SE1,7	0.6976	0.3200	SE2,4	0.6219	0.2170	SE3,4	0.5679	0.1795	SE4,7	0.5337
SE1,8	0.6976	0.3200							SE4,8	0.5337
FT1,1	0.2368	0.4376	FT2,1	0.3535	0.3364	FT3,1	0.4102	0.2596	FT4,1	0.2992
FT1,2	0.2368	0.4376							FT4,2	0.2992
FT1,3	0.2368	0.4376	FT2,2	0.3535	0.3364	FT3,2	0.4102	0.2596	FT4,3	0.2992
FT1,4	0.2368	0.4376							FT4,4	0.2992

Table 4.1(c)

Prob. of packet availability at O/Ports of SEs corresponding to packet generation rate of 1.0 (M_FDOT)

First Stage			Second Stage			Third Stage			Fourth Stage	
SE#	P_{out}	$P_{aux\ in}$	SE#	P_{out}	$P_{aux\ in}$	SE#	P_{out}	$P_{aux\ in}$	SE#	P_{out}
SE1,1	0.7500	0.0000	SE2,1	0.6428	0.1709	SE3,1	0.5887	0.2136	SE4,1	0.5590
SE1,2	0.7500	0.0000							SE4,2	0.5590
SE1,3	0.7500	0.0000	SE2,2	0.6428	0.1709	SE3,2	0.5887	0.2136	SE4,3	0.5590
SE1,4	0.7500	0.0000							SE4,4	0.5590
SE1,5	0.8125	0.5000	SE2,3	0.7028	0.3142	SE3,3	0.6340	0.2597	SE4,5	0.5945
SE1,6	0.8125	0.5000							SE4,6	0.5945
SE1,7	0.8125	0.5000	SE2,4	0.7028	0.3142	SE3,4	0.6340	0.2597	SE4,7	0.5945
SE1,8	0.8125	0.5000							SE4,8	0.5945
FT1,1	0.3750	0.7500	FT2,1	0.4936	0.4658	FT3,1	0.5294	0.5294	FT4,1	0.4026
FT1,2	0.3750	0.7500							FT4,2	0.4026
FT1,3	0.3750	0.7500	FT2,2	0.4936	0.4658	FT3,2	0.5294	0.5294	FT4,3	0.4026
FT1,4	0.3750	0.7500							FT4,4	0.4026

As per second column of first stage in Tables 4.1(a)-4.1(c), the probability (i.e. 0.4727) of a packet being present at the output port of each SE in the lower sub-network#1 is higher than that (i.e. 0.4375) in the upper sub-network#0. This is because the auxiliary links of SEs in the upper sub-network#0 are connected to the auxiliary links of the SEs in the lower sub-network#1. Any conflict (for output port) between packets in the SEs of upper sub-network#0 leads to the steering of packets towards auxiliary links resulting in increase in

traffic in the lower sub-network#1. Hence, the probability of a packet at the output ports of SEs of lower subnetwork#1 is higher.

Again, from the second column of first stage, the probability of the availability of a packet at the output ports of each SE (belonging to fault-tolerant sub-network) is least. Since the first stage SEs of normal subnetwork are fault-free, as such all the sources steer their packets towards primary path and hence first stage SEs of fault-tolerant subnetwork do not receive any packet from any source. These SEs receive only those packets that meet conflicts for output ports in the lower subnetwork and this lower probability value corresponds to these packets only.

From the third column of Tables 4.1(a) to 4.1(c), the probability values for packet availability at auxiliary ports of upper subnetwork SEs are all zero but are non-zero for SEs of lower subnetwork. Since fault-tolerant SEs of first stage do not receive any packets from any source directly and since there is only one auxiliary input port, any packet received at auxiliary port gets the required output port without any conflict and none of the packet is routed towards the auxiliary link of upper subnetwork. But since the auxiliary output ports of SEs of upper subnetwork are linked to the auxiliary ports of SEs of lower subnetwork, hence the probability values at the auxiliary input ports of lower subnetwork are non-zero.

As the packet generation rates considered 0.8 and 1.0 in Table 4.1(b) and 4.1(c) are higher than that considered in the Table 4.1(a), the probability of a packet being present at each of the output ports in every stage in Table 4.1(c) is higher than that in Table 4.1(b) which in turn is higher than that in the Table 4.1(a).

The probability of packet availability corresponding to different packet generation rates for single SE fault in first stage in the upper subnetwork have been presented in Tables 4.2(a) to 4.2(c).

Table 4.2(a)

Prob. of packet availability at O/Ports of SEs corresponding to packet generation rate of 0.5 when single SE faulty in first stage in upper subnetwork (M_FDOT)

First Stage			Second Stage			Third Stage			Fourth Stage	
SE#	P_{out}	$P_{aux\ in}$	SE#	P_{out}	$P_{aux\ in}$	SE#	P_{out}	$P_{aux\ in}$	SE#	P_{out}
SE1,1	0.0000	0.1719	SE2,1	0.2438	0.0642	SE3,1	0.3108	0.0455	SE4,1	0.1554
SE1,2	0.4375	0.0000							SE4,2	0.3401
SE1,3	0.4375	0.0000	SE2,2	0.3936	0.0129	SE3,2	0.3108	0.0455	SE4,3	0.3401
SE1,4	0.4375	0.0000							SE4,4	0.3401
SE1,5	0.4435	0.0215	SE2,3	0.4151	0.0315	SE3,3	0.4017	0.0579	SE4,5	0.3781
SE1,6	0.4727	0.1250							SE4,6	0.3897
SE1,7	0.4727	0.1250	SE2,4	0.4451	0.0970	SE3,4	0.4017	0.0579	SE4,7	0.3897
SE1,8	0.4727	0.1250							SE4,8	0.3897
FT1,1	0.4727	0.1250	FT2,1	0.3106	0.1134	FT3,1	0.2619	0.1096	FT4,1	0.3363
FT1,2	0.0859	0.1719							FT4,2	0.1683
FT1,3	0.0859	0.1719	FT2,2	0.1511	0.1462	FT3,2	0.2619	0.1096	FT4,3	0.1683
FT1,4	0.0859	0.1719							FT4,4	0.1683

Table 4.2(b)

Prob. of packet availability at O/Ports of SEs corresponding to packet generation rate of 0.8 when single SE faulty in first stage in upper subnetwork (M_FDOT)

First Stage			Second Stage			Third Stage			Fourth Stage	
SE#	P_{out}	$P_{aux\ in}$	SE#	P_{out}	$P_{aux\ in}$	SE#	P_{out}	$P_{aux\ in}$	SE#	P_{out}
SE1,1	0.0000	0.4736	SE2,1	0.3855	0.1925	SE3,1	0.4613	0.1519	SE4,1	0.2307
SE1,2	0.6400	0.0000							SE4,2	0.4769
SE1,3	0.6400	0.0000	SE2,2	0.5558	0.0788	SE3,2	0.4613	0.1519	SE4,3	0.4769
SE1,4	0.6400	0.0000							SE4,4	0.4769
SE1,5	0.6673	0.1516	SE2,3	0.5835	0.0805	SE3,3	0.5470	0.1435	SE4,5	0.5159
SE1,6	0.6976	0.3200							SE4,6	0.5269
SE1,7	0.6976	0.3200	SE2,4	0.6219	0.2170	SE3,4	0.5470	0.1435	SE4,7	0.5269
SE1,8	0.6976	0.3200							SE4,8	0.5269
FT1,1	0.6976	0.3200	FT2,1	0.4994	0.2559	FT3,1	0.4528	0.2283	FT4,1	0.4961
FT1,2	0.2368	0.4736							FT4,2	0.3180
FT1,3	0.2368	0.4736	FT2,2	0.3535	0.3364	FT3,2	0.4528	0.2283	FT4,3	0.3180
FT1,4	0.2368	0.4736							FT4,4	0.3180

Table 4.2(c)

Prob. of packet availability at O/Ports of SEs corresponding to packet generation rate of 1.0 when single SE faulty in first stage in upper subnetwork (M_FDOT)

First Stage			Second Stage			Third Stage			Fourth Stage	
SE#	P_{out}	$P_{aux\ in}$	SE#	P_{out}	$P_{aux\ in}$	SE#	P_{out}	$P_{aux\ in}$	SE#	P_{out}
SE1,1	0.0000	0.7500	SE2,1	0.4723	0.3114	SE3,1	0.5448	0.2437	SE4,1	0.2724
SE1,2	0.7500	0.0000							SE4,2	0.5452
SE1,3	0.7500	0.0000	SE2,2	0.6428	0.1709	SE3,2	0.5448	0.2437	SE4,3	0.5452
SE1,4	0.7500	0.0000							SE4,4	0.5452
SE1,5	0.7969	0.3750	SE2,3	0.6650	0.1240	SE3,3	0.6138	0.2160	SE4,5	0.5831
SE1,6	0.8125	0.5000							SE4,6	0.5885
SE1,7	0.8125	0.5000	SE2,4	0.7028	0.3142	SE3,4	0.6138	0.2160	SE4,7	0.5885
SE1,8	0.8125	0.5000							SE4,8	0.5885
FT1,1	0.8125	0.5000	FT2,1	0.6038	0.3576	FT3,1	0.5541	0.3038	FT4,1	0.5707
FT1,2	0.3750	0.7500							FT4,2	0.4126
FT1,3	0.3750	0.7500	FT2,2	0.4936	0.4658	FT3,2	0.5541	0.3038	FT4,3	0.4126
FT1,4	0.3750	0.7500							FT4,4	0.4126

In Table 4.2(a), it has been assumed that switching element SE1,1 becomes faulty and the packet generation rate is 0.5. Since SE1,1 has been assumed faulty, the probability at its output port is 0.0000. The source connected to SE1,1 have secondary paths linked to switching element FT1,1 in the fault-tolerant sub-network. As such, the probability of a packet being present at the output port of FT1,1 is higher (i.e. 0.4727) than any other first stage SEs of fault-tolerant sub-network (i.e. 0.0859). As per design (Figure 4.1), the auxiliary links of first stage SEs in the fault-tolerant sub-network are linked to the auxiliary links of upper sub-network#0. Since the packet generation rate in case of switching element FT1,1 is higher and FT1,1 is linked to SE1,1, as such the probability value at auxiliary link of SE1,1 is non-zero (i.e. 0.1719).

In Table 4.2(b), the packet generation rate has been considered 0.8, higher than that being considered in the previous Table 4.2(a). As such, the packet generation and propagation probability values for each SE is higher than that in the previous Table 4.2(a). The same reason applies for larger probability values in Tables 4.2(c) when compared with values tabulated in 4.2(a) and 4.2(b).

The probability for packet availability for different packet generation rates corresponding to single SE faulty in first stage in the lower subnetwork have been evaluated and are given in Tables 4.3(a) to 4.3(c).

Table 4.3(a)
Prob. of packet availability at O/Ports of SEs corresponding to packet generation rate of 0.5 when single SE faulty in first stage in lower subnetwork (M_FDOT)

First Stage			Second Stage			Third Stage			Fourth Stage	
SE#	P_{out}	$P_{aux\ in}$	SE#	P_{out}	$P_{aux\ in}$	SE#	P_{out}	$P_{aux\ in}$	SE#	P_{out}
SE1,1	0.4727	0.1250	SE2,1	0.4157	0.0415	SE3,1	0.3749	0.0350	SE4,1	0.3795
SE1,2	0.4375	0.0000							SE4,2	0.3652
SE1,3	0.4375	0.0000	SE2,2	0.3936	0.0129	SE3,2	0.3749	0.0350	SE4,3	0.3652
SE1,4	0.4375	0.0000							SE4,4	0.3652
SE1,5	0.0000	0.1719	SE2,3	0.2806	0.1159	SE3,3	0.3614	0.0892	SE4,5	0.1807
SE1,6	0.4727	0.1250							SE4,6	0.3743
SE1,7	0.4727	0.1250	SE2,4	0.4451	0.0970	SE3,4	0.3614	0.0892	SE4,7	0.3743
SE1,8	0.4727	0.1250							SE4,8	0.3743
FT1,1	0.4435	0.0215	FT2,1	0.2736	0.0495	FT3,1	0.2380	0.0901	FT4,1	0.3144
FT1,2	0.0859	0.1719							FT4,2	0.1568
FT1,3	0.0859	0.1719	FT2,2	0.1511	0.1462	FT3,2	0.2380	0.0901	FT4,3	0.1568
FT1,4	0.0859	0.1719							FT4,4	0.1568

Table 4.3 (b)
Prob. of packet availability at O/Ports of SEs corresponding to packet generation rate of 0.8 when single SE faulty in first stage in lower subnetwork (M_FDOT)

First Stage			Second Stage			Third Stage			Fourth Stage	
SE#	P_{out}	$P_{aux\ in}$	SE#	P_{out}	$P_{aux\ in}$	SE#	P_{out}	$P_{aux\ in}$	SE#	P_{out}
SE1,1	0.6976	0.3200	SE2,1	0.5845	0.1235	SE3,1	0.5210	0.1255	SE4,1	0.5184
SE1,2	0.6400	0.0000							SE4,2	0.4971
SE1,3	0.6400	0.0000	SE2,2	0.5558	0.0788	SE3,2	0.5210	0.1255	SE4,3	0.4971
SE1,4	0.6400	0.0000							SE4,4	0.4971
SE1,5	0.0000	0.4736	SE2,3	0.4364	0.2691	SE3,3	0.5140	0.1954	SE4,5	0.2570
SE1,6	0.6976	0.3200							SE4,6	0.5161
SE1,7	0.6976	0.3200	SE2,4	0.6219	0.2170	SE3,4	0.5140	0.1954	SE4,7	0.5161
SE1,8	0.6976	0.3200							SE4,8	0.5161
FT1,1	0.6673	0.1516	FT2,1	0.4493	0.1252	FT3,1	0.4266	0.2033	FT4,1	0.4758
FT1,2	0.2368	0.4736							FT4,2	0.3064
FT1,3	0.2368	0.4736	FT2,2	0.3535	0.3364	FT3,2	0.4266	0.2033	FT4,3	0.3064
FT1,4	0.2368	0.4736							FT4,4	0.3064

Table 4.3(c)
Prob. of packet availability at O/Ports of SEs corresponding to packet generation rate of 1.0 when single SE faulty in first stage in lower subnetwork (M_FDOT)

First Stage			Second Stage			Third Stage			Fourth Stage	
SE#	P_{out}	$P_{aux\ in}$	SE#	P_{out}	$P_{aux\ in}$	SE#	P_{out}	$P_{aux\ in}$	SE#	P_{out}
SE1,1	0.8125	0.5000	SE2,1	0.6671	0.2058	SE3,1	0.5952	0.2100	SE4,1	0.5830
SE1,2	0.7500	0.0000							SE4,2	0.5610
SE1,3	0.7500	0.0000	SE2,2	0.6428	0.1709	SE3,2	0.5952	0.2100	SE4,3	0.5610
SE1,4	0.7500	0.0000							SE4,4	0.5610
SE1,5	0.0000	0.7500	SE2,3	0.5211	0.3869	SE3,3	0.5864	0.2751	SE4,5	0.2932
SE1,6	0.8125	0.5000							SE4,6	0.5803
SE1,7	0.8125	0.5000	SE2,4	0.7028	0.3142	SE3,4	0.5864	0.2751	SE4,7	0.5803
SE1,8	0.8125	0.5000							SE4,8	0.5803
FT1,1	0.7969	0.3750	FT2,1	0.5555	0.1813	FT3,1	0.5317	0.2783	FT4,1	0.5584
FT1,2	0.3750	0.7500							FT4,2	0.4035
FT1,3	0.3750	0.7500	FT2,2	0.4936	0.4658	FT3,2	0.5317	0.2783	FT4,3	0.4035
FT1,4	0.3750	0.7500							FT4,4	0.4035

The probability values in Tables 4.3(a) to 4.3(c) have been calculated considering SE1,5 faulty. As such, the sources connected to SE15 (i.e. S_8 and S_9) route their packets towards secondary path leading to the switching element FT1,1 of fault-tolerant subnetwork. That is why the probability value at the output port of FT1,1 is higher than other SEs in the fault-tolerant subnetwork (i.e. FT1,2; FT1,3; FT1,4).

In the following Tables 4.4(a) to 4.4(c) have been presented the probability values for availability of packets at the output and auxiliary input ports of SEs for different packet generation rates assuming four SEs faulty in the first stage in the upper subnetwork. The four SEs being considered faulty are SE1,1 ; SE1,2; SE1,3 and SE1,4 i.e one SE in each loop.

Table 4.4(a)
Prob. of packet availability at O/Ports of SEs corresponding to packet generation rate of 0.5 when four SEs faulty in first stage in upper subnetwork (M_FDOT)

First Stage			Second Stage			Third Stage			Fourth Stage	
SE#	P_{out}	P_{aux_in}	SE#	P_{out}	P_{aux_in}	SE#	P_{out}	P_{aux_in}	SE#	P_{out}
SE1,1	0.0000	0.1719	SE2,1	0.0736	0.1472	SE3,1	0.1308	0.1262	SE4,1	0.0654
SE1,2	0.0000	0.1719							SE4,2	0.0654
SE1,3	0.0000	0.1719	SE2,2	0.0736	0.1472	SE3,2	0.1308	0.1262	SE4,3	0.0654
SE1,4	0.0000	0.1719							SE4,4	0.0654
SE1,5	0.4435	0.0215	SE2,3	0.3944	0.0000	SE3,3	0.3586	0.0097	SE4,5	0.3613
SE1,6	0.4435	0.0215							SE4,6	0.3613
SE1,7	0.4435	0.0215	SE2,4	0.3944	0.0000	SE3,4	0.3586	0.0097	SE4,7	0.3613
SE1,8	0.4435	0.0215							SE4,8	0.3613
FT1,1	0.4727	0.1250	FT2,1	0.4455	0.0984	FT3,1	0.4196	0.0786	FT4,1	0.3966
FT1,2	0.4727	0.1250							FT4,2	0.3966
FT1,3	0.4727	0.1250	FT2,2	0.4455	0.0984	FT3,2	0.4196	0.0786	FT4,3	0.3966
FT1,4	0.4727	0.1250							FT4,4	0.3966

Table 4.4(b)
Prob. of packet availability at O/Ports of SEs corresponding to packet generation rate of 0.5 when four SEs faulty in first stage in upper subnetwork (M_FDOT)

First Stage			Second Stage			Third Stage			Fourth Stage	
SE#	P_{out}	P_{aux_in}	SE#	P_{out}	P_{aux_in}	SE#	P_{out}	P_{aux_in}	SE#	P_{out}
SE1,1	0.0000	0.4736	SE2,1	0.1722	0.3445	SE3,1	0.2736	0.2605	SE4,1	0.1368
SE1,2	0.0000	0.4736							SE4,2	0.1368
SE1,3	0.0000	0.4736	SE2,2	0.1722	0.3445	SE3,2	0.2736	0.2605	SE4,3	0.1368
SE1,4	0.0000	0.4736							SE4,4	0.1368
SE1,5	0.6673	0.1516	SE2,3	0.5560	0.0000	SE3,3	0.4905	0.0454	SE4,5	0.4971
SE1,6	0.6673	0.1516							SE4,6	0.4971
SE1,7	0.6673	0.1516	SE2,4	0.5560	0.0000	SE3,4	0.4905	0.0454	SE4,7	0.4971
SE1,8	0.6673	0.1516							SE4,8	0.4971
FT1,1	0.6976	0.3200	FT2,1	0.6231	0.2226	FT3,1	0.5641	0.1605	FT4,1	0.5325
FT1,2	0.6976	0.3200							FT4,2	0.5325
FT1,3	0.6976	0.3200	FT2,2	0.6231	0.2226	FT3,2	0.5641	0.1605	FT4,3	0.5325
FT1,4	0.6976	0.3200							FT4,4	0.5325

Table 4.4(c)
Prob. of packet availability at O/Ports of SEs corresponding to packet generation rate of 1.0 when four SEs faulty in first stage in upper subnetwork (M_FDOT)

First Stage			Second Stage			Third Stage			Fourth Stage	
SE#	P_{out}	P_{aux_in}	SE#	P_{out}	P_{aux_in}	SE#	P_{out}	P_{aux_in}	SE#	P_{out}
SE1,1	0.0000	0.7500	SE2,1	0.2416	0.4832	SE3,1	0.3585	0.3403	SE4,1	0.1793
SE1,2	0.0000	0.7500							SE4,2	0.1793
SE1,3	0.0000	0.7500	SE2,2	0.2416	0.4832	SE3,2	0.3585	0.3403	SE4,3	0.1793
SE1,4	0.0000	0.7500							SE4,4	0.1793
SE1,5	0.7969	0.3750	SE2,3	0.6381	0.0000	SE3,3	0.5553	0.0817	SE4,5	0.5655
SE1,6	0.7969	0.3750							SE4,6	0.5655
SE1,7	0.7969	0.3750	SE2,4	0.6381	0.0000	SE3,4	0.5553	0.0817	SE4,7	0.5655
SE1,8	0.7969	0.3750							SE4,8	0.5655
FT1,1	0.8125	0.5000	FT2,1	0.7034	0.3175	FT3,1	0.6252	0.2163	FT4,1	0.5918
FT1,2	0.8125	0.5000							FT4,2	0.5918
FT1,3	0.8125	0.5000	FT2,2	0.7034	0.3175	FT3,2	0.6252	0.2163	FT4,3	0.5918
FT1,4	0.8125	0.5000							FT4,4	0.5918

Since four SEs have been assumed faulty, the sources connected to the faulty SEs route their packets towards secondary paths leading to the fault-tolerant sub-network. In spite of faulty SEs in the upper sub-network#0, there exists probability of a packet being present at the output port of each SE in the last stage of the upper sub-network#0. This is due to the conflict between packets in the fault-tolerant sub-network and hence packets getting routed towards auxiliary links leading to their arrival in the upper sub-network#0.

4.2.2 Probability of Acceptance and Bandwidth

Probability of acceptance, as defined in chapter 1, is the ratio of the average number of requests accepted by the destination to the average number of requests submitted by the sources per network cycle and bandwidth is defined as the average number of requests accepted per network cycle.

The probability of acceptance and bandwidth values for M_FDOT Network corresponding to different packet generation rates under fault-free and faulty scenarios have been presented in the tables below :

Table 4.5(a)

Probability of acceptance and Bandwidth values under fault-free conditions (M_FDOT)

Packet generation rate	Bandwidth	Probability of acceptance	Packet generation rate	Bandwidth	Probability of acceptance
0.1	1.5620	0.9762	0.6	8.3973	0.8747
0.2	3.0551	0.9547	0.7	9.5482	0.8525
0.3	4.4866	0.9347	0.8	10.6094	0.8289
0.4	5.8579	0.9153	0.9	11.5764	0.8039
0.5	7.1642	0.8955	1.0	12.4480	0.7780

Table 4.5(b)

Prob. of acceptance and Bandwidth values for single SE faulty in first stage in upper subnetwork

Packet generation rate	Bandwidth	Probability of acceptance	Packet generation rate	Bandwidth	Probability of acceptance
0.1	1.5665	0.9790	0.6	8.3177	0.8664
0.2	3.0659	0.9581	0.7	9.4147	0.8406
0.3	4.4962	0.9367	0.8	10.4162	0.8138
0.4	5.8525	0.9145	0.9	11.3210	0.7862
0.5	7.1285	0.8911	1.0	12.1303	0.7581

Table 4.5(c)

Prob. of acceptance and Bandwidth values for single SE faulty in first stage in lower subnetwork

Packet generation rate	Bandwidth	Probability of acceptance	Packet generation rate	Bandwidth	Probability of acceptance
0.1	1.5664	0.9790	0.6	8.3179	0.8664
0.2	3.0654	0.9579	0.7	9.4170	0.8408
0.3	4.4949	0.9364	0.8	10.4207	0.8141
0.4	5.8509	0.9142	0.9	11.3275	0.7866
0.5	7.1273	0.8909	1.0	12.1381	0.7586

Table 4.5(d)

Prob. of acceptance and Bandwidth values when all SEs faulty in first stage in lower subnetwork

Packet generation rate	Bandwidth	Probability of acceptance	Packet generation rate	Bandwidth	Probability of acceptance
0.1	1.5402	0.9626	0.6	7.5950	0.7991
0.2	2.9633	0.9260	0.7	8.5095	0.7598
0.3	4.2747	0.8906	0.8	9.3306	0.7290
0.4	5.4805	0.8563	0.9	10.0584	0.6985
0.5	6.5860	0.8233	1.0	10.6925	0.6683

From these Tables, it has been observed that the probability of acceptance and bandwidth values have only a slight degradation in their values under faulty scenarios. This shows the efficiency of M_FDOT under faulty scenarios.

4.2.3 Average Queue Length and Optimal Buffer Requirement

The following Tables 4.6(a) to 4.6(b) give the average queue length of packets and optimal buffer requirement at the output ports and auxiliary input port of each SE at every stage corresponding to request generation rate of 1.0 for fault free and one of the worst faulty scenario i.e. when four SEs are faulty in first stage in upper subnetwork. The SEs that have been considered faulty are SE1,1; SE1,2 SE1,3 and SE1,4. The formula being used for evaluation of average queue length is that of M/M/1 queuing model i.e. average queue length = $\frac{\lambda}{\mu}\frac{\lambda}{(\mu-\lambda)}$ where λ is the mean arrival rate and μ is the mean service rate. M/M/1 model has been used as an approximation. For each SE, $\lambda = P_{out}$ and P_{out} is the probability of a packet being present at the output port of SEs in the previous stage and $\mu = 1$. The packet generation rate has been taken 1.0 that corresponds to maximum traffic and hence the above Table gives the buffer requirements of SE ports under maximum traffic scenario. Since there are no auxiliary links in the fourth stage, therefore hyphen has been shown in Table 4.6(a) corresponding to the SEs of the final stage.

The above Table 4.6(b) provides the optimal buffer requirement for maximum value of packet generation rate considering that four SEs have become faulty in the first stage. Because of faulty SEs, their packets get directed to fault-tolerant subnetwork and that is why the buffer requirement value is higher i.e. 4 as compared to that in Table 4.6(a) i.e one. The next section discusses the terminal reliability of the M_FDOT for favorite as well as for non-favorite destinations.

Table 4.6(b)
Optimal Buffer Requirement for four SEs faulty in first stage in upper subnetwork

SE#	Average Queue Len at each of the regular O/P	Min. No. of buffers at each of the regular O/P	Average Queue Len at the auxiliary I/port	Min. No. of buffers req. at the auxiliary I/ port	SE#	Average Queue Len at each of the regular O/P	Min. No. of buffers at each of the regular O/P	Average Queue Len at the auxiliary Input port	Minimum Number of buffers required at the auxiliary Input port
SE1,1	-	-	2.25	3	SE4,1	0.0392	1	-	-
SE1,2	-	-	2.25	3	SE4,2	0.0392	1	-	-
SE1,3	-	-	2.25	3	SE4,3	0.0392	1	-	-
SE1,4	-	-	2.25	3	SE4,4	0.0392	1	-	-
SE1,5	3.1270	4	0.2250	1	SE4,5	0.7360	1	-	-
SE1,6	3.1270	4	0.2250	1	SE4,6	0.7360	1	-	-
SE1,7	3.1270	4	0.2250	1	SE4,7	0.7360	1	-	-
SE1,8	3.1270	4	0.2250	1	SE4,8	0.7360	1	-	-
FT1,1	3.5217	4	0.5	1	FT4,1	0.8582	1	-	-
FT1,2	3.5217	4	0.5	1	FT4,2	0.8582	1	-	-
FT1,3	3.5217	4	0.5	1	FT4,3	0.8582	1	-	-
FT1,4	3.5217	4	0.5	1	FT4,4	0.8582	1	-	-
SE2,1	0.077	1	0.4518	1	SE3,1	0.2003	1	0.1755	1
SE2,2	0.077	1	0.4518	1	SE3,2	0.2003	1	0.1755	1
SE2,3	1.1252	2	0.0	1	SE3,3	0.6935	1	0.0065	1
SE2,4	1.1252	2	0.0	1	SE3,4	0.6935	1	0.0065	1
FT2,1	1.6682	2			FT3,1	1.0427	2	0.0597	1
FT2,2	1.6682	2			FT3,2	1.0427	2	0.0597	1

4.2.4 Terminal Reliability

The redundancy graph for evaluating the terminal reliability of M_FDOT is shown in Figures 4.2(a) and 4.2(b)

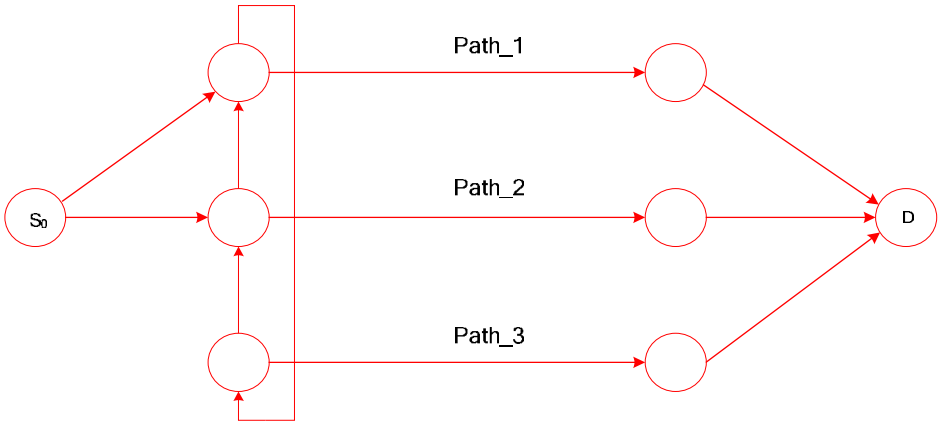

Figure 4.2(a) : Redundancy Graph of M_FDOT for favorite Destinations

The Source S_0 remains connected to the destination D if, atleast, one of the three paths survives. Let r be reliability of each SE. The probability that

Path_1 fails = $1- r^2$

Path_2 fails = $1- r^2$

Path_3 fails = $1- r^2$

All the three paths fail = $(1- r^2)^3$

Probability that at least one path survives

i.e $R_{term} = 1 – [(1- r^2)]^3$

The evaluated terminal reliabilities (for favorite destinations) for various values of SE reliabilities are presented in Table 4.7(a)

Table 4.7(a)

SE Reliability	Terminal Reliability
0.90	0.993
0.92	0.996
0.94	0.998
0.96	0.9995

The redundancy graph for evaluating terminal reliability of M_FDOT for non-favorite destinations is shown below

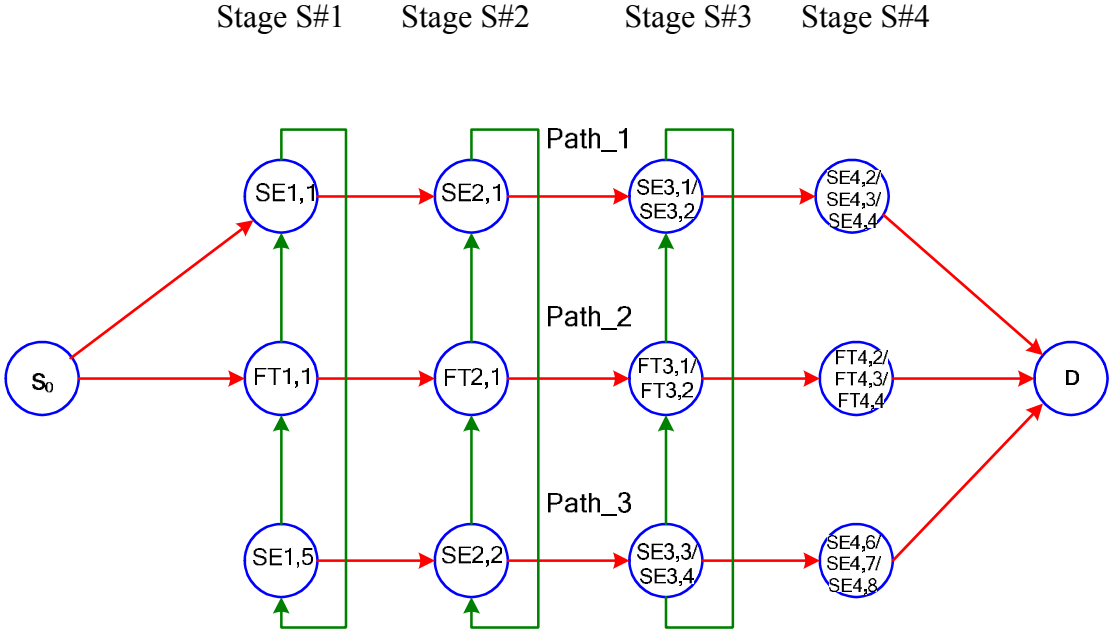

Figure 4.2(b) : Redundancy Graph of M_FDOT for non-favorite Destinations

For stage S#1, the probability that atleast one out of three – SE1,1; FT1,1 and SE1,5 survives is

$R_{S\#1} = \left[1 - (1\text{-}r)^3\right]$

In stage S#2, the probability that atleast one of the three – SE2,1; FT2,2 and SE2,3 survives is

$R_{S\#2} = \left[1 - (1\text{-}r)^3\right]$

In stage S#3, the probability that atleast one of the three – SE3,1; SE3,3 and FT3,1 comprising of loop survives is

$R_{S\#3} = \left[1 - (1\text{-}r)^3\right]$

Terminal Reliability = $R_{S\#1} \times R_{S\#2} \times R_{S\#3} \times r$

The terminal reliabilities for non-favorite destinations for various values of SE reliabilities have been evaluated and presented in Table 4.7(b)

Table 4.7(b)
Terminal Reliability of M_FDOT for non-favorite Destinations

SE Reliability	Terminal Reliability
0.90	0.8973
0.92	0.9186
0.94	0.9394
0.96	0.9598

The terminal reliability values when compared with the corresponding SE reliability values reveal that these values are almost equal and hence comparable and hence this justifies the design of F_DOT.

4.2.5 Hardware Complexity and Cost

To estimate the cost of a network, one common method is to calculate the switch complexity with an assumption that the cost of a switch is proportional to the number of gates involved. For example, a 2×2 SE has 4 units of cost and a 3×3 SE has 9 units of cost. For multiplexers and de-multiplexers, we roughly assume that each of k×1 and 1× k has k units of cost.

Number of stages = n where $n = \log_2 N$

First stage SEs = $\frac{N}{2^i} + \frac{N}{2^{i+1}}$ where i=1 ;

Second stage SEs = $\frac{N}{2^i} + \frac{N}{2^{i+1}}$ where i=2;

Total number of SEs in n stages = $2 * \left(\sum_{i=1}^{n/2} \left(\frac{N}{2^i} + \frac{N}{2^{i+1}} \right) \right)$

Since the SEs in the n^{th} stage are of size 2×2, as such the n^{th} stage SEs i.e $\left(\frac{N}{2}+\frac{N}{4}\right)$ have been subtracted from total number of SEs as their cost will be different as shown in the equation below.

Number of SEs in 1 to (n-1) stages (say Y) = $2*\left(\sum_{i=1}^{n/2}\left(\frac{N}{2^i}+\frac{N}{2^{i+1}}\right)\right)-\left(\frac{N}{2}+\frac{N}{4}\right)$

Link Complexity

Inter-stage links = $\sum_{i=1}^{n/2}\left(\frac{N}{2^i}*2+\frac{N}{2^{i+1}}*2\right)+\sum_{i=2}^{n/2}\left(\frac{N}{2^i}*2+\frac{N}{2^{i+1}}*2\right)$

The first subterm within the first pair of brackets corresponds to inter-stage links existing between first stage to stage $\left(\frac{n}{2}+1\right)$ in the normal subnetwork of M_FDOT. The second subterm within the first pair of brackets corresponds to the number of inter-stage links existing between first stage to stage $\left(\frac{n}{2}+1\right)$ in the fault-tolerant subnetwork. The first subterm within the second pair of brackets corresponds to the inter-stage links between stage $\left(\frac{n}{2}+1\right)$ to stage n in the normal subnetwork of M_FDOT. The second subterm within the second pair of brackets corresponds to the number of inter-stage links existing between stage $\left(\frac{n}{2}+1\right)$ to stage n in the fault-tolerant subnetwork of M_FDOT.

Intra-stage links = $\sum\left(\frac{N}{2^i}+\frac{N}{2^{i+1}}\right)$

$\frac{N}{2^i}$ corresponds to the number of SEs in i^{th} stage of normal subnetwork of M_FDOT and $\frac{N}{2^{i+1}}$ is the number of links in the i^{th} stage of fault-tolerant subnetwork.

Cost of SEs = $9*Y+4*\left(\frac{N}{2}+\frac{N}{4}\right)$

Total number of multiplexers and demultiplexers = 2*N

Cost of multiplexers and demultiplexers = 4*N

Total cost of M_FDOT = $9 * Y + 4 * \left(\frac{N}{2} + \frac{N}{4} \right) + 4 * N$

The cost of the various size M_FDOT has been shown in Table 4.10

Table 4.8
Cost of various sized M_FDOT

Size of MIN	Cost
16 × 16	328
64 × 64	1272
256 × 256	5520
1024×1024	27040

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4.3 Hybrid Network

The Hybrid network is a dynamic fault-tolerant MIN. It has been named Hybrid because normal sub-network is irregular in design whereas fault-tolerant sub-network is regular in topology. The techniques that have been incorporated in an integrated manner to make it fault-tolerant and efficient in performance are : Chaining and an additional fault-tolerant sub-network.

4.3.1 Design of Hybrid Network

The Hybrid MIN of size 16×16 is shown in Figure 4.3. There are in all four stages of SEs labeled as S#1, S#2, S#3 and S#4 starting from left to right. SEs of two different sizes are in use in the entire design. The first stage and intermediate stages of the Hybrid MIN use SEs of size 3×3 and final stage is comprised of SEs of size 2×2. The entire network is comprised of two sub-networks : normal subnetwork (comprising of subnetwork#0 and subnetwork#1) and fault-tolerant sub-network. These two sub-networks together constitute Hybrid MIN.

In normal sub-network, there are twenty four SEs in all i.e. eight SEs each in the first and fourth stage, four SEs each in second and third stage. In fault-tolerant subnetwork, there are sixteen SEs in all i.e. four SEs in each stage. These SEs are being termed as fault-tolerant SEs. The inter-stage connections are to be made as under :

Mark the input and output ports of each SE starting with 0 from top towards bottom in each stage. Connect the even numbered output ports of each stage (except stage n/2) with the same even numbered input ports of SEs of associated stage. The stages which are equidistant from left and right are being termed as associated stages. Connect the odd numbered output ports of two adjacent SEs with the input ports of SE in the next stage. Connect the output ports of each SE in stage (n/2+1) with the odd numbered input ports of two adjacent SEs in the next stage. The connection between stages n/2 and (n/2 + 1) are to be made as under :

Divide the SEs of stage n/2 and stage (n/2+1) into three sets, each set comprising of four SEs (two SEs belonging to stage n/2 and two SEs belonging to stage (n/2+1).

Connect the external output ports of SEs of stage n/2 with the external input ports of SEs of stage (n/2+1) of that very set without crossing. And cross connect the internal output ports of SEs of stage n/2 with the internal input ports of SEs of stage (n/2+1).

The inter-stage connections in fault-tolerant subnetwork are perfect shuffle connections as in Omega network. In general, each subnetwork of Hybrid MIN consists of $N=2^n$ inputs and N outputs where n is even. N is the size of the network. There are n stages in all. Each stage of normal sub-network comprises of $N/2^j$ SEs where j represents the stage. Each stage of fault-tolerant sub-network always comprise of N/4 SEs. The S_0, S_1, … S_{15} marked prior to first stage of SEs in subnetwork_1 denote the sources. Similarly, D_0, D_1… D_{15} denote destinations. In addition to inter-stage links, there are intra-stage connections also in all the stages except the last one. This technique of connecting SEs in the same stage is called chaining. *Chaining* leads to the formation of loops. In the Hybrid MIN, there are four loops in first, second and third stages. Each loop in the first stage comprises of three SEs and each loop in the second and third stages consists of two SEs each. Of the three SEs in each loop in first stage, two SEs belong to normal subnetwork and one belongs to fault-tolerant subnetwork. Chaining contributes towards fault-tolerance as well

as distribution of traffic either during heavy traffic conditions or during conflicts between packets for the same port. The sources and destinations are connected to the multiplexers and demultiplexers as follows:

i) If (s_{n-2}, ……s_1) bits are the same for the two sources, then these two sources are connected to the same multiplexer.

ii) If (d_{n-2},…..d_1) bits are the same for the two destinations, then these two destinations are linked to the same demultiplexer.

4.3.2 Routing Tag and Routing Algorithm

Whenever a packet gets generated at a source, a destination address field is always there where the packet has to reach. This design makes use of two routing tags. The fault-tolerant subnetwork uses destination address field as routing tag. But for the normal sub-network, routing tag is computed from destination address field at each source. The algorithm for evaluating routing tag from destination address field is described below. The routing scheme assumes that the sources and SEs have the ability to detect faults in the SEs to which they are connected. There are two links (i.e. primary and secondary) for each source. The primary link connects each source to normal subnetwork and the secondary link connects the same source to fault-tolerant sub-network to incorporate fault-tolerance. Each source attempts entry into the MIN via its primary link along with the evaluated routing tags. If the source detects that the primary link led SE has become faulty, then the source routes the packet towards the secondary link. For each SE in intermediate stages, if the output link is busy or if the successor SE in the next stage is faulty, then the packet is routed via auxiliary output port of the SE. If at any time there is a conflict for a particular port among three packets (i.e. two arriving at the regular input ports and one coming via auxiliary input port) then any one packet (on random basis) is provided output port, another packet (of the remaining two packets) is provided auxiliary output port (again on random basis) and the left over packet is buffered.

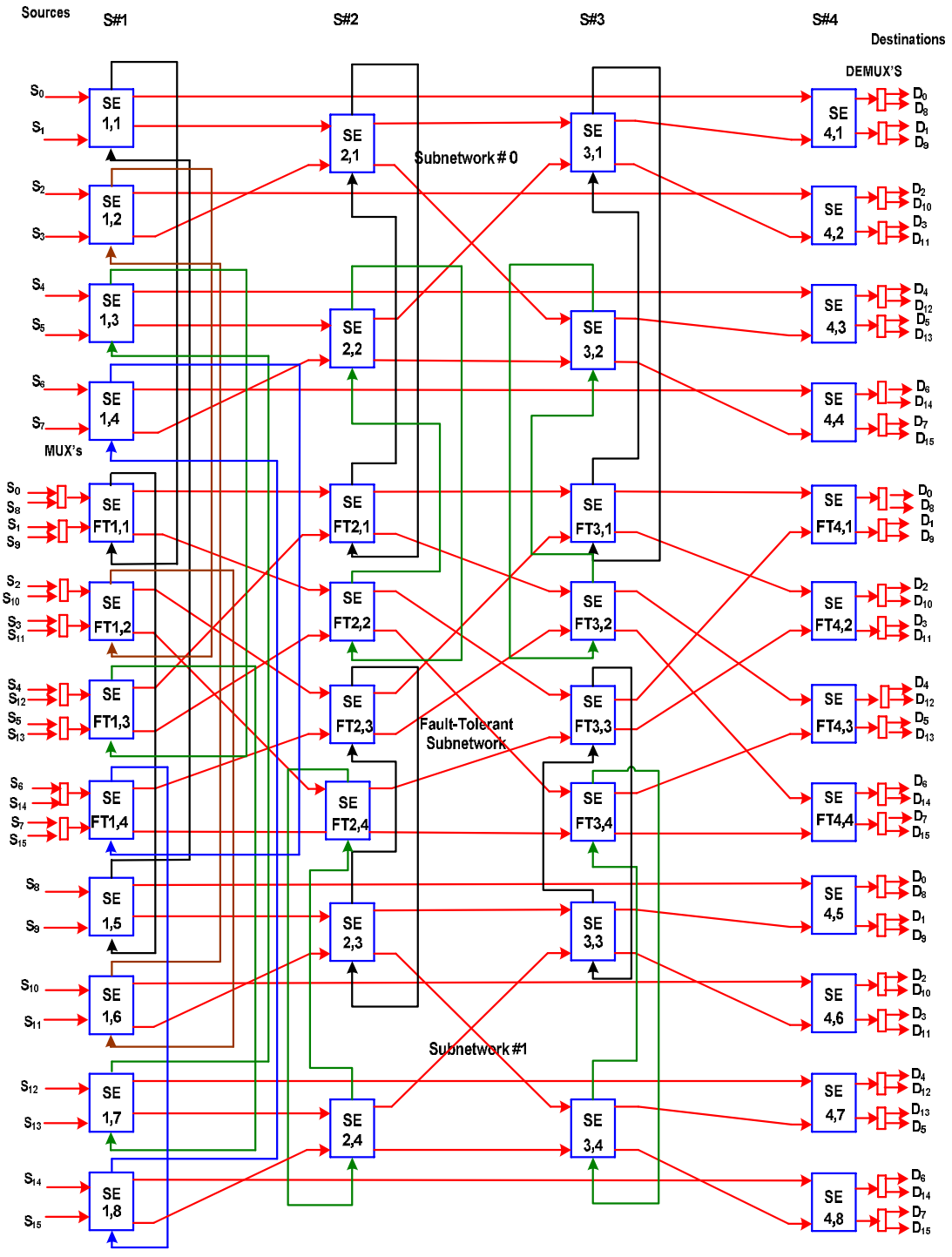

Figure 4.3 : Hybrid Network with N = 16

Routing Tag Algorithm

The algorithm for evaluating routing tag from destination address is calculated as follows.

Let $d_{n-1}d_{n-2}\ldots\ldots d_0$ denote the destination address and

$s_{n-1}s_{n-2}\ldots\ldots\ldots s_0$ be the source address

Let the routing tag be denoted as $t_m t_{n-1} t_{n-2}\ldots.t_0 t_{dm}$.

In the routing tag, the significance of the various bits are as under :

t_m = denotes the multiplexer control bit.

t_{n-1} = denotes the bit that will be sensed by SEs of first stage i.e. S#1.

t_{n-2} = denotes the bit that will be sensed by the SEs of second stage i.e. S#2.

……

t_0 = denotes the bit that will be sensed by the SEs of last stage.

t_{dm} = denotes the demultiplexer control bit.

Mathematical Function for Routing in Hybrid

$t_i = d_i$ for all ($0 \le i \le n/2$) where $n = \log_2 N$ and N is the size of the network

$ti = \{(s_{n-1} \oplus d_{n-1}) + (s_{n-2} \oplus d_{n-2}) + \ldots\ldots\ldots\ldots + (s_{n-i} \oplus d_{n-i})\}$ for all $\{(n/2+1) \le i \le (n-1)\}$

$t_m = s_{n-1}$

$t_{dm} = d_{n-1}$

4.3.3 Fault-Tolerance and Routing

The proposed Hybrid Network possesses the following properties

Lemma 1 : The designed MIN can sustain single faulty SE in any loop.

Let the packet has to get routed from source S_0 to destination D_3. In the absence of any fault, the route followed by the packet is

$S_0 \rightarrow SE1,1 \rightarrow SE2,1 \rightarrow SE3,1 \rightarrow SE4,2 \rightarrow D_3$.

Suppose the SE SE3,1 becomes faulty. The path adopted by the packet under this faulty scenario is

$S_0 \rightarrow SE1,1 \rightarrow SE2,1 \rightarrow FT2,1 \rightarrow FT3,1 \rightarrow FT4,2 \rightarrow D_3$

Lemma 2: If the faults occuring are such that they effect any number of SEs in the normal subnetwork of the designed Hybrid MIN, there exists atleast one path from each source to every destination through the fault-tolerant subnetwork of the designed MIN.

Let the packet has to get routed from source S_0 to destination D_7. The routing tag for normal as well as for fault-tolerant subnetwork becomes 011110. Suppose the SEs SE2,1 and SE3,1 become faulty. In the absence of any fault, the path adopted by the packet would have been

$S_0 \rightarrow SE1,1 \rightarrow SE2,1 \rightarrow SE3,2 \rightarrow SE4,4 \rightarrow D_7$

But under faulty scenarios, the path followed by the packet becomes

$S_0 \rightarrow SE1,1 \rightarrow FT2,1 \rightarrow FT3,2 \rightarrow FT4,4 \rightarrow D_7$

The primary routes from all sources to their favorite and non-favorite destinations for Hybrid MIN are summarized in Tables A2.3(a) and A2.3(b) respectively and the secondary routes in Table A2.3(c) in Annexure 2.

4.4 Analysis of Hybrid Network

In this section, first of all, the proposed Hybrid MIN has been analyzed for the probability of packet availability at the output and auxiliary port of each SE under fault-free as well as faulty scenarios. Then probability analysis has been used subsequently for the evaluation of probability of acceptance and bandwidth, again for faulty-free and faulty scenarios. This probability analysis also leads to the evaluation of average queue length in each SE and hence the optimal buffer requirement to avoid packet discarding. Thereafter, terminal reliability has been evaluated for favorite as well as for non-favorite destinations followed by cost evaluation. The assumptions being considered in the analysis are exactly the same that have been discussed in section 3.3 of Chapter 3. The notations being used for performing analysis are identical to that discussed in section 3.3.

4.4.1 Probability of Packet Availability at ports

The system of equations for evaluating probability of packet availability at auxiliary ports, input ports and output ports for various SEs in different stages of the designed MIN have been presented in Tables A2.4(a) to A2.4(i) in Annexure 2. On the basis of the equations tabulated in A2.4(a) – A2.4(i), the probability values for packet availability at ports of SEs have been presented in the following Tables 4.9(a) to 4.9(c), 4.10(a) to 4.10(c), 4.11(a) to 4.11(c) and 4.12(a) to 4.12(c) for fault-free and various fault scenarios corresponding to various packet generation rates.

The Tables 4.13(a) to 4.13(c) provide the values of probability of a packet being present at the output port and at the auxiliary port of each SE at every stage for packet generation rates of 0.5,0.8 and 1.0 under fault free and selected faulty scenarios for Hybrid Network.

Table 4.9(a)

Prob. of packet availability at O/Ports of SEs corresponding to packet generation rate of 0.5 (Hybrid)

First Stage			Second Stage			Third Stage			Fourth Stage	
SE#	P_{out}	$P_{aux\ in}$	SE#	P_{out}	$P_{aux\ in}$	SE#	P_{out}	$P_{aux\ in}$	SE#	P_{out}
SE1,1	0.4727	0.1250	SE2,1	0.4179	0.0037	SE3,1	0.3769	0.0087	SE4,1	0.3803
SE1,2	0.4727	0.1250							SE4,2	0.3803
SE1,3	0.4727	0.1250	SE2,2	0.4179	0.0037	SE3,2	0.3769	0.0087	SE4,3	0.3803
SE1,4	0.4727	0.1250							SE4,4	0.3803
SE1,5	0.4375	0.0000	SE2,3	0.3908	0.0037	SE3,3	0.3554	0.0087	SE4,5	0.3576
SE1,6	0.4375	0.0000							SE4,6	0.3576
SE1,7	0.4375	0.0000	SE2,4	0.3908	0.0037	SE3,4	0.3554	0.0087	SE4,7	0.3576
SE1,8	0.4375	0.0000							SE4,8	0.3576
FT1,1	0.0859	0.1719	FT2,1	0.1352	0.1117	FT3,1	0.1654	0.0873	FT4,1	0.1563
FT1,2	0.0859	0.1719	FT2,2	0.1352	0.1117	FT3,2	0.1654	0.0873	FT4,2	0.1563
FT1,3	0.0859	0.1719	FT2,3	0.1279	0.0957	FT3,3	0.1606	0.0764	FT4,3	0.1563
FT1,4	0.0859	0.1719	FT2,4	0.1279	0.0957	FT3,4	0.1606	0.0764	FT4,4	0.1563

Table 4.9(b)

Prob. of packet availability at O/Ports of SEs corresponding to packet generation rate of 0.8 (Hybrid)

First Stage			Second Stage			Third Stage			Fourth Stage	
SE#	P_{out}	$P_{aux\ in}$	SE#	P_{out}	$P_{aux\ in}$	SE#	P_{out}	$P_{aux\ in}$	SE#	P_{out}
SE1,1	0.6976	0.3200	SE2,1	0.5819	0.0280	SE3,1	0.5093	0.0480	SE4,1	0.5146
SE1,2	0.6976	0.3200							SE4,2	0.5146
SE1,3	0.6976	0.3200	SE2,2	0.5819	0.0280	SE3,2	0.5093	0.0480	SE4,3	0.5146
SE1,4	0.6976	0.3200							SE4,4	0.5146
SE1,5	0.6400	0.0000	SE2,3	0.5441	0.0280	SE3,3	0.4828	0.0480	SE4,5	0.4842
SE1,6	0.6400	0.0000							SE4,6	0.4842
SE1,7	0.6400	0.0000	SE2,4	0.5441	0.0280	SE3,4	0.4828	0.0480	SE4,7	0.4842
SE1,8	0.6400	0.0000							SE4,8	0.4842
FT1,1	0.2368	0.4736	FT2,1	0.3173	0.2433	FT3,1	0.3463	0.1693	FT4,1	0.3132
FT1,2	0.2368	0.4736	FT2,2	0.3173	0.2433	FT3,2	0.3463	0.1693	FT4,2	0.3132
FT1,3	0.2368	0.4736	FT2,3	0.3024	0.2048	FT3,3	0.3387	0.1480	FT4,3	0.3132
FT1,4	0.2368	0.4736	FT2,4	0.3024	0.2048	FT3,4	0.3387	0.1480	FT4,4	0.3132

Table 4.9(c)

Prob. of packet availability at O/Ports of SEs corresponding to packet generation rate of 1.0 (Hybrid)

First Stage			Second Stage			Third Stage			Fourth Stage	
SE#	P_{out}	$P_{aux\ in}$	SE#	P_{out}	$P_{aux\ in}$	SE#	P_{out}	$P_{aux\ in}$	SE#	P_{out}
SE1,1	0.8125	0.5000	SE2,1	0.6599	0.0703	SE3,1	0.5728	0.0971	SE4,1	0.5763
SE1,2	0.8125	0.5000							SE4,2	0.5763
SE1,3	0.8125	0.5000	SE2,2	0.6599	0.0703	SE3,2	0.5728	0.0971	SE4,3	0.5763
SE1,4	0.8125	0.5000							SE4,4	0.5763
SE1,5	0.7500	0.0000	SE2,3	0.6231	0.0703	SE3,3	0.5491	0.0971	SE4,5	0.5466
SE1,6	0.7500	0.0000							SE4,6	0.5466
SE1,7	0.7500	0.0000	SE2,4	0.6231	0.0703	SE3,4	0.5491	0.0971	SE4,7	0.5466
SE1,8	0.7500	0.0000							SE4,8	0.5466
FT1,1	0.3750	0.7500	FT2,1	0.4488	0.3301	FT3,1	0.4584	0.2177	FT4,1	0.4031
FT1,2	0.3750	0.7500	FT2,2	0.4488	0.3301	FT3,2	0.4584	0.2177	FT4,2	0.4031
FT1,3	0.3750	0.7500	FT2,3	0.4327	0.2812	FT3,3	0.4512	0.1941	FT4,3	0.4031
FT1,4	0.3750	0.7500	FT2,4	0.4327	0.2812	FT3,4	0.4512	0.1941	FT4,4	0.4031

As per P_{out} parameter of first stage in Tables 4.9(a)-4.9(c), the probability (i.e. 0.4727) of a packet being present at the output port of each SE in the upper sub-network#1 is higher than that (i.e. 0.4375) in the lower sub-network#0. This is because the auxiliary links of SEs in the lower sub-network#0 are connected to the auxiliary links of the SEs in the upper sub-network#1. Any conflict (for output port) between packets in the SEs of lower sub-network#0 leads to the steering of packet towards auxiliary links resulting in increase in traffic in the upper sub-network#1. Hence, the probability of a packet at the output ports of SEs of upper subnetwork#1 is higher.

From the third column of Tables 4.9(a) to 4.9(c), the probability values for availability of a packet at auxiliary ports of lower subnetwork SEs are all zero but are non-zero for SEs of upper subnetwork. Since fault-tolerant SEs of first stage do not receive any packets from any source directly and since there is only one auxiliary input port, any packet received at auxiliary port gets the required output port without any conflict and none of the packet is routed towards the auxiliary link of lower subnetwork. Hence the values are zero. But since the auxiliary output ports of SEs of lower subnetwork are linked to the auxiliary ports of SEs of upper subnetwork, hence the probability values at the auxiliary input ports of upper subnetwork are non-zero.

As the packet generation rates considered i.e 0.8 and 1.0 in Table 4.9(b) and 4.9(c) are higher than that considered in the Table 4.9(a), the probability of a packet being present at each of the output ports in every stage in Table 4.9(c) is higher than that in Table 4.9(b) which in turn is higher than that in the Table 4.9(a).

The probability of packet availability corresponding to different packet generation rates for single SE fault in first stage in the upper subnetwork.have been presented in Tables 4.10(a) to 4.10(c)

Table 4.10(a)

Prob. of packet availability at O/Ports of SEs corresponding to packet generation rate of 0.5 when single SE faulty in first stage in the upper subnetwork (Hybrid)

First Stage			Second Stage			Third Stage			Fourth	
SE#	P_{out}	$P_{aux\ in}$	SE#	P_{out}	$P_{aux\ in}$	SE#	P_{out}	$P_{aux\ in}$	SE#	P_{out}
SE1,1	0.0000	0.1719	SE2,1	0.2497	0.0350	SE3,1	0.3185	0.0197	SE4,1	0.1592
SE1,2	0.4723	0.1250							SE4,2	0.3579
SE1,3	0.4723	0.1250	SE2,2	0.4270	0.0350	SE3,2	0.3185	0.0197	SE4,3	0.3579
SE1,4	0.4723	0.1250							SE4,4	0.3579
SE1,5	0.4723	0.1250	SE2,3	0.4049	0.0037	SE3,3	0.3654	0.0225	SE4,5	0.3758
SE1,6	0.4375	0.0000							SE4,6	0.3615
SE1,7	0.4375	0.0000	SE2,4	0.3908	0.0037	SE3,4	0.3654	0.0225	SE4,7	0.3615
SE1,8	0.4375	0.0000							SE4,8	0.3615
FT1,1	0.4435	0.0215	FT2,1	0.2656	0.0279	FT3,1	0.2130	0.0573	FT4,1	0.2073
FT1,2	0.0859	0.1719	FT2,2	0.2968	0.1117	FT3,2	0.2130	0.0573	FT4,2	0.2073
FT1,3	0.0859	0.1719	FT2,3	0.1315	0.1036	FT3,3	0.2257	0.0573	FT4,3	0.2073
FT1,4	0.0859	0.1719	FT2,4	0.1279	0.0957	FT3,4	0.2257	0.0573	FT4,4	0.2073

Table 4.10(b)

Prob. of packet availability at O/Ports of SEs corresponding to packet generation rate of 0.8 when single SE faulty in first stage in the upper subnetwork (Hybrid)

First Stage			Second Stage			Third Stage			Fourth Stage	
SE#	P_{out}	$P_{aux\ in}$	SE#	P_{out}	$P_{aux\ in}$	SE#	P_{out}	$P_{aux\ in}$	SE#	P_{out}
SE1,1	0.0000	0.4736	SE2,1	0.3821	0.1022	SE3,1	0.4522	0.0685	SE4,1	0.2261
SE1,2	0.6976	0.3200							SE4,2	0.4960
SE1,3	0.6976	0.3200	SE2,2	0.5976	0.1022	SE3,2	0.4522	0.0685	SE4,3	0.4960
SE1,4	0.6976	0.3200							SE4,4	0.4960
SE1,5	0.6976	0.3200	SE2,3	0.5634	0.0280	SE3,3	0.4973	0.0773	SE4,5	0.5107
SE1,6	0.6400	0.0000							SE4,6	0.4891
SE1,7	0.6400	0.0000	SE2,4	0.5441	0.0280	SE3,4	0.4973	0.0773	SE4,7	0.4891
SE1,8	0.6400	0.0000							SE4,8	0.4891
FT1,1	0.6673	0.1516	FT2,1	0.4304	0.0608	FT3,1	0.3765	0.1200	FT4,1	0.3487
FT1,2	0.2368	0.4736	FT2,2	0.4840	0.2433	FT3,2	0.3765	0.1200	FT4,2	0.3487
FT1,3	0.2368	0.4736	FT2,3	0.3097	0.2237	FT3,3	0.3952	0.1200	FT4,3	0.3487
FT1,4	0.2368	0.4736	FT2,4	0.3024	0.2048	FT3,4	0.3952	0.1200	FT4,4	0.3487

Table 4.10(c)
Prob. of packet availability at O/Ports of SEs corresponding to packet generation rate of 1.0 when single SE faulty in first stage in the upper subnetwork (Hybrid)

First Stage			Second Stage			Third Stage			Fourth Stage	
SE#	P_{out}	P_{aux_in}	SE#	P_{out}	P_{aux_in}	SE#	P_{out}	P_{aux_in}	SE#	P_{out}
SE1,1	0.0000	0.7500	SE2,1	0.4572	0.1717	SE3,1	0.5201	0.1181	SE4,1	0.2601
SE1,2	0.8125	0.5000							SE4,2	0.5607
SE1,3	0.8125	0.5000	SE2,2	0.6777	0.1717	SE3,2	0.5201	0.1181	SE4,3	0.5607
SE1,4	0.8125	0.5000							SE4,4	0.5607
SE1,5	0.8125	0.5000	SE2,3	0.6420	0.0703	SE3,3	0.5632	0.1312	SE4,5	0.5735
SE1,6	0.7500	0.0000							SE4,6	0.5510
SE1,7	0.7500	0.0000	SE2,4	0.6231	0.0703	SE3,4	0.5632	0.1312	SE4,7	0.5510
SE1,8	0.7500	0.0000							SE4,8	0.5510
FT1,1	0.7969	0.3750	FT2,1	0.5351	0.0825	FT3,1	0.4736	0.1610	FT4,1	0.4248
FT1,2	0.3750	0.7500	FT2,2	0.5919	0.3301	FT3,2	0.4736	0.1610	FT4,2	0.4248
FT1,3	0.3750	0.7500	FT2,3	0.4406	0.3052	FT3,3	0.4927	0.1610	FT4,3	0.4248
FT1,4	0.3750	0.7500	FT2,4	0.4327	0.2813	FT3,4	0.4927	0.1610	FT4,4	0.4248

In 4.10(a), it has been assumed that switching element SE1,1 becomes faulty and the packet generation rate is 0.5. Since SE1,1 has been assumed faulty, the probability at its output port is 0.0000. The source connected to SE1,1 have secondary paths linked to switching element FT1,1 in the fault-tolerant sub-network. As such, the probability of a packet being present at the output port of FT1,1 is higher (i.e. 0.4727) than any other first stage SEs of fault-tolerant sub-network (i.e. 0.0859). As per design (Figure 3.1), the auxiliary links of first stage SEs in the fault-tolerant sub-network are linked to the auxiliary links of upper sub-network#0. Since the packet generation rate in case of switching element FT1,1 is higher and FT1,1 is linked to SE1,1, as such the probability value at auxiliary link of SE1,1 is non-zero (i.e. 0.1719).

In Table 4.10(b), the packet generation rate has been considered 0.8, higher than that being considered in the previous Table 4.10(a). As such, the packet generation and propagation probability values for each SE is higher than that in the previous Table 4.10(a). The same reason applies when for larger probability values in Tables 4.10(c) when compared with values tabulated in 4.10(a) and 4.10(b).

The probability of packet availability for packet generation rates of 0.5, 0.8 and 1.0 corresponding to single SE faulty in first stage in the lower subnetwork have been evaluated and are given in Tables 4.11(a) to 4.11(c) and the probability corresponding to

four SEs being faulty in first stage upper subnetwork are given in Tables 4.16(a) to 4.16(c).

Table 4.11(a)
Prob. of packet availability at O/Ports of SEs corresponding to packet generation rate of 0.5 when single SE faulty in first stage in the lower subnetwork (Hybrid)

First Stage			Second Stage			Third Stage			Fourth Stage	
SE#	P_{out}	$P_{aux\ in}$	SE#	P_{out}	$P_{aux\ in}$	SE#	P_{out}	$P_{aux\ in}$	SE#	P_{out}
SE1,1	0.4435	0.0215	SE2,1	0.4173	0.0390	SE3,1	0.3844	0.0203	SE4,1	0.3713
SE1,2	0.4727	0.1250							SE4,2	0.3831
SE1,3	0.4727	0.1250	SE2,2	0.4282	0.0390	SE3,2	0.3844	0.0203	SE4,3	0.3831
SE1,4	0.4727	0.1250							SE4,4	0.3831
SE1,5	0.0000	0.1719	SE2,3	0.2202	0.0037	SE3,3	0.2926	0.0240	SE4,5	0.1463
SE1,6	0.4375	0.0000							SE4,6	0.3330
SE1,7	0.4375	0.0000	SE2,4	0.3908	0.0037	SE3,4	0.2926	0.0240	SE4,7	0.3330
SE1,8	0.4375	0.0000							SE4,8	0.3330
FT1,1	0.4727	0.1250	FT2,1	0.3075	0.1050	FT3,1	0.2300	0.0894	FT4,1	0.2231
FT1,2	0.0860	0.1719	FT2,2	0.3100	0.1117	FT3,2	0.2300	0.0894	FT4,2	0.2231
FT1,3	0.0860	0.1719	FT2,3	0.0951	0.0240	FT3,3	0.2444	0.0894	FT4,3	0.2231
FT1,4	0.0860	0.1719	FT2,4	0.1280	0.0957	FT3,4	0.2444	0.0894	FT4,4	0.2231

Table 4.11(b)
Prob. of packet availability at O/Ports of SEs corresponding to packet generation rate of 0.8 when single SE faulty in first stage in the upper subnetwork (Hybrid)

First Stage			Second Stage			Third Stage			Fourth Stage	
SE#	P_{out}	$P_{aux\ in}$	SE#	P_{out}	$P_{aux\ in}$	SE#	P_{out}	$P_{aux\ in}$	SE#	P_{out}
SE1,1	0.6673	0.1516	SE2,1	0.5898	0.1091	SE3,1	0.5228	0.0676	SE4,1	0.5078
SE1,2	0.6976	0.3200							SE4,2	0.5190
SE1,3	0.6976	0.3200	SE2,2	0.5991	0.1091	SE3,2	0.5228	0.0676	SE4,3	0.5190
SE1,4	0.6976	0.3200							SE4,4	0.5190
SE1,5	0.0000	0.4736	SE2,3	0.3295	0.0280	SE3,3	0.4162	0.0796	SE4,5	0.2081
SE1,6	0.6400	0.0000							SE4,6	0.4615
SE1,7	0.6400	0.0000	SE2,4	0.5441	0.0280	SE3,4	0.4162	0.0796	SE4,7	0.4615
SE1,8	0.6400	0.0000							SE4,8	0.4615
FT1,1	0.6976	0.3200	FT2,1	0.4928	0.2329	FT3,1	0.3963	0.1767	FT4,1	0.3657
FT1,2	0.2368	0.4736	FT2,2	0.4958	0.2433	FT3,2	0.3963	0.1767	FT4,2	0.3657
FT1,3	0.2368	0.4736	FT2,3	0.2427	0.0512	FT3,3	0.4180	0.1767	FT4,3	0.3657
FT1,4	0.2368	0.4736	FT2,4	0.3024	0.2048	FT3,4	0.4180	0.1767	FT4,4	0.3657

Table 4.11(c)

Prob. of packet availability at O/Ports of SEs corresponding to packet generation rate of 1.0 when single SE faulty in first stage in the upper subnetwork (Hybrid)

First Stage			Second Stage			Third Stage			Fourth Stage	
SE#	P_{out}	$P_{aux\ in}$	SE#	P_{out}	$P_{aux\ in}$	SE#	P_{out}	$P_{aux\ in}$	SE#	P_{out}
SE1,1	0.7969	0.3750	SE2,1	0.6743	0.1763	SE3,1	0.5872	0.1149	SE4,1	0.5751
SE1,2	0.8125	0.5000							SE4,2	0.5806
SE1,3	0.8125	0.5000	SE2,2	0.6785	0.1763	SE3,2	0.5872	0.1149	SE4,3	0.5806
SE1,4	0.8125	0.5000							SE4,4	0.5806
SE1,5	0.0000	0.7500	SE2,3	0.3970	0.0703	SE3,3	0.4848	0.1326	SE4,5	0.2424
SE1,6	0.7500	0.0000							SE4,6	0.5265
SE1,7	0.7500	0.0000	SE2,4	0.6231	0.0703	SE3,4	0.4848	0.1326	SE4,7	0.5265
SE1,8	0.7500	0.0000							SE4,8	0.5265
FT1,1	0.8125	0.5000	FT2,1	0.5957	0.3238	FT3,1	0.4910	0.2288	FT4,1	0.4391
FT1,2	0.3750	0.7500	FT2,2	0.5972	0.3301	FT3,2	0.4910	0.2288	FT4,2	0.4391
FT1,3	0.3750	0.7500	FT2,3	0.3631	0.0703	FT3,3	0.5132	0.2288	FT4,3	0.4391
FT1,4	0.3750	0.7500	FT2,4	0.4327	0.2813	FT3,4	0.5132	0.2288	FT4,4	0.4391

In the above Table 4.11(a), it has been assumed that switching element SE1,5 becomes faulty and the packet generation rate is 0.5. Since SE1,5 has been assumed faulty, the probability at its output port is 0.0000. The source connected to SE1,5 have secondary paths linked to switching element FT1,1 in the fault-tolerant sub-network. From the Table, it has been seen observed that the probability of a packet being present at the output port of FT1,1 (i.e. 0.4727) which is higher than any other first stage SEs of fault-tolerant sub-network (i.e. 0.0860).

In Table 4.11(b), the packet generation rate has been considered 0.8, higher than that being considered in the previous Table 4.11(a). As such, the packet generation and propagation probability values for each SE is higher than that in the previous Table 4.11(a). The same reason applies when for larger probability values in Tables 4.11(c) when compared with values tabulated in 4.11(a) and 4.11(b).

In the following Tables 4.12(a) to 4.12(c) have been tabulated probability values of packet availability for different packet generation rates corresponding to four SEs faulty in first stage in the lower subnetwork.

Table 4.12(a)

Prob. of packet availability at O/Ports of SEs corresponding to packet generation rate of 0.5 when four SEs faulty in first stage in the lower subnetwork (Hybrid)

First Stage			Second Stage			Third Stage			Fourth Stage	
SE#	P_{out}	$P_{aux\ in}$	SE#	P_{out}	$P_{aux\ in}$	SE#	P_{out}	$P_{aux\ in}$	SE#	P_{out}
SE1,1	0.0000	0.1719	SE2,1	0.0492	0.0984	SE3,1	0.0888	0.0846	SE4,1	0.0444
SE1,2	0.0000	0.1719							SE4,2	0.0444
SE1,3	0.0000	0.1719	SE2,2	0.0492	0.0984	SE3,2	0.0888	0.0846	SE4,3	0.0444
SE1,4	0.0000	0.1719							SE4,4	0.0444
SE1,5	0.4727	0.1250	SE2,3	0.4455	0.0984	SE3,3	0.4214	0.0846	SE4,5	0.3972
SE1,6	0.4727	0.1250							SE4,6	0.3972
SE1,7	0.4727	0.1250	SE2,4	0.4455	0.0984	SE3,4	0.4214	0.0846	SE4,7	0.3972
SE1,8	0.4727	0.1250							SE4,8	0.3972
FT1,1	0.4435	0.0215	FT2,1	0.3944	0.0000	FT3,1	0.3694	0.0012	FT4,1	0.3353
FT1,2	0.4435	0.0215	FT2,2	0.3944	0.0000	FT3,2	0.3694	0.0012	FT4,2	0.3353
FT1,3	0.4435	0.0215	FT2,3	0.4282	0.1118	FT3,3	0.3694	0.0012	FT4,3	0.3353
FT1,4	0.4435	0.0215	FT2,4	0.4282	0.1118	FT3,4	0.3694	0.0012	FT4,4	0.3353

Table 4.12(b)

Prob. of packet availability at O/Ports of SEs corresponding to packet generation rate of 0.8 when four SEs faulty in first stage in the lower subnetwork (Hybrid)

First Stage			Second Stage			Third Stage			Fourth Stage	
SE#	P_{out}	$P_{aux\ in}$	SE#	P_{out}	$P_{aux\ in}$	SE#	P_{out}	$P_{aux\ in}$	SE#	P_{out}
SE1,1	0.0000	0.4736	SE2,1	0.1113	0.2226	SE3,1	0.1840	0.1700	SE4,1	0.0920
SE1,2	0.0000	0.4736							SE4,2	0.0920
SE1,3	0.0000	0.4736	SE2,2	0.1113	0.2226	SE3,2	0.1840	0.1700	SE4,3	0.0920
SE1,4	0.0000	0.4736							SE4,4	0.0920
SE1,5	0.6976	0.3200	SE2,3	0.6231	0.2226	SE3,3	0.5663	0.1700	SE4,5	0.5332
SE1,6	0.6976	0.3200							SE4,6	0.5332
SE1,7	0.6976	0.3200	SE2,4	0.6231	0.2226	SE3,4	0.5663	0.1700	SE4,7	0.5332
SE1,8	0.6976	0.3200							SE4,8	0.5332
FT1,1	0.6673	0.1516	FT2,1	0.5560	0.0000	FT3,1	0.4998	0.0062	FT4,1	0.4373
FT1,2	0.6673	0.1516	FT2,2	0.5560	0.0000	FT3,2	0.4998	0.0062	FT4,2	0.4373
FT1,3	0.6673	0.1516	FT2,3	0.6100	0.2433	FT3,3	0.4998	0.0062	FT4,3	0.4373
FT1,4	0.6673	0.1516	FT2,4	0.6100	0.2433	FT3,4	0.4998	0.0062	FT4,4	0.4373

Table 4.12(c)
Prob. of packet availability at O/Ports of SEs corresponding to packet generation rate of 1.0 when four SEs faulty in first stage in the lower subnetwork (Hybrid)

First Stage			Second Stage			Third Stage			Fourth Stage	
SE#	P_{out}	$P_{aux\ in}$	SE#	P_{out}	$P_{aux\ in}$	SE#	P_{out}	$P_{aux\ in}$	SE#	P_{out}
SE1,1	0.0000	0.7500	SE2,1	0.1588	0.3175	SE3,1	0.2470	0.2231	SE4,1	0.1235
SE1,2	0.0000	0.7500							SE4,2	0.1235
SE1,3	0.0000	0.7500	SE2,2	0.1588	0.3175	SE3,2	0.2470	0.2231	SE4,3	0.1235
SE1,4	0.0000	0.7500							SE4,4	0.1235
SE1,5	0.8125	0.5000	SE2,3	0.7034	0.3175	SE3,3	0.6266	0.2231	SE4,5	0.5923
SE1,6	0.8125	0.5000							SE4,6	0.5923
SE1,7	0.8125	0.5000	SE2,4	0.7034	0.3175	SE3,4	0.6266	0.2231	SE4,7	0.5923
SE1,8	0.8125	0.5000							SE4,8	0.5923
FT1,1	0.7969	0.3750	FT2,1	0.6381	0.0000	FT3,1	0.5595	0.0126	FT4,1	0.4812
FT1,2	0.7969	0.3750	FT2,2	0.6381	0.0000	FT3,2	0.5595	0.0126	FT4,2	0.4812
FT1,3	0.7969	0.3750	FT2,3	0.6979	0.3301	FT3,3	0.5595	0.0126	FT4,3	0.4812
FT1,4	0.7969	0.3750	FT2,4	0.6979	0.3301	FT3,4	0.5595	0.0126	FT4,4	0.4812

Here four SEs have been assumed faulty, the sources connected to the faulty SEs steer their packets towards secondary paths leading into the fault-tolerant sub-network. In spite of faulty SEs in the lower subnetwork, there exists probability of a packet being present at the output port of each SE in the last stage of the lower subnetwork. This is due to the conflict between packets in the fault-tolerant sub-network and hence packets getting steered towards auxiliary links leading to their arrival in the lower sub-network.
Since the packet generation rate in Table 4.12(c) i.e. 1.0 is highest followed by 0.8 in Table 4.12(b) and then 0.5 in Table 4.12(a), that is why the probability values are highest in Table 4.12(c) and lowest in Table 4.12(a).

4.4.2 Probability of acceptance and Bandwidth

Probability of acceptance, as defined in chapter 1, is the ratio of the average number of requests accepted by the destination to the average number of requests submitted by the sources per network cycle and bandwidth is defined as the average number of requests accepted per network cycle.
The Tables 4.13(a) to 4.13(e) present the values of probability of acceptance and bandwidth for Hybrid Network for fault-free and faulty scenarios.

Table 4.13(a)

Prob. of acceptance and Bandwidth values under fault-free conditions

Packet generation rate	Bandwidth	Probability of acceptance	Packet generation rate	Bandwidth	Probability of acceptance
0.1	1.5626	0.9766	0.6	8.3638	0.8712
0.2	3.0581	0.9557	0.7	9.4805	0.8465
0.3	4.4912	0.9357	0.8	10.4985	0.8200
0.4	5.8590	0.9155	0.9	11.4051	0.7920
0.5	7.1533	0.8942	1.0	12.2076	0.7630

Table 4.13(b)

Prob. of acceptance and Bandwidth values for single SE faulty in first stage in upper sub network

Packet generation rate	Bandwidth	Probability of acceptance	Packet generation rate	Bandwidth	Probability of acceptance
0.1	1.5640	0.9775	0.6	8.1911	0.8532
0.2	3.0553	0.9548	0.7	9.2349	0.8246
0.3	4.4703	0.9313	0.8	10.1735	0.7948
0.4	5.8027	0.9067	0.9	11.0064	0.7643
0.5	7.0453	0.8807	1.0	11.7353	0.7335

Table 4.13(c)

Prob. of acceptance and Bandwidth values for single SE faulty in first stage in lower sub network

Packet generation rate	Bandwidth	Probability of acceptance	Packet generation rate	Bandwidth	Probability of acceptance
0.1	1.5714	0.9822	0.6	8.2663	0.8611
0.2	3.0800	0.9625	0.7	9.3079	0.8311
0.3	4.5147	0.9406	0.8	10.2408	0.8001
0.4	5.8638	0.9162	0.9	11.0670	0.7685
0.5	7.1169	0.8896	1.0	11.7903	0.7369

Table 4.13(d)

Prob. of acceptance and Bandwidth values when all SEs faulty in first stage in upper subnetwork

Packet generation rate	Bandwidth	Probability of acceptance	Packet generation rate	Bandwidth	Probability of acceptance
0.1	1.5281	0.9550	0.6	7.0763	0.7371
0.2	2.9087	0.9090	0.7	7.8348	0.6995
0.3	4.1438	0.8633	0.8	8.5000	0.6641
0.4	5.2423	0.8191	0.9	9.0787	0.6305
0.5	6.2157	0.7770	1.0	9.5758	0.5985

Table 4.13(e)
Prob. of acceptance and Bandwidth values when all SEs faulty in first stage in lower subnetwork

Packet generation rate	Bandwidth	Probability of acceptance	Packet generation rate	Bandwidth	Probability of acceptance
0.1	1.5405	0.9628	0.6	7.2377	0.7539
0.2	2.9497	0.9218	0.7	8.0116	0.7153
0.3	4.2196	0.8791	0.8	8.6862	0.6786
0.4	5.3520	0.8362	0.9	9.2699	0.6437
0.5	6.3546	0.7943	1.0	9.7699	0.6106

From the above Table 4.13(a) to 4.13(e) , the probability of acceptance and bandwidth values decrease with increase in packet generation probability which is expected from the network.

4.4.3 Average Queue Length and Optimal Buffer Requirement

It has been recognized that buffers in MINs can increase the MIN performance significantly. They also prevent a packet from being lost when a path conflict occurs. When buffers are kept in each SE, then a packet can leave its buffer only when the destination buffer at the succeeding stage is able to accept it.

Table 4.14(a) and 4.14(b) give the average queue length of packets in the buffers of SEs and hence the requirement of the optimal number of buffers for fault-free and faulty scenarios. The formula being used for evaluation of average queue length is that of M/M/1 queuing model i.e. average queue length = $\frac{\lambda}{\mu}\frac{\lambda}{(\mu-\lambda)}$ where λ is the mean arrival rate and μ is the mean service rate. For each SE, $\lambda = P_{out}$ and P_{out} is the probability of a packet being present at the output port of SEs in the previous stage and $\mu = 1$. The packet generation rate has been taken 1.0 that corresponds to maximum traffic and hence the above Table gives the buffer requirements of SE ports under maximum traffic scenario.

Table 4.14(a)
Optimal Buffer Requirement in Hybrid Network under fault-free condtitions

SE#	Avg Queue Length at each of the regular Output port	Min No. of buffers at each of the regular Output Port	Avg Queue Len at the aux Input port	Min No. of buffers required at the regular Input port	SE#	Avg Queue Length at each of the regular Output port	Min No. of buffers at each of the regular Output Port	Average Queue Length at the aux Input port	Min Number of buffers required at the regular Input port
SE1,	3.5211	4	0.5	1	SE4,	0.7838	1	-	-
SE1,	3.5211	4	0.5	1	SE4,	0.7838	1	-	-
SE1,	3.5211	4	0.5	1	SE4,	0.7838	1	-	-
SE1,	3.5211	4	0.5	1	SE4,	0.7838	1	-	-
SE1,	2.25	3	-		SE4,	0.6617	1	-	-
SE1,	2.25	3	-		SE4,	0.6617	1	-	-
SE1,	2.25	3	-		SE4,	0.6617	1	-	-
SE1,	2.25	3	-		SE4,	0.6617	1	-	-
FT1,	0.2250	1	2.25	3	FT4,	0.2722	1	-	-
FT1,	0.2250	1	2.25	3	FT4,	0.2722	1	-	-
FT1,	0.2250	1	2.25	3	FT4,	0.2722	1	-	-
FT1,	0.2250	1	2.25	3	FT4,	0.2722	1	-	-
SE2,	1.2805	2	0.005	1	SE3,	0.7680	1	0.0104	1
SE2,	1.2805	2	0.005	1	SE3,	0.7680	1	0.0104	1
SE2,	1.0303	2	0.005	1	SE3,	0.6687	1	0.0104	1
SE2,	1.0303	2	0.005	1	SE3,	0.6687	1	0.0104	1
FT2,	0.3650	1	0.162	1	FT3,	0.3879	1	0.3879	1
FT2,	0.3650	1	0.162	1	FT3,	0.3879	1	0.3879	1
FT2,	0.1101	1	0.109	1	FT3,	0.3710	1	0.3879	1
FT2,	0.1101	1	0.109	1	FT3,	0.3710	1	0.3879	1

The Table 4.14(b) provides the optimal buffer requirement for maximum value of packet generation rate considering that four SEs have become faulty in the first stage. Because of faulty SEs, their packets get directed to fault-tolerant subnetwork and that is why the buffer requirement value is higher i.e. 4 as compared to that in Table 4.14(a) i.e one. Since the fourth stage is SEs have no auxiliary ports, as such hyphen has been shown in the Tables 4.14(a) and 4.14(b).The next section discusses the terminal reliability of the M_FDOT for favorite as well as for non-favorite destinations.

Table 4.14(b)

Optimal Buffer Requirement in Hybrid Network when four SEs faulty in first stage in lower subnetwork

SE#	Average Queue Length at each of the regular O/P	Minimum Number of buffers at each of the regular O/P	Average Queue Length at the auxiliary Input port	Minimum Number of buffers required at the regular Input port	SE#	Average Queue Length at each of the regular O/P	Minimum Number of buffers at each of the regular O/P	Average Queue Length at the auxiliary Input port	Minimum Number of buffers required at the regular Input port
SE1,1	-	-	2.25	3	SE4,1	0.0175	1	-	-
SE1,2	-	-	2.25	3	SE4,2	0.0175	1	-	-
SE1,3	-	-	2.25	3	SE4,3	0.0175	1	-	-
SE1,4	-	-	2.25	3	SE4,4	0.0175	1	-	-
SE1,5	3.5211	4	0.5	1	SE4,5	0.8604	1	-	-
SE1,6	3.5211	4	0.5	1	SE4,6	0.8604	1	-	-
SE1,7	3.5211	4	0.5	1	SE4,7	0.8604	1	-	-
SE1,8	3.5211	4	0.5	1	SE4,8	0.8604	1	-	-
FT1,1	3.1270	4	0.2250	1	FT4,1	0.4464	1	-	-
FT1,2	3.1270	4	0.2250	1	FT4,2	0.4464	1	-	-
FT1,3	3.1270	4	0.2250	1	FT4,3	0.4464	1	-	-
FT1,4	3.1270	4	0.2250	1	FT4,4	0.4464	1	-	-
SE2,1	0.0300	1	0.0300	1	SE3,1	0.0810	1	0.0641	1
SE2,2	0.0300	1	0.0300	1	SE3,2	0.0810	1	0.0641	1
SE2,3	1.6682	2	0.1477	1	SE3,3	1.0514	2	0.0641	1
SE2,4	1.6682	2	0.1477	1	SE3,4	1.0514	2	0.0641	1
FT2,1	1.1252.	2	-	-	FT3,1	0.7106	1	1.6079	2
FT2,2	1.1252	2	-	-	FT3,2	0.7106	1	1.6079	2
FT2,3	1.6124	2	0.1627	1	FT3,3	0.7106	1	1.6079	2
FT2,4	1.6124	2	0.1627	1	FT3,4	0.7106	1	1.6079	2

4.4.4 Terminal Reliability

Terminal Reliability is the probability that a given source-destination pair has at least one fault-free path between them, given that each SE has a certain reliability (the reliability of a SE is the probability that it is fault-free). The redundancy graph for favorite destination(s) is shown below

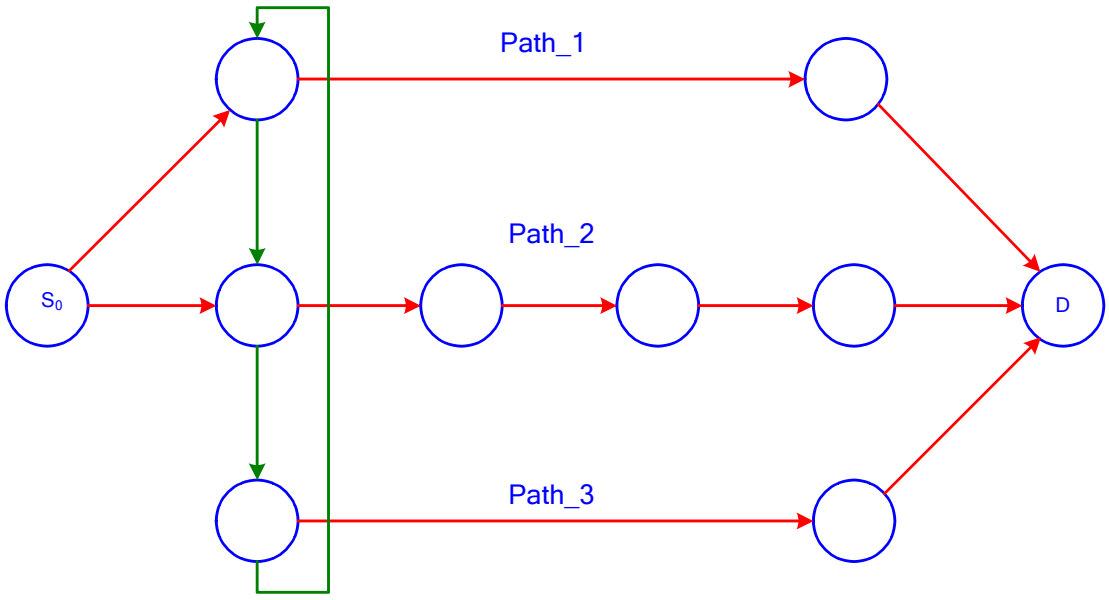

Figure 4.4(a) : Redundancy Graph of Hybrid Network for Favorite Destinations

The Source S_0 remains connected to the destination D if, at least, one of the three paths survives. Let r be reliability of each SE. The probability that

Path_1 fails = $1- r^2$

Path_2 fails = $1- r^4$

Path_3 fails = $1- r^2$

All the three paths fail = $(1- r^2)^2 \times (1- r^4)$

Probability that at least one path survives

i.e $R_{term} = 1 – [(1- r^2)^2 \times (1- r^4)]$

The values have been analyzed and are given below

Table 4.15(a)
Terminal Reliabilities of Hybrid Network (for favorite destinations)

SE Reliability	Terminal Reliability
0.90	0.9876
0.92	0.9932
0.94	0.997
0.96	0.999

The redundancy graph for non-favorite destinations is shown in Figure 4.7 below

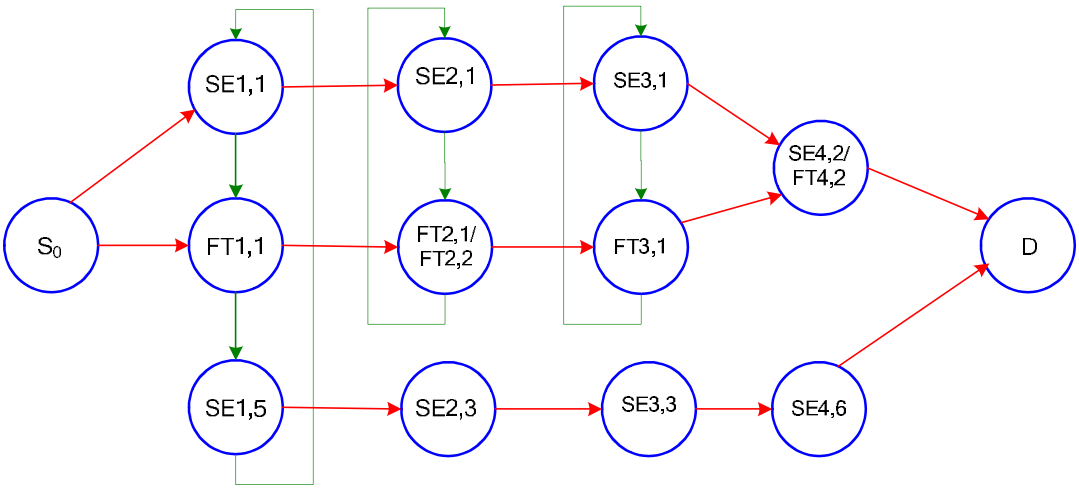

Figure 4.4(b) : Redundancy Graph for HYBRID Network for non-favorite Destinations

For stage S#1, probability that atleast one out of three – SE1,1; FT1,1 and SE1,5 survives is

$$R_{S\#1} = \left[1 - (1-r)^3\right]$$

In stage S#2, probability that atleast one of the two – SE2,1; FT2,1 survives is

$$R_{S\#2} = \left[1 - (1-r)^2\right]$$

In stage S#3, probability that at least one of the two SEs – SE3,1 and FT3,1 comprising of loop survives is

$$R_{S\#3} = \left[1 - (1-r)^2\right]$$

Terminal Reliability = $R_{S\#1} \times R_{S\#2} \times R_{S\#3\_loop} \times r$

Table 4.15(b)

Terminal Reliabilities of Hybrid Network for non-favorite destinations

SE Reliability	Terminal Reliability
0.90	0.8812
0.92	0.9078
0.94	0.933
0.96	0.9569

The terminal reliability values when compared with the corresponding SE reliability values reveal that these values are almost comparable. Hence the proposed design is worthwhile considering the terminal reliability aspect.

4.4.5 Hardware Complexity and Cost

To estimate the cost of a network, one common method is to calculate the switch complexity with an assumption that the cost of a switch is proportional to the number of gates involved. For example, a 2×2 SE has 4 units of cost and a 3×3 SE has 9 units of cost. For multiplexers and de-multiplexers, we roughly assume that each of kx1 and 1xk has k units of cost.

Number of stages = n where n = $\log_2$ N and n is even

First stage SEs = $\frac{N}{2^i} + \frac{N}{4}$ i=1;

Second sage SEs = $\frac{N}{2^i} + \frac{N}{4}$ i=2;

Total number of SEs = $2 * \sum_{i=1}^{n/2} \left(\frac{N}{2^i} \right) + \frac{N}{2^{i+1}}$

Link Complexity

Inter-stage links = $\sum_{i=1}^{n/2} \frac{N}{2^i} * 2 + \left(\frac{N}{4} * 2 \right)(n-1) + \sum_{i=2}^{n/2} \frac{N}{2^i} * 2$

Intra-stage links = $\sum_{i=1}^{n-1} \frac{N}{2^i} + \frac{N}{4} * (n-1)$

Cost of SEs = $9 * 2 * \sum_{i=1}^{(n/2)} (N /2^i + N/j) - 9* (N/2 + N/4) + 4* (N/2+N/4)$

$= 9 * 2 * \sum_{i=1}^{round(n/2)} (N /2^i + N/(2.2^i)) - 5*3*N/4$

Cost of Muxes and Demuxes = 4*N

Total cost of Hybrid Network $= 9 * 2* \sum_{i=1}^{(n/2)} (N /2^i + N/(2.2^i)) - 5*3*N/4 + 4*N;$

$= 9 * 2 * \sum_{i=1}^{(n/2)} (N /2^i + N/j) + N/4;$

The cost of the various sized Hybrid Network calculated according to the above formula has been shown in Table 4.16.

Table 4.16
Cost of various sized Hybrid Network

Size of MIN	Cost
16 × 16	364
64 × 64	1632
256 × 256	7968
1024×1024	41152

4.5 Modified Quad Tree Network (M_QUAD)

M_QUAD is a dynamic irregular fault-tolerant MIN. It is the modification of the existing QUAD Tree Network. Various techniques have been incorporated in an integrated manner to make it better in performance than the existing QUAD Tree Network. The techniques are – Chaining , an additional Fault-tolerant sub-network, three SEs per loop, change in the location of multiplexers and variation in the number of multiplexers and demultiplexers.

4.5.1 Design of M_QUAD

M_QUAD is an irregular type of network as the number of SEs in each stage are not equal. There are in all five stages of SEs : S#1, S#2, S#3, S#4 and S#5 starting from left to right. The entire network is comprised of two sub-networks: Normal QUAD (N_QUAD) and fault-tolerant QUAD (F_QUAD). These two sub-networks (i.e N_QUAD and F_QUAD) together constitute Modified QUAD (M_QUAD). In N_QUAD, there are in all twenty six SE, eight SEs each in the first and fifth stages, four SEs each in second and fourth stages and two SEs in the third stage. In F_QUAD, there are thirteen SEs in all, four SEs each in the first and fifth stages, two SEs each in the second and fourth stages and one SE in the third stage. These SEs are being termed as fault-tolerant (FT) SEs. N_QUAD SEs have been marked as SE#. The inter-stage connections are as per QUAD [9] network. Fault-tolerant sub-network is an addition to the existing network. In general, each subnetwork of M_QUAD consists of $N=2^n$ inputs and N outputs. N is called the size of the network. There are $(2*m-1)$ stages in all where $m=\log_2 N/2$. There are $(2^{m+2}-6)$ number of SEs in N_QUAD and F_QUAD

comprises of $(2^{m+2}-6)/2$ SEs. 2^{n-1} SEs in N_QUAD (in the last stage) are of size 2×2 and the rest are of size 3×3 (in the intermediate stages). The first stage SEs in F_QUAD multiplexers (each of size 2×1) and after the last stage of SEs in M_QUAD, there is a stage of demultiplexers (each of size 1×2). The total number of multiplexers and demultiplexers are N/2 and (2*N+N/2). The S_0, S_1, … S_{15} and the D_0, D_1… D_{15} denote destinations. In addition to inter-stage links, there are intra-stage connections also in all the stages except the last one. Chaining leads to the formation of loops. In the designed M_QUAD, there are four loops in first stage, two loops each in the second and fourth stages and a single loop in the third stage, each loop comprising of three SEs. Of the three SEs in each loop, two belong to N_QUAD and one belongs to F_QUAD. Chaining contributes towards fault-tolerance as well as distribution of traffic either during heavy load conditions or during conflicts between packets for the same port.

4.5.2 Routing Tag and Routing Algorithm

The proposed architecture makes use of distributed routing strategy i.e. each SE contributes towards routing of packets. Whenever a packet gets generated at a source, a destination address field is always there where the packet has to reach. Each source evaluates routing tag by executing routing algorithm. The algorithm for evaluating routing tag from destination address field is given in section 3.4.3. The routing scheme assumes that the sources and SEs have the ability to detect faults in the SEs to which they are connected. There are two links (i.e. primary and secondary) for each source. The primary link connects each source to N_QUAD and the secondary link connects the same source to F_QUAD to incorporate fault-tolerance. Each source attempts entry into the F_QUAD via its primary link along with the evaluated routing tag. If the source detects that the primary link led SE has become faulty, then the source steers the packet towards the secondary link. If the first stage SE/MUX at the termination of secondary link is also detected faulty then the M_QUAD loses its dynamic full access capability. For each SE in intermediate stages, if the regular output link is busy or if the successor SE in the next stage is faulty, then the packet is steered towards the auxiliary output port of the SE.

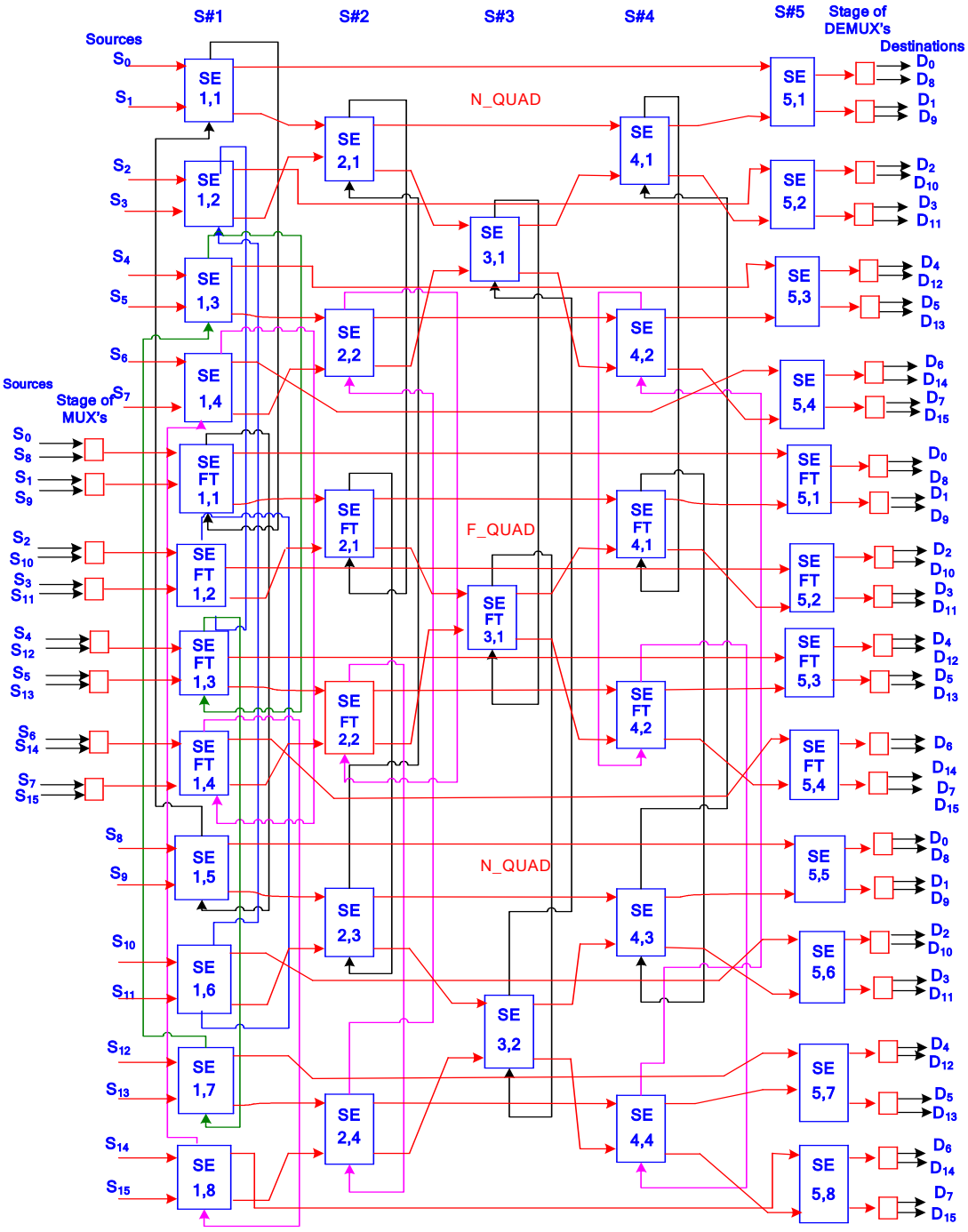

Figure 4.5 : Modified QUAD Tree Network (M_QUAD) with N=16

Routing Tag Algorithm

The algorithm for evaluating routing tag from destination address tag is as follows.

Let the source S and destination D be represented in binary code as

$$S = s_{n-1}s_{n-2}\ldots\ldots\ldots s_0$$

$$D = d_{n-1}d_{n-2}\ldots\ldots\ldots d_0$$

The destination tag is the address where the packet has to reach and source tag is the source address that has generated the packet. Let the routing tag be denoted as

$t_m t_{2m-1} t_{2m-2} \ldots\ldots t_0 t_{dm}$.

In the routing tag, the significance of the various bits is as under :

t_m = denotes the multiplexer control bit.

t_{2m-1} = denotes the bit that will be sensed by first stage SEs.

t_{2m-2} = denotes the bit that will be sensed by the second stage SEs.

……

t_0 = denotes the bit that will be sensed by the last stage SEs.

t_{dm} = denotes the demultiplexer control bit.

For stages round (n/2) to n

$t_n = 0$ [if ((s_1 equals d_1) and (s_2 equals d_2) …….. and (s_{i-2} equals d_{i-2}))]

where $n = 2m - 1$ and $m = \log_2(N/2)$

else $t_n = 1$

$t_{n-1} = 0$ [if (s_2 equals d_2) …….. and (s_{i-2} equals d_{i-2}))]

where $n = 2m - 1$ and $m = \log_2(N/2)$

else $t_{n-1} = 1$

Upto int(n/2) terms

Starting from stage 1

$t_0 = 0$ if (d_0 equals 0)

else $t_0 = 1$

$t_1 = 0$ if (d_1 equals 0)

else $t_1 = 1$

$t_2 = 0$ if (d_2 equals 0)

else $t_2 = 1$

upto (round(n/2)+1) terms/stages.

4.5.3 Fault-Tolerance and Routing

The proposed M_QUAD is having the following properties

Lemma 1 : If the faults occuring are such that they effect any number of SEs in the normal subnetwork of M_QUAD, there exists atleast one path from each source to every destination through the fault-tolerant subnetwork (i.e. F_QUAD) of the designed MIN.

Let the packet has to get routed from source S_{10} to destination D_0. Under fault-free scenario, the path adopted by the packet is

$$S_{10} \rightarrow SE1,6 \rightarrow SE2,3 \rightarrow SE4,3 \rightarrow SE5,5 \rightarrow D_0.$$

Suppose the SEs SE4,3, SE5,5 and also SE2,1 become faulty. The path adopted by the packet under this faulty scenario becomes

$$S_{10} \rightarrow SE1,6 \rightarrow SE2,3 \rightarrow SE2,1 \rightarrow SE4,1 \rightarrow SE5,1 \rightarrow D_0$$

Lemma 2 : The designed MIN can sustain two faulty SEs in any single loop in the intermediate stages. However, in case of first stage, the designed MIN can tolerate the faults in those two SEs in a loop which are connected to different sources. Multiple occurences of this type of, pertaining to the same stage, are tolerable.

Let the packet has to get routed from source S0 to destination D6. Suppose the SEs SE3,1 and SE3,2 become faulty. In the absence of any fault, the route woule have been as under as the routing tag is 0111100.

$$S_0 \rightarrow SE1,1 \rightarrow SE3,1 \rightarrow SE4,2 \rightarrow SE5,4 \rightarrow D_6$$

But due to faults in third stage loop, the path adopted by the packet becomes

$$S_0 \rightarrow SE1,1 \rightarrow SE2,1 \rightarrow FT2,1 \rightarrow FT3,1 \rightarrow FT4,2 \rightarrow FT5,4 \rightarrow D_6$$

Lemma 3 : If the faults occuring in M_QUAD are such that they effect two conjugate SEs (out of three) in the final/last stage, there exists atleast one path from each source to every destination of the network.

Let the packet has to go from source S0 to destination D0. Suppose SEs SE5,1 and FT5,1 of final (fifth) stage become faulty. In case of no faults, the path would have been

$$S_0 \rightarrow SE5,1 \rightarrow D_0$$

But now the packet takes the route

$$S_0 \rightarrow SE1,1 \rightarrow FT1,1 \rightarrow SE1,5 \rightarrow SE5,5 \rightarrow D_0$$

The primary routes from various sources to their favorite and non-favorite destinations for M_QUAD have been summarized in Tables A2.5(a) and A2.5(b) respectively.
The secondary routes have been tabulated in A2.5(c). The Tables A2.5(a) to A2.5(c) are in Annexure 2.

4.6 Analysis of M_QUAD

In this section, first of all, the proposed M_QUAD has been analyzed for the probability of availability of packet at the output and auxiliary port of each SE under fault-free as well as faulty scenarios. Then probability analysis has been used subsequently for the evaluation of probability of acceptance and bandwidth, again for faulty-free and faulty scenarios. This probability analysis also leads to the evaluation of average queue length in each SE and hence the optimal buffer requirement to avoid packet discarding. Thereafter, terminal reliability has been evaluated for favorite as well as for non-favorite destinations followed by cost evaluation.
The assumptions being considered in the analysis are exactly the same that have been discussed in section 3.3 of Chapter 3. The notations being used for performing *probability of acceptance* and *bandwidth* evaluation are identical to that discussed in section 3.3.

4.6.1 Probability of Packet Availability at ports

The set of equations for evaluating the probability of a packet being present at the auxiliary, input and output ports of various SEs in different stages are summarized in Tables A2.6(a) to A2.6(l) in Annexure 2. The probability values for the availability of packet at the output and auxiliary output port of SEs have been presented in the Tables 4.17(a)-4.17(c).

Table 4.17(a)

Prob. of packet availability at O/Ports of SEs corresponding to packet generation rate of 0.5

SE#	P_{out}	$P_{aux\ i}$	SE#	P_{out}	$P_{aux\ i}$	SE#	P_{out}	$P_{aux\ i}$	SE#	P_{out}	$P_{aux\ i}$	SE#	P_{out}
SE1,1	0.472	0.125	SE2,	0.445	0.097				SE4,	0.409	0.076	SE5,	0.392
SE1,2	0.472	0.125				SE3,	0.420	0.081				SE5,	0.392
SE1,3	0.472	0.125	SE2,	0.445	0.097				SE4,	0.409	0.076	SE5,	0.392
SE1,4	0.472	0.125										SE5,	0.392
SE1,5	0.437	0.000	SE2,	0.393	0.012				SE4,	0.352	0.030	SE5,	0.356
SE1,6	0.437	0.000				SE3,	0.363	0.025				SE5,	0.356
SE1,7	0.437	0.000	SE2,	0.393	0.012				SE4,	0.352	0.030	SE5,	0.356
SE1,8	0.437	0.000										SE5,	0.356
FT1,1	0.085	0.171	FT2,	0.151	0.151				FT4,	0.216	0.117	FT5,	0.146
FT1,2	0.085	0.171				FT3,	0.199	0.125				FT5,	0.146
FT1,3	0.085	0.171	FT2,	0.151	0.151				FT4,	0.216	0.117	FT5,	0.146
FT1,4	0.085	0.171										FT5,	0.146

Table 4.17(b)

Prob. of packet availability at O/Ports of SEs corresponding to packet generation rate of 0.8 (M_QUAD)

SE#	P_{out}	$P_{aux\ in}$	SE#	P_{out}	$P_{aux\ in}$	SE#	P_{out}	$P_{aux\ in}$	SE#	P_{out}	$P_{aux\ in}$	SE#	P_{out}
SE1,1	0.6976	0.3200	SE2,1	0.6219	0.2170				SE4,1	0.5486	0.1704	SE5,1	0.5274
SE1,2	0.6976	0.3200				SE3,1	0.5679	0.1795				SE5,2	0.5274
SE1,3	0.6976	0.3200	SE2,2	0.6219	0.2170				SE4,2	0.5486	0.1704	SE5,3	0.5274
SE1,4	0.6976	0.3200										SE5,4	0.5274
SE1,5	0.6400	0.0000	SE2,3	0.5558	0.0788				SE4,3	0.4962	0.1276	SE5,5	0.4887
SE1,6	0.6400	0.0000				SE3,2	0.5096	0.1188				SE5,6	0.4887
SE1,7	0.6400	0.0000	SE2,4	0.5558	0.0788				SE4,4	0.4962	0.1276	SE5,7	0.4887
SE1,8	0.6400	0.0000										SE5,8	0.4887
FT1,1	0.2368	0.4736	FT2,1	0.3535	0.3364				FT4,1	0.4229	0.2363	FT5,1	0.3048
FT1,2	0.2368	0.3200				FT3,1	0.0.4102	0.2596				FT5,2	0.3048
FT1,3	0.2368	0.3200	FT2,2	0.3535	0.3364				FT4,2	0.4229	0.2363	FT5,3	0.3048
FT1,4	0.2368	0.3200										FT5,4	0.3048

Table 4.17(c)

Prob. of packet availability at O/Ports of SEs corresponding to packet generation rate of 1.0 (M_QUAD)

SE#	P_{out}	$P_{aux\ in}$	SE#	P_{out}	$P_{aux\ in}$	SE#	P_{out}	$P_{aux\ in}$	SE#	P_{out}	$P_{aux\ in}$	SE#	P_{out}
SE1,1	0.8125	0.5000	SE2,1	0.7028	0.3142				SE4,1	0.6113	0.2453	SE5,1	0.5877
SE1,2	0.8125	0.5000				SE3,1	0.6340	0.2597				SE5,2	0.5877
SE1,3	0.8125	0.5000	SE2,2	0.7028	0.3142				SE4,2	0.6113	0.2453	SE5,3	0.5877
SE1,4	0.8125	0.5000										SE5,4	0.5877
SE1,5	0.7500	0.0000	SE2,3	0.6428	0.1709				SE4,3	0.5728	0.2159	SE5,5	0.5540
SE1,6	0.7500	0.0000				SE3,2	0.5887	0.2136				SE5,6	0.5540
SE1,7	0.7500	0.0000	SE2,4	0.6428	0.1709				SE4,4	0.5728	0.2159	SE5,7	0.5540
SE1,8	0.7500	0.0000										SE5,8	0.5540
FT1,1	0.3750	0.7500	FT2,1	0.4936	0.4658				FT4,1	0.5314	0.3077	FT5,1	0.4034
FT1,2	0.3750	0.7500				FT3,1	0.5294	0.3412				FT5,2	0.4034
FT1,3	0.3750	0.7500	FT2,2	0.4936	0.4658				FT4,2	0.5314	0.3077	FT5,3	0.4034
FT1,4	0.3750	0.7500										FT5,4	0.4034

4.6.2 Probability of acceptance and Bandwidth

Probability of acceptance, as defined in chapter 1, is the ratio of the average number of requests accepted by the destination to the average number of requests submitted by the sources per network cycle and bandwidth is defined as the average number of requests accepted per network cycle.

Table 4.18(a)
Probability of acceptance and Bandwidth values under fault-free conditions

Packet generation rate	Bandwidth	Probability of acceptance	Packet generation rate	Bandwidth	Probability of acceptance
0.1	1.5622	0.9764	0.6	8.3899	0.8739
0.2	3.0566	0.9552	0.7	9.5261	0.8505
0.3	4.4901	0.9354	0.8	10.5677	0.8256
0.4	5.8621	0.9160	0.9	11.5123	0.7995
0.5	7.1654	0.8957	1.0	12.3610	0.7726

Table 4.18(b)
Prob. of acceptance and Bandwidth for any single SE fault in any loop in first stage

Packet Generation Rate	Bandwidth	Probability of acceptance	Packet Generation Rate	Bandwidth	Probability of acceptance
0.1	1.5703	0.9814	0.6	8.3680	0.8717
0.2	3.0812	0.9629	0.7	9.4459	0.8434
0.3	4.5275	0.9432	0.8	10.4135	0.8136
0.4	5.8990	0.9217	0.9	11.2721	0.7828
0.5	7.1830	0.8979	1.0	12.0268	0.7517

Table 4.18(c)
Probability of acceptance and Bandwidth values when only fault-tolerant subnetwork survives

Packet Generation Rate	Bandwidth	Probability of acceptance	Packet Generation Rate	Bandwidth	Probability of acceptance
0.1	0.7821	0.4888	0.6	4.3789	0.4561
0.2	1.5352	0.4797	0.7	5.0609	0.4519
0.3	2.2672	0.4723	0.8	5.7327	0.4479
0.4	2.9832	0.4661	0.9	6.3934	0.4440
0.5	3.6865	0.4608	1.0	7.0421	0.4401

The results in the Tables 4.18(a) to 4.18(c) reveal that the probability of acceptance and bandwidth values have only a slight degradation in their values under faulty scenarios. This shows the efficiency of M_FDOT under faulty scenarios.

4.6.3 Average queue length and optimal buffer requirement

The following Table 4.19 presents the evaluated queue length of packets and optimal buffer requirement at the output ports and auxiliary input port of each SE at every stage. The formula that has been used for evaluation of average queue length is that of M/M/1 queuing model i.e. average queue length = $\frac{\lambda}{\mu}\frac{\lambda}{(\mu-\lambda)}$ where λ is the mean arrival rate and μ is the mean service rate. For each SE, $\lambda = P_{out}$ and P_{out} is the probability of a packet being present at the output port of SEs in the previous stage and $\mu = 1$. The packet generation rate has been taken 1.0 that corresponds to maximum traffic and hence the above Table gives the buffer requirements of SE ports under maximum traffic scenario.

4.6.4 Terminal Reliability

Terminal Reliability is the probability that a given source-destination pair has at least one fault-free path between them, given that each SE has a certain reliability (the reliability of a SE is the probability that it is fault-free).

The redundancy graph for favorite destinations is shown in Figure 4.6

Table 4.19
Optimal Buffer Requirement for M_QUAD

SE#	Average Queue Length at each of the Output Port	Minimum Number of buffers at each of the Output Port	Average Queue Length at the auxiliary port	Minimum Number of buffers required at the auxiliary port	SE#	Average Queue Length at each of the Output Port	Minimum Number of buffers at each of the Output Port	Average Queue Length at the auxiliary Input port	Minimum Number of buffers required at the auxiliary Port
SE1,1	3.5211	4	0.5000	1	FT3,1	0.5956	1	-	-
SE1,2	3.5211	4	0.5000	1	SE4,1	0.9614	1	0.0798	1
SE1,3	3.5211	4	0.5000	1	SE4,2	0.9614	1	0.0798	1
SE1,4	3.5211	4	0.5000	1	SE4,3	0.7680	1	0.0594	1
SE1,5	2.25	3	0.0000	0	SE4,4	0.7680	1	0.0594	1
SE1,6	2.25	3	0.0000	0	FT4,1	0.6027	1	0.1368	1
SE1,7	2.25	3	0.0000	0	FT4,2	0.6027	1	0.1368	1
SE1,8	2.25	3	0.0000	0	SE5,1	0.8377	1	-	-
FT1,1	0.2250	1	2.2500	3	SE5,2	0.8377	1	-	-
FT1,2	0.2250	1	2.2500	3	SE5,3	0.8377	1	-	-
FT1,3	0.2250	1	2.2500	3	SE5,4	0.8377	1	-	-
FT1,4	0.2250	1	2.2500	3	SE5,5	0.6881	1	-	-
SE2,1	1.6618	2	0.1439	1	SE5,6	0.6881	1	-	-
SE2,2	1.6618	2	0.1439	1	SE5,7	0.6881	1	-	-
SE2,3	1.1568	2	0.0350	1	SE5,8	0.6881	1	-	-
SE2,4	1.1568	2	0.0350	1	FT5,1	0.2727	1	-	-
FT2,1	0.4810	1	0.4062	1	FT5,2	0.2727	1	-	-
FT2,2	0.4810	1	0.4062	1	FT5,3	0.2727	1	-	-
SE3,1	1.0984	2	-		FT5,4	0.2727	1	-	-
SE3,2	0.8427	1	-						

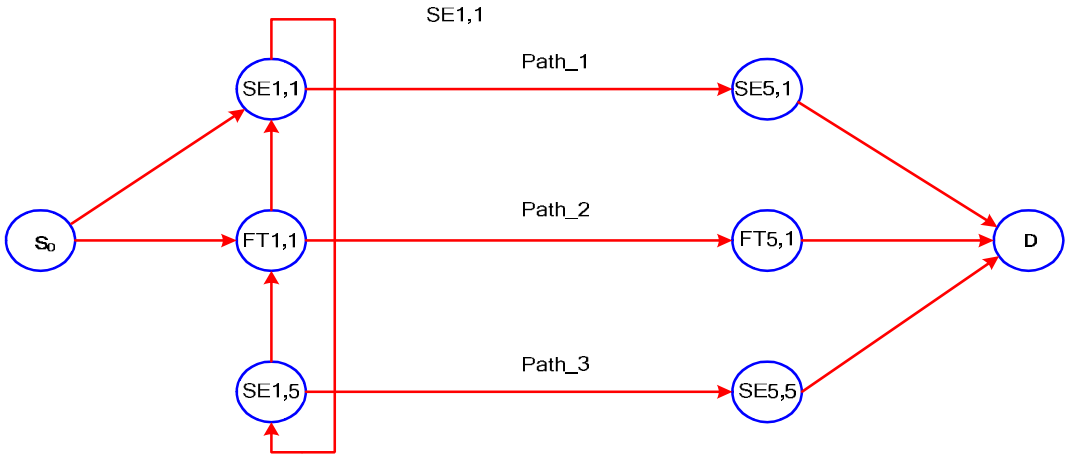

Figure 4.6 : Redundancy Graph for Modified Quad Tree (Favorite Destinations)

The probability that

Path_1 fails = $1 - r^2$

Path_2 fails = $1 - r^2$

Path_3 fails = $1 - r^2$

Probability that the three paths fail = $(1 - r^2)^3$

Probability that, atleast, one of the three paths survives (i.e. fault free) is

$R_{term} = [1 - (1-r^2)^3]$

The terminal reliabilities of M_QUAD (for favorite destinations) for various values of SE reliabilities are given in Table 4.20(a).

Table 4.20(a)
Terminal Reliabilities of M_QUAD Network (for favorite destinations)

SE Reliability	Terminal Reliability
0.90	0.9931
0.92	0.9964
0.94	0.9984
0.96	0.9995

The redundancy graph for non-favorite destinations is shown below :

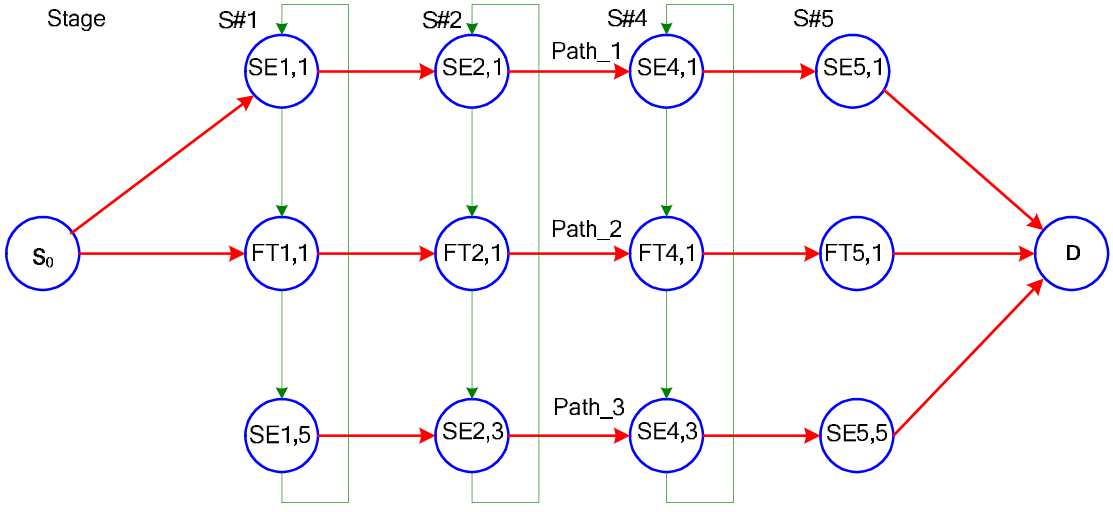

Figure 4.7(a) : Redundancy Graph for M_QUAD for non-favorite Destinations (path length 4)

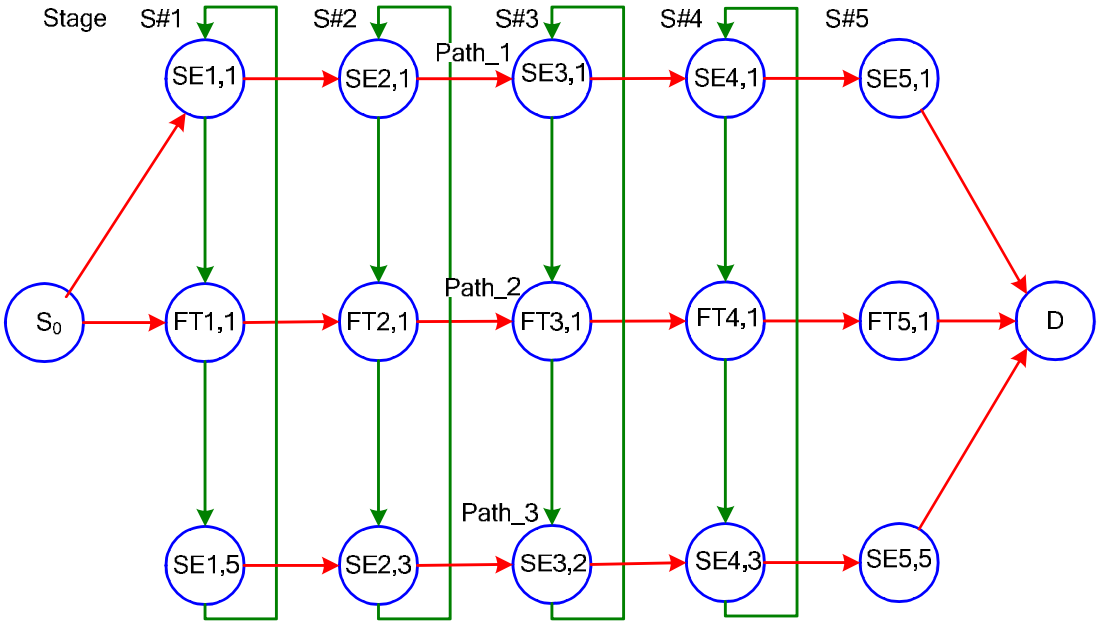

Figure 4.7(b) : Redundancy Graph for M_QUAD for non-favorite Destinations (path length 5)

For stage S#1, probability that atleast one out of three : SE1,1; FT1,1 and SE1,5 survives is

$$R_{S\#1} = \left[1 - (1-r)^3\right]$$

In stage S#2, probability that atleast one of the three : SE2,1; FT2,1 and SE2,3 survives is

$$R_{S\#2} = \left[1 - (1- r)^3\right]$$

In stage S#3, probability that atleast one of the three : SE3,1; SE3,2 and FT3,1 comprising of loop survives is

$$R_{S\#3} = \left[1 - (1- r)^3\right]$$

In stage S#4, probability that atleast one of the three SEs – SE4,1; FT4,1 and SE4,3 survives is

$$R_{S\#4} = \left[1 - (1- r)^3\right]$$

Terminal Reliability for non-favorite destinations having path length four is

$$R_{S\#1} \times R_{S\#2} \times R_{S\#4} \times r$$

Terminal Reliability for non-favorite destinations having path length five is

$$R_{S\#1} \times R_{S\#2} \times R_{S\#3} \times R_{S\#4} \times r$$

The terminal reliabilities of M_QUAD for various values of SE reliabilities are given below in Table 4.20(b)

Table 4.20(b)
Terminal Reliabilities of M_QUAD Network (for non-favorite destinations)

SE Reliability	Terminal Reliability	
	Path length 4	Path length 5
0.90	0.8973	0.8964
0.92	0.9186	0.9182
0.94	0.9394	0.9392
0.96	0.9597	0.9598

The terminal reliability values when compared with the corresponding SE reliability values reveal that these values are almost comparable. Hence the proposed design is worthwhile considering the terminal reliability aspect.

4.6.5 Hardware Complexity and Cost

To estimate the cost of a network, one common method is to calculate the switch complexity with an assumption that the cost of a switch is proportional to the number of gates involved. For example, a 2×2 SE has 4 units of cost and a 3×3 SE has 9 units of cost. For multiplexers and de-multiplexers, we roughly assume that each of k×1 and 1×k has k units of cost.

Total number of stages = (2m-1) where $m=\log_2 N/2$

Total number of SEs = $(2^{m+2}-6) + (2^{m+2}-6)/2$

Link Complexity

Number of inter-stage links = $$\sum_{i=1}^{round(n/2)} \left(\frac{N}{2^i} * 2 + \frac{N}{2^{i+1}} * 2 \right) + \sum_{i=2}^{n/2} \left(\frac{N}{2^i} * 2 + \frac{N}{2^{i+1}} * 2 \right)$$

The term in the first bracelet in the above expression corresponds to the number of inter-stage links existing between first stage and stage (round (n/2) + 1). The

term in the second bracket corresponds to the number of SEs between stage (round(n/2) +1) and n^{th} stage.

Number of Intra-stage links = $\left[\left(2^{m+2}-6\right)+\left(\frac{2^{m+2}-6}{2}\right)-\left(\frac{N}{2}+\frac{N}{4}\right)\right]$

The first term in the above expression corresponds to the number of SEs in the N_QUAD of M_QUAD. The second term corresponds to the number of SEs in the F_QUAD of M_QUAD. Since there are no auxiliary links in the last/final stage (stage closest to outputs), the number of SEs in the last stage are being subtracted as the third term.

No. of SEs in the last stage = N/2 + N/4

Cost of SEs in the last stage = 4 * (N/2 + N/4)

Total cost of SEs = $9 * (2^{m+2}-6) + 9*(2^{m+2}-6)/2 – 9*(N/2 + N/4) + 4*(N/2+N/4)$

$= 9 * (2^{m+2}-6) * (1 + ½) – 5 * (N/2 + N/4)$

Total number of multiplexers = 2*N/4

Total number of demultiplexers = 2*(N/2 + N/4)

Total number of multiplexers and demultiplexers = 2*(N/4+N/2+N/4)

= 2*N

Cost of MUX's and DEMUX's = 2*2*N

Total cost of M_QUAD Tree Network = $9*(2^{m+2}-6)*(1+½)–5*(N/2+N/4)+2*2*N$

The cost of the various size M_QUAD has been evaluated and presented in Table 4.27.

Tahle 4.27
Cost of various sized M_QUAD

Size of MIN	Cost
16 × 16	355
64 × 64	1663
256 × 256	6895
512 × 512	13871
1024 × 1024	27823

4.7 Permutation Capability of MINs

A permutation for a network is pairing of its sources and destinations such that each source appears in exactly one pair and each destination appears also in exactly one pair. In other words, a permutation is a full one-to-one mapping between the network sources and destinations.

In the following tables

S denotes the source

D denotes the destination

and i and j are integral variables.

Corresponding to each of the eight source-destination set in Subtable I, there are eight source-destination sets possible from Subtable II leading to 64 permutations corresponding to each table from A2.7(a) to A2.7(p). As such, in all there all 1024 permutations passable in M_FDOT and Hybrid Networks. In case of M_QUAD Network, permutations corresponding to Tables A2.7(a) to A2.7(h) and Tables A2.7(m) to A2.7(p) are realizable. As such, permutations realizable in case of M_QUAD are 768.

The results of permutations passable feature are summarized below

Table 4.22

MIN	Permutations Passable
M_FDOT	1024
Hybrid	1024
M_QUAD	768

From the above Table, it is clear that as far as permutations passable aspect, M_FDOT and Hybrid are better. A very prominent feature of the proposed networks is that in case of non-critical SE faults, the permutations passable remain unaffected. Even in case of single SE fault in every loop in first stage, the permutations passable feature remains unaffected whereas in case of existing MINs, 50% of permutations are lost.

4.8 Conclusions

In this chapter, three new irregular MINs have been designed, analysed and proposed namely M_FDOT, Hybrid and M_QUAD and analyzed for their performance. The design includes the construction of the MIN, routing algorithm and fault-tolerance analysis. For each proposed design, probability analysis for packet traffic has been carried out for SEs of all stages resulting in the evaluation of probability of acceptance, bandwidth, average queue length and optimal buffer requirement under fault-free and faulty scenarios. The other performance parameters that have been evaluated for the proposed MINs are – terminal reliability, cost and permutations passable. The packet traffic distribution that has been tabulated corresponds to packet generation rate of 0.5, 0.8 and 1.0 under fault-free and faulty scenarios. The M/M/1 Queueing Model along with the results of packet traffic distribution leads to the evaluation of average queue length and hence optimal buffer requirement. The probability of acceptance values in the proposed MINs namely : M_FDOT, Hybrid and M_QUAD corresponding to packet generation rate of 1.0 are 0.7780, 0.7630 and 0.7726 which are higher than the existing MINs of similar type. The bandwidth for the proposed MINs again for maximum packet generation rate which has been evaluated as 12.4480, 12.2076 and 12.3610 are again better than the existing MINs. Regarding fault-tolerance, each of the proposed MIN can maintain all the permutations during fault-free and non-critical fault scenarios.

Comparing the performance results of M_FDOT, Hybrid and M_QUAD, it has been found that M_FDOT has higher values for probability of acceptance and bandwidth followed by M_QUAD and then Hybrid MIN. Considering terminal reliability feature, M_QUAD is having the largest value, followed by Hybrid MIN and then M_FDOT. Considering permutations passable feature, M_FDOT and Hybrid are equally and then comes M_QUAD.

For small sized networks, the proposed Hybrid MIN is better but for larger sized networks M_FDOT and M_QUAD perform better.

The next chapter discusses the "Comparative analysis of the proposed MINs". The performance of the proposed MINs have been compared with the existing MINs of similar type.

Chapter 5

Comparative Analysis of the Proposed MINs

The software programs were initially developed for the existing MINs to evaluate their performance in terms of PA and BW. Software has been developed in 'C' language. The evaluated performance parameters were compared with the existing data available in the literature (under identical conditions of input rate and failure rate) to validate the correctness of the programs. The existing MINs were analyzed in detail for their performances by means of developed software programs. Thereafter, the program was modified as per the architecture of each designed MIN and simulation was carried out to evaluate the values for the performance parameters – probability of acceptance and bandwidth corresponding to different packet generation rates (i.e. input rates) for fault-free as well as under different fault-rate scenarios. The programs are architectural dependent and each of the designed MIN has its own software program.

In this chapter, the performances of the proposed MINs – M_ASEN, M_FDOT, Hybrid, M_QUAD have been compared with the existing networks of similar type and have also been compared among themselves. The performance of M_ASEN has been compared with the existing regular, fault-tolerant dynamic networks. The performances of the proposed irregular, fault-tolerant dynamic MINs namely M_FDOT, Hybrid and M_QUAD have been compared with the existing irregular MINs.

5.1 Comparative Analysis of Performance Parameters of Proposed MINs

The parameters that have been considered for performance comparison are probability of acceptance, bandwidth, fault-tolerance, reliability, permutations passable, path length and cost.

5.1.1 Probability of acceptance

For the purpose of comparative study, the probability of acceptance parameter values have been evaluated and given in tables 5.1(a) to 5.1(e). In table 5.1(a) , the proposed M_ASEN has been compared for probability of acceptance parameters with the existing networks of similar type corresponding to packet generation rate 1.0 under fault-free conditions. In table 5.1(b), M_ASEN has been compared with the existing ASEN-2 and ASEN-MAX i.e ASEN-4 for various packet generation rates under fault-free scenario. Table 5.1(c) corresponds to the case when there occurs a loop fault in the first stage. In Tables 5.1(d) and 5.1(e), the proposed irregular MINs i.e. M_FDOT, Hybrid and M_QUAD have been compared with the existing networks - QUAD, ALN and PHN for fault-free and single SE fault (in first stage) scenarios respectively. In order to clarify, the graphs have also been plotted and shown in Figures 5.1(a) to 5.1(d).

Table 5.1(a)
Probability of acceptance comparison with existing Regular MINs (pkt generation rate 1.0)

MIN	Probability of acceptance
M_ASEN	0.7811
ASEN-2	0.5812
ASEN-MAX (ASEN-4)	0.6000
INDRA	0.539
Modified Omega	0.597
Delta	0.450
Crossbar	0.644

Table 5.1(b)
Probability of acceptance comparison with ASEN-2 and ASEN-MAX (ASEN-4)

Packet Generation Rate (P_{pkt_gen})	M_ASEN	ASEN-2	ASEN-MAX (ASEN-4)
0.1	0.9793	0.9704	0.9726
0.2	0.9603	0.9331	0.9407
0.3	0.9422	0.8906	0.9045
0.4	0.9239	0.8448	0.8646
0.5	0.9047	0.7978	0.8217
0.6	0.8839	0.7509	0.7768
0.7	0.8610	0.7051	0.7312
0.8	0.8361	0.6614	0.6859
0.9	0.8094	0.6199	0.6418
1.0	0.7811	0.5812	0.5998

Table 5.1(c)
Probability of acceptance comparison for regular MINs for single loop fault

Packet Generation Rate (P_{pkt_gen})	M_ASEN	ASEN-2	ASEN-MAX (ASEN-4)
0.1	0.9873	0.9553	0.9462
0.2	0.9729	0.9005	0.8841
0.3	0.9556	0.8414	0.8153
0.4	0.9347	0.7817	0.7436
0.5	0.9099	0.7242	0.6733
0.6	0.8814	0.6702	0.6074
0.7	0.8497	0.6203	0.5476
0.8	0.8156	0.5749	0.4942
0.9	0.7798	0.5337	0.4466
1.0	0.7534	0.4996	0.4040

Table 5.1(d)
Probability of acceptance comparison for fault-free Irregular MINs

Packet Generation Rate (P_{pkt_gen})	M_FDOT	Hybrid	M_QUAD	QUAD	ALN	PHN
0.1	0.9762	0.9766	0.9764	0.9698	0.6123	0.5431
0.2	0.9547	0.9557	0.9552	0.9313	0.5247	0.4798
0.3	0.9347	0.9357	0.9354	0.8873	0.4607	0.4302
0.4	0.9153	0.9155	0.9160	0.8408	0.4114	0.3904
0.5	0.8955	0.8942	0.8957	0.7938	0.3728	0.3578
0.6	0.8747	0.8712	0.8739	0.7477	0.3415	0.3307
0.7	0.8525	0.8465	0.8505	0.7037	0.3158	0.3077
0.8	0.8289	0.8200	0.8256	0.6621	0.2940	0.2879
0.9	0.8039	0.7920	0.7995	0.6230	0.2753	0.2706
1.0	0.7780	0.7630	0.7726	0.5865	0.2590	0.2552

Table 5.1(e)
Probability of acceptance comparison of Irregular MINs for single SE fault

Packet Generation Rate (P_{pkt_gen})	M_FDOT	Hybrid	M_QUAD	QUAD
0.1	0.98	0.98	0.98	0.96
0.2	0.96	0.96	0.96	0.91
0.3	0.94	0.94	0.94	0.86
0.4	0.92	0.92	0.92	0.82
0.5	0.89	0.89	0.90	0.76
0.6	0.87	0.86	0.87	0.71
0.7	0.84	0.83	0.84	0.67
0.8	0.81	0.80	0.81	0.63
0.9	0.79	0.77	0.78	0.59
1.0	0.76	0.74	0.75	0.55

In the tables 5.1(a)-5.1(e), probability of acceptance values have been presented for the proposed as well as for the existing MINs of similar type for various packet generation rates. It is evident from these tables that under fault-free as well as under faulty scenarios, probability of acceptance values for the proposed MINs are higher than the existing networks for all values of packet generation rates. This comparison has been shown graphically in Figures 5.1(a) to 5.1(d).

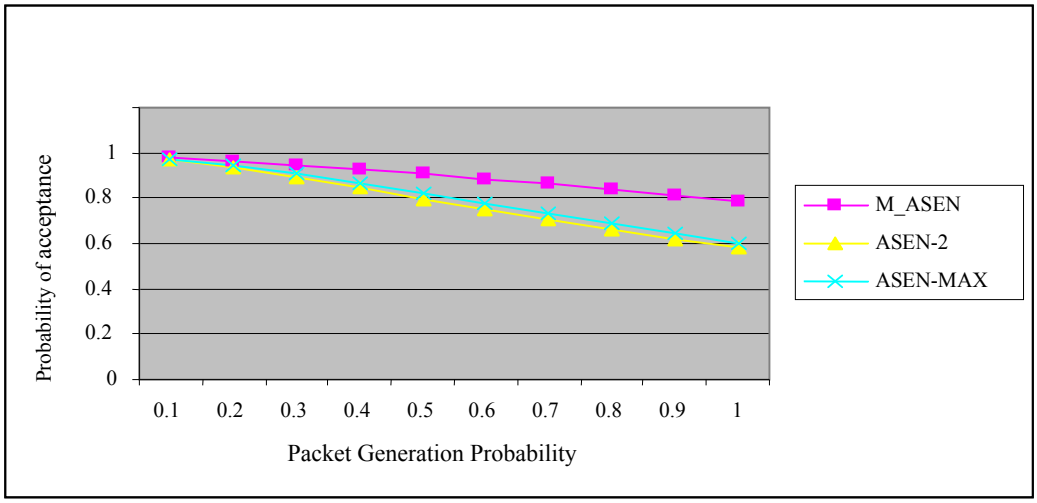

Figure 5.1(a) : Probability of acceptance comparison of M_ASEN with ASEN-2 & ASEN-MAX (ASEN-4)

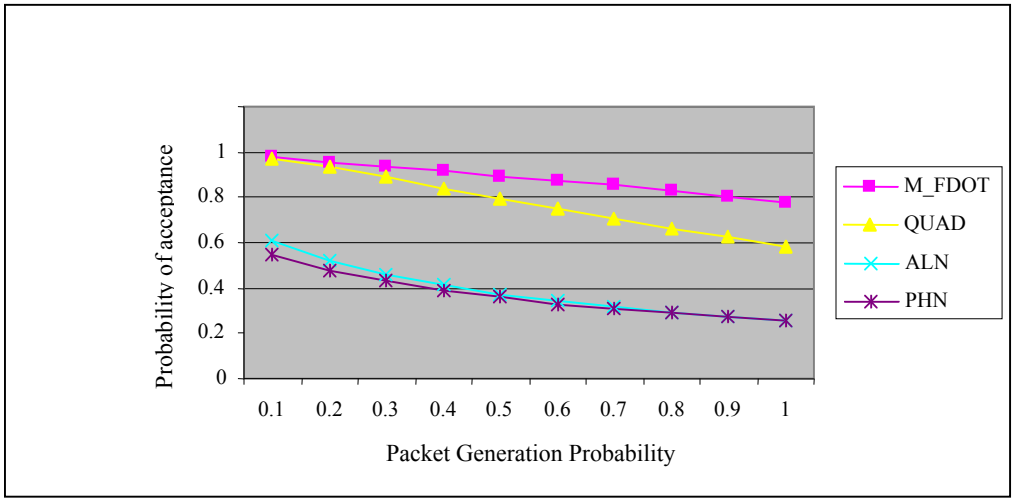

Figure 5.1(b) : Probability of acceptance comparison of M_FDOTwith QUAD, ALN and PHN Networks

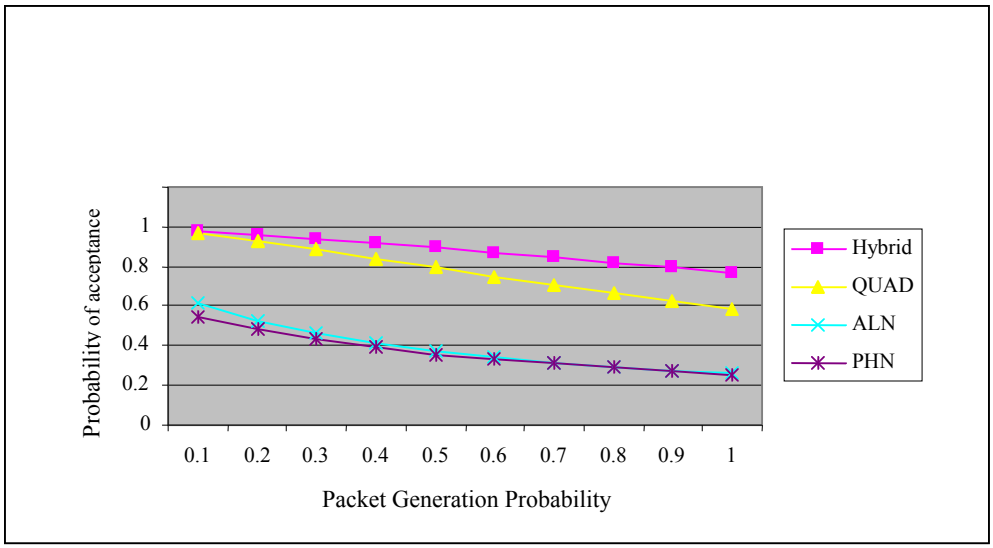

Figure 5.1(c) **:** Probability of acceptance comparison of Hybrid with QUAD, ALN and PHN Networks

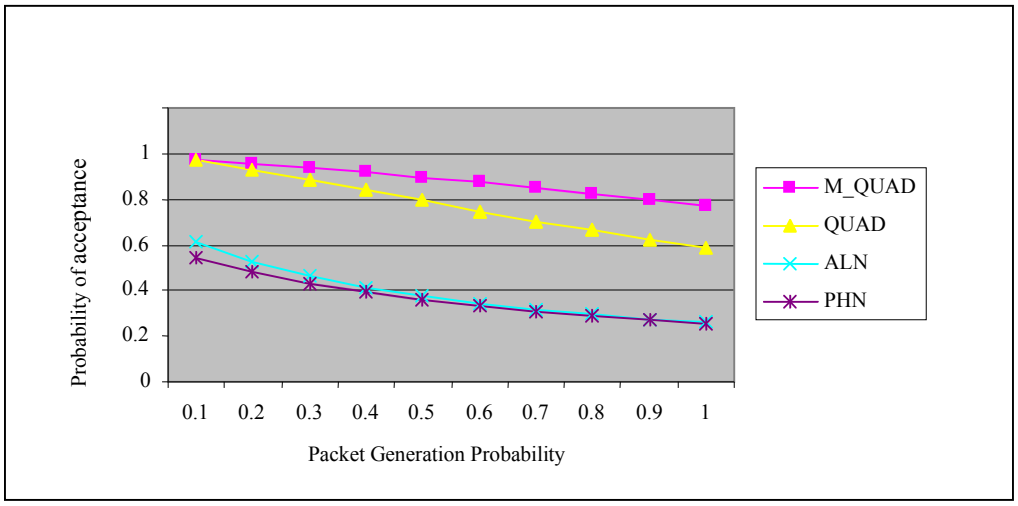

Figure 5.1(d) : Probability of acceptance comparison of M_QUAD with QUAD, ALN and PHN Networks

5.1.2 Bandwidth

Bandwidth of the MIN is defined as the average number of requests accepted per network cycle [76]. For evaluating the proposed MINs, the bandwidth parameter values have been presented in tables 5.2(a) to 5.2(e). In table 5.2(b), M_ASEN has been compared for this performance parameter with existing ASEN-2 and ASEN-MAX for different packet generation rates under fault-free scenario. Table 5.2(c) corresponds to the case when there occurs a loop fault in the first stage. In Table 5.2(d), the proposed irregular MINs i.e. M_FDOT, Hybrid and M_QUAD have been compared with the

existing QUAD Tree Network for fault-free and single SE fault (in first stage) scenarios respectively. In Table 5.2(e)

Table 5.2(a) : Bandwidth - Fault-free Regular MINs

Packet Generation Rate (P_{pkt_gen})	M_ASEN	ASEN-2	ASEN-MAX
0.1	1.5668	1.5526	1.5562
0.2	3.0729	2.9860	3.0101
0.3	4.5223	4.2746	4.3416
0.4	5.9131	5.4069	5.5333
0.5	7.2377	6.3823	6.5733
0.6	8.4851	7.2083	7.4574
0.7	9.6435	7.8976	8.1891
0.8	10.7025	8.4653	8.7791
0.9	11.6549	8.9272	9.2425
1.0	12.4976	9.2986	9.5970

Table 5.2(b) : Bandwidth - Single loop fault in first stage of Regular MINs

Packet Generation Rate (P_{pkt_gen})	M_ASEN	ASEN-2	ASEN-MAX
0.1	1.5796	1.5284	1.5139
0.2	3.1133	2.8817	2.8293
0.3	4.5871	4.0385	3.9134
0.4	5.9823	5.0031	4.7589
0.5	7.2794	5.7935	5.3862
0.6	8.4615	6.4336	5.8315
0.7	9.5167	6.9478	6.1334
0.8	10.4393	7.3587	6.3252
0.9	11.2297	7.6857	6.4308
1.0	11.8936	7.9450	6.4644

Table 5.2(c) : Bandwidth - Fault-free Irregular MINs

Packet Generation Rate (P_{pkt_gen})	M_FDOT	Hybrid	M_QUAD	QUAD	ALN	PHN
0.1	1.5620	1.5626	1.5622	1.5517	0.9798	0.8690
0.2	3.0551	3.0581	3.0566	2.9801	1.6792	1.5356
0.3	4.4866	4.4912	4.4901	4.2592	2.2118	2.0650
0.4	5.8579	5.8590	5.8621	5.3810	2.6332	2.4984
0.5	7.1642	7.1533	7.1654	6.3500	2.9826	2.8626
0.6	8.3973	8.3638	8.3899	7.1784	3.2792	3.1752
0.7	9.5482	9.4805	9.5261	7.8813	2.5374	3.4470
0.8	10.6094	10.4985	10.5677	8.4743	3.7644	3.6856
0.9	11.5764	11.4051	11.5123	8.9714	3.9654	3.8970
1.0	12.4480	12.2076	12.3610	9.3847	4.1440	4.0836

Table 5.2(d) : Bandwidth - Single SE fault in first stage of Irregular MINs

Packet Generation Rate (P_{pkt_gen})	M_FDOT	Hybrid	M_QUAD	QUAD
0.1	1.5665	1.5714	1.5703	1.5342
0.2	3.0659	3.0800	3.0812	2.9189
0.3	4.4962	4.5147	4.5275	4.1391
0.4	5.8525	5.8638	5.8990	5.1943
0.5	7.1285	7.1169	7.1830	6.0941
0.6	8.3177	8.2663	8.3680	6.8529
0.7	9.4147	9.3079	9.4459	7.4868
0.8	10.4162	10.2408	10.4135	8.0108
0.9	11.3210	11.0670	11.2721	8.4378
1.0	12.1303	11.7903	12.0268	8.7790

From the results presented in tables 5.1(a)–5.1(e) and 5.2(a)–5.2(d), it has been observed that probability of acceptance and bandwidth values are higher in faulty scenarios upto packet generation rate of 0.5. But for packet generation rates more than 0.5, probability of acceptance and bandwidth values are comparable.

This comparison has been shown graphically in the Figures 5.2(a) to 5.2(d).

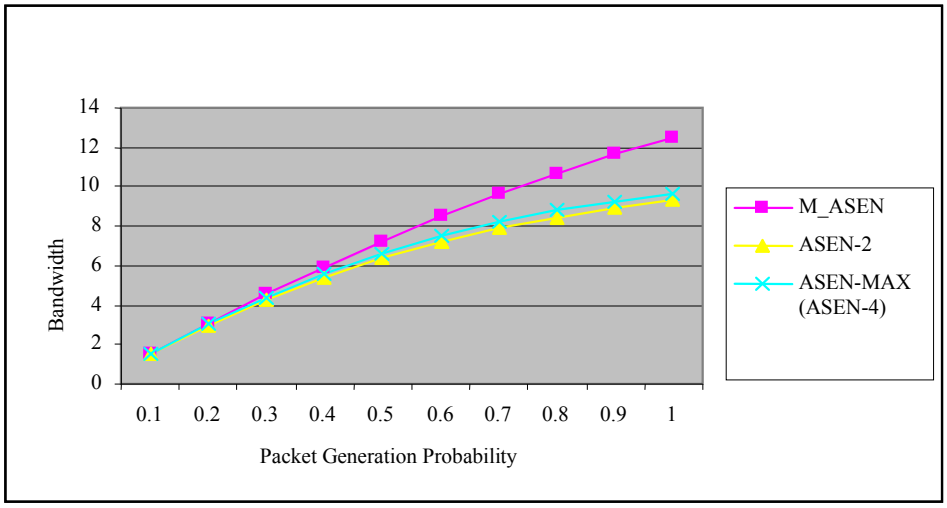

Figure 5.2(a) : Bandwidth comparison of M_ASEN with ASEN-2 & ASEN-MAX (ASEN-4)

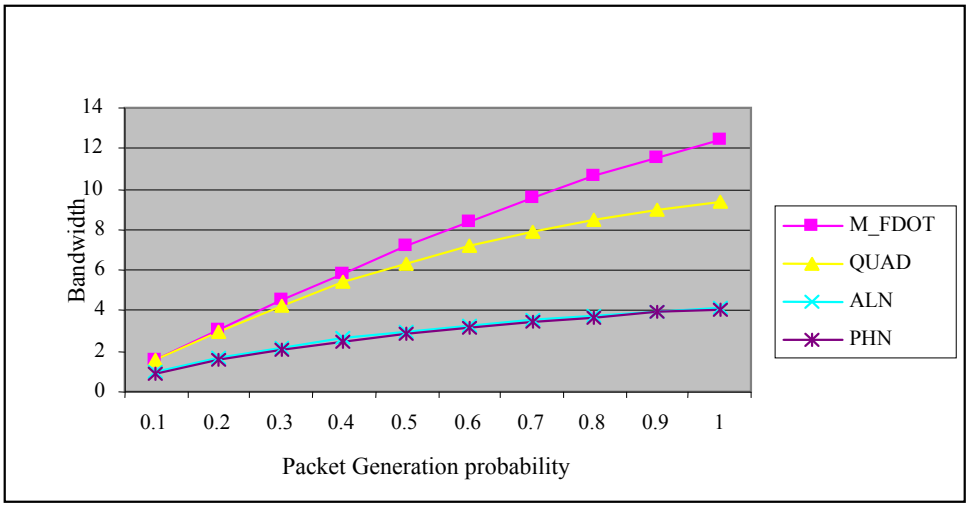

Figure 5.2(b) : Bandwidth comparison of M_FDOTwith QUAD, ALN and PHN Networks

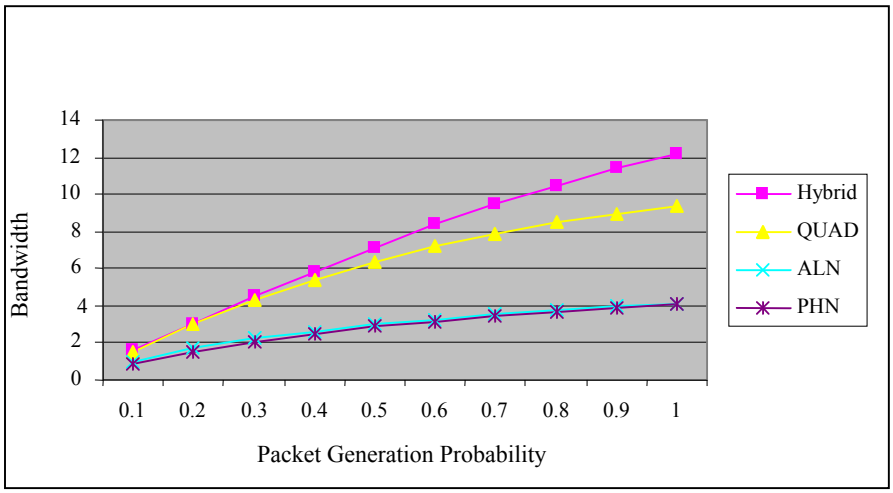

Figure 5.2(c) : Bandwidth comparison of Hybrid with QUAD, ALN and PHN Networks

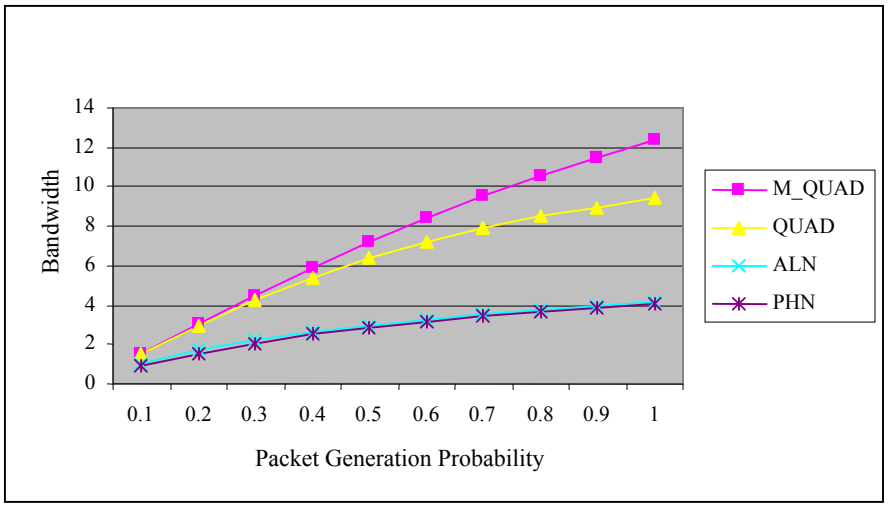

Figure 5.2(d) : Bandwidth comparison of M_QUAD with QUAD, ALN and PHN Networks

5.1.3 Fault-Tolerance

Fault-Tolerance is an important parameter for evaluating the performance of any MIN. In this section, fault-tolerance of the proposed regular and irregular MINs have been compared in tables 5.3(a)- 5.3(b).

Table 5.3 (a)
Fault-Tolerance Comparison of proposed M_ASEN with existing ASEN-2

MIN	Number of faults that can be tolerated in first stage	Number of faults that can be tolerated in second stage	Number of faults that can be tolerated in third stage
M_ASEN	Two SEs per loop	Two SEs per loop	Two of three associated SEs
ASEN-2	Single SE per loop	Single SE per loop	One of two associated SEs

Table 5.3 (b)
Fault-Tolerance Comparison of the proposed Irregular MINs with the existing MINs of similar type

MIN	Number of SE faults that can be tolerated in first stage	Number of SE faults that can be tolerated in second stage	Number of SE faults that can be tolerated in third stage	Number of SE faults that can be tolerated in fourth stage	Number of SE faults that can be tolerated in fifth stage
M_FDOT	Two SEs per loop	Two SEs per loop	Two SEs per loop	Two of three associated	-
Hybrid	Two SEs per loop	Single SE per loop	Single SE per loop		-
M_QUAD	Two SEs per loop	Two SEs per loop	Two SEs per loop	Two SEs per loop	Two of three associated SEs
QUAD	One SE per loop	One SE per loop	One SE per loop	One SE per loop	One of two associated SEs
ALN	One SE per loop	One SE per loop	One SE per loop	One SE per loop	One of two associated SEs
PHN	One SE per loop	One SE per loop	One SE per loop	One of two associated	-

From tables 5.3(a) – 5.3(b), it has been observed that the proposed MINs are better than the existing MINs of similar type as faults in two SEs can be tolerated in each loop as compared to single SE fault-tolerance in the existing MINs.

5.1.4 Terminal Reliability

The terminal reliability is the probability that a given source-destination pair has atleast one fault-free path between them given that each SE has a certain reliability. The terminal reliability is a measure of the robustness of the MIN.

Table 5.4(a) : Terminal Reliability Comparison of Regular MINs for SE reliability = 0.9

MIN	Terminal Reliability
M_ASEN	0.9724
ASEN-2	0.953
ASEN_MAX	0.960
INDRA	0.946
Gamma	0.859
Modified Omega	0.810
Delta (2×2)	0.656
SEN	0.729

Table 5.4(b)
Terminal Reliability Comparison of Irregular MINs for Favorite Destinations

SE Reliability	M_FDOT	Hybrid	M_QUAD	QUAD
0.90	0.9876	0.9876	0.9931	0.9639
0.92	0.9932	0.9932	0.9964	0.9764
0.94	0.997	0.997	0.9984	0.9864
0.96	0.999	0.999	0.9995	0.994

Table 5.4(c)
Terminal Reliability Comparison of Irregular MINs for Non-Favorite Destinations

SE Reliability	M_FDOT	Hybrid	M_QUAD	QUAD
0.90	0.8973	0.8812	0.8964	0.8645
0.92	0.9186	0.9078	0.9182	0.8967
0.94	0.9394	0.933	0.9392	0.9265
0.96	0.9598	0.9569	0.9598	0.9539

It has been observed from the Tables 5.4(a) – 5.4(c) that the terminal reliabilities of the proposed regular and irregular MINs are comparable to that of the existing networks (***regular*** : ASEN-2 and ASEN-4 ; ***irregular*** : QUAD) but appreciably higher than other existing MINs (regular : INDRA, Gamma, Modified Omega, Delta, SEN) as shown in tables 5.4(a)-5.4(c).

5.1.5 Permutations Passable

A permutation is a full one-to-one mapping between the network sources and destinations. Table 5.5 presents the permutations passable feature of the proposed regular and irregular MINs and also those of existing regular : ASEN-2 and irregular : QUAD.

Table 5.5
Permutations Passable

MIN	**Permutations Passable**
M_ASEN	1824
M_FDOT	1024
Hybrid	1024
M_QUAD	768
ASEN_2	1824 (under fault-free conditions)
QUAD	768 (under fault-free scenario)

In fault-free scenario, the permutations passable in M_ASEN and M_QUAD are identical to that in existing MINs i.e. ASEN-2 and QUAD respectively. But in case of single SE fault in every loop in the first stage, the permutations passable in the proposed MINs remain unchanged whereas in the existing MINs it gets reduced by 50%.

5.1.6 Cost and Path Length

The following table presents the cost and path length of the proposed and existing MINs.

Table 5.6
Cost and Path length Comparison (Size 16×16)

MIN	Cost	PL for favorite	PL for non-favorite
M_FDOT	328	2	4
Hybrid	436	2	4
M_ASEN	328	3	3
M_QUAD	355	2	4/5
ASEN-2	240	3	3
ASEN-MAX	240	3	3
QUAD	258	2	4/5
ALN	276	2	5
PHN	200	2	5
ESC	224	3	3
INDRA	320	4	4
FDOT-2	252	2	4/5

5.2 Conclusions

In this chapter, the performances of the proposed regular and irregular MINs, namely M_ASEN, M_FDOT, Hybrid and M_QUAD, have been compared with the existing MINs of similar type. The comparison has been made based on the following performance parameters – probability of acceptance, bandwidth, fault-tolerance, reliability, permutations passable, path length and cost. Probability of acceptance and bandwidth comparisons have also been done under faulty scenarios.

It has been observed that M_ASEN turns out to be better than existing ASEN-2 and ASEN-MAX (loop size 4) on probability of acceptance, bandwidth and fault-tolerance. Considering probability of acceptance and bandwidth, the values are nearly 20% higher for packet generation rate of 1.0 . Considering fault-tolerance, the proposed M_ASEN can tolerate faults in two SEs per loop (in each stage) and in two associated SEs (in the last stage) where as the existing ASEN-2 can tolerate only single SE fault per loop and one of the two associated SEs in the last stage. ASEN-MAX can tolerate (n-1) SE faults per loop if there are n SEs in each loop but at the same time this increases the network cycle time. As such, M_ASEN is optimal considering these two aspects. Permutations passable of M_ASEN is identical to that of ASEN-2 and ASEN-MAX.

Considering cost, the designed M_ASEN is slightly higher ASEN-2 but path length is comparable.

So it is clear that the proposed irregular MINs namely M_FDOT, Hybrid and M_QUAD give better performance than the existing high performance MINs of similar type on many parametric fronts and are comparable on some other performance parameters. Considering probability of acceptance and bandwidth feature, the values for the proposed MINs are higher than the selected existing MINs of similar type – QUAD, ALN and PHN as is evident from table 5.1(a)–5.1(d) and 5.2(a)-5.2(d). When compared with existing networks i.e. QUAD, ALN and PHN, probability of acceptance and bandwidth parameters are better by 18% and 55% respectively. The permutation passable feature of the proposed MINs remains unaffected in case of first stage non-critical paths where as in existing MINs, permutations passable is reduced by 50%. However, path length feature of the designed MINs is comparable to the existing MINs e.g. path length in M_FDOT is identical to that of existing FDOT. Similarly, these parametric features in M_QUAD are identical to that in QUAD. When compared among themselves, M_FDOT is most efficient in terms of bandwidth and probability of acceptance followed by Hybrid and then M_QUAD. Considering terminal reliability, M_QUAD is having the highest value of this parameter and hence is the best among the three. In terms of permutations passable, M_FDOT and Hybrid MINs are equally good followed by M_QUAD. Considering the cost feature, M_FDOT is the most economical among the designed irregular MINs. M_ASEN, which is a regular topology, is highly fault-tolerant and also on-line repairable. However, in M_ASEN, the path length for favorite destinations increases with the increase in the size of the network.

For small sized networks and with the request generation rate being moderate, M_ASEN seems to be the best. But when either the request generation rate is on the higher side or in case of large sized network, then M_FDOT and Hybrid perform better.

Therefore, based on the performance parameters, it is concluded that the proposed networks are better than the existing networks of similar type in terms of probability of acceptance, bandwidth, fault-tolerance, permutations passable and comparable in other parameters except cost which is slightly higher.

Chapter 6

Conclusions

This chapter presents the conclusions which have been derived during the design and analysis of the proposed fault-tolerant MINs. In this thesis, the problem that has been considered is to design MINs with better performance along with efficient routing algorithms than the existing MINs. The methodology that has been incorporate to achieve improved performance comprises of – an additional fault-tolerant subnetwork, chaining of SEs in a loop and designing secondary links from sources in such a way that there is no blocking in the multiplexers. Four designs have been proposed : one regular and three irregular. Irregular Networks have been given more consideration because of their path length advantage for favorite destinations. All the proposed MINs are fault-tolerant and dynamic. The techniques that have been used to achieve fault-tolerance are chaining and redundancy at the network level. Suggestions for future work have also been incorporated.

6.1 Conclusions

In order to design interconnection networks for multiprocessor systems, optimization of the performance is essential for sustained fault-tolerant operations of the network. In view of this, different techniques based upon providing redundancy at the network level and providing multiple paths have been employed to improve the fault-tolerance of the existing MINs and to recommend some new networks. In this thesis, the objective of designing better fault-tolerant dynamic MINs along with routing algorithms and evaluating their performance analytically has been considered. Four new designs of MINs have been proposed. One of the proposed MINs is regular and has been named M_ASEN and the other three MINs are irregular and have been named as M_FDOT, Hybrid and M_QUAD. Modifications in the attributes of the existing Augmented Shuffle Exchange Network (ASEN-2) has resulted in M_ASEN that provides improved performance in terms of probability of acceptance, bandwidth, fault-tolerance and

permutations passable (under fault scenarios). The existing irregular FDOT has been altered in construction and the resulting M_FDOT network shows improvement in performance parameters. The proposed M_QUAD is the result of modification in the existing QUAD tree network with improved performance. Hybrid is a new design that makes use of both topologies i.e. regular and irregular. A very prominent feature that has been kept in each design is to minimize blocking of packets in multiplexers during fault scenarios. The performance parameters that have been considered are – probability of acceptance, bandwidth, fault-tolerance, terminal reliability, permutations passable, path length and cost. Two new performance parameters have been proposed - average queue length and optimal buffer requirement. Each of the proposed MINs before being evaluated for various performance parameters has been analyzed for the distribution of packet traffic i.e. the probability of a packet being present at the ports of each SE in each stage. The packet (traffic) distribution has been analyzed for various value of packet generation rates for fault-free as well as fault scenarios. The various performance parameters that have been evaluated on the basis of this packet (traffic) distribution are average queue length, optimal buffer requirement, probability of acceptance and bandwidth. Probability of acceptance and bandwidth have been evaluated for different values of packet generation rates varying from 0.1 to 1.0 in incremental steps of 0.1 under fault-free and fault scenarios. It has been observed from the analysis that the proposed regular and irregular MINs are better than the existing MINs of similar type. The probability of acceptance and bandwidth values in M_ASEN corresponding to packet generation rate of 1.0 are 0.7811 and 12.4976 which are higher than that of existing ASEN-2 and ASEN-MAX (ASEN-4) (The probability of acceptance and bandwidth values in ASEN-2 are 0.5812 and 9.2986 respectively. In ASEN-4, the corresponding values are 0.5998 and 9.5970 respectively). Regarding fault-tolerance, the proposed M_ASEN can tolerate two SE faults in each loop in any stage whereas ASEN-2 is single SE fault-tolerant. The terminal reliability parameter is almost comparable. In M_ASEN, the terminal reliability has been evaluated as 0.9724 whereas that of existing ASEN-2 is 0.953 and that of ASEN-MAX (ASEN-4) is 0.960. The path length of M_ASEN remains same as that of existing ASEN. The permutations passable in M_ASEN as well as in existing ASEN are 1824. The probability of acceptance values for the proposed irregular

MINs namely M_FDOT, Hybrid and M_QUAD corresponding to packet generation rate of 1.0 are 0.7780, 0.7630 and 0.7726 which are higher than the existing MINs of similar type. The bandwidth values for the proposed MINs, again for maximum value of packet generation rate i.e. 1.0 which are 12.4480, 12.2076 and 12.3610 are again better than the existing MINs of similar type. The comparison of the proposed MINs with existing QUAD reveals that probability of acceptance and bandwidth features show improvement to the extent of 18%. Comparison with existing ALN and PHN reveals 55% improvement in these features. Regarding fault-tolerance, the proposed MINs can tolerate faults of two SEs per loop in each stage compared to single SE (per loop) fault-tolerance capability of existing MINs. Because of better fault-tolerance feature, the proposed irregular MINs are more efficient in terms of permutations passable under faulty scenarios. The permutations passable feature of the proposed MINs remains unaffected under non-critical faults whereas it gets affected in case of existing MINs. A very appreciating feature of the proposed MINs is that in case of fault scenarios, there is slight degradation in probability of acceptance and bandwidth values while maintaining all the permutations. When compared among themselves, M_FDOT and M_QUAD are comparable and better than Hybrid especially for large sized networks. It is due to the reason that the path length for favorite destinations under fault scenarios for Hybrid networks increase with the increase in the size of the network where as in case of M_FDOT and M_QUAD, it remains constant. Considering terminal reliability feature, the proposed MINs are comparable with the existing MINs of similar type. For analyzing fault-tolerance of the proposed MINs, SE faults in the first stage have been considered as first stage faults have the worst effect on performance. The terminal reliabilities have been evaluated considering different values of SE reliabilities for favorite as well as for non-favorite destinations. M_QUAD is having the highest value for terminal reliability. In terms of permutations passable, FDOT and Hybrid MINs realize equal permutations i.e. 1024 followed by M_QUAD i.e 768. The proposed MINs have been observed to be better than the existing networks in permutations passable feature under faulty scenarios but comparable under fault free conditions. Lastly, each of the proposed MIN has been evaluated for its cost. The cost of the proposed MINs have been found to be slightly

higher than the existing networks but considering at the performance improvements of the newly proposed MINS, the slight increase in cost is agreeable.

In short, the proposed networks are better than the existing networks of similar type in terms of probability of acceptance, bandwidth and fault-tolerance. The proposed networks outperform the existing networks in permutation passable feature under faulty scenarios but are comparable under fault-free conditions. Consider terminal reliability, the proposed MINs are better than some of the existing MINs like ALN, PHN and comparable with other MINs like QUAD. The path length for favorite destinations, is comparable with the existing MINs of similar type. The proposed fault-tolerant MINs offer many desirable features for use in high-speed, parallel computing environments.

6.2 Future Scope of Work

There is a lot of scope for further research in this area.

- Search for new topological designs and analysis of dynamic (regular and irregular) MINs needs further exploration with an aim towards increased improvement in performance and reliability.
- VLSI implementation of the proposed networks need to be looked into and analysis of the dynamic multipath networks in the VLSI environment in terms of hardware complexity and improved performance. Another parameter that can be studied in the VLSI environment is the bounds on area requirement of fault-tolerant MINs.
- The use of these regular-irregular MINs in ATM applications may be explored.
- Detailed analysis of optimal buffer requirement and the design of their control units can be an extended area of this research.

Annexure 1

Table A1.1(a)
Primary routes from sources to all destinations

Sources	Path through the Network	Destinations
S_0, S_1	SE1,0 → SE2,0 → SE3,0	D_0, D_1 , D_2, D_3
S_0, S_1	SE1,0 → SE2,0 → SE3,2	D_4,D_5,D_6,D_7
S_0, S_1	SE1,0 → SE2,4 → SE3,4	D_8, D_9 , D_{10}, D_{11}
S_0, S_1	SE1,0 → SE2,4 → SE3,6	D_{12},D_{13}, D_{14},D_{15}
S_2, S_3	SE1,1 → SE2,3 → SE3,1	D_0, D_1 , D_2, D_3
S_2, S_3	SE1,1 → SE2,3 → SE3,3	D_4,D_5 , D_6, D_7,
S_2, S_3	SE1,1 → SE2,5 → SE3,5	D_8, D_9 , D_{10}, D_{11}
S_2, S_3	SE1,1 → SE2,5 → SE3,7	D_{12}, D_{13} , D_{14}, D_{15}
S_4, S_5	SE1,2 → SE2,2 → SE3,0	D_0, D_1 , D_2, D_3
S_4, S_5	SE1,2 → SE2,2 → SE3,2	D_4, D_5 , D_6,D_7
S_4, S_5	SE1,2 → SE2,6 → SE3,4	D_8, D_9 , D_{10}, D_{11}
S_4, S_5	SE1,2 → SE2,6 → SE3,6	D_{12}, D_{13}, D_{14},D_{15}
S_6, S_7	SE1,3 → SE2,3 → SE3,1	D_0, D_1 , D_2, D_3
S_6, S_7	SE1,3 → SE2,3 → SE3,3	D_4, D_5 , D_6, D_7,
S_6, S_7	SE1,3 → SE2,7 → SE3,5	D_8, D_9 , D_{10}, D_{11}
S_6, S_7	SE1,3 → SE2,7 → SE3,7	D_{12}, D_{13} , D_{14}, D_{15}
S_8, S_9	SE1,4 → SE2,0 → SE3,0	D_0, D_1 , D_2, D_3
S_8, S_9	SE1,4 → SE2,0 → SE3,2	D_4,D_5 , D_6, D_7,
S_8, S_9	SE1,4 → SE2,4 → SE3,4	D_8, D_9 , D_{10}, D_{11}
S_8, S_9	SE1,4 → SE2,4 → SE3,6	D_{12}, D_{13} , D_{14}, D_{15}
S_{10}, S_{11}	SE1,5 → SE2,1 → SE3,1	D_0, D_1 , D_2, D_3
S_{10}, S_{11}	SE1,5 → SE2,1 → SE3,3	D_4,D_5 , D_6, D_7,
S_{10}, S_{11}	SE1,5 → SE2,5 → SE3,5	D_8, D_9 , D_{10}, D_{11}
S_{10}, S_{11}	SE1,5 → SE2,5 → SE3,7	D_{12}, D_{13} , D_{14}, D_{15}
S_{12}, S_{13}	SE1,6 → SE2,2 → SE3,0	D_0, D_1 , D_2, D_3
S_{12}, S_{13}	SE1,6 → SE2,2 → SE3,2	D_4,D_5 , D_6, D_7,
S_{12}, S_{13}	SE1,6 → SE2,6 → SE3,4	D_8, D_9 , D_{10}, D_{11}
S_{12}, S_{13}	SE1,6 → SE2,6 → SE3,6	D_{12}, D_{13} , D_{14}, D_{15}
S_{14}, S_{15}	SE1,7 → SE2,3 → SE3,1	D_0, D_1 , D_2, D_3
S_{14}, S_{15}	SE1,7 → SE2,3 → SE3,3	D_4,D_5 , D_6, D_7,
S_{14}, S_{15}	SE1,7 → SE2,7 → SE3,5	D_8, D_9 , D_{10}, D_{11}
S_{14}, S_{15}	SE1,7 → SE2,7 → SE3,7	D_{12}, D_{13} , D_{14}, D_{15}

Table A1.1(b)
Secondary routes from sources to all destinations

Sources	Path through the Network	Destinations
S_0, S_1,S_{14},S_{15}	FT1,1 → FT2,1 → FT3,0	D_0, D_1 , D_2, D_3
S_0, S_1,S_{14},S_{15}	FT1,1 → FT2,1 → FT3,1	D_4,D_5 , D_6, D_7,
S_0, S_1,S_{14},S_{15}	FT1,1 → FT2,3 → FT3,2	D_8, D_9 , D_{10}, D_{11}
S_0, S_1,S_{14},S_{15}	FT1,1 → FT2,3 → FT3,3	D_{12}, D_{13} , D_{14}, D_{15}
S_2, S_3,S_4,S_5	FT1,2 → FT2,0 → FT3,0	D_0, D_1 , D_2, D_3
S_2, S_3,S_4,S_5	FT1,2 → FT2,0 → FT3,1	D_4,D_5 , D_6, D_7,
S_2, S_3,S_4,S_5	FT1,2 → FT2,2 → FT3,2	D_8, D_9 , D_{10}, D_{11}
S_2, S_3,S_4,S_5	FT1,2 → FT2,2 → FT3,3	D_{12}, D_{13} , D_{14}, D_{15}
S_6, S_7,S_8,S_9	FT1,3 → FT2,1 → FT3,0	D_0, D_1 , D_2, D_3
S_6, S_7,S_8,S_9	FT1,3 → FT2,1 → FT3,1	D_4,D_5 , D_6, D_7,
S_6, S_7,S_8,S_9	FT1,3 → FT2,3 → FT3,2	D_8, D_9 , D_{10}, D_{11}
S_6, S_7,S_8,S_9	FT1,3 → FT2,3 → FT3,3	D_{12}, D_{13} , D_{14}, D_{15}
S_{10}, S_{11},S_{12},S_{13}	FT1,0 → FT2,0 → FT3,0	D_0, D_1 , D_2, D_3
S_{10}, S_{11},S_{12},S_{13}	FT1,0 → FT2,0 → FT3,1	D_4,D_5 , D_6, D_7,
S_{10}, S_{11},S_{12},S_{13}	FT1,0 → FT2,2 → FT3,2	D_8, D_9 , D_{10}, D_{11}
S_{10}, S_{11},S_{12},S_{13}	FT1,0 → FT2,2 → FT3,3	D_{12}, D_{13} , D_{14}, D_{15}

Table A1.2(a)
Probability evaluation equations for packet availability at auxiliary ports of first stage SEs

$p_{aux\_SE10} = p_{gen\_SE12} + p_{gen\_FT10} * p_{prop\_SE12}$
$p_{aux\_SE11} = p_{gen\_SE13} + p_{gen\_FT11} * p_{prop\_SE13}$
$p_{aux\_SE12} = p_{gen\_FT10} + p_{gen\_SE10} * p_{prop\_FT10}$
$p_{aux\_SE13} = p_{gen\_FT11} + p_{gen\_SE11} * p_{prop\_FT11}$
$p_{aux\_SE14} = p_{gen\_SE16} + p_{gen\_FT12} * p_{prop\_SE16}$
$p_{aux\_SE15} = p_{gen\_SE17} + p_{gen\_FT13} * p_{prop\_SE17}$
$p_{aux\_SE16} = p_{gen\_FT12} + p_{gen\_SE14} * p_{prop\_FT12}$
$p_{aux\_SE17} = p_{gen\_FT13} + p_{gen\_SE15} * p_{prop\_FT13}$
$p_{aux\_FT10} = p_{gen\_SE10} + p_{gen\_SE12} * p_{prop\_SE10}$
$p_{aux\_FT11} = p_{gen\_SE11} + p_{gen\_SE13} * p_{prop\_SE11}$
$p_{aux\_FT12} = p_{gen\_SE14} + p_{gen\_SE16} * p_{prop\_SE14}$
$p_{aux\_FT13} = p_{gen\_SE15} + p_{gen\_SE17} * p_{prop\_SE15}$

Table A1.2(b)

Probability evaluation equations for packet availability at auxiliary ports of second stage SEs

$p_{aux\_SE20} = p_{gen\_SE22} + p_{gen\_FT20} * p_{prop\_SE22}$
$p_{aux\_SE21} = p_{gen\_SE23} + p_{gen\_FT21} * p_{prop\_SE23}$
$p_{aux\_SE22} = p_{gen\_FT20} + p_{gen\_SE20} * p_{prop\_FT20}$
$p_{aux\_SE23} = p_{gen\_FT21} + p_{gen\_SE21} * p_{prop\_FT21}$
$p_{aux\_SE24} = p_{gen\_SE26} + p_{gen\_FT22} * p_{prop\_SE26}$
$p_{aux\_SE25} = p_{gen\_SE27} + p_{gen\_FT23} * p_{prop\_SE27}$
$p_{aux\_SE26} = p_{gen\_FT22} + p_{gen\_SE24} * p_{prop\_FT22}$
$p_{aux\_SE27} = p_{gen\_FT23} + p_{gen\_SE25} * p_{prop\_FT23}$
$p_{aux\_FT20} = p_{gen\_SE20} + p_{gen\_SE22} * p_{prop\_SE20}$
$p_{aux\_FT21} = p_{gen\_SE21} + p_{gen\_SE23} * p_{prop\_SE21}$
$p_{aux\_FT22} = p_{gen\_SE24} + p_{gen\_SE26} * p_{prop\_SE24}$
$p_{aux\_FT23} = p_{gen\_SE25} + p_{gen\_SE27} * p_{prop\_SE25}$

Table A1.2(c)

Probability evaluation equations for packet availability at input ports of second stage SEs

$p_{in1\_SE20} = p_{out\_SE10}$; $p_{in2\_SE20} = p_{out\_SE14}$
$p_{in1\_SE21} = p_{out\_SE10}$; $p_{in2\_SE21} = p_{out\_SE14}$
$p_{in1\_SE22} = p_{out\_SE11}$; $p_{in2\_SE22} = p_{out\_SE15}$
$p_{in1\_SE23} = p_{out\_SE11}$; $p_{in2\_SE23} = p_{out\_SE15}$
$p_{in1\_SE24} = p_{out\_SE12}$; $p_{in2\_SE24} = p_{out\_SE16}$
$p_{in1\_SE25} = p_{out\_SE12}$; $p_{in2\_SE25} = p_{out\_SE16}$
$p_{in1\_SE26} = p_{out\_SE13}$; $p_{in2\_SE26} = p_{out\_SE17}$
$p_{in1\_SE27} = p_{out\_SE13}$; $p_{in2\_SE27} = p_{out\_SE17}$
$p_{in1\_FT20} = p_{out\_FT10}$; $p_{in2\_FT20} = p_{out\_FT12}$
$p_{in1\_FT21} = p_{out\_FT10}$; $p_{in2\_FT21} = p_{out\_FT12}$
$p_{in1\_FT22} = p_{out\_FT11}$; $p_{in2\_FT22} = p_{out\_FT13}$
$p_{in1\_FT23} = p_{out\_FT11}$; $p_{in2\_FT23} = p_{out\_FT13}$

Table A1.2(d)

Probability evaluation equations for packet availability at output ports of second stage SEs

$p_{out\_SE20} = 1 - (1 - p_{in1\_SE20}/b) * (1 - p_{in2\_SE20}/b)*(1 - p_{aux\_SE20}/b)$
$p_{out\_SE21} = 1 - (1 - p_{in1\_SE21}/b) * (1 - p_{in2\_SE21}/b)*(1 - p_{aux\_SE21}/b)$
$p_{out\_SE22} = 1 - (1 - p_{in1\_SE22}/b) * (1 - p_{in2\_SE22}/b)*(1 - p_{aux\_SE22}/b)$
$p_{out\_SE23} = 1 - (1 - p_{in1\_SE23}/b) * (1 - p_{in2\_SE23}/b)*(1 - p_{aux\_SE23}/b)$
$p_{out\_SE24} = 1 - (1 - p_{in1\_SE24}/b) * (1 - p_{in2\_SE24}/b)*(1 - p_{aux\_SE24}/b)$
$p_{out\_SE25}= 1 - (1 - p_{in1\_SE25}/b) * (1 - p_{in2\_SE25}/b)*(1 - p_{aux\_SE25}/b)$
$p_{out\_SE26} = 1 - (1 - p_{in1\_SE26}/b) * (1 - p_{in2\_SE26}/b)*(1 - p_{aux\_SE26}/b)$
$p_{out\_SE27} = 1 - (1 - p_{in1\_SE27}/b) * (1 - p_{in2\_SE27}/b)*(1 - p_{aux\_SE27}/b)$
$p_{out\_FT20} = 1 - (1 - p_{in1\_FT20}/b) * (1 - p_{in2\_FT20}/b)*(1 - p_{aux\_FT20}/b)$
$p_{out\_FT21} = 1 - (1 - p_{in1\_FT21}/b) * (1 - p_{in2\_FT21}/b)*(1 - p_{aux\_FT21}/b)$
$p_{out\_FT22} = 1 - (1 - p_{in1\_FT22}/b) * (1 - p_{in2\_FT22}/b)*(1 - p_{aux\_FT22}/b)$
$p_{out\_FT23} = 1 - (1 - p_{in1\_FT23}/b) * (1 - p_{in2\_FT23}/b)*(1 - p_{aux\_FT23}/b)$

Table A1.2(e)

Probability evaluation equations for packet availability at output ports of third stage SEs

$p_{out\_SE30} = 1 - (1 - p_{in1\_SE30}/b) * (1 - p_{in2\_SE30}/b)$
$p_{out\_SE31} = 1 - (1 - p_{in1\_SE31}/b) * (1 - p_{in2\_SE31}/b)$
$p_{out\_SE32} = 1 - (1 - p_{in1\_SE32}/b) * (1 - p_{in2\_SE32}/b)$
$p_{out\_SE33} = 1 - (1 - p_{in1\_SE33}/b) * (1 - p_{in2\_SE33}/b)$
$p_{out\_SE34} = 1 - (1 - p_{in1\_SE34}/b) * (1 - p_{in2\_SE34}/b)$
$p_{out\_SE35} = 1 - (1 - p_{in1\_SE35}/b) * (1 - p_{in2\_SE35}/b)$
$p_{out\_SE36} = 1 - (1 - p_{in1\_SE36}/b) * (1 - p_{in2\_SE36}/b)$
$p_{out\_SE37} = 1 - (1 - p_{in1\_SE37}/b) * (1 - p_{in2\_SE37}/b)$
$p_{out\_FT30} = 1 - (1 - p_{in1\_FT30}/b) * (1 - p_{in2\_FT30}/b)$
$p_{out\_FT31} = 1 - (1 - p_{in1\_FT31}/b) * (1 - p_{in2\_FT31}/b)$
$p_{out\_FT32} = 1 - (1 - p_{in1\_FT32}/b) * (1 - p_{in2\_FT32}/b)$
$p_{out\_FT33} = 1 - (1 - p_{in1\_FT33}/b) * (1 - p_{in2\_FT33}/b)$

Table A1.3(a)
Probability for packet availability corresponding to packet generation rate of 0.5 (M_ASEN)

SE#	P_{out}	$P_{aux\ in}$	SE#	P_{out}	$P_{aux\ in}$	SE#	P_{out}
SE1,0	0.4727	0.1250	SE2,0	0.4498	0.1130	SE3,0	0.3874
SE11	0.4727	0.1250	SE2,1	0.4595	0.1462	SE3,1	0.3874
SE1,2	0.4375	0.0000	SE2,2	0.4206	0.0129	SE3,2	0.3912
SE1,3	0.4375	0.0000	SE2,3	0.4558	0.1339	SE3,3	0.3982
SE1,4	0.4727	0.1250	SE2,4	0.4192	0.0970	SE3,4	0.3655
SE1,5	0.4727	0.1250	SE2,5	0.4192	0.0970	SE3,5	0.3655
SE1,6	0.4375	0.0000	SE2,6	0.3932	0.0116	SE3,6	0.3797
SE1,7	0.4375	0.0000	SE2,7	0.3932	0.0116	SE3,7	0.3797
FT1,0	0.0859	0.1719	FT2,0	0.1537	0.1520	FT3,0	0.1428
FT1,1	0.0859	0.1719	FT2,1	0.1537	0.1520	FT3,1	0.1428
FT1,2	0.0859	0.1719	FT2,2	0.1429	0.1284	FT3,2	0.1428
FT1,3	0.0859	0.1719	FT2,3	0.1429	0.1284	FT3,3	0.1428

Table A1.3(b)
Probability for packet availability corresponding to packet generation rate of 0.8 (M_ASEN)

SE#	P_{out}	$P_{aux\ in}$	SE#	P_{out}	$P_{aux\ in}$	SE#	P_{out}
SE1,0	0.6976	0.3200	SE2,0	0.6302	0.2561	SE3,0	0.5164
SE1,1	0.6976	0.3200	SE2,1	0.6473	0.3364	SE3,1	0.5164
SE1,2	0.6400	0.0000	SE2,2	0.5927	0.0788	SE3,2	0.5224
SE1,3	0.6400	0.0000	SE2,3	0.6418	0.3107	SE3,3	0.5224
SE1,4	0.6976	0.3200	SE2,4	0.5878	0.2170	SE3,4	0.4912
SE1,5	0.6976	0.3200	SE2,5	0.5878	0.2170	SE3,5	0.4912
SE1,6	0.6400	0.0000	SE2,6	0.5540	0.0708	SE3,6	0.5090
SE1,7	0.6400	0.0000	SE2,7	0.5540	0.0708	SE3,7	0.5090
FT1,0	0.2368	0.4736	FT2,0	0.3603	0.3539	FT3,0	0.3183
FT1,1	0.2368	0.4736	FT2,1	0.3603	0.3539	FT3,1	0.3183
FT1,2	0.2368	0.4736	FT2,2	0.3370	0.2939	FT3,2	0.3183
FT1,3	0.2368	0.4736	FT2,3	0.3370	0.2939	FT3,3	0.3183

Table A1.3 (c)
Probability for packet availability corresponding to packet generation rate of 1.0 (M_ASEN)

SE#	P_{out}	$P_{aux\ in}$	SE#	P_{out}	$P_{aux\ in}$	SE#	P_{out}
SE1,0	0.8125	0.5000	SE2,0	0.7116	0.3640	SE3,0	0.5719
SE1,1	0.8125	0.5000	SE2,1	0.7296	0.4658	SE3,1	0.5719
SE1,2	0.7500	0.0000	SE2,2	0.6776	0.1709	SE3,2	0.5778
SE1,3	0.7500	0.0000	SE2,3	0.7243	0.4360	SE3,3	0.5778
SE1,4	0.8125	0.5000	SE2,4	0.6707	0.3142	SE3,4	0.5503
SE1,5	0.8125	0.5000	SE2,5	0.6707	0.3142	SE3,5	0.5503
SE1,6	0.7500	0.0000	SE2,6	0.6398	0.1560	SE3,6	0.5662
SE1,7	0.7500	0.0000	SE2,7	0.6398	0.1560	SE3,7	0.5662
FT1,0	0.3750	0.7500	FT2,0	0.5014	0.4893	FT3,0	0.4291
FT1,1	0.3750	0.7500	FT2,1	0.5014	0.4893	FT3,1	0.4291
FT1,2	0.3750	0.7500	FT2,2	0.4762	0.4131	FT3,2	0.4291
FT1,3	0.3750	0.7500	FT2,3	0.4762	0.4131	FT3,3	0.4291

Table A1.4(a)

$S_i \rightarrow D_j$ where j=i and i varying from 0 to N-2 with increment 2	$S_i \rightarrow D_j$ where j varying from (N-k) to 1 with decrement 2 where k = subscript of S i.e. 1 and i varying from 1 to N-1 with increment 2	$S_i \rightarrow D_j$ where j = i+1 and i varying from 0 to N-2 with increment 2	$S_i \rightarrow D_j$ where j varying from (N-k-1) to 0 with decrement 2 where k = subscript of S i.e. 1 and i varying from 1 to N-1 with increment 2
$S_0 \rightarrow D_0$	$S_1 \rightarrow D_{15}$	$S_0 \rightarrow D_1$	$S_1 \rightarrow D_{14}$
$S_2 \rightarrow D_2$	$S_3 \rightarrow D_{13}$	$S_2 \rightarrow D_3$	$S_3 \rightarrow D_{12}$
$S_4 \rightarrow D_4$	$S_5 \rightarrow D_{11}$	$S_4 \rightarrow D_5$	$S_5 \rightarrow D_{10}$
$S_6 \rightarrow D_6$	$S_7 \rightarrow D_9$	$S_6 \rightarrow D_7$	$S_7 \rightarrow D_8$
$S_8 \rightarrow D_8$	$S_9 \rightarrow D_7$	$S_8 \rightarrow D_9$	$S_9 \rightarrow D_6$
$S_{10} \rightarrow D_{10}$	$S_{11} \rightarrow D_5$	$S_{10} \rightarrow D_{11}$	$S_{11} \rightarrow D_4$
$S_{12} \rightarrow D_{12}$	$S_{13} \rightarrow D_3$	$S_{12} \rightarrow D_{13}$	$S_{13} \rightarrow D_2$
$S_{14} \rightarrow D_{14}$	$S_{15} \rightarrow D_1$	$S_{14} \rightarrow D_{15}$	$S_{15} \rightarrow D_0$

Table A1.4(b)

$S_i \rightarrow D_j$ where j=i-1 and i varying from 1 to N-1 with increment 2	$S_i \rightarrow D_j$ where j varying from (N-k-1) to 1 with decrement 2 where k = subscript of S i.e. 0 and i varying from 0 to N-2 with increment 2	$S_i \rightarrow D_j$ where j=i and i varying from 1 to N-1 with increment 2	$S_i \rightarrow D_j$ where j varying from (N-k-2) to 0 with decrement 2 where k = subscript of S i.e. 0 and i varying from 0 to N-2 with increment 2
$S_1 \rightarrow D_0$	$S_0 \rightarrow D_{15}$	$S_1 \rightarrow D_1$	$S_0 \rightarrow D_{14}$
$S_3 \rightarrow D_2$	$S_2 \rightarrow D_{13}$	$S_3 \rightarrow D_3$	$S_2 \rightarrow D_{12}$
$S_5 \rightarrow D_4$	$S_4 \rightarrow D_{11}$	$S_5 \rightarrow D_5$	$S_4 \rightarrow D_{10}$
$S_7 \rightarrow D_6$	$S_6 \rightarrow D_9$	$S_7 \rightarrow D_7$	$S_6 \rightarrow D_8$
$S_9 \rightarrow D_8$	$S_8 \rightarrow D_7$	$S_9 \rightarrow D_9$	$S_8 \rightarrow D_6$
$S_{11} \rightarrow D_{10}$	$S_{10} \rightarrow D_5$	$S_{11} \rightarrow D_{11}$	$S_{10} \rightarrow D_4$
$S_{13} \rightarrow D_{12}$	$S_{12} \rightarrow D_3$	$S_{13} \rightarrow D_{13}$	$S_{12} \rightarrow D_2$
$S_{15} \rightarrow D_{14}$	$S_{14} \rightarrow D_1$	$S_{15} \rightarrow D_{15}$	$S_{14} \rightarrow D_0$

Table A1.4 (c)

$S_i \rightarrow D_j$ where j=(i+2) Mod N and i varying from 0 to N-2 with increment 2	$S_i \rightarrow D_j$ where j varying from (N-k-2) to 1 with decrement 2 where k = subscript of S i.e. 1 and then from (N-1) to (N-k-2+2) with decrement 2 and i varying from 1 to N-1 with increment 2	$S_i \rightarrow D_j$ where j=(i+3) Mod N and i varying from 0 to N-2 with increment 2 and i varying from 1 to N-1 with increment 2	$S_i \rightarrow D_j$ where j varying from (N-k-3) to 0 with decrement 2 where k = subscript of S i.e. 1 and then from (N-2) to (N-k-3+2) with decrement 2 and i varying from 1 to N-1 with increment 2
$S_0 \rightarrow D_2$	$S_1 \rightarrow D_{13}$	$S_0 \rightarrow D_3$	$S_1 \rightarrow D_{12}$
$S_2 \rightarrow D_4$	$S_3 \rightarrow D_{11}$	$S_2 \rightarrow D_5$	$S_3 \rightarrow D_{10}$
$S_4 \rightarrow D_6$	$S_5 \rightarrow D_9$	$S_4 \rightarrow D_7$	$S_5 \rightarrow D_8$
$S_6 \rightarrow D_8$	$S_7 \rightarrow D_7$	$S_6 \rightarrow D_9$	$S_7 \rightarrow D_6$
$S_8 \rightarrow D_{10}$	$S_9 \rightarrow D_5$	$S_8 \rightarrow D_{11}$	$S_9 \rightarrow D_4$
$S_{10} \rightarrow D_{12}$	$S_{11} \rightarrow D_3$	$S_{10} \rightarrow D_{13}$	$S_{11} \rightarrow D_2$
$S_{12} \rightarrow D_{14}$	$S_{13} \rightarrow D_1$	$S_{12} \rightarrow D_{15}$	$S_{13} \rightarrow D_0$
$S_{14} \rightarrow D_0$	$S_{15} \rightarrow D_{15}$	$S_{14} \rightarrow D_1$	$S_{15} \rightarrow D_{14}$

Table A14(d)

$S_i \rightarrow D_j$ where j=(i+1) Mod N and i varying from 1 to N-1 with increment 2	$S_i \rightarrow D_j$ where j varying from (N-k-3) to 1 with decrement 2 where k = subscript of S i.e. 0 and then from (N-1) to (N-k-3+2) with decrement 2 and i varying from 0 to N-2 with increment 2	$S_i \rightarrow D_j$ where j=(i+2) Mod N and i varying from 1 to N-1 with increment 2	$S_i \rightarrow D_j$ where j varying from (N-k-4) to 0 with decrement 2 where k = subscript of S i.e. 0 and then from (N-2) to (N-k-4+2) with decrement 2 and i varying from 1 to N-1 with increment 2
$S_1 \rightarrow D_2$	$S_0 \rightarrow D_{13}$	$S_1 \rightarrow D_3$	$S_0 \rightarrow D_{12}$
$S_3 \rightarrow D_4$	$S_2 \rightarrow D_{11}$	$S_3 \rightarrow D_5$	$S_2 \rightarrow D_{10}$
$S_5 \rightarrow D_6$	$S_4 \rightarrow D_9$	$S_5 \rightarrow D_7$	$S_4 \rightarrow D_8$
$S_7 \rightarrow D_8$	$S_6 \rightarrow D_7$	$S_7 \rightarrow D_9$	$S_6 \rightarrow D_6$
$S_9 \rightarrow D_{10}$	$S_8 \rightarrow D_5$	$S_9 \rightarrow D_{11}$	$S_8 \rightarrow D_4$
$S_{11} \rightarrow D_{12}$	$S_{10} \rightarrow D_3$	$S_{11} \rightarrow D_{13}$	$S_{10} \rightarrow D_2$
$S_{13} \rightarrow D_{14}$	$S_{12} \rightarrow D_1$	$S_{13} \rightarrow D_{15}$	$S_{12} \rightarrow D_0$
$S_{15} \rightarrow D_0$	$S_{14} \rightarrow D_{15}$	$S_{15} \rightarrow D_1$	$S_{14} \rightarrow D_{14}$

Table A1.4(e)

$S_i \rightarrow D_j$ where j=(i+4) Mod N and i varying from 0 to N-2 with increment 2	$S_i \rightarrow D_j$ where j varying from (N-k-4) to 1 with decrement 2 and then from (N-1) to (N-k-4+2) with decrement 2 where k = subscript of S i.e. 1 and i varying from 1 to N-1 with increment 2	$S_i \rightarrow D_j$ where j=(i+5) Mod N and i varying from 0 to N-2 with increment 2	$S_i \rightarrow D_j$ where j varying from (N-k-5) to 0 with decrement 2 and then from (N-2) to (N-k-5+2) with decrement 2 where k = subscript of S i.e. 1 and i varying from 1 to N-1 with increment 2
$S_0 \rightarrow D_4$	$S_1 \rightarrow D_{11}$	$S_0 \rightarrow D_5$	$S_1 \rightarrow D_{10}$
$S_2 \rightarrow D_6$	$S_3 \rightarrow D_9$	$S_2 \rightarrow D_7$	$S_3 \rightarrow D_8$
$S_4 \rightarrow D_8$	$S_5 \rightarrow D_7$	$S_4 \rightarrow D_9$	$S_5 \rightarrow D_6$
$S_6 \rightarrow D_{10}$	$S_7 \rightarrow D_5$	$S_6 \rightarrow D_{11}$	$S_7 \rightarrow D_4$
$S_8 \rightarrow D_{12}$	$S_9 \rightarrow D_3$	$S_8 \rightarrow D_{13}$	$S_9 \rightarrow D_2$
$S_{10} \rightarrow D_{14}$	$S_{11} \rightarrow D_1$	$S_{10} \rightarrow D_{15}$	$S_{11} \rightarrow D_0$
$S_{12} \rightarrow D_0$	$S_{13} \rightarrow D_{15}$	$S_{12} \rightarrow D_1$	$S_{13} \rightarrow D_{14}$
$S_{14} \rightarrow D_2$	$S_{15} \rightarrow D_{13}$	$S_{14} \rightarrow D_3$	$S_{15} \rightarrow D_{12}$

Table A1.4(f)

$S_i \rightarrow D_j$ where j=(i+3) Mod N and i varying from 1 to N-1 with increment 2	$S_i \rightarrow D_j$ where j varying from (N-k-5) to 1 with decrement 2 and then from (N-1) to (N-k-5+2) with decrement 2 where k = subscript of S i.e. 0 and i varying from 0 to N-2 with increment 2	$S_i \rightarrow D_j$ where j=(i+4) Mod N and i varying from 1 to N-1 with increment 2	$S_i \rightarrow D_j$ where j varying from (N-k-6) to 0 with decrement 2 and then from (N-2) to (N-k-6+2) with decrement 2 where k = subscript of S i.e. 0 and i varying from 0 to N-2 with increment 2
$S_1 \rightarrow D_4$	$S_0 \rightarrow D_{11}$	$S_1 \rightarrow D_5$	$S_0 \rightarrow D_{10}$
$S_3 \rightarrow D_6$	$S_2 \rightarrow D_9$	$S_3 \rightarrow D_7$	$S_2 \rightarrow D_8$
$S_5 \rightarrow D_8$	$S_4 \rightarrow D_7$	$S_5 \rightarrow D_9$	$S_4 \rightarrow D_6$
$S_7 \rightarrow D_{10}$	$S_6 \rightarrow D_5$	$S_7 \rightarrow D_{11}$	$S_6 \rightarrow D_4$
$S_9 \rightarrow D_{12}$	$S_8 \rightarrow D_3$	$S_9 \rightarrow D_{13}$	$S_8 \rightarrow D_2$
$S_{11} \rightarrow D_{14}$	$S_{10} \rightarrow D_1$	$S_{11} \rightarrow D_{15}$	$S_{10} \rightarrow D_0$
$S_{13} \rightarrow D_0$	$S_{12} \rightarrow D_{15}$	$S_{13} \rightarrow D_1$	$S_{12} \rightarrow D_{14}$
$S_{15} \rightarrow D_2$	$S_{14} \rightarrow D_{13}$	$S_{15} \rightarrow D_3$	$S_{14} \rightarrow D_{12}$

Table A1.4(g)

$S_i \rightarrow D_j$ where j=(i+6) Mod N and i varying from 0 to N-2 with increment 2	$S_i \rightarrow D_j$ where j varying from (N-k-6) to 1 with decrement 2 and then from (N-1) to (N-k-6+2) with decrement 2 where k = subscript of S i.e. 1 and i varying from 1 to N-1 with increment 2	$S_i \rightarrow D_j$ where j=(i+7) Mod N and i varying from 0 to N-2 with increment 2	$S_i \rightarrow D_j$ where j varying from (N-k-7) to 0 with decrement 2 and then from (N-2) to (N-k-7+2) with decrement 2 where k = subscript of S i.e. 1 and i varying from 1 to N-1 with increment 2
$S_0 \rightarrow D_6$	$S_1 \rightarrow D_9$	$S_0 \rightarrow D_7$	$S_1 \rightarrow D_8$
$S_2 \rightarrow D_8$	$S_3 \rightarrow D_7$	$S_2 \rightarrow D_9$	$S_3 \rightarrow D_6$
$S_4 \rightarrow D_{10}$	$S_5 \rightarrow D_5$	$S_4 \rightarrow D_{11}$	$S_5 \rightarrow D_4$
$S_6 \rightarrow D_{12}$	$S_7 \rightarrow D_3$	$S_6 \rightarrow D_{13}$	$S_7 \rightarrow D_2$
$S_8 \rightarrow D_{14}$	$S_9 \rightarrow D_1$	$S_8 \rightarrow D_{15}$	$S_9 \rightarrow D_0$
$S_{10} \rightarrow D_0$	$S_{11} \rightarrow D_{15}$	$S_{10} \rightarrow D_1$	$S_{11} \rightarrow D_{14}$
$S_{12} \rightarrow D_2$	$S_{13} \rightarrow D_{13}$	$S_{12} \rightarrow D_3$	$S_{13} \rightarrow D_{12}$
$S_{14} \rightarrow D_4$	$S_{15} \rightarrow D_{11}$	$S_{14} \rightarrow D_5$	$S_{15} \rightarrow D_{10}$

Table A1.4(h)

$S_i \rightarrow D_j$ where j=(i+5) Mod N and i varying from 1 to N-1 with increment 2	$S_i \rightarrow D_j$ where j varying from (N-k-7) to 1 with decrement 2 and then from (N-1) to (N-k-7+2) with decrement 2 where k = subscript of S i.e. 0 and i varying from 0 to N-2 with increment 2	$S_i \rightarrow D_j$ where j=(i+6) Mod N and i varying from 1 to N-1 with increment 2	$S_i \rightarrow D_j$ where j varying from (N-k-8) to 0 with decrement 2 and then from (N-2) to (N-k-8+2) with decrement 2 where k = subscript of S i.e. 0 and i varying from 0 to N-2 with increment 2
$S_1 \rightarrow D_6$	$S_0 \rightarrow D_9$	$S_1 \rightarrow D_7$	$S_0 \rightarrow D_8$
$S_3 \rightarrow D_8$	$S_2 \rightarrow D_7$	$S_3 \rightarrow D_9$	$S_2 \rightarrow D_6$
$S_5 \rightarrow D_{10}$	$S_4 \rightarrow D_5$	$S_5 \rightarrow D_{11}$	$S_4 \rightarrow D_4$
$S_7 \rightarrow D_{12}$	$S_6 \rightarrow D_3$	$S_7 \rightarrow D_{13}$	$S_6 \rightarrow D_2$
$S_9 \rightarrow D_{14}$	$S_8 \rightarrow D_1$	$S_9 \rightarrow D_{15}$	$S_8 \rightarrow D_0$
$S_{11} \rightarrow D_0$	$S_{10} \rightarrow D_{15}$	$S_{11} \rightarrow D_1$	$S_{10} \rightarrow D_{14}$
$S_{13} \rightarrow D_2$	$S_{12} \rightarrow D_{13}$	$S_{13} \rightarrow D_3$	$S_{12} \rightarrow D_{12}$
$S_{15} \rightarrow D_4$	$S_{14} \rightarrow D_{11}$	$S_{15} \rightarrow D_5$	$S_{14} \rightarrow D_{10}$

Table A1.4(i)

$S_i \rightarrow D_j$ where j=(i+8) Mod N and i varying from 0 to N-2 with increment 2	$S_i \rightarrow D_j$ where j varying from (N-k-8) to 1 with decrement 2 and then from (N-1) to (N-k-8+2) with decrement 2 where k = subscript of S i.e. 1 and i varying from 1 to N-1 with increment 2	$S_i \rightarrow D_j$ where j=(i+9) Mod N and i varying from 0 to N-2 with increment 2	$S_i \rightarrow D_j$ where j varying from (N-k-9) to 0 with decrement 2 and then from (N-2) to (N-k-9+2) with decrement 2 where k = subscript of S i.e. 1 and i varying from 1 to N-1 with increment 2
$S_0 \rightarrow D_8$	$S_1 \rightarrow D_7$	$S_0 \rightarrow D_9$	$S_1 \rightarrow D_6$
$S_2 \rightarrow D_{10}$	$S_3 \rightarrow D_5$	$S_2 \rightarrow D_{11}$	$S_3 \rightarrow D_4$
$S_4 \rightarrow D_{12}$	$S_5 \rightarrow D_3$	$S_4 \rightarrow D_{13}$	$S_5 \rightarrow D_2$
$S_6 \rightarrow D_{14}$	$S_7 \rightarrow D_1$	$S_6 \rightarrow D_{15}$	$S_7 \rightarrow D_0$
$S_8 \rightarrow D_0$	$S_9 \rightarrow D_{15}$	$S_8 \rightarrow D_1$	$S_9 \rightarrow D_{14}$
$S_{10} \rightarrow D_2$	$S_{11} \rightarrow D_{13}$	$S_{10} \rightarrow D_3$	$S_{11} \rightarrow D_{12}$
$S_{12} \rightarrow D_4$	$S_{13} \rightarrow D_{11}$	$S_{12} \rightarrow D_5$	$S_{13} \rightarrow D_{10}$
$S_{14} \rightarrow D_6$	$S_{15} \rightarrow D_9$	$S_{14} \rightarrow D_7$	$S_{15} \rightarrow D_8$

Table A1.4(j)

$S_i \rightarrow D_j$ where j=(i+7) Mod N and i varying from 1 to N-1 with increment 2	$S_i \rightarrow D_j$ where j varying from (N-k-9) to 1 with decrement 2 and then from (N-1) to (N-k-9+2) with decrement 2 where k = subscript of S i.e.0 and i varying from 0 to N-2 with increment 2	$S_i \rightarrow D_j$ where j=(i+8) Mod N and i varying from 1 to N-1 with increment 2	$S_i \rightarrow D_j$ where j varying from (N-k-10) to 0 with decrement 2 and then (N-2) to (N-k-10+2) with decrement 2 where k = subscript of S i.e. 0 and i varying from 0 to N-2 with increment 2
$S_1 \rightarrow D_8$	$S_0 \rightarrow D_7$	$S_1 \rightarrow D_9$	$S_0 \rightarrow D_6$
$S_3 \rightarrow D_{10}$	$S_2 \rightarrow D_5$	$S_3 \rightarrow D_{11}$	$S_2 \rightarrow D_4$
$S_5 \rightarrow D_{12}$	$S_4 \rightarrow D_3$	$S_5 \rightarrow D_{13}$	$S_4 \rightarrow D_2$
$S_7 \rightarrow D_{14}$	$S_6 \rightarrow D_1$	$S_7 \rightarrow D_{15}$	$S_6 \rightarrow D_0$
$S_9 \rightarrow D_0$	$S_8 \rightarrow D_{15}$	$S_9 \rightarrow D_1$	$S_8 \rightarrow D_{14}$
$S_{11} \rightarrow D_2$	$S_{10} \rightarrow D_{13}$	$S_{11} \rightarrow D_3$	$S_{10} \rightarrow D_{12}$
$S_{13} \rightarrow D_4$	$S_{12} \rightarrow D_{11}$	$S_{13} \rightarrow D_5$	$S_{12} \rightarrow D_{10}$
$S_{15} \rightarrow D_6$	$S_{14} \rightarrow D_9$	$S_{15} \rightarrow D_7$	$S_{14} \rightarrow D_8$

Table A1.4(k)

$S_i \rightarrow D_j$ where j=(i+10) Mod N and i varying from 0 to N-2 with increment 2	$S_i \rightarrow D_j$ where j varying from (N-k-10) to 1 with decrement 2 and then from (N-1) to (N-k-10+2) with decrement 2 where k = subscript of S i.e. 1 and i varying from 1 to N-1 with increment 2	$S_i \rightarrow D_j$ where j=(i+11) Mod N and i varying from 0 to N-2 with increment 2	$S_i \rightarrow D_j$ where j varying from (N-k-11) to 0 with decrement 2 and then from (N-2) to (N-k-11+2) with decrement 2 where k = subscript of S i.e. 1 and i varying from 1 to N-1 with increment 2
$S_0 \rightarrow D_{10}$	$S_1 \rightarrow D_5$	$S_0 \rightarrow D_{11}$	$S_1 \rightarrow D_4$
$S_2 \rightarrow D_{12}$	$S_3 \rightarrow D_3$	$S_2 \rightarrow D_{13}$	$S_3 \rightarrow D_2$
$S_4 \rightarrow D_{14}$	$S_5 \rightarrow D_1$	$S_4 \rightarrow D_{15}$	$S_5 \rightarrow D_0$
$S_6 \rightarrow D_0$	$S_7 \rightarrow D_{15}$	$S_6 \rightarrow D_1$	$S_7 \rightarrow D_{14}$
$S_8 \rightarrow D_2$	$S_9 \rightarrow D_{13}$	$S_8 \rightarrow D_3$	$S_9 \rightarrow D_{12}$
$S_{10} \rightarrow D_4$	$S_{11} \rightarrow D_{11}$	$S_{10} \rightarrow D_5$	$S_{11} \rightarrow D_{10}$
$S_{12} \rightarrow D_6$	$S_{13} \rightarrow D_9$	$S_{12} \rightarrow D_7$	$S_{13} \rightarrow D_8$
$S_{14} \rightarrow D_8$	$S_{15} \rightarrow D_7$	$S_{14} \rightarrow D_9$	$S_{15} \rightarrow D_6$

Table A1.4(l)

$S_i \rightarrow D_j$ where j=(i+9) Mod N and i varying from 1 to N-1 with increment 2	$S_i \rightarrow D_j$ where j varying from (N-k-11) to 1 with decrement 2 and then from (N-1) to (N-k-11+2) with decrement 2 where k = subscript of S i.e. 0 and i varying from 0 to N-2 with increment 2	$S_i \rightarrow D_j$ where j=(i+10) Mod N and i varying from 1 to N-1 with increment 2	$S_i \rightarrow D_j$ where j varying from (N-k-12) to 0 with decrement 2 and then from (N-2) to (N-k-12+2) with decrement 2 where k = subscript of S i.e. 0 and i varying from 0 to N-2 with increment 2
$S_1 \rightarrow D_{10}$	$S_0 \rightarrow D_5$	$S_1 \rightarrow D_{11}$	$S_0 \rightarrow D_4$
$S_3 \rightarrow D_{12}$	$S_2 \rightarrow D_3$	$S_3 \rightarrow D_{13}$	$S_2 \rightarrow D_2$
$S_5 \rightarrow D_{14}$	$S_4 \rightarrow D_1$	$S_5 \rightarrow D_{15}$	$S_4 \rightarrow D_0$
$S_7 \rightarrow D_0$	$S_6 \rightarrow D_{15}$	$S_7 \rightarrow D_1$	$S_6 \rightarrow D_{14}$
$S_9 \rightarrow D_2$	$S_8 \rightarrow D_{13}$	$S_9 \rightarrow D_3$	$S_8 \rightarrow D_{12}$
$S_{11} \rightarrow D_4$	$S_{10} \rightarrow D_{11}$	$S_{11} \rightarrow D_5$	$S_{10} \rightarrow D_{10}$
$S_{13} \rightarrow D_6$	$S_{12} \rightarrow D_9$	$S_{13} \rightarrow D_7$	$S_{12} \rightarrow D_8$
$S_{15} \rightarrow D_8$	$S_{14} \rightarrow D_7$	$S_{15} \rightarrow D_9$	$S_{14} \rightarrow D_6$

Table A1.4(m)

$S_i \rightarrow D_j$ where j=(i+10) Mod N and i varying from 0 to N-2 with increment 2	$S_i \rightarrow D_j$ where j varying from (N-k-10) to 1 with decrement 2 and then from (N-1) to (N-k-10+2) with decrement 2 where k = subscript of S i.e. 1 and i varying from 1 to N-1 with increment 2	$S_i \rightarrow D_j$ where j=(i+11) Mod N and i varying from 0 to N-2 with increment 2	$S_i \rightarrow D_j$ where j varying from (N-k-11) to 0 with decrement 2 and then from (N-2) to (N-k-11+2) with decrement 2 where k = subscript of S i.e. 1 and i varying from 1 to N-1 with increment 2
$S_0 \rightarrow D_{12}$	$S_1 \rightarrow D_3$	$S_0 \rightarrow D_{13}$	$S_1 \rightarrow D_2$
$S_2 \rightarrow D_{14}$	$S_3 \rightarrow D_1$	$S_2 \rightarrow D_{15}$	$S_3 \rightarrow D_0$
$S_4 \rightarrow D_0$	$S_5 \rightarrow D_{15}$	$S_4 \rightarrow D_1$	$S_5 \rightarrow D_{14}$
$S_6 \rightarrow D_2$	$S_7 \rightarrow D_{13}$	$S_6 \rightarrow D_3$	$S_7 \rightarrow D_{12}$
$S_8 \rightarrow D_4$	$S_9 \rightarrow D_{11}$	$S_8 \rightarrow D_5$	$S_9 \rightarrow D_{10}$
$S_{10} \rightarrow D_6$	$S_{11} \rightarrow D_9$	$S_{10} \rightarrow D_7$	$S_{11} \rightarrow D_8$
$S_{12} \rightarrow D_8$	$S_{13} \rightarrow D_7$	$S_{12} \rightarrow D_9$	$S_{13} \rightarrow D_6$
$S_{14} \rightarrow D_{10}$	$S_{15} \rightarrow D_5$	$S_{14} \rightarrow D_{11}$	$S_{15} \rightarrow D_4$

Table A1.4(n)

$S_i \rightarrow D_j$ where j=(i+9) Mod N and i varying from 1 to N-1 with increment 2	$S_i \rightarrow D_j$ where j varying from (N-k-11) to 1 with decrement 2 and then from (N-1) to (N-k-11+2) with decrement 2 where k = subscript of S i.e. 0 and i varying from 0 to N-2 with increment 2	$S_i \rightarrow D_j$ where j=(i+10) Mod N and i varying from 1 to N-1 with increment 2	$S_i \rightarrow D_j$ where j varying from (N-k-12) to 0 with decrement 2 and then from (N-2) to (N-k-12+2) with decrement 2 where k = subscript of S i.e. 0 and i varying from 0 to N-2 with increment 2
$S_1 \rightarrow D_{12}$	$S_0 \rightarrow D_3$	$S_1 \rightarrow D_{13}$	$S_0 \rightarrow D_2$
$S_3 \rightarrow D_{14}$	$S_2 \rightarrow D_1$	$S_3 \rightarrow D_{15}$	$S_2 \rightarrow D_0$
$S_5 \rightarrow D_0$	$S_4 \rightarrow D_{15}$	$S_5 \rightarrow D_1$	$S_4 \rightarrow D_{14}$
$S_7 \rightarrow D_2$	$S_6 \rightarrow D_{13}$	$S_7 \rightarrow D_3$	$S_6 \rightarrow D_{12}$
$S_9 \rightarrow D_4$	$S_8 \rightarrow D_{11}$	$S_9 \rightarrow D_5$	$S_8 \rightarrow D_{10}$
$S_{11} \rightarrow D_6$	$S_{10} \rightarrow D_9$	$S_{11} \rightarrow D_7$	$S_{10} \rightarrow D_8$
$S_{13} \rightarrow D_8$	$S_{12} \rightarrow D_7$	$S_{13} \rightarrow D_9$	$S_{12} \rightarrow D_6$
$S_{15} \rightarrow D_{10}$	$S_{14} \rightarrow D_5$	$S_{15} \rightarrow D_{11}$	$S_{14} \rightarrow D_4$

Table A1.4(o)

$S_i \rightarrow D_j$ where j=(i+10) Mod N and i varying from 0 to N-2 with increment 2	$S_i \rightarrow D_j$ where j varying from (N-k-10) to 1 with decrement 2 and then from (N-1) to (N-k-10+2) with decrement 2 where k = subscript of S i.e. 1 and i varying from 1 to N-1 with increment 2	$S_i \rightarrow D_j$ where j=(i+11) Mod N and i varying from 0 to N-2 with increment 2	$S_i \rightarrow D_j$ where j varying from (N-k-11) to 0 with decrement 2 and then from (N-2) to (N-k-11+2) with decrement 2 where k = subscript of S i.e. 1 and i varying from 1 to N-1 with increment 2
$S_0 \rightarrow D_{14}$	$S_1 \rightarrow D_1$	$S_0 \rightarrow D_{15}$	$S_1 \rightarrow D_0$
$S_2 \rightarrow D_0$	$S_3 \rightarrow D_{15}$	$S_2 \rightarrow D_1$	$S_3 \rightarrow D_{14}$
$S_4 \rightarrow D_2$	$S_5 \rightarrow D_{13}$	$S_4 \rightarrow D_3$	$S_5 \rightarrow D_{12}$
$S_6 \rightarrow D_4$	$S_7 \rightarrow D_{11}$	$S_6 \rightarrow D_5$	$S_7 \rightarrow D_{10}$
$S_8 \rightarrow D_6$	$S_9 \rightarrow D_9$	$S_8 \rightarrow D_7$	$S_9 \rightarrow D_8$
$S_{10} \rightarrow D_8$	$S_{11} \rightarrow D_7$	$S_{10} \rightarrow D_9$	$S_{11} \rightarrow D_6$
$S_{12} \rightarrow D_{10}$	$S_{13} \rightarrow D_5$	$S_{12} \rightarrow D_{11}$	$S_{13} \rightarrow D_4$
$S_{14} \rightarrow D_{12}$	$S_{15} \rightarrow D_3$	$S_{14} \rightarrow D_{13}$	$S_{15} \rightarrow D_2$

Table A1.4(p)

$S_i \rightarrow D_j$ where j=(i+9) Mod N and i varying from 1 to N-1 with increment 2	$S_i \rightarrow D_j$ where j varying from (N-k-11) to 1 with decrement 2 and then from (N-1) to (N-k-11+2) with decrement 2 where k = subscript of S i.e. 0 and i varying from 0 to N-2 with increment 2	$S_i \rightarrow D_j$ where j=(i+10) Mod N and i varying from 1 to N-1 with increment 2	$S_i \rightarrow D_j$ where j varying from (N-k-12) to 0 with decrement 2 and then from (N-2) to (N-k-12+2) with decrement 2 where k = subscript of S i.e. 0 and i varying from 0 to N-2 with increment 2
$S_1 \rightarrow D_{14}$	$S_0 \rightarrow D_1$	$S_1 \rightarrow D_{15}$	$S_0 \rightarrow D_0$
$S_3 \rightarrow D_0$	$S_2 \rightarrow D_{15}$	$S_3 \rightarrow D_1$	$S_2 \rightarrow D_{14}$
$S_5 \rightarrow D_2$	$S_4 \rightarrow D_{13}$	$S_5 \rightarrow D_3$	$S_4 \rightarrow D_{12}$
$S_7 \rightarrow D_4$	$S_6 \rightarrow D_{11}$	$S_7 \rightarrow D_5$	$S_6 \rightarrow D_{10}$
$S_9 \rightarrow D_6$	$S_8 \rightarrow D_9$	$S_9 \rightarrow D_7$	$S_8 \rightarrow D_8$
$S_{11} \rightarrow D_8$	$S_{10} \rightarrow D_7$	$S_{11} \rightarrow D_9$	$S_{10} \rightarrow D_6$
$S_{13} \rightarrow D_{10}$	$S_{12} \rightarrow D_5$	$S_{13} \rightarrow D_{11}$	$S_{12} \rightarrow D_4$
$S_{15} \rightarrow D_{12}$	$S_{14} \rightarrow D_3$	$S_{15} \rightarrow D_{13}$	$S_{14} \rightarrow D_2$

Table A1.4(a)-i

Columns → Sources ↓	Basic Table I Permutation																	
	I	II	III	IV	V	VI	VII	VIII	IX	X	XI	XII	XIII	XIV	XV	XVI		
	Destinations																	
S_0	D_0	D_1	D_0	D_1	D_0	D_1	D_0	D_1	D_0	D_1	D_0	D_1	D_0	D_1	D_0	D_1	D_1	D_0
S_2	D_2	D_3	D_3	D_2	D_2	D_3	D_2	D_3	D_2	D_3	D_2	D_3	D_2	D_3	D_2	D_3	D_2	D_3
S_4	D_4	D_5	D_4	D_5	D_5	D_4	D_4	D_5	D_4	D_5	D_4	D_5	D_4	D_5	D_4	D_5	D_4	D_5
S_6	D_6	D_7	D_6	D_7	D_6	D_7	D_7	D_6	D_6	D_7	D_6	D_7	D_6	D_7	D_6	D_7	D_6	D_7
S_8	D_8	D_9	D_8	D_9	D_8	D_9	D_8	D_9	D_9	D_8	D_8	D_9	D_8	D_9	D_8	D_9	D_8	D_9
S_{10}	D_{10}	D_{11}	D_{10}	D_{11}	D_{10}	D_{11}	D_{10}	D_{11}	D_{10}	D_{11}	D_{11}	D_{10}	D_{10}	D_{11}	D_{10}	D_{11}	D_{10}	D_{11}
S_{12}	D_{12}	D_{13}	D_{12}	D_{13}	D_{12}	D_{13}	D_{12}	D_{13}	D_{12}	D_{13}	D_{12}	D_{13}	D_{13}	D_{12}	D_{12}	D_{13}	D_{12}	D_{13}
S_{14}	D_{14}	D_{15}	D_{14}	D_{15}	D_{14}	D_{15}	D_{14}	D_{15}	D_{14}	D_{15}	D_{14}	D_{15}	D_{14}	D_{15}	D_{15}	D_{14}	D_{14}	D_{15}

Table A1.4(a)-ii

Columns → Sources ↓	Basic Table I Permutation																	
	I	II	III	IV	V	VI	VII	VIII	IX	X	XI	XII	XIII	XIV	XV	XVI		
	Destinations																	
S_1	D_{15}	D_{14}	D_{15}	D_{14}	D_{15}	D_{14}	D_{15}	D_{14}	D_{15}	D_{14}	D_{15}	D_{14}	D_{15}	D_{14}	D_{14}	D_{15}	D_{15}	D_{14}
S_3	D_{13}	D_{12}	D_{13}	D_{12}	D_{13}	D_{12}	D_{13}	D_{12}	D_{13}	D_{12}	D_{13}	D_{12}	D_{12}	D_{13}	D_{13}	D_{12}	D_{13}	D_{12}
S_5	D_{11}	D_{10}	D_{11}	D_{10}	D_{11}	D_{10}	D_{11}	D_{10}	D_{11}	D_{10}	D_{10}	D_{11}	D_{11}	D_{10}	D_{11}	D_{10}	D_{11}	D_{10}
S_7	D_9	D_8	D_9	D_8	D_9	D_8	D_9	D_8	D_8	D_9	D_9	D_8	D_9	D_8	D_9	D_8	D_9	D_8
S_9	D_7	D_6	D_8	D_6	D_7	D_6	D_6	D_7	D_7	D_6	D_7	D_6	D_7	D_6	D_7	D_6	D_7	D_6
S_{11}	D_5	D_4	D_5	D_4	D_4	D_5	D_5	D_4	D_5	D_4	D_5	D_4	D_5	D_4	D_5	D_4	D_5	D_4
S_{13}	D_3	D_2	D_2	D_3	D_3	D_2	D_3	D_2	D_3	D_2	D_3	D_2	D_3	D_2	D_3	D_2	D_3	D_2
S_{15}	D_1	D_0	D_1	D_0	D_1	D_0	D_1	D_0	D_1	D_0	D_1	D_0	D_1	D_0	D_1	D_0	D_0	D_1

Table A1.4(a)-iii

Columns → Sources ↓	Basic Table I Permutation																	
	I	II	III	IV	V	VI	VII	VIII	IX	X	XI	XII	XIII	XIV	XV	XVI		
	Destinations																	
S_0	D_0	D_1	D_0	D_1	D_0	D_1	D_0	D_1	D_0	D_1	D_0	D_1	D_0	D_1	D_1	D_0	D_1	D_0
S_2	D_2	D_3	D_3	D_2	D_2	D_3	D_2	D_3	D_2	D_3	D_2	D_3	D_2	D_3	D_2	D_3	D_3	D_2
S_4	D_4	D_5	D_5	D_4	D_5	D_4	D_4	D_5	D_4	D_5	D_4	D_5	D_4	D_5	D_4	D_5	D_4	D_5
S_6	D_6	D_7	D_6	D_7	D_7	D_6	D_7	D_6	D_6	D_7	D_6	D_7	D_6	D_7	D_6	D_7	D_6	D_7
S_8	D_8	D_9	D_8	D_9	D_8	D_9	D_9	D_8	D_9	D_8	D_8	D_9	D_8	D_9	D_8	D_9	D_8	D_9
S_{10}	D_{10}	D_{11}	D_{10}	D_{11}	D_{10}	D_{11}	D_{10}	D_{11}	D_{11}	D_{10}	D_{11}	D_{10}	D_{10}	D_{11}	D_{10}	D_{11}	D_{10}	D_{11}
S_{12}	D_{12}	D_{13}	D_{12}	D_{13}	D_{12}	D_{13}	D_{12}	D_{13}	D_{12}	D_{13}	D_{13}	D_{12}	D_{13}	D_{12}	D_{12}	D_{13}	D_{12}	D_{13}
S_{14}	D_{14}	D_{15}	D_{14}	D_{15}	D_{14}	D_{15}	D_{14}	D_{15}	D_{14}	D_{15}	D_{14}	D_{15}	D_{15}	D_{14}	D_{15}	D_{14}	D_{14}	D_{15}

Table A1.4(a)-iv

Columns → Sources ↓	I		II		III		IV		V		VI		VII		VIII		IX		X		XI		XII		XIII		XIV		XV		XVI	
	Destinations																															
S_1	D_{15}	D_{14}	D_{15}	D_{14}	D_{15}	D_{14}	D_{15}	D_{14}	D_{15}	D_{14}	D_{15}	D_{14}	D_{14}	D_{15}	D_{14}	D_{15}	D_{15}	D_{14}														
S_3	D_{13}	D_{12}	D_{13}	D_{12}	D_{13}	D_{12}	D_{13}	D_{12}	D_{13}	D_{12}	D_{12}	D_{13}	D_{12}	D_{13}	D_{13}	D_{12}	D_{13}	D_{12}														
S_5	D_{11}	D_{10}	D_{11}	D_{10}	D_{11}	D_{10}	D_{11}	D_{10}	D_{10}	D_{11}	D_{10}	D_{11}	D_{11}	D_{10}	D_{11}	D_{10}	D_{11}	D_{10}														
S_7	D_9	D_8	D_9	D_8	D_9	D_8	D_8	D_9	D_8	D_9	D_9	D_8	D_9	D_8	D_9	D_8	D_9	D_8														
S_9	D_7	D_6	D_7	D_6	D_6	D_7	D_6	D_7	D_7	D_6	D_7	D_6	D_7	D_6	D_7	D_6	D_7	D_6														
S_{11}	D_5	D_4	D_4	D_5	D_4	D_5	D_5	D_4	D_5	D_4	D_5	D_4	D_5	D_4	D_5	D_4	D_5	D_4														
S_{13}	D_3	D_2	D_2	D_3	D_3	D_2	D_3	D_2	D_3	D_2	D_3	D_2	D_3	D_2	D_3	D_2	D_2	D_3														
S_{15}	D_1	D_0	D_1	D_0	D_1	D_0	D_1	D_0	D_1	D_0	D_1	D_0	D_1	D_0	D_0	D_1	D_0	D_1														

Table A1.4(a)-v

Columns → Sources ↓	I		II		III		IV		V		VI		VII		VIII		IX		X		XI		XII		XIII		XIV		XV		XVI	
	Destinations																															
S_0	D_0	D_1	D_0	D_1	D_0	D_1	D_0	D_1	D_0	D_1	D_0	D_1	D_1	D_0	D_1	D_0	D_1	D_0														
S_2	D_2	D_3	D_3	D_2	D_2	D_3	D_2	D_3	D_2	D_3	D_2	D_3	D_2	D_3	D_3	D_2	D_3	D_2														
S_4	D_4	D_5	D_5	D_4	D_5	D_4	D_4	D_5	D_4	D_5	D_4	D_5	D_4	D_5	D_4	D_5	D_5	D_4														
S_6	D_6	D_7	D_7	D_6	D_7	D_6	D_7	D_6	D_6	D_7	D_6	D_7	D_6	D_7	D_6	D_7	D_6	D_7														
S_8	D_8	D_9	D_8	D_9	D_9	D_8	D_9	D_8	D_9	D_8	D_8	D_9	D_8	D_9	D_8	D_9	D_8	D_9														
S_{10}	D_{10}	D_{11}	D_{10}	D_{11}	D_{10}	D_{11}	D_{11}	D_{10}	D_{11}	D_{10}	D_{11}	D_{10}	D_{10}	D_{11}	D_{10}	D_{11}	D_{10}	D_{11}														
S_{12}	D_{12}	D_{13}	D_{12}	D_{13}	D_{12}	D_{13}	D_{12}	D_{13}	D_{13}	D_{12}	D_{13}	D_{12}	D_{13}	D_{12}	D_{12}	D_{13}	D_{12}	D_{13}														
S_{14}	D_{14}	D_{15}	D_{14}	D_{15}	D_{14}	D_{15}	D_{14}	D_{15}	D_{14}	D_{15}	D_{15}	D_{14}	D_{15}	D_{14}	D_{15}	D_{14}	D_{14}	D_{15}														

Table A1.4(a)-vi

Columns → Sources ↓	I		II		III		IV		V		VI		VII		VIII		IX		X		XI		XII		XIII		XIV		XV		XVI	
	Destinations																															
S_1	D_{15}	D_{14}	D_{15}	D_{14}	D_{15}	D_{14}	D_{15}	D_{14}	D_{15}	D_{14}	D_{14}	D_{15}	D_{14}	D_{15}	D_{14}	D_{15}	D_{15}	D_{14}														
S_3	D_{13}	D_{12}	D_{13}	D_{12}	D_{13}	D_{12}	D_{13}	D_{12}	D_{12}	D_{13}	D_{12}	D_{13}	D_{12}	D_{13}	D_{13}	D_{12}	D_{13}	D_{12}														
S_5	D_{11}	D_{10}	D_{11}	D_{10}	D_{11}	D_{10}	D_{10}	D_{11}	D_{10}	D_{11}	D_{10}	D_{11}	D_{11}	D_{10}	D_{11}	D_{10}	D_{11}	D_{10}														
S_7	D_9	D_8	D_9	D_8	D_8	D_9	D_8	D_9	D_8	D_9	D_9	D_8	D_9	D_8	D_9	D_8	D_9	D_8														
S_9	D_7	D_6	D_6	D_7	D_6	D_7	D_6	D_7	D_7	D_6	D_7	D_6	D_7	D_6	D_7	D_6	D_7	D_6														
S_{11}	D_5	D_4	D_4	D_5	D_4	D_5	D_5	D_4	D_5	D_4	D_5	D_4	D_5	D_4	D_5	D_4	D_4	D_5														
S_{13}	D_3	D_2	D_2	D_3	D_3	D_2	D_3	D_2	D_3	D_2	D_3	D_2	D_3	D_2	D_3	D_2	D_2	D_3														
S_{15}	D_1	D_0	D_1	D_0	D_1	D_0	D_1	D_0	D_1	D_0	D_1	D_0	D_0	D_1	D_0	D_1	D_0	D_1														

Table A1.4(a)-vii

Columns → Sources ↓	I		II		III		IV		V		VI		VII		VIII		IX		X		XI		XII		XIII		XIV		XV		XVI	
	Destinations																															
S_0	D_0	D_1	D_0	D_1	D_0	D_1	D_0	D_1	D_0	D_1	D_1	D_0	D_1	D_0	D_1	D_0	D_1	D_0														
S_2	D_2	D_3	D_3	D_2	D_2	D_3	D_2	D_3	D_2	D_3	D_2	D_3	D_3	D_2	D_3	D_2	D_3	D_2														
S_4	D_4	D_5	D_5	D_4	D_5	D_4	D_4	D_5	D_4	D_5	D_4	D_5	D_4	D_5	D_5	D_4	D_5	D_4														
S_6	D_6	D_7	D_7	D_6	D_7	D_6	D_7	D_6	D_6	D_7	D_6	D_7	D_6	D_7	D_7	D_6																
S_8	D_8	D_9	D_9	D_8	D_9	D_8	D_9	D_8	D_9	D_8	D_8	D_9	D_8	D_9	D_8	D_9																
S_{10}	D_{10}	D_{11}	D_{10}	D_{11}	D_{11}	D_{10}	D_{11}	D_{10}	D_{11}	D_{10}	D_{11}	D_{10}	D_{10}	D_{11}	D_{10}	D_{11}	D_{10}	D_{11}														
S_{12}	D_{12}	D_{13}	D_{12}	D_{13}	D_{12}	D_{13}	D_{13}	D_{12}	D_{13}	D_{12}	D_{13}	D_{12}	D_{13}	D_{12}	D_{12}	D_{13}	D_{12}	D_{13}														
S_{14}	D_{14}	D_{15}	D_{14}	D_{15}	D_{14}	D_{15}	D_{14}	D_{15}	D_{15}	D_{14}	D_{15}	D_{14}	D_{15}	D_{14}	D_{15}	D_{14}	D_{14}	D_{15}														

Table A1.4(a)-viii

Columns→→ Sources ↓	I		II		III		IV		V		VI		VII		VIII		IX		X		XI		XII		XIII		XIV		XV		XVI	
	Destinations																															
S_1	D_{15}	D_{14}	D_{15}	D_{14}	D_{15}	D_{14}	D_{15}	D_{14}	D_{15}	D_{14}	D_{15}	D_{14}	D_{14}	D_{15}	D_{14}	D_{15}	D_{15}	D_{14}														
S_3	D_{13}	D_{12}	D_{12}	D_{13}	D_{13}	D_{12}	D_{13}	D_{12}	D_{13}	D_{12}	D_{13}	D_{12}	D_{12}	D_{13}	D_{13}	D_{12}	D_{13}	D_{12}														
S_5	D_{11}	D_{10}	D_{10}	D_{11}	D_{10}	D_{11}	D_{11}	D_{10}	D_{11}	D_{10}	D_{11}	D_{10}	D_{11}	D_{10}	D_{11}	D_{10}	D_{11}	D_{10}														
S_7	D_9	D_8	D_8	D_9	D_8	D_9	D_8	D_9	D_9	D_8	D_9	D_8	D_9	D_8	D_9	D_8	D_9	D_8														
S_9	D_7	D_6	D_6	D_7	D_6	D_7	D_6	D_7	D_6	D_7	D_7	D_6	D_7	D_6	D_7	D_6	D_6	D_7														
S_{11}	D_5	D_4	D_5	D_4	D_4	D_5	D_4	D_5	D_4	D_5	D_4	D_5	D_5	D_4	D_4	D_5	D_4	D_5														
S_{13}	D_3	D_2	D_3	D_2	D_3	D_2	D_2	D_3	D_2	D_3	D_2	D_3	D_2	D_3	D_2	D_3	D_2	D_3														
S_{15}	D_1	D_0	D_1	D_0	D_1	D_0	D_1	D_0	D_0	D_1	D_0	D_1	D_0	D_1	D_0	D_1	D_0	D_1														

Table A1.4(a)-ix

Columns → Sources ↓	I		II		III		IV		V		VI		VII		VIII		IX		X		XI		XII		XIII		XIV		XV		XVI	
	Destinations																															
S_0	D_0	D_1	D_0	D_1	D_0	D_1	D_0	D_1	D_1	D_0	D_1	D_0	D_1	D_0	D_1	D_0	D_1	D_0														
S_2	D_2	D_3	D_3	D_2	D_2	D_3	D_2	D_3	D_2	D_3	D_3	D_2	D_3	D_2	D_3	D_2	D_3	D_2														
S_4	D_4	D_5	D_5	D_4	D_5	D_4	D_4	D_5	D_4	D_5	D_4	D_5	D_5	D_4	D_5	D_4	D_5	D_4														
S_6	D_6	D_7	D_7	D_6	D_7	D_6	D_7	D_6	D_6	D_7	D_6	D_7	D_6	D_7	D_7	D_6	D_7	D_6														
S_8	D_8	D_9	D_9	D_8	D_9	D_8	D_9	D_8	D_9	D_8	D_8	D_9	D_8	D_9	D_8	D_9	D_9	D_8														
S_{10}	D_{10}	D_{11}	D_{11}	D_{10}	D_{11}	D_{10}	D_{11}	D_{10}	D_{11}	D_{10}	D_{11}	D_{10}	D_{10}	D_{11}	D_{10}	D_{11}	D_{10}	D_{11}														
S_{12}	D_{12}	D_{13}	D_{12}	D_{13}	D_{13}	D_{12}	D_{13}	D_{12}	D_{13}	D_{12}	D_{13}	D_{12}	D_{13}	D_{12}	D_{12}	D_{13}	D_{12}	D_{13}														
S_{14}	D_{14}	D_{15}	D_{14}	D_{15}	D_{14}	D_{15}	D_{15}	D_{14}	D_{15}	D_{14}	D_{15}	D_{14}	D_{15}	D_{14}	D_{15}	D_{14}	D_{14}	D_{15}														

Table A1.4(a)-x

Columns→ Sources ↓	I	II	III	IV	V	VI	VII	VIII	IX	X	XI	XII	XIII	XIV	XV	XVI
	Destinations															
S_1	D_{15}	D_{14}	D_{15}	D_{14}	D_{15}	D_{14}	D_{14}	D_{15}	D_{14}	D_{15}	D_{14}	D_{15}	D_{14}	D_{15}	D_{14}	D_{15}	D_{15}	D_{14}
S_3	D_{13}	D_{12}	D_{13}	D_{12}	D_{12}	D_{13}	D_{12}	D_{13}	D_{12}	D_{13}	D_{12}	D_{13}	D_{12}	D_{13}	D_{13}	D_{12}	D_{13}	D_{12}
S_5	D_{11}	D_{10}	D_{10}	D_{11}	D_{10}	D_{11}	D_{10}	D_{11}	D_{10}	D_{11}	D_{10}	D_{11}	D_{11}	D_{10}	D_{11}	D_{10}	D_{11}	D_{10}
S_7	D_9	D_8	D_8	D_9	D_8	D_9	D_8	D_9	D_8	D_9	D_9	D_8	D_9	D_8	D_9	D_8	D_8	D_9
S_9	D_7	D_6	D_6	D_7	D_6	D_7	D_6	D_7	D_7	D_6	D_7	D_6	D_7	D_6	D_6	D_7	D_6	D_7
S_{11}	D_5	D_4	D_4	D_5	D_4	D_5	D_5	D_4	D_5	D_4	D_5	D_4	D_4	D_5	D_4	D_5	D_4	D_5
S_{13}	D_3	D_2	D_2	D_3	D_3	D_2	D_3	D_2	D_3	D_2	D_2	D_3	D_2	D_3	D_2	D_3	D_2	D_3
S_{15}	D_1	D_0	D_1	D_0	D_1	D_0	D_1	D_0	D_0	D_1	D_0	D_1	D_0	D_1	D_0	D_1	D_0	D_1

Table A1.4(a)-xi

Columns → Sources ↓	I	II	III	IV	V	VI	VII	VIII	IX	X	XI	XII	XIII	XIV	XV	XVI
	Destinations															
S_0	D_0	D_1	D_0	D_1	D_0	D_1	D_1	D_0	D_1	D_0	D_1	D_0	D_1	D_0	D_1	D_0	D_1	D_0
S_2	D_2	D_3	D_3	D_2	D_2	D_3	D_2	D_3	D_3	D_2	D_3	D_2	D_3	D_2	D_3	D_2	D_3	D_2
S_4	D_4	D_5	D_5	D_4	D_5	D_4	D_4	D_5	D_4	D_5	D_5	D_4	D_5	D_4	D_5	D_4	D_5	D_4
S_6	D_6	D_7	D_7	D_6	D_7	D_6	D_7	D_6	D_6	D_7	D_6	D_7	D_7	D_6	D_7	D_6	D_7	D_6
S_8	D_8	D_9	D_9	D_8	D_9	D_8	D_9	D_8	D_9	D_8	D_8	D_9	D_8	D_9	D_9	D_8	D_9	D_8
S_{10}	D_{10}	D_{11}	D_{11}	D_{10}	D_{11}	D_{10}	D_{11}	D_{10}	D_{11}	D_{10}	D_{11}	D_{10}	D_{10}	D_{11}	D_{10}	D_{11}	D_{11}	D_{10}
S_{12}	D_{12}	D_{13}	D_{12}	D_{12}	D_{13}	D_{12}	D_{13}	D_{12}	D_{13}	D_{12}	D_{13}	D_{12}	D_{13}	D_{12}	D_{12}	D_{13}	D_{12}	D_{13}
S_{14}	D_{14}	D_{14}	D_{14}	D_{15}	D_{15}	D_{14}	D_{15}	D_{14}	D_{15}	D_{14}	D_{15}	D_{14}	D_{15}	D_{14}	D_{15}	D_{14}	D_{14}	D_{15}

Table A1.4(a)-xii

Columns → Sources ↓	I	II	III	IV	V	VI	VII	VIII	IX	X	XI	XII	XIII	XIV	XV	XVI
	Destinations															
S_1	D_{15}	D_{14}	D_{15}	D_{14}	D_{14}	D_{15}	D_{14}	D_{15}	D_{14}	D_{15}	D_{14}	D_{15}	D_{14}	D_{15}	D_{14}	D_{15}	D_{15}	D_{14}
S_3	D_{13}	D_{12}	D_{12}	D_{13}	D_{12}	D_{13}	D_{12}	D_{13}	D_{12}	D_{13}	D_{12}	D_{13}	D_{12}	D_{13}	D_{13}	D_{12}	D_{13}	D_{12}
S_5	D_{11}	D_{10}	D_{10}	D_{11}	D_{10}	D_{11}	D_{10}	D_{11}	D_{10}	D_{11}	D_{10}	D_{11}	D_{11}	D_{10}	D_{11}	D_{10}	D_{10}	D_{11}
S_7	D_9	D_8	D_8	D_9	D_8	D_9	D_8	D_9	D_8	D_9	D_9	D_8	D_9	D_8	D_8	D_9	D_8	D_9
S_9	D_7	D_6	D_6	D_7	D_6	D_7	D_6	D_7	D_7	D_6	D_7	D_6	D_6	D_7	D_6	D_7	D_6	D_7
S_{11}	D_5	D_4	D_4	D_5	D_4	D_5	D_5	D_4	D_5	D_4	D_4	D_4	D_4	D_5	D_4	D_5	D_4	D_5
S_{13}	D_3	D_2	D_2	D_3	D_3	D_2	D_3	D_2	D_2	D_3	D_2	D_3	D_2	D_3	D_2	D_3	D_2	D_3
S_{15}	D_1	D_0	D_1	D_0	D_1	D_0	D_0	D_1	D_0	D_1	D_0	D_1	D_0	D_1	D_0	D_1	D_0	D_1

Table A1.4(a)-xiii

Columns → Sources ↓	I	II	III	IV	V	VI	VII	VIII	IX	X	XI	XII	XIII	XIV	XV	XVI
	Destinations															
S_0	D_0	D_1	D_0	D_1	D_1	D_0	D_1	D_0	D_1	D_0	D_1	D_0	D_1	D_0	D_1	D_0	D_1	D_0
S_2	D_2	D_3	D_3	D_2	D_2	D_3	D_3	D_2	D_3	D_2	D_3	D_2	D_3	D_2	D_3	D_2	D_3	D_2
S_4	D_4	D_5	D_5	D_4	D_5	D_4	D_4	D_5	D_5	D_4	D_5	D_4	D_5	D_4	D_5	D_4	D_5	D_4
S_6	D_6	D_7	D_7	D_6	D_7	D_6	D_7	D_6	D_6	D_6	D_7	D_7	D_7	D_6	D_7	D_6	D_7	D_6
S_8	D_8	D_9	D_9	D_8	D_9	D_8	D_9	D_8	D_9	D_8	D_8	D_9	D_9	D_8	D_9	D_8	D_9	D_8
S_{10}	D_{10}	D_{11}	D_{11}	D_{10}	D_{11}	D_{10}	D_{11}	D_{10}	D_{11}	D_{10}	D_{11}	D_{10}	D_{10}	D_{11}	D_{11}	D_{10}	D_{11}	D_{10}
S_{12}	D_{12}	D_{13}	D_{12}	D_{12}	D_{13}	D_{12}	D_{13}	D_{12}	D_{13}	D_{12}	D_{13}	D_{12}	D_{13}	D_{12}	D_{12}	D_{13}	D_{13}	D_{12}
S_{14}	D_{14}	D_{14}	D_{15}	D_{14}	D_{15}	D_{14}	D_{15}	D_{14}	D_{15}	D_{14}	D_{15}	D_{14}	D_{15}	D_{14}	D_{15}	D_{14}	D_{14}	D_{15}

Table A1.4(a)-xiv

Columns → Sources ↓	I	II	III	IV	V	VI	VII	VIII	IX	X	XI	XII	XIII	XIV	XV	XVI
	Destinations															
S_1	D_{15} D_{14}	D_{14} D_{15}	D_{14} D_{15}	D_{14} D_{15}	D_{14} D_{15}	D_{14} D_{15}	D_{14} D_{15}	D_{14} D_{15}	D_{14} D_{15}	D_{14} D_{15}	D_{14} D_{15}	D_{14} D_{15}	D_{14} D_{15}	D_{14} D_{15}	D_{15} D_{14}	
S_3	D_{13} D_{12}	D_{12} D_{13}	D_{12} D_{13}	D_{12} D_{13}	D_{12} D_{13}	D_{12} D_{13}	D_{12} D_{13}	D_{12} D_{13}	D_{12} D_{13}	D_{12} D_{13}	D_{12} D_{13}	D_{12} D_{13}	D_{12} D_{13}	D_{12} D_{13}	D_{12} D_{13}	
S_5	D_{11} D_{10}	D_{10} D_{11}	D_{10} D_{11}	D_{10} D_{11}	D_{10} D_{11}	D_{10} D_{11}	D_{10} D_{11}	D_{10} D_{11}	D_{10} D_{11}	D_{10} D_{11}	D_{11} D_{11}	D_{10} D_{10}	D_{11} D_{10}	D_{11} D_{10}	D_{11}	
S_7	D_9 D_8	D_8 D_9	D_8 D_9	D_8 D_9	D_8 D_9	D_8 D_9	D_8 D_9	D_8 D_9	D_9 D_9	D_8 D_8	D_9 D_8	D_9 D_8	D_9 D_8	D_9 D_8	D_9	
S_9	D_7 D_6	D_6 D_7	D_6 D_7	D_6 D_7	D_6 D_7	D_6 D_7	D_7 D_7	D_6 D_6	D_7 D_6	D_7 D_6	D_7 D_6	D_7 D_6	D_7 D_6	D_7 D_6	D_7	
S_{11}	D_5 D_4	D_4 D_5	D_4 D_5	D_4 D_5	D_5 D_4	D_4 D_5	D_4 D_4	D_5 D_4	D_5 D_4	D_4 D_5	D_5 D_4	D_5 D_4	D_5 D_4	D_5 D_4	D_5	
S_{13}	D_3 D_2	D_2 D_3	D_3 D_2	D_2 D_3	D_2 D_3	D_2 D_3	D_3 D_2	D_3 D_2	D_3 D_2	D_2 D_3	D_3 D_2	D_3 D_2	D_3 D_2	D_3 D_2	D_3	
S_{15}	D_1 D_0	D_1 D_0	D_0 D_1	D_0 D_1	D_0 D_1	D_0 D_1	D_1 D_0	D_0 D_1	D_1 D_0	D_0 D_1	D_1 D_0	D_1 D_0	D_1 D_0	D_1 D_0	D_1	

Annexure 2

Table A2.1(a)
Primary Routes from Sources to favorite Destinations (M_FDOT)

Sources	Path through the Network	Destinations
S_0, S_1	SE1,1 → SE4,1	D_0, D_1 , D_8, D_9
S_2, S_3	SE1,2 → SE4,2	D_2, D_3 , D_{10}, D_{11}
S_4, S_5	SE1,3 → SE4,3	D_4, D_5 , D_{12}, D_{13}
S_6, S_7	SE1,4 → SE4,4	D_6, D_7 , D_{14}, D_{15}
S_8, S_9	SE1,5 → SE4,5	D_0, D_1 , D_8, D_9
S_{10}, S_{11}	SE1,6 → SE4,6	D_2, D_3 , D_{10}, D_{11}
S_{12}, S_{13}	SE1,7 → SE4,7	D_4, D_5 , D_{12}, D_{13}
S_{14}, S_{15}	SE1,8 → SE4,8	D_6, D_7 , D_{14}, D_{15}

Table A2.1(b)
Primary Routes from Sources to non-favorite Destinations (M_FDOT)

Sources	Path through the Network	Destinations
S_0, S_1	SE1,1 → SE2,1 → SE3,1 → SE4,2	D_2, D_3 , D_{10}, D_{11}
S_0, S_1	SE1,1 → SE2,1 → SE3,2 → SE4,3/SE4,4	D_4,D_5 , D_{12}, D_{13},D_6,D_7,D_{14},D_{15}
S_2, S_3	SE1,2 → SE2,1 → SE3,1 → SE4,1	D_0, D_1 , D_8, D_9
S_2, S_3	SE1,2 → SE2,1 → SE3,2 → SE4,3/SE4,4	D_4, D_5 , D_{12}, D_{13},D_6,D_7,D_{14},D_{15}
S_4, S_5	SE1,3 → SE2,2 → SE3,2 → SE4,4	D_6, D_7 , D_{14}, D_{15}
S_4, S_5	SE1,3 → SE2,2 → SE3,1 → SE4,1/SE4,2	D_0,D_1 , D_8, D_9,D_2,D_3,D_{10},D_{11}
S_6, S_7	SE1,4 → SE2,2 → SE3,2 → SE4,3	D_4, D_5 , D_{12}, D_{13}
S_6, S_7	SE1,4 → SE2,2 → SE3,1 → SE4,1/SE4,2	D_0, D_1 , D_8, D_9,D_2,D_3,D_{10},D_{11}
S_8, S_9	SE1,5 → SE2,3 → SE3,3 → SE4,6	D_2, D_3 , D_{10}, D_{11}
S_8, S_9	SE1,5 → SE2,3 → SE3,4 → SE4,7/SE4,8	D_4, D_5 , D_{12}, D_{13},D_6,D_7,D_{14},D_{15}
S_{10}, S_{11}	SE1,6 → SE2,3 → SE3,3 → SE4,5	D_0, D_1 , D_8, D_9
S_{10}, S_{11}	SE1,6 → SE2,3 → SE3,4 → SE4,7/SE4,8	D_4, D_5 , D_{12}, D_{13},D_6,D_7,D_{14},D_{15}
S_{12}, S_{13}	SE1,7 → SE2,4 → SE3,4 → SE4,8	D_6, D_7 , D_{14}, D_{15}
S_{12}, S_{13}	SE1,7 → SE2,4 → SE3,3 → SE4,5/SE4,6	D_0, D_1 , D_8, D_9,D_2,D_3,D_{10},D_{11}
S_{14}, S_{15}	SE1,8 → SE2,4 → SE3,4 → SE4,7	D_4, D_5 , D_{12}, D_{13}
S_{14}, S_{15}	SE1,8 → SE2,4 → SE3,3 → SE4,5/SE4,6	D_0, D_1 , D_8, D_9,D_2,D_3,D_{10},D_{11}

Table A2.1(c)
Secondary Routes from Sources to favorite Destinations (M_FDOT)

Sources	Path through the Network	Destinations
S_0,S_1,S_8,S_9	FT1,1 → FT4,1	D_0, D_1,D_8,D_9
S_2,S_3,S_{10},S_{11}	FT1,2→ FT4,2	D_2, D_3, D_{10}, D_{11}
S_4,S_5,S_{12},S_{13}	FT1,3→ FT4,3	D_4,D_5,D_{12},D_{13}
S_6,S_7,S_{14},S_{15}	FT1,4→ FT4,4	D_6,D_7,D_{14},D_{15}

Table A2.1(d)
Secondary Routes from Sources to non-favorite Destinations (M_FDOT)

Sources	Path through the Network	Destinations
S_0,S_1,S_8,S_9	FT1,1 → FT2,1 →FT3,1 → FT4,2	D_2, D_3,D_{10},D_{11}
S_0,S_1,S_8,S_9	FT1,1 → FT2,1 →FT3,2 → FT4,3/FT4,4	$D_4,D_5,D_{12},D_{13},D_6,D_7,D_{14},D_{15}$
S_2,S_3,S_{10},S_{11}	FT1,2 → FT2,1 →FT3,1 → FT4,1	D_0,D_1,D_8,D_9
S_2,S_3,S_{10},S_{11}	FT1,2 → FT2,1 →FT3,2 → FT4,3/FT4,4	$D_4,D_5,D_{12},D_{13},D_6,D_7,D_{14},D_{15}$
S_4,S_5,S_{12},S_{13}	FT1,3 → FT2,2 →FT3,2 → FT4,4	D_6, D_7,D_{14},D_{15}
S_4,S_5,S_{12},S_{13}	FT1,3 → FT2,2 →FT3,1 → FT4,1/FT4,2	$D_0,D_1,D_8,D_9,D_2,D_3,D_{10},D_{11}$
S_6,S_7,S_{14},S_{15}	FT1,4 → FT2,2 →FT3,2 → FT4,3	D_4,D_5,D_{12},D_{13}
S_2,S_3,S_{10},S_{11}	FT1,4 → FT2,2 →FT3,1 → FT4,1/FT4,2	$D_0,D_1,D_8,D_9,D_2,D_3,D_{10},D_{11}$

Table A2.2 (a)
Prob. evaluation equations for packet availability at auxiliary ports of first stage SEs (M_FDOT)

$p_{aux\_SE11} = p_{gen\_FT11} + p_{gen\_SE15} * p_{prop\_FT11}$
$p_{aux\_SE12} = p_{gen\_FT12} + p_{gen\_SE16} * p_{prop\_FT12}$
$p_{aux\_SE13} = p_{gen\_FT13} + p_{gen\_SE17} * p_{prop\_FT13}$
$p_{aux\_SE14} = p_{gen\_FT14} + p_{gen\_SE18} * p_{prop\_FT14}$
$p_{aux\_SE15} = p_{gen\_SE11} + p_{gen\_FT11} * p_{prop\_SE11}$
$p_{aux\_SE16} = p_{gen\_SE12} + p_{gen\_FT12} * p_{prop\_SE12}$
$p_{aux\_SE17} = p_{gen\_SE13} + p_{gen\_FT13} * p_{prop\_SE13}$
$p_{aux\_SE18} = p_{gen\_SE14} + p_{gen\_FT14} * p_{prop\_SE14}$
$p_{aux\_FT11} = p_{gen\_SE15} + p_{gen\_SE11} * p_{prop\_SE15}$
$p_{aux\_FT12} = p_{gen\_SE16} + p_{gen\_SE12} * p_{prop\_SE16}$
$p_{aux\_FT13} = p_{gen\_SE17} + p_{gen\_SE13} * p_{prop\_SE17}$
$p_{aux\_FT14} = p_{gen\_SE18} + p_{gen\_SE14} * p_{prop\_SE18}$

Table A2.2 (b)
Prob. evaluation equations for packet availability at auxiliary ports of second stage SEs (M_FDOT)

$p_{aux\_SE21} = p_{gen\_FT21} + p_{gen\_SE23} * p_{prop\_FT21}$
$p_{aux\_SE22} = p_{gen\_FT22} + p_{gen\_SE24} * p_{prop\_FT22}$
$p_{aux\_SE23} = p_{gen\_SE21} + p_{gen\_FT21} * p_{prop\_SE21}$
$p_{aux\_SE24} = p_{gen\_SE22} + p_{gen\_FT22} * p_{prop\_SE22}$
$p_{aux\_FT21} = p_{gen\_SE23} + p_{gen\_SE21} * p_{prop\_SE23}$
$p_{aux\_FT22} = p_{gen\_SE24} + p_{gen\_SE22} * p_{prop\_SE24}$

Table A2.2 (c)
Prob. evaluation equations for packet availability at input ports of second stage SEs (M_FDOT)

$p_{in1\_SE21} = p_{out\_SE11}$; $p_{in2\_SE21} = p_{out\_SE12}$
$p_{in1\_SE22} = p_{out\_SE13}$; $p_{in2\_SE22} = p_{out\_SE14}$
$p_{in1\_SE23} = p_{out\_SE15}$; $p_{in2\_SE23} = p_{out\_SE16}$
$p_{in1\_SE24} = p_{out\_SE17}$; $p_{in2\_SE24} = p_{out\_SE18}$
$p_{in1\_FT21} = p_{out\_FT11}$; $p_{in2\_FT21} = p_{out\_FT12}$
$p_{in1\_FT22} = p_{out\_FT13}$; $p_{in2\_FT22} = p_{out\_FT14}$

Table A2.2 (d)
Prob. evaluation equations for packet availability at output ports of second stage SEs (M_FDOT)

$p_{out\_SE21} = 1 - (1 - p_{in1\_SE21}/b) * (1 - p_{in2\_SE21}/b) * (1 - p_{aux\_SE21}/b)$
$p_{out\_SE22} = 1 - (1 - p_{in1\_SE22}/b) * (1 - p_{in2\_SE22}/b) * (1 - p_{aux\_SE22}/b)$
$p_{out\_SE23} = 1 - (1 - p_{in1\_SE23}/b) * (1 - p_{in2\_SE23}/b) * (1 - p_{aux\_SE23}/b)$
$p_{out\_SE24} = 1 - (1 - p_{in1\_SE24}/b) * (1 - p_{in2\_SE24}/b) * (1 - p_{aux\_SE24}/b)$
$p_{out\_FT21} = 1 - (1 - p_{in1\_FT21}/b) * (1 - p_{in2\_FT21}/b) * (1 - p_{aux\_FT21}/b)$
$p_{out\_FT22} = 1 - (1 - p_{in1\_FT22}/b) * (1 - p_{in2\_FT22}/b) * (1 - p_{aux\_FT22}/b)$

Table A2.2(e)
Prob. evaluation equations for packet availability at auxiliary ports of third stage SEs (M_FDOT)

$p_{aux\_SE31} = p_{gen\_FT31} + p_{gen\_SE33} * p_{prop\_FT31}$
$p_{aux\_SE32} = p_{gen\_FT32} + p_{gen\_SE34} * p_{prop\_FT32}$
$p_{aux\_SE33} = p_{gen\_SE31} + p_{gen\_FT31} * p_{prop\_SE31}$
$p_{aux\_SE34} = p_{gen\_SE32} + p_{gen\_FT32} * p_{prop\_SE32}$
$p_{aux\_FT31} = p_{gen\_SE33} + p_{gen\_SE31} * p_{prop\_SE33}$
$p_{aux\_FT32} = p_{gen\_SE34} + p_{gen\_SE32} * p_{prop\_SE34}$

Table A2.2(f)
Prob. evaluation equations for packet availability at input ports of third stage SEs (M_FDOT)

$p_{in1\_SE31} = p_{out\_SE21}$; $p_{in2\_SE31} = p_{out\_SE22}$
$p_{in1\_SE32} = p_{out\_SE22}$; $p_{in2\_SE32} = p_{out\_SE21}$
$p_{in1\_SE33} = p_{out\_SE23}$; $p_{in2\_SE33} = p_{out\_SE24}$
$p_{in1\_SE34} = p_{out\_SE24}$; $p_{in2\_SE34} = p_{out\_SE23}$
$p_{in1\_FT31} = p_{out\_FT21}$; $p_{in2\_FT31} = p_{out\_FT22}$
$p_{in1\_FT32} = p_{out\_FT22}$; $p_{in2\_FT32} = p_{out\_FT21}$

Table A2.2(g)
Prob. evaluation equations for packet availability at output ports of third stage SEs (M_FDOT)

$p_{out\_SE31} = 1 - (1 - p_{in1\_SE31}/b) * (1 - p_{in2\_SE31}/b) * (1 - p_{aux\_SE31}/b)$
$p_{out\_SE32} = 1 - (1 - p_{in1\_SE32}/b) * (1 - p_{in2\_SE32}/b) * (1 - p_{aux\_SE32}/b)$
$p_{out\_SE33} = 1 - (1 - p_{in1\_SE33}/b) * (1 - p_{in2\_SE33}/b) * (1 - p_{aux\_SE33}/b)$
$p_{out\_SE34} = 1 - (1 - p_{in1\_SE34}/b) * (1 - p_{in2\_SE34}/b) * (1 - p_{aux\_SE34}/b)$
$p_{out\_FT31} = 1 - (1 - p_{in1\_FT31}/b) * (1 - p_{in2\_FT31}/b) * (1 - p_{aux\_FT31}/b)$
$p_{out\_FT32} = 1 - (1 - p_{in1\_FT32}/b) * (1 - p_{in2\_FT32}/b) * (1 - p_{aux\_FT32}/b)$

Table A2.2(h)
Prob. evaluation equations for packet availability at input ports of fourth stage SEs (M_FDOT)

$p_{in1\_SE41} = p_{out\_SE11}$; $p_{in2\_SE41} = p_{out\_SE31}$
$p_{in1\_SE42} = p_{out\_SE12}$; $p_{in2\_SE42} = p_{out\_SE31}$
$p_{in1\_SE43} = p_{out\_SE23}$; $p_{in2\_SE43} = p_{out\_SE24}$
$p_{in1\_SE44} = p_{out\_SE23}$; $p_{in2\_SE44} = p_{out\_SE24}$
$p_{in1\_SE45} = p_{out\_SE15}$; $p_{in1\_SE45} = p_{out\_SE15}$
$p_{in1\_SE46} = p_{out\_SE16}$; $p_{in2\_SE46} = p_{out\_SE33}$
$p_{in1\_SE47} = p_{out\_SE17}$; $p_{in2\_SE47} = p_{out\_SE34}$
$p_{in1\_SE48} = p_{out\_SE18}$; $p_{in2\_SE48} = p_{out\_SE34}$
$p_{in1\_FT41} = p_{out\_FT21}$; $p_{in2\_FT41} = p_{out\_FT23}$
$p_{in1\_FT42} = p_{out\_FT21}$; $p_{in2\_FT42} = p_{out\_FT23}$
$p_{in1\_FT43} = p_{out\_FT22}$; $p_{in2\_FT43} = p_{out\_FT24}$
$p_{in1\_FT44} = p_{out\_FT22}$; $p_{in2\_FT44} = p_{out\_FT24}$

Table A2.2(i)
Prob. evaluation equations for packet availability at output ports of fourth stage SEs (M_FDOT)

$p_{out\_SE41} = 1 - (1 - p_{in1\_SE41}/b) * (1 - p_{in2\_SE41}/b)$
$p_{out\_SE42} = 1 - (1 - p_{in1\_SE42}/b) * (1 - p_{in2\_SE42}/b)$
$p_{out\_SE43} = 1 - (1 - p_{in1\_SE43}/b) * (1 - p_{in2\_SE43}/b)$
$p_{out\_SE44} = 1 - (1 - p_{in1\_SE44}/b) * (1 - p_{in2\_SE44}/b)$
$p_{out\_SE45} = 1 - (1 - p_{in1\_SE45}/b) * (1 - p_{in2\_SE45}/b)$
$p_{out\_SE46} = 1 - (1 - p_{in1\_SE46}/b) * (1 - p_{in2\_SE46}/b)$
$p_{out\_SE47} = 1 - (1 - p_{in1\_SE47}/b) * (1 - p_{in2\_SE47}/b)$
$p_{out\_SE48} = 1 - (1 - p_{in1\_SE48}/b) * (1 - p_{in2\_SE48}/b)$
$p_{out\_FT41} = 1 - (1 - p_{in1\_FT41}/b) * (1 - p_{in2\_FT41}/b)$
$p_{out\_FT42} = 1 - (1 - p_{in1\_FT42}/b) * (1 - p_{in2\_FT42}/b)$
$p_{out\_FT43} = 1 - (1 - p_{in1\_FT43}/b) * (1 - p_{in2\_FT43}/b)$
$p_{out\_FT44} = 1 - (1 - p_{in1\_FT44}/b) * (1 - p_{in2\_FT44}/b)$

Table A2.3(a)
Primary Routes from Sources to favorite Destinations (Hybrid)

Sources	Path through the Network	Destinations
S_0, S_1	SE1,1 → SE4,1	D_0, D_1 , D_8, D_9
S_2, S_3	SE1,2 → SE4,2	D_2, D_3 , D_{10}, D_{11}
S_4, S_5	SE1,3 → SE4,3	D_4, D_5 , D_{12}, D_{13}
S_6, S_7	SE1,4 → SE4,4	D_6, D_7 , D_{14}, D_{15}
S_8, S_9	SE1,5 → SE4,5	D_0, D_1 , D_8, D_9
S_{10}, S_{11}	SE1,6 → SE4,6	D_2, D_3 , D_{10}, D_{11}
S_{12}, S_{13}	SE1,7 → SE4,7	D_4, D_5 , D_{12}, D_{13}
S_{14}, S_{15}	SE1,8 → SE4,8	D_6, D_7 , D_{14}, D_{15}

Table A2.3(b)
Primary Routes from Sources to non-favorite Destinations (Hybrid)

Sources	Path through the Network	Destinations
S_0, S_1	SE1,1 → SE2,1 → SE3,1 → SE4,2	D_2, D_3 , D_{10}, D_{11}
S_0, S_1	SE1,1 → SE2,1 → SE3,2 → SE4,3/SE4,4	D_4,D_5 , D_{12}, D_{13},D_6,D_7,D_{14},D_{15}
S_2, S_3	SE1,2 → SE2,1 → SE3,1 → SE4,1	D_0, D_1 , D_8, D_9
S_2, S_3	SE1,2 → SE2,1 → SE3,2 → SE4,3/SE4,4	D_4, D_5 , D_{12}, D_{13},D_6,D_7,D_{14},D_{15}
S_4, S_5	SE1,3 → SE2,2 → SE3,2 → SE4,4	D_6, D_7 , D_{14}, D_{15}
S_4, S_5	SE1,3 → SE2,2 → SE3,1 → SE4,1/SE4,2	D_0,D_1 , D_8, D_9,D_2,D_3,D_{10},D_{11}
S_6, S_7	SE1,4 → SE2,2 → SE3,2 → SE4,3	D_4, D_5 , D_{12}, D_{13}
S_6, S_7	SE1,4 → SE2,2 → SE3,1 → SE4,1/SE4,2	D_0, D_1 , D_8, D_9,D_2,D_3,D_{10},D_{11}
S_8, S_9	SE1,5 → SE2,3 → SE3,3 → SE4,6	D_2, D_3 , D_{10}, D_{11}
S_8, S_9	SE1,5 → SE2,3 → SE3,4 → SE4,7/SE4,8	D_4, D_5 , D_{12}, D_{13},D_6,D_7,D_{14},D_{15}
S_{10}, S_{11}	SE1,6 → SE2,3 → SE3,3 → SE4,5	D_0, D_1 , D_8, D_9
S_{10}, S_{11}	SE1,6 → SE2,3 → SE3,4 → SE4,7/SE4,8	D_4, D_5 , D_{12}, D_{13},D_6,D_7,D_{14},D_{15}
S_{12}, S_{13}	SE1,7 → SE2,4 → SE3,4 → SE4,8	D_6, D_7 , D_{14}, D_{15}
S_{12}, S_{13}	SE1,7 → SE2,4 → SE3,3 → SE4,5/SE4,6	D_0, D_1 , D_8, D_9,D_2,D_3,D_{10},D_{11}
S_{14}, S_{15}	SE1,8 → SE2,4 → SE3,4 → SE4,7	D_4, D_5 , D_{12}, D_{13}
S_{14}, S_{15}	SE1,8 → SE2,4 → SE3,3 → SE4,5/SE4,6	D_0, D_1 , D_8, D_9,D_2,D_3,D_{10},D_{11}

Table A2.3(c)
Secondary Routes from Sources to Destinations (Hybrid)

Sources	Path through the Network	Destinations
S_0, S_1,S_8,S_9	FT1,1 → FT2,1 → FT3,1 → FT4,1	D_0, D_1
S_0, S_1,S_8,S_9	FT1,1 → FT2,1 → FT3,1 → FT4,2	D_2, D_3
S_0, S_1,S_8,S_9	FT1,1 → FT2,1 → FT3,2 → FT4,3	D_4, D_5
S_0, S_1,S_8,S_9	FT1,1 → FT2,1 → FT3,2 → FT4,4	D_6, D_7
S_0, S_1,S_8,S_9	FT1,1 → FT2,2 → FT3,3 → FT4,1	D_8, D_9
S_0, S_1,S_8,S_9	FT1,1 → FT2,2 → FT3,3 → FT4,2	D_{10}, D_{11}
S_0, S_1,S_8,S_9	FT1,1 → FT2,2 → FT3,4 → FT4,3	D_{12}, D_{13}
S_0, S_1,S_8,S_9	FT1,1 → FT2,2 → FT3,4 → FT4,4	D_{14}, D_{15}
S_2, S_3,S_{10},S_{11}	FT1,2 → FT2,3 → FT3,1 → FT4,1	D_0, D_1
S_2, S_3,S_{10},S_{11}	FT1,2 → FT2,3 → FT3,1 → FT4,2	D_2, D_3
S_2, S_3,S_{10},S_{11}	FT1,2 → FT2,3 → FT3,2 → FT4,3	D_4, D_5
S_2, S_3,S_{10},S_{11}	FT1,2 → FT2,3 → FT3,2 → FT4,4	D_6, D_7
S_2, S_3,S_{10},S_{11}	FT1,2 → FT2,4 → FT3,3 → FT4,1	D_8, D_9
S_2, S_3,S_{10},S_{11}	FT1,2 → FT2,4 → FT3,3 → FT4,2	D_{10}, D_{11}
S_2, S_3,S_{10},S_{11}	FT1,2 → FT2,4 → FT3,4 → FT4,3	D_{12}, D_{13}
S_2, S_3,S_{10},S_{11}	FT1,2 → FT2,4 → FT3,4 → FT4,4	D_{14}, D_{15}
S_4, S_5,S_{12},S_{13}	FT1,3 → FT2,1 → FT3,1 → FT4,1	D_0, D_1
S_4, S_5,S_{12},S_{13}	FT1,3 → FT2,1 → FT3,1 → FT4,2	D_2, D_3
S_4, S_5,S_{12},S_{13}	FT1,3 → FT2,1 → FT3,2 → FT4,3	D_4, D_5
S_4, S_5,S_{12},S_{13}	FT1,3 → FT2,1 → FT3,2 → FT4,4	D_6, D_7
S_4, S_5,S_{12},S_{13}	FT1,3 → FT2,2 → FT3,3 → FT4,1	D_8, D_9
S_4, S_5,S_{12},S_{13}	FT1,3 → FT2,2 → FT3,3 → FT4,2	D_{10}, D_{11}
S_4, S_5,S_{12},S_{13}	FT1,3 → FT2,2 → FT3,4 → FT4,3	D_{12}, D_{13}
S_4, S_5,S_{12},S_{13}	FT1,3 → FT2,2 → FT3,4 → FT4,4	D_{14}, D_{15}
S_6, S_7,S_{14},S_{15}	FT1,4 → FT2,3 → FT3,1 → FT4,1	D_0, D_1
S_6, S_7,S_{14},S_{15}	FT1,4 → FT2,3 → FT3,1 → FT4,2	D_2, D_3
S_6, S_7,S_{14},S_{15}	FT1,4 → FT2,3 → FT3,2 → FT4,3	D_4, D_5
S_6, S_7,S_{14},S_{15}	FT1,4 → FT2,3 → FT3,2 → FT4,4	D_6, D_7
S_6, S_7,S_{14},S_{15}	FT1,4 → FT2,4 → FT3,3 → FT4,1	D_8, D_9
S_6, S_7,S_{14},S_{15}	FT1,4 → FT2,4 → FT3,3 → FT4,2	D_{10}, D_{11}
S_6, S_7,S_{14},S_{15}	FT1,4 → FT2,4 → FT3,4 → FT4,3	D_{12}, D_{13}
S_6, S_7,S_{14},S_{15}	FT1,4 → FT2,4 → FT3,4 → FT4,4	D_{14}, D_{15}

Table A2.4(a)

Prob. evaluation equations for packet availability at auxiliary ports of first stage SEs (Hybrid)

$p_{aux\_SE11} = p_{gen\_SE15} + p_{gen\_FT11} * p_{prop\_SE15}$
$p_{aux\_SE12} = p_{gen\_SE16} + p_{gen\_FT12} * p_{prop\_SE16}$
$p_{aux\_SE13} = p_{gen\_SE17} + p_{gen\_FT13} * p_{prop\_SE17}$
$p_{aux\_SE14} = p_{gen\_SE18} + p_{gen\_FT14} * p_{prop\_SE18}$
$p_{aux\_SE15} = p_{gen\_FT11} + p_{gen\_SE11} * p_{prop\_FT11}$
$p_{aux\_SE16} = p_{gen\_FT12} + p_{gen\_SE12} * p_{prop\_FT12}$
$p_{aux\_SE17} = p_{gen\_FT13} + p_{gen\_SE13} * p_{prop\_FT13}$
$p_{aux\_SE18} = p_{gen\_FT14} + p_{gen\_SE14} * p_{prop\_FT14}$
$p_{aux\_FT11} = p_{gen\_SE11} + p_{gen\_SE15} * p_{prop\_SE11}$
$p_{aux\_FT12} = p_{gen\_SE12} + p_{gen\_SE16} * p_{prop\_SE12}$
$p_{aux\_FT13} = p_{gen\_SE13} + p_{gen\_SE17} * p_{prop\_SE13}$
$p_{aux\_FT14} = p_{gen\_SE14} + p_{gen\_SE18} * p_{prop\_SE14}$

Table A2.4(b)

Prob. evaluation equations for packet availability at auxiliary ports of second stage SEs (Hybrid)

$p_{aux\_SE21} = p_{gen\_FT21}$; $p_{aux\_SE22} = p_{gen\_FT22}$
$p_{aux\_SE23} = p_{gen\_FT23}$; $p_{aux\_SE24} = p_{gen\_FT24}$
$p_{aux\_FT21} = p_{gen\_SE21}$; $p_{aux\_FT22} = p_{gen\_SE22}$
$p_{aux\_FT23} = p_{gen\_SE23}$; $p_{aux\_FT24} = p_{gen\_SE24}$

Table A2.4 (c)

Prob. evaluation equations for packet availability at input ports of second stage SEs (Hybrid)

$p_{in1\_SE21} = p_{out\_SE11}$; $p_{in2\_SE21} = p_{out\_SE12}$
$p_{in1\_SE22} = p_{out\_SE13}$; $p_{in2\_SE22} = p_{out\_SE14}$
$p_{in1\_SE23} = p_{out\_SE15}$; $p_{in2\_SE23} = p_{out\_SE16}$
$p_{in1\_SE24} = p_{out\_SE17}$; $p_{in2\_SE24} = p_{out\_SE18}$
$p_{in1\_FT21} = p_{out\_FT11}$; $p_{in2\_FT21} = p_{out\_FT13}$
$p_{in1\_FT22} = p_{out\_FT11}$; $p_{in2\_FT22} = p_{out\_FT13}$
$p_{in1\_FT23} = p_{out\_FT12}$; $p_{in2\_FT23} = p_{out\_FT14}$
$p_{in1\_FT24} = p_{out\_FT12}$; $p_{in2\_FT24} = p_{out\_FT14}$

Table A2.4(d)
Prob. evaluation equations for packet availability at output ports of second stage SEs (Hybrid)

$p_{out\_SE21} = 1 - (1 - p_{in1\_SE21}/b)*(1 - p_{in2\_SE21}/b)*(1 - p_{aux\_SE21}/b)$
$p_{out\_SE22} = 1 - (1 - p_{in1\_SE22}/b)*(1 - p_{in2\_SE22}/b)*(1 - p_{aux\_SE22}/b)$
$p_{out\_SE23} = 1 - (1 - p_{in1\_SE23}/b)*(1 - p_{in2\_SE23}/b)*(1 - p_{aux\_SE23}/b)$
$p_{out\_SE24} = 1 - (1 - p_{in1\_SE24}/b)*(1 - p_{in2\_SE24}/b)*(1 - p_{aux\_SE24}/b)$
$p_{out\_FT21} = 1 - (1 - p_{in1\_FT21}/b)*(1 - p_{in2\_FT21}/b)*(1 - p_{aux\_FT21}/b)$
$p_{out\_FT22} = 1 - (1 - p_{in1\_FT22}/b)*(1 - p_{in2\_FT22}/b)*(1 - p_{aux\_FT22}/b)$
$p_{out\_FT23} = 1 - (1 - p_{in1\_FT23}/b)*(1 - p_{in2\_FT23}/b)*(1 - p_{aux\_FT23}/b)$
$p_{out\_FT24} = 1 - (1 - p_{in1\_FT24}/b)*(1 - p_{in2\_FT24}/b)*(1 - p_{aux\_FT24}/b)$

Table A2.4(e)
Prob. evaluation equations for packet availability at auxiliary ports of third stage SEs (Hybrid)

$p_{aux\_SE31} = p_{gen\_FT31}$; $p_{aux\_SE32} = p_{gen\_FT32}$
$p_{aux\_SE33} = p_{gen\_FT33}$; $p_{aux\_SE34} = p_{gen\_FT34}$
$p_{aux\_FT31} = p_{gen\_SE31}$; $p_{aux\_FT32} = p_{gen\_SE32}$
$p_{aux\_FT33} = p_{gen\_SE33}$; $p_{aux\_FT34} = p_{gen\_SE34}$

Table A2.4(f)
Prob. evaluation equations for packet availability at input ports of third stage SEs (Hybrid)

$p_{in1\_SE31} = p_{out\_SE21}$; $p_{in2\_SE31} = p_{out\_SE22}$
$p_{in1\_SE32} = p_{out\_SE21}$; $p_{in2\_SE32} = p_{out\_SE22}$
$p_{in1\_SE33} = p_{out\_SE23}$; $p_{in2\_SE33} = p_{out\_SE24}$
$p_{in1\_SE34} = p_{out\_SE23}$; $p_{in2\_SE34} = p_{out\_SE24}$
$p_{in1\_FT31} = p_{out\_FT21}$; $p_{in2\_FT31} = p_{out\_FT23}$
$p_{in1\_FT32} = p_{out\_FT21}$; $p_{in2\_FT32} = p_{out\_FT23}$
$p_{in1\_FT33} = p_{out\_FT22}$; $p_{in2\_FT33} = p_{out\_FT24}$
$p_{in1\_FT34} = p_{out\_FT22}$; $p_{in2\_FT34} = p_{out\_FT24}$

Table A2.4 (g)

Prob. evaluation equations for packet availability at output ports of third stage SEs (Hybrid)

$p_{out\_SE31} = 1 - (1 - p_{in1\_SE31}/b) * (1 - p_{in2\_SE31}/b)*(1 - p_{aux\_SE31}/b)$
$p_{out\_SE32} = 1 - (1 - p_{in1\_SE32}/b) * (1 - p_{in2\_SE32}/b)*(1 - p_{aux\_SE32}/b)$
$p_{out\_SE33} = 1 - (1 - p_{in1\_SE33}/b) * (1 - p_{in2\_SE33}/b)*(1 - p_{aux\_SE33}/b)$
$p_{out\_SE34} = 1 - (1 - p_{in1\_SE34}/b) * (1 - p_{in2\_SE34}/b)*(1 - p_{aux\_SE34}/b)$
$p_{out\_FT31} = 1 - (1 - p_{in1\_FT31}/b) * (1 - p_{in2\_FT31}/b)*(1 - p_{aux\_FT31}/b)$
$p_{out\_FT32} = 1 - (1 - p_{in1\_FT32}/b) * (1 - p_{in2\_FT32}/b)*(1 - p_{aux\_FT32}/b)$
$p_{out\_FT33} = 1 - (1 - p_{in1\_FT33}/b) * (1 - p_{in2\_FT33}/b)*(1 - p_{aux\_FT33}/b)$
$p_{out\_FT34} = 1 - (1 - p_{in1\_FT34}/b) * (1 - p_{in2\_FT34}/b)*(1 - p_{aux\_FT34}/b)$

Table A2.4(h)

Prob. evaluation equations for packet availability at input ports of fourth stage SEs (Hybrid)

$p_{in1\_SE41} = p_{out\_SE11}$	;	$p_{in2\_SE41} = p_{out\_SE31}$
$p_{in1\_SE42} = p_{out\_SE12}$	;	$p_{in2\_SE42} = p_{out\_SE31}$
$p_{in1\_SE43} = p_{out\_SE23}$	;	$p_{in2\_SE43} = p_{out\_SE24}$
$p_{in1\_SE44} = p_{out\_SE23}$	;	$p_{in2\_SE44} = p_{out\_SE24}$
$p_{in1\_SE45} = p_{out\_SE15}$	;	$p_{in2\_SE45} = p_{out\_SE33}$
$p_{in1\_SE46} = p_{out\_SE16}$	;	$p_{in2\_SE46} = p_{out\_SE33}$
$p_{in1\_SE47} = p_{out\_SE17}$	;	$p_{in2\_SE47} = p_{out\_SE34}$
$p_{in1\_SE48} = p_{out\_SE18}$	;	$p_{in2\_SE48} = p_{out\_SE34}$
$p_{in1\_FT41} = p_{out\_FT21}$	;	$p_{in2\_FT41} = p_{out\_FT23}$
$p_{in1\_FT42} = p_{out\_FT21}$	;	$p_{in2\_FT42} = p_{out\_FT23}$
$p_{in1\_FT43} = p_{out\_FT22}$	;	$p_{in2\_FT43} = p_{out\_FT24}$
$p_{in1\_FT44} = p_{out\_FT22}$	;	$p_{in2\_FT44} = p_{out\_FT24}$

Table A2.4(i)
Prob. evaluation equations for packet availability at output ports of fourth stage SEs (Hybrid)

$p_{out\_SE41} = 1 - (1 - p_{in1\_SE41}/b) * (1 - p_{in2\_SE41}/b)$
$p_{out\_SE42} = 1 - (1 - p_{in1\_SE42}/b) * (1 - p_{in2\_SE42}/b)$
$p_{out\_SE43} = 1 - (1 - p_{in1\_SE43}/b) * (1 - p_{in2\_SE43}/b)$
$p_{out\_SE44} = 1 - (1 - p_{in1\_SE44}/b) * (1 - p_{in2\_SE44}/b)$
$p_{out\_SE45} = 1 - (1 - p_{in1\_SE45}/b) * (1 - p_{in2\_SE45}/b)$
$p_{out\_SE46} = 1 - (1 - p_{in1\_SE46}/b) * (1 - p_{in2\_SE46}/b)$
$p_{out\_SE47} = 1 - (1 - p_{in1\_SE47}/b) * (1 - p_{in2\_SE47}/b)$
$p_{out\_SE48} = 1 - (1 - p_{in1\_SE48}/b) * (1 - p_{in2\_SE48}/b)$
$p_{out\_FT41} = 1 - (1 - p_{in1\_FT41}/b) * (1 - p_{in2\_FT41}/b)$
$p_{out\_FT42} = 1 - (1 - p_{in1\_FT42}/b) * (1 - p_{in2\_FT42}/b)$
$p_{out\_FT43} = 1 - (1 - p_{in1\_FT43}/b) * (1 - p_{in2\_FT43}/b)$
$p_{out\_FT44} = 1 - (1 - p_{in1\_FT44}/b) * (1 - p_{in2\_FT44}/b)$

Table A2.5(a)
Primary Routes from Sources to favorite Destinations (M_QUAD)

Sources	Path through the Network	Destinations
S_0, S_1	SE1,1 → SE5,1	D_0, D_1 , D_8, D_9
S_2, S_3	SE1,2 → SE5,2	D_2, D_3 , D_{10}, D_{11}
S_4, S_5	SE1,3 → SE5,3	D_4, D_5 , D_{12}, D_{13}
S_6, S_7	SE1,4 → SE5,4	D_6, D_7 , D_{14}, D_{15}
S_8, S_9	SE1,5 → SE5,5	D_0, D_1 , D_8, D_9
S_{10}, S_{11}	SE1,6 → SE5,6	D_2, D_3 , D_{10}, D_{11}
S_{12}, S_{13}	SE1,7 → SE5,7	D_4, D_5 , D_{12}, D_{13}
S_{14}, S_{15}	SE1,8 → SE5,8	D_6, D_7 , D_{14}, D_{15}

Table A2.5(b)
Primary Routes from Sources to Non-favorite Destinations (M_QUAD)

Sources	Path through the Network	Destinations
S_0, S_1	SE1,1 → SE2,1 → SE4,1 → SE5,2	D_2, D_3 , D_{10}, D_{11}
S_0, S_1	SE1,1 → SE2,1 → SE3,1 → SE4,2 → SE5,3/SE5,4	D_4,D_5 , D_{12}, D_{13},D_6,D_7,D_{14},D_{15}
S_2, S_3	SE1,2 → SE2,1 → SE4,1 → SE5,1	D_0, D_1 , D_8, D_9
S_2, S_3	SE1,2 → SE2,1 → SE3,1 → SE4,2→ SE5,3/SE5,4	D_4, D_5 , D_{12}, D_{13},D_6,D_7,D_{14},D_{15}
S_4, S_5	SE1,3 → SE2,2 → SE4,2 → SE5,4	D_6, D_7 , D_{14}, D_{15}
S_4, S_5	SE1,1 → SE2,2 → SE3,1 → SE4,1 → SE5,1/SE5,2	D_0,D_1 , D_8, D_9,D_2,D_3,D_{10},D_{11}
S_6, S_7	SE1,4 → SE2,2 → SE4,2 → SE5,3	D_4, D_5 , D_{12}, D_{13}
S_6, S_7	SE1,4 → SE2,2 → SE3,1 → SE4,1→ SE5,1/SE5,2	D_0, D_1 , D_8, D_9,D_2,D_3,D_{10},D_{11}
S_8, S_9	SE1,5 → SE2,3 → SE4,3 → SE5,6	D_2, D_3 , D_{10}, D_{11}
S_8, S_9	SE1,5 → SE2,3 → SE3,2 → SE4,4 → SE5,7/SE5,8	D_4, D_5 , D_{12}, D_{13},D_6,D_7,D_{14},D_{15}
S_{10}, S_{11}	SE1,6 → SE2,3 → SE4,3 → SE5,5	D_0, D_1 , D_8, D_9
S_{10}, S_{11}	SE1,6 → SE2,3 → SE3,2 → SE4,4→ SE5,7/SE5,8	D_4, D_5 , D_{12}, D_{13},D_6,D_7,D_{14},D_{15}
S_{12}, S_{13}	SE1,7 → SE2,4 → SE4,4 → SE5,8	D_6, D_7 , D_{14}, D_{15}
S_{12}, S_{13}	SE1,7 → SE2,4 → SE3,2 → SE4,3 → SE5,5/SE5,6	D_0, D_1 , D_8, D_9,D_2,D_3,D_{10},D_{11}
S_{14}, S_{15}	SE1,8 → SE2,4 → SE4,4 → SE5,7	D_4, D_5 , D_{12}, D_{13}
S_{14}, S_{15}	SE1,8 → SE2,4 → SE3,2 → SE4,3→ SE5,5/SE5,6	D_0, D_1 , D_8, D_9,D_2,D_3,D_{10},D_{11}

Table A2.5(c)
Secondary Routes from Sources to Destinations (M_QUAD)

Sources	Path through the Network	Destinations
S_0, S_1,S_8,S_9	FT1,1 → FT5,1	D_0, D_1, D_8, D_9
S_0, S_1,S_8,S_9	FT1,1 → FT2,1 → FT4,1→ FT5,2	D_2, D_3, D_{10}, D_{11}
S_0, S_1,S_8,S_9	FT1,1 → FT2,1 → FT3,1 → FT4,2→ FT5,3	D_4, D_5, D_{12}, D_{13}
S_0, S_1,S_8,S_9	FT1,1 → FT2,1 → FT3,1 → FT4,2→ FT5,4	D_6, D_7, D_{14}, D_{15}
S_2, S_3,S_{10},S_{11}	FT1,2 → FT5,2	D_2, D_3, D_{10}, D_{11}
S_2, S_3,S_{10},S_{11}	FT1,2 → FT2,1 → FT4,1→ FT5,1	D_0, D_1, D_8, D_9
S_2, S_3,S_{10},S_{11}	FT1,2 → FT2,1 → FT3,1 → FT4,2→ FT5,3	D_4, D_5, D_{12}, D_{13}
S_2, S_3,S_{10},S_{11}	FT1,2 → FT2,1 → FT3,1 → FT4,2→ FT5,4	D_6, D_7, D_{14}, D_{15}
S_4, S_5,S_{12},S_{13}	FT1,3 → FT5,3	D_4, D_5, D_{12}, D_{13}
S_4, S_5,S_{12},S_{13}	FT1,3 → FT2,2 → FT4,2 → FT5,4	D_6, D_7, D_{14}, D_{15}
S_4, S_5,S_{12},S_{13}	FT1,3 → FT2,2 → FT3,1 → FT4,1→ FT5,1	D_0, D_1, D_8, D_9
S_4, S_5,S_{12},S_{13}	FT1,3 → FT2,2 → FT3,1 → FT4,1→ FT5,2	D_2, D_3, D_{10}, D_{11}
S_6, S_7,S_{14},S_{15}	FT1,4 → FT5,4	D_6, D_7, D_{14}, D_{15}
S_6, S_7,S_{14},S_{15}	FT1,4 → FT2,2 → FT4,2 → FT5,3	D_4, D_5, D_{12}, D_{13}
S_6, S_7,S_{14},S_{15}	FT1,4 → FT2,2 → FT3,1 → FT4,1→ FT5,1	D_0, D_1, D_8, D_9
S_6, S_7,S_{14},S_{15}	FT1,3 → FT2,2 → FT3,1 → FT4,1→ FT5,2	D_2, D_3, D_{10}, D_{11}

Table A2.6(a)

Prob. evaluation equations for pkt. availability at auxiliary ports of first stage SEs (M_QUAD)

$p_{aux\_SE11} = p_{gen\_SE15} + p_{gen\_FT11} * p_{prop\_SE15}$
$p_{aux\_SE12} = p_{gen\_SE16} + p_{gen\_FT12} * p_{prop\_SE16}$
$p_{aux\_SE13} = p_{gen\_SE17} + p_{gen\_FT13} * p_{prop\_SE17}$
$p_{aux\_SE14} = p_{gen\_SE18} + p_{gen\_FT14} * p_{prop\_SE18}$
$p_{aux\_SE15} = p_{gen\_FT11} + p_{gen\_SE11} * p_{prop\_FT11}$
$p_{aux\_SE16} = p_{gen\_FT12} + p_{gen\_SE12} * p_{prop\_FT12}$
$p_{aux\_SE17} = p_{gen\_FT13} + p_{gen\_SE13} * p_{prop\_FT13}$
$p_{aux\_SE18} = p_{gen\_FT14} + p_{gen\_SE14} * p_{prop\_FT14}$
$p_{aux\_FT11} = p_{gen\_SE11} + p_{gen\_SE15} * p_{prop\_SE11}$
$p_{aux\_FT12} = p_{gen\_SE12} + p_{gen\_SE16} * p_{prop\_SE12}$
$p_{aux\_FT13} = p_{gen\_SE13} + p_{gen\_SE17} * p_{prop\_SE13}$
$p_{aux\_FT14} = p_{gen\_SE14} + p_{gen\_SE18} * p_{prop\_SE14}$

Table A2.6(b)

Prob. evaluation equations for pkt availability at auxiliary ports of second stage SEs (M_QUAD)

$p_{aux\_SE21} = p_{gen\_SE23} + p_{gen\_FT21} * p_{prop\_SE23}$
$p_{aux\_SE22} = p_{gen\_SE24} + p_{gen\_FT22} * p_{prop\_SE24}$
$p_{aux\_SE23} = p_{gen\_FT21} + p_{gen\_SE21} * p_{prop\_FT21}$
$p_{aux\_SE24} = p_{gen\_FT22} + p_{gen\_SE22} * p_{prop\_FT22}$
$p_{aux\_FT21} = p_{gen\_SE21} + p_{gen\_SE23} * p_{prop\_SE21}$
$p_{aux\_FT22} = p_{gen\_SE22} + p_{gen\_SE24} * p_{prop\_SE22}$

Table A2.6(c)
Prob. evaluation equations for packet availability at input ports of second stage SEs (M_QUAD)

$p_{in1\_SE21} = p_{out\_SE11}$; $p_{in2\_SE21} = p_{out\_SE12}$
$p_{in1\_SE22} = p_{out\_SE13}$; $p_{in2\_SE22} = p_{out\_SE14}$
$p_{in1\_SE23} = p_{out\_SE15}$; $p_{in2\_SE23} = p_{out\_SE16}$
$p_{in1\_SE24} = p_{out\_SE17}$; $p_{in2\_SE24} = p_{out\_SE18}$
$p_{in1\_FT21} = p_{out\_FT11}$; $p_{in2\_FT21} = p_{out\_FT12}$
$p_{in1\_FT22} = p_{out\_FT13}$; $p_{in2\_FT22} = p_{out\_FT14}$

Table A2.6(d)
Prob. evaluation equations for packet availability at output ports of second stage SEs (M_QUAD)

$p_{out\_SE21} = 1 - (1 - p_{in1\_SE21}/b)*(1 - p_{in2\_SE21}/b)*(1 - p_{aux\_SE21}/b)$
$p_{out\_SE22} = 1 - (1 - p_{in1\_SE22}/b)*(1 - p_{in2\_SE22}/b)*(1 - p_{aux\_SE22}/b)$
$p_{out\_SE23} = 1 - (1 - p_{in1\_SE23}/b)*(1 - p_{in2\_SE23}/b)*(1 - p_{aux\_SE23}/b)$
$p_{out\_SE24} = 1 - (1 - p_{in1\_SE24}/b)*(1 - p_{in2\_SE24}/b)*(1 - p_{aux\_SE24}/b)$
$p_{out\_FT21} = 1 - (1 - p_{in1\_FT21}/b)*(1 - p_{in2\_FT21}/b)*(1 - p_{aux\_FT21}/b)$
$p_{out\_FT22} = 1 - (1 - p_{in1\_FT22}/b)*(1 - p_{in2\_FT22}/b)*(1 - p_{aux\_FT22}/b)$

Table A2.6(e)
Prob. evaluation equations for packet availability at auxiliary ports of third stage SEs (M_QUAD)

$p_{aux\_SE31} = p_{gen\_SE32} + p_{gen\_FT31}*p_{prop\_SE32}$
$p_{aux\_SE32} = p_{gen\_FT31} + p_{gen\_SE31}*p_{prop\_FT31}$
$p_{aux\_FT31} = p_{gen\_SE31} + p_{gen\_SE32}*p_{prop\_SE31}$

Table A2.6(f)
Prob. evaluation equations for packet availability at input ports of third stage SEs (M_QUAD)

$p_{in1\_SE31} = p_{out\_SE21}$
$p_{in2\_SE31} = p_{out\_SE22}$
$p_{in1\_SE32} = p_{out\_SE23}$
$p_{in2\_SE32} = p_{out\_SE24}$
$p_{in1\_FT31} = p_{out\_FT21}$
$p_{in2\_FT31} = p_{out\_FT22}$

Table A2.6(g)

Prob. evaluation equations for packet availability at output ports of third stage SEs (M_QUAD)

$p_{out\_SE31} = 1 - (1 - p_{in1\_SE31}/b)*(1 - p_{in2\_SE31}/b)*(1 - p_{aux\_SE31}/b)$
$p_{out\_SE32} = 1 - (1 - p_{in1\_SE32}/b)*(1 - p_{in2\_SE32}/b)*(1 - p_{aux\_SE32}/b)$
$p_{out\_FT31} = 1 - (1 - p_{in1\_FT31}/b)*(1 - p_{in2\_FT31}/b)*(1 - p_{aux\_FT31}/b)$

Table A2.6(h)

Prob. evaluation equations for packet availability at auxiliary ports of fourth stage SEs (M_QUAD)

$p_{aux\_SE41} = p_{gen\_SE43} + p_{gen\_FT41}*p_{prop\_SE43}$
$p_{aux\_SE42} = p_{gen\_SE44} + p_{gen\_FT42}*p_{prop\_SE44}$
$p_{aux\_SE43} = p_{gen\_FT41} + p_{gen\_SE41}*p_{prop\_FT41}$
$p_{aux\_SE44} = p_{gen\_FT42} + p_{gen\_SE42}*p_{prop\_FT42}$
$p_{aux\_FT41} = p_{gen\_SE41} + p_{gen\_SE43}*p_{prop\_SE41}$
$p_{aux\_FT42} = p_{gen\_SE42} + p_{gen\_SE44}*p_{prop\_SE42}$

Table A2.6(i)

Prob. evaluation equations for packet availability at input ports of fourth stage SEs (M_QUAD)

$p_{in1\_SE41} = p_{out\_SE21}$	;	$p_{in2\_SE41} = p_{out\_SE31}$
$p_{in1\_SE42} = p_{out\_SE22}$	;	$p_{in2\_SE42} = p_{out\_SE31}$
$p_{in1\_SE43} = p_{out\_SE23}$	;	$p_{in2\_SE43} = p_{out\_SE32}$
$p_{in1\_SE44} = p_{out\_SE24}$	;	$p_{in2\_SE44} = p_{out\_SE32}$
$p_{in1\_FT41} = p_{out\_FT21}$	;	$p_{in2\_FT41} = p_{out\_FT31}$
$p_{in1\_FT42} = p_{out\_FT22}$	;	$p_{in2\_FT42} = p_{out\_FT31}$

Table A2.6(j)
Prob. evaluation equations for packet availability at output ports of fourth stage SEs (M_QUAD)

$p_{out\_SE41} = 1 - (1 - p_{in1\_SE41}/b)*(1 - p_{in2\_SE41}/b)*(1 - p_{aux\_SE41}/b)$
$p_{out\_SE42} = 1 - (1 - p_{in1\_SE42}/b)*(1 - p_{in2\_SE42}/b)*(1 - p_{aux\_SE42}/b)$
$p_{out\_SE43} = 1 - (1 - p_{in1\_SE43}/b)*(1 - p_{in2\_SE43}/b)*(1 - p_{aux\_SE43}/b)$
$p_{out\_SE44} = 1 - (1 - p_{in1\_SE44}/b)*(1 - p_{in2\_SE44}/b)*(1 - p_{aux\_SE44}/b)$
$p_{out\_FT41} = 1 - (1 - p_{in1\_FT41}/b)*(1 - p_{in2\_FT41}/b)*(1 - p_{aux\_FT41}/b)$
$p_{out\_FT42} = 1 - (1 - p_{in1\_FT42}/b)*(1 - p_{in2\_FT42}/b)*(1 - p_{aux\_FT42}/b)$

Table A2.6(k)
Prob. evaluation equations for packet availability at input ports of fifth stage SEs (M_QUAD)

$p_{in1\_SE51} = p_{out\_SE11}$	;	$p_{in2\_SE51} = p_{out\_SE41}$
$p_{in1\_SE52} = p_{out\_SE12}$	;	$p_{in2\_SE52} = p_{out\_SE41}$
$p_{in1\_SE53} = p_{out\_SE13}$	;	$p_{in2\_SE53} = p_{out\_SE42}$
$p_{in1\_SE54} = p_{out\_SE14}$	;	$p_{in2\_SE54} = p_{out\_SE24}$
$p_{in1\_SE55} = p_{out\_SE15}$	;	$p_{in2\_SE55} = p_{out\_SE43}$
$p_{in1\_SE56} = p_{out\_SE16}$	;	$p_{in2\_SE56} = p_{out\_SE43}$
$p_{in1\_SE57} = p_{out\_SE17}$	;	$p_{in2\_SE57} = p_{out\_SE44}$
$p_{in1\_SE58} = p_{out\_SE18}$	;	$p_{in2\_SE58} = p_{out\_SE44}$
$p_{in1\_FT51} = p_{out\_FT11}$	;	$p_{in2\_FT51} = p_{out\_FT41}$
$p_{in1\_FT52} = p_{out\_FT12}$	;	$p_{in2\_FT52} = p_{out\_FT41}$
$p_{in1\_FT53} = p_{out\_FT13}$	;	$p_{in2\_FT53} = p_{out\_FT42}$
$p_{in1\_FT54} = p_{out\_FT14}$	;	$p_{in2\_FT54} = p_{out\_FT42}$

Table A2.6(l)

Prob. evaluation equations for packet availability at output ports of fifth stage SEs (M_QUAD)

$p_{out\_SE51} = 1 - (1 - p_{in1\_SE51}/b) * (1 - p_{in2\_SE51}/b)$
$p_{out\_SE52} = 1 - (1 - p_{in1\_SE52}/b) * (1 - p_{in2\_SE52}/b)$
$p_{out\_SE53} = 1 - (1 - p_{in1\_SE53}/b) * (1 - p_{in2\_SE53}/b)$
$p_{out\_SE54} = 1 - (1 - p_{in1\_SE54}/b) * (1 - p_{in2\_SE54}/b)$
$p_{out\_SE55} = 1 - (1 - p_{in1\_SE55}/b) * (1 - p_{in2\_SE55}/b)$
$p_{out\_SE56} = 1 - (1 - p_{in1\_SE56}/b) * (1 - p_{in2\_SE56}/b)$
$p_{out\_SE57} = 1 - (1 - p_{in1\_SE57}/b) * (1 - p_{in2\_SE57}/b)$
$p_{out\_SE58} = 1 - (1 - p_{in1\_SE58}/b) * (1 - p_{in2\_SE58}/b)$
$p_{out\_FT51} = 1 - (1 - p_{in1\_FT51}/b) * (1 - p_{in2\_FT51}/b)$
$p_{out\_FT52} = 1 - (1 - p_{in1\_FT52}/b) * (1 - p_{in2\_FT52}/b)$
$p_{out\_FT53} = 1 - (1 - p_{in1\_FT53}/b) * (1 - p_{in2\_FT53}/b)$
$p_{out\_FT54} = 1 - (1 - p_{in1\_FT54}/b) * (1 - p_{in2\_FT54}/b)$

Table A2.7(a)

Subtable I	Subtable II
$S_i \rightarrow D_i, D_{(i+N/2) \text{ MOD } N}$ and i varying from 0 to N-2 with increment 2	$S_i \rightarrow D_{j \text{ MOD } N}, D_{(j+N/2) \text{ MOD } N}$ where j = i+2 And i varying from 1 to N-1 with increment 2
$S_0 \rightarrow D_0, D_8, D_0, D_8, D_0, D_8, D_0, D_8$	$S_1 \rightarrow D_3, D_{11}, D_3, D_{11}, D_3, D_{11}, D_3, D_{11}$
$S_2 \rightarrow D_2, D_{10}, D_{10}, D_2, D_2, D_{10}, D_2, D_{10}$	$S_3 \rightarrow D_5, D_{13}, D_{13}, D_5, D_5, D_{13}, D_5, D_{13}$
$S_4 \rightarrow D_4, D_{12}, D_4, D_{12}, D_{12}, D_4, D_4, D_{12}$	$S_5 \rightarrow D_7, D_{15}, D_7, D_{15}, D_{15}, D_7, D_7, D_{15}$
$S_6 \rightarrow D_6, D_{14}, D_6, D_{14}, D_6, D_{14}, D_{14}, D_6$	$S_7 \rightarrow D_9, D_1, D_9, D_1, D_9, D_1, D_1, D_9$
$S_8 \rightarrow D_8, D_0, D_8, D_0, D_8, D_0, D_8, D_0$	$S_9 \rightarrow D_{11}, D_3, D_{11}, D_3, D_{11}, D_3, D_{11}, D_3$
$S_{10} \rightarrow D_{10}, D_2, D_2, D_{10}, D_{10}, D_2, D_{10}, D_2$	$S_{11} \rightarrow D_{13}, D_5, D_5, D_{13}, D_{13}, D_5, D_{13}, D_5$
$S_{12} \rightarrow D_{12}, D_4, D_{12}, D_4, D_4, D_{12}, D_{12}, D_4$	$S_{13} \rightarrow D_{15}, D_7, D_{15}, D_7, D_7, D_{15}, D_{15}, D_7$
$S_{14} \rightarrow D_{14}, D_6, D_{14}, D_6, D_{14}, D_6, D_6, D_{14}$	$S_{15} \rightarrow D_1, D_9, D_1, D_9, D_1, D_9, D_9, D_1$

Table A2.7(b)

Subtable I	Subtable II
$S_i \rightarrow D_j, D_{(j+N/2) \text{ MOD } N}$ where j = i -1 and i varying from 1 to N-1 with increment 2	$S_i \rightarrow D_{j \text{ MOD } N}, D_{(j+N/2) \text{ MOD } N}$ where j = i+3 and i varying from 0 to N-2 with increment 2
$S_1 \rightarrow D_0, D_8, D_0, D_8, D_0, D_8, D_0, D_8$	$S_0 \rightarrow D_3, D_{11}, D_3, D_{11}, D_3, D_{11}, D_3, D_{11}$
$S_3 \rightarrow D_2, D_{10}, D_{10}, D_2, D_2, D_{10}, D_2, D_{10}$	$S_2 \rightarrow D_5, D_{13}, D_{13}, D_5, D_5, D_{13}, D_5, D_{13}$
$S_5 \rightarrow D_4, D_{12}, D_4, D_{12}, D_{12}, D_4, D_4, D_{12}$	$S_4 \rightarrow D_7, D_{15}, D_7, D_{15}, D_{15}, D_7, D_7, D_{15}$
$S_7 \rightarrow D_6, D_{14}, D_6, D_{14}, D_6, D_{14}, D_{14}, D_6$	$S_6 \rightarrow D_9, D_1, D_9, D_1, D_9, D_1, D_1, D_9$
$S_9 \rightarrow D_8, D_0, D_8, D_0, D_8, D_0, D_8, D_0$	$S_8 \rightarrow D_{11}, D_3, D_{11}, D_3, D_{11}, D_3, D_{11}, D_3$
$S_{11} \rightarrow D_{10}, D_2, D_2, D_{10}, D_{10}, D_2, D_{10}, D_2$	$S_{10} \rightarrow D_{13}, D_5, D_5, D_{13}, D_{13}, D_5, D_{13}, D_5$
$S_{13} \rightarrow D_{12}, D_4, D_{12}, D_4, D_4, D_{12}, D_{12}, D_4$	$S_{12} \rightarrow D_{15}, D_7, D_{15}, D_7, D_7, D_{15}, D_{15}, D_7$
$S_{15} \rightarrow D_{14}, D_6, D_{14}, D_6, D_{14}, D_6, D_6, D_{14}$	$S_{14} \rightarrow D_1, D_9, D_1, D_9, D_1, D_9, D_9, D_1$

Table A2.7(c)

Subtable I	Subtable II
$S_i \rightarrow D_{j \text{ MOD } N}, D_{(j+N/2) \text{ MOD } N}$ where j = i+1 and i varying from 0 to N-2 with increment 2	$S_i \rightarrow D_{j \text{ MOD } N}, D_{(j+N/2) \text{ MOD } N}$ where j = i+1 and i varying from 1 to N-1 with increment 2
$S_0 \rightarrow D_1, D_9, D_1, D_9, D_1, D_9, D_1, D_9$	$S_1 \rightarrow D_2, D_{10}, D_2, D_{10}, D_2, D_{10}, D_2, D_{10}$
$S_2 \rightarrow D_3, D_{11}, D_{11}, D_3, D_3, D_{11}, D_3, D_{11}$	$S_3 \rightarrow D_4, D_{12}, D_{12}, D_4, D_4, D_{12}, D_4, D_{12}$
$S_4 \rightarrow D_5, D_{13}, D_5, D_{13}, D_{13}, D_5, D_5, D_{13}$	$S_5 \rightarrow D_6, D_{14}, D_6, D_{14}, D_{14}, D_6, D_6, D_{14}$
$S_6 \rightarrow D_7, D_{15}, D_7, D_{15}, D_7, D_{15}, D_{15}, D_7$	$S_7 \rightarrow D_8, D_0, D_8, D_0, D_8, D_0, D_0, D_8$
$S_8 \rightarrow D_9, D_1, D_9, D_1, D_9, D_1, D_9, D_1$	$S_9 \rightarrow D_{10}, D_2, D_{10}, D_2, D_{10}, D_2, D_{10}, D_2$
$S_{10} \rightarrow D_{11}, D_3, D_3, D_{11}, D_{11}, D_3, D_{11}, D_3$	$S_{11} \rightarrow D_{12}, D_4, D_4, D_{12}, D_{12}, D_4, D_{12}, D_4$
$S_{12} \rightarrow D_{13}, D_5, D_{13}, D_5, D_5, D_{13}, D_{13}, D_5$	$S_{13} \rightarrow D_{14}, D_6, D_{14}, D_6, D_6, D_{14}, D_{14}, D_6$
$S_{14} \rightarrow D_{15}, D_7, D_{15}, D_7, D_{15}, D_7, D_7, D_{15}$	$S_{15} \rightarrow D_0, D_8, D_0, D_8, D_0, D_8, D_8, D_0$

Table A2.7(d)

Subtable I	Subtable II
$S_i \rightarrow D_i, D_{(i+N/2) \text{ MOD } N}$ and i varying from 1 to N-1 with increment 2	$S_i \rightarrow D_{j \text{ MOD } N}, D_{(j+N/2) \text{ MOD } N}$ where j = i+2 and i varying from 0 to N-2 with increment 2
$S_1 \rightarrow D_1, D_9, D_1, D_9, D_1, D_9, D_1, D_9$	$S_0 \rightarrow D_2, D_{10}, D_2, D_{10}, D_2, D_{10}, D_2, D_{10}$
$S_3 \rightarrow D_3, D_{11}, D_{11}, D_3, D_3, D_{11}, D_3, D_{11}$	$S_2 \rightarrow D_4, D_{12}, D_{12}, D_4, D_4, D_{12}, D_4, D_{12}$
$S_5 \rightarrow D_5, D_{13}, D_5, D_{13}, D_{13}, D_5, D_5, D_{13}$	$S_4 \rightarrow D_6, D_{14}, D_6, D_{14}, D_{14}, D_6, D_6, D_{14}$
$S_7 \rightarrow D_7, D_{15}, D_7, D_{15}, D_7, D_{15}, D_{15}, D_7$	$S_6 \rightarrow D_8, D_0, D_8, D_0, D_8, D_0, D_0, D_8$
$S_9 \rightarrow D_9, D_1, D_9, D_1, D_9, D_1, D_9, D_1$	$S_8 \rightarrow D_{10}, D_2, D_{10}, D_2, D_{10}, D_2, D_{10}, D_2$
$S_{11} \rightarrow D_{11}, D_3, D_3, D_{11}, D_{11}, D_3, D_{11}, D_3$	$S_{10} \rightarrow D_{12}, D_4, D_4, D_{12}, D_{12}, D_4, D_{12}, D_4$
$S_{13} \rightarrow D_{13}, D_5, D_{13}, D_5, D_5, D_{13}, D_{13}, D_5$	$S_{12} \rightarrow D_{14}, D_6, D_{14}, D_6, D_6, D_{14}, D_{14}, D_6$
$S_{15} \rightarrow D_{15}, D_7, D_{15}, D_7, D_{15}, D_7, D_7, D_{15}$	$S_{14} \rightarrow D_0, D_8, D_0, D_8, D_0, D_8, D_8, D_0$

Table A2.7(e)

Subtable I	Subtable II
$S_i \rightarrow D_{j \text{ MOD } N}, D_{(j+N/2) \text{ MOD } N}$ where j = i+2 and i varying from 0 to N-2 with increment 2	$S_i \rightarrow D_i, D_{(i+N/2) \text{ MOD } N}$ and i varying from 1 to N-1 with increment 2
$S_0 \rightarrow D_2, D_{10}, D_2, D_{10}, D_2, D_{10}, D_2, D_{10}$	$S_1 \rightarrow D_1, D_9, D_1, D_9, D_1, D_9, D_1, D_9$
$S_2 \rightarrow D_4, D_{12}, D_{12}, D_4, D_4, D_{12}, D_4, D_{12}$	$S_3 \rightarrow D_3, D_{11}, D_{11}, D_3, D_3, D_{11}, D_3, D_{11}$
$S_4 \rightarrow D_6, D_{14}, D_6, D_{14}, D_{14}, D_6, D_6, D_{14}$	$S_5 \rightarrow D_5, D_{13}, D_5, D_{13}, D_{13}, D_5, D_5, D_{13}$
$S_6 \rightarrow D_8, D_0, D_8, D_0, D_8, D_0, D_0, D_8$	$S_7 \rightarrow D_7, D_{15}, D_7, D_{15}, D_7, D_{15}, D_{15}, D_7$
$S_8 \rightarrow D_{10}, D_2, D_{10}, D_2, D_{10}, D_2, D_{10}, D_2$	$S_9 \rightarrow D_9, D_1, D_9, D_1, D_9, D_1, D_9, D_1$
$S_{10} \rightarrow D_{12}, D_4, D_4, D_{12}, D_{12}, D_4, D_{12}, D_4$	$S_{11} \rightarrow D_{11}, D_3, D_3, D_{11}, D_{11}, D_3, D_{11}, D_3$
$S_{12} \rightarrow D_{14}, D_6, D_{14}, D_6, D_6, D_{14}, D_{14}, D_6$	$S_{13} \rightarrow D_{13}, D_5, D_{13}, D_5, D_5, D_{13}, D_{13}, D_5$
$S_{14} \rightarrow D_0, D_8, D_0, D_8, D_0, D_8, D_8, D_0$	$S_{15} \rightarrow D_{15}, D_7, D_{15}, D_7, D_{15}, D_7, D_7, D_{15}$

Table A2.7(f)

Subtable I	Subtable II
$S_i \rightarrow D_{j \text{ MOD } N}, D_{(j+N/2) \text{ MOD } N}$ where j = i+1 and i varying from 1 to N-1 with increment 2	$S_i \rightarrow D_{j \text{ MOD } N}, D_{(j+N/2) \text{ MOD } N}$ where j = i+1 and i varying from 0 to N-2 with increment 2
$S_1 \rightarrow D_2, D_{10}, D_2, D_{10}, D_2, D_{10}, D_2, D_{10}$	$S_0 \rightarrow D_1, D_9, D_1, D_9, D_1, D_9, D_1, D_9$
$S_3 \rightarrow D_4, D_{12}, D_{12}, D_4, D_4, D_{12}, D_4, D_{12}$	$S_2 \rightarrow D_3, D_{11}, D_{11}, D_3, D_3, D_{11}, D_3, D_{11}$
$S_5 \rightarrow D_6, D_{14}, D_6, D_{14}, D_{14}, D_6, D_6, D_{14}$	$S_4 \rightarrow D_5, D_{13}, D_5, D_{13}, D_{13}, D_5, D_5, D_{13}$
$S_7 \rightarrow D_8, D_0, D_8, D_0, D_8, D_0, D_0, D_8$	$S_6 \rightarrow D_7, D_{15}, D_7, D_{15}, D_7, D_{15}, D_{15}, D_7$
$S_9 \rightarrow D_{10}, D_2, D_{10}, D_2, D_{10}, D_2, D_{10}, D_2$	$S_8 \rightarrow D_9, D_1, D_9, D_1, D_9, D_1, D_9, D_1$
$S_{11} \rightarrow D_{12}, D_4, D_4, D_{12}, D_{12}, D_4, D_{12}, D_4$	$S_{10} \rightarrow D_{11}, D_3, D_3, D_{11}, D_{11}, D_3, D_{11}, D_3$
$S_{13} \rightarrow D_{14}, D_6, D_{14}, D_6, D_6, D_{14}, D_{14}, D_6$	$S_{12} \rightarrow D_{13}, D_5, D_{13}, D_5, D_5, D_{13}, D_{13}, D_5$
$S_{15} \rightarrow D_0, D_8, D_0, D_8, D_0, D_8, D_8, D_0$	$S_{14} \rightarrow D_{15}, D_7, D_{15}, D_7, D_{15}, D_7, D_7, D_{15}$

Table A2.7(g)

Subtable I	Subtable II
$S_i \rightarrow D_{j \text{ MOD } N}, D_{(j+N/2) \text{ MOD } N}$ where j = i+3 and i varying from 0 to N-2 with increment 2	$S_i \rightarrow D_{j \text{ MOD } N}, D_{(j+N/2) \text{ MOD } N}$ where j = i+1 and i varying from 1 to N-1 with increment 2
$S_0 \rightarrow D_3, D_{11}, D_{11}, D_3, D_3, D_{11}, D_3, D_{11}$	$S_1 \rightarrow D_0, D_8, D_0, D_8, D_0, D_8, D_8, D_0$
$S_2 \rightarrow D_5, D_{13}, D_5, D_{13}, D_{13}, D_5, D_5, D_{13}$	$S_3 \rightarrow D_2, D_{10}, D_2, D_{10}, D_2, D_{10}, D_2, D_{10}$
$S_4 \rightarrow D_7, D_{15}, D_7, D_{15}, D_7, D_{15}, D_{15}, D_7$	$S_5 \rightarrow D_4, D_{12}, D_{12}, D_4, D_4, D_{12}, D_4, D_{12}$
$S_6 \rightarrow D_9, D_1, D_9, D_1, D_9, D_1, D_9, D_1$	$S_7 \rightarrow D_6, D_{14}, D_6, D_{14}, D_{14}, D_6, D_6, D_{14}$
$S_8 \rightarrow D_{11}, D_3, D_3, D_{11}, D_{11}, D_3, D_{11}, D_3$	$S_9 \rightarrow D_8, D_0, D_8, D_0, D_8, D_0, D_0, D_8$
$S_{10} \rightarrow D_{13}, D_5, D_{13}, D_5, D_5, D_{13}, D_{13}, D_5$	$S_{11} \rightarrow D_{10}, D_2, D_{10}, D_2, D_{10}, D_2, D_{10}, D_2$
$S_{12} \rightarrow D_{15}, D_7, D_{15}, D_7, D_{15}, D_7, D_7, D_{15}$	$S_{13} \rightarrow D_{12}, D_4, D_4, D_{12}, D_{12}, D_4, D_{12}, D_4$
$S_{14} \rightarrow D_1, D_9, D_1, D_9, D_1, D_9, D_1, D_9$	$S_{15} \rightarrow D_{14}, D_6, D_{14}, D_6, D_6, D_{14}, D_{14}, D_6$

Table A2.7(h)

Subtable I	Subtable II
$S_i \rightarrow D_{j \text{ MOD } N}, D_{(j+N/2) \text{ MOD } N}$ where j = i+2 and i varying from 1 to N-1 with increment 2	$S_i \rightarrow D_{j \text{ MOD } N}, D_{(j+N/2) \text{ MOD } N}$ where j = i and i varying from 0 to N-2 with increment 2
$S_1 \rightarrow D_3, D_{11}, D_{11}, D_3, D_3, D_{11}, D_3, D_{11}$	$S_0 \rightarrow D_0, D_8, D_0, D_8, D_0, D_8, D_8, D_0$
$S_3 \rightarrow D_5, D_{13}, D_5, D_{13}, D_{13}, D_5, D_5, D_{13}$	$S_2 \rightarrow D_2, D_{10}, D_2, D_{10}, D_2, D_{10}, D_2, D_{10}$
$S_5 \rightarrow D_7, D_{15}, D_7, D_{15}, D_7, D_{15}, D_{15}, D_7$	$S_4 \rightarrow D_4, D_{12}, D_{12}, D_4, D_4, D_{12}, D_4, D_{12}$
$S_7 \rightarrow D_9, D_1, D_9, D_1, D_9, D_1, D_9, D_1$	$S_6 \rightarrow D_6, D_{14}, D_6, D_{14}, D_{14}, D_6, D_6, D_{14}$
$S_9 \rightarrow D_{11}, D_3, D_3, D_{11}, D_{11}, D_3, D_{11}, D_3$	$S_8 \rightarrow D_8, D_0, D_8, D_0, D_8, D_0, D_0, D_8$
$S_{11} \rightarrow D_{13}, D_5, D_{13}, D_5, D_5, D_{13}, D_{13}, D_5$	$S_{10} \rightarrow D_{10}, D_2, D_{10}, D_2, D_{10}, D_2, D_{10}, D_2$
$S_{13} \rightarrow D_{15}, D_7, D_{15}, D_7, D_{15}, D_7, D_7, D_{15}$	$S_{12} \rightarrow D_{12}, D_4, D_4, D_{12}, D_{12}, D_4, D_{12}, D_4$
$S_{15} \rightarrow D_1, D_9, D_1, D_9, D_1, D_9, D_1, D_9$	$S_{14} \rightarrow D_{14}, D_6, D_{14}, D_6, D_6, D_{14}, D_{14}, D_6$

Table A2.7(i)

Subtable I	Subtable II
$S_i \rightarrow D_{j \text{ MOD } N}, D_{(j+N/2) \text{ MOD } N}$ where j = i+4 and i varying from 0 to N-2 with increment 2	$S_i \rightarrow D_i, D_{(i+N/2) \text{ MOD } N}$ and i varying from 1 to N-1 with increment 2
$S_0 \rightarrow D_4, D_{12}, D_4, D_{12}, D_4, D_{12}, D_4, D_{12}$	$S_1 \rightarrow D_1, D_9, D_1, D_9, D_1, D_9, D_1, D_9$
$S_2 \rightarrow D_6, D_{14}, D_{14}, D_6, D_6, D_{14}, D_6, D_{14}$	$S_3 \rightarrow D_3, D_{11}, D_{11}, D_3, D_3, D_{11}, D_3, D_{11}$
$S_4 \rightarrow D_8, D_0, D_8, D_0, D_0, D_8, D_8, D_0$	$S_5 \rightarrow D_5, D_{13}, D_5, D_{13}, D_{13}, D_5, D_5, D_{13}$
$S_6 \rightarrow D_{10}, D_2, D_{10}, D_2, D_{10}, D_2, D_2, D_{10}$	$S_7 \rightarrow D_7, D_{15}, D_7, D_{15}, D_7, D_{15}, D_{15}, D_7$
$S_8 \rightarrow D_{12}, D_4, D_{12}, D_4, D_{12}, D_4, D_{12}, D_4$	$S_9 \rightarrow D_9, D_1, D_9, D_1, D_9, D_1, D_9, D_1$
$S_{10} \rightarrow D_{14}, D_6, D_6, D_{14}, D_{14}, D_6, D_{14}, D_6$	$S_{11} \rightarrow D_{11}, D_3, D_3, D_{11}, D_{11}, D_3, D_{11}, D_3$
$S_{12} \rightarrow D_0, D_8, D_0, D_8, D_8, D_0, D_0, D_8$	$S_{13} \rightarrow D_{13}, D_5, D_{13}, D_5, D_5, D_{13}, D_{13}, D_5$
$S_{14} \rightarrow D_2, D_{10}, D_2, D_{10}, D_2, D_{10}, D_{10}, D_2$	$S_{15} \rightarrow D_{15}, D_7, D_{15}, D_7, D_{15}, D_7, D_7, D_{15}$

Table A2.7(j)

Subtable I	Subtable II
$S_i \rightarrow D_{j \text{ MOD } N}, D_{(j+N/2) \text{ MOD } N}$ where j = i+3 and i varying from 1 to N-1 with increment 2	$S_i \rightarrow D_{j \text{ MOD } N}, D_{(j+N/2) \text{ MOD } N}$ where j = i+2 and i varying from 0 to N-2 with increment 2
$S_1 \rightarrow D_4, D_{12}, D_4, D_{12}, D_4, D_{12}, D_4, D_{12}$	$S_0 \rightarrow D_1, D_9, D_1, D_9, D_1, D_9, D_1, D_9$
$S_3 \rightarrow D_6, D_{14}, D_{14}, D_6, D_6, D_{14}, D_6, D_{14}$	$S_2 \rightarrow D_3, D_{11}, D_{11}, D_3, D_3, D_{11}, D_3, D_{11}$
$S_5 \rightarrow D_8, D_0, D_8, D_0, D_0, D_8, D_8, D_0$	$S_4 \rightarrow D_5, D_{13}, D_5, D_{13}, D_{13}, D_5, D_5, D_{13}$
$S_7 \rightarrow D_{10}, D_2, D_{10}, D_2, D_{10}, D_2, D_2, D_{10}$	$S_6 \rightarrow D_7, D_{15}, D_7, D_{15}, D_7, D_{15}, D_{15}, D_7$
$S_9 \rightarrow D_{12}, D_4, D_{12}, D_4, D_{12}, D_4, D_{12}, D_4$	$S_8 \rightarrow D_9, D_1, D_9, D_1, D_9, D_1, D_9, D_1$
$S_{11} \rightarrow D_{14}, D_6, D_6, D_{14}, D_{14}, D_6, D_{14}, D_6$	$S_{10} \rightarrow D_{11}, D_3, D_3, D_{11}, D_{11}, D_3, D_{11}, D_3$
$S_{13} \rightarrow D_0, D_8, D_0, D_8, D_8, D_0, D_0, D_8$	$S_{12} \rightarrow D_{13}, D_5, D_{13}, D_5, D_5, D_{13}, D_{13}, D_5$
$S_{15} \rightarrow D_2, D_{10}, D_2, D_{10}, D_2, D_{10}, D_{10}, D_2$	$S_{14} \rightarrow D_{15}, D_7, D_{15}, D_7, D_{15}, D_7, D_7, D_{15}$

Table A2.7(k)

Subtable I	Subtable II
$S_i \rightarrow D_{j \text{ MOD } N}, D_{(j+N/2) \text{ MOD } N}$ where j = i+5 and i varying from 0 to N-2 with increment 2	$S_i \rightarrow D_{j \text{ MOD } N}, D_{(j+N/2) \text{ MOD } N}$ where j = i-1 and i varying from 1 to N-1 with increment 2
$S_0 \rightarrow D_5, D_{13}, D_5, D_{13}, D_5, D_{13}, D_5, D_{13}$	$S_1 \rightarrow D_0, D_8, D_0, D_8, D_0, D_8, D_0, D_8$
$S_2 \rightarrow D_7, D_{15}, D_{15}, D_7, D_7, D_{15}, D_7, D_{15}$	$S_3 \rightarrow D_2, D_{10}, D_2, D_{10}, D_2, D_{10}, D_2, D_{10}$
$S_4 \rightarrow D_9, D_1, D_9, D_1, D_1, D_9, D_9, D_1$	$S_5 \rightarrow D_4, D_{12}, D_4, D_{12}, D_4, D_{12}, D_4, D_{12}$
$S_6 \rightarrow D_{11}, D_3, D_{11}, D_3, D_{11}, D_3, D_3, D_{11}$	$S_7 \rightarrow D_6, D_{14}, D_6, D_{14}, D_6, D_{14}, D_6, D_{14}$
$S_8 \rightarrow D_{13}, D_5, D_{13}, D_5, D_{13}, D_5, D_{13}, D_5$	$S_9 \rightarrow D_8, D_0, D_8, D_0, D_8, D_0, D_8, D_0$
$S_{10} \rightarrow D_{15}, D_7, D_7, D_{15}, D_{15}, D_7, D_{15}, D_7$	$S_{11} \rightarrow D_{10}, D_2, D_{10}, D_2, D_{10}, D_2, D_{10}, D_2$
$S_{12} \rightarrow D_1, D_9, D_1, D_9, D_9, D_1, D_1, D_9$	$S_{13} \rightarrow D_{12}, D_4, D_{12}, D_4, D_{12}, D_4, D_{12}, D_4$
$S_{14} \rightarrow D_3, D_{11}, D_3, D_{11}, D_3, D_{11}, D_{11}, D_3$	$S_{15} \rightarrow D_{14}, D_6, D_{14}, D_6, D_{14}, D_6, D_{14}, D_6$

Table A2.7(l)

Subtable I	Subtable II
$S_i \rightarrow D_{j \text{ MOD N}}, D_{(j+N/2) \text{ MOD N}}$ where j = i+4 and i varying from 1 to N-1 with increment 2	$S_i \rightarrow D_i, D_{(i+N/2) \text{ MOD N}}$ and i varying from 0 to N-2 with increment 2
$S_1 \rightarrow D_5, D_{13}, D_5, D_{13}, D_5, D_{13}, D_5, D_{13}$	$S_0 \rightarrow D_0, D_8, D_0, D_8, D_0, D_8, D_0, D_8$
$S_3 \rightarrow D_7, D_{15}, D_{15}, D_7, D_7, D_{15}, D_7, D_{15}$	$S_2 \rightarrow D_2, D_{10}, D_2, D_{10}, D_2, D_{10}, D_2, D_{10}$
$S_5 \rightarrow D_9, D_1, D_9, D_1, D_1, D_9, D_9, D_1$	$S_4 \rightarrow D_4, D_{12}, D_4, D_{12}, D_4, D_{12}, D_4, D_{12}$
$S_7 \rightarrow D_{11}, D_3, D_{11}, D_3, D_{11}, D_3, D_3, D_{11}$	$S_6 \rightarrow D_6, D_{14}, D_6, D_{14}, D_6, D_{14}, D_6, D_{14}$
$S_9 \rightarrow D_{13}, D_5, D_{13}, D_5, D_{13}, D_5, D_{13}, D_5$	$S_8 \rightarrow D_8, D_0, D_8, D_0, D_8, D_0, D_8, D_0$
$S_{11} \rightarrow D_{15}, D_7, D_7, D_{15}, D_{15}, D_7, D_{15}, D_7$	$S_{10} \rightarrow D_{10}, D_2, D_{10}, D_2, D_{10}, D_2, D_{10}, D_2$
$S_{13} \rightarrow D_1, D_9, D_1, D_9, D_9, D_1, D_1, D_9$	$S_{12} \rightarrow D_{12}, D_4, D_{12}, D_4, D_{12}, D_4, D_{12}, D_4$
$S_{15} \rightarrow D_3, D_{11}, D_3, D_{11}, D_3, D_{11}, D_{11}, D_3$	$S_{14} \rightarrow D_{14}, D_6, D_{14}, D_6, D_{14}, D_6, D_{14}, D_6$

Table A2.7(m)

Subtable I	Subtable II
$S_i \rightarrow D_{j \text{ MOD N}}, D_{(j+N/2) \text{ MOD N}}$ where j = i+6 and i varying from 0 to N-2 with increment 2	$S_i \rightarrow D_i, D_{(i+N/2) \text{ MOD N}}$ and i varying from 1 to N-1 with increment 2
$S_0 \rightarrow D_6, D_{14}, D_6, D_{14}, D_6, D_{14}, D_6, D_{14}$	$S_1 \rightarrow D_1, D_9, D_1, D_9, D_9, D_1, D_1, D_9$
$S_2 \rightarrow D_8, D_0, D_8, D_0, D_8, D_0, D_8, D_0$	$S_3 \rightarrow D_3, D_{11}, D_3, D_{11}, D_3, D_{11}, D_{11}, D_3$
$S_4 \rightarrow D_{10}, D_2, D_{10}, D_2, D_{10}, D_2, D_{10}, D_2$	$S_5 \rightarrow D_5, D_{13}, D_5, D_{13}, D_5, D_{13}, D_5, D_{13}$
$S_6 \rightarrow D_{12}, D_4, D_{12}, D_4, D_{12}, D_4, D_{12}, D_4$	$S_7 \rightarrow D_7, D_{15}, D_{15}, D_7, D_7, D_{15}, D_7, D_{15}$
$S_8 \rightarrow D_{14}, D_6, D_{14}, D_6, D_{14}, D_6, D_{14}, D_6$	$S_9 \rightarrow D_9, D_1, D_9, D_1, D_1, D_9, D_9, D_1$
$S_{10} \rightarrow D_0, D_8, D_0, D_8, D_0, D_8, D_0, D_8$	$S_{11} \rightarrow D_{11}, D_3, D_{11}, D_3, D_{11}, D_3, D_3, D_{11}$
$S_{12} \rightarrow D_2, D_{10}, D_2, D_{10}, D_2, D_{10}, D_2, D_{10}$	$S_{13} \rightarrow D_{13}, D_5, D_{13}, D_5, D_{13}, D_5, D_{13}, D_5$
$S_{14} \rightarrow D_4, D_{12}, D_4, D_{12}, D_4, D_{12}, D_4, D_{12}$	$S_{15} \rightarrow D_{15}, D_7, D_7, D_{15}, D_{15}, D_7, D_{15}, D_7$

Table A2.7(n)

Subtable I	Subtable II
$S_i \rightarrow D_{j \text{ MOD N}}, D_{(j+N/2) \text{ MOD N}}$ where j = i+5 and i varying from 1 to N-2 with increment 2	$S_i \rightarrow D_{j \text{ MOD N}}, D_{(j+N/2) \text{ MOD N}}$ where j = i+1 and i varying from 0 to N-2 with increment 2
$S_1 \rightarrow D_6, D_{14}, D_6, D_{14}, D_6, D_{14}, D_6, D_{14}$	$S_0 \rightarrow D_1, D_9, D_1, D_9, D_9, D_1, D_1, D_9$
$S_3 \rightarrow D_8, D_0, D_8, D_0, D_8, D_0, D_8, D_0$	$S_2 \rightarrow D_3, D_{11}, D_3, D_{11}, D_3, D_{11}, D_{11}, D_3$
$S_5 \rightarrow D_{10}, D_2, D_{10}, D_2, D_{10}, D_2, D_{10}, D_2$	$S_4 \rightarrow D_5, D_{13}, D_5, D_{13}, D_5, D_{13}, D_5, D_{13}$
$S_7 \rightarrow D_{12}, D_4, D_{12}, D_4, D_{12}, D_4, D_{12}, D_4$	$S_6 \rightarrow D_7, D_{15}, D_{15}, D_7, D_7, D_{15}, D_7, D_{15}$
$S_9 \rightarrow D_{14}, D_6, D_{14}, D_6, D_{14}, D_6, D_{14}, D_6$	$S_8 \rightarrow D_9, D_1, D_9, D_1, D_1, D_9, D_9, D_1$
$S_{11} \rightarrow D_0, D_8, D_0, D_8, D_0, D_8, D_0, D_8$	$S_{10} \rightarrow D_{11}, D_3, D_{11}, D_3, D_{11}, D_3, D_3, D_{11}$
$S_{13} \rightarrow D_2, D_{10}, D_2, D_{10}, D_2, D_{10}, D_2, D_{10}$	$S_{12} \rightarrow D_{13}, D_5, D_{13}, D_5, D_{13}, D_5, D_{13}, D_5$
$S_{15} \rightarrow D_4, D_{12}, D_4, D_{12}, D_4, D_{12}, D_4, D_{12}$	$S_{14} \rightarrow D_{15}, D_7, D_7, D_{15}, D_{15}, D_7, D_{15}, D_7$

Table A2.7(o)

Subtable I	Subtable II
$S_i \rightarrow D_{j \text{ MOD } N}, D_{(j+N/2) \text{ MOD } N}$ where j = i+7 and i varying from 0 to N-2 with increment 2	$S_i \rightarrow D_j, D_{(j+N/2) \text{ MOD } N}$ where j = i-1 and i varying from 0 to N-2 with increment 2
$S_0 \rightarrow D_7, D_{15}, D_{15}, D_7, D_7, D_{15}, D_7, D_{15}$	$S_1 \rightarrow D_0, D_8, D_0, D_8, D_0, D_8, D_0, D_8$
$S_2 \rightarrow D_9, D_1, D_9, D_1, D_1, D_9, D_9, D_1$	$S_3 \rightarrow D_2, D_{10}, D_2, D_{10}, D_2, D_{10}, D_2, D_{10}$
$S_4 \rightarrow D_{11}, D_3, D_{11}, D_3, D_{11}, D_3, D_3, D_{11}$	$S_5 \rightarrow D_4, D_{12}, D_4, D_{12}, D_4, D_{12}, D_4, D_{12}$
$S_6 \rightarrow D_{13}, D_5, D_{13}, D_5, D_{13}, D_5, D_{13}, D_5$	$S_7 \rightarrow D_6, D_{14}, D_6, D_{14}, D_6, D_{14}, D_6, D_{14}$
$S_8 \rightarrow D_{15}, D_7, D_7, D_{15}, D_{15}, D_7, D_{15}, D_7$	$S_9 \rightarrow D_8, D_0, D_8, D_0, D_8, D_0, D_8, D_0$
$S_{10} \rightarrow D_1, D_9, D_1, D_9, D_9, D_1, D_1, D_9$	$S_{11} \rightarrow D_{10}, D_2, D_{10}, D_2, D_{10}, D_2, D_{10}, D_2$
$S_{12} \rightarrow D_3, D_{11}, D_3, D_{11}, D_3, D_{11}, D_{11}, D_3$	$S_{13} \rightarrow D_{12}, D_4, D_{12}, D_4, D_{12}, D_4, D_{12}, D_4$
$S_{14} \rightarrow D_5, D_{13}, D_5, D_{13}, D_5, D_{13}, D_5, D_{13}$	$S_{15} \rightarrow D_{14}, D_6, D_{14}, D_6, D_{14}, D_6, D_{14}, D_6$

Table A2.7(p)

Subtable I	Subtable II
$S_i \rightarrow D_{j \text{ MOD } N}, D_{(j+N/2) \text{ MOD } N}$ where j = i+6 and i varying from 1 to N-1 with increment 2	$S_i \rightarrow D_i, D_{(j+N/2) \text{ MOD } N}$ where j = i+6 and i varying from 0 to N-2 with increment 2
$S_1 \rightarrow D_7, D_{15}, D_{15}, D_7, D_7, D_{15}, D_7, D_{15}$	$S_0 \rightarrow D_0, D_8, D_0, D_8, D_0, D_8, D_0, D_8$
$S_3 \rightarrow D_9, D_1, D_9, D_1, D_1, D_9, D_9, D_1$	$S_2 \rightarrow D_2, D_{10}, D_2, D_{10}, D_2, D_{10}, D_2, D_{10}$
$S_5 \rightarrow D_{11}, D_3, D_{11}, D_3, D_{11}, D_3, D_3, D_{11}$	$S_4 \rightarrow D_4, D_{12}, D_4, D_{12}, D_4, D_{12}, D_4, D_{12}$
$S_7 \rightarrow D_{13}, D_5, D_{13}, D_5, D_{13}, D_5, D_{13}, D_5$	$S_6 \rightarrow D_6, D_{14}, D_6, D_{14}, D_6, D_{14}, D_6, D_{14}$
$S_9 \rightarrow D_{15}, D_7, D_7, D_{15}, D_{15}, D_7, D_{15}, D_7$	$S_8 \rightarrow D_8, D_0, D_8, D_0, D_8, D_0, D_8, D_0$
$S_{11} \rightarrow D_1, D_9, D_1, D_9, D_9, D_1, D_1, D_9$	$S_{10} \rightarrow D_{10}, D_2, D_{10}, D_2, D_{10}, D_2, D_{10}, D_2$
$S_{13} \rightarrow D_3, D_{11}, D_3, D_{11}, D_3, D_{11}, D_{11}, D_3$	$S_{12} \rightarrow D_{12}, D_4, D_{12}, D_4, D_{12}, D_4, D_{12}, D_4$
$S_{15} \rightarrow D_5, D_{13}, D_5, D_{13}, D_5, D_{13}, D_5, D_{13}$	$S_{14} \rightarrow D_{14}, D_6, D_{14}, D_6, D_{14}, D_6, D_{14}, D_6$

List of Publications

1. Sandeep Kumar, P. K. Bansal, Seema Bawa, "Modified Quad Tree Network (M_QUAD) with Architectural Analysis", International Journal of Computer System Science and Engineering (IJCSSE)*, March 2009,* CRL Publishing Ltd.

2. Sandeep Kumar, P. K. Bansal, Seema Bawa, "Modified Quad Tree Network (M_QUAD)", *Apeejay Journal of Management and Technology, January 2008.*

3. Sandeep Kumar, P. K. Bansal, Seema Bawa, "Hybrid Architecture for Multistage Interconnection Networks in Multiprocessor Systems", *Journal of the CSI, Vol. 37, No. 4, October–December 2007.*

4. Sandeep Kumar, P. K. Bansal, Seema Bawa, "Modified Augmented Shuffle Exchange Network", *Journal of the CSI, Vol. 37, No. 2, April-June 2007.*

5. Sandeep Kumar, P. K. Bansal, Seema Bawa, "Highly Fault-Tolerant Irregular Interconnection Network for Multiprocessor Systems", *Journal of the CSI, Vol. 37, No. 1, Jan-March 2007.*

6. Sandeep Kumar, P. K. Bansal, Seema Bawa, "Designing and Mathematical Modeling of Cost-Effective Fault-Tolerant Multistage Interconnection Network for Multiprocessor Systems", *Proceedings of the National Conference on Frontiers in Applied and Computational Mathematics (FACM-2005), March 2005, TIET, Patiala.*

7. Sandeep Kumar, P. K. Bansal, Seema Bawa, "Designing and Analysis of Fault-Tolerant Superb Performance Multistage Interconnection Network for Wireless Networks", *Proceedings of the National Conference on "Issues and Trends in Wireless Networks (IT-WINS2004), Dec. 2004, TIET, Patiala, pp 157-162*.

Papers Communicated

1. Sandeep Kumar, P. K. Bansal, Seema Bawa, "Permutations Realization Capability of Modified F_DOT for Multiprocessor Systems", International Jounral of Computer Systems Science and Engineering (IJCSSE), CRL Publishing Ltd.

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