Thesis

On

DESIGN OF ADAPTIVE BIASED OPERATIONAL TRANSCONDUCTANCE AMPLIFIER WITH ENHANCED DC GAIN

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Submitted By

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CERTIFICATE

I hereby declare that the work which is being presented in the dissertation entitled, **"DESIGN OF ADAPTIVE BIASED OPERATIONAL TRANSCONDUCTANCE AMPLIFIER WITH ENHANCED DC GAIN"** in partial fulfilment of the requirement for the award of degree of Master of Engineering in **VLSI Design** submitted in Electronics and Communication Engineering Department of Thapar University, Patiala, is an authentic record of my own work carried out under the supervision of **Dr. Rishikesh Pandey**, Assistant Professor, ECED and refers other researcher's work which duly listed in the reference section.

The matter presented in this dissertation has not been submitted in any University/Institute for the award of degree.

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ABSTRACT

As the transistors are continuously scaling down, it becomes necessary to reduce voltage supply and power requirements of the circuit to increase its performance and stability. For voltage-mode devices, the output impedance must be low to decrease loading effect and also these devices require large number of stages which results in increased parasitic capacitance and reduced frequency response. Whereas, current- mode devices require less number of stages with high output impedance results in improved performance and large bandwidth as compared to voltage-mode techniques. Operational transconductance amplifiers are current-mode device that takes voltage as input and produces current as output with high gain and large bandwidth. To reduce power dissipation of the circuit without affecting its performance, adaptive biasing technique has been used in proposed OTA. Also, partial positive feedback and frequency dependent current mirrors are employed to further enhance the gain and the bandwidth of the proposed circuit.

The simulations of proposed adaptive biased OTA with enhanced dc gain have been performed using Cadance Virtuoso Analog Design Environment in 180nm process technology. It is observed that the proposed circuit has high gain and high common-mode rejection ratio. The response of the circuit settles very fast with high power supply rejection ratio. Due to adaptive biasing technique used, the proposed OTA becomes highly sensitive to even very small different input with reduced mismatched effects. The proposed OTA can be used for biomedical equipments, gm-C filters, oscillators, variable resistors, capacitors etc.

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ABBREVIATIONS AND SYMBOLS

BW	Bandwidth
VCCS	Voltage Control Current Source
LV	Low-Voltage
LP	Low- Power
MOSFET	Metal Oxide Semiconductor Field Effect Transistor
CMFF	Common Mode Feed Forward
CMOS	Complementary metal-oxide semiconductor
CMRR	Common-mode rejection ratio
Op-amp	Operational amplifier
OTA	Operational transconductance amplifier
RF	Radio frequency
A or G	Gain
C	Capacitance
g_m	Transconductance
r_0	Output resistance

CHAPTER-1

INTRODUCTION

1.1 Introduction

The increasing trends towards miniaturized analog integrated circuits had given a major boost in demand of low-voltage/low-power designs. Low-power is a key requirement for portable systems such as laptops, mobile phones, communication terminal, biomedical equipments etc. Not only portable systems require low-power requirement but also non portable devices require reduced size and weight with low-power in order to reduce total energy cost and heat dissipation in devices. Integrated circuits with scaled MOSFETS are required for high functionality devices but it dissipates a large amount of heat which requires additional circuit for heat sink, that will further increases complexity, chip area and total power dissipation [1]. Therefore, low-power design becomes a major issue in designing of smart compact devices. With the reduction in feature size, there is a need to reduce the supply voltage in the circuit to increase the reliability of the device. This reduction in the voltage makes device reliable as the lower electric field inside MOSFET layers produces less risk to the thinner oxide resulted from scaled MOSFET. The continuous reduction in the supply voltage degrades the performance of device in terms of total dynamic range and device linearity [2, 3]. With the continuous trends towards reduction in supply voltage, design of high performance analog circuits becomes challenging.

Operational amplifiers (op-amp) are being used as the basic building block for many of the low frequency analog circuits. Operational amplifiers are used for various applications such as adder, multiplexer, amplifier, integrator, differentiator, filters, oscillators etc. [2-6]. But, for high frequencies designing of op-amp becomes difficult for its limits on frequency which occurs due to the presence of parasitic and stray capacitances. For high performance and large bandwidth, current-mode techniques prove quite promising as compared to voltage-mode techniques. In current-mode devices as the characteristic length of the MOSFET is scaled down, parasitic capacitances and the channel delays are reduced that leads to increase in cut-off frequency [6-8]. So, for high frequency applications, current mode circuit know as

operational transconductance amplifiers (OTAs) are promising to replace op-amp as building blocks for analog circuits and systems.
OTA is an amplifier in which differential input voltage produces the current as output. OTAs are similar to op-amp but have the added benefit that once OTA has configured, it can still control certain aspects of the operation by applying controlled biasing current [8].

Since, in general voltage is applied as input signals, so amplifiers are majorly divided into two configurations. When input and output both are voltage type, the amplifier resulted in an operational amplifier [9, 10]. When input is the voltage and current is the output, then the amplifier is called as operational transconductance amplifier. The various parameters of Op-amp and OTA are listed in Table 1.1

Table 1.1 Difference between Op-Amp and OTA

S.NO	**Parameters**	**Op-amp**	**OTA**
1	Output type	Voltage	Current
2	Frequency of operation	Low	High
3	Number of inputs	Two	Two or Three
4	Output impedance	Low	High
5	Controlling Parameter	Voltage	Voltage or Current

1.2 Motivation

Designing a high performance, low-power operational transconductance amplifiers have always been a challenging task for every designer. With increasing trend towards miniaturization of high performance analog circuits, dc gain of the circuit is decreased due to decrease in the output resistance. All the biomedical equipments and other communication devices operating at high frequencies require amplifiers with high precision, low power requirement and fast settling time with a gain of around 60 to 70dB. OTAs with large gain, wideband and high common-mode rejection ratio with reduced mismatch are required to serve the purpose effectively. The proposed

OTA has high gain, large unity gain bandwidth and is sensitive to even very small differential signals applied to it.

1.3 Key contribution

The proposed adaptive biased OTA with enhanced dc gain gives an amplified output which is sensitive to even a very fraction change in differential input voltage. The proposed circuit has reduced mismatched effects and large unity gain bandwidth. The common-mode rejection ratio is quite high which results in suppression of the effects introduced by input signals which are common to both input terminals and provides high gain for differential signals applied to it.

1.4 Organisation of the dissertation

The chapters in the dissertation are organized as follows:

Chapter 1 contains the basic introduction of operational transconductance amplifiers and difference between operational amplifiers and operational transconductance amplifiers. It also includes motivation, key contribution and the organisation of the dissertation.

Chapter 2 contains the literature review, in which gain, adaptive biasing and bandwidth enhancement techniques for low-voltage and low-power operational transconductance amplifiers are discussed..

Chapter 3 addresses a brief introduction to the operational transconductance amplifiers (OTAs). Different configurations and topologies of OTA as well as various gain and bandwidth enhancement techniques are discussed.

Chapter 4 proposes adaptive biased OTA with enhanced dc gain. In addition, the basic building block as current subtractor of proposed OTA has also been presented.

The simulation results of proposed OTA are presented in **Chapter 5**. The comparison is performed between proposed circuit and other operational transconductance circuits reported in literature till now.

Chapter 6 gives the concluding remarks and future scope of the work done in dissertation.

CHAPTER-2

LITERATURE REVIEW

The research in analog circuit design is heading towards low-voltage and low-power structures. Operational transconductance amplifiers are the best substitute of operational amplifiers for high gain and wideband analog signal processing applications. In conventional class AB operational transconductance amplifiers, there is a great trade-off between current efficiency and power dissipation. Therefore, conventional class AB OTAs have less performance to power ratio. To increase performance of OTA with less power dissipation and less settling time, various authors have proposed different methods in literature [11-21].

Wang et al. [11] have proposed different methods of partial positive feedback for gain enhancement of low power CMOS OTAs. The first gain enhancement technique includes partial positive feedback at input side and the second gain enhancement technique includes partial positive feedback at load side. By employing first technique gain and bandwidth of circuit has been increased with less harmonic distortions but linearity of circuit reduces by a small amount. On the other hand second technique increases gain and bandwidth of circuit with high linearity but it gives small signal harmonic distortions.

A low-voltage super class AB CMOS OTA with very high power efficiency and slew rate is presented in [12]. It is a simple technique to achieve low voltage, low power and fast settling time independent of slew rate. It is based on combination of Class AB differential input stage, adaptive biasing and local common-mode feedback. Adaptive biasing provides a very low quiescent current which gives low static power dissipation and it automatically boost up the dynamic current well above quiescent point whenever a large differential input is applied giving high current efficiency. This circuit gives increased gain bandwidth product and high current efficiency.

Bouzerara et al. [13] have proposed low-voltage and low-power CMOS OTA for high gain and high bandwidth with increased phase margin. In order to increase the bandwidth of the proposed circuit, feedforward capacitances are introduced which provide a feedforward path for high frequency components to directly reach the output node. In order to prevent distortion of output signals at high frequency, frequency-dependent current mirrors (FDCMs) are used. For FDCMs, resistors are introduced between gate and drain of diode connected transistors which results in a low pass filters to limit high frequency signals and allow dc and low frequency signals to pass comfortably without any distortion. Also these resistances introduced zero to the circuit which improves its stability.

The negative resistance load is used in class AB OTA to enhance gain of the circuit [14]. The work is based on current mirror OTA topology with the local feedback between the output nodes of the input stage. Local feedback behaves as a negative resistance load used for the compensation of the parasitic resistance of the input stage.

Galan et al. [15] have proposed class AB OTAs with adaptive biasing and dynamic output current scaling. The three topologies have been proposed featuring simplicity and compactness, which gives dynamic current boosting. Current boosting has been performed at both differential input stage and non-linear current source stage. Output current has been boosted proportionally to four times the differential input voltage.

The rail-to-rail fully differential OTA with high gain enhancement using current-mode adaptive biasing and positive feedback is presented in [16]. Current-mode adaptive biasing circuit is composed of simple current mirrors configured to result in a current subtractor. Negative resistance load is used at output nodes for gain enhancement. To make the circuit fully differential a common-mode feedback circuit has been employed.

Azhari et al. [17] have proposed high linear, high common-mode rejection ratio, low-power OTA with Class AB output stage. The circuit uses two linearization techniques, one with adaptive biasing of differential pair and second with resistive source degeneration. The adaptive bias circuit and CMFB circuit has enhanced the CMRR and frequency range. The Source degeneration enhances linearity but shows

significant transconductance loss, excessive power consumption and enormous area usage.

The low-power fully differential OTA utilizing adaptive biasing and partial positive feedback is presented in [18]. The circuit uses current-mode adaptive biasing, which dynamically boost the biasing current to achieve high gain with low power dissipation. To make the circuit fully differential, a simple technique of common-mode feedback (CMFB) circuit is used. This CMFB circuit provides high CMRR. The partial positive feedback is employed at input stage of OTA to increase gain of circuit by increasing the effective transconductance of the circuit.

Torfifard et al. [19] have suggested a power efficient CMOS adaptive biasing operational transconductance amplifier. The two stages OTA provides significant improvements in driving capability and power dissipation. Adaptive biasing circuit is a current subtractor based on translinear principle to provide dynamic current boosting and decrease in mismatch effects. Due to reduced mismatched effects of current source circuit and positive feedback loop, the output current is efficiently increased with decreased output distortion and high CMRR.

Sheikh [20] presented a generalized work on High frequency operational transconductance amplifier. The performance analysis of conventional OTA techniques, using advanced process technology has been reported. The effect of variation in input voltage, frequency and temperature on output voltage swing has also been presented.

The OTA based on non-linear current mirror with high slew-rate and low quiescent current is presented in [21]. The adaptive bias circuit employed has dynamically boost the differential current and non-linear current mirror alters the current mirror copying ratio depending upon input applied to further enhance gain with low power dissipation. When a large differential input is applied, the copying ratio is high and when the differential input applied is small, the copying ratio is low.

Table 2.1 Comparison of various OTAs available in literature [12-19, 21]

Reference No.	**[13]**	**[12]**	**[14]**	**[15]**	**[16]**	**[17]**	**[18]**	**[19]**	**[21]**
Year	2002	2005	2006	2007	2007	2010	2010	2013	2015
CMOS process	0.8um	0.5um	0.5um	0.5um	0.35um	0.18um	0.09um	0.18um	0.5um
Supply Voltage V	2.5	+-1	3.3	+-1	+-0.75	+-0.9	+-0.6	+-0.6	2
Capacitive Load	1pF	80pF	-	80pF	15Pf	10pF	10pF	1pF	80pF
DC Gain (db)	90	37.5	-	41	82	42	80.2	44	44.6
Phase Margin (degree)	95	90	0.2	71	81	90	84.9	68	85.1
GBW	-	470 KHz	-	2.3 MHz	6.8 MHz	3.2 MHz	9.5 MHz	590 KHz	3.95 MHz
CMRR (db)	-	69	>50	75	136	169	124	110	-
PSRR+/- (db)	-	57 46	>50	56 51	114 109	-	135 140	73 48	-
SR +/- (V/us)	-	42 80	-	14 28	25	-	37	71 -72	7 6.5
Settling Time	-	100ns 33ns	-	-	410ns	-	274us	160ns	100ns 130ns
Static Power Dissipation (uW)	7000	140	4000	140	84	250	96	0.44	137
Unity Gain Frequency	182 MHz	-	-	16 MHz	-		71.8 MHz	4 KHz	-

Table 2.1 comprises the circuit parameters of different operational transconductance amplifiers present in literature [12-19, 21]. From the table it is observed that the maximum gain achieved till now using adaptive bias OTA is 82dB at 15pF load capacitance. In this topology frequency response is very good but at the cost of slew rate and settling time.

CHAPTER-3

OPERATIONAL TRANSCONDUCTANCE AMPLIFIERS

Operational transconductance amplifier is a device which takes input in terms of voltage and gives current as output with high input and output impedances. An ideal OTA is a constant transconductance voltage controlled current source having infinite bandwidth with all the internals nodes at low impedance and infinite input and output impedances. This chapter is organised as follows: Section 3.1 describes different configurations of OTA. Section 3.2 contains different terminologies of OTA. In the Section 3.3 major concerns for CMOS OTA are described. Section 3.4 addresses different gain boosting techniques and Section 3.5 contains bandwidth enhancement techniques.

3.1 Configurations of OTAs

OTA are configured on the basis of input/output configuration and different type of topology used in each type of input/output configuration.

3.1.1 Input/output based configurations [2,7,9,10]:

Depending upon input and output configurations, OTAs are categorized into major types. These are:

- Single-input, single-output OTA

In this configuration, a single input voltage is applied with respect to ground that gives a single output as current. This configuration is generally not preferred due to high noise effects and low performance.

- Differential-input, single-output (Differential OTA)

Figure 3.1 shows a conventional class AB differential operational transconductance amplifier (OTA) [7, 10, 22]. OTA is generally used in differential mode to achieve

high noise immunity. Since the noise appears in same amount at both differential input terminals, so the common effect of the noise will be cancelled out at the output. In this configuration differential input signals are given to input transistors M1 and M2 and differential output current is obtained at drain of transistor M2. I_b is the constant biasing current. The differential output currents of both the input transistors are combined at single output node with the help of current mirrors.

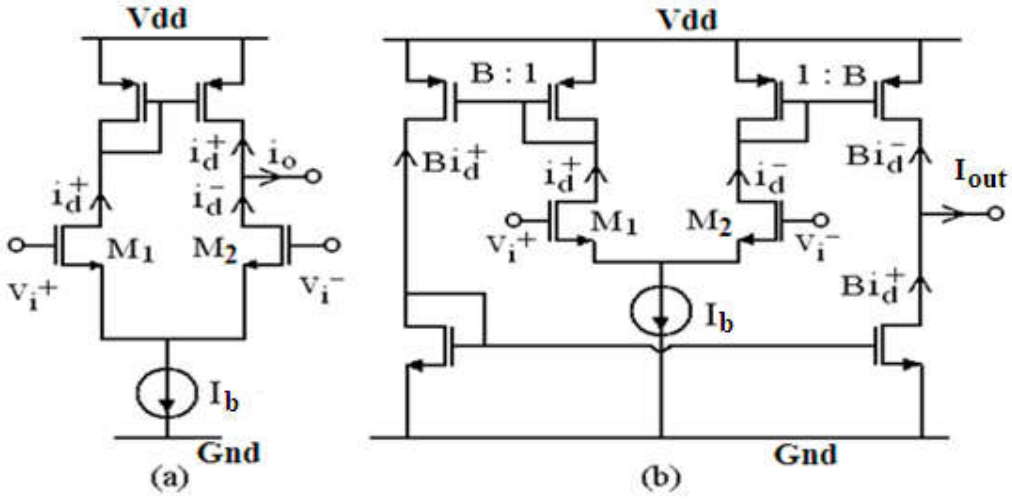

Figure 3.1 Differential-input single-output CMOS OTAs : (a) a simple OTA and (b) a balanced OTA[10]

In balanced configuration, two more PMOS current mirrors have been set with size ratio B times as compared to simple OTA. This is done in order to boost output current by B times and hence the transconductance is increased by B times. This circuit work properly only when the time delay of the current mirrors for the current combinations is negligible with respect to the operating signal cycle. The PMOS counterpart of the circuit shown in Figure 3.1(b) is used as the reference circuit. The performance of the circuit can be improved by increasing biasing current or amplifying factor B of current mirrors. Both these will increase the power dissipation of the circuit. Moreover, increasing B will increase the parasitic capacitance at the output node and hence the frequency response of the circuit degrades.

- Differential-input, differential-output (Fully differential OTA)

Figure 3.2 shows fully differential OTA [9]. Transistor M1 and M2 are input transistors and output is obtained at drain of output current mirrors with amplifying factor B.

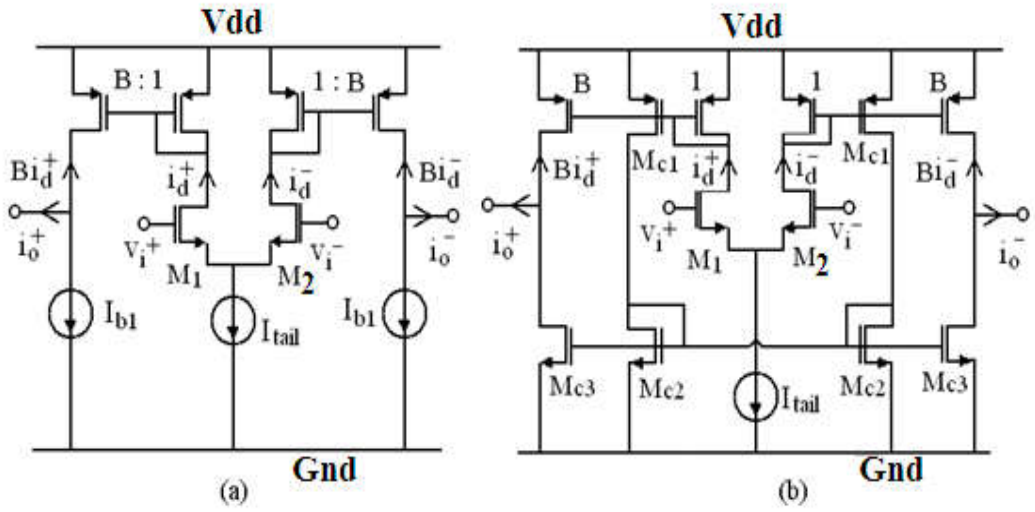

Figure 3.2 Differential-input/output CMOS OTAs: (a) a simple fully differential OTA and (b) Fully differential OTA with common-mode feed-forward circuit [9].

The part(b) has an additional common-mode feed-forward (CMFF) circuit comprising of transistors MC1, MC2 and MC3 to further enhance its common-mode rejection ratio (CMRR). Fully differential circuit provides high noise immunity but require an addition circuitry to obtain differential output current.

One more configuration is there i.e. single-input differential-output but it is not practical and is not used in any of the previous applications.

3.1.2 Configurations based on different topologies

Depending on the topologies of the circuit, OTAs are classified as single stage, multistage, cascode and folded cascode as shown in Figure 3.3. These topologies are applicable in all three configurations of OTA specified in Section 3.1.1 i.e. single input/output, differential and fully differential. For simplicity all topologies are shown

only for single input/output configuration.

The Figure 3.3(a) shows single-NMOS common-source transconductor. The circuit shown is quite simple but it gives low output impedance due to Miller effect. Also linearity of the circuit is low.

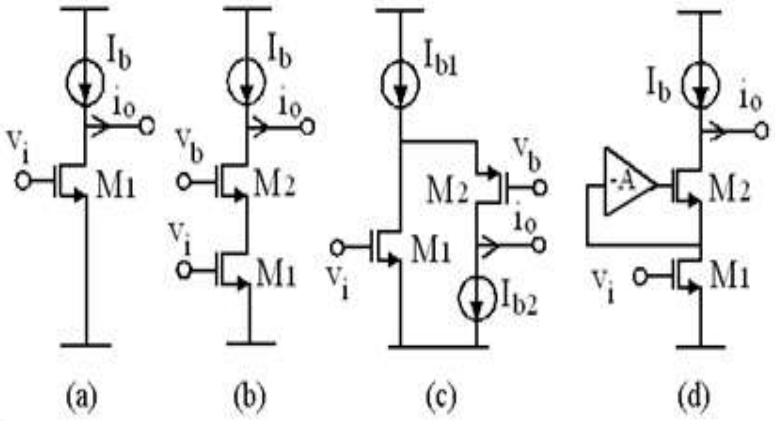

Figure 3.3 Single-input/output OTAs (a) a common source transconductor, (b) a cascode transconductor, (c) a folded-cascode transconductor and (d) a regulated-cascode transconductor [9, 23].

Figure 3.3(b) shows cascode configuration, in which a common gate transistor M2 is stack above common source transistor M1. This configuration provides isolation between input and output which results in high linearity and high output resistance. This topology is suitable for high gain and large bandwidth but on the expense of low output voltage swing. Due to its reduced output voltage swing, it limits further reduction in supply voltage.

Folded cascode topology is shown in Figure 3.3(c), which is quite similar to cascode configuration where a NMOS transistor is replaced by a PMOS transistor. This topology provides the same isolation, but with a better output voltage swing.

Figure 3.3(d) shows regulated-cascode transconductor. It is an enhanced cascode transconductor. The gate voltage of common gate transistor is connected with a negative feedback from drain of transistor M1 instead of dc voltage in simple cascode structures. Due to negative feedback the linearity and output impedance of the circuit is improved by a factor (1+A) as compared to cascode configuration where A is the gain of feedback amplifier.

3.2 OTA terminology:

There are many parameters to determine the qualities of the OTAs are:

- **Transconductance:** Transconductance is the ratio of output current to the voltage difference across the positive and negative terminals. Effective transconductance of OTA is found by the derivative of output current with respect to differential input voltage when no differential input voltage applied.

- **Open loop voltage gain:** This is the ratio of the output voltage of amplifier to the differential input voltage applied to it with no external feedback.

- **Common Mode Rejection Ratio:** Common-mode rejection ratio is the ability of an OTA to cancel out the effect of any signals that are common to both inputs, and amplify all the signals that are differential between them. CMRR is the ratio of the magnitude of the differential gain to the magnitude of the common-mode gain. In Ideal case, differential gain should be infinite and common-mode gain should be zero. So, ideally CMRR should be infinite.

- **Gain-Bandwidth product:** Gain bandwidth product is the product of the amplifier's open-loop voltage gain and frequency of its first dominant pole. Ideally Gain bandwidth product should be infinite.

- **Slew Rate:** It gives the maximum rate of change of the amplifier's transconductance current when the input signals are large and there is no feedback around the device.

- **Settling Time:** Settling time shows the time required for the output of an OTA to approach and remain within a certain tolerance of its final value. Generally the tolerance is considered to be 5% given in fraction of seconds.

- **Output voltage swing:** For a given load and operating supply voltage, output voltage swing is defined as the maximum output voltage that the OTA can deliver to the load or next stage without any clipping of output signal.

- **Total Power dissipation:** Total power dissipation is a measure of the power dissipated in the circuit in order to provide output of the circuit. It is equal to the total dc power supplied to the amplifier minus the power delivered by the amplifier to its load. Ideally no power dissipation should be there in the circuit.

- **Power Supply Rejection Ratio:** Power supply rejection ratio is a measure of an OTA's stability to prevent its output from being affected by noise or ripples at the power supply.

- **Output Impedance:** The output impedance is typically in Mega Ohms. Due to large output impedance, capacitances are generally used as load. OTA are preferable as it does not require any coupling capacitor at input and output side.

3.3 Major concerns of CMOS OTA:

Currently high frequency, high linearity, and low power dissipation are the three main concerns for the CMOS OTA with some other objectives like high CMRR and reduced settling time independent of slew rate [6, 24].

High frequency: Operational transconductance amplifiers are the best replacement of Op-Amps at high frequency applications. OTAs can operate up-to several MHz or even in GHz. To minimize the parasitic capacitance, simple configuration is preferred which is single transistor common source transconductor [7]. Transistor with multiple stages adds parasitic capacitances and hence cannot be preferred for high-frequency applications.

High linearity: The output current of OTA is linearly dependent on input voltage for low voltage input but it shows some non-linear component at output for high input voltage [25]. So, in order to reduce this effect some measures can be considered.

- Use of voltage divider before OTA will reduce input voltage but it will result in decreased transconductance.

- Source degeneration also reduces non linear terms but it also reduces transconductance.
- Triode MOSFET is used in place of degenerate resistance with some internal circuitry to increase transconductance.
- Use of partial positive feedback at load side will increase output resistance of input stage and increase linearity of the circuit [11, 26].

Low power: Power performance plays an important role in portable communication industry. Both portable and non-portable devices require low-power consumption. The power consumption in CMOS OTA is determined by dc supply voltage and dc currents.

- DC power supply reduction is done with reduction in feature size. The supply voltage reduction is limited by the output voltage swing of the circuit.
- DC current is reduced by using class-AB OTA with adaptive biasing. Adaptive biasing requires very low quiescent current value in order to reduce static power consumption. On application of large input signal, dynamic current is automatically boosted to a quite high value above quiescent current [27-30].

3.4 Gain boosting techniques

In order to design high performance analog circuits it is necessary to increase the gain of the amplifiers. A high open loop gain is also required to suppress non-linearity of an amplifier. Gain of the circuit is increased by increasing the effective transconductance of the proposed circuit.

- One way to increase transconductance is to cascode the circuit. But cascoding the circuit will leads to the decrease in output voltage swing which is undesired for a low-voltage and low-power circuits.
- The gain enhancement can be done by multistage design with long channels based at low current levels. But multistage will reduce the frequency of operation.
- Another technique to increase transconductance is by increasing B (output transistors aspect ratio) but it will increase static power dissipation of the circuit.

- The technique of partial positive feedback which increases the output impedance of the OTA input stage is an efficient way to increase gain of the amplifier [11, 14].

3.5 Bandwidth enhancement techniques

Bandwidth enhancement is required for analog signal processing applications.

- Folded cascode method can be used to enhance bandwidth of the circuit but it requires an additional drain-to-source saturation voltage for common gate transistor. So, this method is not suitable for a low -voltage circuits.
- Current mirrors can be used for bandwidth enhancement. Frequency dependent current mirrors (FDCMs) are very advantageous for low-voltage wideband amplifiers than folded cascode configuration. Also, the FDCMs produce lower non-dominant pole and lower output impedance as compared to folded cascode configuration [13, 31].

CHAPTER-4

PROPOSED ADAPTIVE BIASED OTA WITH ENHANCED DC GAIN

This chapter proposes adaptive biased OTA with enhanced dc gain. The chapter is organised as follows: In Section 4.1, the operation of the proposed adaptive biased OTA is described. Mismatched analysis of adaptive biased OTA is presented in Section 4.2. Section 4.3 presents the proposed adaptive biased OTA with enhanced dc gain. The subthreshold analysis of the circuit is addressed in Section 4.4.

4.1 Proposed adaptive biased OTA

Figure 4.1 shows proposed adaptive biased OTA. Transistors M1- M4, M11-M14 are used to form first stage of OTA and transistors M4-M6, M3-M6, M7-M8 form current mirrors. Transistors M11-M12 provides stand-by biasing current. OTA without adaptive biasing will give lower dc gain depending upon biasing current flowing in biasing resistor (R_{I_B}). In order to obtain large gain and slew rate without any increase in power dissipation, adaptive biasing technique is used [12]. Transistors ML0-ML7 and MT0-MT7 are use to form adaptive biasing current subtractor circuits. The positive feedback loops formed by transistors M1, M4, MT0-MT7 and transistors M2, M3, ML0-ML7 increases the tail current of the proposed circuit and improves its driving capability. Even, when a small differential input is applied, a large and finite amount of currents are feedback to the circuit. The amount of the feedback currents depends upon the value of A (amplifying factor of transistor ML5/MT5).

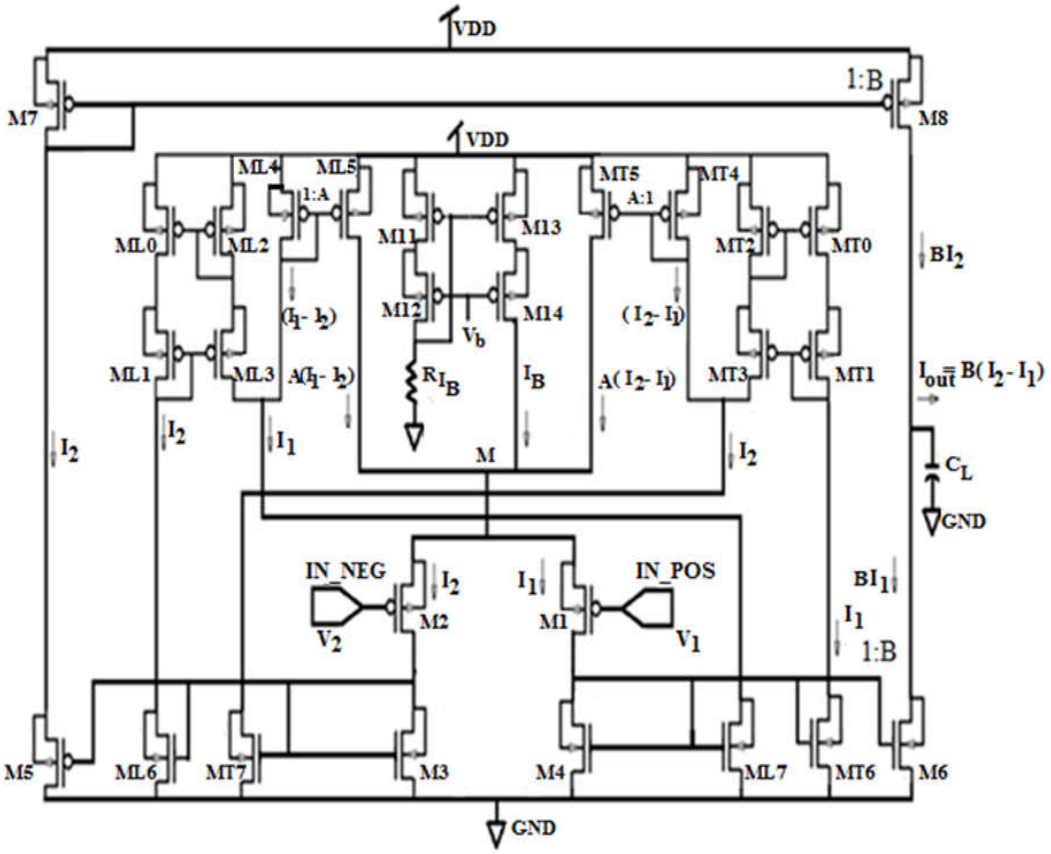

Figure 4.1 Proposed adaptive biased OTA

When positive differential voltage (V_{id}) is applied i.e. $V_{id}>0$, the current source formed by transistors MT0-MT5 realize current A(I2-I1) through the positive feedback loop M2, M3, ML0-ML7. The tail current of the circuit increases, whereas the current source formed by transistors MT0-MT5 does not produce any current.

Similarly, when $V_{id}<0$, the current source formed by transistors MT0-MT5 realizes current A(I1-I2) through the positive feedback loop M1, M4, MT0-MT5. The tail current of the circuit increases, whereas the current source ML0-ML5 does not produce any current. Hence, the current produced by current sources is always being offset by either transistors MT0-MT5 or transistors ML0-ML5 which decrease mismatched effect. The adaptive biasing technique increases gain, slew rate and CMRR of the circuit without any considerable increase in power dissipation of the circuit.

B is the amplifying factor of output transistors M8 and M6. Current I_1 is flowing in transistor M1 and current I_2 is flowing in transistor M2.

Since, transistors M3-M5, M7-M8 form current mirrors, therefore the current flowing through transistor M8 is BI_2.

Similarly, transistors M4-M6 form current mirror, the current of transistor M6 is BI_1.

Applying KCL at output node, the output current (I_{OUT}) of adaptive biased OTA is given by

$$I_{OUT} = B(I_2 - I_1) \tag{4.1}$$

where B is the amplifying factor of output transistors M6 and M8 and is given by

$$B = \frac{(\frac{W}{L})_{M8}}{(\frac{W}{L})_{M7}} = \frac{(\frac{W}{L})_{M6}}{(\frac{W}{L})_{M5}}$$

4.1.1 Proposed adaptive biasing circuit

The current subtractor shown in Figure 4.2 is used as an adaptive biasing circuit in the proposed adaptive biased OTA. The current subtractor circuit [5, 32-34] is developed by using modified Wilson current mirror [5]. Transistors ML0-ML3 form modified Wilson current mirror and transistors ML4-ML5 form simple current mirror to amplify output current (I1-I2) by an amplifying factor A.

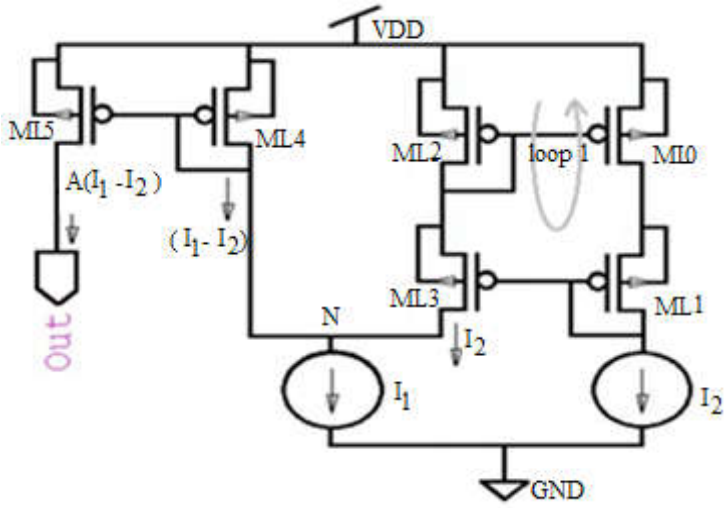

Figure 4.2 Proposed current subtractor circuit

Aspect ratio (W/L) of transistor ML5 is A times that of transistor ML4. All the transistors are in saturation region. The transistors ML4 and ML5 are perfectly matched (i.e. $V_{TPML4}= V_{TPML5}$ and $K_{PML4}= K_{PML5}$). The final output current obtained will be (I1-I2). To neglect body bias effect body of all the transistors are shorted with source of the transistors. Current I_2 is transferring from input transistor ML1 to transistor ML3.

Applying KCL at node N, the current flowing in transistor ML4 is given as

$$I_{ML4}= I_1- I_2 \tag{4.2}$$

Transistors ML4 and ML5 form a current mirror with amplifying factor A. So, the output current is given as

$$I_{out} = A (I_1- I_2) \tag{4.3}$$

In Modified Wilson Current Mirror, due to Negative feedback through transistor ML2, drain current flowing in transistor ML3 is stabilised. If output voltage and output current of Wilson current mirror are Vw and Iw respectively then if Vw increases, then Iw also increase and hence the current flowing through transistor ML0 is increased. But, a constant current I_2 is flowing through transistor ML0 therefore, the drain-to-source voltage (V_{DS0}) will drop to maintain a constant value of the current. Since, transistor ML1 is diode connected, the voltage at gate terminal of transistor ML3 reduces to maintain constant current I2 through transistor ML1, so unwanted increment in current of transistor ML3 will drop down and the current of transistor ML3 becomes stable.

4.1.2 Small signal analysis

The small signal model of current subtractor is shown in Figure 4.3. V_W and I_W are the output voltage and output current of modified Wilson current mirror respectively and V_X and I_X are the output voltage and output current of current subtractor respectively. D_i, S_i and G_i represents for drain, source and gate terminal of PMOS transistor respectively for i= 0,1,2,3,4,5.

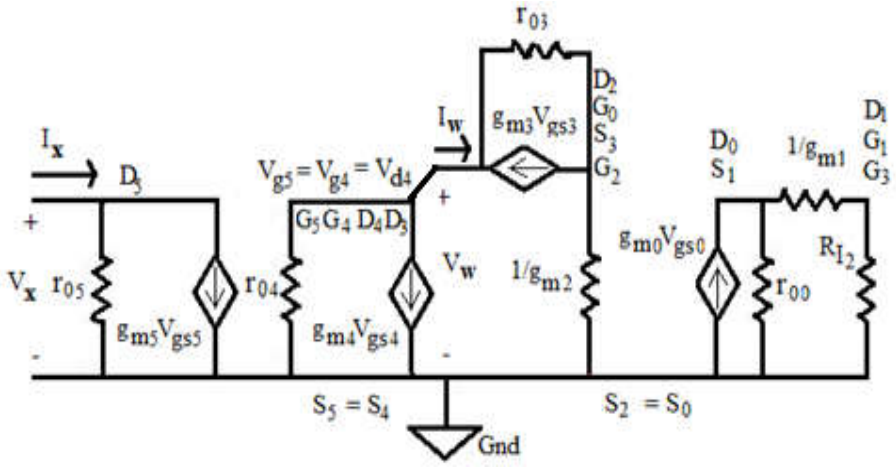

Figure 4.3 Small signal model of adaptive bias circuit

By applying KVL in loop D_3-S_3-S_2, the output voltage (V_W) is given as

$$V_W = (I_W + g_{m3}v_{gs3}) r_{03} + I_W / g_{m2} \quad (4.4)$$

where, r_{03} is drain-to-source channel resistance of transistor ML3, g_{m3} is the transconductance of transistor ML3, g_{m2} is the transconductance of transistor ML2 and $g_{m3}V_{gs3}$ is the voltage dependent current source with current flowing from source to drain of transistor ML3.

The gate voltage (V_{g3}) of transistor ML3 is given as

$$V_{g3} = V_{s1} R_{I2} / (R_{I2} + 1/ g_{m1}) \quad (4.5)$$

where V_{s1} is the source voltage of transistor ML1.
The source voltage of transistor ML1 is written as

$$V_{s1} = g_{m0}V_{gs0} r_{00} \quad (4.6)$$

where r_{00} is drain-to-source channel resistance of transistor ML0 and $g_{m0}V_{gs0}$ is the voltage dependent current source with current flowing from source to drain of transistor ML0.

Substituting the value of V_{s1} in (4.6), the gate voltage (V_{g3}) is modified as

$$V_{g3} = g_{m0}\, r_{0T}\, V_{g0}\, R_{I2} / (R_{I2} + 1/g_{m1}) \quad (4.7)$$

where V_{g0} is gate voltage of transistor ML0 and $r_{0T} = r_{00} // (R_{I2} + 1/ g_{m1})$

Substituting the value of V_{g3} from (4.7) in (4.4), the output voltage (V_W) is obtained as

$$V_W = (I_W + g_{m3}\, g_{m0}\, r_{0T}\, V_{g0}\, R_{I2} / (R_{I2} + 1/g_{m1}))\, r_{03} + I_W / g_{m2} \quad (4.8)$$

The output resistance of modified Wilson current mirror (R_{outW}) is obtained as

$$R_{outW} = V_W/I_W \approx (g_{m3}/g_{m2}) g_{m0}\, r_{0T}\, R_{I2} / (R_{I2} + 1/g_{m1}) \quad (4.9)$$

If $g_{m0} = g_{m1} = g_{m2} = g_{m3} = g_m$ and $R_{I2} > 1/g_{m1}$

Then, (4.9) is modified as

$$R_{outW} \approx g_m\, r_0^2 \quad (4.10)$$

From (4.10), it is observed that the output impedance of modified Wilson current mirror is increased by $g_m r_0$ than the output impedance of simple current mirror.
The output voltage (V_X) of current subtractor from Figure 4.3 is given as

$$V_X = r_{05}\, g_{m5}\, V_{g5} \quad (4.11)$$

where V_{g5} is the gate voltage, r_{05} is drain-to-source resistance and g_{m5} is transconductance of transistor ML5 .

The gate voltage (V_{g5}) of transistor ML5 is given as

$$V_{g5} = (R_{outW} // r_{04}).\, I_X \quad (4.12)$$

Substituting the value of V_{g5} in (4.8), the output voltage (V_X) is given as

$$V_X = r_{05} g_{m5} (R_{outW} // r_{04}) I_X \quad (4.13)$$

Hence, the output resistance of current subtractor (R_{OUT}) is obtained as

$$R_{OUT} = V_X / I_X = r_{05} g_{m5} (R_{outW} // r_{04}) \approx g_m r_0^2 \quad (4.14)$$

From (4.14), it is observed that the output resistance of proposed current subtractor is high as compared to conventional current subtractor. Due to increased output resistance, for the constant currents flowing in input transistors, output current observed is constant.

4.1.3 Subthreshold analysis of proposed adaptive biased OTA

Primary emphasis for amplifying circuits is for micro-power operations, the circuits have been examined in details in subthreshold region [11]. When the applied voltages at gate of transistors M1 and M2 are less than threshold voltages, the transistors are operated in the sub threshold region.

The current flowing in transistor M1 in subthreshold region is given as

$$I_1 = \mu_p Cox (n-1) V_T^2 e^{V_{TP1}/\eta V_T} (W/L)_1 e^{V_{GS1}/\eta V_T} \quad (4.15)$$

where η is the process parameter whose value lies between $1<\eta<2$, μ_p is charge carrier effective mobility, C_{OX} is gate oxide capacitance per unit area, V_T is the thermal voltage, V_{TP1} is threshold voltage, V_{GS1} is the gate-to-source voltage and $(W/L)_1$ is the aspect ratio of transistor M1.

Equation (4.15) can be written as

$$I_1 = I_{SD01} (W/L) e^{V_{GS1}/\eta V_T} \quad (4.16)$$

where, $I_{SD01} = \mu_p Cox (n-1) V_T^2 e^{VTP1/\eta V_T}$

Similarly, the source-to-drain current of transistor M2 is given as

$$I_2 = \mu_p Cox (n-1) V_T^2 e^{V_{TP2}/\eta V_T} (W/L)_2 e^{V_{GS2}/\eta V_T} \quad (4.17)$$

where η is the process parameter whose value lies between $1<\eta<2$, μ_p is charge carrier effective mobility, C_{OX} is gate oxide capacitance per unit area, V_T is the thermal voltage, V_{TP2} is threshold voltage, V_{GS2} is the gate-to- source voltage and $(W/L)_2$ is the aspect ratio of transistor M2.

Equation (4.17) can be written as

$$I_2 = I_{SD02} (W/L)_2 e^{V_{GS2}/\eta V_T} \quad (4.18)$$

where, $I_{SD02} = \mu_p Cox (n-1) V_T^2 e^{VTP2/\eta V_T}$

The transistors M1 and M2 are perfectly matched (i.e. $K_{TP1} = K_{TP2}$ and $V_{TP1} = V_{TP2}$) and aspect ratios are equal.

So, $$I_{SD01} = I_{SD02} = I_{SD0} \quad (4.19)$$

Using (4.16), (4.18) and (4.19), the current ratio is obtained as

$$I_2/I_1 = e^{(V_2 - V_1)/\eta V_T} \quad (4.20)$$

where V_2 and V_1 are gate voltages of transistors M2 and M1 respectively.

The total current (I_B) flowing in the circuit (without adaptive biasing) by applying KCL at node M is obtained as

$$I_B = I_1 + I_2 \tag{4.21}$$

whereas, The total current (I_B) flowing in the circuit (using adaptive biasing) by applying KCL at node M is obtained as

$$I_B = I_1 (1- A) + I_2(1 + A) \tag{4.22}$$

The differential input voltage (V_{id}) is defined as

$$V_{id} = V_1 - V_2 \tag{4.23}$$

From (4.23), the gate voltage of transistor M1 is obtained as

$$V_1 = V_2 + V_{id} \tag{4.24}$$

Using (4.16), (4.18) and (4.24), the current flowing through transistor M1 is given by

$$I_1 = I_2 . e^{(V_{id})/\eta V_T} \tag{4.25}$$

Substituting the value of I_1 from (4.25) in (4.22), the total current (I_B) is modified as

$$I_B = I_2 . e^{(V_{id})/\eta V_T} (1- A) + I_2(1 + A) \tag{4.26}$$

From (4.26) the current flowing in transistor M2 is obtained as

$$I_2 = \frac{I_B}{\{ (1 + A) + e^{(V_{id})/\eta V_T} (1- A) \}} \tag{4.27}$$

Using (4.25) and (4.27), the current (I_1) is given as

$$I_1 = I_2 . e^{(V_{id})/\eta V_T} = \frac{I_B (e^{(V_{id})/\eta V_T})}{\{ (1 + A) + e^{(V_{id})/\eta V_T} (1- A) \}} \tag{4.28}$$

Substituting (4.27), (4.28) and (4.1), output current is modified as

$$I_{out} = B.\ \frac{I_B\,(e^{(V_{id})/\eta V_T} - 1)}{\{(1+A) + e^{(V_{id})/\eta V_T}(1-A)\}} \tag{4.29}$$

From (4.29), it can be seen that a small change in the input voltage gives a large change in the output current.

4.2 Mismatch analysis of proposed adaptive biased OTA

The current provided by adaptive biasing circuits is equal to A|ΔI|, where |ΔI| is the absolute value of the differential output current.

Suppose that all possible mismatches in currents are taken into account in the current source and the matching factor is defined as

$$m=1\ \ \alpha_{mismatch} \tag{4.30}$$

where, m is the matching factor and $\alpha_{mismatch}$ is the mismatched factor.

In Figure 4.1, the output current (I_{out}) is given as

$$I_{out} = B.\ (I_1 \quad mI_2) \tag{4.31}$$

Substituting (4.27), (4.28) in (4.31), the output current is obtained as

$$I_{out} = B.\ \frac{I_B\,(e^{(V_{id})/\eta V_T} - m)}{\{(1+m\,A) + e^{(V_{id})/\eta V_T}(1-A)\}} \tag{4.32}$$

The minimum voltage (V_{min}) required for the OTA to operate in adaptive biasing mode is given as the voltage at which output current becomes zero.

By substituting I_{out} equals to zero, the V_{min} is obtained as

$$V_{min} = \eta V_T \ln(m) \tag{4.33}$$

The escape voltage (V_{escape}) highlights the conditions when the OTA does not slew and the output current tends to infinity.

By substituting I_{out} equals to infinity, the V_{escape} is obtained as

$$V_{escape} = \eta V_T \ln\frac{Am+1}{A-1} = \eta V_T \ln\left(\frac{Am+1}{A-1} \quad \frac{A\alpha mismatch}{A-1}\right) \tag{4.34}$$

Using (4.33) and (4.34), it is observed that when A>> 1, the minimum voltage and escape voltage are reduces to zero indicates that the OTA does not slew except in the case when Vid=0. Therefore, the mismatched effect of the proposed OTA has been reduced by using adaptive biasing technique.

4.3 Proposed adaptive biased OTA with enhanced dc gain

Proposed adaptive biased OTA with enhanced dc gain is shown in Figure 4.4.

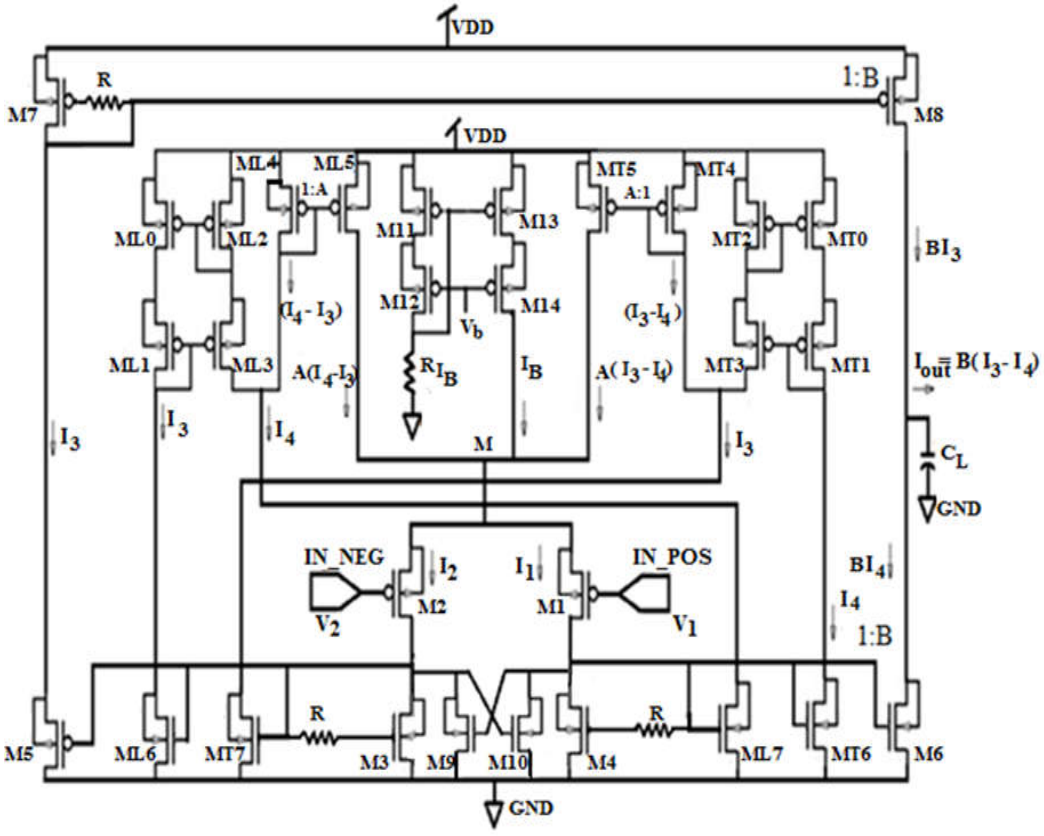

Figure 4.4 Proposed adaptive biased OTA with enhanced dc gain

The gain and linearity of proposed adaptive biased OTA is still low. To further enhance the gain of the circuit, partial positive feedback gain enhancement technique is used at load side [11]. Also, frequency dependent current mirrors [13, 31] are employed to enhance the bandwidth of the proposed OTA circuit. The resistor R is used to connect the drain and gate of diode connected transistors M3, M4 and M7. These resistors are eventually delays the response, but also introduce zero to the circuit which cancels the delay.

The output of the proposed OTA is given as

$$I_{out} = B\,(I_3 - I_4) \tag{4.35}$$

4.3.1 Partial positive feedback gain boosting technique

Partial positive feedback circuit to enhance the gain of the proposed OTA is shown in Figure 4.5 [11]. Transistors M1 and M2 are input transistors, M3 and M4 are active load transistors and M9 and M10 are partial positive feedback transistors.

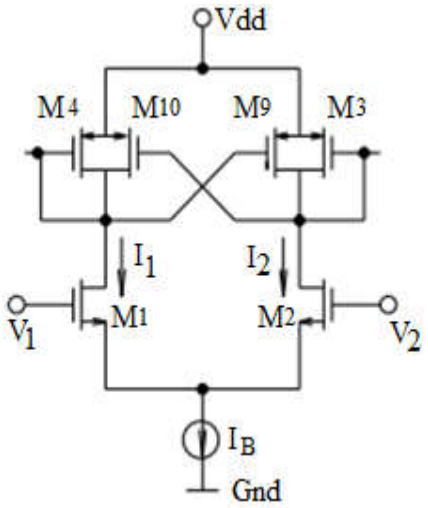

Figure 4.5 Partial positive feedback gain enhancement circuit [11].

The current I_1 and current I_2 are flowing in transistors M1 and M2 respectively. A positive loop is formed between transistors M1-M4-M10 and transistors M2-M3-M9.

Without using gain enhancement technique, the output current of OTA (Figure 4.1) is given by

$$I_{out} = B.(I_2 - I_1) = B. (I_2 + I_1) \frac{(\frac{I_2}{I_1} - 1)}{(\frac{I_2}{I_1} + 1)} \quad (4.36)$$

Substituting (4.20), (4.21) in (4.36), the output current is obtained as

$$I_{out} = B. I_{B.} \tanh (\frac{(V_2 - V_1)}{2\eta V_T}) \quad (4.37)$$

where η is the process parameter whose value lies between $1<\eta<2$, V_T is thermal voltage and V_2 and V_1 are the gate voltages of transistors M2 and M1 respectively.

By applying KCL at drain of transistor M2 in Figure 4.4, the current (I_3) in transistor M3 is given by

$$I_3 = I_2 - I_9 \quad (4.38)$$

where I_2 is the current flowing through transistor M2 and I_9 is the current flowing in transistor M9.

Similarly, by applying KCL at drain of transistor M1, the current (I_4) in transistor M1 is given as

$$I_4 = I_1 - I_{10} \quad (4.39)$$

where I_1 is the current flowing through transistor M1 and I_{10} is the current flowing in transistor M10.

The output current (I_{out}) of proposed adaptive biased OTA with gain enhancement is given as

$$I_{out} = B (I_3 - I_4) \quad (4.40)$$

Substituting the value of currents I_3 and I_4 in (4.40), the output current is obtained as

$$I_{out} = B((I_2 - I_9) - (I_1 - I_{10})) = B.((I_2 - I_1) - (I_9 - I_{10})) \quad (4.41)$$

The differential current (I_9 - I_{10}) in terms of drain voltages of transistor M2 and M1 is given as

$$I_9 - I_{10} = - g_{m9} (V_{d2} - V_{d1}) \quad (4.42)$$

where g_{m9} is the transconductance of transistor M9, V_{d2} and V_{d1} are the drain voltages of transistors M2 and M1 respectively.

Similarly, the differential current ($I_3 - I_4$) in terms of drain voltages of transistor M2 and M1 is given by

$$(I_3 - I_4) = g_{m3.}(V_{d2} - V_{d1}) = \frac{Iout}{B} \quad (4.43)$$

Substituting (4.41), (4.42) in (4.43), the output current is modified as

$$I_{out} = B \frac{1}{1-\frac{gm9}{gm3}} (I_2 - I_1) \quad (4.44)$$

Substituting (4.37) in (4.44), the output current (I_{out}) of OTA with gain enhancement is given by

$$I_{out} = B. I_B \frac{1}{1-\alpha} \tanh (\frac{(V_2-V_1)}{2\eta V_T}) \quad (4.45)$$

where $\alpha = \frac{gm9}{gm3}$, g_{m3} and g_{m9} are the transconductances of transistors M3 and M9 respectively, η is the process parameter whose value lies between 1<η<2 and V_T is the thermal voltage.

From (4.45) it is seen that the output current of the proposed OTA is increased due to gain enhancement technique.

4.3.2 Small signal analysis

The small signal model of proposed adaptive biased OTA with enhanced dc gain is shown in Figure 4.6. V_{in}^{+} is the potential applied at the non-inverting terminal and V_{in}^{-} is the potential with 180° phase difference as compared to voltage applied at non-

inverting terminal and V_O is the output voltage. Due to virtual ground at source of input transistors M1 and M2, adaptive biasing circuit transistors and biasing current source transistors (M11-M14) do not play much role in small signal model. So, these transistors are neglected.

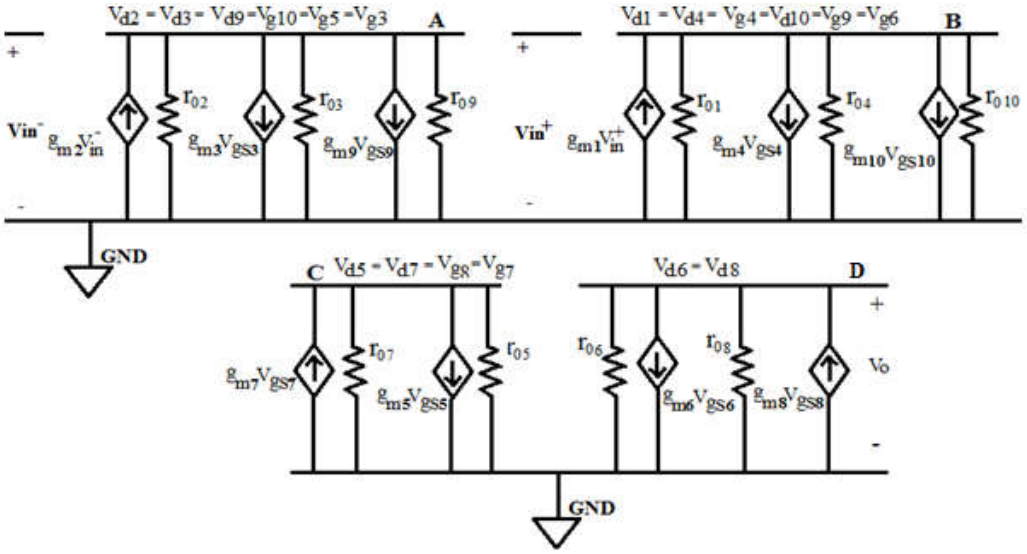

Figure 4.6 Small signal model of proposed adaptive biased OTA with enhanced dc gain

By applying KVL at node D, the output voltage (V_O) is given as

$$V_O = (g_{m8}V_{g8} - g_{m6}V_{g6}) (r_{06} // r_{08}) \quad (4.46)$$

where V_{g8} and V_{g6} are the gate voltages of transistors M8 and M6 respectively, g_{m8} and g_{m6} are the transconductances of transistors M8 and M6 respectively and r_{08} and r_{06} are the drain-to-source resistances of transistors M8 and M6 respectively.

By applying KVL at node C, the gate voltage (V_{g8}) of transistor M8 is given by

$$V_{g8} = \frac{(r_{07} // r_{05})}{(1 - g_{m7}(r_{07} // r_{05}))} (-g_{m5}V_{g5}) \quad (4.47)$$

where V_{g5} is the gate voltage of transistor M5, g_{m5} and g_{m7} are the transconductances of transistors M5 and M7 respectively and r_{05} and r_{07} are the drain-to-source resistances of transistors M5 and M7 respectively.

By applying KVL at node A, gate voltage (V_{g5}) is given by

$$V_{g5}= (r_{03}//r_{02}//r_{09}//\frac{1}{g_{m3}}) (g_{m2}V_{in}^{-} - g_{m9}V_{g9}) \quad (4.48)$$

where, g_{m2}, g_{m3} and g_{m9} are the transconductances of transistors M2, M3 and M9 respective, V_{in}^{-} and $V_{g9}$are the gate voltages of transistors M2 and M9 respectively and r_{03}, r_{09} and $r_{02}$are the drain-to-source resistances of transistors M3, M9 and M2 respectively.

The gate voltage (V_{g5}) of transistor M5 can be written as

$$V_{g5}= R_1 (g_{m2}V_{in}^{-} - g_{m9}V_{g9}) \quad (4.49)$$

where $R_1= (r_{03}//r_{02}//r_{09}//\frac{1}{g_{m3}})$

By applying KVL at node B, the gate voltage (V_{g9}) of transistor M9 is defined as

$$V_{g9}= (r_{04}//r_{01}//r_{010}//\frac{1}{g_{m4}}) (g_{m1}V_{in}^{+} - g_{m10}V_{g10}) \quad (4.50)$$

where g_{m1}, g_{m4} and g_{m10} are the transconductances of transistors M1, M4 and M10 respectively, V_{in}^{+} and V_{g10} are the gate voltages of transistors M1 and M10 respectively and r_{01}, r_{04} and r_{010} are the drain-to-source resistances of transistors M1, M4 and M10 respectively.

The gate voltage (V_{g9}) can be written as

$$V_{g9} = R_2 (g_{m1}V_{in}^{+} - g_{m10}V_{g10}) \quad (4.51)$$

where $R_2 = (r_{04}//r_{01}//r_{010}//\frac{1}{g_{m4}})$

Putting the value V_{g9} in (4.49), the gate voltage (V_{g5}) is modified as

$$V_{g5} = \frac{1}{(1+R_2R_1g_{m9}g_{m10})} (R_1g_{m2}V_{in}^{-} - R_2 R_1g_{m9}g_{m1}V_{in}^{+}) \quad (4.52)$$

The voltages applied at both the terminals of OTA in terms of differential voltage (V_{id}) are given as

$$V_{in}^{+} = \frac{V_{id}}{2} \text{ and } V_{in}^{-} = - \frac{V_{id}}{2} \quad (4.53)$$

Substituting the values of V_{in}^{+} and V_{in}^{-} in (4.52), the gate voltage (V_{g5}) is modified as

$$V_{g5} = - \frac{V_{id}}{2} \frac{(R_1g_{m2}+ R_2 R_1g_{m9}g_{m1})}{(1+R_2R_1g_{m9}g_{m10})} \quad (4.54)$$

Now, putting the value of V_{g5} in (4.47), the gate voltage (V_{g8}) is given as

$$V_{g8}= - \frac{(r_{07}// r_{05})g_{m5}}{(1-g_{m7}(r_{07}// r_{05}))} \frac{(R_1g_{m2}+ R_2 R_1g_{m9}g_{m1})}{(1+R_2R_1g_{m9}g_{m10})} \frac{V_{id}}{2} \quad (4.55)$$

Substituting the value of V_{g5} from (4.54) in (4.49), the gate voltage (V_{g6}) of transistor M6 is given as

$$V_{g6} = \frac{V_{id}}{2} (\frac{g_{m9}(R_1g_{m2}+ R_2 R_1g_{m9}g_{m1})- g_{m2}(1+R_2R_1g_{m9}g_{m10})}{g_{m9}(1+R_2R_1g_{m9}g_{m10})}) \quad (4.56)$$

Substituting the values V_{g8} and V_{g6} in (4.46), the differential gain of proposed circuit is given by

$$A_d = \frac{V_O}{V_{id}} = \frac{-(r_{06}// r_{08})}{2(1+R_2R_1g_{m9}g_{m10})} * [\{ \frac{(r_{07}// r_{05})g_{m5}g_{m8}R_1(g_{m2} + R_2 g_{m9}g_{m1})}{(1-g_{m7}(r_{07}// r_{05}))} \} + \{ \frac{g_{m9}g_{m6}(R_1g_{m2}+ R_2 R_1g_{m9}g_{m1})- g_{m6}g_{m2}(1+R_2R_1g_{m9}g_{m10})}{g_{m9}} \}] \quad (4.57)$$

Equation (4.57) shows that the gain of the proposed circuit is quite high.

4.4 Analysis of proposed adaptive biased OTA with enhanced dc gain in subthreshold region

When the applied voltages at gate of transistors M1 and M2 are less than threshold voltages, the transistors are operated in the subthreshold region.

Substituting (4.27), (4.28) in (4.44), the output current of proposed circuit is given as

$$I_{out} = \frac{BI_B}{1-\alpha} \frac{(e^{(V_{id})/\eta V_T} - 1)}{\{(1+A) + e^{(V_{id})/\eta V_T}(1-A)\}} \quad (4.58)$$

where $\alpha = \frac{gm9}{gm3} = \frac{(\frac{W}{L})_{M9}}{(\frac{W}{L})_{M3}}$

From equation (4.58) it is evident that the output current of the circuit (shown in Figure 4.4) is increased by a factor $\frac{1}{1-\alpha}$ than proposed adaptive biased OTA (shown in Figure 4.1) without gain enhancement.

In (4.58), if α =1 then denominator of output current becomes zero and the circuit will become unstable. To maintain stability of the circuit, α should not be equal to 1.

For α varying from 0 to1, as α increases, the output current increases but this will reduce phase margin of the circuit. Aspect ratio of transistor M9/M10 should be less than the aspect ratio of transistor M3/M4 to increase output current. Hence, the appropriate value of α should be chosen. For the proposed OTA, the value of α is chosen as 94% for the maximum efficiency while maintaining stability.

CHAPTER-5

SIMULATION RESULTS

The simulations of proposed circuit have been performed using Cadance Virtuoso ADE in 180nm CMOS process technology. The chapter is organised as follows: Section 5.1 presents all the simulation results of current subtractor circuit and Section 5.2 addresses the simulation results of proposed adaptive biased OTA with enhanced dc gain.

5.1 Simulation results of adaptive biasing circuit (current subtractor circuit)

Figure 5.1 shows DC characteristics of current subtractor circuit based on modified Wilson current mirror. The plot is between the output current and input current I2 varying from 0nA to 600uA while current I1 is constant as 600uA.

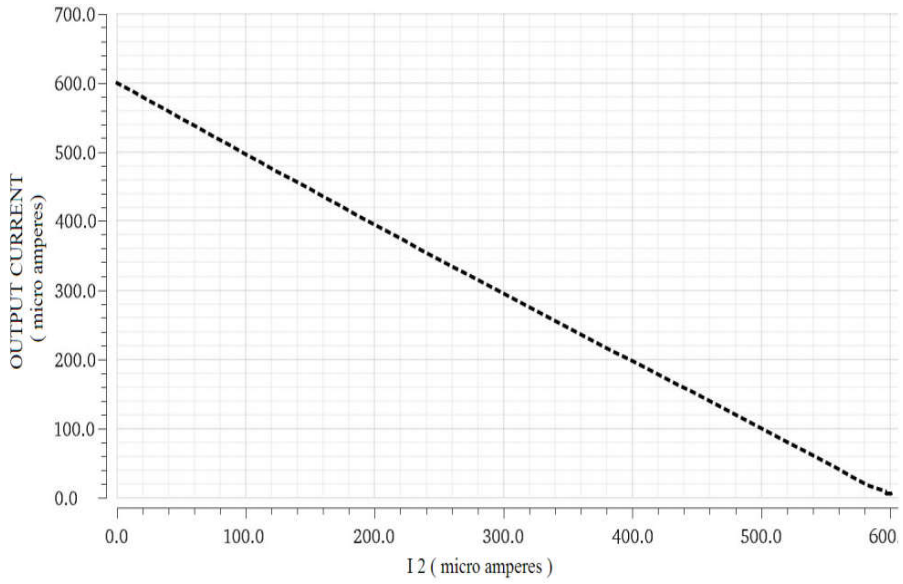

Figure 5.1 DC characteristics of current subtractor circuit

The result obtained is quite linear in the entire current range of 0nA to 600uA. Also it can be observed that the circuit works efficiently for the entire input current range.

Table 5.1 Percentage error of current subtractor circuit

Input Current I2	Input Current I1	Simulated Output I1-I2 (uA)	Calculated Output I1- I2 (uA)	Percentage Error (%)
0nA	600uA	599.99	600	0.0001
50uA	600uA	548.36	550	0.2974
100uA	600uA	496.81	500	0.6367
150uA	600uA	445.48	450	1.0040
200uA	600uA	394.58	400	1.3540
250uA	600uA	344.25	350	1.6400
300uA	600uA	294.52	300	1.8200
350uA	600uA	245.44	250	1.8200
400uA	600uA	197.08	200	1.4600
450uA	600uA	148.93	150	0.7100
500uA	600uA	099.94	100	0.0540
550uA	600uA	050.23	050	0.4740
600uA	600uA	000.00	000	0.0000

A number of observations of percentage error of the circuit is tabulated in Table 5.1. As one of the input currents is increasing from 0nA to 600uA, the output current is decreasing from 600uA to 0nA while keeping the other current fixed at 600uA. The percentage error observed is less than 1.82%.

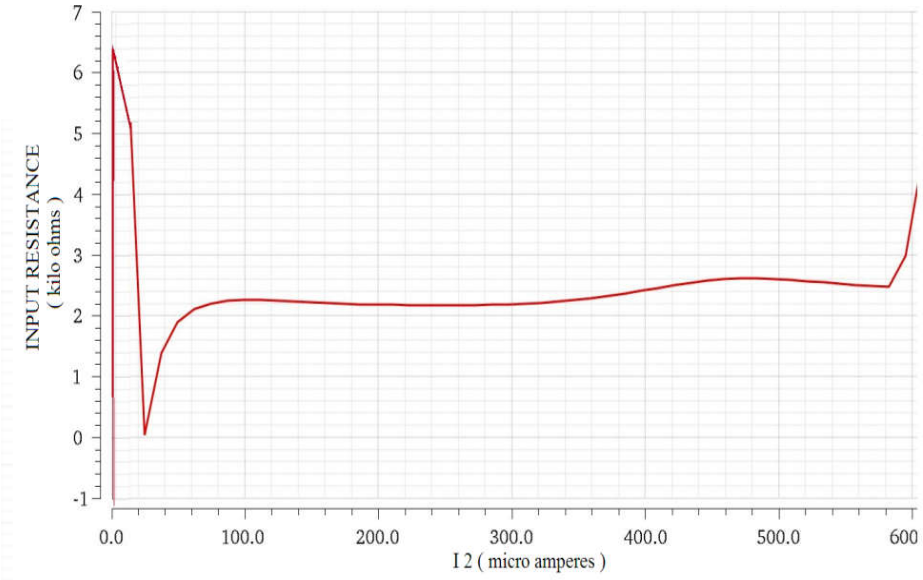

Figure 5.2 Input resistance of the current subtractor circuit

A graph of input resistance of current subtractor circuit vs. input current I2 is shown in Figure 5.2. It is observed that the input resistance is increasing when input current is increasing from 0nA to 600uA. The maximum and minimum values of input resistance are 6 KΩ and 650Ω respectively. The entire range of input resistance is low enough to sense complete input current range without any distortion.

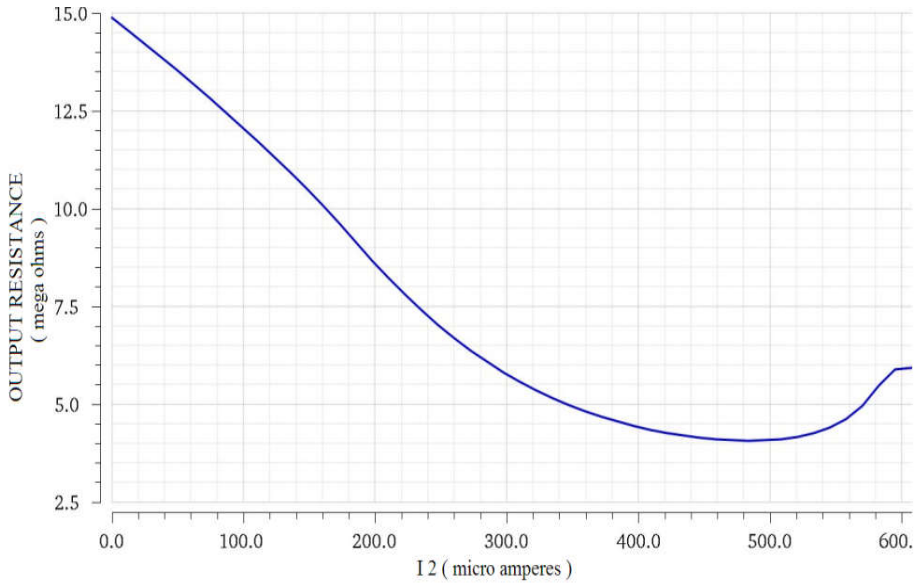

Figure 5.3 Output resistance of current subtractor circuit

Figure 5.3 shows output resistance with varying input current I2 ranging from 0nA to 600uA while current I1 is constant as 600uA. The output resistance is decreasing with the decreasing output current (I2-I1). The maximum and minimum values of output resistance are 14.87 MΩ and 5.89 MΩ respectively. The entire range of output resistance range is a sufficient enough in order to reduce loading effect at the load side.

5.2 Simulation results of adaptive biased OTA with enhanced dc gain

For the simulation of proposed OTA, load capacitance is used as 8pF with biasing current of 80uA and supply voltage of 1.8V. The circuit uses current mode adaptive biasing current subtractor circuit.

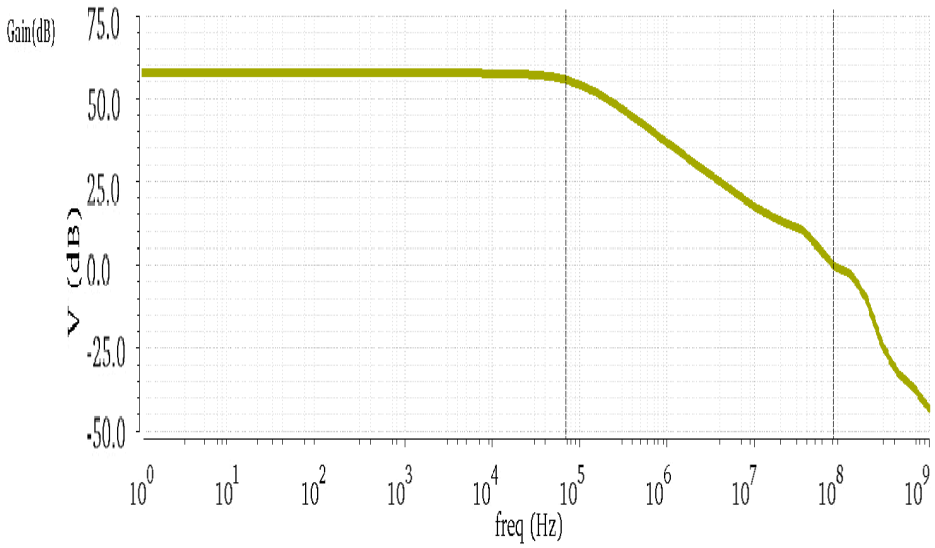

Figure 5.4 Frequency response of proposed adaptive biased OTA

Figure 5.4 shows the frequency response of proposed adaptive biased OTA (shown in Figure 4.1). The gain observed is 57.65dB and unity gain bandwidth is 81.15MHz.

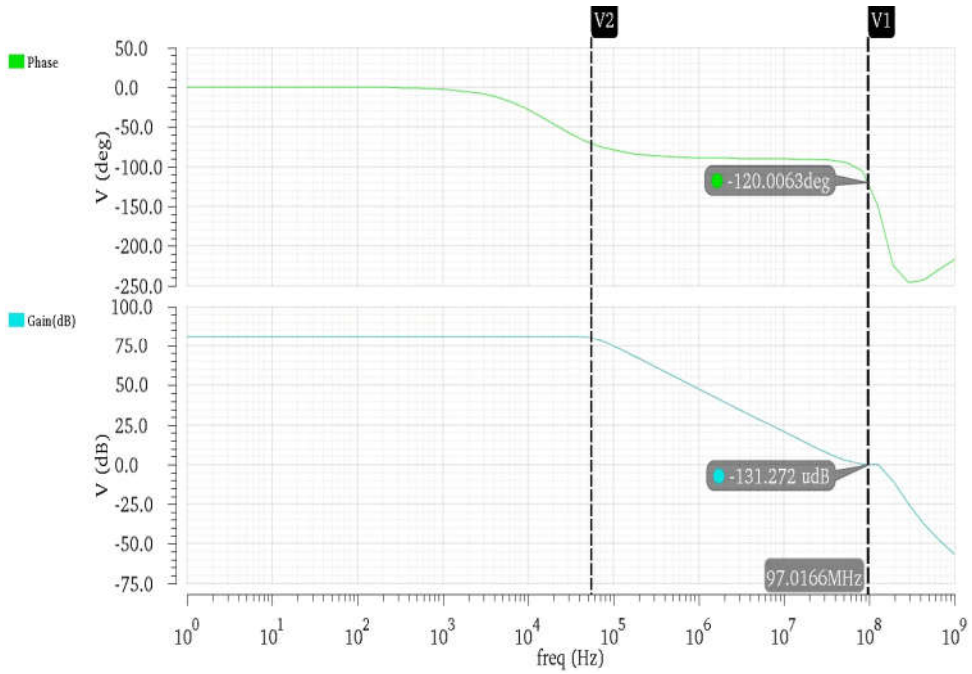

Figure 5.5 Frequency response of proposed adaptive biased OTA with enhanced dc gain

The dc gain and bandwidth have been enhanced using partial positive feedback and frequency dependent current mirrors (shown in Figure 4.3). Frequency response of the

proposed circuit is shown in Figure 5.5. It is observed that the proposed circuit dc gain and unity gain bandwidth have been increased from 57.65dB (adaptive biased OTA without dc gain enhancement) to 81.02dB (adaptive biased OTA with dc gain enhancement) and 81.15MHz(without FDCM) to 97.016MHz(with FDCM) respectively. The gain bandwidth product is 4.31MHz with phase margin of 60 degree.

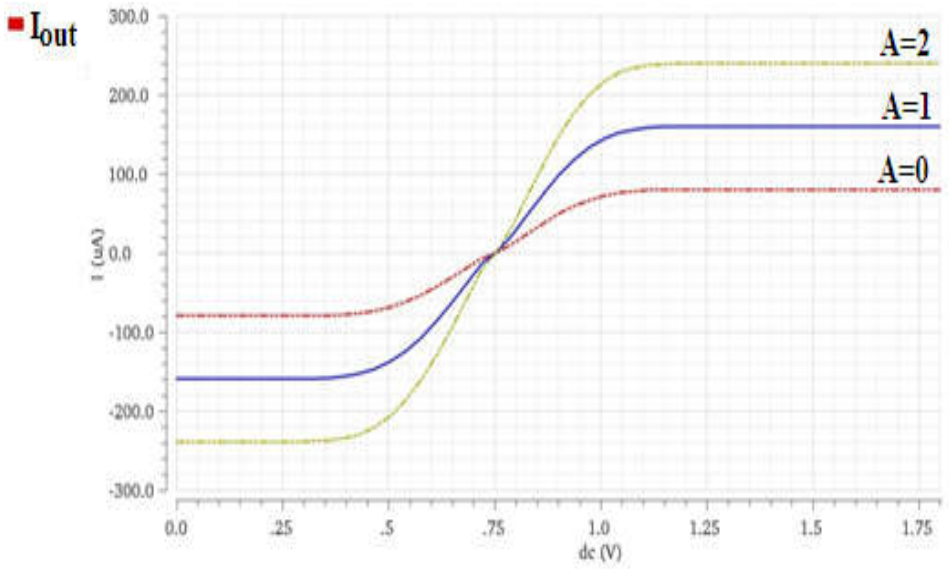

Figure 5.6 Differential output current with different adaptive bias amplifying factor (A)

Figure 5.6 shows differential output current (I2-I1) vs. input voltage at non-inverting terminal for three different values A=0,1,2. When A=0 i.e. without adaptive biasing, the output current is always less than or equal to static biasing current. When differential voltage is less than or equal to saturation voltage ($\pm V_{Dsat}$), the output current increases linearly in both directions whereas, when differential voltage is greater than saturation voltage, the output current saturates and remains constant. As A increases, output current gets amplified.

The plot between DC output voltage(V_{O1}-V_{02}) vs. differential input voltage (V_1- V_2) is drawn in figure 5.7. For the simulation, the value of V_2 is applied as 0.75V. In the plot, as the differential input voltage increases from 0 to $+V_{Dsat}$, the output voltage increases linearly and after $+V_{Dsat,}$ the output voltage approaches the maximum value

and remains constant whereas as the differential input voltage decreases from 0 to -V_{Dsat}, the output voltage decreases linearly and after -V_{Dsat}, the output voltage approaches the minimum value and remains constant.

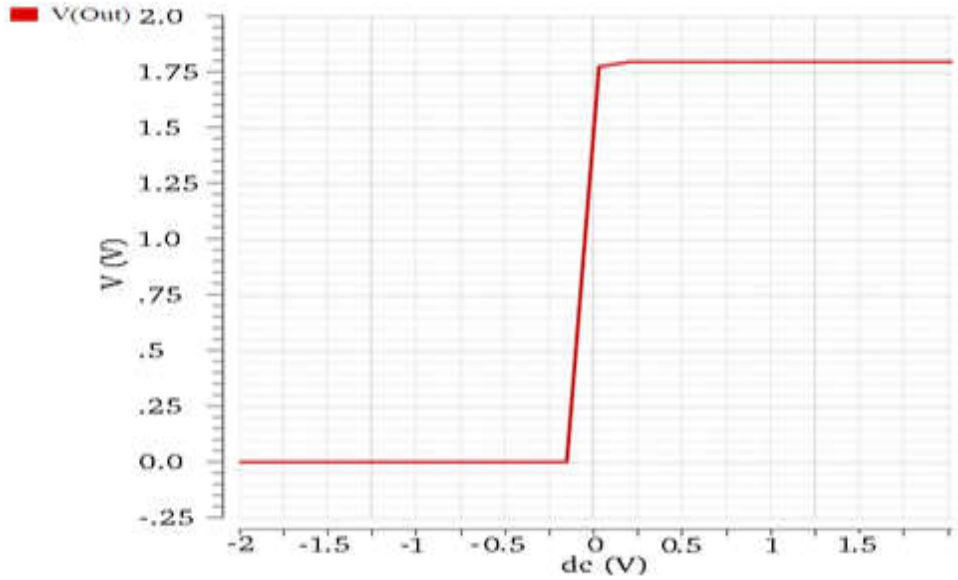

Figure 5.7 Output voltage of proposed adaptive biased OTA circuit

The output voltage is varying linearly for the differential input voltage ranging from -0.15V to +0.13V. The output voltage swing is 32uV to 1.8V.

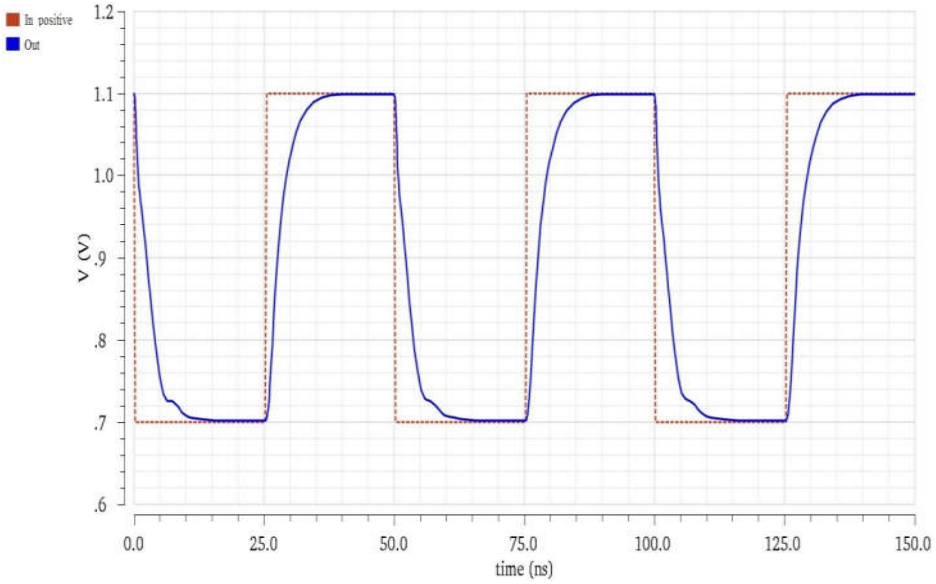

Figure 5.8 Transient analysis of proposed Adaptive biased OTA with enhanced dc gain

Figure 5.8 shows transient analysis of the proposed OTA. In the plot, dotted and dark lines are used to show input and output waveforms respectively. The positive and negative slew rates have been obtained as 40V/us and 48V/us simultaneously. The settling time of the circuit is 10.02ns.

Table5.2 Comparison between OTAs available in literature and proposed OTA

REFERENCE NO.	**[12]**	**[15]**	**[26]**	**[24]**	**[17]**	**[19]**	**[21]**	**Proposed Work**
CMOS process	0.5um	0.5um	0.35um	0.18um	0.18um	0.18um	0.5um	0.18um
Supply Voltage (V)	± 1	± 1	± 0.75	1.8	±0.9	±0.6	2	1.8
Load Capacitance	80pF	80pF	15pF	10pF	10pF	1pF	80pF	8pF
DC Gain (dB)	37.5	41	76	48.97	42	44	44.6	81.02
Phase Margin (degree)	90	71	81	78.18	90	68	85.1	60
GBW	470 KHz	2.3 MHz	3.5 MHz	57.27 KHz	3.2 MHz	590 KHz	3.59 MHz	4.617 MHz
CMRR (dB)	69	75	136	124.37	169	110	-	152.6
PSRR+/- (dB)	57 46	56 51	114 109	81.4 50.3	-	73 48	-	140 120
SR +/- (V/us)	42 80	14 28	25	4.92 5..04	-	71 72	7 6.5	40 48.75
Settling Time	100ns 33ns	-	410ns	1us 2.1us	-	160ns	100ns 130ns	10.02ns
Static Power Dissipation(uW)	140	140	84	1.96	250	0.44	137	178.8
Unity Gain Frequency	-	-	-	-	-	-	-	97.02 MHz
Input offset	-	-	69uV	-	-	-	-	31.25uV

CHAPTER-6

CONCLUDING REMARKS AND FUTURE SCOPE

The adaptive biased OTA with large dc gain is proposed in the work. Slew rate of the proposed circuit is quite high with low settling time, so the circuit can response effectively for the analog circuits with high switching applications. Common-mode rejection ratio is high enough to suppress the input signals which are common to both input terminals and provide high gain to the signals which are differential. It is observed that as the stand-by biasing current increases, the gain of the circuit increases due to increase in transconductance. But, after a certain limit, with the increase in stand-by biasing current, the gain of the circuit decreases due to decrease in the output resistance. The phase margin of 60^o to 70^o is good for the stable circuit operation and this requirement is also fulfilled by the proposed OTA. Due to adaptive biasing in the proposed OTA, the mismatched effects of the circuit are reduces which makes the circuit more sensitive to even very small differential inputs. So, the proposed OTA proves can be widely used in all biomedical equipments as these require high sensitivity and precision. Also, the OTA can be used to design voltage controlled resistors, oscillators, modulators, g_m-C filters, data converters, sample and hold circuits etc.

The proposed OTA can be converted into programmable OTA only by using additional circuitry for the biasing current and the programmable OTA can be used to design various tunable analog circuits.

REFERENCES

[1]. P. E. Allen and D. R. Holberg, "CMOS analog circuit design", 3rd ed., Oxford University Press 2002.

[2]. Z. Wang, "Analytical determination of output resistance and DC matching errors in MOS current mirrors", IEE Proceedings G - Circuits, Devices and Systems , vol. 137,Issue 5, pp.397-404,Oct. 1990.

[3]. S.S. Rajput and S.S. Jamuar, "A Current mirror for low voltage, high performance analog circuits", Analog Integrated Circuits and Signal Processing, vol. 36, Issue 3, pp. 221-233, Nov. 2003.

[4]. Behzad Razavi, "Design of analog CMOS integrated circuits", MGH Edition 2002.

[5]. Jacob Baker, Harry W. Li and David E. Boyce, "CMOS Circuit Design, Layout and Simulation", 2nd ed., IEEE Press, 2005.

[6]. H. Elwan, W. Gao, R. Sadkowski, and M. Ismail, "CMOS low-voltage Class-AB operational transconductance amplifier", Electronics Letter., vol. 36, no. 17, pp. 1439-1440, Aug. 2000.

[7]. G. Palmisano, G. Palumbo and S.Pennisi, " Design procedure for two stage CMOS operational transconductance amplifiers: A tutorial", Analog integrated circuit and signal processing, vol.27, Issue 3, pp.179-189, May 2001

[8]. L. Bouzerara and M. T. Belaroussi, "Low-voltage, low-power and high gain CMOS operational transconductance amplifier", IEEE International Symposium on Circuits and Systems, vol.1, pp. 325-328, May 2002.

[9]. You Zheng, "operational transconductance amplifiers for gigahertz applications", 2008.

[10]. A. S. Sedra and K. C. Smith, "Microelectronic circuits", 4th ed., oxford University Press,2000.

[11]. R. Wang and R. Harjani, "Partial positive feedback for gain enhancement of low-power CMOS OTAs", Analog Integrated Circuits and Signal Processing, vol. 8, Issue 1, pp. 21-35, July 1995.

[12]. A. J. Lopez-Martin, Sushmita Baswa, J. R. Angulo and R.G. Carvajal, "Low-voltage super class AB CMOS OTA cells with very high slew rate and power efficiency," IEEE Journal on Solid State Circuits, vol. 40, no. 5, pp.

1068-1077, May 2005.

[13]. L. Bouzerara, M. T. Belaroussi and B. Amirouche, " Low-voltage, low-power and high gain CMOS OTA using active positive feedback with feedforward and FDCM teachniques", IEEE 23rd International Conference on Microelectronics (MIEL),vol.2, pp.573-576,May 2002.

[14]. Airong Liu, Huazhong Yang," Low voltage low power class AB OTA with negative resistance load," IEEE International Conference on Circuit and System proceedings, vol. 4, pp. 2251-2254, June2006.

[15]. J. A. Galn , A. J. Martin, J. R. Angulo and R .G .Carvajal," Super Class-abota with adaptive biasing and dynamic output current scaling," ;IEEE Transaction on Circuits and Systems,vol.54,no.3, pp. 2251-2254,March 2007.

[16]. Giuseppe Ferri, Vincenzo Stornelli and Angelo Celeste, " Integrated rail-to-rail low-voltage low-power enhanced dc gain fully differential operational transconductance amplifier", ETRI Journal, vol.29, no.6, pp. 785-893, Dec.2007.

[17]. Farzan Rezaei and Seyed Javad Azhari, "A highly linear operational transconductance amplifier (OTA) with high common-mode rejection ratio", International Conference on Signal Acquisition and Processings (ICSAP), pp. 18-22, Feb.2010.

[18]. Tuan Vu Cao, Dag T. Wisland, Tor Sverre Lande and Farshad Moradi, " Rail-to-rail low-power fully differential OTA utilizing adaptive biasing and partial feedback", IEEE International Symposium on Circuits and Systems, pp. 2820-2823, June 2010.

[19]. Jafar Torfifard and Abu Khari Bin A'ain, "A power-efficient CMOS adaptive biasing operational transconductance amplifier", ETRI Journal, vol. 35, no. 2, pp.226-233, April 2013.

[20]. Shireen T. Sheikh, D.J. Dahigoankar and Hemant Lohana, "Comparative Analysis of CMOS OTA,"IOSR Journal of VLSI and Signal Processing (IOSR-JVSP), vol.1, Issue 3, pp. 01-05, Dec.2012

[21]. Pablo P.Nicoli, Francisco Veirano, Pablo Castro Lisboa and Fernando Silveira, "High slew-rate OTA with low quiescent current based on non-linear current mirror", IEEE 6th Latin American Symposium on Circuits and System, pp.1-4, Feb.2015.

[22]. A. Thanachayanont and W. Chaloenlarp, “Low-voltage, rail-to-rail, Gm-enhanced pseudo-differential class AB OTA,” IEEE 47th Midwest Symposium on Circuits and Systems, vol.1, pp.53-56, July 2004.

[23]. J. R. Angulo, Sushmita Baswa, A. J. Lopez-Martin and R.G. Carvajal, “Winner take all class AB input stage : a novel concept for low-voltage power-efficient class AB amplifiers”, International Symposium on Circuits and Systems, pp. 1028-1031, May 2004.

[24]. Ah-Reum Kim, Hyoung-Rae Kim, Yoon-Suk Park, Yoon-Kyung Choi and Bai-Sun Kong, “Low-power class-AB CMOS OTA with high slew-rate”, IEEE International SOC Design Conference , pp.313-316, Nov. 2009.

[25]. Wenchang Huangand Edgar Sánchez-Sinencio, “Robust highly linear high-frequency CMOS OTA with IM3 below-70 dB at 26 MHz”, IEEE Transactions on Circuits and Systems, vol. 53, no. 7, July 2006.

[26]. Giuseppe Ferri, Andrea De Marcellis, Vincenzo Stornelli and Angelo Celeste, “A rail-to-rail DC-enhanced adaptive biased fully differential OTA”, IEEE 18th European Conference on Circuit Theory and Design, pp. 527-530, Aug. 2007.

[27]. Luís H. C. Ferreira, Tales Cleber Pimenta, and Robson L. Moreno, “An ultra-low-voltage ultra-low-power CMOS miller OTA with rail-to-rail input/output swing”, IEEE Transaction on Circuit and System, vol. 54, no.10, pp.843-847, October 2007.

[28]. Tuan Vu Cao, Dag T. Wisland, Tor Sverre Lande and Farshad Moradi, “Low-power, enhanced gain adaptive biasing based operational transconductance amplifiers”, IEEE NORCHIP Conference, pp.1-4, Nov. 2009.

[29]. Seyed Javad Azhari and Farzan Rezaei, “High-linear, high CMRR, low power OTA with class AB output stage”, International journal of computer theory and engineering, vol. 2, no. 4, pp. 473-477, Aug.2010.

[30]. N. Nizza , A. Mondini and Paolo Bruschi, “A current feedback adaptive biasing method for class-AB OTA cells”, IEEE Conference on Research in Microelectronics and Electronics, pp. 186-189, July 2005.

[31]. T. Voo and C. Toumazou, “High speed current mirror resistive compensation technique”, Electronics Letter, vol.31, no.4, pp. 248-250, Feb.1995

[32]. Chun Wei Lin, Yu Huan Wu and Sheng Feng Lin, "A precise current subtractor design", International Conference on Circuits, System and Simulation IPCSIT, vol.7, pp. 82-86, May 2011.

[33]. Amanpreet Kaur and Rishikesh Pandey, "Current mode computational circuits for analog signal processing", International Journal of Advanced Research in Electrical, Electronics and Instrumentation Engineering (IJAREEIE), vol. 3, Issue 4, pp.8987–8995, April 2014.

[34]. Christoph Tzschoppe, Udo Jörges, Alexander Richter, Bastian Lindner and Frank Ellinger, "Theory and design of advanced CMOS current mirrors", SBMO/IEEE MTT-S International Conference on Microwave and Optoelectronics, pp.1-5, Nov.2015.

LIST OF PUBLICATION

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