TEMPERATURE DEPENDENT ANALYSIS OF MIXED CARBON NANOTUBE BUNDLE AS VLSI INTERCONNECTS

Thesis submitted in the partial fulfillment of the requirement for the award of degree of

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IN

VLSI DESIGN

Submitted by

AKRITI SAINI

Enroll no: 601361003

Under the guidance of

DR. MAYANK KUMAR RAI

Assistant Professor

DEPARTMENT OF ELECTRONICS AND COMMUNICATION ENGINEERING

THAPAR UNIVERSITY

PATIALA-147003, PUNJAB, INDIA

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DECLARATION

I hereby declare that the work which is being presented in the thesis entitled, "**Temperature dependent analysis of Mixed Carbon Nanotube bundle as VLSI interconnects**" in partial fulfilment of the requirement for the award of degree of M.Tech (VLSI Design) at Electronics and Communication Engineering Department of Thapar University, Patiala, is an authentic record of my own work carried out under the supervision of Dr. Mayank Kumar Rai, Assistant Professor, ECED.

The matter presented in this thesis has not been submitted in any other University/ Institute for the award of my degree.

Akriti Saini

Date: 23.6.2015

Akriti Saini

Enroll. No. 601361003

It is certified that the above statement made by the student is correct to the best of my knowledge and belief.

Mayank Kumar Rai

Date: 8 July 2015

Dr. Mayank Kumar Rai

Assistant Professor

ECED, Thapar University

Counter signed by:

Dr. Sanjay Sharma

Professor & Head

ECED, Thapar University

Patiala- 147004

Dr. S. S. Bhatia

Dean of Academic Affairs

Thapar University

Patiala- 147004

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ABSTRACT

With advancement in technology as the scaling down of transistors has been accomplished, more and more number of transistors can be fit into a small area of Silicon making it more challenging for the design engineers and VLSI IC manufacturers. This is due to the fact that scaling down of transistors decreases the channel length which leads to more tendency of occurrence of leakage, power loss, thermal dissipation, scattering etc. in interconnects. Also incorporation of large number of transistors in a single IC has lead to the increase in length of interconnects needed which ultimately leads to more propagation delay and power dissipation.

So to overcome these issues lot of materials used for interconnects are made thinner and longer but the earlier used materials like Al, Cu face the problems of electromigration, grain boundary scattering etc. which hinders the overall performance of the circuit. In recent times CNT has emerged as a promising alternative to these materials as it displays some outstanding physical properties suitable for VLSI interconnects. They are one dimensional conductors operating at high frequencies and can carry very high current.

Various parameters of different types of CNTs namely SWCNT, MWCNT, MCB have been worked upon by the researchers and it is found out that CNTs show better results than Cu in terms of propagation delay and power dissipation. Now it is important to optimize these parameters and find out which type of CNT works better.

In this thesis Mixed CNT bundle (MCB) analysis is done by considering the temperature dependent impedance parameters and the results are compared with SWCNT and Cu at varied temperature and for different global lengths of interconnect.

Also various structures of MCB were studied to find out the optimized structure in terms of delay and average power dissipation which can be considered for further studies and a structure with horizontally aligned equal halves of SWCNTs and MWCNTs in a bundle shows the overall better results than other structures of MCB as well SWCNT and Cu. To achieve this modeling of transmission line (TL) of these bundles is done to find out the delay and hence the performance. Meanwhile the results also depict that there is an increase in delay as the temperature increases.

Analytical modeling for global length of interconnect is done by piece-wise transient analysis using alpha-power law model for CMOS inverter driving a π-RLC interconnect using

a fast ramp input signal to predict the response. This response is compared to the SPICE simulation results showing that in the saturation region there is certain difference in the responses while keeping the same discharging time for both. This calls for the need to develop a new and better analytical model for the deep sub-micron technology.

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ABBREVIATIONS

IC	Integrated Circuit
Cu	Copper
CMOS	Complementary Metal Oxide Semiconductor
CNT	Carbon Nanotube
FET	Field Effect Transistor
GNR	Graphene Nanoribbon
GHz	Giga Hertz
MFP	Mean Free Path
MWCNT	Multi Walled Carbon Nanotube
RC	Resistance-Capacitance
RLC	Resistance-Inductance-Capacitance
SPICE	Simulation Program with Integrated Circuit Emphasis
SWCNT	Single Walled Carbon Nanotube
VLSI	Very Large Scale Integration
MCB	Mixed CNT bundle
ESC	Equivalent single conductor
MESC	Multi ESC
ITRS	International technology roadmap for semiconductors
MTL	Multiple transmission line
AR	Aspect ratio
Al	Aluminum

Chapter

1

CARBON NANOTUBE

1.1 Introduction

Electrical connections between two or more nodes of the circuit or system formed in the silicon chip are formed by VLSI interconnects which are a thin film of conducting material. Hence, interconnects play a important role in electronics and communication engineering applications, especially in microelectronics and circuits since they are used as micro and nano interconnects for transporting electric currents inside ICs. All components in an IC are connected with interconnects. Interconnections are used to provide power supply, clock and ground supply to a device and also to provide the output of one device to another device[1].

It is a 3D structure with resistance and capacitance associated to it. Interconnects act as a transmission line and delay caused by them in the circuit is a factor of important concern as technology is scaled down because with scaled down technology more number of transistors etc. are able to be placed on a single chip, so length of interconnects connecting them increase which can lead to increase in delay. So it has become really important to realize an accurate equivalent circuit model for interconnects.

There are basically three types of interconnects: local, intermediate and global interconnects. Local interconnects consist of very thin lines, connecting gates, and transistors within a functional block and span only a few gates. Intermediate interconnects are wider and taller than local interconnects in order to provide lower resistance. It provides clock and signal distribution within a functional block. Global interconnects provide clock and signal distribution between the functional blocks and deliver power/ground to all functions [2]. Global interconnects occupy the top one or two layers, and they are as long as half the chip perimeter. It is critical that low-resistivity global interconnects be used as the bias voltage decreases and the total current consumption of the chip increases. Also it is very important to have very less propagation delay in case of interconnects especially in case of global

interconnects as they are larger in length and also used to provide clock.

Various modeling strategies like Pi, T, H, Hybrid Pi model etc are implemented for realizing the interconnects practically. A design engineer models the interconnect structure for optimization of performance in terms of reduced delay. Many materials have been used as an interconnect material and replaced by other due to their shortcomings or depending upon their applications and also as the technology is scaling down.

With advancement in technology as the scaling down of transistors has been accomplished, more and more number of transistors can fit into a small area of Silicon making it more challenging for the design engineers and VLSI IC manufacturers. This is due to the fact that scaling down of transistors decreases the channel length which leads to more tendency of occurrence of leakage, power loss, thermal dissipation, scattering etc. in interconnects. Also incorporation of large number of transistors in a single IC has lead to the increase in length of interconnects needed which ultimately leads to more propagation delay and power dissipation.

So to overcome these issues lot of materials used for interconnects are made thinner and longer but the earlier used materials like Al, Cu face the problems of electromigration, grain boundary scattering etc. which hinders the overall performance of the circuit. In recent times CNT has emerged as a promising alternative to these materials as it displays some outstanding physical properties suitable for VLSI interconnects. They are one dimensional conductors operating at high frequencies and can carry very high current.

1.2 Objectives worked upon in the report

Following objectives have been worked upon in this thesis report:

1. Development of temperature dependent impedance parameters of various structures of Mixed CNT bundle based interconnect.
2. Study of analytical timing model to extract the transient response of the far end of the Mixed CNT bundle based interconnect using CMOS inverter driver π- RLC circuit.
3. A comparative analysis of analytically extracted transient response at the far end of interconnect for Mixed CNT bundle at 22nm technology node.
4. Study the effect of temperature variation and varied length for global interconnects on delay analysis and power dissipation analysis in Mixed CNT bundle interconnect.
5. Comparison of results obtained from the above analysis with results for Cu interconnect

at different temperature and different length of interconnect at 22nm technology node.

1.3 Organisation of report

Chapter 2 gives the literature review of CNT as an interconnect over Cu for different interconnect technologies. Literature review of models for interconnect delays has been done showing the performance analysis of CNT (SWCNT, MWCNT, MCB) over Cu and also with varying length, pitch diameter and temperature. Delay analysis of CNT is done and role of repeaters is also discussed. Analytical delay models are discussed which are further analyzed in the next chapter.

Chapter 3 shows the temperature dependent impedance parameters for three different structures of MCB. Analysis is done of the parameters for all the structures used at different temperature and also at different global length of interconnect at 22nm technology node. Also the temperature dependent and independent parameters are compared to find out the difference.

Chapter 4 focuses on analytical delay prediction model for CMOS inverter driving π-RLC load interconnect. Alpha-power law MOS model is used to model the CMOS inverter and analytically extracted response of interconnect is then compared to SPICE simulated results for a MCB structure at given temperature. Temperature dependent delay analysis and power analysis is done for MCB structures at varying length and delay is also compared with the temperature independent delay analysis of these structures.

Chapter 5 compares the delay and power performance of CNT interconnect with Cu for different temperature and also at varying global length of interconnect at 22nm technology node.

Chapter 6 marks the conclusion and the future scope for this thesis report.

Chapter

2

LITERATURE REVIEW

2.1 Introduction

In IC manufacturing industry CNT has become a prominent material during the last decade due to the extraordinary physical and chemical properties and are regarded as ideal material for future on-chip VLSI interconnects in deep sub micron technologies. The existing Cu interconnect technology has reached its peak scaling limits as the grain size decreases with scaling because of which their resistivity increases and grain boundary scattering occurs due to which alternate technologies are required to meet the future requirements.

2.2 CNT as future interconnect

2.2.1 Materials used as VLSI interconnects and problems with existing materials

(a) Aluminum as an interconnect

The most widely used material as interconnect earlier was aluminum due to its good conductivity and adherence on silicon dioxide. But due to scaling down of technology as the density of device increased current density for interconnects increased. In case of aluminum at higher current density considerable amount of electromigration takes place. Electromigration is the transport of material caused by the gradual movement of the ions in a conductor due to the momentum transfer between conducting electrons and diffusing metal atoms. In microelectronics and related structures this effect is important as high current density is involved. This effect increases with decrease in structure size such as integrated circuits[3].

Another limitation of using aluminum as interconnect is its higher resistivity which is 2.67 μΩ –cm which is much higher than that of pure copper which is 1.7 μΩ –cm. As higher resistivity leads to higher delay pure aluminum is not used as an interconnection material. Copper was introduced as an alternative to this.

(b) Copper as an interconnect

Due to limitations imposed by aluminum, copper with higher conductivity and a material with higher resistance to electromigration than aluminum is considered as an interconnect with scaling down of technology. Copper is capable of withstanding five times more current density than aluminum with equal reliability for IC applications. Copper due to its higher electrical conductivity and relatively higher melting point and other advantages over aluminum has evolved as interconnect material especially for submicron and deep sub micron high density and high performance chips [4-17].

In the quest for making low power devices and applications that are as miniaturized as possible, researchers in integrated circuit (IC) industry are often pondering upon new techniques to achieve the same. Since the first IC is formed, many improvements and alterations in the process technology, especially lithography techniques, are done to downscale the feature sizes to 22nm at present and future scaling up to 14nm and 12nm are on the pipeline. Obviously, many bottlenecks like leakage of current, tunneling, power and thermal dissipation, reliability and performance are found to hinder further feature miniaturization. **[**18].

Due to increase in chip interconnects due to scaling down of technology, the cross-sectional dimensions of interconnects are reduced rapidly to accommodate more number of interconnects, resulting in dimensions of the order of MFP of electrons in copper (~ 40 nm at room temperature). As the dimension approaches electron mean free path the problems like grain boundary and surface scattering are enhanced eventually leading to higher resistivity of interconnect[3,19]**.** Another effect of dimension scaling is increase in current density. Thus as technology scales these effects on resistivity together with increase in interconnect resistance with length enhances delay. Also not only delay but interconnect power dissipation increases because of increased current density and increase in frequency of operation. The increased heating due to the rise in power dissipation assists electromigration. So copper also faces these limitations with increase in technology.

Due to increase in electromigration and grain boundary scattering, the existing Copper technology for VLSI interconnects cannot be scaled further beyond 22nm. So, next we see

how Carbon nanotubes are becoming the most sought after material for next generation VLSI interconnect technology**.**

(c) Carbon nanotube as VLSI interconnect

Carbon nanotubes were formally found by Sumo Lijima of NEC-Japan in 1991. Scientists have found out that CNTs have exceptional current carrying capabilities of 10^9 A/cm^2 which makes them suitable for interconnect applications and hence can be used as very long and thin interconnects at more scaled down technology nodes than copper.

The aspect ratio (length to diameter ratio) of CNTs is very high and is of the order of 10^4. So, it is essentially a 1D quantum wire with special characteristics. Ballistic conduction takes place in these 1D conductors. Hence the electron movement is non diffusive in nature. This phenomenon reveals that electrons travel like waves in the structure and also they have large mean free paths (MFPs). So, CNT based interconnects are suitable for high frequency integrated circuits that is the future of the technology [18].

Table 1.1: Summary of properties of carbon nanotubes[20,21].

Property	Value
Density	1.33 g/cm^3
Bandgap	0eV for conducting 0.5eV for semiconducting
Current density	10^{14} A/m^2
Thermal conductivity	5800 W/mK
Phonon mean free path	100 nm
Resistance range	7kΩ-100kΩ

K.Banerjee *et al.* [22] have examined the state of art in CNT interconnect research and discussed both the advantages and challenges of this emerging technology and also shown that due to increasing resistivity of copper with technology scaling how CNT is emerging as the new promising material for interconnects. Below shown Figure 2.1 indicates the increase

in resistivity and current density in Cu with increase in technology node which also increases reliability concern due to joule heating inducing significant metal temperature rise [36,37].

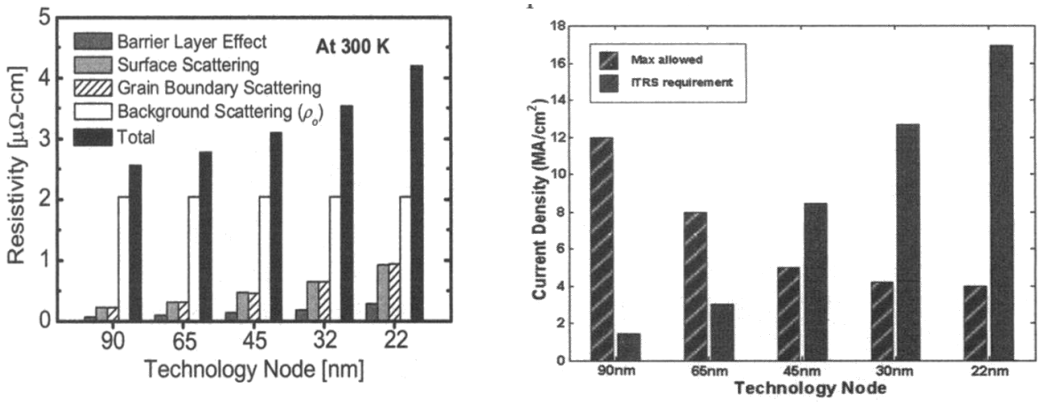


Figure 2.1: The increase in resistivity and current density in Cu with increase in technology node [22].

As the scaling goes beyond 22nm, new materials that can achieve good performance and reliability are being introduced like Carbon nanotubes. They have very large mean free paths up to few micrometers at room temperatures, high current carrying capacity, resistance to electromigration, high thermal conductivity and ability to conduct at very high frequencies (Azad Naeemi *et al.* [28-32])**.** Due to sp2 bonding CNTs are having lesser problem of electromigration than Cu and can carry high current densities [38,39].

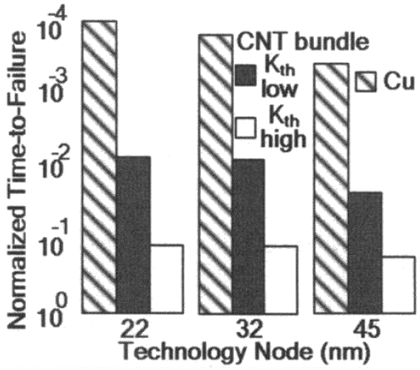


Figure 2.2: Cu interconnect electromigration (EM) lifetimes as a result of high interconnect temperatures normalized to EM lifetime at reference temperature of 378 K when vias are composed of Cu and CNT bundles respectively [22].

As technology advances and the device size is scaled down more and more number of devices are fitted on the ICs and interconnect lengths required to connect them increases and hence its impact on the performance of digital integrated circuits is becoming increasingly significant. The longer the interconnects higher is the propagation delay. (Sakurai [40]), when the resistive component of the interconnect load becomes comparable to the gate output

impedance, a single capacitor is no longer a valid gate load model. The line resistance R acts as capacitance shielding, and as it increases this shielding becomes significant and the output waveform presents an RC tail.

2.2.2 Theory of Carbon nanotubes

Carbon nanotubes are in the shape of cylinders, formed by rolling up of Graphene sheets with diameter of the order of nanometer. Graphene, is a one atom thick layer of Graphite. So, CNTs are constructed with a basic element of a hexagonal ring of carbon – carbon bonds [22-24]. The C-C bonds in the hexagon of a Graphene sheet are sp^2 hybridized as shown in Figure 2.3.

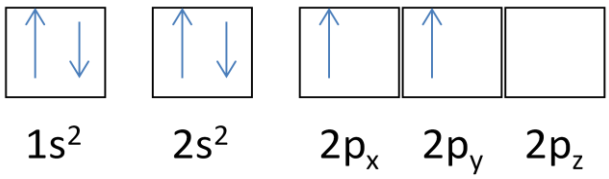


Figure 2.3 : sp^2 hybridization of C-C bonds.

The pi bonds are not attached to any other bonds and are free to combine with other elements, known as dangling bonds contributing to the electrical conduction in metallic CNTs. Depending on the axis we roll up the Graphene sheet, CNTs can be either conducting or semiconducting in nature, known as chirality [22]. For interconnect applications, the metallic CNTs are useful because of their high thermal and mechanical stability.

The fabrication process of CNTs using chemical vapour deposition involves sputtering and deposition of metal catalysts on the substrate while a carbon containing species is blown over it in a CVD apparatus. At high temperatures, the carbon in the species diffuses and reacts with the metal catalyst to form long wires of CNTs. Depending on the metal catalyst and the temperature and pressure, they can be either single walled or multi walled CNTs.

2.3 Performance analysis of SWCNT, MWCNT, Mixed CNT bundle

2.3.1 Types of CNTs

Carbon nanotubes can be grown in various forms as in: single walled CNTs (SWCNTs), multi walled CNTs (MWCNTs) and mixed CNT bundles (MCBs).

(a) SWCNTs

SWCNT is the basic structure of CNT consisting of one shell of rolled up Grapheme sheet. Depending upon the way it is rolled or its chirality it can have armchair, zig zag or

chiral configuration making it metallic or non-metallic in nature. It is a zero bandgap semiconductor.

The high current density of electron carriers (~10^9 A/cm^2) in metallic CNTs is due to the reduced electron-phonon scattering, strong bonding and ability to conduct at very high temperatures[25,26]. These properties make them ideal for interconnect applications.

Distribution of metallic and semiconducting CNTs in bundle is very significant for optimizing the conductance. Diameter dependence of resistance of SWCNT bundles is also important to determine the overall conductivity. The factors that are responsible for the resistance of CNT bundles are individual nanotube diameters, density of nanotubes in the bundle and the bundle's geometric configuration. Resistance of SWCNT bundles reduces 90% in comparison to Cu interconnects if the diameter is 0.5nm whereas it reduces by 50% when the diameter is 1nm. The diameter of a single walled nanotube is normally considered as 1nm [27]. Therefore, one third of an SWCNT bundle contains metallic CNTs in it. So, in scaled technologies, more metallic CNTs are needed to keep bundle resistance independent of bias voltage. CNTs in a bundle have weak coupling and hence carry currents independent of each other [28-31].

The most popular transmission line (TL) model is discussed here that is followed by many researchers in CNT interconnect as well as Cu interconnect modeling. Ideally, the CNT is considered to be placed over a ground plane as shown in Figure 2.4

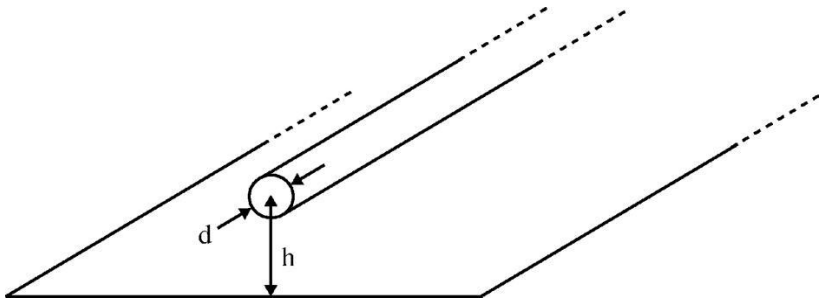


Figure 2.4 : CNT placed over a ground plane, Equivalent Structure of Carbon nanotube[2].

This equivalent circuit is then used in analysis and simulation of interconnect performance. The separation between the nanotube and the ground is 'y' and the diameter of the SWCNT is 'd'. Assuming SWCNT to be in cylindrical form, an electrical equivalent of the structure as shown in Figure 2.5 as-

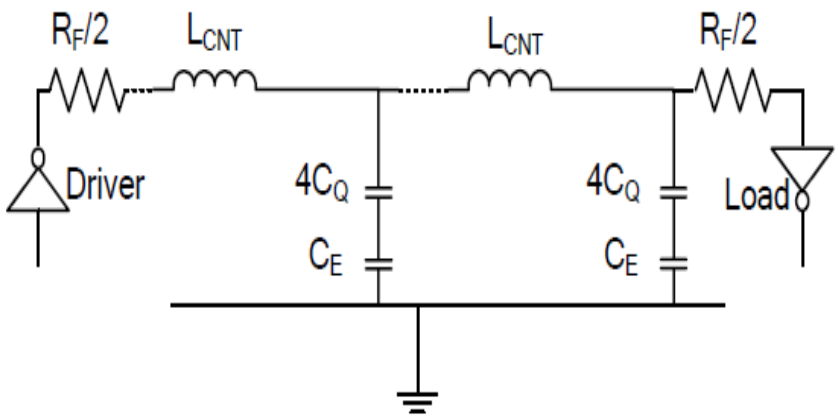


Figure 2.5 : Equivalent RLC circuit for an isolated SWCNT[2].

In practical reality, not all CNTs of a bundle are metallic. Non-metallic SWCNTs are treated as not contributing to current conduction and their presence is taken into account by considering "sparsely" populated bundles.

Due to the lack of control on chirality, any bundle of SWCNTs consists of metallic as well as semi-conducting nanotubes (the semi-conducting CNTs do not contribute to current conduction in interconnects). Although multi-walled CNTs (MWCNTs) are predominantly metallic, it is difficult to achieve ballistic transport over long lengths with them. Single-walled CNTs (SWCNTs) on the other hand, have electron mean free paths of the order of a 1 micron. Hence, in the domain of interconnects, metallic SWCNTs are the preferred candidates.

(b) MWCNTs

The structure of MWCNT is more complex than SWCNT. MWCNTs have concentric shells that are either metallic or semiconducting. The adjacent shells in an MWCNT are separated by 0.34nm due to the vander Waal force of attraction. The number of conducting channels per shell depends on K_BT, where K_B and T are Boltzmann constant and temperature respectively. Each shell has different band structure and hence, complex analysis is required for studying its properties. The structure of an MWCNT placed over a ground plane is shown in Figure 2.6. This is the most widely used model for MWCNT interconnect design.

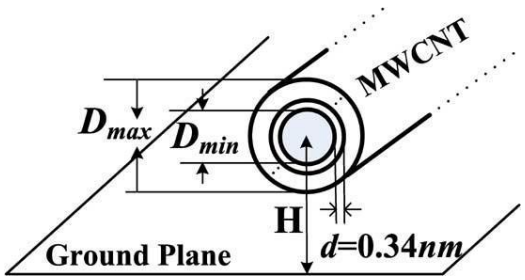


Figure 2.6 : Structure of a MWCNT over a ground plane [32].

The MFP of an MWCNT is directly proportional to its diameter irrespective of whether it is metallic or semiconducting. Due to the presence of more conduction channels, MWCNTs exhibit better conductivity than SWCNTs. However, perfect contacts should be made to all the shells to avoid high contact resistance. Multiple shell conduction is possible at higher temperatures because of more conducting channels inside. An isolated MWCNT is placed on an infinite ground plane and the concept behind conduction of multiple shells was explained earlier [32]. MWCNTs are best suited for both intermediate and global interconnects. When compared with Cu, MWCNTs have shown enhanced improvements of signal delay.

Figure 2.7 shows the equivalent distributed circuit model for an individual shell of MWCNT where R_{mc} is the imperfect contact resistance, R_Q is the quantum contact resistance, R_S is the scattering-induced resistance, L_K and L_M are the kinetic and magnetic inductances respectively, and C_Q and C_E are the quantum and electrostatic capacitances, respectively.

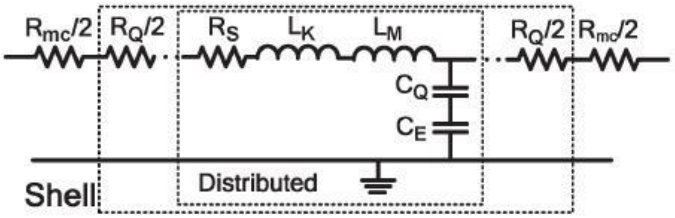


Figure 2.7: Equivalent distributed circuit model of an individual shell [32].

The concentric shells in MWCNTs have varying conductivity as they have different chirality. However, at higher temperatures, multiple shell conduction is possible (P.G. Collins *et al.* [59]. This is because at high temperatures where ICs work, the electrons in semiconducting shells get excited and hence they behave like conducting shells thereby contributing more number of conducting channels in the MWCNT. So, the overall conductivity is better than SWCNTs as they have more number of conduction channels. However, perfect contacts should be made to all the shells to avoid high contact resistance.

MWCNTs are proposed as long global interconnects as they have large conductivities at long lengths. As these nanotubes are long and have large diameters, their MFP also is large. The spacing between two adjacent shells is given by the van der Waals force of attraction (0.34 nm). Conductivity models of MWCNTs are further studied in a comprehensive distributed circuit model for MWCNTs is described in (H.Li *et al.* [53]). Here, an isolated MWCNT is considered on an infinite ground plane. The concept behind conduction of multiple shells is further explained here.

The various resistances associated with MWCNTs are quantum contact resistance R_Q (=12.9kΩ), scattering induced resistance R_S, and imperfect contact resistance R_{mc}. R_S and R_Q are intrinsic and R_{mc} is due to fabrication process. R_S is present in only larger than MFP nanotubes. Figure 2.8 shows the circuit of an MWCNT interconnect. The MFP of a MWCNT is directly proportional to its diameter irrespective of whether it is metallic or semiconducting.

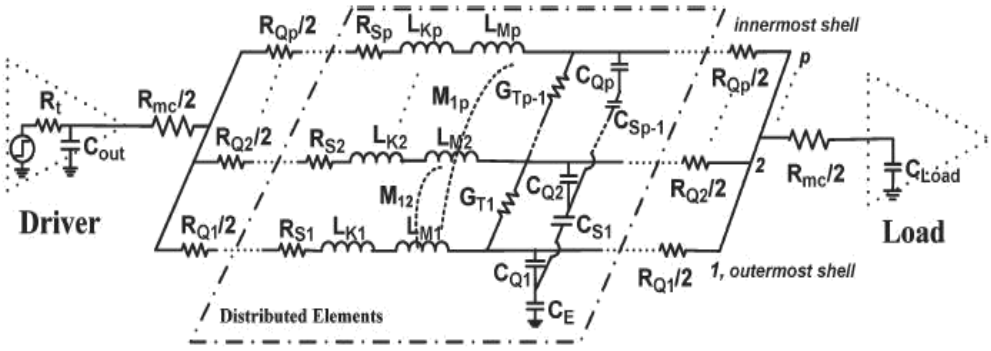


Figure 2.8: Equivalent distributed circuit model of an MWCNT with p shells [53].

Normally, the magnetic and kinetic inductances are measured per unit length. The magnetic inductance L_M is one to two orders smaller than the kinetic inductance L_K and hence, is neglected in the literature. The quantum capacitance C_Q is calculated as ≈193 aF/μm. Unlike SWCNT bundles, MWCNT structures cannot be converted into simple circuit models since they have shells with varying diameters. This means different shells have different channel numbers and varying MFPs giving rise to different circuit parameters. So, these parameters cannot be combined in a way like in SWCNT bundles. Also, the potentials are different for different diameters and hence, shell to shell electrostatic coupling capacitance is present. It will be very high due to small separation between adjacent shells. The tunneling phenomenon in MWCNTs is explained and the equivalent circuit with RLC parameters is

shown (H. Li, *et al.* [53]). The attractiveness in MWCNTs lies in their independence on chirality. They are very useful in immediate applications as global and intermediate interconnects. Further, they are studied as power interconnects at intermediate level (A. Naeemi *et al*. [31]). At 50 nm diameter, they provide 2.3 times smaller sheet resistance compared to Cu.

As the diameter of each CNT and length of the CNT bundles increases, the relative stability increases. M.S. Sarto, *et al.* [61] presents a rigorous work on the equivalent single conductor (ESC) transmission line model of MWCNTs that is derived from the complex multi-conductor model. Generally, metallic nanotubes are modelled as 1-D conductors having *n* conducting channels in parallel and only one of the two sub bands crossing the Fermi level. Including the spin degeneracy, CNTs have *n* =2. The ESC model is applicable till 10GHz with a relative percent error of 1% and another few percent as the frequency increases to 50GHz and beyond.

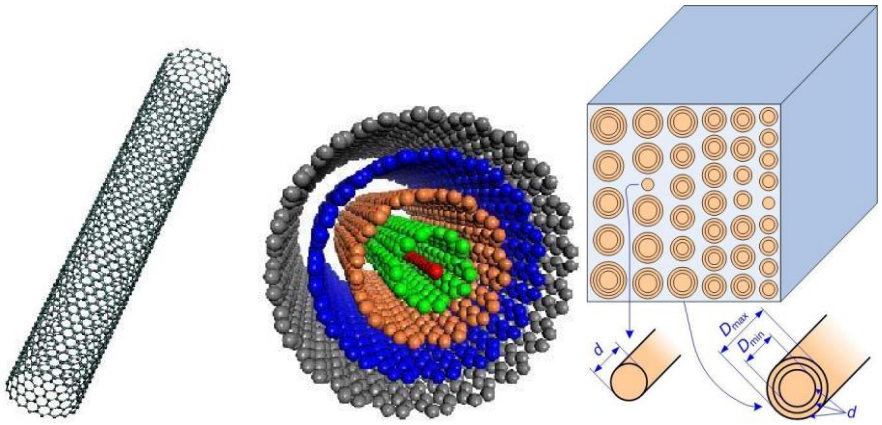
(c) Mixed CNT (MCB):

Since SWCNTs show more desirable material properties than MWCNTs which are also more complex to fabricate, most existing studies focused on the SWCNT. Individual SWCNTs suffer from an intrinsic ballistic resistance of approximately, which can cause excessive delay. To reduce the impact of the individual tube, bundles of SWCNTs in parallel are more in favor. However, the CNT bundles are generally a mixed CNT bundles consisting of multiwall as well as single wall CNT. Experimental results demonstrate that a realistic nanotube bundle is a mixed bundle of single- and multi-wall CNTs.

Mixed CNT bundles are a new class of materials that were conceived lately as the interconnect material. The R, L, C of MCBs is reviewed here. The mean free path (MFP) of a mixed CNT bundle is dependent on the individual mean free paths of SWCNTs and MWCNTs in it. SWCNTs have an MFP of around 1μm considering perfect contacts at room temperature. The value of MFP is proportional to tube diameter (both metallic and semiconducting). So, MWCNTs, which are large in diameter, possess large MFP. Thus, mixed CNT bundles with metallic SWCNTs and large diameter MWCNTs at the core will have large mean free paths.

In a large diameter nanotube, phonon scattering becomes negligible. The high density of electrons due to more no. of conducting channels in large diameter MWCNTs in the bundle leads to larger mean free paths. Mixed CNT bundle conductance was derived from total no. of shells, shell diameter and number of conducting channels per shell. A bundle of large diameter has more CNTs in it and hence improved conductance. Also, increase in length beyond mean free path will reduce conductance. However, MCBs possess very large mean free paths. MCBs show better conductance than Cu as obtained in chapter 3 and 4.

The magnetic inductance depends on the magnetic field around and inside a bundle. The total kinetic inductance of an MCB depends on total number of channels and no. of shells. For two channels which represent spin up and spin down of electrons, L_K per channel is around 8nH/μm. Diameter of the tube determines the number of conducting channels (W. Wang, *et al.* [62]). Metallic SWCNTs has N=2 while semiconducting tubes has N=0. MWCNT shells with diameter >4nm have conducting sub-bands. Also, large diameter semiconducting shells will also have some sub-bands as its energy gap is reduced. So, large diameter MWCNTs are preferred in MCB interconnects.



(a) (b) (c)

Figure 2.9: (a) SWCNT (b) MWCNT (c) MCB [41].

In deep-submicron, designers tend to keep a high Aspect Ratio (ratio of interconnect thickness/height) since higher interconnect thickness/height decreases the inter-line capacitance. But, the two-dimensional fringing fields and capacitances between neighbouring lines become important and, after a certain point, larger aspect ratios yield no additional advantage. Figure 2.9 shows all the types of CNT i.e. SWCNT, MWCNT, MCB.

N. Alam *et al.* [41] presented a comprehensive analysis of mixed bundles of CNTs and

compared various transmission line model interconnect parameters with that of Cu showing that CNTs have smaller impedance parameters at intermediate and global level than Cu. Therefore, more accurate load models have to be used for taking into account the increased role of the resistance in the determination of the load behavior and consequently the propagation delay of the driving CMOS gates.

For a single transistor that drives many clock lines, the network of clock lines produces excessive clock skew and sets an upper limit on clock frequency (Bakoglu and Mendl[42,43]). Clock frequency determines the overall performance of the chip (cycle time, access time, instructions per second) because, despite its fast switching speed, a transistor must normally wait until the next clock cycle before it can change its state.

In contrast, all these phenomena find their applications at high temperatures. Lüttinger liquid theory for SWCNTs is studied in detail and its application in CNT interconnects was explained by P.J. Burke [44]. Additionally, resonant tunneling through discrete energy levels and proximity- induced superconductivity were experienced at high temperatures according to Burke. He presented the RF circuit model as a base for research of nanotube transistors with high frequency speed.

2.3.2 Effect of interconnect length on delay analysis

CNTs are modeled as transmission lines and these wires have varying lengths according to the signal it propagates[47]. At short lengths, the driver resistance is dominant and latency is determined by capacitance and not resistance. So, mono- layered CNT bundles were preferred as ideal for interconnects due to its smaller kinetic inductance (A. Naeemi *et al.* [29,45]). The inter-CNT (or line to line) capacitance comes into play in CNT bundles and this will increase the capacitance drastically. So, mono- layer and bi- layer interconnects are confined as short local interconnects due to their large resistances and time of flights. But later it was disproved that mono layer interconnects are not feasible as they cannot be used beyond 1µm lengths in advanced technology nodes due to their high resistance (Navin Srivastava *et al*. [46]).

SWCNTs are quantum wires that have quantum effects of kinetic inductance and quantum capacitance due to the energy transfer and the charging up of the energy states. Modeling of CNT interconnects is very important to understand its electrical transportation

and hence to derive its impedance and delay for the performance comparison with Cu technology.

CNT interconnects are used at local, intermediate and global levels in an IC according to A. Nieuwoudt and Y. Massoud [48]. Local interconnects are short and have lengths up to 3μm. They are used to connect gates of transistors. Intermediate interconnects are used to carry signals between two or more logical blocks. The delay is determined by the RC product at this level. Improved latency and larger mean free path are the advantages of CNTs at intermediate level. Density of metallic nanotubes is also important. Typically, CNTs have the same performance as Cu at this level. Global interconnects, that carry clock signals, are larger in dimensions. They can have large mutual inductance which leads to crosstalk induced noise. They also found out that optimized nanotube bundles can provide up to 69% delay reduction in 22nm technology node [49,50].

2.3.3 Delay models

The optimization of wire width for global interconnects was done by A.Naeemi [31]. The performance limiter of interconnects at global and intermediate levels is the number of metallic CNTs in the bundle. The delay models include the RLC parameters rather than RC delay models which give better delay estimates (N. Srivastava [46])**.** The metal- nanotube contact resistance varies with respect to temperature. SWCNTs provide four times reduction in power dissipation at 22nm node while it reduces by eight times at 14nm (A. Naeemi [51]).

The effect of scattering gives rise to scattering resistance or acoustic phonon resistance. This resistance is exponentially dependent on the length of the nanotube (A. Naeemi *et al.* [52]). However, it is assumed the resistance is linear with respect to the length. This is because, at small bias, the electrons will only be back-scattered by defects and acoustic phonons, which lead to large MFPs of 1.6μm. H. Li *et al.* [53] considered contact resistance as lumped and scattering resistance as distributed and on the basis of this model found out CNTs outperform Cu at intermediate and global level[54]. CNT bundles, should have large density of metallic nanotubes and all nanotubes should make good contact with the electrodes and the substrate. The diameter of a single nanotube is considered as 1nm throughout the literature. So, one metallic CNT is there for every 3 nm^2. The sum of individual resistances of the nanotubes gives the total resistance of the bundle. But, larger numbers of metallic CNTs

are needed in the bundle at scaled technologies to keep bundle resistance independent of bias voltage. CNTs in a bundle are assumed to have weak coupling and hence carry currents independent of each other (N. Srivastava *et al.* [55]). For a single CNT, the chemical reactivity leads to large tunneling barrier at the contacts. Hence, bundles of CNTs are preferred.

The kinetic energy of electrons due to the current flow gives rise to the kinetic inductance. Theoretically, the per unit length kinetic inductance is about 4nH/μm for an SWCNT bundle. The electrostatic capacitance comes into picture since energy is required to store electrons in available energy states. Initial models have neglected the inter-CNT capacitance citing that the nanotubes in a bundle are held at the same potential. The imperfect metal-nanotube contacts vary the potential in each CNT and hence inter-CNT capacitance will come into effect. The quantum capacitance arises due to the density of states of a CNT. At higher metallic CNT densities, C_Q becomes very small compared to C_E and hence is neglected. The roughness of the bundle also contributes to its capacitance. It was shown that the Cu wire capacitance is approximately same as the C_E of the SWCNT bundle (K.H. Koo *et al.* [56]). The capacitance values of CNT bundles are calculated per unit length. C_E is modeled by considering a CNT or a bundle of CNTs placed over a ground plane and calculating the capacitance between them.

Transient voltage analysis of multi equivalent single conductor (MESC) model of SWCNT bundles and MWCNTs is carried in M. D'Amore *et al.* [58]). The crosstalk is modeled and delay is compared with the 50% time delay of multi conductor TL (MTL) model. Both are in good agreement and it is pointed that MESC model is the simpler approach for finding effects induced by crosstalk coupling. Here, MWCNTs out performed SWCNT bundles in terms of delay. The outer shells of MWCNTs, compared to the inner ones, represent a low- impedance path at high frequencies.

2.3.4 Effect of pitch

There is a trend to increase the line width to increase the signal speed leading to reduction of spacing between two lines (smaller *pitch*). But Deodhar and Davis [59] showed that this leads to a continuous increase in resistance and capacitance showing negligible improvement in interconnect delays, even forcing longer RC interconnect delays with each

generation.

It is also reported by K. Banerjee and N. Srivastava [46] that pitch influences semi global and global relative performance of CNT as it does in case of local lengths. For the local interconnects, the influence of pitch on delay of CNT bundle is quite significant. It can be seen that with the increase in pitch the delay ratio of CNT bundle to Cu interconnect is increased.

2.3.5 Effect of tube diameter

Mayank K. Rai and S. Sarkar[63] addressed the influence of tube diameter on single walled carbon nanotube (SWCNT) bundle interconnect delay and power output in VLSI application. They found that SWCNT bundle interconnects are of lower delay than copper interconnect due to low resistance and inductance. Power dissipation decreases with increase in tube diameter of the constituent SWCNT. CNT interconnect resistance and inductance increases with increase in tube diameter. On the other hand, with increase in tube diameter interconnect capacitance decreases. There is a tradeoff between delay and power dependence on tube diameter.

Recent research in the study of metallic carbon nanotube by S. Sarkar *et al*. [64] suggests that at 32 nm and 22 nm nodes, CNT shows better relative performance for longer interconnects. They have reviewed all the possible parameters to explore the applicability of CNTs as future interconnects. Thus, as technology nodes are scaled down in the future, CNT has become the prospective material of future.

2.3.6 Effect of temperature

E. Pop *et al.* [76] did the first electro-thermal study of Single-walled CNT for interconnect applications. In this study it was suggested that at high bias self heating is significant in short length interconnects while above 250 K temperature the low bias resistance is also found to be affected.

M. K. Rai and S. Sarkar [77] analyzed for capacitive coupled SWCNT bundle interconnect and for Cu the crosstalk induced, temperature dependent, noise voltage waveform and the frequency spectrum at 22nm technology node and suggested a improved model for extracting inter bundle, coupling capacitances between single walled CNT bundles.

2.4 Delay analysis in CNT bundle interconnect

As the feature size decreases to the submicron dimension, the transmission-line effects now play an important role in determining interconnect delays and system performance (Ismail, et al., [65]). Various techniques have been proposed for the delay analysis of interconnects.

2.4.1 Analytical delay modeling

In order to find analytical expressions for the propagation delay and the output waveform shape, an interconnect line may be modeled in different ways. An expression for the propagation delay when a load is modeled simply by a resistor in series with a capacitor (RC model) was derived by Adler and E. G. Friedman[66] utilizing Elmore [67] delay model. Elmore delay approximation represents the first moment of the transfer function. Elmore's expression approximates the mid-point of the monotonic step response waveform by the mean of the impulse response as [67]

$$\tau Di = \int t.v(t)dt \quad (2.1)$$

For the general topology of this RC tree network, this formula can be modified as

$$\tau Di = \sum Cj\ N\ j{=}1 \sum Rk\ for\ all\ k{\in}j \quad (2.2)$$

which is the Elmore delay at node i of this RC tree, which has the following path definitions:

Pi denotes the unique path from the input node to node i, i = 1,2,3, ... , N.

$Pij = Pi \cap Pj$ denotes the portion of the path between the input and the node i, which is common to the path between the input and node j.

The limitation of Elmore delay is that it cannot accurately estimate the delay for RLC interconnects, i.e. interconnects in which inductive impedance cannot be ignored (Kahng and Muddu[68]). This is chiefly due to the fact that the Elmore delay does not cover nonmonotonic responses which can occur in RLC circuits. This impreciseness of Elmore delay is critical to current performance-driven routing methods which try to optimize interconnect section lengths and widths as well as driver and buffer sizes. In Friedman's model, the driving transistor was always considered to operate in linear mode and only the simplified case of step input was studied.

Sakurai [69] suggested the response and delay calculation for the distributed RC line. He used the Heaviside expression over the poles of the transfer function to calculate the time-

domain response from the transfer function. Then he used a single pole to approximate the response and observed the variation of delay with respect to load and source parameters. His heuristic delay formula is nearly identical to the Elmore delay equation. Therefore, it buffers of the same constraints related to Elmore delay model mentioned above.

Kahng *et al*. [70] used this delay model only to realize that it is not accurate for several source and load parameters and obtained a good and simple approximation of an interconnect line and studied various combinations of first and second moments, from which they incorporated inductance effects while assuming step input when developing their first delay analytical model of RLC interconnects. The developed solutions showed that their proposed analytical delay model estimates are within 15% of the SPICE delays while Elmore delay [67] estimates can vary as much as 50% from the SPICE-computed delays. Also, they found that when a π-model is used, RLC model achieves an accuracy better than 3% in delay calculations, which the L-model achieves in 100 segments. For this reason, π-model is often used in SPICE simulations instead of large number of segments as a rational approximation of distributed RC.

Sakurai [69], made the first attempt to model the interconnect line by a π-circuit, however the driving transistor was replaced by a simple resistor. More accurate analytical expressions for the propagation delay and the output waveform can be found if the corresponding system equations of an inverter driving a circuit are solved. Ismail and Friedman [71] introduced a simple controllable delay formula for RLC trees. They tried to preserve the useful characteristics of the Elmore delay model while maintaining the same accuracy characteristics. This delay model with the closed-form expressions considers all damping conditions of an RLC circuit including the under damped response, which was not considered by the Elmore delay due to the non-monotonic nature of the response. They have given an empirical relationship for the propagation delay of a CMOS gate driving a distributed resistive inductive capacitive load, which gives an error within 5 percent of AS/X simulations. These solutions are presented for the 50% delay, rise time, overshoots and settling time of signals in an RLC tree. Errors in propagation delay over 35% and use of larger area results of neglecting inductance in on-chip interconnects. The CMOS devices are modeled as discrete RC components.

D. Das and H. Rahaman [72] presented analytical model for timing and crosstalk in

CNT and on comparison with SPICE found out that it is very accurate and 250 times faster than SPICE. They considered a RLC circuit with contact resistance as lumped and scattering resistance as distributed where the analytical model for crosstalk analyzing with process variation is proposed by P. Sun and R. Luo [73] and the temperature effects on CNTs are analyzed by L. Jia and W. Yin [74] and W. C. Chen *et al* [75].

M.K. Majumdar *et al.* [78] presented a modeling hierarchy for MCB. On the basis of it various structures for MCBs are proposed and an ESC model for MCBs has also been developed and observed that delay performances in structures containing equal halves of SWCNTs and MWCNTs called the novel structures.

P.U. Sathyakam *et al.* [35] for the first time presented the accurate modeling hierarchy for MCB interconnects and found out that they are superior to both SWCNTs and MWCNTs in terms of propagation delay.

2.4.2 Inserting repeaters

The increase in load in VLSI circuits especially due to large fanouts and the long interconnects, emphasize the need for effective driver circuits that can discharge capacitances with sufficient speed, thus helping in delay minimization. The insertion of repeaters is used to minimize the interconnect response time by mitigating the effect of resistance and capacitance (Bakoglu[42]). Bakoglu and Meindl ([43]) proposed various types of repeaters viz. uniform cascaded and cascaded tapered repeaters to optimally drive resistive-capacitive interconnect to reduce the delay. They utilized Elmore approach to evaluate delay in interconnections loaded with such repeaters. They have shown that delay of a repeater loaded interconnect becomes a linear function of line length. MOSFETs have been modeled as discrete resistance and capacitance depending upon the geometric dimensions. They derived the optimum value of tapering factor for the cascaded buffer to be "e" the base of natural logarithm. However, this method is useful for capacitive loads as well as when interconnect resistance is small and driver resistance is dominant; but it is not adequate when interconnect resistance is comparable to or larger than driver resistance. Another important advantage of inserting repeaters within interconnect trees is to decouple a large capacitance from the critical path in order to minimize the total overall delay of the critical path.

2.4.3 Analytical method for an inverter driving π-RLC load

Much research effort has been devoted during the last few years to model CMOS gates

driving simple capacitive loads, especially *CMOS inverter/repeater*. The CMOS inverter is the simplest buffer or repeater in VLSI interconnects. Sakurai and Newton [69] gave alpha-power MOS model for current voltage characteristics for short channel MOSFETs. They included input waveform slope effects and parasitic drain/source resistance effects. The short channel CMOS inverter delay becomes less sensitive to the input waveform slope and to the V_{DD} variation as compared to the conventional classic MOSFETs based on square law model given by Shockley.

Recently, Kaushik, *et al*. [79] presented an analytical method with emphasis on the short-circuit power dissipation has been presented for an inverter driving an π-RLC load. The model shows an impressive accuracy. However, the proposed analysis is far too complex to be integrated into a CAD timing analysis system in spite of the simplified assumptions that are made for the short-circuit current.

2.5 Conclusion

With development of technology or we can say with scaling down of technology more number of transistors can fit in a single chip which leads to increase in the interconnect length required on chip which also leads to increase in propagation delay. To reduce it the material used for interconnects is changed from Al to Cu and now CNT which proves to be a promising alternative to Cu at deep sub- micron technology. Further to reduce the delay various delay models have been developed by the researchers. The effect of various interconnect parameters like length, diameter etc. are calculated by various researchers on the impedance parameters which is used for delay analysis. Also efforts have been made to study the effect of temperature on CNT.

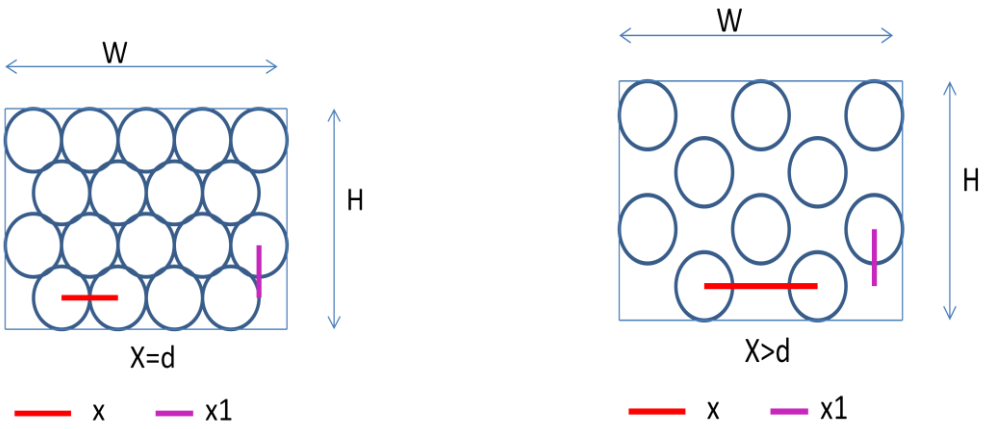
Chapter

3

TEMPERATURE DEPENDENT CIRCUIT PARAMETERS OF MIXED CNT BUNDLE

3.1 Introduction

A MCB bundle interconnect is assumed to be composed of hexagonally packed identical metallic single walled CNTs and multi walled CNTs. Each CNT is surrounded by six immediate neighbors with their centers uniformly separated by a distance 'x'. Figure 3.1 shows the densely and sparsely packed structures with x=d and x=d+Sp respectively where d is the diameter of SWCNT which is replaced by D (diameter of the outer shell of MWCNT) while calculating impedance for MWCNT and Sp is the peripheral spacing in sparsely packed structure and is equal to zero in case of densely packed structure.



(a) (b)

Figure 3.1: (a) densely packed cnt bundle (b) sparsely packed cnt bundle.

To obtain the number of CNTs in a bundle, equations for three different MCB structures containing different number of SWCNTs and MWCNTs aligned differently using the above mentioned notations the following equations are obtained giving the number of rows and

columns in the structure and ultimately the number of CNTs that can be placed in the structure.

Below are shown the general equations to obtain the no. of rows and columns of SWCNT and MWCNT in a bundle:

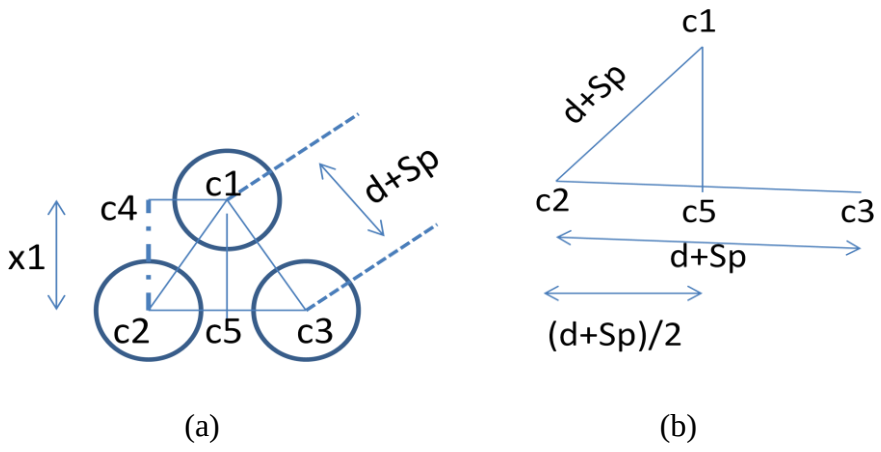
3.1.1 Rows and columns in SWCNT bundle

No. of columns $N_w = \left\lfloor \frac{w-d}{x} \right\rfloor + 1$ (3.1)

No. of rows $N_h = \left\lfloor \frac{H-d}{x1} \right\rfloor + 1$ (3.2)

Where x1 is the vertical distance from centre to centre of CNT as shown in the above figure 3.1

To find x_1



(a) (b)

Figure 3.2: (a) three sparsely placed cnt with centre c1, c2 ,c3 and diameter d with peripheral spacing Sp are shown (b) depicting the values of c2c3 , c1c2, c2c5.

To find $c_1 c_5 = x_1$

$$x_1 = \sqrt{(d+Sp)^2 - \left(\frac{d+Sp}{2}\right)^2}$$

$$= \sqrt{\frac{3}{4}(d+Sp)^2} = \frac{\sqrt{3}}{2}(d+Sp) \quad (3.3)$$

$$N_h = \left\lfloor \frac{H-d}{\frac{\sqrt{3}}{2}(d+Sp)} \right\rfloor + 1 \quad (3.4)$$

3.1.2 Rows and columns in MWCNT bundle

Similarly for MWCNT

$$\text{No. of columns } N_w = \left\lfloor \frac{w-D}{x} \right\rfloor + 1 \quad (3.5)$$

Where x = D for densely packed structure

x = D+Sp for sparsely packed structure

$$\text{No. of rows } N_h = \left\lfloor \frac{H-D}{x1} \right\rfloor + 1 \quad (3.6)$$

$$N_h = \left\lfloor \frac{H-D}{\frac{\sqrt{3}}{2}(D+Sp)} \right\rfloor + 1 \quad (3.7)$$

3.1.3 Number of CNTs in structure 1 of MCB

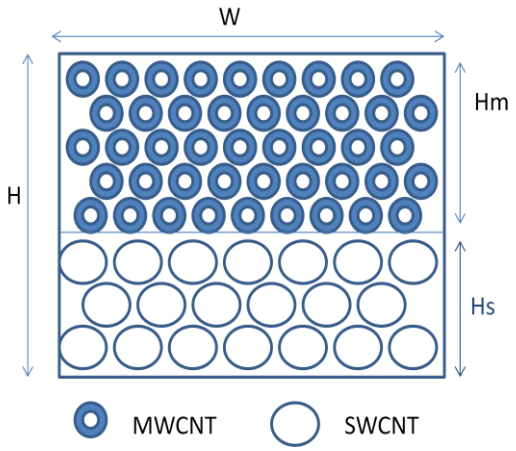


Figure 3.3: Mixed CNT bundle structure 1.

Figure 3.3 shows the first MCB structure and parameters are marked in the figure. Using equations 3.1 to 3.7 following equations for this structure are obtained to show the total no. of SWCNTs and MWCNTs in this structure.

Hs +Hm =H (condition to be satisfied)

(a) Number of SWCNTs in stucture1

No. of columns $N_w = \left\lfloor \frac{w-d}{d+Sp} \right\rfloor + 1$ (3.8)

No. of rows $N_{hs} = \left\lfloor \frac{Hs-d}{\frac{\sqrt{3}}{2}(d+Sp)} \right\rfloor + 1$ (3.9)

No. of SWCNT = Nswcnt $= N_w N_h - \left\lfloor \frac{Nhs}{2} \right\rfloor$

$= \left(\left\lfloor \frac{w-d}{d+Sp} \right\rfloor + 1\right)\left(\left\lfloor \frac{Hs-d}{d+Sp} \right\rfloor + 1\right) - \left\lfloor \frac{1}{2}\left(\left\lfloor \frac{Hs-d}{\frac{\sqrt{3}}{2}(d+Sp)} \right\rfloor + 1\right)\right\rfloor$ (3.10)

(b) Number of MWCNTs in stucture1

No. of columns $N_w = \left\lfloor \frac{w-D}{D+Sp} \right\rfloor + 1$ (3.11)

No. of rows $N_{hm} = \left\lfloor \frac{Hm-D}{\frac{\sqrt{3}}{2}(D+Sp)} \right\rfloor + 1$ (3.12)

No. of MWCNT = Nmwcnt $= N_w N_{hm} - \left\lfloor \frac{Nhm}{2} \right\rfloor$

$= \left(\left\lfloor \frac{w-D}{D+Sp} \right\rfloor + 1\right)\left(\left\lfloor \frac{Hm-D}{\frac{\sqrt{3}}{2}(D+Sp)} \right\rfloor + 1\right) - \left\lfloor \frac{1}{2}\left(\left\lfloor \frac{Hm-D}{\frac{\sqrt{3}}{2}(D+Sp)} \right\rfloor + 1\right)\right\rfloor$ (3.13)

3.1.4 Number of CNTs in structure 2 of MCB

Figure 3.4 shows the second MCB structure and parameters are marked in the figure 3.4. Using equations 3.1 to 3.7 following equations for this structure are obtained to show the total no. of SWCNTs and MWCNTs in this structure.

(a) Number of MWCNTs in stucture2

No. of columns Nwm= $\left\lfloor \frac{Wm-D}{D+Sp} \right\rfloor + 1$ (3.14)

No. of rows Nhm= $\left\lfloor \frac{Hm-D}{D+Sp} \right\rfloor + 1$ (3.15)

No. of MWCNT =Nmwcnt = Nwm Nhm – $\left\lfloor \frac{Nhm}{2} \right\rfloor$

$$= \left(\left\lfloor \frac{Wm-D}{D+Sp} \right\rfloor + 1\right)\left(\left\lfloor \frac{Hm-D}{\frac{\sqrt{3}}{2}(D+Sp)} \right\rfloor + 1\right) - \left\lfloor \frac{1}{2}\left(\left\lfloor \frac{Hm-D}{\frac{\sqrt{3}}{2}(D+Sp)} \right\rfloor + 1\right)\right\rfloor \quad (3.16)$$

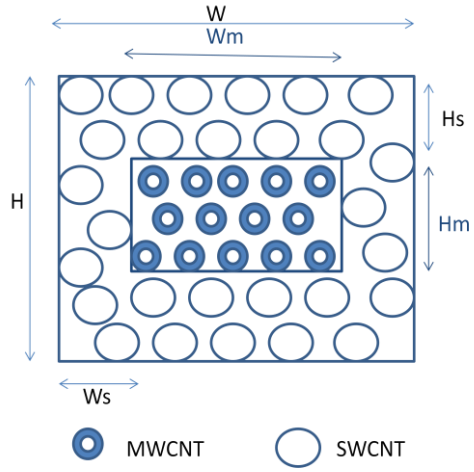


Figure 3.4: Mixed CNT bundle structure 2.

(b) Number of SWCNTs in stucture2

While d≤ Ws and D ≤ Wm

$$Ws = \frac{W-Wm}{2} \quad (3.17)$$

$$Hs = \frac{H-Hm}{2} \quad (3.18)$$

AREA 1 is given by H by Ws has :

$$\text{No. of rows } Nh = \left\lfloor \frac{H-d}{\frac{\sqrt{3}}{2}(d+Sp)} \right\rfloor + 1 \quad (3.19)$$

$$\text{No. of columns } Nws = \left\lfloor \frac{Ws-d}{d+Sp} \right\rfloor + 1 \quad (3.20)$$

No. SWCNTs in area 1 = Nsw_1 =Nws Nh – $\left\lfloor \frac{Nh}{2} \right\rfloor$

$$Nsw_1 = \left(\left\lfloor \frac{Ws-d}{d+Sp} \right\rfloor + 1\right)\left(\left\lfloor \frac{H-d}{\frac{\sqrt{3}}{2}(d+Sp)} \right\rfloor + 1\right) - \left\lfloor \frac{1}{2}\left(\left\lfloor \frac{H-d}{\frac{\sqrt{3}}{2}(d+Sp)} \right\rfloor + 1\right)\right\rfloor \quad (3.21)$$

AREA 2 is given by Hs by Wm has:

$$\text{No. of rows Nhs} = \left\lfloor \frac{Hs-d}{\frac{\sqrt{3}}{2}(d+Sp)} \right\rfloor + 1 \tag{3.22}$$

$$\text{No. of columns Nwm} = \left\lfloor \frac{Wm-d}{d+Sp} \right\rfloor + 1 \tag{3.23}$$

$$\text{No. of SWCNTs in area 2} = Nsw_2 = Nwm\ Nhs - \left\lfloor \frac{Nhs}{2} \right\rfloor$$

$$Nsw_2 = \left(\left\lfloor \frac{Wm-d}{d+Sp} \right\rfloor + 1\right)\left(\left\lfloor \frac{Hs-d}{\frac{\sqrt{3}}{2}(d+Sp)} \right\rfloor + 1\right) - \left\lfloor \frac{1}{2}\left(\left\lfloor \frac{Hs-d}{\frac{\sqrt{3}}{2}(d+Sp)} \right\rfloor + 1\right)\right\rfloor \tag{3.24}$$

Total No. of SWCNTs in the structure 2 are:

$$Nswcnt = 2*Nsw_1 + 2*Nsw_2$$

$$=2*\left(\left(\left\lfloor \frac{Ws-d}{d+Sp} \right\rfloor + 1\right)\left(\left\lfloor \frac{H-d}{\frac{\sqrt{3}}{2}(d+Sp)} \right\rfloor + 1\right) - \left\lfloor \frac{1}{2}\left(\left\lfloor \frac{H-d}{\frac{\sqrt{3}}{2}(d+Sp)} \right\rfloor + 1\right)\right\rfloor\right) +$$

$$2*\left(\left(\left\lfloor \frac{Wm-d}{d+Sp} \right\rfloor + 1\right)\left(\left\lfloor \frac{Hs-d}{\frac{\sqrt{3}}{2}(d+Sp)} \right\rfloor + 1\right) - \left\lfloor \frac{1}{2}\left(\left\lfloor \frac{Hs-d}{\frac{\sqrt{3}}{2}(d+Sp)} \right\rfloor + 1\right)\right\rfloor\right) \tag{3.25}$$

3.1.5 Number of CNTs in structure 3 of MCB

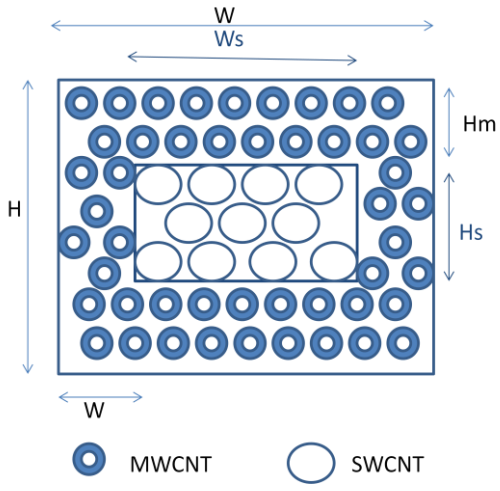


Figure 3.5: Mixed CNT bundle structure 3.

Figure 3.5 shows the third MCB structure and parameters are marked in the figure. Using equations 3.1 to 3.7 following equations for this structure are obtained to show the total no. of SWCNTs and MWCNTs in this structure.

(a) Number of SWCNTs in stucture3

No. of columns Nws= $\left\lfloor \frac{Ws-D}{d+Sp} \right\rfloor + 1$ (3.26)

No. of rows Nhs= $\left\lfloor \frac{Hs-d}{d+Sp} \right\rfloor + 1$ (3.27)

No. of SWCNT =Nswcnt = Nws Nhs – $\left\lfloor \frac{Nhs}{2} \right\rfloor$

$= \left(\left\lfloor \frac{Ws-d}{d+Sp} \right\rfloor + 1\right)\left(\left\lfloor \frac{Hm-d}{\frac{\sqrt{3}}{2}(d+Sp)} \right\rfloor + 1\right) - \left\lfloor \frac{1}{2}\left(\left\lfloor \frac{Hs-d}{\frac{\sqrt{3}}{2}(d+Sp)} \right\rfloor + 1\right) \right\rfloor$ (3.28)

(b) Number of MWCNTs in stucture3

While D≤ Hm and D ≤ Wm

Wm= $\frac{W-Ws}{2}$ (3.29)

Hm= $\frac{H-Hs}{2}$ (3.30)

AREA 1 is given by H by Wm has :

No. of rows Nh= $\left\lfloor \frac{H-D}{\frac{\sqrt{3}}{2}(D+Sp)} \right\rfloor + 1$ (3.31)

No. of columns Nwm= $\left\lfloor \frac{Wm-D}{D+Sp} \right\rfloor + 1$ (3.32)

No. MWCNTs in area 1 = Nmw_1 =Nwm Nh – $\left\lfloor \frac{Nh}{2} \right\rfloor$

$Nmw_1 = \left(\left\lfloor \frac{Wm-D}{D+Sp} \right\rfloor + 1\right)\left(\left\lfloor \frac{H-D}{\frac{\sqrt{3}}{2}(D+Sp)} \right\rfloor + 1\right) - \left\lfloor \frac{1}{2}\left(\left\lfloor \frac{H-D}{\frac{\sqrt{3}}{2}(D+Sp)} \right\rfloor + 1\right) \right\rfloor$ (3.33)

AREA 2 is given by Hm by Ws has:

No. of rows Nhm = $\left\lfloor \frac{Hm-D}{\frac{\sqrt{3}}{2}(D+Sp)} \right\rfloor + 1$ (3.34)

No. of columns Nws= $\left\lfloor \frac{Ws-D}{D+Sp} \right\rfloor + 1$ (3.35)

No. of MWCNTs in area 2 = Nmw_2 = Nws Nhm – $\left\lfloor \frac{Nhm}{2} \right\rfloor$

$Nmw_2 = \left(\left\lfloor \frac{Ws-D}{D+Sp} \right\rfloor + 1\right)\left(\left\lfloor \frac{Hm-D}{\frac{\sqrt{3}}{2}Dd+Sp)} \right\rfloor + 1\right) - \left\lfloor \frac{1}{2}\left(\left\lfloor \frac{Hm-D}{\frac{\sqrt{3}}{2}(D+Sp)} \right\rfloor + 1\right)\right\rfloor$ (3.36)

Total No. of MWCNTs in the structure 3 are:

Nmwcnt =2* Nmw_1 +2* Nmw_2

$$=2*\left(\left(\left\lfloor \frac{Wm-D}{D+Sp} \right\rfloor + 1\right)\left(\left\lfloor \frac{H-D}{\frac{\sqrt{3}}{2}(D+Sp)} \right\rfloor + 1\right) - \left\lfloor \frac{1}{2}\left(\left\lfloor \frac{H-D}{\frac{\sqrt{3}}{2}(D+Sp)} \right\rfloor + 1\right)\right\rfloor\right) +$$

$$2*\left(\left(\left\lfloor \frac{Ws-D}{D+Sp} \right\rfloor + 1\right)\left(\left\lfloor \frac{Hm-D}{\frac{\sqrt{3}}{2}Dd+Sp)} \right\rfloor + 1\right) - \left\lfloor \frac{1}{2}\left(\left\lfloor \frac{Hm-D}{\frac{\sqrt{3}}{2}(D+Sp)} \right\rfloor + 1\right)\right\rfloor\right)$$ (3.37)

3.2 Impedance parameters of Mixed CNT bundle

3.2.1 Temperature dependant resistance:

The temperature dependence of the resistance is obtained through the temperature dependence of the electron scattering mean free paths (MFPs) with acoustic (AC) and optical (OP) phonons [78]. The total resistance of the isolated SWCNT is written as:

$R(V,T) = Rc + \frac{h}{4q^2}\left[\frac{L+\lambda eff(V,T)}{\lambda eff(V,T)}\right]$ (3.38)

$R_{SWCNT} = R(V,T)$

Where Rc is the electrical contact resistance ($\approx 24k$) and λeff is the net effective electron MFP

$\lambda eff = \left({\lambda_{AC}}^{-1} + {\lambda_{OP,ems}}^{-1} + {\lambda_{OP,abs}}^{-1}\right)$ (3.39)

Which include electron scattering both by OP emission and absorption. The AC scattering and OP absorption lengths can be written respectively as:

$$\lambda_{AC} = \lambda_{AC,300}(\frac{300}{T}) \tag{3.40}$$

$$\lambda_{OP,abs}(T) = \lambda_{OP,300}\ \frac{N_{OP}(300)+1}{N_{OP}(T)} \tag{3.41}$$

Where $\lambda_{AC,300} = 1600\,nm$ is the AC scattering length at 300 K, $\lambda_{OP,300} = 15\,nm$ is the spontaneous OP emission length at 300 K. We note that OP emission can occur both after electrons gain sufficient energy from the electric field, and after an OP absorption event:

$$\lambda_{OP,ems} = \left(\frac{1}{\lambda_{OP,ems}^{fld}} + \frac{1}{\lambda_{OP,ems}^{abs}}\right)^{-1} \tag{3.42}$$

$$\lambda_{OP,ems}^{fld}(T) = \frac{\hbar\omega_{OP}}{qV}L + \frac{N_{OP}(300)+1}{N_{OP}(T)+1}\lambda_{OP,300} \tag{3.43}$$

Where the first term estimates the distance electrons must travel in the electric field (F=V/L) to reach the OP emission threshold energy ($\hbar\omega_{OP} \approx 0.18\,eV$) and the second term represents the temperature dependence of the spontaneous OP emission length. The OP emission MFP after an absorption event is obtained by replacing the first term with OP absorption length

$$\lambda_{OP,ems}^{abs}(T) = \frac{N_{OP}(300)+1}{N_{OP}(T)+1}\lambda_{OP,300}\ + \lambda_{OP,abs}(T) \tag{3.44}$$

This approach lets us express the temperature dependence of the relevant MFPs with respect to the acoustic and optical scattering lengths at 300 K. The OP occupation is given by:

$$N_{OP} = \frac{1}{\left[exp\left(\frac{\hbar\omega_{OP}}{k_B T}\right)-1\right]} \tag{3.45}$$

Resistance per shell of the MWCNT is given by[60]:

$$\text{Rshell} = \frac{h}{2e^2 N(i)}\left[1 + \frac{L}{\lambda eff}\right] \tag{3.46}$$

Where $\frac{h}{2e^2}$ =12.9kΩ and L, λeff and N(i) are the length , MFP, and number of conducting channels of the shell respectively[60]. Where

$N(i) = a.\ D_i + b, \qquad D>3\ nm$ (3.47)

where D is the diameter of the shell ,a= 0.0612 nm^{-1} and b= 0.425 and

$D_i = D_{max} - 2d.\ (i - 1), \qquad 1 \leq i \leq p$ (3.48)

Where the number of shells p of the MWCNT is determined by

$$p = 1 + \text{inter}\left[\frac{(Dmax - Dmax/2)}{2d}\right] \quad (3.49)$$

Hence the cumulative resistance R_{MWCNT} of the MWCNT is the parallel combination of all the shell resistance. This will give the resistance of the isolated cnt. The ***CNT-bundle resistance*** is then given as shown below where $R_{isolated}$ is the resistance of an isolated CNT (R_{SWCNT} or R_{MWCNT}) and n_{CNT} is the total number of CNTs forming the bundle as calculated before.

$$R_{BUNDLE} = R_{isolated} / n_{CNT} \quad (3.50)$$

MCB resistance is the parallel combination of both R_{SWCNT} and R_{MWCNT}

3.2.2 Capacitance :

The capacitance of a CNT arises from two sources. The electrostatic capacitance (C_E) is calculated by treating the CNT as a thin wire, with diameter d placed at distance y away from a ground plane and is given as:

$$C_E = \frac{2\pi\varepsilon}{\ln(\frac{y}{d})} \quad (3.51)$$

The quantum capacitance (C_Q) accounts for the quantum electrostatic energy stored in the nanotube when it carries current given by:

$$C_Q = \frac{2e^2}{h v_F} \quad (3.52)$$

Where h is the planck's constant and $v_F = 8 * 10^5 \frac{m}{s}$ is the Fermi velocity. As a CNT has four conducting channels the effective quantum capacitance resulting from four parallel capacitances C_Q is given by $4C_Q$.

Each CNT in the bundle is replaced by a square conductor circumscribing the tube. The total electrostatic capacitance of the bundle is given by the sum of the contribution from each CNT as:

$$C_E^{bundle} = 2C_{En} + \frac{n_w - 2}{2} C_{Ef} + \frac{3(n_H - 2)}{5} C_{En} \quad (3.53)$$

$$C_Q^{bundle} = C_Q^{CNT} . n_{CNT} \quad (3.54)$$

Where $C_{Ef} = \frac{2\pi\varepsilon}{\ln((Sp+w)/d)}$ and (3.55)

$$C_{En} = \frac{2\pi\varepsilon_{ox}}{\ln(Sp/d)} \quad (3.56)$$

The total effective capacitance of bundle of SWCNT per unit length is given by :

$$C_{bundle} = \left(\frac{C_E^{bundle} . C_Q^{bundle}}{C_E^{bundle} + C_Q^{bundle}} \right) \quad (3.57)$$

An MWCNT consists of many concentric shells, which can be viewed as several shells in parallel. The quantum and electrostatic capacitance in case of MWCNT are given by quantum capacitance per unit length of a shell can be derived as:

$$C_{Q/Channel} = 2 * \frac{2e^2}{h v_F} \quad (3.58)$$

$$C_{Q/shell} = C_{Q/Channel} . N(i) \quad (3.59)$$

The electrostatic capacitance is give as: $C_E = \frac{2\pi\varepsilon}{\ln(\frac{y}{Dmax})}$ (3.60)

For MCB both the bundle capacitances of SWCNT and MWCNT are connected in parallel.

3.2.3 Inductance:

For a SWCNT there are 2 types of inductance termed magnetic inductance and kinetic inductance. Magnetic inductance (Lm) is due to the total magnetic energy resulting from the current flowing in the wire. The kinetic inductance (Lk) arises from kinetic energy stored in

each conducting channel of the CNT. The four parallel conducting channels in a CNT results in an effective kinetic inductance of Lk/ 4. The expression for Lm and Lk are:

$$L_M = \frac{\mu}{2\pi} \ln\left(\frac{y}{d}\right) \tag{3.61}$$

$$L_k = \frac{h}{2e^2 v_F} \tag{3.62}$$

$$L_{Bundle(SWCNT)} = \frac{\left(L_M + \frac{L_k}{4}\right)}{n_{CNT}} \tag{3.63}$$

For CNT there are magnetic and kinetic inductance. The magnetic and kinetic inductances per unit length of a shell in MWCNT with configuration are:

$$L_{magnetic} = \frac{\mu}{2\pi} cosh^{-1}\left(\frac{2H}{D}\right) \tag{3.64}$$

$$L_{kinetic/channel} = \frac{h}{2e^2 v_F} * \frac{1}{2} \tag{3.65}$$

$$L_{\frac{kinetic}{channel}/shell} = L_{kinetic/channel} / N(i) \tag{3.66}$$

Meanwhile magnetic inductance ranges from 0.2 to 1.2 pH/μm , which is much smaller than the kinetic inductance so it has been ignored. The total kinetic inductance $L_{kinetic(total)}$ of all the shells in a CNT is obtained by parallel combination of all the shell kinetic inductance. Then the inductance of bundle is obtained by :

$$L_{Bundle(MWCNT)} = L_{kinetic(total)} / n_{CNT} \tag{3.67}$$

For MCB the inductance is obtained by:

$$L_{Bundle(MCB)} = \frac{L_{Bundle(SWCNT)} \cdot L_{Bundle(MWCNT)}}{L_{Bundle(SWCNT)} + L_{Bundle(MWCNT)}} \tag{3.68}$$

3.3 Temperature dependent impedance parameters for Cu

To find out the performance of Cu we need to calculate its impedance parameters with respect to temperature. For this purpose the temperature dependent resistance is given as:

$$R(T) = Ro(1 + \alpha(T - To)) \tag{3.69}$$

α is the temperature coefficient of resistance measured at room temperature 300K and for Cu it is calculated to be $0.0039K^{-1}$. To calculate other parameters for Cu following expressions can be used:

$$L_s = \frac{\mu_0 L}{2\pi}\left[ln\frac{2L}{w+H} + \frac{1}{2} + \frac{0.22(w+H)}{L}\right] \quad (3.70)$$

$$Cg = \varepsilon\left[\frac{w}{y} + 2.22\left(\frac{s}{s+0.7y}\right)^{3.19} + 1.17\left(\frac{s}{s+1.15y}\right)^{0.76}\left(\frac{s}{H+4.53y}\right)^{0.12}\right] \quad (3.71)$$

$$C_C = \varepsilon\left[1.14\frac{H}{s}\left(\frac{y}{y+2.06s}\right)^{0.09} + 0.74\left(\frac{w}{w+1.59s}\right)^{1.14} + 1.16\left(\frac{w}{w+1.87s}\right)^{0.16}\left(\frac{y}{y+0.98s}\right)^{1.18}\right] \quad (3.72)$$

Where Ls is the self inductance, Cg is the capacitance with respect t ground, Cc is the coupling capacitance between adjacent interconnects, R is the resistance, L is length, w is width, H is thickness, ρ is resistivity, y is height above the ground, s is the spacing , ε is the dielectric constant and μ_0 is the permeability.

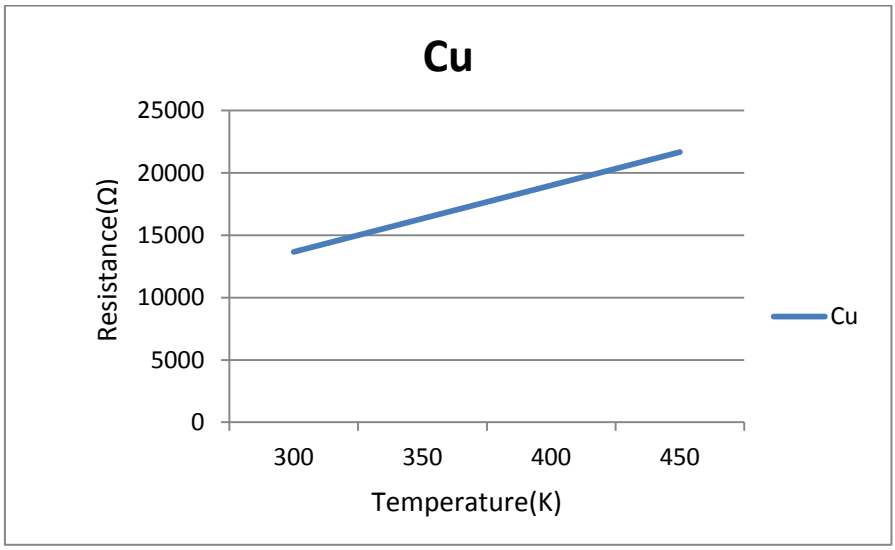


Figure 3.6: Resistance of Cu interconnect as function of temperature.

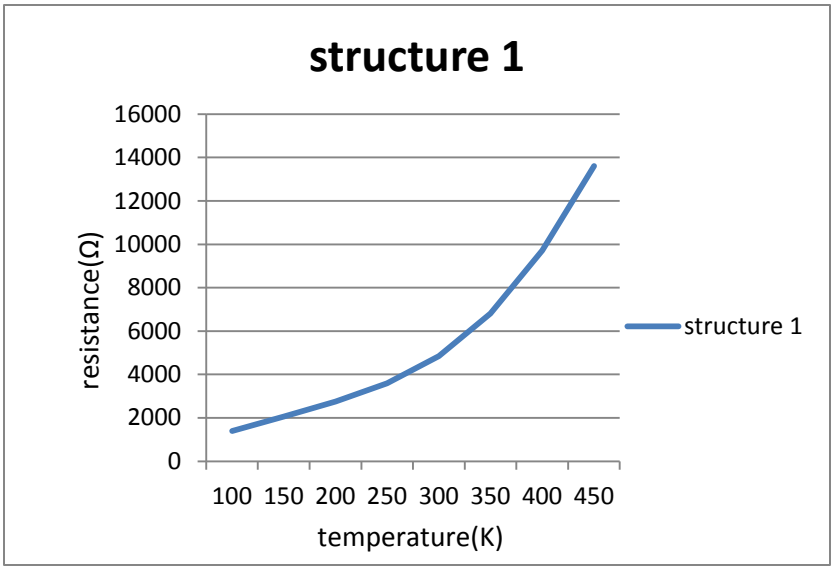
3.4 Temperature dependant impedance analysis of MCB

Impedance parameters for three different structures of MCB are calculated using the equations discussed earlier in this chapter using MATLAB tool. Figure 3.7 (a),(b),(c) shows the resistance of MCB for the three structures and as we compare it with the figure 3.1

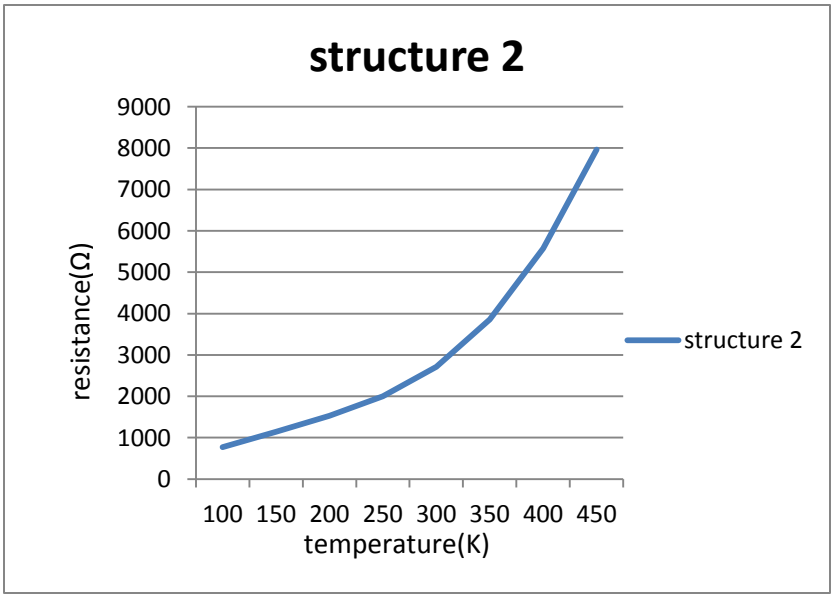
showing the resistance of Cu, we find out that that the resistance imposed by CNT interconnects is much less than that of Cu, the factor which is directly proportional to the delay. Lesser the resistance less should be the delay.

Using the equations discussed in this chapter impedance parameters are calculated for three MCB structures while varying the temperature and also to verify the temperature dependent equations impedance parameters independent of temperature are also calculated.

(a)



(b)



(c)

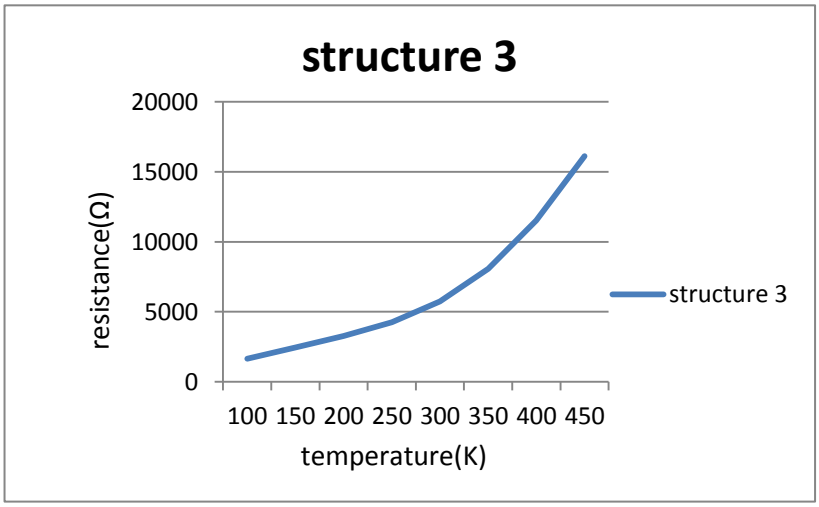


Figure 3.7: Resistance of MCB (a) structure1 (b) structure2 (c) structure3 with respect to temperature at 22nm technology node.

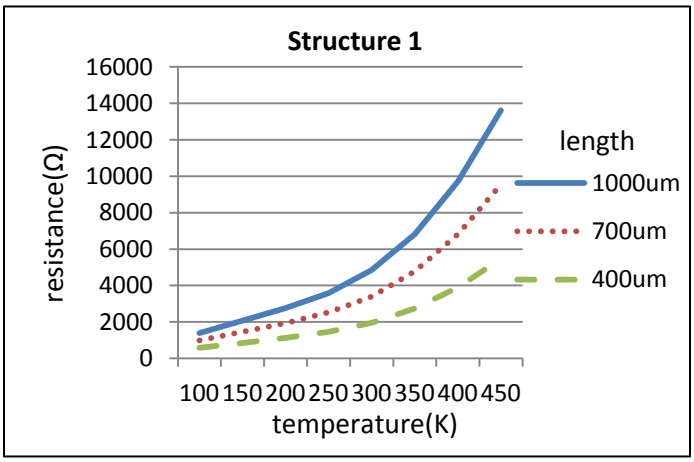
Table 3.1: Impedance parameters for three MCB structures as a function of temperature and without the function of temperature at 300K for interconnect length 1mm for 22nm technology node.

MCB	Resistance= f(T)	Resistance≠f(T)	Inductance	Capacitance
Structure 1	4.8414kΩ	5.1366 kΩ	1.404pH	1.6227pF
Structure 2	2.7165kΩ	3.5003 kΩ	0.77095pH	2.0979pF
Structure 3	5.7456kΩ	6.0292 kΩ	1.6685pH	2.2749pF

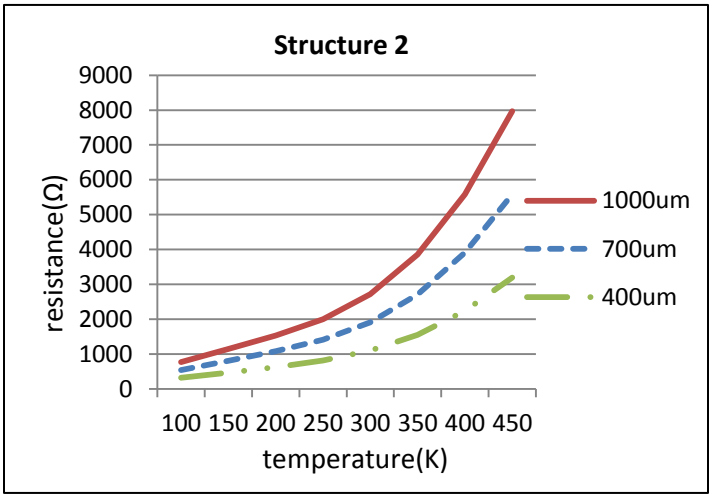
In Table 3.1 are shown the resistance values for three structures at 300K calculated as a function of temperature given by Resistance= f(T) and resistance not as a function of temperature given by Resistance ≠f(T) as shown above.

In Figure 3.8 effect of length on resistance for all the three MCB structures varying with temperature are also shown. This shows that the resistance for MCB increases with temperature as well as length which will eventually increase the delay.

(a)



(b)



(c)

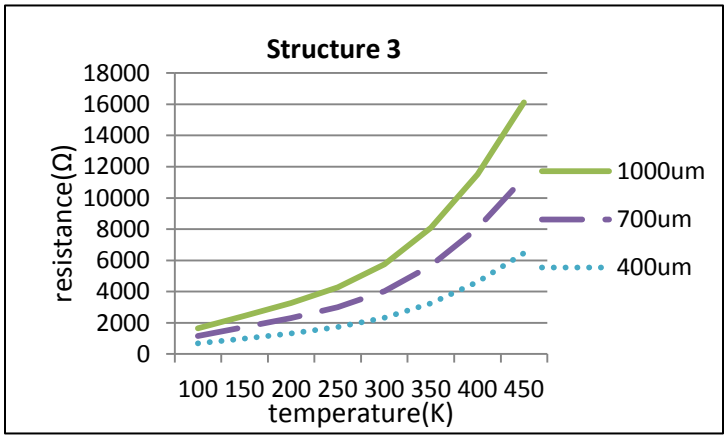


Figure 3.8: Dependence of resistance of MCB (a) structure 1 , (b) structure 2 and (c) structure 3 on temperature and length at 22nm technology node.

Similarly the effect of variation in length is also calculated on capacitance and impedance imposed by the three MCB structures as interconnect at 22nm technology node as shown in Table 3.2. This comparative analysis is clearly shown in Figures 3.9 and 3.10 for capacitance and inductance respectively. It is observed that the capacitance and inductance both increases with length. Depending upon the structure of MCB chosen the impedance parameters vary and is observed that for structure 2 the inductance and resistance both are comparatively lower than the other two structures.

Table 3.2: Capacitance and Inductance for three MCB structures as a function of interconnect length for 22nm technology node.

Length (μm)	**Capacitance (F)**			**Inductance (H)**		
	Structure 1	**Structure 2**	**Structure 3**	**Structure 1**	**Structure 2**	**Structure 3**
100	1.62E-13	2.1E-13	2.27E-13	1.40E-13	0.77E-13	1.67E-13
200	3.25E-13	4.20E-13	4.55E-13	2.81E-13	1.54E-13	3.34E-13
300	4.87E-13	6.29E-13	6.82E-13	4.21E-13	2.31E-13	5.01E-13
400	6.49E-13	8.39E-13	9.10E-13	5.62E-13	3.08E-13	6.67E-13
500	8.11E-13	1.05E-12	1.14E-12	7.02E-13	3.85E-13	8.34E-13
600	9.74E-13	1.26E-12	1.36E-12	8.42E-13	4.63E-13	1.00E-12
700	1.14E-12	1.47E-12	1.59E-12	9.83E-13	5.40E-13	1.17E-12
800	1.30E-12	1.68E-12	1.82E-12	1.12E-12	6.17E-13	1.33E-12
900	1.46E-12	1.89E-12	2.05E-12	1.26E-12	6.94E-13	1.50E-12
1000	1.62E-12	2.10E-12	2.27E-12	1.40E-12	7.71E-13	1.67E-12

Kinetic and magnetic inductance which are the two components of interconnect inductance on the increase of line length increases as the number of inductance elements increase while the value of inductance elements per unit length remain same. Quantum capacitance, electrostatic capacitance are the components of capacitance. The net effective capacitance of the line increases as the line length increases. This is due to increase in number of capacitive elements in the line as its length increases.

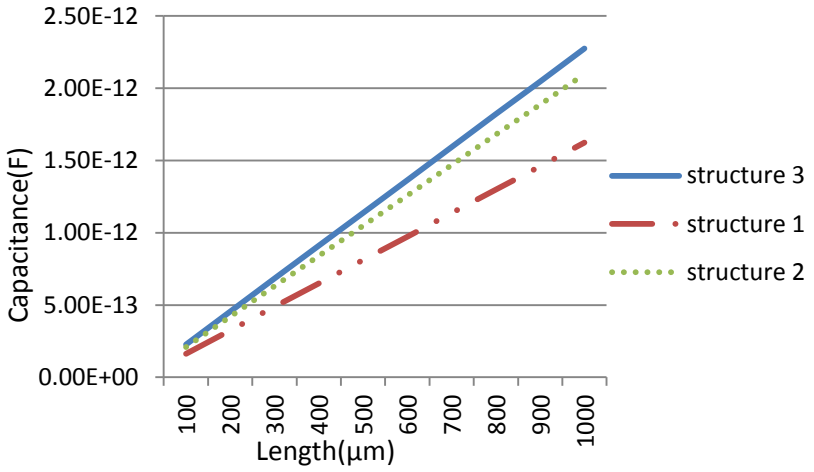


Figure 3.9: Effect of length on capacitance of the three MCB structures at 22nm technology node.

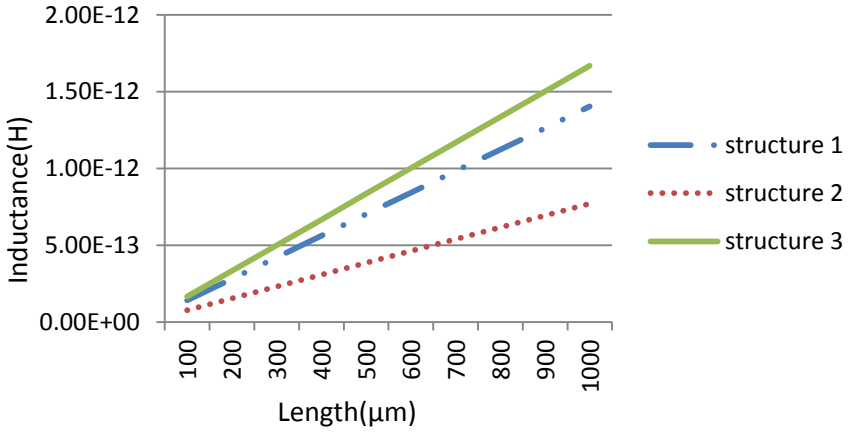


Figure 3.10: Effect of length on inductance of the three MCB structures at 22nm technology node.

3.5 Conclusion

Temperature dependent impedance parameters for three different type of MCB structures are calculated. They are also varied with length for global interconnects. The results show that capacitance and inductance which are temperature independent but length dependent increases with increase in length of interconnect for all the structures an resistance which is both temperature and length dependent parameter increases with increase in both the temperature and length of interconnect. Also at 300K the value of temperature dependent and independent impedance parameters are compared to find out the minimal difference in the two showing good results by temperature dependent equations derived for impedance parameters.

Chapter

4

TEMPERATURE DEPENDENT PERFORMANCE ANALYSIS OF MIXED CNT BUNDLE

4.1 Introduction

It has become necessary to model the interconnects as transmission lines in the deep sub micron technology meaning that more accurate model for RLC transmission line is required for the analysis of interconnects. The RC model is the limiting case of RLC model as inductance is considered to be negligible. Elmore delay model which is also a RC model is inaccurate as the frequency increases and ultimately gives increased inductive impedance hence gives an inaccurate delay model.

Along with the requirement to model interconnects, there is a need to model the CMOS invertor/repeater driving them. The CMOS invertor is the simplest buffer or repeater in VLSI interconnects. Alpha power MOS model for the current voltage characteristics for short channel MOSFET was given by Newton and Sakurai [69]. Kaushik ,*et al.* presented an analytical model for a CMOS invertor driving a RLC load [79]. The alpha-power law MOS model has been used to derive the delay performance of a CMOS invertor which is driving a RLC interconnect load. A π-RLC interconnect model is used for MCB in 22nm technology to calculate the delay mathematically.

To get the delay analysis of interconnects simulation through SPICE to calculate 90% delay. Such techniques give the most accurate insight into arbitrary interconnect structures but are computationally expensive.

4.2 Temperature dependent delay model

A CMOS inverter driving a π-segment RLC circuit is shown in Figure 4.1. Alpha power law MOS model is used to model the inverter. The drain current under different regions of operations of MOSFET is formulated as given by equation 4.1:

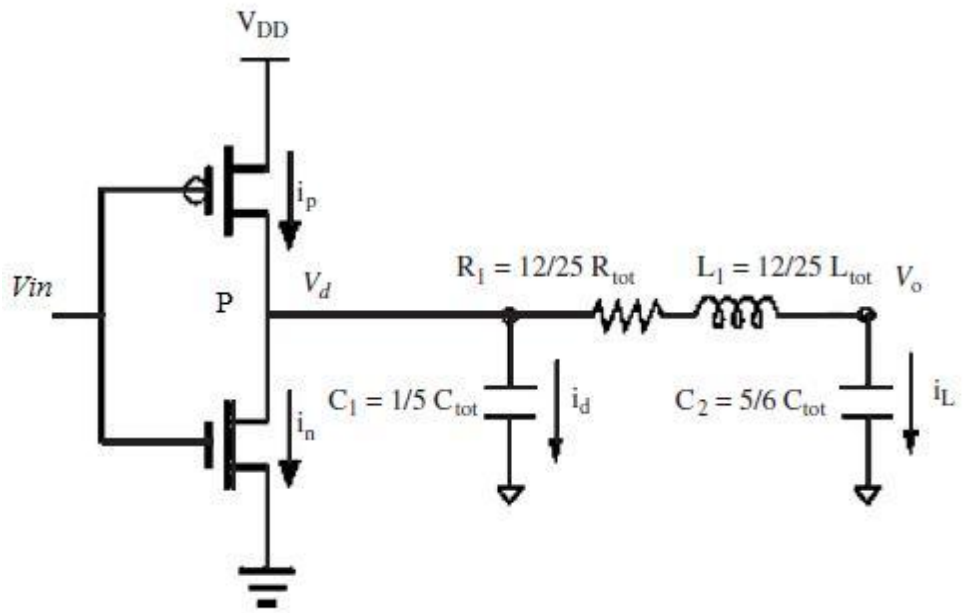


Figure 4.1: A CMOS buffer driving a π model RLC interconnect line [69].

$$I_D = \begin{cases} 0, & V_{GS} \le V_{To}: cut\ off\ region \\ k_l(V_{GS} - V_{To})^{\alpha/2} V_{DS}, & V_{DS} < V_{D-sat}: linear\ region \\ k_s(V_{GS} - V_{To})^{\alpha}, & V_{DS} \ge V_{D-sat}: saturation\ region \end{cases} \quad (4.1)$$

Here α is known as the velocity saturation index, $k_l$and $k_s$are the trans-conductance parameters in the linear and saturation regions of the transistor respectively, V_{D-sat} and V_{To} are the drain-saturation voltage and the zero bias threshold voltage respectively.

The input signal is assumed to be fast ramp [79]. The analytical expression for the output voltage is obtained for four different regions of operation of the transistor for the input signal. Apply KCL at the node P,

$$i_n + i_d + i_L - i_P = 0 \quad (4.2)$$

where i_n, i_P, i_d and i_L are NMOS drain current, PMOS drain current, current through C_1 and C_2 respectively. Now, as the input signal is rising, the NMOS will start discharging the voltage at the output node via the RLC circuit and the output voltage level starts decreasing. Thus the NMOS will go from the cut-off region to the saturation region to the linear region. Hence for fast input ramp accordingly the four regions are suggested for the operation of discharging of the output.

Region 1 ($0<t<t_1$):

In this time interval the NMOSFET is in cut-off region until the input signal level reaches to the value equal to the threshold voltage ($V_{GS} = V_{To}$) of NMOS and it is turned on. Therefore i_n, i_P gets neglected in cutoff region. Thus the equation (4.2) reduces to:

$$i_d + i_L = 0 \quad (4.3)$$

where ,

$$i_d = C_1\frac{dV_d}{dt} \quad \text{and} \quad i_L = C_2\frac{dV_o}{dt} \quad (4.4)$$

where V_d is drain source voltage across nmos and V_o is the output voltage at the far end of the interconnect. By applying KVL the value of $V_d$is obtained as:

$$V_d = LC_2\frac{d^2V_o}{dt^2} + RC_2\frac{dV_o}{dt} + V_o \quad (4.5)$$

Substituting values from equations 4.4 and 4.5 to 4.3 we get a differential equation

$$a\frac{d^3V_o}{dt^3} + b\frac{d^2V_o}{dt^2} + \frac{dV_o}{dt} = 0 \quad (4.6)$$

where the constants a and b are given as:

$$a = C_1C_2L/(C_1 + C_2), \quad b = a = C_1C_2R/(C_1 + C_2), \quad t_1 = \tau V_{To}/V_{DD} \quad (4.7)$$

and the initial conditions are

$$V_o(0) = V_{DD} \text{ and } \frac{dV_o}{dt}(0) = 0 \quad (4.8)$$

Solving equation 4.6 using 4.7 and 4.8 we obtain $V_o = V_{DD}$ till time t_1 while Vin = V_{To}.

Region 2 ($t_1<t<\tau$):

During this time interval, the NMOS operates in the saturation region while input is in state of transition. Applying KVL at node P in saturation condition using equation 4.2 we get:

$$i_n + i_d + i_L = 0 \quad (4.9)$$

now by substituting the values into equation 4.9 from 4.1, 4.6 we obtain the third order differential equation 4.10 which is further solved by second order Taylor series at time $t=\tau/2$ obtaining equation 4.11 as:

$$a\frac{d^3V_o}{dt^3} + b\frac{d^2V_o}{dt^2} + \frac{dV_o}{dt} + \frac{k_s}{(C_1+C_2)}\left(\frac{V_{DD}}{\tau} - V_{To}\right)^{\alpha} = 0 \quad (4.10)$$

$$i_n/(C_1 + C_2) = A_0 + A_1t + A_2t^2 \quad (4.11)$$

putting values in equation 4.11 we get:

$$V_o\ (t) = K_1 t^3 + K_2 t^2 + K_3 t - K_4 e^{-(b-M)t/2a} - K_5 e^{-(b+M)t/2a} + C[3] \quad (4.12)$$

Where we have:

$$\mathrm{M} = \sqrt{\mathrm{b}^2 - 4\mathrm{a}}$$

$$K_1 = -\ \mathrm{A}_2/3$$

$$K_2 = \ \mathrm{A}_2\mathrm{b} - \mathrm{A}_1/2$$

$$K_3 = 2a\ \mathrm{A}_2 - 2\mathrm{b}^2\ \mathrm{A}_2 - \mathrm{A}_0 + b\ \mathrm{A}_1$$

$$K_4 = 2a\mathrm{C}[2]/\ b - M$$

$$K_5 = 2[1]\ /b + M \quad (4.13)$$

C[1], C[2] and C[3] are integration constants.

Region 3 (τ<t<t_2):

During this region, the input has reached V_{DD} and NMOS is still in saturation. The differential equation for the output is:

$$\mathrm{a}\ \frac{d^3V_o}{dt^3} + \mathrm{b}\ \frac{d^2V_o}{dt^2} + \frac{dV_o}{dt} + \mathrm{A}_3\ = 0 \quad (4.14)$$

and A_3 is given as:

$$\frac{k_s}{(\mathrm{C}_1+\mathrm{C}_2)}(V_{DD} - \ V_{To})^{\alpha} \quad (4.15)$$

Using the initial conditions, we get the output equation with respect to time as:

$$V_o\ (t) = -A_3 t - K_6 e^{-(b-M)t/2a} - K_7 e^{-(b+M)t/2a} + C[6] \quad (4.16)$$

With values of constants and variables as:

$$K_6 = 2[5]\ /b - M$$

$$K_7 = 2[4]/\ b + M \quad (4.17)$$

C[4],C[5] and C[6] are integration constants.

Region 4 (t>t_2):

During this region, NMOS operates in the linear region and t_2 is time where drain to source voltage equal to the drain saturation voltage of the NMOS device. The differential equation describing the output is expressed as:

$$a\frac{d^3V_o}{dt^3} + K_8\ \frac{d^2V_o}{dt^2} + K_9\ \frac{dV_o}{dt} + K_{10}V_o\ = 0 \quad (4.18)$$

and variables in the equation are given as:

$$K_8 = \frac{\mathrm{nLC_2}}{(\mathrm{C_1 + C_2})} + b$$

$$K_9 = \frac{\mathrm{nRC_2}}{(\mathrm{C_1 + C_2})} + 1$$

$$K_{10} = \frac{\mathrm{n}}{(\mathrm{C_1 + C_2})}$$

$$\mathrm{n} = k_l(V_{GS} - V_{To})^{\alpha/2} \quad (4.19)$$

Solving the differential equation using the boundary conditions, we get

$$V_o\ (t) =$$

$$C[7]e^{(-1/2\left(\beta^{\frac{2}{3}}-12aK_9+4{K_8}^2+4K_8\beta^{\frac{1}{3}}-36aK_9+12{K_8}^2\right)t/\alpha\beta^{\frac{1}{3}})} +$$

$$C[8]e^{(1/12\left(-\beta^{\frac{2}{3}}+12aK_9+4{K_8}^2+4K_8\beta^{\frac{1}{3}}-36aK_9+12{K_8}^2\right)t/\alpha\beta^{\frac{1}{3}})} +$$

$$C[9]e^{(1/6\left(-\beta^{\frac{2}{3}}+12aK_9+4{K_8}^2+4K_8\beta^{\frac{1}{3}}\right)t/\alpha\beta^{\frac{1}{3}})} \quad (4.20)$$

Where C[7], C[8] and C[10] are integration constants and

$$\beta = 36aK_8K_9 - 108a^2K_{10} - 8{K_8}^3 + 12\sqrt{3}(4a{K_9}^3 - {K_8}^2{K_9}^2 - 18aK_8K_9K_{10} + 27a^2{K_{10}}^2 + 4K83K10)1/2a \quad (4.21)$$

Using equations 4.8, 4.12, 4.16, 4.21 analytical transient response is obtained by calculating the time for different regions of the MOS inverter and putting those values into these equations. The time is calculated as 0 to 0.7 nano seconds for region 1, 0.7 to 3.9 nano seconds for region 2, 3.9 to 5 nanoseconds for region 3 and 5 to 10 nano seconds for region 4. This analytically obtained graph for Mixed CNT bundle structure 2 at temperature 300K is compared with the simulated graph in Tanner EDA tool. The difference shows the error in the analytical modeling.

The rise time of the input ramp signal is 5ns. The total time of output fall is 10ns. The MCB parameters were calculated using the expressions described in the previous chapter. The values of all impedance factors are calculated for a line length of 1000μm and the parameters used for these calculations are shown in table 4.1.

The transient response is shown in Figure 4.2 obtained analytically and the SPICE simulated waveform is also plotted in the same graph. The difference between the analytical

and SPICE waveform results are the errors in the analytical model shown in table 4.2.

Table 4.1: Parameters used for calculation in analytical model and spice simulation [80].

Parameters	**value**
technology	22nm
Vdd	0.7v
Length of interconnect	1mm
Width of interconnect bundle	32nm
Thickness of interconnect bundle	96nm
Oxide thickness	76.9nm
ε	2.05
Aspect ratio of driver	40
Threshold voltage	0.369v
Velocity saturation index	1

Using Alpha law power model the transient response of CMOS inverter driven π-RLC interconnect is extracted. The results show that there is a disagreement between the results extracted using analytically and SPICE simulation during the saturation period.

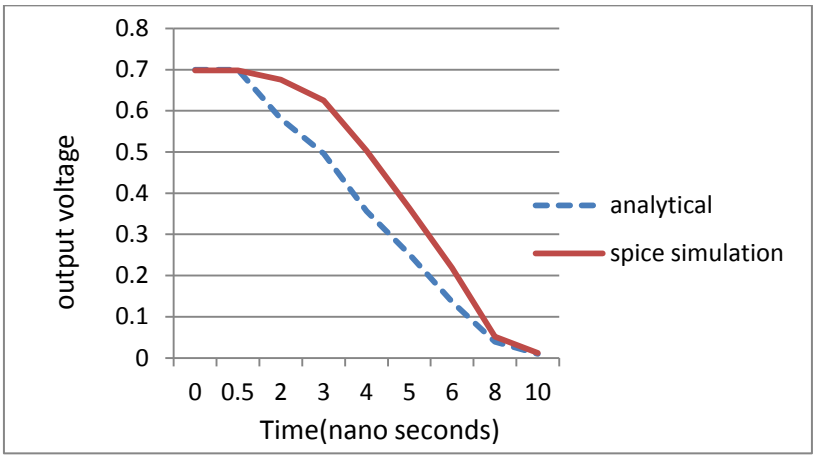


Figure 4.2: Comparison of analytical and spice simulated transient response of MCB structure at 300K at 22nm technology node.

The error is shown in the table 4.2. The discharging time is same for both cases. This

is because alpha-power law is not accurate for technologies less than 90nm [79]. Thus, new improved models are required to predict the response more accurately.

Table 4.2: Difference in output voltage with respect to time for analytically calculated values using alpha law power model and spice simulated response at 22nm technology at 300 K for MCB structure at 1mm length.

Time (ns)	Analytical Vout	Spice simulated Vout	% error
0	0.7	0.698	-0.2
0.5	0.7	0.698	-0.2
2	0.580664	0.67538	14.12
3	0.496206	0.625	20.6
4	0.356359	0.503	29.15
5	0.25130	0.3632	30.8
6	0.1362	0.219	37.8
8	0.038923	0.052	25.14
10	0.00998	0.012	16.8

4.3 Delay analysis

The optimum driver aspect ratios found using the Lumped RLC model for interconnect. The optimum driver aspect ratio for interconnect 1mm long with width 32nm and thickness 96nm and aspect ratio equal to 3 at the global level is calculated and setting it at 40 all the delay and power calculations are done. The schematics for the circuit were drawn using Tanner EDA tool S-Edit 12 (Schematic Capture) version 12.5. Simulations were done using Tanner EDA tool T-Spice 12 (Circuit Simulator) version 12.5. All simulations were done for 22nm technology node. 90% delay is calculated using SPICE simulated results. Values of various parameters were calculated using their expressions given below:

Feature size λ = 11nm =L/2

Width of transistor $W = \lambda(A/R)$

Area of source/drain $AS/AD = 5\lambda W$

Perimeter of source/drain $PS/PD = 10\lambda + 2W$ (4.21)

After the values to all the parameters are given, the input pulse signal of magnitude 0.7

V with time period 24ns, rise time and fall time of 5ns. The average delay is calculated and is equal to the mean of the rise time and fall time calculated by 90% delay method. This is done for all temperature for all the structures and at various length. The aspect ratio which has the minimum delay and average power dissipation is selected as the optimum aspect ratio.

Once the aspect ratio is fixed, the number of optimum repeaters is calculated. For this interconnect RLC distributed model is used. The resistance, inductance and capacitance gets divided in this model. For *n* repeaters, the value of R, L and C gets divided by *n*+1 among the model. The rise time, fall time and average delay is calculated for different number of repeaters from simulation. The number of repeaters which give the minimum average delay is selected as the optimum number of repeaters. It is observed that the delay decreases as the number of repeaters is increased up to a point after which the delay starts increasing and so does power dissipation.

The equivalent circuit of interconnect formed by CNT bundle is used to SPICE-simulate signal propagation down the three structures of MCB interconnect for 22nm technology node at different temperatures and lengths. Simulation is carried out for copper interconnects for same technology and temperatures from 300K to 450 K at 1mm length at the same clock speed. For the sake of comparison the load capacitance is kept same for both the cases. Optimum number of repeaters has been found out to get the optimum performance for both MWCNT and copper.

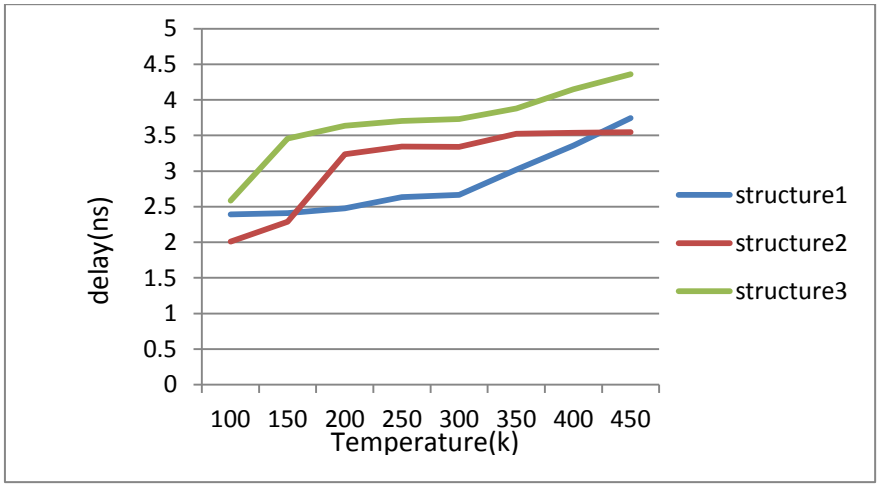
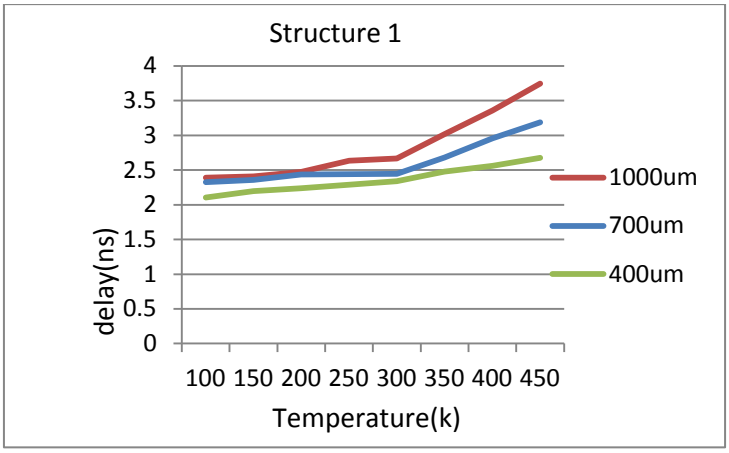


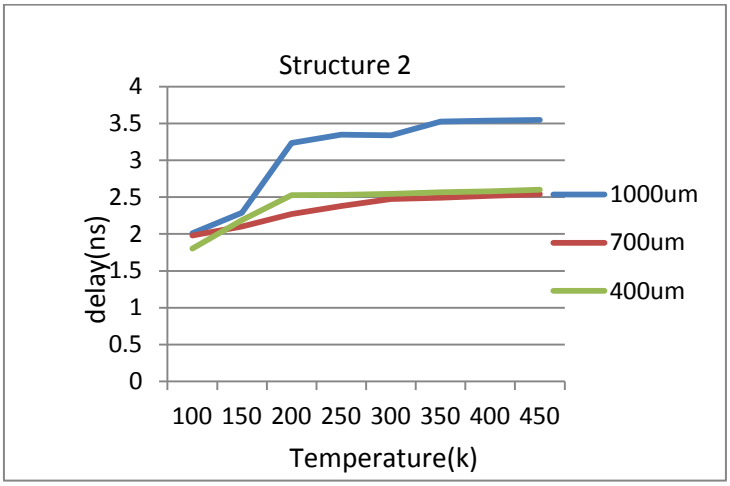
Figure 4.3: Delay analysis of three MCB structures at variable temperature at 1mm length for 22nm technology node.

The comparative delay analysis of the three structures of MCB is shown in figure 4.3 showing that structure 1 and 2 perform better than the structure 3. Also their delay is found

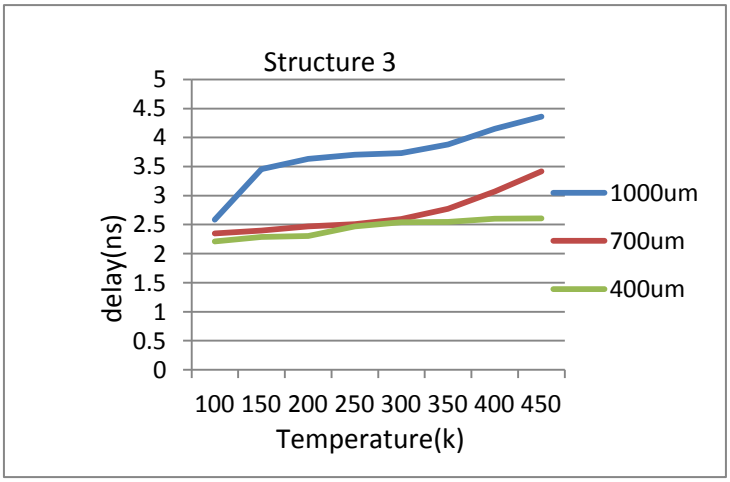
out at various lengths in figure 4.4 (a),(b), (c) for structure 1,2,3 respectively.



(a)



(b)



(c)

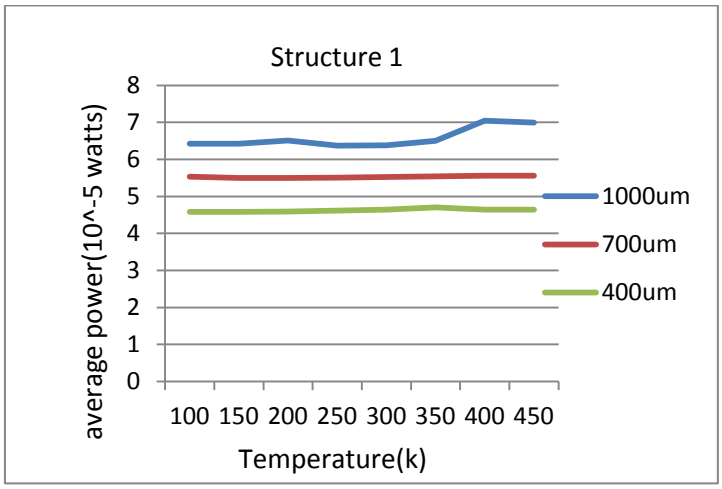
Figure 4.4: Delay of three MCB structures (a) 1 (b)2 (c) 3 at variable temperature and length.

4.4 Power analysis

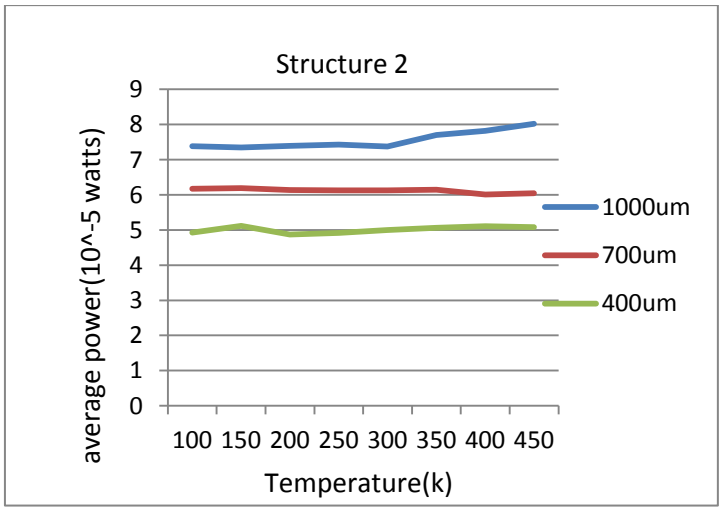
Power dissipation in all the structures of MCB is calculated at various temperatures and length as shown in figure 4.5(a),(b), (c) and is noted that power dissipation increases with increase in length of the interconnect.

SPICE simulations are used to calculate power dissipation MCB interconnect at different temperature and lengths of interconnect. It can be seen that the value increases as the line length increases. It is because in CNT, capacitance increases with length. The transmitter and receiver circuitry is the source of power dissipation in optical interconnect system.

(a) Structure 1:



(b) Structure 2:



(c) Structure 3:

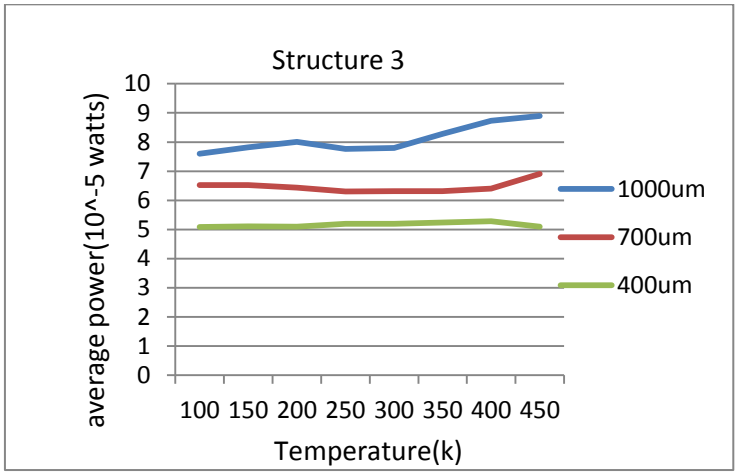


Figure 4.5: Power dissipation at variable temperature and lengths for three MCB structures (a) 1 (b)2 (c) 3 respectively at 22nm technology node.

4.5 Comparison between temperature dependent and independent delay

Delay for all the three structures is calculated at 300K for various lengths. This is done by calculating the impedance parameters for all the structures using temperature dependent and independent equations as discussed in the previous chapter. Using these parameters the delay is calculated for both the cases and it is noted that there is some amount of difference in both given as the error in tables 4.3 (a), (b), (c) as shown below:

Table 4.3 : Comparative delay analysis of temperature dependent and independent MCB (a) structure 1 (b) structure 2 (c) structure 3 at various lengths for 22nm technology node.

(a) Structure 1:

Length	**Temperature dependent delay(sec)**	**Temperature independent delay(sec)**	**% difference**
1000µm	2.665n	2.555n	4.1
700µm	2.445n	2.41n	1.4
400µm	2.34n	2.39n	-2.1
Average	2.48n	2.451n	1.16

(b) Structure 2:

Length	Temperature dependent delay(sec)	Temperature independent delay(sec)	% difference
1000μm	3.34n	3.37n	-0.89
700μm	2.475n	2.41n	2.6
400μm	2.45n	2.47n	-0.81
Average	2.755n	2.75n	0

(c) Structure 3:

Length	Temperature dependent delay(sec)	Temperature independent delay(sec)	% difference
1000μm	3.73n	3.775n	-1.2
700μm	2.595n	2.555n	1.5
400μm	2.54n	2.51n	1.8
Average	2.955n	2.946n	0.03

4.6 Conclusion

Using Alpha law power model the transient response of CMOS inverter driven π-RLC interconnect is extracted for analytical and SPICE simulation analysis. The results show that there is a bit of disagreement between the results extracted using analytical analysis and SPICE simulation i.e. by average of 19.32%. This is due to the fact that alpha-power law is not accurate for technologies less than 90nm [79]. Thus, new improved models are required to predict the response more accurately. Also using Spice simulation delay and power dissipation analysis is done for the three MCB structures which shows that structure 1 can be considered for forming the MCB structure as it shows reduced delay and power dissipation results than structure 2 and 3. Considering 1mm length of interconnect structure 1 shows lesser delay than structure 2 and 3 by 8.55% and 22.88% respectively and lesser power dissipation by 12.92% and 18.90 % respectively.

Chapter

5

TEMPERATURE DEPENDENT COMPARITIVE ANALYSIS

5.1 Introduction

As described in the earlier chapter the impedance parameters for copper, SWCNT and the three structures of MCB interconnects at different global lengths of interconnect with respect to temperature are calculated and their effect on performance of interconnect is analyzed. The equivalent circuit models presented in the previous chapters are used to calculate the equivalent impedance parameters. For calculating the values of resistance, inductance and capacitance, programs have been developed in MATLAB R2013a. All the three structures of MCB and SWCNT are taken as sparsely packed with a distance of 0.34nm as non conducting CNTs are also present in the structure which makes the structure sparsely packed.

For analyzing the effect of change in length on the performance of interconnect, the length of the SWCNT, MCB1 ,MCB2 ,MCB3, Cu interconnects is taken at 400μm, 700μm, 1000μm while diameter d for SWCNT, Cu is kept constant at 1nm for global interconnect and its width and height are also kept constant at their respective minimum values, i.e., 32nm and 96nm respectively for *A/R* equal to 3 and for MCB structures the SWCNT diameter is taken as 1nm and MWCNT in the structure have maximum diameter of 8nm.

Table 5.1: Simulation parameters used for calculation at 22nm [80].

Parameters	CNT	Cu
Vdd	0.7v	0.7v
Width of global interconnect	32nm	32nm
Aspect ratio for global	3	3
Thickness for global	96nm	96nm
K_{ILD}	2.05	2.05

The delay and power dissipation analysis is done by finding out the normalized values of

delay and power dissipation of various CNT bundles with respect to Cu. For the simulation purpose the parameters used are given as in table 5.1. Also the calculated values of impedance for Cu and SWCNT are shown in the tables 5.2 and 5.3 respectively at variable temperature and global length of interconnect.

5.1.1 Cu Impedance Parameters:

Temperature dependent impedance parameters for Cu is calculated using MATLAB 2013a for global interconnect length at 1000μm, 700μm and 400μm at 22nm technology node as shown in table 5.2 below.

Table 5.2: Impedance parameters for Cu calculated at 22nm technology node.

Length → **Temperature ↓**	**1000um**	**700um**	**400um**
300 K	13.671kΩ	9.57kΩ	5.468kΩ
350 K	16.337kΩ	11.4kΩ	6.535kΩ
400 K	19.003kΩ	13.3kΩ	7.601kΩ
450 K	21.669kΩ	15.2kΩ	8.667kΩ
capacitance	14.8fF	10.4fF	5.92fF
inductance	2.03nH	1.37nH	0.738nH

5.1.2 SWCNT Impedance Parameters:

Temperature dependent impedance parameters for SWCNT bundle are calculated using MATLAB 2013a for global interconnect length at 1000μm, 700μm and 400μm at 22nm technology node as shown in table 5.3 below.

Table 5.3: Impedance parameters for SWCNT calculated at 22nm technology node.

Length → **Temperature↓**	**1000um**	**700um**	**400um**
300 K	2.5338kΩ	1.7786kΩ	1.0233kΩ
350 K	3.6019kΩ	2.5262kΩ	1.4506kΩ
400 K	5.2194kΩ	3.6585kΩ	2.0975kΩ
450 K	7.4735kΩ	5.2364kΩ	2.9992kΩ

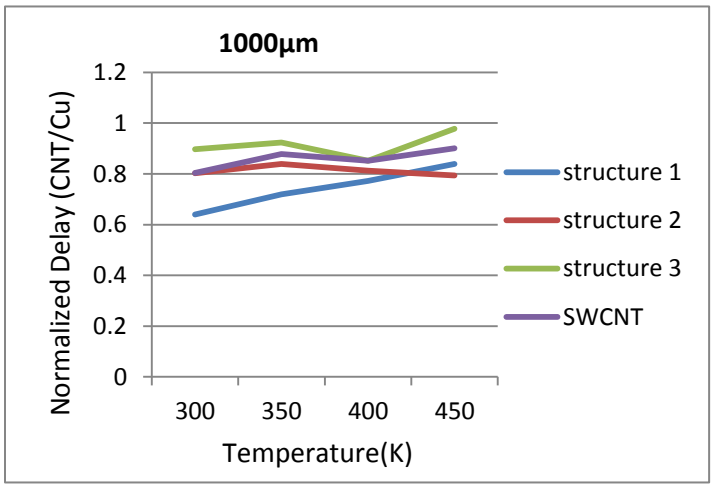
capacitance	2.47pF	1.73pF	0.989pF
inductance	0.107pH	0.187pH	0.268pH

5.2 Temperature dependent delay analysis

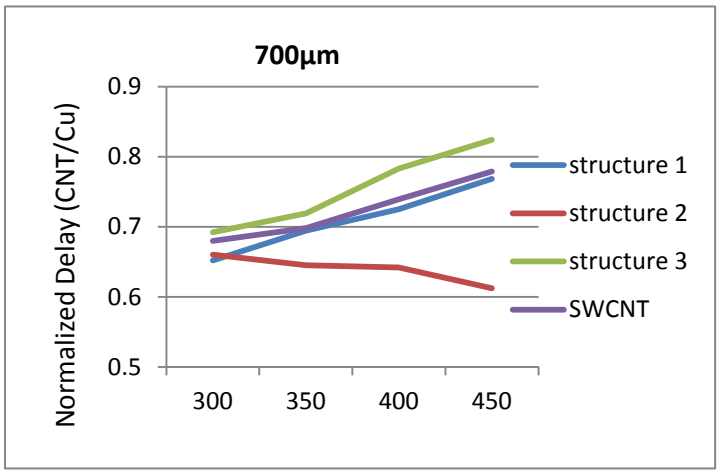
It is observed that the values of resistance, inductance and capacitance increases as the line length increases and also it has been observed that value of resistance , inductance increases with increase in temperature for SWCNT and MCB structures. Similar effects are observed in copper. The impedance parameters affect the delay and power dissipation of interconnect.

The Lumped RLC model for interconnect is used to find the optimum driver aspect ratio *A/R*. The optimum driver aspect ratio for driving interconnect 1000µm long with width 32nm and aspect ratio equal to 3 at the global level is calculated. Rise time, fall time, average delay and power dissipation were calculated. The schematics for the circuit were drawn using Tanner EDA tool S-Edit version 12.5. All simulations were done for 22nm technology. 90% delay is calculated using SPICE simulated results. After the values to all the parameters are given, the input signal is defined. Here the input signal is a square wave of amplitude 0.7V, time period 24ns, rise time and fall time of 5ns. The rises time and fall times are calculated from the simulation graph. The average delay is calculated and is equal to the mean of the rise time and fall time.

(a)



(b)



(c)

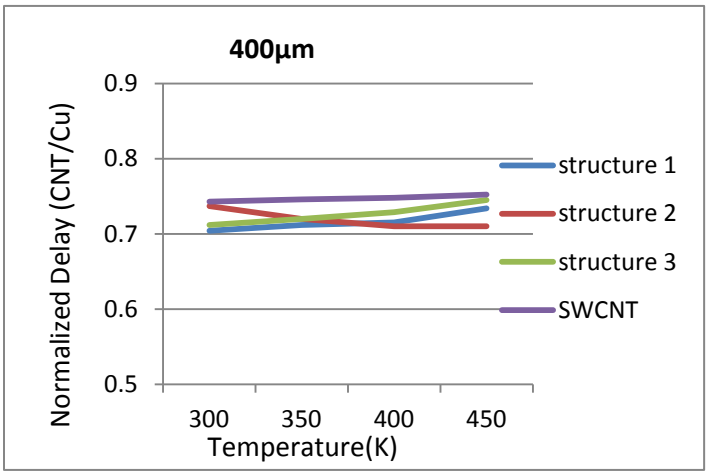


Figure 5.1: Normalized delay of MCB 1 ,MCB 2 , MCB 3, SWCNT with respect to Cu at (a) 1000µm (b) 700µm (c) 400µm length at 22nm technology node.

Once the aspect ratio is fixed, the number of optimum repeaters is calculated. For this interconnect RLC distributed model is used. The resistance, inductance and capacitance gets divided in this model .For *n* repeaters, the value of R, L and C gets divided by *n*+1 among the model. The rise time, fall time and average delay is calculated for different number of repeaters from simulation. The number of repeaters which give the minimum average delay is selected as the optimum number of repeaters. It is observed that the delay decreases as the number of repeaters is increased up to a point after which the delay starts increasing and so does power dissipation.

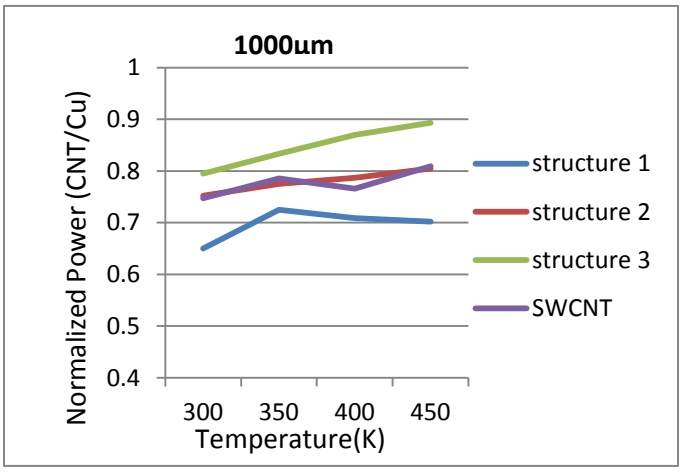
The 90% delay has been extracted for SWCNT, all three structures of MCB and copper

interconnects using SPICE simulation results. Predictive Technology Model (PTM) has been used for CMOS driver [82]. Copper interconnect propagation delay is used to normalize corresponding MWCNT delays. This ratio will be referred to as normalized delay from now on. Results are shown in figure 5.1 for various lengths and temperature depicting that CNT performs better than Cu and delay shown by them is less than Cu.

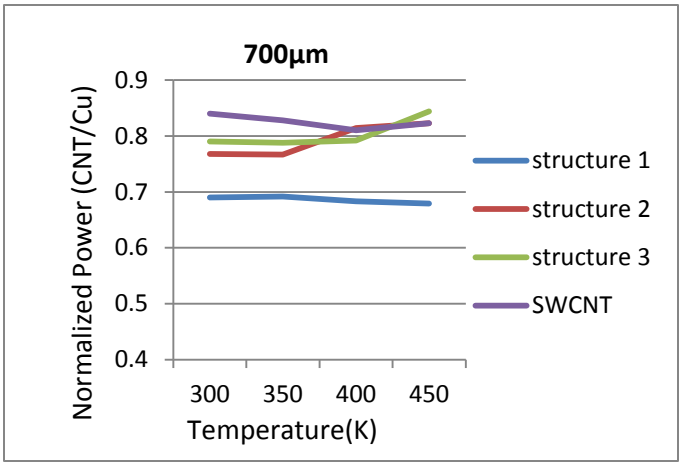
5.3 Temperature dependent power dissipation analysis

The ratio of power dissipation in SWCNT , MCB structures 1,2 and 3 with respect to copper interconnects at different line lengths for temperature dependent parameters has been illustrated in Figure 5.2. It has been seen that the SWCNT and MCBs are of lower power dissipation for all global length interconnect. Result also reveals that the ratio increases with increase in temperature and interconnect length. This is due to the fact that as the temperature and line length increases, the capacitance becomes more dominating in CNT.

(a)



(b)



(c)

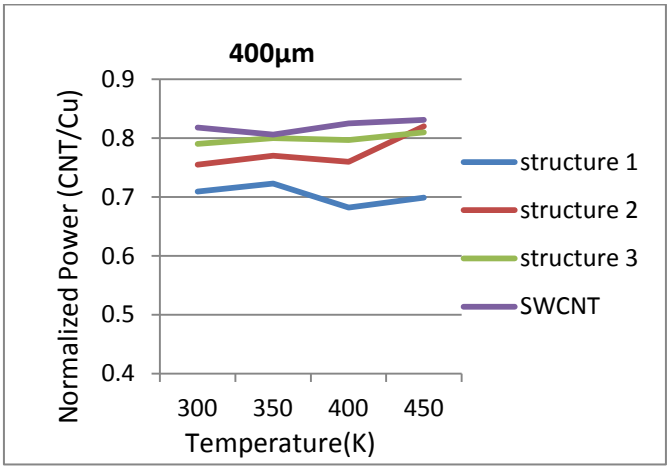


Figure 5.2: Normalized power of MCB 1 ,MCB 2 , MCB 3, SWCNT with respect to Cu at (a) 1000µm (b) 700µm (c) 400µm length at 22nm technology node.

5.4 Conclusion

Temperature dependent performance analysis in terms of propagation delay and power dissipation at 22nm technology node for global lengths indicate that MCB structures and SWCNT are more preferable choice for global interconnects compared to copper. Also the comparison between the three structures of MCB and SWCNT shows that structure 1 with horizontally oriented equal halves of SWCNT and MWCNT in the MCB bundle performs better in terms of overall delay and power dissipation than any other MCB structure and SWCNT bundle. The results also indicate that with increase in temperature the propagation delay of all CNTs and Cu increases.

Chapter

6

CONCLUSION AND FUTURE SCOPE

6.1 Introduction

Analytical and simulation analysis in this thesis report are done for 22nm technology node for global lengths of interconnects. SPICE simulations are carried out using 54 level model files given in appendix A1. Predictive Technology model (PTM) is used to model the CMOS driver. Propagation delay comparisons are done for 90% delay.

6.2 VLSI interconnects

Interconnects act as a transmission line with resistance, inductance and capacitance associated to it and delay caused by them in the circuit is a factor of important concern as technology is scaled down. Earlier the delay models used were RC delay models but study has proved that impact of inductance is also important for delay analysis. So it is important to realize equivalent circuit model for interconnects more accurately. Various lumped and distributed delay models have been developed in the recent time. There are three types of interconnects: local, intermediate and global interconnects and the materials used for them have certain physical properties associated to them which changes with variation in length and other parameters of the interconnects.

6.3 CNT as future VLSI interconnect

With scaling down of technology more number of transistors can fit in a single chip which leads to increase in the interconnect length required on chip which also leads to increase in propagation delay. To reduce it the material used for interconnects is changed from Al to Cu and now CNT which proves to be a promising alternative to Cu at deep sub-micron technology.

The effect of various parameters like length, diameter, temperature, pitch, aspect ratio, pitch etc. are noted for delay and power dissipation analysis and it has been found out that

CNT is a great material as alternative to Cu.

6.4 Influence of impedance parameters on MCB structures

Temperature dependent impedance parameters for three different type of MCB structures are calculated. Temperature dependent and independent impedance parameters are compared showing that temperature dependent equations derived for impedance parameters are at par with the results of temperature independent parameters. Impedance parameters are also varied with length for global interconnects. The results show that capacitance and inductance which are temperature independent but length dependent increases with increase in length of interconnect for all the structures and resistance which is both temperature and length dependent parameter increases with increase in both the temperature and length of interconnect.

6.5 Analytical results

Using Alpha law power model the transient response of CMOS inverter driven π-RLC interconnect is extracted for analytical and SPICE simulation analysis. The results show that there is a difference between the results extracted using analytical analysis and SPICE simulation. On average the error between the two results is 19.32% considering all the three regions whereas the maximum error occurs during the saturation region. Thus, new improved models are required to predict the response more accurately.

6.6 Delay analysis and power dissipation analysis

SPICE simulation is done to find out delay and power dissipation analysis for the three MCB structures which shows that structure 1 with horizontally placed equal halves of SWCNT and MWCNT in the structure can be considered for forming the MCB structure as it shows overall reduced delay and power dissipation results than structure 2 and 3 where structure 2 is such that all the tubes which conduct least are at the middle and structure 3 is such that all the tubes which conduct maximum current are placed at the centre of the bundle as conductivity of SWCNTs is more than that of MWCNTs. Considering 1mm length of interconnect structure 1 shows lesser delay than structure 2 and 3 by 8.55% and 22.88% respectively and lesser power dissipation by 12.92% and 18.90 % respectively.

Temperature dependent performance analysis in terms of propagation delay and power

dissipation at 22nm technology node for global lengths indicate that MCB structures and SWCNT are more preferable choice for global interconnects compared to copper. Also the comparison between the three structures of MCB and SWCNT shows that structure 1 performs better in terms of overall delay and power dissipation than any other MCB structure and also SWCNT bundle. For global length interconnect structure 1 shows lesser delay than SWCNT bundle by 13.50% at 1mm length and lesser power dissipation by 14.35%. The results also indicate that with increase in temperature the propagation delay of all CNTs and Cu increases.

6.7 Future scope

Future work on diameter dependent parameter extraction of MCBs which leads to the calculation of MFP, more accurate positioning of CNTs in the bundle for maximum power transmission for application as long interconnects should be carried out. Performance comparison of MWCNT and MCB interconnects needs to be done.

CNTs are also considered as the future transistor material as a replacement to Silicon. Graphene nano-ribbons (GNRs) are also finding application in FETs. The advantage of GNR over CNT is that it can have more number of fan outs compared to one fan out of CNT. This can make a drastic change in the technologies that are currently used in the semiconductor industry. New tools, methods and techniques are needed to fabricate CNT-FETs in a large scale and use them in the integrated circuits.

REFERENCES

[1] S.D.Pable, Mohd. Hasan, Mohd. Ajmal Kafeel, "Performance Analysis of Ultra Low-power Mixed CNT Interconnects for Scaled Technology*", IEEE International Symposium on Electronic System Design,* pp. 285-289,2011.

[2] M. K. Rai and S. Sarkar, "Carbon Nano Tube as VLSI Interconnect*", Electronic Property of Carbon Nanotube,* chapter 22, pp. 475-494, 2011.

[3] M.S. Dresselhaus, G. Dresselhaus and P. Avouris, "Carbon Nanotubes: Synthesis, Structure, Properties and Applications", *New York: Springer- Verlag*, 2001.

[4] W. Steinhogl, G. Schindler, G. Steinlesberger, M. Tranving, and M. Engelhardt, "Comprehensive study of the resistivity of copper wires with lateral dimensions of 100nm and smaller", *Journal of Applied Physics*, Vol.97, 023706,2005.

[5] Naeemi *et al*.,"Performance comparison between carbon nanotube and copper interconnects for giga scale integration (GSI)", *Electron Device letters*, Vol. 26, No. 2, pp. 84-86, 2005.

[6] C. Schonenberger *et al*., "Interference and interaction in multiwalled carbon nanotubes", *Journal of Applied Physics*, Vol, 69, pp.283-295, 1999.

[7] A. Naeemi and J. D. Meindl, "Monolayer metallic interconnects: promising candidates for short local interconnects", *Electron device letters*, Vol. 26, No. 8, pp. 544-546, 2005.

[8] G. Zhang, *et.al.*, "Ultra-high-yield Growth of Vertical Single-Walled Carbon Nanotubes: Hidden Roles of Hydrogen and Oxygen," *Proc. Nation Academy of Sciences*, Vol.102,No.45, pp.16141-16145,2005.

[9] B.Q.Wei, R. Vajtai and P.M. Ajayan, "Reliability and current carrying capacity of carbon nanotubes", *Applied Physics Letters*,Vol.79, No.8, pp.1172-1174,2001.

[10] C. Dong, S. Haruehanroengra and W. Wang, "Exploring Carbon Nanotubes and NiSi Nanowires as On -Chip Interconnections", *Proceedings of ISCAS*, pp. 3510-3513,2000.

[11] A. Gayasen, N. Vijaykrishnan and M.J. Irwin, "Exploring technology alternatives for nano- scale FPGA interconnects," *Proc. of DAC'05*, pp. 921-926, 2005.

[12] Y.Wu, J. Xiang, C.Yang, W. Lu, "Single crystal metallic nanowires and metal/semiconductor nanowire heterostructures", *Nature*, Vol. 430, pp. 61-65,2004.

[13] T. Morimoto, "Self-aligned nickel-mono-silicide technology for high-speed deep submicrometer logic CMOS ULSI", *IEEE Trans. Electron Devices*, Vol.42, pp. 915–922, 1995.

[14] Y. Cui, L.J. Lauhon, M.S. Gudiksen, J. Wang and C.M. Lieber, "Diameter-controlled synthesis of single-crystal silicon nanowires", *Applied Physics Letter*,Vol.78, pp. 2214–2216,2001.

[15] Y.Wu,"Controlled growth and structures of molecular-scale silicon nanowires*", Nano Letter* ,Vol.4, pp. 433– 436,2004.

[16] K. Toman, "The structure of NiSi", *Acta Crystallogr*,Vol.4, pp. 462–464,1951.

[17] B. Meyer et al., "Intrinsic properties of NiSi", *J. Alloys Compounds* 262/263, pp.235–237, 1997.

[18] P.U. Sathyakam and P.S. Mallick, "Transient Analysis of Mixed Carbon Nanotube Bundle Interconnects", *Electronics Letters.* Vol. 47, No. 20, pp. 1134-1136, 2011.

[19] W. Wu and K. Maex, "Studies on size effects of copper interconnect lines," *Proc. Solid-State and Integrated-Circuit Technology, Shanghai, China*, Vol. 1, pp. 416–418 Oct, 2001.

[20] S. Belluci, "Carbon nanotubes: Physics and applications", *Physica Status Solidi C*, No. 2, pp. 34 – 47.

[21] S.B. Sinnott, R. Andrews, "Carbon Nanotubes: Synthesis, Properties, and Applications", *Critical Reviews in Solid State and Materials Sciences*, No. 26(3), pp. 145–249.

[22] K. Banerjee and N. Srivastava, "Are carbon nanotubes the future of VLSI interconnections?", *43rd ACM IEEE DAC Conference Proceedings, San Francisco, CA*, pp. 809-814, 2006.

[23] Th.Hunger, *et al.,* "Transport in Ropes of Carbon Nanotubes: Contact Barriers and Luttinger Liquid Theory", *PRB*,Vol.69, 195406,2004.

[24] W. Liang *et al.*, "Fabri-parrot interference in a nano electron waveguide", *Nature*,Vol. 411, pp. 665-669, 2001.

[25] M.L.Paul ,M. S. Fuhrer, and H. Park, "Single-walled carbon nanotube electronics", *IEEE Trans. Nanotechnol.*, Vol. 1, No. 1, pp. 78–85,2008.

[26] Z.Yao, C. L. Kane, and C. Dekker, "High- field electrical transport in single-wall carbon nanotubes", *Phys. Rev. Lett.,* Vol. 84, pp. 941–944,2000.

[27] P. Avouris ,"Carbon nanotube electronics", *Chemical Physics*, No. 281, pp. 429-445,2002.

[28] A.Naeemi ,J. D. Meindl, "Monolayer Metallic Nanotube Interconnects: Promising Candidates for Short Local Interconnects", *IEEE Elect. Dev. Lett.,* Vol. 26, No. 8, pp. 544-546,2005.

[29] A. Naeemi, James D. Meindl, "Compact Physical Models for Multiwall Carbon-Nanotube Interconnects", *IEEE Electron Device Letters*, Vol. 27, No. 5, pp. 338-340,2006.

[30] A. Naeem , James D. Meindl, "Design and Performance Modeling for Single-Walled Carbon Nanotubes as Local, Semiglobal, and Global Interconnects in Gigascale Integrated Systems", *IEEE Trans. On Electron Devices*, Vol. 54, No. 1, pp. 26-37,2007.

[31] A. Naeemi, James D. Meindl, "Performance Modeling for Single- and Multiwall Carbon Nanotubes as Signal and Power Interconnects in Gigascale Systems*", IEEE TRANS. ON ELECT. DEV.*, Vol. 55, No. 10, pp. 2574-2582,2005.

[32] H. Li, W.Y. Yin, K. Banerjee, and J. F. Mao, "Circuit Modelling and Performance Analysis of Multi-Walled Carbon Nanotube Interconnects", *IEEE Transactions on Electron Devices.* Vol. 55, no. 6, pp. 1328-1337, 2008.

[35] P. U. Sathyakam and P. S. Mallick, “Towards realization of mixed Carbon nanotube bundles as VLSI interconnects: A review”, Nano Communication Networks, Vol. 3, No. 3, pp. 175 – 182, 2012.

[36] S. Im, *et al*., “Scaling Analysis of Multilevel Interconnect Temperatures for High Performance ICs”, *IEEE TED*, Vol. 52, No. 12, pp. 2710-2719, 2005.

[37] N. Srivastava and K. Banerjee, “A comparative scaling analysis of metallic and carbon nanotubes interconnections for nanometer scale VLSI technologies”, *Proc. VMIC,* pp. 393-398, 2004.

[38] L.Shang, and M. Liu, “Analyzing Mixed Carbon Nanotube Bundles: A current Density Study”, *IEEE Internation Symposium on Circuits and Systems*. pp. 173-176, 2008.

[39] J. Hone, *et al*., “Electrical and thermal transport properties of magnetically aligned Single Wall Carbon Nanotube Films,” *App. Phy. Lett.,*Vol. 77, No. 5, pp. 666-668, 2000.

[40] T. Sakurai, "Closed form expression for interconnection delay, coupling and crosstalk in VLSI's", IEEE Trans. Electron Devices, Vol. 40, pp.118 – 124, 1993.

[41] N. Alam, A. K. Kureshi, M. Hasan and T. Arslan, “Analysis of Carbon Nanotube Interconnects and their Comparison with Cu Interconnects”, *IEEE Conference on Multimedia, Signal Processing and Communication Technologies*. Vol. 9, pp. 124-127, 2009.

[42] H. B. Bakoglu, “Circuits, interconnections and Packaging for VLSI”, *AddisonWesley, Reading , MA,* 1990.

[43] Bakoglu, H.B. and Meindl, J.D., “Optimal interconnection circuits for VLSI”, *IEEE Transactions on Electron Devices*, Vol. 32 No. 5, pp. 903-9, 1985.

[44] P.J. Burke, “Lütitinger Liquid Theory as a Model of the Gigahertz Electrical Properties of Carbon Nanotubes”, *IEEE Transactions on Nanotechnology*. Vol. 1, No. 3, pp. 129-144, 2002.

[45] A. Naeemi and James D. Meindl, “Physical Modeling of Temperature Coefficient of Resistance for Single and Multi-Wall Carbon Nanotube Interconnects*”, IEEE Electron Device Letters*, Vol. 28, No. 2, February 2007.

[46] N. Srivastava, and K. Banerjee, “Performance Analysis of Carbon Nanotube Interconnects for VLSI Applications”, *IEEE/ACM International Conference on ICCAD*. Vol. 5, pp. 383-390, 2005.

[47] P.L. McEuen, and J.Y.Park, "Electron Transport in Single-Walled Carbon Nanotubes," *MRS Bulletin*, Vol. 29, No. 4, pp. 272-275,2004.

[48] A. Nieuwoudt and Y. Massoud, "RC Circuit Model for Multi-Walled Carbon Nanotubes", *Proceedings of the 7th IEEE International Conference on Nanotechnology, Hong Kong*, 2007.

[49] Y. Massoud and A. Nieuwoudt, "Performance analysis of Optimised Carbon nanotube interconnect", *IEEE Symp. On Circuits and Syst.*, pp. 792-795, 2009.

[50] M. K. Majumder, B. K. Kaushik and S. K. Manhas, "A Comparative Analysis of Single Walled CNT Bundle and Multi Walled CNT as Future Global VLSI Interconnects", *Proceedings published by International Journal of Computer Applications (IJCA) International Conference on Networks and Computer Communications (ETNCC)* ,2011.

[51] A. Naeemi *et al.*, "Performance comparison between carbon nanotube and copper interconnects for giga scale integration (GSI)", *Electron Device letters*, Vol. 26, No. 2, pp. 84-86, 2005.

[52] A. Naeemi and J. D. Meindl, "Monolayer metallic interconnects: promising candidates for short local interconnects*", Electron device letters*, Vol. 26, No. 8, pp. 544-546, 2005.

[53] H. Li, W.Y. Yin, K. Banerjee and J.F. Mao, "Circuit Modeling and Performance Analysis of Multi-Walled Carbon Nanotube Interconnects", *IEEE Transactions on Electron Devs*, Vol. 55, No. 6, 2008.

[54] H. Li, N. Srivastava, J. Mao, W. Yin and K. Banerjee, "Carbon Nanotube Vias: A Reality Check*", IEEE Transactions on Electron Devices*, Vol. 65 No. 6, pp. 207-10, 2007.

[55] N. Srivastava, R.V. Joshi and K. Banerjee, "Carbon Nanotube Interconnects: Implications for Performance, Power Dissipation and Thermal Management", *IEDM*, pp. 257-260, 2005.

[56] Kyung-Hoae Koo, Hoyeol Cho, Pawan Kapur and Krishna C. Saraswat, "Performance Comparisons between Carbon Nanotubes, Optical, and Cu for Future High-Performance On-Chip Interconnect Applications*", IEEE Transaction on Electron Devices*, Vol. 54, No. 12, December 2007.

[58] M. D'Amore, M. S. Sarto, A. Tamburrano, "Fast Transient Analysis of Next-Generation Interconnects Based on Carbon Nanotubes*", IEEE Trans. On Electromagnetic Compatibility*, Vol. 52, No. 2, pp. 496-503,2010.

[59] V.V. Deodhar and J. V. Davis, "Voltage scaling and repeater insertion for high-throughput low power interconnects", *ISCAS'05*,Vol. 5, pp. 349-352,2005.

[60] Y. S. Duksh, B. K. Kaushik, S. Sarkar and R. Singh, "Effect of Driver Size and Number of Shells on Propagation Delay in MWCNT Interconnects", *ICDeCom, International Conference on 24-25*, 2011.

[61] M. S. Sarto and A. Tamburrano, "Single-Conductor Transmission Line Model of Multiwall Carbon Nanotubes", *IEEE Transactions on Electromagnetic compatibility*, Vol. 52, No. 2, 2010.

[62] W. Wang, S. Haruehanroengra, L. Shang, M. Liu, "Inductance of mixed carbon nanotube bundles", *IET Micro & Nano Letters*, Vol. 2, Issue. 2, pp. 35-39, 2007.

[63] M. K. Rai and S. Sarkar, "Influence of tube diameter on carbon nanotube interconnect delay and power output", *Phys. Status Solidi A*, pp. 1–5,2011.

[64] M. K. Rai, Nivedita and S. Sarkar, "Carbon Nanotube Based Interconnects for VLSI Application", *IE (I) Journal-ET*, Vol. 91, pp. 3-6, 2011.

[65] Y.I. Ismail, E.G. Friedman, "Effects of inductance on the propagation delay and repeater insertion in VLSI circuits", *IEEE Trans. VLSI Syst.* ,Vol. 8, pp. 195–206, 2000.

[66] V.Adler and E.G. Friedman, "Repeater design to reduce delay and power in resistive interconnects*", IEEE Transactions on Circuits and Systems-II: Analog and Digital Signal Processing*, Vol. 45 No. 5, pp. 607-16, 1998.

[67] W. C. Elmore, "The transient response of damped linear networks with particular regard to wide-band amplifiers", *Journal of Applied Physics*, Vol. 19, pp. 55–63, Jan. 1948.

[68] A.B. Kahng, S. Muddu, "Efficient gate delay modeling for large interconnect loads", *IEEE Multi-Chip Module Conf.*, pp. 202–207, 1996.

[69] T. Sakurai and A.R. Newton, "Alpha power law MOSFET model and its applications to CMOS inverter delay and other formulas", *IEEE Journal of Solid State Circuits*, Vol. 25, No. 2, pp. 584-94, 1990.

[70] A. B. Kahng, S. Muddu, and E. Sarto, "On switch-factor based analysis of coupled RC interconnects", *Proc. DAC*, pp. 79 - 84, 2000.

[71] Y. I. Ismail and E. G. Friedman, "Sensitivity of Interconnect Delay to On-Chip Inductance", *ISCAS*, pp. 403-409, 2000.

[72] D. Das and H. Rahaman, " Unified model for analyzing timing delay and crosstalk effects in carbon nanotube interconnects", *IEEE 4th Asia symposium on Quality Electronic Design*, pp. 100-109, 2012.

[73] P. Sun and R. Luo, "Analytical modelling for crosstalk noise induced by process variations among CNT-based interconnects", *IEEE*, 2009.

[74] L. Jia and W. Yin, "Temperature effects on crosstalk in carbon nanotube interconnects", *IEEE*, 2008.

[75] W. C. Chen, W. Yin, L. Jia and Q. H. Liu, "Electro-thermal characterisation of single walled carbon nanotube (SWCNT) interconnect arrays", *IEEE trans. On nanotech.* , Vol. 8, No. 6, pp. 718-728, 2009.

[76] E. Pop, D. Mann, J. Reifenberg, K. Goodson And H. Dai, "Electro-Thermal Transport in Mettalic Single-Wall Carbon Nanotubes for Interconnect Applications", *Journal of Applied Physics*. Vol. 101, pp. 256-259, 2007.

[77] M.K. Rai and S. Sarkar, "Temperature dependant crosstalk analysis in coupled single-walled carbon naotube (SWCNT) bundle interconnects", *Internationak Jouranl of Circuit theory and Applications.*

[78] N.D. Pandaya, M.K. Majumdar, B.K. Kaushik and S.K. Manhas, "Performance Comparison of Mixed CNT Bundle in Global VLSI Interconnect", *International Conference on Communication Systems and Network Technologies.* pp. 790-793, 2012.

[79] B.K. Kaushik, S. Sarkar, R.P. Agarwal, "Waveform analysis and delay prediction for a CMOS gate driving RLC interconnect load", *Integration, the VLSI journal* ,Vol.40, pp. 394–405, 2007.

[80] Predictive Technology Model[Online].www.eas.asu.edu/ ptm/.

APPENDIX

.model nmos nmos level = 54

+version = 4.0 binunit = 1 paramchk= 1 mobmod = 0

+capmod = 2 igcmod = 1 igbmod = 1 geomod = 1

+diomod = 1 rdsmod = 0 rbodymod= 1 rgatemod= 1

+permod = 1 acnqsmod= 0 trnqsmod= 0

+tnom = 27 toxe = 6.5e-010 toxp = 4e-010 toxm = 6.5e-010

+dtox = 2.5e-010 epsrox = 3.9 wint = 5e-009 lint = 1.35e-009

+ll = 0 wl = 0 lln = 1 wln = 1

+lw = 0 ww = 0 lwn = 1 wwn = 1

+lwl = 0 wwl = 0 xpart = 0 toxref = 6.5e-010 xl = -9e-9

+dlcig = 1.35e-009

+vth0 = 0.3692 k1 = 0.2 k2 = 0 k3 = 0

+k3b = 0 w0 = 2.5e-006 dvt0 = 1 dvt1 = 2

+dvt2 = 0 dvt0w = 0 dvt1w = 0 dvt2w = 0

+dsub = 0.078 minv = 0.05 voffl = 0 dvtp0 = 1e-011

+dvtp1 = 0.1 lpe0 = 0 lpeb = 0 xj = 7.2e-009

+ngate = 1e+023 ndep = 1.2e+019 nsd = 2e+020 phin = 0

+cdsc = 0 cdscb = 0 cdscd = 0 cit = 0

+voff = -0.13 nfactor = 2.3 eta0 = 0.0045 etab = 0

+vfb = -1.058 u0 = 0.0181 ua = -5e-010 ub = 1.7e-018

+uc = 0 vsat = 200000 a0 = 1 ags = 0

+a1 = 0 a2 = 1 b0 = 0 b1 = 0

+keta = 0.04 dwg = 0 dwb = 0 pclm = 0.06

+pdiblc1 = 0.001 pdiblc2 = 0.001 pdiblcb = -0.005 drout = 0.5

+pvag = 1e-020 delta = 0.01 pscbe1 = 2.0e+009 pscbe2 = 1e-007

+fprout = 0.2 pdits = 0.01 pditsd = 0.23 pditsl = 2300000

+rsh = 5 rdsw = 60 rsw = 30 rdw = 30

+rdswmin = 0 rdwmin = 0 rswmin = 0 prwg = 0

+prwb = 0 wr = 1 alpha0 = 0.074 alpha1 = 0.005

+beta0 = 30 agidl = 0.0002 bgidl = 2.1e+009 cgidl = 0.0002

+egidl = 0.8 aigbacc = 0.012 bigbacc = 0.0028 cigbacc = 0.002

+nigbacc = 1 aigbinv = 0.014 bigbinv = 0.004 cigbinv = 0.004

+eigbinv = 1.1 nigbinv = 3 aigc = 0.0213 bigc = 0.0025889

+cigc = 0.002 aigsd = 0.0213 bigsd = 0.0025889 cigsd = 0.002

+nigc = 1 poxedge = 1 pigcd = 1 ntox = 1

+xrcrg1 = 12 xrcrg2 = 5

+cgso = 7e-011 cgdo = 7e-011 cgbo = 0 cgdl = 7.5e-013

+cgsl = 7.5e-013 clc = 1e-007 cle = 0.6 cf = 1.1e-010

+ckappas = 0.6 ckappad = 0.6 vfbcv = -1 acde = 1

+moin = 15 noff = 1 voffcv = 0

+kt1 = -0.154 kt1l = 0 kt2 = 0.022 ute = -1.1

+ua1 = 1e-009 ub1 = -1e-018 uc1 = -5.6e-011 prt = 0

+at = 33000

+fnoimod = 1 tnoimod = 0 noia = 6.25e+041 noib = 3.125e+026

+noic = 8.75e+009 em = 41000000 af = 1 ef = 1

+kf = 0 tnoia = 1.5 tnoib = 3.5 ntnoi = 1

+jss = 1.2e-006 jsws = 2.4e-013 jswgs = 2.4e-013 njs = 1

+ijthsfwd= 0.1 ijthsrev= 0.1 bvs = 10 xjbvs = 1

+jsd = 1.2e-006 jswd = 2.4e-013 jswgd = 2.4e-013 xjbvd = 1

+pbs = 1 cjs = 0.0018 mjs = 0.5 pbsws = 1

+cjsws = 1.2e-010 mjsws = 0.33 cjswgs = 2.1e-010 cjd = 0.0018

+cjswd = 1.2e-010 mjswd = 0.33 pbswgd = 1 cjswgd = 2.1e-010

+mjswgd = 0.33 tpb = 0 tcj = 0 tpbsw = 0

+tcjsw = 0 tpbswg = 0 tcjswg = 0 xtis = 3

+dmcg = 0 dmci = 0 dmdg = 0 dmcgt = 0

+dwj = 0 xgw = 0 xgl = 0

+rshg = 0.4 gbmin = 1e-010 rbpb = 5 rbpd = 15

+rbps = 15 rbdb = 15 rbsb = 15 ngcon = 1

.model pmos pmos level = 54

+version = 4.0 binunit = 1 paramchk= 1 mobmod = 0

+capmod = 2 igcmod = 1 igbmod = 1 geomod = 1

+diomod = 1 rdsmod = 0 rbodymod= 1 rgatemod= 1

+permod = 1 acnqsmod= 0 trnqsmod= 0

+tnom = 27 toxe = 6.7e-010 toxp = 4e-010 toxm = 6.7e-010

+dtox = 2.7e-010 epsrox = 3.9 wint = 5e-009 lint = 1.35e-009

+ll = 0 wl = 0 lln = 1 wln = 1

+lw = 0 ww = 0 lwn = 1 wwn = 1

+lwl = 0 wwl = 0 xpart = 0 toxref = 6.7e-010 xl = -9e-9

+dlcig = 1.35e-009

+vth0 = -0.25399 k1 = 0.2 k2 = -0.01 k3 = 0

+k3b = 0 w0 = 2.5e-006 dvt0 = 1 dvt1 = 2

+dvt2 = -0.032 dvt0w = 0 dvt1w = 0 dvt2w = 0

+dsub = 0.1 minv = 0.05 voffl = 0 dvtp0 = 1e-011

+dvtp1 = 0.05 lpe0 = 0 lpeb = 0 xj = 7.2e-009

+ngate = 1e+023 ndep = 4.4e+018 nsd = 2e+020 phin = 0

+cdsc = 0 cdscb = 0 cdscd = 0 cit = 0

+voff = -0.13 nfactor = 2.3 eta0 = 0.0037 etab = 0

+vfb = -1.058 u0 = 0.0023 ua = -5e-010 ub = 1.6e-018

+uc = 0 vsat = 78000 a0 = 1 ags = 1e-020

+a1 = 0 a2 = 1 b0 = 0 b1 = 0

+keta = -0.047 dwg = 0 dwb = 0 pclm = 0.1

+pdiblc1 = 0.001 pdiblc2 = 0.001 pdiblcb = 3.4e-008 drout = 0.6

+pvag = 1e-020 delta = 0.01 pscbe1 = 2e+009 pscbe2 = 9.58e-007

+fprout = 0.2 pdits = 0.08 pditsd = 0.23 pditsl = 2300000

+rsh = 5 rdsw = 60 rsw = 30 rdw = 30

+rdswmin = 0 rdwmin = 0 rswmin = 0 prwg = 0

+prwb = 0 wr = 1 alpha0 = 0.074 alpha1 = 0.005

+beta0 = 30 agidl = 0.0002 bgidl = 2.1e+009 cgidl = 0.0002

+egidl = 0.8 aigbacc = 0.012 bigbacc = 0.0028 cigbacc = 0.002

+nigbacc = 1 aigbinv = 0.014 bigbinv = 0.004 cigbinv = 0.004

+eigbinv = 1.1 nigbinv = 3 aigc = 0.012731 bigc = 0.00115

+cigc = 0.0008 aigsd = 0.012731 bigsd = 0.00115 cigsd = 0.0008

+nigc = 1 poxedge = 1 pigcd = 1 ntox = 1

+xrcrg1 = 12 xrcrg2 = 5

+cgso = 7e-011 cgdo = 7e-011 cgbo = 0 cgdl = 3e-011

+cgsl = 3e-011 clc = 1e-007 cle = 0.6 cf = 1.1e-010

+ckappas = 0.6 ckappad = 0.6 vfbcv = -1 acde = 1

+moin = 15 noff = 1 voffcv = 0

+kt1 = -0.14 kt1l = 0 kt2 = 0.022 ute = -1.1

+ua1 = 1e-009 ub1 = -1e-018 uc1 = -5.6e-011 prt = 0

+at = 33000

+fnoimod = 1 tnoimod = 0 noia = 6.25e+041 noib = 3.125e+026

+noic = 8.75e+009 em = 41000000 af = 1 ef = 1

+kf = 0 tnoia = 1.5 tnoib = 3.5 ntnoi = 1

+jss = 2e-007 jsws = 4e-013 jswgs = 4e-013 njs = 1

+ijthsfwd= 0.1 ijthsrev= 0.1 bvs = 10 xjbvs = 1

+jsd = 2e-007 jswd = 4e-013 jswgd = 4e-013 xjbvd = 1

+pbs = 1 cjs = 0.0015 mjs = 0.5 pbsws = 1

+cjsws = 9.4e-011 mjsws = 0.33 cjswgs = 2e-010 cjd = 0.0015

+cjswd = 9.4e-011 mjswd = 0.33 pbswgd = 1 cjswgd = 2e-010

+mjswgd = 0.33 tpb = 0 tcj = 0 tpbsw = 0

+tcjsw = 0 tpbswg = 0 tcjswg = 0 xtis = 3

+dmcg = 0 dmdg = 0 dmcgt = 0 xgw = 0

+xgl = 0

+rshg = 0.1 gbmin = 1e-012 rbpb = 50 rbpd = 50

+rbps = 50 rbdb = 50 rbsb = 50 ngcon = 1