

DESIGN OF DUAL OUTPUT DIFFERENTIAL PAIR SECOND GENERATION CURRENT CONVEYOR

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MASTER OF TECHNOLOGY

in VLSI Design

Submitted By

RADHIKA SINGH

601562019

Under Supervision of

Dr. Rishikesh Pandey

Assistant Professor, ECED

Thapar University, Patiala, Punjab



ELECTRONICS AND COMMUNICATION ENGINEERING DEPARTMENT

THAPAR UNIVERSITY, PATIALA, PUNJAB

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DECLARATION

I, Radhika Singh declare that the work presented in this thesis entitled "Design of Dual Output Differential Pair Second Generation Current Conveyor" in fulfillment of the requirement for the award of degree of Master of Technology submitted at Electronics and Communication Engineering Department, Thapar University, Patiala is an authentic record of work carried out under supervision of Dr. Rishikesh Pandey, Assistant Professor, ECED, Thapar University, Patiala.

The matter presented in this has not been submitted either in part or full to any other university or institute for the award of any other degree.

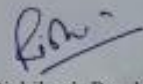
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Radhika Singh

Roll No.-601562019

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Date: 28/08/2017


Dr. Rishikesh Pandey
Assistant Professor, ECED
Thapar University, Patiala

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Radhika Singh

Roll. No - 601562019

ABSTRACT

Current Conveyors have proved to be the emerging class of current mode circuits. It is an extremely flexible and versatile analog building block used for both current and voltage processing applications. Among the three generations of current conveyors, second generation current conveyors are widely used. Current Conveyors give high performance parameters in terms of high frequency response, high current and voltage gain, high current and voltage transfer bandwidth, low power consumption and low supply voltage requirement.

In the thesis, CMOS class AB dual output differential pair second generation current conveyor (DODCCII) and quasi floating gate MOSFET based dual output differential pair second generation current conveyor (QFGDODCCII) are presented. The feedback network is used in the circuit to obtain low parasitic resistance. The DODCCII uses current mirror load for the differential pair whereas the QFGDODCCII eliminates the current mirror load and uses quasi floating gate MOSFET as the input transistors of the differential pair. The circuits have high current and voltage gains, high current and voltage transfer bandwidths at two different nodes Z- and Z+, high power dissipation, high output impedance and low supply voltage requirement. The QFGDODCCII has rail to rail dynamic range of -0.7V to 0.7V and low parasitic input impedance of 8.53Ω . The above discussed circuits are designed and simulated in 0.18 μm BSIM3V3 environment.

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SYMBOLS

CMOS	CMOS Complementary Metal Oxide Semiconductor
BSIM	Berkeley Short- Channel IGFET Model
MOSFET	Metal Oxide Semiconductor Field Effect Transistor
CCI	First Generation Current Conveyor
CII	Second Generation Current Conveyor
CCIII	Third Generation Current Conveyor
QFGMOS	Quasi Floating Gate Metal Oxide Semiconductor
CCCII	Current Controlled Second Generation Conveyor
ECCII	Electronically Tunable Second Generation Current Conveyor
DDCC	Differential Difference Current Conveyor
MIDCC	Multiple Input Differential Current Conveyors
MOCCII	Multiple Output Second Generation Current Conveyors
LCMFB	Local Common-Mode Feedback Amplifier
FG-MOS	Floating Gate MOSFET
FDCCCII	Fully Differential Current Controlled Conveyor
DDCC	Differential Difference Current Conveyor
FVF	Flipped Voltage Follower
DCCDVDOCCII	Double Current Controlled Differential Voltage Dual Output Current Conveyor
VFCOA	Voltage Feedback Current Operational Amplifier
CMRR	Common Mode Rejection Ratio
DODCCII	Dual Output Differential Pair Second Generation Current Conveyor
QFGDODCCII	Quasi Floating Gate MOSFET based dual output differential second generation current conveyor
DRC	Design Rule Check

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CHAPTER 1

INTRODUCTION

1.1 Introduction

Always there is a need for low voltage and low power design, for example, with portable systems where a low supply voltage given by a single battery is used. In the past years, the trend of operating analog designs gained a lot of appreciation as the information was represented by voltages at the various input and output nodes of the circuit. The voltage mode circuits have high input resistance and low output resistance. Various disadvantages of voltage mode circuits are its low slew rate which is dependent on time constants associated with the circuits, higher supply voltage required for better signal to noise ratio and tradeoff between speed and bandwidth [1]. Due to sudden change in input voltage and associated stray and other capacitances, the output voltage does not change instantly due to which voltage mode circuits exhibit moderate performance. The voltage mode circuits do not perform well in high frequency applications because the high valued resistors with parasitic capacitances create a dominant pole at relative low frequency which limits the bandwidth. So, there was a need to change the functioning of the circuits to achieve all the performance parameters such as low supply voltage, low power consumption, larger bandwidth, high dynamic range, high current and voltage gain using current signals instead of voltage signals. There are various advantages of current mode circuits over voltage mode circuits as they achieve high performance in terms of precision, speed and data transmission. Current mode circuits have low input impedance, high output impedance, wide bandwidth, high slew rate, low supply voltage requirement, low power consumption, higher dynamic range and easy mathematical operations of signals. In these circuits, there is no trade-off between speed and bandwidth and performance gets improved. The influence of reduction in supply voltage is less severe in current mode circuits as compared to voltage mode circuits. In order to achieve advantages of current mode circuits, various analog building blocks were introduced such as current mirrors, current conveyors, etc. Current conveyors are preferred over current mirrors as current conveyors provide high speed and high frequency response in both current and voltage signal processing whereas current mirrors play a major role in current processing only. The introduction of current conveyors in 1968 by Smith and Sedra and its

modification and reformation has gained acceptance rapidly in terms of flexibility and versatility as a practical analog building block [2].

The function of current conveyor is to convey current from input to output with amplification as signal is conveyed not attenuated. A current conveyor is composed as a three terminal analogue electronic device. It is basically a unity gain element that exhibits high linearity, wide dynamic range, high bandwidth and better high frequency performance. It has high voltage and current transfer bandwidth, simple circuitry and capability to operate at low voltages. The capability of current conveyors to operate at low voltages also creates tradeoff with the threshold voltage. With decrease in supply voltage, threshold voltage also decreases to maintain high drive current but leakage current increases. So, to prevent leakage current use of halo implants and retrograde wells can be made. Current Conveyors when configured with other circuit elements perform many analogue signal processing functions, in a similar manner to the way op amps. Current Conveyors further give various advantages and disadvantages based on its three generations namely first generation current conveyor (CCI), second generation current conveyor (CCII) and third generation current conveyors (CCIII).

1.2 Motivation

Among all the three generations of current conveyors, the second generation current conveyor (CCII) is the most preferred versatile and widely used building block which has high input impedance and low output impedance, thus giving the main advantage of avoiding the loading effect. A circuit with low output impedance and high input impedance has a greater load which can be withstand. The first and third generation current conveyors however, cause loading of the device. Moreover, in both the generations the current flows in all the blocks terminals which becomes problematic and reduces their flexibility and versatility. Also dropping too much voltage across output impedance of one amplifier caused by overloading of amplifier makes other amplifier to be under driven which causes overloading of second amplifier. The second generation current conveyors give high performance parameters in terms of reduced supply voltage, higher dynamic range, higher frequency response, higher current and voltage gains and reduced power consumption and most importantly the reduced parasitic input impedance and higher output impedance. Further there are many topologies of current conveyors such as class A topology, class AB topology, differential pair topology and translinear loop topology. The differential pair topology is the most widely used topology for CCII. It offers the reduced input

parasitic impedance, high output voltage swing and high bandwidth as compared to other topologies. The quasi floating gate MOSFETs when used at the inputs further give the improved characteristics by lowering the threshold below the ideal threshold value. The circuit based on quasi floating gate MOSFETs use reduced supply voltage and give rail to rail dynamic range of current as well as voltage.

1.3 Organization of Thesis

The organization of the thesis is as follows:

CHAPTER 1: This chapter discusses the need for current mode approach, current conveyors, motivation and the organization of the thesis.

CHAPTER 2: This chapter gives various topologies of current conveyors along with the work being reported in literature, comparison of various topologies on the basis of the survey, discussion of the compared work to find out the best work reported so far.

CHAPTER 3: In this chapter, a low power low supply dual output second generation current conveyor and QFG based low power low supply dual output second generation current conveyor has been proposed with reduced input parasitic resistance, higher bandwidth and higher linearity.

CHAPTER 4: The simulation results of proposed low power low supply dual output second generation current conveyor and QFG based low power low supply dual output second generation current conveyor have been discussed, comparison of the two proposed circuits and the best reported work in literature is being done and layout of the proposed circuits are shown.

CHAPTER 5: This chapter summarizes the dissertation and discusses the future scope of the proposed work.

CHAPTER 2

LITERATURE REVIEW

Current Conveyors present the emerging class of high performance analog circuit design based on current mode approach. The current mode circuits are used in voltage signal processing and current signal processing applications. The most widely used basic analog building block is second generation current conveyor (CCII) which is used for various high frequency applications such as oscillators, filters, differentiators, integrators, etc. It exhibits high gain, high frequency response, high dynamic range of current and voltage signals, low power dissipation, low parasitic input impedance and high output impedance. The four topologies namely class A, class AB, differential pair and translinear loop are used to develop current conveyors.

The various second generation current conveyors reported in literature [3-32] are as follows:

Class A second generation current conveyor with controlled current gain is suggested by Fabre *et al.* [3]. The circuit is made up of mixed translinear loop in the input and two complementary current mirrors with adjustable gains using a cascode stage. The limitation of harmonic distortion which usually occurs in class A is overcome in the circuit. The circuit has severe peaks in the frequency response and very low output impedance. The cascode stage minimizes the effect of these limitations and with the help of translinear loop the current gain is controlled instead of being fixed.

The class AB current conveyor is presented by Oliaei *et al.* [4]. The class AB CCII with floating voltage source in the structure gives low input resistance with variability of about 10% in the dynamic range. The input parasitic resistance is reduced by the use of negative feedback at the input. The current conveyor based on class AB design with floating voltage source maintains voltage difference between the gates of the transistor and hence, a good tracking accuracy is obtained. The circuit can be used to design both positive and negative types of current conveyors as well as current mirrors.

Emami *et al.* [5] has proposed a class A current conveyor using CMOS. The circuit provides high performance by lowering input resistance and improving transfer gain errors. Also, it is free from body effect. In the circuit, the effect of series resistance which adds up due to level shifting

is compensated by the changed input resistance of the source follower stage. Therefore, a negligible input resistance is obtained and also the circuit is quiet stable.

A wideband CMOS current conveyor based on flipped voltage follower is suggested by Lopez Martin *et al.* [6]. The circuit has low power consumption, low supply voltage requirement, simple circuitry and compactness. In the circuit with the use of flipped voltage follower the d.c level shifter which is diode connected is being avoided. Also, the feedback from the amplifier further reduces the input impedance and increases the voltage gain. A universal biquadratic filter is also designed using the current conveyor.

Hassanein *et al.* [7] proposed high accuracy class A CMOS second generation current conveyor. This circuit exhibits voltage gain of almost unity, low voltage, low resistance and the high tracking accuracy which is independent of input current.

A third order current controlled quadrature oscillator is proposed by Maheshwari *et al.* [8]. The circuit has high input impedance and non interactive frequency. The circuit is made up of voltage-mode low pass filter and an integrator in feedback loop in inverting mode. The advantage of this circuit is that it only uses grounded capacitors and no resistors. Also, this third order oscillator has low total harmonic distortion with wide tunability of bias currents of CCCIs.

The proposed circuit by Dutta *et al.* [9] gives the designing of second generation current conveyor based on translinear loop structure. The technique used in implementation uses exponential property of diodes and the current conveying action of second generation current conveyors. Different mathematical functions are implemented which give squaring, geometric-mean and square root operation which are basically static translinear circuits. The dynamic translinear circuits also give applications such as a second order low pass filter and fourth order filter with all frequency responses. The filters are electronically tunable by the alteration of bias currents.

Minaei *et al.* [10] suggested an electronically tunable current conveyor of second generation (ECCII) implemented by CMOS technology. The circuit is based on differential pair based topology. The current gain of the circuit is electronically controlled by adjustment of the ratio of d.c bias currents. The circuit exhibits low input impedance and high output impedance which enables cascability. The supply voltage requirement and average power consumption of the circuit is low. The various applications of CCII with electronically controlled gain is an universal

filter which gives high pass, band pass and low pass responses. The low pass response is obtained at high impedance and its gain is varied by changing the biasing current of ECCII.

A three input and one output biquadratic filter which makes use of three differential difference current conveyors (DDCC) has been proposed by Chiu *et al.* [11]. The circuit uses differential pair topology and is operated in voltage mode. The circuit has high input impedance and low output impedance. Due to the low output impedance of the circuit, it can be easily connected to the input of another stage without using a buffer. The circuit offers advantages of low sensitivities and limited use of grounded capacitors and resistors along with DDCCs. The circuit implements various filters such as high pass, band pass, all pass and low pass filters without any condition of component matching.

A multiple input differential current conveyor (MIDCC) suggested by Horng *et al.* [12] gives the advantage of processing multiple inputs at a time. The circuit is deduced from differential difference amplifier, universal current conveyor and differential difference current conveyor. In the circuit the high gain is attained by composition of a current mirror which has the ability to convert the differential current into output voltage. Low resistance of the circuit is achieved by using a source follower stage. The circuit offers all performance characteristics of a conveyor and is basically transformed version of MOCCII. The circuit helps in converting a current mode filter employed by multiple output second generation current conveyors (MOCCII) into voltage mode filter using MIDCCs.

Thankanchan *et al.* [13] proposed a BiCMOS class A current conveyor structure. In the circuit, the bipolar current mirror is used due to large dynamic range. Also, the input stage and the current source are implemented through MOS in order to achieve high input resistance. The circuit is good for applications of VLSI which require low voltage and exhibit low power consumption. The circuit is insensitive to the variations in threshold voltage. It has small bandwidth and wide dynamic range of both current and voltage signals.

A current controlled multiphase sinusoidal oscillator has been suggested by Kumngern *et al.* [14] employed by translinear loop topology. Basically the current controlled second generation current conveyor has a controlled current gain which is developed by using current mirror having adjustable gain. The addition of simple current mirrors and the cross coupled ones make CCCIIs multiple output in nature. The main features of the oscillator circuit are that it uses one CCCII and one grounded capacitor for each phase and the phases are equally spaced. The same circuit

produces odd as well as even phase at a time. The circuit has low sensitivities and high output impedances which make cascading easy.

A low voltage and low power second generation current conveyor circuit for resistive gas sensors has been proposed by Ferri *et al.* [15]. The circuit evaluates the resistive behavior of gas sensors without any calibration and exciting the gas sensor with a dc voltage. The gas sensor circuit operates at a low supply voltage and consumes low power. Also, it can be used in portable applications.

The class AB current mode circuit suggested by Lopez Martin *et al.* [16] with quasi floating gate technique gives high accuracy and micro power operation. The quasi floating gate technique predicts the class AB behavior of the circuit by preserving low distortion for the currents even beyond the bias current. The d.c. level shift is implemented by the diode connected transistors which sets the quiescent current in transistors. Due to this, the supply requirement and the power consumption is increased. In the circuit, a feedback loop is also implemented which lowers the input resistance and increases the dynamic range of the circuit.

A buffer for high density microelectrode arrays has been proposed by Livi *et al.* [17] with low voltage class AB operation. The current conveyor operates in two modes i.e current mode and voltage mode. Class AB based voltage follower with a local common-mode feedback amplifier (LCMFB) is implemented in voltage mode which possess high current. A good linear range is obtained. For operation in current mode, current conveyor with the same local common mode feedback amplifier as was used in voltage mode is implemented with cascode stages to increase the gain. This structure is used for recordings of neuronal cells with stimulation feature of the circuit.

A compact second generation current conveyor has been suggested by Naik *et al.* [18] which is made up of flipped current mirror and flipped voltage follower. The advantage of high speed for a given consumption of current and requirement of low supply voltage are related to simplicity of buffer in terms of stacking of transistors and number of internal nodes. The feedback in the flipped voltage follower makes low output impedance. The circuit has high current and voltage gain, low power consumption, low supply voltage requirement and limited bandwidth.

Kumngern *et al.* [19] has suggested a single-input-multiple-output filter using translinear loop topology of current controlled second generation current conveyor (CCCII). The circuit makes

use of two grounded capacitors and three translinear CCCII. Also the circuit exhibits high output impedance which provides easy cascading of the circuit. The natural frequency of the circuit, its quality factor and other parameters of the circuit are orthogonally tuned with the adjustment of biasing currents of CCCII. The various applications where the circuit is used are low pass, band pass, high pass and all pass filters.

Abolila *et al.* [20] suggested a class AB folded cascode amplifier based on second generation current conveyor. The circuit uses class AB topology but is based on cross quad differential pair so as to increase the dynamic range. In order to get high level of circuit performance, a folded cascode operational amplifier is presented. The proposed circuit has low voltage and low power operation. It exhibits low resistance at input, high output impedance and wide bandwidth with rail to rail dynamic range of current and voltage. One of the applications of conveyor as a square wave oscillator has also been reported.

Khateb *et al.* [21] has proposed a class AB current conveyor using bulk driven technique. In the circuit, input is applied to bulk terminal of input transistors and gates are connected to supply voltage. The folded cascode structure is utilized to get single ended signals. The circuit has high linearity, low input resistance, high output resistance, acceptable current and voltage bandwidths, high performance and low supply voltage requirements.

A current controlled second generation conveyor (CCCI) has been suggested by Hassen *et al.* [22] which is operated at low supply voltage and has high current and voltage transfer bandwidth. Also, the parasitic resistance at input is low for a specified control current. Basically, the circuit introduces two flipped voltage follower based current mirrors in the conventional CCCII so as to have high bandwidth of the circuit. The circuit is linear in voltage and current conveying action. A universal current mode filter is also presented as an application of the circuit.

R. Chaisrichareon *et al.* [23] has proposed a current controlled second generation conveyor (CCCI) implemented with multiple differential pairs. The circuit uses the gain of PMOS differential pair to lower the intrinsic resistance at the input. The reduced input impedance at input along with good current and voltage gains is obtained.

A FG-MOS based fully differential second generation current controlled conveyor (FDCCCI) is presented by R.Fani *et al.* [24]. The circuit is based on differential pair topology and uses

floating gate MOSFETs at the inputs. The circuit offers rail to rail dynamic range, low power consumption, low supply voltage requirements and low parasitic impedance.

The circuit proposed by Kumngern [25] uses the differential pair topology of current conveyors. The circuit is a realization of a CMOS second generation current conveyors (CCII) with a technique which gives the advantage of variable current gain. The circuit makes use of a differential difference current conveyor (DDCC) based log-antilog current amplifier which has composition of one DDCC along with four diodes. Basically the variable current gain CCII is made up of a follower cell and a current amplifier. The current gain controllability is achieved by the adjustment of ratio of the biasing currents.

Monstakas *et al.* [26] has proposed a current conveyor based on a basic cell named flipped voltage follower. The current conveyor has low supply voltage requirement and low power consumption. The biasing current does not limit the driving capability in class AB and depends only on the transistor aspect ratios and hence, driving the current at input and output nodes. The circuit offers low harmonic distortion, low output impedance, high dynamic range and high input impedance. Also, a super source follower is discussed which is a folded version of FVF to further improve dynamic range at higher supply voltages.

A wideband oscillator with low supply has been suggested by J. Jain *et al.* [27]. The circuit uses differential pair topology and has high frequency response, low supply voltage requirements and low power consumption. The differential pair based CCII in the circuit has wider bandwidth than voltage mode circuits. A low supply voltage and minimum number of transistors are used in the circuit. It has high current gain, high voltage gain and high voltage and current transfer bandwidths. A low voltage low power oscillator with wide bandwidth is implemented using the current conveyor.

Yenkar *et al.* [28] has suggested a double current controlled differential voltage dual output current conveyor (DCCDVDOCII) which works on the principle of differential amplifier and current conveyor. The circuit comprises of voltage followers, dual output current conveyors and second generation current conveyors. All the blocks are internally connected with each other. The circuit has fine electronic tuning due to the currents flowing through external resistances. The various advantages of the circuit are high common mode rejection ratio, efficiency to vary the gain by current controlling resistance and voltage controlling resistance. The circuit is used for implementation of various applications such as differential voltage amplifier, differential

voltage to current converter, floating impedance converter, square wave generator and Schmitt trigger comparator.

A CMOS charge pump is proposed by Moustakas *et al.* [29], which uses a differential pair CCII. The current conveyor based voltage buffer is used to replicate the operating condition of NMOS and produce equal current at input. Then this current is conveyed to output terminal and is used to source the current at the output of the charge pump. The scheme of source switching helps in reducing glitches. The circuit gives high performance in terms of its static and dynamic operation and has a very low mismatching of current and reduced glitching. The output voltage range of the circuit is rail to rail so as to obtain wide output swing.

A second generation current conveyor based on super class AB OTA cells is suggested by Ettaghzouti [30]. The current conveyor is implemented by the use of adaptive bias which improves the linearity of the circuit making it rail to rail operated. The circuit has low supply voltage requirement, high frequency response, low parasitic input resistance and low power consumption. Due to wide bandwidth the circuit is used for various applications such as filters by making use of two or more current conveyors.

A class AB voltage feedback current operational amplifier (VFCOA) has been proposed by Alfaro *et al.* [31]. The function of VFCOA is to combine variable and constant tunable bandwidths. The circuit composed of cascode NMOS current mirror and the transformed PMOS static bias current circuit into quasi floating gate dynamic bias current mirror gives class AB operation. The circuit exhibits variable gain, high input impedance, low output impedance, high linearity, low power, high current capability and low total harmonic distortion.

Kumngern *et al.* [32] suggested a fully differential current conveyor by the use of bulk driven quasi floating gate (QFG) technique. Due to the bulk driven nature of the structure, it has low supply voltage requirement and high output swing. The QFG increases the performance in terms of high frequency response. The QFG based current conveyor along with bulk driven feature provides rail to rail d.c current and voltage range, high current and voltage bandwidth, low power dissipation, low input resistance and high CMRR. The circuit implements various applications such as biquadratic filter and low pass filter.

Table 1: Current Conveyors Available In Literature

Ref. No.	CMOS Technology	Supply Voltage	Voltage Transfer Bandwidth	Current Transfer Bandwidth	Voltage gain	Current gain	Output Dynamic Range	Power consumption	R _x	R _y	R _z
[23]	0.5μm	3.3V	-	-	-	-	-	-	12.6Ω	-	-
[16]	2μm	V _{dd} = V _{ss} =2.5V	-	-	-	-	-1.5V-1.2V, -10μA-10μA	-	<30Ω	-	-
[12]	0.5μm	V _{ss} =0V, V _{dd} =+1.5V	100MHz	-	-	-	-	750μW	-	-	-
[5]	0.5μm	V _{dd} = V _{ss} =0.96V	-	-	1	1	-	-	-	-	-
[25]	0.35μm	V _{dd} = V _{ss} =-1.5V	NA/ suitable for cascading	-	Variable	Variable	-	6600μW	46Ω	5.9GΩ	73MΩ
[26]	0.35μm	V _{dd} = V _{ss} =1.65V	NA	-	Variable	Variable	-	-	-	-	-
[27]	0.35μm	V _{dd} = V _{ss} =1.65V	391MHz	-	0.9228	0.9957	-	-	43Ω	∞	>75KΩ
[14]	0.25μm	V _{dd} = V _{ss} =0.5V	30MHz	480MHz	0.95	1	-0.5V-0.5V	771μW	13Ω	1E20Ω	2KΩ
[9]		V _{dd} = V _{ss} =0.75V	10.5MHz	-	1	1	-		13Ω	>1GΩ	2.6MΩ
[20]	0.5μm	V _{dd} = V _{ss} =1.65V	-	-	2		-	99uW	30Ω	-	-
[24]	0.6μm	5V	223KHz	115KHz	48dB	51dB	0.5V-3.5V	-	-	-	-
[17]	0.5μm	1.5V	100MHz	-	1.8	1.1	-	105μW	14KΩ	7MΩ	15KΩ
[28]	0.5μm	V _{dd} = V _{ss} =2.5V	-	-	Variable	Variable	-	-	4.5KΩ	490MΩ	41.75KΩ
[18]	0.35μm	V _{dd} = V _{ss} =1.5V	57.2MHz	-	0.994	-	-320mV-+360mV	19.5uW	54Ω	5MΩ	4.1MΩ
[1]	0.18μm	V _{dd} = V _{ss} =0.7V	2.686GHz	2.667GHz	0.998	0.967	650mV-550mV	270μW	-	∞	-
[31]	0.1μm	V _{dd} = V _{ss} =3.0V	-	-	β=R ₁₂ /R ₁₁	-	-	-	-	-	-
[30]	65nm	1.1V	-	-	-	-	100mV-920mV	-	-	-	-
[21]	0.18μm	V _{dd} = V _{ss} =0.75V	3GHz	2.96GHz	1	1	-0.75V-+0.75V/-220uA-+220uA	230μW	8.26Ω	∞	46.5KΩ
[41]	0.5μm	3.3V	-	-	-	0-24dB	--	280.5μW	-	-	5.6KΩ

Discussion

The circuits presented in [21] and [1] give high performance parameters as shown in Table 1. The circuits exhibit low supply voltage requirement, high voltage and current transfer bandwidth, high current and voltage gain, low power consumption, low input impedance, high output impedance and high current and voltage output dynamic range. In [21] the supply voltage is more than [1] but current and voltage transfer bandwidth is higher as compared to [1].

CHAPTER 3

DESIGN OF DIFFERENTIAL PAIR SECOND GENERATION CURRENT CONVEYORS

3.1 Introduction

In this chapter, design of dual output class AB differential second generation current conveyor (DODCCII) and quasi floating gate MOSFET (QFGMOS) based dual output second generation current conveyor (QFGDODCCII) with low input parasitic resistance (R_x) is presented. The chapter is organized as follows. Section 3.2 presents a dual output differential second generation current conveyor (DODCCII) using conventional MOSFETs. The operation of QFGMOS has been discussed in section 3.3. In section 3.4, a QFGMOS based dual output class AB differential second generation current conveyor (QFGDODCCII) has been proposed.

3.2 Dual Output Class AB Differential Pair Second Generation Current Conveyor

The class AB current conveyor improves the performance of second generation current conveyors and the differential pair topology helps in implementing a feedback connection to the input, thus making the two input voltages equal. The circuit is simple to implement and the feedback connection at the input makes the input impedance low. Earlier, the biasing of the feedback stage and output stage was dependent on aspect ratio of the transistors due to which there was large dependence on the supply voltage. This fundamental problem of biasing currents at the output stages is overcome by use of a differential pair topology because biasing of feedback transistors is done by suitable choice of the biasing currents flowing through the diode connected transistors which act as biasing current sources and a resistance R . Also, there is no dependence on supply level.

The dual output conveyor is obtained by using class AB current follower which changes the direction of current with respect to the input, that is, if the output current is decreasing with increase in input current linearly, it changes and increases with increase in input current. Therefore, the circuit works as both CCII- and CCII+. Therefore, the circuit behaves as dual output CCII.

circuit has two output nodes Z- and Z+. The two nodes have equal currents flowing through them with the use of class AB current follower.

In Figure 3.1, in order to find the low input resistance, the differential pair circuitry (M3-M6) and transistors M10 and M11 are of interest.

The output voltage (V_x) is taken from the drains of transistor M10 and M11. The equivalent output voltage from transistors M10 and M11 is equal to the output voltage of the differential pair. Therefore,

$$V_a = \left(r_0 * \frac{(gm_3 * V_x - gm_4 * V_4)}{2} \right) \quad (3.1)$$

where r_0 is the parallel combination of r_{04} and r_{06} . r_{04} and r_{06} are the output impedances of transistors M4 and M6 respectively.

$$I_x = (gm_{10} + gm_{11}) * V_a \quad (3.2)$$

In (eq.3.2) gm_{10} and gm_{11} are the small signal trans-conductance parameters of M10 and M11 respectively.

Since the small signal analysis drops out the input voltage to ground, V_4 becomes zero. Substituting V_a in I_x , the expression of I_x comes out to be,

$$I_x = \frac{(gm_{10} + gm_{11}) * (gm_3 * V_x) * r_0}{2} + (gm_{10} || gm_{11}) * V_x \quad (3.3)$$

Further, (eq.3.3) becomes

$$\frac{V_x}{I_x} = \frac{1}{\left(gm_{10} + gm_{11} + \frac{gm_3 * r_0}{2} * (gm_{10} + gm_{11}) \right)} \quad (3.4)$$

where gm_3 is the trans-conductance of transistor M3. The input parasitic impedance R_x at input port X is given as

$$R_x = \frac{1}{\left[\left(\frac{r_{010} + r_{011}}{r_{010} * r_{011}} \right) + \left(\frac{gm_3 * gm_{r0}}{2} \right) * (gm_{10} + gm_{11}) \right]} \quad (3.5)$$

where r_{010} and r_{011} are the output impedances of transistors M10 and M11 respectively. The impedance at port Y is quite high and given as

The equivalent model of QFGMOS is shown in Figure 3.3(b) where all the capacitances along with the large resistance R_L are mentioned which are used to find the expressions for input voltage, gate voltage, threshold voltage and total capacitance. The coupling capacitances appearing between the control gate and the QFGMOS couple the signal applied at the input to QFGMOS [202]. Capacitances appear as floating nodes to the circuit simulators, therefore, resistances in the range of $G\Omega$ are connected in parallel to the capacitances. The value of capacitances is so selected that the time constant RC of all the pairs comes same, such that $R_1 \cdot C_1 = R_L \cdot C_{gd}' = R_{gs} \cdot C_{gs} = R_{gb} \cdot C_{gb} = R_{gd} \cdot C_{gd}$.

Moreover, due to the connection of large valued resistor implemented by the diode connected MOS to the supply rail eliminates the problem of trapped charge on floating gate. The reverse biased diode connected MOS operates in cut off region and the QFGMOS operates in triode region. Due to its operation in triode region, rail to rail dynamic range is obtained. The use of large resistances does not affect the a.c operation of the signals and makes the QFGMOS floating for low frequency operation. By modifying the operation of conventional MOSFET, the equation of QFGMOS can be obtained.

The voltage (V) at the gate of QFGMOS is expressed by eq.3.4.

$$V = \frac{s \cdot R_L \cdot C_T}{1 + s \cdot R_L \cdot C_T} * V_{in} \quad (3.8)$$

where R_L is the large resistance, V_{in} is the input voltage and $C_T (= \sum_{k=1,2,3...n} C_k + C_{gs} + C_{gd} + C_{gb} + C_{gd}')$ is the total capacitance of the QFGMOS. C_k represents the capacitance between the gate and the nth input capacitance, C_{gs} represents the gate to source capacitance, C_{gd} is the gate to drain capacitance, C_{gb} is the gate to bulk capacitance and C_{gd}' is the gate to drain capacitance of the weakly connected diode connected MOSFET.

The effective threshold voltage of QFGMOS (V_{Teff}) is lower than V_T of conventional MOSFET and is given by eq.3.10.

$$V_{Teff} = \frac{V_T - K_2 \cdot V_{dd}}{K_1} \quad (3.9)$$

where $K_1 = C_1/C_T$ and $K_2 = C_{gd}'/C_T$, V_{dd} is the supply voltage.

3.4 Proposed QFGMOS Based Class AB Dual Output Differential Pair Second Generation Current Conveyor

A dual output differential pair second generation current conveyor (CCII) using QFGMOS at the input has been proposed. The proposed QFGMOS based dual output differential pair second generation current conveyor (QFGDODCCII) is shown in Figure 3.4.

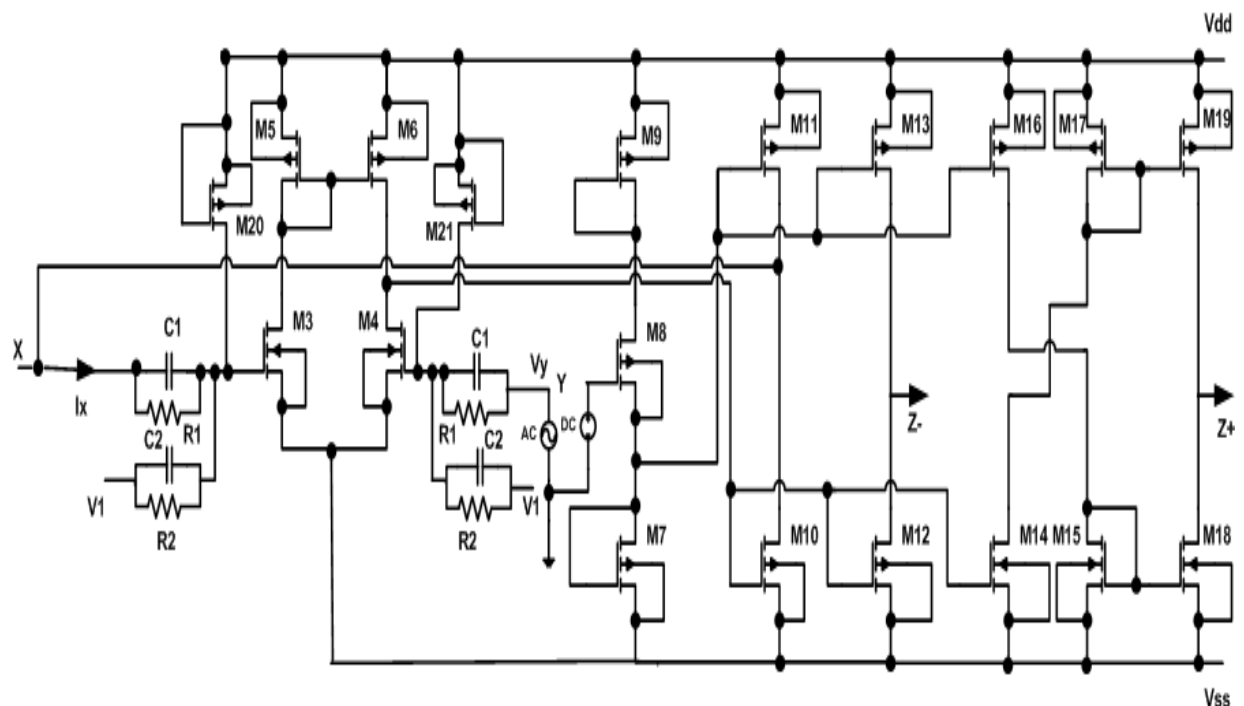


Figure 3.4 Dual Output Differential Pair Second Generation Current Conveyor using QFGMOS

The proposed circuit is the modified form of circuit shown in Figure 3.1. In figure 3.4, the current mirror circuit and a d.c current source I_{bias} has been removed due to the use of QFGMOS at the input of differential pair. Transistors M3 and M4 are the QFGMOS transistors. The transistors M20 and M21 are reverse diode connected PMOS which offer a large value of resistance to get the gate voltage (V) and lower the threshold voltage of QFGMOS than the conventional MOSFET. Voltage V1 is used as d.c bias voltage for the transistors M3 and M4. The transistors M10 and M11 are used to provide a feedback path to node X and the transistors M12 and M13 operate in saturation region and used as output stage giving output at node Z-. The circuit is implemented so as to get low parasitic input resistance at node X.

The parasitic input impedance at node X is calculated same as of the circuit in Figure 3.1 but with the QFGMOS at the inputs of the differential pair. The equations change due to the

presence of capacitors which configure the QFGMOS. The expression for g_{m3} changes and is written as G_{mx} . The expression of G_{mx} includes various capacitances associated with it and the output impedances of various transistors.

$$G_{mx} = \left(\frac{g_{m3}}{g_{d4} * g_{d6}} \right) * (g_{m10} + g_{m11}) * \left(\frac{C_1}{C_T} \right) \quad (3.10)$$

where g_{d4} and g_{d6} are the output conductances of transistors M4 and M6, C_1 is the input capacitance applied at the gate of QFGMOS and $C_T = C_1 + C_2 + C_{GS} + C_{GD} + C_{GB}$.

$$R_x = \frac{1}{g_{d10} + g_{d11} + G_{mx}} \quad (3.11)$$

Substituting value of G_{mx} , R_x comes out to be

$$R_x = \frac{1}{\left[\left(\frac{r_{010} + r_{011}}{r_{010} * r_{011}} \right) + \left(\frac{G_{mx} * r_0}{2} \right) * (g_{m10} + g_{m11}) \right]} \quad (3.12)$$

where,

$$r_0 = r_{04} || r_{06} \quad (3.13)$$

r_{010} and r_{011} are the output impedances of transistors M10 and M11. G_{mx} is the the equivalent trans-conductance of the QFGMOS, g_{m10} and g_{m11} are the trans-conductance of M10 and M11 and r_0 is the equivalent output resistance of M4 and M6. G_{mx} is the equivalent trans-conductance given by the product of the ratio of capacitance C_1 and total capacitance C_T , trans-conductance of the conventional MOSFET M3 used in figure 3.2 and the sum of the trans conductance of transistors M10 and M11 .

The output impedance and resistance at node Y are similar to the proposed circuit in section 3.2. The circuit provides wide bandwidth, rail to rail dynamic range and low parasitic impedance at the input.

CHAPTER 4

SIMULATIONS AND RESULTS

In this chapter, the simulation results of dual output differential pair second generation current conveyor (DODCCII) and QFGMOS based dual output second generation current conveyor (QFGDODCCII) has been presented. The circuits are simulated using BSIM3V3 0.18 μm in Cadence design environment. The biasing current and supply voltage used for the circuits are 28 μA and $\pm 0.7\text{V}$ respectively. The chapter is organized as follows. In section 4.1, the simulation results of the DODCCII have been discussed. Section 4.2 presents the simulation results of QFGDODCCII. The layout of DODCCII is presented in section 4.3.

4.1 Simulation Results of Dual Output Differential Pair Second Generation Current Conveyor (DODCCII)

Various simulations are carried out to obtain the d.c and a.c characteristics of the DODCCII circuit. The d.c analysis of the DODCCII is shown in Figure 4.1. A good dynamic range of the output voltage from -650mV to 595mV is obtained which means in this range output voltage follows input voltage exactly. The variation of output current at two different nodes of DODCCII namely Z- and Z+ with input current is shown in Figure 4.2 and Figure 4.3 respectively. In Figure 4.2, at port Z-, the output current decreases with increase in the input current and in Figure 4.3, the output current at port Z+ increases with increase in input current. The d.c characteristics of current reveal that dynamic range is -130 μA to 130 μA for both ports Z- and Z+.

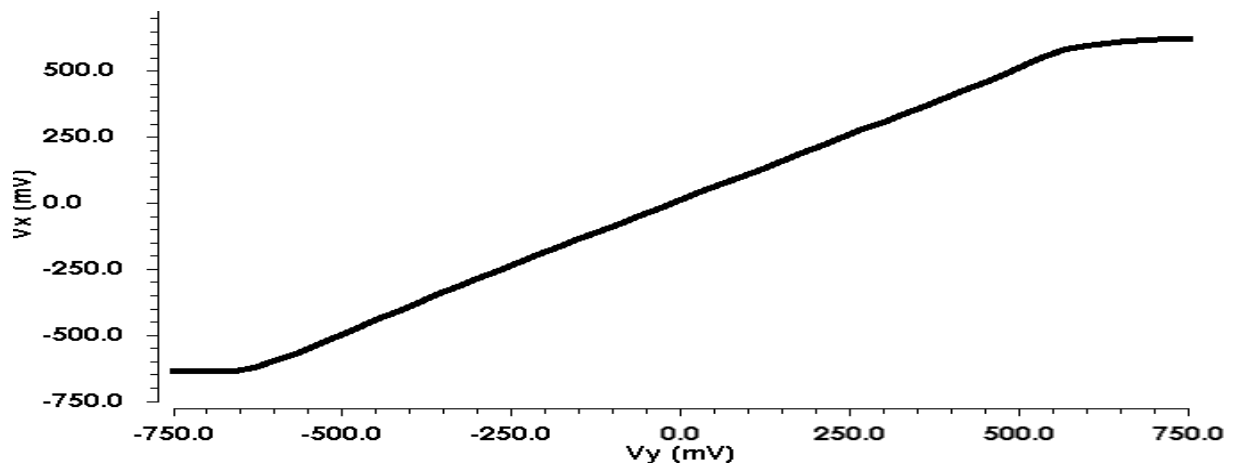


Figure 4.1 D.C Voltage Characteristics of DODCCII

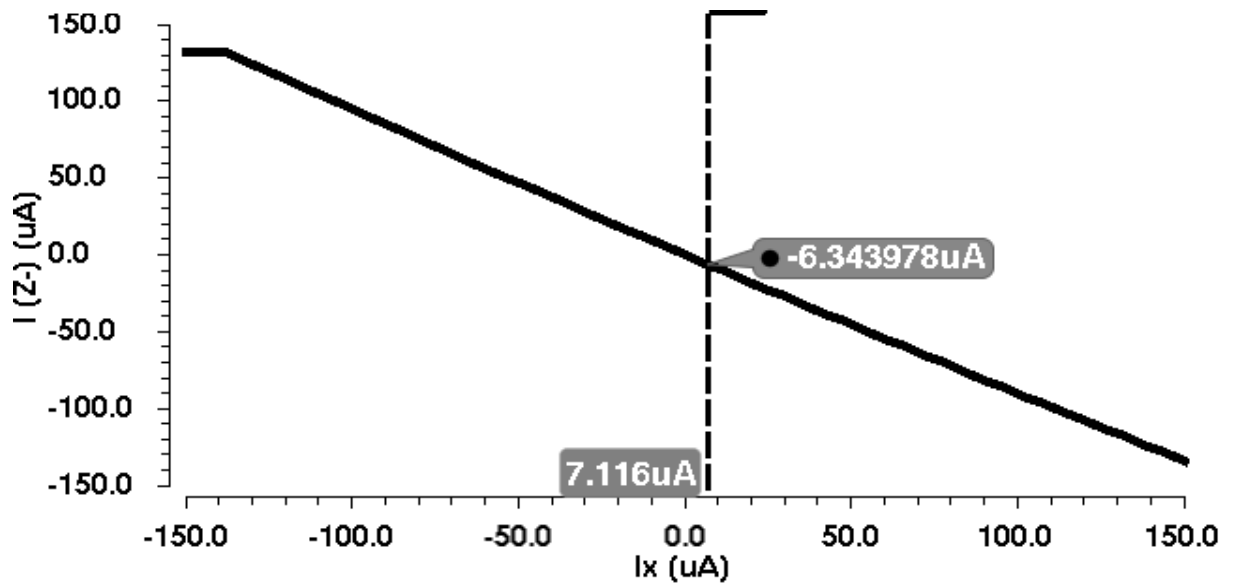


Figure 4.2 D.C Current Characteristics of DODCCII at Port Z-

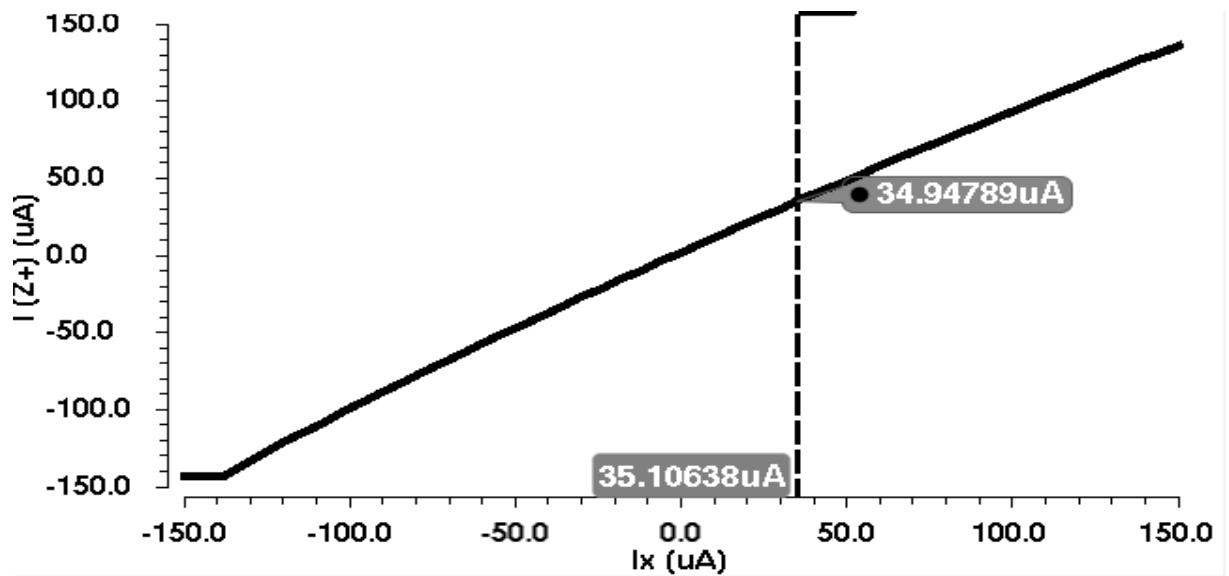


Figure 4.3 D.C Current Characteristics of DODCCII at Port Z+

The a.c analysis has been performed by applying a.c magnitude of 200mVp-p at 1KHz. The input is applied to obtain the voltage gain and voltage transfer bandwidth of the circuit. The frequency response of DODCCII is shown in Figure 4.4. From the figure, it can be seen that the voltage gain and the voltage transfer bandwidth are 83.38mdB (1.009) and 3.09GHz respectively.

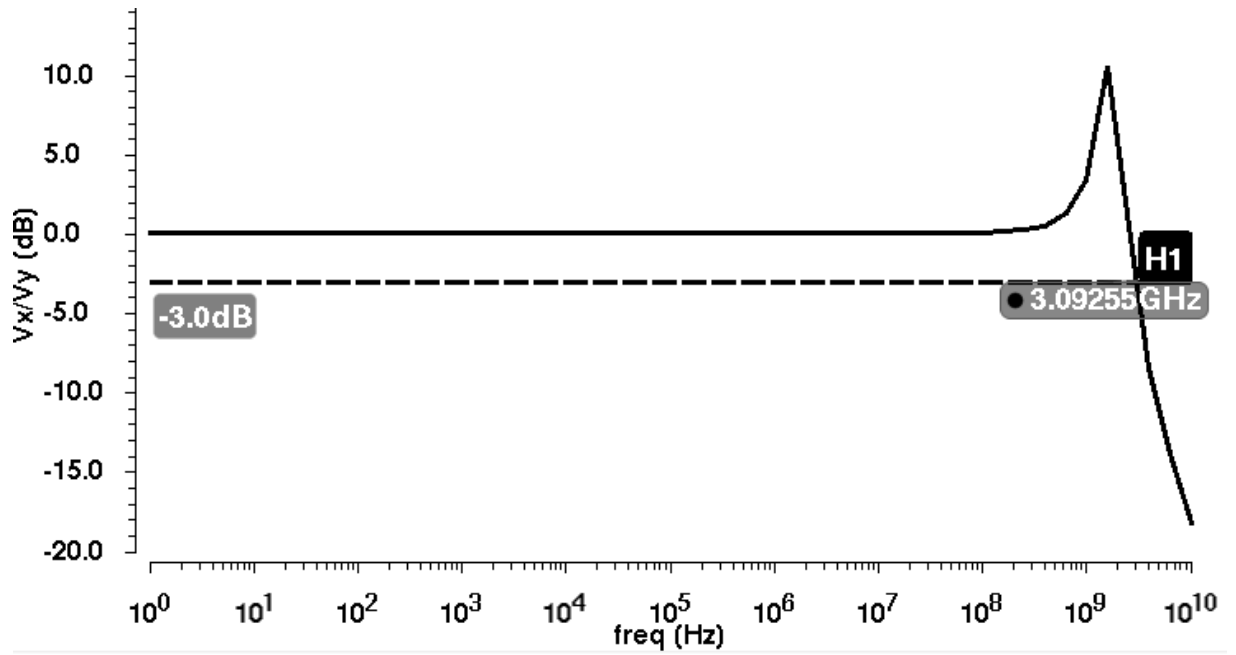


Figure 4.4 Voltage Transfer Bandwidth of DODCCII

To obtain the current gain and current transfer bandwidth at nodes Z- and Z+, the input current of $20\mu\text{A}_{\text{p-p}}$ at 1KHz has been applied. The frequency responses of DODCCII at nodes Z- and Z+ are shown in Figures 4.5 and 4.6 respectively. From the Figure 4.5, it is evident that the current gain and current transfer bandwidth are 389 mdB (1.04) and 2.86GHz respectively.

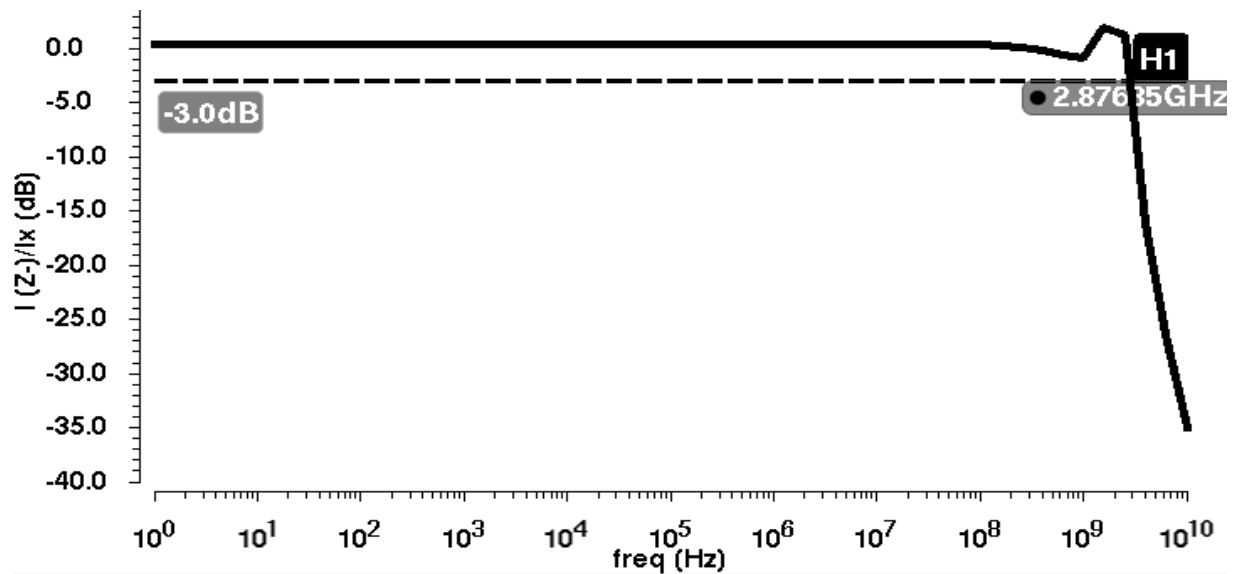


Figure4.5 Current Transfer Bandwidth at Port Z- of DODCCII

It is clear that in Figure 4.6, the current gain and current transfer bandwidth are 115mdB (1.01) and 2.63GHz respectively.

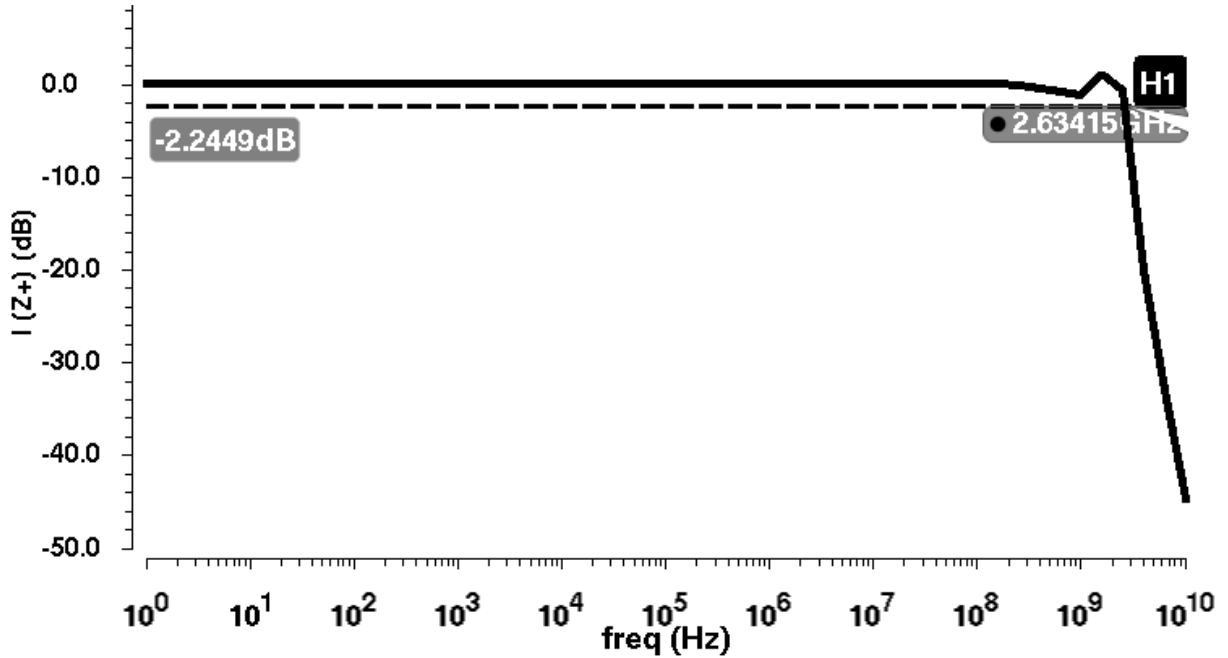


Figure4.6 Current Transfer Bandwidth at Port Z+ of DODCCII

The DODCCII offers parasitic input impedance of 65.67Ω at port X and an output impedance of $45.8K\Omega$ at port Z. The impedance at node Y is approximately infinite. The power consumption of the DODCCII is $451\mu W$.

4.2 Simulation Results of QFGDODCCII

The QFGMOS used in the design has capacitors C1 and C2 whose values are maintained so as to have constant RC for all the QFGMOS. The values of capacitors are chosen as 35fF and 70fF respectively. The resistances R1 and R2 are used to get the d.c characteristics as capacitors block d.c which has the values of $20G\Omega$ and $10G\Omega$ respectively. The input voltage at node X is passed through parallel combination of resistor R1 and capacitor C1 whereas a biasing voltage source is applied at the parallel combination of R2 and C2 which helps in lowering the threshold voltage of the QFGMOS.

The d.c characteristics of QFGDODCCII are shown in Figure 4.7. The circuit has dynamic range rail to rail from -0.7V to +0.7V which means output voltage follows input voltage exactly.

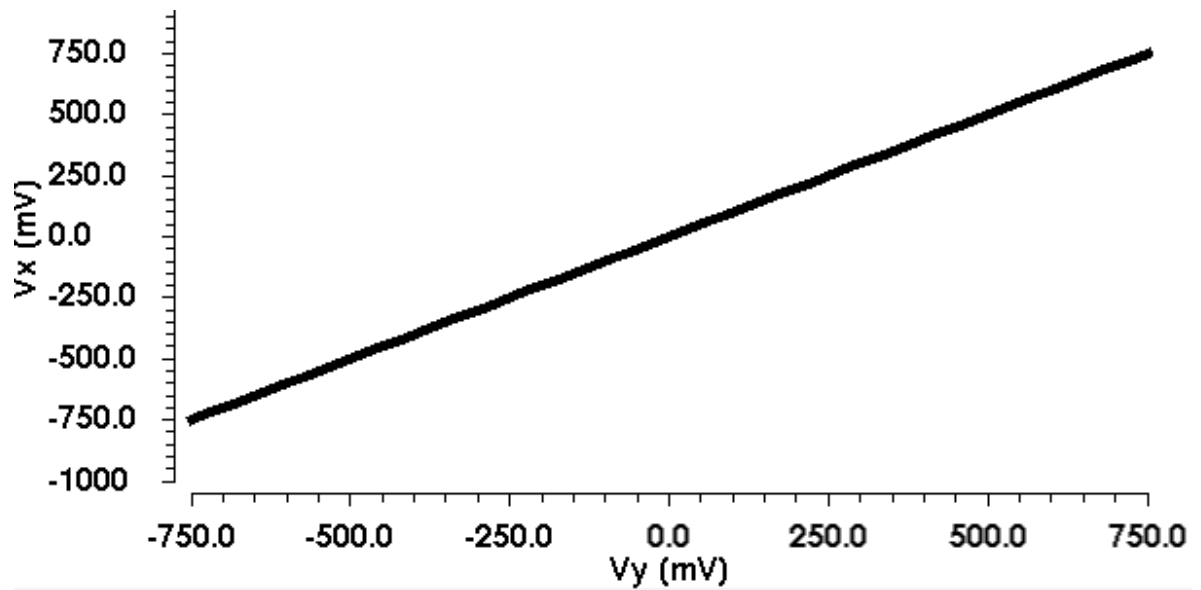


Figure 4.7 Variation of Output Voltage with respect to the Input of QFGDODCCII

The output current varies with input current at two different nodes namely Z- and Z+ shown in Figure 4.8 and 4.9, respectively. The d.c characteristics of current reveal that dynamic range is -200 μ A to +200 μ A for both ports Z- and Z+.

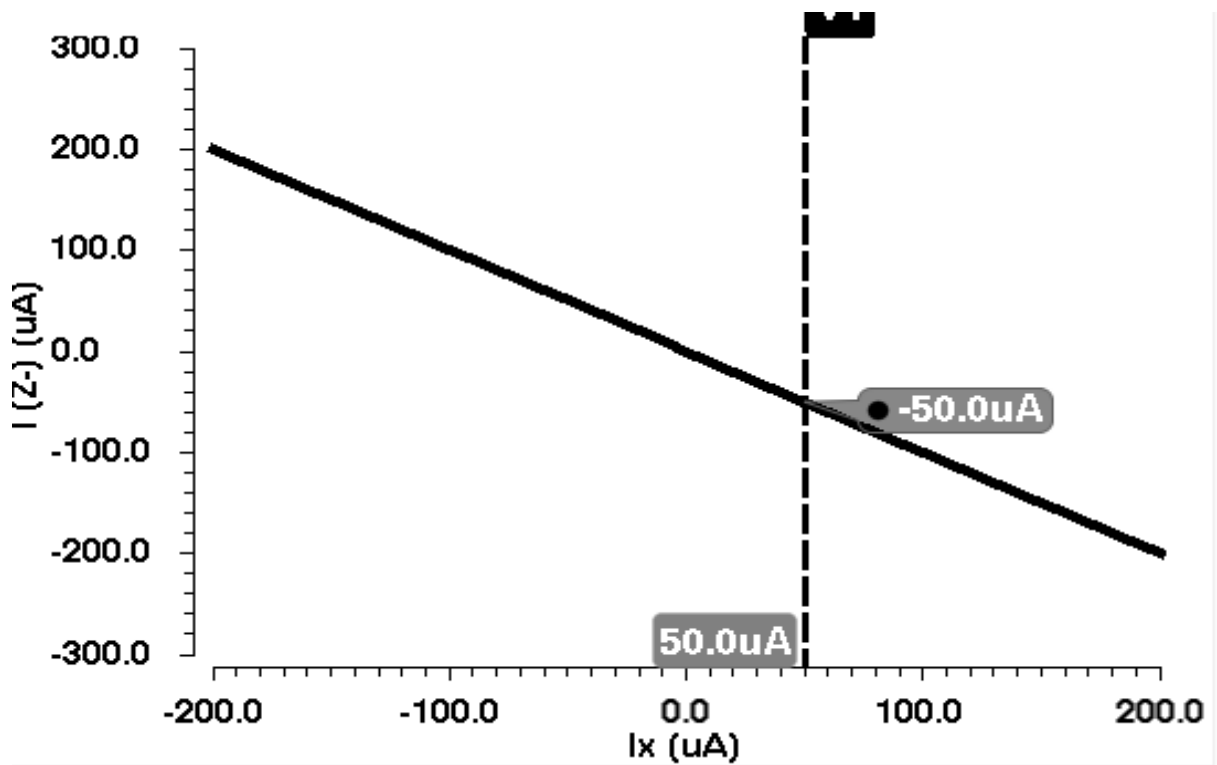


Figure 4.8 Variation of Output Current with Input Current at Port Z-

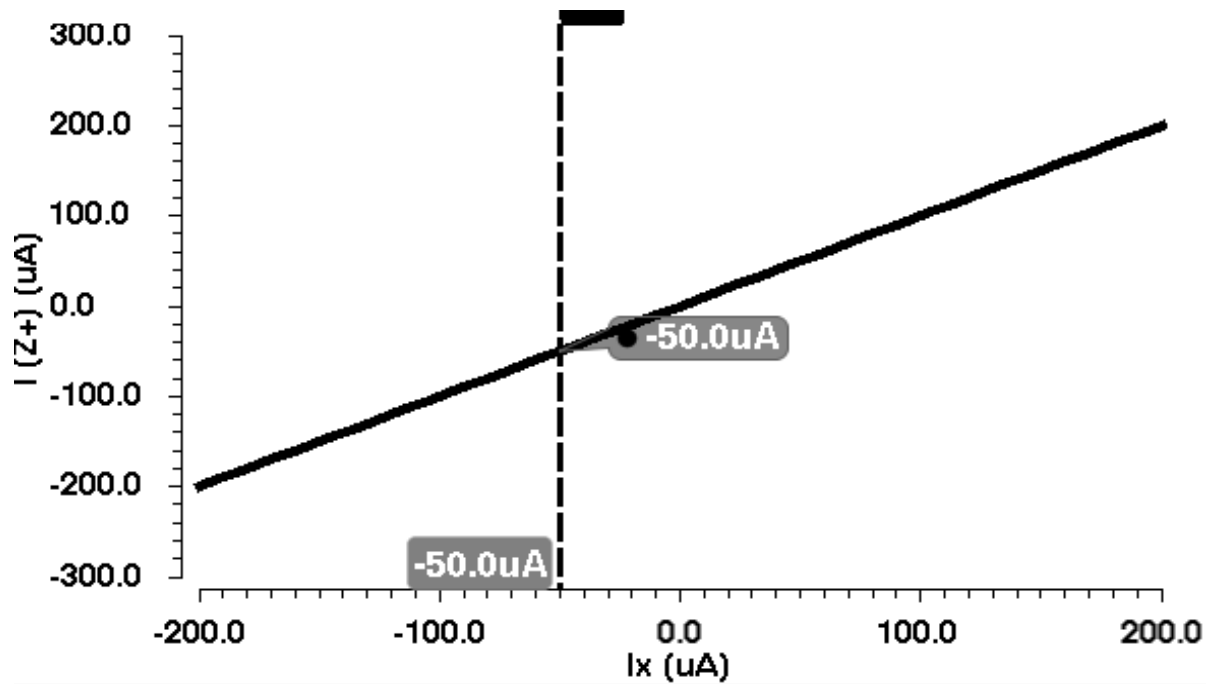


Figure 4.9 Variation of Output Current with Input Current at Port Z-

The a.c analysis has been performed by applying a.c magnitude of 200mVp-p at 1 KHz and from Figure 4.10 the voltage gain and voltage transfer bandwidth are obtained as 812mdB (1.09) and 2.67GHz respectively.

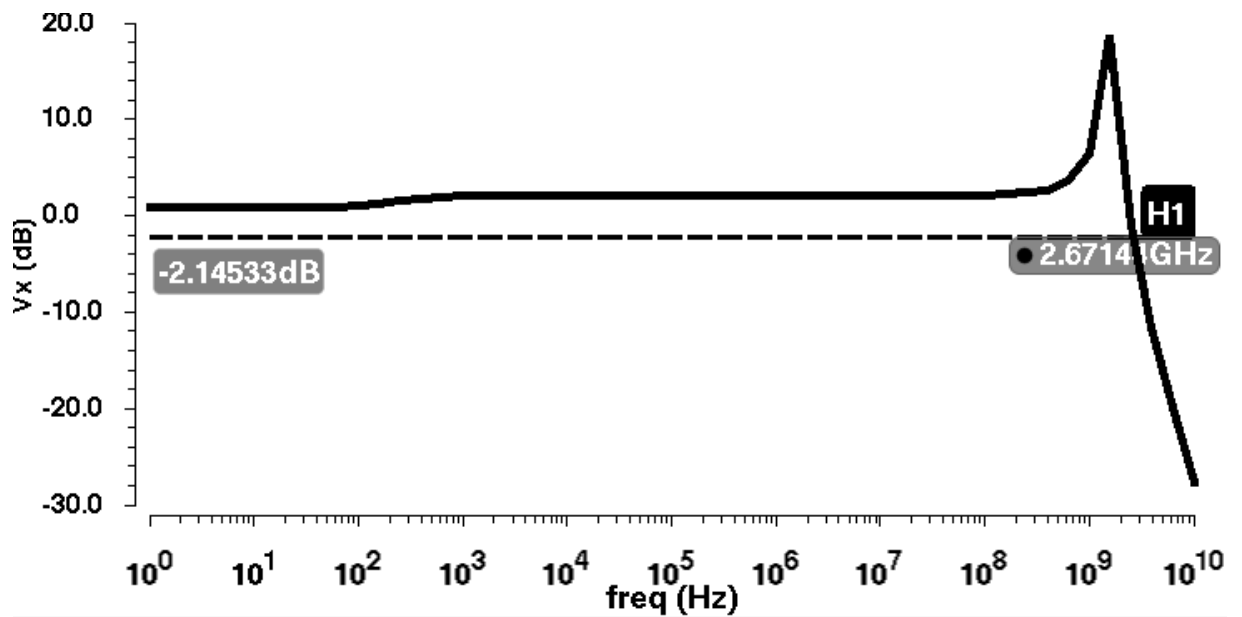


Figure 4.10 Voltage Transfer Bandwidth of QFGDODCCII

To obtain the current gain and current transfer bandwidth at nodes Z- and Z+, the input current of 20 μ A_{p-p} has been applied at 1KHz. The frequency response of QFGDODCCII is shown in Figure 4.11 and 4.12 respectively.

From Figure 4.11 it is clear that current gain and current transfer bandwidth is 73.7mdB (1.00) and 2.54GHz respectively at node Z-.

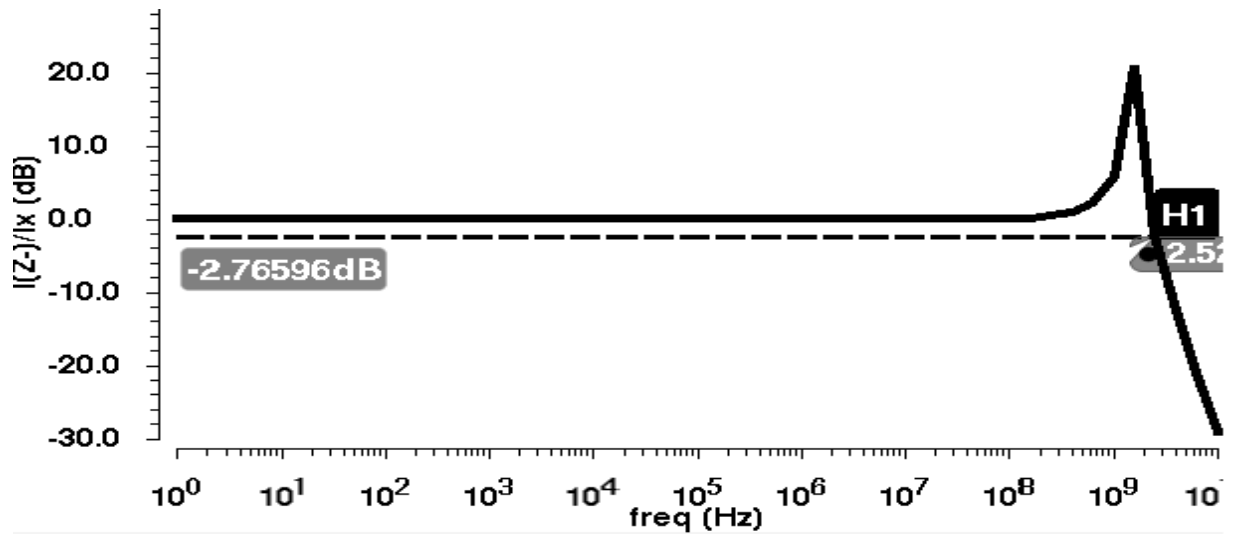


Figure 4.11 Current Transfer Bandwidth of QFGDODCCII at port Z-

From Figure 4.12, it is evident that the current gain and the current transfer bandwidth at node Z+ are 106 mdB (1.01) and 2.45GHz respectively.

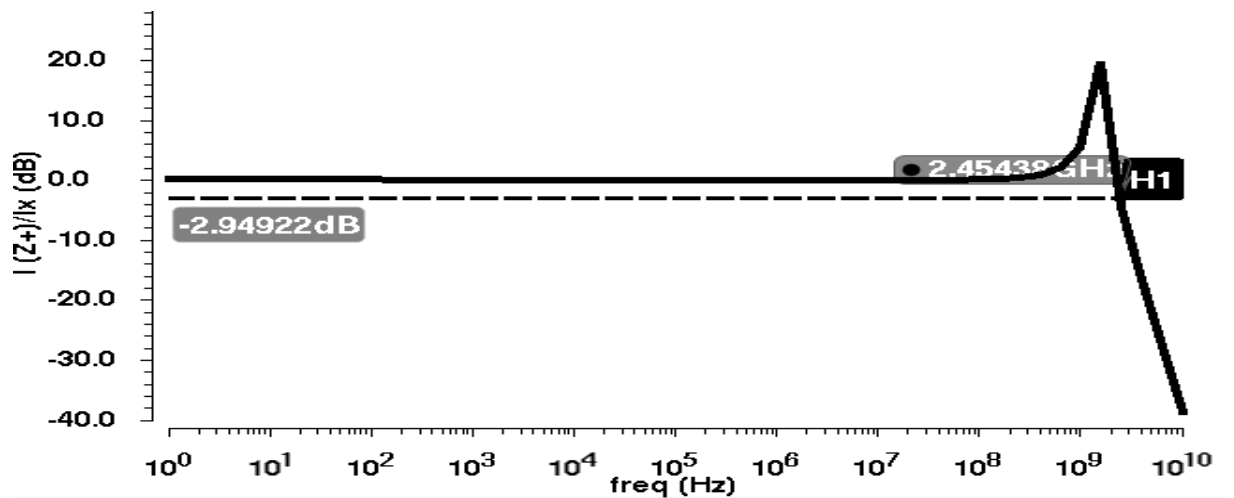


Figure 4.12 Current Transfer Bandwidth of QFGDODCCII at port Z+

The QFGMOS-DODCCII has the lowest input impedance of 8.53Ω which is required for functioning in high frequency applications effectively. The circuit has infinite impedance at the input node Y and also has a high output impedance of 45.3Ω . In Table 4.1 DODCCII and QFGDODCCII are compared with the reported work and it has been found that both the circuits have high output impedance, high current and voltage gains, high voltage and current transfer bandwidths and operate at low supply voltage. The QFGDODCCII has rail to rail dynamic range of voltage and current. It has lowest parasitic input impedance.

Table 4.1: Comparison of the Proposed DODCCII and QFGMOS-DODCCII

Ref. No.	CMOS Technology	Supply Voltage	Voltage Transfer Bandwidth	Current Transfer Bandwidth	Voltage gain	Current gain	Output Dynamic Range	Power consumption	Rx	Ry	Rz
[25]	$0.35\mu\text{m}$	$V_{dd}= V_{ss} =1.5\text{V}$	NA/ suitable for cascading	-	Variable	Variable	-	$6600\mu\text{W}$	46Ω	$5.9\text{G}\Omega$	$73\text{M}\Omega$
[27]	$0.35\mu\text{m}$	$V_{dd}= V_{ss} =1.65\text{V}$	391MHz	-	0.9228	0.9957	-	-	43Ω	∞	$>75\text{K}\Omega$
[14]	$0.25\mu\text{m}$	$V_{dd}= V_{ss} =0.5\text{V}$	30MHz	480MHz	0.95	1	$-0.5\text{V}-0.5\text{V}$	$771\mu\text{W}$	13Ω	$1\text{E}20\Omega$	$2\text{K}\Omega$
[9]		$V_{dd}= V_{ss} =0.75\text{V}$	10.5MHz	-	1	1	-		13Ω	$>1\text{G}\Omega$	$2.6\text{M}\Omega$
[20]	$0.5\mu\text{m}$	$V_{dd}= V_{ss} =1.65\text{V}$	-	-	2		-	$99\mu\text{W}$	30Ω	-	-
[24]	$0.6\mu\text{m}$	5V	223KHz	115KHz	48dB	51dB	$0.5\text{V}-3.5\text{V}$	-	-	-	-
[17]	$0.5\mu\text{m}$	1.5V	100MHz	-	1.8	1.1	-	$105\mu\text{W}$	$14\text{K}\Omega$	$7\text{M}\Omega$	$15\text{K}\Omega$
[28]	$0.5\mu\text{m}$	$V_{dd}= V_{ss} =2.5\text{V}$	-	-	Variable	Variable	-	-	$4.5\text{K}\Omega$	$490\text{M}\Omega$	$41.75\text{K}\Omega$
[18]	$0.35\mu\text{m}$	$V_{dd}= V_{ss} =1.5\text{V}$	57.2MHz	-	0.994	-	$-320\text{mV}-+360\text{mV}$	$19.5\mu\text{W}$	54Ω	$5\text{M}\Omega$	$4.1\text{M}\Omega$
[1]	$0.18\mu\text{m}$	$V_{dd}= V_{ss} =0.7\text{V}$	2.686GHz	2.667GHz	0.998	0.967	$650\text{mV}-550\text{mV}$	$270\mu\text{W}$	-	∞	-
[21]	$0.18\mu\text{m}$	$V_{dd}= V_{ss} =0.75\text{V}$	3GHz	2.96GHz	1	1	$-0.75\text{V}-+0.75\text{V}/-220\mu\text{A}-+220\mu\text{A}$	$230\mu\text{W}$	8.26Ω	∞	$46.5\text{K}\Omega$
Proposed DODCCII	$0.18\mu\text{m}$	$V_{dd}=V_{ss}=0.7\text{V}$	3.092GHz	$2.876\text{GHz}(\text{Z-})$ $2.631\text{GHz}(\text{Z+})$	1.009	$1.04(\text{Z-})$ $1.01(\text{Z+})$	$-650\text{mV}-595\text{mV}-130\mu\text{A}-130\mu\text{A}$	$300\mu\text{W}(\text{single})$ $451\mu\text{W}(\text{dual})$	65.67Ω	∞	$45.8\text{K}\Omega$
Proposed QFGMOS-DODCCII	$0.18\mu\text{m}$	$V_{dd}= V_{ss} =0.7\text{V}$	2.67GHz	$2.523\text{GHz}(\text{Z-})$ $2.456\text{GHz}(\text{Z+})$	1.09	$1.00(\text{Z-})$ $1.01(\text{Z+})$	$-700\text{mV}-700\text{mV}-200\mu\text{A}-+200\mu\text{A}$	$121\mu\text{W}(\text{single})$ $359.5\mu\text{W}(\text{dual})$	8.53Ω	∞	$45.3\text{K}\Omega$

4.3 Layout of Dual Output Differential Pair Second Generation Current Conveyor (DODCCII)

The layout of the second generation current conveyor is shown in Figure 4.13. The layout has the same pins as the schematic and the transistors also have the same size as that of the schematic.

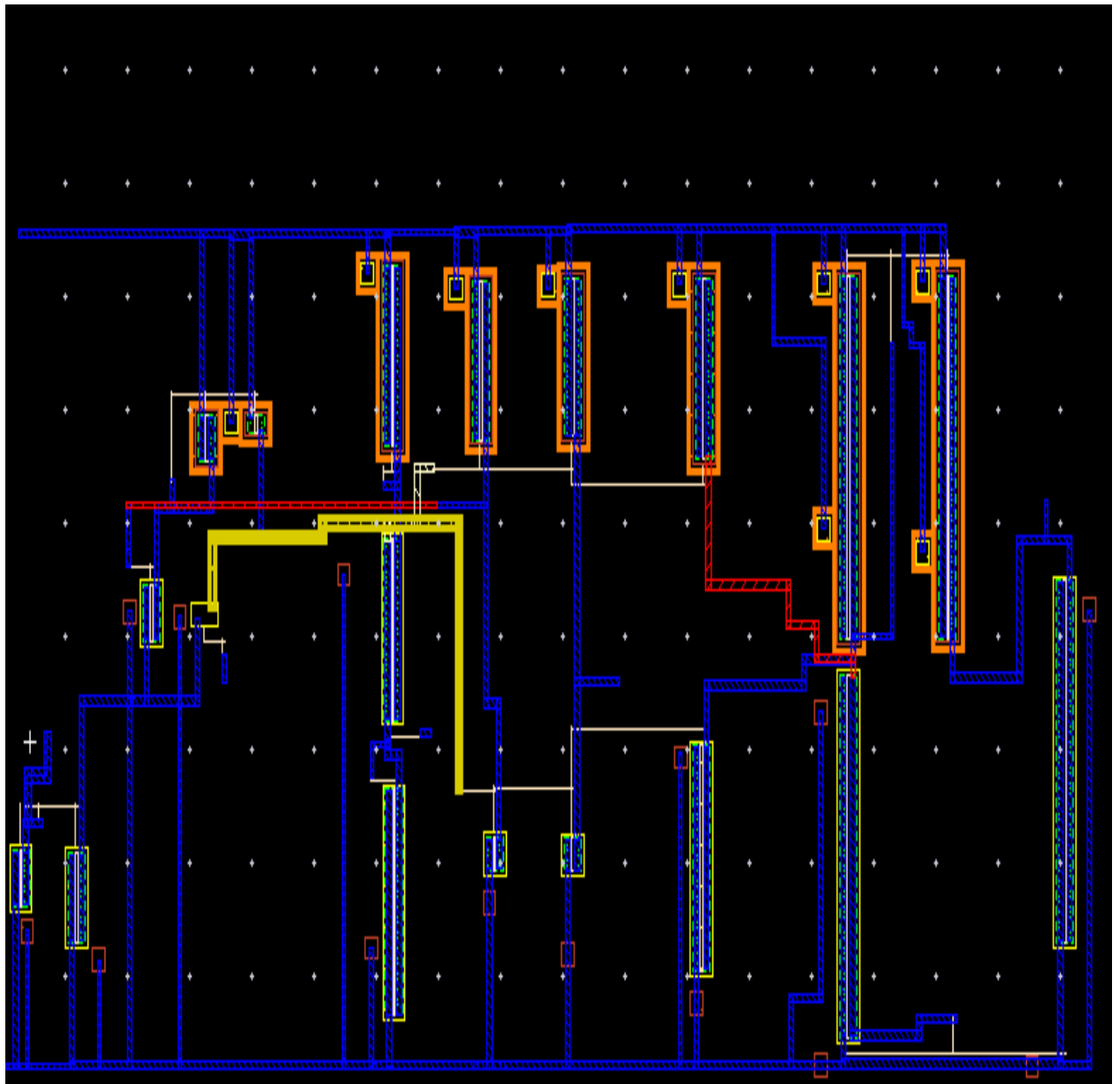


Figure 4.13 Layout of DODCCII

The layout is made up by considering the various design rules so as to have it free from any design rule check (DRC) errors. The various design rules are summarized below in Table 4.2.

Table 4.2 Design Rules for Layout in Virtuoso 180nm Technology

Metal to Metal Spacing	>0.3 μm
Metal to Poly Spacing	>10.0 μm
Poly to Poly Spacing	>10.0 μm
P+SD to NWell Tap Spacing	<25.0 μm
N+SD to PWell Tap Spacing	<25.0 μm

The DRC is run to verify that there is no violation of design rules in the layout of DODCCII. The Figure 4.14 shows that the circuit is free from DRC errors. The DRC report is shown in Figure 4.15 which shows the total errors in the designing of layout which are found to be zero.

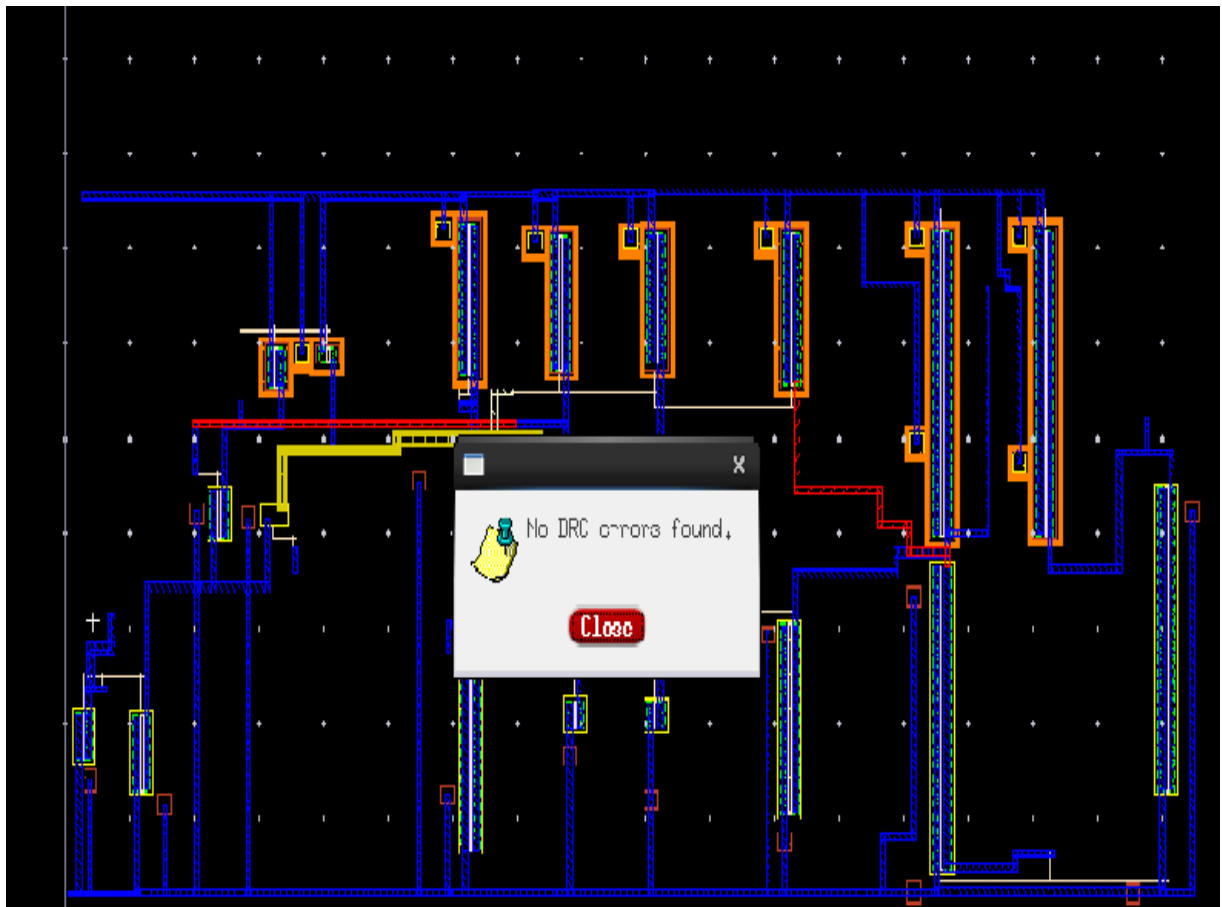


Figure 4.14 DRC Error Free Layout of DODCCII

File Edit Help			
(204)	8C: Metal1 to Via1 enclosure must be >=	0	0
(205)	10B: Via2 to Via2 spacing must be >= 0.3	0	0
(206)	10A: Via2 shapes must be 0.2x0.2 rectang	0	0
(207)	10C: Metal2 to Via2 enclosure must be >=	0	0
(208)	10C: Metal2 to Via2 enclosure must be >=	0	0
(209)	14B: Via3 to Via3 spacing must be >= 0.3	0	0
(210)	14A: Via3 shapes must be 0.2x0.2 rectang	0	0
(211)	14C: Metal3 to Via3 enclosure must be >=	0	0
(212)	14C: Metal3 to Via3 enclosure must be >=	0	0
(213)	16B: Via4 to Via4 spacing must be >= 0.3	0	0
(214)	16A: Via4 shapes must be 0.2x0.2 rectang	0	0
(215)	16C: Metal4 to Via4 enclosure must be >=	0	0
(216)	16C: Metal4 to Via4 enclosure must be >=	0	0
(217)	18B: Via5 to Via5 spacing must be >= 0.3	0	0
(218)	18A: Via5 shapes must be 0.2x0.2 rectang	0	0
(219)	18C: Metal5 to Via5 enclosure must be >=	0	0
(220)	18C: Metal5 to Via5 enclosure must be >=	0	0
(221)	12D: CapMetal to Metal3 enclosure must b	0	0
(222)	12A: CapMetal width must be >= 0.5 um	0	0
(223)	12B: Metal2 to Via2Cap enclosure must be	0	0
(224)	12B: Metal2 to Via2Cap enclosure must be	0	0
(225)	12C: CapMetal to Via2Cap enclosure must	0	0
(226)	12C: CapMetal to Via2Cap enclosure must	0	0
(227)	11D: Metal3 to Via2Cap enclosure must be	0	0
(228)	11D: Metal3 to Via2Cap enclosure must be	0	0
(229)	20C: Metal1 to Bondpad enclosure must be	0	0
(230)	20C: Metal1 to Bondpad enclosure must be	0	0
(231)	20D: Metal2 to Bondpad enclosure must be	0	0
(232)	20D: Metal2 to Bondpad enclosure must be	0	0
(233)	20E: Metal3 to Bondpad enclosure must be	0	0
(234)	20E: Metal3 to Bondpad enclosure must be	0	0
(235)	20F: Metal4 to Bondpad enclosure must be	0	0
(236)	20F: Metal4 to Bondpad enclosure must be	0	0
(237)	20G: Metal5 to Bondpad enclosure must be	0	0
(238)	20G: Metal5 to Bondpad enclosure must be	0	0
(239)	20H: Metal6 to Bondpad enclosure must be	0	0
(240)	20H: Metal6 to Bondpad enclosure must be	0	0
(241)	20A: Minimum Pad width = 45.0	0	0
(242)	20B: Minimum Pad spacing to Pad = 10.0	0	0
(243)	13A1: P+SD to NW tap spacing must be <=	0	0
(244)	13A2: N+SD to Iso Psub tap spacing must	0	0
(245)	13A3: N+SD to Psub tap spacing must be <	0	0
(246)	13A3: N+SD to PW tap spacing must be <=	0	0
Total errors:		0	0

Figure 4.15 DRC report for error free DODCCII

CHAPTER 5

CONCLUSION AND FUTURE SCOPE

5.1 Conclusion

Current Conveyors are beneficial analog blocks for achieving low voltage, low power operation with advantages of high dynamic range and high frequency response. CCII is the widely used conveyor across various current and voltage processing applications. In the work, DODCCII and QFGDODCCII are designed which gives various advantages in terms of performance parameters. Both the circuits have low supply voltage requirement, high frequency response, high voltage and current gain, high output impedance and low power consumption. The QFGMOS based DODCCII gives additional advantage of rail to rail dynamic range and very low parasitic input impedance. Moreover, it eliminates the use of d.c current source and current mirror load of differential pair. The circuits can be used for various analog high frequency applications

5.2 Future Scope

The work presented in thesis uses QFGMOS as the differential inputs for rail to rail dynamic range, low input impedance and low supply voltage requirement. The QFGDODCCII is dual output which works as CCII- as well as CCII+. The circuit can be further used to increase the dynamic range even beyond the supply voltage. The QFGDODCCII can be used in designing of various tunable multifunction filters such as low pass, high pass, all pass and band pass filters. The circuits can be used for making oscillator circuits so as to have low power consumption with increased gain, bandwidth, dynamic range and low supply voltage requirement. The bandwidth can be increased to further extent by using various bandwidth enhancement techniques along with low power consumption and low supply voltage. Also, various optimization techniques by using the optimization algorithms can prove beneficial to reduce the parasitic input impedance and increase the frequency response by optimizing the widths and lengths of the transistors.

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