Design and Analysis of High Performance Voltage Reference Circuits

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CERTIFICATE

I, **Arvind Thakur**, hereby certify that the research work presented in the thesis entitled "**Design and Analysis of High Performance Voltage Reference Circuits**" being submitted by me with **Registration No. 901706028** to the Department of Electronics and Communication Engineering, Thapar Institute of Engineering and Technology, Patiala, India in the fulfilment of the requirements for the award of the degree of **"Doctor of Philosophy"**. It is an authentic record of bonafide research work carried out under the guidance and supervision of ***Assistant Professor (Dr.) Rishikesh Pandey, ECED, TIET, Patiala*** and ***Assistant Professor (Dr.) Shireesh Kumar Rai, ECED, TIET, Patiala***.

The matter presented in this has not been submitted either in part or full to any other university or institute for the award of any other degree.

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ARVIND THAKUR

DEDICATED TO MY

FAMILY

&

FRIENDS

ABSTRACT

Nowadays, low-voltage and low-power integrated circuits (ICs) are gaining importance due to the increased demand for portable electronic systems like hearing aids, music players, digital cameras, laptops, mobile phones, etc. An essential part of analog and mixed-signal circuits designing is the realization of reliable and precise voltage references. A voltage reference in an entire circuit establishes a stable reference point which is used by other sub-circuits to generate predictable and repeatable results. This reference point mustn't change significantly under various operating conditions. Therefore, the voltage reference should have a low-temperature coefficient, high power supply rejection ratio (PSRR), low supply voltage requirement, low power consumption, small occupied chip area, etc. to improve the performance of the entire circuit. But it is difficult to improve all the parameters simultaneously, and therefore, in the thesis four different CMOS voltage references namely, CMOS voltage reference-I, CMOS voltage reference-II, CMOS voltage reference-III, and CMOS voltage reference-IV are proposed to achieve optimum values of these performance parameters. The proposed voltage references have been simulated in 180 nm standard CMOS technology using Cadence virtuoso analog design environment and the simulation results of these proposed voltage references have been compared with the voltage references available in the literature.

The proposed CMOS voltage reference-I and CMOS voltage reference-II are based on the addition of proportional-to-absolute-temperature (PTAT) and complementary-to-absolute-temperature (CTAT) behaviours to generate their output reference voltages. The proposed CMOS voltage reference-I operating at a supply voltage of 0.85 V has a low temperature coefficient of 21.9 ppm/°C over a temperature range of -60 °C to 120 °C and a PSRR of -65.85 dB at 100 Hz. To improve the PSRR of the proposed CMOS voltage reference-I, another voltage reference named proposed voltage reference-II operating at a supply voltage of 0.8 V has been presented which offers a PSRR of -91.69 dB at 100 Hz and a temperature coefficient of 29.5 ppm/°C over a temperature range of -55 °C to 125 °C.

Generally, the PTAT behaviour generator circuits require a large number of transistors, and therefore, the voltage references which are based on the addition of PTAT and CTAT behaviours do not offer much improvement in terms of power consumption, and area. In view of this, CMOS voltage reference-III is proposed which uses only CTAT behaviours to generate its output reference voltage. The proposed CMOS voltage reference-III operating at a supply voltage of 0.8 V, consumes low power of 2.75 µW and occupies a small area of 0.0027 mm^2. The proposed

CMOS voltage reference-III has a temperature coefficient of 38.85 ppm/°C over a temperature range of -40 °C to 125 °C and PSRR of -80.84 dB. To further improve the performance parameters such as supply voltage requirement, temperature coefficient, and PSRR of the CMOS voltage reference-III, another voltage reference named CMOS voltage reference-IV has been proposed. The proposed CMOS voltage reference-IV operating at a low supply voltage of 0.65 V, also uses only CTAT behaviours to generate its output reference. The proposed voltage reference-IV has a low power consumption of 1.95 µW, a temperature coefficient of 31.5 ppm/°C over a temperature range of -55 °C to 125 °C, and a PSRR of -85.4 dB.

To validate the performances of the proposed voltage references, these voltage references have been employed in the conventional LDO and it is observed that the LDOs based on proposed voltage references show improved PSRR, load regulation, temperature coefficient, and line sensitivity than the LDO based on a conventional voltage reference.

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LIST OF ABBREVIATIONS

BJT	Bipolar junction transistor
CCG	CTAT currents generator
CMOS	Complementary metal-oxide-semiconductor
CTAT	Complementary-to-absolute-temperature
EA	Error amplifier
FOM	Figure of merit
IC	Integrated circuit
KCL	Kirchoff's current law
LDO	Low dropout voltage regulator
MOSFET	Metal oxide semiconductor field-effect transistor
NMOS	N-type metal-oxide-semiconductor
OP -AMP	Operational amplifier
PMOS	P-type metal-oxide-semiconductor
PSRR	Power supply rejection ratio
PTAT	Proportional-to-absolute-temperature
PVT	Process, supply voltage and temperature
SICG	Supply independent CTAT generator
SIFTCVR	Supply independent first-order temperature-compensated voltage references
TC	Temperature coefficient
VLSI	Very large-scale ntegration

CHAPTER 1
INTRODUCTION

1.1 Introduction

The growing demand for portable and miniaturized electronic products in today's market has shifted the attention of researchers towards low-voltage and low-power system-on-chip applications. Due to the increased packing density of integrated circuits (ICs), the electric field and power consumption per unit area in the ICs increase with the scaling down of the feature size of the semiconductor devices. This leads to the degradation in the overall performance of an IC as electromigration and package-related failure can occur. Hence, low-voltage and low-power ICs must be developed to resolve the expected issues caused by device downscaling. This inherent trend towards low-voltage and low-power ICs is not only due to the aforementioned technology constraints, but also to extend the battery life. The low-voltage and low-power ICs are in higher demand for a wide range of applications, from small biomedical systems such as hearing aids to bigger and more sophisticated devices like music players, digital cameras, laptops, and mobile phones. These ICs consist of analog and mixed-signal circuits, where different blocks having specific functions are integrated to obtain a specific function [1-2]. A voltage reference is one of the important building blocks of analog, and mixed-signal circuits which provides constant output voltage with variations in process, supply voltage, temperature, etc. [3-4]. A few applications in which voltage references are the key elements are digital-to-analog converters, analog-to-digital converters, and low drop-out regulators [5-11]. In the literature, different methods have been used to generate the output reference voltage of the voltage reference circuit. First, the Zener and avalanche diodes were used to generate the output reference voltage [12]. Using some precautionary measures, the stable output reference voltage over a moderate range of temperature has been obtained [13].The breakdown mechanism and the voltage behaviour of these silicon junction diodes have been studied. But, these diodes require large bypass capacitors to remove the huge noise and consume more current. Due to these reasons, the Zener and avalanche diodes are not suitable to generate reference voltage for IC applications. This led to the development of voltage reference circuits, where temperature dependent voltages are explored and analysed to generate the reference voltage. In these circuits, two different voltage behaviours, namely the complementary-to-absolute-temperature (CTAT) and proportional-to-absolute-temperature (PTAT), are generated using the base-to-emitter voltages of the forward-biased bipolar junction transistors (BJTs). Using the addition of these

different temperature behaviours, the temperature-compensated voltage having ideally zero temperature coefficient is obtained at the output of the circuit. The concept of voltage reference was first suggested by D. F. Hilbiber [13] in 1964, but it became popular when R. J. Widlar introduced the basic bandgap voltage reference also called as Widlar circuit in 1971 [14]. After this, A. P. Brokaw introduced another topology of voltage reference in 1974 which is also known as Brokaw bandgap [15]. Earlier, these voltage references were also called bandgap reference circuits because they provide a constant output voltage around 1.26 V, which is nearly the same voltage as the bandgap of silicon at 0 K [16-18]. The generated voltage has better temperature stability than Zener diodes. In comparison to the Zener diode that consumes a large amount of current, the voltage reference circuit consumes less current and low power. Since the output voltage of BJT-based bandgap voltage reference is around 1.26 V, the minimum supply voltage requirement of the circuit approaches a higher value. But, for modern VLSI circuits, the values of supply voltage and reference voltage are too high especially for portable circuits, which are designed for biomedical and sensor network applications [19]. So, a typical approach is used in the voltage reference, which can be implemented by using the temperature characteristics of the gate-to-source voltages of the subthreshold MOS transistors. The PTAT behaviour is generated by the subtraction of two gate-to-source voltages of MOS transistors operating in the subthreshold regions while the CTAT behaviour is generated across the gate-to-source voltage of a MOS transistor operating in the subthreshold region. Using a subthreshold MOS transistor, the circuit generates a low output reference voltage with low supply voltage, low power consumption, and small chip area.

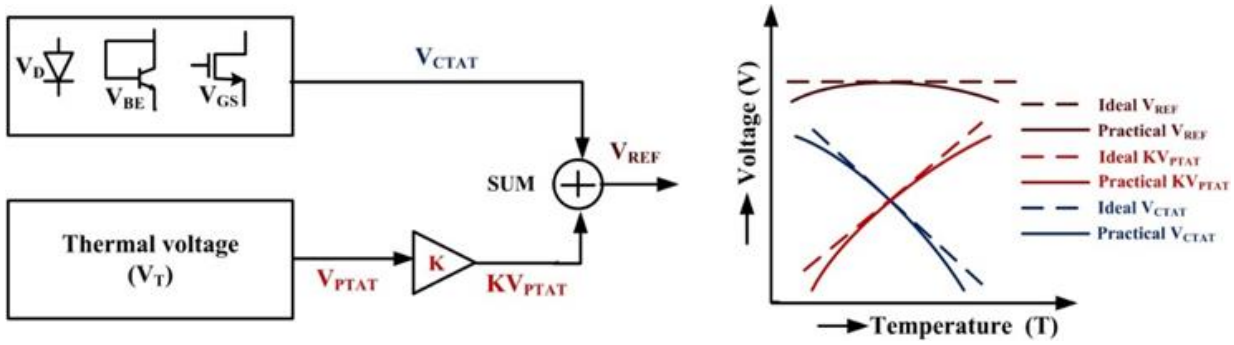
1.2 Voltage reference

The voltage reference is a circuit that can provide a temperature compensated output reference voltage by the addition of two opposite temperature behaviours of the voltages namely the proportional-to-absolute-temperature (PTAT) behaviour and complementary-to-absolute-temperature (CTAT) behaviour. Ideally, the constant output reference voltage is obtained but practically it has little variations with respect to temperature, process, supply voltage, etc.

The voltage references are classified into two different categories based on two conventional topologies [20]. The first topology is known as the voltage-mode topology, where voltages having opposite temperature dependencies are used to obtain the output reference voltage. The second topology is the current-mode topology in which currents having opposite temperature dependencies are used to obtain the output reference voltage.

1.2.1 Voltage-mode voltage reference

The basic concept used in voltage-mode voltage reference is shown in Figure 1.1(a) [21]. The effect of temperature variations on the reference voltage is mutually compensated by the addition of proportional-to-absolute-temperature voltage (V_{PTAT}) and complementary-to-absolute-temperature voltage (V_{CTAT}). Since voltages V_{PTAT} and V_{CTAT} have different slopes, the PTAT voltage is multiplied by a constant K in such a way that the temperature dependent terms of both the voltages are cancelled out and zero (ideally) temperature coefficient is achieved. The variations of voltages V_{PTAT}, $V_{CTAT,}$ and V_{REF} with temperature are shown in Figure 1.1(b) [21]. The dotted lines show ideal variations and the solid lines show practical variations of voltages with respect to temperature. It is shown that when the voltages V_{PTAT} and V_{CTAT} are added then ideally constant reference voltage (V_{REF}) is obtained but practically it has little variations with respect to temperature.



(a) (b)

Figure 1.1 (a) Basic concept of a voltage-mode voltage reference, (b) Variations of voltages V_{PTAT}, V_{CTAT}, and V_{REF} with temperature [21]

In the voltage-mode voltage reference, the CTAT and PTAT behaviours can be generated using MOS transistors operating in the subthreshold regions. The MOS transistor can operate in the subthreshold region when the applied gate-to-source voltage is less than the threshold voltage (V_{TH}). In this region, the drain-to-source current exhibits an exponential relationship [22] with the gate-to-source voltage (V_{GS}) and drain-to-source voltage (V_{DS}) which is expressed as

$$I_{DS}=\mu C_{ox}\frac{W}{L}(\eta-1)V_T^2\exp\left(\frac{V_{GS}-V_{TH}}{\eta V_T}\right)\left(1-\exp\left(-\frac{V_{DS}}{V_T}\right)\right) \quad (1.1)$$

where C_{ox} is the gate-oxide capacitance per unit area, η is the non-ideality factor, μ is the carrier mobility, V_{TH} is the threshold voltage and V_T is the thermal voltage.

If $V_{DS}>>4V_T$, the term $\left(1\text{-}\exp\left(-\frac{V_{DS}}{V_T}\right)\right)$ can be approximated as 1 and equation (1.1) reduces to

$$I_{DS}=\mu C_{ox}\frac{W}{L}(\eta\text{-}1)V_T^2\exp\left(\frac{V_{GS}\text{-}V_{TH}}{\eta V_T}\right) \tag{1.2}$$

Using equation (1.2), the gate-to-source voltage (V_{GS}) of MOS transistor is given as

$$V_{GS}=V_{TH}+\eta V_T\ln\left(\frac{I_{DS}}{\mu C_{ox}\frac{W}{L}(\eta\text{-}1)V_T^2}\right) \tag{1.3}$$

The threshold voltage (V_{TH}), mobility (μ), and thermal voltage (V_T) in terms of temperature [23] can be written as

$$V_{TH}(T)=V_{TH0}\text{-}k_T T \tag{1.4}$$

$$\mu(T)=\mu_0\left(\frac{T}{T_0}\right)^{-m} \tag{1.5}$$

$$V_T(T)=\frac{kT}{q} \tag{1.6}$$

where V_{TH0} is the threshold voltage at room temperature (T_o), k_T is a constant having value ranging from 0.5 to 3 mV/$^\circ$C, μ_o is the mobility at room temperature (T_o), parameter m is the mobility temperature exponent ($1\leq m\leq 2$), k is the Boltzmann constant, T is the absolute temperature and q is the electronic charge.

Substituting m=2 and using equations (1.4), (1.5) and (1.6) in equation (1.3), equation (1.3) is modified as

$$V_{GS}=V_{TH0}\text{-}k_T T+\eta\frac{kT}{q}\ln\left(\frac{I_{DS}LT_0{}^2q^2}{\mu_0 C_{ox}W(\eta\text{-}1)k^2}\right) \tag{1.7}$$

From equation (1.7), the derivative of gate-to-source voltage $\left(\frac{\partial V_{GS}}{\partial T}\right)$ can be written as

$$\frac{\partial V_{GS}}{\partial T}=\text{-}k_T+\frac{\eta k}{q}\ln\left(\frac{I_{DS}Lq^2}{\mu_0 T_0{}^2 C_{ox}W(\eta\text{-}1)k^2}\right) \tag{1.8}$$

Since $\frac{I_{DS}Lq^2}{\mu_0 T_0{}^2 C_{ox}W(\eta\text{-}1)k^2}<1$, both the terms of equation (1.8) are negative and hence, V_{GS} has a negative temperature coefficient as V_{GS} decreases with an increase in temperature [24]. Hence, the CTAT voltage (V_{CTAT}) using a MOS transistor operating in the subthreshold region can be expressed as

$$V_{CTAT}=V_{GS}=V_{TH}+\eta V_T\ln\left(\frac{I_{DS}}{\mu C_{ox}(W/L)(\eta\text{-}1)V_T^2}\right) \tag{1.9}$$

The PTAT voltage (V_{PTAT}) can be generated by the subtraction of two gate-to-source voltages of MOS transistors operating in the subthreshold regions. The V_{PTAT} can be expressed as

$$V_{PTAT}=\eta V_T \ln(N) \tag{1.10}$$

where N is the ratio of aspect ratios of MOS transistors used to generate PTAT voltage.

From equation (1.10), it is observed that the voltage V_{PTAT} is directly proportional to the thermal voltage which confirms its PTAT behaviour.

Hence, the output reference voltage V_{REF} can be expressed as

$$V_{REF}=V_{PTAT}+V_{CTAT}=\eta V_T \ln(N)+\left(V_{TH}+\eta V_T \ln\left(\frac{I_{DS}}{\mu C_{ox}(W/L)(\eta-1)V_T^2}\right)\right) \tag{1.11}$$

1.2.2 Current-mode voltage reference

The basic concept of current-mode voltage reference is shown in Figure 1.2 [25]. The two currents proportional-to-absolute-temperature current (I_{PTAT}) and complementary-to-absolute-temperature current (I_{CTAT}) having opposite temperature dependence are added to obtain a constant voltage V_{REF} across the resistor which is independent of temperature variations. From the figure, it can be observed that the currents I_{PTAT} and I_{CTAT} have different slopes therefore, I_{PTAT} is multiplied by a constant 'K' in such a way that the temperature dependent terms of both the currents are cancelled out and a reference current I_{REF} with zero (ideally) temperature coefficient is achieved. After that, a resistor is used at the output to convert the temperature compensated current I_{REF} into temperature compensated reference voltage.

In the current-mode voltage reference, the CTAT and PTAT behaviours can be generated using MOS transistors operating in the subthreshold regions. The MOS transistor can operate in the subthreshold region when the applied gate-to-source voltage (V_{GS}) is less than the threshold voltage (V_{TH}). The CTAT current (I_{CTAT}) generated by using a MOS transistor operating in the subthreshold region and a resistor (R) can be expressed as

$$I_{CTAT}=\frac{V_{GS}}{R}=\frac{V_{TH}+\eta V_T \ln\left(\frac{I_{DS}}{\mu C_{ox}(W/L)(\eta-1)V_T^2}\right)}{R} \tag{1.12}$$

The PTAT current (I_{PTAT}) can be generated by the subtraction of two gate-to-source voltages of MOS transistors operating in the subthreshold regions and a resistor (R). It can be expressed as

$$I_{PTAT}=\frac{\eta V_T}{R}\ln(N) \tag{1.13}$$

where N is the ratio of aspect ratios of MOS transistors used to generate the PTAT voltage.

The reference current (I_{REF}) is obtained as

$$I_{REF}=I_{PTAT}+I_{CTAT}=\frac{\eta V_T}{R}\ln(N)+\frac{V_{TH}+\eta V_T \ln\left(\frac{I_{DS}}{\mu C_{ox}(W/L)(\eta-1)V_T^2}\right)}{R} \quad (1.14)$$

Hence, the output reference voltage (V_{REF}) across the resistor (R_{REF}) is expressed as

$$V_{REF}=I_{REF}R_{REF}=\frac{R_{REF}}{R_1}\eta V_T \ln(N)+\frac{R_{REF}}{R_2}\left(V_{TH}+\eta V_T \ln\left(\frac{I_{DS}}{\mu C_{ox}(W/L)(\eta-1)V_T^2}\right)\right) \quad (1.15)$$

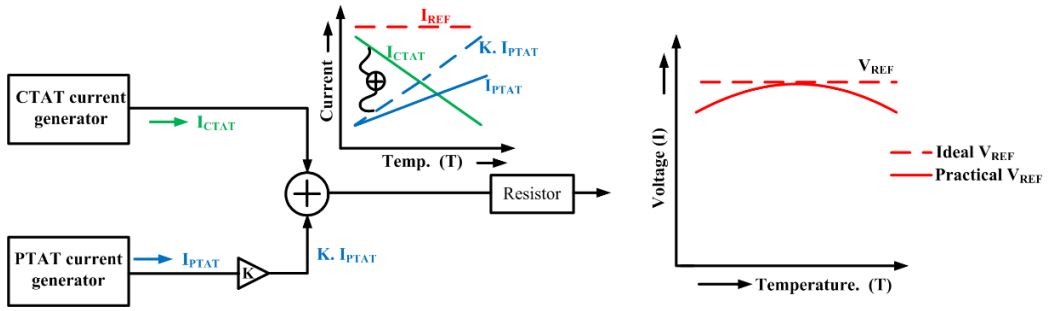


Figure 1.2 Basic concept of current-mode voltage reference [25]

1.2.3 Performance parameters of voltage reference

The characterization of a circuit is the best way to quantify its performance and to relate with similar circuits. In order to identify the accuracy and reliability of the voltage reference circuit, it should be measured in terms of different performance parameters such as temperature coefficient, line sensitivity, power supply rejection ratio (PSRR), and output noise [26]. The following sections provide formal definitions of each performance parameter of the voltage reference circuit.

1.2.3.1 Temperature coefficient

The temperature coefficient describes the change in the output reference voltage of the circuit over a given range of operating temperatures. The temperature coefficient is expressed in parts-per-million per degree Celsius (ppm/℃). The temperature coefficient is defined as

$$\text{Temperature coefficient}=\frac{\Delta V_{REF,\,V_{IN(nominal)}}(\Delta T)}{\Delta T \times V_{REF(nominal)}}10^6 \quad (\text{ppm/°C}) \quad (1.16)$$

where ΔT represents the variations of temperature, $V_{REF(nominal)}$ is the output reference voltage at nominal temperature and $\Delta V_{REF,V_{IN(nominal)}}(\Delta T)$ is the change in the reference voltage within the operating temperature range.

1.2.3.2 Line sensitivity

The line sensitivity is defined as a variation in the output voltage of the voltage reference circuit with respect to the input voltage variation at a nominal temperature. Line sensitivity is specified in μV/V or %/V with the following definition

$$\text{Line sensitivity} = \frac{\Delta V_{REF,T(nominal)}(\Delta V_{IN})}{\Delta V_{IN}} \quad (\mu V/V) \quad (1.17)$$

where $\Delta V_{REF,T(nominal)}(\Delta V_{IN})$ is the variation in the output voltage of the voltage reference circuit measured within input voltage variation in the range of $(V_{IN(min)}, V_{IN(max)})$ and $\Delta V_{IN} = V_{IN(max)} - V_{IN(min)}$.

1.2.3.3 Power supply rejection ratio

The power supply rejection ratio (PSRR) is the ability of the voltage reference circuit to reject the supply noise and other undesired signals on the power supply at a particular frequency. PSRR is a function of frequency specified in decibels (dB) with the following definition

$$PSRR = 20\log\frac{V_{REF,AC}(f)}{V_{IN,AC}(f)} \quad (dB) \quad (1.18)$$

where $V_{IN,AC}(f)$ is the power supply voltage affected by noise at a particular frequency f and $V_{REF,AC}(f)$ is the output reference voltage at the same frequency.

1.2.3.4 Output noise

The output noise is another frequency-dependent parameter that affects the performance of the voltage reference circuit. The noise is created by various physical phenomena and is due to random motion of electrons and holes. Output noise is specified by a graph of noise voltage spectral density versus frequency in $nV/\sqrt{Hz}$.

1.3 Motivation

The various analog and mixed-signal circuits such as low dropout regulators, DC-DC converters, digital to analog converters, analog to digital converters, phase-locked loop, and power converters require a reference voltage in their cores. But, the reference voltages are sensitive to the fabrication process, supply voltage, and temperature (PVT) variations which degrade the overall performance of the circuit. To improve the performance of the circuits, highly accurate voltage references with significantly less sensitivity to PVT variations are required. The reference voltage variation over the operating temperature range is known as temperature

coefficient, which is the most important performance parameter among all the performance parameters of a voltage reference, such as power supply rejection ratio (PSRR), line sensitivity, and output noise. In the MOS transistor, an electric field exists between the gate and the channel of the device, resulting in a leakage current from the gate to the channel. The leakage current is the main source of shot noise but this current is usually very small. For this reason, we can usually neglect shot noise during noise analysis. With the advancement in the VLSI industry over the past few decades, highly accurate voltage references which consume low power and occupy a small area are required. The low power supply is a critical parameter of the voltage reference as it also affects the power consumption of the system where voltage reference has been used. The voltage reference is also sensitive to the noise that is available in the supply voltage. Therefore, to make the voltage reference less prone to noise present in the supply voltage and other undesired signals, the voltage reference should have high PSRR over a wide frequency range. So, there is a need to design voltage references having high PSRR, low line sensitivity, low temperature sensitivity, low supply voltage, low power consumption, and small area. But, it is very difficult to achieve these goals simultaneously, and therefore, voltage reference needs to be investigated carefully to achieve an optimum value of these parameters.

1.4 Organization of thesis

The thesis consists of five chapters and the overview of all the chapters are as follows:

Chapter 1 presents a brief introduction of the voltage reference, working principle, and performance parameters. The chapter also addresses the motivation of the proposed work and the organization of the thesis.

In chapter 2, the literature survey of voltage references based on different topologies is presented. The identified research gaps and formulated objectives are discussed in the chapter. Finally, the research methodology followed to achieve the proposed objectives is also addressed.

Chapter 3 proposes four different structures of the voltage reference, namely CMOS voltage reference-I, CMOS voltage reference-II, CMOS voltage reference-III, and CMOS voltage reference-IV. The chapter includes the descriptions and analyses of the proposed circuits. The applications of the proposed voltage references as low dropout regulators have also been demonstrated.

In chapter 4, the physical layouts and post-layout simulation results of the proposed voltage references have been presented. The performance parameters of the proposed voltage references have been compared with the voltage references available in the literature to demonstrate the effectiveness of the proposed voltage references. The chapter addresses the simulation results of the low dropout regulators using proposed voltage references and conventional voltage reference (MOS version). The performances of the LDOs using proposed voltage references and conventional voltage reference (MOS version) have also been compared to show the workability of the proposed voltage references.

The conclusion of the research work is addressed in Chapter 5. The future work which can be done in this area has also been discussed in this chapter.

CHAPTER 2
LITERATURE SURVEY

The voltage references can be classified into two main categories: voltage-mode and current-mode voltage references [20]. This chapter discusses the research work carried out on the voltage references reported by various authors. A brief review based on the study is as follows.

2.1 Voltage-mode voltage references

The first temperature-compensated voltage reference is presented by R. J. Widlar in 1971 [14]. The circuit generates a temperature compensated output voltage by combining negative temperature coefficient and positive temperature coefficient voltages. The reported voltage reference offers advantages over the Zener diode voltage regulator as it increases the output current capability and reduces the requirement of external components to adjust the output voltage. The reported voltage reference circuit consisting of bipolar junction transistors (BJTs) is difficult to implement in the modern CMOS process as BJTs realized in the CMOS process are sensitive to the process variations.

A. P. Brokaw [15] presented a three-terminal IC bandgap reference to realize a stabilized bandgap voltage. The circuit uses two BJTs and collector current sensing to achieve the bandgap voltage. The circuit has a low temperature coefficient, high supply voltage requirement, and high power consumption.

M. Pan *et al.* [22] presented a voltage reference that works over a wide temperature range. The parallel transistors are used to remove the leakage problem and these transistors also improve the operating temperature range of the circuit. Low line sensitivity and high PSRR are achieved with the help of an operational amplifier. The limitations of the circuit are high temperature coefficient and large chip area.

K. E. Kuijik [27] proposed a voltage reference that generates temperature-compensated output voltage. In a conventional voltage reference, there is an error due to the voltage drift of the operational amplifier. The presented reference circuit overcomes the error of the conventional voltage reference by using an operational amplifier and an integrated circuit that consists of diode pairs, a low drift preamplifier, and an emitter follower. The circuit offers low noise and

high PSRR but the circuit has limitations of high supply voltage requirement and high power consumption.

G. C. M. Meijer *et al.* [28] suggested a curvature corrected voltage reference circuit. The curvature correction technique is used to reduce the non-linear temperature terms of the reference voltage. In the reported voltage reference circuit, the nonlinearity of base-to-emitter voltage with temperature has been compensated directly. The output voltage with low temperature dependency is obtained and the supply voltage variations are also stabilized in the circuit. The limited operating temperature range, high power consumption, and high supply voltage requirement are the main disadvantages of the circuit.

B. S. Song *et al.* [29] presented a high precision curvature compensated CMOS voltage reference circuit. The output reference voltage is obtained by the addition of linear temperature compensated PTAT voltage, quadratic temperature compensated PTAT voltage, and CTAT voltage. In order to minimize the temperature sensitivity, each compensated voltage is individually trimmed. The circuit has a high supply voltage requirement and high power consumption.

A. V. Staveren *et al.* [30] proposed a low supply voltage, low power second-order compensated voltage reference circuit. The second-order compensation is achieved by using two base-to-emitter voltages of different BJTs, where one of the BJTs is operated with PTAT current and another BJT is biased with a constant current. The circuit compensates additional temperature dependency of the output voltage due to the reverse early effect. The high supply voltage, high power consumption, and large area are the main disadvantages of the circuit.

A. E. Buck *et al.* [31] suggested a voltage reference without resistors. The circuit consists of diodes and MOS transistors operating in the strong inversion region. The proposed circuit has high power consumption and high temperature sensitivity.

K. N. Leung *et al.* [32] proposed a voltage reference based on the weighted difference of gate-to-source voltages of NMOS and PMOS transistors working in the saturation region. The circuit has high power consumption and high line sensitivity.

Y. Dai *et al.* [33] presented a voltage reference circuit that uses temperature dependence behaviours of PMOS and NMOS threshold voltages to generate a temperature-compensated

output reference voltage. These threshold voltages are insensitive to the supply voltage variations which improve the line sensitivity of the circuit. The supply voltage requirement and power consumption of the circuit are high.

A. Lahiri *et al.* [34] suggested voltage reference circuits that provide sub-1 V reference voltages. The reported circuits use the concept of reverse bandgap voltage principle to generate temperature-compensated reference voltages at the outputs. The reported circuits have high supply voltage requirements and limited operating temperature ranges.

K. Ueno *et al.* [35] presented a CMOS voltage reference circuit with a low temperature coefficient and high PSRR. The reported circuit has a current source subcircuit and a bias-voltage subcircuit. The current source subcircuit uses a MOS resistor to generate the current, which is copied to bias-voltage subcircuit and an output reference voltage is produced. The circuit uses MOS transistors operating in the subthreshold region. The operating temperature range of the circuit is limited while the supply voltage requirement of the circuit is high.

S. S. Chouhan *et al.* [36] presented a CMOS voltage reference circuit using MOS transistors only. Using a series composite NMOS transistors, the thermal compensation has been achieved to generate the output reference voltage. The power consumption and the area occupied by the circuit are less. The circuit has a high supply voltage requirement and a moderate temperature coefficient over a limited operating temperature range.

B. Wang *et al.* [37] presented a compact CMOS voltage reference circuit. An active curvature compensation technique is introduced in the circuit to achieve a precision voltage reference. This curvature compensation technique is more effective than many other curvature-corrected techniques in terms of current consumption, operating temperature range, and temperature coefficient. But the circuit has disadvantages of high supply voltage requirement and large area.

A high PSRR CMOS voltage reference circuit is presented by S. Yousefi *et al.* [38] which is based on the difference of weighted gate-to-source voltages of MOS transistors. The MOS transistors used in the circuit are operating in the subthreshold region. The values of PSRR of the circuit are improved by reordering the locations of poles and zeros of the PSRR transfer function and supply independent biasing circuit. The high temperature coefficient, high supply voltage requirement, and large area are the main disadvantages of the circuit.

X. Li *et al.* [39] proposed a low temperature coefficient and high PSRR voltage reference circuit. The low temperature coefficient is achieved by using a high-order temperature compensation technique. The negative feedback is also used in the high-order compensation technique to enhance the PSRR and line sensitivity of the circuit. The circuit has disadvantages of high supply voltage requirement and large area.

H. Wu *et al.* [40] presented a high precision voltage reference circuit with curvature compensation and high PSRR. The pre-regulator of the supply voltage is used to immune the circuit from supply variations which increases the PSRR. The curvature compensation decreases the temperature dependency for a better temperature coefficient. The high supply voltage requirement, high power consumption, and large area are the main disadvantages of the circuit.

A low-voltage CMOS voltage reference circuit with a small temperature coefficient is proposed by J. Wang *et al.* [41]. The reference voltage is obtained by the addition of a CMOS voltage divider and a current source. The temperature coefficient of the circuit is reduced by compensating the temperature dependency of the current source. The circuit has low power consumption and high PSRR. But, the operating temperature range of the circuit is limited.

J. Jiang *et al.* [42] proposed a voltage reference circuit using MOS transistors only. The circuit has a low temperature coefficient and high PSRR. The curvature compensation technique is used to achieve a low temperature coefficient over a wide temperature range. A high PSRR of the circuit is achieved by using an active attenuator and impedance adapting compensation technique. The circuit has the disadvantage of high power consumption.

A compact temperature compensated CMOS voltage reference circuit has been proposed by S. Huang *et al.* [43]. The suggested circuit consists of a cascode current generator and a voltage reference generator. The cascode current generator uses a start-up circuit, the self-biased generator, and the PTAT core to generate a PTAT current. The temperature coefficient of the gate-to-source voltage of the NMOS transistor operating in the subthreshold region has been utilized for adequate temperature compensation with the PTAT current. The operating temperature range is limited and current consumption is high in the circuit.

N. Alhassan *et al.* [44] presented a CMOS voltage reference circuit without resistors and BJTs. All MOS transistors are biased in the strong inversion region. A feedback topology is also used to enhance the PSRR. However, the circuit occupies a large area.

Z. Luo *et al.* [45] presented a low-power voltage reference circuit. To obtain a low temperature coefficient, the second-order curvature compensation technique has been employed by using the resistor ratio of two types of resistors having opposite temperature dependency. In the circuit, a voltage divider is used to reduce the supply voltage value, and PTAT voltage generators are employed to reduce the values of resistors for low-power applications. But the temperature coefficient, area, and operating temperature range of the circuit are not much improved as per the demand of modern VLSI circuits.

S. S. Chouhan *et al.* [46] proposed a voltage reference using parasitic BJTs, MOS transistors, and resistors. In the circuit, the PTAT current thermally compensates the threshold voltage of the diode-connected NMOS transistor to obtain the output reference voltage. The circuit consumes low power and occupies a small area but it has a high supply voltage requirement, high temperature coefficient, and limited operating temperature range.

All MOS transistor-based low-power current reference circuit is presented by S. S. Chouhan *et al.* [47]. The reference circuit is based on a resistorless beta multiplier circuit and an additional temperature compensation technique. This technique decreases the reference current value and improves the temperature coefficient over a wide temperature range. The circuit has some limitations like high supply voltage requirement, high line sensitivity, and large area.

A. C. D. Oliveira *et al.* [48] presented a voltage reference based on self-cascode MOS that gives a reference voltage proportional to the threshold voltage difference of two NMOS transistors. Since the circuit is derived from the subtraction of two different threshold voltages, two devices having different threshold voltages are required. Therefore, the manufacturing cost of the design is comparatively high, and accuracy may be affected by the manufacturing variations.

L. Liu *et al.* [49] presented a low power, high-precision voltage reference circuit. A curvature compensation circuit is used to reduce the temperature coefficient over a wide temperature range. The clock scaling-down circuit is employed in the suggested circuit to achieve a good line sensitivity. However, the area occupied by the circuit is large.

Q. L. Li *et al.* [50] presented a voltage reference circuit with low line sensitivity in which high-order curvature compensation technique is used to achieve a low temperature coefficient over a wide temperature range. The negative feedback technique applied in the reported circuit replaces

the requirement of the operational amplifier. The circuit requires high supply voltage and it consumes more current.

Y. Liu *et al.* [51] proposed a low-power CMOS voltage reference circuit. In the circuit, the PTAT voltage is generated by injecting the leakage current of the NMOS transistor to two diode-connected NMOS transistors in series whereas the CTAT voltage is generated by using the body diodes of another NMOS transistor. The main limitations of the circuit are high line sensitivity and low PSRR.

X. Ming *et al.* [52] proposed a high precision and area-efficient voltage reference circuit. The first-order and high-order curvature compensation techniques are used to improve the temperature coefficient over a wide temperature range. The supply noise bypassing technique is used to achieve high PSRR for high frequency. However, the supply voltage and current consumption of the circuit are high.

L. Wang *et al.* [53] proposed a CMOS voltage reference circuit with high PSRR and low temperature coefficient. The single BJT, two resistors, and subthreshold MOS transistors are used to realize the voltage reference circuit. The CTAT voltage circuit uses two resistors and a vertical BJT, whereas the PTAT circuit uses two cascaded sub-PTAT circuits with MOS transistors operating in the subthreshold region. But, the supply voltage requirement of the circuit is high, and the occupied chip area is large.

R. Nagulapalli *et al.* [54] presented a voltage reference using MOS transistors. In the circuit, PTAT voltage is generated using a self-bias cascode structure whereas CTAT voltage is generated by the threshold voltage of the MOS transistor. The circuit consumes low power and less area, but the temperature sensitivity of the output voltage is high.

L. Wang *et al*. [55] proposed a CMOS voltage reference circuit in which the MOS transistors are operated in the subthreshold region for low voltage operation. But, the sensitivity of reference voltage due to temperature variations and supply variations is high. Also, the design occupies a large area due to large valued resistors and capacitors.

Y. Liang *et al.* [56] presented a low power voltage reference circuit using MOS transistors only. Since the circuit does not use an amplifier, resistor, or BJT, the reported structure of the voltage

reference is a power-efficient structure. However, the circuit has disadvantages of high temperature coefficient, low operating temperature range, and high line sensitivity.

Z. Zhou *et al.* [57] proposed a resistorless CMOS voltage reference circuit. The high-order curvature compensation technique is used to compensate the thermal nonlinearity of the base-to-emitter voltage of the BJT. A resistorless self-biased current source with feedback is also employed to improve the power supply noise attenuation without increasing the power supply. The high supply voltage requirement, high current consumption, high line sensitivity, and large area are the main disadvantages of the circuit.

The voltage reference presented by T. G. Nejad *et al.* [58] uses a logarithmic-curvature compensation technique to cancel the logarithmic temperature dependent terms. The linear temperature dependence of the reference voltage is eliminated by the addition of PTAT and CTAT voltages. The first-order and high-order temperature compensation in the circuit provides a low temperature coefficient over a wide temperature range. The circuit is insensitive to mobility temperature exponent, which makes the circuit compatible with various technologies. However, the circuit requires high supply voltage.

T. M. Brito *et al.* [59] suggested a resistorless voltage reference circuit using a self-cascode composite transistor and a Schottky diode. The self-cascode composite transistor is used to generate the PTAT behaviour whereas the CTAT behaviour is generated by a Schottky diode. The trimming circuit is also used to improve the temperature coefficient of the output reference voltage. The main limitations of the circuit are high supply voltage requirement and high line sensitivity.

J. lin *et al.* [60] proposed a voltage reference circuit with a self-regulating circuit to improve the line sensitivity of the reference voltage without using passive devices and amplifiers. The circuit also mitigates the channel length modulation effect. All the MOS transistors of the circuit are working in the subthreshold region, which helps to achieve low voltage operation. The main limitation of the circuit is the high-temperature coefficient.

A low temperature coefficient, low-noise, and low-offset voltage reference is suggested by L. Liu *et al.* [61]. The offset and noise suppression techniques are used to reduce the offset and noise generated by the error amplifier. The five-piece linear compensation technique is used to

improve the temperature sensitivity of the reported circuit. The limitations of the circuit are the high supply voltage requirement and high-power consumption.

J. Lei *et al.* [62] presented a resistorless voltage reference with low power consumption. The circuit consists of a BJT, MOS transistors, and a temperature compensation amplifier. The PTAT and CTAT voltages are generated using four PMOS transistors and a BJT, respectively. The high supply voltage, high line sensitivity, and large chip area are the major limitations of the presented circuit.

R. B. A. Zawawi *et al.* [63] proposed a voltage reference in which a line regulation control unit is used to decrease the effect of the channel length modulation factor. The curvature corrected control unit is also used to provide output reference voltage with improved temperature sensitivity. The high PSRR is achieved by using a high-gain operational amplifier. The limitation of the circuit is the high supply voltage requirement.

S. R. Khan [64] suggested a low temperature coefficient and high PSRR voltage reference circuit. To improve the power consumption and area of the circuit, a single-node-based temperature compensation feature and a single transistor-based start-up circuit are used. The dual PSRR enhancement stages are utilized to improve the PSRR of the suggested circuit. However, the circuit requires high supply voltage for proper operation.

P. K. Pal *et al.* [65] suggested a low voltage and low power CMOS voltage reference in which temperature compensated output reference voltage is obtained by combining the PTAT and CTAT voltages along with body biasing. The basic beta multiplier circuit with cascode transistor is used to generate the supply independent current which is given to the active load circuit. The body bias technique employed in the circuit reduces the process effect. The major disadvantages of the suggested circuit are low operating temperature range, low PSRR, low line sensitivity, and large area.

Y. Shi *et al.* [66] presented a self-biased voltage reference with high PSRR. The local negative loop and global self-biased feedback loop are used to enhance the PSRR of the circuit. The global self-biased loop is also used to bias the voltage reference in the steady-state which eliminates the requirement of an additional bias circuitry and hence it helps to save the chip area. The main limitations of the self-biased voltage reference are high supply voltage requirement and high power consumption.

H. Aminzadeh *et al.* [67] proposed a voltage reference circuit without any integrated resistor or BJT. The reported design uses a voltage reference core which is driven by a flexible biasing current. The voltage reference core consists of NMOS transistors and it is shielded from supply voltage variations through a voltage follower MOS transistor. Since the reported circuit uses only MOS transistors instead of linear capacitors and passive resistors, it has a low supply voltage requirement, low power consumption, and small area. The high temperature coefficient and high line sensitivity are the limitations of the circuit.

J. Liang *et al.* [68] presented a high PSRR and low temperature coefficient voltage reference circuit with a non-linear compensation technique. The high-order non-linear compensation technique utilizes the systematic non-linear offset voltage within the voltage reference to improve the temperature coefficient. The feedback loop of the start-up circuit and coupling structure of the supply voltage increase the PSRR of the voltage reference circuit. The circuit has a high supply voltage requirement and high power consumption.

J. Hu *et al.* [69] proposed a low-power voltage reference using a self-biased circuit. The temperature characteristics of the base-to-emitter voltage of BJT and the threshold voltage of the MOS transistor are used to generate a temperature-compensated reference voltage. The circuit has high line sensitivity and low PSRR.

M. Caselli *et al.* [70] presented a voltage reference circuit with low power consumption and low temperature coefficient over a wide temperature range. The output reference voltage of the circuit is obtained by the addition of PTAT and CTAT voltages. The presented circuit is biased using a PTAT current, which is insensitive to the MOS transistor process tolerance. The CTAT voltage is developed across the base-to-emitter voltage of BJT. The high supply voltage requirement, high line sensitivity, and large area are the limitations of the reported circuit.

For modern VLSI circuits, the values of supply voltage and output reference voltage should be low, especially for portable devices and internet of things (IoT) applications. Therefore, the voltage references should be designed that can operate at low supply voltage and generate low output reference voltage with more accuracy. Due to the high supply voltage requirement, the voltage-mode voltage references are not suitable for the low-voltage environment [16].

2.2 Current-mode voltage references

Y. Jiang *et al.* [1] proposed a low voltage reference by using a transimpedance amplifier. The operational amplifier of the conventional voltage reference is replaced by a transimpedance amplifier to overcome the limitation of the high supply voltage requirement. The limitations of the proposed voltage reference are low operating temperature range, low PSRR, and high power consumption.

The voltage reference presented by H. Banba *et al.* [16] uses diodes, resistors, PMOS transistors, and an operational amplifier. The output reference voltage is obtained by the addition of two currents with a feedback loop, which results in a low-voltage operation as compared to the conventional voltage reference. But, the main disadvantage of the reported voltage reference is the high temperature sensitivity.

P. B. Basyurt *et al.* [17] presented two low-supply voltage references using two different compensation schemes; one is known as current regulated loop and another is known as a duty-cycle regulated loop. The circuits use sampled-data amplifiers to optimize the power consumption. Low temperature coefficients of the circuits are obtained without using any trimming technique. However, the circuits occupy a large area.

G. Souliotis *et al.* [19] proposed a voltage reference with low line sensitivity and low temperature coefficient. The conventional operational amplifier is used instead of the rail-to-rail operational amplifier, making the circuit simple in design and more compact in the layout. The large valued external capacitor is not required for the filtering or stability issues. The high supply voltage requirement, high power consumption, and large area are the main limitations of the circuit.

The current-mode voltage reference suggested by J. D. Chen *et al.* [21], uses two-stage operational amplifiers. The regulated cascode is also used in the circuit to increase the output impedance and accuracy of the current mirror. The suggested circuit achieves low temperature coefficient and high PSRR by using the curvature compensation technique and increased gain of the feedback loop, respectively. However, the circuit has disadvantages of high supply voltage, high power consumption, and large area.

Z. K. Zhou *et al.* [25] proposed a CMOS voltage reference by using the mutual temperature compensation of threshold voltages of NMOS and PMOS transistors. The low temperature

coefficient of the reference voltage is achieved by using strong inversion MOS transistors. The high power supply noise attenuation and low line sensitivity are achieved via negative feedback branches in the proposed design. Since the circuit uses strong inversion MOS transistors, the power consumption of the circuit is high.

G. Giustolisi *et al.* [71] suggested a voltage reference circuit based on subthreshold MOS transistors. The temperature characteristics of gate-to-source voltage of subthreshold MOS transistor have been used. The PTAT behaviour is generated using two gate-to-source voltages of subthreshold MOS transistors and a resistor. In contrast, the CTAT behaviour is generated using a gate-to-source voltage of the subthreshold MOS transistor. The high temperature coefficient, high supply voltage, and large area are the main limitations of the circuit.

P. Huang *et al.* [72] proposed a voltage reference circuit using subthreshold MOS transistors and channel length modulation compensation technique. The channel length modulation compensation technique is used to enhance the line sensitivity of the reference voltage. But, the circuit has a high temperature coefficient over a wide temperature range and large area.

H. Luo *et al.* [73] proposed a subthreshold current-mode voltage reference circuit that uses a body bias technique to compensate the process-related fluctuations at the reference voltage. The circuit provides different body bias voltages to the MOS transistors using resistor trimming to control the threshold voltages of the MOS transistors, thus it compensates the process variations. This body bias technique also improves the PSRR and line regulation of the circuit. The limitations of the circuit are high supply voltage requirement, low operating temperature range, high current consumption, and large area.

The voltage reference presented by A. Tsitouras *et al.* [74] is based on current-mode topology. The circuit uses a conventional bandgap core to generate the PTAT current and a voltage to current converter converts a CTAT voltage into a CTAT current. The addition of these currents generates a temperature compensated current which is converted to a reference voltage across a resistor. The circuit also uses two rail-to-rail output stage operational amplifiers to improve the stability and decrease the supply voltage and process variations. The circuit has high PSRR and low temperature coefficient over a wide temperature range but it suffers from high supply voltage requirement, high power consumption, and large area.

J. Wu *et al.* [75] proposed a voltage reference circuit with high PSRR. The circuit consists of MOS transistors, BJTs, resistors, and an error amplifier. In the error amplifier, a local feedback loop is employed to achieve high gain. The error amplifier and a trimming resistor array are used to enhance the PSRR of the circuit. The limitations of this circuit are high supply voltage requirement and low operating temperature range.

Y. W. Zhang *et al.* [76] presented a voltage reference circuit with low offset voltage. The offset voltage compensation technique is used in the circuit which is designed by using two feedback loops and a cross-coupled BJTs structure. The proposed voltage reference has high PSRR and low temperature coefficient over a wide temperature range but it requires a high supply voltage.

D. Osipov *et al.* [77] presented a current reference based on a temperature-compensated beta multiplier circuit. The reference circuit consists of MOS transistors, BJTs, and a resistor. The temperature coefficient and process variations of the circuit have been improved by using the compensation technique. The limitations of the circuit are high supply voltage requirement, high power consumption, and high line sensitivity.

A. Parisi *et al.* [78] introduced a low power voltage reference circuit based on PTAT current and CTAT current generators. The first-order temperature compensation is used to provide the reference voltage which is less sensitive to the temperature. The MOS transistors operating in the weak inversion region and an operational amplifier are employed in the circuit to achieve low power consumption and high PSRR. The circuit has a low operating temperature range, high supply voltage requirement, high line sensitivity, and large area.

L. Wang *et al.*[79] proposed a current-mode voltage reference circuit in which cascode current mirrors and a frequency compensation technique are employed to increase the PSRR of the circuit. However, the circuit occupies a large area.

J. Duan *et al.* [80] presented a CMOS voltage reference circuit with low power and high PSRR. The temperature compensation of the reference current is obtained by the current subtracting technique. The area and power consumption of the circuit are reduced because it uses only MOS transistors. The cascode current mirrors increase the PSRR of the reported circuit. The circuit has a low operating temperature range and it requires high supply voltage.

The voltage reference based on the difference of two similar CTAT behaviours has been suggested by F. Olivera *et al.* [81]. The presented circuit provides an adjustable reference voltage that depends on the value of the output resistance. But, it has the disadvantages of high power supply requirement, high line sensitivity, and large chip area.

G. C. Huang *et al.* [82] presented a current-mode voltage reference with a low temperature coefficient and high PSRR. The proposed circuit uses the complementary loop locking technique that stabilizes the drain-to-source voltages of the current mirrors to increase PSRR. The reported circuit consumes more power.

K. Kondo *et al.* [83] suggested a current-mode voltage reference with low supply and low power consumption. The self-regulator with adaptive biasing technique is used in the circuit to minimize the PVT variations of the core reference circuit. The limitations of the circuit are high temperature coefficient and large area.

Y. Liu *et al.* [84] presented a voltage reference with low temperature coefficient and high PSRR. The curvature compensation technique is applied that offers a low temperature coefficient and high PSRR. But, the main disadvantages of the circuit are the high value of the supply voltage and high power consumption.

X. Guan *et al.* [85] proposed a current-mode voltage reference circuit using resistors, BJTs, MOS transistors, and an operational amplifier. A curvature compensation technique is employed in the circuit to decrease the sensitivity of reference voltage with temperature variations. But, the drawbacks of the circuit are high supply voltage requirement and high power consumption.

J. Li *et al.* [86] suggested a voltage reference circuit in which piecewise curvature-corrected technique is used to compensate the high-order temperature dependent terms of the reference voltage. The PTAT current is used to bias the rail-to-rail operational amplifier that provides negative feedback to the circuit. The circuit achieves low temperature coefficient and high PSRR at the cost of high supply voltage, high line sensitivity, and high power consumption.

D. F. Bowers *et al.* [87] presented a curvature compensated CMOS voltage reference circuit. In the circuit, MOS transistors are used to form a feedback loop and the BJTs are used to generate the reference voltage. The temperature coefficient is improved by using the curvature

compensation technique. The limitations of the presented circuit are high supply voltage requirement, high power consumption, and large area.

B. Ma *et al.* [88] proposed a voltage reference circuit with a high-order curvature compensation technique to compensate the temperature dependent nonlinearities. The circuit has two operational amplifiers operating in the linear amplification state. The circuit has low temperature coefficient over a wide temperature range and low line sensitivity at the expense of high supply voltage, high power consumption, and large area.

Q. Duan *et al.* [89] suggested a CMOS voltage reference that uses a high-order curvature compensation technique to achieve the low temperature coefficient. In the curvature compensation technique, two conventional bandgap cores and a curvature corrected circuit are employed. A low temperature coefficient over a wide temperature range is achieved without using any trimming circuit. The high supply voltage requirement, high power consumption, low PSRR, and large area are the limitations of the circuit.

J. Lv *et al.* [90] proposed a voltage reference in which a high-order curvature compensation technique is employed to obtain low temperature coefficient. The curvature compensation technique has been realized using two dual differential input operational amplifiers. The circuit has a high current driving capability and high PSRR. However, the circuit requires high supply voltage and a large area.

The current-mode curvature compensated voltage reference has been introduced by P. B. Basyurt *et al.* [91]. It uses a non-linear current to further compensate the temperature variations to achieve a better temperature coefficient. The limitations of the circuit are high supply voltage requirement, high power consumption, and large area.

C. M. Andreou *et al.* [92] presented a high-order curvature compensation voltage reference circuit with low supply voltage, low power consumption, and low temperature coefficient over a wide temperature range. The performance of the circuit has been improved by combining the non-linearities of NMOS transistors operating in the subthreshold region with the non-linearities of two different kinds of poly-silicon resistors. The circuit has low PSRR and a large area.

H. M. Chen *et al.* [93] proposed a voltage reference in which an adjusted-temperature-curvature compensation circuit is employed to obtain the low temperature coefficient over a wide temperature range. The adjusted-temperature-curvature compensation circuit consists of an

addition circuit, subtraction circuit, and current mirror. The high supply voltage and high power consumption are the main limitations of the voltage reference circuit.

R. Wang *et al.* [94] suggested a high precision CMOS voltage reference. The process-insensitive logarithmic, leakage, and piecewise curvature compensation techniques are used to improve the temperature coefficient over a wide temperature range. Beta compensation technique is also used in the circuit to cancel the inaccuracy due to beta variations in the BJTs. The circuit has a high supply voltage requirement and high power consumption.

L. Liu *et al.* [95] presented a voltage reference circuit that uses a high-order curvature compensation technique to improve the temperature coefficient over a wide temperature range. The circuit employs second-order and third-order curvature current generators with current-to-voltage converters. All the MOS transistors of the compensation circuit are operated in the subthreshold region which reduces the quiescent current. The presented voltage reference circuit has low line sensitivity and high PSRR due to the utilization of cascode structure. However, the circuit uses a high supply voltage and a large area.

G. Pan *et al.* [96] proposed a current-mode curvature compensated voltage reference. The curvature compensation technique compensates non-linear temperature term which is generated by the voltage difference of two transistors working in the different current states. The proposed circuit achieves a low temperature coefficient over a wide temperature range at the expense of high supply voltage, high power consumption, and a large area.

A curvature compensated voltage reference circuit proposed by X. Liu *et al.* [97] consists of two first-order voltage references and a subtraction circuit. Temperature characteristics of BJT are utilized to generate the first-order temperature compensated reference voltages. The circuit has a low temperature coefficient over a wide temperature range and high PSRR at the expense of increased power consumption and a large area.

A voltage reference is presented by T. Yan *et al.* [98] in which a segmented curvature compensation technique is used to achieve a low temperature coefficient over a wide temperature range and low power consumption. The circuit has the disadvantages of high supply voltage, high line sensitivity, and large area.

Y. Zhang *et al.* [99] proposed a voltage reference with a curvature compensation technique to achieve a low temperature coefficient. In the presented design, the piecewise curvature compensation and digital trimming techniques are combined to improve the temperature coefficient, mismatches due to current mirrors, and process variations. The high supply voltage and large area are the main limitations of the design.

Finally, it can be concluded that the current-mode voltage references based on diodes or BJTs require a higher power supply and larger chip area than the MOS-based current-mode voltage references. Therefore, new techniques can be applied in the current-mode voltage references based on MOS transistors to improve their performance parameters.

2.3 Research gaps identified

Several authors reported the various structures of voltage references and presented their performances in terms of temperature coefficient, PSRR, area, power, *etc*. The architectures proposed in recent years are studied and the following gaps are identified:

- The voltage references composed of diodes or BJTs require high power supply, high power consumption, and large chip area, which degrade the performance of the circuit. Therefore, the diode or BJT free voltage references may be investigated.
- The temperature coefficient has been decreased by using several curvature compensation techniques but the high-order temperature dependent nonlinearities of PTAT and CTAT voltages in the voltage references resulted in high temperature coefficient, which decreases the temperature stability of the circuit. So, design techniques may be investigated that provide high temperature stability over a wide temperature range.
- The PSRR has been increased to suppress the supply voltage variations from the voltage references at the expense of area and power dissipation. Alternate schemes for improving PSRR may be investigated.

2.4 Objectives of the proposed work

From the research gaps, the following objectives are formulated:

- To design a voltage reference circuit with high temperature stability over a wide range of temperature.
- To design a voltage reference circuit with high power supply rejection ratio (PSRR).
- To demonstrate the capability of proposed voltage reference circuit for an application.

2.5 Research methodology

To achieve the objectives, the following research methodology has been used:

- The specifications required for designing the voltage references for 180 nm CMOS technology are defined and then the proposed voltage references as per the specifications have been developed.

- The analyses of the proposed voltage references have been performed to validate the results.

- The low dropout regulators using proposed voltage references have been presented and the specifications of these low dropout regulators for 180 nm CMOS technology are also defined.

- The proposed voltage references and low dropout regulators have been simulated using Cadence virtuoso analog design environment and their performances have been compared with the similar circuits available in the literature.

CHAPTER 3
PROPOSED CMOS VOLTAGE REFERENCES AND THEIR APPLICATIONS

3.1 Introduction

The voltage references are essential building blocks for analog and mixed-signal circuits which are widely used in portable devices, computer systems, biomedical electronics, communication systems, etc. [17, 100-102]. The ever-increasing development of very large-scale integration (VLSI) circuits also necessitates the need for accurate voltage references. The conventional voltage references designed using BJTs [16, 29, 34, 103] have been improved continuously in terms of supply voltage requirement, power consumption, temperature sensitivity, line sensitivity, and chip area. But, the improvements in supply voltage requirement, power consumption, output reference voltage, and chip area are not significant as per the demand of modern VLSI circuits which are designed for portable devices and internet of things (IoT) applications. Thus, to overcome these drawbacks, the current trend is to design CMOS voltage references based on MOS transistors. In the conventional first-order temperature-compensated voltage reference, the output reference voltage (V_{REF}) depends on proportional-to-absolute-temperature (PTAT) and complementary-to-absolute-temperature (CTAT) voltages [21]. The effect of temperature variations on the reference voltage is mutually compensated by adding the weighted sum of PTAT voltage (V_{PTAT}) and CTAT voltage (V_{CTAT}). But the temperature sensitivity of the first-order circuit is high, which results in a large temperature coefficient (TC). Also, the conventional voltage reference provides an output reference voltage of around 1.26 V, which needs a supply voltage greater than 1.4 V to attain reasonable PSRR [21]. But, for modern VLSI circuits, these supply and reference voltage values are too high. In conventional voltage reference, the complexity, power consumption, and area are also increased. Thus, to overcome the limitations of a conventional voltage reference, it is necessary to design a novel CMOS voltage reference to enhance its performance at low supply voltage.

In the literature, various voltage references with improved performance have been proposed in which output reference voltages depend on PTAT and CTAT behaviours [66, 72-73, 78-79, 89, 101, 104–110]. The voltage references [89, 104, 105] use the compensation technique to improve the temperature coefficient but the supply voltage, output reference voltage, and power consumption of these circuits are high. S. K. Koh and L. Lee [106] presented a voltage reference using two temperature-compensation techniques which are based on the resistor-subdivision and

resistor-less techniques, but the temperature coefficient and the power dissipation of the circuit are not improved. The voltage reference presented by L. Wang *et al.* [79] achieves high PSRR by using a frequency compensation technique and cascode current mirrors but the temperature coefficient of the circuit is high. H. Luo *et al.* [73] suggested a voltage reference that uses the operational amplifiers to increase the accuracy, but the circuit has a high supply voltage requirement, high-power consumption, and large chip area. The voltage references [72, 78] are based on MOS transistors operating in the subthreshold region for low power consumption and less chip area, but the output reference voltages are more sensitive to the temperature variations. R. Nagulapalli *et al.* [107] proposed a voltage reference using a modified beta multiplier circuit. The circuit is operated at low supply voltage, but the values of line sensitivity, temperature coefficient, and power consumption are high. The voltage references [108–110] use the curvature compensation techniques to improve the temperature coefficients but these circuits have high power consumption and high supply voltage requirement. Y. Shi *et al.* [66] presented a self-biased voltage reference that uses two types of feedback loops, namely, local negative feedback loop and global self-biased loop to enhance the PSRR at the expense of high supply voltage and high power consumption.

In this brief, it can be concluded that most of the designs of voltage references reported in the literature are based on the addition of PTAT and CTAT behaviours. The PTAT behaviour is generated by the subtraction of two gate-to-source voltages of MOS transistors operating in subthreshold region having different aspect ratios with a resistor in the loop while the CTAT behaviour is generated across the gate-to-source voltage of a MOS transistor operating in a sub-threshold region. So, the PTAT generator requires a greater number of transistors with complex circuitry than the CTAT generator. However, the output reference voltage can also be obtained by the subtraction of two CTAT behaviours. Therefore, the voltage references based on the addition of PTAT and CTAT behaviours use a large number of transistors and hence they consume a large chip area and high power. Some of the recently reported designs use subtraction of two CTAT behaviours to overcome the disadvantages of the topology which was based on the addition of PTAT and CTAT behaviours [25, 81, 111-112]. Z. K. Zhou *et al.* [25] proposed a CMOS voltage reference by applying mutual temperature compensation of N-type and P-type threshold voltages. Since the circuit uses strong inversion MOS transistors, the power consumption of the circuit is high. The voltage reference based on the difference of two voltages having similar CTAT behaviours has been suggested by F. Olivera and A. Petraglia [81]. The perfectly matched NMOS transistors are used to develop similar CTAT behaviour curves. The

suggested circuit provides an adjustable reference voltage that depends on the output resistance value, but it has the disadvantages of high supply voltage requirement, high line sensitivity, and large chip area. F. Olivera and A. Petraglia [111] presented another voltage reference by using a computer-aided design approach. The circuit is based on the difference of two similar CTAT behaviours which are generated by using perfectly matched NMOS transistors. The circuit has the disadvantages of high supply voltage requirement, high line sensitivity, and large chip area. C. J. Liang *et al.* [112] presented a voltage reference in which the difference of two base-to-emitter voltages of BJTs are combined to generate the reference voltage. The power consumption of the circuit is low, but the values of line sensitivity, temperature coefficient, and supply voltage are high.

In this chapter, four different circuits of voltage references namely CMOS voltage reference-I, CMOS voltage reference-II, CMOS voltage reference-III, and CMOS voltage reference-IV are proposed. The proposed CMOS voltage references I and II use PTAT and CTAT behaviours to generate their output reference voltages while proposed CMOS voltage references III and IV use only CTAT behaviours to generate their output reference voltages. The proposed CMOS voltage references offer various improved performance parameters such as low temperature coefficient, wide operating temperature range, high PSRR, low line sensitivity, low supply voltage, and low power consumption. Further, the performances of the proposed voltage references have been validated using a basic VLSI circuit of the low dropout voltage regulator (LDO).

This chapter is organized as follows. The circuit descriptions of proposed CMOS voltage references I and II are described in section 3.2 while section 3.3 explains the circuit descriptions of proposed CMOS voltage references III and IV. The analyses of proposed CMOS voltage references are presented in section 3.4. The design considerations used in the proposed voltage references are addressed in section 3.5. The trimming circuit for the proposed CMOS voltage references is explained in section 3.6. Section 3.7 presents the applications of proposed CMOS voltage references. Finally, the chapter is concluded in section 3.8.

3.2 Proposed CMOS voltage references I and II

In this section, the circuit descriptions of proposed CMOS voltage references (I and II) are discussed.

3.2.1 Basic principle

The basic concept employed to design the proposed CMOS voltage references (I and II) is depicted in Figure 3.1. The PTAT and CTAT current generators are used to generate PTAT and CTAT behaviours, respectively which have opposite temperature dependencies and different slopes. The effect of temperature variations is mutually compensated by the weighted sum of PTAT and CTAT behaviours to obtain the temperature-compensated current (I_{REF}). Finally, the current I_{REF} is converted into a temperature-compensated reference voltage (V_{REF}) by using a resistor.

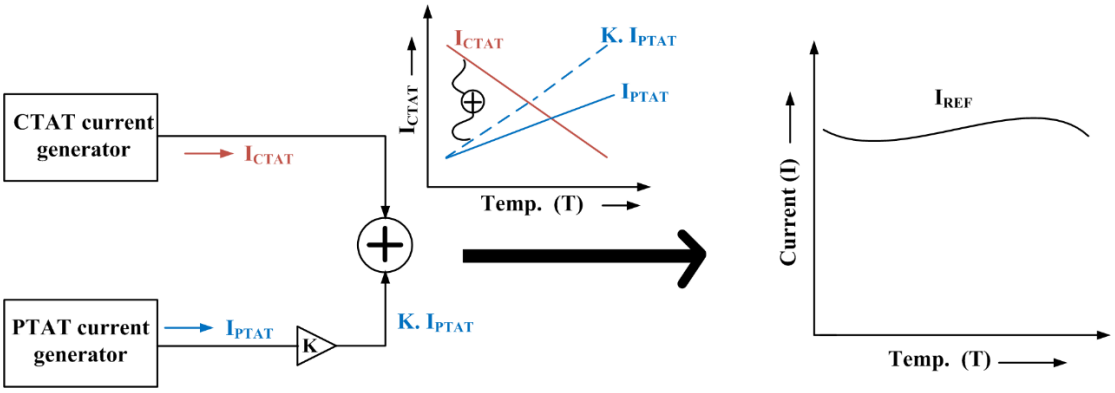


Figure 3.1 The basic principle of proposed CMOS voltage references I and II

3.2.2 Proposed CMOS voltage reference-I

The proposed CMOS voltage reference-I shown in Figure 3.2 consists of two similar supply independent first-order temperature-compensated voltage references (SIFTCVR-I and SIFTCVR-II) and a curvature compensation circuit.

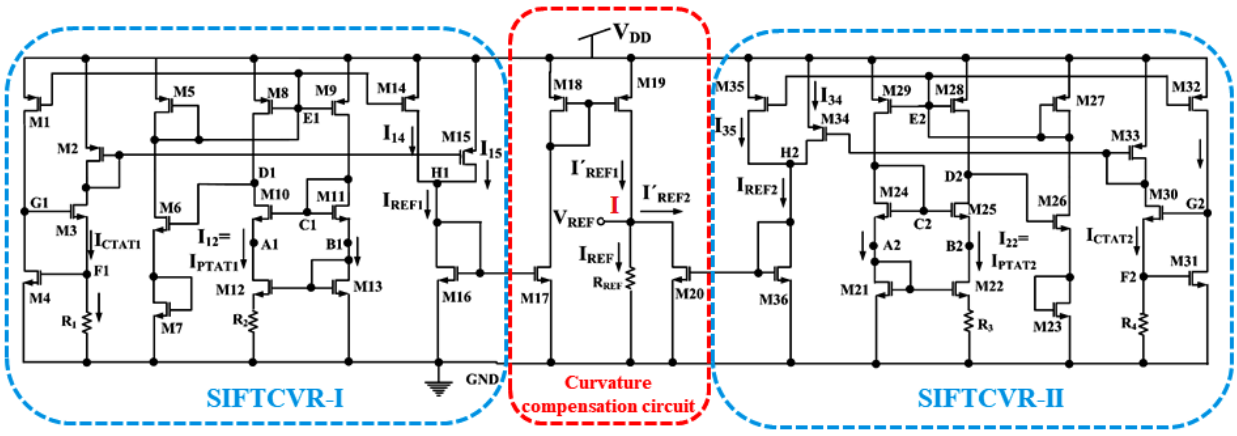


Figure 3.2 Proposed CMOS voltage reference-I

The proposed SIFTCVR-I and SIFTCVR-II are based on the basic principle discussed in section 3.2.1, in which PTAT and CTAT currents having opposite temperature dependencies are used to generate first-order temperature-compensated reference currents I_{REF1} and I_{REF2}, respectively. In SIFTCVR-I or SIFTCVR-II, only the simple first-order temperature dependent terms are compensated to reduce the temperature dependency of the output reference current whereas high-order temperature dependent terms are not compensated. So, a curvature compensation circuit that compensates the high-order temperature dependent terms by subtracting first-order temperature-compensated reference currents I'_{REF1} and I'_{REF2} of SIFTCVR-I and SIFTCVR-II, respectively is used to provide a low temperature coefficient output reference voltage across resistor R_{REF}.

3.2.2.1 Supply independent first-order temperature-compensated voltage references

The supply independent first-order temperature-compensated voltage reference-I (SIFTCVR-I) uses two resistors (R_1 and R_2) and sixteen transistors (M1 to M16) which are operating in the subthreshold region. In the proposed SIFTCVR-I, the supply independent I_{PTAT1} and I_{CTAT1} currents are generated using negative feedback loops. The transistors M11, M10, M6, M5, M8, and M9 form a negative feedback loop to generate a supply independent current I_{PTAT1}. Also, this negative feedback ensures equal voltages at nodes A1 and B1. If the voltage of node C1 increases with the increase in the supply voltage, then voltage at node D1 decreases. The decreased voltage at node D1 increases the voltage at node E1, and finally, this increased voltage of node E1 will help to decrease the voltage of node C1. So, the voltage at node C1 is constant and independent of the supply voltage variations, which generates a supply independent current I_{PTAT1}. Similarly, another negative feedback loop formed by transistors M1 to M4 is used to generate a supply independent current I_{CTAT1}. As the supply voltage increases, the current I_{CTAT1} will increase, which increases the voltage at node F1. This increased voltage increases the current in the M4 branch, and the voltage at node G1 will be dropped down. The current I_{CTAT1} will decrease, and the voltage at node F1 will be dropped down. So, the voltage at node F1 remains constant with respect to supply voltage variations, and hence the current I_{CTAT1} flowing across R_1 is also independent of the supply voltage variations. Due to these supply independent currents I_{PTAT1} and I_{CTAT1}, the proposed circuit shows improved line sensitivity and PSRR. But the addition of the weighted sum of I_{PTAT1} current and I_{CTAT1} current across node H1 gives the first-order temperature-compensated reference current I_{REF1}.

The supply independent first-order temperature-compensated voltage reference-II (SIFTCVR-II) is also used in the circuit, which consists of transistors M21 to M36 operating in the subthreshold region and two resistors (R3 and R4) to generate another first-order temperature-compensated reference current I_{REF2}. These two supply independent currents I_{REF1} and I_{REF2} generated from SIFTCVR-I and SIFTCVR-II, respectively have the same curvatures with respect to temperature.

3.2.2.2 Curvature compensation circuit

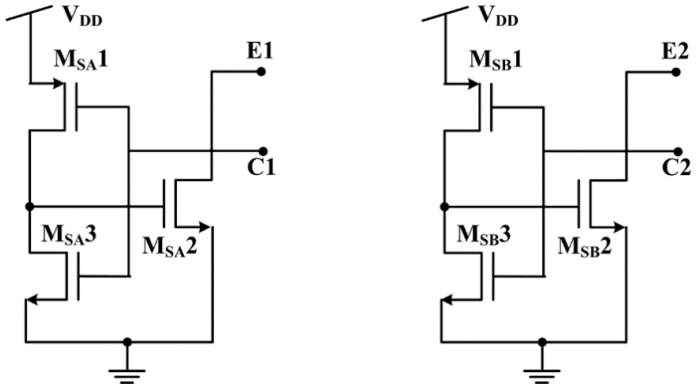
The curvature compensation circuit is developed using transistors M17 to M20 and a resistor (R_{REF}). A current mirror formed by transistors M16 to M17 is used to copy the current I_{REF1}. The current mirrors formed by transistors M18 & M19 and M20 & M36 are used to generate currents I'_{REF1} and I'_{REF2}, respectively, at node I. The current I'_{REF2} is subtracted from I'_{REF1} to compensate the high-order temperature dependent terms of gate-to-source voltages (V_{GS4} and V_{GS31}) and a curvature-compensated output reference voltage is obtained across the resistor R_{REF}.

The proposed CMOS voltage reference-I can offer an improved temperature coefficient due to the high-order curvature compensation technique as compared to first-order temperature-compensated voltage references available in literature but at the expense of the high supply voltage requirement, complexity, and increased chip area.

3.2.2.3 Start-up circuit

The start-up circuit [113] for SIFTCVR-I shown in Figure 3.3 (a) is connected at nodes E1 and C1. It uses transistors $M_{SA}1$-$M_{SA}3$ and helps the SIFTCVR-I to come out from the zero-current state. At the beginning of the start-up process, the potential at node C1 is low which will turn ON transistor $M_{SA}1$ and increase the potential at the gate of $M_{SA}2$. The increased potential at the gate of $M_{SA}2$ will turn ON transistor $M_{SA}2$ and drop down the potential at node E1. The decreased potential at node E1 helps to flow the currents into the circuit through the transistors M8 and M9. Finally, when the SIFTCVR-I starts working properly, the start-up circuit turns OFF without affecting the normal operations. The start-up circuit [113] for SIFTCVR-II is shown in Figure 3.3 (b) which uses transistors $M_{SB}1$-$M_{SB}3$. It is connected at nodes E2 and C2. It helps the SIFTCVR-II to come out from the zero-current state. At the beginning of the start-up process, the potential at node C2 is low which will turn ON transistor $M_{SB}1$ and increase the potential at the gate of $M_{SB}2$. The increased potential at the gate of $M_{SB}2$ will turn ON transistor $M_{SB}2$ and drop down the potential at node E2. The decreased potential at node E2 helps to flow the currents into

the circuit through the transistors M28 and M29. Finally, when SIFTCVR-II starts working properly, the start-up circuit turns OFF without affecting the normal operations.



(a) (b)

Figure 3.3 Start-up circuits [113] for (a) SIFTCVR-I (b) SIFTCVR-II

3.2.3 Proposed CMOS voltage reference-II

The proposed CMOS voltage reference-II shown in Figure 3.4 is also based on the basic principle discussed in section 3.2.1, in which output reference voltage is obtained by the addition of PTAT and CTAT currents across resistor R_{REF}. The proposed circuit mainly consists of a start-up circuit, a bias current generator, a self-biased cascode branch, a PTAT and CTAT currents generator, and a current adder. The proposed CMOS voltage reference-II overcomes the limitations of the proposed CMOS voltage reference-I by using only a self-biased cascode branch to generate both the PTAT and CTAT voltages which makes the circuit simple and area efficient. The operational amplifiers (OP-AMPs) are used in the negative feedback topology. The negative feedback makes it possible to set the gain and cut-off frequency to the desired values, thereby improving their stability and reducing performance variation, part-to-part variation, and sensitivity to the temperature as well as other environmental parameters. Due to the high gain of the OP-AMP, the voltage at inverting input terminal is maintained almost equal to the voltage at the output terminal. The relation of output voltage to the input voltage is expressed as

$$V_{OUT} = G.(V_{IN} - V_{OUT}) \tag{3.1}$$

where G is the open loop gain of the operational amplifier.

After simplification, the output voltage V_{OUT} is obtained as

$$V_{OUT} = \frac{V_{IN}}{1 + \left(\frac{1}{G}\right)} \tag{3.2}$$

From equation (3.2), it can be seen that the output voltage is equal to the input voltage for high value of gain G.

The high gain operational amplifiers in the negative feedback loop are used to achieve low line sensitivity and high PSRR of the proposed CMOS voltage reference-II.

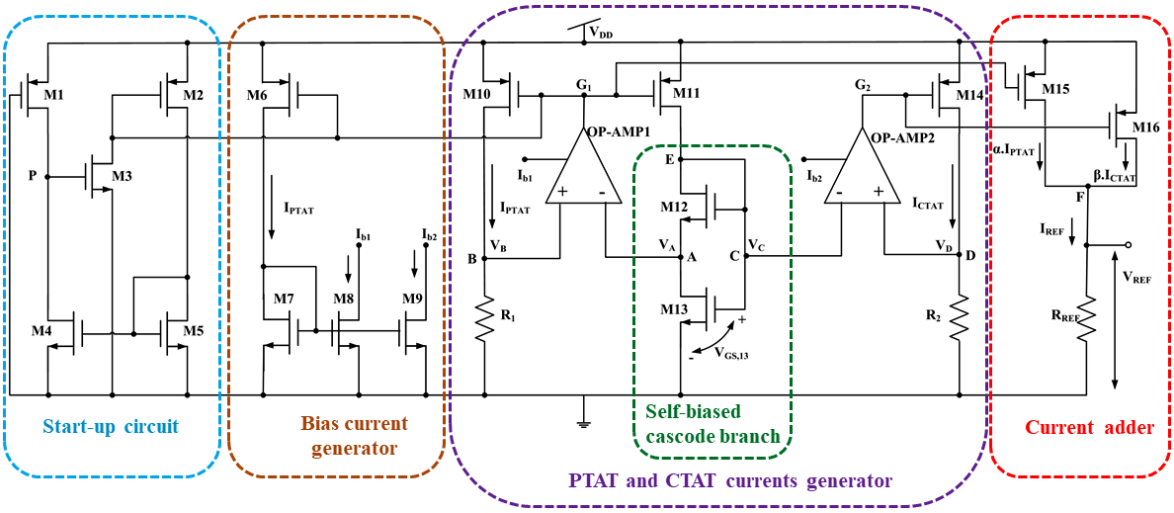


Figure 3.4 Proposed CMOS voltage reference-II

3.2.3.1 Start-up circuit

The start-up circuit developed by transistors M1-M5 supports the proposed circuit to come out from a zero-current state. The gate of transistor M1 is connected to the ground, which will help to increase the potential at node P, due to which the transistor M3 turns ON. The turned ON transistor M3 decreases the potential at node G1, which will provide the current in the circuit through the transistors M10 and M11. Finally, the circuit starts working properly and the well-conducted transistor M4 will drop down the potential at node P. So, the transistor M3 enters into the cut-off region and the start-up circuit is turned OFF.

3.2.3.2 Bias current generator

The bias current generator block consists of transistors M6-M9 is employed to generate the bias currents I_{b1} and I_{b2} for the operational amplifiers OP-AMP1 and OP-AMP2, respectively.

3.2.3.3 Self-biased cascode branch

The self-biased cascode branch using transistors M12 and M13 generates the PTAT and CTAT voltages at nodes A and C, respectively. The transistors M12 and M13 are operating in the subthreshold region.

3.2.3.4 PTAT and CTAT currents generator

PTAT current generator uses transistors M10 and M11, a resistor R_1, and an operational amplifier OP-AMP1 to generate the current I_{PTAT} while CTAT current generator uses a transistor M14, a resistor R_2, and an operational amplifier OP-AMP2 to generate the current I_{CTAT}. The OP-AMP1 with transistor M10 forms a negative feedback loop that maintains the equal potential at nodes A and B. Hence, the potential at node B and the current flowing through transistor M10 have PTAT behaviours. The OP-AMP2 with transistor M14 forms a negative feedback loop that maintains the equal potential at nodes C and D. Hence, the potential at node D and the current flowing through transistor M14 have CTAT behaviours.

The circuit diagrams of operational amplifiers namely OP-AMP1 and OP-AMP2 [4], which are used in the negative feedback loop to improve the line sensitivity and PSRR are shown in Figures 3.5 and 3.6, respectively. In OP-AMP1, PMOS transistors are used to design the differential pair. Due to the low voltage at node A in the proposed design, PMOS transistor-based differential amplifier is required which can be effectively operated at the low voltage. In OP-AMP2, the NMOS transistors are used to design the differential pair. The high voltage at node C makes the NMOS transistors-based differential amplifier a good choice as the NMOS transistors are effectively operated at the high voltage.

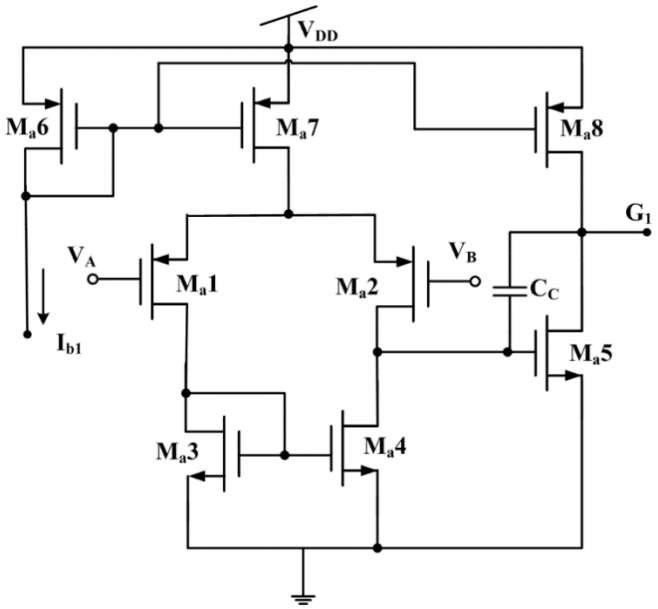


Figure 3.5 OP-AMP1 [4]

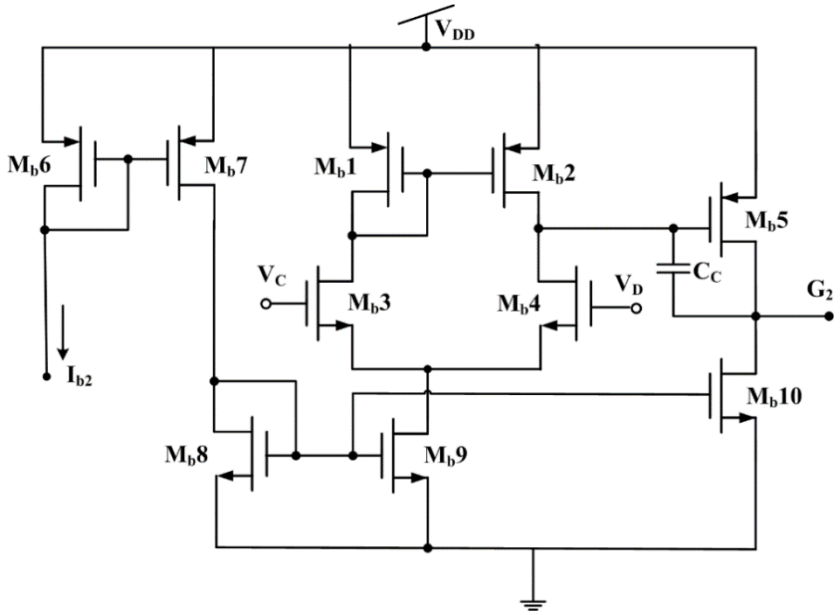


Figure 3.6 OP-AMP2 [4]

3.2.3.5 Current adder

The current adder circuit uses transistors M15-M16 and a resistor (R_{REF}). The transistor M15 copies the PTAT current (I_{PTAT}) from transistor M10 with a scaling factor of 'α' and the transistor M16 copies the CTAT current (I_{CTAT}) from transistor M14 with a scaling factor of 'β'. To obtain a constant reference current I_{REF}, the currents $\alpha.I_{PTAT}$ and $\beta.I_{CTAT}$ are added at node F. The reference voltage V_{REF} is generated across resistor R_{REF} by the reference current I_{REF}.

In the proposed CMOS voltage references I and II, the output reference voltages are obtained by the addition of PTAT and CTAT behaviours [66, 72-73, 78-79, 89, 101, 104–110]. In both of the proposed circuits, the PTAT behaviours have been generated by the subtraction of two gate-to-source voltages of MOS transistors operating in the sub-threshold regions with the resistor in the loop while the CTAT behaviours have been generated across the gate-to-source voltage of the MOS transistor operating in the sub-threshold region. So, the PTAT generators require more transistors with complex circuitries than the CTAT generators and therefore it is evident that the reference voltage generators which are based on the addition of PTAT and CTAT behaviours use a large number of transistors. Hence, this technique does not offer much improvement in the circuit's complexity, power consumption, and chip area. To overcome these limitations, the CTAT-CTAT technique that uses less number of transistors has been employed to design the proposed CMOS voltage references III and IV.

3.3 Proposed CMOS voltage references III and IV

In this section, the circuit descriptions of proposed CMOS voltage references (III and IV) are described.

3.3.1 Basic principle

The basic concept used to design the proposed CMOS voltage references (III and IV) is illustrated in Figure 3.7. Two CTAT current generators (I and II) provide two currents (I_{CTAT1} and I_{CTAT2}) which have different slopes but similar temperature dependencies. The current I_{CTAT2} is multiplied by a constant 'N' and hence, a current $N.I_{CTAT2}$ is obtained, whose temperature slope is equal to the temperature slope of the current I_{CTAT1}. Thereafter, the current $N.I_{CTAT2}$ is subtracted from I_{CTAT1} using a current subtractor, which results in a temperature independent reference current (I_{REF}) due to the cancellation of the same temperature dependence behaviour of the currents. The temperature-compensated current I_{REF} is converted into a temperature-compensated reference voltage (V_{REF}) by using a resistor.

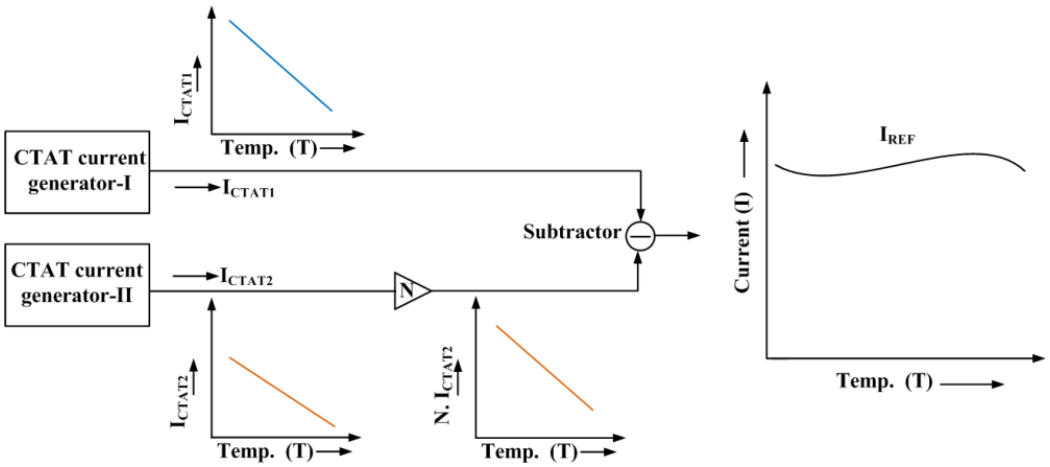


Figure 3.7 Basic principle of the proposed CMOS voltage references III and IV

3.3.2 Proposed CMOS voltage reference-III

The proposed CMOS voltage reference-III shown in Figure 3.8 is based on the CTAT-CTAT technique that offers various advantages in terms of circuit simplicity, power consumption, and area[114]. It is designed using two supply independent CTAT generators (SICG-I & SICG-II) and a current subtractor. The supply independent CTAT generator consists of cascode current mirrors and a negative feedback loop that opposes the change in the CTAT current with the change in the supply voltage. The SICG-I and SICG-II generate two currents (I_{CTAT1} and I_{CTAT2})

which have different slopes but similar temperature dependencies. The current I_{CTAT2} is multiplied by a constant N and hence, a current $N.I_{CTAT2}$ is obtained, whose temperature slope is equal to the temperature slope of the current I_{CTAT1}.

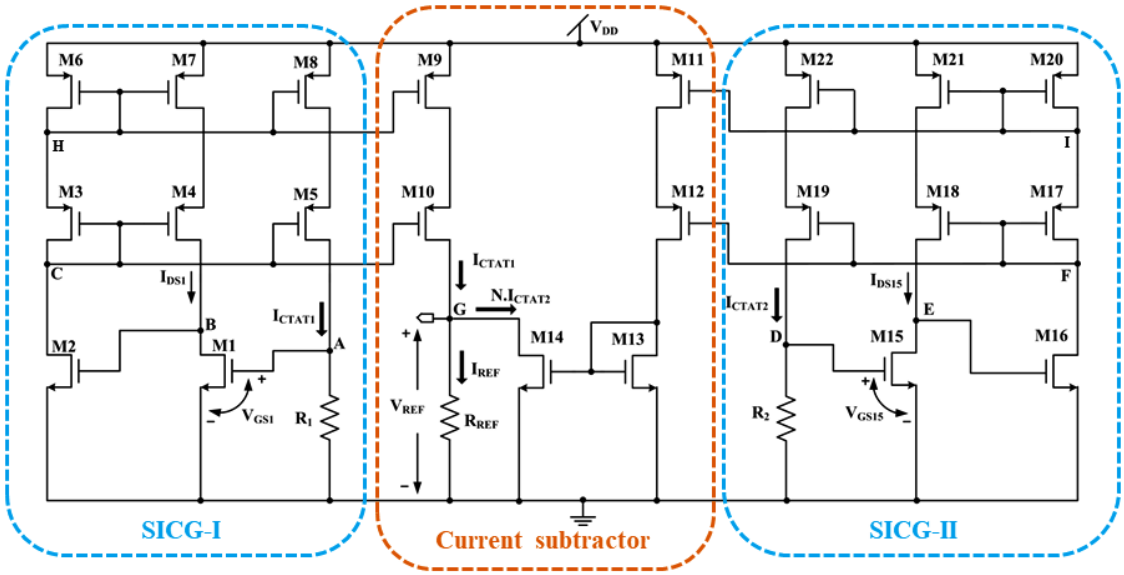


Figure 3.8 Proposed CMOS voltage reference-III

After that, a current subtractor is used to subtract $N.I_{CTAT2}$ from I_{CTAT1}, which results in a temperature independent reference current (I_{REF}) due to the cancellation of the same temperature dependence behaviour of the currents. Finally, the temperature-compensated current I_{REF} is converted into a temperature-compensated reference voltage (V_{REF}) using a resistor (R_{REF}).

3.3.2.1 Supply independent CTAT generator

The supply independent CTAT generator-I (SICG-I) consists of transistors M1-M8 and a resistor (R_1). The transistor M1 is operating in the subthreshold region and it generates the current I_{CTAT1} across the resistor (R_1). The transistors M1, M2, M3, and M5 form negative feedback in the circuit that opposes any change in the value of the current I_{CTAT1} and hence, an independent of supply voltage variations current I_{CTAT1} can be achieved. As the supply voltage increases, the current I_{CTAT1} will increase, which increases the voltage at node A. This increased voltage increases the current in the M1 branch and thus, the voltage at node B will be dropped down. This dropped voltage at node B decreases the current in the M2 branch, due to which the voltage at node C will increase. Finally, this increased voltage at node C will help to decrease the current I_{CTAT1}.

The supply independent CTAT generator-II (SICG-II) consists of transistors M15-M22 and a resistor (R_2). The transistor M15 operates in the subthreshold region and generates a current I_{CTAT2} across the resistor (R_2). The transistors M15, M16, M17, and M19 of SICG-II form negative feedback in the circuit that opposes the change in the value of current I_{CTAT2} and hence, a current I_{CTAT2} that is also independent of supply voltage variations can be achieved. The cascode current mirrors are used in the proposed circuit to improve the line sensitivity and PSRR.

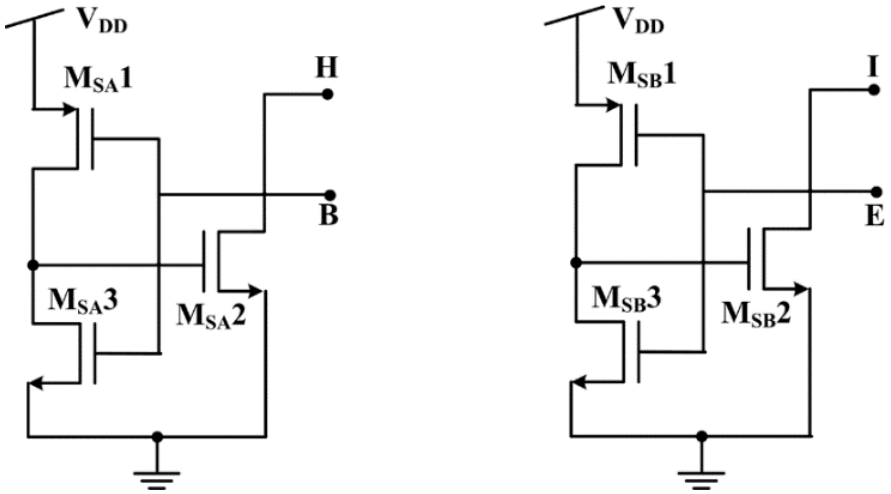
3.3.2.2 Current subtractor

The transistors M9-M14 and a resistor (R_{REF}) form a current subtractor that generates a reference current I_{REF}. The current I_{CTAT1} is copied from SICG-I using cascode current mirror formed by transistors M9 and M10, whereas the current I_{CTAT2} of SICG-II is mirrored through cascode current mirror formed by transistors M11and M12. The current I_{CTAT2} is multiplied by a constant 'N' using the current mirror formed by transistors M13 and M14. At node G, the current $N.I_{CTAT2}$ is subtracted from I_{CTAT1} to obtain a constant reference current I_{REF}. Finally, the current I_{REF} is used to generate the output reference voltage V_{REF} across resistor R_{REF}.

3.3.2.3 Start-up circuit

The start-up circuit [113] for SICG-I shown in Figure 3.9 (a) is connected at nodes B and H. It uses transistors $M_{SA}1$-$M_{SA}3$ and helps the SICG-I to come out from the zero-current state. At the beginning of the start-up process, the potential at node B is low which will turn ON transistor $M_{SA}1$ and increase the potential at the gate of $M_{SA}2$. The increased potential at the gate of $M_{SA}2$ will turn ON transistor $M_{SA}2$ and drop down the potential at node H. The decreased potential at node H helps to flow the currents into the circuit through the transistors M6 and M7. Finally, when the SICG-I starts working properly, the start-up circuit turns OFF without affecting the normal operations. The start-up circuit [113] for SICG-II is shown in Figure 3.9 (b) which uses transistors $M_{SB}1$-$M_{SB}3$. It is connected at nodes E and I. It helps the SICG-II to come out from the zero-current state. At the beginning of the start-up process, the potential at node E is low which will turn ON transistor $M_{SB}1$ and increase the potential at the gate of $M_{SB}2$. The increased potential at the gate of $M_{SB}2$ will turn ON transistor $M_{SB}2$ and drop down the potential at node I. The decreased potential (at node I) helps to flow the currents into the circuit through the transistors M20 and M21. Finally, when the SICG-II starts working properly, the start-up circuit turns OFF without affecting the normal operations.

The proposed CMOS voltage reference-III uses a reduced number of transistors with less complexity as compared to the proposed CMOS voltage reference-I and II. However, as per the demand of modern VLSI, the proposed CMOS voltage reference-III requires further improvements in the line sensitivity and PSRR.



(a) (b)

Figure 3.9 Start-up circuits [113] for (a) SICG-I (b) SICG-II

3.3.3 Proposed CMOS voltage reference-IV

To achieve low line sensitivity and high PSRR, another circuit of voltage reference named CMOS voltage reference-IV is proposed. The proposed CMOS voltage reference-IV shown in Figure 3.10 is also based on the subtraction of two CTAT behaviours having similar temperature dependencies. A beta-multiplier is used in the proposed CMOS voltage reference-IV to generate two CTAT voltages. These CTAT voltages are converted into CTAT currents by using two operational amplifiers in the negative feedback loop to achieve low line sensitivity and high PSRR. The proposed voltage reference-IV uses a start-up circuit, a bias current generator, a beta-multiplier circuit, two CTAT currents generators (CCG-I and CCG-II), and a current subtractor.

3.3.3.1 Start-up circuit

The start-up circuit [113] developed using transistors M1-M3 helps the proposed circuit to come out from the zero-current state. At the beginning of the start-up process, the potential at node E is low which will turn ON transistor M1 and increase the potential at node C. The increased potential at node C will turn ON transistor M2 and drop down the potential at node D. The

decreased potential at node D helps to flow the currents into the circuit through the transistors M9 and M11. Finally, the proposed circuit starts working properly and the start-up circuit turns OFF without affecting the normal operation of the circuit.

3.3.3.2 Bias current generator

The bias currents I_{bias1} and I_{bias2} for the operational amplifiers OP-AMP1' and OP-AMP2', respectively are generated from the bias current generator block, which consists of transistors M4-M7.

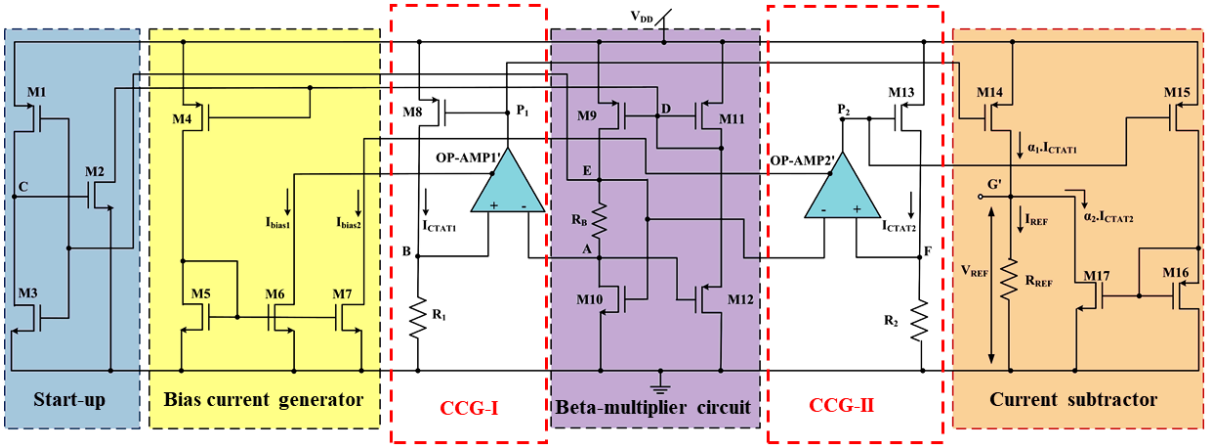


Figure 3.10 Proposed CMOS voltage reference-IV

3.3.3.3 Beta-multiplier circuit

The standard beta-multiplier circuit [115] consists of transistors M9-M12 and a resistor R_B. It is used to generate the CTAT voltages at nodes A and E. The transistors M9 and M11 form a current mirror that provides the same current through transistors M10 and M12. The transistors M10 and M12 are operating in the subthreshold region. These transistors generate the CTAT behaviours at nodes A and E due to their exponential current-voltage relationships.

3.3.3.4 CTAT currents generators

The CTAT currents generators CCG-I and CCG-II are used to generate two CTAT currents I_{CAT1} and I_{CTAT2}, respectively. The CCG-I consists of an operational amplifier OP-AMP1' [4], transistor M8 and resistor R_1. The CCG-II consists of an operational amplifier OP-AMP2' [4], transistor M13, and resistor R_2. The circuit diagram of the OP-AMP1' and OP-AMP2' is shown in Figure 3.5. A negative feedback loop formed by OP-AMP1' and transistor M8 provides an equal voltage at nodes A and B. The voltage at node A has CTAT behaviour due to the gate-to-source voltage ($V_{GS,12}$) of transistor M12 working in the subthreshold region and hence, the

voltage with CTAT behaviour can also be achieved at node B. The resistor R_1 at node B converts the CTAT voltage into a CTAT current I_{CTAT1}. The operational amplifier OP-AMP2' and transistor M13 form a negative feedback loop that provides an equal voltage at nodes E and F. The voltage at node E has CTAT behaviour due to the gate-to-source voltage ($V_{GS,10}$) of transistor M10 working in the subthreshold region and hence, the voltage with CTAT behaviour can also be obtained at node F. The resistor R_2 at node F converts the CTAT voltage into a CTAT current I_{CTAT2}.

3.3.3.5 Current subtractor

The current subtractor circuit uses transistors M14-M17 and a resistor R_{REF}. The current I_{CTAT1} is copied from transistor M8 to M14 with a scaling factor of α_1 while current I_{CTAT2} is copied from transistor M13 to M17 with a scaling factor of α_2. The currents $\alpha_1.I_{CTAT1}$ and $\alpha_2.I_{CTAT2}$ are subtracted at node G' to obtain a constant reference current I_{REF}. Thereafter, the reference current I_{REF} is converted into a reference voltage V_{REF} across the resistor R_{REF}.

3.4 Analysis of proposed CMOS voltage references

The analyses of all of the proposed CMOS voltage references (I, II, III, and IV) have been presented in this section.

3.4.1 Analysis of proposed CMOS voltage reference-I

This section includes the output reference voltage expression of the proposed CMOS voltage reference-I (Figure 3.2) and minimum temperature coefficient conditions of supply independent first-order temperature-compensated voltage references (SIFTCVR-I and SIFTCVR-II). To improve the temperature sensitivity of the proposed CMOS voltage reference-I, a high-order curvature compensation technique has also been employed.

3.4.1.1 Output reference voltage

In the proposed CMOS voltage reference-I, the transistors M12 and M13 of supply independent first-order temperature-compensated voltage reference-I (SIFTCVR-I) are operating in the subthreshold region and due to the equal voltages at nodes A1 and B1, the relation between gate-to-source voltages V_{GS12} and V_{GS13} is given as

$$V_{GS13}=V_{GS12}+I_{12}R_2 \tag{3.3}$$

Since the voltages V_{DS12} and V_{DS13} are greater than $4V_T$, the gate-to-source voltages V_{GS12} and V_{GS13} of transistors M12 and M13, respectively can be expressed using equation (1.3) as

$$V_{GS12}=V_{TH12}+\eta V_T \ln\left(\frac{I_{12}}{\mu C_{ox}(W/L)_{12}(\eta-1)V_T^2}\right) \tag{3.4}$$

$$V_{GS13}=V_{TH13}+\eta V_T \ln\left(\frac{I_{13}}{\mu C_{ox}(W/L)_{13}(\eta-1)V_T^2}\right) \tag{3.5}$$

Substituting the values of V_{GS12} and V_{GS13} from equations (3.4) and (3.5) in equation (3.3), the current I_{12} is obtained as

$$I_{12}=\frac{V_{GS13}-V_{GS12}}{R_2}=\frac{\eta V_T}{R_2}\ln\left(\frac{(W/L)_{12}}{(W/L)_{13}}\right)=I_{PTAT1} \tag{3.6}$$

where $(W/L)_{12}$ and $(W/L)_{13}$ are the aspect ratios of transistors M12 and M13, respectively.
From equation (3.6), it is evident that the current I_{PTAT1} is directly proportional to the thermal voltage V_T and independent of power supply variations.
From Figure 3.2, the current I_{CTAT1} can be expressed as

$$I_{CTAT1}=\frac{V_{GS4}}{R_1} \tag{3.7}$$

From equation (3.7), it can be seen that current I_{CTAT1} depends on the gate-to-source voltage of transistor M4 working in the subthreshold region.
The currents I_{14} and I_{15} are expressed as

$$I_{14}=\left(\frac{(W/L)_{14}}{(W/L)_9}\right)I_{PTAT1} \tag{3.8}$$

$$I_{15}=\left(\frac{(W/L)_{15}}{(W/L)_2}\right)I_{CTAT1} \tag{3.8}$$

where $(W/L)_2$, $(W/L)_9$, $(W/L)_{14}$, and $(W/L)_{15}$ are the aspect ratios of transistors M2, M9, M14 and M15, respectively.
Applying KCL at node H1, the reference current (I_{REF1}) of the SIFTCVR-I is obtained as

$$I_{REF1}=I_{14}+I_{15}=\frac{(W/L)_{14}}{(W/L)_9}I_{PTAT1}+\frac{(W/L)_{15}}{(W/L)_2}I_{CTAT1} \tag{3.10}$$

Substituting the values of I_{PTAT1} and I_{CTAT1} from equations (3.6) and (3.7) in equation (3.10), the current I_{REF1} is expressed as

$$I_{REF1}=\left(\frac{(W/L)_{14}}{(W/L)_{9}}\right)\frac{\eta V_T}{R_2}\ln\left(\frac{(W/L)_{12}}{(W/L)_{13}}\right)+\left(\frac{(W/L)_{15}}{(W/L)_{2}}\right)\frac{V_{GS4}}{R_1} \tag{3.11}$$

Since the thermal voltage (V_T) possesses PTAT behaviour and gate-to-source voltage (V_{GS4}) has CTAT behaviour then these PTAT and CTAT behaviours can be cancelled out to achieve first-order temperature-compensated reference current by choosing appropriate values of resistances and aspect ratios of transistors.

Similarly, the current I_{REF2} of the SIFTCVR-II can be expressed as

$$I_{REF2}=\left(\frac{(W/L)_{35}}{(W/L)_{29}}\right)\frac{\eta V_T}{R_3}\ln\left(\frac{(W/L)_{22}}{(W/L)_{21}}\right)+\left(\frac{(W/L)_{34}}{(W/L)_{33}}\right)\frac{V_{GS31}}{R_4} \tag{3.12}$$

Since thermal voltage (V_T) possesses PTAT behaviour and gate-to-source voltage (V_{GS31}) has CTAT behaviour, these PTAT and CTAT behaviours can be cancelled out to achieve first-order temperature-compensated reference current by choosing appropriate values of resistances and aspect ratios of transistors.

Now, the high-order curvature-compensated reference current I_{REF} can be obtained using a curvature compensation circuit formed by transistors M17-M20. The current I_{REF} is expressed as

$$I_{REF}=I'_{REF1}-I'_{REF2} \tag{3.13}$$

The current I'_{REF1} across transistor M19 is given as

$$I'_{REF1}=\left(\frac{(W/L)_{19}}{(W/L)_{18}}\right)\left(\frac{(W/L)_{17}}{(W/L)_{16}}\right)I_{REF1} \tag{3.14}$$

where $(W/L)_{16}$, $(W/L)_{17}$, $(W/L)_{18}$ and $(W/L)_{19}$ are the aspect ratios of transistors M16, M17, M18 and M19, respectively.

Substituting the value of I_{REF1} from equation (3.11) in equation (3.14), the current I'_{REF1} is modified as

$$I'_{REF1}=\left(\frac{(W/L)_{19}}{(W/L)_{18}}\right)\left(\frac{(W/L)_{17}}{(W/L)_{16}}\right)\left(\frac{(W/L)_{14}}{(W/L)_{9}}\right)\frac{\eta V_T}{R_2}\ln\left(\frac{(W/L)_{12}}{(W/L)_{13}}\right)+$$
$$\left(\frac{(W/L)_{19}}{(W/L)_{18}}\right)\left(\frac{(W/L)_{17}}{(W/L)_{16}}\right)\left(\frac{(W/L)_{15}}{(W/L)_{2}}\right)\left(\frac{V_{GS4}}{R_1}\right) \tag{3.15}$$

The current I'_{REF1} can also be written as

$$I'_{REF1}=\alpha_1 \frac{V_T}{R_2} \ln N_{REF1} +\beta_1 \frac{V_{GS4}}{R_1} \tag{3.16}$$

where $\alpha_1=\eta \left(\frac{(W/L)_{19}}{(W/L)_{18}}\right)\left(\frac{(W/L)_{17}}{(W/L)_{16}}\right)\left(\frac{(W/L)_{14}}{(W/L)_{9}}\right)$,

$\beta_1= \left(\frac{(W/L)_{19}}{(W/L)_{18}}\right)\left(\frac{(W/L)_{17}}{(W/L)_{16}}\right)\left(\frac{(W/L)_{15}}{(W/L)_{2}}\right)$, and $N_{REF1}=\left(\frac{(W/L)_{12}}{(W/L)_{13}}\right)$

The current I'_{REF2} across transistor M20 can be written as

$$I'_{REF2}=\left(\frac{(W/L)_{20}}{(W/L)_{36}}\right) I_{REF2} \tag{3.17}$$

where $(W/L)_{20}$ and $(W/L)_{36}$ are the aspect ratios of transistors M20 and M36, respectively. Substituting the value of I_{REF2} from equation (3.12) in equation (3.17), current I'_{REF2} is modified as

$$I'_{REF2}=\left(\frac{(W/L)_{20}}{(W/L)_{36}}\right)\left(\frac{(W/L)_{35}}{(W/L)_{29}}\right)\frac{\eta V_T}{R_3} \ln\left(\frac{(W/L)_{22}}{(W/L)_{21}}\right)+ \left(\frac{(W/L)_{20}}{(W/L)_{36}}\right)\left(\frac{(W/L)_{34}}{(W/L)_{33}}\right)\frac{V_{GS31}}{R_4} \tag{3.18}$$

The current I'_{REF2} can also be written as

$$I'_{REF2}=\alpha_2 \frac{V_T}{R_3} \ln N_{REF2} +\beta_2 \frac{V_{GS31}}{R_4} \tag{3.19}$$

where $\alpha_2=\eta \left(\frac{(W/L)_{20}}{(W/L)_{36}}\right)\left(\frac{(W/L)_{35}}{(W/L)_{29}}\right)$, $\beta_2=\left(\frac{(W/L)_{20}}{(W/L)_{36}}\right)\left(\frac{(W/L)_{34}}{(W/L)_{33}}\right)$ and $N_{REF2}=\left(\frac{(W/L)_{22}}{(W/L)_{21}}\right)$

By substituting the values of I'_{REF1} and I'_{REF2} from equations (3.15) and (3.18) in equation (3.13), the current I_{REF} is obtained as

$$I_{REF}=\left(\frac{(W/L)_{19}}{(W/L)_{18}}\right)\left(\frac{(W/L)_{17}}{(W/L)_{16}}\right)\left(\frac{(W/L)_{14}}{(W/L)_{9}}\right)\frac{\eta V_T}{R_2} \ln\left(\frac{(W/L)_{12}}{(W/L)_{13}}\right)+ \left(\frac{(W/L)_{19}}{(W/L)_{18}}\right)\left(\frac{(W/L)_{17}}{(W/L)_{16}}\right)\left(\frac{(W/L)_{15}}{(W/L)_{2}}\right)\left(\frac{V_{GS4}}{R_1}\right)- \left(\frac{(W/L)_{20}}{(W/L)_{36}}\right)\left(\frac{(W/L)_{35}}{(W/L)_{29}}\right)\frac{\eta V_T}{R_3} \ln\left(\frac{(W/L)_{22}}{(W/L)_{21}}\right)- \left(\frac{(W/L)_{20}}{(W/L)_{36}}\right)\left(\frac{(W/L)_{34}}{(W/L)_{33}}\right)\frac{V_{GS31}}{R_4} \tag{3.20}$$

Using equation (3.20), the high-order curvature-compensated output reference voltage (V_{REF}) across the resistor (R_{REF}) is expressed as

$$V_{REF}=\left(I'_{REF1}-I'_{REF2}\right)R_{REF}=I_{REF}R_{REF} \tag{3.21}$$

From equation (3.21), it is clear that output reference voltage (V_{REF}) with a low temperature coefficient is obtained using a curvature compensation circuit by eliminating the higher-order temperature dependent terms.

3.4.1.2 Conditions for minimum temperature coefficients of SIFTCVRs

In the SIFTCVR-I of the proposed CMOS voltage reference-I, the condition for minimum temperature coefficient can be obtained by differentiating the output reference current of the SIFTCVR-I with respect to temperature and equating it to zero. Therefore, by differentiating the equation (3.11) with respect to temperature and equating it to zero, we have

$$\frac{\partial I_{REF1}}{\partial T}=\frac{(W/L)_{14}}{(W/L)_9}\frac{\eta\cdot\frac{\partial V_T}{\partial T}\ln\left(\frac{(W/L)_{12}}{(W/L)_{13}}\right)}{R_2}+\frac{(W/L)_{15}}{(W/L)_2}\frac{\frac{\partial V_{GS4}}{\partial T}}{R_1}=0 \tag{3.22}$$

Equation (3.22) can be written as

$$\frac{(W/L)_{14}}{(W/L)_9}\frac{\eta\cdot\frac{\partial V_T}{\partial T}\ln\left(\frac{(W/L)_{12}}{(W/L)_{13}}\right)}{R_2}=\frac{(W/L)_{15}}{(W/L)_2}\frac{-\frac{\partial V_{GS4}}{\partial T}}{R_1} \tag{3.23}$$

After simplification, the condition for the minimum temperature coefficient of SIFTCVR-I is obtained as

$$\frac{R_1}{R_2}=\frac{(W/L)_{15}}{(W/L)_2}\cdot\frac{(W/L)_9}{(W/L)_{14}}\cdot\frac{-\frac{\partial V_{GS4}}{\partial T}}{\eta.\ln\left(\frac{(W/L)_{12}}{(W/L)_{13}}\right)\frac{\partial V_T}{\partial T}} \tag{3.24}$$

Similarly, the condition for the minimum temperature coefficient of SIFTCVR-II is expressed as

$$\frac{R_4}{R_3}=\frac{(W/L)_{34}}{(W/L)_{33}}\cdot\frac{(W/L)_{29}}{(W/L)_{35}}\cdot\frac{-\frac{\partial V_{GS31}}{\partial T}}{\eta.\ln\left(\frac{(W/L)_{22}}{(W/L)_{21}}\right)\frac{\partial V_T}{\partial T}} \tag{3.25}$$

Equations (3.24) and (3.25) give the relations between resistors, aspect ratios of MOS transistors and technology-dependent parameters to obtain the minimum temperature coefficient (TC) for

SIFTCVR-I and SIFTCVR-II, respectively. The technology-dependent parameters η, V_T and V_{GS} are fixed for the particular technology while resistors and the aspect ratios of transistors are the only free variables that can be selected during circuit designing to attain the minimum TC. But, the high-order temperature dependent terms are not compensated in SIFTCVR-I and SIFTCVR-II. Therefore, to achieve low temperature sensitivity, a high-order curvature compensation technique is employed in the proposed CMOS voltage reference-I for the cancellation of high-order temperature dependent terms.

3.4.1.3 Temperature stability improvement using a high-order curvature compensation technique

In the high-order curvature compensation technique introduced in the proposed CMOS voltage reference-I, it is necessary that the derivatives of currents I'_{REF1} and I'_{REF2} with respect to temperature (i.e. $\frac{\partial I'_{REF1}}{\partial T}$ and $\frac{\partial I'_{REF2}}{\partial T}$) must be equal at a minimum of two points to achieve high-order curvature compensation so that $\frac{\partial I_{REF}}{\partial T}$ becomes zero at two points [24]. These two points are used to obtain the minimum and maximum values of the current I_{REF}.

From equations (3.15) and (3.18), it is clear that the currents I'_{REF1} and I'_{REF2} depend on the gate-to-source voltages V_{GS4} and V_{GS31}, respectively. Since the voltages V_{DS4} and V_{DS31} are greater than $4V_T$, the gate-to-source voltages V_{GS4} and V_{GS31} can be expressed in equations (3.26) and (3.27), respectively using equation (1.3).

$$V_{GS4}=V_{TH}+\eta V_T \ln\left(\frac{I'_9 L q^2}{\mu_0 T_0^{\,2} C_{ox} W(\eta-1)k^2 T^{2-m}}\right) = V_{TH}+\eta V_T \left(\ln(A_1)-(2-m)\ln(T)\right) \quad (3.26)$$

$$V_{GS31}=V_{TH}+\eta V_T \ln\left(\frac{I_{18} L q^2}{\mu_0 T_0^{\,2} C_{ox} W(\eta-1)k^2 T^{2-m}}\right) = V_{TH}+\eta V_T \left(\ln(A_2)-(2-m)\ln(T)\right) \quad (3.27)$$

where $A_1=\frac{I'_9 L q^2}{\mu_0 T_0^{\,2} C_{ox} W(\eta-1)k^2}$ and $A_2=\frac{I_{18} L q^2}{\mu_0 T_0^{\,2} C_{ox} W(\eta-1)k^2}$.

However, for appropriate design, the gate-to-source voltage relation can be expressed as a function of reference temperature (T_r). Using equation (3.26), the gate-to-source voltage V_{GS4} at the reference temperature (T_r) is given as [116].

$$V_{GS4}(T_r)=V_{TH}(T_r)+\eta V_{T_r}\left(\ln(A_1)-(2-m)\ln(T_r)\right) \quad (3.28)$$

where $V_{GS4}(T_r)$ is the gate-to-source voltage of transistor M4 at the reference temperature T_r, V_{Tr} is the thermal voltage at the reference temperature T_r and $V_{TH}(T_r)$ is the threshold voltage at a reference temperature T_r.

From equation (3.28), the constant $\ln(A_1)$ at reference temperature (T_r) is defined as

$$\ln(A_1)=\frac{V_{GS4}(T_r)+(2-m)\eta V_{T_r}\ln(T_r)-V_{TH}(T_r)}{\eta V_{T_r}} \tag{3.29}$$

Using equations (3.26) and (3.29), the gate-to-source voltage V_{GS4} is expressed as

$$V_{GS4}=V_{TH}+\frac{V_T}{V_{T_r}}\left(V_{GS4}(T_r)-V_{TH}(T_r)\right)-(2-m)V_T\ln\left(\frac{T}{T_r}\right) \tag{3.30}$$

Similarly, the gate-to-source voltage V_{GS31} is given as

$$V_{GS31}=V_{TH}+\frac{V_T}{V_{T_r}}\left(V_{GS31}(T_r)-V_{TH}(T_r)\right)-(2-m)V_T\ln\left(\frac{T}{T_r}\right) \tag{3.31}$$

Using Taylor series expansion, the logarithmic terms of equations (3.30) and (3.31) can be expanded for the cancellation of linear as well as high-order temperature dependent terms to obtain a high-order curvature-compensated reference voltage.

Now, the Taylor series expansion of the logarithmic term $\left(T\ln\left(\frac{T}{T_r}\right)\right)$ can be written as

$$T\ln\left(\frac{T}{T_r}\right)=b_0+b_1(T-T_r)+b_2\frac{(T-T_r)^2}{2!}+b_3\frac{(T-T_r)^3}{3!}+\ldots\ldots+b_n\frac{(T-T_r)^n}{n!} \tag{3.32}$$

where $b_i=\left.\frac{\partial^i\left(T\ln\left(\frac{T}{T_r}\right)\right)}{\partial T^i}\right|_{T=T_r}$; i=1, 2, 3, ……, n.

Using equations (3.30), (3.31) and (3.32), gate-to-source voltages V_{GS4} and V_{GS31} for third-order polynomials (it is important to mention that these higher-order terms like T^2, T^3, …..etc., will also affect the lower-order terms since the expansion is done about temperature T_r, e.g., $(T-T_r)^3=T^3-T_r^3-3T^2T_r+3TT_r^2$) are obtained as

$$V_{GS4}=V_{TH}+\frac{T}{T_r}V_{GS4}(T_r)-\frac{T}{T_r}V_{TH}(T_r)+\frac{\eta k}{q}(m-2)(b_0+b_1T-b_1T_r+$$
$$b_2\frac{T^2}{2}+b_2\frac{T_r^2}{2}-b_2TT_r+\frac{b_3}{6}T^3-\frac{b_3}{6}T_r^3-\frac{b_3}{2}T^2T_r+\frac{b_3}{2}TT_r^2) \tag{3.33}$$

$$V_{GS31}=V_{TH}+\frac{T}{T_r}V_{GS31}(T_r)-\frac{T}{T_r}V_{TH}(T_r)+\frac{\eta k}{q}(m-2)(b_0+b_1T-b_1T_r+$$
$$b_2\frac{T^2}{2}+b_2\frac{T_r^2}{2}-b_2TT_r+\frac{b_3}{6}T^3-\frac{b_3}{6}T_r^3-\frac{b_3}{2}T^2T_r+\frac{b_3}{2}TT_r^2) \quad (3.34)$$

Substituting the values of V_{GS4} and V_{GS31} from (3.32) and (3.34) in (3.16) and (3.19), respectively, the currents I'_{REF1} and I'_{REF2} are obtained as

$$I'_{REF1}=T^3\frac{\beta_1}{R_1}\left(\frac{b_3}{6}(m-2)\frac{\eta k}{q}\right)+T^2\frac{\beta_1}{R_1}\left[\frac{\eta k}{q}(m-2)\left(\frac{b_2}{2}-\frac{b_3}{2}T_r\right)\right]+$$
$$T\frac{\beta_1}{R_1}\left[\frac{V_{GS4}(T_r)}{T_r}-\frac{V_{TH}(T_r)}{T_r}+\frac{\eta k}{q}(m-2)\left(b_1-\right.\right.$$
$$\left.\left.b_2T_r+\frac{b_3}{2}T_r^2\right)+\frac{\alpha_1R_1k}{\beta_1R_2q}\ln N_{REF1}-k_T\right]+$$
$$\frac{\beta_1}{R_1}\left[V_{TH}(T_0)+\frac{\eta k}{q}(m-2)\left(b_0-b_1T_r+b_2\frac{T_r^2}{2}-\frac{b_3}{6}T_r^3\right)\right] \quad (3.35)$$

$$I'_{REF2}=T^3\frac{\beta_2}{R_4}\left(\frac{b_3}{6}(m-2)\frac{\eta k}{q}\right)+T^2\frac{\beta_2}{R_4}\left[\frac{\eta k}{q}(m-2)\left(\frac{b_2}{2}-\frac{b_3}{2}T_r\right)\right]+$$
$$T\frac{\beta_2}{R_4}\left[\frac{V_{GS31}(T_r)}{T_r}-\frac{V_{TH}(T_r)}{T_r}+\frac{\eta k}{q}(m-2)\left(b_1-\right.\right.$$
$$\left.\left.b_2T_r+\frac{b_3}{2}T_r^2\right)+\frac{\alpha_2R_4k}{\beta_2R_3q}\ln N_{REF2}-k_T\right]+$$
$$\frac{\beta_2}{R_4}\left[V_{TH}(T_0)+\frac{\eta k}{q}(m-2)\left(b_0-b_1T_r+b_2\frac{T_r^2}{2}-\frac{b_3}{6}T_r^3\right)\right] \quad (3.36)$$

Now, substituting the values of I'_{REF1} and I'_{REF2} from equations (3.35) and (3.36) in equation (3.13), the high-order curvature-compensated current (I_{REF}) is given as

$$I_{REF}=(A_{3,REF1}-A_{3,REF2})T^3+(A_{2,REF1}-A_{2,REF2})T^2+(A_{1,REF1}-A_{1,REF2})T^1+(A_{0,REF1}-A_{0,REF2}) \quad (3.37)$$

where

$$A_{0,REF1}=\frac{\beta_1}{R_1}\left[V_{TH}(T_0)+\frac{\eta k}{q}(m-2)\left(b_0-b_1T_r+b_2\frac{T_r^2}{2}-\frac{b_3}{6}T_r^3\right)\right],$$

$$A_{0,REF2}=\frac{\beta_2}{R_4}\left[V_{TH}(T_0)+\frac{\eta k}{q}(m-2)\left(b_0-b_1T_r+b_2\frac{T_r^2}{2}-\frac{b_3}{6}T_r^3\right)\right],$$

$$A_{1,REF1}=\frac{\beta_1}{R_1}\left[\frac{V_{GS4}(T_r)}{T_r}-\frac{V_{TH}(T_r)}{T_r}+\frac{\eta k}{q}(m-2)\left(b_1-b_2T_r+\frac{b_3}{2}T_r^2\right)+\frac{\alpha_1 R_1 k}{\beta_1 R_2 q}\ln N_{REF1}-k_T\right],$$

$$A_{1,REF2}=\frac{\beta_2}{R_4}\left[\frac{V_{GS31}(T_r)}{T_r}-\frac{V_{TH}(T_r)}{T_r}+\frac{\eta k}{q}(m-2)\left(b_1-b_2T_r+\frac{b_3}{2}T_r^2\right)+\frac{\alpha_2 R_4 k}{\beta_2 R_3 q}\ln N_{REF2}-k_T\right],$$

$$A_{2,REF1}=\frac{\beta_1}{R_1}\left[\frac{\eta k}{q}(m-2)\left(\frac{b_2}{2}-\frac{b_3}{2}T_r\right)\right],$$

$$A_{2,REF2}=\frac{\beta_2}{R_4}\left[\frac{\eta k}{q}(m-2)\left(\frac{b_2}{2}-\frac{b_3}{2}T_r\right)\right],$$

$$A_{3,REF1}=\frac{\beta_1}{R_1}\left(\frac{b_3}{6}(m-2)\frac{\eta k}{q}\right), \text{ and}$$

$$A_{3,REF2}=\frac{\beta_2}{R_4}\left(\frac{b_3}{6}(m-2)\frac{\eta k}{q}\right).$$

The first-order and second-order derivatives of current I_{REF} can be expressed in equations (3.38) and (3.39), respectively.

$$\frac{\partial I_{REF}}{\partial T}=3\left(A_{3,REF1}-A_{3,REF2}\right)T^2+2(A_{2,REF1}-A_{2,REF2})T+(A_{1,REF1}-A_{1,REF2}) \tag{3.38}$$

$$\frac{\partial^2 I_{REF}}{\partial T^2}=6\left(A_{3,REF1}-A_{3,REF2}\right)T+2(A_{2,REF1}-A_{2,REF2}) \tag{3.39}$$

By choosing appropriate values of resistances and aspect ratios of transistors used in the proposed CMOS voltage reference-I, the coefficients $A_{i,REF1}$ and $A_{i,REF2}$ (i= 0 to 3) can be cancelled out and $\partial I_{REF}/\partial T$ becomes zero at two points. The current I_{REF} will have minimum and maximum values at these two points and the turning point where the I_{REF} changes from minimum to the maximum value is obtained by setting $\partial^2 I_{REF}/\partial T^2$ equals to zero. By choosing appropriate values of resistances and aspect ratios of transistors, the coefficients $(A_{i,REF1}- A_{i,REF2})|_{i=1,2,3}$ become zero and hence temperature dependent terms of equation (3.37) are cancelled out. The high-order curvature-compensated reference current is obtained as

$$I_{REF}= (A_{0,REF1}-A_{0,REF2}) \tag{3.40}$$

Using equations (3.21) and (3.40), the curvature-compensated output reference voltage (V_{REF}) of the proposed CMOS voltage reference-I is given as

$$V_{REF}= (A_{0,REF1}-A_{0,REF2})R_{REF} \tag{3.41}$$

From equation (3.41), it can be seen that the higher-order temperature dependent terms are eliminated and a less temperature-sensitive output reference voltage is obtained.

3.4.2 Analysis of proposed CMOS voltage reference-II

This section presents the output reference voltage expression and minimum temperature coefficient condition of the proposed CMOS voltage reference-II.

3.4.2.1 Output reference voltage

In the proposed CMOS voltage reference-II (Figure 3.4), the PTAT voltage (V_{PTAT}) across node A is generated by using the transistors M12 and M13 operating in the subthreshold region.
Since the voltages V_{DS12} and V_{DS13} are greater than $4V_T$, the gate-to-source voltages V_{GS12} and V_{GS13} can be written using equation (1.3) as

$$V_{GS12}=V_{TH}+\eta V_T \ln\left(\frac{I_{DS12}}{\mu C_{ox}(W/L)_{12}(\eta-1)V_T^2}\right) \tag{3.42}$$

$$V_{GS13}=V_{TH}+\eta V_T \ln\left(\frac{I_{DS13}}{\mu C_{ox}(W/L)_{13}(\eta-1)V_T^2}\right) \tag{3.43}$$

The voltage at node A is expressed as

$$V_A=V_{GS13}-V_{GS12} \tag{3.44}$$

Substituting the values of V_{GS12} and V_{GS13} from equations (3.42) and (3.43) in equation (3.44), the voltage at node A (V_A) is obtained as

$$V_A=\eta V_T \ln(N) \tag{3.45}$$

where $N=\frac{\left(\frac{W}{L}\right)_{12}}{\left(\frac{W}{L}\right)_{13}}$.

Now, OP-AMP1 with transistor M10 makes the negative feedback loop which results in equal potential at nodes A and B. Therefore, we can write

$$V_A=\eta V_T \ln(N)=V_B \tag{3.46}$$

From equation (3.46), it is observed that the voltages V_A and V_B are directly proportional to the thermal voltage, which confirms their PTAT behaviour.
The PTAT current I_{PTAT} flowing through resistor R_1 is expressed as

$$I_{PTAT}=\frac{V_B}{R_1}=\frac{\eta V_T \ln(N)}{R_1} \tag{3.47}$$

The potential at node C has CTAT behaviour due to the gate-to-source voltage of subthreshold transistor M13. The potentials at nodes C and D become equal due to the negative feedback formed by OP-AMP2 and M14, which is expressed as

$$V_C=V_D=V_{GS13}=V_{CTAT} \tag{3.48}$$

The CTAT current I_{CTAT} flowing through resistor R_2 is expressed as

$$I_{CTAT}=\frac{V_D}{R_2}=\frac{V_{GS13}}{R_2} \tag{3.49}$$

The currents I_{15} and I_{16} can be expressed as

$$I_{15}=\alpha.I_{PTAT} \tag{3.50}$$

$$I_{16}=\beta.I_{CTAT} \tag{3.51}$$

where $\alpha=\frac{\left(\frac{W}{L}\right)_{15}}{\left(\frac{W}{L}\right)_{10}}$ and $\beta=\frac{\left(\frac{W}{L}\right)_{16}}{\left(\frac{W}{L}\right)_{14}}$.

The current adder circuit is used to add PTAT and CTAT currents to obtain reference current I_{REF}. By applying KCL at node F, the reference current I_{REF} is obtained as

$$I_{REF}=I_{15}+I_{16}=\alpha.I_{PTAT}+\beta.I_{CTAT} \tag{3.52}$$

Substituting the values of currents I_{PTAT} and I_{CTAT} from equations (3.47) and (3.49), respectively in equation (3.52), the current I_{REF} is expressed as

$$I_{REF}=\alpha.\frac{\eta V_T \ln(N)}{R_1}+\beta.\frac{V_{GS13}}{R_2} \tag{3.53}$$

The output reference voltage V_{REF} across the resistor (R_{REF}) is given as

$$V_{REF}=R_{REF}.I_{REF} \tag{3.54}$$

Substituting the value of I_{REF} from equation (3.53) in equation (3.54), the output reference voltage V_{REF} at node F is obtained as

$$V_{REF}=R_{REF}.\left(\alpha.\frac{\eta V_T \ln(N)}{R_1}+\beta.\frac{V_{GS13}}{R_2}\right) \tag{3.55}$$

From equation (3.55), it is clear that the first term of the equation possesses a PTAT behaviour due to thermal voltage (V_T) and the second term possesses CTAT behaviour due to gate-to-source voltage (V_{GS13}). These PTAT and CTAT behaviours can be neutralized by selecting the

appropriate values of α, β, N, R_1, R_2, and R_{REF}. The resistance R_{REF} can also be reduced to keep the layout compact with the help of α and β.

3.4.2.2 Condition for minimum temperature coefficient of proposed CMOS voltage reference-II

The condition for minimum temperature coefficient can be obtained by differentiating the output reference voltage with respect to temperature and equating it to zero. Hence, by differentiating equation (3.55) with respect to temperature and equating it to zero, we get

$$\frac{\partial V_{REF}}{\partial T}=R_{REF}.\left(\alpha.\frac{\eta\frac{\partial V_T}{\partial T}\ln(N)}{R_1}+\beta.\frac{\frac{\partial V_{GS13}}{\partial T}}{R_2}\right)=0 \tag{3.56}$$

Equation (3.56) can be written as

$$\alpha.\frac{\eta\frac{\partial V_T}{\partial T}\ln(N)}{R_1}=\beta.\frac{-\frac{\partial V_{GS13}}{\partial T}}{R_2} \tag{3.57}$$

After simplification, the condition for the minimum temperature coefficient is obtained as

$$\frac{R_1}{R_2}=\frac{\alpha.\eta.\ln(N).\frac{\partial V_T}{\partial T}}{\beta.\frac{-\partial V_{GS13}}{\partial T}} \tag{3.58}$$

Equation (3.58) gives the relation between resistors (R_1 and R_2), ratios (α, β, and N) of aspect ratios, and technology-dependent parameters (η, V_T and V_{GS13}) to obtain the minimum TC. The equation shows that the resistors and ratios of aspect ratios are the only free variables that can be selected properly during the circuit designing.

3.4.3 Analysis of proposed CMOS voltage reference-III

This section addresses the output reference voltage expression and minimum temperature coefficient condition of the proposed CMOS voltage reference-III.

3.4.3.1 Output reference voltage

The current I_{CTAT1} of SICG-I (Figure 3.8) shows CTAT behaviour with the variations in temperature due to transistor M1 operating in the subthreshold region. The current I_{CTAT1} flowing through the resistance R_1 of SICG-I is expressed as

$$I_{CTAT1}=\frac{V_{GS1}}{R_1} \tag{3.59}$$

Similarly, I_{CTAT2} flowing through the resistance R_2 of SICG-II is expressed as

$$I_{CTAT2}=\frac{V_{GS15}}{R_2} \tag{3.60}$$

From equations (3.59) and (3.60), it can be seen that the currents I_{CTAT1} and I_{CTAT2} are directly proportional to the gate-to-source voltages of the transistors M1 and M15, respectively. These gate-to-source voltages of subthreshold transistors M1 and M15 decrease with an increase in temperature as discussed in section 1.2.1.1 of chapter 1. Thus, we can conclude that the currents I_{CTAT1} and I_{CTAT2} have the same CTAT behaviours. Also, the currents I_{CTAT1} and I_{CTAT2} are supply independent due to the formation of the negative feedback paths in SICG-I and SICG-II, respectively.

Substituting the value of V_{GS} from equation (1.3) in equations (3.59) and (3.60), we get

$$I_{CTAT1}=\frac{V_{TH1}+\eta V_T \ln\left(\frac{I_{DS1}}{\mu C_{ox}\left(\frac{W}{L}\right)_1 (\eta-1)V_T^2}\right)}{R_1} \tag{3.61}$$

$$I_{CTAT2}=\frac{V_{TH15}+\eta V_T \ln\left(\frac{I_{DS15}}{\mu C_{ox}\left(\frac{W}{L}\right)_{15} (\eta-1)V_T^2}\right)}{R_2} \tag{3.62}$$

Since the threshold voltage (V_{TH}) and mobility (μ) depend on temperature, the equations (3.61) and (3.62) can be written as

$$I_{CTAT1}=\frac{(V_{TH0}-k_{T1}.T)+\eta V_T \ln\left(\frac{I_{DS1}}{\mu_0 (T/T_0)^{-m} C_{ox}\left(\frac{W}{L}\right)_1 (\eta-1)V_T^2}\right)}{R_1} \tag{3.63}$$

$$I_{CTAT2}=\frac{(V_{TH0}-k_{T15}.T)+\eta V_T \ln\left(\frac{I_{DS15}}{\mu_0 (T/T_0)^{-m} C_{ox}\left(\frac{W}{L}\right)_{15} (\eta-1)V_T^2}\right)}{R_2} \tag{3.64}$$

where $V_{TH}=V_{TH0}-k_T.T$, $\mu=\mu_0(T/T_0)^{-m}$, V_{TH0} is the threshold voltage at room temperature, k_T is a temperature parameter of the threshold voltage (lies between 0.5 to 3 mV/℃), μ_0 is the mobility at room temperature, m is the mobility temperature exponent (lies between 1.5 to 2), I_{DS1} is the drain current of transistor M1 and I_{DS15} is the drain current of transistor M15.

Using equation (3.64), the current $N.I_{CTAT2}$ can be written as

$$N.I_{CTAT2}=N.\left(\frac{(V_{TH0}-k_{T15}.T)+\eta V_T \ln\left(\frac{I_{DS15}}{\mu_0(T/T_0)^{-m}C_{ox}\left(\frac{W}{L}\right)_{15}(\eta-1)V_T^2}\right)}{R_2}\right) \tag{3.65}$$

where scaling factor $N=\left(\frac{(W/L)_{11}}{(W/L)_{22}}\times\frac{(W/L)_{12}}{(W/L)_{19}}\times\frac{(W/L)_{14}}{(W/L)_{13}}\right)$.

The current $N.I_{CTAT2}$ is subtracted from I_{CTAT1} using the current subtractor and the temperature-compensated reference current I_{REF} is obtained as

$$I_{REF}=I_{CTAT1}-N.I_{CTAT2} \tag{3.66}$$

From equation (3.66), the output reference voltage V_{REF} can be expressed as

$$V_{REF}=(I_{CTAT1}-N.I_{CTAT2}).R_{REF} \tag{3.67}$$

Substituting the value**s** of I_{CTAT1} and I_{CTAT2} from equations (3.59) and (3.60) in equation (3.67), the output reference voltage V_{REF} is obtained as

$$V_{REF}=\left(\frac{V_{GS1}}{R_1}-N.\frac{V_{GS15}}{R_2}\right).R_{REF} \tag{3.68}$$

Equation (3.68) can be written as

$$V_{REF}=V_{GS1}.\frac{R_{REF}}{R_1}-N.V_{GS15}.\frac{R_{REF}}{R_2} \tag{3.69}$$

From equation (3.69), it can be seen that the first and second terms of output reference voltage depend on gate-to-source voltages that have the same CTAT behaviours.

Using equations (3.62), (3.64) and (3.67), the output reference voltage V_{REF} can also be expressed as

$$V_{REF}=\left((V_{TH0}-k_{T1}.T)+\eta V_T \ln\left(\frac{I_{DS1}}{\mu_0(T/T_0)^{-m}C_{ox}\left(\frac{W}{L}\right)_1(\eta-1)V_T^2}\right)\right).\frac{R_{REF}}{R_1}-$$
$$N.\left((V_{TH0}-k_{T15}.T)+\eta V_T \ln\left(\frac{I_{DS15}}{\mu_0(T/T_0)^{-m}C_{ox}\left(\frac{W}{L}\right)_{15}(\eta-1)V_T^2}\right)\right).\frac{R_{REF}}{R_2} \quad (3.70)$$

Using the value of scaling factor N from equation (3.65), equation (3.70) is modified as

$$V_{REF}=\left((V_{TH0}-k_{T1}.T)+\eta V_T \ln\left(\frac{I_{DS1}}{\mu_0(T/T_0)^{-m}C_{ox}\left(\frac{W}{L}\right)_1(\eta-1)V_T^2}\right)\right).\frac{R_{REF}}{R_1}-$$
$$\left(\frac{(W/L)_{11}}{(W/L)_{22}}\times\frac{(W/L)_{12}}{(W/L)_{19}}\times\frac{(W/L)_{14}}{(W/L)_{13}}\right).$$
$$\left((V_{TH0}-k_{T15}.T)+\eta V_T \ln\left(\frac{I_{DS15}}{\mu_0(T/T_0)^{-m}C_{ox}\left(\frac{W}{L}\right)_{15}(\eta-1)V_T^2}\right)\right).\frac{R_{REF}}{R_2} \quad (3.71)$$

If, $\left(\frac{W}{L}\right)_1=\frac{W}{L}$, $\left(\frac{W}{L}\right)_{15}=\frac{5}{2}.\frac{W}{L}$, $\left(\frac{W}{L}\right)_{13}=\frac{125}{9}.\frac{W}{L}$, $\left(\frac{W}{L}\right)_{14}=\frac{25}{9}.\frac{W}{L}$,

$\left(\frac{W}{L}\right)_{11}=\left(\frac{W}{L}\right)_{12}=\left(\frac{W}{L}\right)_{19}=\left(\frac{W}{L}\right)_{22}=\frac{100}{3}.\frac{W}{L}$, $\frac{R_{REF}}{R_1}\approx\frac{R_{REF}}{R_2}$=R, and K_{T1}=K_{T15}=K_T then equation (3.71) can be written as

$$V_{REF}=\left(\frac{4}{5}.(V_{TH0}-k_T.T)+\eta V_T \ln\left(\frac{(I_{DS1}).\left(\frac{2}{5}I_{DS15}\right)^{-\frac{1}{5}}.}{\left(\frac{W}{L}\mu_0(T/T_0)^{-m}C_{ox}(\eta-1)V_T^2\right)^{-\frac{4}{5}}}\right)\right).R \quad (3.72)$$

From equation (3.72), it is evident that the output reference voltage V_{REF} depends on the technology-dependent parameters (K_T, C_{ox}, V_{TH0}, V_T, μ, and η), the aspect ratio (W/L) of the transistor, and resistance (R).

3.4.3.2 Condition for minimum temperature coefficient of proposed CMOS voltage reference-III

The derivative of the output reference voltage (given in equation (3.70)) with respect to temperature defines the temperature coefficient (TC) as

$$TC=\frac{\partial V_{REF}}{\partial T}=\left(\frac{\partial(V_{TH0}-k_{T1}.T)}{\partial T}+\frac{\partial\left(\frac{\eta kT}{q}\ln\left(\frac{I_{DS1}q^2}{\mu_0 T_0^{\,2} C_{ox}\left(\frac{W}{L}\right)_1(\eta-1)k^2}\right)\right)}{\partial T}\right).\frac{R_{REF}}{R_1}-$$

$$N.\left(\frac{\partial(V_{TH0}-k_{T15}.T)}{\partial T}+\frac{\partial\left(\frac{\eta kT}{q}\ln\left(\frac{I_{DS15}q^2}{\mu_0 T_0^{\,2} C_{ox}\left(\frac{W}{L}\right)_{15}(\eta-1)k^2}\right)\right)}{\partial T}\right).\frac{R_{REF}}{R_2} \quad (3.73)$$

$$TC=\left(-k_T+\frac{\eta k}{q}\ln\left(\frac{I_{DS1}.A}{\left(\frac{W}{L}\right)_1}\right)\right).\frac{1}{R_1}-\left(-N.k_T+\frac{N\eta k}{q}\ln\left(\frac{I_{DS15}.A}{\left(\frac{W}{L}\right)_{15}}\right)\right).\frac{1}{R_2} \quad (3.74)$$

where $A=\frac{q^2}{\mu_0 T_0^{\,2} C_{ox}(\eta-1)k^2}$ and $k_{T1}=k_{T15}=k_T$.

$$TC=N.k_T-k_T.\frac{R_2}{R_1}-\frac{\eta k}{q}\left(\ln\left(\frac{I_{DS15}.A}{\left(\frac{W}{L}\right)_{15}}\right)^N-\ln\left(\frac{I_{DS1}.A}{\left(\frac{W}{L}\right)_1}\right).\frac{R_2}{R_1}\right) \quad (3.75)$$

$$TC=k_T\left(N-\frac{R_2}{R_1}\right)-\frac{\eta k}{q}\left(\ln\left(\frac{I_{DS15}.A}{\left(\frac{W}{L}\right)_{15}}\right)^N-\ln\left(\frac{I_{DS1}.A}{\left(\frac{W}{L}\right)_1}\right)^{R_2/R_1}\right) \quad (3.76)$$

$$TC=k_T\left(N-\frac{R_2}{R_1}\right)-\frac{\eta k}{q}\left(\ln\left(\left(\frac{I_{DS15}}{\left(\frac{W}{L}\right)_{15}}\right)^N\times\left(\frac{\left(\frac{W}{L}\right)_1}{I_{DS1}}\right)^{R_2/R_1}\right)+\ln\left(A^{N-R_2/R_1}\right)\right) \tag{3.77}$$

After simplification, the TC is obtained as

$$TC=\left(N-\frac{R_2}{R_1}\right)\left(k_T-\frac{\eta k}{q}\ln(A)\right)-\frac{\eta k}{q}\ln\left(\left(\frac{I_{DS15}}{\left(\frac{W}{L}\right)_{15}}\right)^N\times\left(\frac{\left(\frac{W}{L}\right)_1}{I_{DS1}}\right)^{R_2/R_1}\right) \tag{3.78}$$

The expressions for I_{DS1} and I_{DS15} can be written as

$$I_{DS1}=\left(V_{GS1}/R_1\right).\left(\frac{(W/L)_7}{(W/L)_8}.\frac{(W/L)_4}{(W/L)_5}\right) \tag{3.79}$$

$$I_{DS15}=\left(V_{GS15}/R_2\right).\left(\frac{(W/L)_{21}}{(W/L)_{22}}.\frac{(W/L)_{18}}{(W/L)_{19}}\right) \tag{3.80}$$

The values of currents I_{DS1} and I_{DS15} have been substituted in equation (3.78) from equations (3.79) and (3.80) and then the simplified equation (3.78) is equated to zero to obtain the condition for minimum temperature coefficient as

$$R_1=\frac{B.R_2+\frac{\eta k}{q}.R_2\left(\ln\left(\frac{\alpha}{V_{GS1}}\right)+\ln\left(\frac{R_2}{p}\right)-\frac{1}{p}\ln(R_2)\right)}{N\left(B-\frac{\eta k}{q}\ln\left(\frac{V_{GS15}}{\beta}\right)\right)} \tag{3.81}$$

where $R_2=p.R_1$, $B=\left(k_T-\frac{\eta k}{q}\ln(A)\right)$, $\alpha=\frac{(W/L)_1.(W/L)_5.(W/L)_8}{(W/L)_4.(W/L)_7}$, and $\beta=\frac{(W/L)_{19}.(W/L)_{22}}{(W/L)_{15}.(W/L)_{18}.(W/L)_{21}}$.

From the equation (3.81), it is clear that μ_0, k_T, C_{OX}, and η are technology-dependent parameters, whereas resistances (R_1 and R_2) and the aspect ratios of transistors (M1 and M5) are the only free variables that can be selected during circuit designing to obtain the condition of minimum temperature coefficient.

3.4.4 Analysis of proposed CMOS voltage reference-IV

The expressions of the output reference voltage and minimum temperature coefficient condition of the proposed CMOS voltage reference-IV is presented in this section.

3.4.4.1 Output reference voltage

In the proposed CMOS voltage reference-IV (Figure 3.10), the CTAT voltages across nodes A and node E are generated using the transistors M12 and M10, respectively. The transistors M12 and M10 are working in the subthreshold region. Since the drain-to-source voltages $V_{DS,12}$ and $V_{DS,10}$ are greater than $4V_T$, the gate-to-source voltages $V_{GS,12}$ and $V_{GS,10}$ of transistors M12 and M10, respectively can be expressed as

$$V_{GS,12}=V_{TH}+\eta V_T \ln\left(\frac{I_{DS,12}}{\left(\frac{W}{L}\right)_{12}.\mu C_{ox}(\eta-1)V_T^2}\right) \tag{3.82}$$

$$V_{GS,10}=V_{TH}+\eta V_T \ln\left(\frac{I_{DS,10}}{\left(\frac{W}{L}\right)_{10}.\mu C_{ox}(\eta-1)V_T^2}\right) \tag{3.83}$$

The operational amplifier OP-AMP1' and transistor M8 form a negative feedback loop that provides the equal voltage at nodes A and B, which can be expressed as

$$V_A=V_{GS,12}=V_{TH}+\eta V_T \ln\left(\frac{I_{DS,12}}{\left(\frac{W}{L}\right)_{12}.\mu C_{ox}(\eta-1)V_T^2}\right)=V_B \tag{3.84}$$

Similarly, the operational amplifier OP-AMP2' and transistor M13 form a negative feedback loop that provides the equal voltage at nodes E and F which can be expressed as

$$V_E=V_{GS,10}=V_{TH}+\eta V_T \ln\left(\frac{I_{DS,10}}{\left(\frac{W}{L}\right)_{10}.\mu C_{ox}(\eta-1)V_T^2}\right)=V_F \tag{3.85}$$

The current I_{CTAT1} flowing through the resistance R_1 of CCG-I is given as

$$I_{CTAT1}=\frac{V_B}{R_1}=\frac{V_{GS,12}}{R_1} \tag{3.86}$$

Similarly, I_{CTAT2} flowing through the resistance R_2 of CCG-II is expressed as

$$I_{CTAT2}=\frac{V_F}{R_2}=\frac{V_{GS,10}}{R_2} \tag{3.87}$$

The currents I_{CTAT1} and I_{CTAT2} are copied to the transistors M14 and M17 and hence, the currents I_{14} and I_{17} can be expressed as

$$I_{14}=\alpha_1.I_{CTAT1} \tag{3.88}$$

$$I_{17}=\alpha_2.I_{CTAT2} \tag{3.89}$$

where $\alpha_1=\frac{\left(\frac{W}{L}\right)_{14}}{\left(\frac{W}{L}\right)_{8}}$ and $\alpha_2=\frac{\left(\frac{W}{L}\right)_{17}}{\left(\frac{W}{L}\right)_{16}}\times\frac{\left(\frac{W}{L}\right)_{15}}{\left(\frac{W}{L}\right)_{13}}$.

The current subtractor circuit is used to subtract the CTAT currents at node G' to obtain reference current I_{REF}. The reference current I_{REF} at node G' is expressed as

$$I_{REF}=I_{14}-I_{17}=\alpha_1.I_{CTAT1}-\alpha_2.I_{CTAT2} \tag{3.90}$$

Using equation (3.90), the output reference voltage (V_{REF}) across the resistor (R_{REF}) is given as

$$V_{REF}=I_{REF}.R_{REF}=(\alpha_1.I_{CTAT1}-\alpha_2.I_{CTAT2}).R_{REF} \tag{3.91}$$

Using equations (3.86), (3.87) and (3.91), the output reference voltage V_{REF} is obtained as

$$V_{REF}=\alpha_1.V_{GS,12}.\frac{R_{REF}}{R_1}-\alpha_2.V_{GS,10}.\frac{R_{REF}}{R_2} \tag{3.92}$$

From equation (3.92), it is clear that the first and second terms of output reference voltage possess CTAT behaviours due to the dependencies on the gate-to-source voltages of transistors M12 and M10 working in the subthreshold region.

Using equations (1.3), (3.84), (3.85) and (3.91), the output reference voltage V_{REF} can also be expressed as

$$V_{REF}=\left((V_{TH0}-k_{T12}.T)+\eta V_T\ln\left(\frac{I_{DS12}}{\left(\frac{W}{L}\right)_{12}\mu_0(T/T_0)^{-m}C_{ox}(\eta-1)V_T^2}\right)\right)\alpha_1.\frac{R_{REF}}{R_1}-$$
$$\left((V_{TH0}-k_{T10}.T)+\eta V_T\ln\left(\frac{I_{DS10}}{\left(\frac{W}{L}\right)_{10}\mu_0(T/T_0)^{-m}C_{ox}(\eta-1)V_T^2}\right)\right)\alpha_2.\frac{R_{REF}}{R_2} \tag{3.93}$$

Using the values of scaling factors α_1 and α_2 from equations (3.88) and (3.89), V_{REF} can be written as

$$V_{REF}=\left(\frac{\left(\frac{W}{L}\right)_{14}}{\left(\frac{W}{L}\right)_{8}}\right).\left((V_{TH0}-k_{T12}.T)+\eta V_T \ln\left(\frac{I_{DS12}}{\left(\frac{W}{L}\right)_{12}\mu_0(T/T_0)^{-m}C_{ox}(\eta-1)V_T^2}\right)\right).\frac{R_{REF}}{R_1}-$$

$$\left(\frac{\left(\frac{W}{L}\right)_{17}}{\left(\frac{W}{L}\right)_{16}}\times\frac{\left(\frac{W}{L}\right)_{15}}{\left(\frac{W}{L}\right)_{13}}\right).\left((V_{TH0}-k_{T10}.T)+\eta V_T \ln\left(\frac{I_{DS10}}{\left(\frac{W}{L}\right)_{10}\mu_0(T/T_0)^{-m}C_{ox}(\eta-1)V_T^2}\right)\right).\frac{R_{REF}}{R_2} \quad (3.94)$$

If, $\left(\frac{W}{L}\right)_4=\frac{W}{L}$, $\left(\frac{W}{L}\right)_{12}=\frac{10}{2}.\frac{W}{L}$, $\left(\frac{W}{L}\right)_{13}=\frac{2}{1}.\frac{W}{L}$, $\left(\frac{W}{L}\right)_{14}=\frac{3}{1}.\frac{W}{L}$, $\left(\frac{W}{L}\right)_{15}=\frac{W}{L}$, $\left(\frac{W}{L}\right)_{16}=\frac{1}{2}.\frac{W}{L}$, $\left(\frac{W}{L}\right)_{17}=\frac{1}{2}.\frac{W}{L}$, $\frac{R_{REF}}{R_1}\approx\frac{R_{REF}}{R_2}=R$, and $K_{T10}=K_{T12}=K_T$ then equation (3.94) can be expressed as

$$V_{REF}=\left(\frac{5}{2}.(V_{TH0}-k_T.T)+\eta V_T \ln\left(\frac{(I_{DS12})^3.(I_{DS10})^{-\frac{1}{2}}.}{\left(\frac{W}{L}\mu_0(T/T_0)^{-m}C_{ox}(\eta-1)V_T^2\right)^{-\frac{5}{2}}}\right)-5.175\right).R \quad (3.95)$$

From equation (3.95), it is clear that the output reference voltage depends on the technology-dependent parameters (V_{TH0}, K_T, V_T, μ, and η), the size (W/L) of the MOS transistor, and resistor (R).

3.4.4.2 Condition for minimum temperature coefficient of proposed CMOS voltage reference-IV

By differentiating the output reference voltage with respect to temperature, the condition for minimum temperature coefficient can be obtained. Hence, by differentiating equation (3.93) with respect to temperature and equating it to zero, we get equation (3.96).

$$TC=\frac{\partial V_{REF}}{\partial T}=\left(\frac{\partial(V_{TH0}-k_{T12}.T)}{\partial T}+\frac{\partial\left(\frac{\eta kT}{q}\ln\left(\frac{I_{DS12}q^2}{\left(\frac{W}{L}\right)_{12}\mu_0 T_0^2 C_{ox}(\eta-1)k^2}\right)\right)}{\partial T}\right)\alpha_1.\frac{R_{REF}}{R_1}-$$

$$\left(\frac{\partial(V_{TH0}-k_{T10}.T)}{\partial T}+\frac{\partial\left(\frac{\eta kT}{q}\ln\left(\frac{I_{DS10}q^2}{\left(\frac{W}{L}\right)_{10}\mu_0 T_0^2 C_{ox}(\eta-1)k^2}\right)\right)}{\partial T}\right)\alpha_2.\frac{R_{REF}}{R_2}=0 \quad (3.96)$$

Equation (3.96) can be written as

$$\left(-k_T+\frac{\eta k}{q}\ln\left(\frac{I_{DS12}.C_1}{\left(\frac{W}{L}\right)_{12}}\right)\right)\alpha_1.\frac{R_{REF}}{R_1}-\left(-k_T+\frac{\eta k}{q}\ln\left(\frac{I_{DS10}.C_1}{\left(\frac{W}{L}\right)_{10}}\right)\right)\alpha_2.\frac{R_{REF}}{R_2}=0 \quad (3.97)$$

where $C_1=\frac{q^2}{\mu_0 T_0^2 C_{ox}(\eta-1)k^2}$ and $k_{T10}=k_{T12}=k_T$.

Equation (3.97) can also be expressed as

$$\left(\alpha_2.\frac{R_1}{R_2}-\alpha_1\right).C_2=\frac{\eta k}{q}\left(\alpha_2.\frac{R_1}{R_2}.\ln\left(\frac{I_{DS10}}{\left(\frac{W}{L}\right)_{10}}\right)-\alpha_1\ln\left(\frac{I_{DS12}}{\left(\frac{W}{L}\right)_{12}}\right)\right) \quad (3.98)$$

where $C_2=\left(k_T-\frac{\eta k}{q}\ln(C_1)\right)$.

After simplification, the equation (3.98) is given as

$$\frac{R_1}{R_2}=\frac{C_2-\frac{\eta k}{q}\ln(I_{DS12}/(W/L)_{12})}{C_2-\frac{\eta k}{q}\ln(I_{DS10}/(W/L)_{10})} \quad (3.99)$$

Equation (3.99) provides the relationship between resistors (R_1 and R_2) and aspect ratios of the transistors ($(W/L)_{10}$ and $(W/L)_{12}$). From the equation, it is clear that some of the parameters such

as k_T, C_{OX}, μ_0, and η are technology-dependent while some of the parameters that can be selected during circuit designing are values of resistors and aspect ratios of MOS transistors.

3.5 Design considerations used in the proposed CMOS voltage references

The various design considerations used in the proposed CMOS voltage references (I, II, III and IV) are discussed in this section.

3.5.1 Subthreshold conduction

To ensure the subthreshold region operation of MOS transistors used in proposed CMOS voltage references, the MOS transistor's gate-to-source voltage (V_{GS}) must be less than the threshold voltage (V_{TH}) which is expressed as

$$V_{GS}<V_{TH0}-k_T.T_{max} \tag{3.100}$$

where V_{TH} ($= V_{TH0}-k_T.T_{max}$) is the threshold voltage of the MOS transistor at maximum operating temperature.

3.5.2 Process variability

The devices used in an IC will usually deviate from the designed values due to the variation in the manufacturing environment is known as process variation. The process variability is an important parameter in the designing of analog circuits. The effect of process variability depends on the aspect ratios of the MOS transistors used in the circuit. The effect of process variability can be approximated by using the mathematical relation of the standard deviation of the threshold voltage and is expressed as [117].

$$\sigma^2_{V_{TH}} = \frac{A^2}{W.L} \tag{3.101}$$

where A is the technology-dependent coefficient, W is the effective channel width and L is the effective channel length of the MOS transistor.

From equation (3.101), it is observed that the large aspect ratio of the MOS transistor helps in decreasing the process variability. Hence, large values of lengths and widths of MOS transistors are selected in the proposed CMOS voltage references to achieve good process stability.

3.5.3 Transistor size

The appropriate aspect ratios of the MOS transistors help to achieve good performance parameters of the circuit. The temperature-compensated output reference voltages of the

proposed CMOS voltage references are obtained by selecting the proper aspect ratios of the MOS transistors.

3.5.4 Minimum supply voltage

In this section, the selections of minimum values of the supply voltages for proposed CMOS voltage references (I, II, III and IV) are explained.

3.5.4.1 Minimum supply voltage for proposed CMOS voltage reference-I

For the proposed CMOS voltage reference-I (Figure 3.2), the supply voltage (V_{DD}) requirement can be expressed as

$$V_{DD} \geq |V_{DS,19}| + V_{REF} \tag{3.102}$$

where $V_{DS,19}$ is the drain-to-source voltage of the MOS transistor M19 and V_{REF} is the output reference voltage.

From equation (3.102), it can be seen that the supply voltage depends on the drain-to-source voltage of transistor M19 operating in the subthreshold region and the reference voltage.

Also, from equations (1.1) and (1.2), it is clear that the drain-to-source current is almost independent of the drain-to-source voltage when $V_{DS} \gg 4V_T$. So, the minimum value of supply voltage ($V_{DD,min}$) for the proposed CMOS voltage reference-I is given as

$$V_{DD,min} \geq 4V_{T,max} + V_{REF} \tag{3.103}$$

where $V_{T,max}$ is the thermal voltage at maximum operating temperature.

3.5.4.2 Minimum supply voltage for proposed CMOS voltage reference-II

The supply voltage (V_{DD}) requirement for the proposed CMOS voltage reference-II (Figure 3.4), can be written as

$$V_{DD} \geq \max\left[|V_{DS,15}|, |V_{DS,16}|\right] + V_{REF} \tag{3.104}$$

where $V_{DS,15}$ is the drain-to-source voltage of transistors M15, $V_{DS,16}$ is the drain-to-source voltage of transistor M16, and V_{REF} is the output reference voltage.

From equation (3.104), it can be seen that the supply voltage depends on the maximum value of the drain-to-source voltage of transistor M15 or M16 operating in the subthreshold region and the reference voltage. Also, from equations (1.1) and (1.2), it is clear that the drain-to-source

current is almost independent of the drain-to-source voltage when $V_{DS} \gg 4V_T$. So, the minimum value of supply voltage ($V_{DD,min}$) for the proposed CMOS voltage reference-II is expressed as

$$V_{DD,min} \geq 4V_{T,max} + V_{REF} \tag{3.105}$$

where $V_{T,max}$ is the thermal voltage at maximum operating temperature.

3.5.4.3 Minimum supply voltage for proposed CMOS voltage reference-III

For the proposed CMOS voltage reference-III (Figure 3.8), the supply voltage (V_{DD}) requirement can be expressed as

$$V_{DD} \geq |V_{DS,9}| + |V_{DS,10}| + V_{REF} \tag{3.106}$$

where $V_{DS,9}$ is the drain-to-source voltage of transistors M9, $V_{DS,10}$ is the drain-to-source voltage of transistor M10, and V_{REF} is the output reference voltage.

From equation (3.106), it can be seen that the supply voltage depends on the drain-to-source voltages of the transistors (M9 and M10) operating in the subthreshold region and the reference voltage.

Also, from equations (1.1) and (1.2), it is clear that the drain-to-source current is almost independent of the drain-to-source voltage when $V_{DS} \gg 4V_T$. So, the minimum value of supply voltage ($V_{DD,min}$) for the proposed CMOS voltage reference-III is given as

$$V_{DD,min} \geq 4V_{T,max} + 4V_{T,max} + V_{REF} \text{ or } V_{DD,min} \geq 8V_{T,max} + V_{REF} \tag{3.107}$$

where $V_{T,max}$ is the thermal voltage at the maximum operating temperature.

3.5.4.4 Minimum supply voltage for proposed CMOS voltage reference-IV

The minimum supply voltage (V_{DD}) requirement for the proposed CMOS voltage reference-IV (Figure 3.10), can be written as

$$V_{DD} \geq |V_{DS,14}| + V_{REF} \tag{3.108}$$

where $V_{DS,14}$ is the drain-to-source voltage of the transistor M14, and V_{REF} is the output reference voltage.

From equation (3.108), it is clear that the supply voltage depends on the drain-to-source voltage of transistor M14 operating in the subthreshold region and the output reference voltage.

Also, from equations (1.1) and (1.2), it is observed that when drain-to-source voltage is greater than $4V_T$ then drain-to-source current is almost independent of drain-to-source voltage. So, the

minimum value of supply voltage ($V_{DD,min}$) for the proposed CMOS voltage reference-IV is expressed as

$$V_{DD,min} \geq 4V_{T,max} + V_{REF} \tag{3.109}$$

where $V_{T,max}$ is the thermal voltage at maximum operating temperature.

3.6 Trimming circuit

In order to guarantee the accuracy required by the voltage reference circuit beyond the limitations of process variations after chip tape-out is achieved by using a trimming circuit. The process variations are mainly due to the deviation in the circuit elements. The circuit elements used in the proposed CMOS voltage references are MOS transistors and resistances. These process variations can be compensated by using trimming circuits but trimming at more than one circuit element is very expensive. Therefore, a typical trimming procedure only provides the calibration of one circuit element to adjust a particular parameter of the voltage reference. Thus, a resistance trimming circuit can be used to compensate the process variations of the proposed CMOS voltage references. The resistance trimming circuit shown in Figure 3.11 can be used to trim the resistance R_{REF} of the proposed CMOS voltage references. To cover the trimming range, four bits are used to control the switches S_3, S_2, S_1 and S_0. The switches S_3 and S_0 are the highest bit and lowest bit, respectively. The disconnection and closure of the switch are considered as 1 and 0, respectively. At the nominal conditions, the trimming bits are given as "0000" for $S_3S_2S_1S_0$. The final control code of these switches to trim the reference voltage (V_{REF}) depends on the variation. The trimming resistance R_T, $2R_T$, $4R_T$, and $8R_T$ are used to cover the process variations with sufficient margin. The nodes I, F, G and G' in the Figure 3.11 indicate the nodes of the proposed voltage references I, II, III and IV, respectively at which resistance R_{REF} is connected.

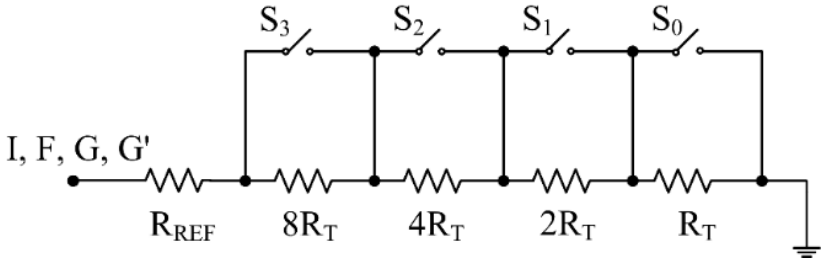


Figure 3.11 Resistance trimming circuit

3.7 Applications of the proposed CMOS voltage references

This section presents the low dropout regulators as the applications of proposed CMOS voltage references (I, II, III and IV), which have been discussed in sections 3.2 and 3.3. The low dropout regulator (LDO) is mainly used as a power supply source in portable electronic devices such as calculators, mobile, laptops, etc. The LDO provides a constant DC voltage with low input to output voltage drop. The proposed CMOS voltage references, namely CMOS voltage reference-I, CMOS voltage reference-II, CMOS voltage reference-III, and CMOS voltage reference-IV have been employed in a conventional LDO to validate their performances. The block diagram of the conventional LDO is shown in Figure 3.12 [118]. It mainly consists of a voltage reference, error amplifier (EA), pass transistor, and a feedback network.

The voltage reference V_{REF} is used to provide the stable and precise reference voltage at the input of the error amplifier (EA) for the proper working of the LDO. The error amplifier is used to sense the output voltage and compare it with the reference voltage to produce an error signal at its output. The error signal is provided at the gate terminal of pass transistor M_P to adjust the amount of load current required by the load. The feedback network consists of resistors R_1 and R_2 is used to feed the portion of output voltage back to the input terminal of the error amplifier, which helps in calculating the error signal and adjusting the output voltage of LDO to the desired value.

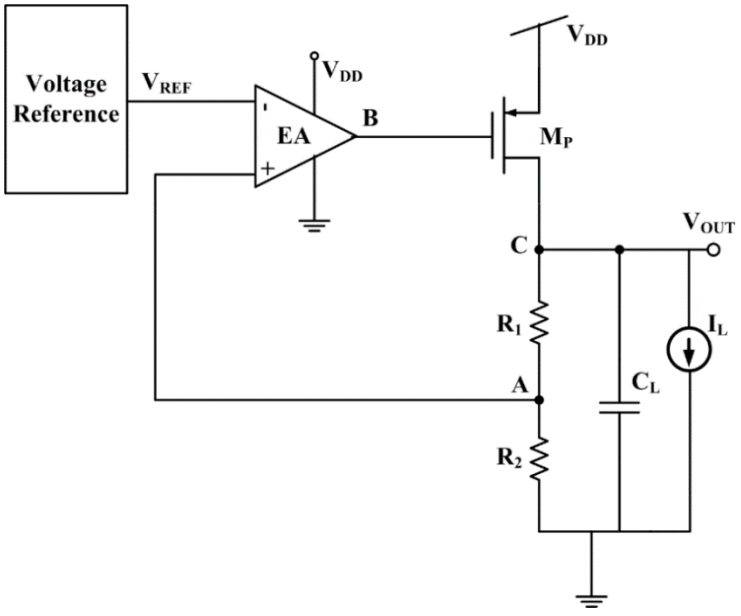


Figure 3.12 Block diagram of conventional LDO [118]

The circuit diagram of the conventional LDO is shown in Figure 3.13. It consists of transistors (M_P1-M_P5, M_N1-M_N3, and M_P), resistors (R_1, R_2), and capacitors (C_C and C_L). The transistors M_P1-M_P5 and M_N1-M_N3 are used to form the error amplifier (EA) [4], which generates the error signal to control the load current flowing through the pass transistor. Since the output reference voltages of the proposed CMOS voltage references I, II, III and IV are 118.5 mV, 425 mV, 312 mV and 350 mV, respectively, the PMOS transistor-based differential amplifier in EA is required that can operate effectively at these low reference voltages. The PMOS transistor M_P is used as a pass transistor. The feedback network is formed by using resistors R_1 and R_2. The capacitor C_L is added as a load capacitor at the output of the LDO. This capacitor is used as a charge storage element to enhance the stability of the circuit by providing stored charges when required. The output voltage V_{OUT} of the conventional LDO can be written as

$$V_{OUT}=\left(1+\frac{R_1}{R_2}\right)\times V_{REF} \tag{3.110}$$

The circuit of the conventional LDO shown in Figure 3.13 is used to demonstrate the workability of the proposed CMOS voltage references I, II, III, and IV. In the figure, the reference voltage V_{REF} at the inverting input terminal (gate terminal of transistor M_P1) of the error amplifier has been provided from the outputs of the proposed voltage references I, II, III, IV, and conventional voltage reference. The performance parameters of the LDOs based on proposed CMOS voltage references (I, II, III, and IV) have also been compared with a conventional LDO that uses a conventional voltage reference to show the effectiveness of the proposed voltage references.

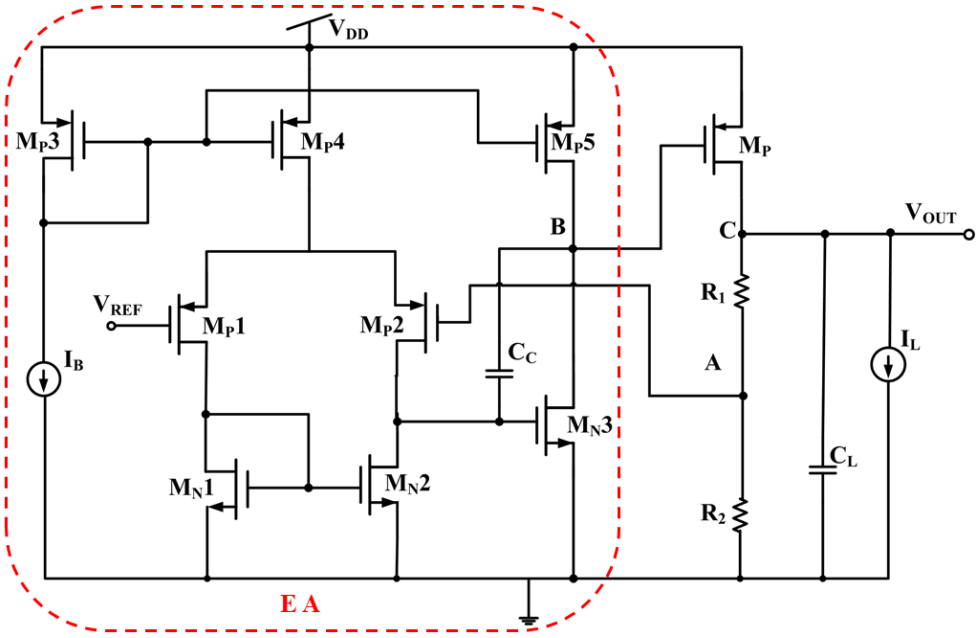


Figure 3.13 Circuit diagram of the conventional LDO

For better comparison with each proposed voltage reference, the conventional voltage reference using MOS transistors shown in Figure 3.14 [16] has been designed to maintain the same input supply voltage, operating temperature range, and output reference voltage. It uses resistors, MOS transistors and an operational amplifier (OP-AMP1''). The start-up circuit [113] is used to help the conventional voltage reference to come out from the zero-current state and connected at nodes B and C. It uses transistors $M_{SA}1$-$M_{SA}3$. At the beginning of the start-up process, the potential at node B is low which will turn ON transistor M_S1 and increase the potential at node A. The increased potential at node A will turn ON transistor M_S3 and drop down the potential at node C. The decreased potential at node C helps to flow the current into the circuit through transistors M1 and M2. Finally, when the voltage reference starts working properly, the start-up circuit turns OFF without affecting its normal operations. The circuit diagram of the OP-AMP1'' is shown in Figure 3.5. The transistors M1, M2, and M3 have the same gate-to-source voltages (V_{GS}), which result in equal currents I_1, I_2, and I_3, respectively. The OP-AMP1'' employed in the negative feedback is used to make potentials V_a and V_b equal by using transistors M1 and M2 that have the same dimensions. The two currents I_{2a} and I_{2b} having opposite temperature dependency are added to obtain a constant voltage (V_{REF}) across the resistor R_4.

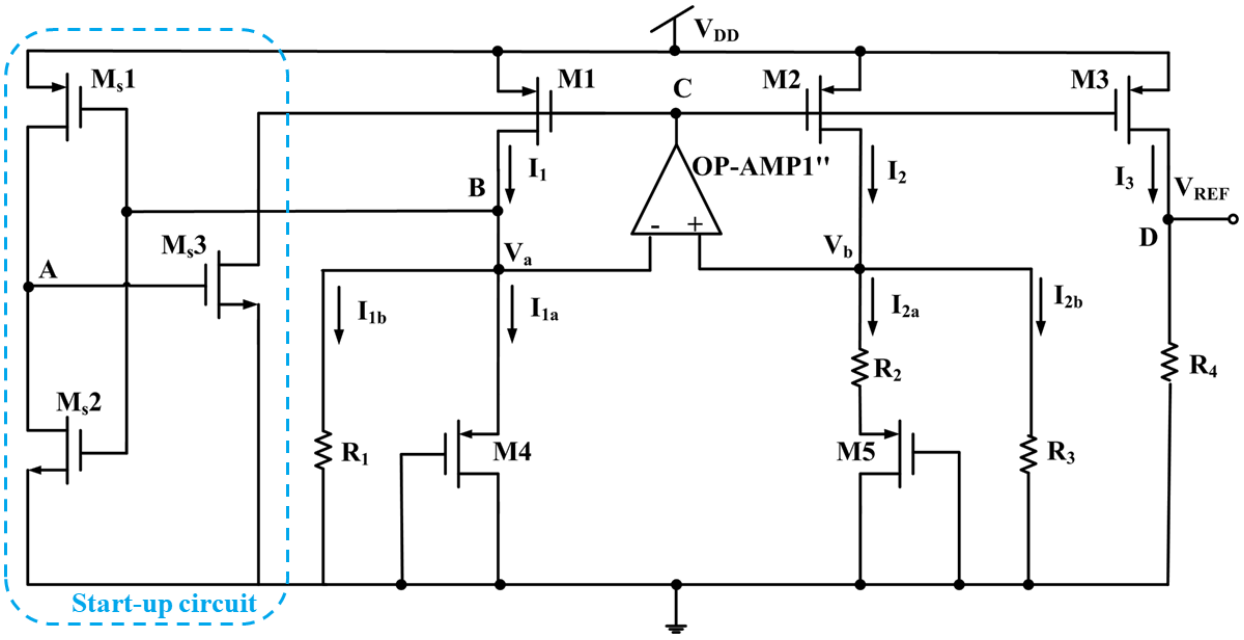


Figure 3.14 Conventional voltage reference using MOS transistors [16]

In the conventional voltage reference, the PTAT and CTAT currents are generated by the transistors M4 and M5. These transistors are operating in the subthreshold region. Since the voltages V_{DS4} and V_{DS5} are greater than $4V_T$, the gate-to-source voltages V_{GS4} and V_{GS5} of transistors M4 and M5 can be expressed using equation (1.3), as

$$V_{GS4}=V_{TH}+\eta V_T \ln\left(\frac{I_{DS4}}{\mu C_{ox}(W/L)_4(\eta-1)V_T^2}\right) \tag{3.111}$$

$$V_{GS5}=V_{TH}+\eta V_T \ln\left(\frac{I_{DS5}}{\mu C_{ox}(W/L)_5(\eta-1)V_T^2}\right) \tag{3.112}$$

If potentials V_a and V_b are equal and resistors R1 and R3 are of the same value, then the current $I_{1a} = I_{2a}$ and $I_{1b}= I_{2b}$. The current I_{2a} is given as

$$I_{2a}=\frac{V_{GS4}-V_{GS5}}{R_2}=\frac{V_T.\ln(N)}{R_2} \tag{3.113}$$

where V_T is the thermal voltage and $N=\frac{(W/L)_5}{(W/L)_4}$.

From equation (3.113), it is observed that the current I_{2a} is directly proportional to the thermal voltage, which confirms its PTAT behaviour.

The current I_{2b} flowing through resistor R_3 is directly proportional to gate-to-source voltage of subthreshold transistor M4, which confirms its CTAT behaviour. It can be expressed as

$$I_{2b}=\frac{V_{GS4}}{R_3} \tag{3.114}$$

Since the current I_2 is the addition of two currents I_{2a} and I_{2b} and current I_2 is mirrored to I_3 using transistors M2 and M3, the current I_3 can be written as

$$I_3=I_2=I_{2a}+I_{2b}=\frac{V_T.\ln(N)}{R_2}+\frac{V_{GS4}}{R_3} \tag{3.115}$$

Using current I_3, the reference voltage V_{REF} across the resistor R_4 is expressed as

$$V_{REF}=\frac{R_4}{R_2}V_T.\ln(N)+\frac{R_4}{R_3}V_{GS4} \tag{3.116}$$

Since thermal voltage (V_T) possesses PTAT behaviour and gate-to-source voltage (V_{GS4}) has CTAT behaviour, these PTAT and CTAT behaviours can be cancelled out by choosing appropriate values of resistances and aspect ratios of transistors.

3.7.1 Performance parameters of low dropout regulator

In order to identify the accuracy and reliability of the low dropout regulator (LDO), it should be measured in terms of different performance parameters such as dropout voltage, line sensitivity, load regulation, and power supply rejection ratio. The following sections will provide formal definitions of each of the LDO performance parameters.

3.7.1.1 Dropout voltage

The dropout voltage is defined as the input-to-output voltage difference at which the LDO is no longer able to regulate against the further decrease in the input supply. it is expressed as

$$\text{Dropout voltage} = I_L \times R_{DS,ON} \quad (V) \quad (3.117)$$

where I_L is the load current and $R_{DS,ON}$ is the drain-to-source on-resistance of pass element.

3.7.1.2 Line sensitivity

The line sensitivity is defined as the change in the regulated output voltage of LDO with respect to the change in input supply voltage and it is expressed as

$$\text{Line sensitivity} = \frac{\Delta V_{OUT}}{\Delta V_{IN}} \quad (\%/V) \quad (3.118)$$

where ΔV_{OUT} is the change in output voltage and ΔV_{IN} is the change in input voltage.

3.7.1.3 Load regulation

Load regulation is defined as a change in the regulated output voltage with respect to the change in load current. It is given as

$$\text{Load regulation} = \frac{\Delta V_{OUT}}{\Delta I_L} \quad (mV/A) \quad (3.119)$$

where ΔV_{OUT} is the change in the output voltage and ΔI_L is the change in the load current.

3.7.1.4 Power supply rejection ratio

The power supply rejection ratio (PSRR) is defined as the ability of LDO to suppress the supply noise and other undesired signals on the input supply voltage at a particular frequency. PSRR is a function of frequency specified in decibels and is expressed as

$$PSRR = 20\log \frac{V_{OUT,AC}(f)}{V_{IN,AC}(f)} \quad (dB) \quad (3.120)$$

where $V_{IN,AC}(f)$ is the input supply voltage affected by noise at a particular frequency f and $V_{OUT,AC}(f)$ is the output voltage at the same frequency.

3.8 Conclusions

Four different CMOS voltage references, namely CMOS voltage reference-I, CMOS voltage reference-II, CMOS voltage reference-III, and CMOS voltage reference-IV have been presented in this chapter. Out of these four voltage references, the first two voltage references (I and II) use PTAT and CTAT behaviours to generate their output reference voltages while the last two voltage references (III and IV) use only CTAT behaviours to generate their output reference voltages. The proposed CMOS voltage reference-I use two similar supply independent first-order voltage references in which negative feedback loops are employed to improve the line sensitivity. Further, to achieve low temperature sensitivity of output reference voltage over a wide temperature range, a high-order curvature-compensation technique is used. But, the proposed circuit suffers from some limitations such as circuit complexity, high supply voltage requirement and large area. The CMOS voltage reference-II uses only a self-biased cascode branch to generate both the PTAT and CTAT voltages, which makes the circuit simple and area efficient. To achieve high PSRR and low line sensitivity, two operational amplifiers are used in the negative feedback loop. Since the PTAT behaviour generator circuit requires more transistors with complex circuitry than the CTAT behaviour generator circuit, these voltage references (I and II) require a large number of transistors. Therefore, this technique does not offer much improvement in the circuit's complexity, power consumption, and area. The proposed CMOS voltage reference-III based on the CTAT-CTAT technique uses a reduced number of transistors with less complexity as compared to the proposed CMOS voltage reference-I and II. It uses two supply independent CTAT generators and a current subtractor. However, as per the demand of modern VLSI, the proposed CMOS voltage reference-III requires further improvements in the line sensitivity and PSRR. To achieve low line sensitivity and high PSRR, another circuit of voltage reference named CMOS voltage reference-IV has also been presented. The proposed CMOS voltage reference-IV is based on the subtraction of two CTAT behaviours. A beta-multiplier circuit is used to generate two CTAT voltages. These CTAT voltages are converted into CTAT currents by using two operational amplifiers in the negative feedback loop to achieve low line sensitivity and high PSRR. In this chapter, the performances of the proposed CMOS voltage reference-I, CMOS voltage reference-II, CMOS voltage reference-III, and CMOS voltage reference-IV have also been validated using a conventional LDO.

CHAPTER 4

SIMULATION RESULTS OF PROPOSED CMOS VOLTAGE REFERENCES AND LOW DROPOUT REGULATORS

4.1 Introduction

The proposed CMOS voltage references (I, II, III, and IV) presented in chapter 3 have been simulated using Cadence virtuoso analog design environment in BSIM3v3 180 nm CMOS technology. The physical layouts of the proposed CMOS voltage references are designed using Cadence Virtuoso Layout XL editor in 180 nm CMOS technology. The resistances of the proposed CMOS voltage references are implemented using polysilicon resistances. The polysilicon resistances have very small temperature coefficients as compared to the temperature coefficient of the reference current. The performances of four different CMOS voltage references have been compared with the various voltage references available in the literature using three figures of merit namely FOM_1, FOM_2, and FOM_3.

The first figure of merit (FOM_1) is expressed in terms of the temperature range (T_{max} - T_{min}), temperature coefficient (TC), power, and area [48, 119]. The FOM_1 is specified in $°C^3/W.m^2$ with the following definition

$$FOM_1=\frac{(T_{max}-T_{min})^2}{TC\times Power\times Area}\times\frac{1}{10^{21}} \qquad (°C^3/W.m^2) \qquad (4.1)$$

The second figure of merit (FOM_2) is defined by considering the performance parameters such as power supply rejection ratio (PSRR), temperature coefficient (TC), area, and supply current [38]. The FOM_2 is denoted in $dB.°C/ppm.\mu A.mm^2$ with the following definition

$$FOM_2=\frac{\text{PSRR @ 100 Hz}}{TC\times Area\times \text{Supply Current}} \qquad (dB.°C/ppm.\mu A.mm^2) \qquad (4.2)$$

where PSRR @ 100 Hz is the power supply rejection ratio at a frequency of 100 Hz (frequency of 100 Hz is selected for better comparison with the existing voltage references).

The third figure of merit (FOM_3) is derived from the geometric mean of FOM_1 and FOM_2, which is expressed as

$$FOM_3=\sqrt{FOM_1\times FOM_2} \qquad ((°C/m)^2.\ (dB/W.ppm.\ \mu A)^{1/2}.10^3) \qquad (4.3)$$

The FOM_3 is specified in $(°C/m)^2.\ (dB/W.ppm.\ \mu A)^{1/2}.10^3$.

The higher values of FOM_1, FOM_2, and FOM_3 confirm the better performance of the voltage reference.

The proposed CMOS voltage references namely CMOS voltage reference-I, CMOS voltage reference-II, CMOS voltage reference-III, and CMOS voltage reference-IV have been employed in a conventional low dropout regulator (LDO) to validate their performances. The low dropout regulators (LDOs) based on proposed voltage references (I, II, III, and IV) have also been simulated using Cadence virtuoso analog design environment in BSIM3v3 180 nm CMOS technology. The performances of the LDOs based on proposed voltage references (I, II, III, and IV) have also been compared with a conventional LDO that uses a conventional voltage reference to show the effectiveness of the LDOs based on proposed voltage references.

This chapter is organized as follows. The post-layout simulation results of proposed CMOS voltage reference-I and CMOS voltage reference-II are presented in section 4.2 whereas section 4.3 describes the post-layout simulation results of proposed CMOS voltage reference-III and CMOS voltage reference-IV. The simulation results of the LDOs based on proposed CMOS voltage references are discussed in section 4.4. Finally, the conclusion is addressed in section 4.5

4.2 Simulation results of proposed CMOS voltage references I and II

In this section, the post-layout simulation results of proposed CMOS voltage reference-I and CMOS voltage reference-II are presented.

4.2.1 Post-layout simulation results of proposed CMOS voltage reference-I

The aspect ratios (W/L) of MOS transistors and the values of passive components used in the proposed CMOS voltage reference-I are listed in Table 4.1. For the simulations, the operating temperature and supply voltage of proposed CMOS voltage reference-I are chosen as 27 ℃ and 0.85 V, respectively.

Table 4.1 Circuit elements' dimensions used in the proposed CMOS voltage reference-I

Circuit elements' dimensions			
NMOS transistors	W/L (μm/μm)	PMOS transistors	W/L (μm/μm)
M_3, M_4	0.5/0.5	M_1, M_{32}	0.4/2
M_{30}, M_{31}	0.4/0.2	M_2, M_{33}	5/0.2
M_6, M_{26}	1/1	M_5, M_{27}	1/4
M_7, M_{23}	2/0.5	M_8, M_9	1/6
M_{10}, M_{11}	0.5/3	M_{28}, M_{29}	5/6
M_{24}, M_{25}	1/1	M_{14}, M_{35}	3/3
M_{12}, M_{22}	0.4/1	M_{15}, M_{34}	3/3.5
M_{13}, M_{21}	1/3	M_{18}, M_{19}	2/0.18
M_{16}, M_{17}	24/6		
Resistors		(kΩ)	
R_1, R_4		200	
R_2, R_3		110	
R_{REF}		80	

The physical layout of the proposed CMOS voltage reference-I is shown in Figure 4.1. The proposed voltage reference-I occupies an area of 64.7 µm × 67 µm.

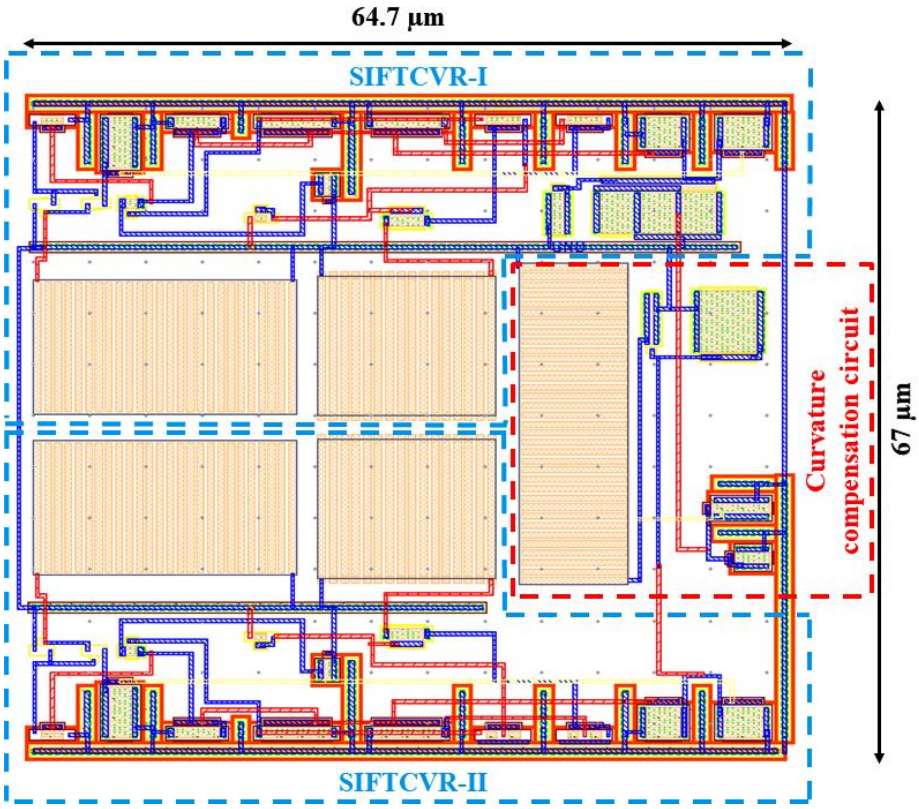


Figure 4.1 Layout of the proposed CMOS voltage reference-I

Figure 4.2 shows the output reference voltage (V_{REF}) versus temperature plot of the proposed CMOS voltage reference-I. From the figure, the value of V_{REF} at a nominal temperature of 27 ℃ is obtained as 118.51 mV. The maximum variation of V_{REF} is 0.47 mV over the temperature ranging from -60 ℃ to 120 ℃, which gives the TC of 21.9 ppm/℃.

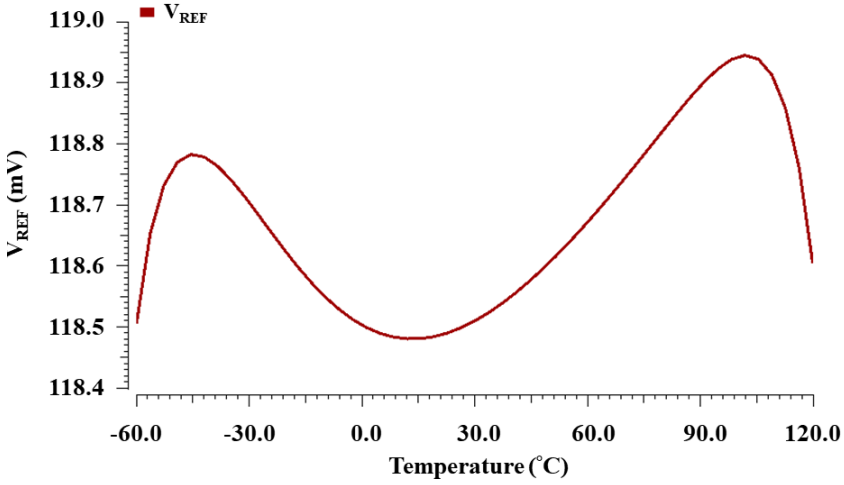
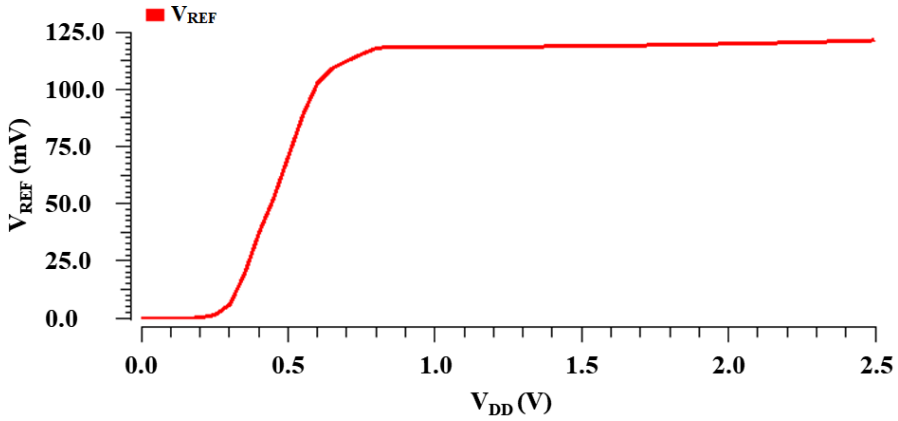
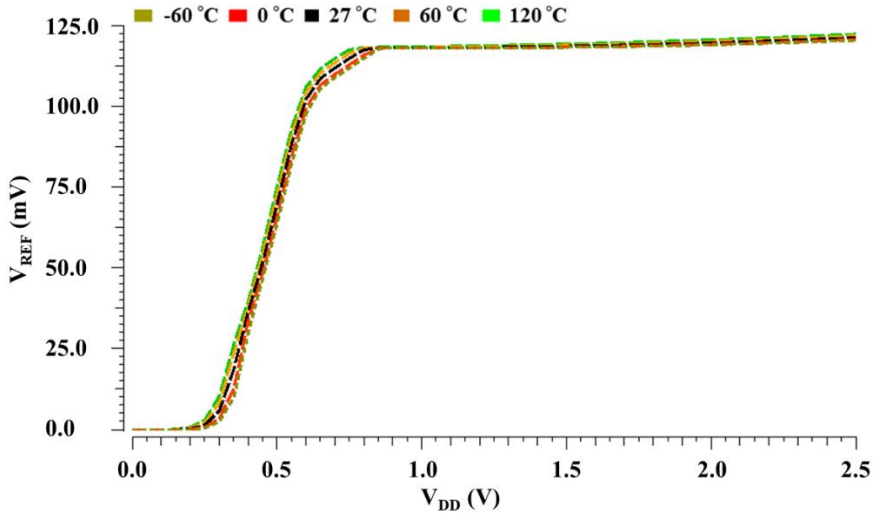


Figure 4.2 Output reference voltage (V_{REF}) versus temperature plot of the proposed CMOS voltage reference-I

Figure 4.3 (a) illustrates the variation of V_{REF} with respect to the supply voltage varying from 0 V to 2.5 V at a nominal temperature of 27 ℃. The plot confirms that the proposed CMOS voltage reference-I works properly when the supply voltage is more than or equal to 0.85 V. Also, the line sensitivity of the proposed CMOS voltage reference-I is observed as 0.04 %/V for the supply voltage ranging from 0.85 V to 2.5 V. The output reference voltage (V_{REF}) versus supply voltage plots for different operating temperatures such as -60 ℃, 0 ℃, 27 ℃, 60 ℃, and 120 ℃, are shown in Figure 4.3 (b). It is observed that the variation of the output reference voltage (V_{REF}) with respect to supply voltage remains almost the same for different operating temperatures. The worst-case value of line sensitivity is observed as 0.048 %/V for the different operating temperatures.



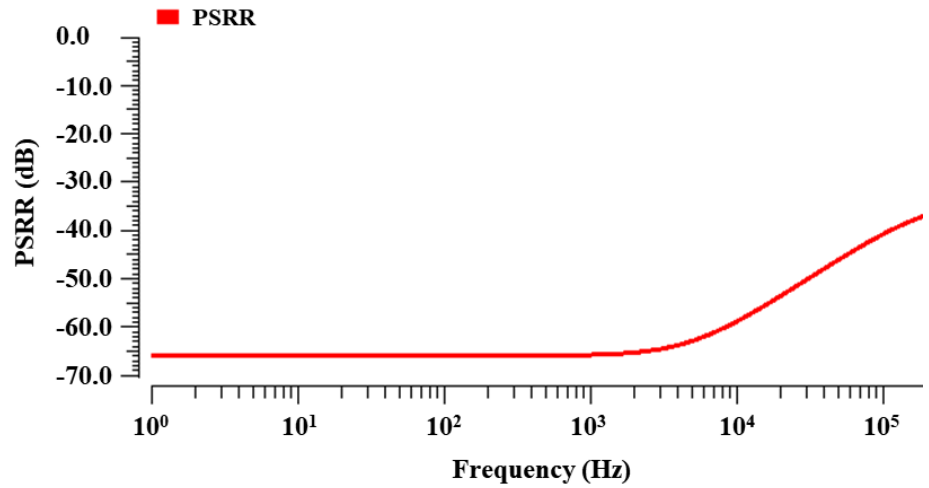
(a)



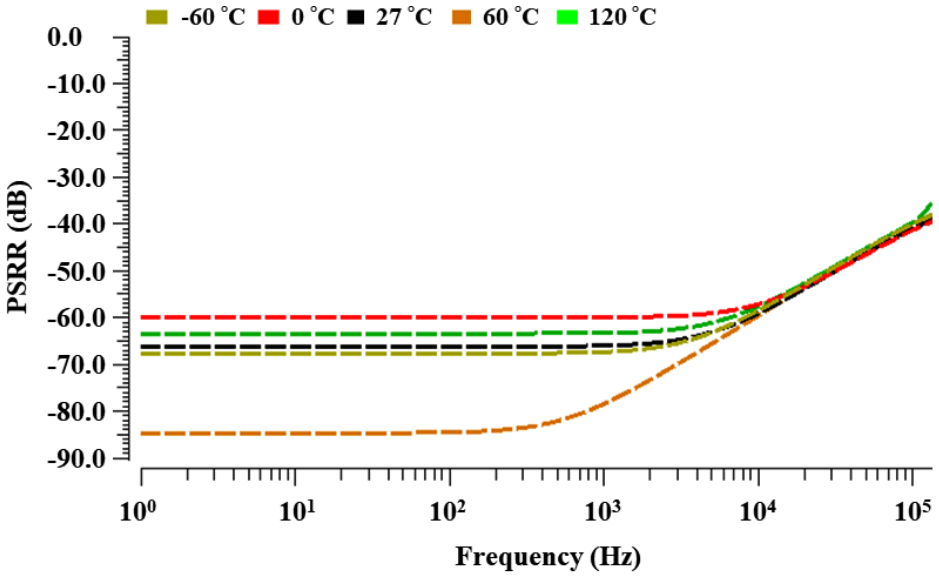
(b)

Figure 4.3 (a) Variation of V_{REF} with respect to the supply voltage (b) Output reference voltage (V_{REF}) versus supply voltage plots for different operating temperatures

Figure 4.4 (a) shows the PSRR versus frequency plot and from the plot, the values of PSRR are obtained as -65.83 dB, -65.66 dB, and -58.84 dB at the frequencies of 100 Hz, 1 kHz, and 10 kHz, respectively. For different operating temperatures such as -60 ℃, 0 ℃, 27 ℃, 60 ℃, and 120 ℃, the PSRR versus frequency plots are also shown in Figure 4.4 (b). From the plots, it can be seen that the minimum value of PSRR for the different operating temperatures is -59.82 dB at the frequency of 100 Hz. Figure 4.4 (c) shows the plots of PSRR with respect to the frequency for various supply voltages such as 0.85 V, 1.5 V, 2 V, and 2.5 V at a nominal temperature of 27 ℃. The figure shows that the minimum value of PSRR for different supply voltages is -59.63 dB at the frequency of 100 Hz. Thus, it can be concluded that the proposed CMOS voltage reference-I can suppress the supply noise and other undesired signals imposed on the supply voltage.



(a)



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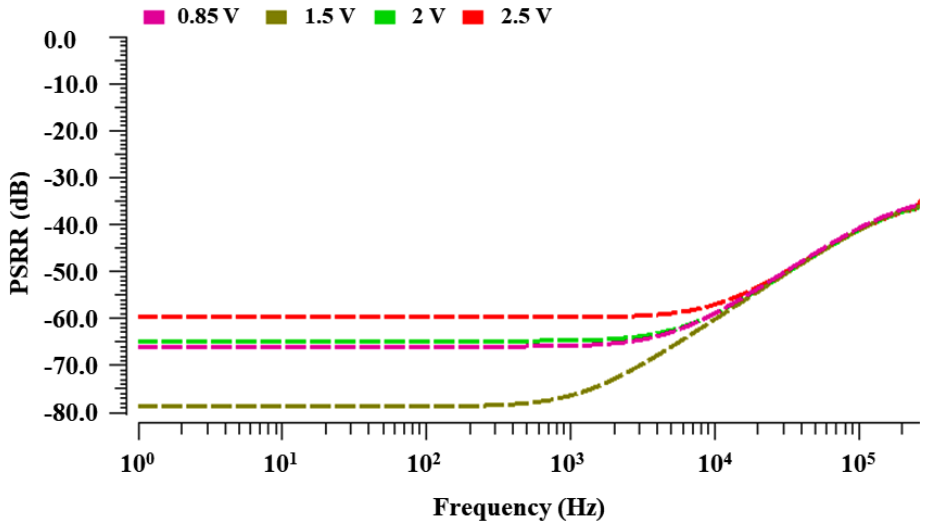
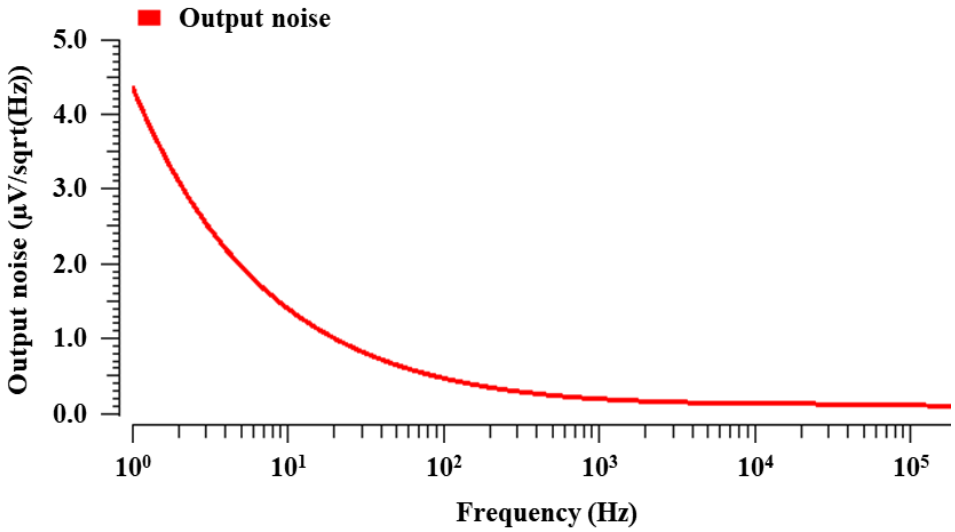


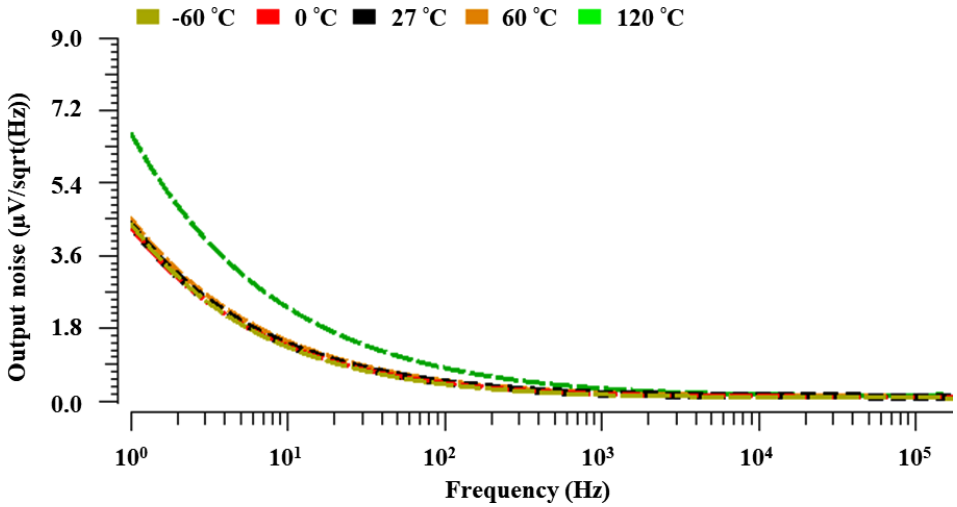
(c)

Figure 4.4 (a) PSRR versus frequency plot of the proposed CMOS voltage reference-I (b) PSRR versus frequency plots for different operating temperatures (c) PSRR versus frequency plots for different supply voltages

The output noise versus frequency plot of the proposed CMOS voltage reference-I is shown in Figure 4.5 (a). From the plot, the values of output noise are observed as 480.32 nV/$\sqrt{\text{Hz}}$, 201.77 nV/$\sqrt{\text{Hz}}$ and 140.56 nV/$\sqrt{\text{Hz}}$ at the frequencies of 100 Hz, 1 kHz, and 10 kHz, respectively. For different operating temperatures such as -60 ℃, 0 ℃, 27 ℃, 60 ℃, and 120 ℃, the output noise versus frequency plots are also illustrated in Figure 4.5 (b). From the plots, it can be seen that the values of output noise for the different operating temperatures are less than 836.14 nV/$\sqrt{\text{Hz}}$ at the frequency of 100 Hz.



(a)



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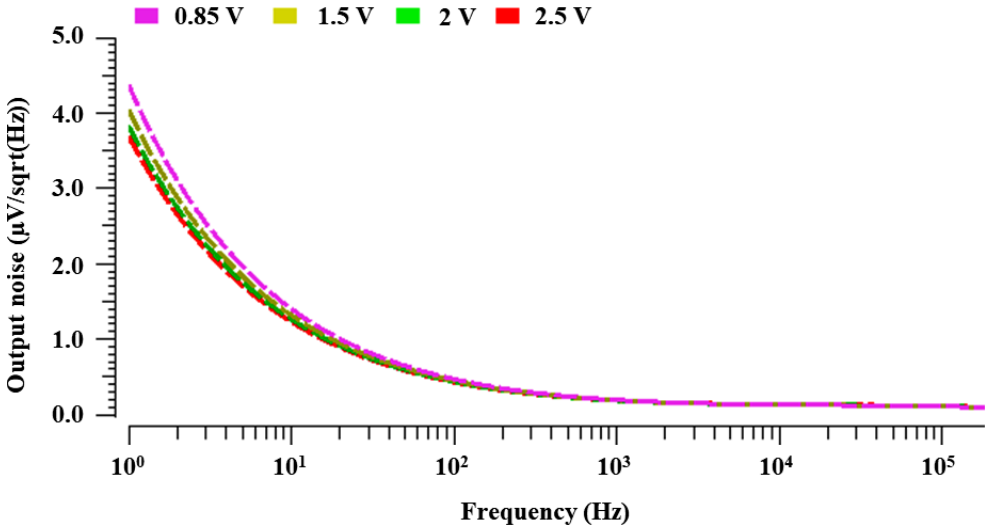


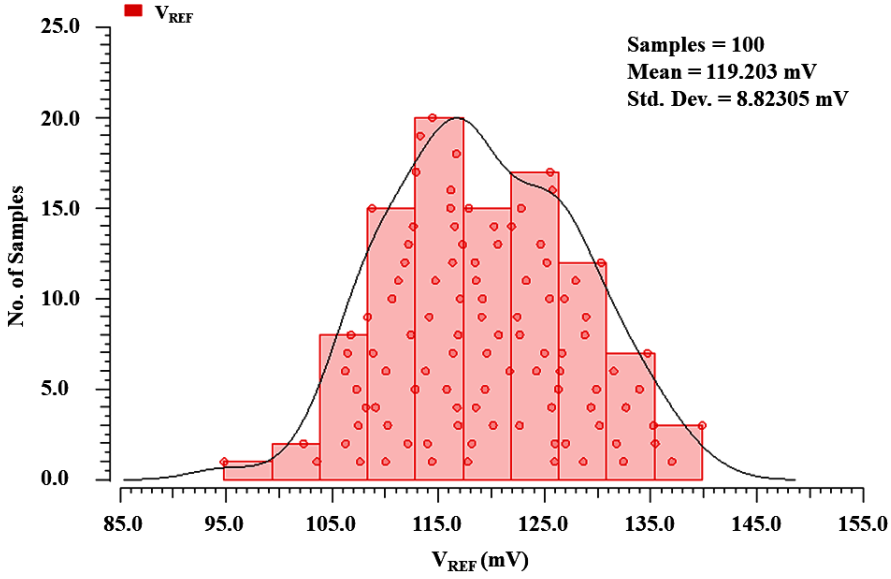
(c)

Figure 4.5 (a) Output noise versus frequency plot of the proposed CMOS voltage reference-I (b) Output noise versus frequency plots for different operating temperatures (c) Output noise versus frequency plots for different supply voltages

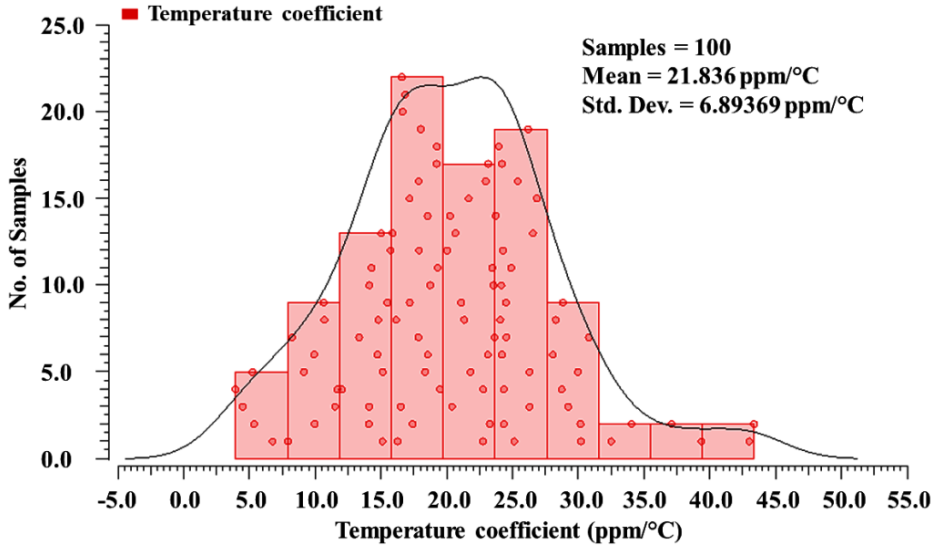
Figure 4.5 (c) shows the output noise versus frequency plots for different supply voltages such as 0.85 V, 1.5 V, 2 V, and 2.5 V at the nominal temperature of 27℃. From the plots, it is evident that the values of output noise for different supply voltages are less than 480.32 nV/$\sqrt{\text{Hz}}$ at the frequency of 100 Hz.

4.2.1.1 Monte Carlo simulations

The Monte Carlo simulations of the proposed CMOS voltage reference-I for 100 samples have been performed by considering both the process variations and mismatch-induced variations. Figures 4.6 (a), (b), (c), and (d) show the Monte Carlo simulations of the output reference voltage (V_{REF}), TC, line sensitivity, and PSRR, respectively. These Monte Carlo simulation plots show the realistic picture of the proposed CMOS voltage reference-I behaviour. From Figure 4.6 (a), it is observed that the mean value of V_{REF} is 119.20 mV with a standard deviation of 8.82 mV. From Figure 4.6 (b), the mean value of TC is obtained as 21.83 ppm/℃ with a standard deviation of 6.89 ppm/℃.



(a)



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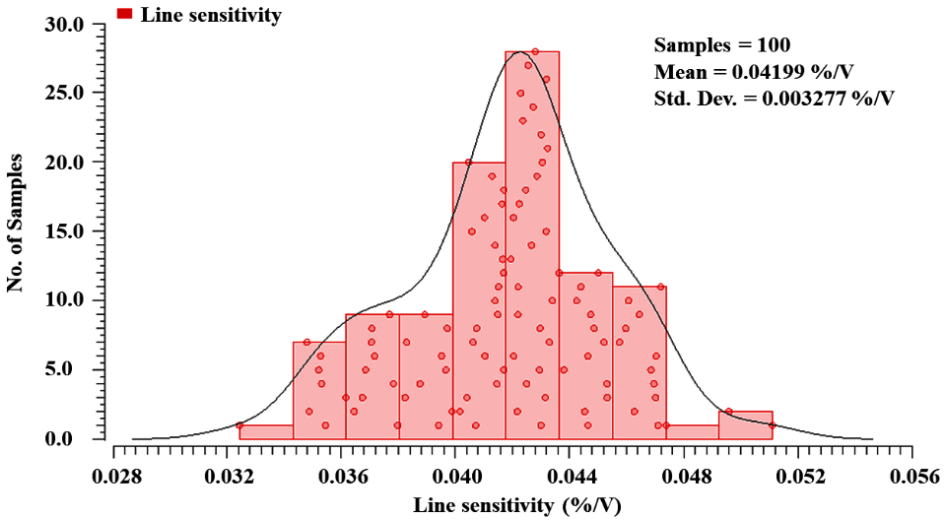

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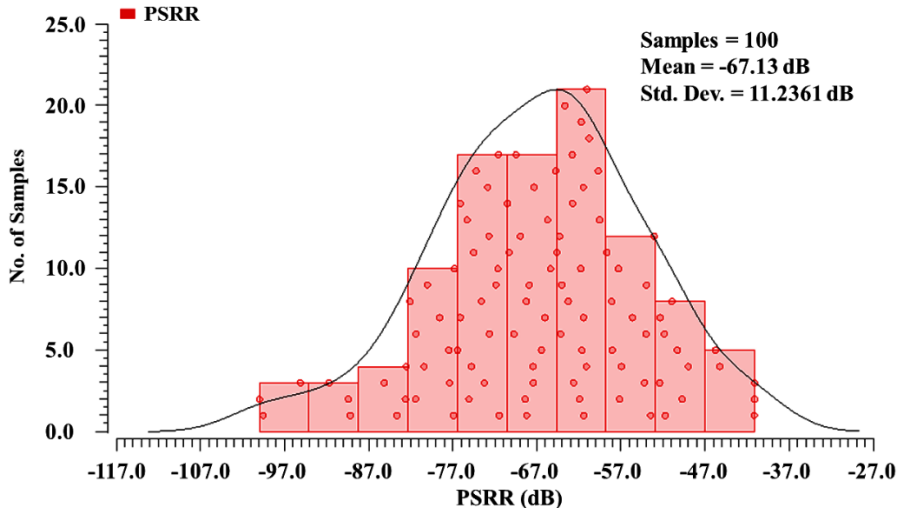


(d)

Figure 4.6 (a) Monte Carlo simulation results of the reference voltage (V_{REF}) for 100 samples (b) Monte Carlo simulation results of the TC for 100 samples (c) Monte Carlo simulation results of line sensitivity for 100 samples (d) Monte Carlo simulation results of PSRR for 100 samples.

From Figure 4.6 (c), the mean value of line sensitivity is observed as 0.04199 %/V with a standard deviation of 0.003277 %/V. From Figure 4.6 (d), it is observed that the mean value of PSRR is -67.13 dB with a standard deviation of 11.23 dB.

The performance parameters of the proposed CMOS voltage reference-I and existing voltage references [72-73, 79, 81, 101, 104, 106-107] are listed in Table 4.2. On the basis of performance parameters, it is very difficult to compare the different designs, as there is a trade-off between the performance parameters to reach an optimum value as per the specifications. So, for a fair comparison, three figures of merit (FOM_1, FOM_2, and FOM_3) discussed in section 4.1 are used, which provide numerical values by combining the overall performance parameters of the designs. From the table, it can be seen that the proposed CMOS voltage reference-I has higher FOM_1, FOM_2, and FOM_3 than the existing voltage references which confirm its better performance. Further, it has also been observed that the proposed CMOS voltage reference-I has high PSRR and low line sensitivity as compared to the other state-of-art solutions which define the robustness of the proposed circuit against the supply noise and supply voltage variations.

Table 4.2 Comparison of proposed CMOS voltage reference-I with existing voltage references

References→ Parameters↓	[72]	[73]	[79]	[81]	[101]	[104]	[106]	[107]	Proposed voltage reference-I
Technology (nm)	180	130	180	180	180	180	180	45	180
Supply voltage (V)	0.9 to 2.5	1 to 2.3	1.2 to 2	1.2 to 1.8	3.3	1.3	0.9 to 10	0.6 to 1.2	0.85 to 2.5
Temp. range (˚C)	-20 to 120	0 to 100	-40 to 125	0 to 100	-40 to 150	-10 to 120	0 to 100	-40 to 125	-60 to 120
V_{REF} (mV)	224	781	800	500	861	596	551.78	475	118.5
TC (ppm/℃)	191.3	48	34	22	75	30.95	102	31	21.9
PSRR (dB) @ 100 Hz	-----	-51.4	-62	-42	----	38	-----	-53	-65.83
Line sensitivity (%/V)	0.2	0.34	0.2	0.280	-----	-----	-----	0.433	0.04
Area (mm^2)	0.0238	0.053	0.04	0.073	0.0249	0.8	0.25	0.004875	0.0043
Power consumption (µW)	3.78	8.1	9.996	6.12	112.2	3.51	96.67	15.996	5.168
FOM_1 ($°C^3/W.m^2$)	1.02	0.41	2.01	1.02	0.173	0.19	0.0041	11.25	52.65
FOM_2 (dB.°C/ ppm.µA.mm^2)	-----	2.5	5.47	5.13	----	0.57	----	13.33	90.92
FOM_3 ($(°C/m)^2$. (dB/W.ppm. µA)$^{1/2}$.10^3)	-----	1.6	3.32	2.29	-----	0.33	----	12.25	69.19

4.2.2 Post-layout simulation results of proposed CMOS voltage reference-II

The aspect ratios (W/L) of MOS transistors and the values of passive components used in the proposed CMOS voltage reference-II are given in Table 4.3. For the simulations, the operating temperature and supply voltage of the proposed CMOS voltage reference-II are selected as 27 ℃ and 0.80 V, respectively.

Table 4.3 Circuit elements' dimensions used in proposed CMOS voltage reference-II

Circuit elements' dimensions			
NMOS transistors	W/L (μm/μm)	PMOS transistors	W/L (μm/μm)
M_3	4/0.5	M_1	3/1
M_4, M_5	1/3	M_2	5/2
M_7,M_8, M_9	0.5/2	M_6	1/1
M_{12}	0.5/2	M_{10}, M_{11}	1/1
M_{13}	10/0.5	M_{14}	1/1
	3/0.5	M_{15}	3/1
Resistors		(kΩ)	
R_1		200	
R_2		110	
R_{REF}		225	

The physical layout of the proposed CMOS voltage reference-II is illustrated in Figure 4.7. The proposed voltage reference occupies an area of 52 μm × 58 μm.

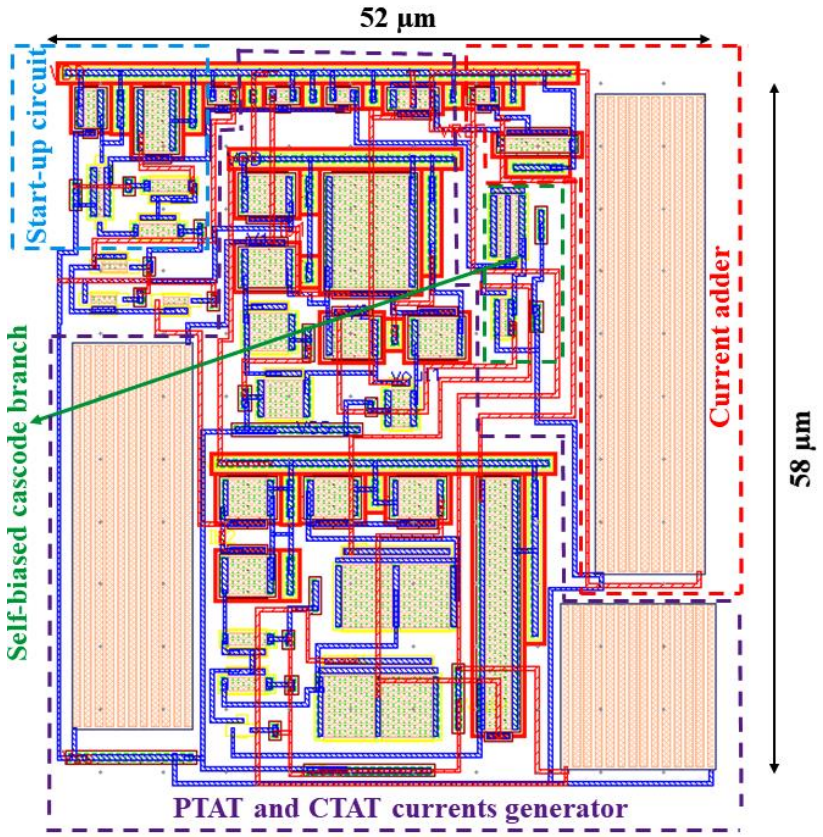


Figure 4.7 Layout of the proposed CMOS voltage reference-II

The output reference voltage (V_{REF}) versus temperature plot of the proposed CMOS voltage reference-II is shown in Figure 4.8. The temperature is varying from -55 ℃ to 125 ℃. From the figure, the value of V_{REF} at a nominal temperature of 27 ℃ is obtained as 424.85 mV. The maximum variation of V_{REF} is 2.26 mV over the temperature ranging from -55 ℃ to 125 ℃, which gives the TC of 29.5 ppm/℃. Figure 4.9 (a) shows the variation of V_{REF} with respect to the supply voltage ranging from 0 V to 5 V at a nominal temperature of 27 ℃. From the plot, it can be seen that the proposed CMOS voltage reference-II works properly when the supply voltage is more than or equal to 0.80 V. The line sensitivity of the proposed CMOS voltage reference-II is also observed as 0.0035 %/V for the supply voltage ranging from 0.80 V to 5 V.

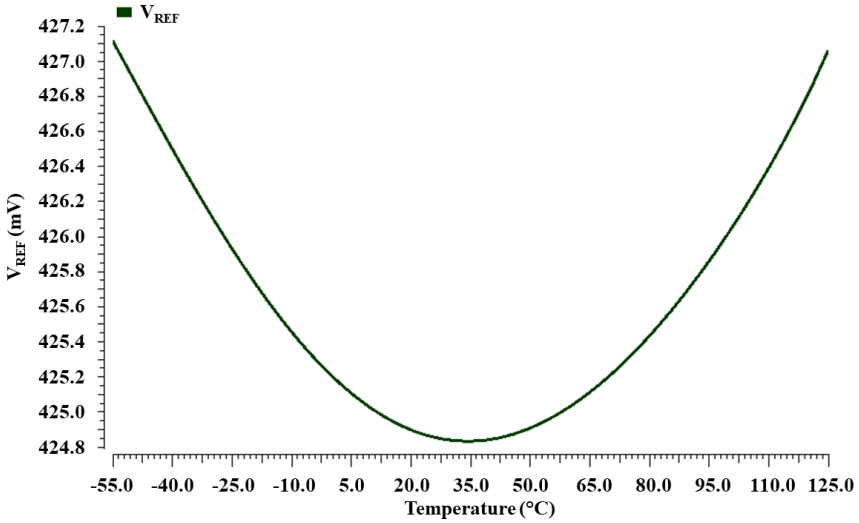
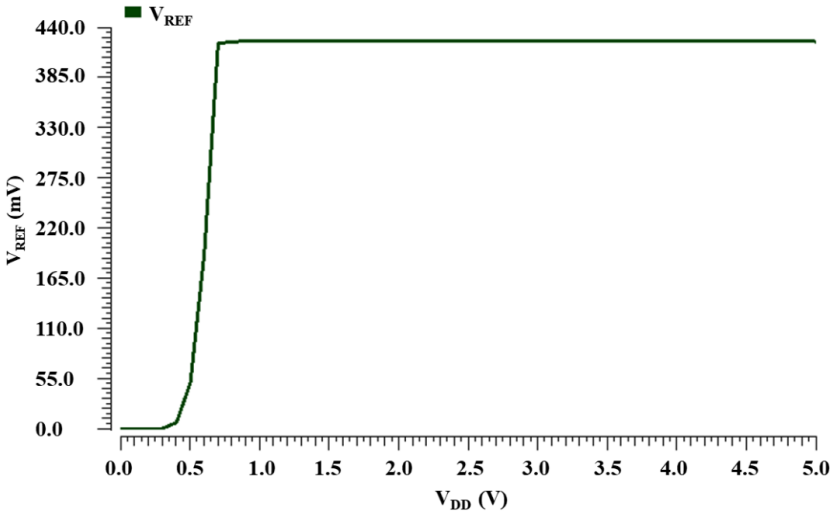
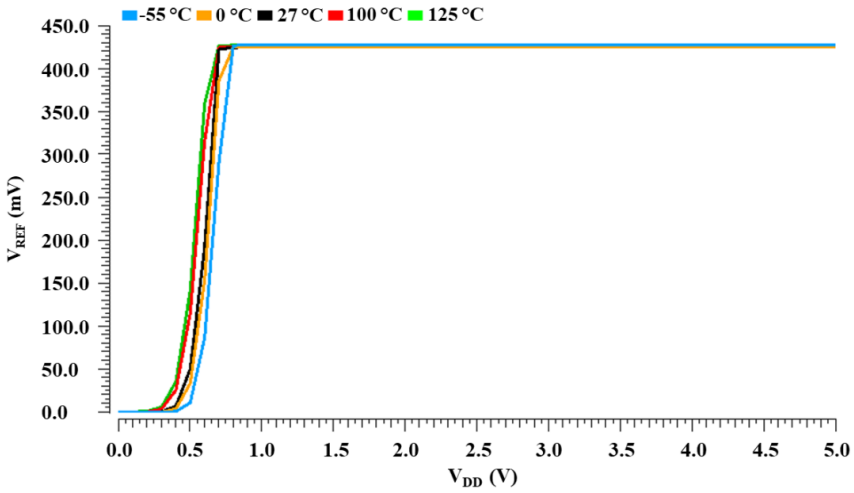


Figure 4.8 Output reference voltage (V_{REF}) versus temperature plot of the proposed CMOS voltage reference-II



(a)

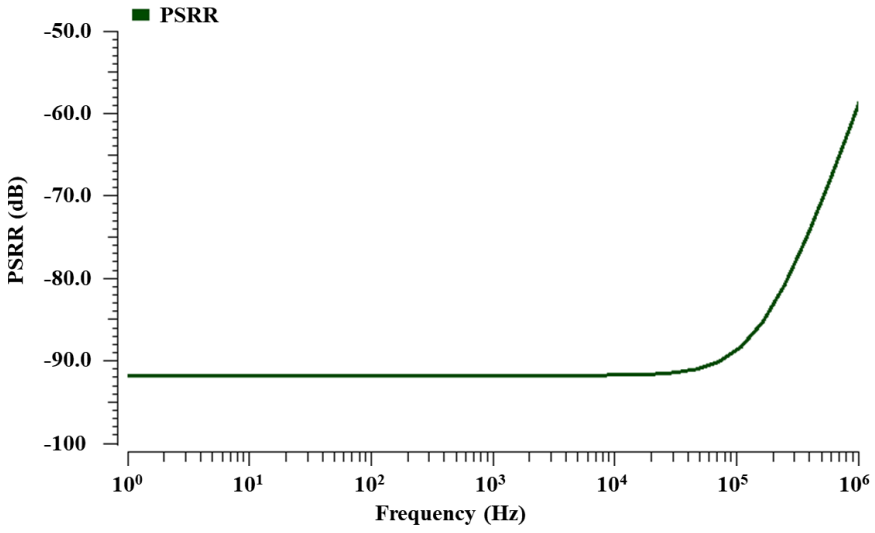


(b)

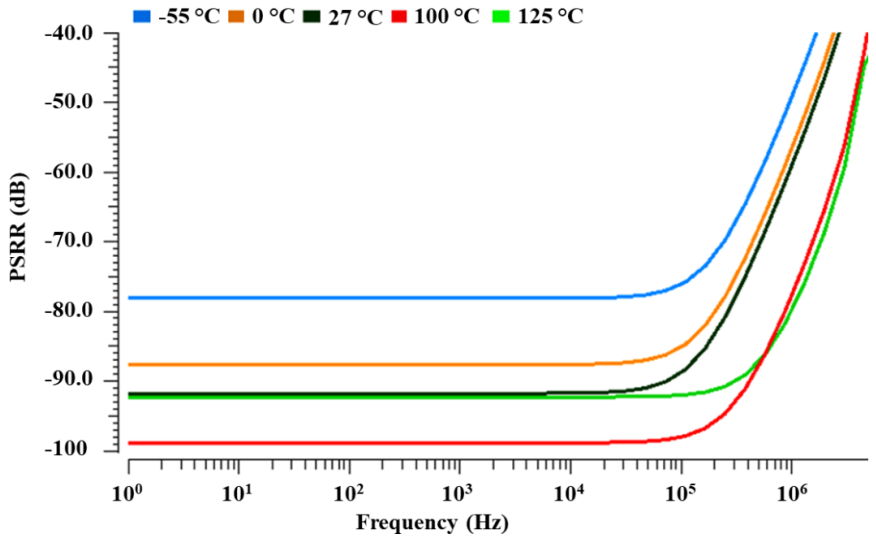
Figure 4.9 (a) Variation of V_{REF} with respect to the supply voltage (b) Output reference voltage (V_{REF}) versus supply voltage plots for different operating temperatures

The output reference voltage (V_{REF}) versus supply voltage plots for different operating temperatures such as -55 ℃, 0 ℃, 27 ℃, 100 ℃, and 125 ℃, are shown in Figure 4.9 (b). It is observed that the variation of the output reference voltage (V_{REF}) with respect to supply voltage remains almost the same for different operating temperatures. The worst-case value of line sensitivity is observed as 0.0043%/V for the different operating temperatures.

The PSRR versus frequency plot of the proposed CMOS voltage reference-II is illustrated in Figure 4.10 (a). From the figure, the values of PSRR are obtained as -91.69 dB, -91.3 dB, and -90.8 dB at the frequencies of 100 Hz, 1 kHz, and 10 kHz, respectively. Figure 4.10 (b) shows the PSRR versus frequency plots for different operating temperatures such as -55 ℃, 0 ℃, 27 ℃, 100 ℃, and 125 ℃.



(a)



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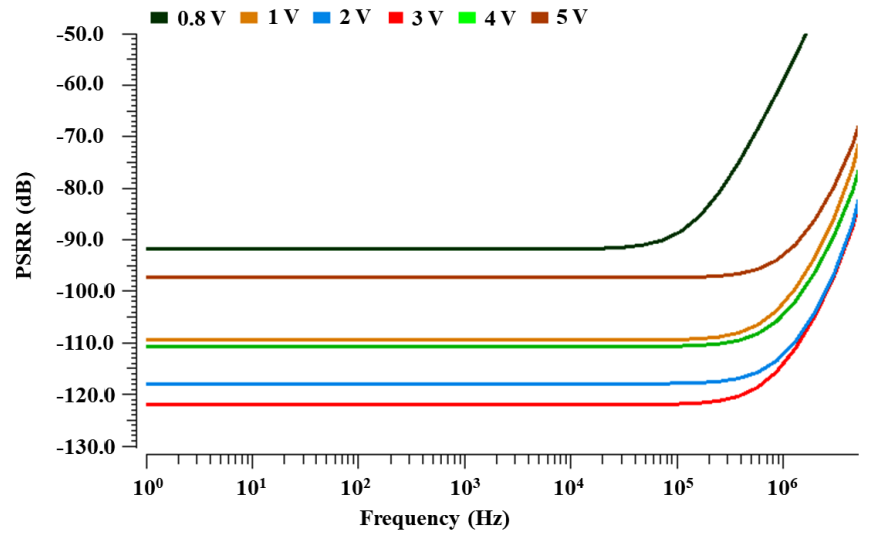
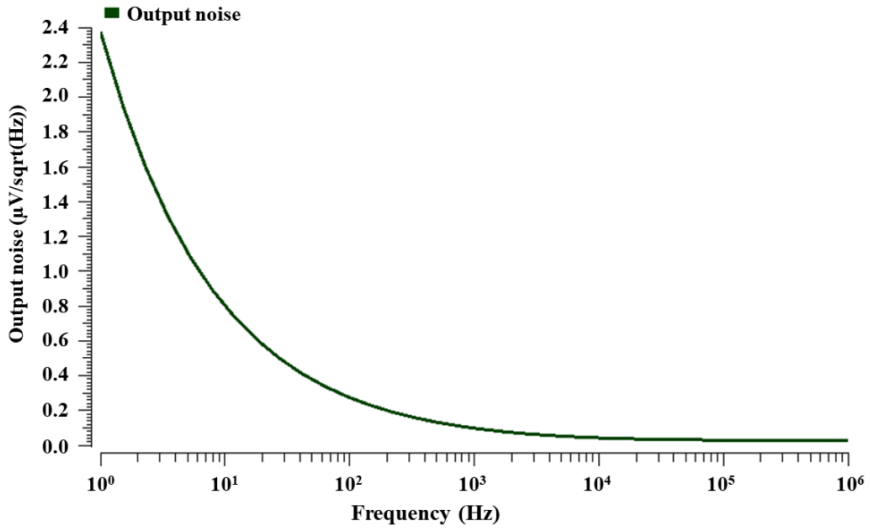


(c)

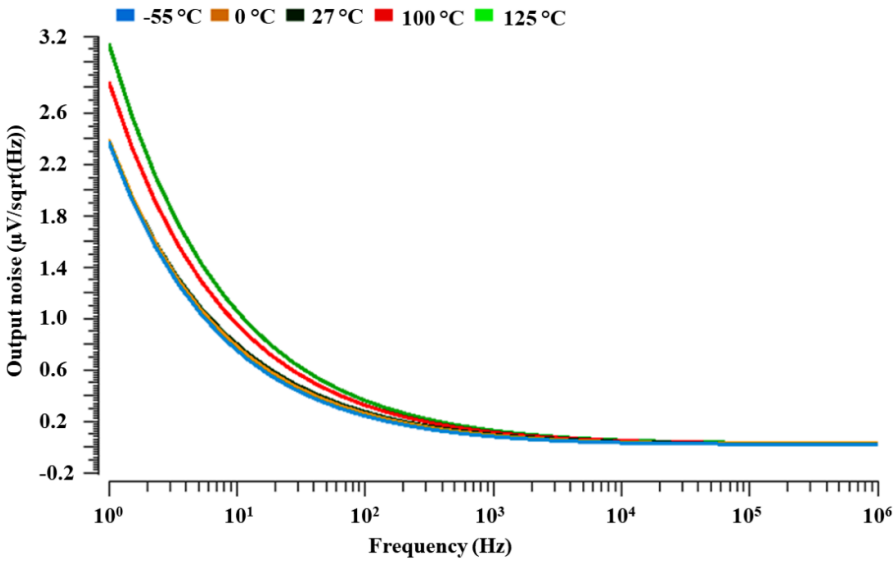
Figure 4.10 (a) PSRR versus frequency plot of proposed CMOS voltage reference-II (b) PSRR versus frequency plots for different operating temperatures (c) PSRR versus frequency plots for different supply voltages

From the plots, it is observed that the minimum value of PSRR is -78.06 dB for the different operating temperatures at the frequency of 100 Hz. Figure 4.10 (c) shows the PSRR versus frequency plots at a nominal temperature of 27 ℃ for different supply voltages such as 0.8 V, 1.0 V, 2.0 V, 3.0 V, 4 V, and 5.0 V. The figure shows that the minimum value of PSRR for different supply voltages is -91.66 dB at the frequency of 100 Hz. Hence, it can be concluded that the proposed CMOS voltage reference-II has high immunity to suppress supply noise and other unwanted signals imposed on the supply voltage.

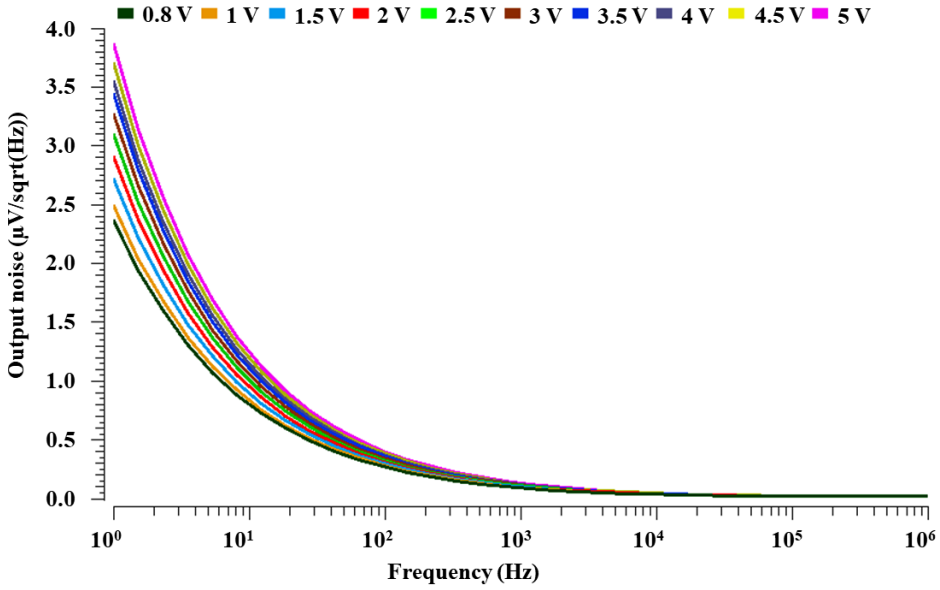
The output noise versus frequency plot of the proposed CMOS voltage reference-II is illustrated in Figure 4.11 (a). From the plot, the values of output noise are obtained as 277.527 nV/$\sqrt{Hz}$, 101.42 nV/$\sqrt{Hz}$, and 45.26 nV/$\sqrt{Hz}$ at the frequencies of 100 Hz, 1 kHz, and 10 kHz, respectively. Figure 4.11 (b) shows the plots of output noise with respect to the frequency for different operating temperatures such as -55 ℃, 0 ℃, 27 ℃, 100 ℃, and 125 ℃. From the figure, it can be seen that the values of output noise are less than 366.05 nV/$\sqrt{Hz}$ for different operating temperatures at the frequency of 100 Hz.



(a)



(b)



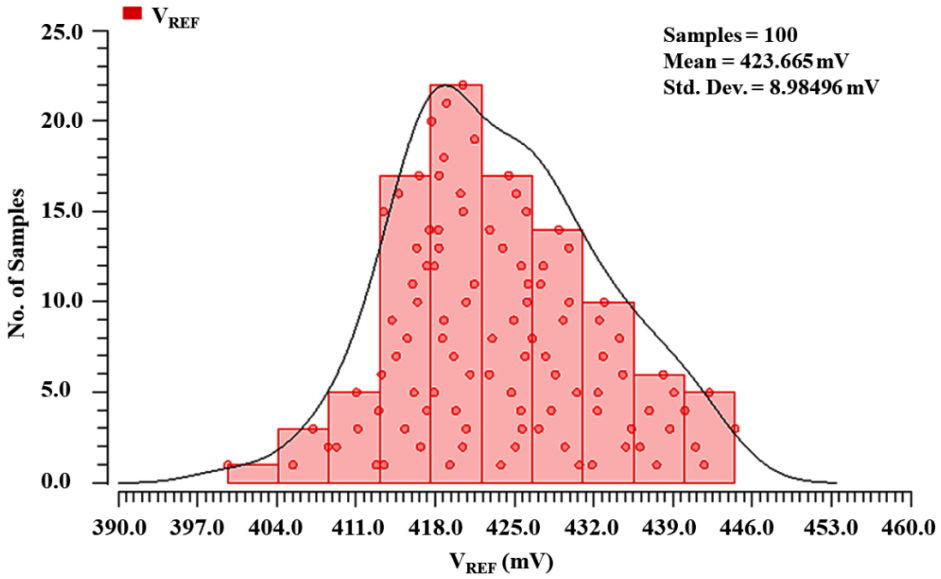
(c)

Figure 4.11 (a) Output noise versus frequency plot of the proposed CMOS voltage reference-II (b) Output noise versus frequency plots for different operating temperatures (c) Output noise versus frequency plots for different supply voltages

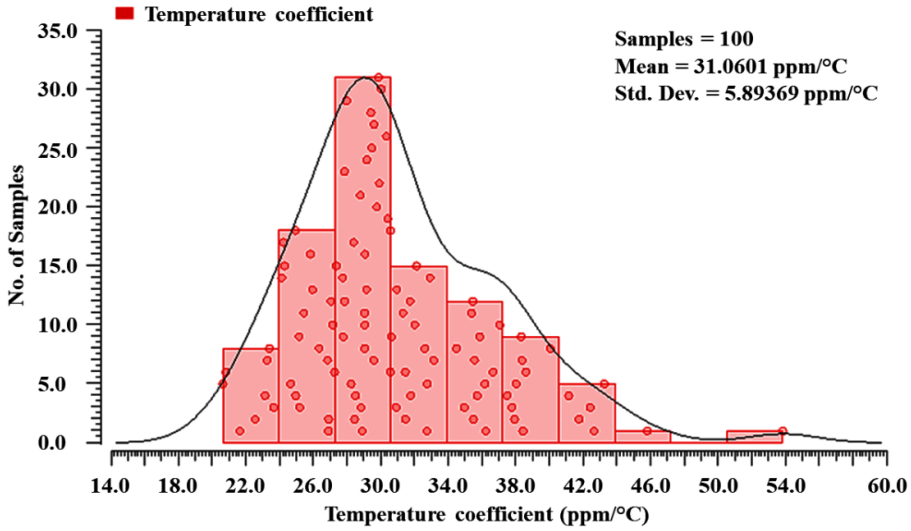
Figure 4.11 (c) illustrates the output noise versus frequency plots for different supply voltages such as 0.8 V, 1.0 V, 1.5 V, 2.0 V, 2.5 V, 3.0 V, 3.5 V, 4.0 V, 4.5 V, and 5.0 V at the nominal temperature of 27 ℃. From the figure, it is observed that the values of output noise for the different supply voltages are less than 408.35 nV/$\sqrt{\text{Hz}}$ at the frequency of 100 Hz.

4.2.2.1 Monte Carlo simulations

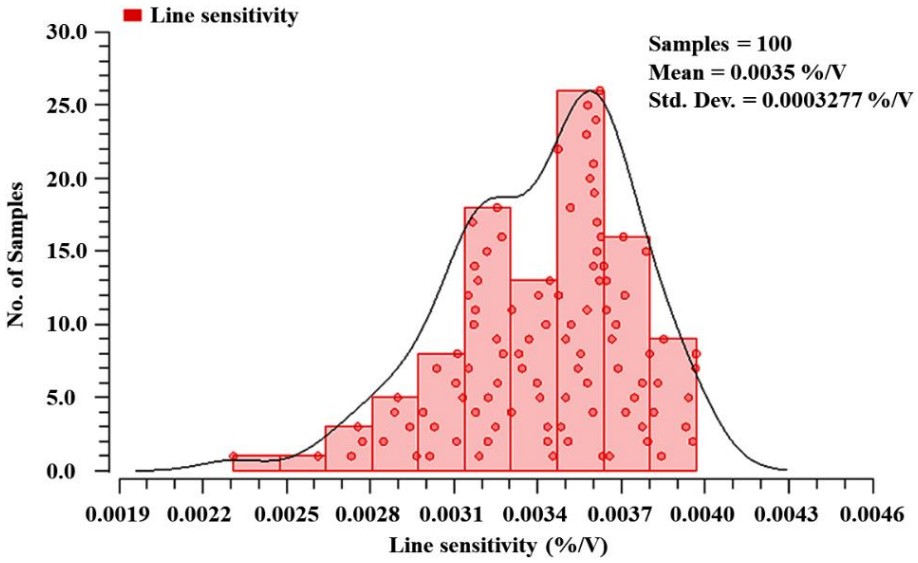
The Monte Carlo simulations for various performance parameters of the proposed CMOS voltage reference-II have been performed by considering both the process variations and mismatch-induced variations. The Monte Carlo simulation results of the output reference voltage (V_{REF}), TC, line sensitivity, and PSRR for 100 samples each have been presented in Figures 4.12 (a), (b), (c), and (d), respectively. These Monte Carlo simulation plots present a realistic picture of the proposed CMOS voltage reference-II behavior. From Figure 4.12 (a), the mean value of V_{REF} is obtained as 423.665 mV with a standard deviation of 8.98496 mV. From Figure 4.12 (b), the mean value of TC is obtained as 31.0601 ppm/℃ with a standard deviation of 5.89369 ppm/℃. From Figure 4.12 (c), the mean value of line sensitivity is observed as 0.0035 %/V with a standard deviation of 0.0003277 %/V. From Figure 4.12 (d), it is observed that the mean value of PSRR is -90.848 dB with a standard deviation of 8.6226 dB.


V_REF
Samples = 100
Mean = 423.665 mV
Std. Dev. = 8.98496 mV
No. of Samples
25.0
20.0
15.0
10.0
5.0
0.0
390.0 397.0 404.0 411.0 418.0 425.0 432.0 439.0 446.0 453.0 460.0
V_REF (mV)

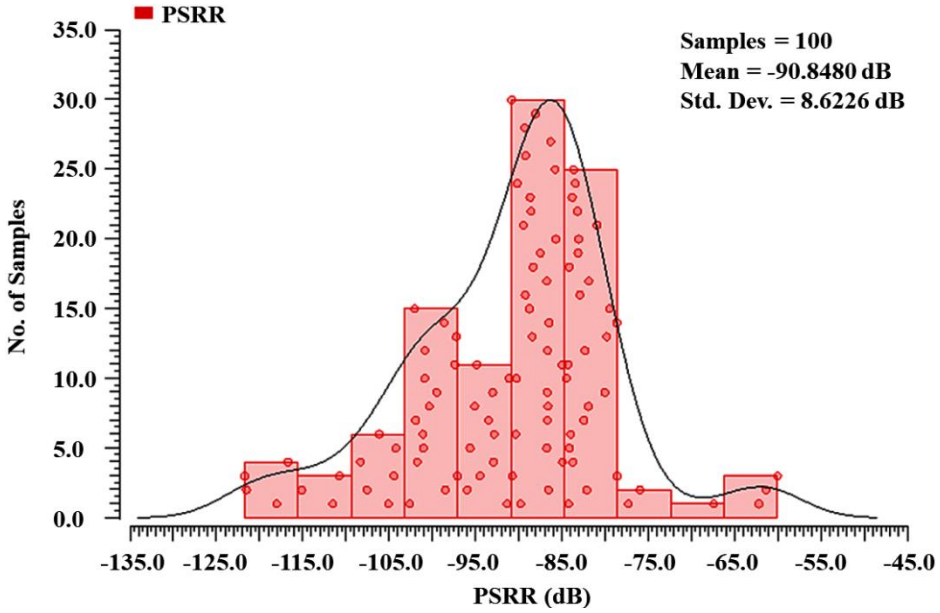
(a)


Temperature coefficient
Samples = 100
Mean = 31.0601 ppm/°C
Std. Dev. = 5.89369 ppm/°C
No. of Samples
35.0
30.0
25.0
20.0
15.0
10.0
5.0
0.0
14.0 18.0 22.0 26.0 30.0 34.0 38.0 42.0 46.0 50.0 54.0 60.0
Temperature coefficient (ppm/°C)

(b)


Line sensitivity
Samples = 100
Mean = 0.0035 %/V
Std. Dev. = 0.0003277 %/V
No. of Samples
30.0
25.0
20.0
15.0
10.0
5.0
0.0
0.0019 0.0022 0.0025 0.0028 0.0031 0.0034 0.0037 0.0040 0.0043 0.0046
Line sensitivity (%/V)

(c)



(d)

Figure 4.12 (a) Monte Carlo simulation results of the reference voltage (V_{REF}) for 100 samples (b) Monte Carlo simulation results of the TC for 100 samples (c) Monte Carlo simulation results of line sensitivity for 100 samples (d) Monte Carlo simulation results of PSRR for 100 samples

Table 4.4 shows the various performance parameters of the proposed CMOS voltage reference-II and the existing voltage references [66, 79, 81, 108-110]. For a fair comparison, three figures of merit FOM_1, FOM_2, and FOM_3 are used to compare the proposed CMOS voltage reference-II with existing voltage references.

Table 4.4 Comparison of proposed CMOS voltage reference-II with existing voltage references

References→ Parameters↓	[66]	[79]	[81]	[108]	[109]	[110]	Proposed voltage reference –II
Technology (nm)	180	180	180	180	130	180	180
Supply voltage (V)	3 to 5	1.2 to 2	1.2 to 1.8	1.5	1.6 to 1.8	4.5 to 5.5	0.8 to 5
Temp. range (°C)	-55 to 125	-40 to 125	0 to 100	-10 to 130	0 to 150	-40 to 100	-55 to 125
V_{REF} (mV)	2506	800	500	658	1112	2560	424.85
TC (ppm/℃)	25	34	22	9.6	13.1	2.6	29.5
PSRR (dB) @ 100 Hz	76	-62	-42	-42.3	-36	-63	-91.69
Line sensitivity (%/V)	0.08	0.2	0.280	0.89	0.24	0.2	0.0035
Area (mm^2)	0.0596	0.04	0.073	0.022	0.128	0.075	0.003
Power consumption (µW)	45	9.996	6.12	449	288	30.6	6.1
FOM_1 ($°C^3/W.m^2$)	0.51	2.01	1.02	0.21	0.05	3.28	60.02
FOM_2 (dB.°C/ ppm.µA.mm^2)	3.56	5.47	5.13	0.66	0.12	47.51	135.6
FOM_3 ($(°C/m)^2$. $(dB/W.ppm.\ \mu A)^{1/2}.10^3$)	2.54	3.32	2.29	0.3	0.008	12.48	90.22

The proposed CMOS voltage reference-II has higher FOM_1, FOM_2, and FOM_3 than the existing voltage references [66, 79, 81, 108-110] which confirm its better performance. From Table 4.4, it can also be concluded that the proposed circuit has numerous advantages such as low supply voltage requirement, low line sensitivity, high PSRR, large operating supply voltage range, and wide temperature range. Low line sensitivity and high PSRR define the robustness of the proposed circuit against supply voltage variations and supply noise.

4.3 Simulation results of proposed CMOS voltage reference-III and IV

In this section, the post-layout simulation results of proposed CMOS voltage reference-III and CMOS voltage reference-IV are discussed.

4.3.1 Post-layout simulation results of proposed CMOS voltage reference-III

The aspect ratios (W/L) of MOS transistors and the values of resistances used in the proposed CMOS voltage reference-III are listed in Table 4.5. For the simulations, the operating temperature and supply voltage of the proposed CMOS voltage reference-III are chosen as 27 ℃ and 0.8 V, respectively.

Table 4.5 Circuit elements' dimensions used in proposed CMOS voltage reference-III

Circuit elements' dimensions			
NMOS transistors	W/L (μm/μm)	PMOS transistors	Aspect ratios (μm/μm)
M_1	2/0.5	M_3, M_{17}	5/0.5
M_2	5/0.5	M_4, M_{18}	5/1
M_{13}	10/0.18	M_5, M_8	24/0.18
M_{14}	2/0.18	M_6, M_{20}	5/0.5
M_{15}	2/0.2	M_7, M_{21}	2/0.4
M_{16}	5/0.5	M_{19}, M_{22}	24/0.18
		M_9, M_{10}	24/0.18
Resistors		(kΩ)	
R_1		325	
R_2		320	
R_{REF}		385	

The physical layout of the proposed CMOS voltage reference-III is illustrated in Figure 4.13. The proposed circuit occupies an area of 45.75 µm × 59.65 µm.

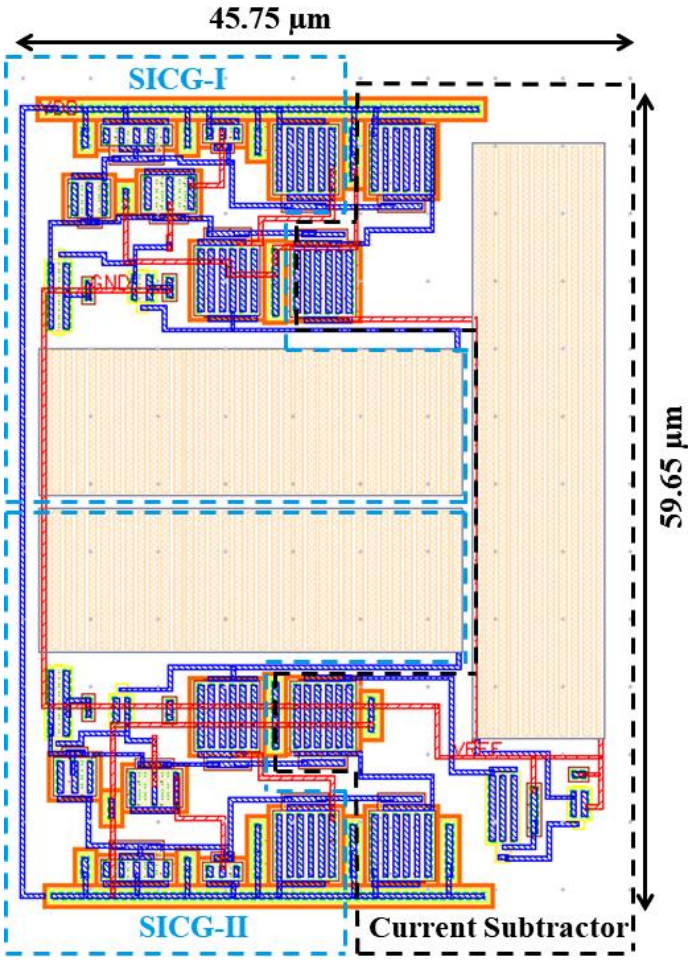


Figure 4.13 Layout of the proposed CMOS voltage reference-III

The plot of the output reference voltage (V_{REF}) with respect to the temperature is shown in Figure 4.14. The temperature is varying from -40 ℃ to 125 ℃. From the figure, the value of V_{REF} at a nominal temperature of 27℃ is obtained as 312 mV. The maximum deviation of V_{REF} is observed as 2 mV over the temperature ranging from -40 ℃ to 125 ℃ and therefore, the TC of 38.85 ppm/℃ is achieved. The variation of V_{REF} versus supply voltage plot is shown in Figure 4.15 (a), in which the supply voltage varies from 0 V to 3 V at a nominal temperature of 27℃. From the figure, it can be seen that the proposed CMOS voltage reference-III works properly when the supply voltage is more than or equal to 0.80 V. The line sensitivity of the proposed CMOS voltage reference-III is calculated as 0.027 %/V for the supply voltage ranging from 0.80 V to 3 V. The output reference voltage (V_{REF}) versus supply voltage plots for different operating temperatures such as -40 ℃, 0 ℃, 27 ℃, 100 ℃, and 125 ℃ are shown in Figure 4.15 (b).

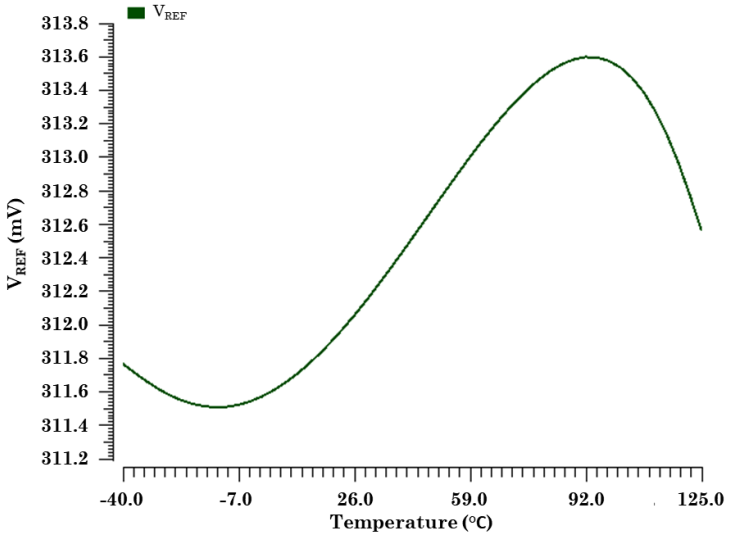
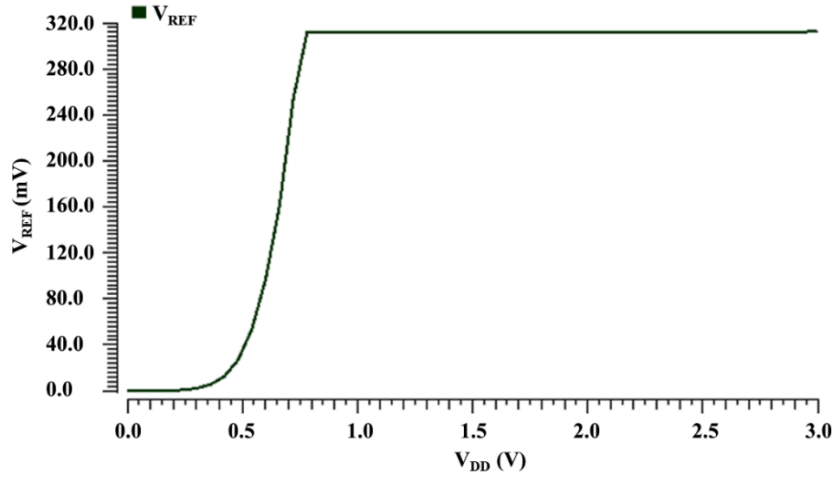
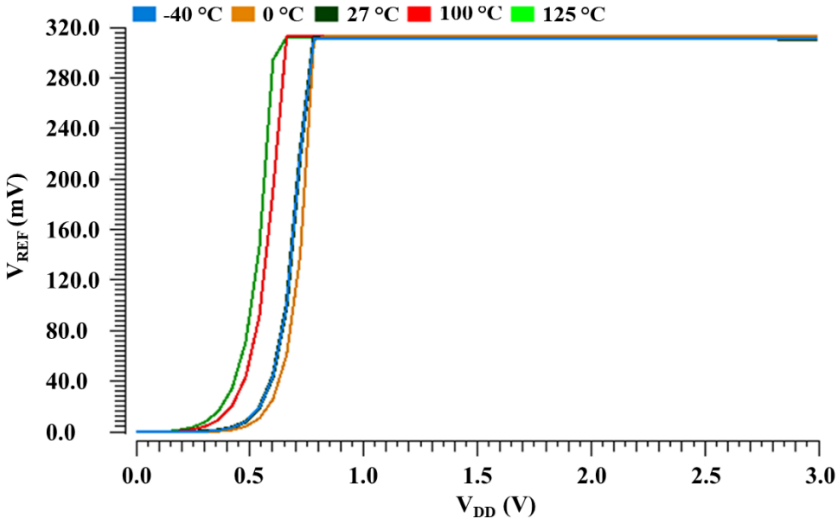


Figure 4.14 Output reference voltage (V_{REF}) versus temperature plot of the proposed CMOS voltage reference-III



(a)

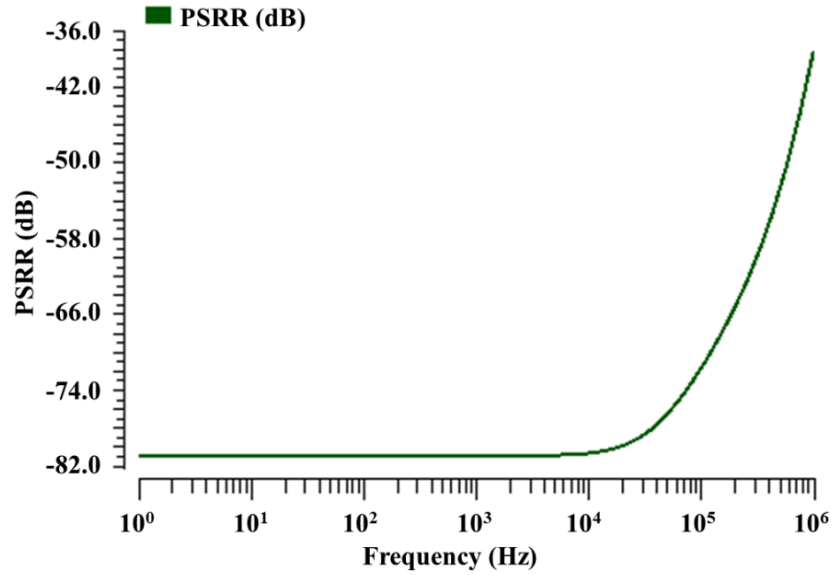


(b)

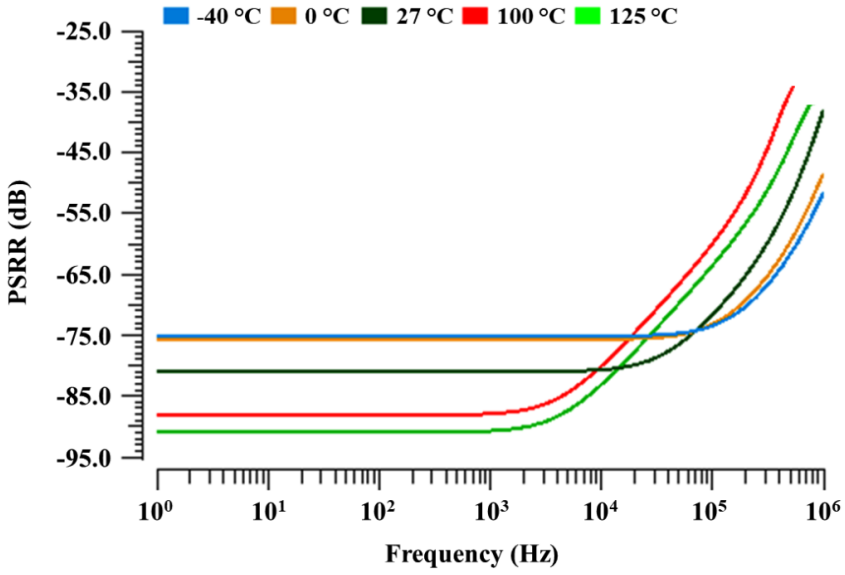
Figure 4.15 (a) Variation of V_{REF} with respect to the supply voltage (b) Output reference voltage (V_{REF}) versus supply voltage plots for different operating temperatures

It is observed that the variation of the output reference voltage (V_{REF}) with respect to supply voltage remains almost the same for different operating temperatures. The worst-case value of line sensitivity is observed as 0.04%/V for the different operating temperatures.

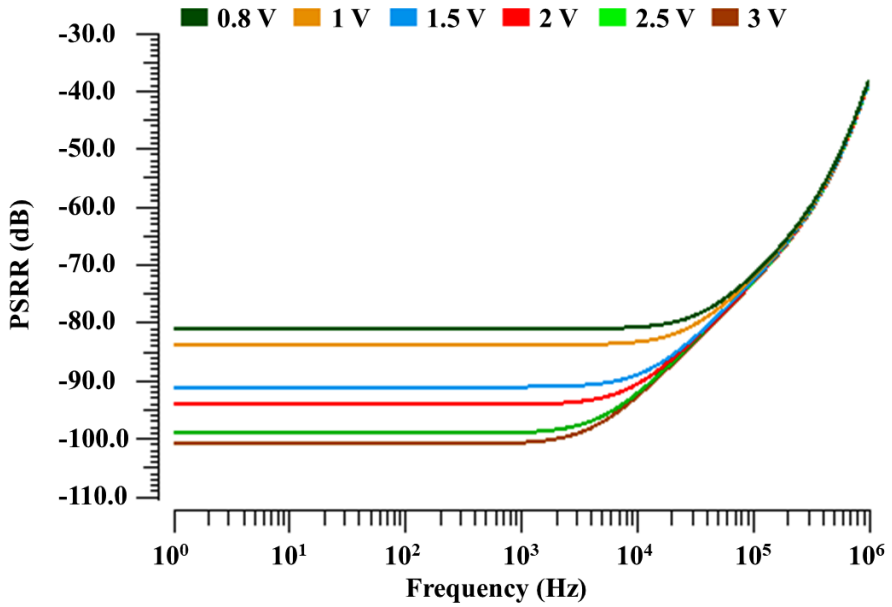
The PSRR versus frequency plot of the proposed CMOS voltage reference-III is illustrated in Figure 4.16 (a). From the figure, the values of PSRR of the proposed CMOS voltage reference-III are obtained as -80.84 dB, -80.84 dB, and -80.55 dB at the frequencies of 100 Hz, 1 kHz, and 10 kHz, respectively. For different operating temperatures such as -40 ℃, 0 ℃, 27 ℃, 100 ℃, and 125 ℃, the PSRR versus frequency plots are shown in Figure 4.16 (b). From the plots, it is observed that the minimum value of PSRR for different temperatures is -75.05 dB at the frequency of 100 Hz.



(a)



(b)

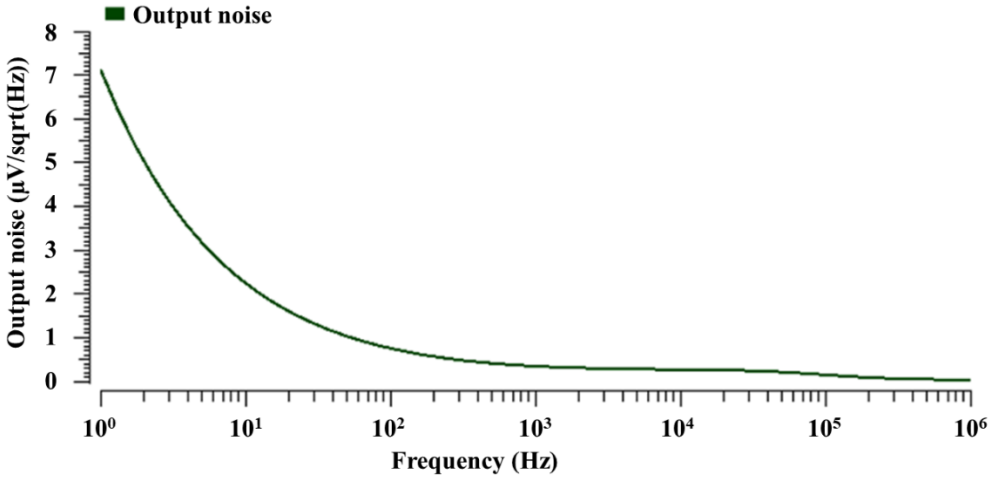


(c)

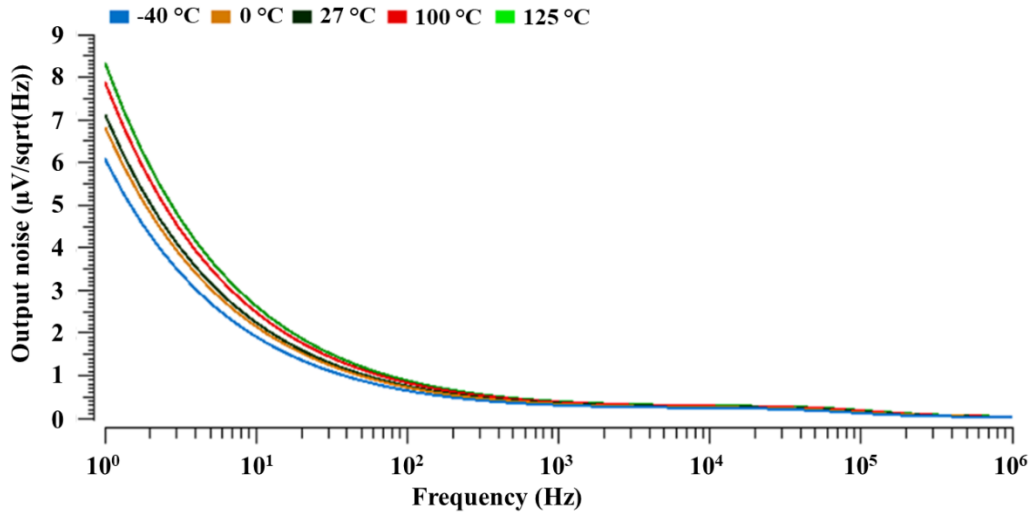
Figure 4.16 (a) PSRR versus frequency plot of proposed CMOS voltage reference-III (b) PSRR versus frequency plots for different operating temperatures (c) PSRR versus frequency plots for different supply voltages

The PSRR versus frequency plots at a nominal temperature of 27 ℃ for different supply voltages such as 0.8 V, 1 V, 1.5 V, 2 V, 2.5 V, and 3 V are shown in Figure 4.16 (c). The figure shows that the minimum value of PSRR for different supply voltages is -80.84 dB at the frequency of 100 Hz. Hence, it can be concluded that the proposed CMOS voltage reference-III can work efficiently under the supply noise and other undesired signals imposed on the supply voltage**.**

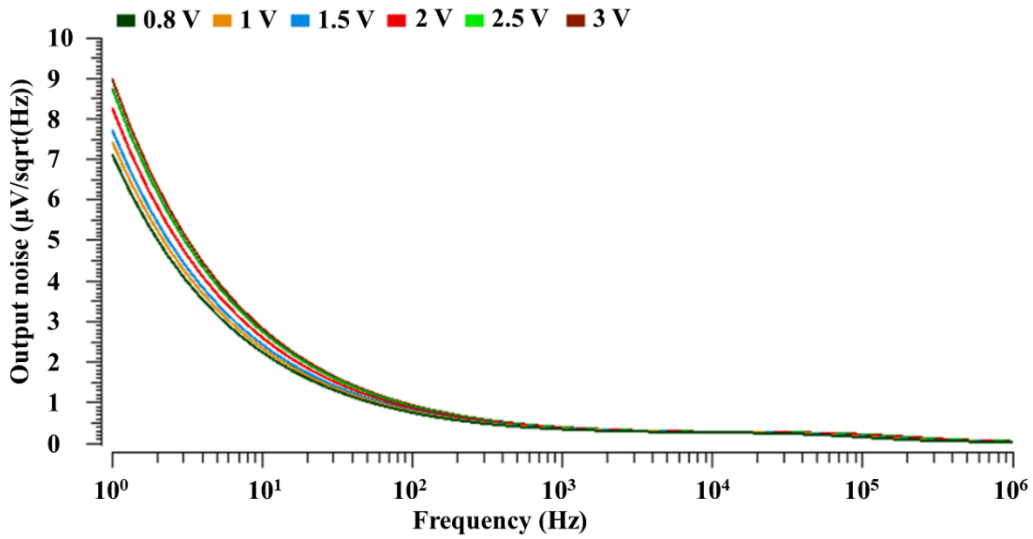
The output noise versus frequency plot of the proposed CMOS voltage reference-III is shown in Figure 4.17 (a). From the plot, the values of output noise are obtained as 772.4 nV/$\sqrt{\text{Hz}}$, 361 nV/$\sqrt{\text{Hz}}$, and 282.5 nV/$\sqrt{\text{Hz}}$ at the frequencies of 100 Hz, 1 kHz, and 10 kHz, respectively.



(a)



(b)



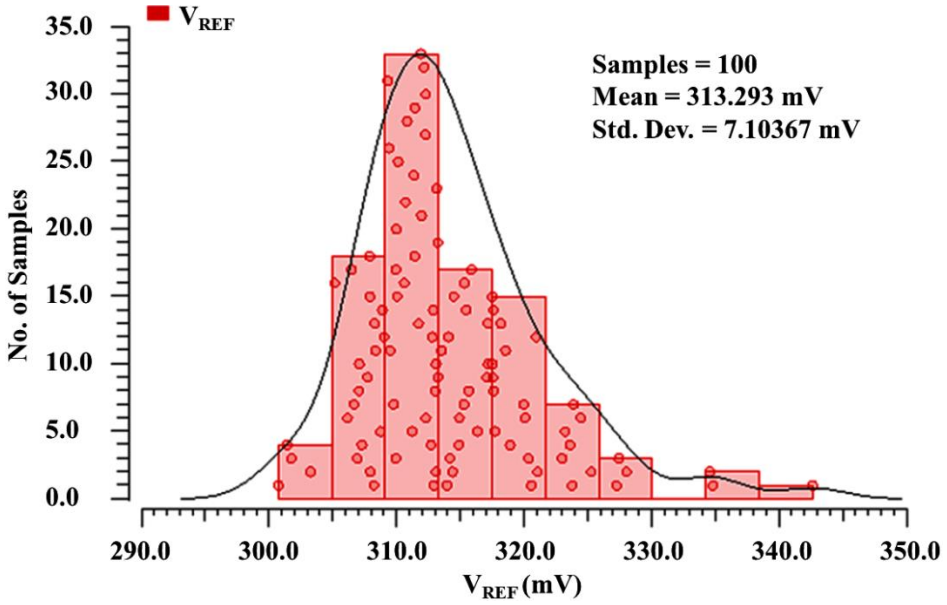
(c)

Figure 4.17 (a) Output noise versus frequency plot of the proposed CMOS voltage reference-III (b) Output noise versus frequency plots for different operating temperatures (c) Output noise versus frequency plots for different supply voltages

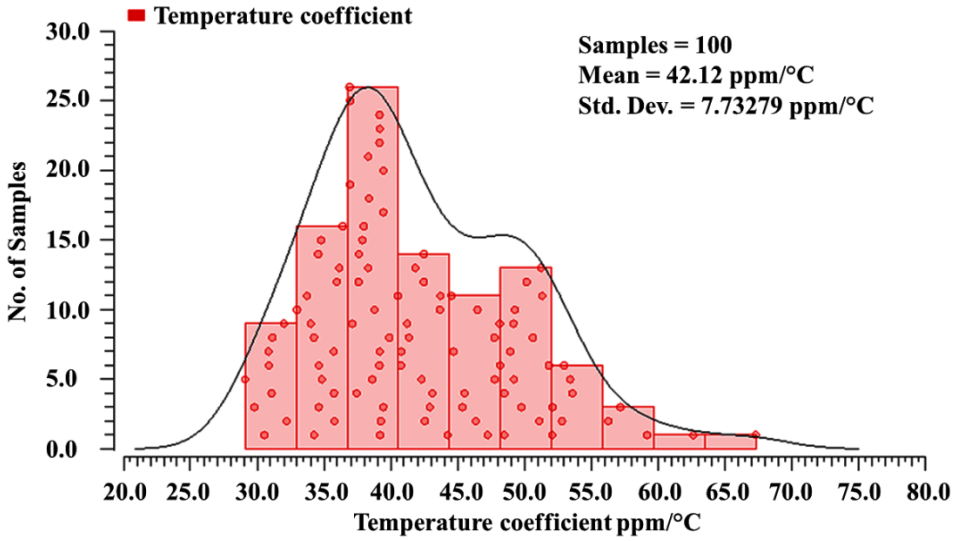
Figure 4.17 (b) illustrates the plots of output noise with respect to the frequency for different operating temperatures such as -40 ℃, 0 ℃, 27 ℃, 100 ℃, and 125 ℃. From the figure, it can be seen that the values of output noise are less than 897.8 nV/$\sqrt{\text{Hz}}$ for different operating temperatures at the frequency of 100 Hz. Figure 4.17 (c) shows the output noise versus frequency plots for different supply voltages such as 0.8 V, 1 V, 1.5 V, 2 V, 2.5 V, and 3 V at the nominal temperature of 27 ℃. From the figure, it is observed that the values of output noise for the different supply voltages are less than 956.44 nV/$\sqrt{\text{Hz}}$ at the frequency of 100 Hz.

4.3.1.1 Monte Carlo simulations

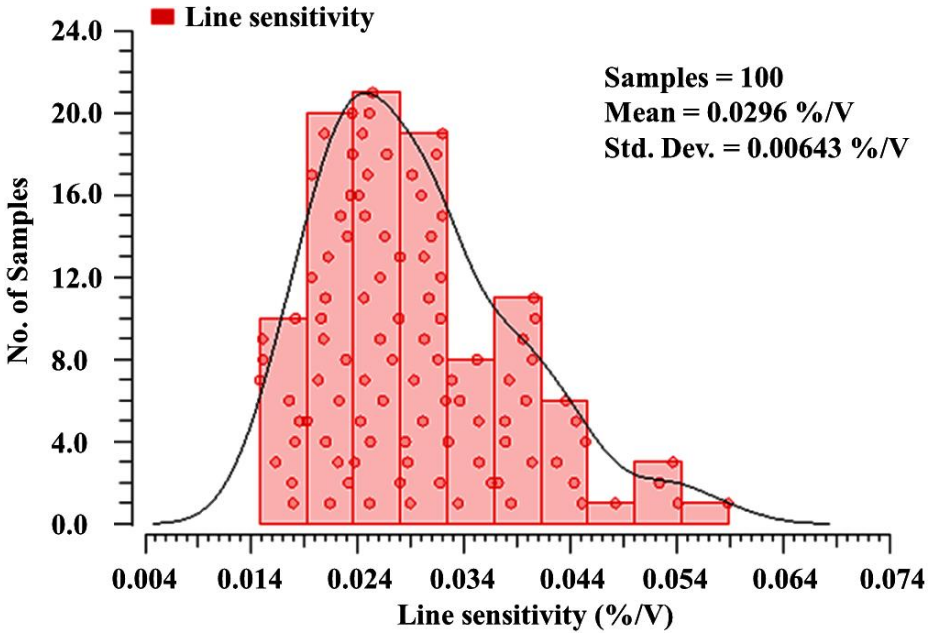
The Monte Carlo simulations of the proposed CMOS voltage reference-III for 100 samples have been performed by considering both the mismatch-induced and process variations. Figures 4.18 (a), (b), (c), and (d) show the Monte Carlo simulations of the output reference voltage (V_{REF}), TC, line sensitivity, and PSRR, respectively. These Monte Carlo simulation plots show the realistic picture of the proposed CMOS voltage reference-III behaviour. From Figure 4.18 (a), it is observed that the mean value of V_{REF} is 313.29 mV with a standard deviation of 7.1 mV. From Figure 4.18 (b), it can be seen that the mean value of TC is 42.12 ppm/℃ with a standard deviation of 7.73279 ppm/℃.



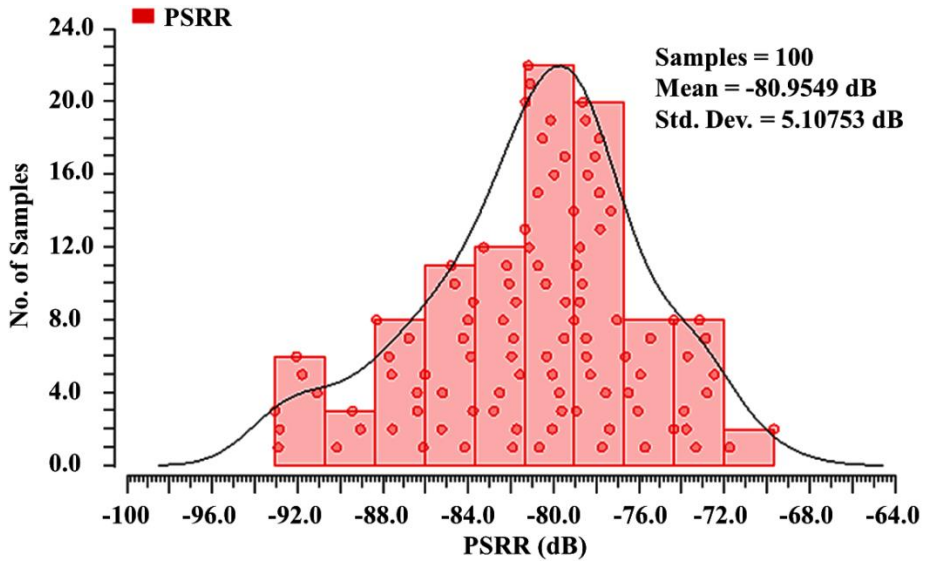
(a)



(b)



(c)



(d)

Figure 4.18 (a) Monte Carlo simulation results of the reference voltage (V_{REF}) for 100 samples (b) Monte Carlo simulation results of the TC for 100 samples (c) Monte Carlo simulation results of line sensitivity for 100 samples (d) Monte Carlo simulation results of PSRR for 100 samples.

From Figure 4.18 (c), it is observed that the mean value of line sensitivity is 0.0296 %/V with a standard deviation of 0.00643 %/V. From Figure 4.18 (d), it is observed that the mean value of PSRR is -80.95 dB with a standard deviation of 5.11dB.

The performance parameters of the proposed CMOS voltage reference-III and existing voltage references [25, 66, 73, 78, 81, 89, 105, 108, 111-112] are listed in Table 4.6. For a fair comparison, three figures of merit FOM_1, FOM_2, and FOM_3 are used to compare the proposed CMOS voltage reference-III with existing voltage references. From Table 4.6, it is observed that the proposed CMOS voltage reference-III achieves a higher FOM_1 of 94.4, FOM_2 of 224.03, and FOM_3 of 145.43 than the existing voltage references, which confirm its better performance. The proposed CMOS voltage reference-III achieves higher FOM_1 mainly because of the wide temperature range, low TC, low power, and less area in comparison to the existing voltage references. The higher FOM_2 confirms that the proposed CMOS voltage reference-III has higher PSRR, lower TC, lesser area, and lower supply current than the existing voltage references. The high PSRR and low line sensitivity define the robustness of the proposed CMOS voltage reference-III against the supply noise and supply voltage variations.

Table 4.6 Comparison of proposed CMOS voltage reference-III with existing voltage references

References→ Parameters↓	[25]	[66]	[73]	[78]	[81]	[89]	[105]	[108]	[111]	[112]	Proposed voltage reference – III
Technology (nm)	350	180	130	130	180	130	180	180	180	180	180
Supply voltage (V)	1.8	3 to 5	1 to 2.3	1 to 3.3	1.2 to 1.8	1.1 to 1.3	1.8	1.5	1.2 to 1.8	0.95 to 2.5	0.8 to 3
Temp. range (˚C)	0 to 130	-55 to 125	0 to 100	-40 to 85	0 to 100	-40 to 120	-20 to 120	-10 to 130	-40 to 100	-20 to 100	-40 to 125
V_{REF} (mV)	847.5	2506	781	598	500	735	410.39	658	500	169.4	312
TC (ppm/℃)	13.6	25	48	47	22	9.3	7.3	9.6	15.19	64	38.85
PSRR (dB) @ 100 Hz	-72	76	-51.4	-44	-42	-30	-52.6	-42.3	-57	-----	-80.84
Line sensitivity (%/V)	0.0185	0.08	0.34	0.19	0.280	-----	-----	0.89	0.25	0.11	0.027
Area (mm^2)	0.011	0.0596	0.053	0.02	0.073	0.063	-----	0.022	0.072	0.029	0.0027
Power consumption (µW)	14.4	45	8.1	1	6.12	1.44	5.61	449	6	2.4	2.75
FOM_1 ($°C^3/W.m^2$)	7.84	0.51	0.41	16.62	1.02	0.3	----	0.21	3	3.2	94.4
FOM_2 (dB.°C/ ppm.µA.mm^2)	60.16	3.56	2.5	46.81	5.13	0.43	----	0.66	10.42	----	224.03
FOM_3 ($(°C/m)^2$. (dB/W.ppm. µA)$^{1/2}$.10^3)	21.72	2.54	1.6	27.89	2.29	0.24	----	0.3	5.59	----	145.43

4.3.2 Post-layout simulation results of proposed CMOS voltage reference-IV

The aspect ratios (W/L) of MOS transistors and the values of resistances used in the proposed CMOS voltage reference-IV are listed in Table 4.7. For the simulations, the operating temperature and supply voltage of the proposed CMOS voltage reference-IV are chosen as 27 ℃ and 0.65 V, respectively.

Table 4.7 Circuit elements' dimensions used in proposed CMOS voltage reference-IV

Circuit elements' dimensions			
NMOS transistors	W/L (μm/μm)	PMOS transistors	W/L (μm/μm)
M_3	0.5/0.5	M_1	0.4/8
M_6	1/4	M_4	1/2
M_7	1/4	M_8	1/1
M_{10}	1/2	M_9	5/3
M_{12}	10/2	M_{11}	5/3
M_{16}	1/2	M_{13}	2/1
M_{17}	1/2	M_{14}	3/1
		M_{15}	1/1
Resistors		(kΩ)	
R_1		600	
R_B		200	
R_{REF}		600	

The physical layout of the proposed CMOS voltage reference-IV is shown in Figure 4.19. The proposed circuit occupies an area of 57.48 μm × 50.36 μm.

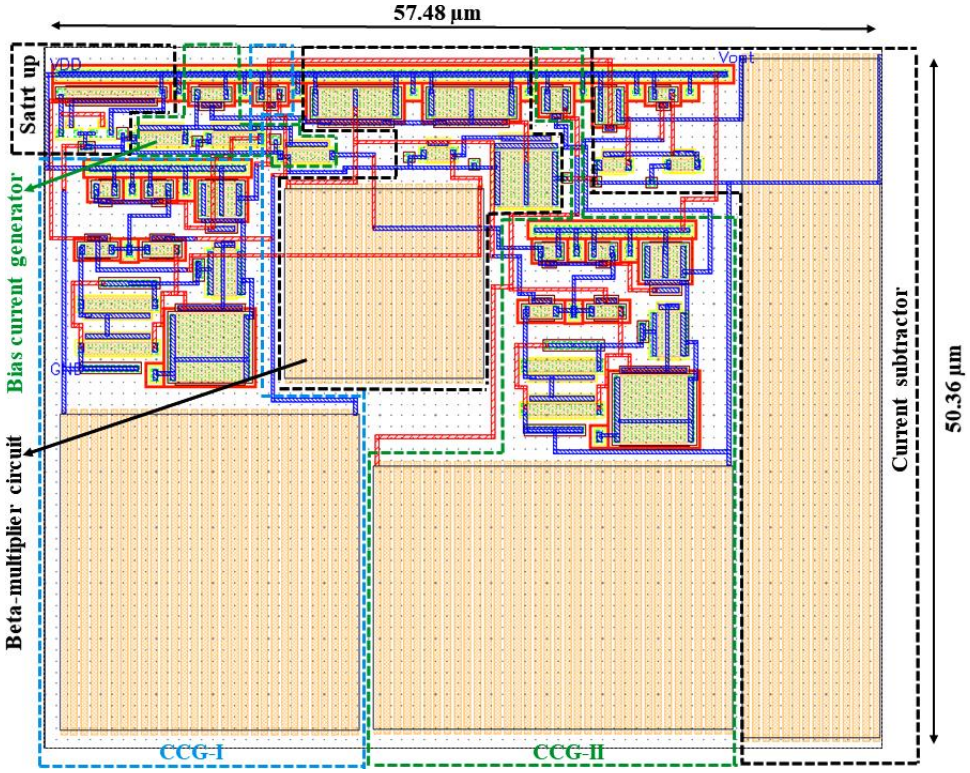


Figure 4.19 Layout of the proposed voltage reference-IV

The output reference voltage (V_{REF}) versus temperature plot of the proposed CMOS voltage reference-IV is shown in Figure 4.20. The temperature is varying from -55 ℃ to 125 ℃. From the figure, the value of V_{REF} at a nominal temperature of 27 ℃ is obtained as 350 mV. The maximum variation of V_{REF} is 2 mV over the temperature ranging from -55 ℃ to 125 ℃, which gives the TC of 31.5 ppm/℃. Figure 4.21 (a) shows the variation of V_{REF} with respect to the supply voltage ranging from 0 V to 3.5 V at a nominal temperature of 27 ℃. From the plot, it can be seen that the proposed CMOS voltage reference-IV works properly when the supply voltage is more than or equal to 0.65 V. The line sensitivity of the proposed CMOS voltage reference-IV is also observed as 0.015 %/V for the supply voltage ranging from 0.65 V to 3.5 V.

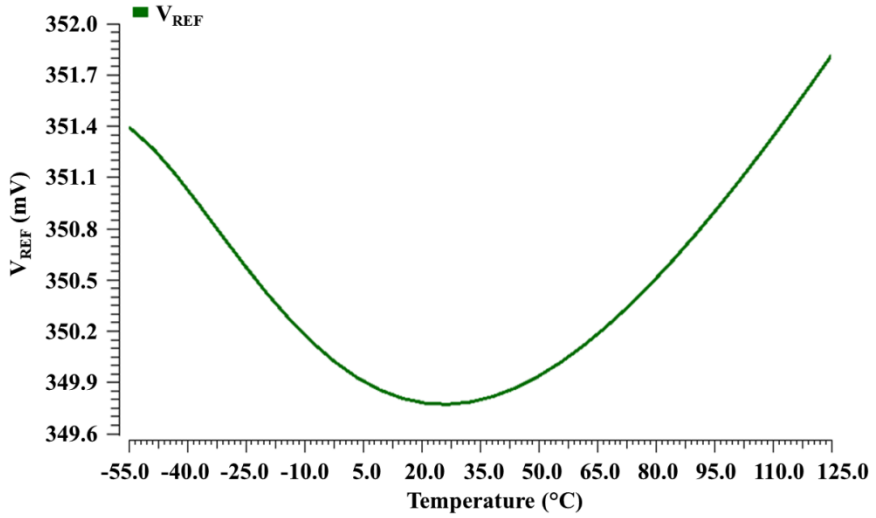
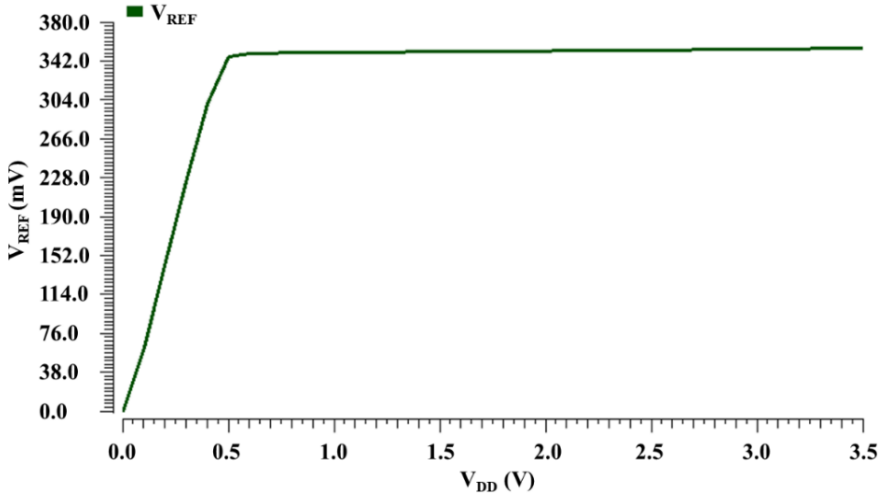
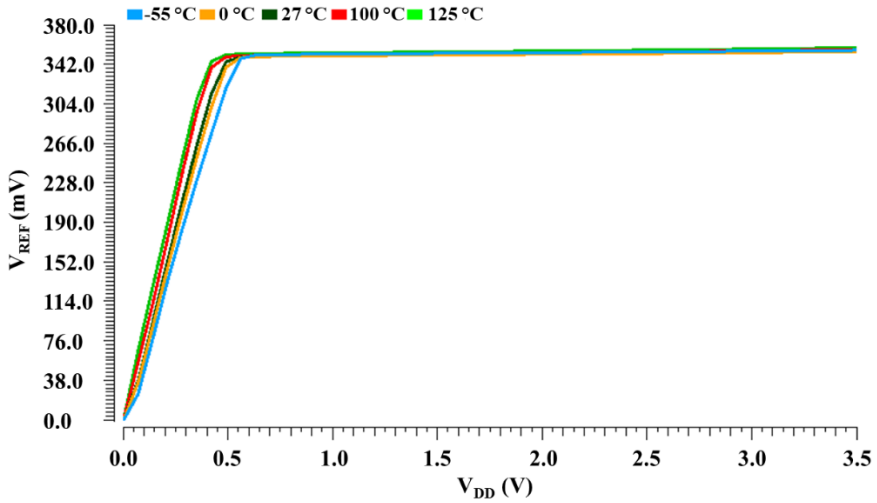


Figure 4.20 Output reference voltage (V_{REF}) of the proposed CMOS voltage reference-IV



(a)

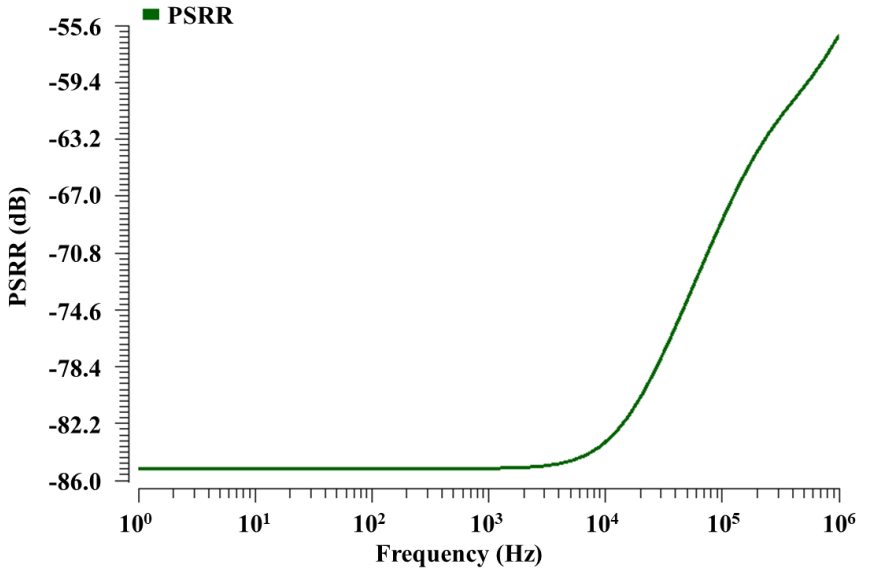


(b)

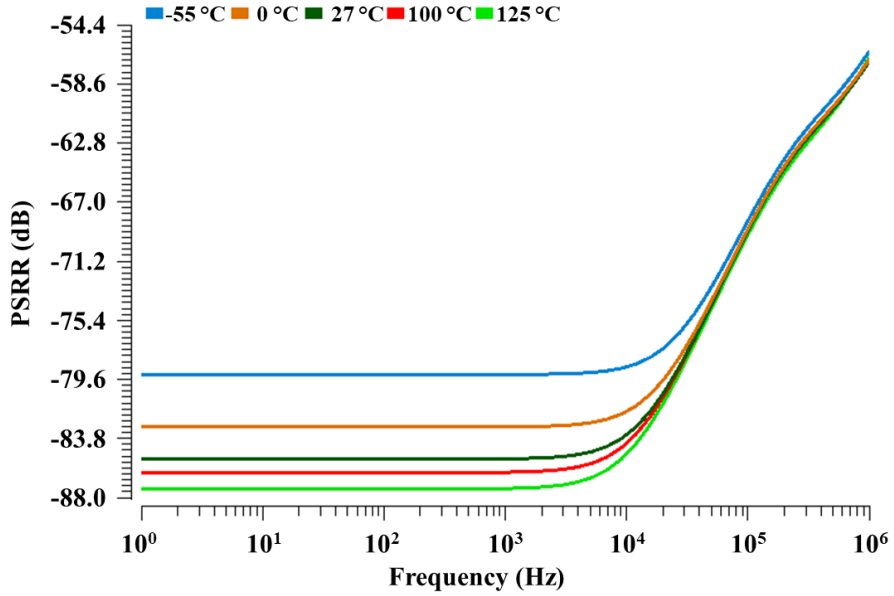
Figure 4.21 (a) Variation of V_{REF} with respect to supply voltage (b) Output reference voltage (V_{REF}) versus supply voltage plots for different operating temperatures

The output reference voltage (V_{REF}) versus supply voltage plots for different operating temperatures such as -55 ℃, 0 ℃, 27 ℃, 100 ℃, and 125 ℃, are shown in Figure 4.21 (b). It is observed that the variation of the output reference voltage (V_{REF}) with respect to supply voltage remains almost the same for different operating temperatures. The worst-case value of line sensitivity is observed as 0.021%/V for the different operating temperatures.

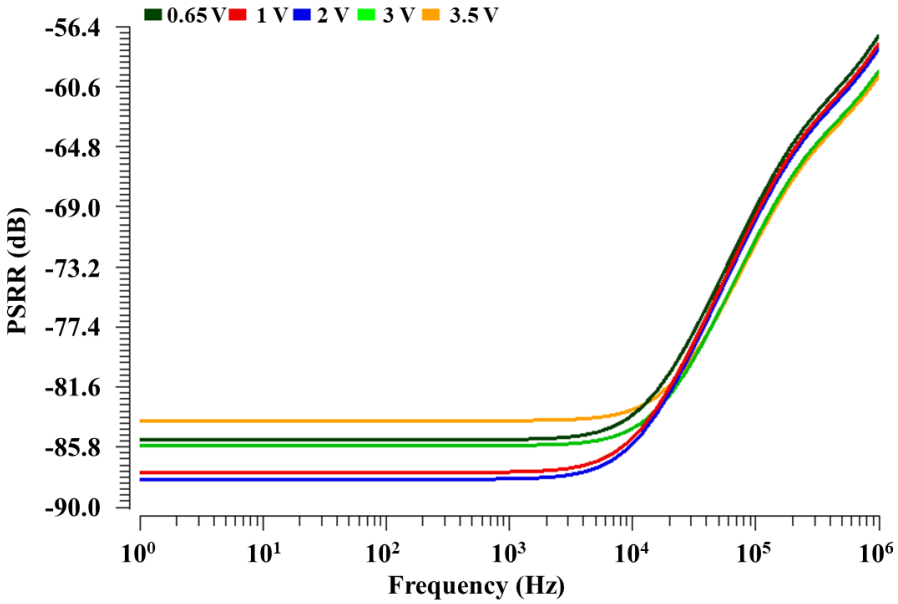
The PSRR versus frequency plot of the proposed CMOS voltage reference-IV is shown in Figure 4.22 (a). From the figure, the values of PSRR of the proposed CMOS voltage reference-IV are obtained as -85.4 dB, -85.19 dB, and -83.47 dB at the frequencies of 100 Hz, 1 kHz, and 10 kHz, respectively.



(a)



(b)



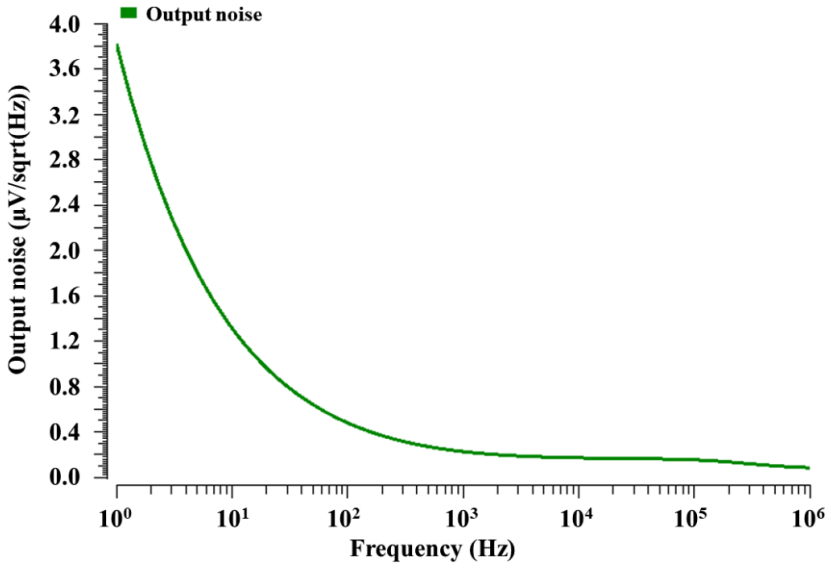
(c)

Figure 4.22 (a) PSRR versus frequency plot of proposed CMOS voltage reference-IV (b) PSRR versus frequency plots for different operating temperatures (c) PSRR versus frequency plots for different supply voltages

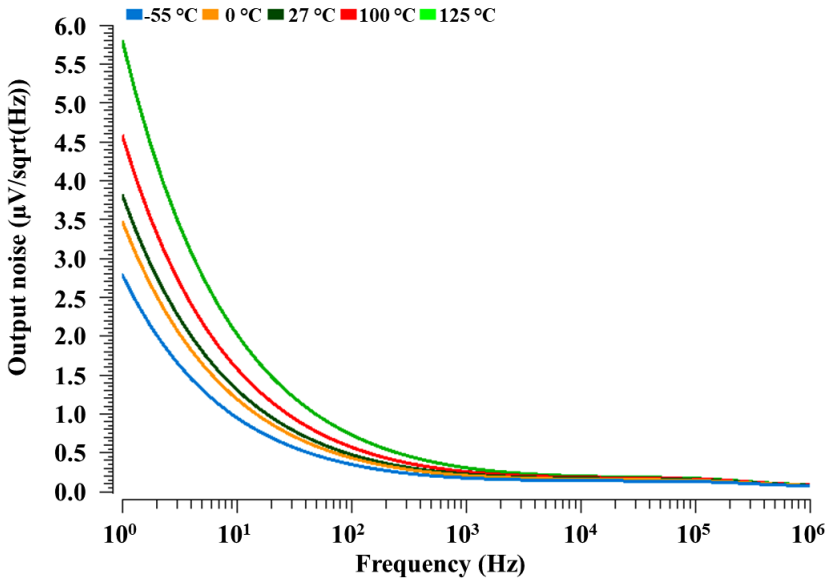
For different operating temperatures such as -55 ℃, 0 ℃, 27 ℃, 100 ℃, and 125 ℃, the PSRR versus frequency plots are shown in Figure 4.22 (b). From the plots, it is observed that the minimum value of PSRR for different temperatures is -79.11 dB at the frequency of 100 Hz. The PSRR versus frequency plots at a nominal temperature of 27 ℃ for different supply voltages such as 0.65 V, 1 V, 2 V, 3 V, and 3.5 V are shown in Figure 4.22 (c). The figure shows that the minimum value of PSRR for different supply voltages is -83 dB at the frequency of 100 Hz.

Hence, it can be concluded that the proposed CMOS voltage reference-IV can work efficiently under the supply noise and other undesired signals imposed on the supply voltage.

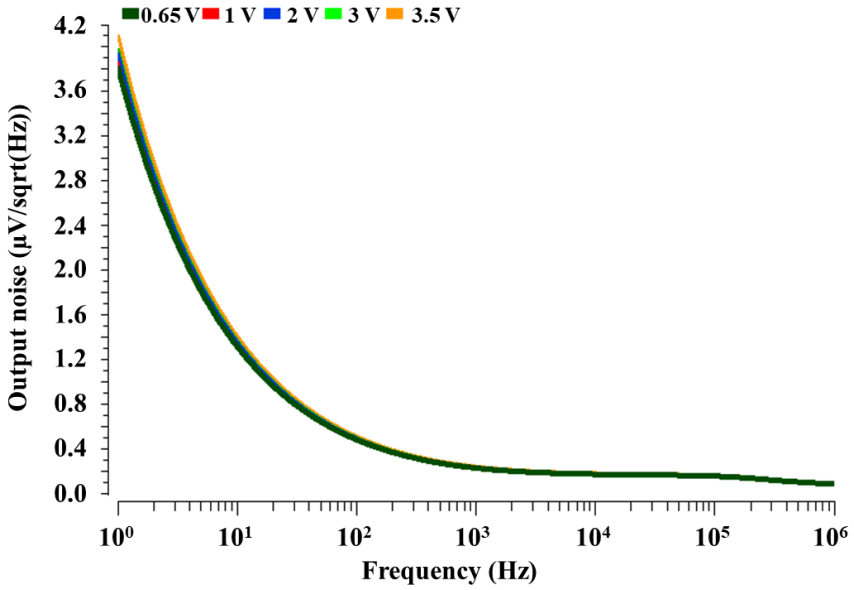
The output noise versus frequency plot of the proposed CMOS voltage reference-IV is illustrated in Figure 4.23 (a). From the plot, the values of output noise are obtained as 485.2 nV/$\sqrt{\text{Hz}}$, 229.87 nV/$\sqrt{\text{Hz}}$, and 174.96 nV/$\sqrt{\text{Hz}}$ at the frequencies of 100 Hz, 1 kHz, and 10 kHz, respectively. Figure 4.23 (b) depicts the plots of output noise with respect to the frequency for different operating temperatures such as -55 ℃, 0 ℃, 27 ℃, 100 ℃, and 125 ℃. From the figure, it is observed that the values of output noise for the different supply voltages are less than 740.1 nV/$\sqrt{\text{Hz}}$ at the frequency of 100 Hz.



(a)



(b)



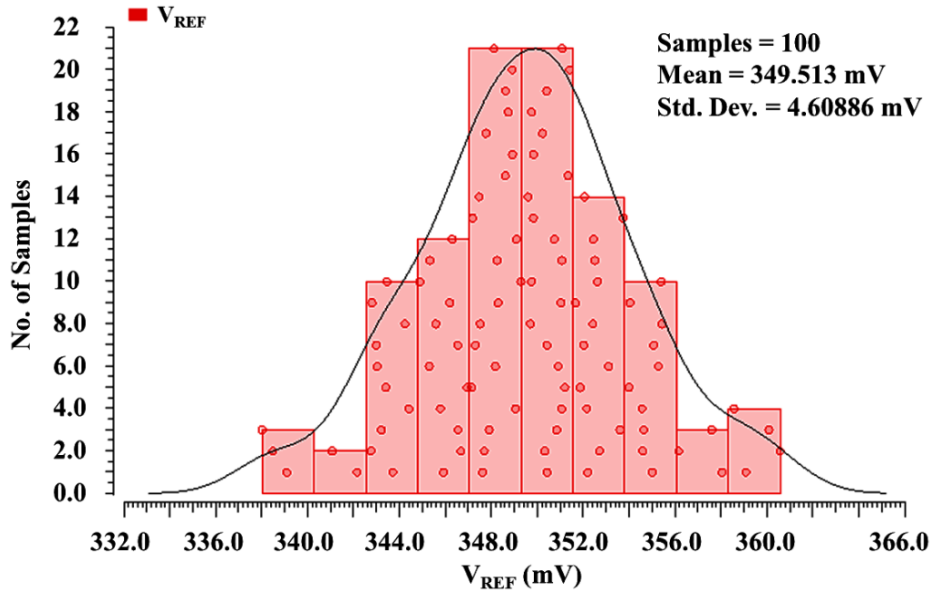
(c)

Figure 4.23 (a) Output noise versus frequency plot of the proposed CMOS voltage reference-IV (b) Output noise versus frequency plots for different operating temperatures (c) Output noise versus frequency plots for different supply voltages

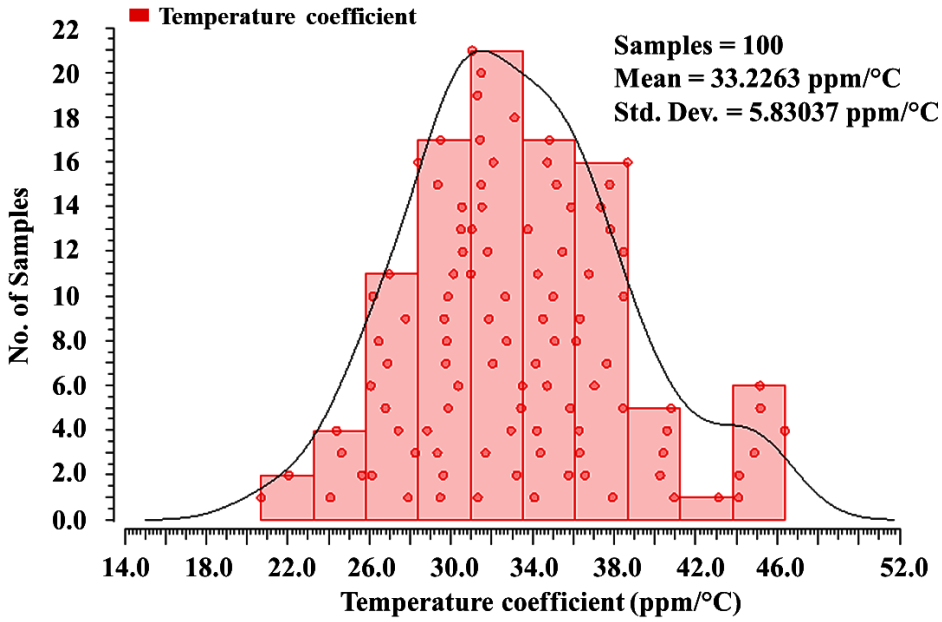
Figure 4.23 (c) shows the output noise versus frequency plots for different supply voltages such as 0.65 V, 1 V, 2 V, 3 V, and 3.5 V at the nominal temperature of 27 ℃. From the figure, it is observed that the values of output noise for the different supply voltages are less than 517.8 nV/$\sqrt{\text{Hz}}$ at the frequency of 100 Hz.

4.3.2.1 Monte Carlo simulations

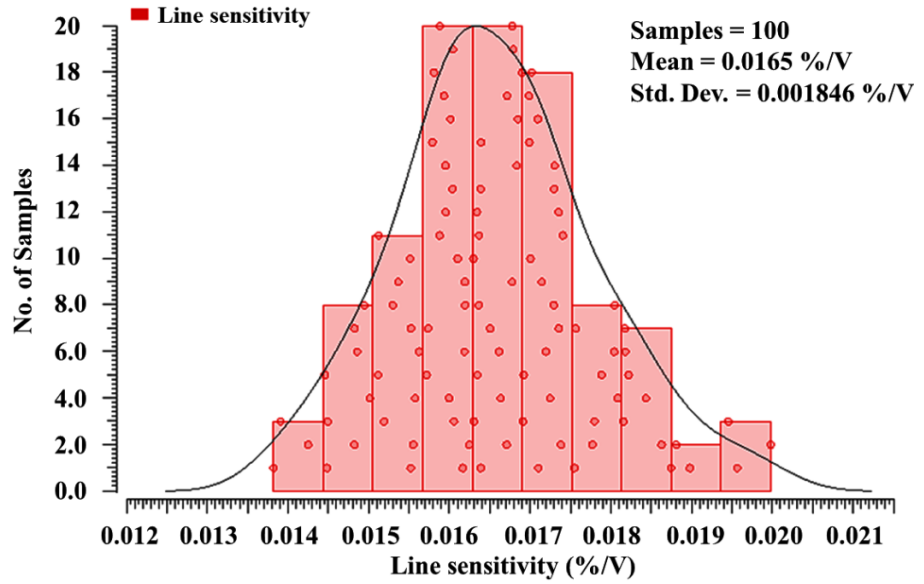
The Monte Carlo simulations for various performance parameters of the proposed CMOS voltage reference-IV have been performed by considering both the process variations and mismatch-induced variations. The Monte Carlo simulation results of the output reference voltage (V_{REF}), TC, line sensitivity, and PSRR for 100 samples each have been presented in Figures 4.24 (a), (b), (c), and (d), respectively. These Monte Carlo simulation plots present the realistic picture of the proposed CMOS voltage reference-IV behaviour. From Figure 4.24 (a), the mean value of V_{REF} is obtained as 349.51 mV with a standard deviation of 4.61 mV. From Figure 4.24 (b), the mean value of TC is obtained as 33.22 ppm/°C with a standard deviation of 5.83 ppm/℃. From Figure 4.24 (c), the mean value of line sensitivity is observed as 0.0165 %/V with a standard deviation of 0.001846 %/V. From Figure 4.24 (d), it is observed that the mean value of PSRR is -83.49 dB with a standard deviation of 4.178 dB.


VREF
Samples = 100
Mean = 349.513 mV
Std. Dev. = 4.60886 mV
No. of Samples
0.0
2.0
4.0
6.0
8.0
10
12
14
16
18
20
22
332.0
336.0
340.0
344.0
348.0
352.0
356.0
360.0
366.0
VREF (mV)

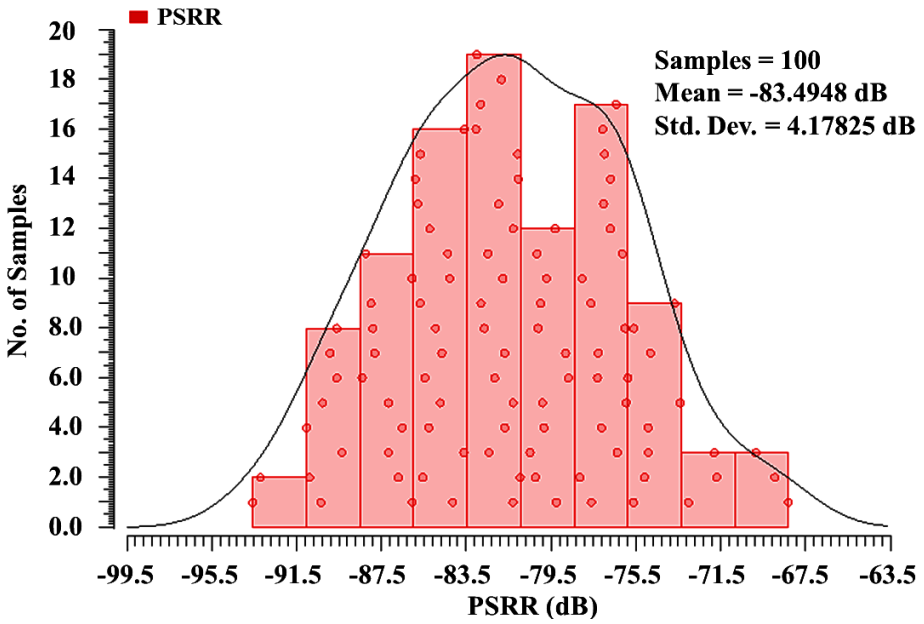
(a)


Temperature coefficient
Samples = 100
Mean = 33.2263 ppm/°C
Std. Dev. = 5.83037 ppm/°C
No. of Samples
0.0
2.0
4.0
6.0
8.0
10
12
14
16
18
20
22
14.0
18.0
22.0
26.0
30.0
34.0
38.0
42.0
46.0
52.0
Temperature coefficient (ppm/°C)

(b)



(c)



(d)

Figure 4.24 (a) Monte Carlo simulation results of the reference voltage (V_{REF}) for 100 samples (b) Monte Carlo simulation results of the TC for 100 samples (c) Monte Carlo simulation results of line sensitivity for 100 samples (d) Monte Carlo simulation results of PSRR for 100 samples

Table 4.8 shows the various performance parameters of the proposed CMOS voltage reference-IV and the voltage references available in the literature [66, 72-73, 81, 89, 108-111]. For a fair comparison, three figures of merit FOM_1, FOM_2, and FOM_3 are used to compare the proposed CMOS voltage reference-IV with the existing voltage references [66, 72-73, 81, 89, 108-111]. The proposed CMOS voltage reference-IV has higher FOM_1 FOM_2 and FOM_3 than the existing voltage references [66, 72-73, 81, 89, 108-111], which confirm its better performance. From Table 4.8, it can also be concluded that the proposed circuit has various advantages such as low supply voltage requirement, wide operating temperature range, low line sensitivity, high PSRR, less area, and low power consumption. The high PSRR and low line sensitivity also define the robustness of the proposed CMOS voltage reference-IV against the supply noise and supply voltage variations.

Table 4.8 Comparison of proposed CMOS voltage reference-IV with existing voltage references

References→ Parameters↓	[66]	[72]	[73]	[81]	[89]	[108]	[109]	[110]	[111]	Proposed voltage reference – IV
Technology (nm)	180	180	130	180	130	180	130	180	180	180
Supply voltage (V)	3 to 5	0.9 to 2.5	1 to 2.3	1.2 to 1.8	1.1 to 1.3	1.5	1.6 to 1.8	4.5 to 5.5	1.2 to 1.8	0.65 to 3.5
Temp. range (˚C)	-55 to 125	-20 to 120	0 to 100	0 to 100	-40 to 120	-10 to 130	0 to 150	-40 to 100	-40 to 100	-55 to 125
V_{REF} (mV)	2506	224	781	500	735	658	1112	2560	500	350
TC (ppm/℃)	25	191.3	48	22	9.3	9.6	13.1	2.6	15.19	31.5
PSRR (dB) @ 100 Hz	76	-----	-51.4	-42	-30	-42.3	-36	-63	-57	-85.4
Line sensitivity (%/V)	0.08	0.2	0.34	0.280	-----	0.89	0.24	0.2	0.25	0.015
Area (mm^2)	0.0596	0.0238	0.053	0.073	0.063	0.022	0.128	0.075	0.072	0.00289
Power consumption (µW)	45	3.78	8.1	6.12	1.44	449	288	30.6	6	1.95
FOM_1 ($°C^3/W.m^2$)	0.51	1.02	0.41	1.02	0.3	0.21	0.05	3.28	3	182
FOM_2 (dB.°C/ ppm.µA.mm^2)	3.56	-----	2.5	5.13	0.43	0.66	0.12	47.51	10.42	312
FOM_3 ($(°C/m)^2$. (dB/W.ppm. µA)$^{1/2}$.10^3)	2.54	-----	1.6	2.29	0.24	0.3	0.008	12.48	5.59	238.3

4.4 Simulation results of low dropout voltage regulators based on proposed CMOS voltage references

The low dropout voltage regulator (LDO) is used as an application of the voltage reference to validate the performance of proposed voltage references. This section presents the simulation results of LDOs based on proposed voltage references (I, II, III, and IV). The performances of the LDOs based on proposed voltage references (I, II, III, and IV) have also been compared with a conventional LDO that uses a conventional voltage reference to show the effectiveness of the LDOs based on proposed voltage references.

4.4.1 Simulation results of LDO using proposed CMOS voltage reference-I

The values of the supply voltage and reference voltage (V_{REF}) for both LDOs (LDO using proposed voltage reference-I and conventional LDO) are chosen as 0.85 V and 118.5 mV, respectively. Figure 4.25 shows the output voltages (V_{OUT}) versus temperature plots of LDOs using proposed CMOS voltage reference-I and conventional voltage reference. From the plots, the output voltages of LDOs using proposed CMOS voltage reference-I and conventional voltage reference are obtained as 589 mV at a nominal temperature of 27 ℃. Therefore, the dropout voltages of LDOs using proposed CMOS voltage reference-I and conventional voltage reference are obtained as 261 mV. In Figure 4.25, the green colour plot shows the deviation of V_{OUT} in the temperature range of -60 °C to 120 °C is 3.3 mV which gives the TC of 31.13 ppm/°C for LDO using proposed voltage reference-I. The red colour plot shows that the overall deviation of V_{OUT} in the temperature range of -60 °C to 120 °C is 16.5 mV which gives the TC of 155 ppm/°C for the LDO using conventional voltage reference.

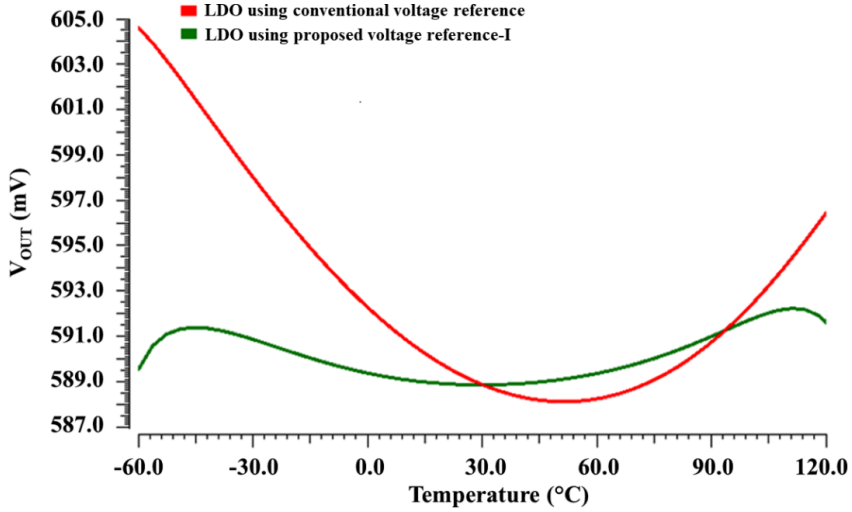


Figure 4.25 Output voltage (V_{OUT}) versus temperature plots of LDOs using proposed CMOS voltage reference-I and conventional voltage reference

The output voltage (V_{OUT}) versus supply voltage plots of LDOs using proposed CMOS voltage reference-I and conventional voltage reference are illustrated in Figures 4.26. From the figure, the variations of V_{OUT} for the supply voltage ranging from 0 V to 2.5 V give the line sensitivity of 0.275 %/V for LDOs using proposed voltage reference-I and conventional voltage reference. Figure 4.27 shows output voltage (V_{OUT}) versus load current plots of LDOs using proposed CMOS voltage reference-I and conventional voltage reference. The load current varies from 5 mA to 10 mA, which gives the load regulation of 0.23 mV/mA and 0.236 mV/mA for LDO using proposed voltage reference-I and LDO using conventional voltage reference, respectively.

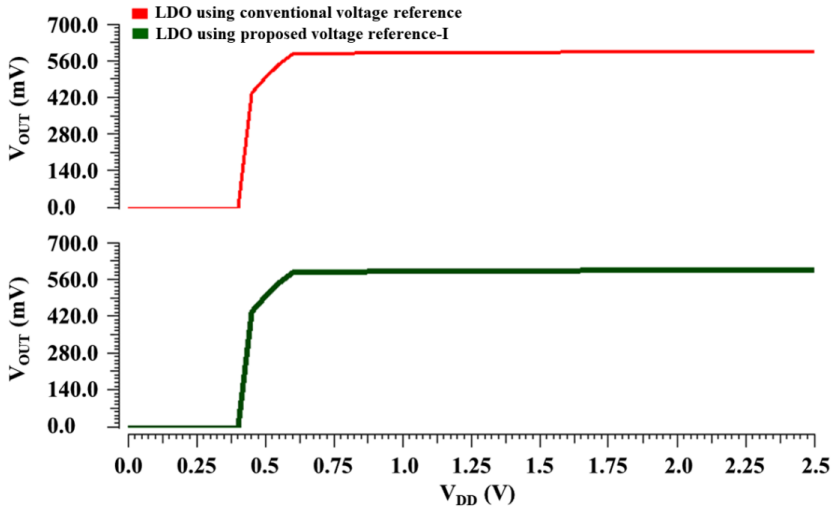


Figure 4.26 Output voltage (V_{OUT}) versus supply voltage plots of LDOs using proposed CMOS voltage reference-I and conventional voltage reference

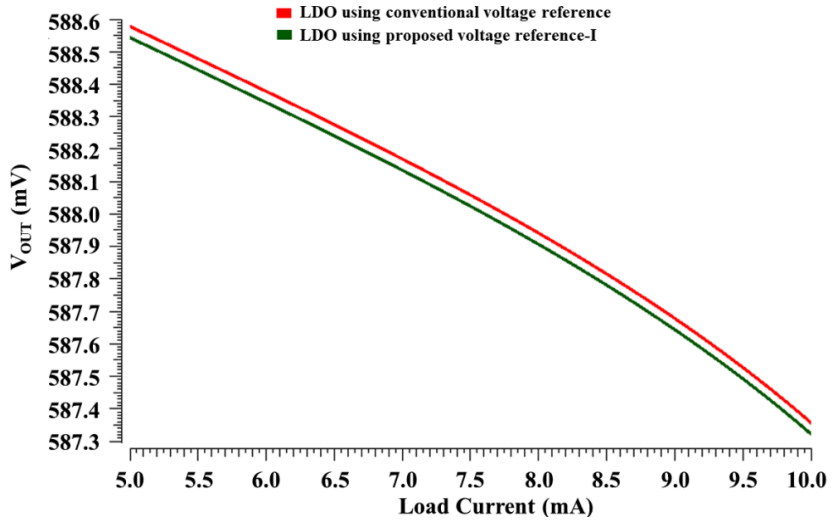


Figure 4.27 Output voltage (V_{OUT}) versus load current plots of LDOs using proposed CMOS voltage reference-I and conventional voltage reference

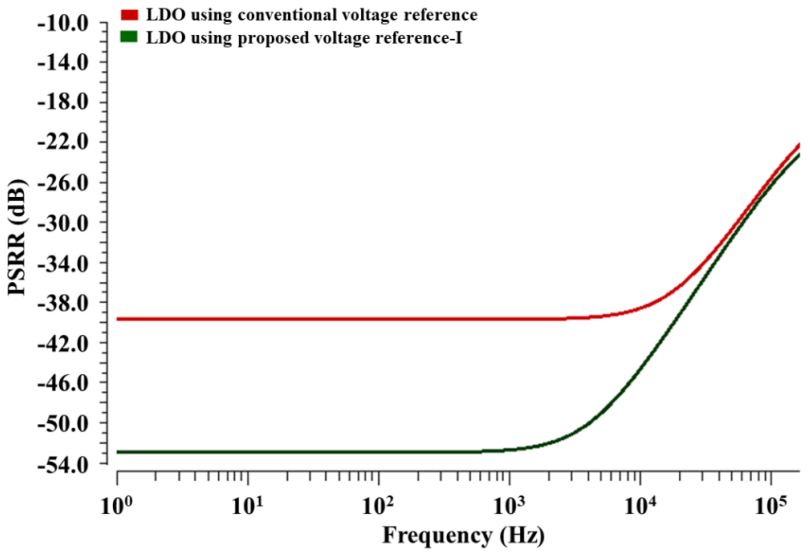


Figure 4.28 PSRR versus frequency plots of LDOs using proposed CMOS voltage reference-I and conventional voltage reference

Figure 4.28 illustrates the PSRR versus frequency plots of LDOs using proposed CMOS voltage reference-I and conventional voltage reference. From the plots, the values of PSRR are observed as -52.91 dB and -39 dB for LDO using proposed voltage reference-I and LDO using conventional voltage reference, respectively at the frequency of 100 Hz.

4.4.2 Simulation results of LDO using proposed CMOS voltage reference-II

The values of the supply voltage and reference voltage (V_{REF}) for both LDOs (LDO using proposed voltage reference-II and conventional LDO) are selected as 0.80 V and 424.85 mV, respectively. The output voltages (V_{OUT}) versus temperature plots of LDOs using proposed CMOS voltage reference-II and conventional voltage reference are shown in Figure 4.29.

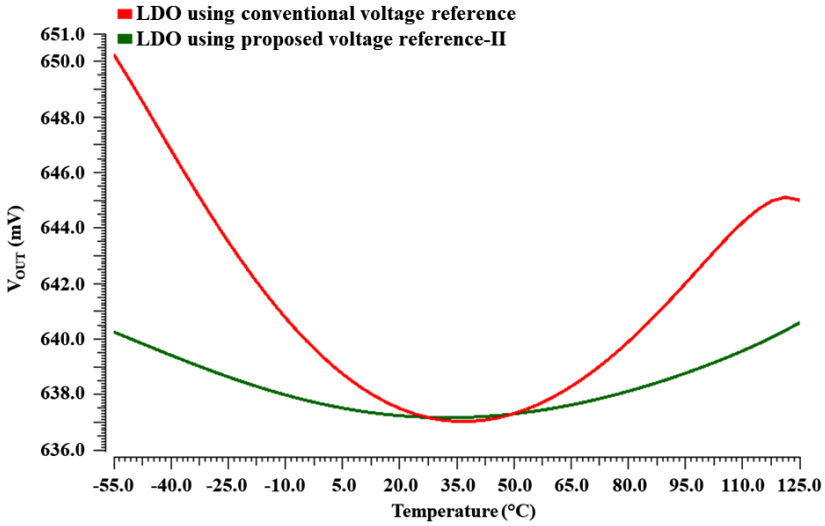


Figure 4.29 Output voltage (V_{OUT}) versus temperature plots of LDOs using proposed CMOS voltage reference-II and conventional voltage reference

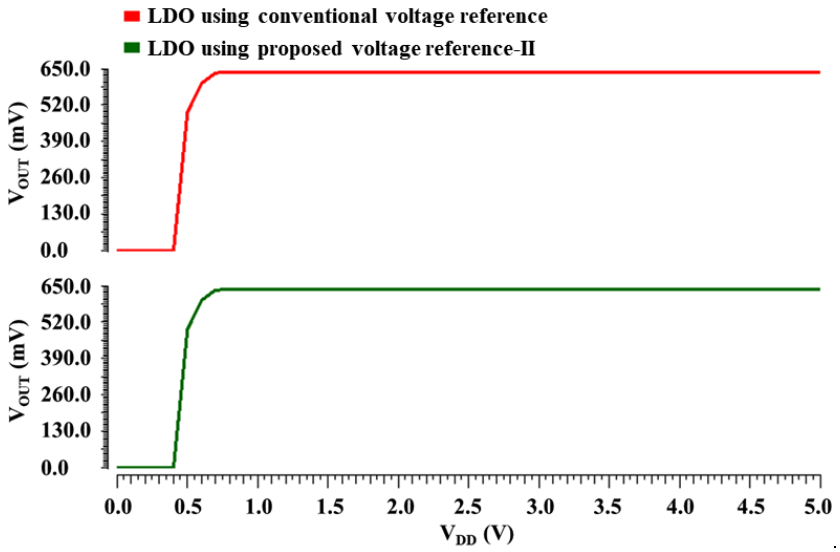


Figure 4.30 Output voltage (V_{OUT}) versus supply voltage plots of LDOs using proposed CMOS voltage reference-II and conventional voltage reference

From the plots, the output voltages of LDOs using proposed CMOS voltage reference-II and conventional voltage reference are obtained as 637 mV at a nominal temperature of 27 ℃. Therefore, the dropout voltages of LDOs using proposed CMOS voltage reference-II and conventional voltage reference are obtained as 163 mV. In Figure 4.29, the green colour plot shows the deviation of V_{OUT} in the temperature range of -55 ℃ to 125 ℃ is 4.41 mV which gives the TC of 39.75 ppm/°C for LDO using proposed voltage reference-II. The red colour plot shows that the overall deviation of V_{OUT} in the temperature range of -55 ℃ to 125 ℃ is 13.19 mV which gives the TC of 115 ppm/°C for the LDO using conventional voltage reference. The output voltage (V_{OUT}) versus supply voltage plots of LDOs using proposed CMOS voltage reference-II and conventional voltage reference are shown in Figures 4.30. From the figure, the variations of V_{OUT} for the supply voltage ranging from 0.8 V to 5 V give the line sensitivity of 0.0039 %/V for LDOs using proposed voltage reference-II and conventional voltage reference.

Figure 4.31 shows output voltage (V_{OUT}) versus load current plots of LDOs using proposed CMOS voltage reference-II and conventional voltage reference. The load current varies from 5 mA to 10 mA, which gives the load regulation of 0.009 mV/mA and 0.0092 mV/mA for LDO using proposed voltage reference-II and LDO using conventional voltage reference, respectively. Figure 4.32 shows the PSRR versus frequency plots of LDOs using proposed CMOS voltage reference-II and conventional voltage reference. From the plots, the values of PSRR are observed as -86.28 dB and -45 dB for LDO using proposed voltage reference-II and LDO using conventional voltage reference, respectively at the frequency of 100 Hz.

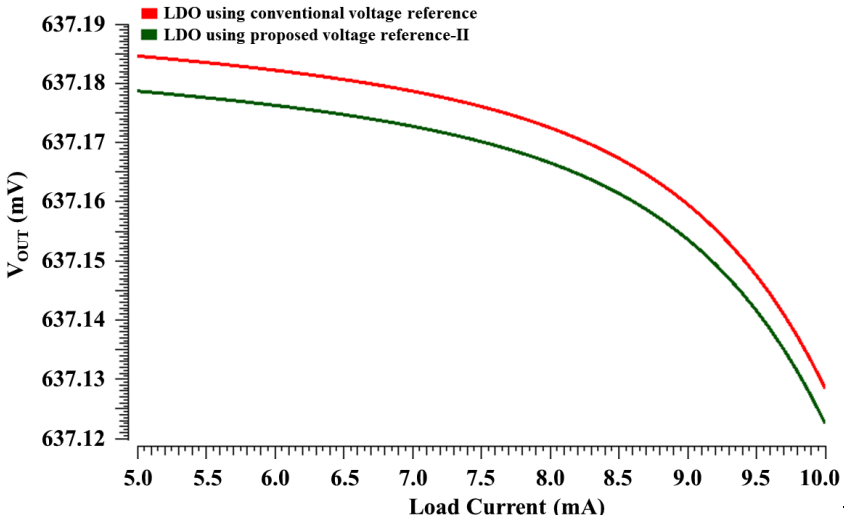


Figure 4.31 Output voltage (V_{OUT}) versus load current plots of LDOs using proposed CMOS voltage reference-II and conventional voltage reference

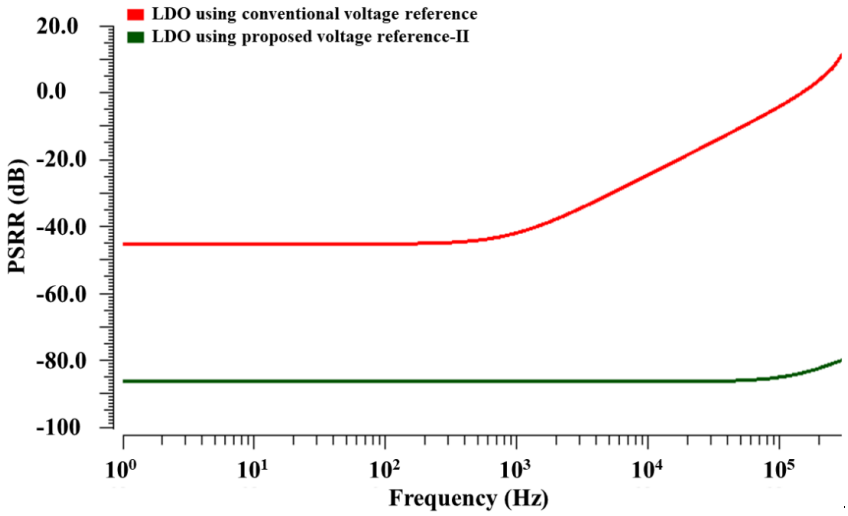


Figure 4.32 PSRR versus frequency plots of LDOs using proposed CMOS voltage reference-II and conventional voltage reference

4.4.3 Simulation results of LDO using proposed CMOS voltage reference-III

The values of the supply voltage and reference voltage (V_{REF}) for both LDOs (LDO using proposed voltage reference-III and conventional LDO) are chosen as 0.8 V and 312 mV, respectively. Figure 4.33 shows the output voltages (V_{OUT}) versus temperature plots of LDOs using proposed CMOS voltage reference-III and conventional voltage reference. From the plots, the output voltages of LDOs using proposed CMOS voltage reference-III and conventional voltage reference are obtained as 624 mV at a nominal temperature of 27 ℃. Therefore, the dropout voltages of LDOs using proposed CMOS voltage reference-III and conventional voltage reference are obtained as 176 mV. In Figure 4.33, the green colour plot shows the deviation of V_{OUT} in the temperature range of -40 °C to 125 °C is 4.23 mV which gives the TC of 41 ppm/°C

for LDO using proposed voltage reference-III. The red colour plot shows that the overall deviation of V_{OUT} in the temperature range of -40 °C to 125 °C is 9.7 mV which gives the TC of 94 ppm/°C for the LDO using conventional voltage reference. The output voltage (V_{OUT}) versus supply voltage plots of LDOs using proposed CMOS voltage reference-III and conventional voltage reference are illustrated in Figures 4.34. From the figure, the variations of V_{OUT} for the supply voltage varying from 0.8 V to 3 V give the line sensitivity of 0.005 %/V for LDOs using proposed voltage reference-III and conventional voltage reference.

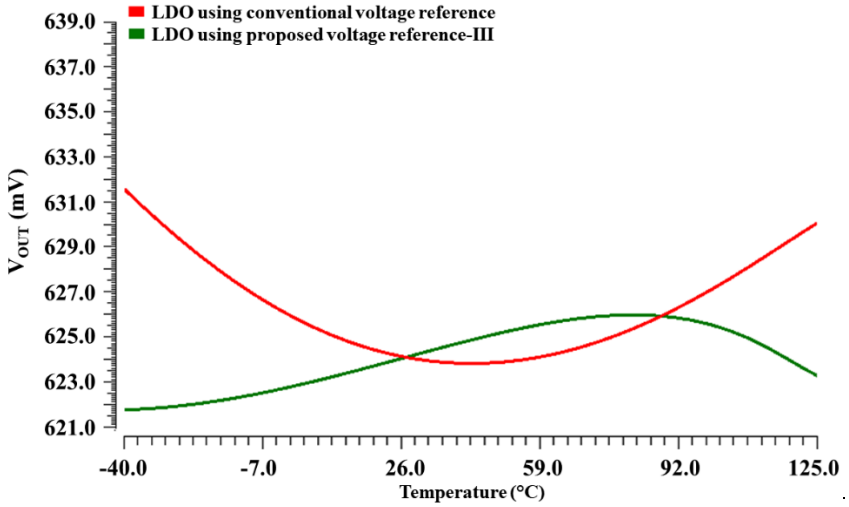


Figure 4.33 Output voltage (V_{OUT}) versus temperature plots of LDOs using proposed CMOS voltage reference-III and conventional voltage reference

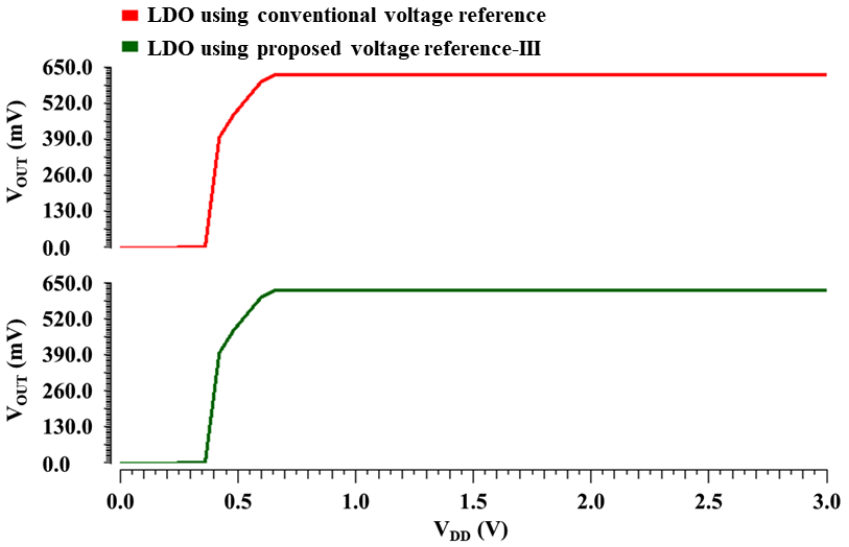


Figure 4.34 Output voltage (V_{OUT}) versus supply voltage plots of LDOs using proposed CMOS voltage reference-III and conventional voltage reference

Figure 4.35 shows output voltage (V_{OUT}) versus load current plots of LDOs using proposed CMOS voltage reference-III and conventional voltage reference. The load current varies from 5 mA to 10 mA, which gives the load regulation of 0.0116 mV/mA and 0.013 mV/mA for LDO using proposed voltage reference-III and LDO using conventional voltage reference, respectively. Figure 4.36 illustrates the PSRR versus frequency plots of LDOs using proposed CMOS voltage reference-III and conventional voltage reference. From the plots, the values of PSRR are observed as -82.2 dB and -51.28 dB for LDO using proposed voltage reference-III and LDO using conventional voltage reference, respectively at the frequency of 100 Hz.

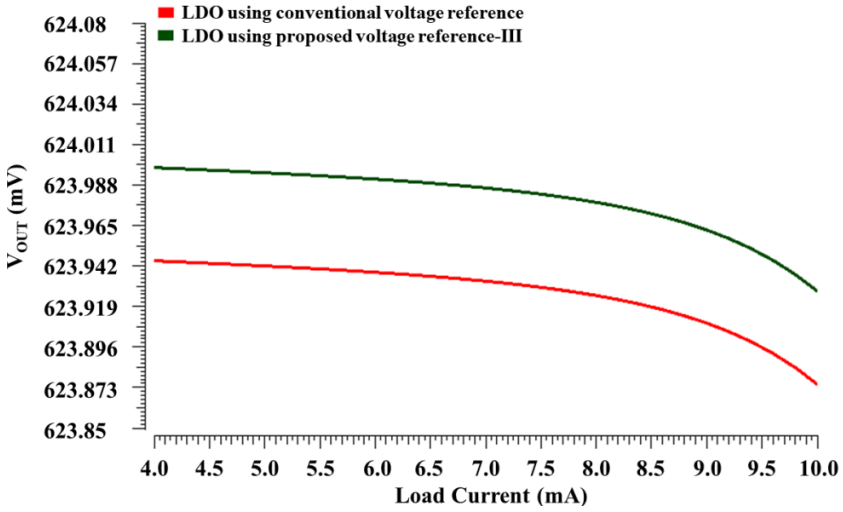


Figure 4.35 Output voltage (V_{OUT}) versus load current plots of LDOs using proposed CMOS voltage reference-III and conventional voltage reference

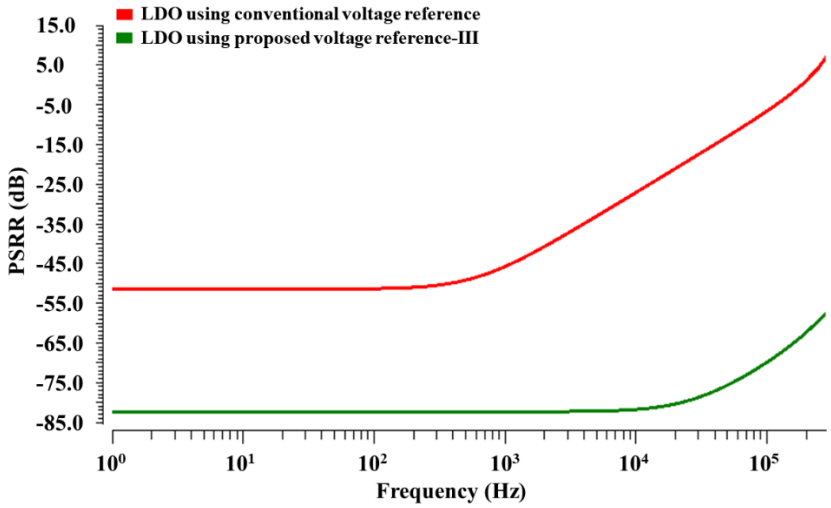


Figure 4.36 PSRR versus frequency plots of LDOs using proposed CMOS voltage reference-III and conventional voltage reference

4.4.4 Simulation results of LDO using proposed CMOS voltage reference-IV

The values of the supply voltage and reference voltage (V_{REF}) for both LDOs (LDO using proposed voltage reference-IV and conventional LDO) are selected as 0.65 V and 350 mV, respectively. The output voltages (V_{OUT}) versus temperature plots of LDOs using proposed CMOS voltage reference-IV and conventional voltage reference are illustrated in Figure 4.37. From the plots, the output voltages of LDOs using proposed CMOS voltage reference-IV and conventional voltage reference are obtained as 560 mV at a nominal temperature of 27 ℃. Therefore, the dropout voltages of LDOs using proposed CMOS voltage reference-IV and conventional voltage reference are obtained as 90 mV. In Figure 4.37, the green colour plot shows the deviation of V_{OUT} in the temperature range of -55 °C to 125 °C is 3.52 mV which gives the TC of 35 ppm/°C for LDO using proposed voltage reference-IV. The red colour plot shows that the overall deviation of V_{OUT} in the temperature range of -55 °C to 125 °C is 11.95 mV which gives the TC of 118.65 ppm/°C for the LDO using conventional voltage reference. The output voltage (V_{OUT}) versus supply voltage plots of LDOs using proposed CMOS voltage reference-IV and conventional voltage reference are shown in Figures 4.38. From the figure, the variations of V_{OUT} for the supply voltage ranging from 0.8 V to 3.5 V give the line sensitivity of 0.004 %/V for LDOs using proposed voltage reference-IV and conventional voltage reference. Figure 4.39 shows output voltage (V_{OUT}) versus load current plots of LDOs using proposed CMOS voltage reference-IV and conventional voltage reference.

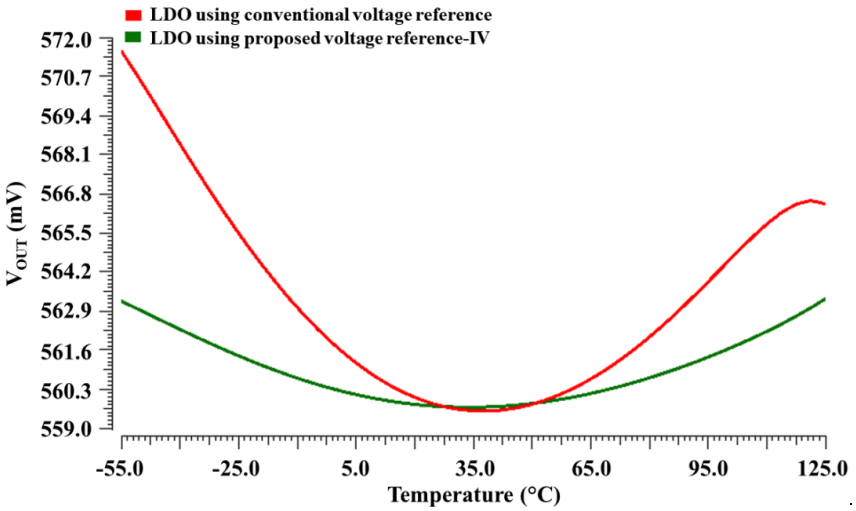


Figure 4.37 Output voltage (V_{OUT}) versus temperature plots of LDOs using proposed CMOS voltage reference-IV and conventional voltage reference

The load current varies from 5 mA to 10 mA, which gives the load regulation of 0.004 mV/mA and 0.0042 mV/mA for LDO using proposed voltage reference-IV and LDO using conventional voltage reference, respectively. Figure 4.40 shows the PSRR versus frequency plots of LDOs using proposed CMOS voltage reference-IV and conventional voltage reference. From the plots, the values of PSRR are observed as -79 dB and -48 dB for LDO using proposed voltage reference-IV and LDO using conventional voltage reference, respectively at the frequency of 100 Hz.

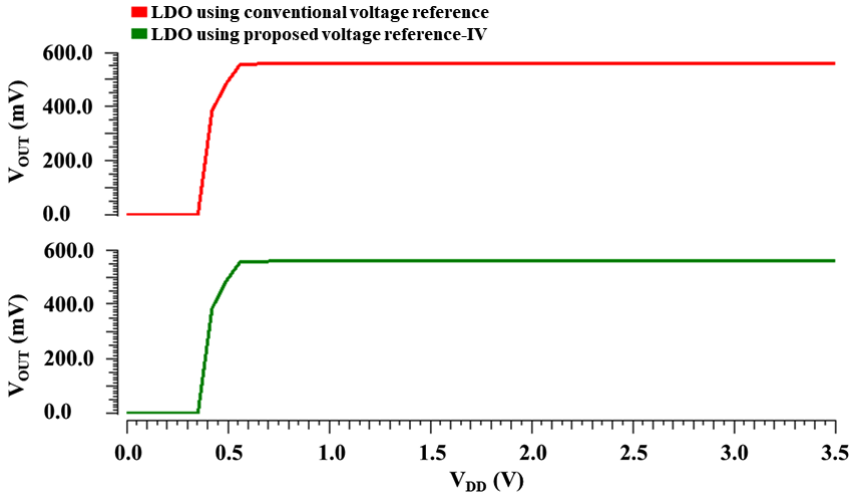


Figure 4.38 Output voltage (V_{OUT}) versus supply voltage plots of LDOs using proposed CMOS voltage reference-IV and conventional voltage reference

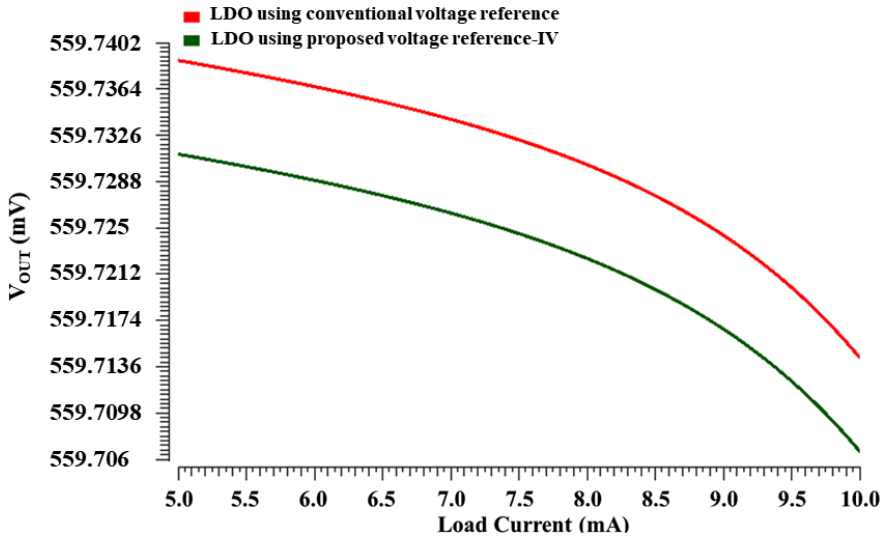


Figure 4.39 Output voltage (V_{OUT}) versus load current plots of LDOs using proposed CMOS voltage reference-IV and conventional voltage reference

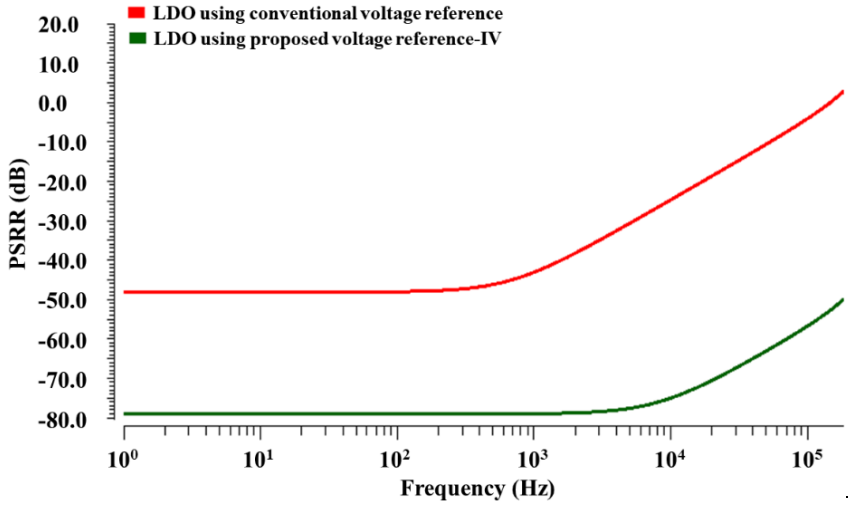


Figure 4.40 PSRR versus frequency plots of LDOs using proposed CMOS voltage reference-IV and conventional voltage reference

The performance parameters of the LDOs based on proposed voltage references (I, II, III, and IV) and conventional voltage reference are listed in Table 4.9. From the table, it can be seen that the LDOs based on proposed voltage references have several advantages such as higher PSRR, lower load regulation, lower temperature coefficient, and lower line sensitivity than the LDOs based on conventional voltage reference.

Table 4.9 Performance parameters of LDOs using proposed CMOS voltage references and conventional voltage reference

LDOs→ Parameters↓	**LDO using**		**LDO using**		**LDO using**		**LDO using**	
	conventional voltage reference	**proposed voltage reference-I**	**conventional voltage reference**	**proposed voltage reference-II**	**conventional voltage reference**	**proposed voltage reference-III**	**conventional voltage reference**	**proposed voltage reference-IV**
Technology (nm)	180	180	180	180	180	180	180	180
Supply voltage (V)	0.85	0.85	0.8	0.8	0.8	0.8	0.65	0.65
Drop-out voltage (mV)	261	261	163	163	176	176	90	90
Output voltage (mV)	589	589	637	637	624	624	560	560
Temp. range (°C)	-60 to 120	-60 to 120	-55 to 125	-55 to 125	-40 to 125	-40 to 125	-55 to 125	-55 to 125
Reference voltage (mV)	118.5	118.5	424.85	424.85	312	312	350	350
TC (ppm/°C)	155	31.13	115	39.75	94	41	118.65	35
Maximum load current (mA)	5 to 10	5 to 10	5 to 10	5 to 10	5 to 10	5 to 10	5 to 10	5 to 10
Line sensitivity (%/V)	0.275	0.275	0.0039	0.0039	0.005	0.005	0.004	0.004
Load regulation (mV/mA)	0.236	0.23	0.0092	0.009	0.013	0.0116	0.0042	0.004
PSRR @ 100 Hz (dB)	-39	-52.91	-45	-86.28	-51.28	-82.2	-48	-79

4.5 Conclusions

The post-layout simulation results of four different CMOS voltage references, namely CMOS voltage reference-I, CMOS voltage reference-II, CMOS voltage reference-III, and CMOS voltage reference-IV have been presented in this chapter. The proposed CMOS voltage reference-I offers low temperature sensitivity over a wide temperature range and low-line sensitivity but, the proposed circuit occupies a large area and requires high supply voltage. The proposed CMOS voltage reference-II overcomes the limitations of area and supply voltage requirement of CMOS voltage reference-I. The CMOS voltage reference-II also shows lower line sensitivity and higher PSRR than CMOS voltage reference-I but it consumes high power. The CMOS voltage reference-III consumes low power and occupies less area as compared to CMOS voltage reference-II. However, the CMOS voltage reference-III does not show much improvement in the line sensitivity and PSRR. The proposed CMOS voltage reference-IV shows lower line sensitivity and higher PSRR as compared to CMOS voltage reference-III. The CMOS voltage reference-IV requires low supply voltage and it consumes low power. The proposed voltage references have also been compared with the voltage references available in the literature and it has been observed that the proposed voltage references offer improved performance. The performances of proposed voltage references have been demonstrated using a conventional LDO. It has been observed that LDOs based on proposed voltage references offer better performance than LDOs based on conventional voltage reference.

CHAPTER 5
CONCLUSION AND FUTURE SCOPE

5.1 Conclusion

The voltage references are the essential components of analog and mixed-signal circuits which are extensively used in portable devices, computer systems, biomedical electronics, communication systems, etc. The voltage references provide constant output voltage with variations in process, supply voltage, temperature, etc. The thesis proposes four different CMOS voltage references, namely CMOS voltage reference-I, CMOS voltage reference-II, CMOS voltage reference-III, and CMOS voltage reference-IV. The proposed CMOS voltage reference-I uses a high-order curvature compensation technique to achieve low-temperature sensitivity over a wide temperature range. But, this technique increases the complexity, supply voltage requirement, and chip area. In CMOS voltage reference-II, a self-biased cascode branch generates the PTAT and CTAT voltages, which makes the circuit simple and area efficient. The high PSRR and low line sensitivity have also been achieved by using two operational amplifiers in the negative feedback loop. Since the proposed CMOS voltage references I and II use PTAT and CTAT behaviours to generate their output reference voltages, they require a large number of transistors, and hence power consumption and area of these circuits are not improved significantly.

To overcome the limitations of the proposed CMOS voltage references I and II, the CMOS voltage reference-III has been proposed which uses two CTAT behaviours to generate the output reference voltage. The CTAT behaviours have been generated using two similar supply-independent CTAT generators. It consumes low power and occupies less area as compared to CMOS voltage references I and II. However, the CMOS voltage reference-III does not show much improvement in the line sensitivity and PSRR. Therefore, to achieve low line sensitivity and high PSRR, another circuit of voltage reference named CMOS voltage reference-IV is proposed which uses two CTAT behaviours to generate the output reference voltage. But these CTAT behaviours are generated by a single beta multiplier circuit that makes the circuit simple and area efficient. The supply voltage requirement and power consumption of the proposed CMOS voltage reference-IV have also been improved.

The proposed CMOS voltage references, namely CMOS voltage reference-I, CMOS voltage reference-II, CMOS voltage reference-III, and CMOS voltage reference-IV have been employed in a conventional LDO to validate their performances. The performance parameters of the LDOs

based on proposed CMOS voltage references have also been compared with an LDO that uses a conventional voltage reference and it has been observed that LDOs based on proposed voltage references show better performance than the LDO that uses a conventional voltage reference in terms of PSRR, load regulation, temperature coefficient, and line sensitivity.

5.2 Future scope

In this work, four different voltage references with improved performance parameters have been presented, but there is still some scope to be carried forward in future research. In one of the proposed voltage references, the high-order curvature compensation technique has been used to improve the temperature coefficient. However, other techniques such as piecewise curvature compensation or logarithmic curvature compensation can also be used to further improve the temperature coefficient over a wide temperature range. The MOS transistor-based low pass filter can be used at the output of the proposed voltage references to reduce the output noise. Further, the mismatches in the current mirrors caused by the channel length modulation effect in the proposed voltage references can be mitigated by using channel length modulation effect compensation techniques. The programmable voltage references can also be investigated to optimize the values of the temperature coefficients digitally, which can increase the performance of the circuits.

List of Publications

SCI Journal Papers:

Published

1. A. Thakur, R. Pandey, and S. K. Rai, "Low temperature coefficient and low line sensitivity subthreshold curvature-compensated voltage reference," *International Journal of Circuit Theory and Applications*, vol. 48, no. 11, pp. 1900–1921, 2020. (SCI **Journal, Impact Factor: 2.378, Publisher: Wiley**)
2. A. Thakur, R. Pandey, and S. K. Rai, "A low supply voltage, low line sensitivity and high PSRR subthreshold CMOS voltage reference," *Journal of Circuits, Systems and Computers*, vol. 30, no. 12, pp. 2150227 (1-28), 2021. (SCI Journal**, Impact Factor: 1.278, Publisher: World Scientific)**
3. A. Thakur, R. Pandey, and S. K. Rai, "A sub-1-V CMOS voltage reference with high PSRR and high accuracy, " *Journal of Circuits, Systems and Computers*, vol. 31, no. 10, pp. 2250176 (1-34), 2022. (SCI Journal**, Impact Factor: 1.278, Publisher: World Scientific)**
4. A. Thakur, R. Pandey, and S. K. Rai, "High-performance sub-1 V CMOS voltage reference with low supply voltage," *AEU - International Journal of Electronics and Communications*, vol. 156, p. 154392, 2022. (SCI Journal**, Impact Factor: 3.169, Publisher: Elsevier)**

References

[1] Y. Jiang and E. K. F. Lee, "Design of low-voltage bandgap reference using transimpedance amplifier," *IEEE Transactions on Circuits and Systems—II: Analog and Digital Signal Processing*, vol. 47, no. 6, pp. 552–555, 2000.

[2] A. Garbaya, M. Kotti, M. Fakhfakh, and E. Tlelo-Cuautle, "Surrogate assisted optimization for low-voltage low-power circuit design," *Journal of Low Power Electronics and Applications*, vol. 10, no. 20, pp. 1–16, 2020.

[3] Z. Zhou, L. Feng, Y. Ma, Y. Shi, X. Ming, and B. Zhang, "A resistorless CMOS bandgap reference with low temperature coefficient and high PSRR," *International Journal of Electronics*, vol. 99, no. 10, pp. 1427–1438, 2012.

[4] B. Razavi, *Design of analog CMOS integrated circuits*. McGraw-Hill, 2017.

[5] V. B. Vulligaddala, R. Adusumalli, S. Singamala, and M. B. Srinivas, "A Digitally Calibrated Bandgap Reference with 0.06% Error for Low-Side Current Sensing Application," *IEEE Journal of Solid-State Circuits*, vol. 53, no. 10, pp. 2951–2957, 2018.

[6] T. Nonthaputha, M. Kumngern, and P. Moungnoul, "CMOS D/A converter using current conveyor analogue switches," in *2016 International Symposium on Intelligent Signal Processing and Communication Systems (ISPACS)*, 2016, pp. 1–4.

[7] F. Márquez *et al.*, "A novel autozeroing technique for flash analog-to-digital converters," *Integration*, vol. 47, no. 1, pp. 23–29, 2014.

[8] G. Raut, A. P. Shah, V. Sharma, G. Rajput, and S. K. Vishvakarma, "A 2.4-GS/s Power-Efficient, High-Resolution Reconfigurable Dynamic Comparator for ADC Architecture," *Circuits, Systems, and Signal Processing*, vol. 39, pp. 4681–4694, 2020.

[9] R. Pandey, N. Pandey, and R. Anurag, "Voltage Reference Circuits: A Classification," *International Journal of Engineering Science and Technology*, vol. 2, no. 9, pp. 4929–4935, 2010.

[10] A. Khatak, S. Dhull, and M. Kumar Taleja, "A Study on Advanced High Speed and Ultra Low Power ADC Architectures," *Indian Journal of Science and Technology*, vol. 10, no. 10, pp. 1–8, 2017.

[11] B. Aggarwal, Y. Arora, and J. K. Dhanoa, "Bandgap current reference using widlar current source," *Indian Journal of Engineering & Materials Sciences*, vol. 27, pp. 934-938, 2020.

[12] R. H. Murphy, "The Zener diode-an accurate voltage-reference source," *Electronics & Power*, vol. 12, no. 12, pp. 430–432, 1966.

[13] D. F. Hilbiber, “A new semiconductor voltage standard,” in *1964 IEEE International Solid-State Circuits Conference. Digest of Technical Papers*, 1964, pp. 32–33.

[14] R. J. Widlar, “New developments in IC voltage regulators,” *IEEE Journal of Solid-State Circuits*, vol. SC-6, no. 1, pp. 2–7, 1971.

[15] A. P. Brokaw, “A Simple Three-Terminal IC Bandgap Reference,” *IEEE Journal of Solid-State Circuits*, vol. 9, no. 6, pp. 388–393, 1974.

[16] H. Banba *et al.*, “A CMOS Bandgap Reference Circuit with Sub-1-V Operation,” *IEEE Journal of Solid-State Circuits*, vol. 34, no. 5, pp. 670–674, 1999.

[17] P. B. Basyurt, E. Bonizzoni, D. Yilmaz, and F. Maloberti, “Voltage reference architectures for low-supply-voltage low-power applications,” *Microelectronics Journal*, vol. 46, no. 11, pp. 1012–1019, 2015.

[18] J. P. Calvillo, R. Póvoa, J. Guilherme, and N. Horta, “Second-order compensation BGR with low TC and high performance for space applications,” *Integration*, vol. 63, pp. 256–265, 2018.

[19] G. Souliotis, F. Plessas, and S. Vlassis, “A high accuracy voltage reference generator,” *Microelectronics Journal*, vol. 75, no. February, pp. 61–67, 2018.

[20] C. R. Popa, *Superior-order curvature-correction techniques for voltage references*. Springer, 2009.

[21] J. da Chen and C. K. Ye, “Design of a CMOS bandgap reference circuit with a wide temperature range, high precision and low temperature coefficient,” *Journal of Circuits, Systems and Computers*, vol. 23, no. 8, pp. 1450107-(1-17), 2014.

[22] M. Pan, L. Pang, J. Xie, Y. Han, and Q. Xu, “A 0.6V 44.6 ppm/^{o}C subthreshold CMOS voltage reference with wide temperature range and inherent leakage compensation,” *Integration*, vol. 72, pp. 111–122, 2020.

[23] C. M. Andreou and J. Georgiou, “A 0.75-V, 4-μW, 15-ppm/°C, 190°C temperature range, voltage reference,” *International Journal of Circuit Theory and Applications*, vol. 44, no. 5, pp. 1029–1038, 2016.

[24] A. H. Adl, K. El-Sankary, and E. El-Masry, “A high-order curvature compensation technique for bandgap voltage reference using subthreshold MOSFETs,” *International Journal of Electronics*, vol. 97, no. 7, pp. 783–796, 2010.

[25] Z. K. Zhou *et al.*, “A CMOS Voltage Reference Based on Mutual Compensation of Vtn and Vtp,” *IEEE Transactions on Circuits and Systems II: Express Briefs*, vol. 59, no. 6, pp. 341–345, 2012.

[26] C.-Wah. Kok and W.-Shan. Tam, *CMOS voltage references : an analytical and practical perspective*, Wiley, 2013.

[27] K. E. Kuijk, "A Precision Reference Voltage Source," *IEEE Journal of Solid-State Circuits*, vol. 8, no. 3, pp. 222–226, 1973.

[28] G. C. M. Meijer, P. C. Schmale, and K. Van Zalinge, "A New Curvature-Corrected Bandgap Reference," *IEEE Journal of Solid-State Circuits*, vol. 17, no. 6, pp. 1139–1143, 1982.

[29] B. S. Song and P. R. Gray, "A Precision Curvature-Compensated CMOS Bandgap Reference," *IEEE Journal of Solid-State Circuits*, vol. 18, no. 6, pp. 634–643, 1983.

[30] A. van Staveren, J. van Velzen, C. J. M. Verhoeven, and A. H. M. van Roermund, "An integratable second-order compensated bandgap reference for 1V supply," *Analog Integrated Circuits and Signal Processing*, vol. 8, no. 1, pp. 69–81, 1995.

[31] A. E. Buck, C. L. McDonald, S. H. Lewis, and T. R. Viswanathan, "A CMOS Bandgap Reference Without Resistors," *IEEE Journal of Solid-State Circuits*, vol. 37, no. 1, pp. 81–83, 2002.

[32] K. N. Leung, P. K. T. Mok, and S. Member, "A CMOS Voltage Reference Based on Weighted ΔVGS for CMOS Low-Dropout Linear Regulators," *IEEE Journal of Solid-State Circuits*, vol. 38, no. 1, pp. 146–150, 2003.

[33] Y. Dai, D. T. Comer, D. J. Comer, and C. S. Petrie, "Threshold voltage based CMOS voltage reference," *IEE Proc.-Circuits Devices Syst*, vol. 151, no. 1, pp. 58–62, 2004.

[34] A. Lahiri and N. Agarwal, "Design of sub-1-V CMOS bandgap reference circuit using only one BJT," *Analog Integrated Circuits and Signal Processing*, vol. 71, no. 3, pp. 359–369, 2012.

[35] K. Ueno, T. Hirose, T. Asai, and Y. Amemiya, "A 300 nW, 15 ppm/°C, 20 ppm/V CMOS Voltage Reference Circuit Consisting of Subthreshold MOSFETs," *IEEE Journal of Solid-State Circuits*, vol. 44, no. 7, pp. 2047–2054, 2009.

[36] S. S. Chouhan and K. Halonen, "Design and implementation of a micro-power CMOS voltage reference circuit based on thermal compensation of Vgs," *Microelectronics Journal*, vol. 46, no. 1, pp. 36–42, 2015.

[37] B. Wang, M. K. Law, and A. Bermak, "A precision CMOS voltage reference exploiting silicon bandgap narrowing effect," *IEEE Transactions on Electron Devices*, vol. 62, no. 7, pp. 2128–2135, 2015.

[38] S. Yousefi and M. Jalali, “A high-PSRR low-power CMOS voltage reference based on weighted VGS difference,” *AEU - International Journal of Electronics and Communications*, vol. 70, no. 1, pp. 50–57, 2016.

[39] X. Li, L. Zhou, Y. Chen, Y. Zhang, C. Cao, and D. Guo, “A curvature-compensated CMOS bandgap with negative feedback technique,” *Microelectronics Journal*, vol. 52, pp. 104–110, 2016.

[40] H. Wu and H. Liu, “An Improved Bandgap Reference with Curvature-Compensated and High Power Supply Rejection,” *Journal of Circuits, Systems and Computers*, vol. 25, no. 11, pp. 1650147-(1-9), 2016.

[41] J. Wang, S. Member, Q. Li, L. Ding, and H. Shinohara, “A 3.5 ppm/°C 0.85 V Bandgap Reference Circuit without Resistors,” *IEICE Trans. Fundamentals*, vol. E99–A, no. 7, pp. 1430–1437, 2016.

[42] J. Jiang, W. Shu, and J. S. Chang, “A 5.6 ppm/°C Temperature Coefficient, 87-dB PSRR , Sub-1 V Voltage Reference in 65-nm CMOS Exploiting the Zero- Temperature-Coefficient Point,” *IEEE Journal of Solid-State Circuits*, vol. 52, no. 3, pp. 623–633, 2017.

[43] S. Huang, S. Diao, and F. Lin, “A 0.7-V, 8.9-μ A compact temperature-compensated CMOS subthreshold voltage reference with high reliability,” *Analog Integrated Circuits and Signal Processing*, vol. 91, no. 1, pp. 53–61, 2017.

[44] N. Alhasssan, Z. Zhou, and E. S. Sinencio, “An All-MOSFET Sub-1-V Voltage Reference with a - 51 -dB PSR up to 60 MHz,” *IEEE Transactions on Very Large Scale Integration (VLSI) Systems*, vol. 25, no. 3, pp. 919–928, 2017.

[45] Z. Luo *et al.*, “A sub-1V 78-nA bandgap reference with curvature compensation,” *Microelectronics Journal*, vol. 63, pp. 35–40, 2017.

[46] S. S. Chouhan and K. Halonen, “A 139 nW, 67 ppm/°C BJT-CMOS-Based Voltage Reference Circuit,” *Circuits, Systems, and Signal Processing*, vol. 36, no. 12, pp. 5062–5078, 2017.

[47] S. singh Chouhan and K. Halonen, “A 352nW, 30 ppm/°C all MOS nano ampere current reference circuit,” *Microelectronics Journal*, vol. 69, no. September, pp. 45–52, 2017.

[48] A. C. de Oliveira, D. Cordova, H. Klimach, and S. Bampi, “A 0.12-0.4 V, versatile 3-transistor CMOS voltage reference for ultra-low power systems,” *IEEE Transactions on Circuits and Systems I: Regular Papers*, vol. 65, no. 11, pp. 3790–3799, 2018.

[49] L. Liu, J. Mu, and Z. Zhu, “A 0.55-V, 28-ppm/°C, 83-nW CMOS Sub-BGR with UltraLow Power Curvature Compensation,” *IEEE Transactions on Circuits and Systems I: Regular Papers*, vol. 65, no. 1, pp. 95–106, 2018.

[50] Q. L. Li, W. Deng, and J. Huang, “A Novel Low Line Regulation Voltage Reference with No Amplifier,” *Journal of Circuits, Systems, and Computers*, vol. 27, no. 10, pp. 1850152-(1-12), 2018.

[51] Y. Liu, C. Zhan, and L. Wang, “An Ultralow Power CMOS Subthreshold Voltage Reference without Requiring Resistors or BJTs,” *IEEE Transactions on Very Large Scale Integration (VLSI) Systems*, vol. 26, no. 1, pp. 201–205, 2018.

[52] X. Ming, L. Hu, Y. L. Xin, X. Zhang, D. Gao, and B. Zhang, “A High-Precision Resistor-Less CMOS Compensated Bandgap Reference Based on Successive Voltage-Step Compensation,” *IEEE Transactions on Circuits and Systems I: Regular Papers*, vol. 65, no. 12, pp. 4086–4096, 2018.

[53] L. Wang, C. Zhan, J. Tang, Y. Liu, and G. Li, “A 0.9-V 33.7-ppm/°C 85-nW Sub-Bandgap Voltage Reference Consisting of Subthreshold MOSFETs and Single BJT,” *IEEE Transactions 0n Very Large Scale Integration (VLSI) Systems*, vol. 26, no. 10, pp. 2190–2194, 2018.

[54] R. Nagulapalli, K. Hayatleh, S. Barker, A. A. Tammam, P. Georgiou, and F. J. Lidgey, “A 0.55 V Bandgap Reference with a 59 ppm/°C Temperature Coefficient,” *Journal of Circuits, Systems and Computers*, vol. 28, no. 7, pp. 1950120-(1-12), 2019.

[55] L. Wang, C. Zhan, J. Tang, and G. Li, “An amplifier-offset-insensitive and high PSRR subthreshold CMOS voltage reference,” *International Journal of Circuit Theory and Applications*, vol. 46, no. 2, pp. 259–271, 2018.

[56] Y. Liang and Z. Zhu, “A 42 ppm/°C 0.7V 47nW Low-Complexity All-MOSFET Sub-Threshold Voltage Reference,” *Journal of Circuits, Systems, and Computers*, vol. 27, no. 7, pp. 1850105-(1-8), 2018.

[57] Z. Zhou *et al.*, “A Resistorless High-Precision Compensated CMOS Bandgap Voltage Reference,” *IEEE Transactions on Circuits and Systems I: Regular Papers*, vol. 66, no. 1, pp. 428–437, 2019.

[58] T. Ghanavati Nejad, E. Farshidi, H. Sjöland, and A. Kosarian, “A high precision logarithmic-curvature compensated all CMOS voltage reference,” *Analog Integrated Circuits and Signal Processing*, vol. 99, no. 2, pp. 383–392, 2019.

[59] T. M. Brito, D. M. Colombo, R. L. Moreno, and K. El-Sankary, “CMOS voltage reference using a self-cascode composite transistor and a schottky diode,” *Electronics*, vol. 8, no. 11, pp. 1–17, 2019.

[60] J. Lin, L. Wang, C. Zhan, and Y. Lu, “A 1-nW Ultra-Low Voltage Subthreshold CMOS Voltage Reference with 0.0154%/V Line Sensitivity,” *IEEE Transactions on Circuits and Systems II: Express Briefs*, vol. 66, no. 10, pp. 1653–1657, 2019.

[61] L. Liu, X. Liao, and J. Mu, “A 3.6 μVrms Noise, 3 ppm/◦C TC Bandgap Reference With Offset/Noise Suppression and Five-Piece Linear Compensation,” *IEEE Transactions on Circuits and Systems I: Regular Papers*, vol. 66, no. 10, pp. 3786–3796, 2019.

[62] J. Lei, Z. Wang, and X. Wang, “A 68-nW novel CMOS sub-bandgap voltage reference circuit,” *Microelectronics Journal*, vol. 89, pp. 37–40, 2019.

[63] R. B. A. Zawawi, W. H. Abbasi, S. H. Kim, H. Choi, and J. Kim, “Wide-supply-voltage-range cmos bandgap reference for in vivowireless power telemetry,” *Energies*, vol. 13, no. 11, pp. 1–14, 2020.

[64] S. R. Khan, “Sub-1 V, 5.5 ppm/°C, High PSRR all CMOS Bandgap Voltage Reference,” *IETE Journal of Research*, vol. 66, no. 4, pp. 527–532, 2020.

[65] P. K. Pal and R. K. Nagaria, “A low-power, Sub-1-V All-MOSFET subthreshold voltage reference using body biasing,” *Journal of Circuits, Systems and Computers*, vol. 28, no. 13, pp. 1950215-(1-22), Dec. 2019.

[66] Y. Shi, S. Li, J. Cao, Z. Zhou, and W. Ling, “A 180 nm Self-biased Bandgap Reference with High PSRR Enhancement,” *Nanoscale Research Letters*, vol. 15, no. 104, pp. 1–10, 2020.

[67] H. Aminzadeh and M. M. Valinezhad, “0.7-V supply, 21-nW All–MOS voltage reference using a MOS-Only current-driven reference core in digital CMOS,” *Microelectronics Journal*, vol. 102, p. 104841, 2020.

[68] J. Liang *et al.*, “A −80 dB PSRR 4.99 ppm/°C TC bandgap reference with nonlinear compensation,” *Microelectronics Journal*, vol. 95, p. 104664, 2020.

[69] J. Hu, K. Liang, J. Wang, and G. Li, “A 1.8-nW sub-1-V self-biased sub-bandgap reference for low-power systems,” *IEICE Electronics Express*, vol. 18, no. 11, pp. 1–6, 2021.

[70] M. Caselli, C. van Liempd, A. Boni, and S. Stanzione, “A low-power native NMOS-based bandgap reference operating from −55°C to 125°C with Li-Ion battery compatibility,”

International Journal of Circuit Theory and Applications, vol. 49, no. 5, pp. 1327–1346, 2021.

[71] G. Giustolisi, G. Palumbo, M. Criscione, and F. Cutrì, "A low-voltage low-power voltage reference based on subthreshold MOSFETs," *IEEE Journal of Solid-State Circuits*, vol. 38, no. 1, pp. 151–154, 2003.

[72] P. Huang, H. Lin, and Y. T. Lin, "A Simple Subthreshold CMOS Voltage Reference Circuit With Channel- Length Modulation Compensation," *IEEE Transactions on Circuits and Systems II: Express Briefs*, vol. 53, no. 9, pp. 882–885, 2006.

[73] H. Luo, Y. Han, R. C. C. Cheung, G. Liang, and D. Zhu, "Subthreshold CMOS voltage reference circuit with body bias compensation for process variation," *IET Circuits, Devices and Systems*, vol. 6, no. 3, pp. 198–203, 2012.

[74] A. Tsitouras, F. Plessas, M. Birbas, J. Kikidis, and G. Kalivas, "A sub-1V supply CMOS voltage reference generator," *International Journal of Circuit Theory and Applications*, vol. 40, no. 8, pp. 745–758, 2012.

[75] J. Wu, C. Chen, H. Shen, C. Huang, and H. Liu, "A high PSRR CMOS voltage reference with 1.2 V operation," *Analog Integrated Circuits and Signal Processing*, vol. 77, no. 1, pp. 79–86, 2013.

[76] Y. W. Zhang, J. Zhu, W. F. Sun, G. Sun, and S. L. Lu, "A novel sub-1V bandgap reference with offset compensated techniques," *Analog Integrated Circuits and Signal Processing*, vol. 78, no. 2, pp. 391–397, 2014.

[77] D. Osipov and S. Paul, "Temperature-Compensated β-Multiplier Current Reference Circuit," *IEEE Transactions on Circuits and Systems II: Express Briefs*, vol. 64, no. 10, pp. 1162–1166, 2017.

[78] A. Parisi, A. Finocchiaro, and G. Palmisano, "An accurate 1-V threshold voltage reference for ultra-low power applications," *Microelectronics Journal*, vol. 63, pp. 155–159, 2017.

[79] L. Wang *et al.*, "Analysis and design of a current-mode bandgap reference with high power supply ripple rejection," *Microelectronics Journal*, vol. 68, pp. 7–13, 2017.

[80] J. Duan, Z. Zhu, J. Deng, W. Xu, and B. Wei, "A Novel 0.8 V 79 nW CMOS-Only Voltage Reference With -55 dB PSRR @ 100 Hz," *IEEE Transactions on Circuits and Systems II: Express Briefs*, vol. 65, no. 7, pp. 849–853, 2018.

[81] F. Olivera and A. Petraglia, "Adjustable Output CMOS Voltage Reference Design," *IEEE Transactions on Circuits and Systems II: Express Briefs*, vol. 67, no. 10, pp. 1690–1694, 2020.

[82] G. C. Huang, H. G. Yang, T. Yin, X. D. Xu, and Y. M. Zhu, “A sub-1 V temperature-insensitive-PSR bandgap reference with complementary loop locking,” *Journal of Circuits, Systems and Computers*, vol. 28, no. 3, pp. 1950047-(1-14), 2019.

[83] K. Kondo, H. Tamura, and K. Tanno, “High-PSRR, low-voltage CMOS current mode reference circuit using self-regulator with adaptive biasing technique,” *IEICE Transactions on Fundamentals of Electronics, Communications and Computer Sciences*, vol. E103-A, no. 2, pp. 486–491, 2020.

[84] Y. Liu, Z. Li, P. Luo, and B. Zhang, “A 0.52 ppm/°C high-order temperature-compensated voltage reference,” *Analog Integrated Circuits and Signal Processing*, vol. 62, no. 1, pp. 17–21, 2010.

[85] X. Guan, X. Wang, A. Wang, and B. Zhao, “A 3 V 110 μw 3.1 ppm/°C curvature-compensated CMOS bandgap reference,” *Analog Integrated Circuits and Signal Processing*, vol. 62, no. 2, pp. 113–119, 2010.

[86] J. Li, X. Zhang, and M. Yu, “A 1.2-V Piecewise Curvature- Corrected Bandgap Reference in 0.5 μm CMOS Process,” *IEEE Transactions 0n Very Large Scale Integration (VlSI) Systems*, vol. 19, no. 6, pp. 1118–1122, 2011.

[87] D. F. Bowers and E. J. Modica, “Curvature-corrected low-noise sub-bandgap reference in 28 nm CMOS technology,” *Electronics Letters*, vol. 50, no. 5, pp. 396–398, 2014.

[88] B. Ma and F. Yu, “A novel 1.2-V 4.5-ppm/°C curvature-compensated CMOS bandgap reference,” *IEEE Transactions on Circuits and Systems I: Regular Papers*, vol. 61, no. 4, pp. 1026–1035, 2014.

[89] Q. Duan and J. Roh, “A 1.2-V 4.2-ppm/°C High-Order Curvature- Compensated CMOS Bandgap Reference,” *IEEE Transactions on Circuits and Systems—I: Regular Papers*, vol. 62, no. 3, pp. 662–670, 2015.

[90] J. Lv, L. Wei, and S. S. Ang, “A new curvature-compensated, high-PSRR CMOS bandgap reference,” *Analog Integrated Circuits and Signal Processing*, vol. 82, no. 3, pp. 675–682, 2015.

[91] P. B. Basyurt and D. Y. Aksin, “A compact curvature corrected bandgap reference in 0.35 μm CMOS process,” *Analog Integrated Circuits and Signal Processing*, vol. 83, no. 1, pp. 65–73, 2015.

[92] C. M. Andreou and J. Georgiou, “A 0.7 V, 2.7 μW, 12.9 ppm/° C over 180° C CMOS subthreshold voltage reference,” *International Journal of Circuit Theory and Applications*, vol. 45, no. 10, pp. 1349–1368, 2017.

[93] H. M. Chen, C. C. Lee, S. H. Jheng, W. C. Chen, and B. Y. Lee, “A Sub-1 ppm/°C Precision Bandgap Reference with Adjusted-Temperature-Curvature Compensation,” *IEEE Transactions on Circuits and Systems I: Regular Papers*, vol. 64, no. 6, pp. 1308–1317, 2017.

[94] R. Wang *et al.*, “A Sub-1 ppm /°C Current-Mode CMOS Bandgap Reference With Piecewise Curvature Compensation,” *IEEE Transactions on Circuits and Systems–I: Regular Papers*, vol. 65, no. 3, pp. 904–913, 2018.

[95] L. Liu, W. Huang, J. Mu, Z. Zhu, and Y. Yang, “A 1.2 V, 3.0 ppm/°C, 3.6 μA CMOS bandgap reference with novel 3-order curvature compensation,” *Microelectronics Journal*, vol. 72, pp. 49–57, 2018.

[96] G. Pan, Q. Hua, and B. Zhang, “A 1.8 V 0.918 ppm/°C CMOS bandgap voltage reference with curvature-compensated,” *IEICE Electronics Express*, vol. 16, no. 23, pp. 1–5, 2019.

[97] X. Liu, S. Yang, J. Wang, and Z. Xu, “A high-order curvature compensated voltage reference based on lateral BJT,” *AEU - International Journal of Electronics and Communications*, vol. 124, p. 153325, 2020.

[98] T. Yan, C. W. U, M. K. Law, and C. S. Lam, “A −40 °C–125 °C, 1.08 ppm/°C, 918 nW bandgap voltage reference with segmented curvature compensation,” *Microelectronics Journal*, vol. 105, p. 104897, 2020.

[99] Y. Zhang, J. Li, X. Wang, Z. Luo, and Y. Zhou, “A 1.2-V 2.18-ppm/°C curvature-compensated CMOS bandgap reference,” *IEICE Electronics Express*, vol. 18, no. 11, pp. 1–6, 2021.

[100] N. Lyu, N. Yu, and M. Yi, “An improved voltage bandgap reference with high-order curvature compensation,” in *2015 IEEE 11th International Conference on ASIC (ASICON)*, 2015, pp. 1–4.

[101] D. Ha, Y. Park, and S. Kim, “A current-mirror technique used for high-order curvature compensated bandgap reference in automotive application,” in *2016 IEEE 59th International Midwest Symposium on Circuits and Systems (MWSCAS)*, 2016, pp. 1–4.

[102] C. J. B. Fayomi, G. I. Wirth, H. F. Achigui, and A. Matsuzawa, “Sub 1V CMOS bandgap reference design techniques: A survey,” *Analog Integrated Circuits and Signal Processing*, vol. 62, no. 2, pp. 141–157, 2010.

[103] S. Saponara, L. Fanucci, T. Baldetti, and E. Pardi, “Bandgap voltage reference IC for HV automotive applications with pseudo-regulated bias and service regulator,” *Journal of Circuits, Systems and Computers*, vol. 22, no. 1, pp. 1250069-(1-17), 2013.

[104] S. Y. Lee, Z. X. Liao, and C. H. Lee, “Energy-harvesting circuits with a high-efficiency rectifier and a low temperature coefficient bandgap voltage reference,” *IEEE Transactions on Very Large-Scale Integration (VLSI) Systems*, vol. 27, no. 8, pp. 1760–1767, 2019.

[105] J. Geng, Y. Zhao, and H. Zhao, “A high-order curvature-corrected CMOS bandgap voltage reference with constant current technique,” *International Journal of Circuit Theory and Applications*, vol. 42, no. 1, pp. 43–52, Jan. 2014.

[106] S. K. Koh and L. Lee, “Low power CMOS Bandgap Reference circuit,” in *2014 IEEE Student Conference on Research and Development*, 2014, pp. 1–5.

[107] R. Nagulapalli, K. Hayatleh, S. Barker, S. Zourob, N. Yassine, and S. Sridevi, “A Microwatt Low Voltage Bandgap Reference for Bio-medical Applications,” in *2017 International Conference on Recent Advances in Electronics and Communication Technology (ICRAECT)*, 2017, pp. 61–65.

[108] W. S. Tam, O. Y. Wong, C. W. Kok, and H. Wong, “Generating sub-1V reference voltages from a resistorless CMOS bandgap reference circuit by using a piecewise curvature temperature compensation technique,” *Microelectronics Reliability*, vol. 50, no. 8, pp. 1054–1061, 2010.

[109] Y. Huang, L. Zhu, F. Kong, C. Cheung, and L. Najafizadeh, “BiCMOS-Based Compensation: Toward Fully Curvature-Corrected Bandgap Reference Circuits,” *IEEE Transactions on Circuits and Systems I: Regular Papers*, vol. 65, no. 4, pp. 1210–1223, 2018.

[110] Q. Liu, B. Zhang, S. Zhen, W. Xue, and M. Qiao, “A 2.6 ppm/◦C 2.5 V Piece-Wise Compensated Bandgap Reference with Low Beta Bipolar,” *Electronics*, vol. 8, no. 555, pp. 1–13, 2019.

[111] F. Olivera and A. Petraglia, “A Computer-Aided Approach for Voltage Reference Circuit Design,” *Analog Integrated Circuits and Signal Processing*, vol. 89, pp. 511–520, 2016.

[112] C.-J. Liang, C.-C. Chung, and H. Lin, “A low-voltage band-gap reference circuit with second-order analyses,” *International Journal of Circuit Theory and Applications*, vol. 39, no. 12, pp. 1247–1256, 2011.

[113] Z. Zhou, L. Feng, Y. Ma, Y. Shi, X. Ming, and B. Zhang, “A resistorless CMOS bandgap reference with low temperature coefficient and high PSRR,” *International Journal of Electronics*, vol. 99, no. 10, pp. 1427–1438, Oct. 2012.

[114] I. Lee, D. Sylvester, and D. Blaauw, “A subthreshold voltage reference with scalable output voltage for low-power IoT systems,” *IEEE Journal of Solid-State Circuits*, vol. 52, no. 5, pp. 1443–1449, 2017.

[115] S. Liu and R. J. Baker, “Process and temperature performance of a CMOS beta-multiplier voltage reference,” in *Midwest Symposium on Circuits and Systems*, 1998, pp. 33–36.

[116] G. Alfonso Rincon-Mora, *Voltage references from diodes to precision high-order bandgap circuits*. Wiley-IEEE Press, 2002.

[117] M. J. M. Pelgrom, A. C. J. Duinmaijer, and A. P. G. Welbers, “Matching Properties of MOS Transistors,” *IEEE Journal of Solid-State Circuits*, vol. 24, no. 5, pp. 1433–1439, 1989.

[118] J. María, H. Clara, L. Martínez, and A. Torralba, “Internally Compensated LDO Regulators for Modern System-on-Chip Design,” SPRINGER, 2019.

[119] A. C. de Oliveira, D. Cordova, H. Klimach, and S. Bampi, “Picowatt, 0.45-0.6 V Self-Biased Subthreshold CMOS Voltage Reference,” *IEEE Transactions on Circuits and Systems I: Regular Papers*, vol. 64, no. 12, pp. 3036–3046, 2017.