SYNTHESIS OF ANALOG IC BUILDING BLOCKS

A Thesis

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Doctor of Philosophy

By

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Certificate

Certified that the thesis entitled **"Synthesis of Analog IC Building Blocks"** being submitted by **Ms. Alpana Kansal, Registration No. 9010451** to the **Department of Electronics and Communication Engineering, Thapar University, Patiala, India** in fulfillment of the requirements for the award of degree of **"Doctor of Philosophy"** is a record of bonafide research work carried out by her under my guidance and supervision during the period 2002-2009. She has fulfilled the requirements for the submission of this thesis, which has reached the requisite standard. The matter presented in this thesis does not incorporate any material previously published or written by any other person except where due reference is made in the text.

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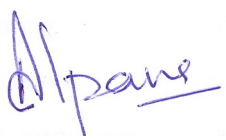

(Alpana Kansal)

Abstract

A new methodology based on the concept of figure of merit that includes the three performance parameters, namely input-referred noise, differential dc voltage gain and unity-gain bandwidth, has been proposed for synthesizing optimal performance differential input-stage amplifiers and second stage amplifier under the constraints of area. This concept has been validated with examples both at low and medium frequencies. The four different figures of merit proposed for different structures and in different frequency domains peak at certain values of relative area allocation to the input transistors in the range of 62 % to 92 % of the available area. The peak achievable value of the figure of merit is a function of both area and power. However, at low frequencies, it is independent of biasing current (and hence power) subject to a minimum current (and hence a minimum power) required to keep all the transistors biased in the saturation region. It is observed that the differential dc voltage gain, unity-gain bandwidth and input-referred noise achieved at peak figure of merit are very close to their best individually achievable values. The study also highlights that the total band noise for a given area is practically independent of relative allocation of areas between the input and load transistors and also does not vary significantly with the total area assigned to the circuit at medium frequencies.

Incorporating the above ideas, a CAD tool has been developed in C/C++, for the synthesis of differential amplifiers. The tool has been tested for 2400 design-syntheses with dc power varying from 100 μW to 1000 μW, differential dc voltage gain in the range of 10 – 1000 V/V, unity-gain bandwidth in the range of 1 – 100 MHz, and input-referred noise in the range of 1 – 20 nV/rtHz. The synthesized circuits are mainly governed by power and noise. At a constant power, area required increases exponentially with the requirement of reduced input-referred noise. Area requirement can also be reduced at the cost of increased power consumption and

reduced differential dc voltage gain for the same input-referred noise. Hence, a clear Area – Power tradeoff is seen in the synthesized designs. The layouts of some of the synthesized circuits were drawn manually in 1.25 µm CMOS technology and were simulated and compared against the simulated results on schematics for final validation of the synthesis tool.

The limits and limiting relationships on differential dc voltage gain, Ad and Unity-Gain Bandwidth, UGB of an unloaded differential amplifier were explored. It has been observed that the product $Ad \cdot UGB$ of an unloaded differential amplifier is a technology constant.

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List of Acronyms, Abbreviations and Symbols

Symbol	Quantity	Units
Δf	Frequency band	Hz
μ	Charge carrier mobility	cm^2/V_S
μ_n	Electron mobility	cm^2/V_S
μ_p	Hole mobility	cm^2/V_S
A	Area	μm^2
Ad	Differential dc voltage gain	dB or V/V
ADC	Analog-to-Digital Converter	
CAD	Computer-Aided Design	
CCCS	Current Controlled Current Source	
C_{gs}	Gate to source capacitance	f
C_L	Load capacitor	f
CMOS	Complementary MOS	
CMRR	Common-Mode Rejection Ratio	dB
C_{OX}	Gate oxide capacitance per unit area	f/m^2
DAC	Digital-to-Analog Converter	
DM	Differential Mode signal	
DSP	Digital Signal Processing	
f	Frequency	Hz
FoM	Figure of Merit	
GBW	Gain Bandwidth product	Hz
g_d	Drain conductance	Ω^{-1}
g_{d0}	Drain conductance g_d at $V_d = 0$	Ω^{-1}
g_{di}	Drain conductance of input transistor	Ω^{-1}
g_{dl}	Drain conductance of load transistor	Ω^{-1}
g_m	Trans-conductance	Ω^{-1}

$g_{m,n}$	Trans-conductance of n-transistor	Ω^{-1}
$g_{m,p}$	Trans-conductance of p-transistor	Ω^{-1}
$g_{m,i}$	Trans-conductance of i^{th} transistor	Ω^{-1}
g_{mb}	Back-gate trans-conductance	Ω^{-1}
GND	Ground	
GP	Geometric Programming	
IC	Integrated Circuit	
ICMR	Input Common Mode Range	dB
I_d	Drain to source current	A
I_o	Bias tail current	A
IR	Infra-Red	
IRN	Input Refereed Noise	$V/\sqrt{Hz}$
$IRN(th)$	Input-referred thermal noise spectral density	$V/\sqrt{Hz}$
i_{nT}	Noise current source	A
k	Boltzmann's constant	J/K
k_n	NMOS process trans-conductance parameter	A/V^2
k_p	PMOS process trans-conductance parameter	A/V^2
K_F	Flicker noise coefficient	$V^2.F$
K_{Fn}	Flicker noise coefficient of nMOS transistor	$V^2.F$
K_{Fp}	Flicker noise coefficient of pMOS transistor	$V^2.F$
L	Channel length	µm
L_{eff}	Effective channel length	µm
L_i	Channel length of input transistor	µm
L_l	Channel length of load transistor	µm
L_p	Channel length of pMOS transistor	µm
L_n	Channel length of nMOS transistor	µm
LNA	Low Noise Amplifiers	
LVS	Layout Vs. Schematic	
MOS	Metal Oxide Semiconductor	
nMOS	n-channel MOS	

OCA	Operational Current Amplifier	
Op-Amp	Operational Amplifier	
OTA	Operational Trans-conductance Amplifier	
P_{noise}	Output noise power	V^2
$P_{peak\text{-}signal}$	Peak to peak signal power	V^2/Hz
PLL	Phase-Locked Loop	
pMOS	p-channel MOS	
PSD	Power Spectral Density	
PSRR	Power Supply Rejection Ratio	dB
q	Electronic charge	C
R	Resistance	Ω
RF	Radio Frequency	Hz
S_i	Noise Current Spectral Density	A^2/Hz
S_V	Noise Voltage Spectral Density	V^2/Hz
S_{VG}	Noise Voltage Spectral Density at the Gate	V^2/Hz
SA	Simulated Annealing	
SNR	Signal-to-Noise Ratio	dB
SPICE	Simulation Program with Integrated Circuit Emphasis	
T	Temperature	°C
UGB	Unity Gain Bandwidth	Hz
V_{BE}	Base to emitter voltage	V
V_{CM}	Common-mode input voltage	V
V_d	Drain voltage	V
V_{DG}	Drain to gate voltage	V
V_{dsat}	V_d value at the border of the linear and saturation regions	V
V_{DD}	Positive supply	V
V_{DS}	Drain to source voltage	V
V_{eq}	Equivalent voltage	V
V_{GS}	Gate to source voltage	V
v_{nT}	Noise voltage source	V

V_{on}	Output noise voltage	V
Vsb	Source-bulk voltage	V
V_{SS}	Negative supply	V
V_T	Thermal voltage	V
V_{tn}	Threshold voltage of nMOS transistor	V
V_{tn0}	Zero bias threshold voltage of nMOS transistor	V
V_{tp}	Threshold voltage of pMOS transistor	V
V_{tp0}	Zero bias threshold voltage of pMOS transistor	V
VCO	Voltage Controlled Oscillators	
VLSI	Very Large Scale Integration	
W	Channel width	µm
W_{eff}	Effective channel width	µm
W_i	Channel width of input transistor	µm
W_l	Channel width of load transistor	µm
W_n	Channel width of nMOS transistor	µm
W_p	Channel width of pMOS transistor	µm
x	Fraction	
x_d	Depletion width	

Chapter 1

Introduction

1.1 Introduction

Growth in the integrated circuit industry is now expanding beyond the traditional emphasis on digital computation. With increasing interest in employing integrated circuits in a growing number of "real world" applications, analog circuits are becoming a key part of just about every design.

While many types of signal processing have indeed moved to the digital domain; analog circuits have proved fundamentally necessary in many of today's complex, high performance systems. There exist numerous applications where it is very difficult or even impossible to replace analog functions with their digital counterparts regardless of advances in technology, for example, design of analog-to-digital converters (ADCs) and digital-to-analog converters (DACs) for high speed, high precision, and low power; design of high-performance analog amplifiers and filters to boost and suppress the out-of-band components; optical receivers to process a low-level signal at a very high-speed requiring low-noise, broadband circuit design; electrical and optical sensors which employ amplifiers, filters and converters (ADC and DAC); high-speed sense amplifiers for semiconductor memories; *etc*. Furthermore, many issues related to the distribution and timing of high-speed signals, non-idealities in signal and power interconnects, package parasitics, *etc*. of even digital chips require a solid understanding of analog design. These examples clearly demonstrate the wide and inevitable spread of analog circuits in modern industry.

But, the difficulty level of analog design is much higher than that of the digital design for the following reasons:

- With the speed and precision required in processing analog signals, analog signals are much more sensitive to noise, crosstalk, and other interferers than are digital signals.
- Second-order effects in devices influence the performance of analog circuits much more heavily than that of digital circuits.
- Despite tremendous progress, modeling and simulation of many effects in analog circuits continue to pose difficulties, forcing the designers to draw upon experience and intuition when analyzing the results of a simulation.
- An important thrust in today's semiconductor industry is to design analog circuits in mainstream IC technologies which are developed and characterized to fabricate digital products and do not easily lend themselves to analog design, requiring novel circuits and architectures to achieve high performance.
- The design of high-performance analog circuits can rarely be automated, usually requiring that every device be "hand-crafted". By contrast, many digital circuits are automatically synthesized and laid out.

In recent years, complete systems that earlier occupied one or more boards are increasingly being integrated on a few chips or even one single chip. Although most functions in such integrated systems are implemented with digital or digital signal processing (DSP) circuitry, the analog circuits needed at the interface between the electronic system and the real world, are also being integrated on the same die for reasons of cost and performance. The analog sections of such mixed-signal IC designs are generally small; however, demands for low power and increased system integration increase analog design complexity. At the same time, many present ASIC application markets are characterized by shortening product life cycles and time-to-market constraints. These constraints can only be met by using advanced Computer-Aided Design (CAD) tools. In the digital world, logic

synthesis and semi-custom layout have emerged as the de facto strategies for managing the front-end (specifications to gate-level netlist steps) and the back-end (netlist to mask steps) of the design process. Unfortunately, we do not yet have robust circuit synthesis and layout tools in the analog domain. The design cycle for analog and mixed-signal ICs remain long and error-prone [Gray87].

In order to reduce analog IC design time, and thereby the time-to-market for most products, the development of analog IC design synthesis tools has been going on since the early 1970's [Nagel71, Nagle75, Kuhn87, DeGrauwe87, Nye88, Harjani89, Koh90, Rutenbar93, Carley96] and continues to occupy the attention of contemporary researchers [Aldana99, Ray02, Gielen05, Lee06, Unno06, Unno07]. The present thesis work also addresses the subject of analog circuit synthesis.

1.2 Thesis Organization

Chapter 2 introduces the available CAD tools and methodologies (available in the literature) and discusses the background and motivation that led to the present work.

Chapter 3 describes the concept of figure of merit based on small signal parameters, for the design of differential input stage amplifier for low frequency applications under the constraints of area. It outlines the analytical expressions developed for the figure of merit and its maximization under the constraints of area. It then compares the analytical results obtained with the SPICE simulated results.

In chapter 4 the proposed approach of figure of merit based design-synthesis of differential input stage amplifier has been applied at mid/moderate frequencies, where thermal noise dominates the flicker noise. Again the analytical results have been compared with SPICE simulation results.

Chapter 5 discusses the figure of merit based design of second stage of the operational amplifier, where noise does not play a dominant role.

Chapter 6 describes the CAD tool developed for the optimal synthesis of differential input stage amplifier under the constraints of maximum power and input-referred noise, and minimum differential dc gain and unity-gain bandwidth. The chapter includes the results of 2400 designs, which were synthesized using the tool. Layouts of the ten prototype circuits have been built in a 1.25 micron CMOS technology, and the performance predicted by the developed CAD tool and by SPICE simulations on extracted circuits is compared.

Chapter 7 is the concluding chapter of the thesis. It summarizes results, and discusses the application of the proposed figure of merit based methodology in CAD tools for the circuit synthesis of analog circuits. The chapter also highlights the future scope of work in this direction.

Chapter 2

Literature Survey

2.1 Introduction

The design of a complex analog macro-block like a phase-locked loop (PLL) or an analog-to-digital converter (ADC) or filters can be typically decomposed into smaller basic cells *e.g.* comparators, operational amplifiers, *etc.*, each of which is an interconnection of basic building blocks such as differential input stage, current sources/sinks, current mirrors, current and voltage references, differential pairs, output buffers, *etc.* Each of these basic building blocks can be designed in various possible architectures. Each of these architectures has its distinct features and its limitations. In this chapter, the existing literature has been explored to identify the gaps and hence the scope for the present work.

2.2 Basic Building Blocks

Some of the important building blocks of analog IC have been discussed in this section.

2.2.1 Differential Input Stage Amplifier

A differential pair is widely used as the input stage of the operational amplifiers. The configuration of a CMOS differential pair is shown in Fig. 2.1. It is made of two transistors with their source in common, fed by a current source. The transistors may either be n-channel, as shown, or p-channel and they are matched

to each other. The main function of the differential stage is to amplify the differential input signal and reject any common-mode component.

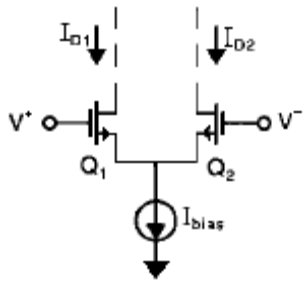


Figure 2.1 A CMOS Differential Pair.

Other design architectures of differential amplifier *e.g.* for current sensing [Bird89], for sensing amplifier in memory [Matsuda79], self-biased configuration for high speed applications [Bazes91], fully differential amplifier for large bandwidth [Ahn02], and optimization methods for achieving high CMRR [Areny91], increasing common-mode input-voltage range [Huijsing85, Bazes90, Wassenaar94] and stability [Brooks93], improved frequency compensation [Nelson93, Ho98], output swing stabilization [Johnson95, Suzuki09].

2.2.2 Current Sources/Sinks

A current sink and current source are two terminal components whose current at any instant of time is independent of the voltage across their terminals. The current of a current sink or source flows from the positive node, through the sink or source to the negative node. The simplest source/sink is a pMOS/nMOS transistor connected between V_{DD}/V_{SS} and the output node. It suffers from two limitations, one output resistance, which ought to be more. Secondly, the limited range of output voltage over which it works properly. Another implementation is the Cascode current source/sink, which has an improved value of output resistance [Allen87].

2.2.3 Current Mirrors

A current mirror is used to generate a replica (if necessary, it may be attenuated or amplified) of a given reference current. It uses the principle that if two identical MOS transistors are operating in their saturation region and their gate-source potentials are equal, then the channel currents should be equal. Electrically, a current mirror is a current controlled current source (CCCS). In real circuits, current mirrors are not able to accomplish the function of a CCCS, exactly. The current gain factor can only be positive while the output impedance, the dynamic range and the speed are finite. Moreover, the current to be copied is not measured ideally as it would be necessary to show a short circuit. Instead, to measure the reference current, a diode connected MOS transistor is normally used. The most commonly used circuits that accomplish the current mirror function are [Maloberti03]:

- Simple current mirror
- Wilson current mirror
- Improved Wilson current mirror [Palumbo93]
- Cascode current mirror
- Modified cascode current mirror
- High compliance current mirror
- Regulated cascode current mirror

All these circuits may deviate from ideal behaviour due to imperfect geometrical matching, technological parameter mismatch and parasitic resistances.

2.2.4 Current and Voltage References

Most of the basic building blocks use a current reference or voltage reference. The current value controls the trans-conductance of transistors and in turn,

influences the static and dynamic properties of the circuit in addition to the power consumption. Voltage reference is required to provide additional intermediate bias voltages. To avoid extra pins, designer prefers to generate them on chip. The characteristics of references are identical to those of the ideal voltage and current source. The references have more precision and stability than ordinarily found in a source. A reference is typically dependent upon the load connected to it, which possibly can be isolated by using a buffer amplifier in between and the high performance of the reference could be maintained. Therefore, an important designer task is to endow the master currents and bias voltages of the system with the required accuracy and independent of supply voltage and temperature. Further, a high performance voltage reference can be used to implement a high performance current reference.

A very crude voltage reference can be made from a voltage divider between the two power supplies. Two possible implementations are — one using nMOS transistors in diode arrangement and second by using both nMOS and pMOS transistors in diode arrangement [Maloberti03]. Unfortunately, the voltage divider also transfers to its output almost the same fraction of the noise and disturbances present on the supply lines. There are more design techniques used to generate an accurate and precise voltage reference. The accurate voltage elements made available by the CMOS technology are:

- The difference between the threshold voltages of an MOS transistor.
- The base-to-emitter voltages (V_{BE}), of a parasitic bipolar transistor.
- The thermal voltage, $V_T = kT/q$.

These three techniques can be used to design three different voltage references. Voltage reference based on threshold difference is temperature-independent and has a remarkable quality. But, it requires a technology that provides transistors of the same type and with different thresholds, which is rare and very expensive. The second voltage reference based on V_{BE} has a negative temperature coefficient

while the third voltage reference based on V_T has a positive temperature coefficient. Another type of voltage reference in the band-gap voltage reference that is able to keep the temperature coefficient to zero or near to zero in the given temperature range. It operates on the principle of compensating the negative temperature coefficient of V_{BE} with the positive temperature coefficient of the thermal voltage, V_T.

2.2.5 Output Buffers

All intermediate stages, which are used in op-amp or comparator before the output buffer, have the common characteristics of large output resistance to get a large voltage gain. A large output resistance can be undesirable when the load consists of a small resistance and/or large capacitance, where as a small load resistance requires a large current in order to provide a large output voltage swing. A large load capacitor requires large output currents to supply charging currents needed to meet transient response requirements. In order to provide a sufficient output current on a steady state or transient basis, it is necessary to use a low-resistance output buffer.

The primary objective of the CMOS output buffer is to function as a current transformer. Most output buffers have a high current gain and a low voltage gain. The specific requirements of an output buffer are:

- To provide sufficient output power in the form of voltage or current.
- To avoid signal distortion.
- To be efficient.
- To provide protection from abnormal conditions (short circuit, over temperature, *etc.*).

The first requirement is to meet the primary objective. The second requirement results from the fact that the signal swings are large and the non-linearities that

normally are not encountered in small-signal amplifiers will become important in output amplifiers. The third requirement is born out of the need to minimize power dissipation in the driver transistors themselves compared with that dissipated in the load. The fourth requirement is normally met with CMOS output stages since MOS devices are, by nature, self-limiting.

There are several approaches to implement the output buffer. The simplest one is an inverter with active load. It gives the best output dynamic range but an asymmetrical output driving capability. Other configurations used are cascode, and cascode with cascode load. The other configurations that give lower output resistance and keep some control on output resistance linearity are source follower and push-pull output buffers.

2.3 Basic Cells

The above-mentioned basic building blocks can be assembled to design basic cells *i.e.* operational amplifiers (Op-Amps) and comparators.

2.3.1 Operational Amplifiers

Operational amplifiers, usually referred to as op-amps, are key elements in analog processing elements. Ideally they perform the function of a voltage controlled current source with an infinite voltage gain. Only those circuit implementations that are specifically used to achieve the op-amp function in CMOS integrated VLSI systems are of relevance here. When used inside an integrated architecture, op-amps are mainly employed to drive capacitive loads, namely gates of transistors, capacitors or arrays of capacitors. This makes the request of having a low output impedance of little importance. Therefore, very often, op-amps are replaced by Operational Trans-conductance Amplifiers (OTAs) whose output impedance is quite high.

A large number of architectures for op-amps and OTAs are available in the literature *e.g.* Miller compensated two-stage op-amp, RC compensated two-stage op-amp that use two stages first the differential stage and second is the simple CMOS inverter. Other two stage op-amps include OTA op-amp, two-stage cascoded op-amp, Folded-Cascode op-amp [Hershenson98, Allen87], Active-cascode op-amp [Gray01], Symmetrical CMOS OTA [Laker94], uncompensated two-stage CMOS op-amp [Gregorian99] which is derived from its bipolar counterpart [Widlar69], two-stage op-amp with cascode differential stage [Gregorian99], improved uncompensated CMOS op-amp [Gregorian79]. Several of single stage op-amps such as simple OTA op-amp [Hershenson98], telescopic cascode, and mirrored cascode have been reported in [Maloberti03]. Other CMOS configurations reported are Cascode CMOS, cascode symmetrical CMOS OTA, symmetrical Miller CMOS OTA with high PSRR [Laker94], CMOS OTA with high PSRR [Steyaert90], folded cascode CMOS OTA [Laker94, Maloberti03]. Fully differential op-amps have been reported by several authors [Johns97, Laker94, Maloberti03, Razavi01, Gray01]. [Sedra87] has reported an Operational Current Amplifier (OCA) for differential current amplification.

2.3.2 Comparators

A comparator is the basic component mainly used in analog-to-digital converters. A comparator is the circuit that compares an analog signal with another analog signal, and outputs a binary signal based upon the comparison. There can be two possible types of input — voltage or current. In the former case, the input voltage is measured with respect to a given reference level. Therefore, the comparator determines whether the amplitude of the input is higher or not than a reference. When current is the input variable, the comparator determines whether the input current is flowing in or out of the input terminal.

One of the simplest practical implementation of CMOS comparator circuit is the current-sink inverter. The gain of this comparator implementation is low, but

could be improved substantially using cascode techniques. The major drawback is not the gain, but the fact that trip point is dependent upon the power supply. In addition, there is a limited range at which the trip point can be placed while still maintaining adequate gain. These problems can be solved by using differential input scheme. The key attribute of this circuit is its ability to amplify the difference between the inverting and non-inverting inputs. As a result, the trip point of a comparator can be made independent of process and supply variations. But, it cannot be controlled perfectly due to process-dependent input-offset voltage, which can be caused by threshold voltage, geometry, and/or temperature mismatch. Therefore, neither of the two proposed circuits performs the comparator function satisfactorily. But, they can have satisfactory performance if they are combined. In this two-stage comparator [Allen87], first stage is the differential stage and second is the inverting stage. With this configuration the limitations of the two are overcome.

Often a comparator is placed in a very noisy environment in which it must detect signal transitions at the threshold point. If the comparator is fast enough (depending upon the frequency of the most prevalent noise) and the amplitude of the noise is great enough, the output will also be noisy. In such a situation, a modification on the transfer characteristics of the comparator is desired. Specifically, hysteresis is needed in the comparator. There are several ways to accomplish it, primarily by involving some form of positive feedback. The most popular method is by introducing it in the input differential stage [Allstot82]. Regenerative Comparator [Gregorian99] has been used to convert a very slowly varying input signal into an output with abrupt changes, or in a noisy environment to detect an input signal crossing a threshold level.

In precision applications, such as high-resolution A/D converters, large input-offset voltages cannot be tolerated. While systematic offset can be nearly eliminated with proper design, random offsets still remain, and are unpredictable. Fortunately, there are offset-cancellation techniques in MOS technology. The

practical implementations of an auto-zeroed comparator are given by [Yee78, Allen87, Maloberti03]. CMOS cascode comparator uses pre-charging operations for biasing and auto-zeroing. Other comparators, such as, differential comparator, op-amp comparator, switched-capacitor comparator, *etc.* have been given in the literature [Gregorian99].

For high-accuracy applications, an effective way for reducing the dc offset voltage due to the feed-through charge is to use a fully differential comparator [Martin83, Razavi92, Razavi95, Maloberti03].

2.4 Design-Synthesis Methods

Circuit synthesis is the inverse operation of circuit analysis, where the sub-block parameters, such as device sizes and bias values, are given and the resulting performance of the overall block is calculated, as is done in SPICE. Synthesis in the analog domain refers to the automatic design of a circuit with a known qualitative behavior, such as amplification, to meet the performance (rather than behavioral) specifications of the problem [Ochotta98]. During synthesis, block performance is specified and values for the sub-block parameters needed to meet these specifications have to be determined. This inverse process is not a one-to-one mapping, but usually is an under-constrained problem with many degrees of freedom.

The different analog circuit synthesis methods that have been explored up till now can essentially be classified into four groups [Hershenson98].

2.4.1 Classical Optimization Methods

Classical optimization methods, such as steepest descent, sequential quadratic programming and Lagrange multiplier methods, have been widely used in analog circuits CAD. The general-purpose optimization codes NPSOL [Gill86] and

MINOS are used in [Maulik92, Chang92]. Other CAD methods based on classical optimization methods, and extensions such as a minimax formulation, include OPASYN [Koh90], OAC [Onodera90], and STAIC [Harvey92]. These classical methods can be used with complicated circuit models, including full SPICE simulations in each iteration, as in DELIGHT.SPICE [Nye88].

The main disadvantage of classical methods is that they only find locally optimal designs. This means that it is possible that some other set of design parameters, far away from the one found, may result in a better design. The same problem arises in determining feasibility — they may fail to find a feasible design, even if one exists. In order to avoid local solutions, the minimization method is carried out from many different initial designs. This increases the likelihood of finding the globally optimal design but it also destroys one of the advantages of classical methods, *i.e.* speed, since the computation effort is multiplied by the number of different initial designs that are tried. It also requires human intervention to give good initial designs, which makes the method less automated. Also, these methods become slow if complex models are used, as in DELIGHT.SPICE [Nye88].

2.4.2 Knowledge-Based Methods

Knowledge-based and expert-systems methods have been widely used in analog circuits in late 1980s. Specific heuristic design knowledge about the circuit topology under design was encoded explicitly in some computer executable form that was then executed during the synthesis run for a given set of input specifications to obtain the design solution. The knowledge was encoded in different ways in different systems.

The IDAC tool [Degrauwe87] used manually derived and prearranged design plans or design scripts to carry out the circuit sizing. The design equations specific for a particular circuit topology had to be derived and the degrees of

freedom in the design had to be solved explicitly during the development of the design plan using simplifications and design heuristics. The big advantage of using design plans is their fast execution speed, which allows for fast performance space explorations [Harjani89]. The big disadvantages are the lack of flexibility and the large time needed to develop a plan for each topology and design target (typically 4 times than needed to actually design the circuit once [Beenker93]), as analog design heuristics are very difficult to formalize in a general and context-independent way.

OASYS [Harjani89] adopted a similar design plan based sizing approach, but explicitly introduced hierarchy in the design of analog circuits and also added a heuristic approach towards topology selection to the system. Hierarchy allowed to reuse design plans of lower-level cells while building up higher-level cell design plans, and therefore also leveraged the number of device-level schematics covered by one top-level topology template. Collecting and ordering all the design knowledge in the design plan however still remained a time-consuming job. The approach was later on adopted in the commercial MIDAS system [Beenker93].

The other ways to encode the knowledge have been explored as well, such as in BLADES [Turky89] which is a rule-based system to size analog circuits and DARWIN [Kruiskamp95] which uses genetic algorithms or evolution system.

2.4.3 Global Optimization Methods

Global optimization methods such as branch-and-bound [Xinghao96] and simulated annealing [Laarhoven87, Wong88] have also been used, *e.g.*, in [Maulik95]. Branch-and-bound unambiguously determines the global optimal design but it is extremely slow, with computation growing exponentially with problem size. Global Simulated Annealing (SA) is another very popular method that can avoid becoming trapped in a locally optimal design. In principle it can compute the globally optimal solution, but in practical implementations there is

no guarantee at all as termination is heuristic. Like classical and knowledge-based methods, SA allows a very wide variety of performance measures and objectives to be handled. Simulated annealing has been used in several tools such as ASTR/OBLX [Ochotta96] and OPTIMAN [Gielen90, Gielen91]. The main disadvantage of SA is that it can be very slow, and in practice it cannot guarantee a global optimal solution.

2.4.4 Convex Optimization and Geometric Programming Methods

In a convex optimization problem we minimize a convex objective function subjected to linear equality constraints, and inequality constraints that are expressed as upper bounds on convex functions. The great practical advantage of convex optimization is beginning to be widely appreciated, mostly due to the development of extremely powerful interior-point methods for general convex optimization problems in last five years [Nesteroy94, Wright97]. These methods can solve large problems, with thousands of variables and tens of thousands of constraints, very efficiently. One great advantage of convex optimization, compared to general-purpose optimization methods, is that the global solution is always found, regardless of the starting point and infeasibility is also unambiguously detected. One of the disadvantages is that the types of problems, performance specifications, and objectives that can be handled are far more restricted than any of the methods described above.

Geometric Programming (GP) is a special type of convex optimization problem, which is recently being used for transistor and wire sizing in digital circuits [Fishburn85, Shyu88, Sapatnekar93, Sapatnekar96] and in analog circuits [Hershenson01, Mandal01]. But the current GP transistor models support the traditional long channel MOS transistors and the GP models for submicron devices are still under development.

2.5 Concept of Figure of Merit

The concept of Figure of Merit to estimate the performance in terms of power, propagation delay and area started in digital circuits and later was adopted by analog circuit designers as well. In analog domain Figures of Merit have been defined for four basic circuits [Brederlow01] Low Noise Amplifiers (LNA) [Yoshida06], Voltage Controlled Oscillators (VCO) [Muer00], Power Amplifiers (PA) and Analog-to-Digital Converters (ADC). The concept of figure of merit has also been applied to evaluate the performance of instrumentation amplifiers [Menolfi99], to study the performance in terms of small signal and large signal behavior of driver/output stage amplifiers [Leung00, Ramos02], for the linearity test of differential amplifiers [Nam03], to study testability of mixed-signal circuits and systems [Soma01], for architecture selection in active filter designs, *etc*. The concept has been widely used in performance evaluation, comparison and selection of ADCs [Walden99, Vogels03], to design of sigma-delta ADC [Rabii97, Marques98], flash ADC [Yoshii84], asynchronous ADC [Allier05] and speed-power tradeoffs of high speed ADC [Uyttenhove02] and many more.

The use of figure of merit is also seen in literature to evaluate the performance of RF CMOS circuits [Woerlee01, Walden99a].

2.6 Gaps Identified

The existing literature in books and journals was explored. So far mostly it is said that for analog circuits, there is no area constrain and only the performance is the requirement. However, there are per pixel processing applications, where area is becoming a major constraint. For example, consider a camera with only a resolution of 4 Mega-pixels. It requires an IC, which captures the image/signal. We require an array of 2K $\times$ 2K preprocessing circuits one for each pixel. If we assume that the size of IC is such that 1 cm^2 area is available for these circuits, we get only 1 cm^2/4Mega = 10^8 $\mu m/4 \times 10^6$ = 25 μm^2 for the processing of a pixel!

Some researchers have indicated sharing of resources between columns or group of 4 pixels, *etc.* [Pain93, Espejo94, Fowler95, Mendis97, Fossum97, Yang99, Kleinfelder01, Bermak02, Lin04, Dudek05, Eltoukhy06].

It was found that there had been no attempt so far to design and optimize analog integrated circuits in the area-constrained environment. And hence there is a scope to work in this direction.

Another application domain is the night vision cameras employed for strategic applications, where signals to be captured are normally weak and noise becomes very significant. And therefore, noise is one of the significant parameters, which can be taken along with the area-constraint.

Hence, this gap sets the exploration path and motivation for the present research work.

Chapter 3

Area Constrained Optimization of Input Stage Differential Amplifier for Low Frequency Applications

3.1 Introduction

The first stage of an operational amplifier and several types of comparators is typically a differential amplifier that needs to provide sufficient gain and bandwidth while introducing as little noise as possible. Moreover, if this is desired with a constraint on area, the problem becomes more difficult. The classical noise optimization technique for Low Noise Amplifier (LNA) design presumes a device given with fixed characteristics, and thus offers no explicit guidance on how to best exercise the IC designer's freedom in tailoring device geometries under the constraints of area [Shaeffer97].

3.2 Concept of Figure of Merit

To compare different solutions for an analog circuit design, first a figure of merit must be agreed upon. This can then be used to design the circuit with maximal figure of merit under constraints of area. Here, a figure of merit has been proposed that takes into account the three key performance parameters of a differential amplifier *i.e.* the differential dc gain, unity-gain bandwidth and input-referred noise.

The proposed figure of merit (FoM) is

$$FoM = \frac{UGB * Ad}{IRN} \tag{3.1}$$

where UGB is the unity-gain bandwidth, Ad is the differential dc gain and IRN is the peak input-referred noise spectral density. The differential amplifier is illustrated in Fig. 3.1.

The differential amplifier is comprised of transistors M1 through M4. Transistors M1 and M2 are standard nMOS transistors, which form the basic input stage of the amplifier. The gate of M1 is the inverting input and the gate of M2 is the non-inverting input. A differential input signal applied across the two input terminals will be amplified according to the gain of the differential stage.

Such a FoM is useful for image sensors (optical/IR) that do not have a very fast frame rate and the signal is at low frequencies. Attaining a high UGB results in a low time-constant, this allows the output signal to settle faster. The target applications feature narrow bandwidths at lower frequencies where flicker noise is the dominant noise and hence thermal noise has not been included in the Figure of Merit.

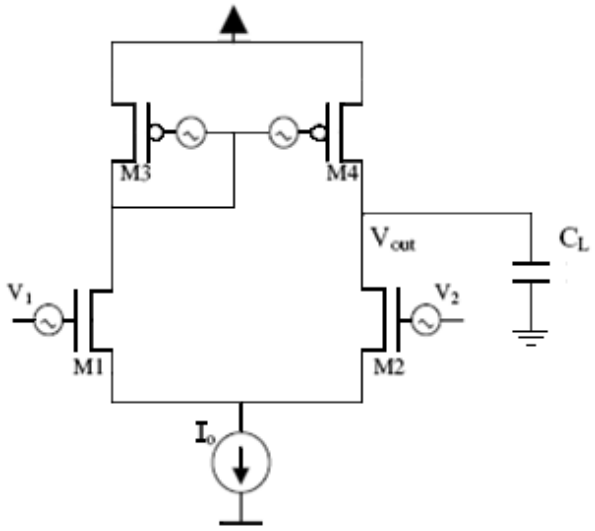


Figure 3.1 Differential Amplifier

3.3 Performance Parameters

This section discusses the three performance parameters, namely noise, differential dc voltage gain and unity-gain bandwidth being considered for the formulation of the figure of merit. It then arrives at an analytical expression for the figure of merit in terms of the device parameters.

3.3.1 Noise in MOS Transistor

Each semiconductor device in the circuit introduces noise. Three types of noises are common in a MOS device, namely — Shot, Thermal and Flicker ($1/f$). At low frequencies, flicker ($1/f$) noise dominates all other noises. Therefore, here only flicker noise has been considered to develop the concept.

FLICKER NOISE MODEL(S)

In an MOS transistor, extra electron energy states exist at the boundary between the Si and SiO_2. These can trap and release electrons from the channel, and hence introduce noise [Das74, Gray92]. Since the process is relatively slow, most of the noise energy will be at low frequencies. A possible model of this noise phenomenon is a current source in parallel with the channel resistance or a voltage source in series with the gate resistance as shown in Fig. 4.2. The dc value of noise current or voltage is zero. Its mean-square value increases with temperature and density of surface states and decreases with the gate area $W \times L$ and the gate oxide capacitance per unit area, C_{OX}. There exist numerous models for flicker noise in MOS transistor [Hung90, Chang94, Jakobson98, Arnaud04, Xie00, Zhou01, Arnaud03, Vandamme00, Gray01]. According to the most popular model [Gray01], the flicker noise in a MOS transistor can be lumped as a voltage source at the gate and is given by

$$\overline{V_{eq}^2} = \frac{K_F}{C_{OX} \cdot W_{eff} \cdot L_{eff}} \cdot \frac{\Delta f}{f} \tag{3.2}$$

in the noise bandwidth of Δf at frequency f. W_{eff} and L_{eff} are the effective width and length of the gate of the MOS transistor, K_F is the flicker noise coefficient for the MOS transistor which depends on temperature and fabrication process, a typical value being $2\times10^{-24} V^2 \cdot F$. C_{OX} is the gate capacitance per unit area. The noise process described above is usually called *flicker noise* or *1/f noise*. At low frequencies, it is usually the dominant noise mechanism in a MOS transistor. For devices fabricated with a "clean" process, the gate-referred noise voltage is nearly independent of the bias conditions. However, the overall circuit noise depends on the circuit configuration.

INPUT-REFERRED NOISE

For the differential amplifier shown in Fig. 3.1, there are four different voltage noise sources – each connected to the gate of every transistor. If all these sources are lumped together at the gate of transistor M1, the mean square value of the equivalent noise voltage source at input (gate of M1) for the total circuit noise is given by

$$\overline{V_{eqT}^2} = \overline{V_{eq1}^2} + \overline{V_{eq2}^2} + \left(\frac{g_{ml}}{g_{mi}}\right)^2 \cdot \left(\overline{V_{eq3}^2} + \overline{V_{eq4}^2}\right) \tag{3.3}$$

where $\overline{V_{eq1}^2}$, $\overline{V_{eq2}^2}$, $\overline{V_{eq3}^2}$, $\overline{V_{eq4}^2}$ are the noise sources at the gates of transistors M1, M2, M3 and M4. g_{mi} and g_{ml} are the trans-conductance of the input (M1 and M2) and load (M3 and M4) transistors, respectively, and are given by

$g_{mi} = \sqrt{2 \cdot k_n \cdot \left(\frac{W_i}{L_i}\right) \cdot \left(\frac{I_o}{2}\right)}$, and

$$g_{ml} = \sqrt{2 \cdot k_p \cdot \left(\frac{W_l}{L_l}\right) \cdot \left(\frac{I_o}{2}\right)}. \tag{3.4}$$

where W_i, W_l and L_i, L_l are respectively the widths and lengths of input and load transistors, k_n and k_p are the process trans-conductance parameters for n-channel and p-channel MOS transistors, and I_o is the tail current of the differential amplifier.

Using equations (3.2), (3.3) and (3.4), the power spectral density (PSD) of noise at the gate of M1 is written as

$$S_{VG}^2 = \frac{\overline{V_{eqT}^2}}{\Delta f} = \frac{2 \cdot K_{Fn}}{C_{OX} \cdot W_i \cdot L_i \cdot f} \cdot \left[1 + \frac{k_p \cdot K_{Fp} \cdot L_i^2}{k_n \cdot K_{Fn} \cdot L_l^2}\right] \tag{3.5}$$

Therefore, root mean square value of spectral power density better known as input-referred noise (IRN) at frequency f is written as

$$IRN = \sqrt{\frac{2 \cdot K_{Fn}}{C_{OX} \cdot W_i \cdot L_i \cdot f} \cdot \left[1 + \frac{k_p \cdot K_{Fp} \cdot L_i^2}{k_n \cdot K_{Fn} \cdot L_l^2}\right]} \tag{3.6}$$

3.3.2 Unity-Gain Bandwidth

Unity-gain bandwidth of the differential input stage, UGB is given by

$$UGB = \frac{g_{mi}}{2 \cdot \pi \cdot C_L} = \frac{1}{2 \cdot \pi \cdot C_L} \sqrt{\frac{k_n \cdot W_i \cdot I_o}{L_i}} \tag{3.7}$$

where C_L is the total load capacitance at the output node.

3.3.3 Differential dc Gain

The differential dc gain, *Ad* of the differential amplifier is given by

$$Ad = \frac{g_{mi}}{g_{di} + g_{dl}} = 20 \cdot \sqrt{\frac{k_n}{I_o} \cdot \left(\frac{W_i}{L_i}\right)} \cdot \left(\frac{1}{L_i} + \frac{1}{2.L_l}\right)^{-1} \tag{3.8}$$

where g_{di} and g_{dl} are the drain conductances of input and load transistors respectively.

The drain conductance g_d is approximated as

$$g_d = \frac{I_o}{2.L} \cdot \left(\frac{dx_d}{dV_{DS}}\right) \tag{3.9}$$

where $\left(\frac{dx_d}{dV_{DS}}\right)$ (known as channel-length modulation parameter) is a process parameter [Gray92] and its value has been taken as 0.1 μm/V for nMOS and 0.05 μm/V for pMOS transistors for 1.25 μm CMOS process.

The expression also assumes that M1 and M2 are identical and M3 and M4 are identical as well. The current mirror active load used in this circuit has three distinct advantages:

- The use of active load devices creates a large output resistance in a relatively small amount of die area.
- The current mirror topology performs the differential to single-ended conversion of the input signal.
- The load also helps with common mode rejection ratio (CMRR).

Using a current mirror active load device as the load resistance in a differential stage increases the CMRR. The current biasing transistor M5, which presents a

large source degeneracy resistor to the differential stage, also contributes to the effectiveness of the amplifier at suppressing common mode signals.

3.3.4 Figure of Merit

Substituting the values of UGB, Ad and IRN from equations (3.6), (3.7) and (3.8) in (3.1), we get

$$FoM = \frac{5\sqrt{2}\cdot\mu_n\cdot C_{OX}^{3/2}\cdot W_i^{3/2}\cdot L_i^{3/2}}{\pi\cdot C_L\cdot\sqrt{K_{fn}\cdot\left(\frac{1}{f}\right)}}\cdot\frac{1}{L_i}$$
$$\cdot\left(1+\frac{L_i}{2.L_l}\right)^{-1}\cdot\left(1+\frac{k_p\cdot K_{fp}\cdot L_i^2}{k_n\cdot K_{fn}\cdot L_l^2}\right)^{-1/2} \quad (3.10)$$

3.4 Maximization of Figure of Merit Under Area Constraints

Many imaging applications have per pixel signal integrators. The area constraint is important for such applications. Therefore, area has been taken as the first constraint and the expression for figure of merit has been maximized under that constraint through relative area allocations between the input and load transistors.

If A is the total area available for the devices in the differential amplifier, let us assign a fraction x of A *i.e.* $(x\cdot A)$ to the input transistors and $(1-x)\cdot A$ to load transistors. Then, writing the expressions for UGB, Ad and peak IRN (at $f = 1$ Hz) in terms of x, area (A), bias current (I_o) and technology parameters, we get

$$A_d = 20\cdot\sqrt{\frac{k_n\cdot(x\cdot A)}{I_o}}\cdot\left(1+\frac{L_i}{2.L_l}\right)^{-1} \quad (3.11)$$

$$UGB = \frac{\sqrt{k_n.I_o \cdot (x \cdot A)}}{2\sqrt{2}.\pi \cdot C_L} \cdot \frac{1}{L_i} \tag{3.12}$$

$$IRN = \sqrt{\frac{4 \cdot K_{Fn}}{C_{OX} \cdot (x \cdot A)} \cdot \left[1 + \frac{k_p \cdot K_{Fp} \cdot L_i^2}{k_n \cdot K_{Fn} \cdot L_l^2}\right]} \tag{3.13}$$

Hence, from equations (3.1), (3.11), (3.12) and (3.13) figure of merit (FoM) in terms of x, area (A), bias current (I_0) and technology parameters is written as

$$FoM = \frac{5\sqrt{2} \cdot k_n \cdot C_{OX}^{1/2} \cdot (x \cdot A)^{3/2}}{\pi.C_L \cdot K_{Fn}^{1/2}} \cdot \frac{1}{L_i} \cdot \left(1 + \frac{L_i}{2.L_l}\right)^{-1} \cdot \left(1 + \frac{k_p \cdot K_{Fp} \cdot L_i^2}{k_n \cdot K_{Fn} \cdot L_l^2}\right)^{-1/2} \tag{3.14}$$

From equation (3.14), following conclusions can be drawn

- Figure of Merit, FoM is dependent on technology parameters, $k_n, k_p, C_{OX}, K_{Fn}, K_{Fp}$.
- It is inversely proportional to the output load, C_L.
- To maximize FoM, length of input transistor L_i should be kept minimum for a given area A, as that choice maximizes all the three product terms above where it appears.
- Figure of Merit is independent of the width of load transistor, W_l hence it should be kept as minimum.
- Length of load transistor L_l should be as large as possible under the constraints of area since it maximizes the last two product terms and hence maximizes Figure of Merit FoM.

3.5 Analytical Results

Fig. 3.2 shows the variation of differential dc gain as a function of relative area allocated to input transistors at different values of total area. It is clear that as the total area increases, the differential dc gain increases. But, it does not keep on increasing with increase in input transistor area. The peak value of dc gain is obtained for x in the range of 0.6 to 0.8. Fig. 3.3 shows that the unity-gain bandwidth is a monotonically increasing function of x.

The variation of peak value of input-referred noise as a function of x is shown in Fig. 3.4. For larger values of x, the noise is reducing because with increasing x the gate area of input transistors is increasing and their noise contribution is decreasing. But, it is interesting to note that it starts increasing beyond a point for all the values of A. It implies that beyond this point, the contribution of noise from load transistors over and above the contribution of input transistors increases.

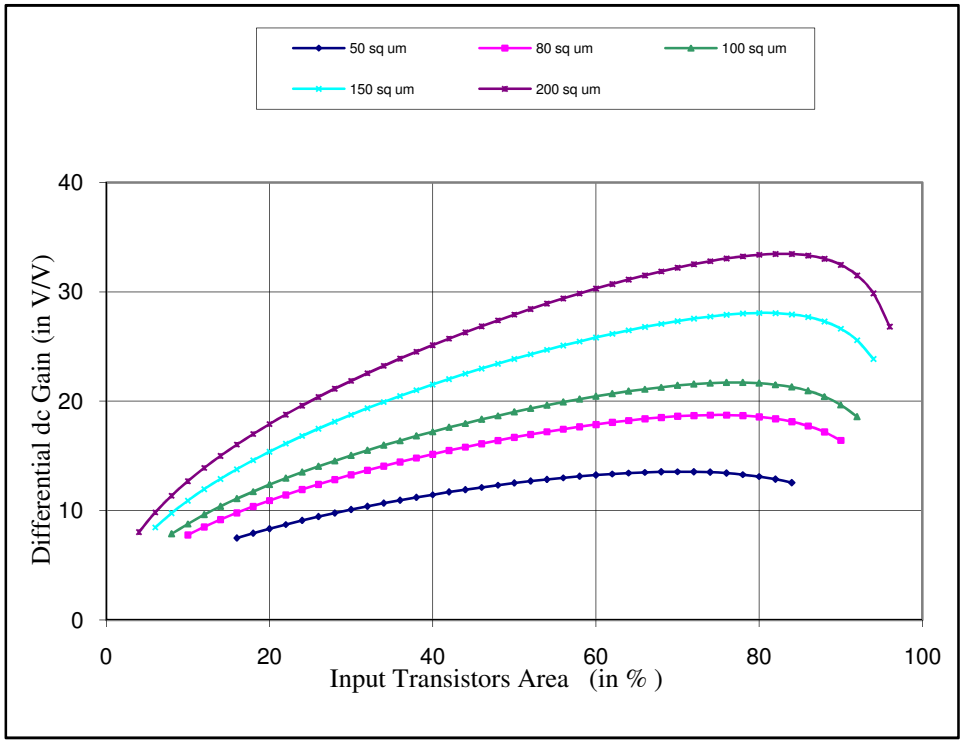


Figure 3.2 The differential dc gain as a function of input transistor area.

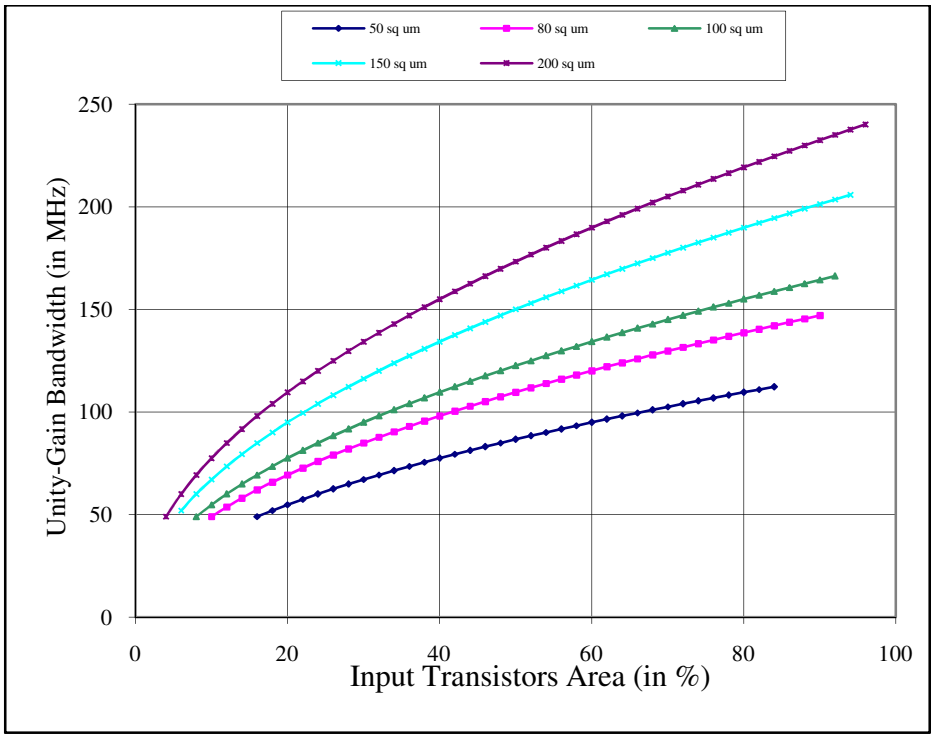


Figure 3.3 Unity-Gain Bandwidth (in MHz) as a function of input transistor area.

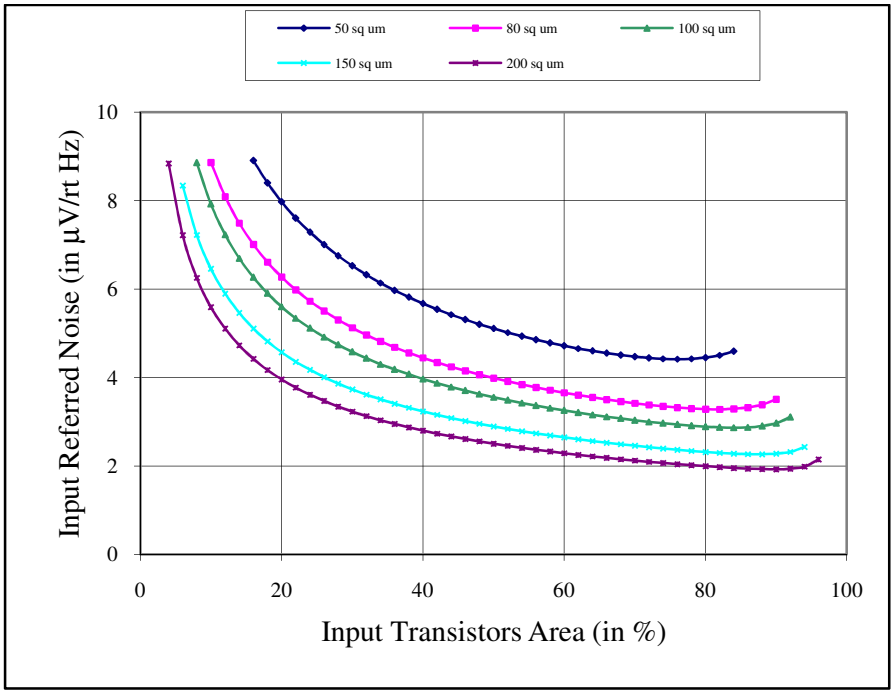


Figure 3.4 Input-referred noise (in µV/rtHz) as a function of input transistor area.

Next the figure of merit is plotted as a function of percent area allocated to input transistors. Figure of Merit is a peaking function of x in the domain of 60% to 80% as shown in Fig. 3.5. It is clear that figure of merit increases with total area, A.

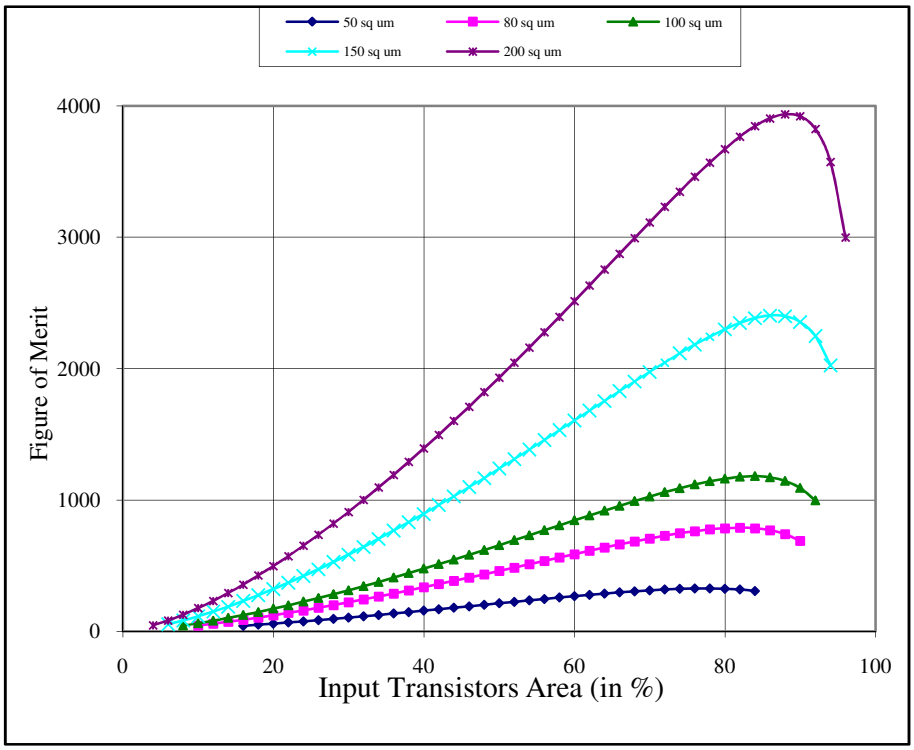


Figure 3.5 The Figure of Merit, FoM (in $*10^{12}$ $Hz^{3/2}/V$) as a function of input transistor area.

It also indicates that for a fixed value of total area, what percentage of total area should be assigned to input transistors to obtain a maximum value of Figure of Merit. Equation (3.14) clearly indicates that the figure of merit, FoM is also a function of total area. Peak value of figure of merit as a function of total area is plotted in Fig. 3.6.

The value of Figure of Merit is independent of Bias Current, I_o. However, a minimum value of power is essential to keep all the transistors in saturation. Fig. 3.7 shows the minimum bias current required for keeping all the transistors in the circuit in saturation region (and in strong inversion) as a function of total area. It implies that for a given area, a minimum power has to be provided. To increase

the figure of merit, area increase alone is not enough; more power is also required to keep the transistors in saturation.

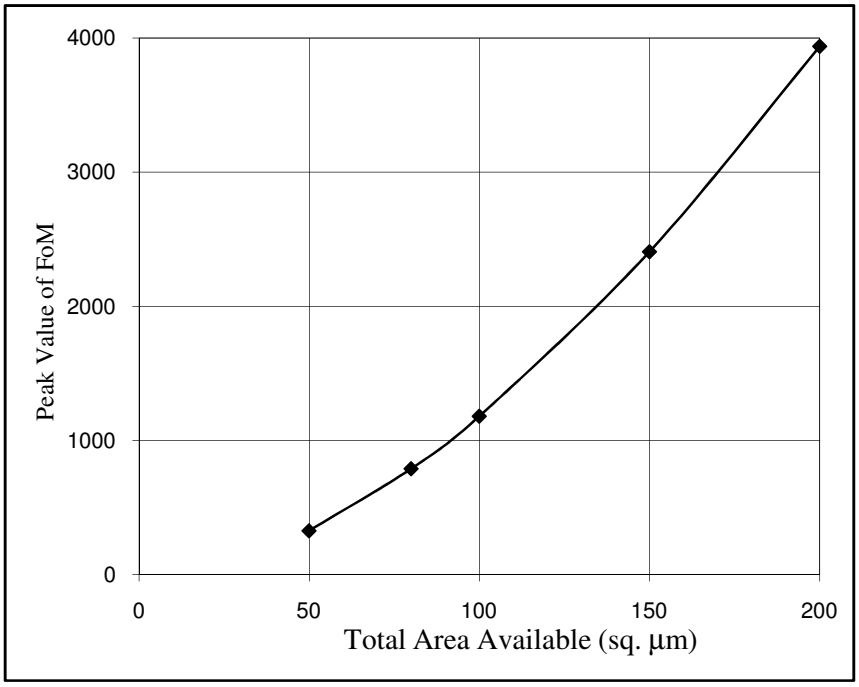


Figure 3.6 Peak value of figure of merit (FoM) as a function of area.

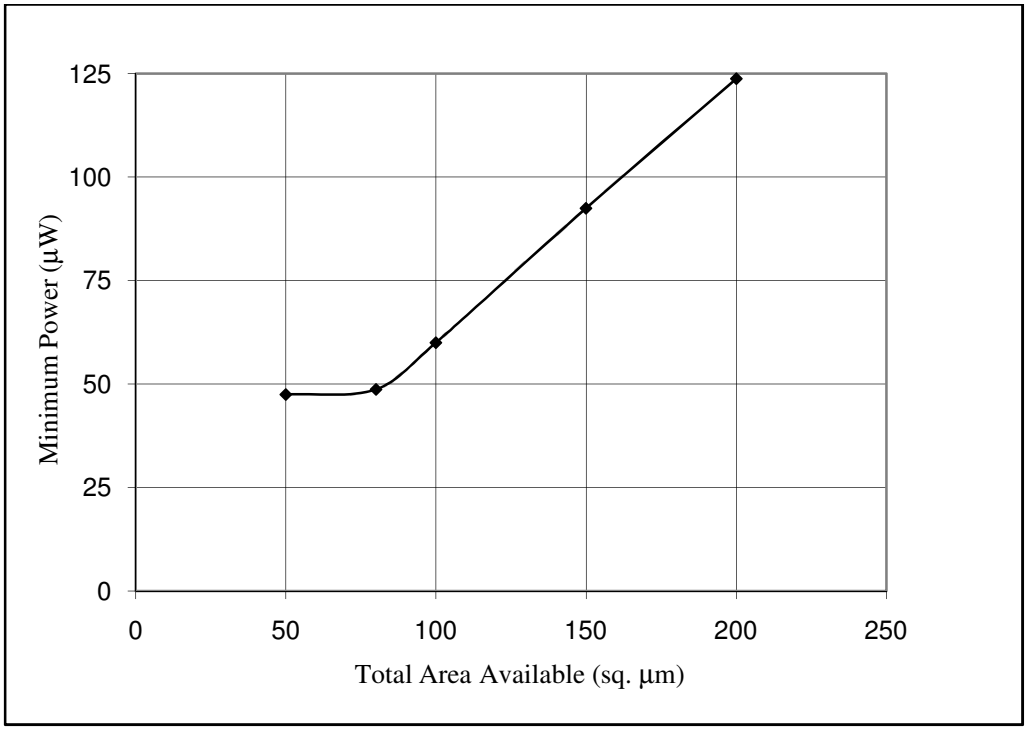


Figure 3.7 Minimum power desired as a function of total area.

3.6 Simulation Results

SPICE simulations using Tanner Tools Pro, have also validated the analytical results. To perform this task, a value of total area was chosen. The total area was divided between input and load transistors in a predefined ratio. Then for this distribution of areas all combinations of aspect ratio of input and load transistors were simulated to obtain the differential dc gain, unity-gain bandwidth and peak value of input-referred noise. The figure of merit was computed from these parameters. The peak figure of merit as a function of input transistor area in percent of total available area for all the transistors for various values of total area is plotted as shown in Fig. 3.8. This plot matches well with the analytical results shown in previous section.

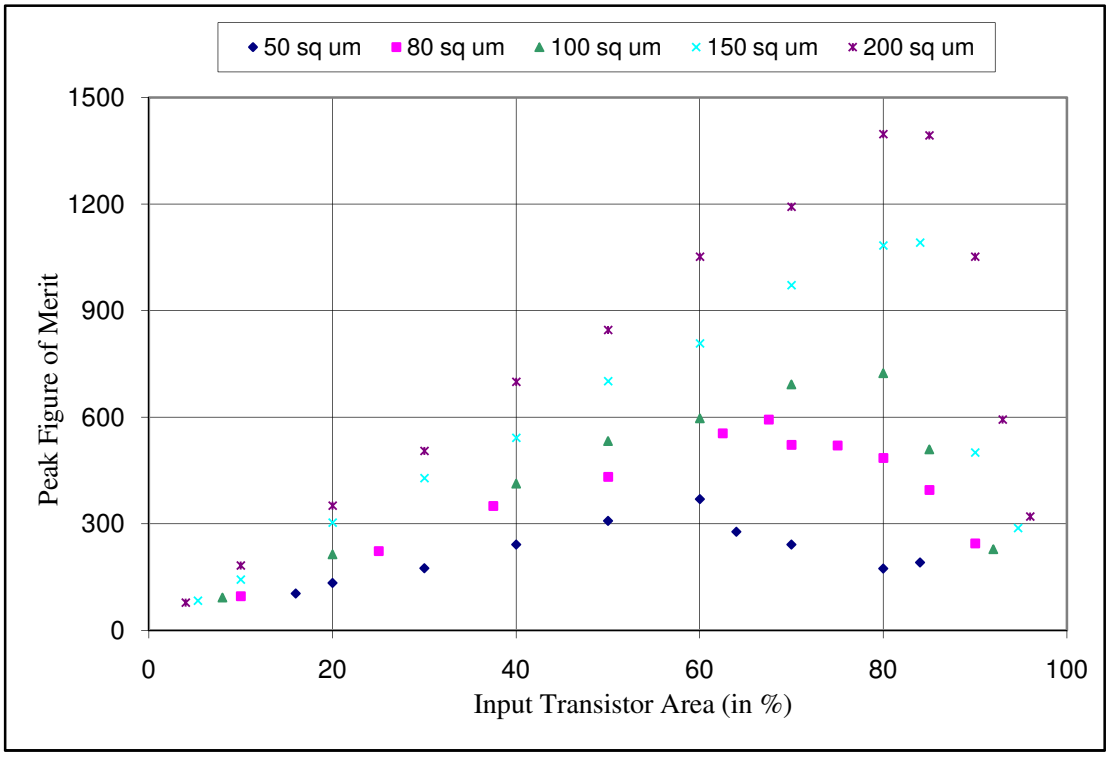


Figure 3.8 Simulated plot of figure of merit, FoM (in $*10^{12}$ $Hz^{3/2}/V$) as a function of input transistor area.

TABLE 3.1 Comparison Between Analytical and Simulated Performances at Peak Figure of Merit

Area (μm^2)	Peak Figure of Merit (in $*10^{12}$ $Hz^{3/2}/V$)		$Ad\%$		$UGB\%$		$IRN\%$	
	Analytical	Simulated	Analytical	Simulated	Analytical	Simulated	Analytical	Simulated
50	325.44	369.47	98.05	94.55	96.36	95.06	100.16	100
80	787.86	594.21	98.23	95.25	95.45	92.68	100	100
100	1179.8	723.55	98.11	99.56	95.55	94.84	100	100
150	2405.63	1091.78	98.71	98.92	95.65	91.2	100.13	100
200	3938.29	1397.69	98.66	94.24	95.74	81.85	100.16	100

In order to demonstrate the utility of figure of merit as a tool to optimize the design, we define three new parameters as follows:

$Ad\%$ — Differential dc gain at peak figure of merit as a percentage of maximum differential dc gain achievable for a given area.

$UGB\%$ — Unity-gain bandwidth at peak figure of merit as a percentage of maximum unity-gain bandwidth achievable for a given area.

$IRN\%$ — Input-referred noise at peak figure of merit as a percentage of minimum input-referred noise achievable for a given area.

Table 3.1 compares the analytical and simulated values of peak figure of merit, $Ad\%$, $UGB\%$, $IRN\%$ for constant area. In most cases the value of $Ad\%$ is more than 95%, the value of $UGB\%$ is more than 91% and the value of $IRN\%$ is less than 101% , which goes to demonstrate the usefulness of the proposed approach.

The concept of Figure of Merit is a suitable tool for synthesizing optimal design of differential amplifiers under area constraints and leads to the realization of differential dc gain, unity-gain bandwidth and input-referred noise values that are also very close to their individually achievable maximum values under the same

area constraints. The above analyses validate that the idea of FoM is deployable in a CAD tool for automatically synthesizing the differential amplifiers and can be extended for many other building blocks for low frequency applications. The approach also highlights the dependence of peak figure of merit and the minimum power required to achieve it on the area available for the transistors for a given technology.

Chapter 4

Area-Constrained Design of Differential Input Stage at Mid/Moderate Frequency Ranges

4.1 Introduction

In this chapter, the proposed methodology of designing the differential input stage amplifier using the concept of Figure of Merit at low operating frequencies in the previous chapter has been revalidated in the mid/moderate frequency ranges.

4.2 Figures of Merit

The concept of Figure of Merit was proposed in chapter 3 for the low frequency applications where flicker noise is the dominant noise. This figure of merit is not suitable for the first stage of a two-stage compensated operational amplifier operating in mid frequency ranges for two reasons. One, at these frequencies, thermal noise dominates the flicker noise and secondly, the pole of the first stage has to be shifted towards left in order to provide proper splitting of poles.

Here, two expressions for the figure of merit are proposed. Firstly, the same expression, as proposed before in chapter 3 with flicker noise replaced by thermal noise, as thermal noise will dominate the flicker noise at mid/moderate frequencies, given by

$$FoM2 = \frac{UGB * Ad}{IRN(th)} \tag{4.1}$$

where UGB is the unity-gain bandwidth, Ad is the differential dc gain and $IRN(th)$ is the input-referred thermal noise spectral density in the band of interest for the differential amplifier illustrated in Fig. 4.1.

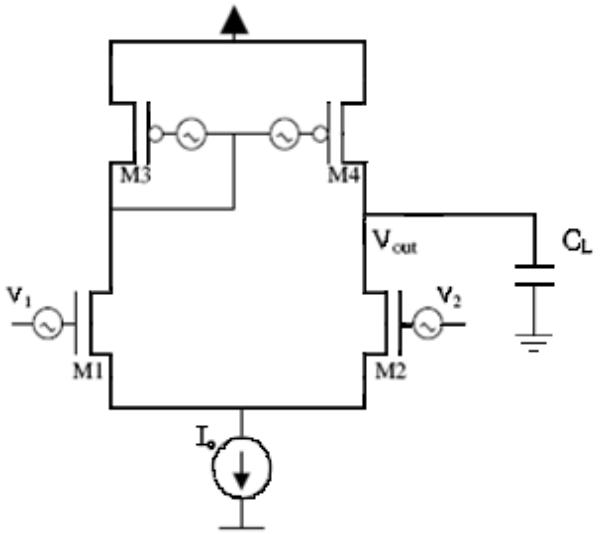


Figure 4.1 Differential amplifier.

Another figure of merit has been proposed for differential input stage of a two stage compensated operational amplifier operating at mid frequency that takes into account the maximization of differential gain with minimization of total mean square noise in the gain band and is proposed to be given by:

$$FoM3 = \frac{Ad}{UGB * \left(IRN(th)\right)^2} \tag{4.2}$$

where UGB is the unity-gain bandwidth, Ad is the differential dc voltage gain and $\left(IRN(th)\right)^2$ is the mean square input-referred thermal noise spectral density.

4.3 Thermal Noise Model for MOS Transistor

Each semiconductor device in the circuit introduces noise. Out of the various types of noises that could be possible in a device, thermal noise starts dominating at mid frequencies.

In a real resistor R, the electrons are in random thermal motion. As a result, a fluctuating voltage v_{nT} appears across the resistor even in the absence of a current from an external circuit as shown in Fig. 4.2(a). Thus, the Thévenin model of the real (noisy) resistor is that shown in Fig. 4.2(b). Clearly, the higher the absolute temperature (T) of the resistor, the larger is v_{nT}. In fact, it can be shown that the mean square of v_{nT} is given by

$$\overline{v_{nT}^2} = 4kTR\Delta f \ . \tag{4.3}$$

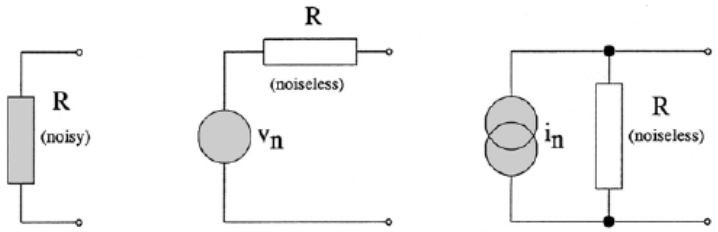


Figure 4.2 (a) Noisy resistor, (b) Thévenin equivalent circuit, (c) Norton equivalent circuit.

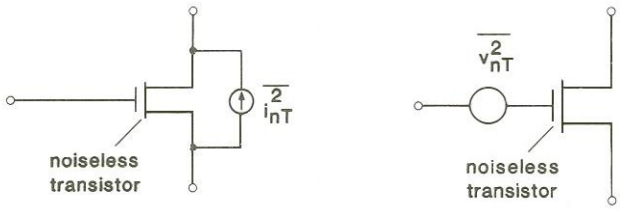
Here, k is the ubiquitous Boltmann's constant, and Δf is the bandwidth in which the noise is measured, in Hz.

If the above equation was true for any bandwidth, then the energy of the noise would be infinite. In fact, however, for very high frequencies ($\approx 10^{13}$) other physical phenomena enter, which cause $\overline{v_n^2}$ to decrease with increasing frequency so that the overall noise energy is finite.

The average value (dc component) of the thermal noise is zero. Since its spectral density $\overline{v_{nT}^2}/\Delta f$ is independent of frequency (at least for lower frequencies), it is a "white noise". Clearly, Fig. 4.2(b) may be redrawn in the form of a Norton equivalent, that is as a noiseless resistor R in parallel with a noise current source i_{nT} as shown in Fig. 4.2(c). The value of the latter is given by

$$\overline{i_{nT}^2} = \frac{4kT\Delta f}{R}. \tag{4.4}$$

Since the channel of a MOSFET in conduction contains free carriers, it is subject to thermal noise. Therefore, the two equations (4.3) and (4.4) will hold, with R given by the incremental channel resistance. The noise can then be modeled by a current source, as shown in Fig. 4.3(a). If the device is in saturation, its channel tapers off, and the approximation $R \cong \frac{3}{2g_m}$ can be used in the above equation.



(a) (b)

Figure 4.3 Equivalent models for the thermal noise in a MOS transistor.

In most circuits, it is convenient to pretend that i_{nT} is caused by a voltage source connected to the gate of an (otherwise noiseless) MOS transistor as shown in Fig. 4.3(b). This "gate referred" noise voltage source is then given by

$$\overline{v_{nT}^2} \cong \overline{(i_{nT}/g_m)^2} = \frac{8}{3}\frac{kT}{g_m}\Delta f. \tag{4.5}$$

Both i_{nT} and v_{nT} thus depend on the dimensions, bias conditions, and temperature of the device. If the device is switched off, then R becomes very high, and the equivalent noise current source $\overline{i_{nT}^2}$ is very small; hence, for usual (low or moderate) external impedance levels, the MOS transistor can be regarded as a noiseless open circuit if it is turned off.

In the SPICE2 circuit simulator the drain-current-referred thermal noise power spectral density (PSD) for MOS transistor utilizes the model of equation (4.5) and is given by

$$S_i = \frac{\overline{i_{nT}^2}}{\Delta f} = \left(\frac{2}{3}\right) 4kTg_m \tag{4.6}$$

This model is clearly invalid in the linear region [Tsividis84], because for the drain voltage $V_d = 0$, it predicts $S_i = 0$, whereas the PSD should be $4kTg_{d0}$, where g_{d0} is the drain conductance g_d at $V_d = 0$. There exists many analog applications *e.g.* switch-capacitor and MOS-C continuous-time filters, in which MOS transistor operates in linear region and hence the noise must be modeled in the linear region.

Another model [Nicollini87] defines the drain-current referred thermal noise power spectral density as

$$S_i = \alpha kT\left(g_m + g_{mb} + g_d\right) \tag{4.7}$$

where g_{mb} is the back-gate trans-conductance, and $\alpha = 1 - V_b/\left(3V_{dsat}\right)$ for $V_d < V_{dsat}$ or $\alpha = 2/3$ for $V_d \geq V_{dsat}$. V_{dsat} is the V_d value at the border of the linear and saturation regions. The added term g_d ensures that the noise is nonzero in the linear region, and the factor α varies linearly from 1 (at $V_d = 0$) to $2/3$ (at $V_d = V_{dsat}$) to give the proper noise values in saturation and at $V_d = 0$. The serious deficiency of this model is that it is inconsistent with SPICE model levels due to

the g_{mb} term in equation (4.7) which can be a substantial fraction of $g_m + g_d$ [Fox93].

In the present work, the most popular model given by equation (4.6) has been used. According to it, the thermal noise due to a MOS transistor can also be lumped as a voltage source at its gate and can be written as

$$\overline{V_{eq}^2} = 4kT \cdot \left(\frac{2}{3g_m} \right) \cdot \Delta f \tag{4.8}$$

or

$$S_v = \frac{\overline{V_{eq}^2}}{\Delta f} = 4kT \cdot \left(\frac{2}{3g_m} \right) \tag{4.9}$$

in the noise bandwidth of Δf and g_m is the device trans-conductance at the operating point.

However, the overall circuit noise depends on the circuit configuration.

4.3.1 Input-Referred Noise of a Differential Input Stage

The differential input stage amplifier is shown in Fig. 4.1.

If the noise generated in the channel of each MOSFET is represented by a current source in parallel with the channel which can be represented by its equivalent input noise voltage generator as shown in Fig. 4.1, the equivalent input thermal noise voltage of the circuit, $\overline{V_{eqT}^2}$ at input (gate of M1) can be given by the following equation [Gray93].

$$\overline{V_{eqT}^2} = \overline{V_{eq1}^2} + \overline{V_{eq2}^2} + \left(\frac{g_{ml}}{g_{mi}} \right)^2 \cdot \left(\overline{V_{eq3}^2} + \overline{V_{eq4}^2} \right) \tag{4.10}$$

where $\overline{V_{eq1}^2}$, $\overline{V_{eq2}^2}$, $\overline{V_{eq3}^2}$, $\overline{V_{eq4}^2}$ are the noise sources at the gates of transistors M1, M2, M3 and M4. g_{mi} and g_{ml} are the transconductances of the input (M1 and M2) and load (M3 and M4) transistors, respectively, and are given by

$$g_{mi} = \sqrt{2 \cdot k_n \cdot \left(\frac{W_i}{L_i}\right) \cdot \left(\frac{I_o}{2}\right)}, \qquad \text{and}$$

$$g_{ml} = \sqrt{2 \cdot k_p \cdot \left(\frac{W_l}{L_l}\right) \cdot \left(\frac{I_o}{2}\right)}. \tag{4.11}$$

where $W_i, W_l, L_i,$ and L_l are the widths and lengths of input and load transistors respectively, k_n and k_p are the process trans-conductance parameters for n-channel and p-channel MOS transistors, and I_o is the tail current of the differential amplifier.

Using equations (4.9), (4.10) and (4.11), the Power Spectral Density (PSD) of noise voltage at the gate of M1 is written as

$$S_{VG}^2 = \frac{\overline{V_{eqT}^2}}{\Delta f} = 4kT \frac{4}{3\sqrt{2 \cdot k_n \cdot (W_i/L_i) \cdot (I_o/2)}} \cdot \left[1 + \sqrt{\frac{k_p \cdot (W_l/L_l)}{k_n \cdot (W_i/L_i)}}\right] \tag{4.12}$$

Therefore, root mean square value of spectral power density better known as input-referred noise is written as

$$IRN = IRN(th) = \sqrt{S_{VG}^2} = \sqrt{4kT \frac{4}{3\sqrt{2 \cdot k_n \cdot (W_i/L_i) \cdot (I_o/2)}} \cdot \left[1 + \sqrt{\frac{k_p \cdot (W_l/L_l)}{k_n \cdot (W_i/L_i)}}\right]} \tag{4.13}$$

4.4 Formulation of Figure of Merit

Unity-gain bandwidth of the circuit, UGB is given by

$$UGB = \frac{g_{mi}}{2 \cdot \pi \cdot C_L} = \frac{1}{2 \cdot \pi \cdot C_L} \sqrt{\frac{k_n \cdot W_i \cdot I_o}{L_i}} \tag{4.14}$$

where C_L is the total load capacitance at the output node.

And the differential dc gain, Ad of the differential input amplifier given by

$$Ad = \frac{g_{mi}}{g_{di} + g_{dl}} = 2 \cdot \sqrt{\frac{k_n}{I_o} \cdot \left(\frac{W_i}{L_i}\right)} \cdot \left(\frac{1}{L_i} \left(\frac{dx_d}{dV_{DS}} \right)_n + \frac{1}{L_l} \left(\frac{dx_d}{dV_{DS}} \right)_n \right)^{-1} \tag{4.15}$$

where g_{di} and g_{dl} are the drain conductances of input and load transistors, respectively. The drain conductance g_d is approximated as

$$g_d = \frac{I_o}{2.L} \cdot \left(\frac{dx_d}{dV_{DS}} \right) \tag{4.16}$$

where $\left(\frac{dx_d}{dV_{DS}} \right)$ (known as channel-length modulation parameter) is a process parameter [Gray92] and its value has been taken as 0.1 μm/V for nMOS and 0.05 μm/V for pMOS transistors for the 1.25 μm CMOS technology.

Substituting the values of UGB, Ad and IRN from equations (4.13), (4.14) and (4.15) in equations (4.1) and (4.2), we get

$$FoM\ 2 = \frac{\sqrt{3} I_o^{1/4} k_n^{7/4} (W_i L_i)^{7/4}}{4\pi (kT)^{1/2} C_L L_i^{3/2}} \cdot \left[\left(\frac{dx_d}{dV_{DS}} \right)_n + \frac{L_i}{L_l} \left(\frac{dx_d}{dV_{DS}} \right)_p \right]^{-1} \cdot \left(1 + \frac{L_i}{L_l} \cdot \sqrt{\frac{k_p W_l L_l}{k_n W_i L_i}} \right)^{-1/2} \tag{4.17}$$

$$FoM\ 3 = \frac{3\pi C_L k_n^{1/2} (W_i \cdot L_i)^{1/2}}{4kT\sqrt{I_o}} \cdot \left[\left(\frac{dx_d}{dV_{DS}} \right)_n + \frac{L_i}{L_l} \left(\frac{dx_d}{dV_{DS}} \right)_p \right]^{-1} \cdot \left(1 + \frac{L_i}{L_l} . \sqrt{\frac{k_p W_l L_l}{k_n W_i L_i}} \right)^{-1} \tag{4.18}$$

4.5 Maximization of Figure of Merit Under Area Constraints

If A is the total area available for the devices in the differential amplifier, let us assign fraction x of A *i.e.* $x \cdot A$ to the input transistors and $(1-x) \cdot A$ to load transistors. Then, writing the expressions for UGB, Ad and IRN in terms of x, area (A), bias current (I_o) and technology parameters, we get

$$A_d = 2. \sqrt{\frac{2 \cdot k_n \cdot (x \cdot A)}{I_o}} \cdot \left(\left(\frac{dx_d}{dV_{DS}} \right)_n + \frac{L_i}{L_l} \cdot \left(\frac{dx_d}{dV_{DS}} \right)_p \right)^{-1} \tag{4.19}$$

$$UGB = \frac{\sqrt{k_n . I_o \cdot (x \cdot A)}}{2\sqrt{2} . \pi \cdot C_L} \cdot \frac{1}{L_i} \tag{4.20}$$

$$IRN^2 = \frac{16.k.T}{3.\sqrt{k_n . (x.A) . I_o}} . \frac{1}{L_i} . \left(1 + \frac{L_i}{L_l} . \sqrt{\frac{k_p . (1-x) A}{k_n . (xA)}} \right) \tag{4.21}$$

$$IRN = \left[\frac{16.k.T}{3.\sqrt{k_n . (x.A) . I_o}} . \frac{1}{L_i} . \left(1 + \frac{L_i}{L_l} . \sqrt{\frac{k_p . (1-x) A}{k_n . (xA)}} \right) \right]^{1/2} \tag{4.22}$$

Hence, from equations (4.1), (4.2), (4.19), (4.20), (4.21) and (4.22) figure of merit $FoM\,2$ and $FoM\,3$, in terms of x, area (A), bias current (I_o) and technology parameters can be written as

$$FoM\ 2 = \frac{\sqrt{3} I_o^{1/4} k_n^{7/4} (xA)^{7/4}}{4\pi (kT)^{1/2} C_L L_i^{3/2}} \cdot \left(1 + \frac{L_i}{L_l} \cdot \sqrt{\frac{k_p (1-x) A}{k_n x A}}\right)^{-1/2} \cdot \left[\left(\frac{dx_d}{dV_{DS}}\right)_n + \frac{L_i}{L_l}\left(\frac{dx_d}{dV_{DS}}\right)_p\right]^{-1} \quad (4.23)$$

$$FoM\,3 = \frac{3\pi . C_L \cdot k_n^{1/2} \cdot (xA)^{1/2}}{4kT \cdot \sqrt{I_o}} \cdot \left(1 + \frac{L_i}{L_l} \cdot \sqrt{\frac{k_p . (1-x) A}{k_n . (xA)}}\right)^{-1} \cdot \left[\left(\frac{dx_d}{dV_{DS}}\right)_n + \frac{L_i}{L_l}\left(\frac{dx_d}{dV_{DS}}\right)_p\right]^{-1} \quad (4.24)$$

From equations (4.23) and (4.24), following conclusions can be drawn

- Figures of merits, $FoM\,2$ and $FoM\,3$ are dependent on technology parameters *i.e.* process transconductance parameters, k_n for n-channel transistor, k_p for p-channel transistor; and device channel length modulation parameters, $\left(\frac{dx_d}{dV_{DS}}\right)_n$ for n-channel transistor and $\left(\frac{dx_d}{dV_{DS}}\right)_p$ for p-channel transistor.
- To maximize $FoM\,2$ and $FoM\,3$ for a given load C_L, the length of input transistor L_i should be kept minimum for a given area (A), as it maximizes all the three product terms where it appears.
- Length of load transistor L_l should be as large as possible under the constraints of area since it maximizes the last two product terms and hence maximizes Figures of merits $FoM\,2$ and $FoM\,3$.
- Figures of merits are independent of the width of the load transistor, W_l and hence it should be kept at minimum.

- Figure of merit, $FoM2$ increases with the increase in the bias current whereas Figure of merit $FoM3$ decreases with the increase in the bias current.
- Figure of merit, $FoM2$ is a strong function of the area allocated to input transistors (xA), whereas Figure of merit, $FoM3$ is relatively a weaker function of the area allocated to input transistors (xA).

4.6 Analytical Results

The above analytical formulations have been used to draw the following curves.

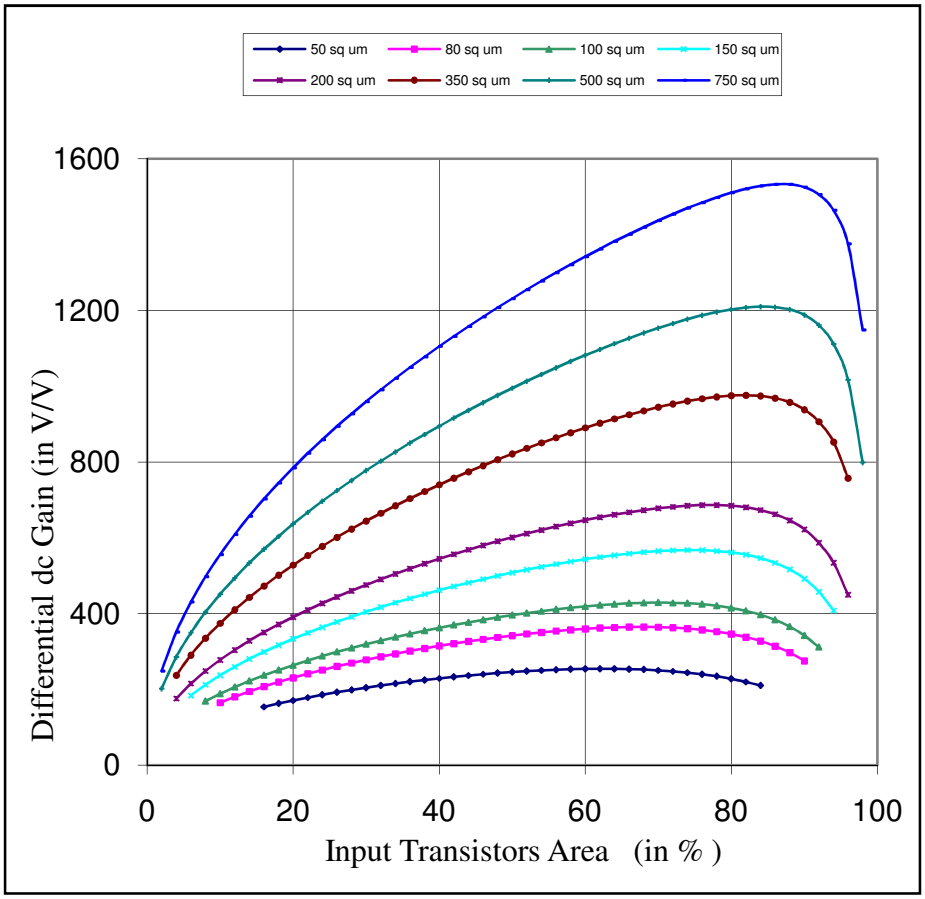


Figure 4.4 The differential dc voltage gain as a function of input transistor area.

The variation of differential dc voltage gain as a function of relative area allocated to input transistors (xA) at different values of total area, A is shown in Fig. 4.4. It is clear that it increases with increasing area allocation to input transistor and peaks at a certain value of x. Also, as the total area increases, the peak value of differential voltage gain increases. The peak value of voltage gain is obtained for x in the range of 0.64 to 0.86.

Fig. 4.5 shows that the unity-gain bandwidth is a monotonically increasing function of the relative area allocated to the input transistors x in percent.

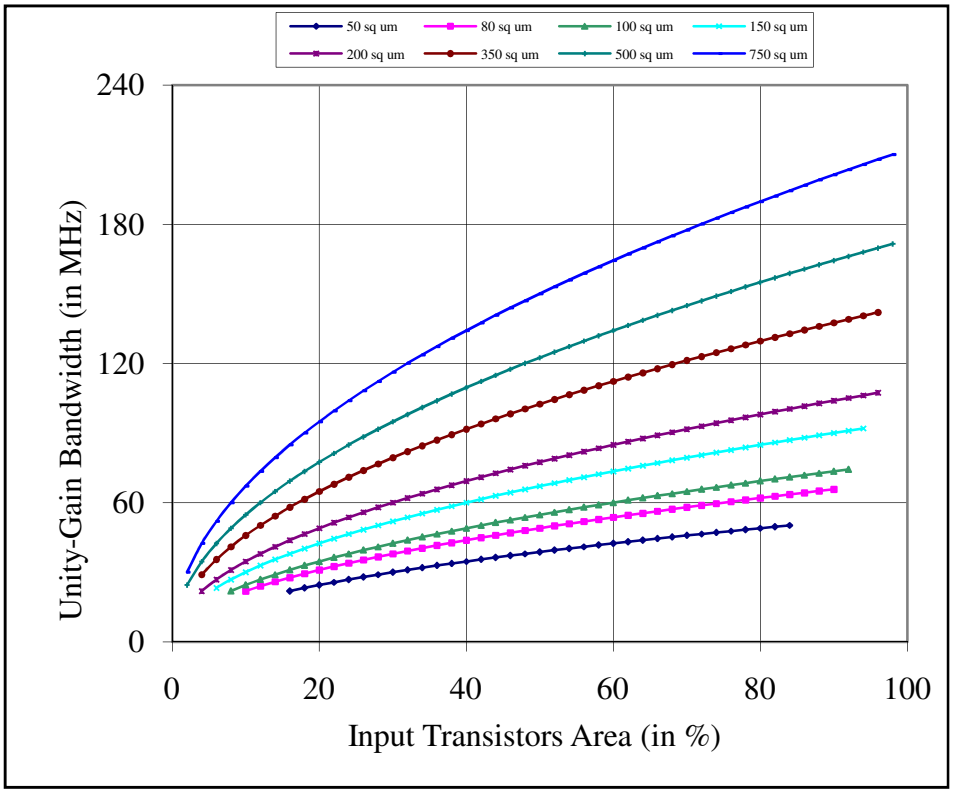


Figure 4.5 Unity-Gain Bandwidth (in MHz) as a function of input transistor area.

The variation of input-referred noise as a function of x is shown in Fig. 4.6. For larger values of x, the noise is reducing initially, because with increasing x the gate area of input transistors is increasing and their noise contribution is decreasing. But as the x increases beyond 0.4 the contribution of noise from load

transistors increases and starts dominating the noise contribution at the gate of transistor M1.

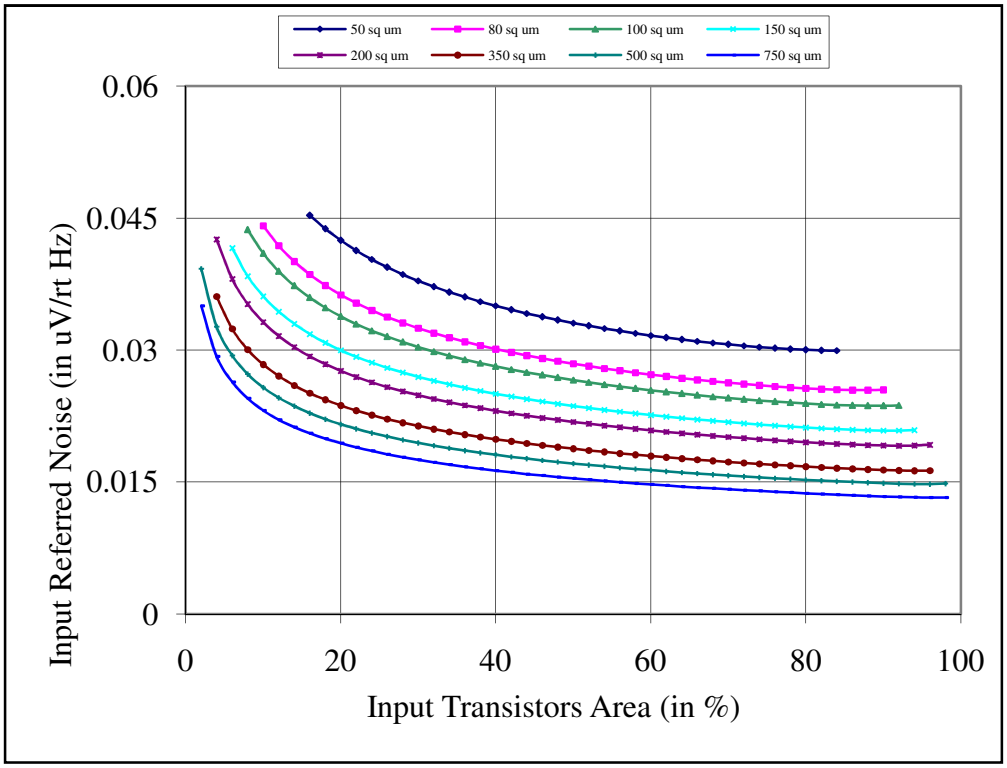


Figure 4.6 Input-Referred Noise (in nV/rtHz) as a function of input transistor area.

Fig. 4.7 shows the total band-noise *i.e.* the product of unity-gain bandwidth and input-referred thermal noise (mean square value) as a function of x for different values of A. It is clearly observed that it becomes almost constant for x greater than about 0.4 in all cases. It is interesting to note that the total band-noise does not change significantly with the total area A assigned to the circuit. It implies that by allocating more area to the input transistors, the unity-gain gain bandwidth of the circuit can be increased with reduced input referred noise such that the total band noise is almost the same.

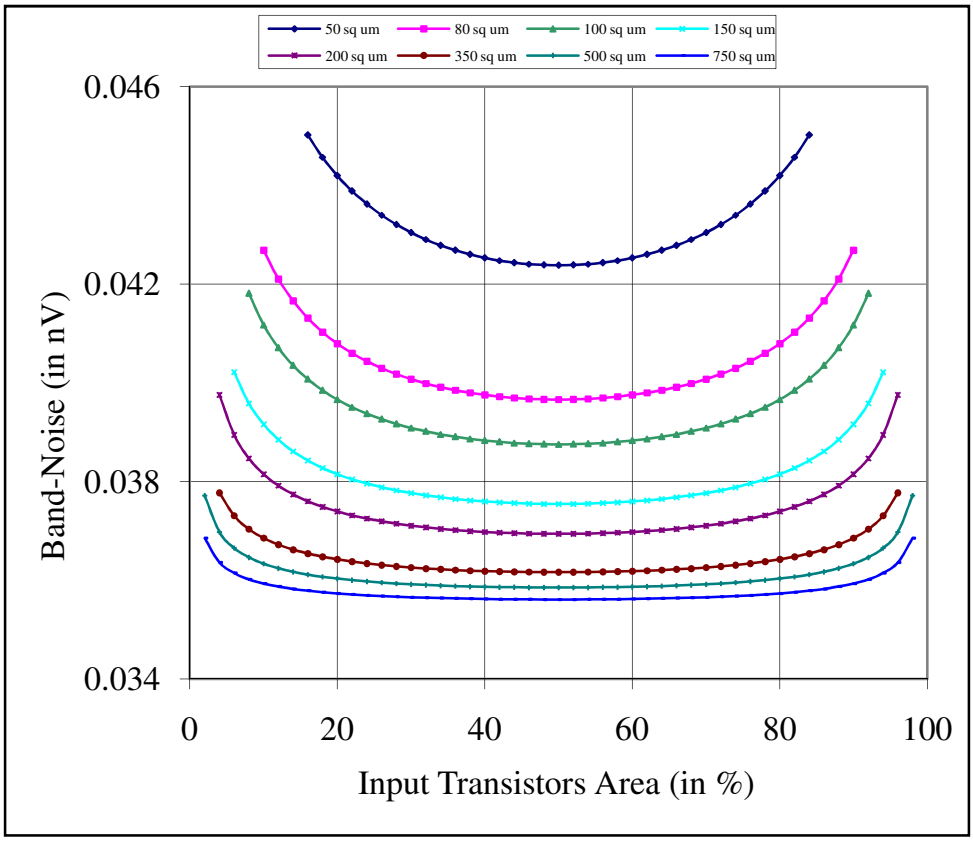


Figure 4.7 Total band-noise (in nV) as a function of input transistor area.

The figure of merit, $FoM2$ is plotted as a function of percentage area allocated to input transistors as shown in Fig. 4.8. It is a peaking function of x in the range 80% to 90%.

Next the figure of merit, $FoM3$ is plotted as a function of percent area allocated to input transistors. Figure of Merit, $FoM3$ is also a peaking function of x in the range 64% to 84% as shown in Fig. 4.9. The $FoM2$ is a much stronger function of x than $FoM3$. It is clear that both figures of merit increase with total area A. It also indicates that for a fixed value of total area, how much percentage of total area should be assigned to input transistors to obtain a maximum value of a figure of merit. Peak value of figure of merit, $FoM3$ as a function of total area is plotted in Fig. 4.10.

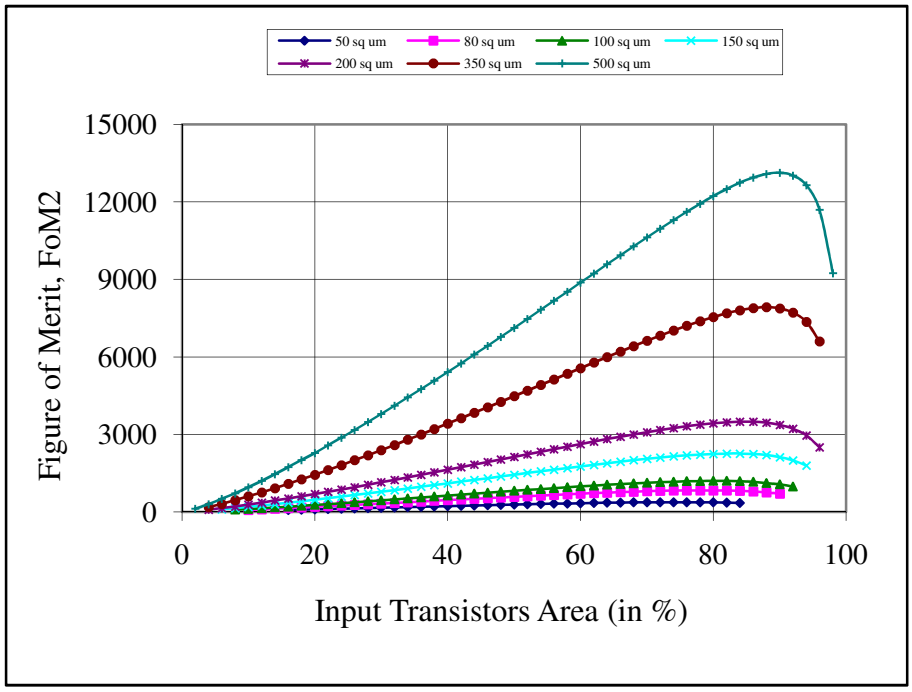


Figure 4.8 The $FoM2$ as a function of input transistor area.

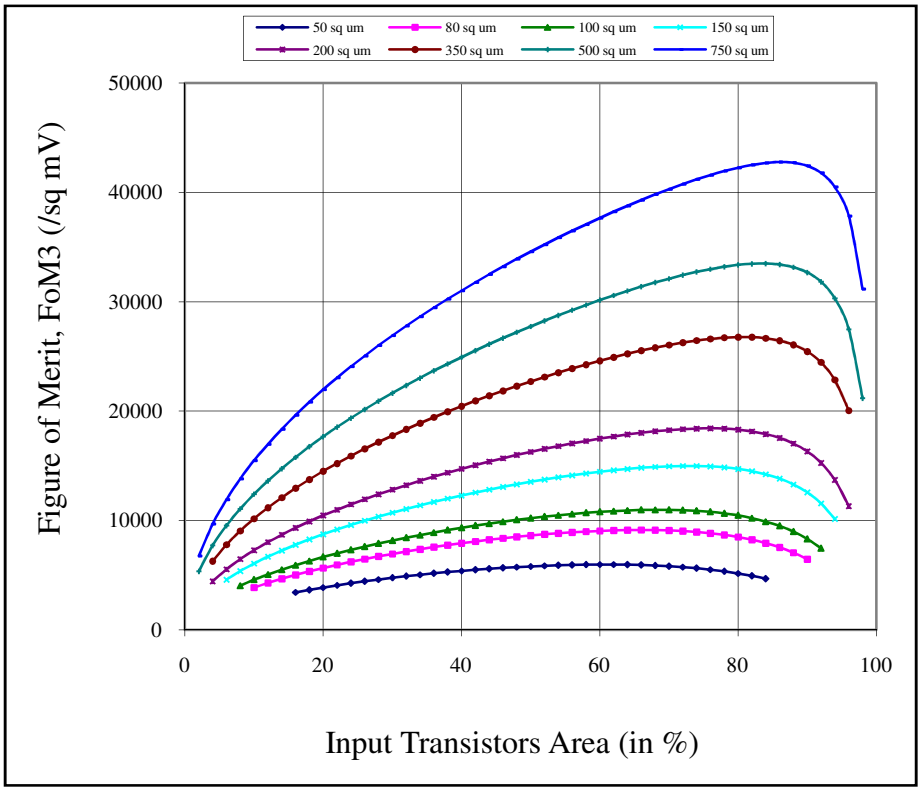


Figure 4.9 The $FoM3$ as a function of input transistor area.

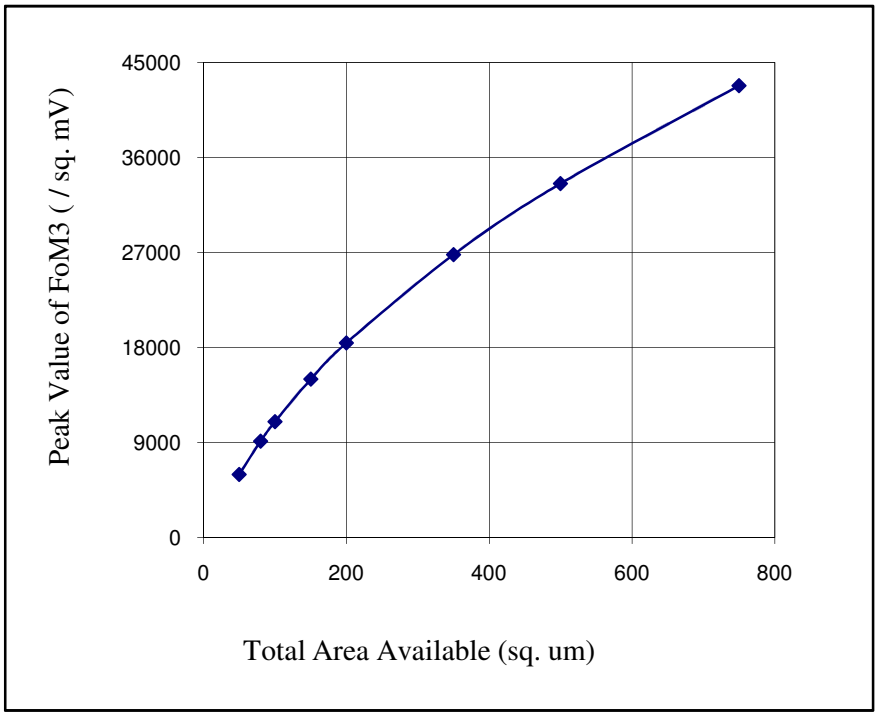


Figure 4.10 Peak value of $FoM3$ as as function of total area.

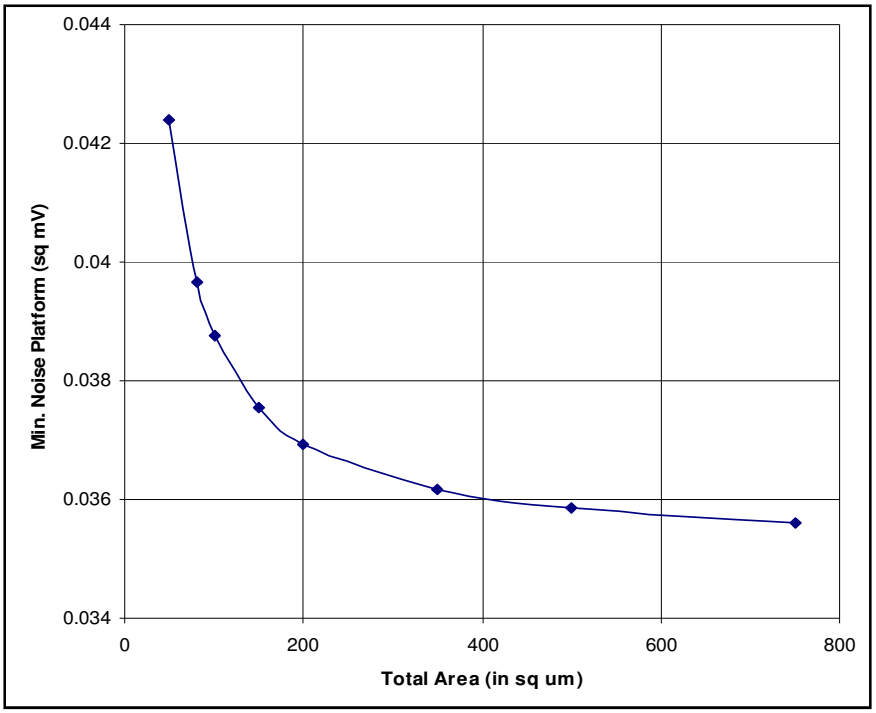


Figure 4.11 Minimum noise platform as a function of total area.

Fig. 4.11 indicates that for a fixed value of total area, there is a minimum value of band noise present in the circuit. It implies that if the total area of the circuit is reduced the noise platform may increase exponentially beyond a point. It is also clear that one cannot lower the noise platform beyond a limit, whatever large area is assigned to the circuit.

4.7 Simulation Results

Circuit simulations using SPICE, also validated the analytical results. To perform this task, a value of total area was chosen. The total area was divided between input and load transistors in a predefined ratio. Then for this distribution of areas a large number of combinations of aspect ratio of input and load transistors were simulated to obtain the differential dc voltage gain, unity-gain bandwidth and input-referred thermal noise.

The total band noise and the figures of merit, $FoM2$ and $FoM3$ were computed from these parameters. The total band-noise and figures of merit as a function of input transistor area in percent (ratio of area allocated to input transistors to the total available area, A) for various values of total area are plotted as shown in Figs. 4.12, 4.13 & 4.14, respectively. These plots match well with the analytical results shown in previous section.

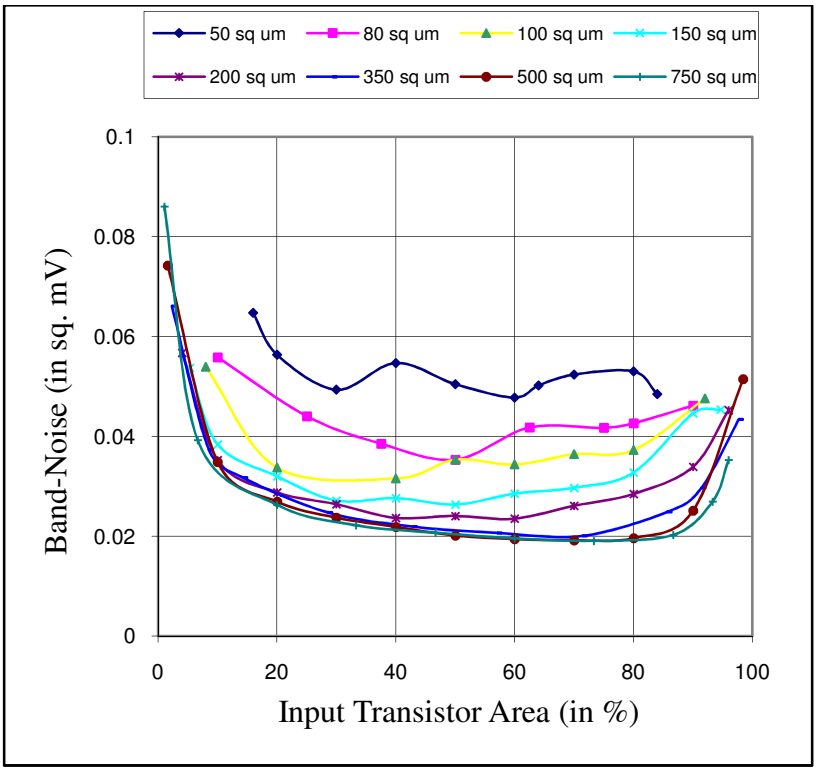


Figure 4.12 Simulated plot of total band-noise as a function of area.

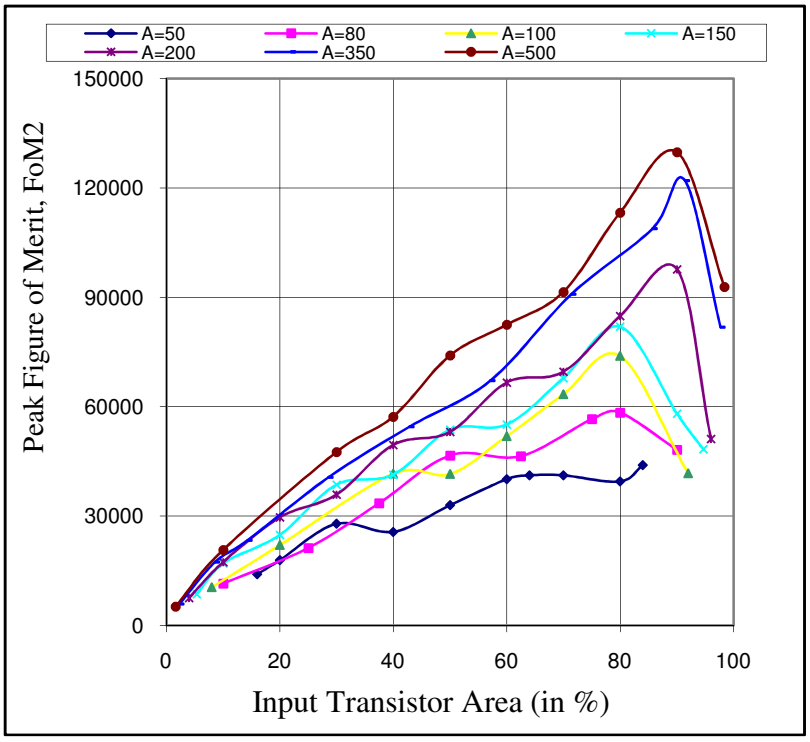


Figure 4.13 Simulated plot of figure of merit, $FoM2$ as a function of area.

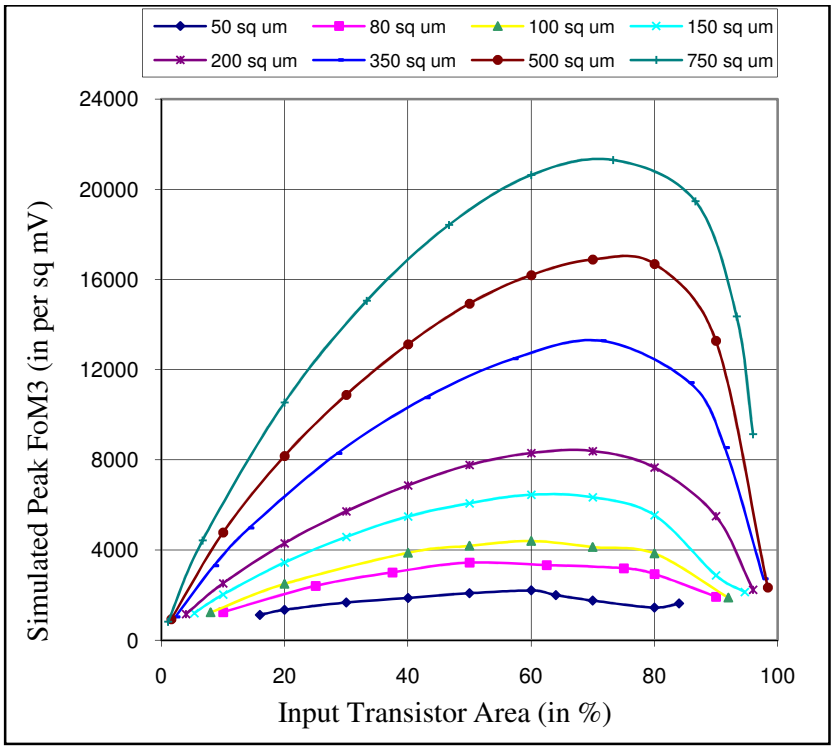


Figure 4.14 Simulated plot of figure of merit, $FoM3$ as a function of area.

In order to demonstrate the utility of figure of merit as a tool to optimize the design, we define $BN\%$ -- Band Noise obtained at the peak figure of merit as a percentage of minimum band-noise achievable for a given area in addition to previously defined parameters $Ad\%$, $UGB\%$ and $IRN\%$ (in chapter 3).

Table 4.1 compares the analytical and simulated values of peak figure of merit $FoM2$, $Ad\%$, $UGB\%$ and $IRN\%$ for constant area. Table 4.2 compares the analytical and simulated values of peak figure of merit, $FoM3$, $Ad\%$, $BN\%$ for constant area. The analytical and simulated values of voltage gain, unity-gain bandwidth and input-referred noise at the respective peak values of figure of merit are close to the best achievable values at that area.

This validates that the proposed methodology can be deployed in CAD tools for the automatic synthesis of optimal circuit of differential amplifier under the constraint of area.

Table 4.1 Comparison Between Analytical and Simulated Performance at Peak Figure of Merit, $FoM2$.

Area (μm^2)	Peak Figure of Merit, FoM2		Ad%		UGB%		IRN%	
	Analytical	Simulated	Analytical	Simulated	Analytical	Simulated	Analytical	Simulated
50	380	44036	96.1	100	93.86	100	101.34	100
80	838	58404	96.64	100	93.1	96.38	101.57	100
100	1202	73893	96.72	96.87	93.25	91.62	101.1	100
150	2263	81954	97.86	94.74	93.4	86.3	101.2	100
200	3496	97730	98.11	99.94	93.55	89.95	101.15	100
350	7924	121967	98.07	99.2	95.74	80.54	100.86	100
500	13131	129797	98.16	93.84	95.83	71.78	102.31	100.57
750	23033	181063	98.21	100	96.89	59.7	100.59	100

Table 4.2 Comparison Between Analytical and Simulated Performance at Peak Figure of Merit, $FoM3$.

Area (μm^2)	Peak Figure of Merit, FoM3 (per sq. mV)		Ad%		BN%	
	Analytical	Simulated	Analytical	Simulated	Analytical	Simulated
50	5973.92	2202	99.84	95.69	100.31	100
80	9136.22	3438.2	99.92	77.93	100.63	100
100	10981.2	4397.7	99.88	83.5	100.67	100
150	14990.2	6454.6	99.85	79.97	100.71	100
200	18423.9	8385.4	99.99	82.72	100.84	100
350	26776.3	13279	99.9	83.51	100.72	115.3
500	33501.5	16885	100	87.45	100.74	120.7
750	42781.4	21303	100	87.0	100.60	116.7

Chapter 5

Area-Constrained Design of Second Stage

5.1 Introduction

Operational amplifiers are basic building blocks of analog electronic circuitry. Typically on-chip operational amplifiers are two-stage amplifiers that include an input stage and a second gain stage (which also serves as the output stage). The input stage is designed to receive a differential input signal and provide an amplified single-ended intermediary signal at its output node. The second gain stage is designed to receive the amplified single-ended intermediary signal produced at the output of the input stage and further amplify it by a large gain factor.

5.2 Two Stage Operational Amplifier Design

A common circuit of CMOS operational amplifier for on-chip use along with its biasing circuitry is depicted in Fig. 5.1.

This structure has received considerable attention in the literature [Solomon74, Gray82] as well as in textbooks focusing on linear circuit design. It can provide modest performance, especially if the application is on-chip or driving light off-chip loads. It is comprised of four subsections [Wilson68], examining the subsections further will provide valuable insight into the operation of this amplifier.

The first subsection of interest is the differential gain stage, which is comprised of transistors M1 through M4. Transistors M1 and M2 are standard nMOS transistors, which form the basic input stage of the amplifier. The gate of M1 is the inverting input and the gate of M2 is the non-inverting input. A differential input signal applied across the two input terminals will be amplified according to the gain of the differential stage. The design of this stage under the constraints of area was the subject of the previous two chapters.

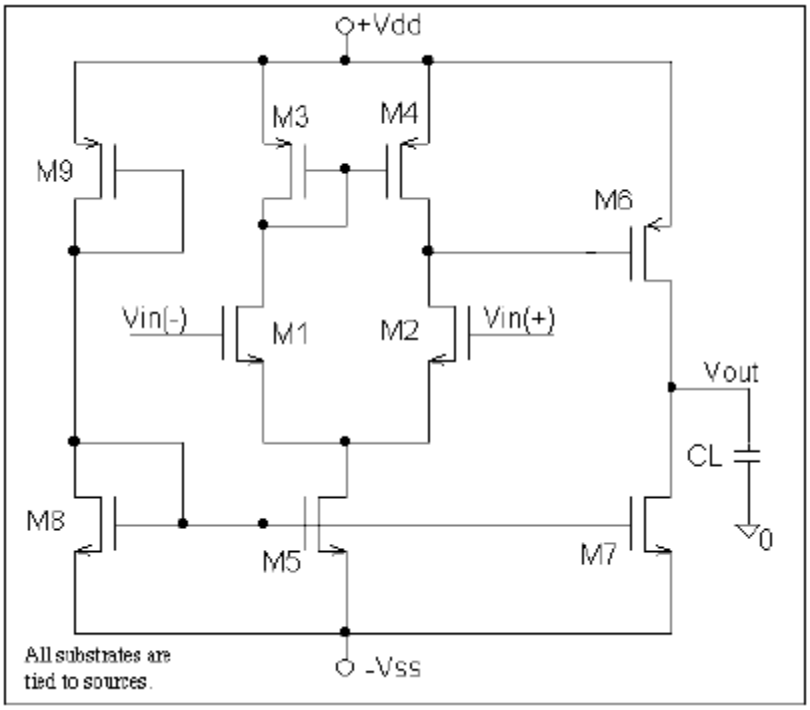


Figure 5.1 Two-stage operational amplifier.

5.3 Second Gain Stage

The purpose of the second gain stage, as the name implies, is to provide additional gain in the amplifier. Consisting of transistors M6 and M7, this stage takes the output from the drain of M2 and amplifies it through M6, which is in the standard common source configuration. Again, similar to the differential gain stage, this stage employs an active device, M7, to serve as the load resistance for M6. The

overall voltage gain of the op-amp is a function of the voltage gains of the two stages.

The biasing of the operational amplifier is achieved with only four transistors. Transistors M8 and M9 form a simple current mirror bias string that supplies a voltage between the gate and source of M5 and M7. Using the equations for current in a MOS transistor and the fact that current scaling can be achieved in MOS transistors by choosing appropriate width to length ratios, transistors M5 and M7 sink a certain amount of current based on their gate to source voltage, which is controlled by the bias string. M8 and M9 are diode connected to ensure they operate in the saturation region.

Proper biasing of the other transistors (M1 – M4, M6) in the circuit is controlled by the node voltages present in the circuit itself. Most importantly, M6 is biased by the gate to source voltage (V_{GS}) set up by the V_{GS} of the current mirror load as are the transistors M1 and M2.

5.4 Figure of Merit

To compare different solutions for the second stage, we need to define a figure of merit ($FoM\,4$) for this stage which can then be used to design the circuit with maximal figure of merit under the constraints of area. Here, a figure of merit has been proposed that takes into account the key small signal performance parameters *i.e.* the differential dc gain and unity-gain bandwidth. The noise generated in the second stage contributes much less to the overall noise of the operational amplifier, and is therefore dropped from inclusion in the definition of figure of merit for the second stage.

Thus, the proposed figure of merit ($FoM\,4$) for the second stage is given by

$$FoM\,4 = UGB_2 * A_V \tag{5.1}$$

where UGB_2 is the unity-gain bandwidth and A_V is the dc voltage gain of the second stage.

5.4.1 dc Voltage Gain

The dc voltage gain of this stage is the trans-conductance of M6, $g_{m6} = g_{mp}$ times the effective load resistance comprised of the output resistances of M5 and M6, $(g_{d6} + g_{d7})^{-1} = (g_{dp} + g_{dn})^{-1}$. The dc voltage gain in the second stage can be written as:

$$A_V = -\frac{g_{m6}}{g_{d6} + g_{d7}} = \frac{-g_{mp}}{g_{dp} + g_{dn}} \tag{5.2}$$

where $g_{d6} = g_{dp}$ and $g_{d7} = g_{dn}$ are the drain conductances of input and load transistors respectively.

The drain conductance g_d is approximated as given in equation (3.9) and reproduced below

$$g_d = \frac{I}{L} \cdot \left(\frac{dx_d}{dV_{DS}} \right) \tag{5.3}$$

5.4.2 Unity-Gain Bandwidth

Unity-gain bandwidth of the second stage, UGB_2 is given by

$$UGB_2 = \frac{g_{mp}}{2\pi \cdot C_L} = \frac{1}{2\pi \cdot C_L} \sqrt{\frac{k_p \cdot W_p \cdot I_p}{L_p}} \tag{5.4}$$

Where C_L is the total load capacitance at the output of the second stage.

5.4.3 Formulation of Figure of Merit

Substituting the values of UGB_2 and A_V from equations (5.2), (5.3) and (5.4) in equation (5.1), we get

$$FoM\,4 = \frac{k_p}{\pi \cdot C_L} \cdot \left(\frac{W}{L}\right)_p \cdot \left(\frac{1}{L_p} \cdot \left(\frac{dx_d}{dV_{DS}}\right)_p + \frac{1}{L_n} \cdot \left(\frac{dx_d}{dV_{DS}}\right)_n\right)^{-1} \tag{5.5}$$

Substituting the values of $\left(\frac{dx_d}{dV_{DS}}\right)$ for nMOS and pMOS transistors as in earlier chapters, we get

$$FoM\,4 = \frac{20 \cdot k_p \cdot W_p}{\pi \cdot C_L} \cdot \left(1 + \frac{2.L_p}{L_n}\right)^{-1} \tag{5.6}$$

5.5 Maximization of Figure of Merit Under Area Constraints

Again, as in earlier chapters, area has been taken as the first constraint and the expression for figure of merit has been maximized under that constraint through relative area allocations between the input and load transistors.

If A is the total area available for the input and load devices in the second stage, let us assign a fraction x of A *i.e.* $(x \cdot A)$ to the input transistor and $(1-x) \cdot A$ to load transistor. Then, writing the expressions for magnitude of A_V and UGB_2 in terms of x, area (A), bias current (I_p) and technology parameters, we get

$$A_V = 10 \cdot \sqrt{\frac{2 \cdot k_p \cdot (x \cdot A)}{I_p}} \cdot \left(\frac{1}{2} + \frac{L_p}{L_n}\right)^{-1} \tag{5.7}$$

$$UGB_2 = \frac{\sqrt{k_p.I_p \cdot (x \cdot A)}}{\sqrt{2}.\pi \cdot C_L} \cdot \frac{1}{L_p} \tag{5.8}$$

Hence, from equations (5.1), (5.7) and (5.8) figure of merit ($FoM\,4$) in terms of x, area (A), bias current (I_p) and technology parameters is written as

$$FoM\,4 = \frac{20 \cdot k_p \cdot (x \cdot A)}{\pi \cdot C_L} \cdot \left(\frac{1}{L_p}\right) \cdot \left(1 + \frac{2.L_p}{L_n}\right)^{-1} \tag{5.9}$$

From equation (5.9), following conclusions can be drawn

- Figure of Merit, $FoM\,4$ is dependent on technology parameter, k_p.
- It is inversely proportional to the total load at output node, C_L.
- To maximize $FoM\,4$, Length of input transistor L_p should be kept minimum for a given area A. As that choice maximizes the second product term in equation (5.9) above and hence maximizes Figure of Merit ($FoM\,4$).
- $FoM\,4$ is independent of the width of load transistor (W_n), hence it should be kept as minimum.
- Length of load transistor (L_n) should be as large as possible under the constraints of area since it maximizes the last product term and hence maximizes Figure of Merit ($FoM\,4$).

5.6 Analytical Results

Fig. 5.2 shows the variation of magnitude of dc voltage gain of the second stage as a function of relative area allocated to input transistors at different values of

total area. It is clear that as the total area increases, the voltage gain increases. But, it does not keep on increasing with increase in input transistor area. The peak value of dc voltage gain is obtained for x in the range of 0.68 to 0.86. Fig. 5.3 shows that the unity-gain bandwidth is a monotonically increasing function of x.

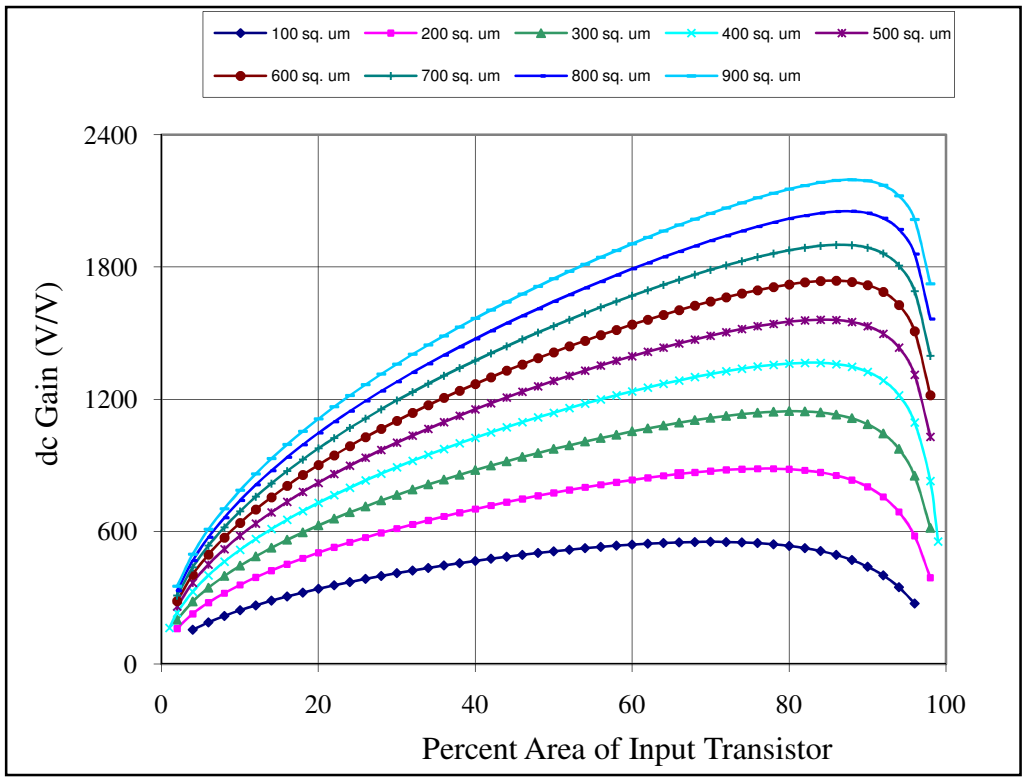


Figure 5.2 The voltage gain as a function of input transistor area.

Next the figure of merit is plotted as a function of percent area allocated to input transistors. Figure of Merit is a peaking function of x in the domain of 76% to 92% as shown in Fig. 5.4. It is clear that figure of merit increases with total area (A).

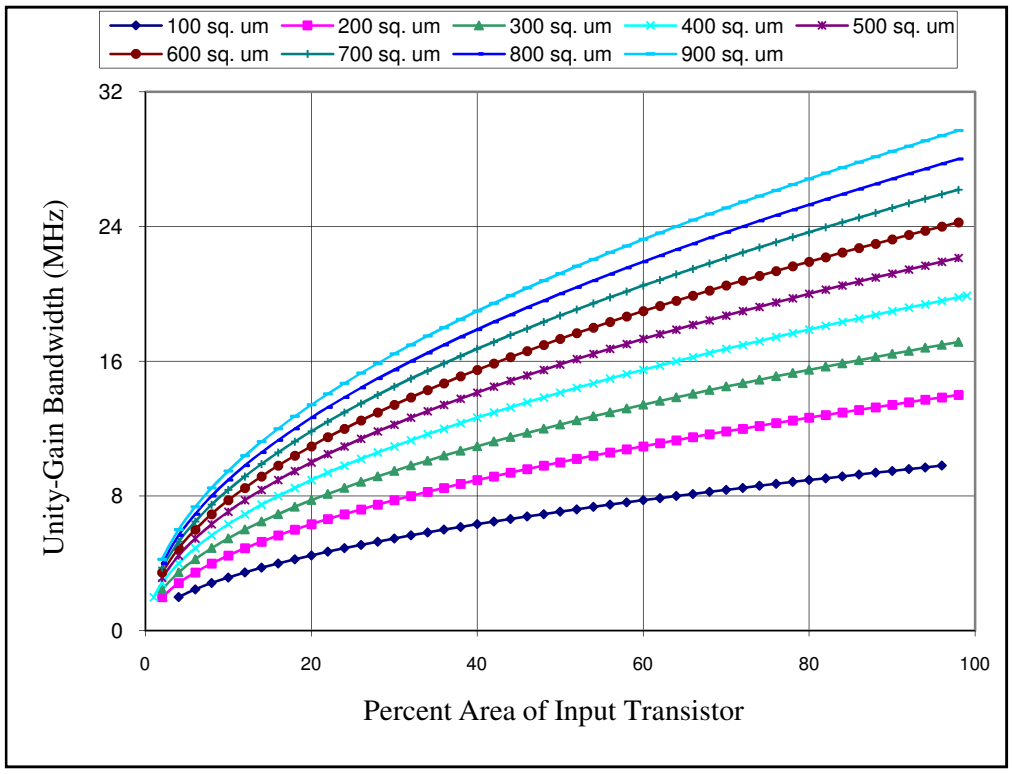


Figure 5.3 Unity-Gain Bandwidth (in MHz) as a function of input transistor area.

It also indicates that for a fixed value of total area, what percentage of total area should be assigned to input transistors to obtain a maximum value of figure of merit. Equation (5.9) indicates that the figure of merit (FoM 4) is also a function of total area. Peak value of figure of merit as a function of total area is plotted in Fig. 5.5. The value of figure of merit is independent of bias current (I_p). However, a minimum value of power is essential to keep the transistors in saturation and to achieve a respectable slew rate.

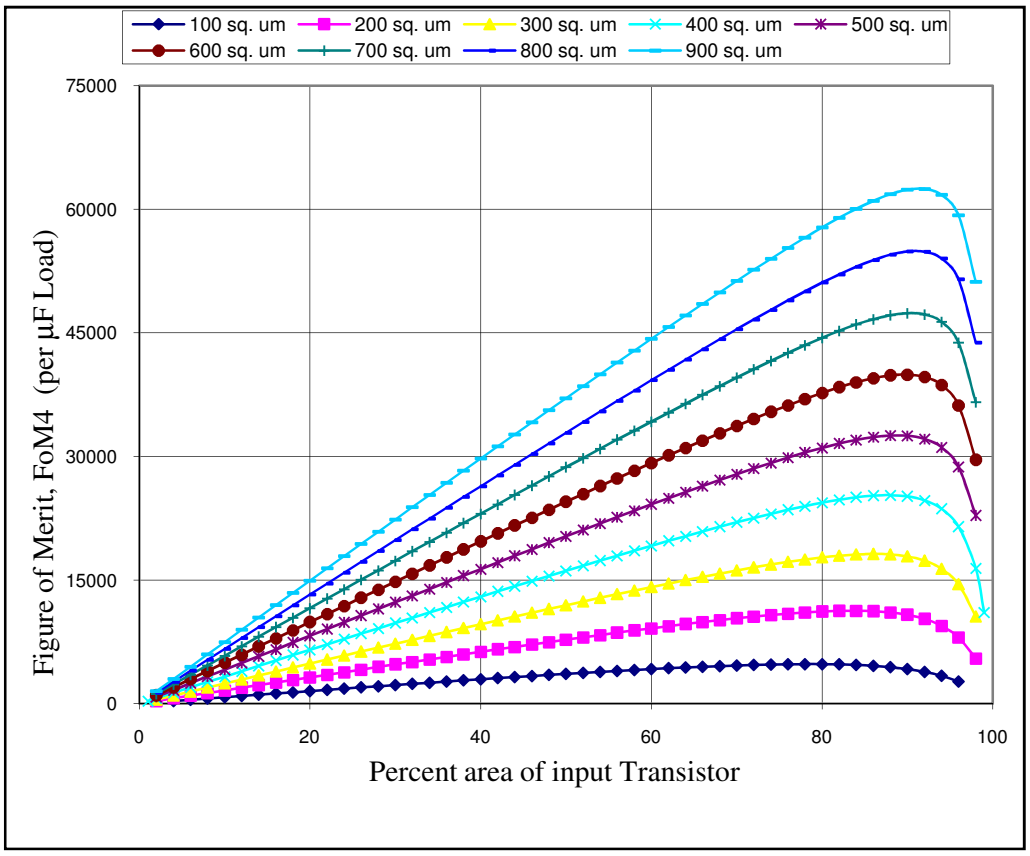


Figure 5.4 The figure of merit, $FoM4$ as a function of input transistor area.

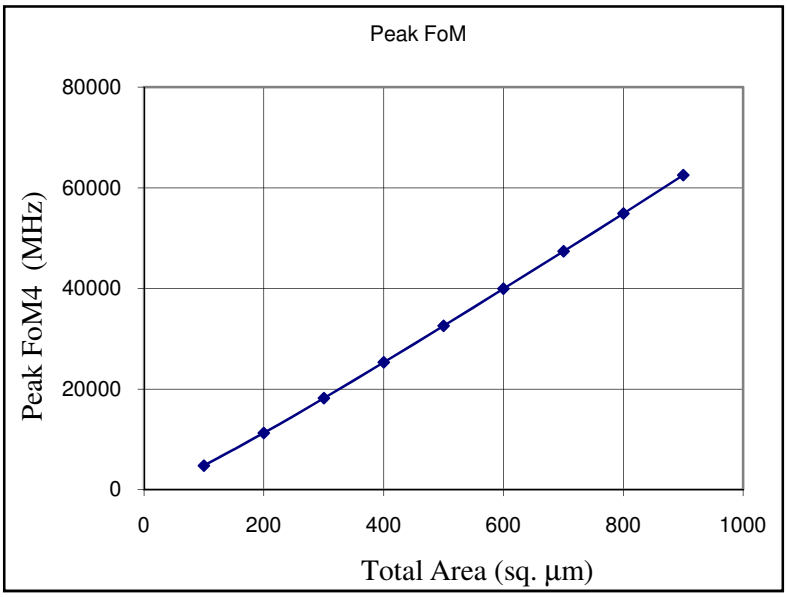


Figure 5.5 Peak value of figure of merit (FoM 4) as a function of area.

5.7 Simulation Results

Simulations using SPICE in Tanner Tools Pro, have also validated the analytical results. To perform this task, a value of total area was chosen. The total area was divided between input and load transistors in a predefined ratio. Then for this distribution of areas all combinations of aspect ratio of input and load transistors were simulated to obtain the dc voltage gain and unity-gain bandwidth. The figure of merit was computed from these parameters. The second stage dc gain, unity-gain bandwidth and peak figure of merit as a function of input transistor area in percent of total available area for the second stage transistors for various values of total area are plotted at a power of 15 μW as shown in Figs. 5.6, 5.7 and 5.8 respectively.

The variations in dc voltage gain, unity-gain bandwidth and $FoM4$ were also studied with varying power for a given fixed area. The Figs. 5.9, 5.10 and 5.11 show the simulated plots for voltage gain, unity-gain bandwidth and $FoM4$ with different power values for a fixed area of 300 sq. μm.

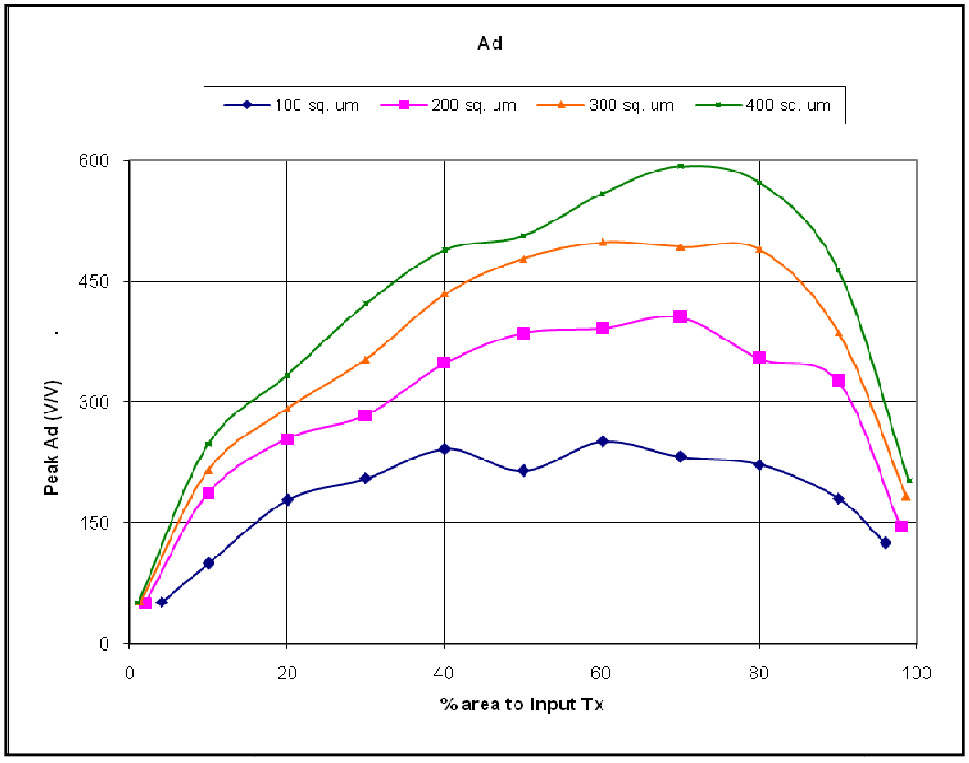


Figure 5.6 Simulated plot of dc voltage gain as a function of input transistor area.

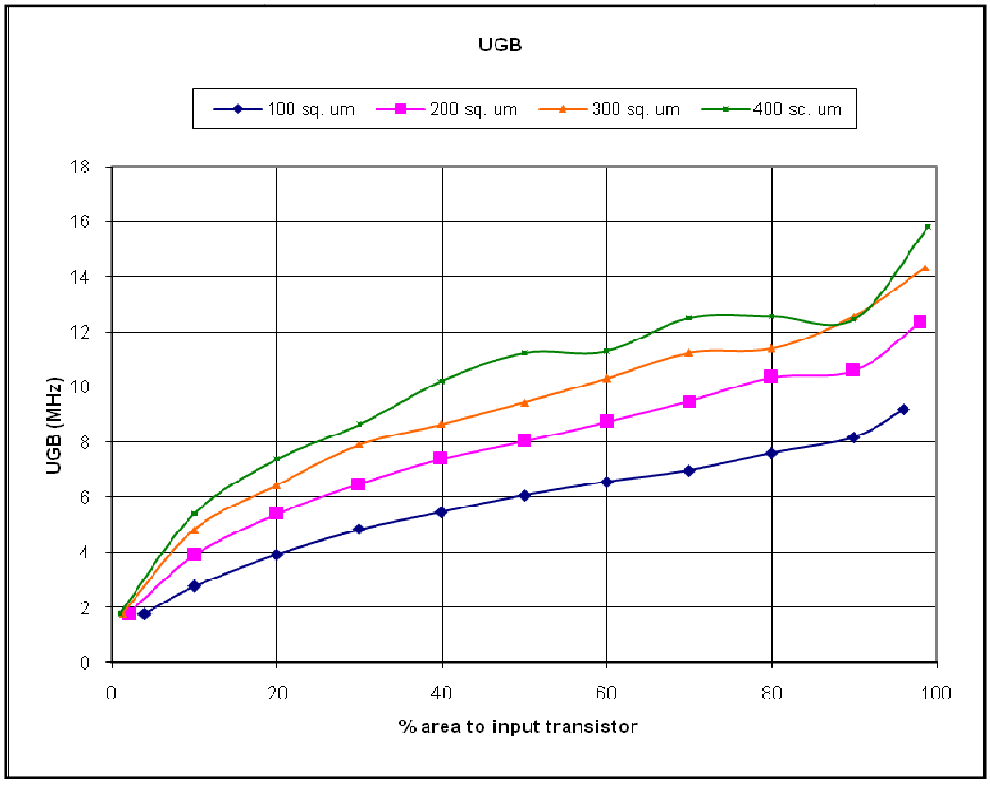


Figure 5.7 Simulated plot of Unity-Gain Bandwidth as a function of input transistor area.

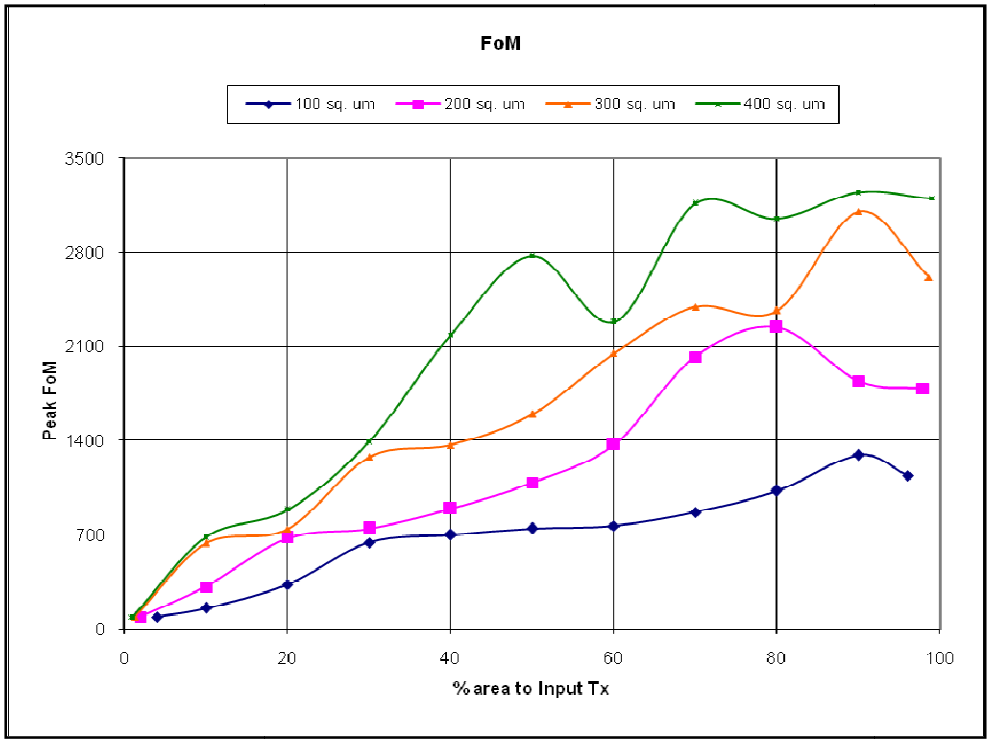


Figure 5.8 Simulated plot of figure of merit (FoM 4) as a function of input transistor area.

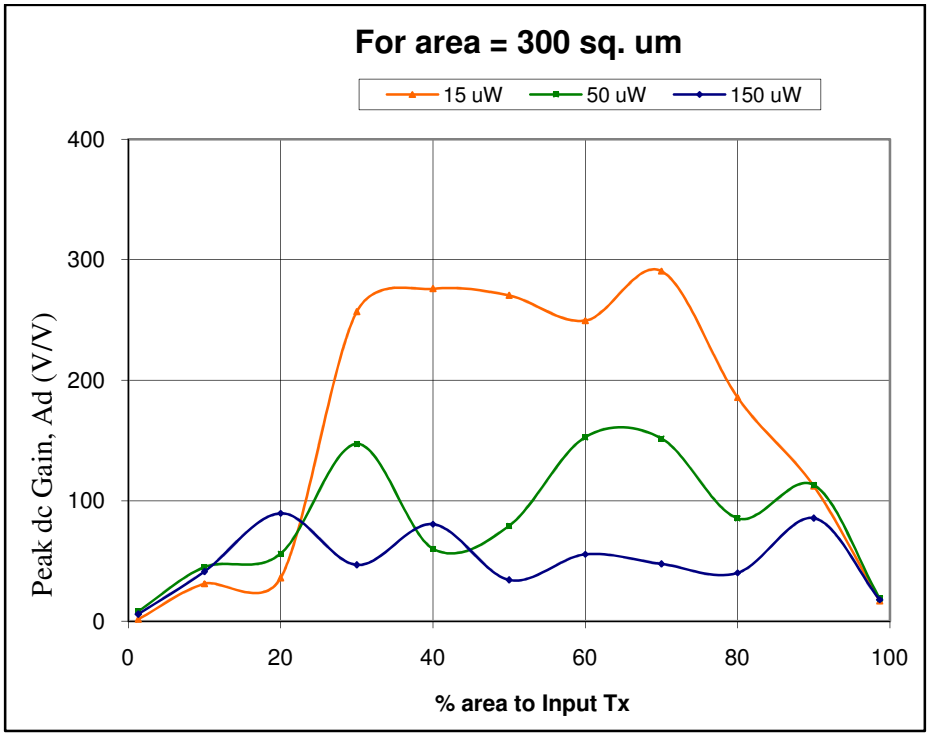


Figure 5.9 Simulated plot of dc gain as a function of input transistor area.

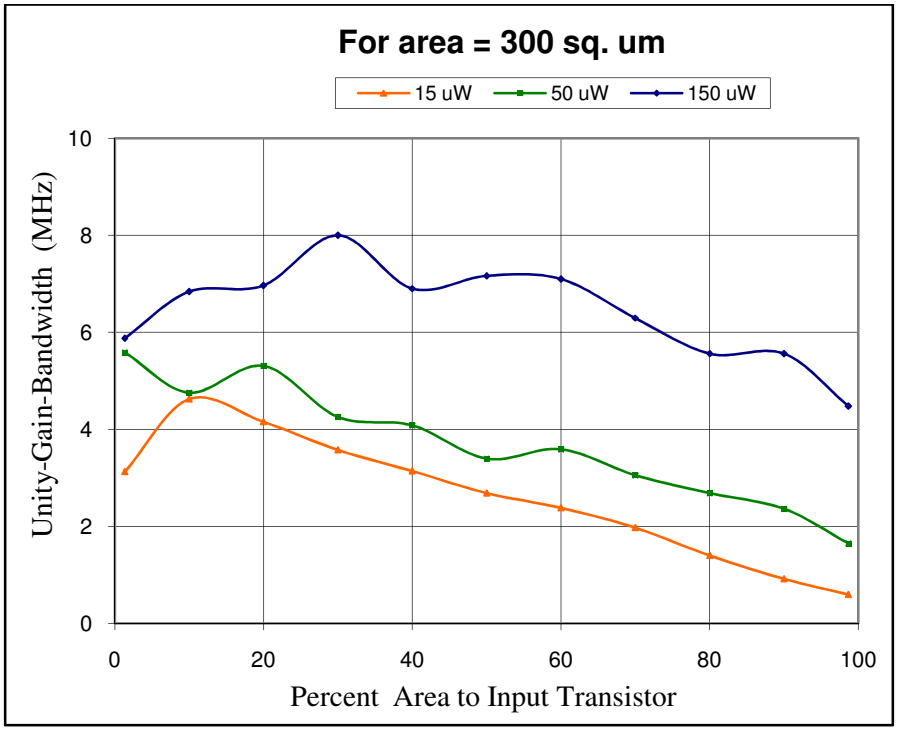


Figure 5.10 Simulated plot of Unity-Gain Bandwidth as a function of input transistor area.

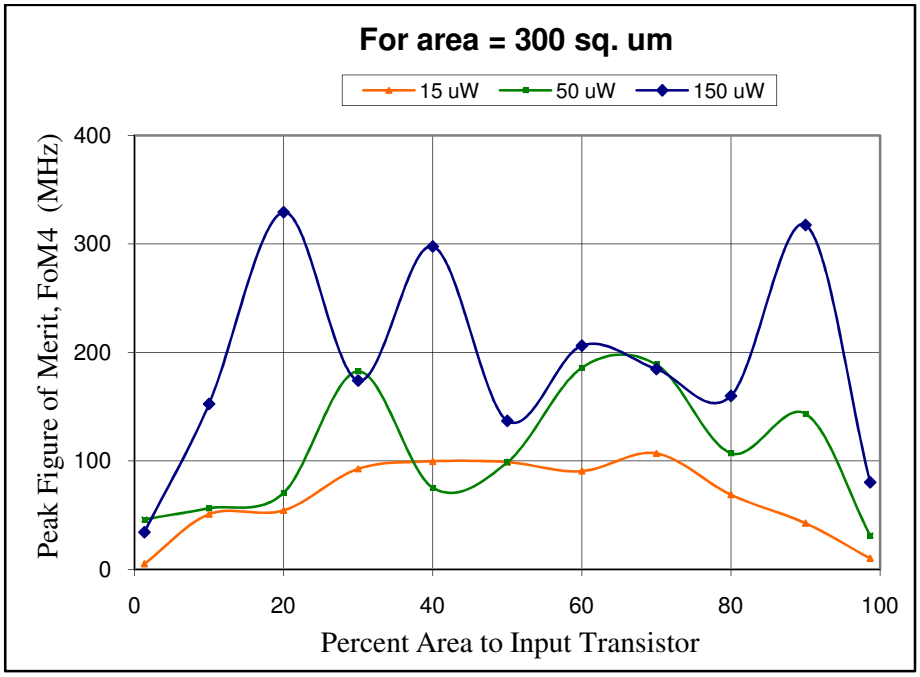


Fig. 5.11. Simulated plot of figure of merit, $FoM4$ as a function of input transistor area.

Chapter 6

A CAD Tool for the Optimal Synthesis of Input Stage Differential Amplifier

6.1 Introduction

The rapid progress of design automation for digital integrated circuits (ICs) has enabled rapid synthesis of digital designs. Analog circuit design methodologies have not kept up with this pace. Although the circuit design software used by today's analog IC design engineers is more user friendly, and converges to solutions better than fifteen years ago, there has not been a parallel explosion of design capability for analog circuit designers. Today's analog circuit designers often use a combination of hand analysis and circuit simulation that was widely available in 1980. There has been some improvement in efficiency and capability since that time, due to the development of improved user interfaces for software tools, and new capabilities for behavioral, high level, and mixed signal simulation, but the task of circuit design is still reserved for experienced circuit designers using manual design and layout.

The general goal of Analog Computer Aided Design (ACAD) is to reduce the manual design and layout time required for circuit design. Improving analytical tools is a first step, and creating in-house cell libraries from previous designs is a low-tech way to speed circuit development through design re-use, but more aggressive techniques which result in design information reuse and automated design synthesis offer greater promise for reducing design time.

Analog circuit synthesis is a process in which design specifications such as amplification, bandwidth, *etc*. are used as inputs, to select appropriate circuit topologies, size devices and set the device biases. This process is not a one-to-one mapping, but usually is an under-constrained problem with many degrees of freedom. Also, since the process technology is just an input to the synthesis process, changing technology is no more complicated than changing the specifications. In either case the synthesis tool will create the best design for the input specifications.

In the present thesis, a CAD tool has been developed for the circuit synthesis of an optimal differential input stage operating in mid-frequency ranges, for the given maximum power budget, minimum differential voltage gain, minimum unity-gain bandwidth and a maximum input-referred noise. The circuit topology chosen is the same as shown in Fig. 4.1. The tool uses the methodology as described in the following section.

6.2 Implementation Methodology

From the given specifications in terms of maximum power budget, minimum differential voltage gain, minimum unity-gain bandwidth and maximum input-referred noise, we proceed as follows:

We know,

i) Unity-Gain Bandwidth of the differential input stage is given by

$$UGB = \frac{g_{mi}}{2\pi C_L}. \tag{6.1}$$

ii) Input-Referred Noise of the differential input stage at the gate of the input transistor is given by

$$IRN = \left[\frac{16}{3}\frac{kT}{g_{mi}}\left(1+\frac{g_{ml}}{g_{mi}}\right)\right]^{1/2} \tag{6.2}$$

ignoring flicker noise as thermal noise dominates the flicker noise in mid/moderate frequency ranges.

iii) Differential Voltage Gain of the differential input stage is written as

$$Ad = \frac{g_{mi}}{g_{di} + g_{dl}} \tag{6.3}$$

Substituting the expressions for g_{mi}, g_{di} and g_{dl} from equations (3.4) and (3.9), we get

$$\begin{aligned} Ad &= \frac{\sqrt{k_n \left(\frac{W}{L}\right)_i I_{ref}}}{\frac{I_{ref}}{2}\left[\frac{1}{L_i}\left(\frac{dx_d}{dV_{DS}}\right)_n + \frac{1}{L_l}\left(\frac{dx_d}{dV_{DS}}\right)_p\right]} \\ &= \frac{2\sqrt{\frac{k_n}{L_i}}}{\left[\frac{1}{L_i}\left(\frac{dx_d}{dV_{DS}}\right)_n + \frac{1}{L_l}\left(\frac{dx_d}{dV_{DS}}\right)_p\right]} \frac{\sqrt{W_i}}{\sqrt{I_{ref}}} \end{aligned} \tag{6.4}$$

Let us choose the minimum permissible channel lengths for input and load transistors. Other parameters k_n, $\left(\frac{dx_d}{dV_{DS}}\right)_n$ and $\left(\frac{dx_d}{dV_{DS}}\right)_n$ being the technology parameters, Ad can be rewritten as

$$Ad = G \cdot \frac{\sqrt{W_i}}{\sqrt{I_{ref}}} \tag{6.5}$$

Where G is the technology constant given by

$$G = \frac{2\sqrt{\frac{k_n}{L_i}}}{\left[\frac{1}{L_i}\left(\frac{dx_d}{dV_{DS}}\right)_n + \frac{1}{L_l}\left(\frac{dx_d}{dV_{DS}}\right)_p\right]} \tag{6.6}$$

where L_i and L_l are the minimum permissible channel lengths for the input and load devices.

After rearranging the equation, we can write

$$\sqrt{I_{ref}} = \frac{G}{Ad}\sqrt{W_i} \tag{6.7}$$

If we plot the graph between $\sqrt{I_{ref}}$ and $\sqrt{W_i}$ for different values of Ad it is as shown in Fig. 6.1. As the Ad increases, the slope of the line reduces. For a given value of Ad, there are infinite solutions possible in the $\sqrt{I_{ref}}$ and $\sqrt{W_i}$ space. For a the given maximum power budget, the maximum value of I_{ref} hence $\sqrt{I_{ref}}$ gets frozen which decides the minimum value of $\sqrt{W_i}$ from the constant Ad line (point A on Fig. 6.1).

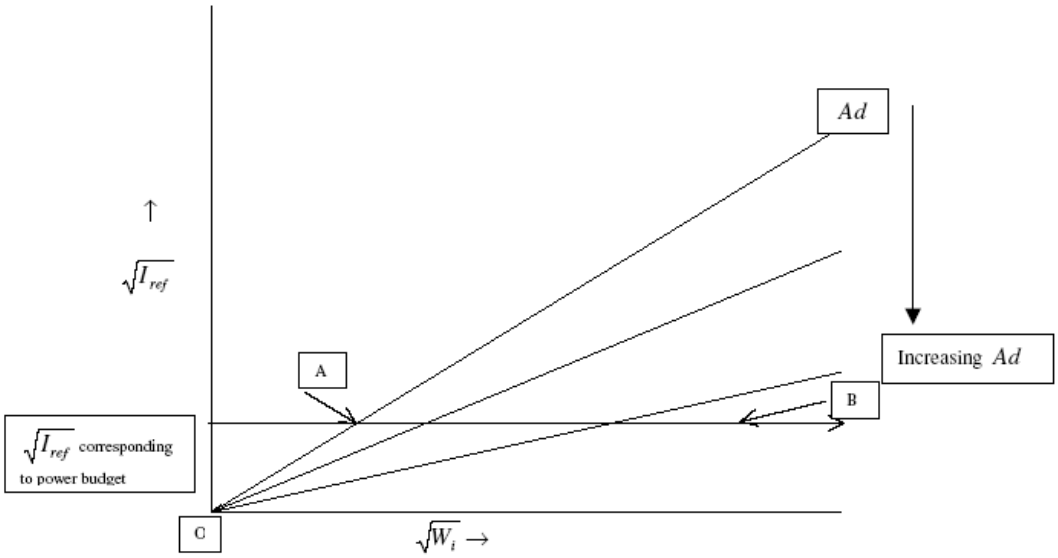


Figure 6.1 Variation of $\sqrt{I_{ref}}$ vs. $\sqrt{W_i}$ with Ad (differential dc voltage gain) as parameter.

iv) From these values of $\sqrt{I_{ref}}$ and $\sqrt{W_i}$, we can calculate a value of g_{mi}, as it is given by

$$g_{mi} = \sqrt{2\frac{k_n}{L_i}}\sqrt{W_i}\sqrt{I_{ref}}\,. \tag{6.8}$$

v) Find the minimum requisite g_{mi} to meet the UGB requirement from equation (6.1) under (i) above. If this value of g_{mi} is larger than the above calculated g_{mi}, then use this new g_{mi} as the minimum requisite g_{mi} of the circuit.

vi) To meet this new g_{mi}, the only parameter that can be altered is the width, W_i of the input transistor. To find the new W_i move on line AB (the constant power line chosen by power constraint) in Fig. 6.1 towards right hand side (lines for higher gain), which meets this g_{mi}.

vii) In order to find the required g_{mi} to meet the IRN requirements, manipulate the equation (6.2) given in (ii) above as under

$$\begin{aligned} g_{mi} &= \frac{-(-16kT) \pm \sqrt{(-16kT)^2 - 4 \times 3IRN^2(-16kTg_{ml})}}{2 \times 3IRN^2} \\ &= \frac{16kT \pm \sqrt{(16kT)^2 + 192IRN^2 kTg_{ml}}}{6IRN^2}. \end{aligned} \tag{6.9}$$

In this expression –ve sign will give a –ve g_{mi}, which is not a real solution and hence we take the solution with +ve sign. Secondly, g_{mi} is dependent on g_{ml}, which is further dependent on $\left(\frac{W}{L}\right)_l$. As g_{ml} increases g_{mi} reduces, but this dependance in very small, for large increase in L_l *i.e.* a large decrease in $\left(\frac{W}{L}\right)_l$ and hence a large reduction in g_{ml} results only in a small decrease in g_{mi}. Therefore, W_l and L_l are chosen to be the minimum permissible under the technology. Using these values g_{ml} is calculated and hence the minimum desired g_{mi} to meet the noise requirements. If this required g_{mi} is larger than the previously fixed g_{mi}, then the new g_{mi} is used to further find an enhanced value of W_i by moving to the right (increasing gain region) on the constant power line chosen.

viii) This gives the final values of device sizes and biasing for the differential amplifier circuit.

6.3 Verification by Simulation

The above methodology was coded using C, in a tool which was used to synthesize 2400 designs with different combinations of power budget, differential voltage gain, unity-gain bandwidth and input referred noise parameters in the ranges given below:

Power budget	—	100 – 1000 μW
Differential Voltage gain	—	10 – 1000
Unity Gain Bandwidth	—	1 – 1000 MHz
Input Referred Noise	—	1 – 20 nV/rtHz

The synthesized netlists of all the 2400 designs were simulated to compare their performance with the anticipated values of input-referred noise, differential dc voltage gain and unity-gain bandwidth.

6.3.1 Variation in Input-Referred Noise

The desired value of input-referred noise is plotted against the simulated value of input-referred noise for a fixed value of differential dc gain, Ad = 10 and UGB = 1 MHz as shown in Fig. 6.2. In absence of the error or in other words if simulated value perfectly matched with the desired value, then the graph should be a straight line with 45° inclination *i.e.* with slope as unity. But, the observed graphs do not show this behaviour in regions of low desired IRN. A closer look at the lines close to x-axis can be taken in Fig. 6.3.

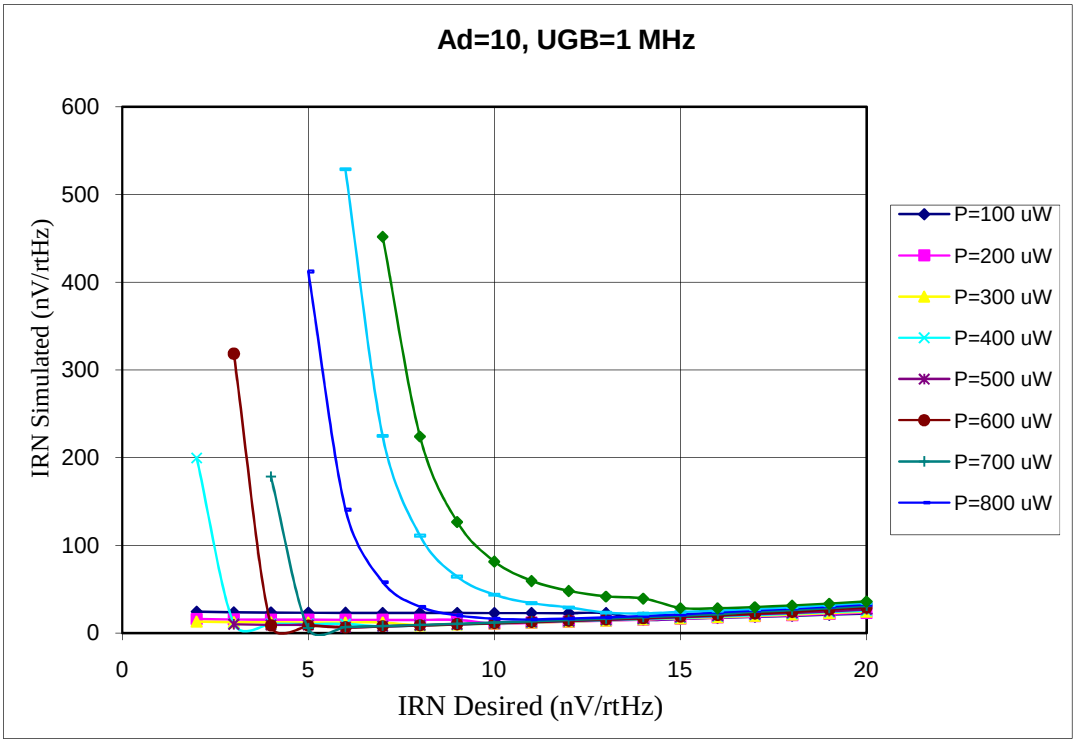


Figure 6.2 Variation in desired and simulated values of input referred noise at Ad=10 and UGB= 1 MHz.

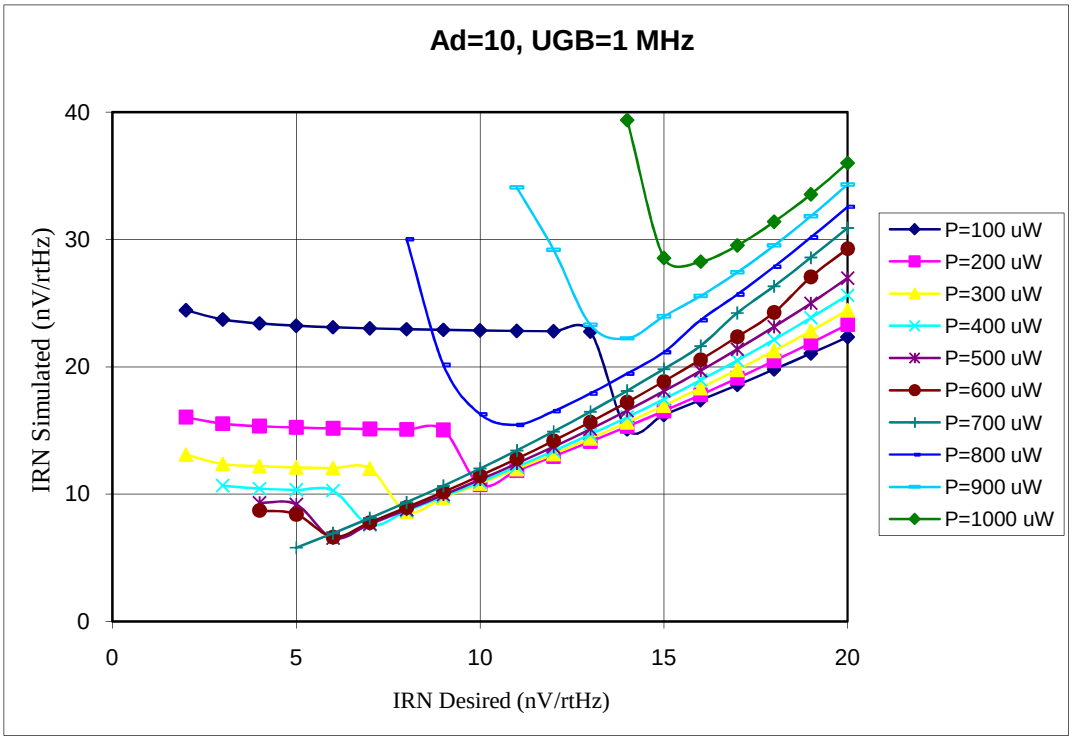


Figure 6.3 Close-up of lower portion of Fig. 6.2.

From the graph it is observed that the lines are straight upto a certain value of desired IRN below which the simulations predicted IRN increases sharply. This is because in these regions the input transistors leave the saturation region and go into the cutoff region. The slope is somewhat larger than unity, which implies that the simulated value of noise is slightly higher than the desired value and also changes with the power applied. In the case shown at desired value of 20 nV/rtHz, the simulated value is 22.3 nV/rtHz at 100 μW and it goes upto 36 nV/rtHz at 1000 μW. The reason for this variation with power is due to approximation of the model used, which has been explained in more detail in section 6.4. Every curve in the graph has a minima indicating that at this power, noise cannot be reduced beyond this point in the given technology. The minimum input referred noise achieved is 5.79 nV/rtHz at 700 μW.

Fig. 6.4 shows the desired value of input-referred noise plotted against the simulated value of input-referred noise for another combination of fixed values of differential dc gain, Ad = 10 and UGB = 100 MHz. It has been observed that with the demand of higher unity-gain bandwidth up to 100 MHz, the trend and values of simulated input-referred noise do not change.

However, it has been observed as shown in Fig. 6.5 that if an order of magnitude higher differential dc voltage gain is demanded, then the simulated input-referred noise patterns change significantly. The simulated input-referred noise is almost constant at a much lower value *e.g.* just 7.9 nV/rtHz at desired value of 8 to 20 nV/rtHz at the power of 700 μW and then further reduces up to 5.78 nV/rtHz at the desired value of 5.0 nV/rtHz and then increases sharply as shown in Fig. 6.6. It is also observed that at this high gain, if power larger than 700 μW is applied, then the noise increases to a much higher value for the reason that the input transistors leave the saturation region and move into the linear region of operation.

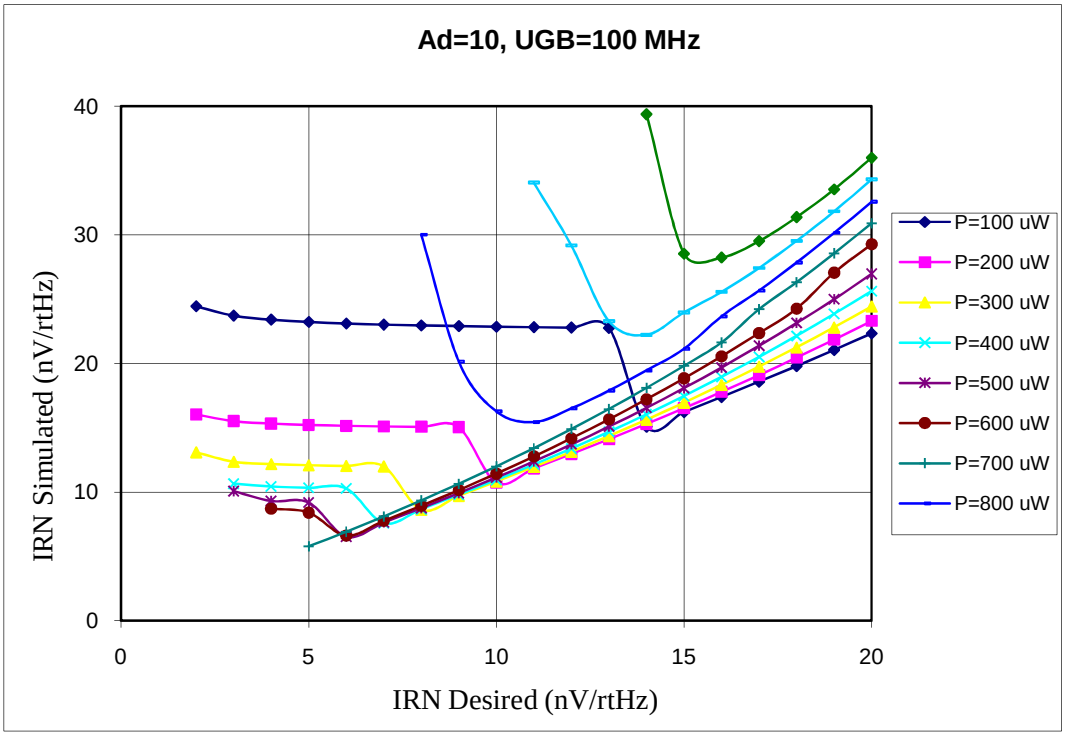


Figure 6.4 Variation in desired and simulated values of input referred noise at Ad=10 and UGB= 100 MHz.

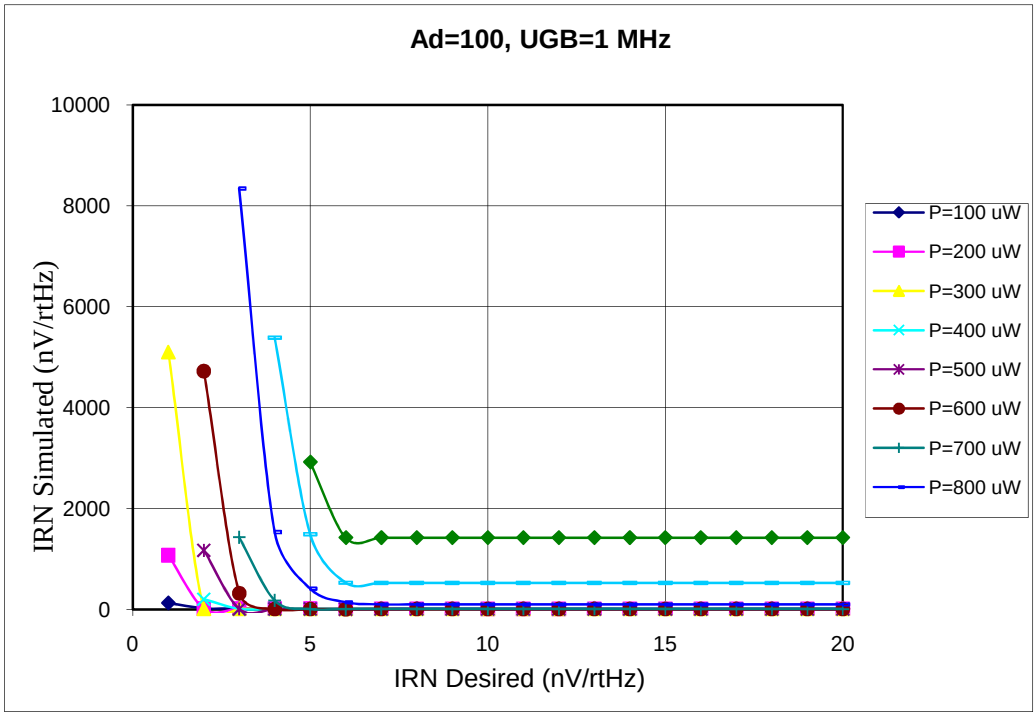


Figure 6.5 Variation in desired and simulated values of input referred noise at Ad=100 and UGB= 1 MHz.

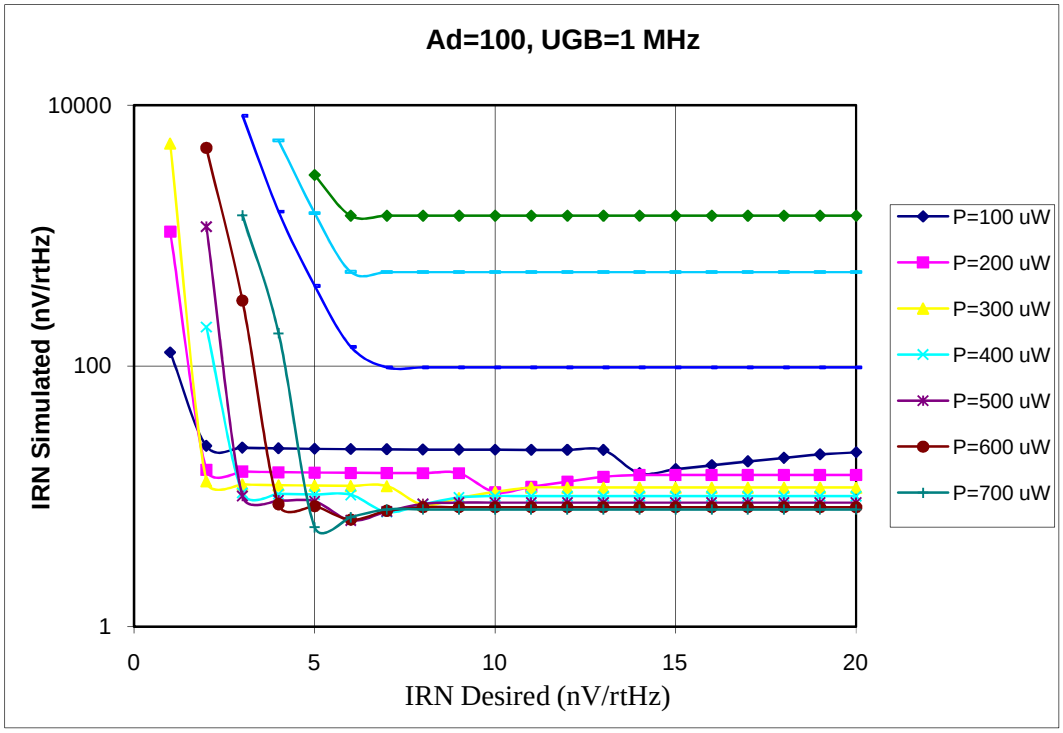


Figure 6.6 A close-up lower region of graph in Fig. 6.5.

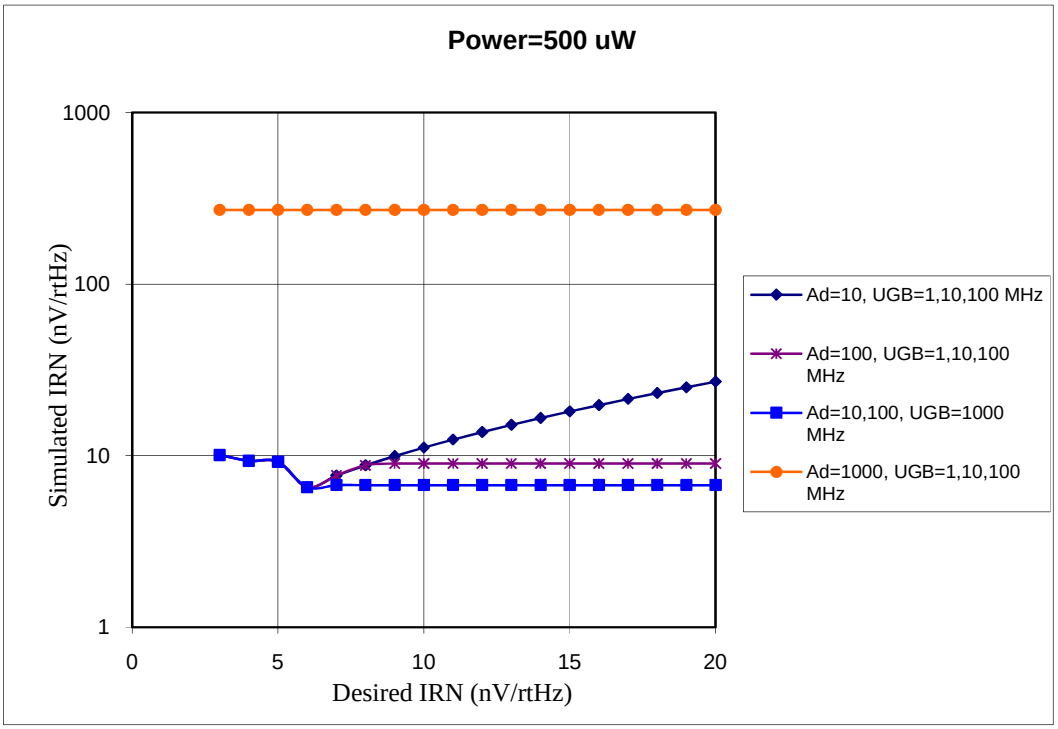


Figure 6.7 Variation in desired and simulated values of input referred noise with different combinations of Ad and UGB at a constant power of 500 μW.

Fig. 6.7 shows the variations between desired value of the input-referred noise and the simulated value of input-referred noise, for more combinations of differential dc voltage gain and the unity-gain bandwidths at the fixed power of 500 μW.

6.3.2 Area Power Trade-Off

An important trade-off between power and area always crops up in design. In order to meet other design objectives can we reduce area at the cost of power in area-constraint designs or can we reduce power at the cost of area in power conscious designs? The answer is yes. Fig. 6.8 analytically plots the area required for various values of input-referred noise, at different levels of applied power. From the graph it is clearly seen that at a given value of input-referred noise, the area required increases as the power applied reduces and vice-a-versa. The simulated equivalent graph is shown in Fig. 6.9, which validates the above observation over a substantial range. However, it deviates at the lower values of noise for powers below and up to 700 μW, because input transistors are in cutoff region and at high powers these transistors move into the linear region of operation. In either case the noise increases substantially as the current models used are valid only in the saturation region of operation.

6.4 Boundary Conditions

In this section, it has been attempted to bring out the boundary conditions in which the tool operates and gives satisfactory results. Beyond the boundary conditions, the tool may not give reasonable results. The boundary conditions have been found in terms of the minimum input referred noise, maximum differential dc voltage and maximum unity-gain bandwidth that can be achieved; and the power range that gives the best performance.

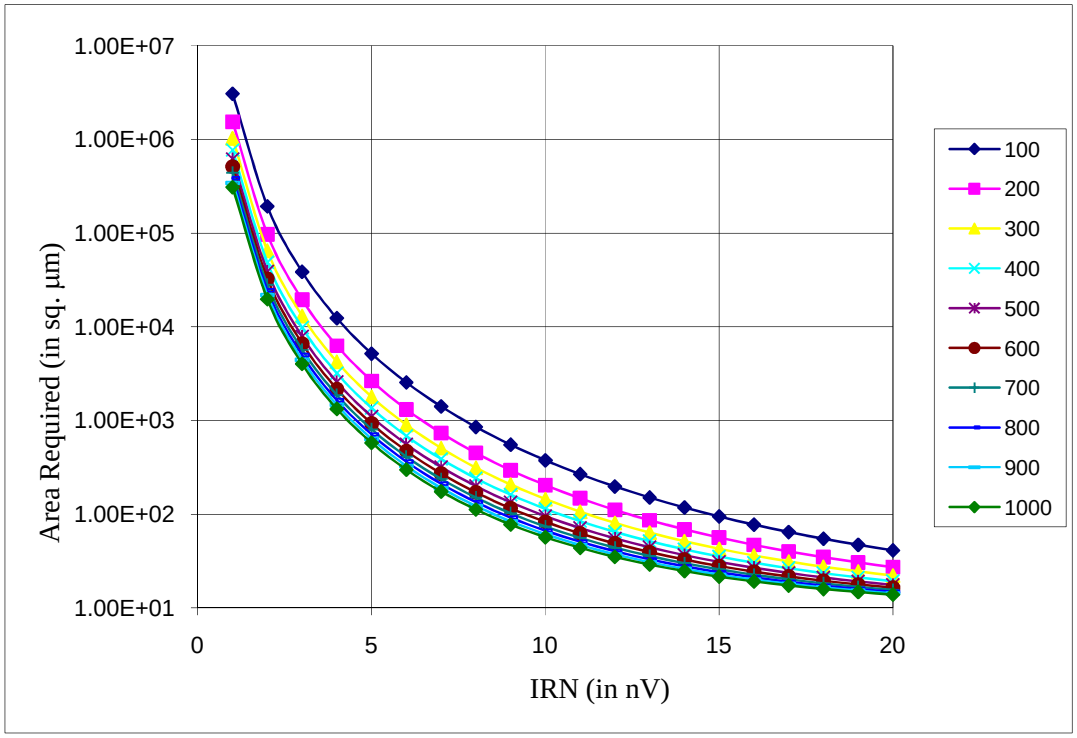


Figure 6.8 Analytical Area-Power trade off with varying input referred noise.

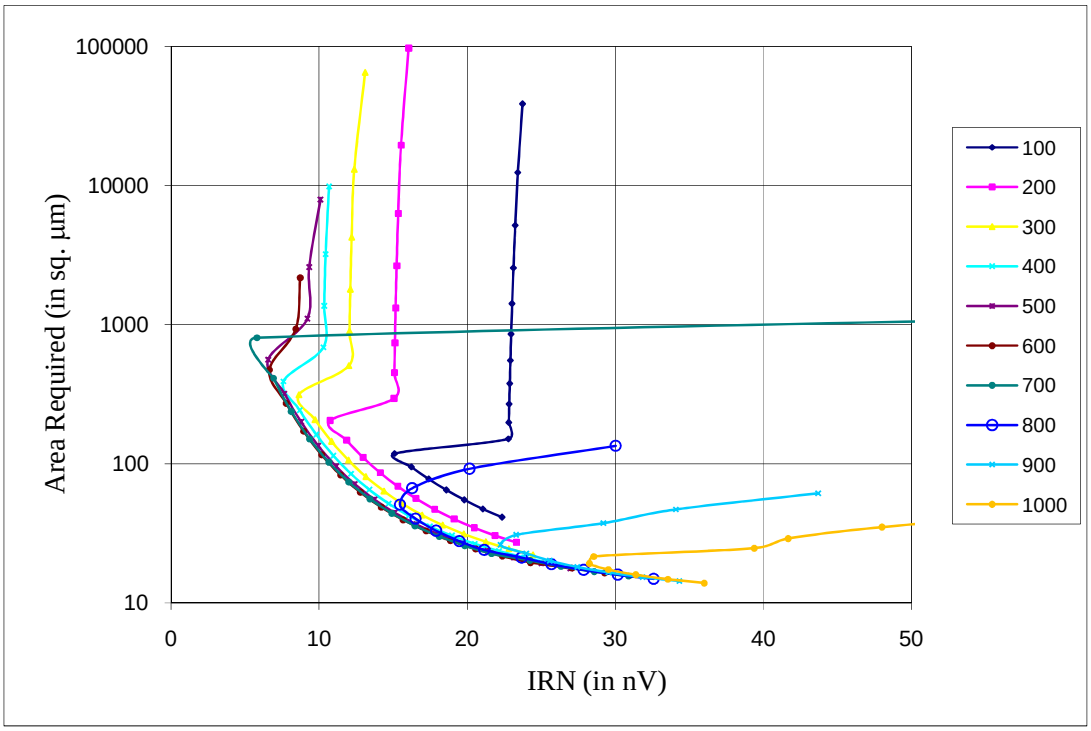


Figure 6.9 Simulated Area-Power trade off with varying input referred noise.

6.4.1 Power Range

Figure 6.10 plots the minimum achieved input referred noise as a function of power applied to the circuit. It is evident from the plot that to achieve a low noise circuit increasing or decreasing power beyond a limit is not going to help. However, the minimum value of thermal noise for the circuit is observed at 700 μW, the optimum value of power in this case appears to be in the range of 300 μW – 700 μW.

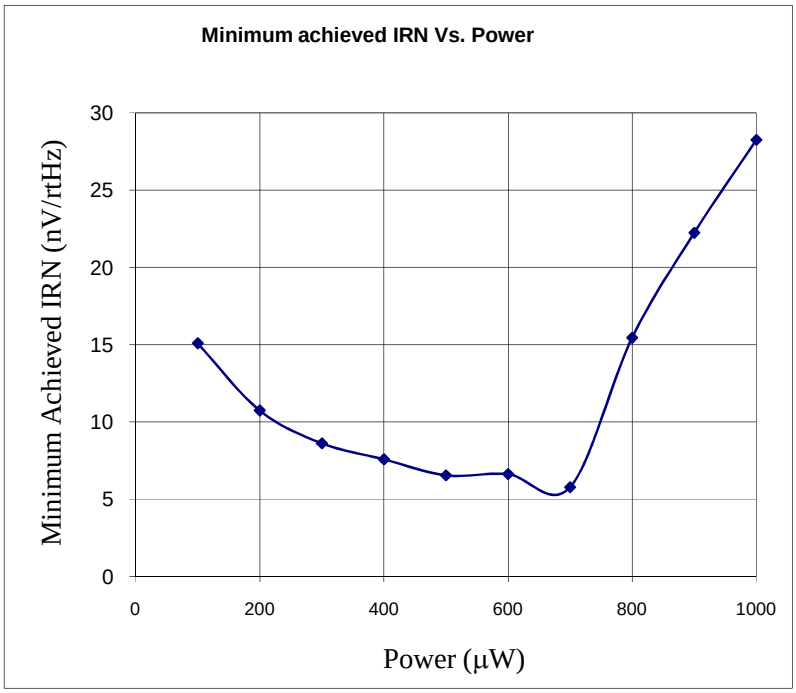


Figure 6.10 Minimum achieved IRN as a function of Power.

6.4.2 Limit on Noise Reduction, Gain and Bandwidth Enhancement

Clearly, from the previous discussions, there is a limit on each parameter, *i.e.* the best values that can be achieved for a technology. In the current technology based on the simulations performed on the designs, which were synthesized using this tool, minimum value of input referred noise that could be achieved is 5.3 nV/rtHz at 700 μW as seen in Fig. 6.10. The maximum value of differential dc voltage

gain achieved is 60.4 at 100 μW (refer Fig. 6.11) and the maximum value of unity gain bandwidth is 261.2 MHz at 700 μW (see Fig. 6.12).

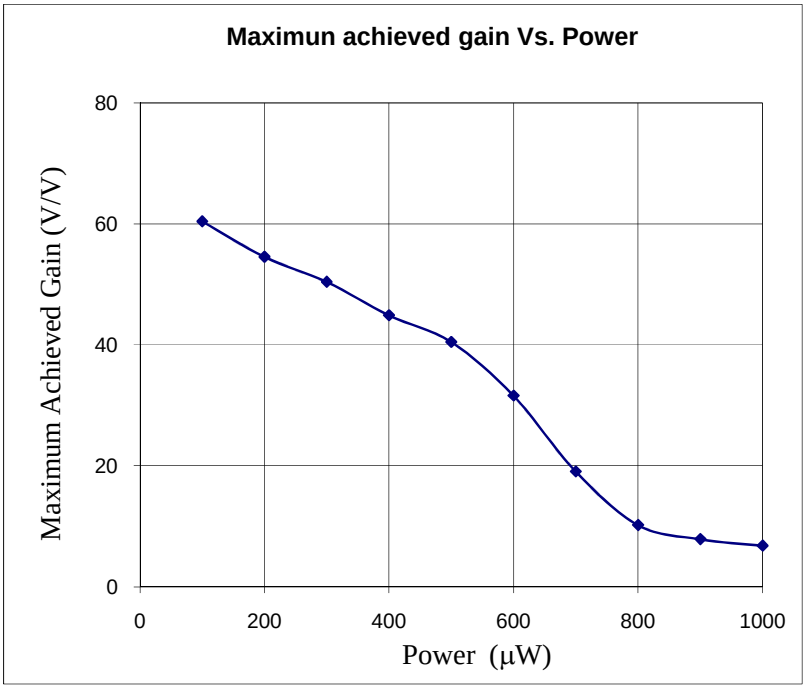


Figure 6.11 Maximum achieved differential dc voltage gain as a function of power.

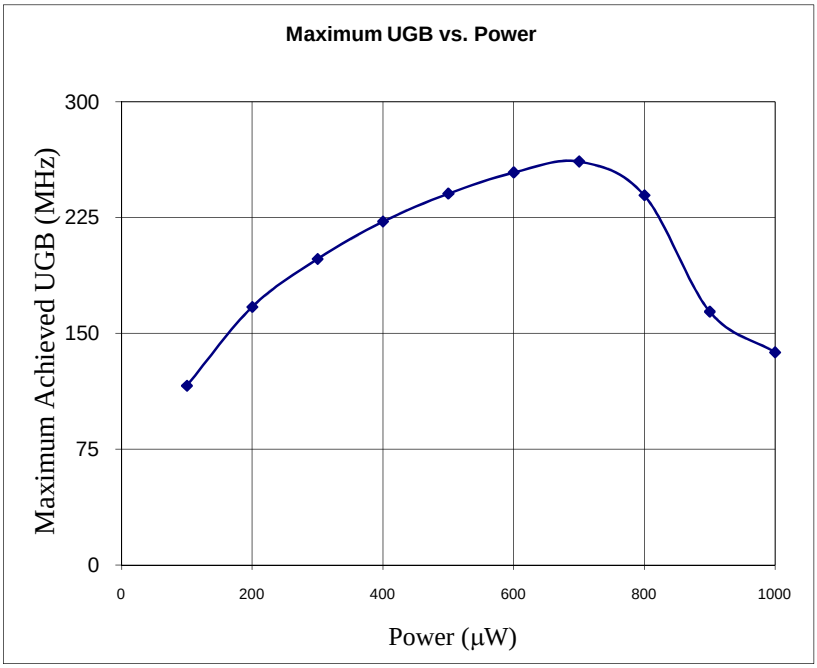


Fig. 6.12. Maximum achieved unity-gain bandwidth as a function of power.

6.5 Some Practical Implications

Whether a desired combination of differential gain, unity gain bandwidth and input referred noise is possible to achieve at all in a given technology is a question that needs to be engaged into. Limits and limiting relationships need to be explored in terms of the technology parameters, which govern differential gain, unity gain bandwidth and input referred noise.

This section is devoted to the exploration of limits and limiting relationships on differential dc voltage gain, Ad and unity gain bandwidth, UGB of an unloaded differential amplifier.

Since, the differential dc voltage gain, Ad and unity-gain bandwidth, UGB of a differential amplifier with the current mirror load (Fig. 4.1) are given by equations (4.14) and (4.15) reproduced below

$$UGB = \frac{g_{mi}}{2\pi \cdot C_L} = \frac{1}{2\pi \cdot C_L}\sqrt{\frac{k_n \cdot W_i \cdot I_o}{L_i}} \tag{6.10}$$

$$Ad = \frac{g_{mi}}{g_{di} + g_{dl}} = 2 \cdot \sqrt{\frac{k_n}{I_o} \cdot \left(\frac{W_i}{L_i}\right)} \cdot \left(\frac{1}{L_i}\left(\frac{dx_d}{dV_{DS}}\right)_n + \frac{1}{L_l}\left(\frac{dx_d}{dV_{DS}}\right)_n\right)^{-1} \tag{6.11}$$

All symbols have their usual meaning as mentioned in chapter 4.

The product of the differential dc voltage gain and unity-gain bandwidth can be written as

$$\begin{aligned} Ad * UGB &= \frac{1}{2\pi \cdot C_L}\sqrt{\frac{k_n \cdot W_i \cdot I_o}{L_i}} \cdot 2 \cdot \sqrt{\frac{k_n}{I_o} \cdot \left(\frac{W_i}{L_i}\right)} \cdot \left(\frac{1}{L_i}\left(\frac{dx_d}{dV_{DS}}\right)_n + \frac{1}{L_l}\left(\frac{dx_d}{dV_{DS}}\right)_n\right)^{-1} \\ &= \frac{k_n}{\pi \cdot C_L} \cdot \frac{W_i}{L_i} \cdot \left(\frac{1}{L_i}\left(\frac{dx_d}{dV_{DS}}\right)_n + \frac{1}{L_l}\left(\frac{dx_d}{dV_{DS}}\right)_n\right)^{-1} \end{aligned} \tag{6.12}$$

From section (3.3.3) substituting the values of $\left(\frac{dx_d}{dV_{DS}}\right)$ for n and p transistors in equation (6.12), it can also be written as

$$Ad * UGB = \frac{10k_n \cdot W_i}{\pi \cdot C_L} \cdot \left(1 + \frac{L_i}{2.L_l}\right)^{-1} \tag{6.13}$$

For an unloaded amplifier, the external capacitance is zero implying that the drain-to-bulk capacitances of the input and the load transistors form the capacitive load [Johns97], *i.e.*

$$C_L = C_{dbi} + C_{dbl} \tag{6.14}$$

where C_{dbi} and C_{dbl} are the drain-to-bulk capacitances of the input and load transistors respectively.

For a transistor the drain-to-bulk capacitance is given by

$$C_{db} = C'^{'}_{db} + C_{d-sw} \tag{6.15}$$

where C'_{db} is bottom plate capacitance of the drain junction and C_{d-sw} is the side wall capacitance of the drain junction.

Further,

$$C'_{db} = A_d \cdot C_{jd} \tag{6.16}$$

A_d is the area of the bottom plate of the junction, which is same as the drain area and C_{jd} is the junction capacitance per unit area for the one-sided step junction and is given by

$$C_{jd} = \frac{C_{j0}}{\sqrt{1 + \frac{V_{DB}}{\phi_0}}} \tag{6.17}$$

where C_{j0} is the zero-bias junction capacitance and is a process constant given by

$$C_{j0} = \sqrt{\frac{qK_s\varepsilon_0 N_D}{2\phi_0}} \tag{6.18}$$

and V_{DB} is the drain-to-bulk potential of the junction. All other symbols have their usual meanings.

The built-in potential, ϕ_0 is given by

$$\phi_0 = V_T \cdot \ln\left(\frac{N_A \cdot N_D}{n_i^2}\right). \tag{6.19}$$

The sidewall capacitance of the drain region, C_{d-sw} is given by

$$C_{d-sw} = P_d \cdot C_{j-sw} \tag{6.20}$$

where P_d is the perimeter of the drain region excluding the portion/wall adjacent to the gate and

$$C_{j-sw} = \frac{C_{j\_sw0}}{\sqrt{1+\frac{V_{DB}}{\phi_0}}}. \tag{6.21}$$

Hence the drain-to-bulk capacitance of a transistor can be written as

$$C_{db} = A_d \cdot C_{jd} + P_d \cdot C_{j-sw} \tag{6.22}$$

For the input transistor (n-type) we rewrite it as

$$C_{dbi} = \left(W_i * L_{d,n}\right) \cdot C_{jd,n} + \left(W_i + 2L_{d,n}\right) \cdot C_{j-sw,n} \tag{6.23}$$

and for load transistor (p-type)

$$C_{dbl} = \left(W_l * L_{d,p}\right) \cdot C_{jd,p} + \left(W_l + 2L_{d,p}\right) \cdot C_{j-sw,p} \tag{6.24}$$

where $L_{d,n}$ and $L_{d,p}$ are the lengths of drain extensions beyond the gate for n-type and p-type transistors respectively.

In order to simplify the overall expression of the product $Ad*UGB$, we make the following assumptions:

i) Typically drain extends 4λ beyond the gate, therefore

$$L_{d,n} = L_{d,p} = 4\lambda \tag{6.25}$$

ii) Since the differential gain and unity-gain bandwidth are independent of width of the load transistor, W_l, it can be chosen to be minimum *i.e.* 2λ. With this

$$C_{dbi} = (W_i * 4\lambda) \cdot C_{jd,n} + (W_i + 2 * 4\lambda) \cdot C_{j-sw,n} \tag{6.26}$$

$$C_{dbl} = (2\lambda * 4\lambda) \cdot C_{jd,p} + (2\lambda + 2 * 4\lambda) \cdot C_{j-sw,p} \tag{6.27}$$

iii) Further, if we approximate that $C_{jd,n} \sim C_{jd,p} = C_{jd}$ and $C_{j-sw,n} \sim C_{j-sw,p} = C_{j-sw}$, the total load capacitance is given by

$$C_L = C_{dbi} + C_{dbl} = (W_i + 2\lambda) \cdot 4\lambda \cdot C_{jd} + (W_i + 18\lambda) \cdot C_{j-sw} \tag{6.28}$$

iv) For most analog applications, to increase the input transistor trans-conductance, $W_i >> 2\lambda$, which further reduces equation (6.28) to the approximation

$$C_L \approx W_i \cdot 4\lambda \cdot C_{jd} + (W_i + 18\lambda) \cdot C_{j-sw} \tag{6.29}$$

Eqn. (6.29) can also be written as

$$C_L = W_i \left[4\lambda \cdot C_{jd} + \left(1 + \frac{18\lambda}{W_i} \right) \cdot C_{j-sw} \right] \cdot \tag{6.30}$$

Substituting this as the load in equation (6.13) the upper bound on the product $Ad*UGB$ becomes

$$Ad*UGB < \frac{10k_n}{\pi \cdot \left[4\lambda \cdot C_{jd} + \left(1 + \frac{18\lambda}{W_i} \right) \cdot C_{j-sw} \right]} \cdot \left(1 + \frac{L_i}{2.L_l} \right)^{-1} \tag{6.31}$$

v) Further, for most analog applications $W_i >> 18\lambda$, then the above equation (6.31) further reduces to

$$Ad*UGB < \frac{10k_n}{\pi \cdot \left[4\lambda \cdot C_{jd} + C_{j-sw}\right]} \cdot \left(1 + \frac{L_i}{2.L_l}\right)^{-1} \tag{6.32}$$

vi) Also, typically $L_i << L_l$, which further reduces the above expression (6.32) to

$$Ad*UGB < \frac{10k_n}{\pi \cdot \left[4\lambda \cdot C_{jd} + C_{j-sw}\right]} \tag{6.33}$$

This is a pure technology constant. Therefore, we can say that the product $Ad*UGB$ is a technology constant.

Even if $L_i << L_l$ is not true, and $L_i = L_l$ as in our case, the equation (6.32) reduces to

$$Ad*UGB < \frac{20k_n}{3\pi \cdot \left[4\lambda \cdot C_{jd} + C_{j-sw}\right]} \tag{6.34}$$

which is also a technology constant.

Equation (6.31) with $L_i = L_l$, is plotted as a function of W_i for several technologies as shown in Fig. 6.13. Clearly $Ad*UGB$ becomes independent of W_i for wide transistors and is a constant for a technology. It implies that gain of the circuit in a technology can only be increased at the cost of unity-gain bandwidth or vice-a-versa. The value of $Ad*UGB$ at $W_i = 500\mu m$ in various technologies has been plotted in Fig. 6.14. It is evident that in most cases the value of $Ad*UGB$ increases with the scaling of technology.

The simulated values of $Ad*UGB$ for 1.2 μm CMOS technology have been plotted in Fig. 6.15. Here, it is observed that the $Ad*UGB$ product becomes a function of the power applied to the circuit although in the analytical model it is independent of the power. This is because of the approximate model used for

channel length modulation, λ. It is assumed to be constant but actually it varies with the current flowing through the transistor.

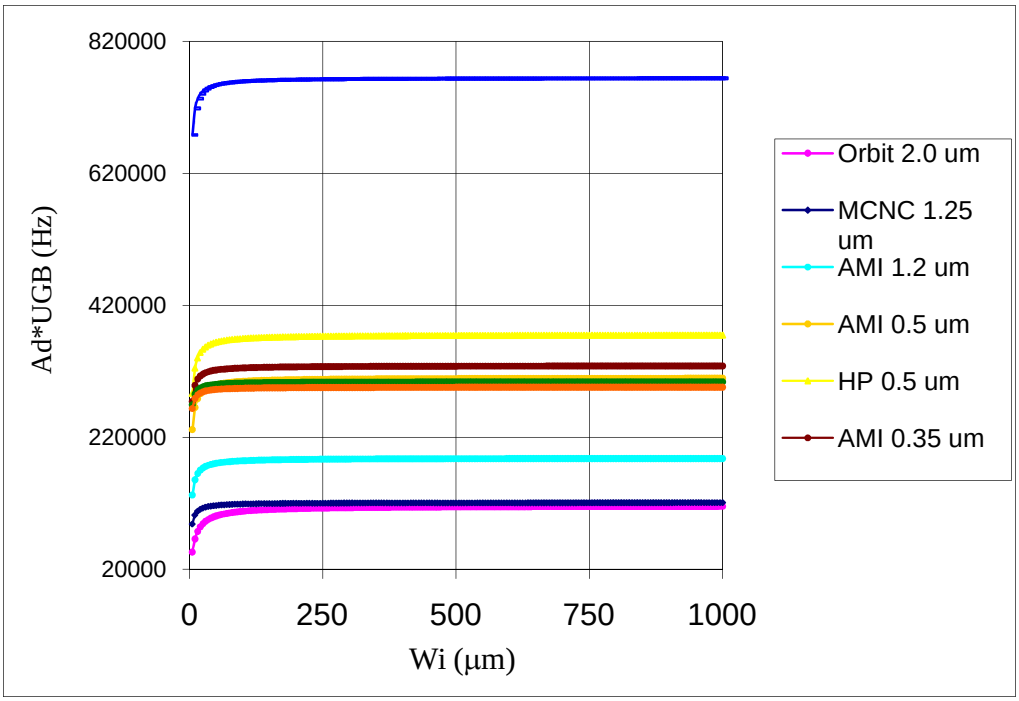


Figure 6.13 Analytical Ad*UGB product variation with technology.

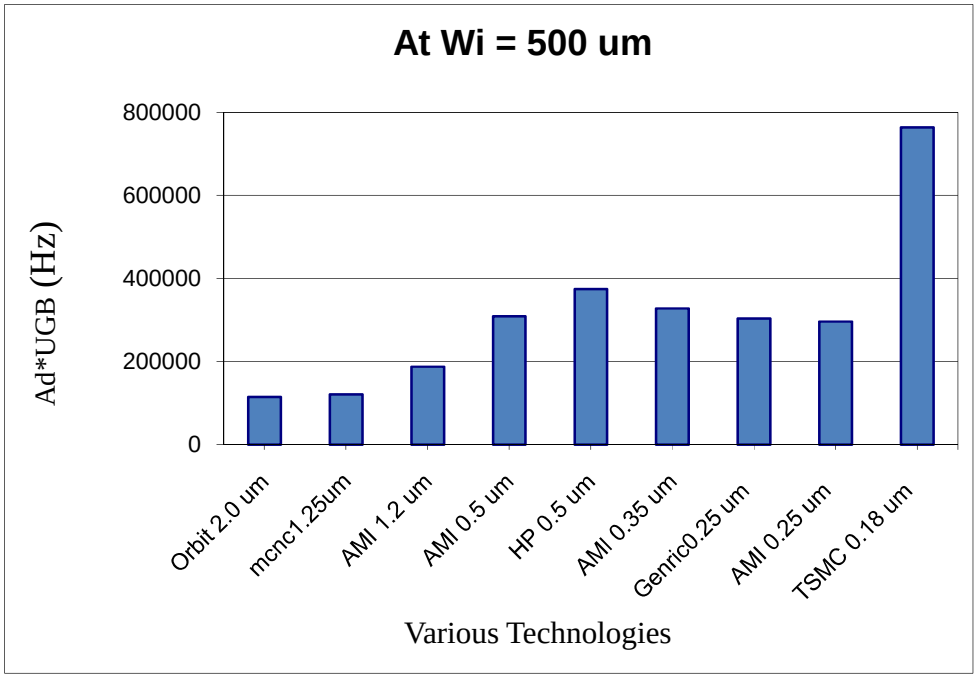


Figure 6.14 Ad*UGB product variation at $W_i = 500\mu m$ for various technologies.

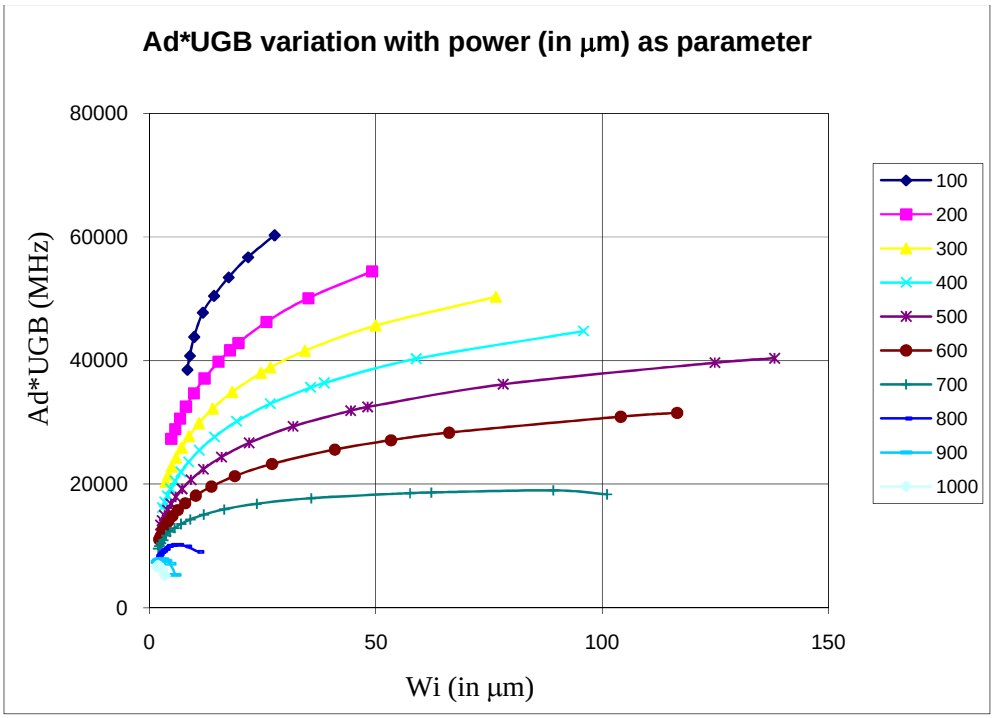


Figure 6.15 Simulated Ad*UGB product variation with power in MCNC 1.25 μm CMOS technology.

The above results (both analytical and simulated) were obtained with no external load connected to the output of the differential amplifier. Only the parasitic drain capacitance loads of the input and load transistors were considered. However, given that the unity gain bandwidth, UGB is inversely proportional to the load connected at the output of the differential amplifier, the limiting value of the gain unity-gain bandwidth product, $Ad*UGB$ for an amplifier loaded with external capacitor of value C_L can be worked out as

$$(Ad*UGB)_{loaded} = \frac{(Ad*UGB)*(C_{di}+C_{dl})}{(C_{di}+C_{dl}+C_L)} \tag{6.35}$$

$$= \frac{(Ad*UGB)}{1+\left(\frac{C_L}{C_{di}+C_{dl}}\right)} \tag{6.36}$$

$$= f_{load}*(Ad*UGB) \tag{6.37}$$

where f_{load} is a load dependent degradation factor defined by

$$f_{load} = \frac{1}{1 + \frac{C_L}{(C_{di} + C_{dl})}} \tag{6.38}$$

Equations (6.37) and (6.38) provides a rapid way of computing the loaded gain unity-gain bandwidth product, $Ad*UGB$ for any differential amplifier given its unloaded $Ad*UGB$ product. Fig. 6.16 shows how the $Ad*UGB$ product varies with the external load C_L.

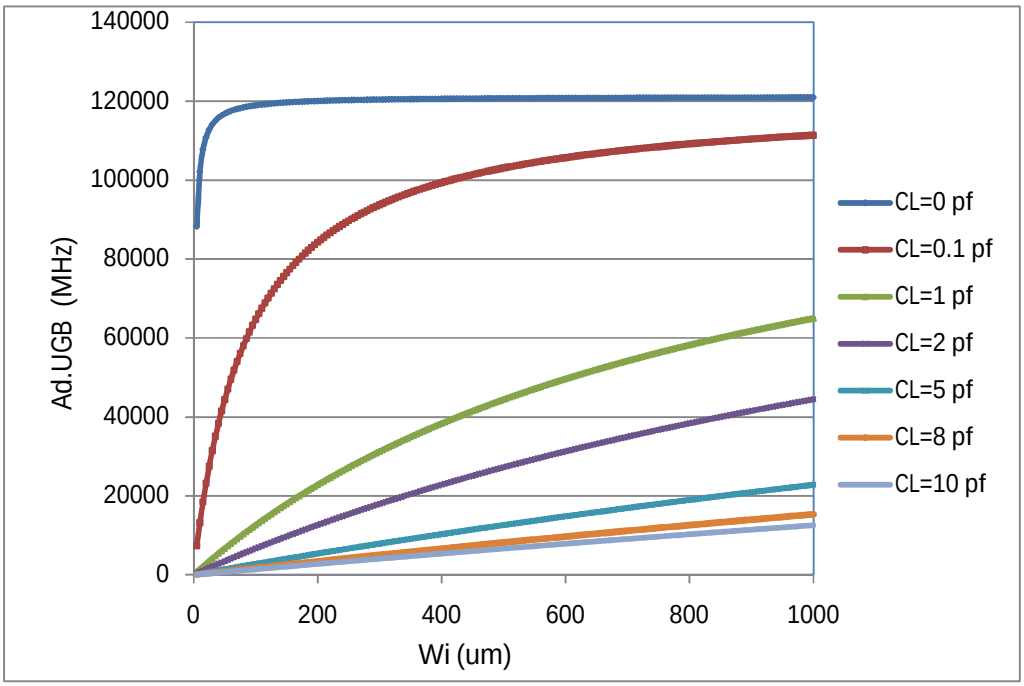


Figure 6.16 Analytical Ad*UGB product variation with external load C_L for MCNC 1.25 μm CMOS technology.

6.6 Layouts and Their Simulations

The layouts of five differential amplifiers were made in the given technology (MCNC 1.25 μm) chosen from the various synthesized circuits. They varied from each other in the widths of the input transistors, W_i = 200 μm, 100 μm, 50 μm, 20 μm, 10 μm. One such schematic and one associated layout corresponding to W_i = 200 μm are shown in Figs. 6.17 and 6.18.

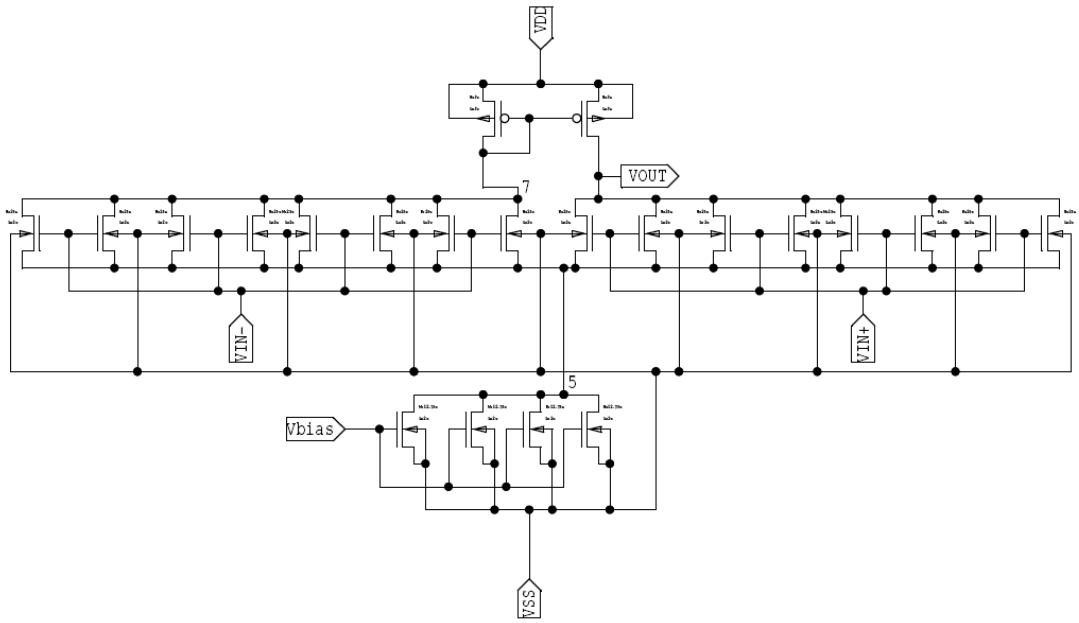


Figure 6.17 Fingered schematic of a Differential Amplifier with W_i = 200 µm.

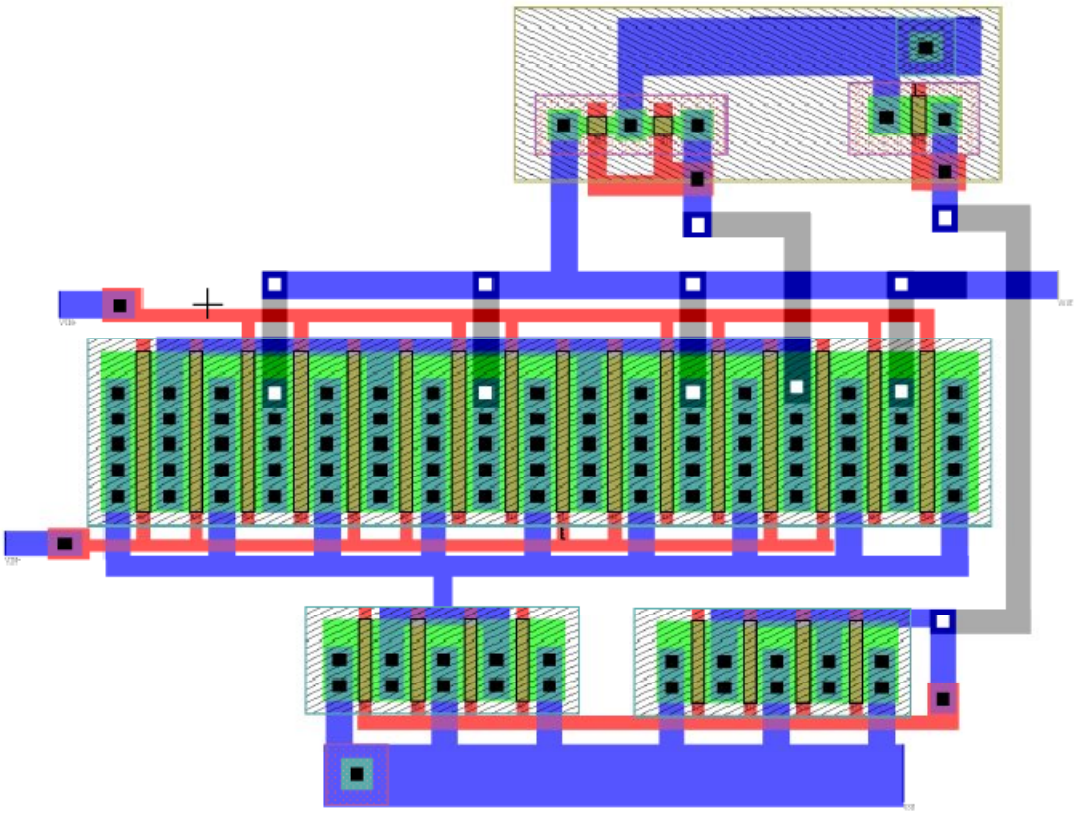


Figure 6.18 Layout of a Differential Amplifier with W_i = 200 µm.

The values of differential dc voltage gain, Unity-gain bandwidth and input referred noise for the schematics and layouts are compared as shown in Figs. 6.19, 6.20 and 6.21. The obtained values are in close match.

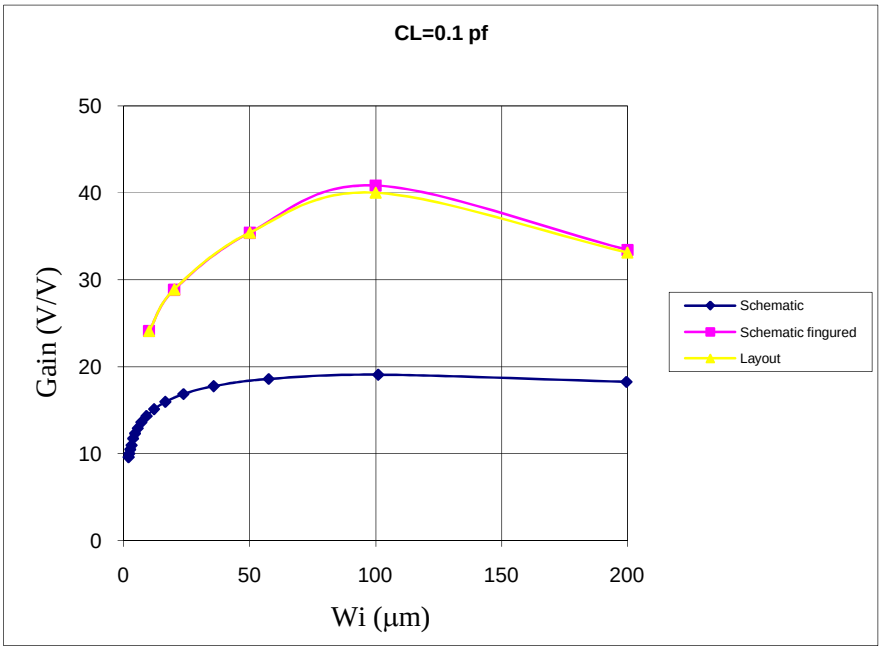


Figure 6.19 Differential dc voltage gain at an external load of 0.1 pf.

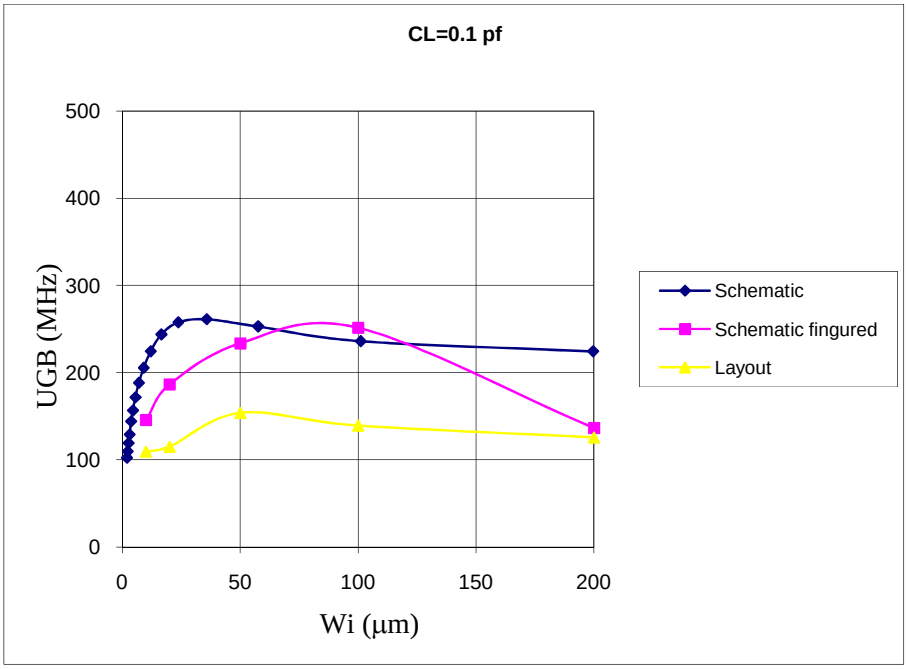


Figure 6.20 Unity-gain bandwidth at an external load of 0.1 pf.

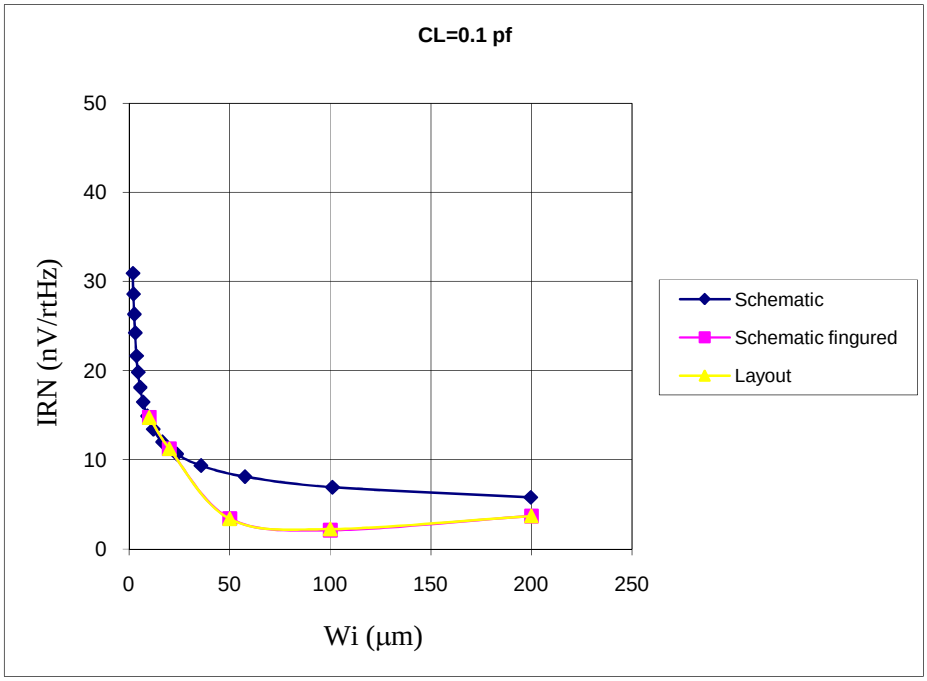


Figure 6.21 Input-referred noise at an external load of 0.1 pf.

The product $Ad \cdot UGB$ obtained from Figs. 6.19 and 6.20 is plotted in Fig. 6.22.

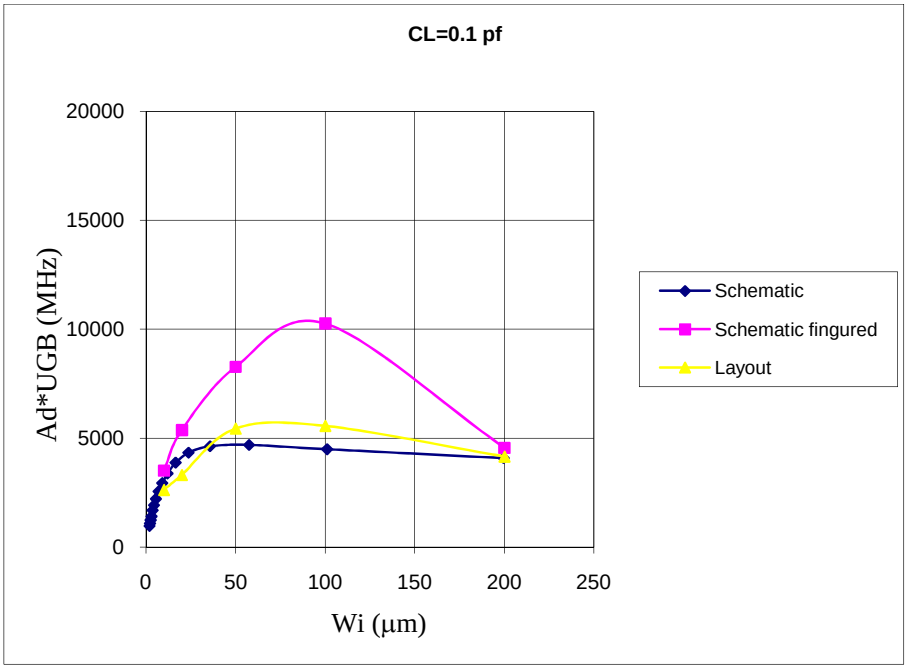
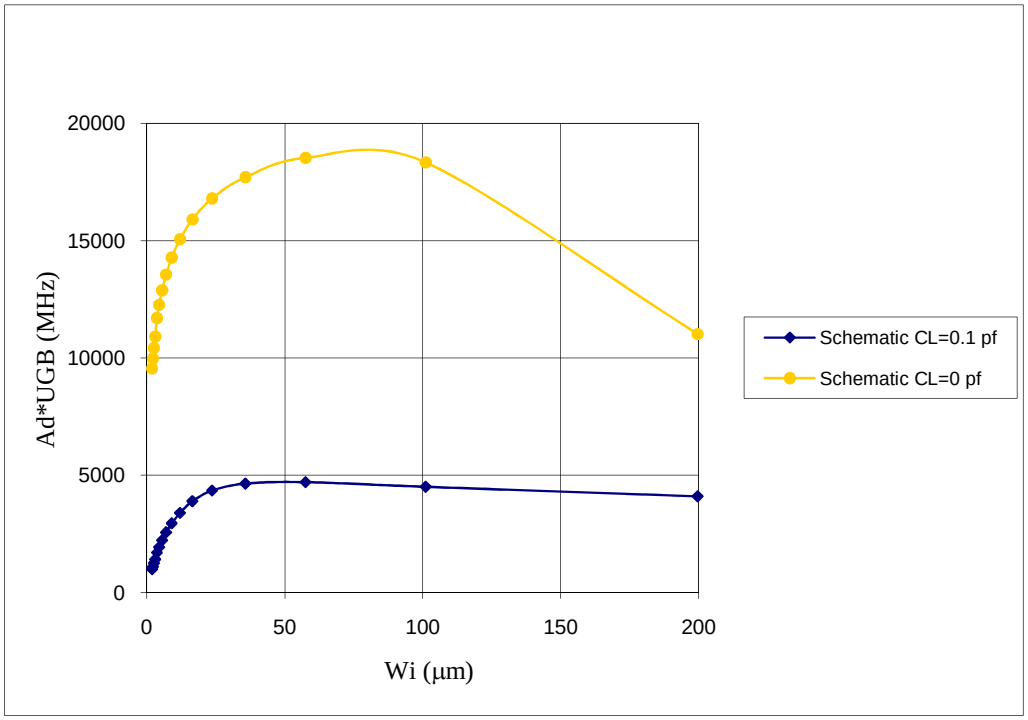


Figure 6.22 Product $Ad \cdot UGB$ at an external load of 0.1 pf.

The product $Ad \cdot UGB$ varying with the applied external load, C_L from schematics and layouts in the given technology are shown in Figs. 6.23 and 6.24.



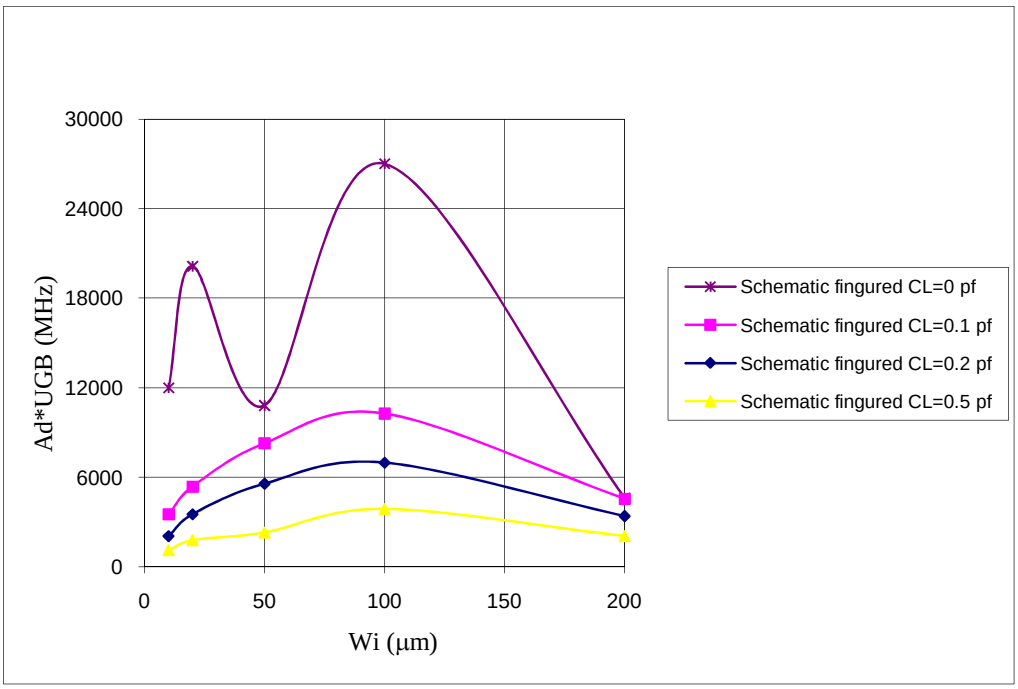


Figure 6.23 Product $Ad \cdot UGB$ varying with external load.

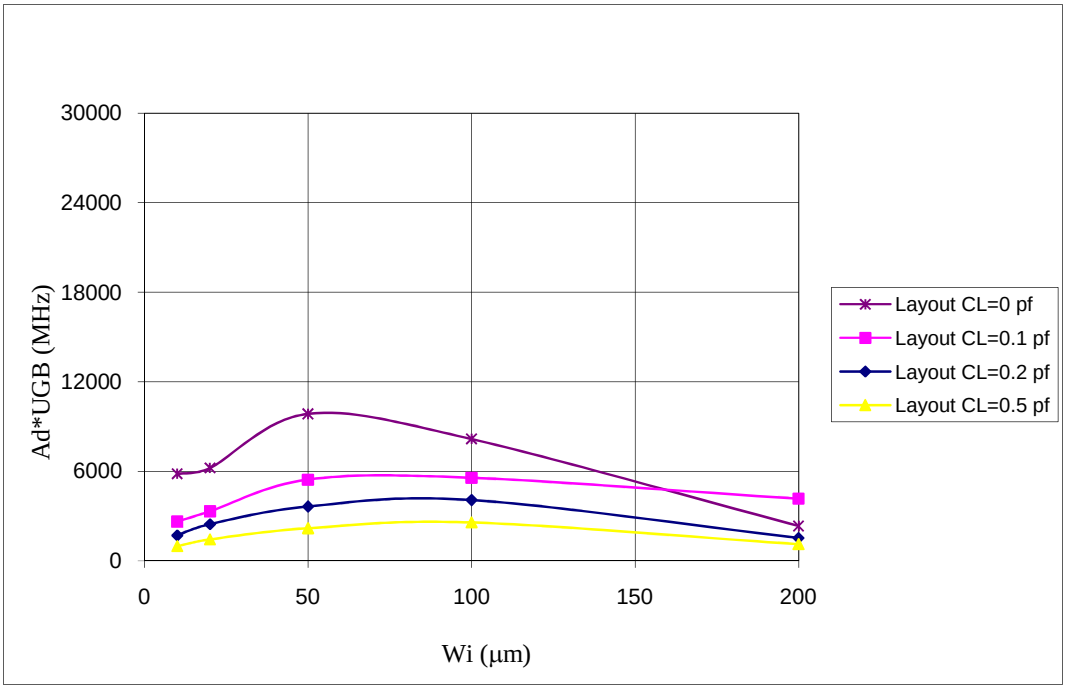


Figure 6.24 Product $Ad \cdot UGB$ from layouts with an external load.

Chapter 7

Conclusions and Future Scope of Work

7.1 Conclusions

- A new methodology based on the concept of figure of merit that includes the three performance parameters, namely input-referred noise, differential dc gain and unity-gain bandwidth, has been proposed for synthesizing optimal performance differential amplifiers under the constraints of area. The figure of merit peaks at a certain value of relative area allocation to the input transistors in the range of $\mathbf{60}$ % to $\mathbf{80}$ % of the available area. The peak value of figure of merit is a function of area. However, it is independent of biasing current (and therefore power consumption) subject to the minimum current (and therefore a minimum power) required to keep all the transistors biased in the saturation region. The peak figure of merit and minimum power required to achieve the peak figure of merit are thus both functions of area. These analyses help in synthesizing optimal differential amplifier circuit designs under area constraints.
- The above concept has been validated with examples of input stage differential amplifier and second stage amplifier designs both at low and medium/moderate frequencies. It is observed that the dc gain, bandwidth and noise achieved at peak $\boldsymbol{FoM}$ are very close to the best achievable values.
- The above ideas have been incorporated in a CAD Tool developed in C/C++, for the synthesis of differential amplifiers. The tool has been tested for 2400 design-syntheses with dc power varying from 100 to 1000 mW, dc voltage gain in the range of 10 – 1000, unity-gain bandwidth in the range of 1– 100 MHz, and input-referred noise in the range of 1 – 20 $\boldsymbol{nV/rtHz}$.

- The synthesized circuits are mainly governed by power and noise. Area required increases exponentially with reduced noise requirement. Area requirement can be reduced with increased power for the same input-referred noise. Hence, a clear Area – Power tradeoff is seen in the synthesized designs.
- The proposed concept of figure of merit is a suitable approach for synthesizing optimal designs of differential input stage of two-stage compensated operational amplifiers under area constraints and leads to the realization of differential dc gain, unity-gain bandwidth and input-referred noise values that are also very close to their individually achievable best values under the same area constraints.
- The analyses validate that the idea of FoM may be employed in a CAD tool for automatically synthesizing differential input stage amplifiers and can be extended for other building blocks. The study also highlights that the total band noise for a given area is almost constant and also does not vary significantly with total area assigned to the circuit.
- The limits and limiting relationships on differential dc voltage gain Ad, and unity-gain bandwidth UGB, of an unloaded differential amplifier were explored. It has been observed that the product $Ad \cdot UGB$ of an unloaded differential amplifier is a technology constant.
- The layouts of some of the synthesized circuits were drawn manually and were simulated and compared against simulated results on schematics. The results are in close match agreement.

7.2 Future Scope of Work

- The concept of Figure of Merit based synthesis can be extended for more analog circuit blocks.
- Studies can be extended to the relative area allocations between various stages of an amplifier.

- More performance parameters, like Input common mode range, slew rate, *etc*. may be included in Figure of Merit, and bounding limits as well as the feasibility of realization of a given set of performance parameters vis-à-vis a given technology analyzed to guide the user to not set goals unrealizable through a given technology.
- Formulation of these limits and their simultaneous realizability can also be used to select an appropriate technology (if one exists) and the associated area and power requirement for the realization of all the performance parameters.

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