DESIGN OF COSINE CONTROL FIRING CIRCUIT USING SINUSOIDAL OSCILLATOR

A Dissertation submitted in partial fulfillment of the requirements for the award of degree

Of

MASTER OF ENGINEERING

In

Power Systems

Submitted by

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JULY 2015

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CERTIFICATE

I hereby certify that the work which is being presented in the dissertation entitled, **"Design of Cosine Control Firing Circuit Using Sinusoidal Oscillator"**, in partial fulfillment of the requirements for the award of degree of Master of Engineering in **Power Systems** submitted in Electrical and Instrumentation Engineering Department of Thapar University, Patiala, is an authentic record of my own work carried out under the supervision of Mr.Shailesh Kumar, lecturer, EIED.

The matter presented in this thesis has not been submitted for the award of any other degree or diploma anywhere.

(Rajeev Kumar Raut)

This is to certify that the above statement made by the candidate is true to the best of my knowledge and belief.

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ACKNOWLEDGEMENT

I feel honored in expressing my profound sense of gratitude and indebtedness to **Mr. Shailesh Kumar**, Lecturer, Electrical and Instrumentation Engineering Department, Thapar University, Patiala for his guidance, meticulous efforts, constructive criticism, inspiring encouragement, unflinching support and invaluable co-operation which enabled me to enrich my knowledge and reproduce it in the present form.

I also like to extend my gratefulness to **Dr. Ravinder Agarwal**, Professor and Head, Electrical and Instrumentation Engineering Department, Thapar University, Patiala for his perpetual encouragement, generous help and inspiring guidance.

I am very grateful to **Ms. Manbir Kaur**, Associate Professor and PG Coordinator, Electrical and Instrumentation Engineering Department, Thapar University, Patiala for her co-ordination throughout my M.E. Degree.

I am also very thankful to the entire faculty and staff members of Electrical and Instrumentation Engineering Department for their direct–indirect help, co-operation, love and affection, which made my stay at Thapar University memorable.

I wish to thank all my classmates for their time to time suggestions and cooperation without which I would not have been able to complete my work.

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ABSTRACT

The theme of dissertation is to design & implement the firing circuit for a converter. The idea behind our dissertation is to use cosine signal for the firing circuit which has several advantage. The various circuits like UJT relaxation oscillator triggering, RC triggering & Ramp triggering etc undergoes the problem of limited firing angle. But Cosine Firing Scheme (CFS) can be implemented for the very precise control of firing angle. Another advantage of CFS is that it can be controlled digitally using microcontrollers. Thus can be used for the closed loop circuit. For giving the AC supply of 6-0-6 V earlier we are using the Centre tap transformer which makes the circuit bulky and also the overall cost of the firing circuit is high. Instead of Centre tap transformer we are using sinusoidal oscillator which has a high frequency in the firing circuit and its cost is cheaper than transformer and easily available and the bulkiness of the firing circuit reduces. In the earlier research the voltage which we get at the pulse transformer doesn’t have the high frequency therefore so there will be delay to turn-on the thyristor. For designing the firing circuit we are using digital & analog component such as SCRs, BJTs, MOSFETs, 1-phase converter comparator, Monoshot, SR flip flop, 555 timer, opamp etc. The model is simulated on Multisim software and implemented on bread board for its real time implementation and several results are obtained on oscilloscope.

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LIST OF ABBREVIATIONS

SCR	Silicon Controlled Rectifier
GTO	Gate Turn Off Thyristor
IGBT	Insulated Gate Bipolar Transistor
A	Anode
K	Cathode
G	Gate
V_{AK}	Voltage from Anode to Cathode
V_{BO}	Forward Break-over Voltage
I_g	Gate Current
V_g	Gate Voltage
V_{BR}	Reverse Breakdown Voltage
I_L	Latching Current
I_H	Holding Current
t_q	Device Turn-off time
t_{rr}	Reverse Recovery Time
t_{gr}	Gate Recovery time
t_c	Circuit turn-off time
t_c	Delay time

t_r	Rise time
t_s	Spread time
SF	Safety Margin
I_c	Charging Current
LASCR	Light activated SCR
δ	Duty cycle
V_{gt}	Gate turn-on Voltage
α	Firing angle
$\uparrow$	Increase
$\downarrow$	Decreases
ZnO	Zinc oxide
η	Efficiency
DRF	Derating Factor

CHAPTER 1

INTRODUCTION

1.1 OVERVIEW

Power Electronics have revolutionized the concept of power control for power conversion and for control of electric motor drives from one form to another in an efficient, compact and robust manner for better utilisation. Power semiconductor devices should be capable to withstand or handle large magnitudes of power with high efficiency. Because of these dynamic properties of semiconductor devices it may be used as switches [1-5]. These devices operate by controlling the flow of electrons in a semiconductor which is a crystalline solid .The physical, chemical and electrical properties of a solid depend on the arrangement of atoms in the substance. [6]The conduction electrons in a solid are distributed in energy. The Silicon Controlled Rectifier was discovered at Bell Labs and commercially produced by General Electric.

The SCR is the most utilized of the thyristor family of four layers [1-5]. It is normally switched on by the triggering of a gate pulse when a forward bias voltage from anode to cathode is present at the main terminals. Being regenerative it cannot be turned off by the gate terminals especially at the highly amplifying factor of the gate. These devices are the work horses of the Power control in an efficient manner. They are switched off by natural commutation and are reverse biased for a few milliseconds subsequent to a conduction period. . [6] SCR can be used as the control elements for phase angle triggered controllers, ph0ase fired controllers and many more application.

1.2 BACKGROUND

The usage of rectifier is a common in industrial company nowadays. For the time being, there are many rectifier listed on the datasheet of a power semiconductor company. One of the rectifiers is known as uncontrolled rectifier, which has been used to provide a constant output voltage. In the other hand, there is also controlled rectifier that was used to regulate the speed of dc motor [33]. In industrial application, controlled rectifiers are widely used in DC welder, DC motor drive, and battery charger. The controlled rectifier obtained power supply from a single phase or three phase alternating current (AC) power. For home appliances such as hair dryers, single phase input supply is used [1-6]. Besides that, most of electronic devices virtually require a DC voltage to perform tasks. The three phase rectifier consists of complex circuitry and has a complicated operation. In order to design the controlled rectifier for the first time, it is better to understand the operation of single phase controlled rectifier. The purpose of this dissertation is to design hardware of a single phase controlled rectifier and its control circuit.

1.3 PROBLEM STATEMENT

There are many ways to control or trigger the Silicon Controlled Rectifier (SCR) gate terminals which are called firing or triggering circuit. For instance, the SCR gates can be triggered using Unijunction Transistor (UJT). At the present time, more of the SCR is triggered using Ramp Comparator Scheme, RC triggering, Pedestrial Triggering etc undergoes the problem of limited firing angle. For the very precise control of firing angle, Cosine Firing Scheme (CFS) can be implemented. Added advantage of CFS is that it can be controlled digitally using microcontrollers also, thus can be used in closed loop applications. In this thesis, the development of firing circuit is done using analog approaches with Cosine firing Scheme by using sinusoidal oscillator.

1.4 LITERATURE REVIEW

Here is review of some literature that is relevant to carry out thesis work.

Ilango B. et al. Presented the firing circuit for 3-phase silicon controlled rectifiers bridge used for different industrial purposes. It is a compressed scheme using less integrated circuit components which gives a fast response for triggering angle correction and gives full different ranges of control of voltage **[8].**

Daniels A.R et al. presented a digital firing angle controller that can operate in conjunction with microcomputer or microprocessor for online control of DC machine using thyristor as a controller **[9].**

Ainsworth J.D. et al. Presented a thyristor controlled reactor (TCR) which is used to control the voltage of AC power system. It includes a reactor in series with reverse parallel connected thyristor. A phase inaccessible oscillator is used in which the oscillator controls the valve directly. A phase locked oscillator is sometimes used to create a fixed phase for time orientation **[10].**

Zaid S.A et al. Presented about SCR controlled series converter which is the collective circuit in SVC. TCSC is fired with firing circuit which are formed by the harmonization with sinusoidal phase current. However the line current is not sinusoidal and constitute of some harmonics. They have discussed the possible firing technique for TCSC **[11].**

Gupta Mukesh et al. presented a controlled electronics circuit by using cosine control method for a regulated dc voltage with linear transfer characteristic. He has also shown the desired results simulated in MATLAB/SIMULINK **[12].**

Kim J.M.S. et al. Presented a DC power supply which is constructed on frequency converter and a double converter to solve the problem in conservative approach because of this problem the power dissipation across the transistor banks have occurred. This method improves the vigorous response **[13].**

Lo Yu-Kang et al. presented an enhanced cosine control method for silicon controlled rectifier. In this method monostable blocks is replaced by ZCD and AND gates. The difficulty of rebounding of comparators output can be lessened by using the AND gates. So it stops the false triggering of SCR **[14].**

Peter Geno et. al Presented cosine wave crossing control is used for triggering circuit. The benefits of this scheme are that the output voltage is proportional to the control voltage. He has included various fortifications like short circuit, under voltage and over voltage etc. The main resolution of this project is to project an effective, simple, robust and reasonable control circuit **[15].**

Gupta S.C. et al. Presented delay angle function of a linear ramp or the cosine of the phase angle variation by using the comprehensive phase detector. A precise offset voltage is introduced into the PLL to simulate an error signal within the hoop. As the PLL tracks the reference signal, voltage control oscillator generates a phase intelligible signal having a frequency which is a numerous of the reference frequency and owning a finite phase difference with it, which is controllable. This signal gets protected with the phase frequency signal and continuously tracks it **[16].**

Sheikh A. B. et al. Designed simulated and made-up a triggering circuit for converters used in DC drives applications. The purposes of this design integrate the specific control of firing angle, provision for feedback control for motor control applications and realising pulse of designed nature **[17].**

Harade K. et al. Presented a magnetic circuit to control the triggering of bridge inverter so that the range of the output voltage is self-governing of operating frequency and the variation DC source voltage **[18].**

Abou-Elela M. et al. Presented simple arrangement for use in three phase firing circuit four cable ac voltage controller systems. It enables the firing circuit to regulate itself against any phase. It also senses if the system contains faulty thyristors **[19].**

Subramanian K. et al. Presented a linear ramp signal based harmonization technique has been propose and realized effectively, for the capacitor converting operation of a simple power system. This feature leads to elimination of the phase locked-loop (PLL) control, are commonly used to synchronize the pulse generations with respect to the system the supply frequency **[20].**

Torseng S. et al. Presented that the arrangement of TSC and TSR which is controlled by the thyristors. One method to humid power oscillation, using TSC with a certain four control strategy, is presented. The problem of unstable loads and load balancing methods has been also discussed. The total collective system does not generate any harmonics **[21]**.

Tang Pei-Chong et al. presented a microprocessor-based firing system. Composed with software procedure in microprocessor, the digitized ac power signals are used to find the correct firing output signals. This arrangement uses less hardware components and has higher energetic performance in four-quadrant procedure **[22].**

Simard Remy et al. Presented intermediate pulse scheme, a single pulse train is produced whose phase can be shifted with respect to a regulator voltage. A loop counter is used to undeviating the train of pulses in six dissimilar paths through pulse amplifiers and isolating transformers. An extreme number of combined circuits are used and the total number of discrete components is reduced to a least so that it’s vital for integrated circuits **[23].**

Saridis G.N et al. presented a linear SCR regulator amplifier comprises of two major distributions of fire circuit and bridge power circuit. The input signal is improved and used to control the phase of UJT pulses. The relation among the input signal and firing angle is considered to be the inverse of the non-linearity presented by the power circuit. The power bridge balancing realisation is used to engage the major portion of the negative power pulse caused by an inductive load and it advances the efficiency of the amplifier **[24].**

Mirbod Ali et al. presented a progressive microprocessor-based control system for a phase-controlled rectifier which has the aforementioned anticipated characteristics. It has a constant open loop gain even for the cases where the converter is nourished by a weak ac system of unfettered frequency, while the handling delay of the control system is fewer than 20µs. With continually decreasing microprocessor and digital hardware expenses, the application of such a control system, for engineering applications, is moderately economical **[25].**

Rafique M.U. et al. presented a system which is fully insulated and affords full and stable governor over the firing angle of the SCR from 0 to π. Segregation in interfacing of the high power AC/DC circuits from the small power digital governor circuit is one of the key experiments in such designs. This method eliminates the pulse transformer that is not only affluent but also provides the means of captivating coupling that is damaging for the circuit **[26].**

E A Faulkner et al. A innovative and modest clock abstraction circuit is defined. It is based on feedback around a monostable multivibrator resulting in a self-sustaining clock signal. The technique suitable in systems which do not require the clock perfectly harmonized to the data. The circuit protections of three customary IC gates and two interruption units **[27].**

Rohit Gupta et al. Presented dissimilar speed regulator techniques of DC motor and makes a relational study of dissimilar converter based speed supervisor techniques. It is also pragmatic that the choice of non-linearity is small in semi converter as related to limited wave and full converter drives, so semi converter drives can be favoured for the varied range of load torque **[28].**

Taka shih Origome et al. Presented the design structures and assessment results of a thyristor power converter for very high voltage dc (HVDC) transmission for learning of its feasibility. It comprises of a thyristor regulator (which signifies one armrest of a bridge) through a bridge output of 100-kV dc. This regulator structures series use of 120 2.5-kV, 500-ampere thyristors and claim of optoelectronics technology where incandescent diodes and a light-sensitive device are engaged for gate firing, overvoltage security, and amount of device-distributed voltage **[29].**

Wade John Sperry et al. Presented a scheme of common pulse triggering for a three-phase SCR bridge, which features a control circuit that derives its synchronization and power from the ripple potential of a three-phase half-wave rectifier, thee ripple potential is separated from the average dc by clamping and after clipping is utilized as bias for a pulse forming UJT circuit [**30].**

Krishnan Thadiappan et al. designed a thyristorised fastness control unit for a separately enthusiastic DC motor. This motor is nourished from a three phase entirely controlled thyristor bridge. A loop of proportional and integral maintains a desired speed irrespective of load **[31].**

Zhao Yongxi et al. BOD are thyristor overvoltage protection. If voltage threshold of BOD is so low that deed time will contend with decision. If threshold is very high that arrester of capacitor overvoltage protection will endure heat damage. The article introduces BOD procedure arrangement. Threshold effect is studied with action time and arrester energy. With simulation calculation threshold effect rule is summarised and design numerical value is got **[34].**

J. S. Ford et al. A method of sensing current zeros in thyristor convenors is designated. The technique employs an optically coupled isolator to sagacity the voltage across each of the thyristors in the convertor, thus sensing the transference state of each device. This information is then handled by modest logic to sense current zeros from the convertor **[35].**

1.3PURPOSE

The purpose of this thesis is to design and build single phase controlled rectifier using thyristor as a switch. The output waveform of a bridge rectifier can be controlled byadjusting the firing angle of thyristor that produce a variable output waveform.

1.4 OBJECTIVE OF THE THESIS

1. To study controller circuit for SCR drives and single phase full wave bridge rectifier circuit.
2. Design and construct control circuit.
3. To design and build single phase full wave bridge rectifier circuit using four thyristor and implement on the hardware.
4. Design of sinusoidal oscillator

1.5 SCOPE OF THE THESIS

A full wave controlled rectifier converts AC voltage to variable DC voltage. The main part of the dissertation is to build rectifier control circuit. Further, there are thyristor as a controlled for adjusting firing angle in the control circuit. The control circuit comprising multiple sub circuits such as sinusoidal oscillator, pulse generator circuit, cosine integrator, comparator, logic circuit and driver circuit which will be explained more on chapter two later on. The load used is resistive and inductive load, which is suitable for basic design of full wave rectifier.

Each of the control sub-circuit was designed, modelled and simulated using Multisim software and finally implemented on bread board.

1.6 ORGANISATION OF THE THESIS

This thesis consists of five chapters.

In Chapter One, it discuss about the overview, background, literature review, objective, problem statement and scope of the thesis.

In Chapter Two, it discuss about the Thyristors and its conduction and rectifier theory

In Chapter Three discusses about methodology used to enterprise the control circuit of 1-phase full bridge controlled rectifier and also the simulation of the rectifier circuit is studied and executed before moving to the hardware implementation.

In Chapter 4 The result and discussion will be presented

In Chapter 5 conclusion and future Scope

CHAPTER 2

THYRISTORS AND IT'S CONDUCTION

2.1 INTRODUCTION

Thyristor recommended by William Shockley in 1950 and campaigned by Moll and others at Bell Labs was advanced in 1956 by power engineers at General Electric, directed by Gordon Hall and commercialized by G.E.'s Frank W. "Bill" Gutzwiller. [4]

Today SCR has steered the uprising in the control of electric power that is in the arena of power electronics. About 70% of electric power is consumed by power electronics apparatus, and it is expected to grow in future. Previously gas occupied tube device called a thyratron provided a related electronic switching ability, where a minor control voltage might switch a large current. It is from an arrangement of "thyratron" and "transistor" that the word "thyristor" is originated. [1]- [5]

SCR is the name known to a universal family of three terminal devices that exhibit inherent regenerative action in their operation. The basic thyristor is a four layer p-n-p-n structure. These devices are widely used in static power converters such as switches, choppers, inverters, and cycloconverters which provide static means of ac and dc power control. The commercially available thyristors have current ratings in excess of 5 KA, and the voltage ratings extended beyond 10 KV.

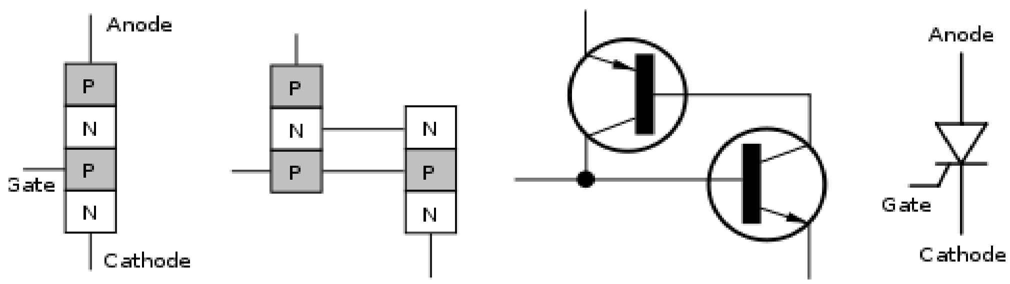


Figure 2.1 the construction of the SCR on physical and electronic identification, Symbol

The device consists of four regions p_1, n_1, p_2, n_2 and three layers junction J_1 , J_2 and J_3 .The p_1 region is referred to as anode , n_1 and p_2 -regions are called bases and the n_2 -region as the cathode. The fabrication of the devices starts with a high resistivity n-type **Si** wafer that forms

n_1-base .Simultaneously p-type diffusions are performed into the two sides of the wafer, resulting in junction J_1 and J_2 which are nearly symmetrical.[1] The heavily doped n_2-region is then produced on one side either by diffusion or by alloying. Finally, ohmic constants are made to the anode, cathode, and p_2-region which serves as the gate electrode. n^- n^+ p^+

2.2 BASIC STRUCTUE AND TERMINALS CHARACTERISTICS

Anode (A) and cathode (K) are the main terminals and on state can be controlled by gate (G) signal and no control on off state i.e. why SCR is called as semi-controlled device.

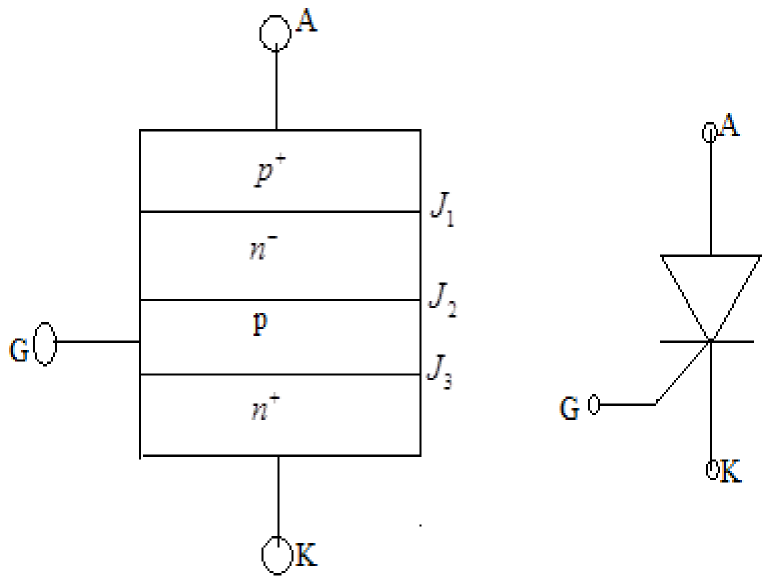


Figure 2.2 Thyristors symbol and three pn-junctions

2.2.1 FORWARD BLOCKING MODE

Once the anode voltage is made positive w.r.t the cathode, the junction J_1 and J_3 are forward biased .The junction J_2 is reversed biased, and only a small amount of leakage current flows from anode to cathode. The thyristor is said to be in forward blocking mode or off-state.

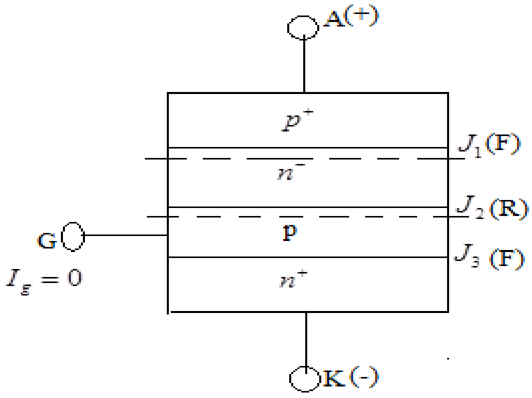


Figure 2.3 shows the depletion layer at J_2 blocks the entire forward voltage

2.2.2 FORWARD CONDUCTION MODE

When voltage from anode to cathode (V_{AK}) is amplified to an appropriately large value, the reverse biased junctions J_2 breaks. This is known as avalanche breakdown and the corresponding voltage is known as forward breakdown voltage (V_{BO}) when $I_g = 0$.

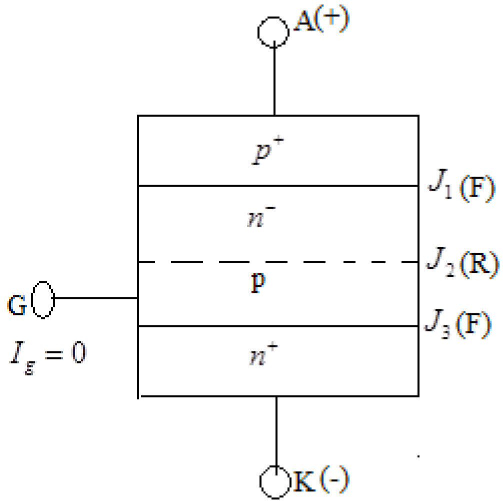


Figure 2.4 shows the forward conduction mode when breakdown occurs at J_2

Due to the breakdown of junction J_2 thyristors turned on.

At $I_g = 0$, $V_{BO} \simeq V_{BR}$ for symmetrical SCR

This method is not preferred to turn on the SCR because SCR may destroy due to high power loss when triggered at high voltage without gate signal.

2.2.3 SIGNIFICANCE OF GATE SIGNAL

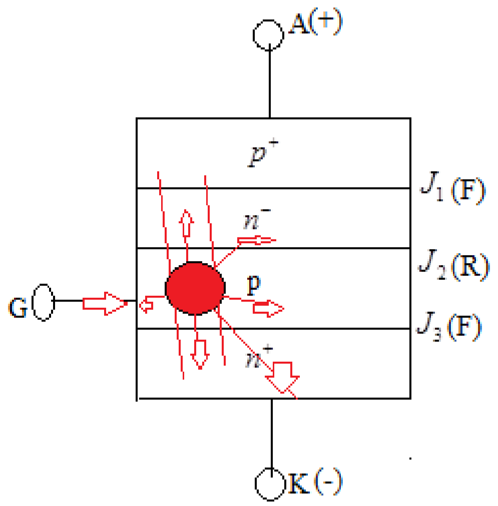


Figure 2.5 Significance of Gate signal

Gate specification is specified by:-

$$I_{g(\min)} \le I_g \le I_{g(\max)} \qquad (2.1)$$

$$V_{g(\min)} \le V_g \le V_{g(\max)} \qquad (2.2)$$

When $I_g \uparrow or \frac{dI_g}{dt} \uparrow \Rightarrow$ initial conduction area increases

$\Rightarrow \frac{dI_A}{dt} \uparrow$ (Initial rate) $\Rightarrow V_{BO} \downarrow$ (Therefore depletion layer around J_2 decreases).

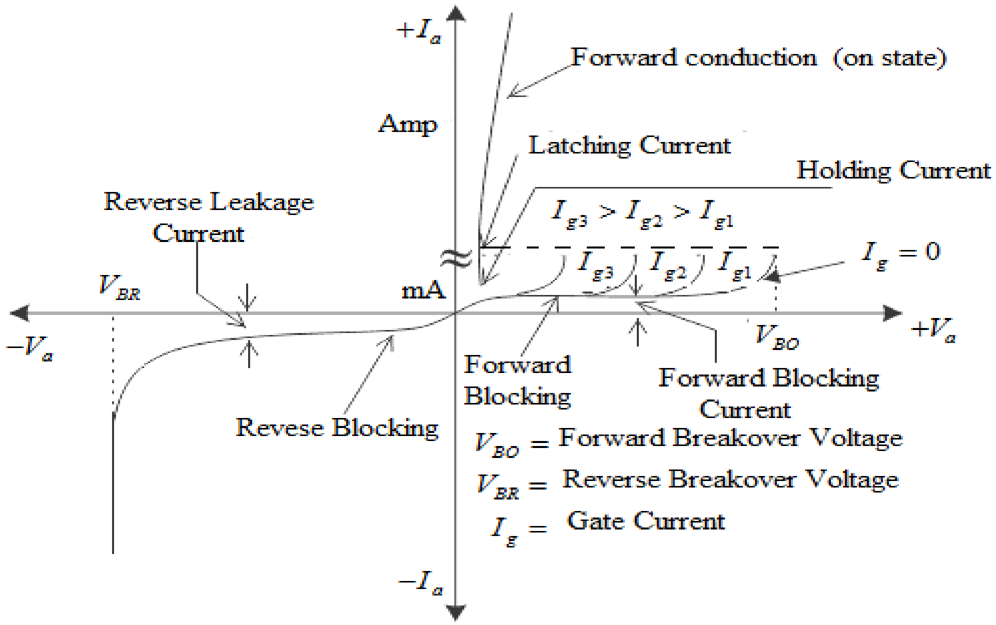


Figure 2.6 V-I characteristics of Thyristors

2.2.4 REVERSE BLOCKING MODE

J_2 has very low reverse blocking capability (V_{BR} is less than in either case or direction).Here J_1 and J_3 is responsible to block reverse voltage.

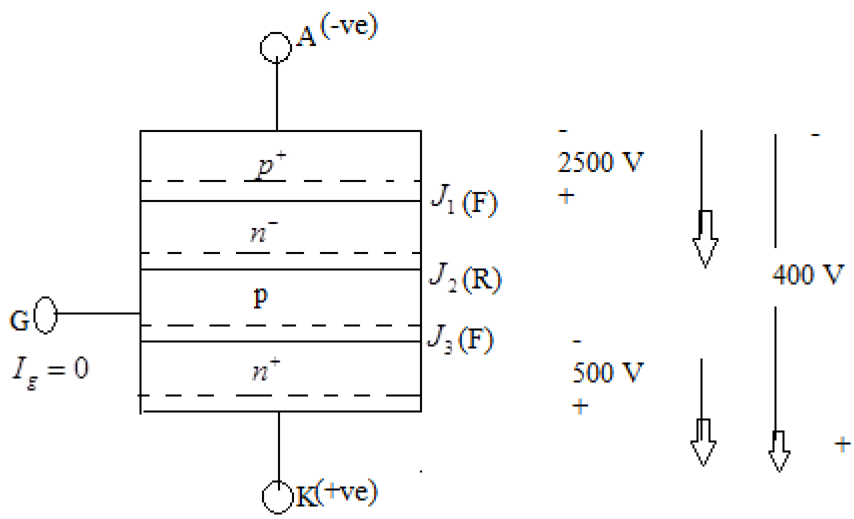


Figure 2.7 Reverse Blocking Mode

When a positive gate signal is given to a reverse biased thyristor then J_1 blocks the complete reverse voltage, this commutatively increases the power loss and temperature leakage current. Finally the SCR is thermally damage at J_1 this phenomenon is known as thermal runway.

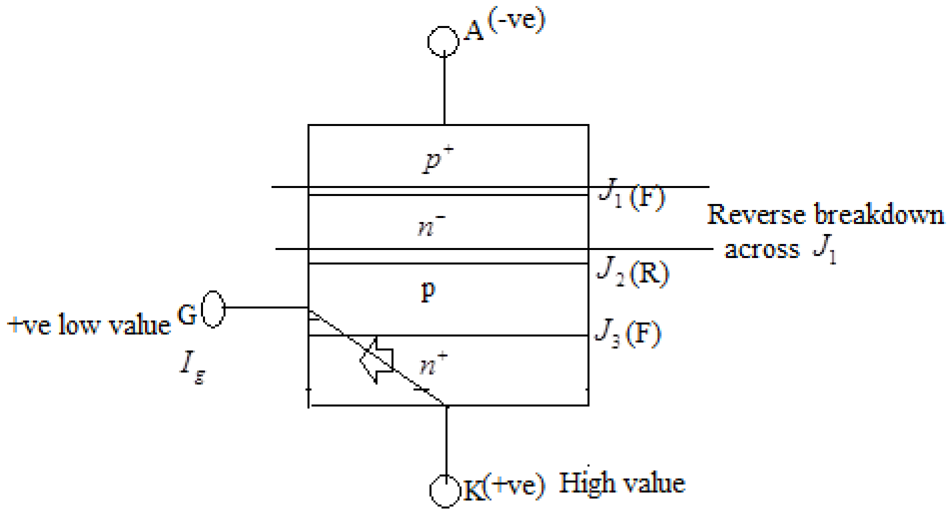


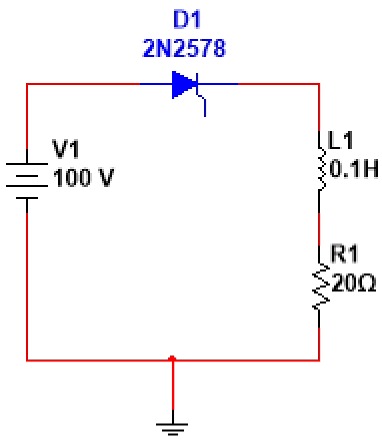
Figure 2.8 positive gate signal given to reverse biased thyristor

2.2.5 SIGNIFICANCE OF LATCHING CURRENT

1. Latching current is related to turn-on process
2. Gate signal initiates the turn-on process but once the SCR is in ON state, gate loses control on the device. Therefore we remove the gate signal when SCR becomes ON in order to avoid the continuous gate power loss.
3. If we remove the gate signal when anode current is lesser than the latching valve than SCR fails to turn-on. Therefore , we must maintain the gate pulse width at least for a period until anode current reaches certain minimum value(that minimum value is known as Latching current)
4. Therefore latching current is specified to estimate the lowest gate pulse width requirement to Switched on the SCR.
5. The minimum gate pulse width requirement depends on latching current and load circuit parameter.[3]
    1) If latching current increases, then the minimum pulse width of gate signal increases.

2) If the load inductance increases then also, minimum pulse width of gate signal increases.

6. The minimum gate pulse width is required to turn-on SCR is



$$I_A = \frac{V_S}{R}(1 - e^{-Rt/L}) \qquad (2.3)$$

$$I_A = 5(1 - e^{-200t})$$

$$I_L = I_A$$

$$I_L = 5(1 - e^{-200t_{\min}}) = 100 \times 10^{-3} \qquad (2.4)$$

$$1 - e^{-200t_{\min}} = 20 \times 10^{-3}$$

$$t_{\min} = 10\mu s$$

2.2.6 SIGNIFICANCE OF HOLDING CURRENT

1. Holding current is related to turn-off process.

2. Gate signal has no control to turn-off the SCR. In some of the cases when the supply is dc we require commutation circuit to turn-off the SCR

3. Commutation forces the anode current to below holding current to stop conduction of SCR.

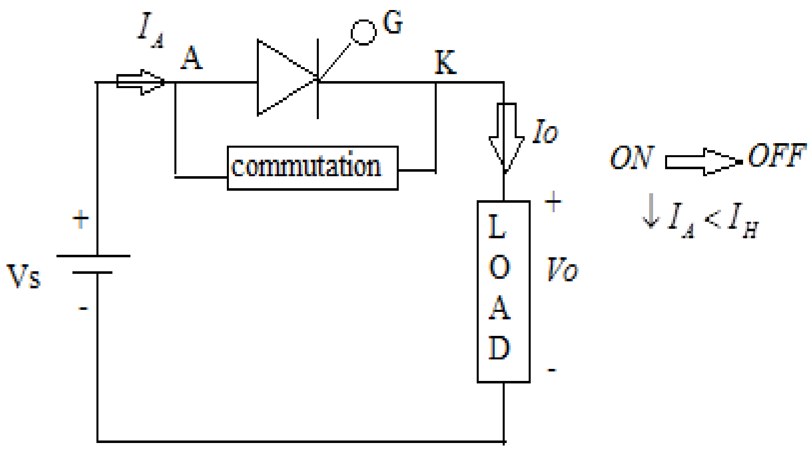


Figure 2.9 circuit diagram

$t_q = t_{rr} + t_{gr}$

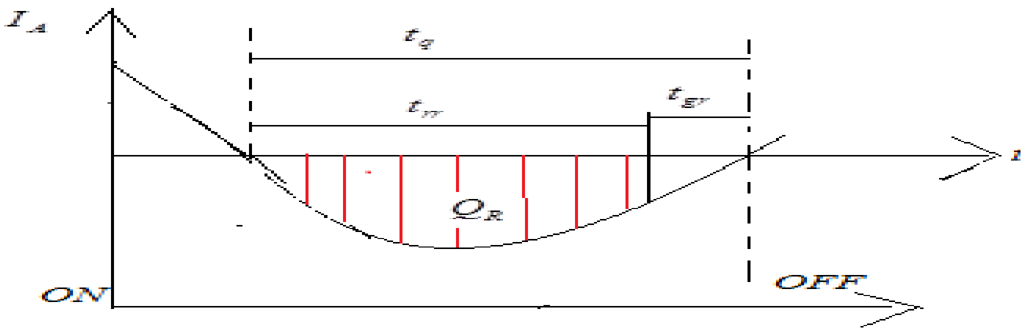


Figure 2.10 graphs shows the significance of Holding current

t_{rr} - Reverse retrieval time

t_{gr} -gate retrieval time

t_q -Device turn-off time

4. During device turn-off time t_q , all the excess charge carriers are completely removed in the device.

5. Role of commutation circuit :-Commutation circuit force the anode current to reduce below a certain minimum value (that minimum value is known as Holding current) and then applied reverse voltage across the SCR at least for a period until the complete excess charge is removed.

6. Circuit turn-off time (t_c):-Circuit turn-off time is the time for which commutation circuit applies reverse voltage across the SCR after the anode current becomes zero. It must always be greater than turn-off time (t_q) for successful commutation, otherwise commutation fails. If $t_c < t_q$. Some excess charges still present in the device, SCR did not recover completely. For the next operation if anode is made positive w.r.t. cathode then SCR will turn-on immediately before the gate signal is given. Here, SCR behaves as a diode losing the forward blocking capability. This is known as commutation failure .Therefore, if $t_c < t_q$ then commutation fails.

7. Definition of Holding current:-It is the minimum anode current below which SCR stops conducting and regains the forward blocking capability when the reverse voltage is applied across the SCR at least for a period of t_q or greater than that .($t_c > t_q$). [1]- [6]

2.3 SWITCHING CHARACTERISTICS OF SCR

2.3.1. DELAY TIME

It depends on gate signal magnitude and $\frac{d}{dt}$ (gate signal magnitude) that will be increase the initial conduction area .Therefore, original amount of increase of anode current increases .($\frac{dI_A}{dt}$ increases). Delay time t_d reduces and therefore, t_{ON} also reduces.

2.3.2 RISE TIME

It depends on the load parameters.

Example - $L \uparrow \Rightarrow \frac{dI_A}{dt} \downarrow \Rightarrow t_r \uparrow \Rightarrow t_{ON} \uparrow$ (If inductance increases then rate of change of anode current decreases and thus it results in the increase of rise time .Therefore thyristor turn-on time (t_{ON}) also increases.

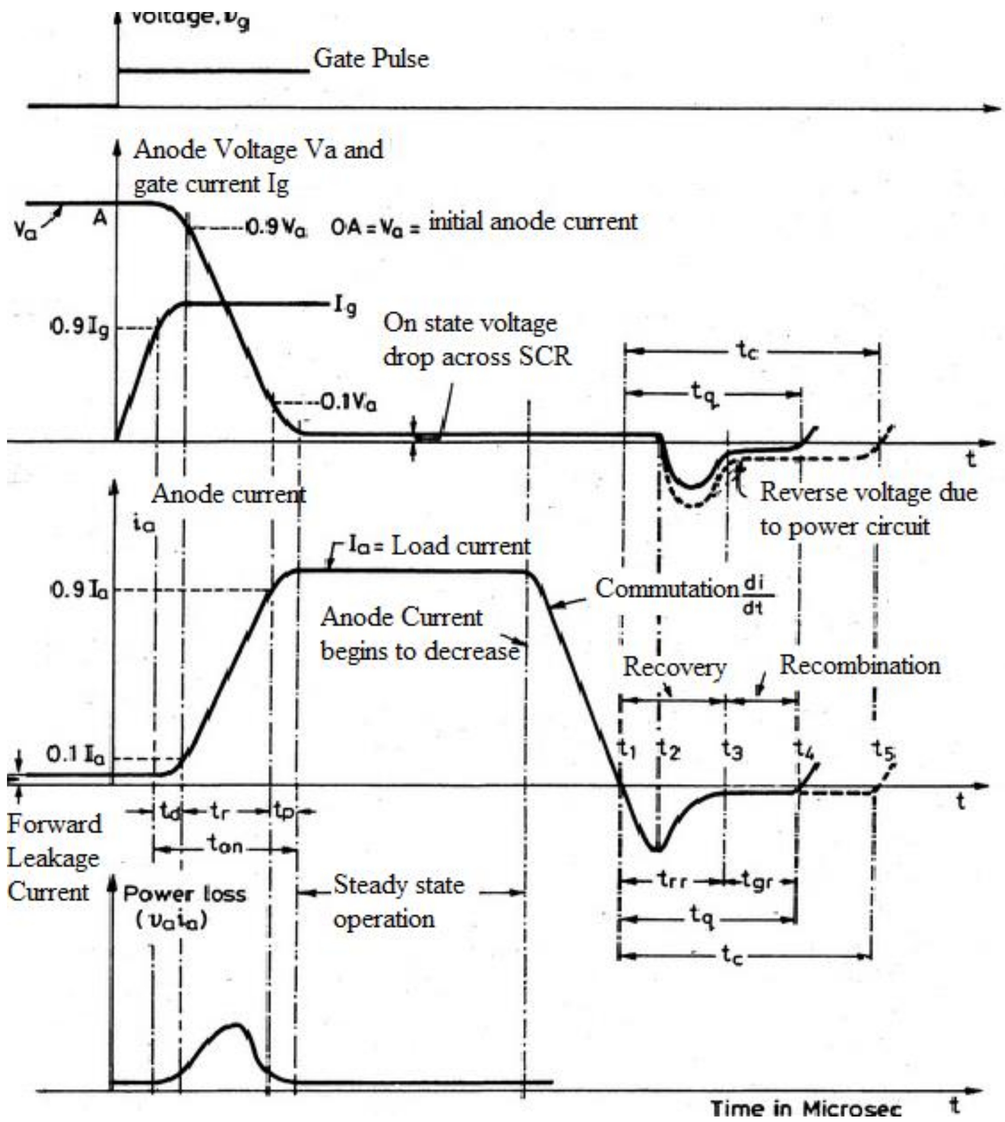


Figure 2.11 Switching characteristics of SCR

2.3.3 SPREAD TIME

During spread time, the current density spreads throughout the cross-sectional area of the SCR. Therefore spread time depends on the physical geometrical structure of the device. During reverse recovery time the additional charge carriers existing in the outer layers are removed. During gate recovery time the extra charge carriers present in the inner layers near the gate junction is removed. [1]

2.3.4 SAFETY FACTOR (SF) or SAFETY MARGIN (SM)

Safety margin should be greater than 1 for successful commutation.

$t_c \geq t_q$ For successful commutation.

$t_c = (SF) t_q$ (2.5)

$SF \simeq 2$ If not given

2.4 TURN-ON METHODS OR TRIGGERING METHODS OF SCR

2.4.1 FORWARD VOLTAGE TRIGGERING METHOD

$V_{AK} \uparrow \Rightarrow V_{BO}$, Breakdown occurs at j_2 .Therefore SCR turn-on. This method is not preferred generally because SCR may destroy when it is turn-on at such a high voltage due to high power loss.

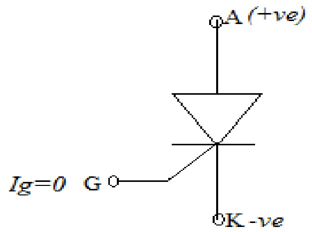


Figure 2.12 forward voltages triggering of SCR

2.4.2 dv/dt TRIGGERING METHOD

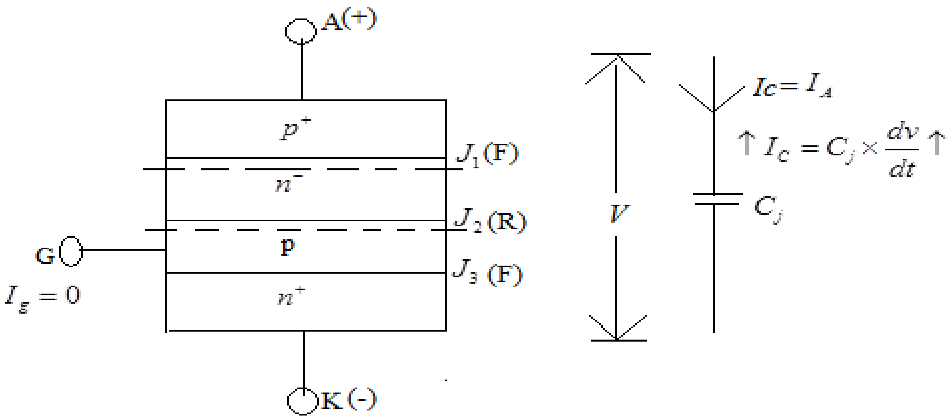


Figure 2.13 dv/dt Triggering

If the amount of rise of the anode to cathode voltage is high, the charging current of the capacitive junction may be enough to turn-on the SCR ($\uparrow I_C = C_j \times \frac{dv}{dt} \uparrow$).At high dv/dt the charging circuit increases. If the increases in charging current is more than latching value of current, then SCR will turn-on.

2.4.3. LIGHT TRIGGERING METHOD

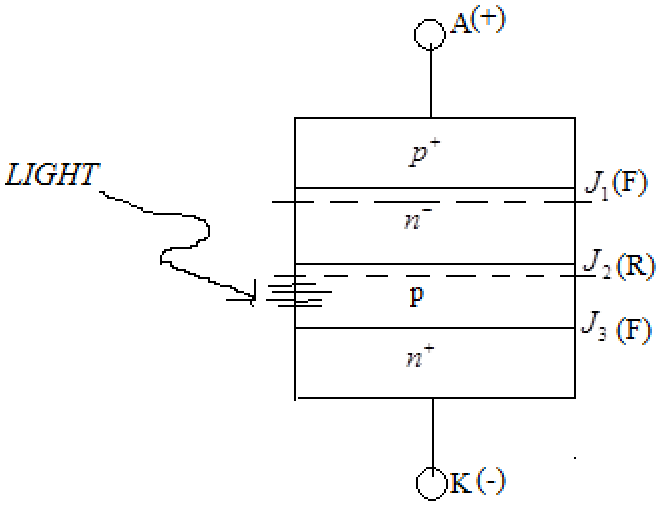


Figure 2.14 Light Triggering Method

When the light radiation of certain wavelength is incident near the depletion layer then large t no. of electron hole pairs is formed in the depletion layer via absorbing the light triggering, this initiates the turn-on process.

Example: - light triggering is used in LASCR for HVDC applications. Light triggering is more efficient and reliable to trigger multiple no. of SCR's simultaneously.

2.4.4 THERMAL TRIGGERING

When temperature is increased near the reverse biased depletion layer then more no. of electron hole pairs are produced in the depletion layer by absorbing the thermal energy, this initiates the turn-on process. This method is not preferred generally because temperature changes the characteristics of the SCR.

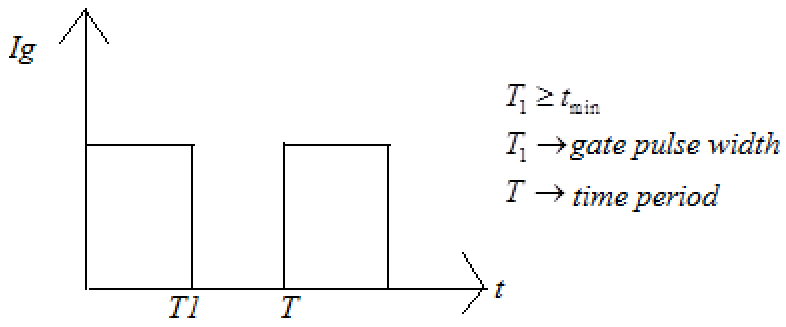
2.4.5 GATE TRIGGERING METHOD

If the SCR is forward biased, the injection of gate current by applying positive gate voltage between the gate terminals turns-on the SCR.

1. Continuous Gate Signal

In this we provide continuous gate signal until it is in an ON-state, this is not an efficient method due to continuous gate power loss.

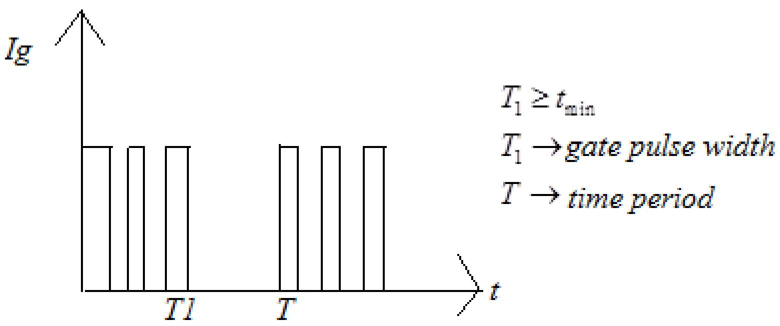
2. Pulse Gate Signal



Duty cycle, $\delta = \frac{T_1}{T}$ (2.6)

Mark to space ratio, MSR = $\frac{T_1}{T - T_1} = \frac{\delta}{1-\delta}$ (2.7)

3. **High Frequency Gate Pulse**



We can reduce the size of pulse X^r by using high frequency gate pulse. Pulse X^r provides electrical seclusion among the high power main circuit and low power gate firing circuit. We can trigger more than one SCR simultaneously by using pulse X^r .[1]-[5]

2.5 FIRING CIRCUITS OF THE SCR

Firing circuit use the necessary gate pulse to turn-on the SCR.

1. Resistive Firing Circuit

$$(I_g)_{\min} \le I_g \le \left(I_g\right)_{\max}$$
$$(V_g)_{\min} \le V_g \le (V_g)_{\max}$$
$$I_g \rightarrow mA$$
$$V_s \rightarrow Volts$$
$$(R_1 + R + R_2) \rightarrow K\Omega$$
$$R_L \ll (R_1 + R + R_2)$$

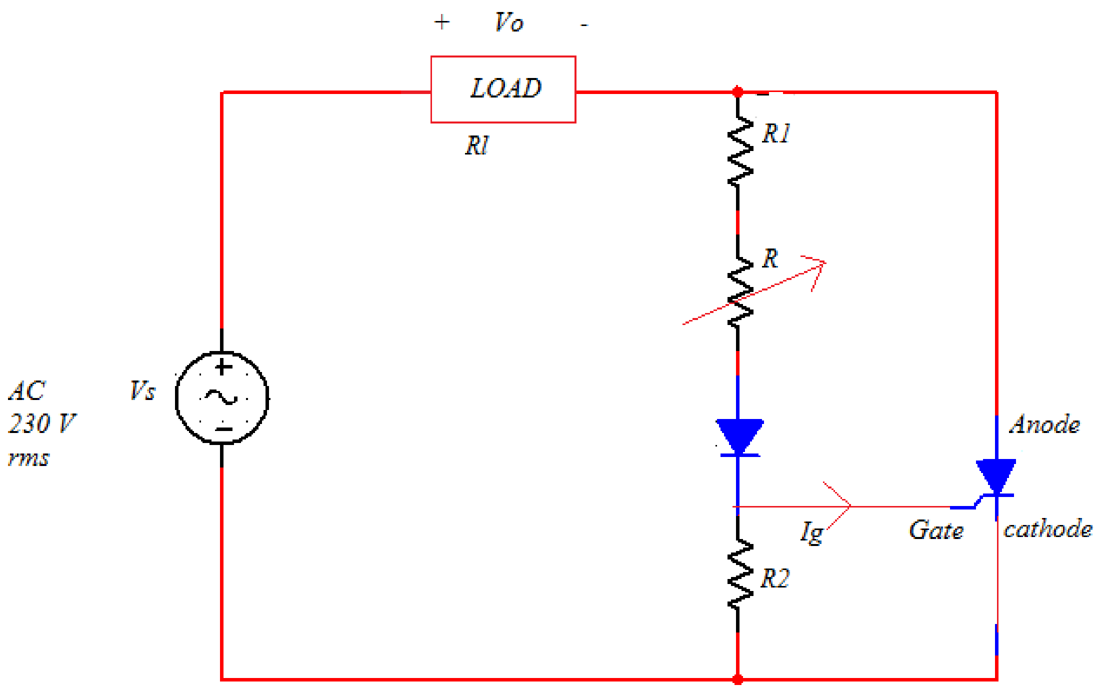


Figure 2.15 Main circuit of 1-phase half wave rectifier

Purpose of R_1

The purpose of R_1 is to limit the I_g within the maximum value .For worst condition, maximum gate current,

$$= \frac{V_m}{R_1} \le \left(I_g\right)_{\max} \qquad (2.8)$$

$$R_1 \ge \frac{V_m}{\left(I_g\right)_{\max}}$$

Purpose of R_2

We have to design the value of R_2 for limiting the V_g within the maximum value.

For worst condition, maximum gate voltage

$$= \frac{V_m \times R_2}{\left(R_1 + R_2\right)} \le \left(I_g\right)_{\max} \qquad (2.9)$$

From the above equation, we can find the design value of R_2 .

Purpose of R

Variable Resistance, R is used to vary the firing angle, α

Purpose of Diode

Diode is used to avoid the negative gate pulse in the negative cycle

$$V_g = \frac{V_m \sin \omega t \bullet R_2}{\left(R_1 + R + R_2\right)} \qquad (2.10)$$

$$V_g = \frac{V_m \bullet R_2}{\left(R_1 + R + R_2\right)} \bullet \sin \omega t$$

$$V_g = V_{gm} \sin \omega t$$

$$where, V_{gm} = \frac{V_m \bullet R_2}{\left(R_1 + R + R_2\right)} \qquad (2.11)$$

Gate turn-on Voltage (V_{gt})

When a gate voltage reaches V_{gt} **,** then SCR will turn-on.

If gate voltage is equal to gate turn-on voltage i.e. then SCR gets turned on at $\omega t = \alpha$.

$$V_{gm} \sin \alpha = V_{gt} \quad (2.12)$$

$$\alpha = \sin^{-1}\left(\frac{V_{gt}}{V_{gm}}\right) \quad (2.13)$$

α Increases when V_{gm} decreases, therefore increase in R decreases V_{gm} and thus α increases.

1. Let

$$R = R_a$$
$$\alpha = \alpha_a$$

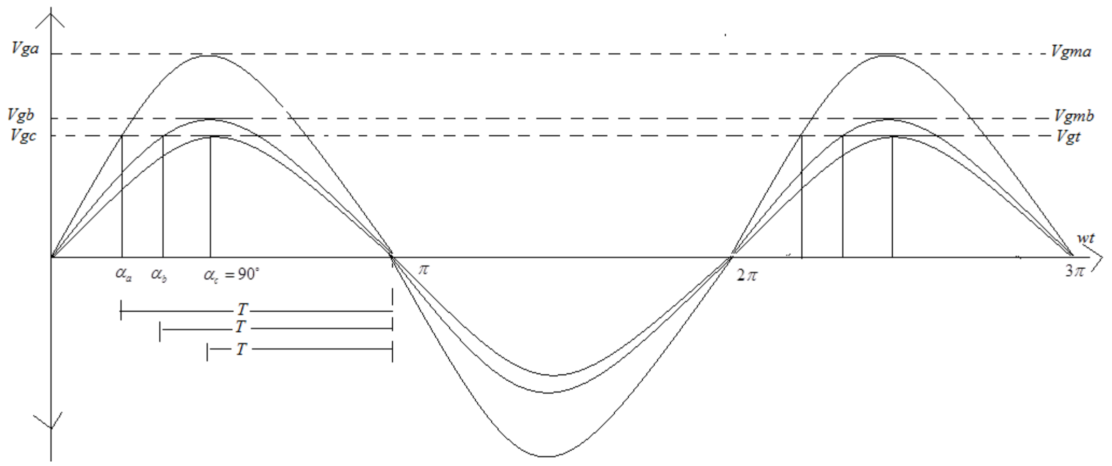
Then,

$$V_{gma} = \frac{V_m \times R_2}{(R_1 + R_2 + R_a)} \quad (2.14)$$
$$V_{ga} = V_{ma} \sin \omega t$$

2. If **R** increases then,

$$R_b > R_a, \alpha = \alpha_b$$

$$V_{gmb} < V_{gma}$$
$$V_{gb} = V_{gmb} \sin \omega t \quad (2.15)$$



$\alpha_c = 90^\circ$

Figure 2.16 shows the gate turn-on voltage characteristics

3. If

$$V_{gmc} = V_{gt} \qquad (2.16)$$
$$\alpha = \alpha_c = 90^0 \left(\alpha_{max}\right)$$

The maximum firing angle is limited to 90°.

2.6 PROTECTION OF THYRISTORS

2.6.1 OVER CURRENT PROTECTION

For overcurrent protection, we have to connect fuse or circuit breaker in series with the SCR.

2.6.2 OVER VOLTAGE PROTECTION

All metal oxide (e.g. ZnO) behaves as a non-linear resistors.

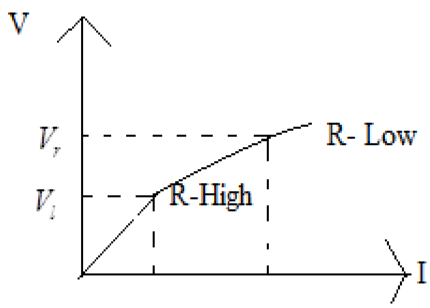


Figure 2.17 Bypasses changes at high voltage spikes

1. Varistors are connected across the SCR for over voltage protection .Varistors is a non-linear resistor.
2. All metal oxide resistors behave as non-linear resistors. (e.g. - ZnO gives good non-linearity)

2.6.3 $\frac{dV}{dt}$ PROTECTION

$$\uparrow I_c = C_j \bullet \frac{dV}{dt} \uparrow \qquad (2.17)$$

Effect of high $\frac{dV}{dt}$

1. At high $\frac{dV}{dt}$, SCR may turn-on before the gate signal is given .This unwanted turn-on is known as false turn-on.

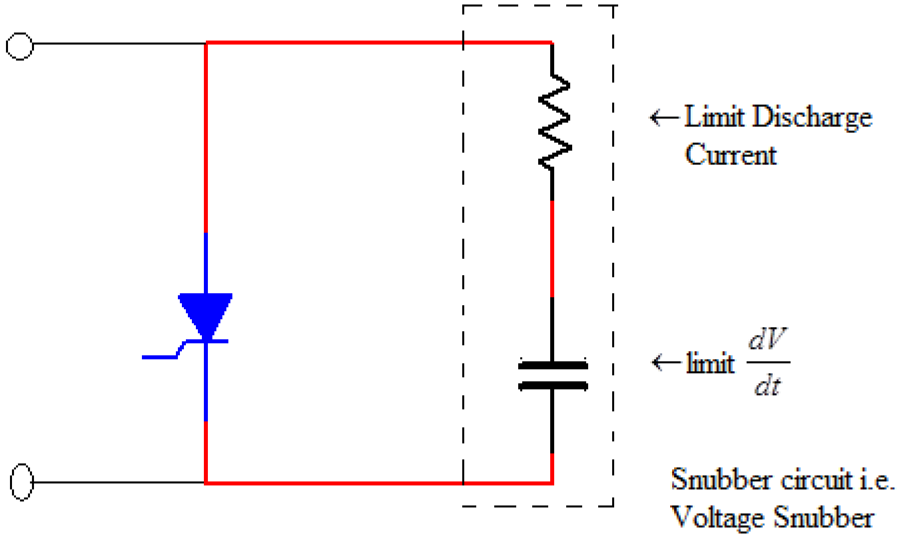


Figure 2.18 Circuit diagram with snubber circuit

2. We must connect an RC circuit across the SCR against high electrical stress ($\frac{dV}{dt}$ **or** $\frac{di}{dt}$ stress) during switching operations.

$$I_c = C_j.\frac{dv}{dt} \quad (2.18)$$

$$I_L = C_j.\left(\frac{dv}{dt}\right)_{critical}$$

$$\left(\frac{dV}{dt}\right)_{critical} = \frac{I_l}{C_j} \quad (2.19)$$

$\left(\frac{dV}{dt}\right)_{critical}$ Is the value of $\frac{dV}{dt}$ at which **the** SCR will be false turn-on of applied $\frac{dV}{dt}$ is more than this critical, then SCR may false turn-on.

4. $\frac{dI_A}{dt}$ Protection

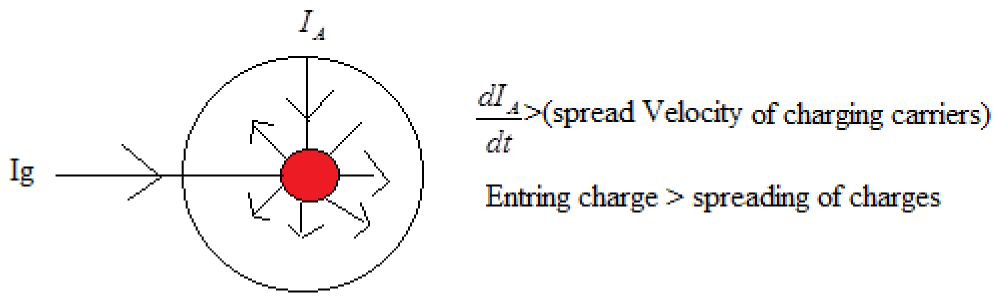


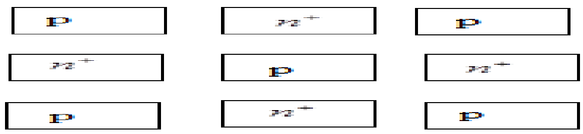
Figure 2.19 shows the spread velocity of charging carriers

Affect of $\frac{dI_A}{dt}$

1. If $\frac{dI_A}{dt}$ is higher than spread velocity of charge carriers the charge density increases commutatively in a small conduction area and results in local hot spots damaging the device.
2. We must connect inductor in series with the SCR for $\frac{dI_A}{dt}$ protection.
3. Methods to improve $\frac{dI_A}{dt}$ rating:-
    1. By increasing the gate signal magnitude or $\frac{d}{dt}$ (gate signal magnitude).
    2. Structural Modification:-
        a. Centre gated thyristor
        b. Side gated thyristor

        The $\frac{dI_A}{dt}$ rating is higher in centre gated thyristor when compared to the side gated thyristors.

3. Intedigitation Method:-



4. Manufacturing cost is high

In this method, we intermix gate-controlled regions in large proportions; this increases the initial conduction area and hence $\frac{dI_A}{dt}$ rating.

5. Thermal Protection

Thyristors gets over heated due to its initial power loss, therefore thyristor is mounted in heat sinks which absorb the internal power loss and cool the device. [3]

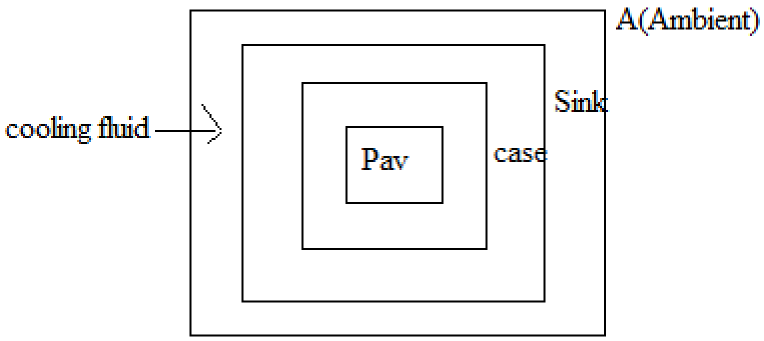


Figure 2.20 shows the heat sink structure for the thermal protection of thyristors

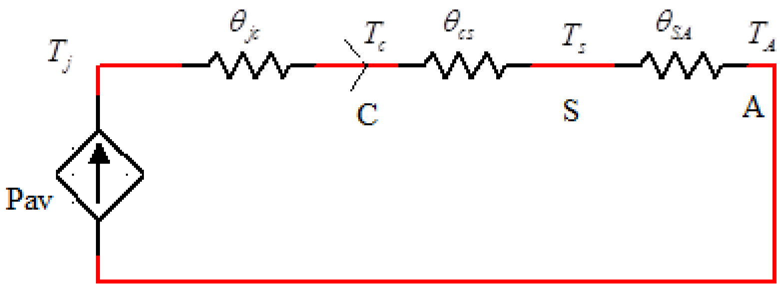


Figure 2.21 shows the circuit diagram for thermal protection

Here, θ is the thermal resistance. ($\circ_C / w$).

$$P_{av} = \frac{T_j - T_C}{\theta_{jc}} = \frac{T_C - T_A}{\theta_{cs}} = \frac{T_j - T_s}{\theta_{jc} + \theta_{cs}} = \frac{T_c - T_A}{\theta_{cs} + \theta_{sA}} \quad (2.20)$$

$$= \frac{T_j - T_A}{\theta_{jA}}; \theta_{js} = \theta_{jc} + \theta_{cs} + \theta_{sA}$$

$$P = I^2 R_F \Rightarrow I \alpha \sqrt{P} \quad (2.21)$$

Therefore, increase in rating of SCR is directly proportional to

$$\alpha \sqrt{P_{av} \uparrow}$$

$$\alpha \sqrt{\frac{T_j - T_A \downarrow}{\theta_{js}}}$$

Rating of SCR depends on the cooling methods used for heat sink.

6. Gate Protection

1. Connect the resistance in series with the gate to limit the I_g within the (I_g)max.

2. Connect the zener diode across gate cathode terminals for over-voltage protection.

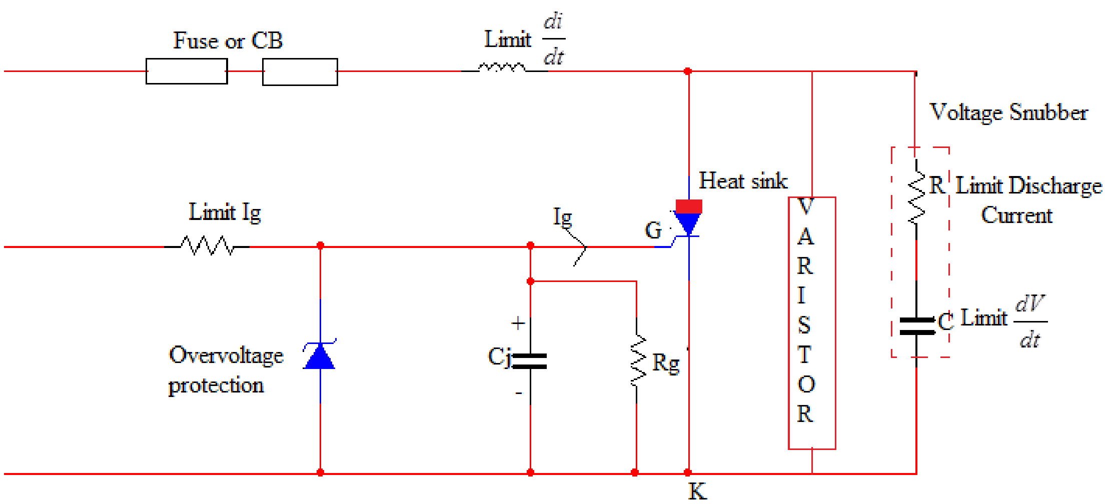


Figure 2.21 circuits for the gate protection of thyristors

Noise is an unwanted signal in the firing circuit .This noise signal may false turn-on the SCR. We must connect parallel RC across gate cathode terminals to protect the SCR against the noise signals.

Series and Parallel connections of SCR

We must connect some of the SCR's in series and parallel combination in order to improve the voltage and current capabilities.

1. **Series connection**

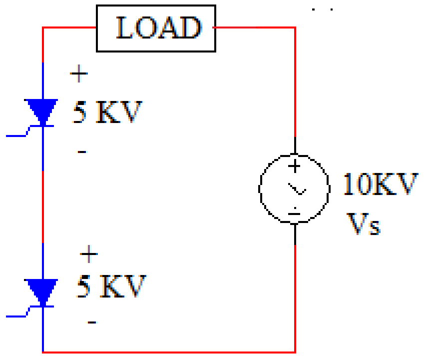


Figure 2.22 series connection of SCR

String Efficiency

It is a measure of utilizing the SCR's ratings.

String $\eta = \frac{\textit{Total string Voltage or current}}{n\ X\ \textit{individual voltage or Current rating of each SCR}}$

String efficiency η = 10/2*5 =1 or 100%

Derating factor

It is a measure of reliability of string .The mathematical formulae is

DRF = 1 – string η.

Problems Related to series connected thyristors:

1. Unequal sharing of voltage during the blocking state

The main reason of unequal sharing of voltage is due to the difference in forward blocking characteristics. To avoid such problem we have to connect static equalizing circuit.

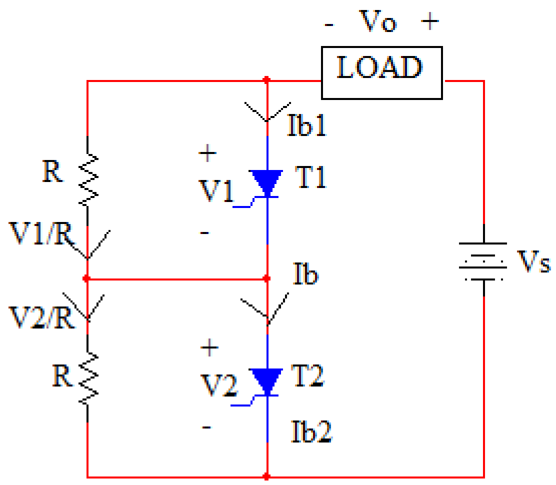


Figure 2.23 shows the circuit diagram of series connected SCR

$$R \geq \frac{n \bullet V_{bm} - V_s}{(n-1)\Delta I_b} \quad (2.22)$$

Where, V_{bm} is maximum blocking voltage

n is the no. of series connected SCR

V_s is the supply Voltage

$$\Delta I_b = I_{b(\max)} - I_{b(\min)} \quad (2.23)$$

$$\frac{V_1}{R} + I_{b1} = \frac{V_2}{R} + I_{b2}$$

KVL,

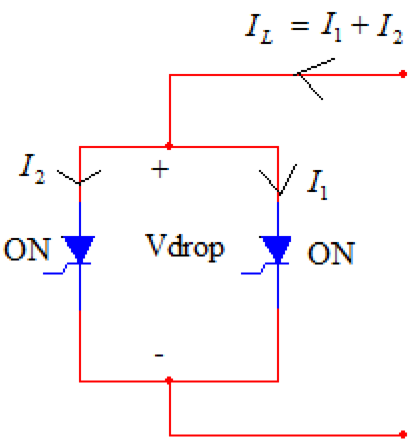
$$V_1 - V_2 = (I_{b2} - I_{b1})R \quad (2.24)$$

$$V_1 + V_2 = V_s$$

From solving the above equation we can find the values of V_1 and V_2

Problems related to parallel connected Thyristors

1. Unequal sharing of current



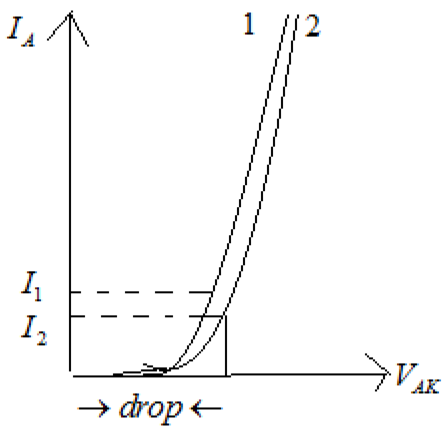


Figure 2.24 parallel connected SCR and their characteristics

Unequal sharing of current is due to the difference in forward conduction characteristics of the SCR.

In order to rectify such type of problem we have to use a current equalizing circuit.

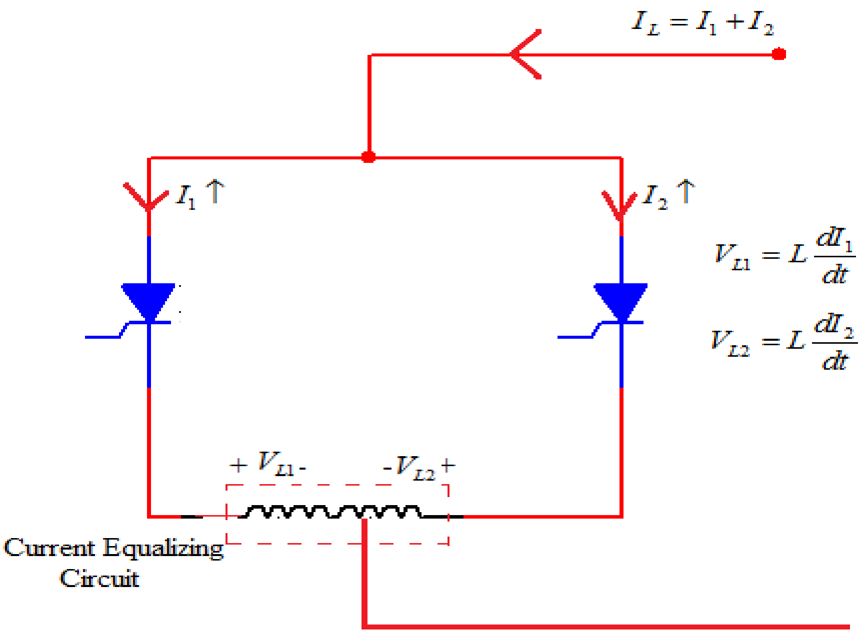


Figure 2.25 Current equalizing Circuit

Current equalizing Circuit works on Lenz's law concept.

$$I_L = \uparrow I_1 + I_2 \downarrow = \text{Constant} \tag{2.25}$$

$$V_{L1} = L\frac{dI_1}{dt} = +ve \text{ ; opposes increase of } I_{1,} \therefore I_1 \downarrow \tag{2.26}$$

$$V_{L2} = L\frac{dI_2}{dt} = +ve \text{ ; opposes decrease of } I_{2,} \therefore I_2 \uparrow \tag{2.27}$$

This continues until $I_1 = I_2$.

Whenever there is a change of current in any parallel path, then emf is induced in the reactor to oppose the change of current and then equalizes the current sharing in all parallel SCR's.

1. Unequal sharing of current is also due to the temperature difference in the parallel connected SCR's. We can use a common symmetrical Heat sink for all the parallel SCR's.

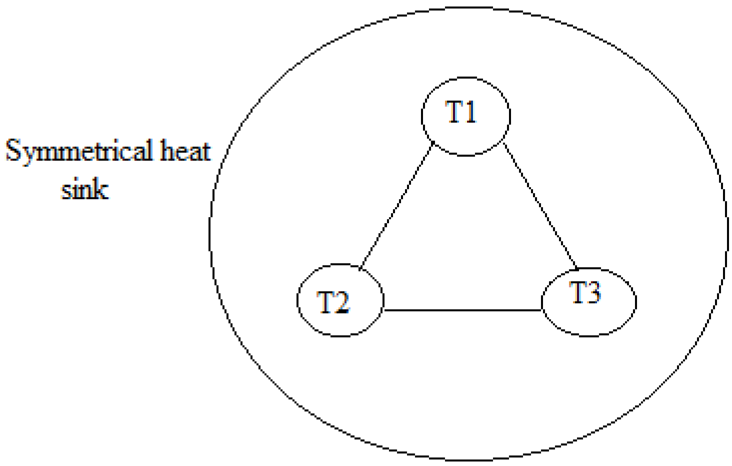


Figure 2.26 Symmetrical heat sink

2.7 APPLICATION OF SCR

The capability of a silicon controlled rectifier to regulate large currents to a load by means of lesser gate currents creates the device very useful in switching and control applications. Some of the promising applications of SCR are:

2.7.1 PHASE CONTROLLED RECTIFIER

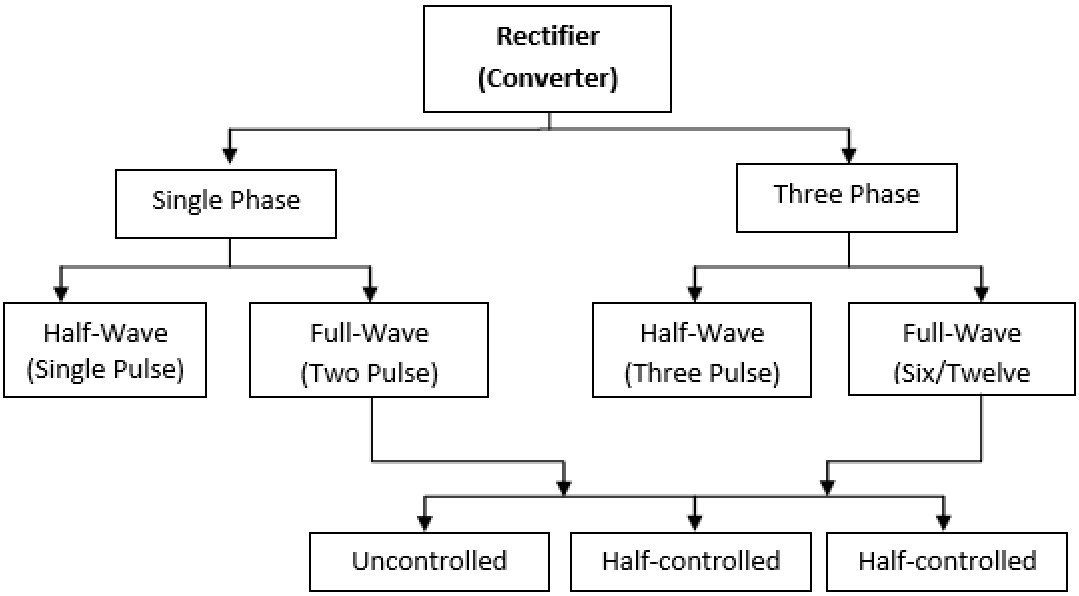
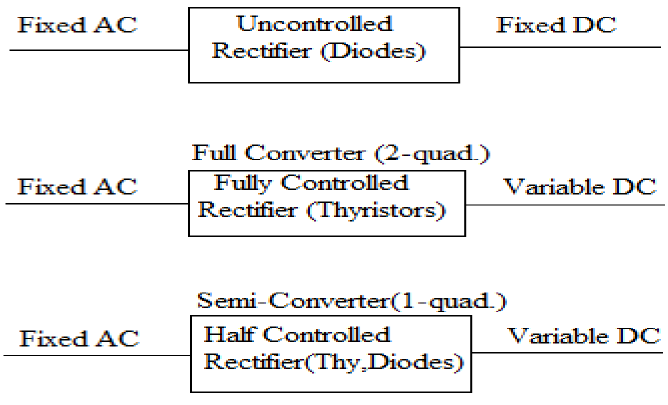


Figure 2.27 Single Phases and Three Phase Rectifier



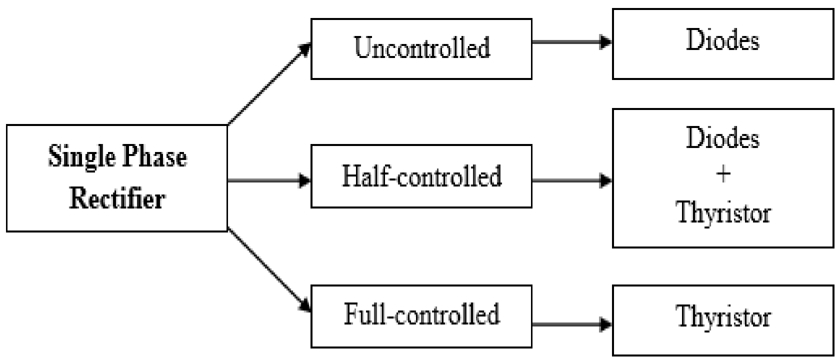


Figure 2.28 Electronic Switching Devices for Various Single Phase Rectifiers

2.7.2 CLASSIFICATION BASED ON PULSE NUMBER (m)

Pulse no. gives the no. of output pulse for one cycle of AC source voltage.

One pulse converter (1-ϕ HWR)

Pulse Length = $\pi or 180^\circ$, $f_o = f_s$

Two Pulse Converters (1-ϕ HWR)

Pulse length = $\frac{2\pi}{2} = \pi or 180^\circ$, $f_o = 2f_s$

Three pulse Converter (3-ϕ HWR)

Pulse Length = $\frac{2\pi}{3} = \left(\frac{4\pi}{6}\right) = 120^\circ$; $f_o = 3f_s$

Six Pulse Converters (3-ϕ HWR)

Pulse Length = $\frac{2\pi}{6} = \left(\frac{\pi}{3}\right) = 60^\circ$; $f_o = 6f_s$

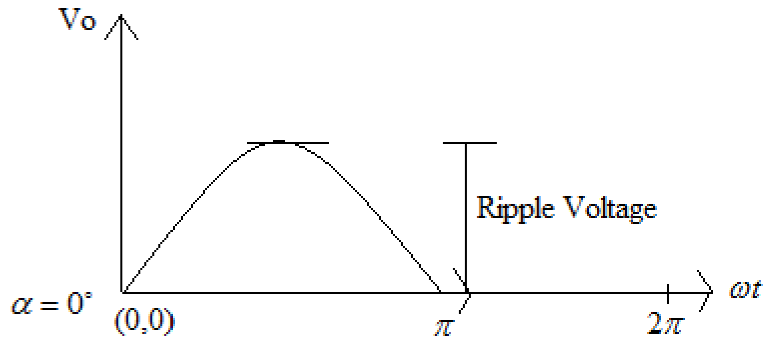


Figure 2.29 single pulse converters

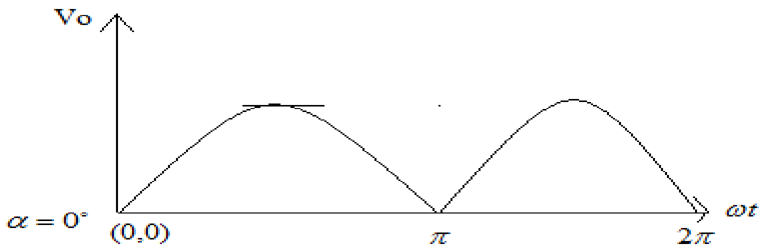


Figure 2.30 Two pulse Converters

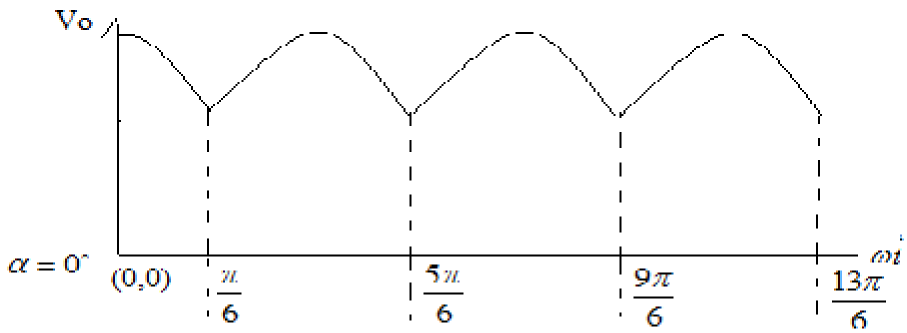


Figure 2.31 Three pulse Converters

2.7.3 SINGLE-PHASE FWR (2-PULSE CONVERTER)

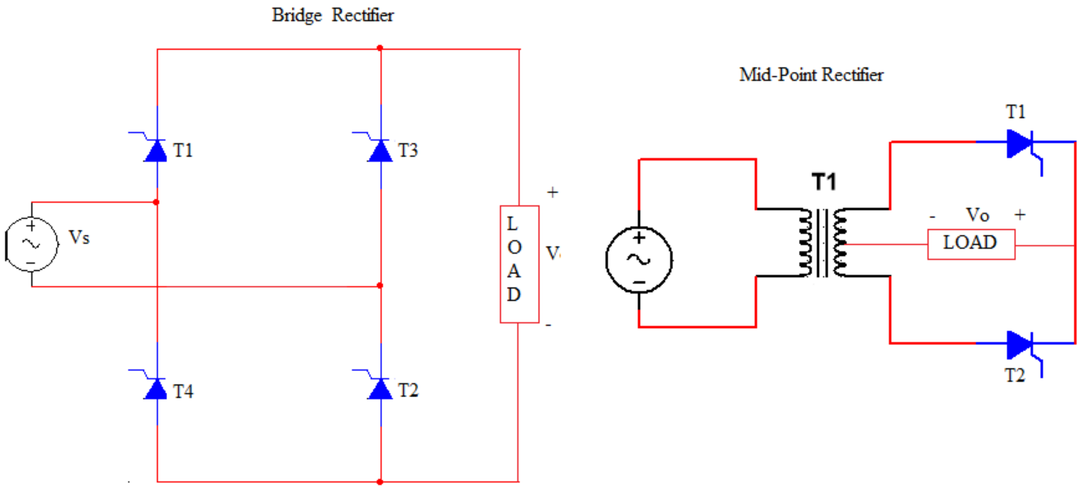


Figure 2.32 (a) two pulse two quadrant bridge converter and (b) midpoint rectifier

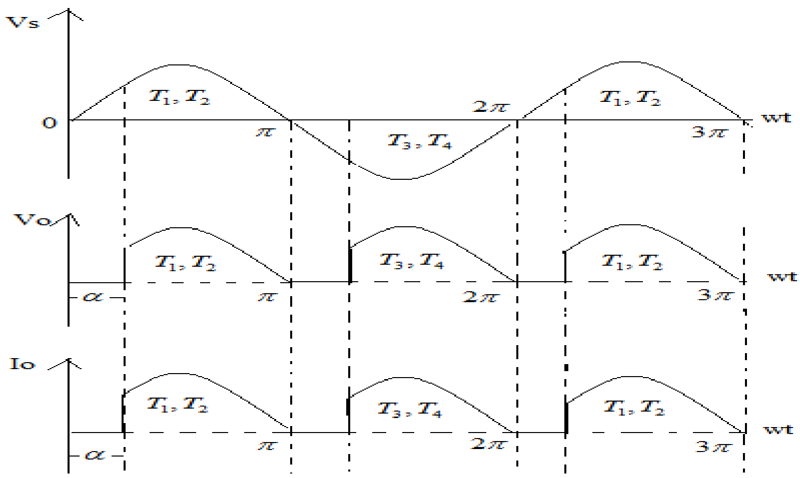


Figure 2.33 Theoretical waveforms of two pulse converters

The full-wave rectifier is the corresponding of dual half wave rectifiers. A full wave rectifier is a device that has two or more diodes prescribed so that load current drifts in the same direction throughout each half cycle of the AC supply. Slightly than half-wave rectifier, full-wave rectifier has certain fundamental advantages. The main advantage of full-wave rectifier is to harvest purely DC with fewer ripples in the voltage or current. Besides that, the benefits of full-wave rectifier is likewise stated by Daniel W. Hart (1997), "the average current in the ac source is zero in the full wave rectifier, thus circumventing problems associated with nonzero average source currents, mainly in transformer."

OPERATION OF FULL WAVE RECTIFIER

When T_1, T_2 is on then,

$$V_o = V_s \quad (2.28)$$

$$I_o = \frac{V_s}{R} \quad (2.29)$$

When T_3, T_4 is on then,

$$V_o = -V_s \quad (2.30)$$

$$I_o = -\frac{V_s}{R} \quad (2.31)$$

2.8 ADVANTAGE OF BRIDGE RECTIFIER

1. The PIV of the thyristor in bridge rectifier is half of that when compared with the midpoint rectifier.

2. When thyristors with same ratings is used in both converters, then the average output voltage and power handled by the bridge rectifier is double that of midpoint rectifiers.

For application, usually inductive load is considered, hence current is assumed constant as load is same.

CHAPTER 3

IMPROVED COSINE CONTROL METHOD

3.1 INTRODUCTION

The class of firing schemes for thyristors consist of various digital and analog circuits used to create gate pulses which are given to the gate of the thyristors in order to trigger it. The two most famous method of firing angle control are Cosine control and linear control. The various circuits like UJT relaxation oscillator triggering, RC triggering, Ramp and Pedestrial

Triggering, etc undergoes the problem of limited firing angle. We cannot reduce the firing angle below α = 26° using such circuits, as the value of capacitor and resistor limits the firing angle. For the very precise control of firing angle, Cosine Firing Scheme (CFS) can be implemented. There are several version of this method. The pulses are generated at the crossing of control voltage V_c and ac line voltage. [14]

$$\alpha = \cos^{-1}\left(\frac{V_c}{V_m}\right); V_d = V_{do}\cos\alpha = kV_c \tag{3.1}$$

This control system results in linear transfer characteristics. Added advantage of CFS is that it can be controlled digitally using microcontrollers also, thus can be used in closed loop applications. A firing circuit should fulfil the three following criteria.

1. If the power circuit has more than single silicon controlled rectifier, the triggering circuit should yield gating pulses for each SCR at the ideal instant for proper procedure of the power circuit. These pulses essential be periodic in nature and the sequence of firing must correspond with the type of thyristorised power controller.
2. **Synchronization**: The basic requirement from a trigger control circuit is to produce sharp pulses at specific instant of time scale. These pulses appear at variable positions to make the control possible. It is said to have produced a definite and desired time delay from a specific mark. It is at this mark where from the time delay is counted.
3. The regulator signal produced by a firing circuit might not be able to turn-on an SCR. It is therefore mutual to produce the voltage pulses toward a driver circuit and then to gate-cathode circuit. A driver circuit involves of a pulse amplifier and a pulse transformer.

A common arrangement of firing circuit scheme is shown in Fig 1. A controlled DC power supply is obtained from an alternating voltage source. Pulse generator, supplied from ac and dc sources, gives out voltage pulses which are then fed to pulse amplifier for their amplification. Shielded cables transmit the amplified pulses to pulse transformers. The function of pulse transformer is to isolate the low-voltage gate-cathode circuit from high voltage anode-cathode circuit.

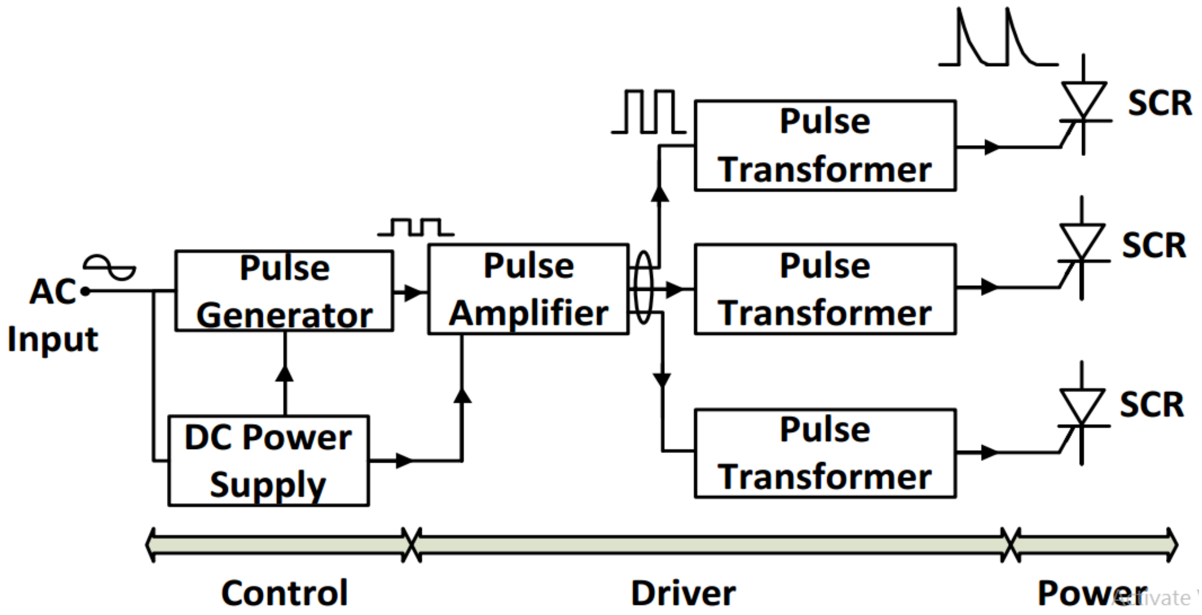


Figure 3.1 General Layout of the Firing circuit scheme for SCRs

3.2 BLOCK DIAGRAM REPRESENTATION OF IMPROVED CFS

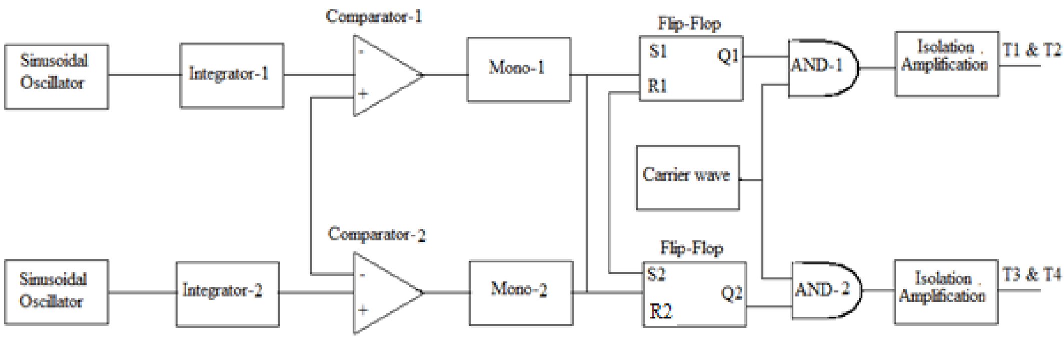


Figure 3.2 Block diagram of improved cosine firing scheme

3.2.1SINUSOIDAL OSCILLATOR

An Oscillator is the basic element of all ac signals of known frequency and amplitude. It is one of the basic and useful instruments used in electrical and electronic measurements. Sinusoidal oscillator constitute of operational amplifiers with RC or LC circuits that have unpredictable oscillation frequencies. Opamp sinusoidal wave oscillators function without an superficially functional input signals. Particular arrangement of +ve and -ve feedback is used to effort the Opamp into an uneven state causing the output to evolution back and forth at a continuous rate. The amplitude and the Oscillation frequency are set by the procedure of passive and active components around a central opamp**.**

Requirements for Oscillation

The acknowledged or simplest form feedback system is used to validate the requirements for oscillation to follow. The block diagram of this system is shown in the figure below:

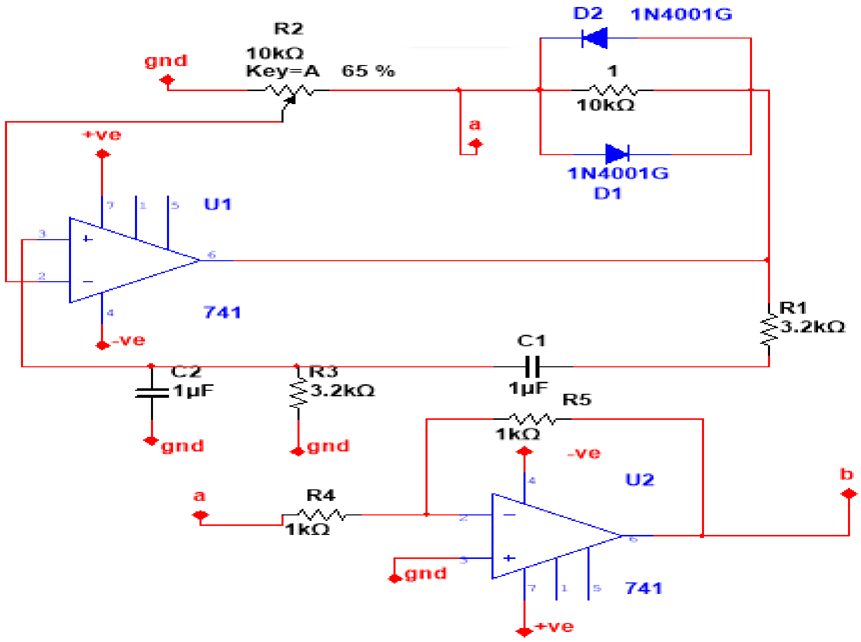


Figure 3.3 simulated circuit of sinusoidal oscillator with phase shift of 0 degree and 180 degree

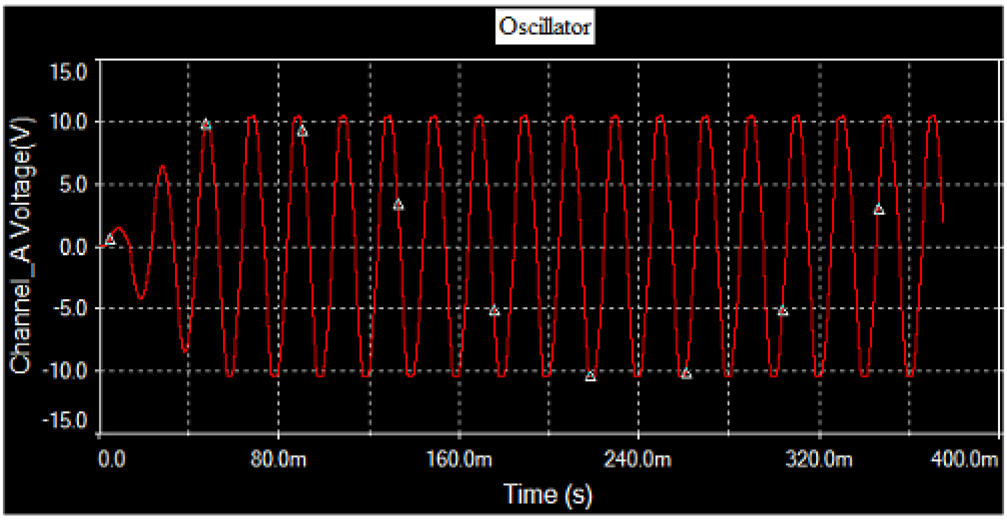


Figure 3.4 output of sinusoidal oscillator with 0 degree phase shift

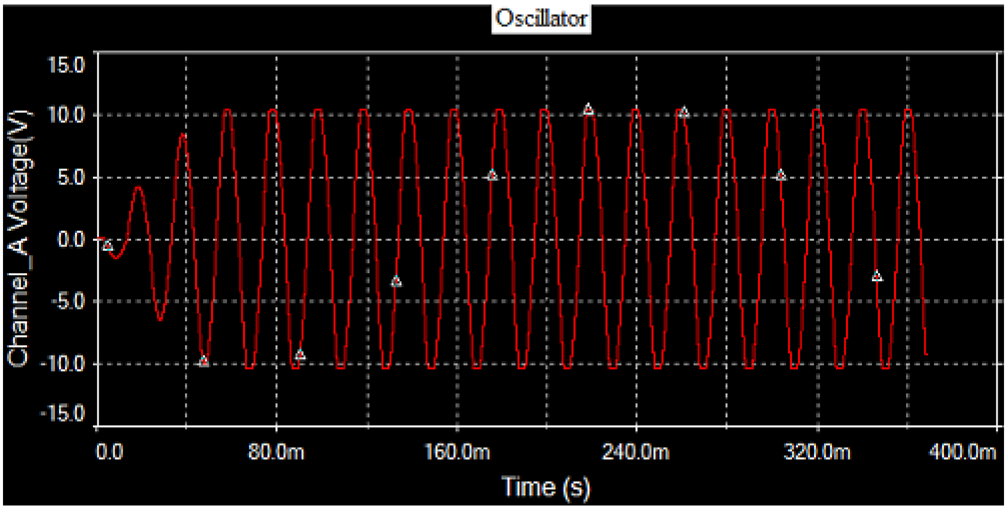


Figure 3.5 output of sinusoidal oscillator with 180 degree phase shift

3.2.2 INTEGRATOR

A circuit in which the output voltage waveform is the integral of the input voltage waveform is called integrator. Once a signal is arrived to the negative input terminal (Inverting input) of the opamp, the opamp tries to output the signal of the antiphase (180° shifted signal) as the output. Since it is 90° after in the voltage of the capacitor from the charging current, the output voltage of the opamp becomes the signal to interrupt 270 degrees (180° + 90°) from the input signal.

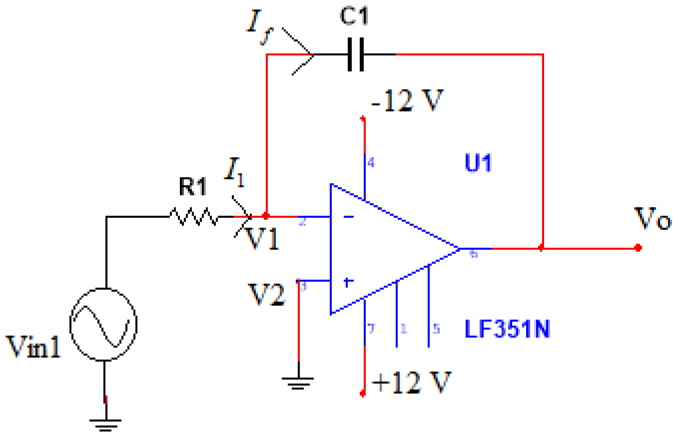


Figure 3.6 Circuit Diagram of Integrator

The feedback component is a capacitor. The current drained by opamp is zero and also the V_2 is almost grounded.

Therefore, $\therefore I_1 = I_f$ and $V_2 = V_1 = 0$ (3.2)

$$\frac{V_{in} - 0}{R} = C\frac{d(0 - V_o)}{dt}$$

Integrating equally side's w.r.t time from 0 to t, we get

$$\int_0^t \frac{V_{in}}{R} = \int_0^t C\frac{d(0-V_o)}{dt}dt \quad (3.3)$$

$$= C(-V_o) + V_o |_0^t$$

If $V_o |_{t=0} = 0V$, then

$$V_o = \frac{-1}{R}\int_0^t V_{in}dt \quad (3.4)$$

The output voltage is directly proportional to the negative integral of the input voltage and inversely proportional to the time constant RC.

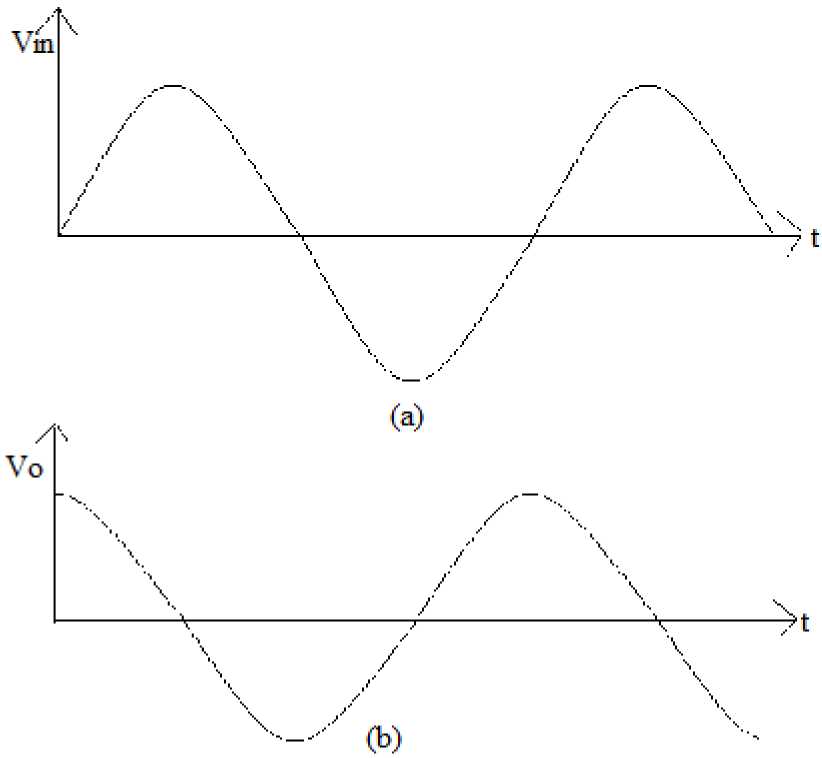


Figure 3.7 (a) Shows the input of the integrator and (b) shows the output of integrator

3.2.3 COMPARATOR

A voltage comparator is an electronic circuit that equals two input voltages and lets us distinguish which of the two is superior. It's informal to generate a voltage comparator from an opamp, since the polarity of the opamp output circuit depends on the polarisation of the difference between the two input voltages.

Input Voltage	**Output Voltage**
< than reference voltage	-ve
= to reference voltage	0
> than reference voltage	+ve

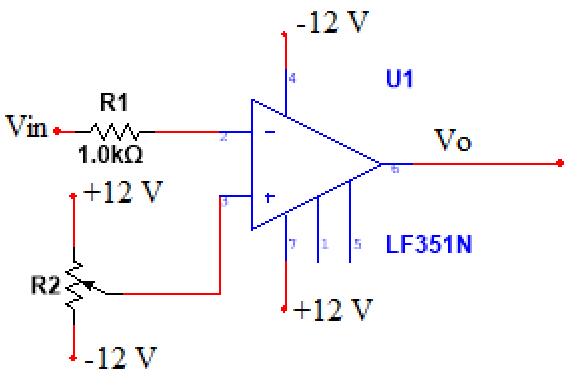


Figure 3.8 Circuit diagram of comparator

Points to be remebered while using comparators circuits

1. **Ensure differential input not exceed**: As there is no feedback the two inputs to the circuit will be at different voltages. Hence it is necessary to ensure that the maximum variance input is not exceeded.
2. **Input current change:** Again as a result of the lack of feedback the load will change. Predominantly as the circuit changes there will be a small increase in the input current. For most circuits this will not be a problem, but if the source impedance is large it may lead to a few unusual responses.
3. **Input signal noise**: The main difficulty with this circuit is that new the exchange point, uniform small amounts of noise will cause the output to alteration back and forth. Thus near the exchange point there may be numerous transitions at the output and this may give increase to problems somewhere else in the complete circuit.

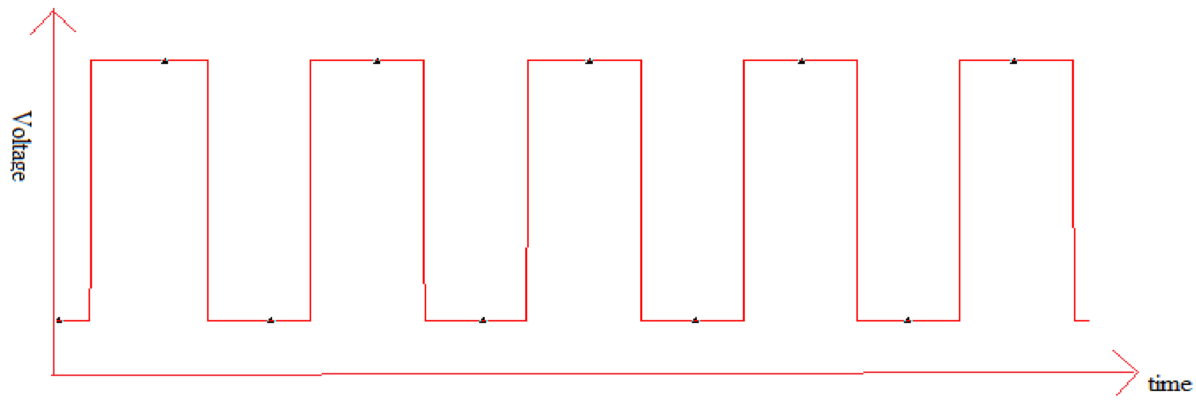


Figure 3.9 Output of Comparator

3.2.4 MONOSHOT BLOCK USING EXCLUSIVE OR-GATE

A Monoshot block is hypothetical to generate thin pulses when the input four-sided signal V_i alterations state from 0 to 1, a Monoshot block is shown with input signal V_i and with the desired output signal V_o .In Exclusive OR gate, the output is high or 1 when one of the inputs is high (1) or odd matching with the others and the output is low or 0 when both the inputs are same or even nature.

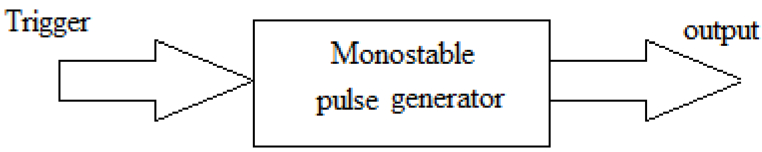


Figure 3.10 Block Diagram of Monoshot

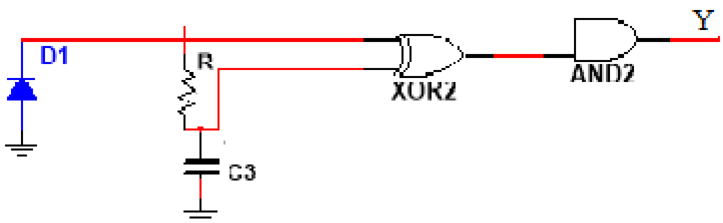


Figure 3.11 Circuit Diagram of Monoshot

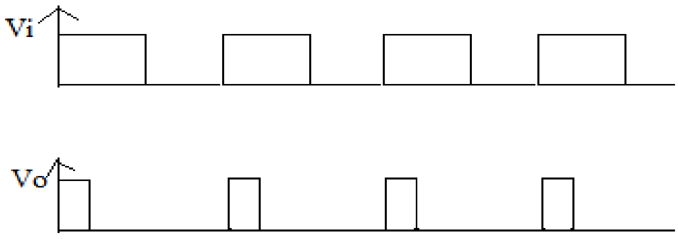


Figure 3.12 output of Monoshot by using Ex-OR gate

3.2.5 SR Flip-Flop to get 180° width pulse

The adjustable width pulse achieve from the comparator output is converted into a train of thin pulses separated by 360° at the output of the Monoshot. Therefore SR flip-flop are used to get 180° width pulse.

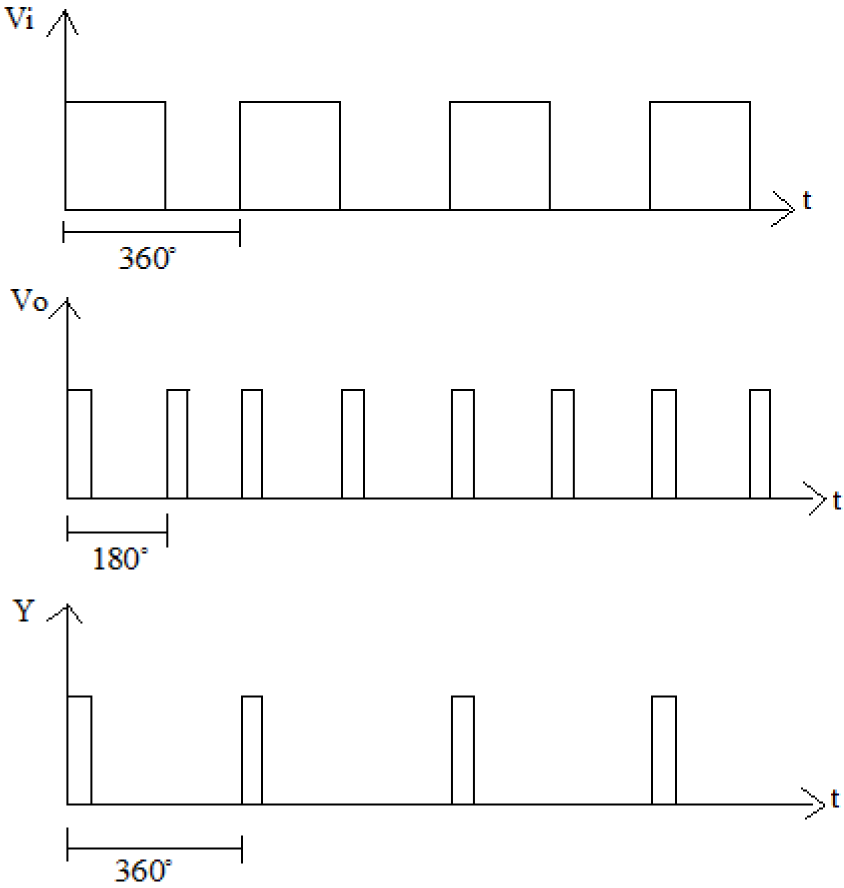


Figure 3.13 Output of SR Flip-Flop

3.2.6 ANDing the rectangular pulse with frequency using 555 timers

The four-sided voltage signals get from the flip flops 1 and 2 are balancing which means separated by 180° as desired. In our circumstance where the supply frequency is 50 Hz, the time period of the signals will be 20 ms and for 10 ms it will continue high and for rest of the 10 ms it will be low. Outputs of the flip flops cannot though, be connected directly between the gate and cathode of a SCR, and since the output from a TTL chip will not be able to supply the necessary current required by the gate circuit of a thyristor. Apart from this, we involve isolation between the governor circuit and power circuit. Thus with the support of a transistor and a pulse transformer these two purposes of strengthening the pulse and provided that the isolation are met.

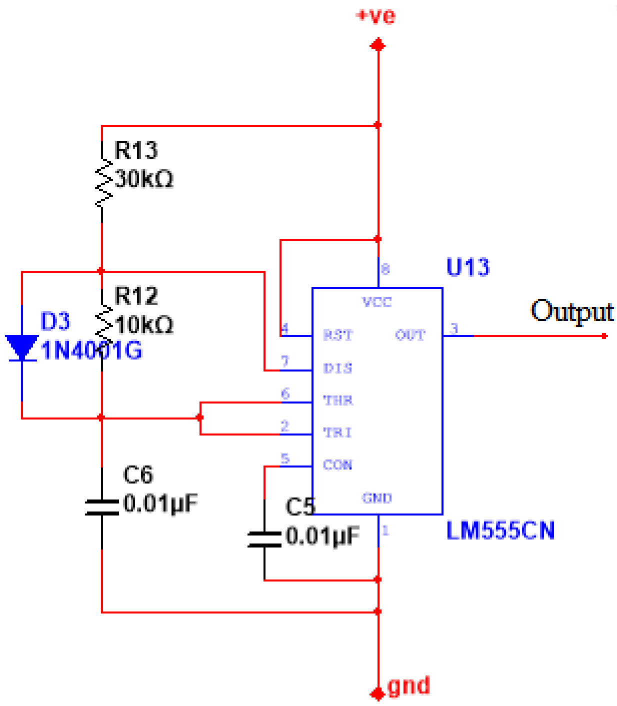


Figure 3.14 Circuit Diagrams of 555 Timers

3.2.7 GENERATOR CIRCUIT

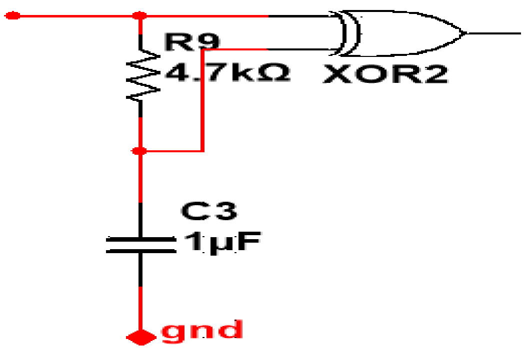


Figure 3.15 Circuit Diagrams of Generator Circuit

The circuit contains of 4.7k Ω resistor, and 1 μ F capacitor, and obsessed by a voltage source. The pulse generator circuit also involves of delay circuit or R-C integrator circuit that will yield output waveform based on time constant which are attained from resistance and capacitance value according to the equation below:

$$180^{\circ} \quad \tau = RC \tag{3.5}$$

The accomplishment of the circuit can also be designated in terms of a related quantity, the Turn over Frequency, f_o which has a value:

$$f_o = \frac{1}{2\pi\tau} = \frac{1}{2\pi RC} \tag{3.6}$$

And the period of the RC integrator's waveform can be restrained using:

$$T = \frac{1}{f_o} \tag{3.7}$$

In this model, the pulse generator circuit have two purposes. The first one is to produce square waveform that has low on period, T_{ON} that will be used to reset the waveform of comparator and to provide dead time for logic circuit in controller circuit.

4.2.8 LOGIC CIRCUIT

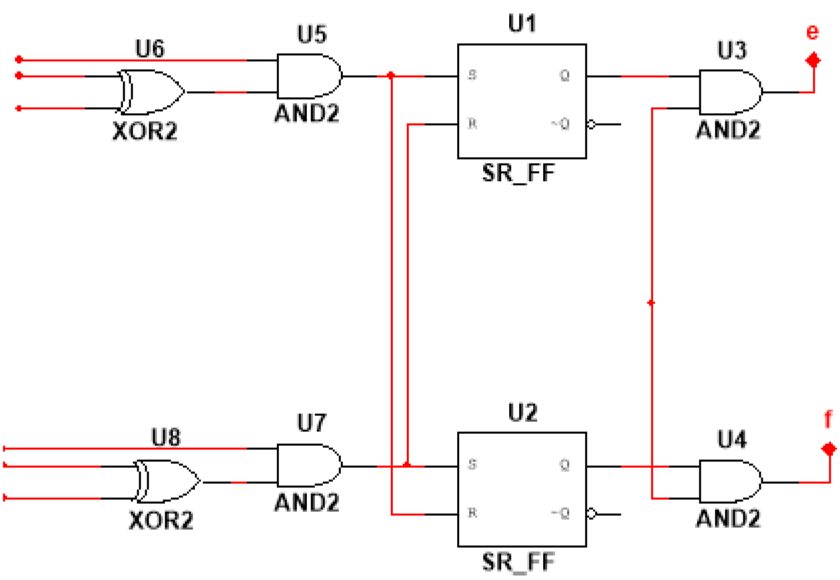


Figure3.16 Logic Circuit Diagram

The logic circuit contains of two 4070 ICs, four 4081 ICs and two 4043 ICs. That the adjustable breadth pulse gets from the comparator output is changed into a train of thin pulses alienated by 360° at the output of the Monoshot. ICs 4043 are balancing which means separated by 180° as desired. In this case where the supply frequency is 50 Hz, the time period of the signals will be 20 ms and for 10 ms it will continue high and for rest of the 10 ms it will be low

3.2.9 DRIVER CIRCUIT

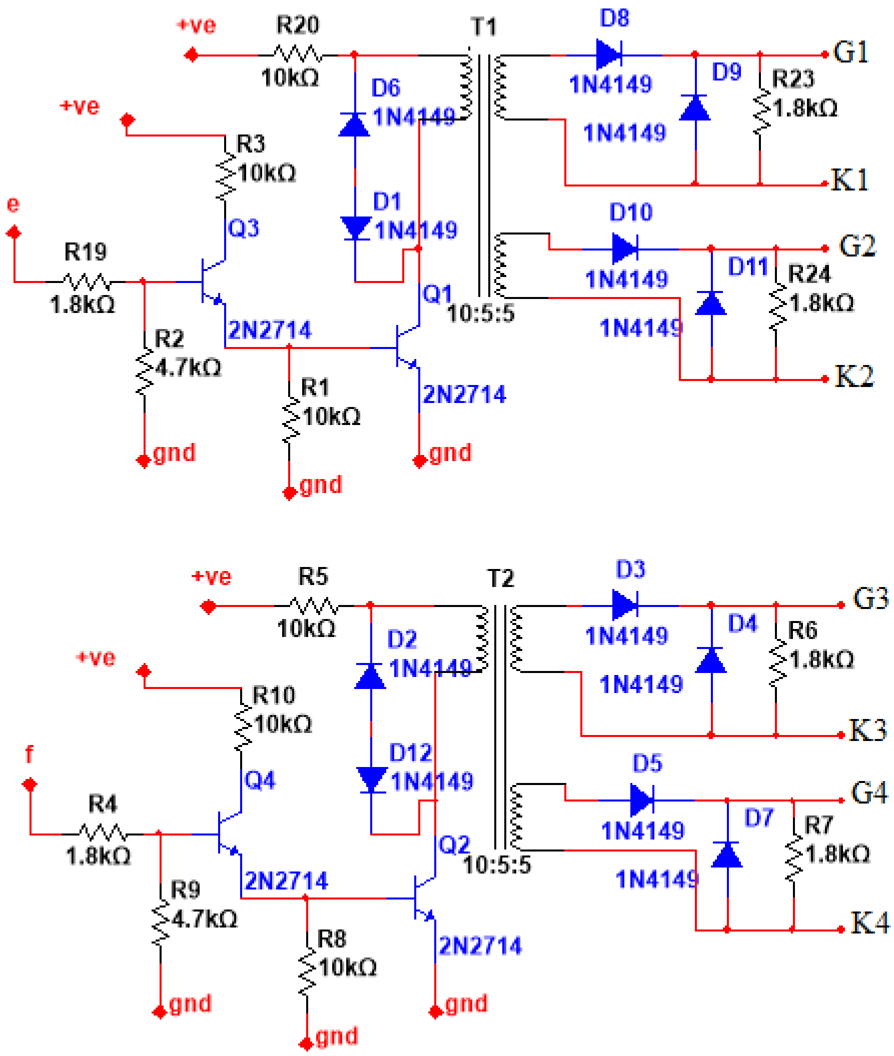


Figure 3.17 Driver Circuit for the converters

They are typically used to control current flowing through a circuit or is used to isolating the control circuit and the power circuit, seeing faults, loading and reporting failures to the control system, helping as a protections against failure, examining device signals, and producing assisting voltages. The terminals G1, G2, G3 and G4 are given to the gate of the thyristors of the converter.

3.2.10 Overall Cosine Firing Scheme

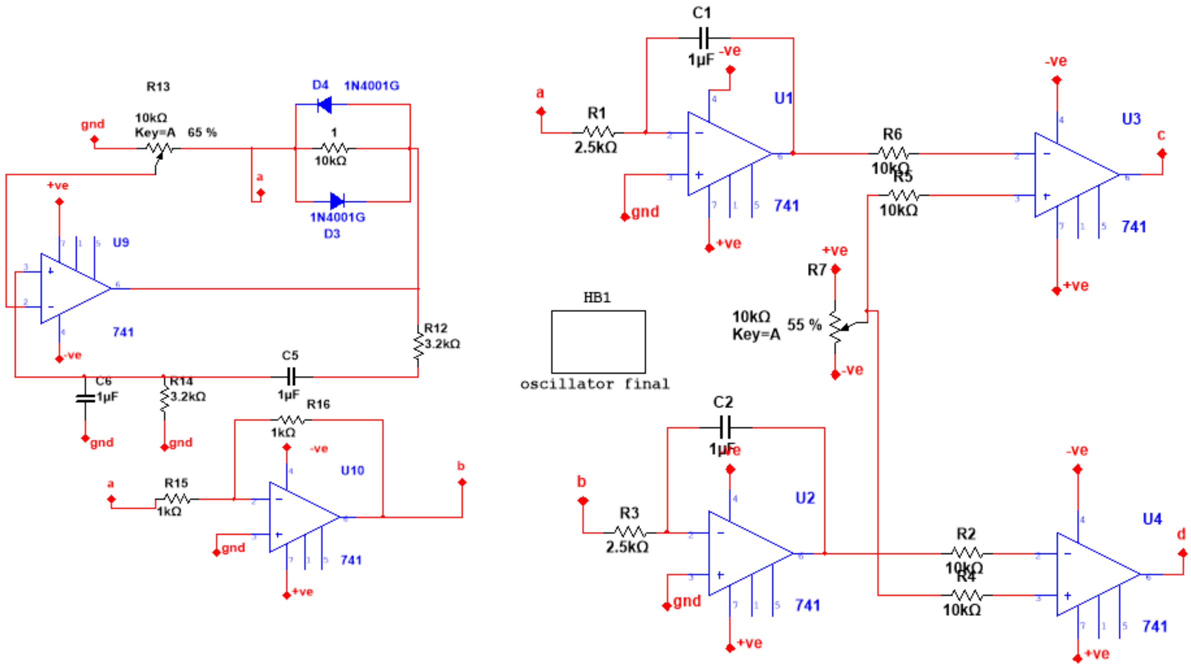


Figure3.18 Oscillator, Integrator and Comparator Circuit Simulated on Multisim Software

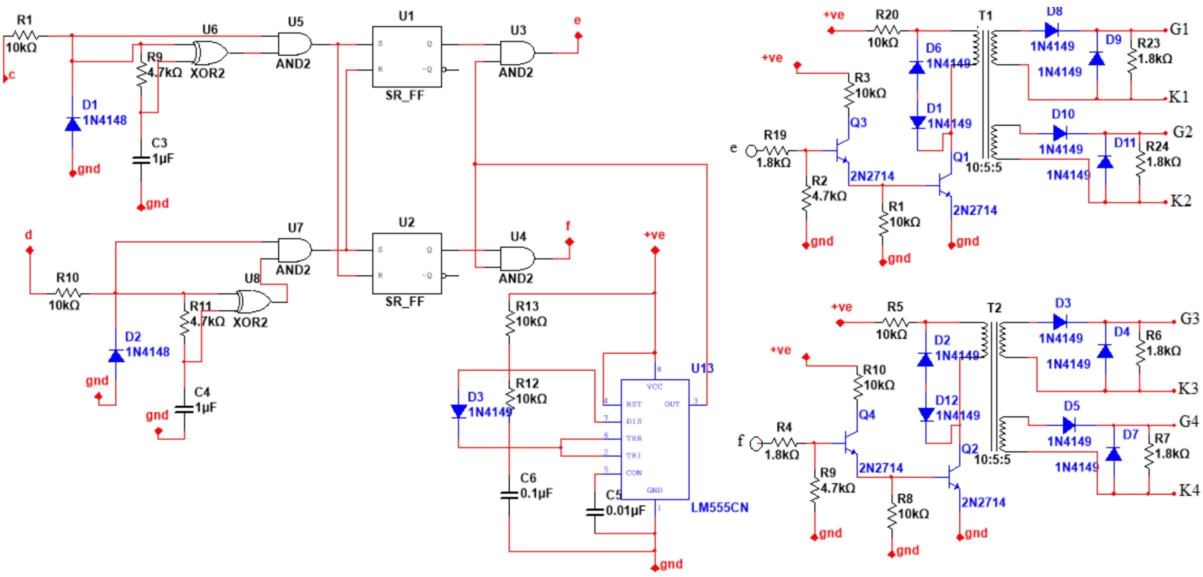


Figure 3.19 Monoshot, Logic Circuit, 555 timers and Driver Circuit

3.2.11 DESCRIPTION OF IC CIRCUIT USED

The following things are elaborated for the method using:

1. IC 4043 is used for realizing SR flip flop. In this chip 4 distinct SR flip flops are obtainable. This chip working with a d. c. supply of +3 V to + 15 V. In our case power supply used is + 12 V. The chip has 16 pins as shown in Fig 3.19.

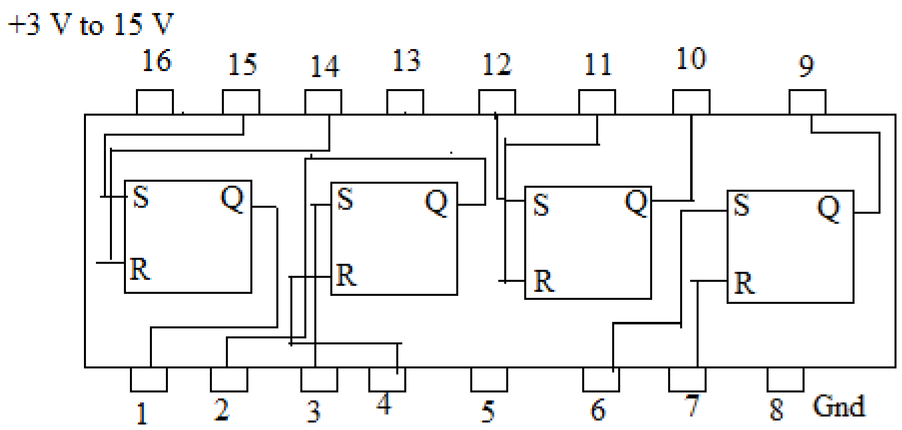


Figure 3.20 Pin diagram of IC 4043

2. IC 4081 is used for realizing AND logic gate. In this chip 4 separate AND logic gates are available. This chip works with a D.C. supply range of + 3 V to +15 V. In our case power supply used is + 12 V.

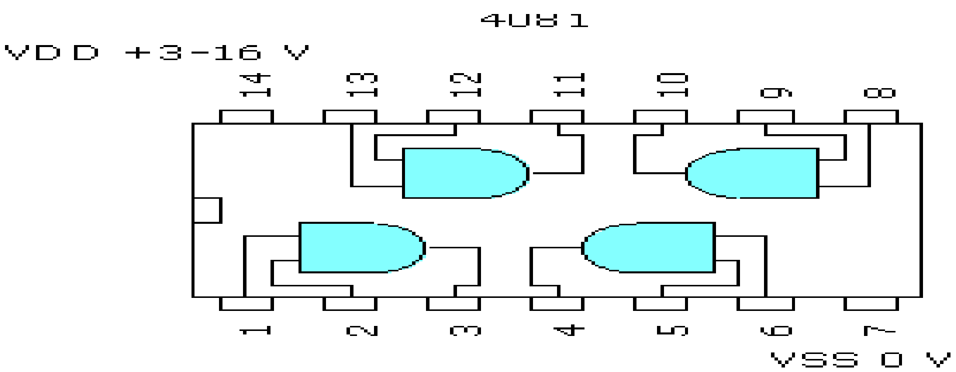


Figure 3.21 Pin Diagrams of IC 4081

3. IC 4070 is used for realizing Ex-OR gates. In this 4 separate Ex-OR gates are available. This chip works with a D.C. supply range of + 3V to + 15 V. In our case power supply used is +12 V. The chip has 14 pins as shown in Fig 3.21.

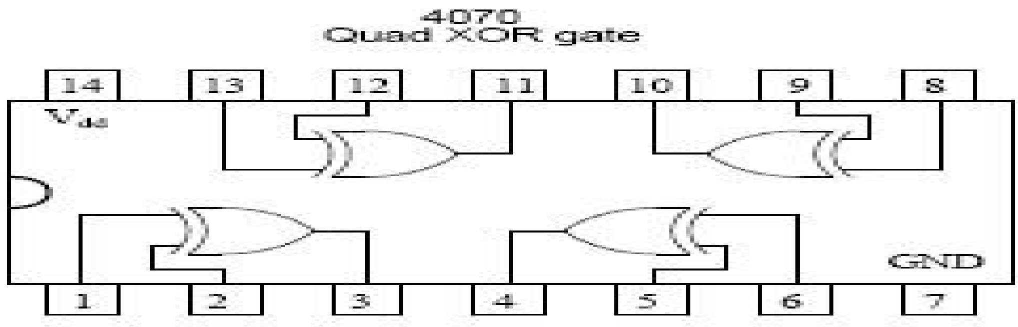


Figure 3.22 Pin Diagrams of IC 4070

B. Components used the followings components are used for the circuit: .

1. Two IC 741 opamp for two integrators

2. Two IC 741 opamp for Oscillator

3. Two IC 741 OP AMP for two comparators.

4. One IC 4070 which families of four EX-OR gates.

5. One IC 4081 which families four AND gates.

6. One IC 4043 which families 4 SR flip flops gates.

7. One 555 timer for producing high frequency pulses.

8. Number of resistors and capacitors of various values as detailed shown in the circuit.

9. Few diodes for making the ± 12 V power supply and also to clip the negative half of rectangular pulse obtained at the output of the comparator.

10. One 10 KΩ potentiometer for having variable D.C. voltage Vr.

CHAPTER 4

RESULTS AND DISCUSSIONS

4.1 INTRODUCTION

This chapter, it will discourse about the outcomes and discussion for the project. Two results we get in our thesis, one of them is comes from simulation process using Multisim software and another one by accompanying experiment in the Electronics Lab. For the first part, the circuit is modelled in the Multisim and simulation result is obtained. Next, the circuit was tested on Bread board as hardware. The hardware had been experimented to verify waveform of the control circuits based on theoretical and hardware implementation. Then, output waveform got from the testing is compared to the theoretical waveform.

4.2 SIMULATION CIRCUIT

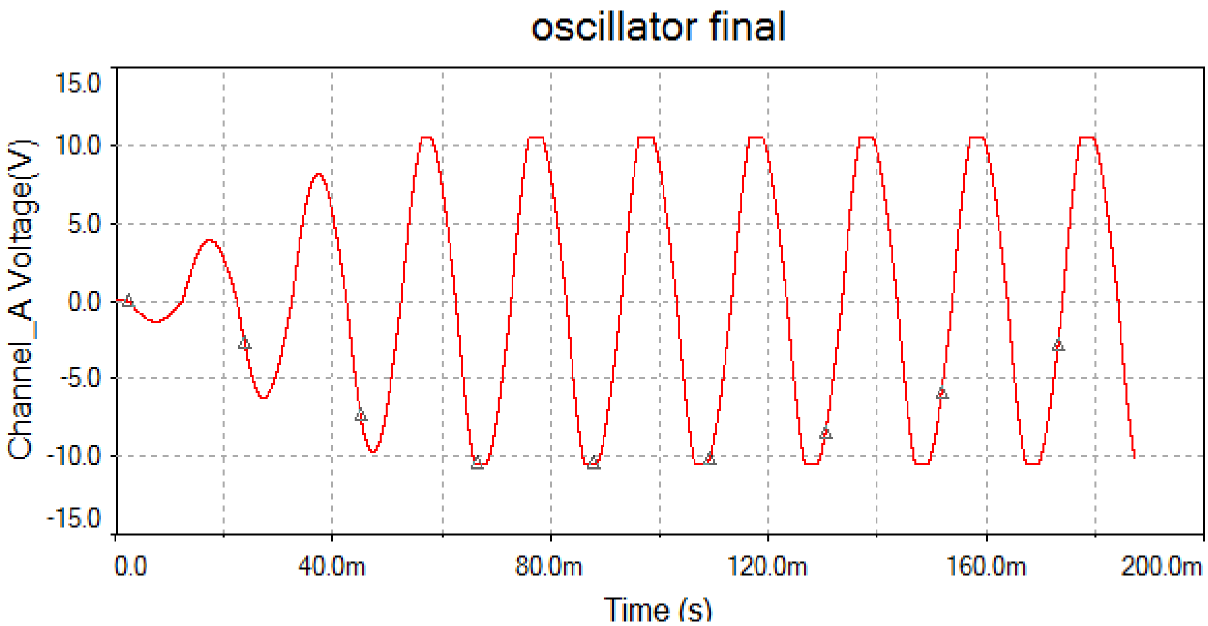


Figure 4.1 waveform of Sinusoidal Oscillator with 0 degree phase shift

Here potentiometer is used to control the magnitude of the generated waveform and by varying it we can change also generate a square wave by making the sine wave hit the power rails so that its upper and lower part cut off to give a square wave.

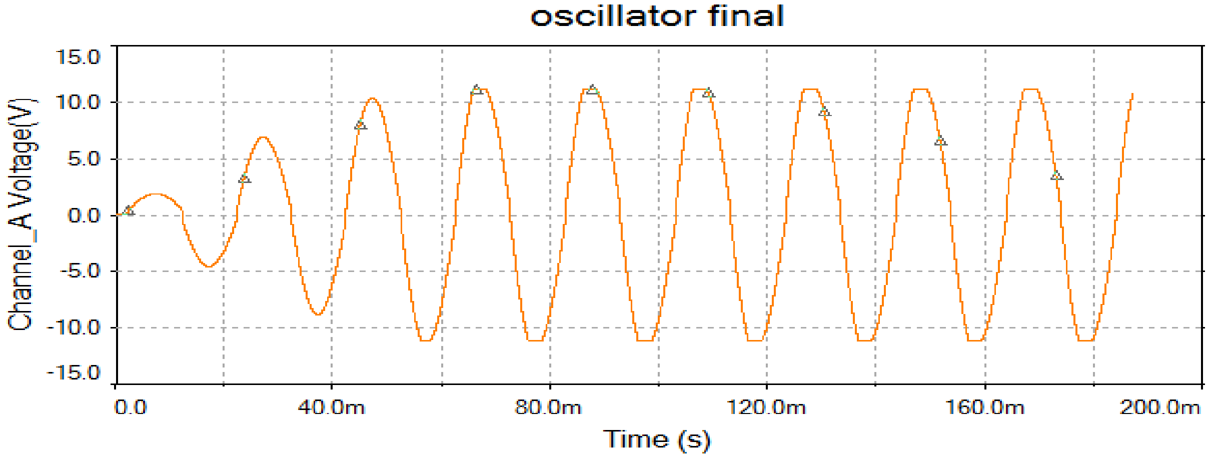


Figure 4.2 Output of Oscillator with 180° phase shift, V_b

BY the use of Opamp 741, resistor and the output of sinusoidal Oscillator we get the waveform of 180 degree with the same magnitude.

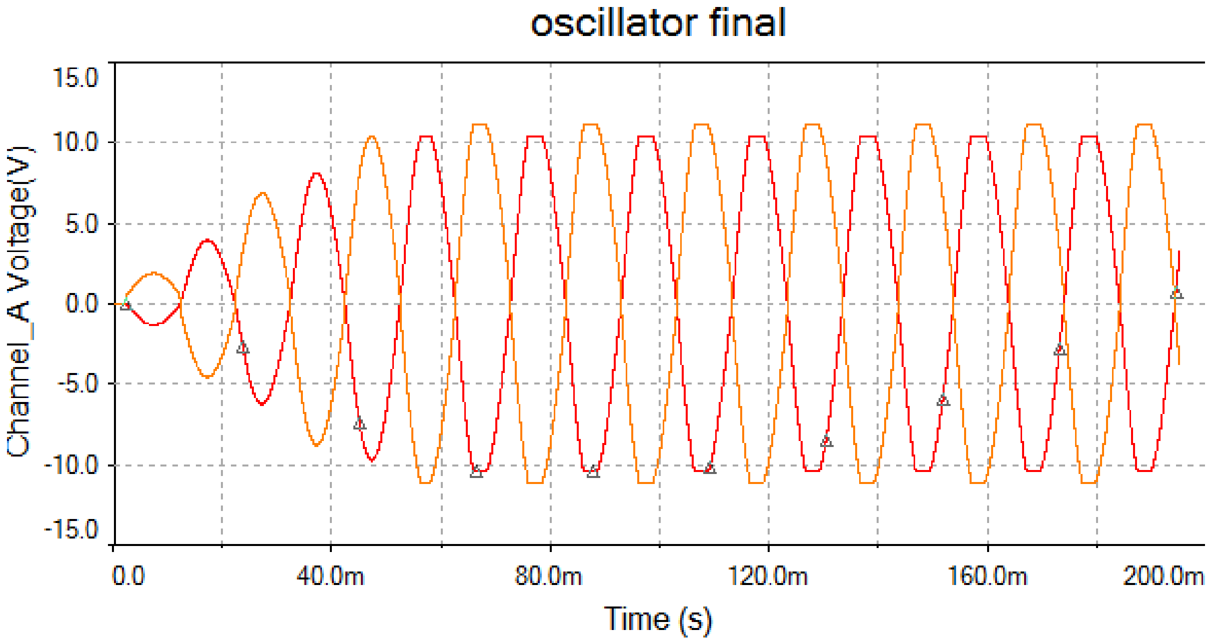


Figure 4.3 Combined Output of Sinusoidal Oscillator with 0 degree and 180° phase shift

Here we can see that the combined waveform of oscillator and the phase shift of 180 degree waveform with same magnitude and frequency.

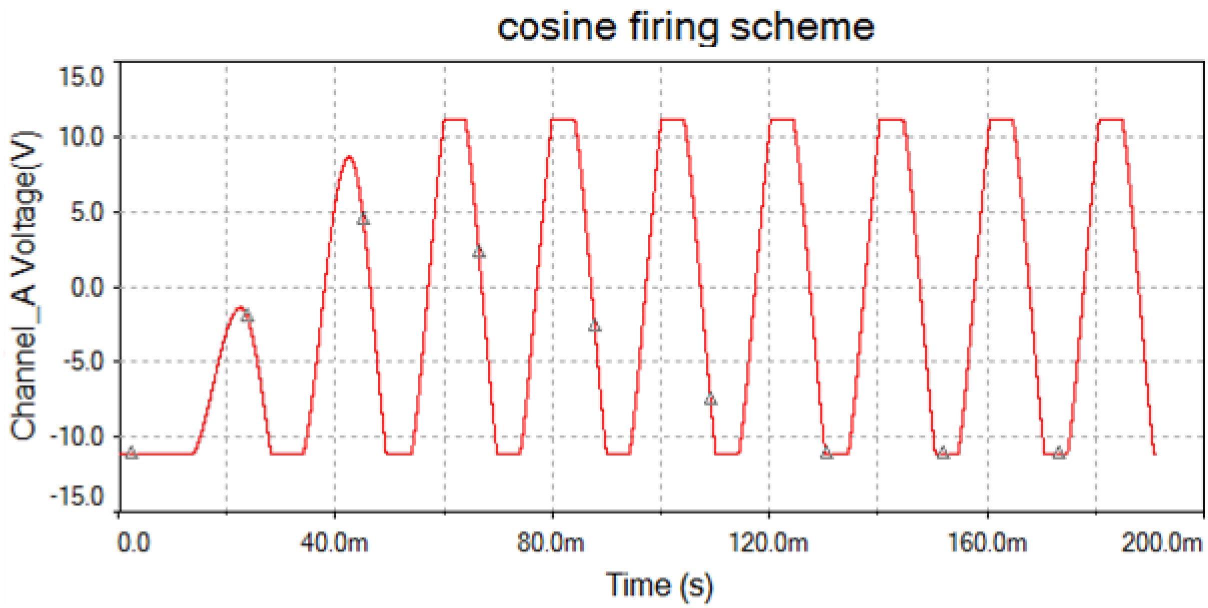


Figure 4.4 Output of first Integrator with 90 degree of phase shift

The Output waveform of oscillator is integrated into the cosine waveform by shifting the output waveform of oscillator to 90 degree.

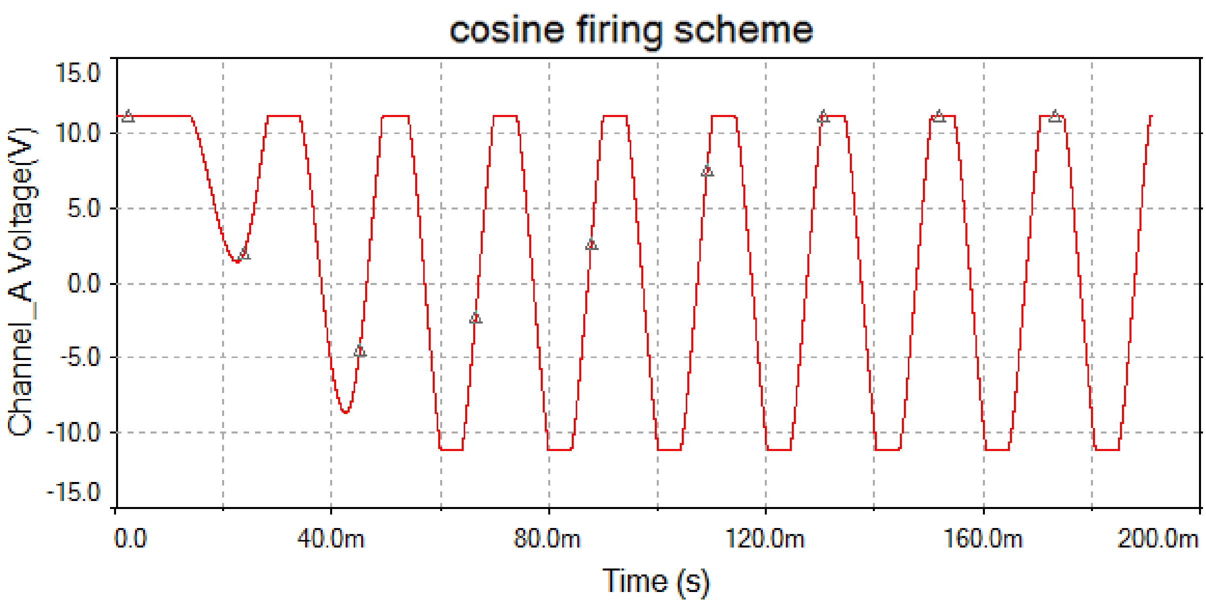


Figure 4.5 Output of second Integrator with 90 degree of phase shift

The output waveform of the V_b which is converted into the cosine waveform by integrator.

Figure 4.6 Output of first Comparator

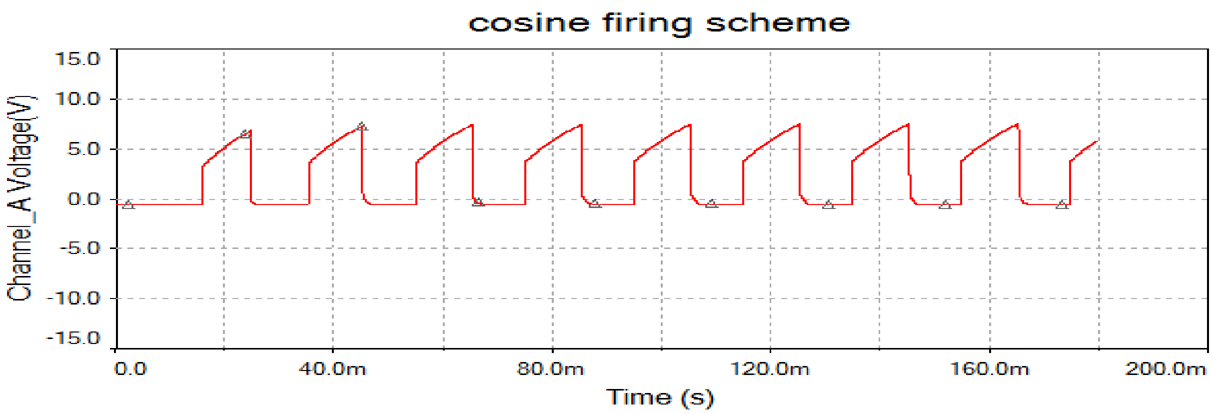


Figure 4.7 Output of second Comparator

The cosine wave so obtained is compared with a reference d.c. voltage (Vref). Therefore square pulses will be generated at the output terminal of the comparator. The signal at Comparator is synchronized with the pulse and is delayed from the supply zero crossing by an angle α . The value of   can be varied a range of $0^{\circ} \leq \alpha \leq 180^{\circ}$.

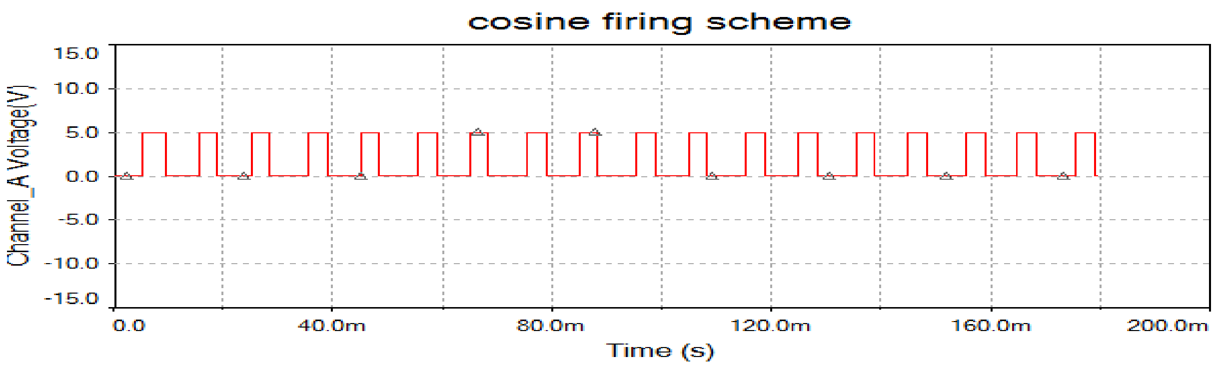


Figure 4.8 Output of first Ex-OR gate

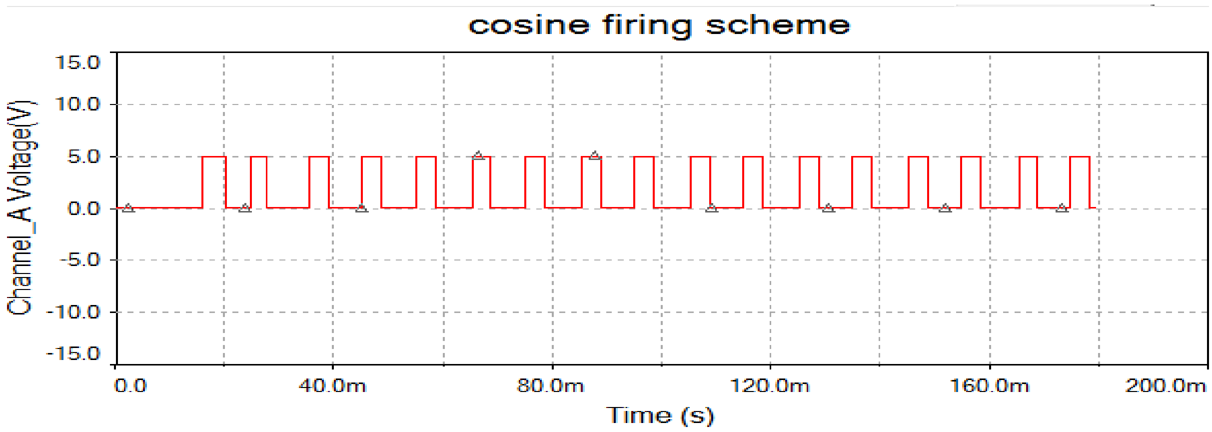


Figure 4.9 Output of Second Ex-OR gate

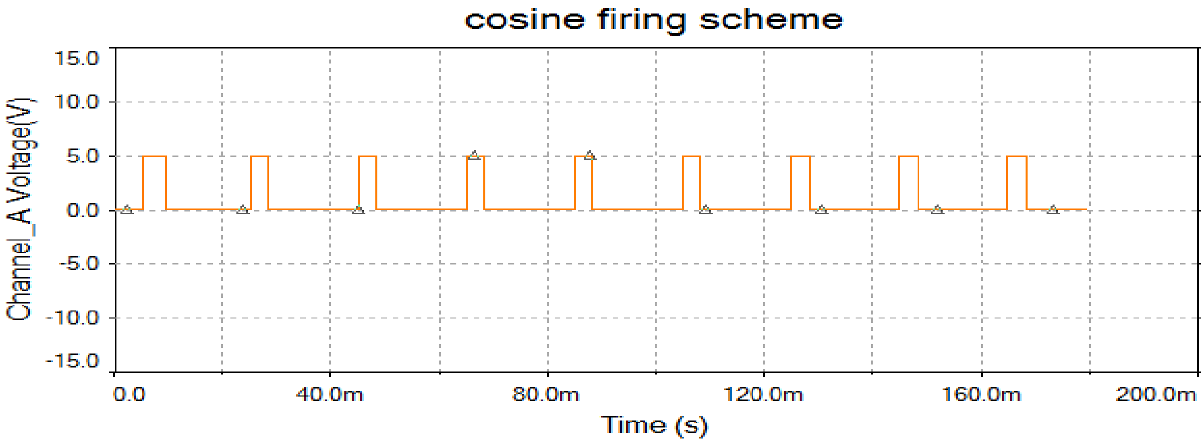


Figure 4.10 Output of first AND gate

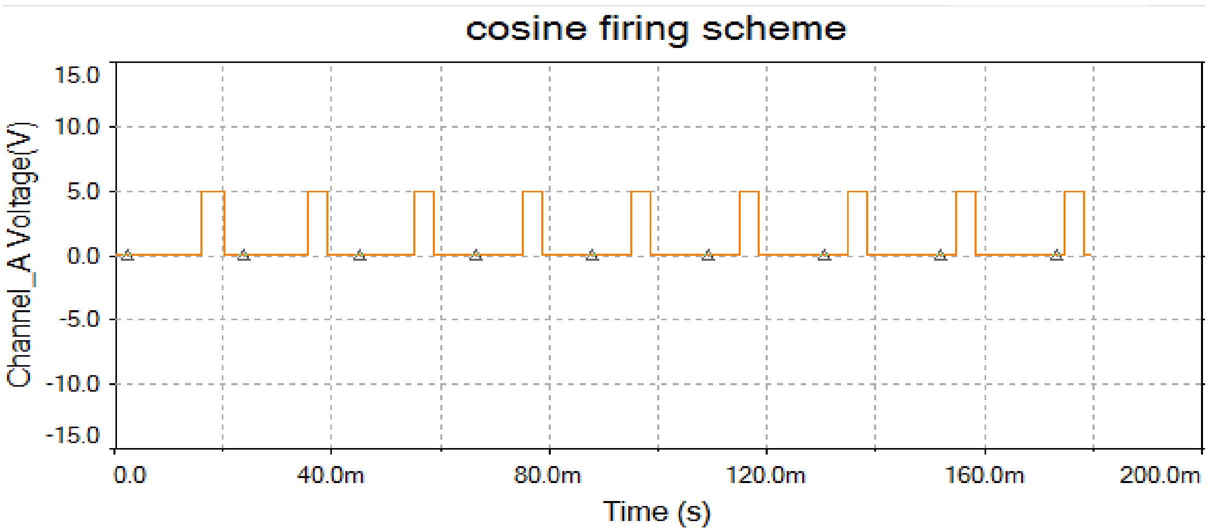


Figure 4.11 Output of second AND gate

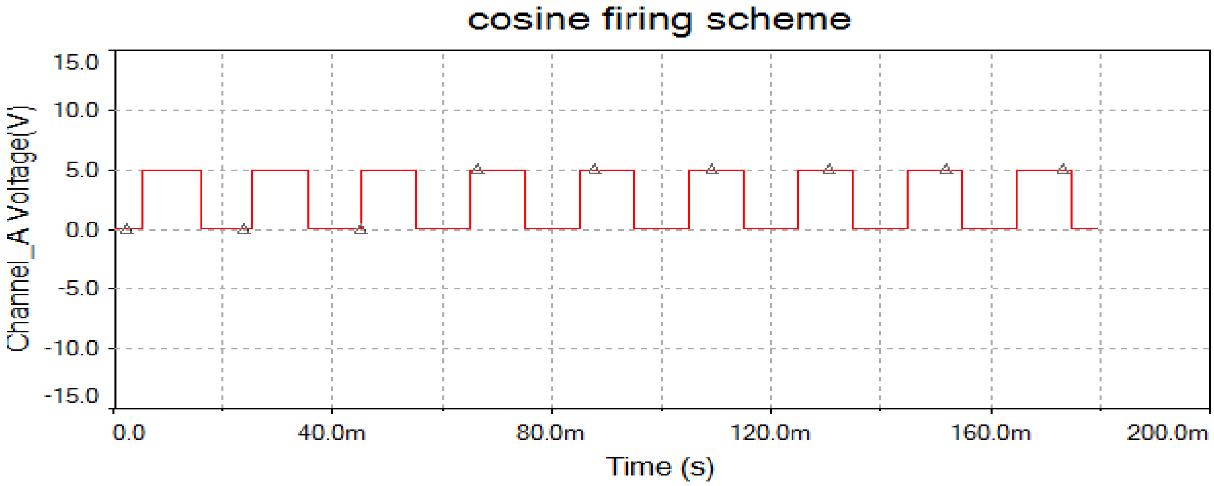


Figure 4.12 Output of first SR Flip-Flop

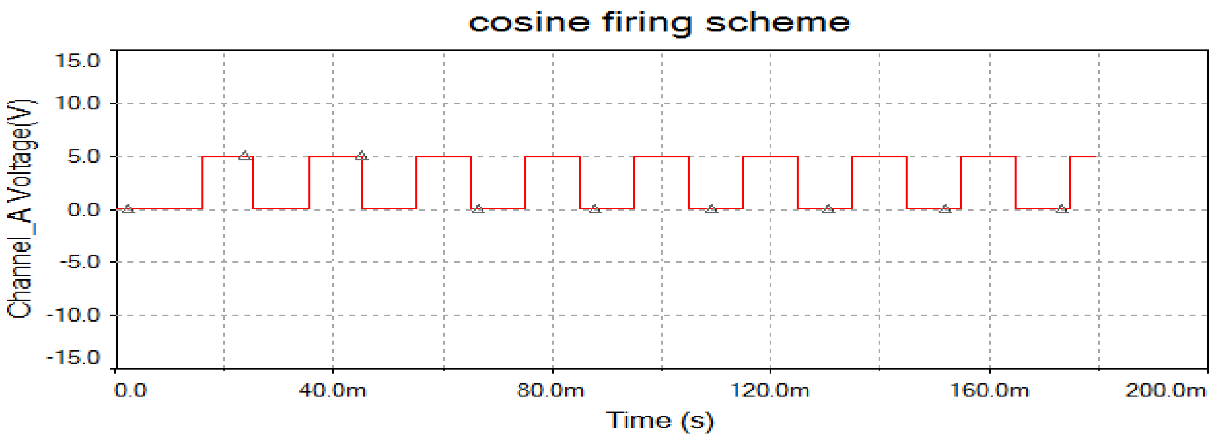


Figure 4.13 Output second SR Flip-FloP

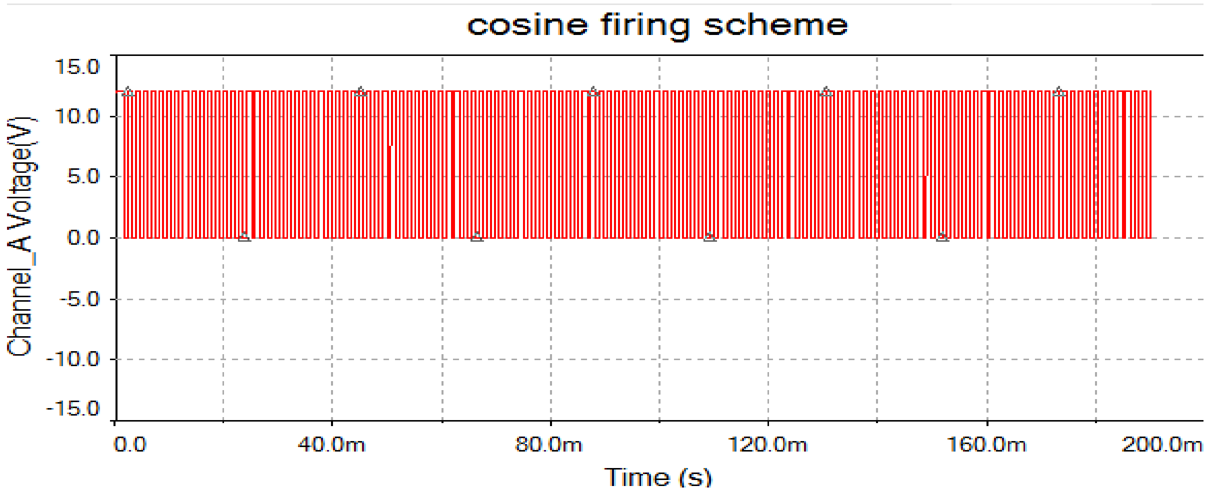


Figure 4.14 Outputs of 555 Timers

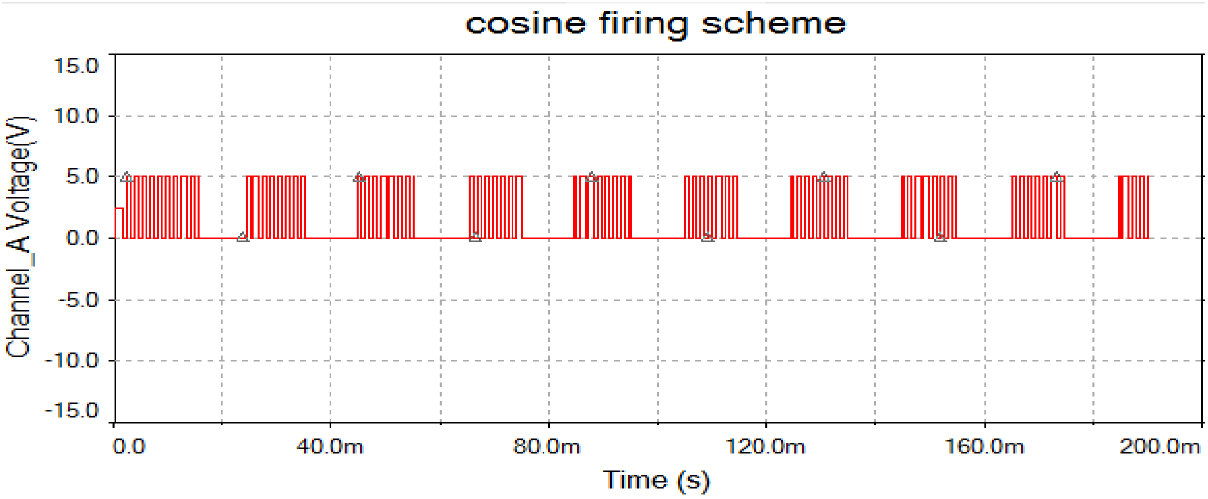


Figure 4.15 Final gate Pulses for Thyristor T1 and T2

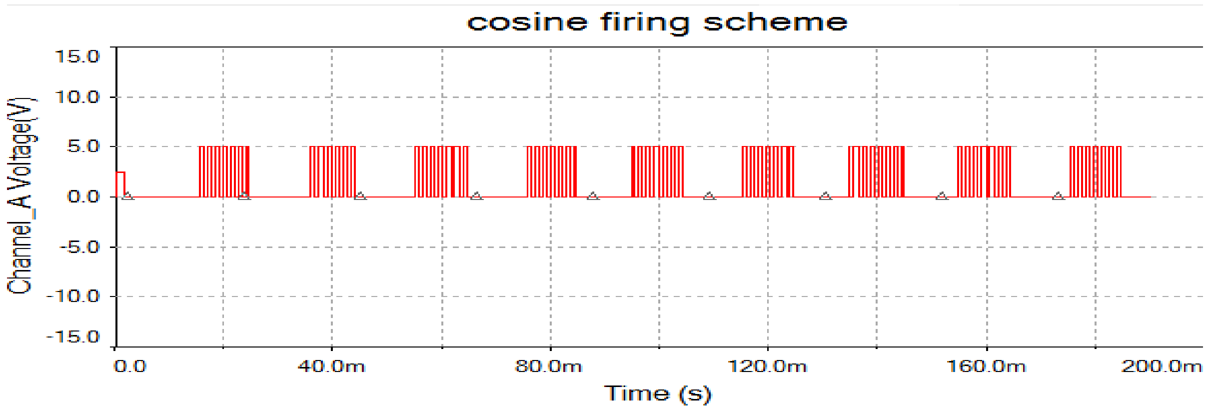


Figure 4.16 Final gate Pulses for Thyristor T3 and T4

4.3 Experimental Circuit of Cosine Firing Scheme by using Sinusoidal Oscillator

The control firing Circuit Implemented on Hardware is shown in figure 4.16 and the experimental result obtained on CRO at different stages will be given below:

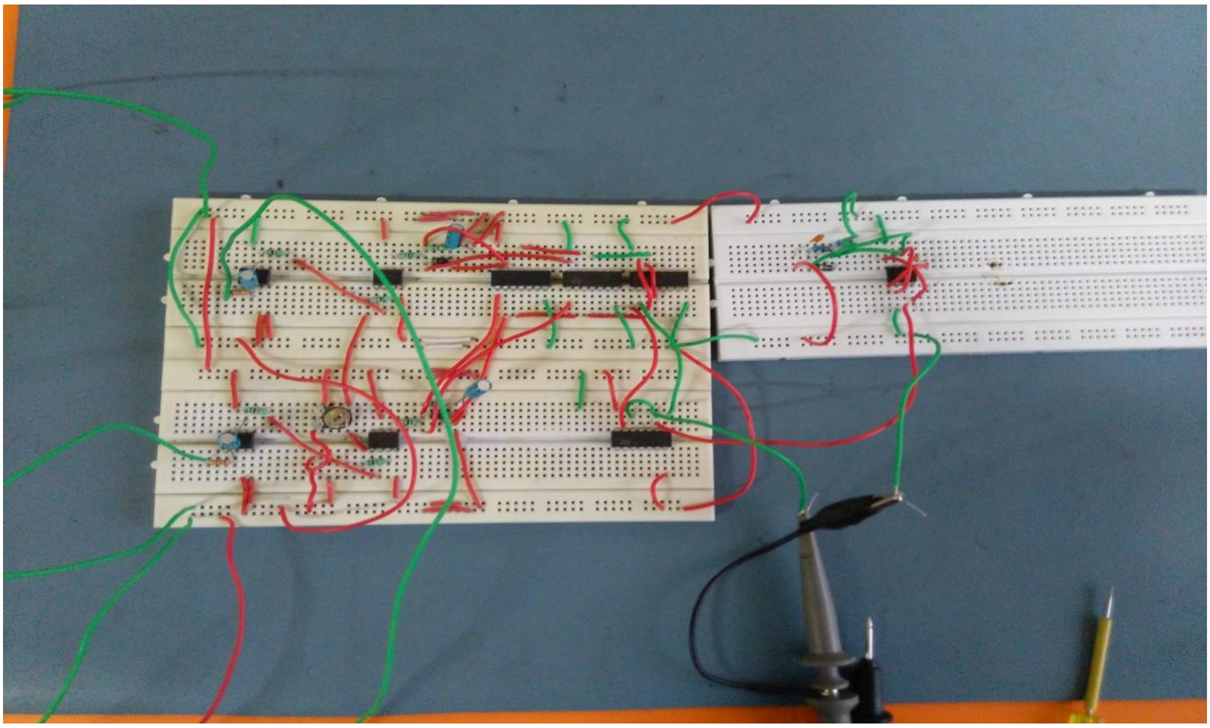


Figure 4.17 the complete control firing circuit implemented on hardware

4.4 HARDWARE RESULTS

Design of cosine control firing circuit using sinusoidal oscillator is implemented on hardware. The experimental results at different stages of the circuit are shown in the figure below:

1 Results of Sinusoidal Oscillator with 0 degree phase shift

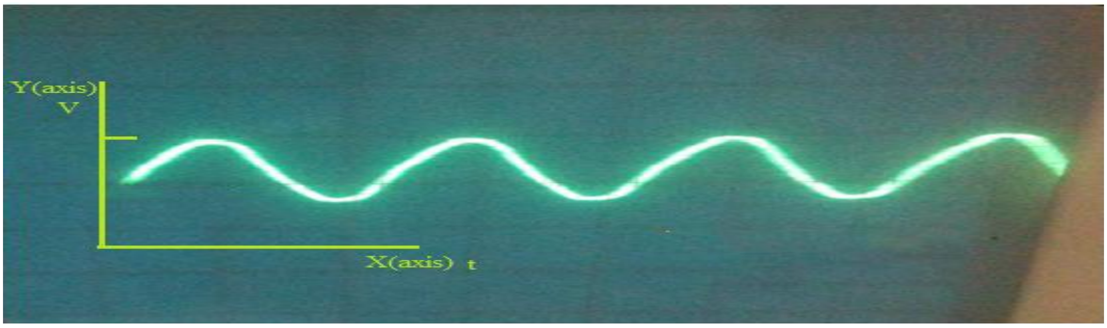


Figure 4.18 Output of sinusoidal Oscillator with 0 degree phase shift

2 Results of Sinusoidal Oscillator with 180 degree phase shift

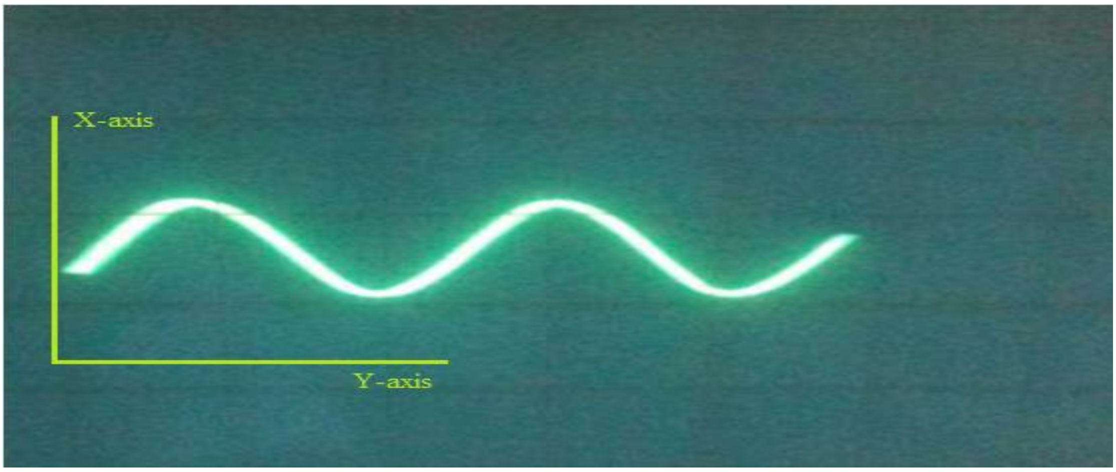


Figure 4.19 Results of Sinusoidal Oscillator with 180 degree phase shift

3. Results of first integrator

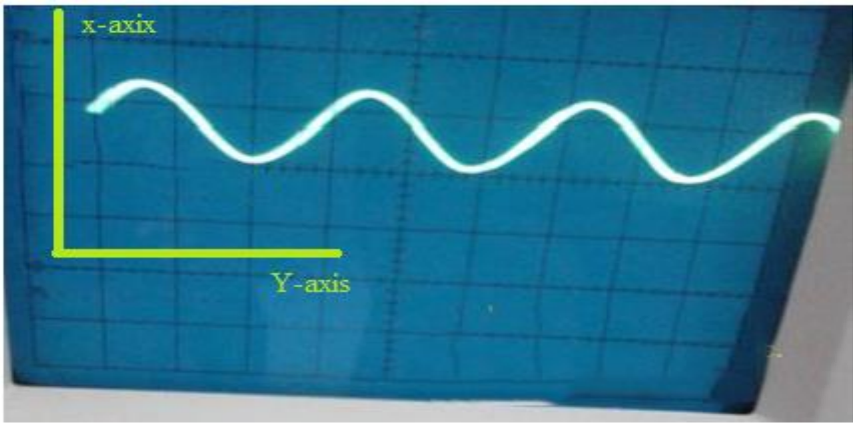


Figure 4.20 Output of first integrator

4. Results of second integrator

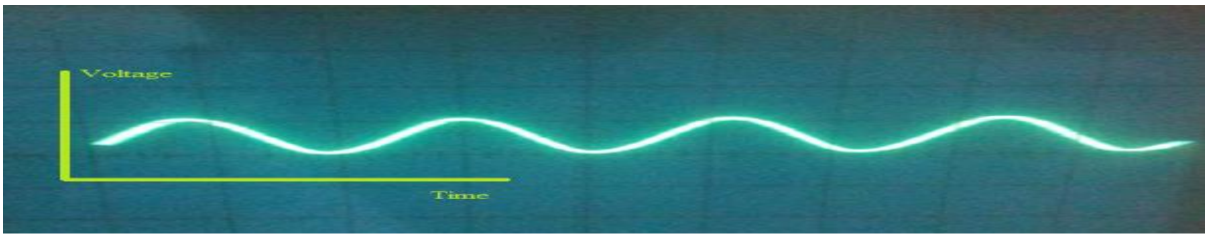


Figure 4.21 Output of second Integrator

4. Results of first Comparator

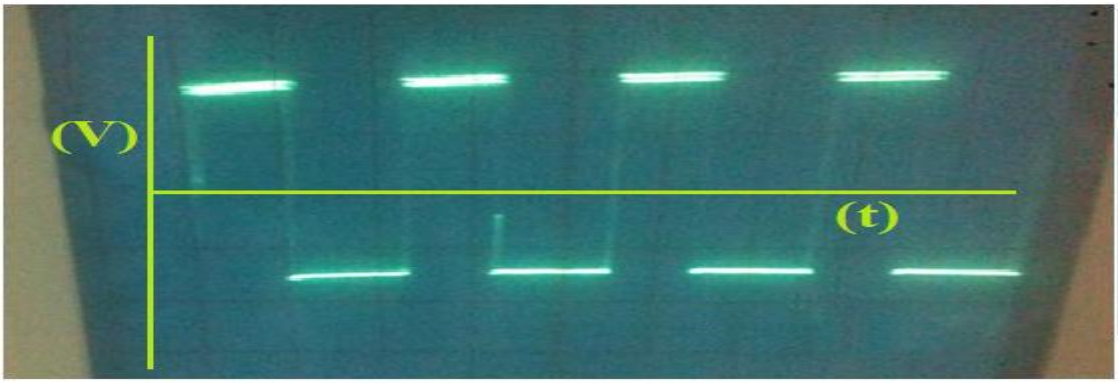


Figure 4.22 Output of first Comparator

4. Results of second Comparator

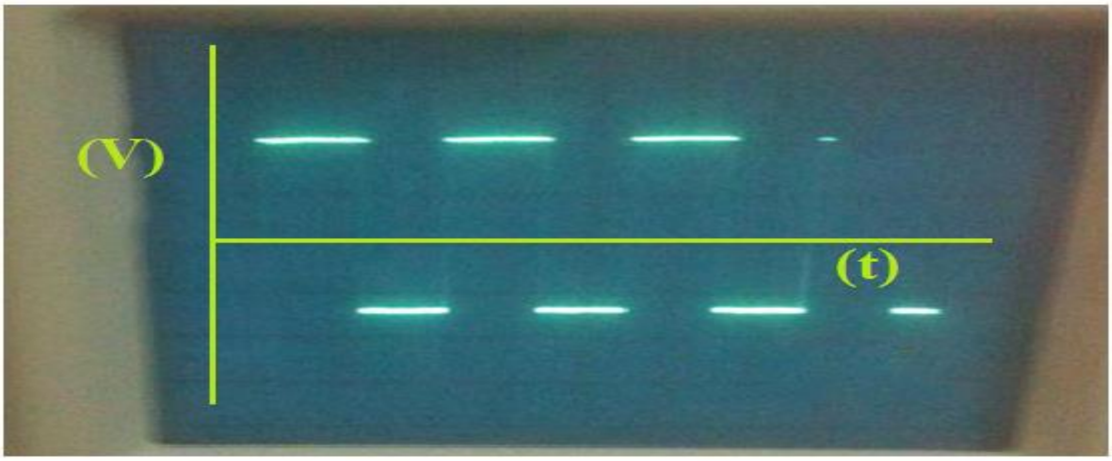


Figure 4.23 Output of second Comparator

5. Results of first Ex-OR gate

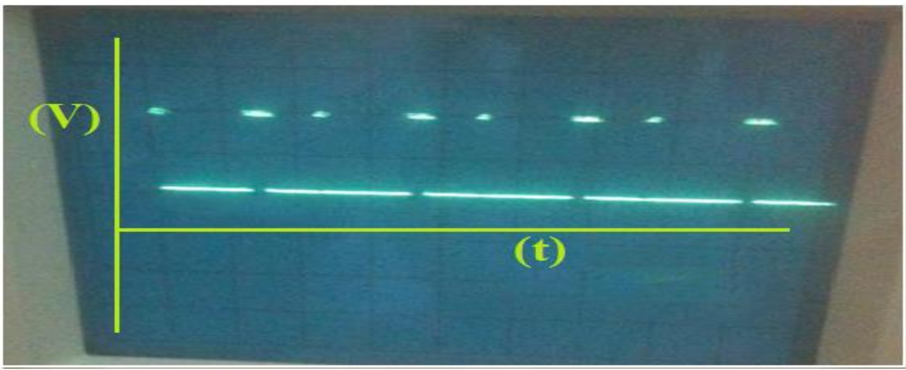


Figure 4.24 Output of first EX-OR gate

6. Results of Second Ex-OR gate

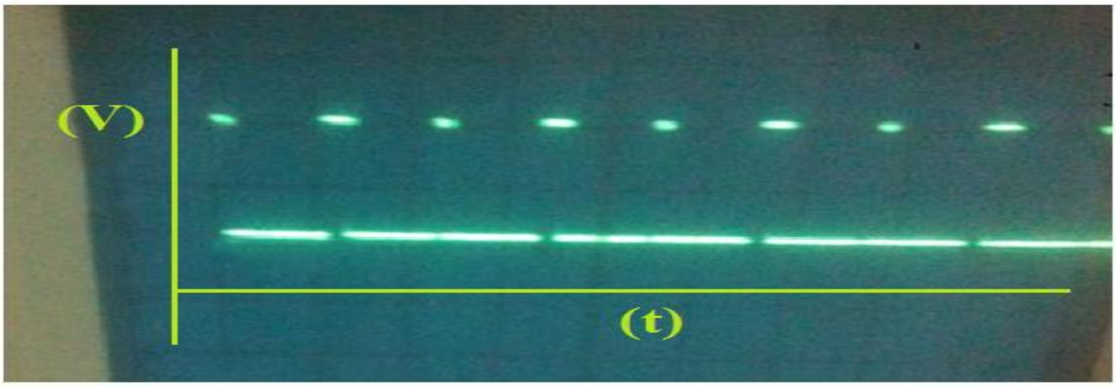


Figure 4.25 Output of Second Ex-OR gate

7. Results of First AND gate of Monoshot Block-1

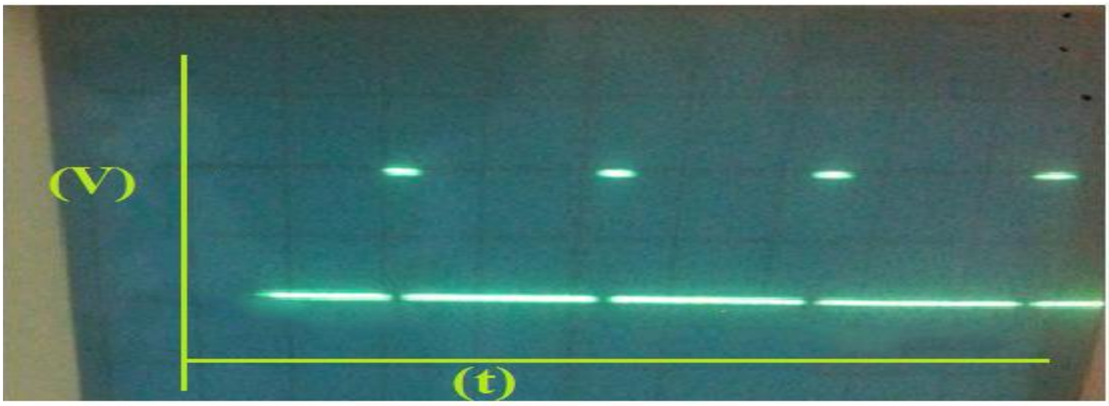


Figure 4.26 Output of First And gate of Monoshot block-1

8. Results of Second AND gate of Monoshot Block-2

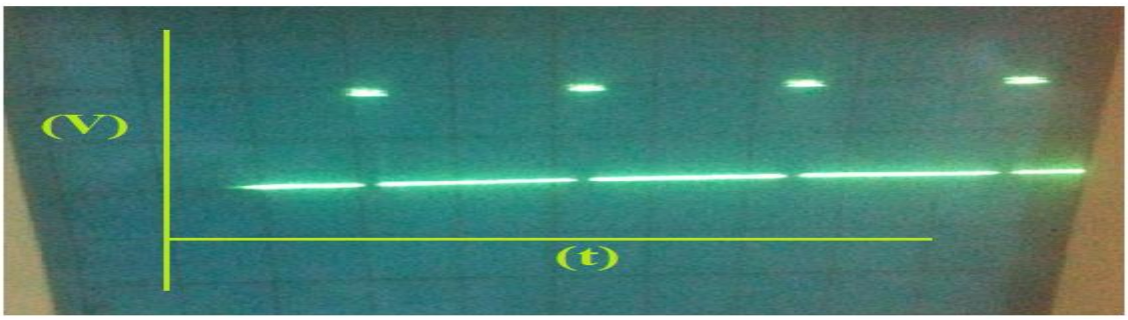


Figure 4.27 Output of Second AND gate of Monoshot block-2

8. Results of SR Flip-Flop

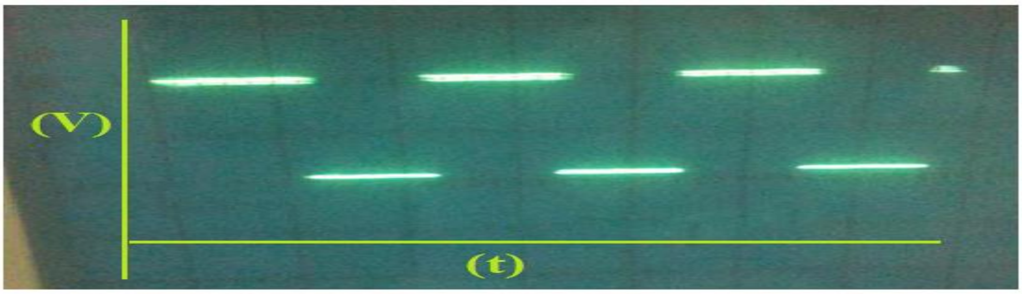


Figure 4.28 Output of first SR Flip-Flop

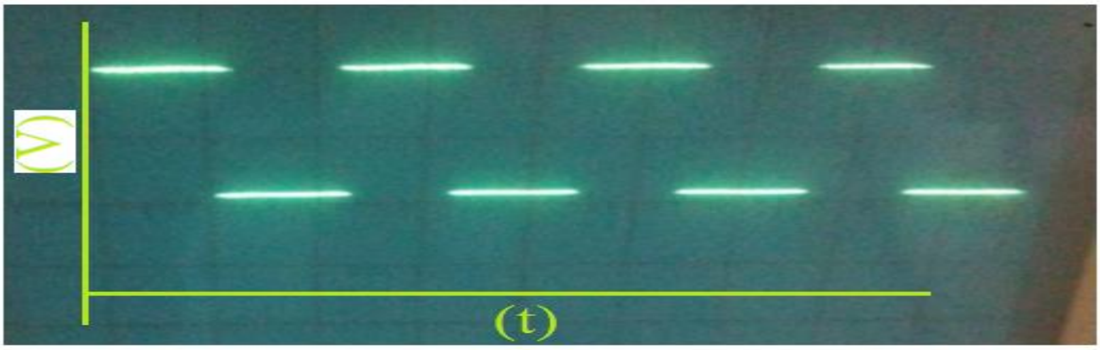


Figure 4.29 Output of Second SR Flip-Flop

9. Results of 555 Timers

Figure 4.30 outputs of 555 timers

10. Results of final pulses at Second AND gate

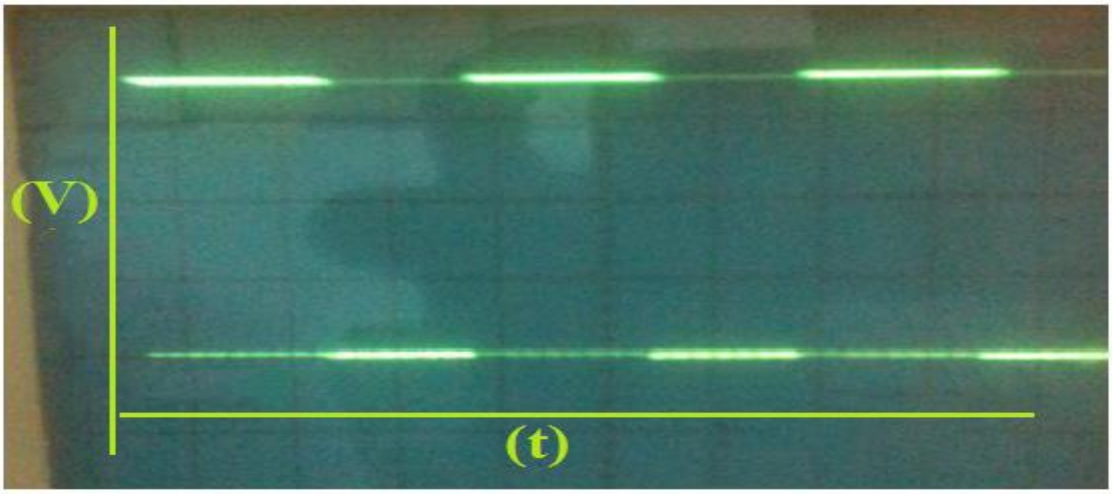


Figure 4.31 Outputs of Second AND Gate for Triggering Thyristor T1 and T2

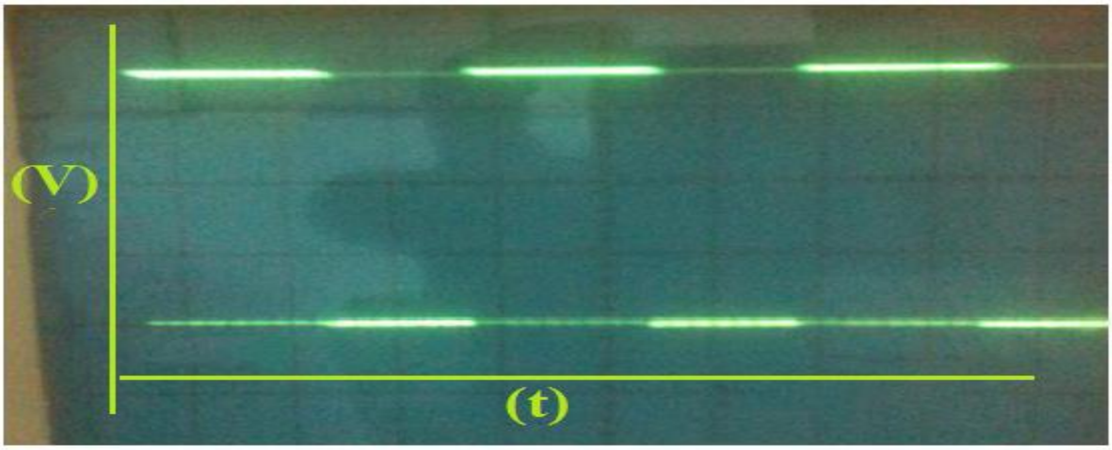


Figure 4.32 Outputs of Second AND Gate for Triggering Thyristor T2 and T3

CHAPTER 5

CONCLUSION AND FUTURE SCOPE

5.1 CONCLUSION

In this modern world which science and technology becomes an essential part in industrial application, the rapid developments in power electronics technology especially in rectification area to provide a wide range scope of application of controllable DC voltage for industrial usage such as DC motor drives and for electronic devices that virtually requires a DC voltage to perform tasks. Thus, the controlled rectifier is quite useful and applicable of various types of load.

The main objective of this project is to design hardware for control circuit to be used in single phase full wave rectifier circuit. The designated hardware used analog approach which the phase of the full wave rectifier are controlled by varying the firing circuit angle of the control circuit. Each of the firing circuit angles determines the level of DC output voltage when AC voltages are applied across a load in bridge rectifier.

In conclusion, the control circuit with a full controlled bridge rectifier is design successfully. Although the objective of the project is successfully carried out, the output waveform of designated rectifier is slightly unsmooth. The recommendation to improve the pulsating DC output is stated in the recommendation part.

5.2 FUTURE SCOPE

The designated hardware produced some problem related to unsmooth DC output waveform. For future works, there are some recommendations have been listed based on the problems below.

1. In order to produce steady DC from a rectified AC supply, a smoothing circuit as a filter is required at the output to smooth the ripple present on the pulsating DC voltage to come close to a constant DC voltage value required. This can be achieved by installing capacitor across the load of the rectifier.

2. The AC supply voltage of rectifier circuit in terms of RMS value used in the project is too low. A variac or isolation transformer which can be used to regulate AC supply voltage can be used to produce high level DC output voltage.

3. Install over current protection circuit into the PCB for protecting the thyristor in full bridge rectifier circuit.

4. The driver circuits for power device used transistor and pulse transformer (1:1+1) ratios. But in software development, there are no simulation modelling for pulse transformer. Thus, the pulse transformer driver circuit can be replaced by the use of Mosfet or Optocoupler as driver circuit.

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