Design of Low Noise Amplifier for WCDMA Reception Range

(2.11 GHz−2.17 GHz)

A thesis submitted in the partial fulfillment of requirement

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In

VLSI Design

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DECLARATION

I, Varun Patial, hereby certify that the work which is being presented in this thesis entitled "Design of Low Noise Amplifier for WCDMA Reception Range (2.14 GHz – 2.17 GHz)" by me in partial fulfillment of the requirements for the award of degree of Master of Technology in VLSI Design from Thapar University, Patiala, is an authentic record of my own work carried out under the supervision of Dr. Alpana Agarwal.

The matter presented in this thesis has not been submitted in this or any other University/ Institute for the award of any degree.

Date: 9th July '2012

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It is certified that the above statement made by the student is correct to the best of my knowledge and belief.

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Date: (Varun Patial)

Place: Patiala

ABSTRACT

As the demand for 3G wireless network access is increasing so does the need for high performance Wide Band Code Division Multiple Access (WCDMA) transceivers. One of the key components of the WCDMA transceiver is the Low-Noise Amplifier (LNA). In this report, the design of a LNA to meet specifications is explained. The circuit was built using the BSIM3V2 model (Level 49) UMC CMOS 0.18μm technology along with Cadence Virtuoso as CAD tool.

The Concepts of RF IC design needed for the design of a Low Noise Amplifier such as nonlinearity, noise, skin effect, design of passive components is discussed in the report.
The understanding of these concepts is being applied to design a single ended and differential Low Noise Amplifier. With the LNA designed, the physical layout of the amplifier was performed using Cadence Assura. The layout/Physical design of LNA has been done so as to get the best possible matching with the actual fabricated circuit.

The design of the LNA for WCDMA reception range (2.11 GHz – 2.17 GHz) was simulated in Cadence to verify its performance. Single ended LNA is also successfully simulated for different corner conditions. From corner analysis the worst case power dissipation is found to be 8.703 mW and best one is 6.0912 mW. Similarly the worst case noise figure is 4.495 dB and best one is 3.247 dB. Variations found in center frequency is 1.4%.

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LIST OF ABBREVIATIONS

RF	Radio Frequency
LNA	Low Noise Amplifier
MOSFET	Metal Oxide Semiconductor Field Effect Transistor
IC	Integrated Circuits
WLAN	Wireless Local Area Network
WiMax	Worldwide Interoperability for Microwave Access
CDMA	Code Division Multiple Access
WCDMA	Wideband Code Division Multiple Access
EGPRS	Edge General Packet Radio Service
GSM	The Global System for Mobile Communications
BSIM	Berkeley Short-channel IGFET Model
UMC	United Microelectronics Corporation
CMOS	Complementary Metal Oxide Semiconductor
SNR	Signal to Noise Ratio
IIP3	Third Order Intercept Point
PF	Power Factor
ESR	Effective Series Resistance
DF	Dissipation Factor
GPS	Global Positioning System
DECT	Digital Enhanced Cordless Communications
UWB	Ultrawideband Wireless Receiver
DRC	Design Rule Check
LVS	Layout versus Schematic
PSS	Periodic Steady State
SNDR	Signal to Noise plus Distortion Ratio
SFDR	Spurious Free Dynamic Range

Chapter 1

Introduction

1.1 Overview of RF Industry

RF industry has changed quite a bit since the days of Marconi and Tesla-both the men who enabled radio communications. Modern radio frequency engineering is an exciting and dynamic field, due to the beneficial interdependency between recent developments in electronic device technology and the increase in demand for voice, data, and video communication capacity. Prior to this revolution in communications, RF technology was the nearly exclusive domain of the defence industry but the recent increase in demand for communications systems with applications such as wireless paging, broadcast video, Bluetooth transceiver, Wi–Fi (WLAN), WiMax, CDMA, WCDMA, EGPRS, GSM and many more is revolutionizing the industry. RF technology is important for these applications because these require high operational frequencies which allow both large numbers of independent channels as well as significant available bandwidth per channel for high speed communication. Figure 1.1 shows some disciplines that requires RF design.

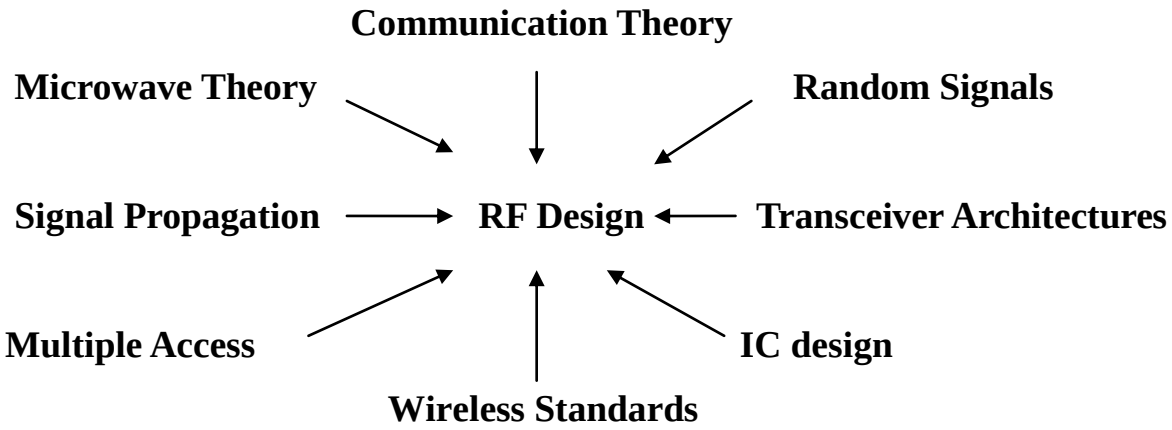

Figure 1.1: Disciplines Requiring RF Design [1].

The field of design in the electronics system that employs RF and Microwave Engineering includes the frequencies ranging from 300 kHz to over 100 GHz. RF engineering refers to the circuits/devices operating in the frequency range 300 kHz to over 1 GHz while the

microwave engineering refers to the circuits/devices operating in the frequency range between 300 kHz or 1 GHz to over 100 GHz. Unfortunately, RF IC design is quite complex when tested results are obtained that differ drastically from the simulation results. The reasons for this disparity may normally be traced to one of the following [2]:

- The frequency of operation is such that the circuit elements display complex behaviour, not represented by the pure element definitions utilized during the design.
- The circuit layout includes coupling paths not accounted for in the design.
- The ratio of the transverse dimensions of transmission lines to wavelength is non-negligible thus, additional unwanted stored modes become available.
- The package that houses the circuit becomes an energy storage cavity, thus absorbing some of the energy propagating through it.
- The perfect (ideally) dc bias source is not adequately decoupled from the circuit.
- The degree of impedance match among interconnected circuits is not good enough, so that large voltage standing wave ratio (VSWR) is present, which give rise to inefficient power transfer and to ripples in the frequency response.

1.2 Objective of Research

The main objective of the research presented in this thesis is to design a low noise amplifier to be used in radio technology for multimode operation. The goal of design is to understand the concepts of RF design such as gain, linearity, noise and matching networks that are essential for amplifiers. The approach for achieving this target is to use low noise amplifier in radio technology application for WCDMA reception range (2.11 GHz to 2.17 GHz).

1.3 Thesis Structure

This section describes the design of an amplifier used as the first building block of receiver of a transceiver system. For this design, BSIM3V2 model (Level 49) and CMOS 0.18μm technology is used. The overall thesis work is organised in eight chapters.

Chapter 2 discusses the introduction of Low Noise Amplifiers. This chapter also emphasis on different elements involved in RFICs design as they are essential for the design of low noise amplifier.

Chapter 3 discusses the details about the research work carried out so far in the design of low noise amplifiers for different domains of RF.

Chapter 4 discusses the design flow and design specifications that are followed in the design of low noise amplifier.

Chapter 5 discusses the different design steps involved for the design of this amplifier. It includes the single ended cascode amplifier with inductive source degeneration and also differential configuration.

Chapter 6 discusses the simulation results obtained from the different analysis carried out on the amplifiers.

Chapter 7 discusses the layout techniques and layout of single ended and differential low noise amplifier.

Chapter 8 discusses the conclusion and future scope of work.

Chapter 2

Low Noise Amplifier

2.1 Definition of Low Noise Amplifier

Low Noise Amplifier combines a low noise figure, reasonable gain, matching and stability without oscillation over entire useful frequency range. The Low Noise Amplifier (LNA) always operates in Class A, typically at 15-20% of its maximum useful current. Class A is characterized by a bias point more or less at the centre of maximum current and voltage capability of the device used, and by RF current and voltages that are sufficiently small relative to the bias point that the bias point does not shift. The smallest signal that can be received by a receiver defines the receiver sensitivity. The largest signal that can be received by a receiver establishes the upper power level limit of what can be handled by the system while preserving voice or data quality. The dynamic range of the receiver, the difference between the largest possible received signal and the smallest possible received signal, defines the quality of the receiver chain. The LNA function, plays an important role in the receiver designs. Its main function is to amplify extremely low signals without adding noise, thus preserving the required Signal-to-Noise Ratio (SNR) of the system at extremely low power levels. Additionally, for large signal levels, the LNA amplifies the received signal without introducing any distortions, which eliminates channel interference.

2.2 Elements of RF Circuit Design Required for Designing Low Noise Amplifier

Low Noise Amplifier was designed to be operated for radio frequency WCDMA application. Concepts of RF circuit design were necessary to understand before designing the low noise amplifier and some of them are discussed in this section.

2.2.1 Linearity

A system is said to be linear if output can be expressed as linear combinations of responses to input for two outputs $x_1(t)$ and $x_2(t)$ related to inputs $y_1(t)$ and $y_2(t)$ system is said to

be linear if

$$ax_1(t) + bx_2(t) = ay_1(t) + by_2(t) \quad (2.1)$$

In equation (2.1), is true for small signal but for large signal nonlinearities occurs between the input and output.

Some diverse effects of nonlinear behavior are discussed below:

Harmonic Distortion

For a memory-less time variant non linear system input is related to output as

$$y(t) = a_1x(t) + a_2x^2(t) + a_3x^3(t) + \cdots \quad (2.2)$$

where, a_j are in general functions of time if the system is time variant.

If sinusoidal signal $x\,(t) = B\,cos\omega t$ is applied to the nonlinear system the output is related to input as

$$y\,(t) = \frac{B^2a_2}{2} + (a_1B - \frac{3B^3a_3}{4})\,cos\,\omega t + \frac{B^2a_2}{2}cos\,2\omega t + \frac{B^3a_3}{4}cos\,3\omega t + \quad (2.3)$$

From equation (2.3), two conclusions can be made

- Even order harmonics (including dc component) vanish if the system has odd symmetry.
- The amplitude of the nth harmonic consists of a term proportional to n.

1dB Compression Point

By equation (2.3), because of addition of magnitude of third order harmonic to first order harmonic gain get reduced also when magnitude of third harmonic gets equal to that of magnitude of first order harmonic gain gets saturated. The input power/voltage for which gain gets reduced by 1dB compression point [1].

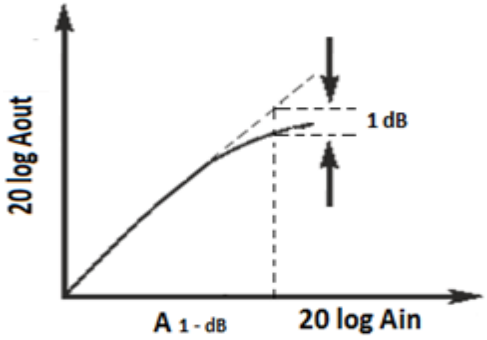

Figure 2.1: 1dB Compression Point [1].

Intermodulation

Another effect which can be noticed is that the RF amplifier tends to act as a mixer. It is quite possible for a harmonic of one signal to mix with the fundamental or a harmonic of the other. The third order sum products like $2f1 + f2$ are unlikely to cause a problem, but the difference products like $2f1 - f2$ can give significant problems. Take the example of a receiver set to 50 MHz where two strong signals are present, one at 50.00 MHz and the other at 50.01 MHz. The difference signals produced will be at 49.99 MHz and another at 50.01 MHz. As it can be seen either of these could cause interference on the band. Other higher order products can also cause problems: 3f1 - 2f2, 4f1 - 3f2, 5f1 - 4f2, and so forth all give products which may be able to pass through the receiver if it is tuned to the relevant frequency [2].

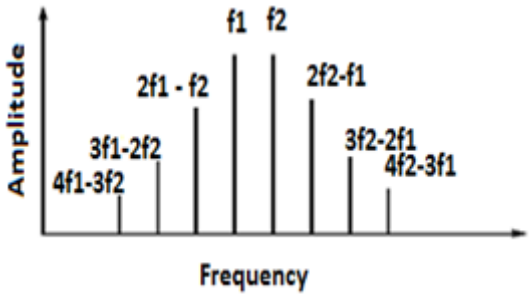

Figure 2.2: Intermodulation Products [2].

Third Order Intercept Point

It is found that the level of the intermodulation products rise faster than that of the required signal at the output. Essentially the RF amplifier will run into saturation and the levels of the signal will be limited. There is a point at which the level of a specific intermodulation product reaches that of the required signal that is it intercepts the level line for the required signal. This intercept point is called as third order intercept point (IIP3). Higher the level of intercept point the better the performance of the amplifier [1].

Intercept point for third order intercept is given by following equation:

$$\text{IIP3} = \sqrt{\frac{4}{3}\left|\frac{a_1}{a_3}\right|} \tag{2.4}$$

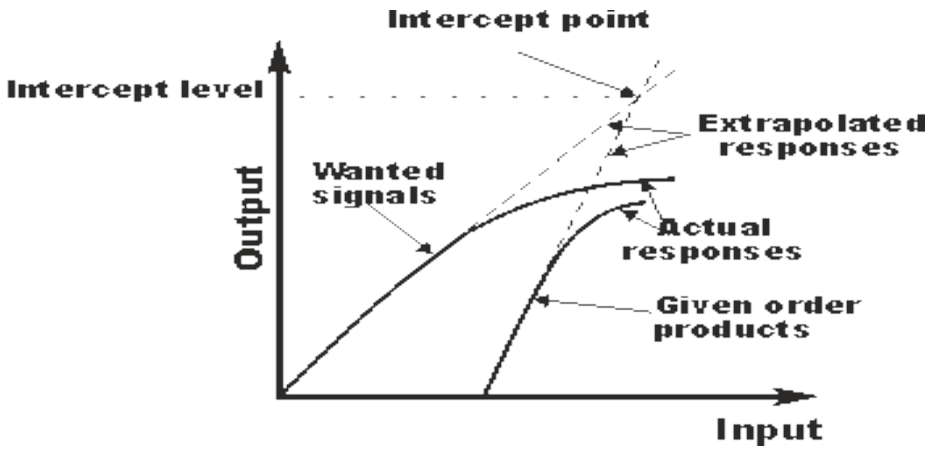

Figure 2.3: Receiver Intercept Point [2].

2.2.2 High Frequency MOSFET Model

Since RF IC designers have to deal with the issues like noise, gain, linearity and efficiency. A very important part of the design system is the accuracy of the model. It is also well known that as the frequency of operation increases parasitic components present in the circuit starts dominating. So the MOSFET model should be that it includes all these parasitic parameters into consideration.

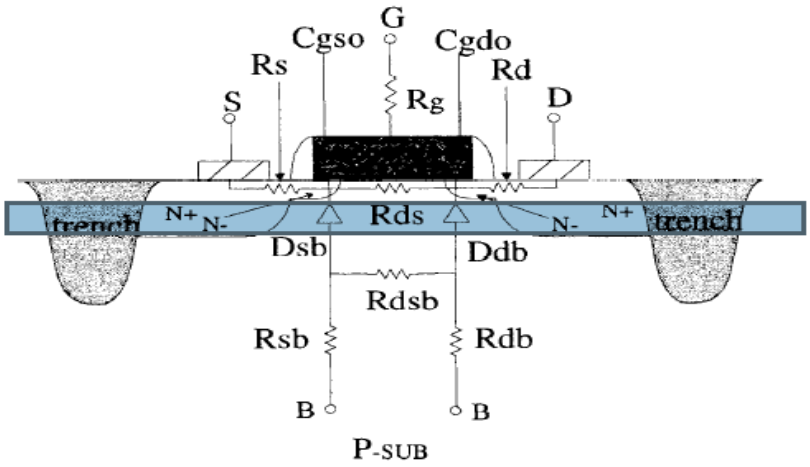

Figure 2.4: MOSFET High Frequency Model with Parasitic Components [3].

Figure 2.4 shows a BSIM3V3 high frequency MOSFET model with parasitic components. It is clear from the model that it's not only width and length that determines the accuracy of the model. For example, if for the same circuit one uses even number of fingers and other uses odd numbers of fingers, however length and width for both the designs are same but

perimeters for both the designs will be different. As a result diffusion capacitances are different for both cases which will lead to different behavior. Therefore, MOSFET model accuracy is very critical.

2.2.3 Circuit Noise

Noise limits the minimum signal level that a circuit can process with acceptable quality. Since noise is a random process, noise cannot be predicted at any time even if the past values are known. Analog integrated circuits are corrupted by two types of noise:-

- Environmental Noise: - It is due to the random disturbances that a circuit experiences through the supply or ground lines or through the substrate.
- Device Electronic Noise :- It is the noise created within the device and is of following types:-
    i. Thermal noise
    ii. Flicker noise

The environmental noise can be minimized by using differential input circuits with high CMRR. Here, our major concern is the device noise.

Thermal Noise

Thermal noise is due to the random thermal motion of the carriers in the channel. It is commonly referred to as a white noise source because its power spectral density holds a constant value up to very high frequencies (over 1 THz). Thermal noise has a power spectral density [3] given by:

$$\frac{\overline{i_d^2}}{\Delta f} = 4\,kT\,\frac{\mu}{L^2}\,(-Q1) \qquad (2.5)$$

where k is Boltzmann's constant, T is the absolute temperature, μ is the carrier mobility, L is the transistor length and Q1 is the total inversion layer charge. Equation (2.5) is suitable for both strong inversion and weak inversion provided that the appropriate Q1 is used [3].

Thermal Noise Due to Induced Drain Current

Since MOSFET is voltage controlled device. In the triode region of operation particularly, noise commensurate with resistance value [4].

$$i_d^2 = 4\,kT\,\gamma g_{d0}\Delta f \qquad (2.6)$$

where g_{d0} is the drain-source conductance at zero V_{DS}. The parameter γ has value of unity for

short channel devices and decreases to 2/3 for long channel devices [4].

Thermal Noise Due to Gate

The fluctuating channel potential couples capacitively into the gate terminal, leading to a noisy gate current [3].

The gate noise may be expressed as

$$\overline{\iota_{ng}^2} = 4\,\mathrm{kT}\delta g_g\,\Delta\mathrm{f} \tag{2.7}$$

where the parameter in equation (2.8), g_g is

$$g_g = \frac{\omega^2 C_{gs}^2}{5 g_{d0}} \tag{2.8}$$

The gate noise current clearly has a spectral density that is not constant. In fact, it increases with frequency, so it is often called as blue noise [4].

Noise Contribution Due to Distributed Gate Resistance

The distributed gate resistance of the CMOS transistor also contributes to the noise in low noise amplifier. This noise source is modelled as a series resistance with the gate and has a noise power equal to

$$v_g^2 = 4\mathrm{kT}R_g\Delta\mathrm{f} \tag{2.9}$$

where R_g is the gate resistance and is equal to

$$\mathrm{R_g} = \frac{\mathrm{R_{sq}W}}{3\mathrm{n^2L}} \tag{2.10}$$

In equation (2.10), $\mathrm{R_{sq}}$ is the sheet resistsnce of polysilicon, n is the number of fingers and the 3 comes from the distributed nature of the gate resistance . So from equation (2.10), this noise source can be made negligible by increasing the number of fingers used to make a transistor.

Noise Contribution Due to Source and Drain Resistance

Spectral noise power due to drain resistance ($\mathrm{R_D}$) and source resistance ($\mathrm{R_S}$) is calculated by following equation

$$\overline{\iota_n^2} = \frac{4\mathrm{kT}}{\mathrm{R_{S,D}}}\Delta\mathrm{f} \tag{2.11}$$

Flicker Noise

Flicker Noise is also known as 1/f noise and is more prominent in devices that are sensitive to surface phenomenon. Hence, MOSFET's exhibit significantly more 1/f noise. Charge trapping phenomenon are usually invoked to explain 1/f noise in MOSFET's. Some type of

defects and certain impurities can randomly trap and release charge. The trapping times are distributed in a way that lead to a 1/f noise spectrum in MOS. However, larger MOSFET exhibit less 1/f noise because their larger gate capacitance smooths the fluctuations in channel charge [4]. As the name suggests 1/f noise is not significant at high frequencies as compare to low frequencies.

2.2.4 Skin Effect

A conductor, at low frequencies, utilizes its entire cross-sectional area as a transport medium for charge carriers. As the frequency is increased magnetic field at the centre of the conductance presents impedance to the charge carriers, thus decreasing the current density at the corner of the conductor and increasing the current density around its perimeter. This increased current density near the edge of the conductor is known as skin effect. It occurs in all conductors including resistor leads, capacitor leads, and inductor leads. The depth at which the charge carrier-current density falls to 1/ e or 37% of its value along the surface, is known as skin depth and is a function of the frequency and the permeability and conductivity of the medium. The net result of skin effect is effective decrease in the cross sectional area of the conductor and therefore, a net increase in the ac resistance of the wire.

Shaded region in the figure 2.5 shows the area in which RF current flow. From the figure 2.5 skin depth area is equal to $\pi\,(R_2^2 - R_1^2)$ and skin depth (δ) is given by

$$\delta = \frac{1}{\sqrt{\pi f \mu \sigma}} \tag{2.12}$$

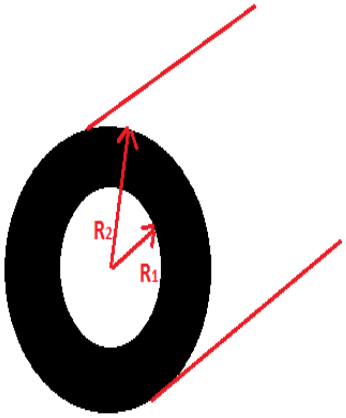

Figure 2.5: Skin Depth Area of a Conductor [5].

In equation (2.12), f is the signal frequency, μ is permeability of the medium surrounding the conductor, and σ is the conductivity of the metal making the conductor. It is clear that the skin depth is inversely proportional to the square root of the frequency and the conductivity. Since the skin depth represents the frequency-dependent energy loss due to propagation in the resistive region within a skin depth of the surface, it is important to minimize it. This can be achieved by choosing a conductor metal with high conductivity.

2.2.5 Scattering Parameters

Scattering parameters or S-parameters (the elements of a scattering matrix or S-matrix) describe the electrical behavior of linear electrical networks when undergoing various steady state stimuli by electrical signals. The parameters are useful for electrical engineering, electronics engineering, and communication systems design, and especially for microwave engineering. The S-parameters are members of a family of similar parameters, other examples being: Y-parameters, Z-parameters, H-parameters, T-parameters or ABCD-parameters. They differ from these, in the sense that S-parameters do not use open or short circuit conditions to characterize a linear electrical network; instead, matched loads are used. These terminations are much easier to use at high signal frequencies than open-circuit and short-circuit terminations. Moreover, the quantities are measured in terms of power. Many electrical properties of networks of components (inductors, capacitors, resistors) may be expressed using S-parameters, such as gain, return loss, voltage standing wave ratio (VSWR), and reflection coefficient and amplifier stability. The term scattering is more common to optical engineering than RF engineering, referring to the effect observed when a plane electromagnetic wave is incident on an obstruction or passes across dissimilar dielectric media. In the context of S-parameters, scattering refers to the way in which the traveling currents and voltages in a transmission line are affected when they meet a discontinuity caused by the insertion of a network into the transmission line. This is equivalent to the wave meeting impedance differing from the line's characteristic impedance. Although applicable at any frequency, S-parameters are mostly used for networks operating at radio frequency (RF) and microwave frequencies where signal power and energy considerations are more easily quantified than currents and voltages. S-parameters change with the measurement frequency, so frequency must be specified for any S-parameter measurements stated, in addition to the characteristic impedance or system impedance. By

definition S-parameters for any two port system can be defined as

$$b_1 = S_{11}a_1 + S_{12}a_2 \quad (2.13)$$

$$b_2 = S_{21}a_1 + S_{22}a_2 \quad (2.14)$$

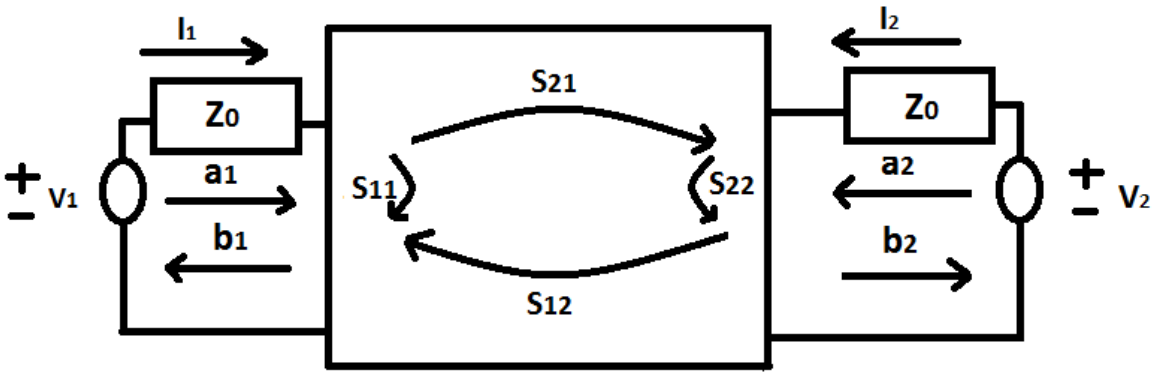

Figure 2.6: S-Parameter Two Port Model.

From figure 2.6, the independent variables, a1 and a2 are normalized incident voltage defined as:-

$$a_1 = \frac{V_1 + I_1 Z_0}{2\sqrt{Z_0}} = \frac{Voltage\ wave\ incident\ on\ port1}{2\sqrt{Z_0}} = \frac{v_{i1}}{\sqrt{Z_0}} \quad (2.15)$$

$$a_2 = \frac{V_2 + I_2 Z_0}{2\sqrt{Z_0}} = \frac{Voltage\ wave\ incident\ on\ port2}{2\sqrt{Z_0}} = \frac{v_{i2}}{\sqrt{Z_0}} \quad (2.16)$$

The dependent variables, b1 and b2 are normalized reflected waves defined as

$$b_1 = \frac{V_1 - I_1 Z_0}{2\sqrt{Z_0}} = \frac{Voltage\ wave\ reflected\ from\ port1}{2\sqrt{Z_0}} = \frac{v_{r1}}{\sqrt{Z_0}} \quad (2.17)$$

$$b_2 = \frac{V_2 - I_2 Z_0}{2\sqrt{Z_0}} = \frac{Voltage\ wave\ reflected\ \ from\ port2}{2\sqrt{Z_0}} = \frac{v_{r2}}{\sqrt{Z_0}} \quad (2.18)$$

In equations (2.15, 2.16, 2.17 and 2.18),

V_1 is voltage incident on input port,

I_1 is current entering in input port,

I_2 is reverse current flowing from output port to input port,

V_2 is voltage obtained at output port, and Z_0 is characteristic impedance.

a_i and b_i represents transmission and reflections of power or voltage at the input and output port. From equations (2.13 and 2.14) scattering coefficients are defined as:

S_{11} (power / voltage reflected back to port1, not transmitted) $= \frac{b_1}{a_1}$ at ($a_2 = 0$) (2.19)

S_{21} (power / voltage transmitted to port2 from port1) $= \frac{b_2}{a_1}$ at ($a_2 = 0$) (2.20)

S_{12} (power/voltage transmitted to port1 from port2) $= \frac{b_1}{a_2}$ at ($a_1 = 0$) (2.21)

S_{22} (power/voltage reflected back to port2, not transmitted) $= \frac{b_2}{a_2}$ at ($a_1 = 0$) (2.22)

Reflection Coefficient and Scattering Parameter Coefficient

The reflection coefficient is defined as the ratio of the amplitude of the reflected wave to the amplitude of the incident wave. This is typically represented with a Ґ. The reflection coefficient can be given by the equations below, where Z_S is the impedance toward the source, Z_L is the impedance toward the load.

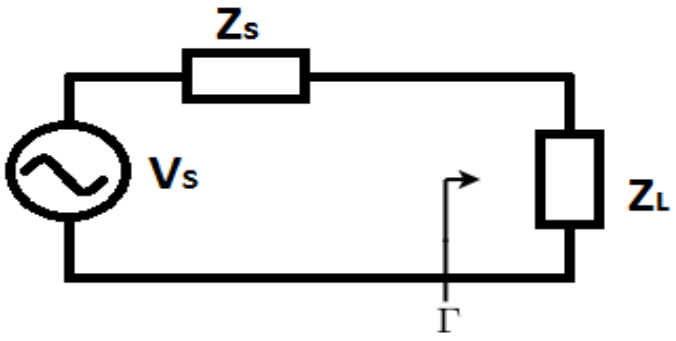

Figure 2.7: Circuit for Measuring Reflection Co-efficient.

From figure 2.7, reflection co-efficient can be given as

$$Ґ = \frac{Z_L - Z_S}{Z_L + Z_S} \quad (2.23)$$

From equation (2.19),

$$S_{11} = \frac{b_1}{a_1} = \frac{\frac{V_1}{I_1} - Z_0}{\frac{V_1}{I_1} + Z_0} = \frac{Z_1 - Z_0}{Z_1 + Z_0} = \acute{\Gamma}_{in} \quad (2.24)$$

From equation (2.24), scattering coefficient S_{11} is equal to input reflection coefficient of a two port RF system, so ideal value of S_{11} is equal to zero. Similarly S_{22} is equal to output reflection coefficient and its value is also equal to zero.

2.2.6 Passive Components

Resistors

Resistors are used everywhere in circuits, as transistor bias networks, pads, and signal combiners. However, very rarely is there any thought given to how a resistor actually behaves once depart from the world of direct current. In some instances as in MOSFET's biasing networks, the resistors will still perform its DC circuit function, but it may also disrupt the circuit's RF operating point [5].

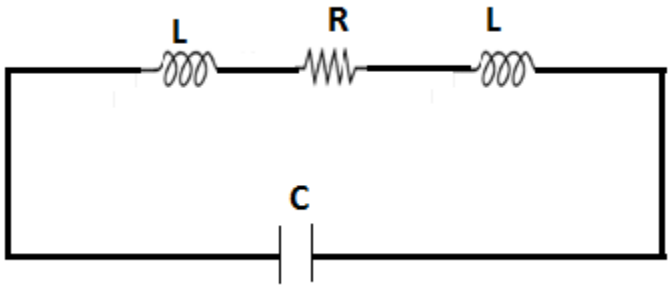

Figure 2.8: Resistor Equivalent Circuit [5].

Figure 2.8 shows the equivalent circuit of resistor at radio frequencies. In figure 2.8, R is the resistor value itself, L is the lead inductance, and C is parasitic capacitances which vary from resistor to resistor's structure. A carbon composition resistor is notoriously poor structure. Wirewound resistors have problems at radio frequencies these resistors tend to exhibit varying impedances over various frequencies. The inductor shown in figure 2.8 is much larger for wirewound resistors than for a carbon composition resistor. Because wirewound resistors look like inductors, their frequencies will first increases. At some frequency $F_{r,}$ however, it resonates with shunt capacitance C, producing an impedance peak. Any further increase in the frequency will cause the resistor's value to decrease as shown in figure 2.9.

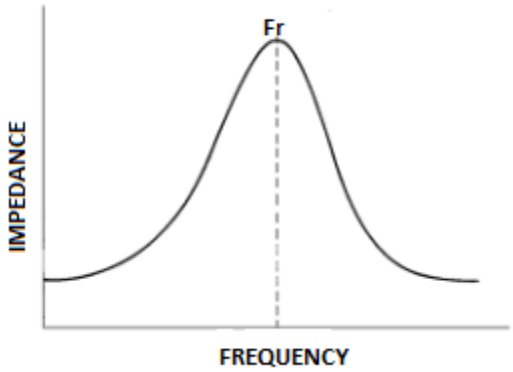

Figure 2.9: Impedance Characteristics of a Wirewound Resistor [5].

Capacitors

Capacitors are used extensively in RF applications, such as bypassing, interstage coupling, and in resonant circuits and filters. It is important to remember, however, that not all capacitors lend themselves equally well to each of the above-mentioned applications.

Real-World Capacitors

The usage of capacitors is primarily dependent upon the characteristics of its dielectric. Any losses or imperfections in the dielectric have an enormous effect on circuit operation.

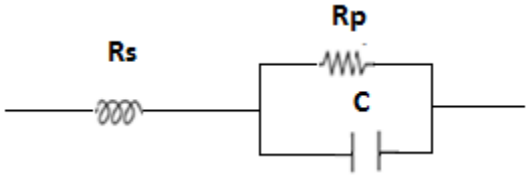

Figure 2.10: Capacitor Equivalent Circuit [5].

Figure 2.10 shows the equivalent circuit of capacitor at high frequencies where C equals the capacitance, R_s is the heat-dissipation loss expressed either as a power factor (PF) or a dissipation factor (DF), R_p is the insulation resistance, and L is the inductance of the leads and plates.

Following are some definitions regarding real capacitors:

Power Factor (PF)

In a perfect capacitor, the alternating current will lead the applied voltage by 90 degrees. This phase angle (φ) will be smaller in a real capacitor due to the total series resistance ($R_s + R_p$) shown in equivalent circuit in figure 2.10.

Insulation Resistance

This is a measure of amount of DC current that flows through the dielectric of a capacitor with a voltage applied. No material is perfect insulator; thus some, leakage current must flow. This current path is shown by R_p in the equivalent circuit in figure 2.10.

Effective Series Resistance (ESR)

This resistance is the combined equivalent of R_s and R_p, and is the ac resistance of a capacitor

$$\text{ESR} = \frac{\text{PF}}{\omega \text{C}} (10^6) \tag{2.25}$$

where ω is angular frequency and is equal to 2πf.

Dissipation Factor (DF)

The DF is the ratio of the ac resistance to the reactance of a capacitor and is given by

$$DF = \frac{ESR}{X_c} \times 100\% \tag{2.26}$$

Quality Factor

The Q of a circuit is the reciprocal of DF. Thus larger the Q, better the capacitor.

The effect of these imperfections in the capacitor is shown graphically.

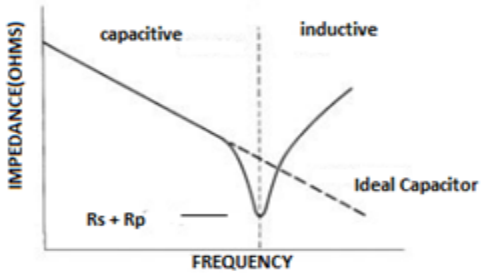

Figure 2.11: Ideal versus Real Capacitors [5].

Inductors

Inductors are used extensively in RF design in resonant circuits, filters and delay networks, and as RF chokes used to prevent, or at least, the flow of RF energy along a certain path.

Real-World Inductors

Whenever two conductors are brought into close proximity but separated by a dielectric, and

place a voltage differential between the two, we form a capacitor. Thus, if any wire resistance at all exists, a voltage drop will occur between the windings, and small capacitors will be formed.

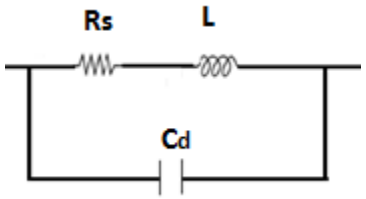

Figure 2.12: Inductor Equivalent Circuit [5].

This effect occurs in the real-world and results in the formation of capacitance C_d as shown in the figure 2.12. The effect of C_d is shown in figure 2.13 as it can be observed that ideally at high frequencies inductor impedance should increase but due to C_d it decreases.

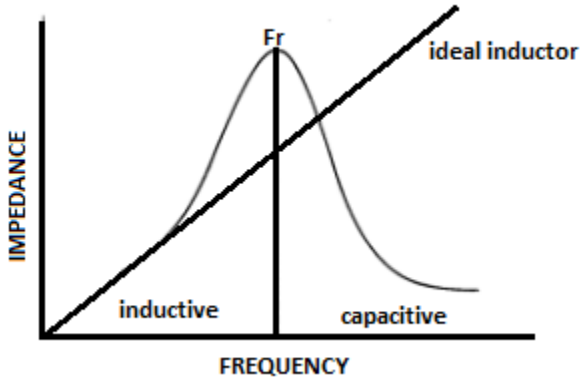

Figure 2.13: Ideal versus Real Inductors [5].

Quality Factor

Quality factor of inductor is defined as the ratio of an inductor's reactance to series resistance. The larger the ratio, the better is the inductor.

$$Q = \frac{X}{R_S} \tag{2.27}$$

If the inductors were wound with a perfect conductor, its Q would be infinite and it will be a lossless inductor. Since no conductor is perfect, inductor always has some finite Q. At low frequencies, the Q of an inductor is very good because the only resistance in the winding is the dc resistance of the wire which is very small. But as the frequency increases, skin effect and winding capacitances begin to degrade the quality of the inductor.

Chapter 3

Literature Survey

Low Noise Amplifier is an important component of the transceivers used at radio frequencies. It combines low noise figure, reasonable gain, matching and stability without oscillation over entire useful frequency range. Figure 3.1 shows the block diagram of typical LNA that employs matching and amplifying stage.

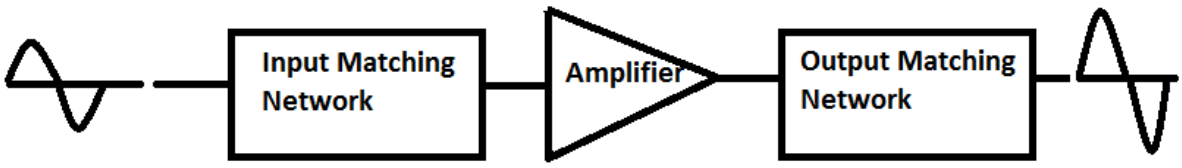

Figure 3.1: LNA Block Diagram.

Lot of research is being currently done in designing Low Noise Amplifier. Some of them are discussed below:

3.1 Application Based LNA's

An 1. 5 GHz, low noise amplifier, intended for use in a Global Positioning System (GPS) Receiver is discussed by Derek K. Shaeffer *et al.* [7]. They used inductive source degeneration topology for design of LNA.

An 1. 9 GHz, low noise amplifier, intended for use in a **DECT (Digital Enhanced Cordless Communications) Receiver** is discussed by **Jerome Le Ny *et al.* [6].** They used differential configuration with inductive source degeneration and constant g_m bias for design of LNA.

The concept of **Concurrent Multiband Low Noise Amplifiers** is introduced by **Hussein Hashemi *et al.* [8].** They discuss the advantages of field effect transistors over bipolar junction transistor and concurrent dual band low noise amplifier in communication systems.

An $3.1\ GHz - 10.6\ GHz$, low-noise amplifier, intended for use in **Ultrawideband Wireless Receiver** is discussed by **Andrea Bevilacqua *et al.* [9].** In the design they discussed why the low noise amplifier is essential for UWB receiver role of LNA in UWB receiver. In their design they used multisection Chebyshev filter at the input network and buffer stage at the output stage for design of LNA.

An $3.0\ GHz - 4.9\ GHz$ and $6.2\ GHz - 10.2\ GHz$, low-noise amplifier, intended for use in **Ultrawideband Wireless Receiver** is discussed by **Che-Cheng Huang1 *et al.* [5].** They used of two stage cascode amplifiers with shunt-peaked load, two 2^{nd} order notch filters and an output buffer for design of LNA.

An $2.0\ GHz - 9.6\ GHz$, low-noise amplifier, intended for use in **Ultrawideband Wireless Receiver frontend** is discussed *by* **Qiang Li *et al.* [11].** They used current-reuse topology, capacitive peaking for design of LNA. Inductors were not used in the design.

An $3.1\ GHz - 10.6\ GHz$, low-noise amplifier, intended for use in **Ultrawideband Wireless Receiver** is discussed by **Michael T. Reiha *et al.* [12].** They used current-reuse topology and reactive feedback for design of LNA.

An $3.1\ GHz - 5.1\ GHz$, low-noise amplifier, intended for use in **Ultrawideband Wireless Receiver** is discussed by **Zhe-Yang Huang *et al.* [13].** They used wideband input impedance matching network, a cascode amplifier with shunt-peaked load, a RLC impedance feedback loop and an output buffer for design of LNA.

An 402 MHz – 405 MHz, low-noise amplifier, intended for use in **Medical Implant Communication Service** is discussed by **Sherif A. Saleh *et al*.[14].** They used cascode LNA with inductive source degeneration, LC folded cascode LNA topology and current reuse technique for comparison of three RF LNA's.

An 7.2 GHz and 7.0 GHz, multistage low-noise amplifier, intended for use in **Ultrawideband Wireless Receiver** frontend is discussed by **Meng-Ping Chen *et al.* [15].** They used three LC-tank cascode amplifier and one output buffer for design of LNA.

An 5 GHz and 5.5 GHz, **low-noise amplifier**, intended for use in **Multiband Applications** is discussed by **Bevin G. Perumana, Jing-Hong *et al*. [16].** They designed two low noise amplifiers one with current reuse topology and second with tuned resistive feedback for measurement purpose also inductors were not used in both designs.

An 2.4 GHz, low-noise amplifier, a frequency doubler subharmonic mixer, intended for use in **Short-Range Radio in Biomedical Devices** is discussed by **T. Hui Teo *et al.* [17].** They used common-gate, common-source topology for design of LNA.

An 3.3 GHz – 3.8 GHz, **low-noise amplifier,** intended for use in **WiMax system** is discussed by **Yu-Lin Wang [18].** They used differential, cascode configuration RC shunt feedback and shunt peak load for design of LNA.

An 0.9/2.4 *GHz*, low noise amplifier, intended for use in **Concurrent Dual Band GSM and Bluetooth Application** is discussed by **Sambit Datta *et al.* [19].** They used capacitor between the gate and source instead of conventional source degeneration and peak shunting at the output for the design of LNA.

An 3.1 GHz– 10.6 GHz, low-noise amplifier, intended for use in **Ultrawideband Wireless Receiver** is also discussed by **Shila Shamsadini *et al.* [20].** They used two-stage, common-

gate in cascade with cascode for design of LNA. Table 1 shows the summary of application based LNA's.

Table 1: Summary of Application Based LNA's

Parameters	**[7]**	**[6]**	**[9]**	**[10]**	**[11]**	**[15]**	**[18]**	**[20]**
Year	1997	2002	2004	2007	2007	2008	2009	2010
Technology (μm)	0.6	0.25	0.18	0.18	0.13	0.09	0.18	0.18
S11(dB)	-	-	-10	-6.4	-8.3	-	-11	-10
S22(dB)	-	-		-10.1	-	-	-10.9	-10
S21(dB)	22	15	9.3	13.3, 15.5	11	24.4	14.4, 12.4	-
Area Occupied(mm^2)	0.12	0.23	-	-	0.05	0.02	-	-
IIP3(dBm)	12.7	-5	-6.7	-	0.72	-	-	-
Power Consumed(mW)	30	25	9	21.9	19	9.2	14.8	10
Noise Figure(dB)	3.5	2	4	2.5, 2.8	4.8	2.4	3.8	2.9

3.2 High Gain LNA's

Bevin G.Perumana *et al.* [16], used inductorless resistive feedback with current reuse topology and tuned resistive feedback for increase of gain in low noise amplifier for **multiband applications.**

T. Hui Teo *et al.* [17], used fully integrated differential configuration for increase of gain in low noise amplifier for **short-range radio in biomedical devices.**

Shila Shamsadini *et al.* [20], used two-stage, common-gate in cascade with cascode for increase in gain low noise amplifier **for UltraWideband applications.**

Jenn-Tzer Yang *et al.* [21], used differential configuration and high-Q active inductor for

design of low noise amplifier for **multiband applications.**

Baoyong Chi *et al.* [22], used L type inter-stage matching network between the input transistors and the cascode transistor which could enhance both the gain and the gain bandwidth. The gain bandwidth could be further enhanced by the resistors inserted between the bulks and the sources of the input transistors since the resistors could reduce the effects of the drain-bulk capacitance of the input transistors. Table 2 shows the summary of high gain LNA's.

Table 2: Summary of High Gain LNA's

Parameters	**[16]**	**[17]**	**[20]**	**[21]**
Year	2008	2008	2010	2007
Technology(μm)	0.09	0.18	0.18	0.18
S21(dB)	22,24.4	26	25	40.7

3.3 Different Matching Techniques for LNA's

Derek K. Shaeffer *et al*. [7], discussed the different matching topologies at the input. It includes resistive termination, $1/g_m$ termination, shunt−series feedback, inductive degeneration. For designing they used inductive degeneration because of its advantage of providing low noise figure, high linearity, and high gain.

Andrea Bevilacqua *et al*. [9], used an inductively degenerated common-source amplifier by embedding the input network of the amplifying device in a multisection reactive network so that the overall input reactance is resonated over a wider bandwidth.

Michael T. Reiha *et al.* [12], used modified cascode in a negative feedback configuration. Negative feedback offer tailor port impedances for noise and impedance matching.

Zhe-Yang Huang *et al.* [13], used wideband input impedance matching network, a cascode amplifier with shunt-peaked load, a RLC impedance feedback loop and an output buffer for input and output matching.

Meng-Ping Chen *et al.* [15], used input impedance matching network that included the conventional source degeneration input matching and an inductor shunted in a shunted resistor in RF signal path. The shunted resistor in RF path saved the three inductors used for design of Butterworth filter required earlier for the design in specified application.

Sambit Datta *et al.* [19], in their design conventional source degeneration inductor was eliminated for higher signal gain while providing reasonable input impedance. They also used capacitor between the gate and the source of the input transistor by that a noise source from the gate resistance is partly suppressed. The output matching network was constructed of shunt peaking. Table 3 shows the summary of different matching techniques for LNA's.

Table 3: Summary of Different Matching Techniques for LNA's

Parameters	[7]	[9]	[12]	[13]	[15]	[19]
Year	1997	2004	2007	2007	2008	2010
Technology(μm)	0.6	0.18	0.13	0.18	0.18	0.13
S11(dB)	-	-10	-44 to 9.9	-10.1	-6.8	-25/-15
S22(dB)	-	-	-	-9.76	-9.5	-

3.4 Low Noise Techniques for LNA's

Derek K. Shaeffer *et al.* [7], used the inductive degeneration topology for design of low noise amplifier. They discussed the advantage of having low noise figure of the induction degeneration over the other existing topologies (resistive termination, $1/g_m$ termination, shunt–shunt feedback).

Michael T. Reiha *et al.* [12], used the reactive (negative) feedback for design of low noise amplifier, reactive feedback reduces the noise figure by reducing the input insertion loss, flat group delay and lowering input referred noise.

Andries J. Scholten *et al.* [23], discussed the noise modeling for RF CMOS circuits that included effect of drain current noise and gate noise for short channel MOSFETs. The results

was modeled with a non quasi- static RF model, based on channel segmentation, which is capable of predicting both drain and gate current noise accurately. Two additional noise mechanisms: avalanche noise associated with the avalanche current from drain to bulk and shot noise in the direct-tunneling gate leakage current is also discussed.

Xiao-dong Wang *et al.* [24], they added the capacitor between the gate and the source of the input MOSFET in cascode low noise inductive degeneration topology for reducing the noise figure in amplifiers.

Jenn-Tzer Yang *et al.* [25], used high-Q active inductor and differential configuration for lowering the noise figure. Table 4 shows the summary of low noise techniques for LNA's.

Table 4: Summary of Low Noise Techniques for LNA's

Parameters	[7]	[12]	[24]	[25]
Year	1997	2007	2008	2007
Technology(μm)	0.6	0.13	0.18	0.18
NF(dB)	3.5	0.43	0.655	0.55 to 0.758

3.5 Low Power LNA's

Michael T. Reiha *et al.* [12], and G. Perumana *et al.* [16], design the low noise amplifier using current reuse topology for low power measurement purpose.

T.Hui Teo *et al.* [17], used common-gate common-source configuration to design topology for low power measurement purpose. Besides being able to operate at low-power CG-CS LNA eliminates the use of on-chip spiral inductors for input matching in the CS-LNA design. Table 5 gives the summary of low power LNA's.

Table 5: Summary of Low Power LNA's

Parameters	[12]	[16]	[17]
Year	2007	2008	2008
Technology(μm)	0.13	0.09	0.18
Power Consumed(W)	9m	9.2m – 12m	4.5m

3.6 Gaps in Present Study

The literature available mainly focuses

- Minimizing noise and maximizing gain of Low Noise Amplifiers. Still a lot of work has to be carried out related with low power consumption, low area and linearity of Low Noise Amplifiers.
- The most of architectures available in the literature made use of resistors for biasing purposes instead of using reference circuits and very less attention is given to the PVT variations.
- Very less literature is available on the layout techniques of inductors which are essential in RF domain.

3.7 Problem Definition

Physical design of Low Noise Amplifier for WCDMA application with frequency range as (2.11 GHz – 2.17 GHz) having power consumption less than 9 mW.

Chapter 4

Custom IC Design Flow and Design Specifications

4.1 Custom IC Design Flow

Low noise amplifier is designed in Cadence Virtuoso Environment version 5.14. Cadence design environment supports custom IC design flow (full custom design flow) that includes following steps to design any circuit.

Design Specifications The design flow for a any circuit always starts with a set of design specifications. The "specs" typically describe the expected functionality of the designed block, as well as the maximum allowable delay times, the silicon area and other properties such as power dissipation. Usually, the design specifications allow considerable freedom on issues concerning the choice of a specific circuit topology, individual placement of the devices, the locations of input and output pins, and the overall aspect ratio (width-to-height ratio) of the final design.

Schematic Capture The traditional method for describing the design is via the schematic editor. Schematic editors provide simple, intuitive means to draw, to place and to connect individual components that make up design. The resulting schematic drawing must accurately describe the main electrical properties of all components and their interconnections. Also included in the schematic are the power supply and ground connections, as well as all "pins" for the input and output signals of the circuit. This information is crucial for generating the corresponding netlist, which is used in later stages of the design. The generation of a complete circuit schematic is therefore the first important step of the design flow.

Simulation Once the transistor-level description of a circuit is completed using the schematic Editor, the electrical performance and the functionality of the circuit must be verified using a simulation tool. The detailed transistor-level simulation of design will be the first in-depth validation of its operation, hence, it is extremely important to complete this step before proceeding with the subsequent design optimization steps. The initial simulation phase also serves to detect some of the design errors that may have been created during the

schematic entry step. It is quite common to discover errors such as a missing connection or an unintended crossing of two signals in the schematic.

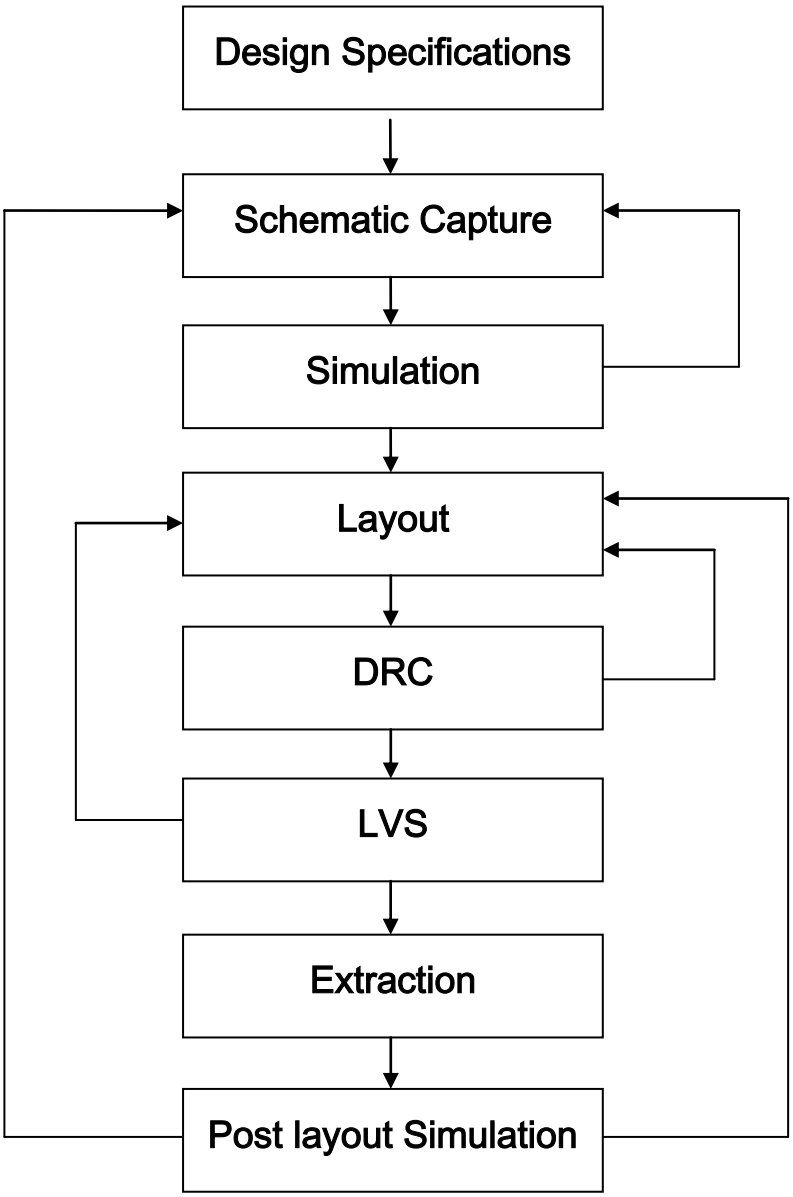

Figure 4.1: Custom IC Design Flow [5].

Layout The creation of the mask layout is one of the most important steps in the full-custom design flow, where the designer details all geometries and the relative positioning of each geometry or mask layer to be used in actual fabrication, using a layout editor. Physical

layout design is very tightly linked to overall circuit performance (area, speed and power dissipation) since the physical structure determines the transconductances of the transistors, the parasitic capacitances and resistances, and obviously, the silicon area which is used to realize a certain function.

Design Rule Check (DRC) The created mask layout must conform to a complex set of design rules, in order to ensure a lower probability of fabrication defects.

Layout Versus Schematic Check (LVS) After the mask layout design of the circuit is completed, the design should be checked against the schematic circuit description created earlier. It is done by "Layout Versus Schematic (LVS) Check". It will compare the original network with from the mask layout, and prove that the two networks are indeed equivalent. The LVS step provides an additional level of confidence for the integrity of the design, and ensures that the mask layout is a correct realization of the intended circuit topology. The LVS check only guarantees topological match. A successful LVS will not guarantee that the mask layout will actually satisfy the performance requirements. Any errors that may show up during LVS (such as unintended connections between transistors, or missing connections/devices, *etc.*) should be corrected in the mask layout before proceeding to post-layout simulation.

Extraction Circuit extraction is performed after the mask layout design is verified against schematic, in order to create a detailed net-list (or circuit description) for the simulation tool. The circuit extractor is capable of identifying the individual transistors and their interconnections (on various layers), as well as the parasitic resistances and capacitances that are inevitably present between these layers. Thus, the "extracted net-list" can provide a very accurate estimation of the actual device dimensions and device parasitics that ultimately determine the circuit performance.

Post Layout Simulation The electrical performance of a full-custom design can be best analyzed by performing a post-layout simulation on the extracted circuit net-list. At this point, the design should have a complete mask layout of the intended circuit/system, and should have passed the DRC and LVS steps with no violations. The detailed (transistor-level) simulation performed using the extracted net-list will provide a clear assessment of the circuit speed, the influence of circuit parasitics (such as parasitic capacitances and

resistances), and any glitches that may occur due to signal delay mismatches. If the results of post-layout simulation are not satisfactory, the design need to modify some of the transistor dimensions and/or the circuit topology, in order to achieve the desired circuit performance under "realistic" conditions, *i.e.*, taking into account all of the circuit parasitics. This may require multiple iterations on the design, until the post-layout simulation results satisfy the original design requirements. Finally, the satisfactory result in post-layout simulation is still no guarantee for a completely successful product; the actual performance of the chip can only be verified by testing the fabricated prototype.

4.2 Design Specifications

Low Noise amplifier designed for WCDMA reception range (2.11GHz−2.17GHz) using 0.18μm CMOS technology. CMOS technology was used because of its several advantages such as low cost, low static power dissipation and low area. Following specifications outline the requirements for LNA.

Table 6: LNA Specifications

Parameters	Specification
Voltage Gain(dB)	14
Centre Frequency(GHz)	2.14
Noise Figure(dB)	5
Third Order Intercept Point(dBm)	−20
Matching Parameters (dB)	−5
Supply Voltage(V)	1.8
Power Consumption(mW)	9

These specifications ensure that the LNA will provide sufficient gain with minimum noise added while maintaining linearity.

Chapter 5

Design Methodology

5.1 Matching Technique Used

It's not amplifier that alone determines the performance but matching networks also play a crucial role in the design of low noise amplifier. Consider if the load is not properly terminated, now imagine the path from the antenna to the amplifier, it will usually go through either a cable or through PCB trees before reaching the LNA. If the LNA is not matched, the impedance seen by the antenna depends on length of the transmission line.

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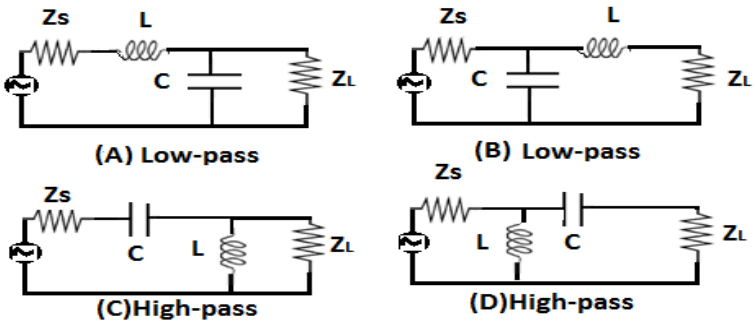

Figure 5.1: Impedance Matching Circuits [5].

This is a bad situation because the power reaching the LNA cannot be predicted. But if the impedance is match, then certainly regardless of the length of the transmission line the input power is well known and fixed. Different matching networks are shown in the figure 5.1. Over the years many modified impedance matching networks have been used. The brief description of various impedance matching networks are discussed in the following sections.

5.1.1 Resistive Termination

Although resistive termination shown in figure 5.2 provide 50Ω termination but it suffers from poor noise figure.

Noise figure of a circuit is given by following relation:

$$\text{Noise figure} = \frac{\text{Total Output Noise}}{\text{Total Noise Due To Source}} \quad (5.1)$$

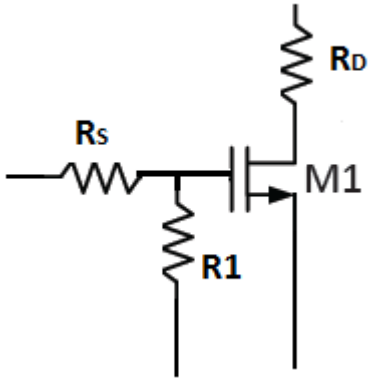

Figure 5.2: Resistive Termination Matching MOSFET [7].

Calculating noise figure from figure 5.2:

Indentifying the noise sources in the circuit

(i) Due to source resistance R_S

$$\overline{v_{nR_S}^2} = 4kTBR_S \tag{5.2}$$

(ii) Due to termination resistance R_1

$$\overline{v_{nR_1}^2} = 4kTBR_1 \tag{5.3}$$

(iii) Due to induced drain current

$$\overline{\imath_d^2} = 4kT\,(\gamma g_{do})\,B \tag{5.4}$$

In equation (5.4), γ is a constant that has value unity for linear region and reduced to 2 / 3 in saturation region and g_{do} is zero bias drain conductance.

(iv) Due to load resistance R_L

$$\overline{\imath_L^2} = 4kT\,G_L\,B \tag{5.5}$$

G_L is the load transconductance.

So from equations (5.2) to (5.5) total output noise current is given by

$$\overline{\imath_o^2} = \overline{\imath_d^2} + \overline{\imath_L^2} + \left(\overline{v_{nR_S}^2} + \overline{v_{nR_1}^2}\right) g_m^2 \tag{5.6}$$

So noise figure using equation (5.2, 5.3, 5.4, 5.5 and 5.6) is given by

$$F = 1 + \frac{R_1}{R_S} + \frac{\gamma}{g_m R_S} + \frac{G_L G_S}{g_m^2} \tag{5.7}$$

From equation (5.7), it is observed that even if g_m becomes very large noise figure still will be dominated by termination resistance R_1. Hence, termination by resistor is not a good option as noise figure is very high.

5.1.2 Common Gate Termination

This type of termination can be achieved by using the source of common base or gate as the input termination as shown in figure 5.3.

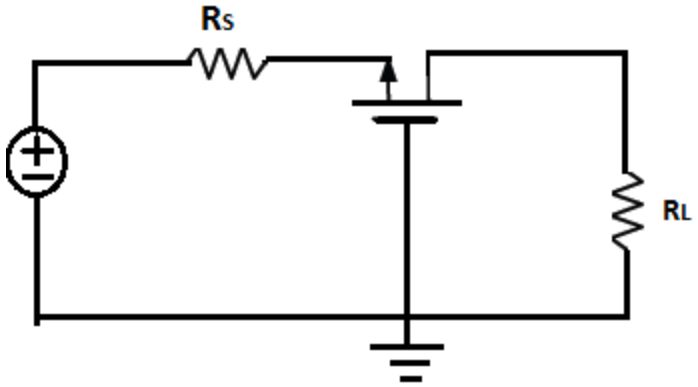

Figure 5.3: Common Gate Termination MOSFET [7].

The noise figure of this configuration can be calculated by just considering the effect of drain current. Since the drain current is injected into the input, it adds noise in the shunt with the input noise current. By definition,

$$\text{Noise figure (F)} = \frac{\text{Total output noise}}{\text{Total noise due to source}} = \frac{\overline{i_s^2}+\overline{i_d^2}}{\overline{i_s^2}} \tag{5.8}$$

$$F = 1 + \frac{4kT\,\gamma B g_{ds0}}{4kTGsB} \tag{5.9}$$

on solving equation (5.9)

$$F = 1 + \frac{\gamma}{\alpha} \tag{5.10}$$

in equation (5.10) it is assumed that Gs = g_m and $\alpha = {g_m}/{g_{ds0}}$

Since γ is 2 /3 for saturation region and α is unity. Putting these values in equation (5.10), noise figure is typically equal to 2.2dB and for short channel devices this value may increase to 3dB [5]. So (1 / g_m) termination is not a good way for matching purposes.

5.1.3 Shunt−Series Feedback

Figure 5.4 illustrates yet another topology, which uses resistive shunt feedback to set the input impedance of the LNA. Amplifiers using shunt-series feedback often have extraordinarily high power dissipation compared to others with similar noise performance. Intuitively, the higher power is partially due to the fact that shunt-series amplifiers of this type are naturally broadband, and hence techniques which reduce the power consumption through *LC* tuning are not applicable [7].

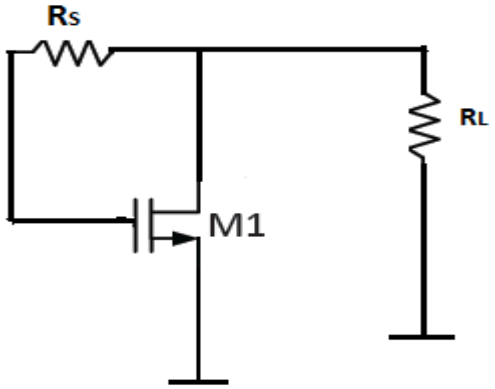

Figure 5.4: Resistive Shunt Series Feedback [7].

5.1.4 Inductive Source Degeneration

Ideal inductor contributes no internal noise. However, real inductors suffer from both internal and external noise [8]. Inductive source degeneration offers the best noise match among the all techniques discussed earlier.

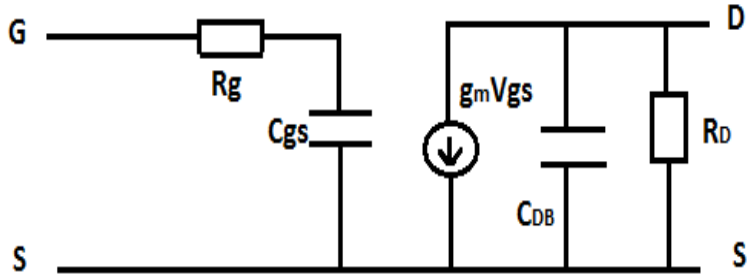

Figure 5.5: Equivalent Model of MOSFET.

Figure 5.5 shows the equivalent model of MOSFET consisting of voltage source in parallel with the load resistance R_D. As goal is to provide 50Ω proper termination but in reality the

input of the device is reactive, with real and capacitive impedance. Capacitive reactance can be removed by adding inductive feedback to the source.

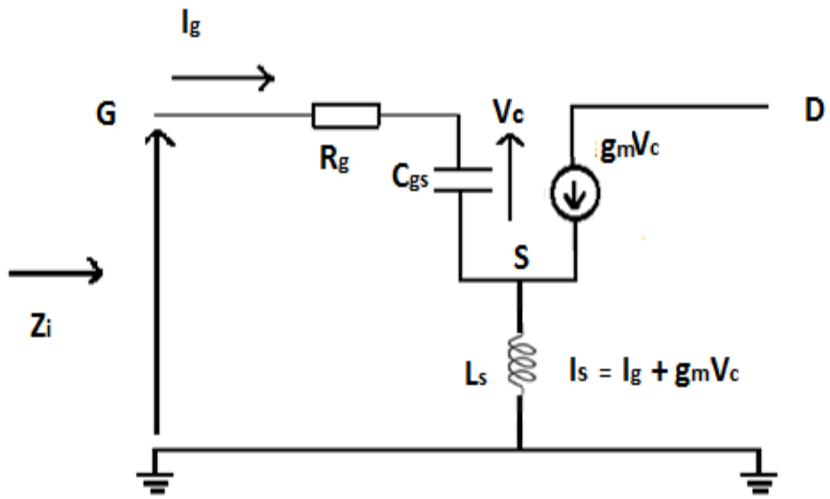

Figure 5.6: Equivalent MOSFET Model with Inductive Source Degeneration.

Calculating input impedance from figure 5.6 by applying KVL at input, it comes out to be

$$Zi = R_a + Rg + j\,(X_{Ls} - X_{cgs}) \tag{5.11}$$

In equation (5.11), $R_a = \frac{L_s g_m}{C_{gs}}$

From equation (5.11), it can be observed that by adding series feedback, $R_a + jX_{L_s}$ term is added to original input impedance. Additionally, another inductor is added in series with the gate L_g that is selected to resonate with the C_{gs}. L_g is designed so that at resonant frequency it cancels out C_{gs} that is

$$j\,(X_{L_s} - X_{C_{gs}}) = 0 \text{ such that } Zi = \frac{L_s g_m}{C_{gs}} = 50\Omega \tag{5.12}$$

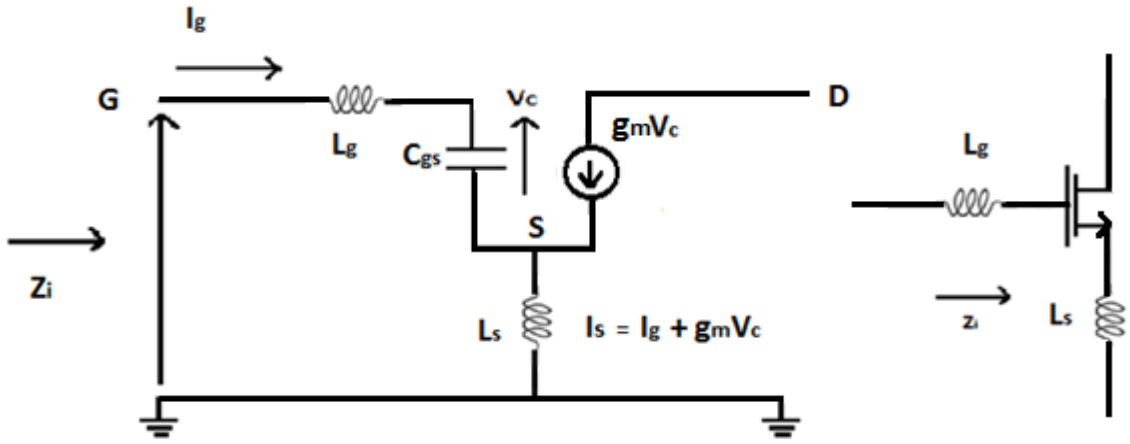

Figure 5.7: MOSFET Model with Inductive Gate and Inductive Source Degeneration.

5.1.5 Input and Output Matching Parameters (S11 and S22)

S11 and S22 define matching parameters and their value is equal to reflection coefficient.

As,

$$S11 = \text{Input Reflection Coefficient} = \frac{Z_{in} - Z_s}{Z_{in} + Z_s} \tag{5.13}$$

Since

$$Z_{in} = 1 + s^2 C_{gs}(L_G + L_s) \tag{5.14}$$

also the source impedance of the MOSFET is equal to

$$Z_s = sR_S C_{gs} \tag{5.15}$$

At resonance,

$$\omega^2 = \frac{1}{(L_G + L_S)C_{gs}} \tag{5.16}$$

Putting equations (5.14, 5.15 and 5.16) in equation 5.13 gives

$$S11 = 0dB \text{ (at resonance)} \tag{5.17}$$

Hence optimum value of S11 and S22 is less than equal to zero.

5.2 Classical Two Port Noise Theory

With the help of classical two port noise theory noise models is develop that simplify the noise analysis and lead to the acquisition of useful design insight.

Noise Factor

Noise factor is a measure of the degradation in signal-to-noise- ratio that a system introduces. The larger the degradation, the larger the noise factor.

$$F = \frac{Total\ output\ noise\ power}{Output\ noise\ due\ to\ input\ source} \tag{5.18}$$

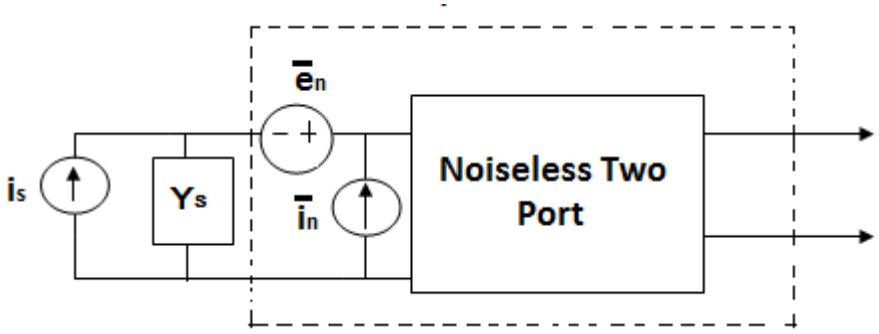

Figure 5.8: Equivalent noise model [4].

From figure 5.8 the noise factor for the noiseless two port in which all the noise has been referred to the input is given by:-

$$F = \frac{\overline{i_s^2} + \overline{|i_n + Y_s e_n|^2}}{i_s^2} \tag{5.19}$$

where, i_n and e_n is the noise generate from two port,

i_s is the noise generated from the source

In equation (5.19), the noise of the source is uncorrelated with the two equivalent noise generators of equivalent noise generator of two port also the noise of two port generators is uncorrelated with each other.

Noise Factor by accommodating the correlation between, i_n and e_n is given by:

$$F = 1 + \frac{\overline{i_u^2} + |Y_c + Y_s|^2 \overline{e_n^2}}{i_s^2} \tag{5.20}$$

In equation (5.20), i_u is uncorrelated current,

Y_C is correlation admittance,

Y_s is source admittance.

Equation (5.20), contains three independent noise sources, each of which may be treated as thermal noise produced by an equivalent resistance or conductance.

$$R_n = \frac{\overline{e_n^2}}{4kT\Delta f} \tag{5.21}$$

$$G_u = \frac{\overline{i_u^2}}{4kT\Delta f} \tag{5.22}$$

$$G_s = \frac{\overline{i_s^2}}{4kT\Delta f} \tag{5.23}$$

Using above equivalencies, the expression for noise factor can be written purely in terms of impedances and admittances:-

$$F = 1 + \frac{G_u + \left[(G_c + G_s)^2 + (B_c + B_s)^2\right] R_n}{G_s} \tag{5.24}$$

In equation (5.24), G_u is uncorrelated admittance,

G_c , is correlated admittance,

G_s is source conductance,

R_n is thermal noise conductance,

B_c is correlated suspectance,

B_s is source supectance.

From equation (5.24), two-port's noise has been characterised into four noise parameters, $(G_c\ , B_c\ , R_n\ and\ G_u)$ and goal is to minimize these parameters. Taking the first derivative with respect to the source admittance and setting it equal to zero yields

$$B_s = -B_c = B_{opt} \tag{5.25}$$

$$G_s = \sqrt{\frac{G_u}{R_n} + G_c^2} = G_{opt} \tag{5.26}$$

Hence to minimize the noise figure the source suspectance should be made equal to the inverse of the correlation suspectance, while the source conductance should be set equal to the value in equation (5.26).

The noise factor corresponding to this choice is given by:-

$$F_{min} = 1 + 2R_n\left[G_{opt} + G_c\right] = 1 + 2R_n\left[\sqrt{\frac{G_u}{R_n} + G_c^2} + G_c\right] \tag{5.27}$$

5.3 Derivation of Intrinsic MOSFET Two-Port Noise Parameters

Four noise parameters,$(G_c, B_c, R_n \text{ and } G_u)$ has to minimize in order to minimize the noise figure. MOSFET noise model consists of mainly two sources.

The mean-square drain current noise is

$$\overline{\imath_{nd}^2} = 4kT\gamma g_{d0}\Delta f \tag{5.28}$$

The mean-square gate current noise is

$$\overline{\imath_{ng}^2} = 4kT\gamma g_g\Delta f \tag{5.29}$$

Correlation coefficient that correlates the gate noise and drain noise with each other is defined formally as

$$c = \frac{\overline{\imath_{ng}\,\imath_{nd}}}{\sqrt{\overline{\imath_{ng}^2}}\sqrt{\overline{\imath_{nd}^2}}} \tag{5.30}$$

Using equation (5.21) first noise parameter R_n is given by

$$R_n = \frac{\overline{e_n^2}}{4kT\Delta f} = \frac{\gamma g_{d0}}{g_m^2} \tag{5.31}$$

where $\overline{e_n^2}$ is equivalent input noise voltage.

The correlation admittance that correlates the two equivalent noise generators of the two port is given by

$$Y_c = \frac{i_{n1}+i_{ngc}}{e_n} = j\omega C_{gs} + g_m\frac{i_{ngc}}{i_{nd}} \tag{5.32}$$

where $i_{n1} \text{ and } i_{ngc}$ are correlated gate and drain currents, C_{gs} is gate to source capacitance.

Solving equation (5.32) correlation admittance is given by [4],

$$Y_c = j\omega C_{gs}\left(1 - \alpha|c|\sqrt{\frac{\delta}{5\gamma}}\right) \tag{5.33}$$

From equation (5.33),

$$G_c = 0 \tag{5.34}$$

and

$$B_c = j\omega C_{gs}\left(1 - \alpha|c|\sqrt{\frac{\delta}{5\gamma}}\right) \tag{5.35}$$

Finally last noise parameter G_u (uncorrelated gate conductance) is given by

$$G_u = \frac{\delta\omega^2 C_{gs}^2(1-|c|^2)}{5g_{do}} \tag{5.36}$$

Putting equations (5.31, 5.34, 5.35, and 5.36) into equation (5.27) gives the minimum noise figure for MOSFET model.

$$F_{min} = 1 + \frac{2}{\sqrt{5}}\frac{\omega}{\omega_t}\sqrt{\gamma\delta(1-|c|^2)} \tag{5.37}$$

5.4 Power Constrained Noise Optimization

Device size can be calculated by taking power into constraint and that can be used to reformulate the noise figure calculated in equation (5.37).

Optimum Device size [4] calculated by taking power into constraint is given by

$$W_{optp} = \frac{3}{2}\frac{1}{\omega L C_{ox} R_s Q_{sp}} \approx \frac{1}{3\omega L C_{ox} R_s} \tag{5.38}$$

where, Q_{sp} is optimal source quality factor and is given by

$$Q_{sp} = |c|\sqrt{\frac{5\gamma}{\delta}}\left[1 + \sqrt{1 + \frac{3}{|c|^2}\left(1 + \frac{\delta}{5\gamma}\right)}\right] \approx 4 \tag{5.39}$$

With a device of width obtained in equation5.38 the noise figure obtained within the power constraint is given by [4]

$$F_{minp} = 1 + 2.4\frac{\gamma}{\alpha}\left[\frac{\omega}{\omega_t}\right] \tag{5.40}$$

5.5 Cascode Low Noise Amplifier with Inductive Load

Miller Effect

An important phenomenon that occurs in many analog circuits is related to "Miller Effect". It states that figure 5.9 for any impedance can be converted to figure 5.10 provided that the impedance Z appears in parallel with the main signal.

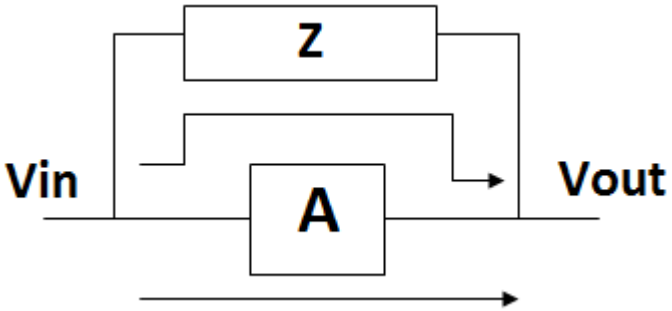

Figure 5.9: Typical Case for Miller's Theorem [26].

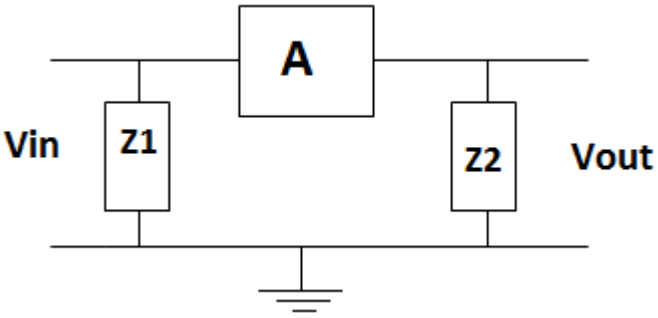

Figure 5.10: Application of Miller Theorem [26].

In figure 5.10

$$Z1 = \frac{Z}{1-A} \tag{5.41}$$

and

$$Z2 = \frac{Z}{1-A^{-1}} \tag{5.42}$$

equation Z1 and Z2 can be resistive, capacitive or inductive and produces undesired results. For example if Z is capacitive in nature then at high frequencies it will limit the frequency response both at the input and output. So, some means should be provided in order to suppress the miller effect.

Cascode Configuration

Cascode refers to the combination of common source and common gate. Main purpose of using the cascode configuration is to suppress the miller effect at the output and to increase the gain by increasing the output impedance of the circuit.

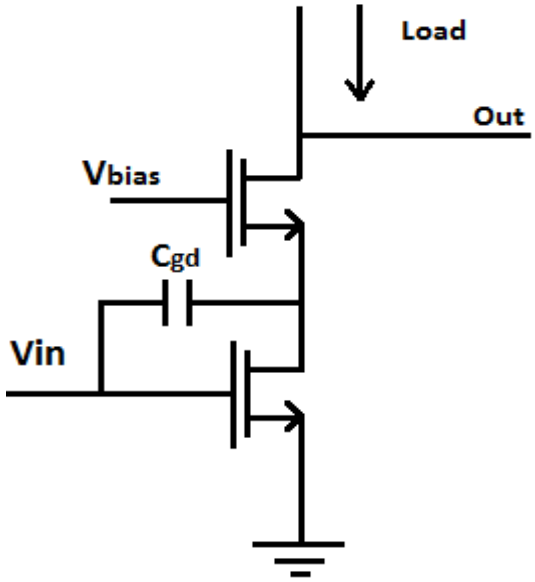

Figure 5.11: Cascode Configuration.

From the figure 5.11 it is clear that the effect of miller capacitance C_{gd} has been suppressed at the output.

Inductive Load

Instead of using resistive load inductive load is used for design of the low noise amplifier because of following advantages: -

- The inductor between the cascode source and supply blocks any RF leaking to the supply rail and maybe varied in value to optimize the gain response of the LNA.
- To tune out the capacitances producing at the output, thereby providing bandpass filtering.
- Compare to resistive load inductive load produces less noise.

5.6 Inductor Used for Design of Low Noise Amplifier

Inductors can be classified into two types:-

***Active Inductors*:** The one that can be realized through circuits like gyrators, opamp based oscillators *etc.* Active inductors cannot be used at RF frequencies because of following disadvantages:

- High noise
- Consumes more power
- Produces more distortion

***Passive Inductors*: -** These inductors are used for RF applications. They are further classified into two types:

- Bond wire Inductors: They are avoided for RF applications because they suffer from process variations.
- Spiral Inductors: These are formed by forming the spirals of metal forming a bunch of transmission lines.

Spiral Inductors

Spiral inductors are mostly used in RF applications because they are very area intensive and suffer lees from process variations as compare to bond wire inductors.

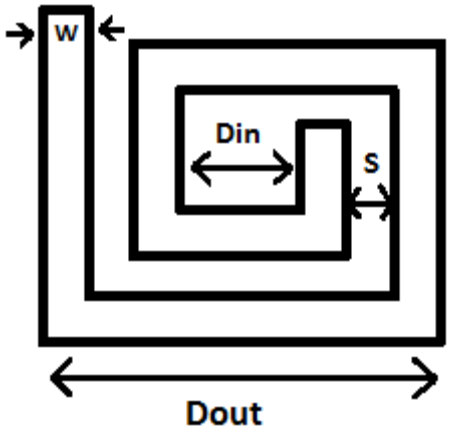

Figure 5.12: Square Spiral Inductors.

In figure 5.12, Dout is the outer diameter,

Din is the inner diameter,

W is width of the metal wire, and S is spacing between the two turns.

All these parameters Dout, Din, W, S forms the figure of merit for inductors. Also inductance of any inductor mainly depends upon core area, number of turns and mutual effects.

Mutual Effects

In figure 5.13 region A corresponds to the positive mutual effects while region B corresponds to negative mutual effects region because of reverse of direction.

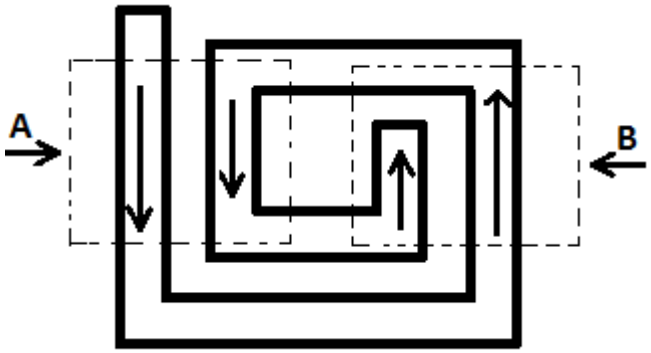

Figure 5.13: Square Spiral Inductors Considering Mutual Effects.

Since our goal is to maximize the inductance value so we have to minimize the negative mutual effects. Negative mutual effects can be reduced by using the hollow inductors by increasing the inner diameter Din. Further the inductance value can be increased by reducing spacing between the turns that increases number of turns as well as mutual effects.

Using uniform Current Density Inductors

In figure 5.14 region C refers to high current density point it produces crowding effects.

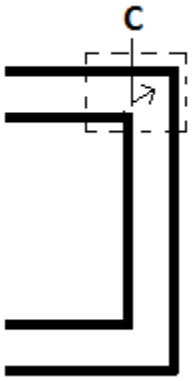

Figure 5.14: Crowding effects in Spiral Inductors.

So instead of using square inductors either circular or hexagonal spiral inductor is preferred so that uniform distribution of current is all where in inductors.

5.7 Complete Schematic of Single Ended Low Noise Amplifier

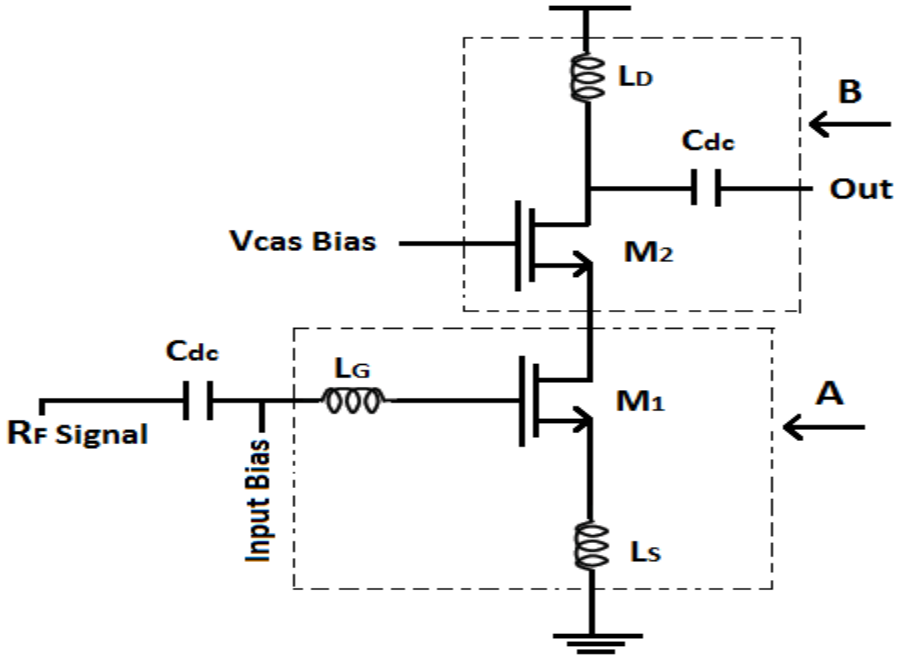

Figure 5.15: Single Ended LNA.

In figure 5.15,

B region corresponds to output matching network,

A region corresponds to input matching network,

C_{dc} are dc blocking capacitors

M1, M2 together made cascode configuration.

Input bias is decided in such a way that it meets all the requirements for example its minimum value should be such that all the transistors are in saturation. Secondly the power consumed by the low noise amplifier also depends upon the bias value.

Small Signal Gain

Drawing small signal model of the single ended low noise amplifier drawn in figure 5.16 (ignoring body bias effect and parasitic capacitances)

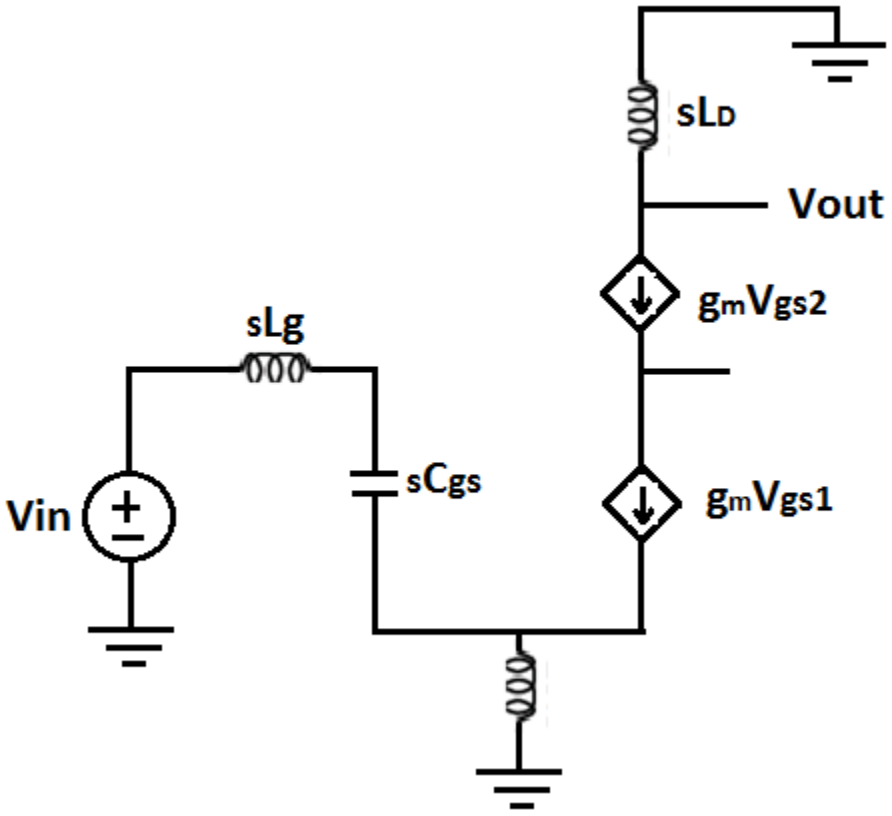

Figure 5.16: Small Signal Model of Single Ended LNA

gives small signal gain as

$$\frac{V_{out}}{V_{in}} = -\frac{L_D}{L_s} \tag{5.43}$$

Hence, from equation (5.43) it is observed that, if we want to increase the small signal gain value of L_D should be large as compare to L_s.

5.8 Differential Low Noise Amplifier

Since in differential configuration only even order nonlinearities cancels while the odd order nonlinearities of the two transistors gets added and most of designers are concerned with the odd-order nonlinearities that generates IM3 distortion, there is no benefit of using the differential LNA's over their single-ended counterparts also we will have to bias the diff pair at the same I_{dc} to get the same IM3 distortion as that of a common-source stage. So, why to use differential topology for LNA's. The reasons for going to differential circuits are many

and most relate to IC implementations. Typical IC mixers have differential inputs, so we must do that conversion somewhere. NF may be worse but compared to what? Looking at the losses in front of the LNA (filters, duplexers, switches, components, *etc.*) and we find the LNA is not the biggest contributor. The most compelling reason though is elimination of common mode effects. The differential LNA gain is not impacted by large common-mode impedances to ground. Ideally there is no RF feedback across common-ground ties. This enhances stability. Not all antennas are single-ended. Another reason for using differential stages in receivers is that bond wire and pins have values in the order of a few nH. In differential circuits the current flowing through the LNA remains constant. This implies less drop across the bondwire over the differential case. In the single ended LNA would not have a constant current consumption with respect to time thus generate an AC induced voltage drop across the bondwire on the ground and VCC pins. Common mode and substrate noise injection effects are vastly reduced in differential pairs over single ended types. Single-ended circuits have no immunity to these effects, mixed signal chips are especially prone to this effect due to digital and baseband functions combine with RF circuits.

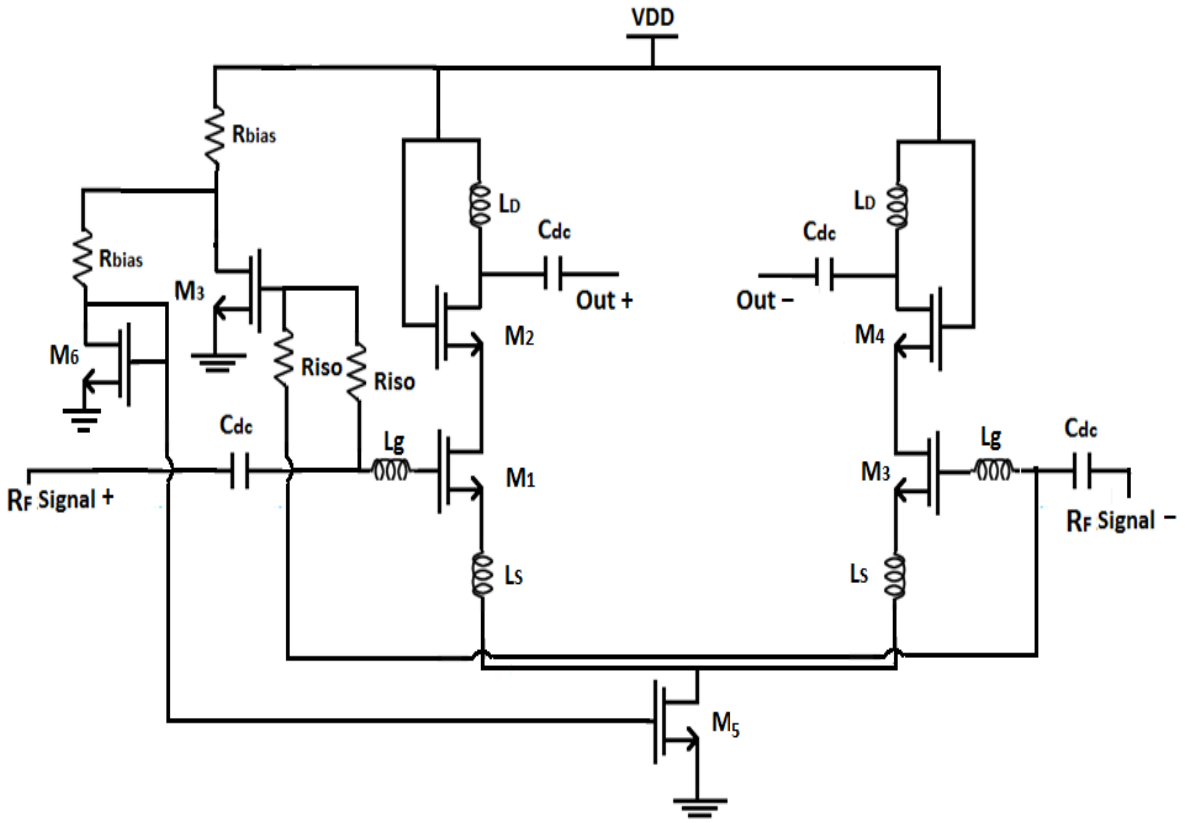

Figure 5.17: Differential LNA.

5.9 Components Value for Single Ended Low Noise Amplifier

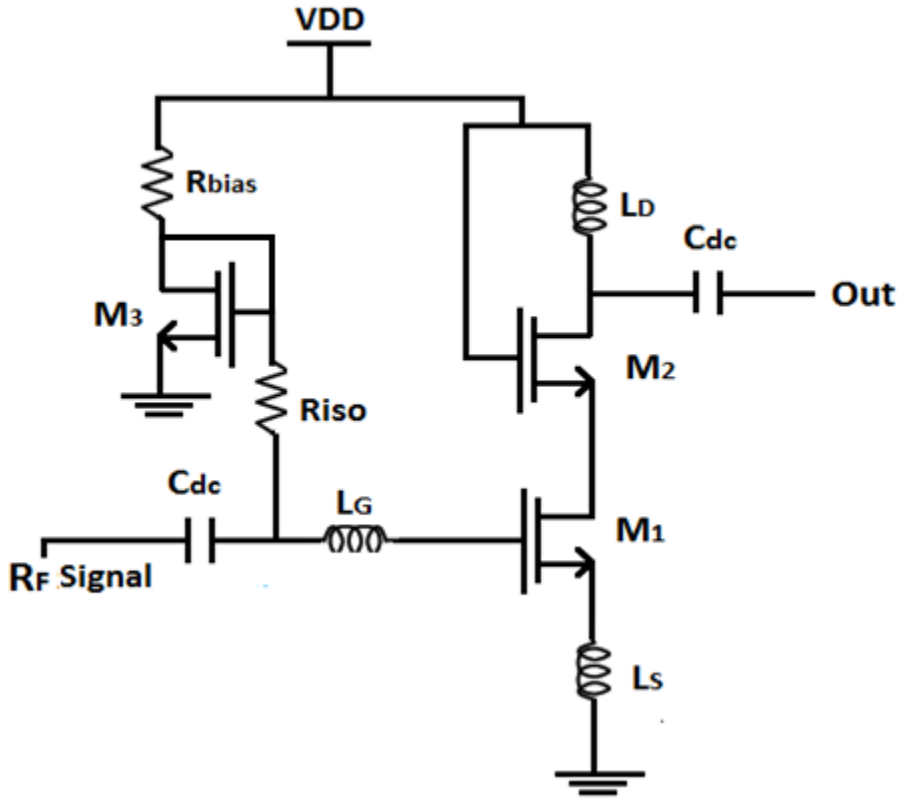

Figure 5.18: Single Ended LNA with Current Mirror [4].

Width of M1, M2 and M3

The low noise amplifier is to operated in WCDMA reception range ($2.11 - 2.17$ GHz) having centre frequency 2.14 GHz.

So resonant frequency, ω is equal to 2.14 GHz. Width of the transistor M1 is calculated by using the expression calculated in the equation (5.38)

$$W_{optp} = \frac{3}{2}\frac{1}{\omega L C_{ox} R_S Q_{sp}} \tag{5.44}$$

Since, $\omega = 2.14\text{GHz}$

$R_s =$ Source resistance = 50Ω for RF system

$L =$180nm for 0.18μm CMOS technology

$C_{0x} = 8.37 \times 10^{-3}$F (from BSIM3V2 RF model file)

$Q_{sp} =$3.5

Putting these values in equation (5.44) gives

W (M1) = 370µm

Width of M2 is also kept equal to 370µm in order to get high gain and high output impedance. M3 MOSFET is used for biasing purposes microns of current flows through this transistor is equal to 25µm. Length for all transistors is equal to 180nm.

Biasing of M2

Gate terminal of cascoded MOSFET M2 is connected to the power supply so that we have negligible voltage headroom and we get maximum swing at the output.

Value of Inductor L_S

From equation 5.12, for proper matching

$$R_s = \frac{g_m L_s}{C_{gs1}} \tag{5.45}$$

$$g_m = \mu_n \times C_{ox} \times \frac{W}{L} \times V_{od}$$

$$g_m = 277 \times 10^{-6} \times \frac{370}{0.18} \times 0.12 \approx 0.065 mho \tag{5.46}$$

$$C_{gs1} = \frac{2}{3} \times C_{ox} \times W_1 \times L_1$$

$$C_{gs1} = \frac{2}{3} \times 8.37 \times 10^{-3} \times 370\mu \times 0.18\mu = 0.37pF \tag{5.47}$$

Putting values from equations (5.46 and 5.47) into equation (5.45) gives

$$L_s = 0.29nH$$

Considering effect of miller capacitance at the input

$$R_s = \frac{2\, w_t\, L_s}{1 + 2\frac{C_{gd}}{C_{gs}}} \tag{5.48}$$

Hence from equation (5.48) in order to reduce the effect of miller capacitance C_{gd} value of L_s has to increased, also increase in L_s reduces parasitic ground effects.

After iterations value of source inductance comes out to be

$$L_s = 0.585nH$$

Value of Inductor L_G

Inductor L_g along with L_s provides means of matching.

At resonant frequency,

$$\omega = \frac{1}{\sqrt{(L_g + L_s)C_{gs}}} \tag{5.49}$$

Putting values of $(L_s,\ C_{gs}\ \text{and}\ \omega)$ gives

$$L_G = 13.59nH$$

Value of Load Inductance L_D

Inductive load value depends upon mainly following factors: -

- It is used to tune out the parasitic capacitance appearing at the output providing band pass filtering. Hence, at resonant frequency

$$\omega = \frac{1}{\sqrt{L_D\ C_{out}}} \tag{5.50}$$

- Secondly gain of the system depends upon the ratio of load inductance to the source inductance. Hence to maximize gain value of L_D should be large.

For our specification the value of L_D at which the amplifier resonate at resonate frequency comes out to be

$$L_D = 5.38nH$$

Value of Biasing Resistor and Isolation Resistor

- Value of R_{bias} together with dimensions of MOSFET M3 determines the gate voltage of MOSFET M1.
- R_{iso} value is chosen large enough that its equivalent noise current is small enough to be ignored.

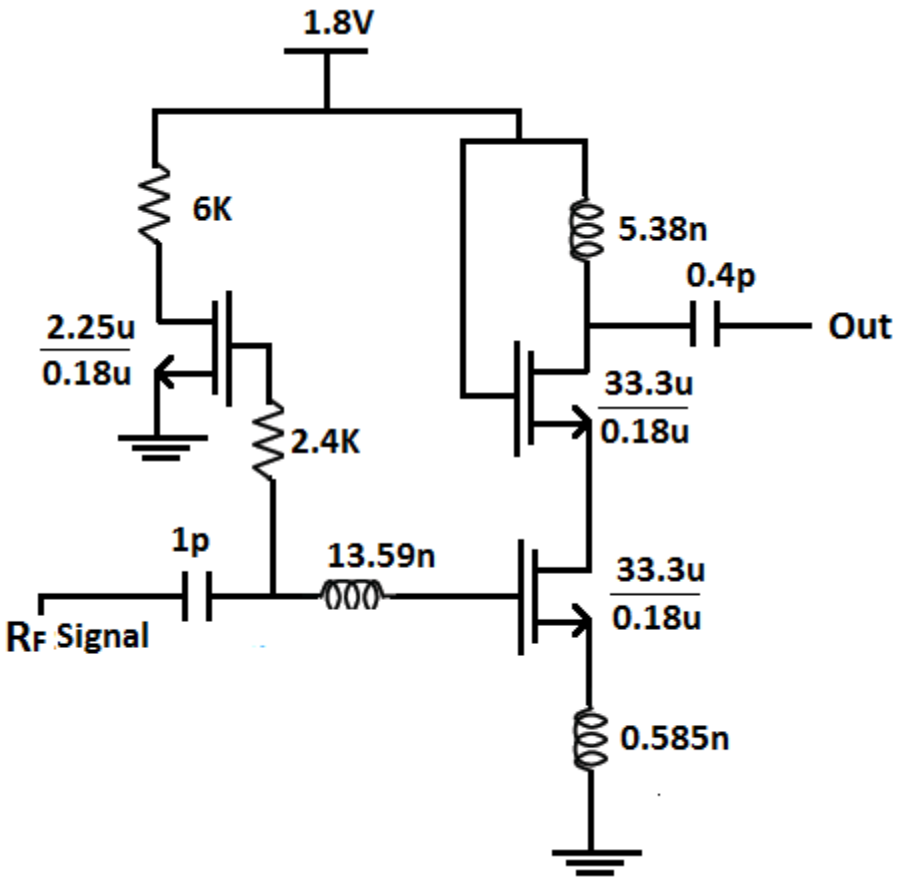

Figure 5.19: Single Ended LNA with Components Value.

5.10 Minimum Detectable Signal

Once the component values has been found next step is to find the maximum RF signal that can be detected. The smallest signal that can be received by a signal defines the receiver sensitivity and largest signal that can be detected by a receiver establishes the upper limit of what can be handled by the system while preserving the voice or data quality.

The dynamic range of the receiver is defined as the difference between the largest possible received signal and the smallest possible received signal that defines the quality of the receiver chain. The noise floor is given by [27]: -

$$P_{min} = kTB \tag{5.51}$$

where, k = Boltzman's Constant

T = Temperature

B = Bandwidth

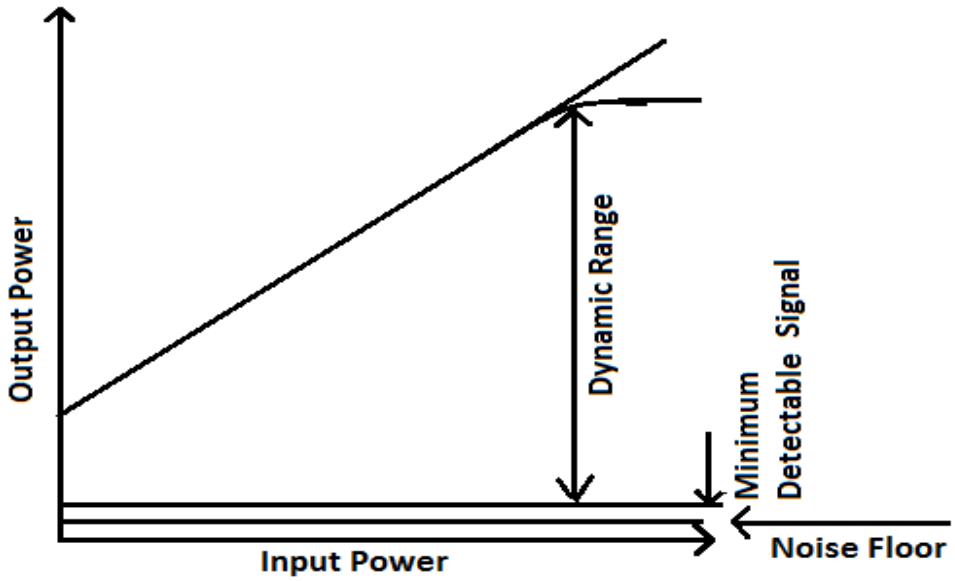

Figure 5.20: Dynamic Range Plot for low Noise amplifier [27].

Since WCDMA reception range is from (2.11GHz to 2.17GHz), so noise floor (P_{min}) for low noise amplifier after normalizing the result into dBm is given by:

$$\mathrm{P_{min}(dB_m)} = -96 \tag{5.52}$$

Hence from equation (5.52) it is observed that minimum signal that can be detected by the receiver has power of $-96dBm$.

5.11 Noise Figure

Figure 5.21 shows the equivalent noise model for source degeneration single ended LNA.

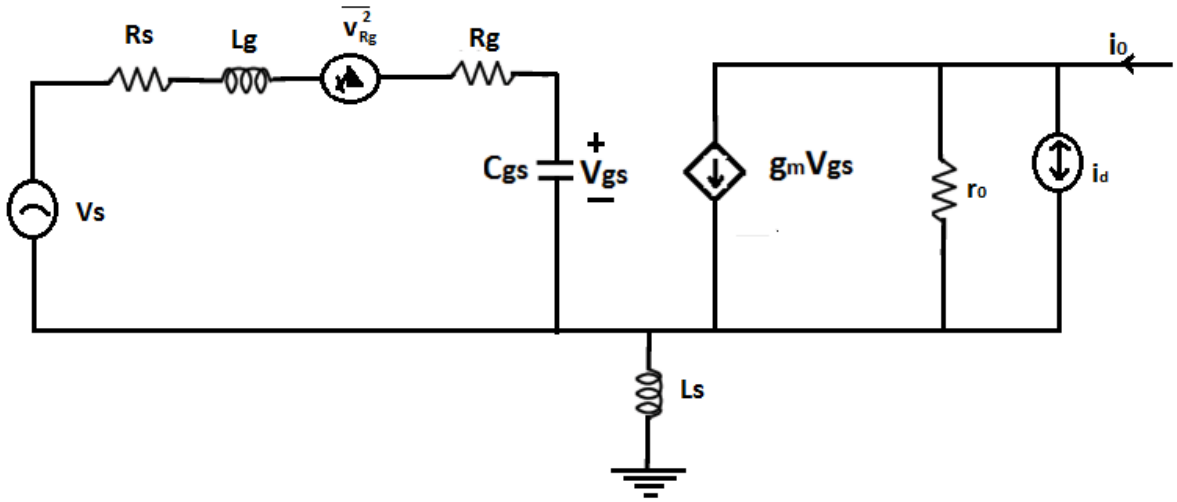

Figure 5.21: Small Signal Noise Model for Single Ended LNA.

Noise Figure [27], with source degeneration is given by:

$$F = 1 + \frac{R_g}{R_S} + \left(\frac{\gamma}{\alpha}\right) g_m R_s \left(\frac{\omega}{\omega_t}\right)^2 \quad (5.53)$$

which is similar as that of common source amplifier. Hence, inductive degeneration did not raise the noise. So the minimum noise figure is same. The main advantage of using source degeneration is that the input impedance is real and programmable ($\omega_t L_s$). Figure6.8 shows the graph for noise figure of single ended LNA.

5.12 Power Consumption of Inductive Source Degeneration

Power Consumption of Inductive Source Degeneration [27] is given by:

$$P = \frac{L^2}{\mu} \frac{R_S^2}{\omega^2} \frac{1}{L_S^3\left[1+\frac{L_G}{L_S}\right]} \quad (5.54)$$

Chapter 6

Simulation

6.1 Small Signal Analysis

Small Signal Analysis was done by SP analysis. Small signal gain S21, matching parameters (S11 and S22) and noise figure were plotted using this analysis.

Figure 6.1 shows the result for small signal gain S21 for single ended low noise amplifier.

Figure 6.2 shows the result for matching parameters (S11 amd S22) single ended low noise amplifier.

Figure 6.3 shows the result for noise figure for single ended low noise amplifier.

Also small signal analysis was done to plot the graphs for differential low noise amplifier.

Figure 6.8 shows the result for small signal gain S21 for differential low noise amplifier.

Figure 6.9 shows the result for matching parameters (S11 amd S22) differential low noise amplifier.

Figure 6.10 shows the result for noise figure for differential low noise amplifier.

Figure 6.13 shows the result for common mode gain for differential low noise amplifier.

6.2 Large Signal Analysis

PSS Analysis

PSS analysis was done to find out the maximum signal that the low noise amplifier can handle. It was observed that up to input power -25dBm large signal gain and noise figure remains under specifications limit. So -25dBm was chosen as input signal level.

Table 7: Large Signal Analysis

Input Power(dBm)	Voltage Gain(dB)	Noise Figure(dB)
-100	17.16	3.013
-80	17.15	3.031

Input Power(dBm)	Voltage Gain(dB)	Noise Figure(dB)
-60	17.15	3.031
-40	17.15	3.05
-30	17.31	3.223
-25	16.99	3.653
-20	15.66	4.94
-10	9.461	9.597

Figure 6.4 shows the large signal gain of single ended LNA for input−25dBm.

Figure 6.5 shows the noise figure (large signal) of single ended LNA for input −25dBm.

Figure 6.11 shows the large signal gain of differential LNA for input −25dBm.

Figure 6.12 shows the noise figure (large signal) of differential LNA for input−25dBm.

Also PSS analysis was done to plot the result for third order intercept point.

Figure 6.6 shows the result for third order intercept point for single ended low noise amplifier.

Figure 6.14 shows the result for third order intercept point for differential low noise amplifier.

Swept PSS Analysis

Swept PSS analysis was done to plot the graph for 1dB compression point by varying input power from -100dBm to 0dBm.

Figure 6.7 shows the result for 1dB compression point for single ended low noise amplifier.

Figure 6.15 shows the result for 1dB compression point for differential low noise amplifier.

6.3 DC Analysis

DC analysis was done to calculate the power consumed by the low noise amplifier.

Power consumed by single ended low noise amplifier was 7.353mW.

Power consumed by differential low noise amplifier was 8.738mW.

6.4 Corner Analysis

Corner simulation was performed for single ended LNA. There were 4 conditions that can be performed for the transistor's corner analysis, and these are the normal-N normal- P, weak-N strong-P, strong-N weak-P and lastly, weak-N weak-P. Only two transistor conditions were used for the corner simulations in this work, these are the SNSP (ff) and WNWP (ss) conditions. This selection was made due to the extreme conditions that these two can impose on the transistors and, consequently, providing the worst or best performance the transistor is capable of. The differences between SNSP and WNWP are in the channel length and width variations, threshold voltage, and junction capacitance and oxide thickness. Single ended LNA was simulated for following corner conditions:

a) Resistor maximum, capacitor minimum, transistor ss (both slow).
b) Resistor minimum, capacitor maximum, transistor ss (both slow).
c) Resistor maximum, capacitor maximum, transistor ss (both slow).
d) Resistor normal, capacitor normal, transistor ss (both slow).
e) Resistor minimum, capacitor maximum, transistor ff (both fast).
f) Resistor maximum, capacitor maximum, transistor ff (both fast).
g) Resistor normal, capacitor normal, transistor ff (both fast).
h) Resistor maximum, capacitor minimum, transistor ff (both slow).

Table 8: Corner Analysis for Single Ended LNA

Conditions	Parameters						Current Consump. (mA)
	Small Signal Analysis				Large Signal Analysis		
	S21(dB)	S11(dB)	S22(dB)	NF(dB)	S21(dB)	NF(dB)	
a)	15.92	-26.62	-13.568	3.194	15.95	4.382	3.384
b)	16.7	-25.96	-25.76	3.132	14.71	4.495	4.835
c)	16.69	-25.96	-25.76	2.057	14.71	4.495	3.384
d)	16.43	-29.47	-23.2	3.143	15.61	4.489	3.962
e)	18.17	-34.08	-29.03	2.815	17.52	3.312	4.835
f)	18.15	-34.08	-29.03	2.815	17.52	3.312	3.384
g)	17.81	-45.08	-19.56	2.842	17.702	3.247	3.962
h)	16.42	-16.5	-13.865	3.00	16.404	3.753	3.384

It is observed from the table 8 that, the lowest current consumption was when the resistors were at maximum values. The contributor to this effect is R_{bias} for having a maximum voltage drop across it under this condition and consequently resulting in minimum V_{DS} and V_{GS} for M3, minimum V_{GS} for M1 and resulting in minimum flow of current from cascode transistor M2. Also the maximum current consumption was when the resistors were at minimum values. The main contributor to this effect was again R_{bias} for having a minimum voltage drop across it under this condition and consequently resulting in maximum V_{DS} and V_{GS} for M3, maximum V_{GS} for M1 and resulting in maximum flow of current from cascode transistor M2.Components M1, M2, M3 and R_{bias} are shown in figure 5.19.

6.5 Graphs for Single Ended Low Noise Amplifier

Figure 6.1 shows the small signal gain of single ended low noise amplifier. Gain obtained by amplifier for WCDMA reception range $(2.11\ \text{GHz} - 2.17\ \text{GHz})$ was greater than 15dB and at centre frequency $\omega = 2.14\ \text{GHz}$ gain obtained was 17.14dB.

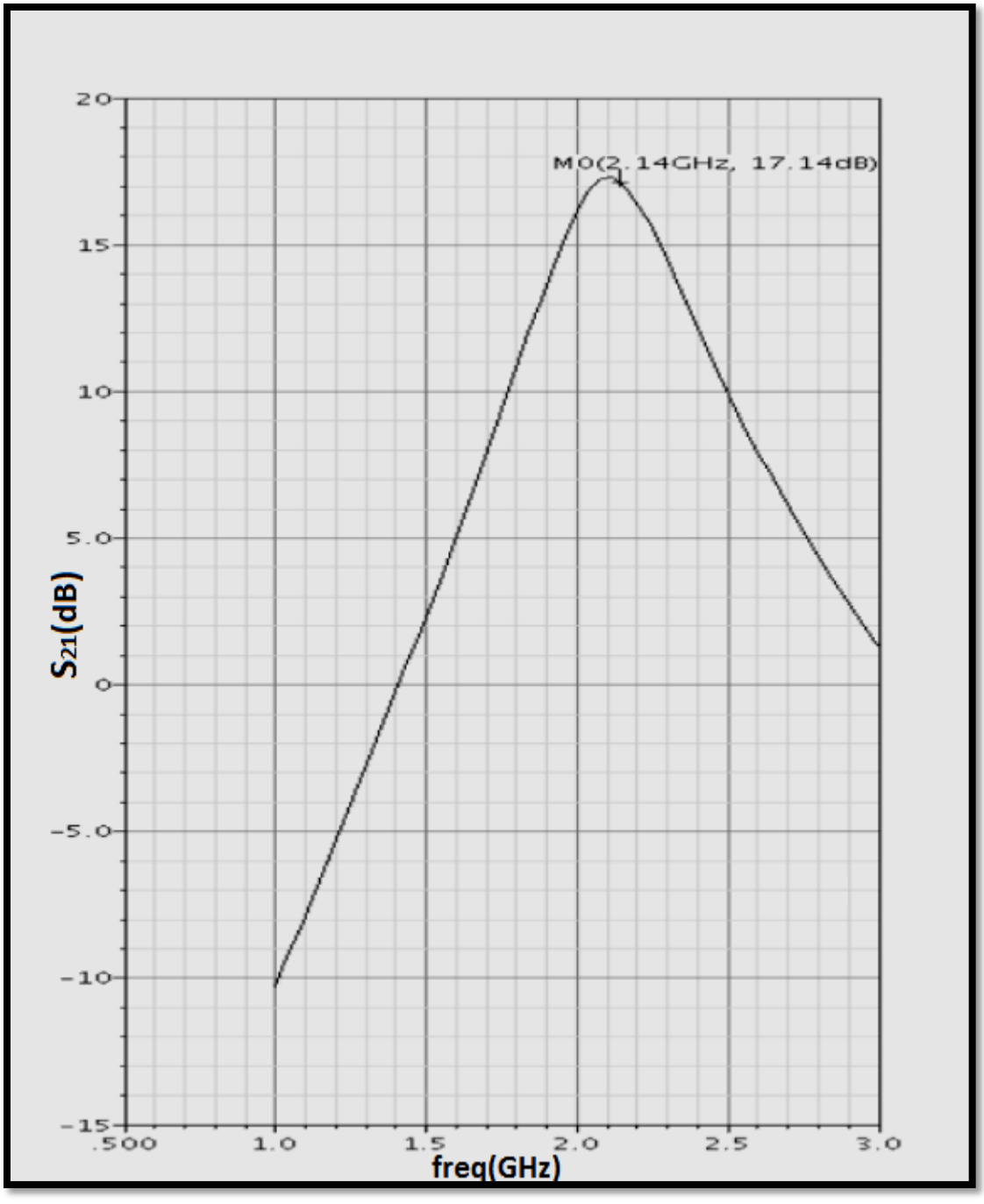

Figure 6.1: Small Signal Gain of Single Ended LNA.

Figure 6.2 shows the matching parameters (S11 and S22) of single ended low noise amplifier. As S11 and S22 represents the input and output reflection coefficient respectively, for proper their value of should be less than 0dB. For single ended LNA value obtained for $S11$ and S22 at centre frequency $\omega = 2.14$ GHz was -26.96dB and -18.17dB respectively.

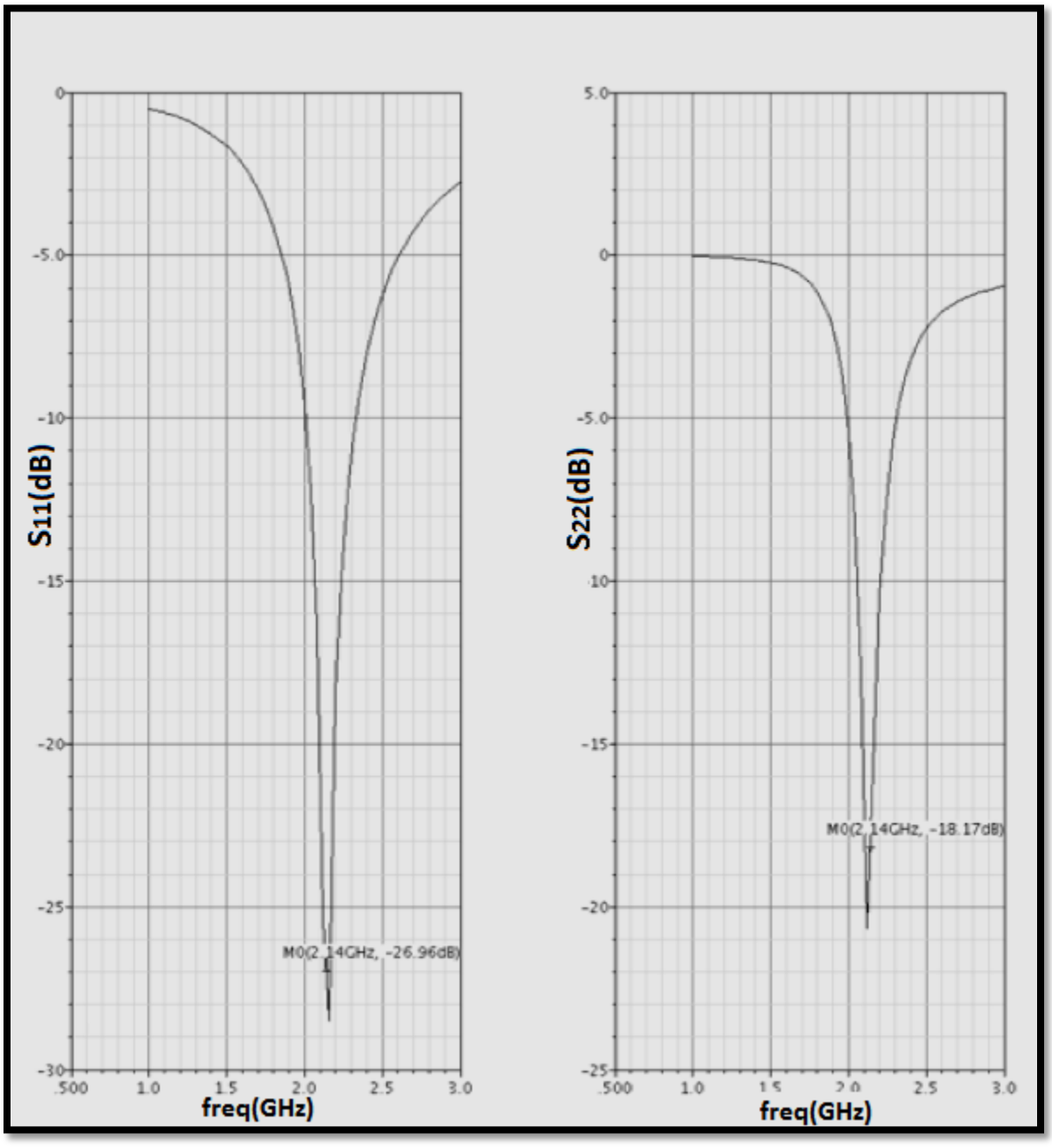

Figure 6.2: Input and Output Matching Curves for Single Ended LNA.

Figure 6.3 shows the graph for noise figure of single ended LNA. One of the main characteristic of amplifier is that it produces low noise. Noise figure obtained at centre frequency was 2.455dB (F_{min}) and 2.976dB (F_{tot}).

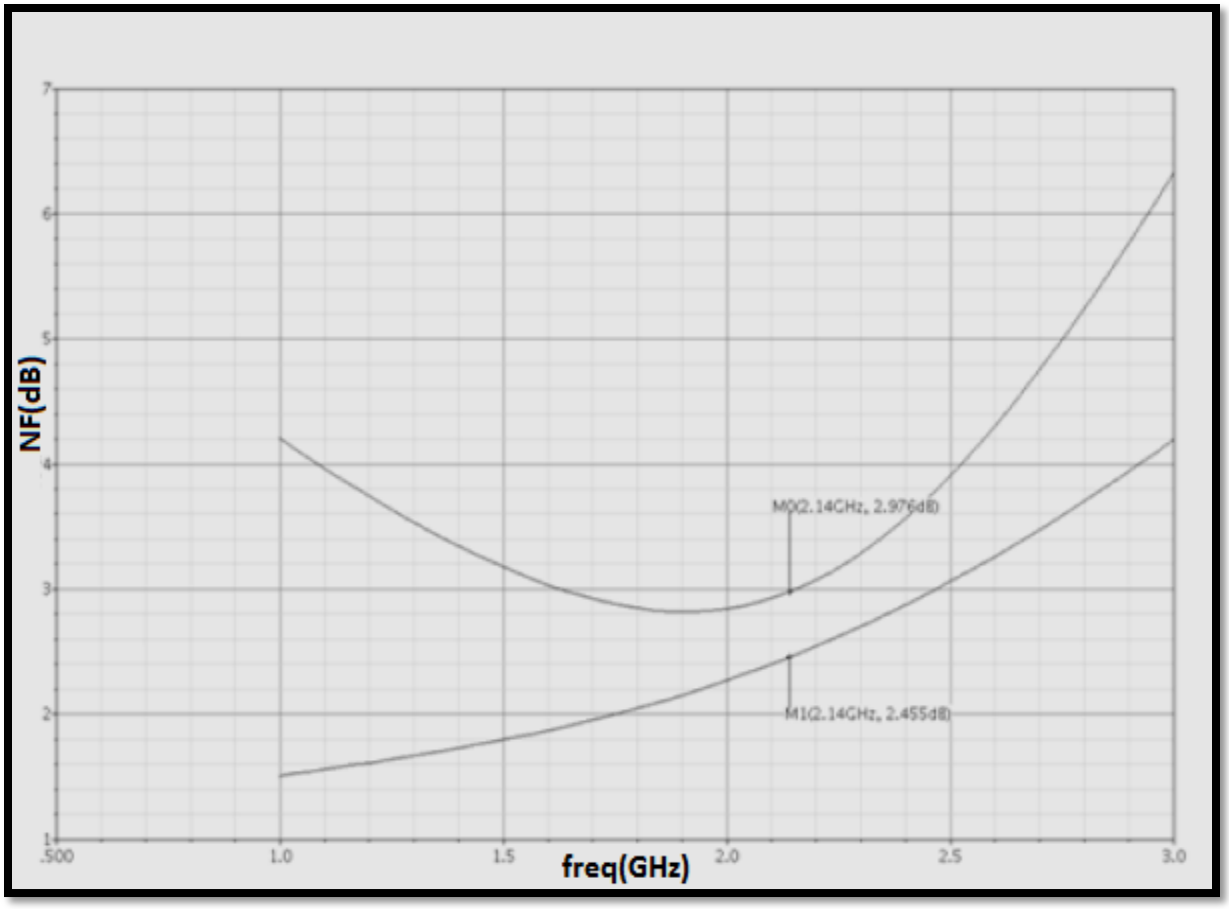

Figure 6.3: Noise Figure for Single Ended LNA (Small Signal).

Figure 6.4 and figure 6.5 shows the graphs for large signal gain and noise figure of single ended low noise amplifier. Large signal is defined as any signal that changes the operating point of circuit resulting in deterioration of the performance of any circuit. Single ended low noise amplifier simulated under large signal conditions produced 0.8% of error for gain and 18% for noise figure as compared to the values obtained under small signal conditions.

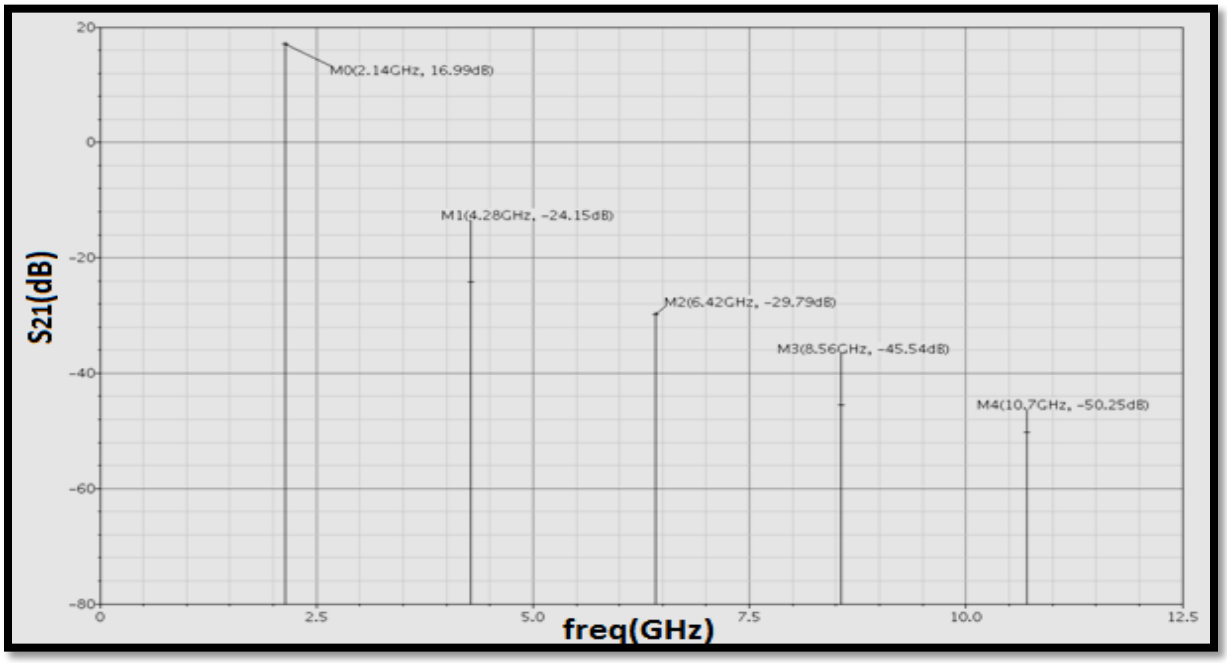

Figure 6.4: Large Signal Gain of Single Ended LNA.

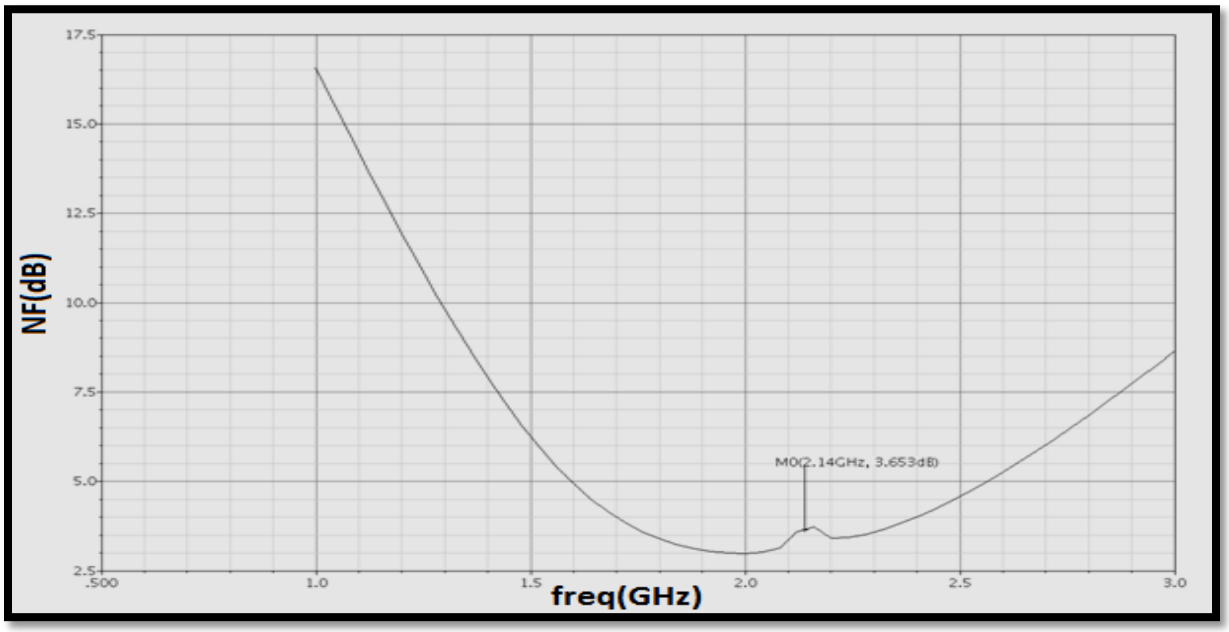

Figure 6.5: Noise Figure of Single Ended LNA (Large Signal).

Figure 6.6 shows the graph for third order intercept point of single ended LNA. Since the intermodulation products produced due to nonlinear behavior of circuit saturates the levels of the signal, the third order input intercept point (IIP3) should be high for linear response of amplifier. For single ended LNA the obtained value for IIP3 was -12dBm.

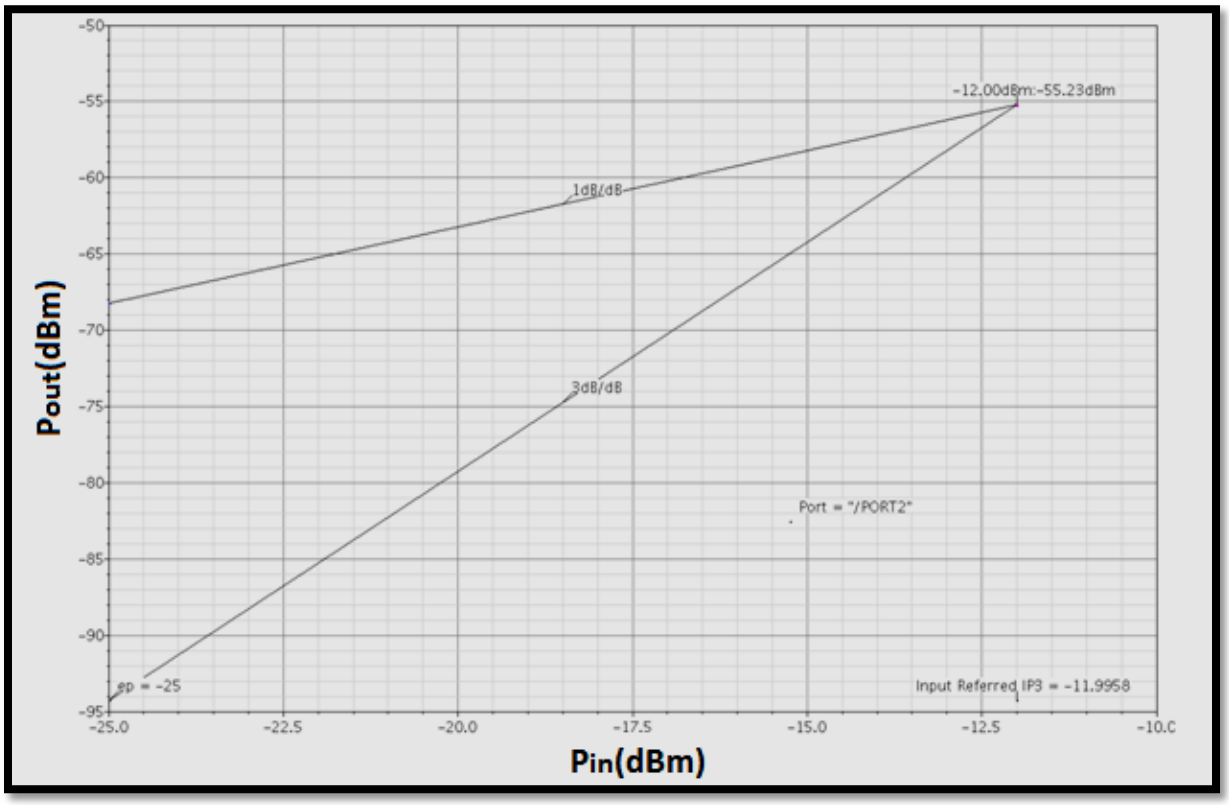

Figure 6.6: Third Order Intercept Point for Single Ended LNA.

Figure 6.7 shows the graph for 1dB compression point of single ended low noise amplifier. Value of input power/voltage where the gain of amplifier gets reduced by 1dB is called 1dB compression point. Reduction in gain occurs due to rise of harmonics that combines with fundamental signal and results in reduction of gain. Input referred 1dB compression point for single ended LNA obtained was -21.38dBm.

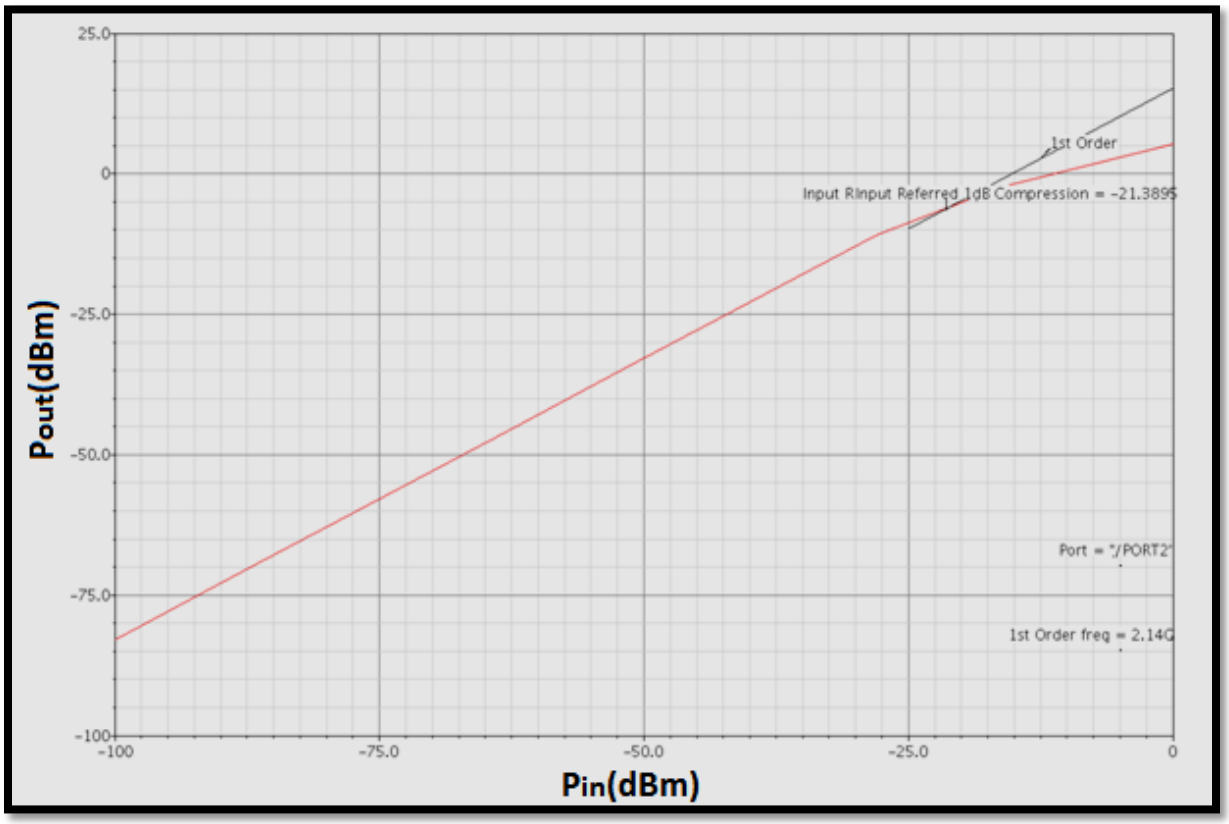

Figure 6.7: 1dB Compression Point for Single Ended LNA.

6.4 Graphs for Differential Low Noise Amplifier

Figure 6.8 shows the small signal gain of differential low noise amplifier. Gain obtained by amplifier for WCDMA reception range $(2.11\ \text{GHz} - 2.17\ \text{GHz})$ was greater than 14dB and at centre frequency $\omega = 2.14\ \text{GHz}$ gain was 15.19dB.

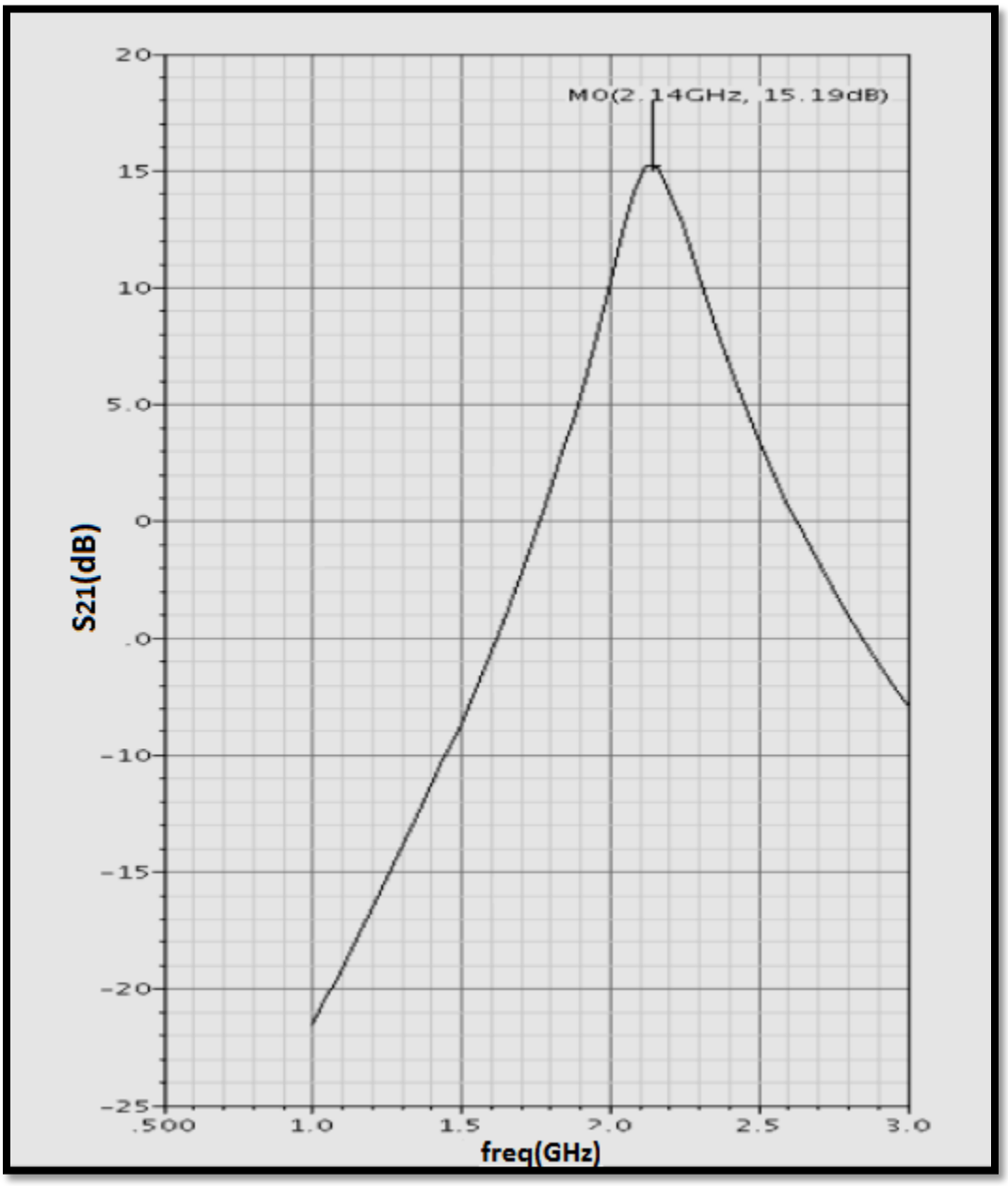

Figure 6.8: Small Signal Gain of Differential LNA.

Figure 6.9 shows the matching parameters (S11 and S22) of differential low noise amplifier. Value obtained for $S11$ and S22 at centre frequency $\omega = 2.14$ GHz was -17.47dB and -6.857dB respectively.

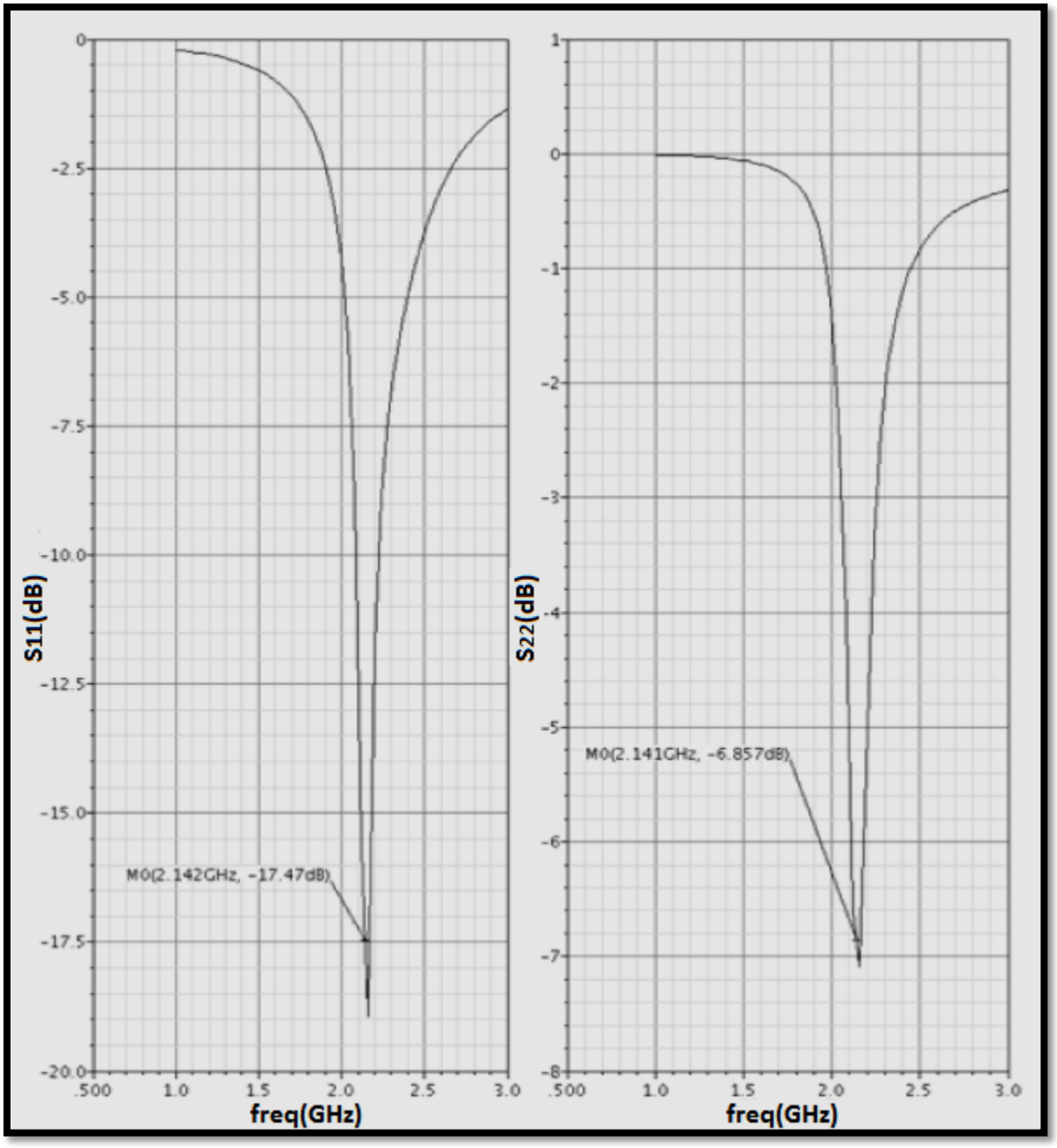

Figure 6.9: Input and Output Matching Curves for Differential LNA.

Figure 6.10 shows the graph for noise figure of differential LNA. Noise figure obtained at centre frequency was 2.523dB (F_{min}) and 4.038dB (F_{tot}) respectively. Differential configuration required more components as compare to single ended LNA for designing and that result in increase of circuit noise of former.

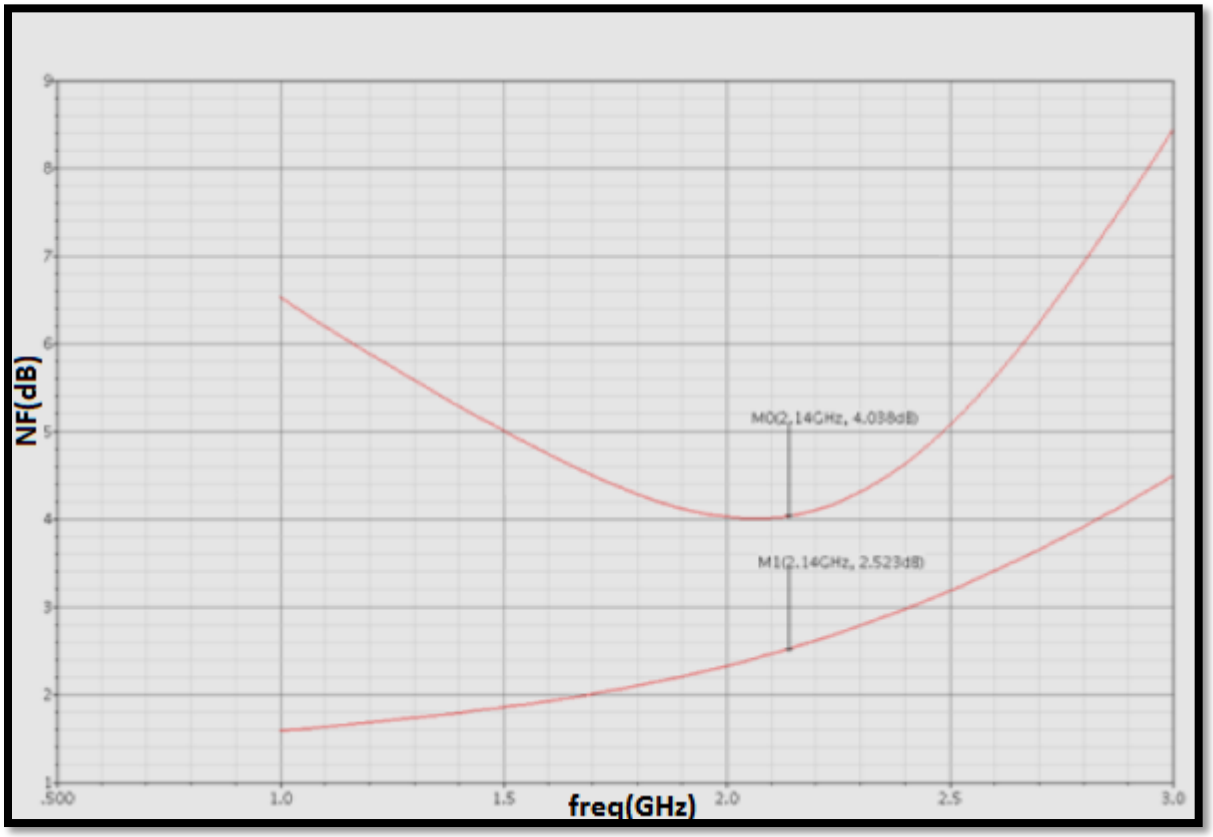

Figure 6.10: Noise Figure for Differential LNA (Small Signal).

Figure 6.11 and figure 6.12 shows the graphs for large signal gain and noise figure of differential amplifier. Differential amplifier simulated under large signal conditions produced 11% of error for gain and 19% for noise figure as compared to the values obtained under small signal conditions.

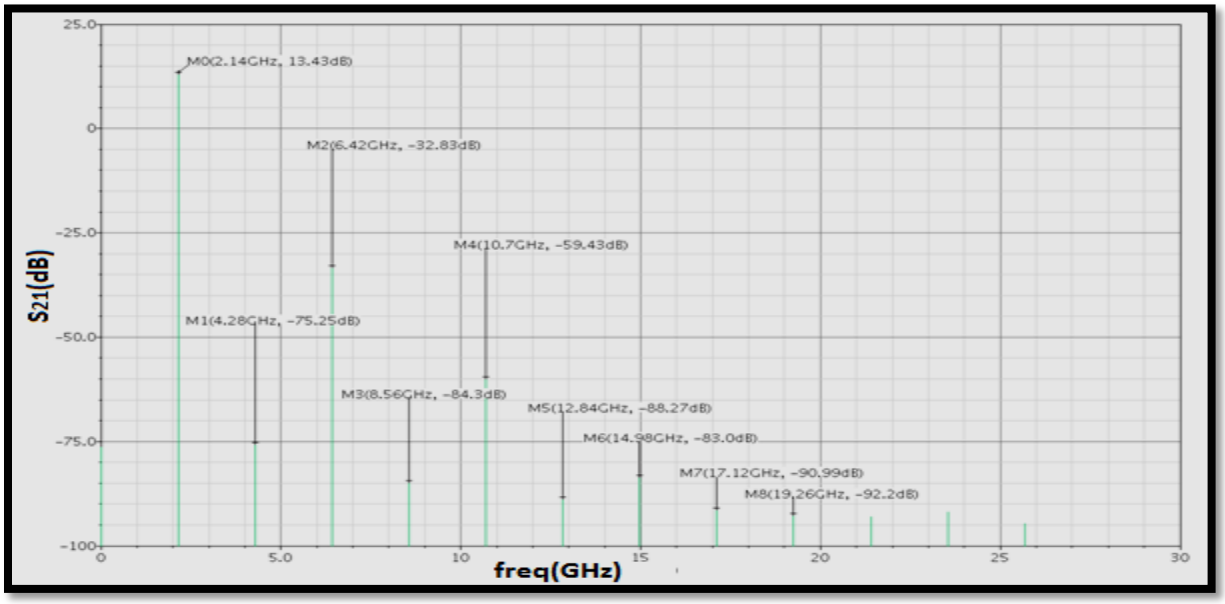

Figure 6.11: Large Signal Gain of Differential LNA.

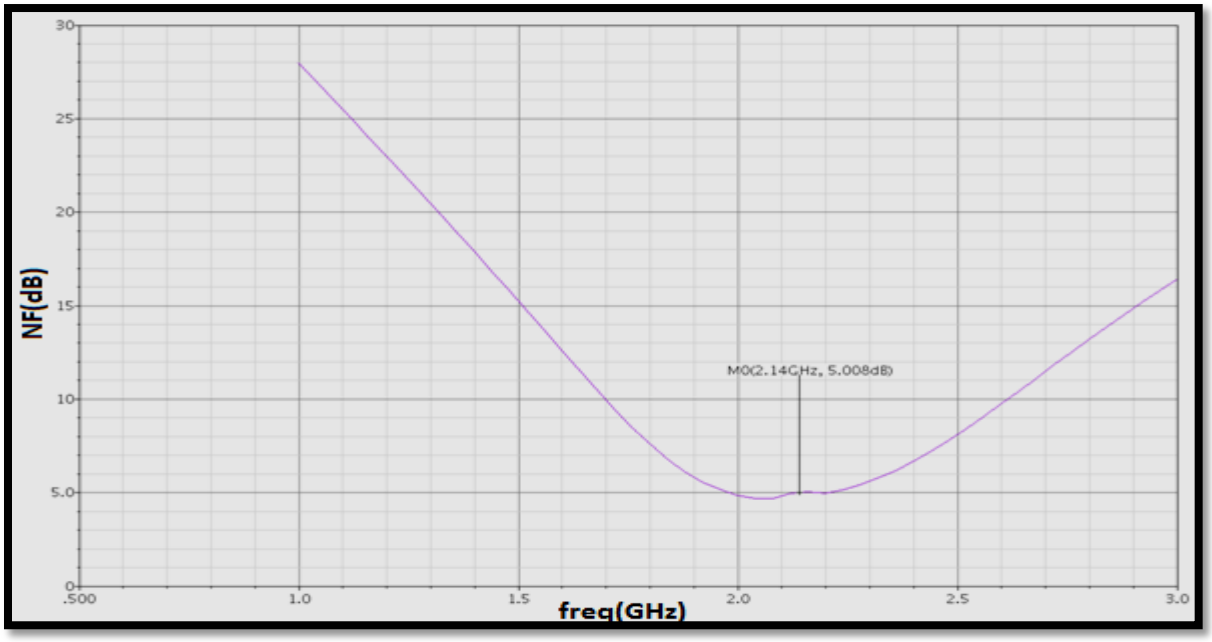

Figure 6.12: Noise Figure of Differential LNA (Large Signal).

Figure 6.13 shows the common mode gain of differential LNA. Main advantage of using differential configuration was common mode rejection. The common mode gain obtained at the centre frequency was -216.7dB.

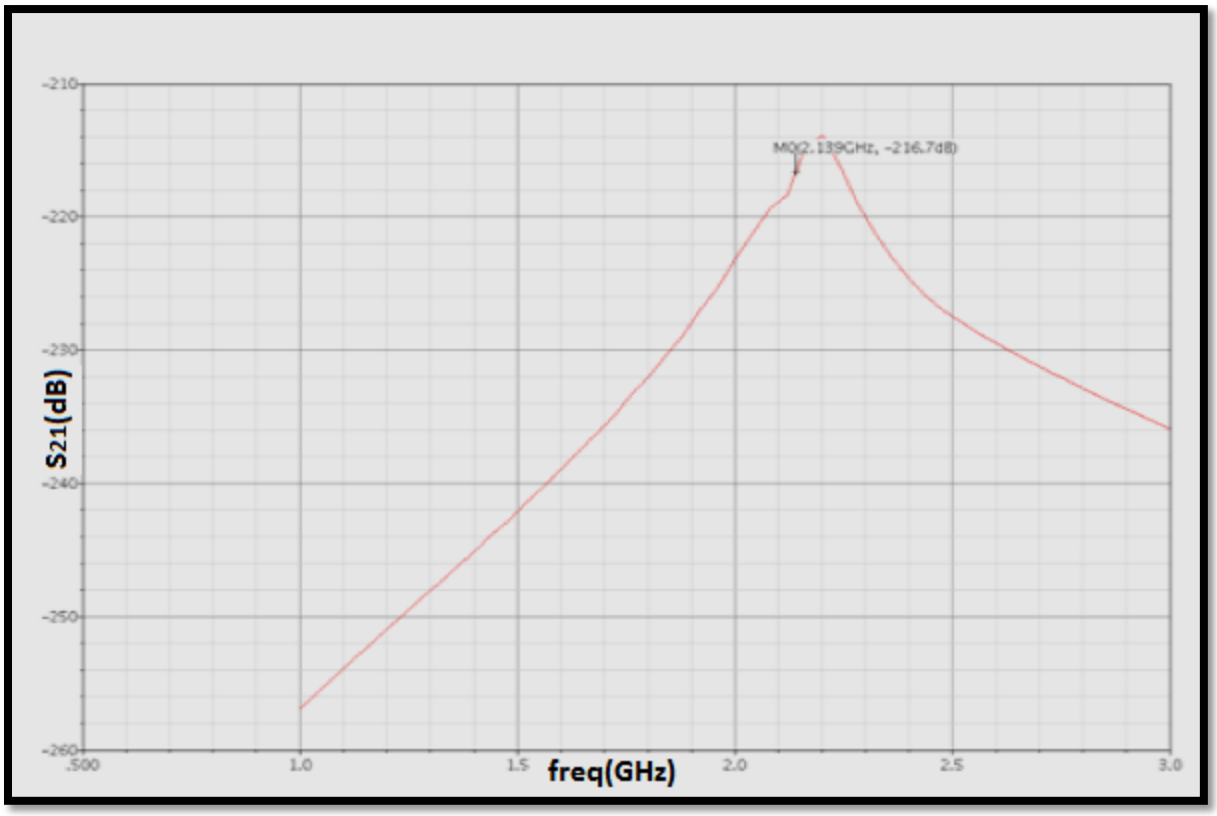

Figure 6.13: Common Mode Gain for Differential LNA (Small Signal).

Figure 6.14 shows the graph for third order intercept point of differential LNA. The obtained value for IIP3 was -12.98dBm.

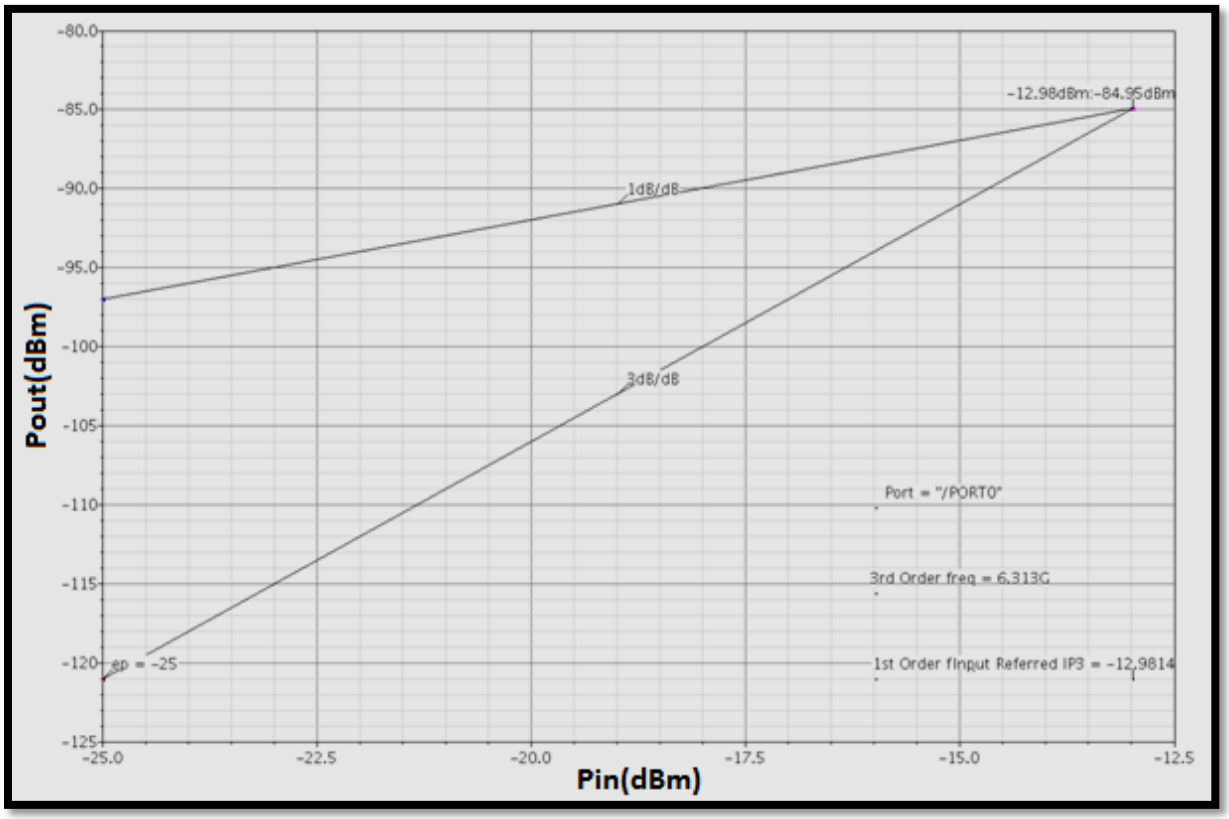

Figure 6.14: Third Order Intercept Point for Differential LNA.

Figure 6.15 shows the graph for 1dB compression point of differential low noise amplifier. Input referred 1dB compression point for differential LNA was -22.52dBm.

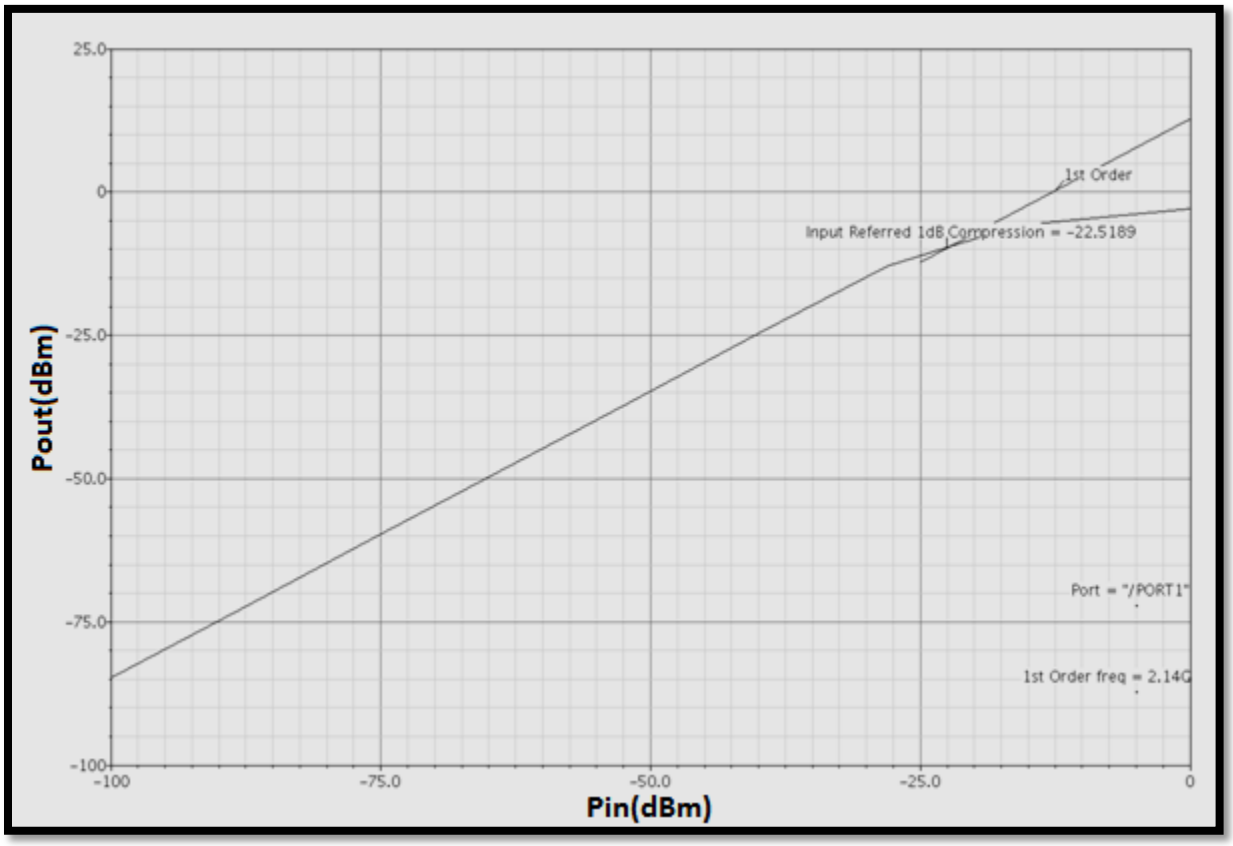

Figure 6.15: 1dB Compression Point for Differential LNA.

Chapter 7

Layout

With the LNA designed, the final step was the layout process. Layout is an important step in RFIC design for several reasons. Layout determines actual the physical area that the LNA will occupy which is important as there are chip size specifications for wireless LAN transceivers. More importantly, the physical layout of the LNA will have a direct impact on its actual performance. The performance is affected as the physical layout introduces parasitics, coupling, matching as an issue and many other factors noted included in the design of the LNA.

7.1 Matching of Components

The mismatch between two components is usually expressed as a deviation of the measured device ratio from the intended device ratio from the intended device ratio. Suppose pair of resistors having value 10 kΩ is used by designer in layout. After fabrication, one pair of these resistors is found equal to 12.47 kΩ and 12.34 kΩ. This pair of resistors therefore exhibits a mismatch of approximately 1%.

Mismatch due to Random Variation

All components exhibit microscopic irregularities in their dimensions and composition. These irregularities fall into two categories: those that occur only along the edges of a device, and those that occur throughout a device. The former are called ***peripheral variations*** because they scale with device periphery, while the latter are called ***areal variations*** because they scale with device area.

Mismatch due to Process Biases

The dimensions of geometries fabricated in silicon never exactly match those in the layout database because the geometries shrink or expand during photolithography, etching, diffusion, and implantation. The difference between the drawn width of geometry and its actual measured width constitutes the ***process bias.*** Process biases can introduce major systematic mismatches in poorly designed components [25].

Mismatch due to Interconnect Parasitics

The leads that connect components into a circuit can introduce systematic mismatches. Ideally, leads should contribute negligible resistance and capacitance to the circuit, but real leads exhibit sufficient nonidealities to disturb the matching of both precision resistors and capacitors. One way to reduce the impact of lead resistance to reduce the lengths where possible and by placing multiple vias where one would normally employ but one.

Mismatch due to Etch Rate Variations in Resistors and Capacitors

Poly resistors are created by etching a doped polysilicon film. The etching rate depends, at least to some extent, on the geometry of the poly openings. Larger openings grant more access to the etchant and thus clear more quickly than small openings. Consequently, sidewall erosion occurs to a greater degree around the edges of a larger opening than the edges of a small one. This effect causes widely separated poly geometries to have smaller widths than closely packed geometries do. This mismatch can be reduce by adding ***dummy resistors*** are added to either end of aaray of matched resistors to ensure uniform etching.The dummy resistors may be constructed in one of two ways. Unconnected dummies are simply strips of polysilicon placed on either side of the array however unconnected dummies suffers from the problem of electrostatic modulation . Electrostatic modulation can be eliminated by connecting the dummies to ground or to some other suitable low-impedance node.

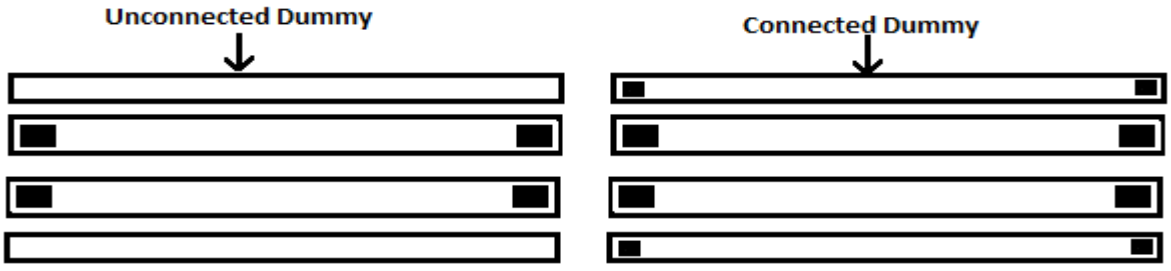

Figure 7.1: Unconnected and Connected Dummies [27].

Poly-poly capacitors experience the same etch rate variations as poly resistors. When matching arrays of capacitors, additional ***dummy capacitors*** should be placed around the edges of the array.

Stress Gradients

Mechanical stresses that affect the whole of the die give rise to regular patterns of stress. These patterns, and the effects they produce upon electrical parameters, can be minimized by proper layout precautions.

Piezoresistivity

The piezoresistivity of (100)-oriented silicon varies with orientation and doping. An N-type (100) silicon wafer exhibits maximum piezoresistivity along <100> axes and minimum piezoresistivity along <110> axes. Since dice are laid out in rows and columns relative to the wafer flat, the X- and Y- axes of the layout correspond to the desired <110> directions. The stress sensitivity of N-type monocrystalline resistors can therefore be minimized by them out either horizontally or vertically. A P-type (100) silicon wafer exhibits maximum piezoresistivity along <110> axes and minimum piezoresistivity along <100> axes. P-type monocrystalline resistors therefore exhibit the least stress resistivity if they are placed at 45 degrees to the X- and Y- axes of the layout.

The rate of change of stress intensity in a die is called the ***stress gradient***. The stress gradient is usually much greater at the extreme corners of the die than at any other point. If matched devices are resided close to one another it is possible to minimize the differences in stresses between them.

Centroids

The stress difference between two matched devices is proportional to the product of the stress gradient and the separation between them. For the purpose of the calculation, the location of each device is computed by averaging the contribution of each portion of the device to the whole. The resulting location is called ***centroid*** of the device.

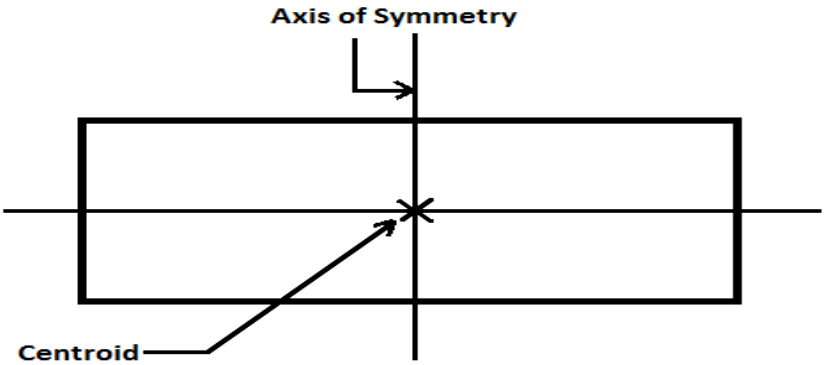

Figure 7.2: The Centroid of a Rectangle [27].

The centroid of a rectangular device lies in its exact centre. The centroids of other geometries can often be located by applying the ***principle of centroidal symmetry,*** which states that the centroid of geometry must lie on any axis of symmetry of that geometry.

Common Centroid Layout

If matched device is divided into identical sections and if they are arranged to form a symmetric pattern, then the centroid of the device will lie at the intersection of the axes of symmetry passing through the array. It is actually possible to arrange two arrayed devices so that they share common axes of symmetry. If this can be achieved, then the principle of centroidal symmetry ensures that the centroids of the two devices coincide. Figure 7.3 shows an example of such a ***common-centroid layout.***

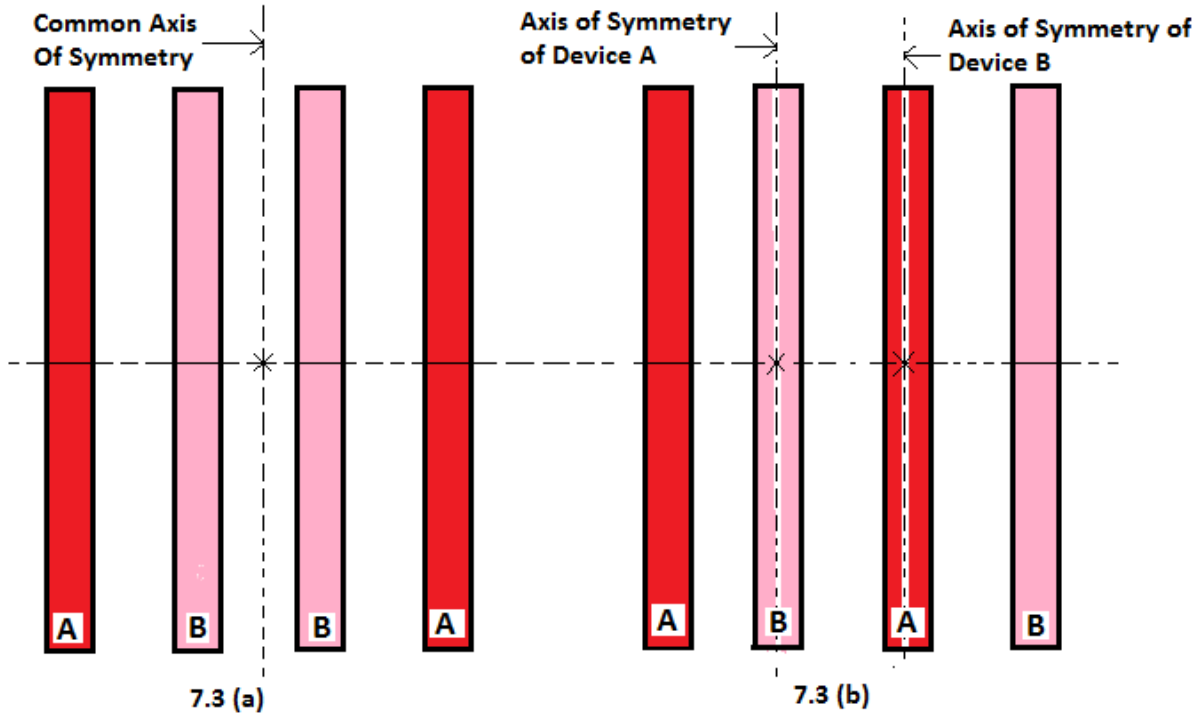

Figure 7.3: One Dimensional Common-Centroid Arrays [27].

Figure 7.3 shows two examples of common-centroid layouts produced by arraying segments of matched devices along one dimension. These types of layouts are usually called ***interdigitated arrays*** because the sections of one device interpenetrate the sections of the other like the intermeshed fingers of two hands. Figure7.3 (a) shows an interdigitated array consisting of two devices, each composed of two segments. The arrangement showed in figure 7.3 (a) follows the interdigitated pattern ABBA. This pattern has an axis of symmetry that divides it into two mirror-image halves (AB and BA). The interdigitated pattern ABAB

that is shown in figure 7.3 (b) should be avoided because it does not completely align the centroids of two devices, and the resulting separation of the centroids leaves the devices of being getting attacked or harmed by stress-induced mismatches. Second way by which one dimensional common centroid layout can be made is shown in figure 7.4.

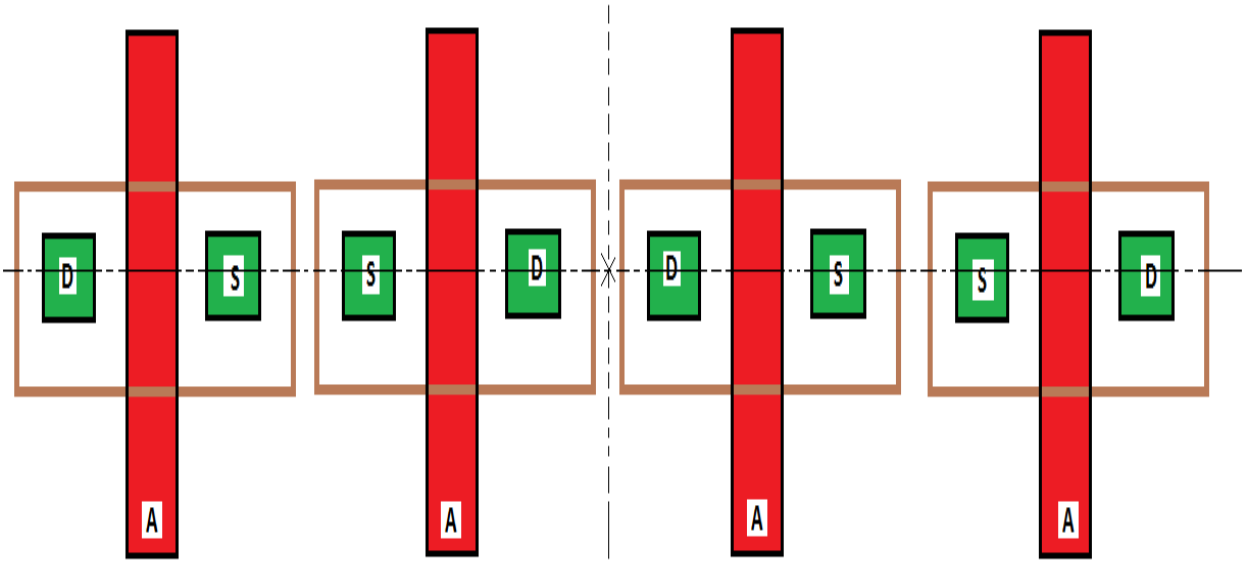

Figure 7.4: Second Way of Drawing Common Centroid Geometry [25].

In figure 7.4 fingering of device A is done in order to reduce the gate resistance [25]. Fingered MOSFET are placed in such a way that the principle of centroids is applicable as it is clear from the figure that MOSFET from a mirror image around the axis of symmetry thereby producing minimum stress gradients. One more way to optimize the layout technique shown in figure 7.4 is addition of dummies on extreme left and right side of device so that outer MOSFET' see same environment to their surroundings.

7.2 Layout Process

The first step in the process was to generate a layout which transformed all of the components from the schematic into their physical layout. Once the layout was generated, the components were moved into positions that would be advantageous. Interdigitated technique was used for MOSFET. The next step in layout was connecting all of the nets from the schematic. With the help of Cadence, all of the incomplete nets between components were identified. Metal path were used to connect the components. Arrays of vias between the metal layers were used as much as possible since a single via has a higher resistance than an

array of vias. The completed layout of single ended and differential ended LNA is shown in figure 7.4 and 7.5 respectively.

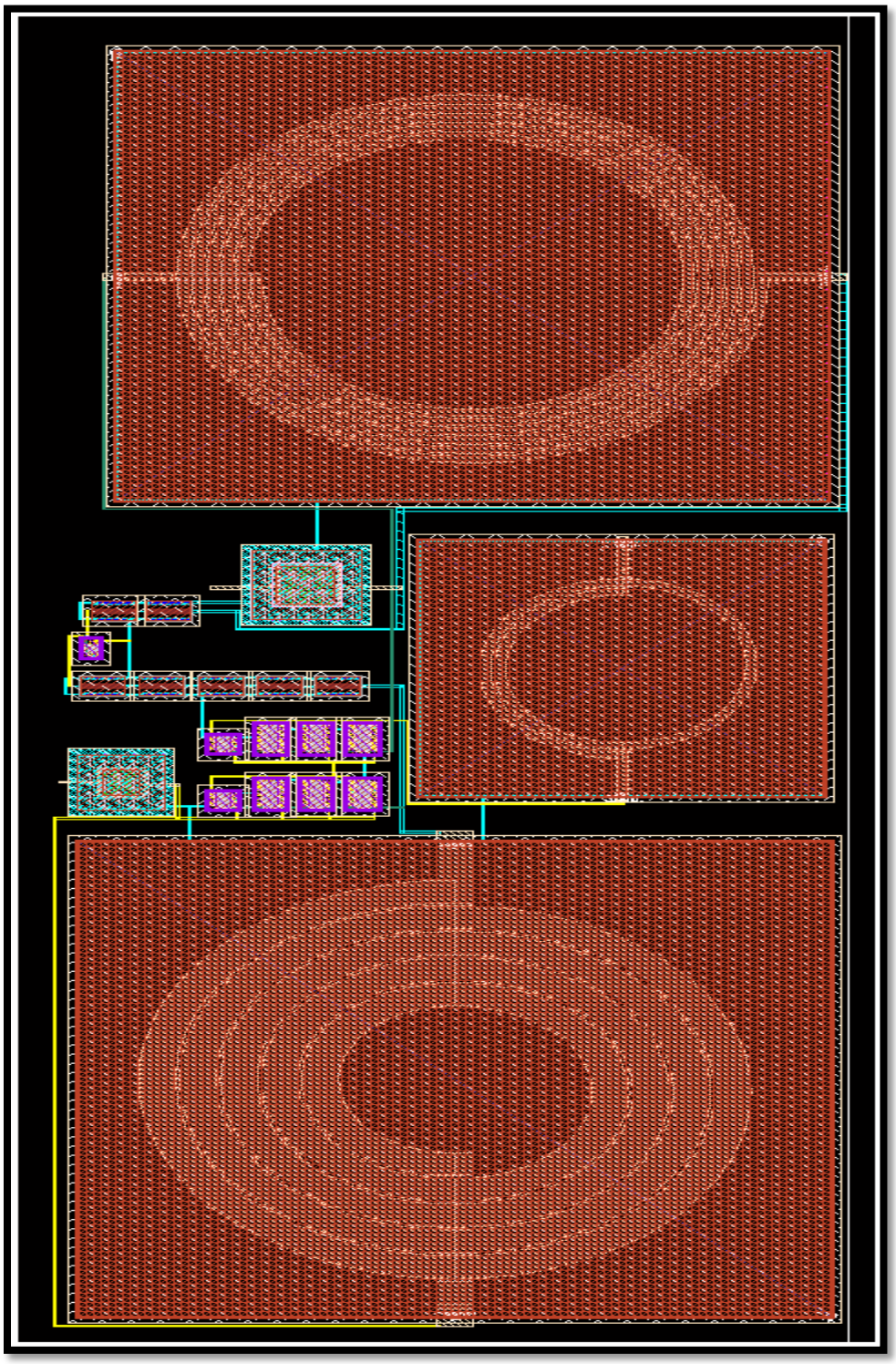

Figure 7.5: Layout Schematic of Single Ended LNA.

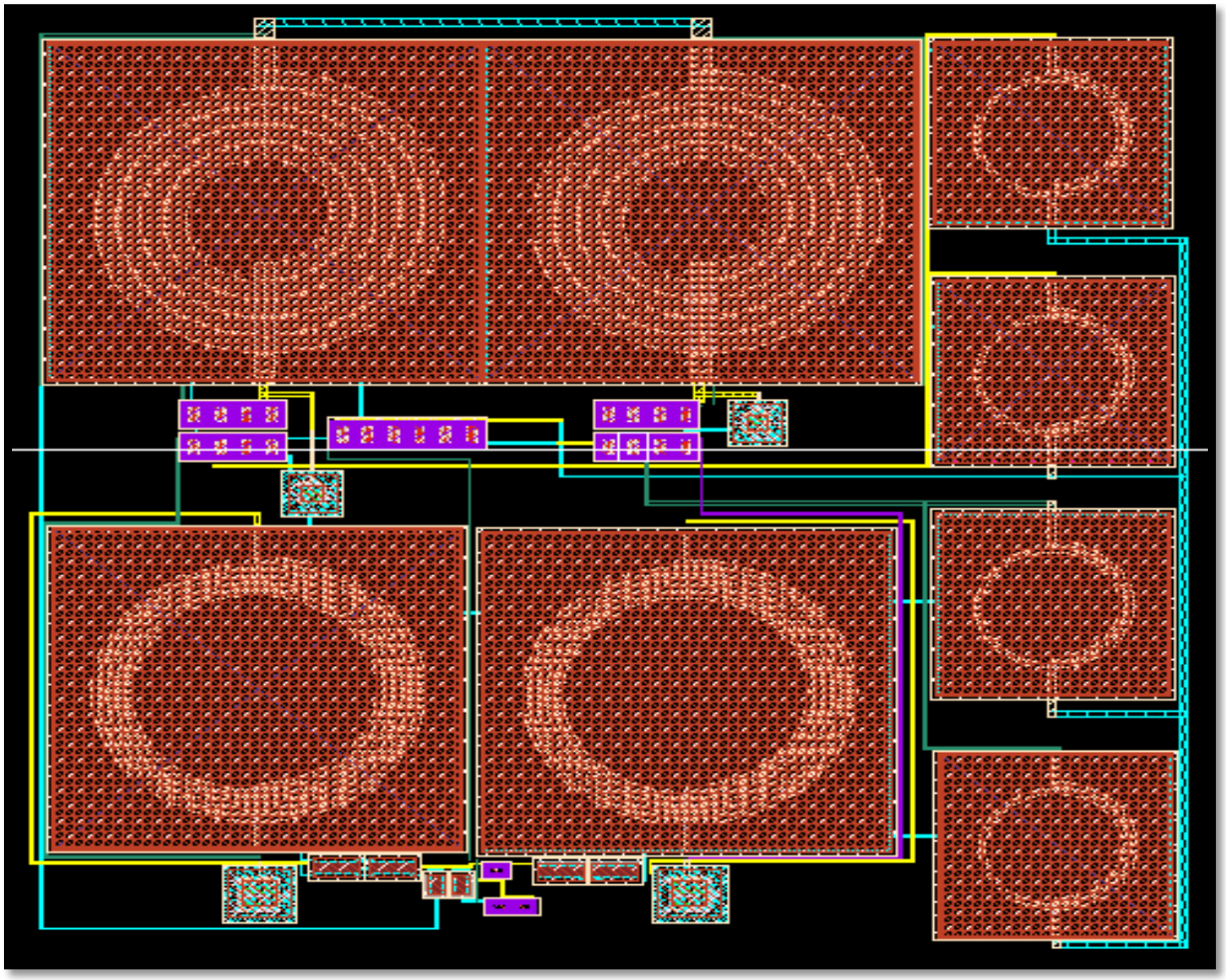

Figure 7.6: Layout Schematic of Differential LNA.

Design Rule Check

Once the layout was generated for single low noise amplifier and the incomplete nets were connected, the next step was to verify that the layout met the design rules of the fabrication process. The design rules specify the limitations of fabrication using the particular process. This verification was performed using the DRC function of Cadence. The DRC test compares the layout to the design rules of the process. When first performed, there were hundreds of DRC errors. Through iterations, these errors were reduced to zero.

Layout versus Schematic Check

After the mask layout design of the circuit is completed, the design should be checked against the schematic circuit description created earlier. The LVS check was completed successfully.

Chapter 8

Conclusion and Future Scope

8.1 Conclusion

Low Noise Amplifiers are an important component used in different RF Transceivers (Wi-Max, Wi-Fi, WLAN, WCDMA, Bluetooth *etc.).* They provide amplification, good matching and minimal noise to the system while maintaining linearity. Since, CMOS technology has become dominant because of its several advantages such as low cost, low static power dissipation and low area, the design of low noise amplifier using CMOS technology was top choice for design of Low Noise Amplifier.

The single ended and differential LNA was designed to operate in a WCDMA reception range $(2.11\ \text{GHz} - 2.17\ \text{GHz})$ using a BSIM3V2 model (Level 49) CMOS UMC 0.18μm technology in Cadence Virtuoso Environment. The key issues in the design, gain, noise and linearity were considered. The LNA's was designed to provide high gain, matching to 50Ω RF system, good linearity and minimum noise on the operation of the circuit.

The design used inductive source degeneration topology as it provided good matching and low noise figure as compared to other topologies. Additionally, power constrained noise optimization technique was used for power and noise optimization. Finally, layout of single ended and differential LNA was drawn. In layout process, interdigitated technique was used for minimizing mismatches and also physical sizes was altered to minimize the chip area.

Table 9: Results Obtained for Single Ended and Differential LNA.

Parameters		**Results Obtained**	
		Single Ended LNA	**Differential LNA**
Voltage Gain(dB)		17.14	15.19
Noise Figure(dB)		2.976	4.038
Third Order Intercept Point(dBm)		−12.00	−13.00
Matching Parameters (dB)	S11	−26.97	−17.47
	S22	−18.17	−6.587
Power Consumption(mW)		7.353	8.738

Table 9 shows the results for the LNA's designed. All results obtained were within the specified limits. Single Ended LNA was also successfully simulated for various corner conditions. During corner conditions it was observed that when resistors were at minimum values the current consumption get increased. From corner analysis the worst case power dissipation was found to be 8.703 mW and best one was 6.0912 mW. Similarly the worst case noise figure was 4.495 dB and best one is 3.247 dB. Variations found in centre frequency was 1.4%.

8.2 Future Scope

In future, for investigating design of Low Noise Amplifiers for RF applications following work may be extended:

- Passive inductors occupy large area so either inductorless or active inductors may be used for design purpose.
- The low noise amplifier may also include additional constraints such as signal to noise ratio (SNR), signal to noise plus distortion ratio (SNDR), spurious free dynamic range (SFDR).
- Bandgap reference generators should be may used instead of resistors for providing bias as they produce less noise and are temperature independent.

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