CERTIFICATE

I hereby certify that the work which is being presented in the thesis entitled, **"DESIGN OF NMOS FOUR QUADRANT ANALOG MULTIPLIER"** in partial fulfillment of the requirement for the award of degree of M.Tech (VLSI Design & CAD) at Electronics and communication Department of Thapar University Patiala, is an authentic record of my own carried out under the supervision of Ms. Manu Bansal, Senior Lecturer, ECED. The matter embodied in this thesis has not been submitted in any other University/Institute for the award of any degree.

15/7/09

Abhishek Misra

Date **(60761027)**

It is certified that the above statement made by the student is correct to the best of my knowledge and belief.

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Abstract

Analog multipliers found its wide spread applications in the era of signal processing, neural networks as well as frequency doublers, RMS circuits and phase detectors (Phase lock loop). High Input signal range, linearity and high operating frequency are the prime issues for the multipliers in conventional applications like modulation circuits. Power consumption is the criteria in case of massive parallel processing based networks.

This thesis explains the design process of four-quadrant multiplier designed using eldo simulator at 0.35µm technology which could be able to address the challenges mentioned above. Initially, different multipliers architectures have been discussed. A NMOS based four quadrant voltage mode multiplier is designed using differential summing, squaring and amplifier circuits and is simulated for DC, transient and AC analysis to confirm the correctness of the design. In addition to these, bandwidth, mismatching of transistors and active area of the chip are also optimized. The final design of multiplier has ±0.66V input range, 67.79MHz bandwidth, 1.51mW power consumption with 0.691V bias voltage. Special layout techniques like interdigitation and common centriod methods can be utilized to reduce mismatches between transistors and effects of process variations are minimized.

Chapter-1

INTRODUCTION

1.1 Analog Multiplier

In electronics, an analog multiplier is a device which takes two analog signal and produces an output which is their product. Such circuits can be used to implement related functions such as squares.

Although analog multiplier circuits are very similar to operational amplifiers, they are far more susceptible to noise and offset voltage-related problems as these errors may become multiplied. When dealing with high frequency signals, phase-related problems may be quite complex. For this reason, manufacturing wide-range general-purpose analog multipliers is far more difficult than ordinary operational amplifiers. This means they have a relatively high cost and so they are generally used only for circuits where they are indispensable.

In most cases the functions performed by an analog multiplier may be performed better and at lower cost using Digital Signal Processing techniques. At low frequencies a digital solution is cheaper and more effective, and allows the circuit function to be modified in firmware. As frequencies rise, the cost of implementing digital solutions increases much more steeply than for analog solutions. As digital technology advances, the use of analog multipliers tends to be ever more marginalized towards higher-frequency circuits or very specialist applications. Multiplier is much better than other structures in terms of power consumption, and is hence especially suitable for implementation of large-scale circuits.

1.2 COMPARISON BETWEEN ANALOG MULTIPLIER AND DIGITAL MULTIPLIER

1.2.1 Decline of the Analog Multiplier

In most cases the functions performed by an analog multiplier may be performed better and at lower Processing cost using Digital Signal techniques. At low frequencies a digital solution is cheaper and more effective, and allows the circuit function to be modified in firmware. As frequencies rise, the cost of implementing digital solutions increases much more steeply than for analog solutions. As digital technology advances, the use of analog multipliers tends to be ever more marginalized towards higher-frequency circuits or very specialist applications.

In addition, most signals are now destined to become digitized sooner or later in the signal path, and if at all possible the functions that would require a multiplier tend to be moved to the digital side. For example, in early digital multimeters, true RMS functions were provided by external analog multiplier circuits. Nowadays (with the exception of high-frequency measurements) the tendency is to increase the sampling rate of the ADC in order to digitize the input signal allowing RMS and a whole range of other functions to be carried out by a digital processor.

1.2.2 Analog Multiplier

In an instrument with an analog multiplier, the phase sensitive detector (PSD) comprises an electronic circuit which multiplies the applied signal with a sine wave at the same frequency as the applied reference signal. Although the technique is very simple in principle, in practice it is difficult to manufacture an analog multiplier which is capable of operating linearly in the presence of large noise, or other interfering, signals. Non-linear operation results in poor noise rejection and thereby limits the signal recovery capability of the instrument.

1.2.3 Digital Switching Multiplier

The switching multiplier uses the simplest form of demodulator consisting of an analog polarity-reversing switch driven at the applied reference frequency. The great advantage of this approach is that it is very much easier to make such a demodulator operate linearly over a very wide range of input signals.

1.2.4 Requirement of Analog Multiplier

In fact there are a number of operations where analog processing has clear advantages over digital. Digital multiplication is simple and cheap, but if the original data and the required output are both analog, the cost and complexity of analog-to-digital converters (ADCs) and digital-to-analog converters (DACs) to convert from analog to digital and back again often exceed those of an analog multiplier. Also, the digital propagation delay may be too great for a high-speed system.

In addition, it may be more efficient to process the analog signals before the ADC, even if digital data is required. An example is ac power measurement. If the signal to be measured is a simple 50 or 60 Hz sine wave and the load is resistive, then the measurement is simple. But if the signal is more complex, the load is reactive, or the frequency is higher, then it is necessary to over-sample both the voltage and the current in the load to determine the actual power, increasing the demands on converters and processor. An analog multiplier driven by the voltage and current in the load has an output proportional to instantaneous power, which may be integrated and sampled quite slowly.

Even if we are only interested in the root-mean-square (rms) voltage of a complex waveform, analog rms computation works at several gigahertzes – 100 times faster than an over-sampled digital system.

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The digital implementation, in treating the MOS capacitor-based devices as binary switches, sacrifices power efficiency for the ability to regenerate weak or degraded signals within the circuit. The analog implementation uses the fundamental device I-V transistor relationships to efficiently achieve the sum and multiplication functions. However, the analog circuit is unable to regenerate weak or degraded internal signals.

The digital circuit is more sensitive to changes in speed. This sensitivity is due to the ability of the digital circuit to exploit a decrease in operating frequency by supporting a corresponding decrease in the supply voltage. The digital circuit is also more sensitive to changes in technology. By decreasing the minimum feature size of the CMOS technology, a significant power savings is achieved. This behavior is not necessarily true for the analog circuit, since device physics limits the analog circuit more severely than the digital circuit

Chapter 2

APPLICATION OF ANALOG MULTIPLIER

2.1 Modulators

Modulation is a process wherein an information-carrying signal is introduced into a carrier signal. In amplitude modulation, the amplitude of the carrier carries the information of the modulating signal

$$V_o = V_{cA}(1 + m\cos\omega_c t)\cos\omega_c t \tag{2.1}$$

$$= V_1 V_2 \cos\omega_c t + \frac{V_1 V_2}{2} m\cos(\omega_c - \omega_m)t + \frac{V_1 V_2}{2}\cos(\omega_c + \omega_m)t$$

For high frequencies, single-device modulators are used and the square-law term of the transfer characteristic of the device provides the multiplication function which is done by MOS device not by BJT.

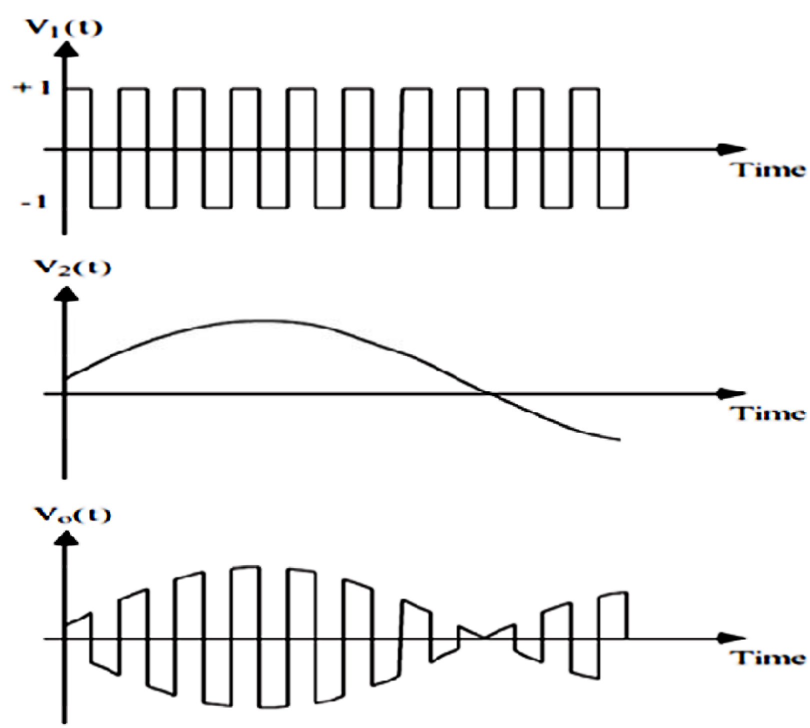

Fig. 2.1: Amplitude modulation

$$V_o(t)=K\left(V_c(t)V_m(t)\right)$$

$$= K \sum_{n=1}^{\infty} V_1 V_2 \cos nW_c t + V_1 V_2 \cos W_m t$$

$$=K \sum_{n=1}^{\omega} V_1 V_2 \cos(nW_c t\text{-}W_n t) + V_1 V_2 \cos(nW_c t + W_n t)$$

2.2 Phase-Locked Loops

Phase detector is an essential element in phase locked loops. PLLs are widely used in frequency synthesizers .Phased locked loop is a universal building block used in both analog and digital applications. The basic structure of Phase locked loop is shown in the Figure 1.1. Phase detector finds the phase difference between input and output signals of the controlled oscillator and locks the PLL on zero phase difference. Analog multiplier is most widely used as phase detector in PLLs

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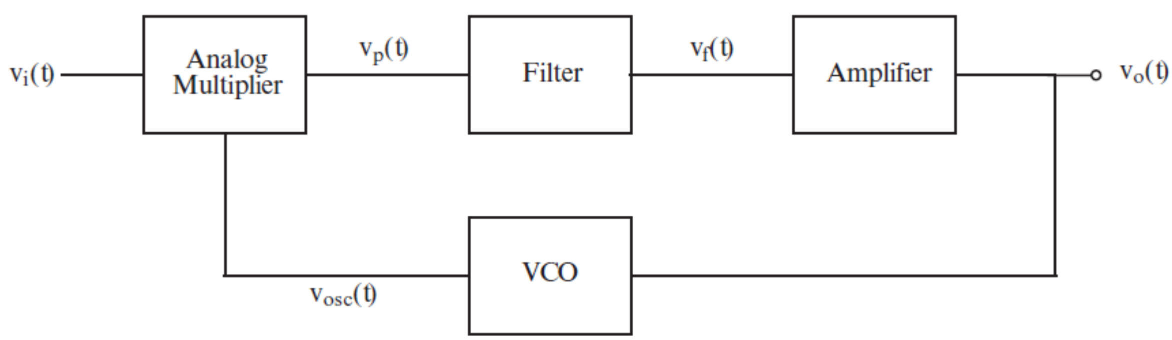

Figure2.2: Block diagram of a phase-locked loop

If unmodulated signals of identical frequency are applied to the two inputs, the circuit behaves as a phase detector and produces an output whose dc component is proportional to the phase difference between the two inputs. The output waveform that results is shown in Fig (c) and consists of a dc component and a component at twice the incoming frequency. The dc component is given by:

$$V_{avg} = \frac{1}{2\pi}\int_0^{2\pi} V_o(t)d(W_o t) \quad (2.2)$$

If input signals are comparable to or smaller than V_t, the circuit still acts as a phase detector. However, the output voltage then depend both on the phase difference and on the amplitude of the two input waveforms.

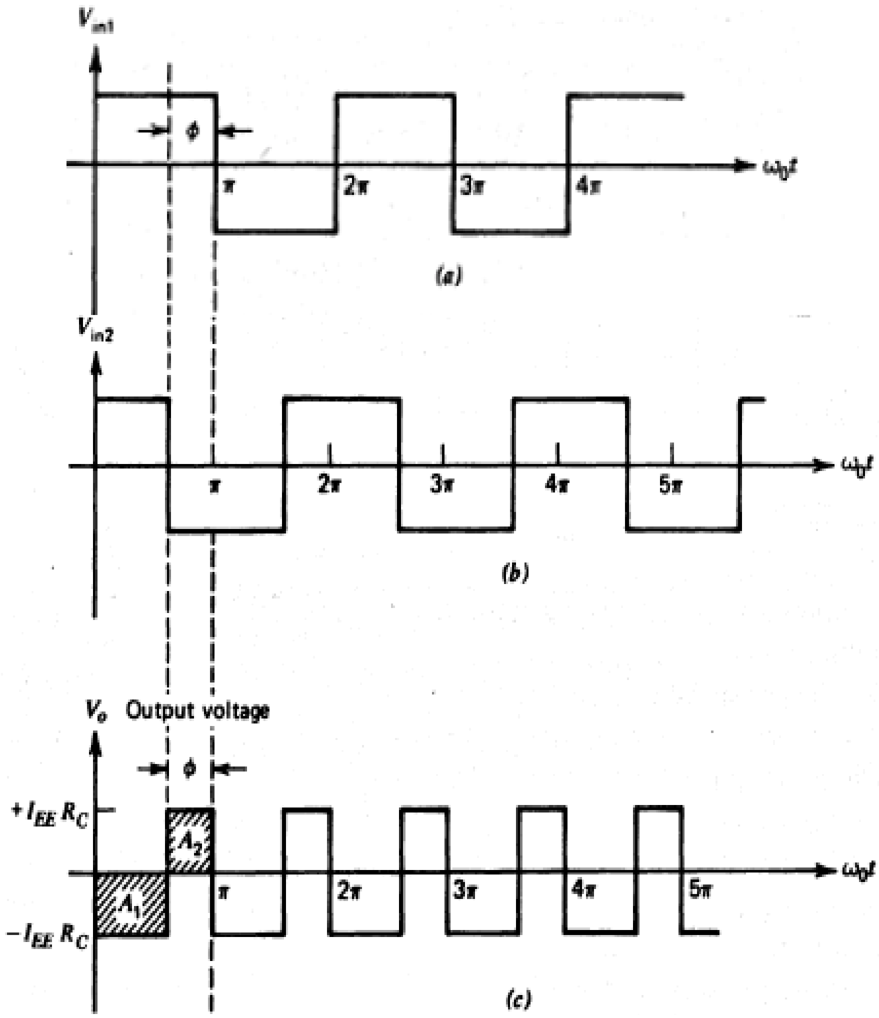

Figure 2.3: (a) signal 1 (b) signal2 (c) phase detector output

2.3 Generation of integer powers

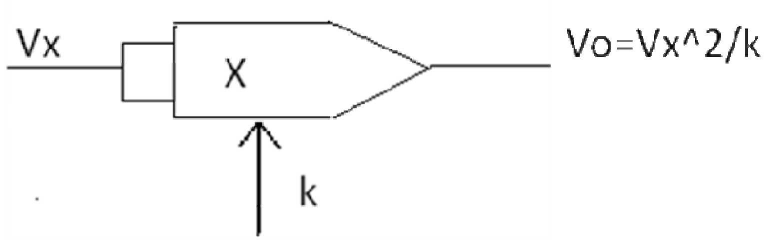

Figure 2.3: Squarer

By connect the two input of a multiplier together, a square can be obtained. If the input to the square can be obtained. If input to the square is V_x , the output is $\frac{V^2}{2K}$. By feeding the output of square along with original input to another multiplier, we get a squarer. The sample principle can be extended to generate any higher integer power of analog signals.

2.4 Frequency Multiplier

A square can be used as a frequency doubler. if the input V_x to the squarer is sinusoidal signal , a sin wt, its output is given as

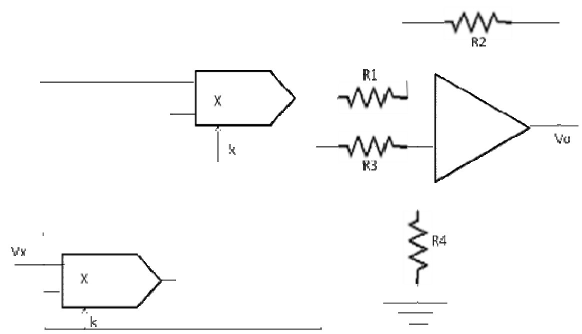

Figure 2.4 : Frequency tripler

$$V_o = \frac{A^2 sin^2(wt)}{k}$$

$$= \frac{A^2(1-\cos(2wt))}{k} \qquad (2.3)$$

Thus the output signal contains a DC component and co sinusoidal component of frequency 2w, which is twice that of the input signal.

2.5 Divider circuit

The output of multiplier is $V_o V_x / k$. Kcl at node E gives

$$\frac{V_1}{R_1} + \frac{V_2}{R_2} = 0$$

And $V_o V_x / k$.

$$V_o = kR_1V_z/R_2V_x$$

If $R_1 = R_2$ then

$$V_o = kV_z/V_x \quad (2.4)$$

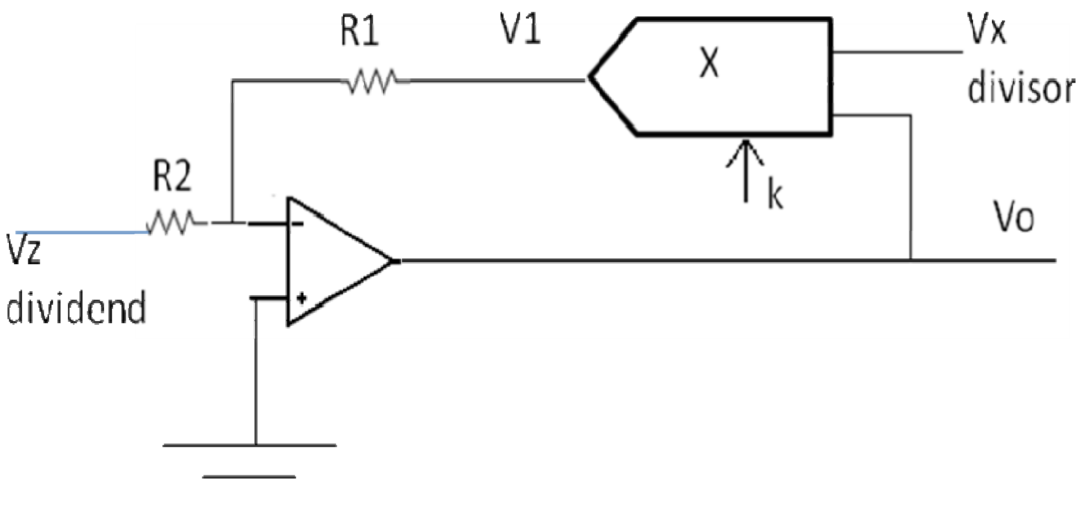

Figure 2.5: Divider circuit

2.6 Square root extractor

A square root circuit can be obtained by connecting the V_x terminal of the divider to V_o terminal. Setting V_o=V_x,

$$V_o = -k\frac{R_1}{R_2}\frac{V_z}{V_o}$$

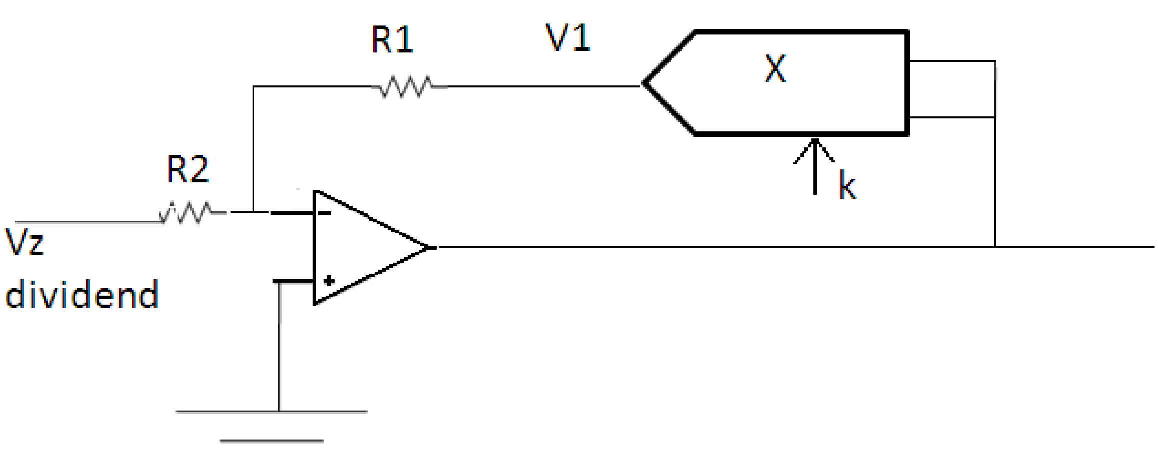

Figure 2.6: Square rooter

$$V_o = \sqrt{-k\frac{R_1}{R_2}V_z} \qquad (2.4)$$

2.7 Root mean square measurement

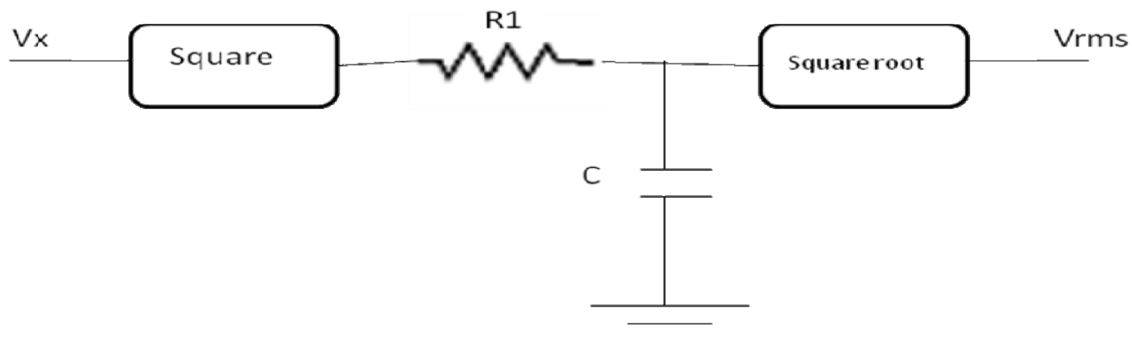

Figure 2.7: RMS converter circuit

A frequent use of analog multiplier is in the measurement of the root mean square of an analog signal

$$V_{rms} = \sqrt{\overline{V_x^2}} \qquad (2.5)$$

Channel length modulation, long channel transistor must be used

Chapter 3

Background

3.1 Introduction

Non linear operation on the continuous value analog signal is often required in instrumentation, communication and control system design. The operation include Modulation and demodulation

1. Frequency translation
2. Multiplication

In this chapter contain most commonly used techniques for performing multiplication with in monolithic integrated IC. In analog signal processing the need often arises for a circuit that takes to analog input and produces an output propositional to their product. Such circuits are termed analog multiplier.

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3.2 The Emitter-Coupled Pair as a Simple Analog Multiplier

The simple emitter-coupled pair of Figure 3.1a provides a very simple example of an elementary multiplier.

$$I_{c1} = \frac{I_{EE}}{2}\left[1 + \tanh\left(\frac{d}{2}\right)\right] \quad (3.1)$$

$$I_{C2} = \frac{I_{EE}}{2}\left[1 - \tanh\left(\frac{d}{2}\right)\right] \quad (3.2)$$

Where d = V_{i1}/V_t and $V_{i1} = V_{i1} - V_{i2}$ is the differential-mode input signal. As usual, base currents are neglected. A common-mode (bias) input, $V_{B1} = \frac{V_{i1}+V_{i2}}{2}$, may affect the value of IEE, the dc value of the common-emitter current source. For $\gg 1$, the tanh function can be approximated well by the first term of its power-series expansion of tanh

$$\tanh\left(\frac{V_{i1}}{2V_t}\right) \approx \frac{V_{t1}}{2V_t} \quad (3.3)$$

$$V_{o\approx -} I_{EE} R_c \frac{V_{i1}}{2V_t} \quad (3.4)$$

A second input signal can be introduced into a transistor realization of IEE as shown in fig (3.1b).

$$I_{ee} \approx \frac{V_{i2} - V_{BEon} - (-V_{EE})}{R_B} \tag{3.5}$$

This second input in terms of its bias and variational components is

$$V_{i2} = V_{i2} + V_{B2} \tag{3.6}$$

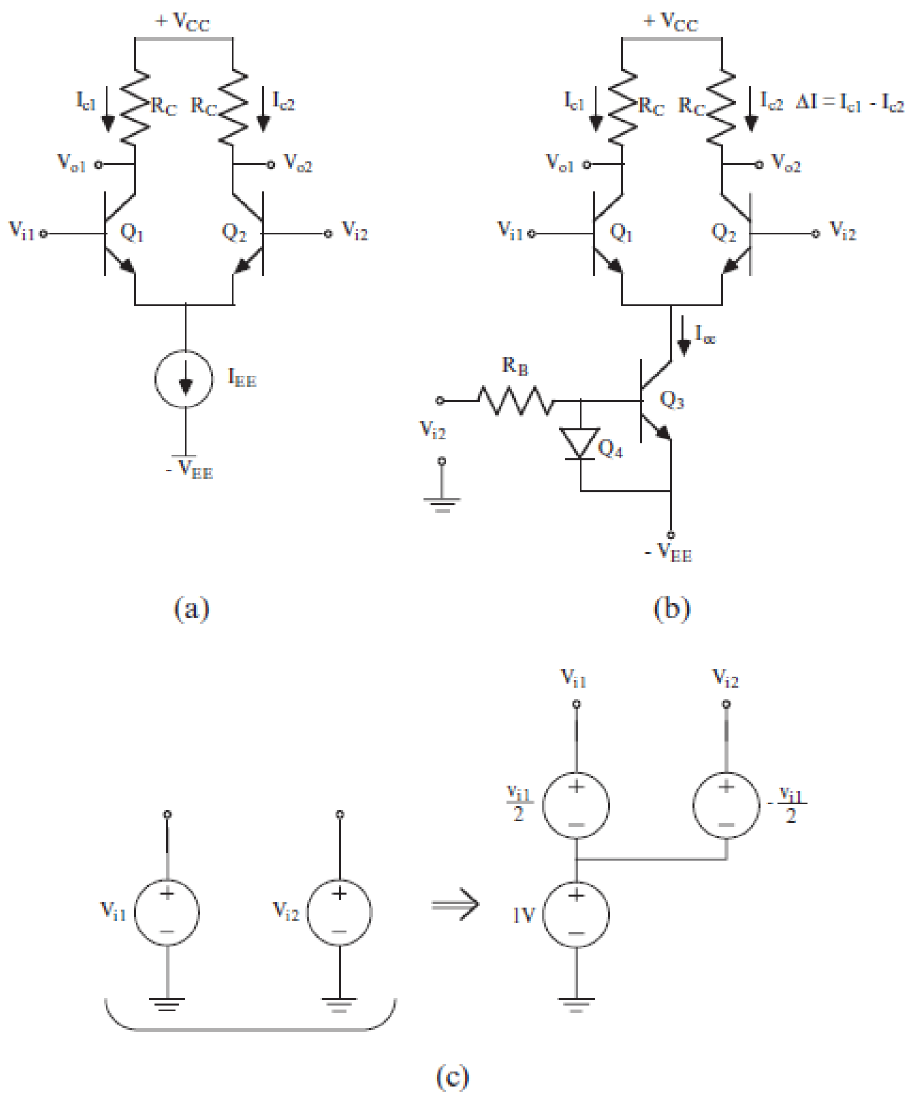


Figure 3.1: (a) A simple emitter coupled pair. (b) A second input introduced through I_{ee} (c) Common-mode and differential-mode input signals with reference[20]

The total common-emitter current source is

$$I_{ee} = i_{ee} + I_{EE} = \frac{V_{i2}}{R_B} + \frac{V_{B2} - V_{BEon} + V_{EE}}{R_B} \tag{3.8}$$

$$= \frac{V_{i2}}{R_B} + I_{EE} \tag{3.9}$$

where iee is the incremental value dependent upon vi2 and I_{EE} is the dc value. (Remember that I_{EE} may also depend upon V_{B1}). The differential output voltage of the ECP becomes

$$V_o = -\frac{R_C}{R_B}\frac{v_{i1}v_{i2}}{2V_t} - \frac{R_C I_{EE} V_{i1}}{2V_t} \tag{3.10}$$

The output voltage can then be written

$$V_o = V_{on} + f(I_{EE}, V_{i1}) \tag{3.11}$$

The v_{om} term above is the one of immediate interest and can be considered the 'ideal' multiplier output.

$$v_{om} = -Kv_{i1}v_{i2} > \tag{3.12}$$

where the multiplier coefficient is

$$K = \frac{R_C}{R_B}\frac{1}{2V_t} \tag{3.13}$$

3.3 A Subtraction Improvement

The simple ECP analog multiplier suffers from the small input signal restriction and the offset voltage due to v_{i1} alone. In terms of the original equations

$$v_o = V_{o1} - V_{o2} = \frac{R_C}{R_B}\tanh\left(\frac{v_{i1}}{2V_t}\right)V_{i2} - R_C I_{EE}\tanh\left(\frac{v_{i1}}{2V_t}\right)$$

The second term can be eliminated by an addition (subtraction) configuration involving an additional ECP. In the configuration of Figure(3.2a), a second pair, $Q_3 - Q_4$, is in parallel with the first ECP, $Q_1 - Q_2$, except that the input voltage drive to the second pair is inverted, i.e., has the opposite phase as of the first pair. The differential output voltage is

$$v_0 = -[(I_1 - I_2) + (I_3 - I_4)]R_C \quad (3.14)$$

$$= -\left[I_{EE1}\tanh\left(\frac{v_{i1}}{2V_t}\right) + I_{EE2}\tanh\left(\frac{-v_{i1}}{2V_t}\right)\right]R_C \quad (3.15)$$

$$= -(I_{EE1} - I_{EE2})R_C\tanh\left(\frac{v_{i1}}{2V_t}\right) \quad (3.16)$$

if the two pairs have equal common-emitter current sources, the differential output voltage cancels and is zero. This cancellation aspect at first does not seem promising unless we also consider the case where the two common-emitter currents sources have incremental components which are also out of phase and are proportional of $V_{i2.}$

$$I_{ee1} = I_{EE} + i_{ee} \quad (3.17)$$

$$I_{ee2} = I_{EE} - i_{ee} \quad (3.18)$$

Using these in (3.27), we obtain

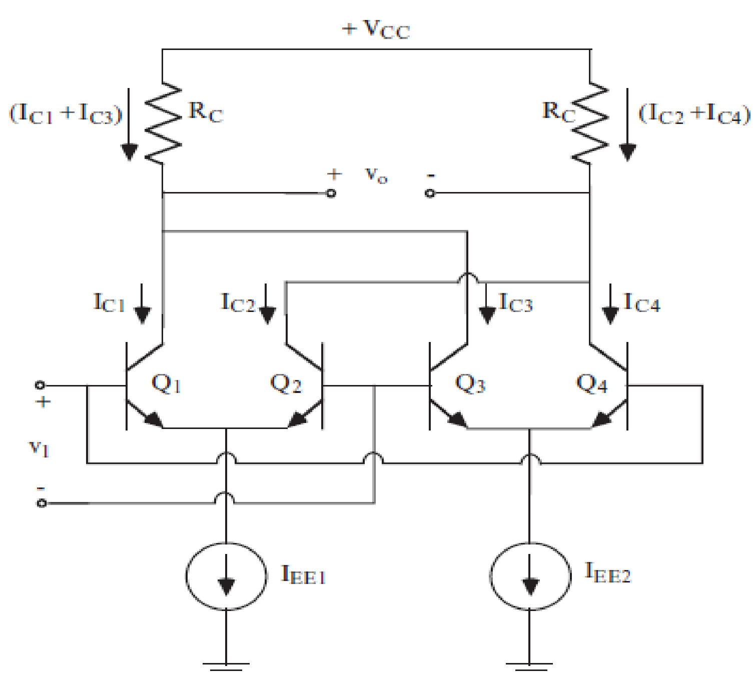


Figure 3.2: (a) Circuit to eliminate the second term of Equation (3.9) with reference[20]

$$v_o = 2i_{ee}R_C\tanh\left(\frac{v_{i1}}{2V_t}\right) \tag{3.19}$$

The dc offset in v_o is eliminated provided that we can produce the currents in (3.3.85). A new inverting stage is necessary to obtain $-v_{i2}$ and thus $-iee$. A simpler scheme uses a third ECP, $Q_5 - Q_6$, as shown in fig (3.2b). The difference of the 'source' currents IC_5 and IC_6 is

$$I_{C5} - I_{C6} - I_{EE}\tanh\left(\frac{v_{i2}}{2V_t}\right) \tag{3.20}$$

Starting with (3.10), we obtain

$$v_o = -R_C[(I_{C1} + I_{C3}) - (I_{C2} + I_{C4})] \tag{3.20}$$

$$v_o = -R_C[(I_{C1} - I_{C2}) - (I_{C3} - I_{C4})] \tag{3.21}$$

$$v_o = -R_C\left[I_{C5}\tanh\left(\frac{v_{i1}}{2V_t}\right) + I_{i6}\tanh\left(-\frac{V_{i1}}{2V_t}\right)\right]$$

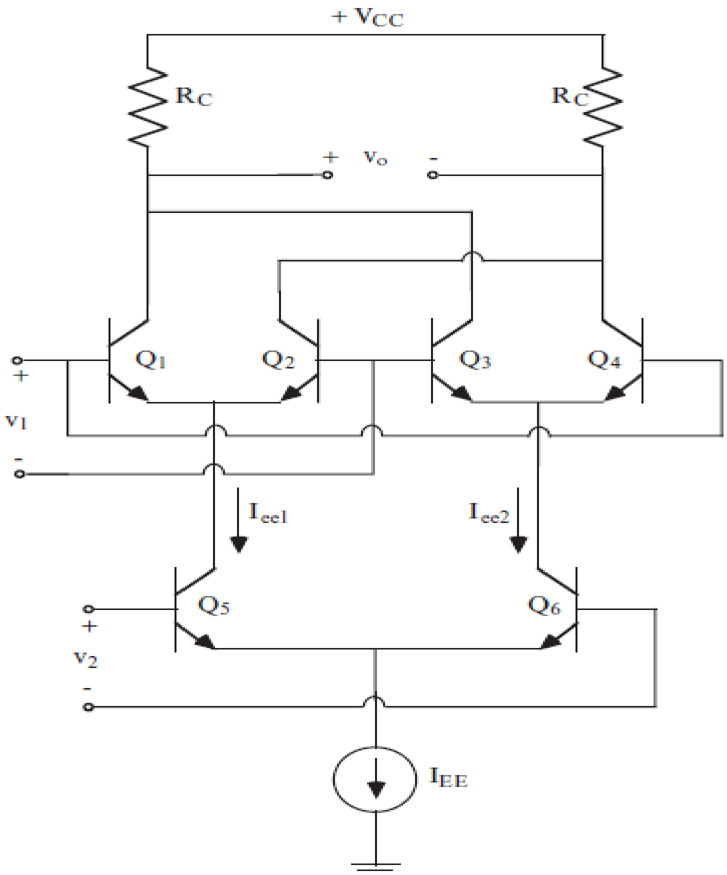


Figure 3.2: (b) A fully balanced four-quadrant multiplier circuit. with reference[20]

$$v_o = -R_C\left[(I_{C5} - I_{C6})\tanh\left(\frac{v_{i1}}{2V_t}\right)\right] \tag{3.22}$$

$$v_o = -R_C I_{EE}\tanh\left(\frac{V_{i2}}{2V_t}\right)\tanh\left(\frac{v_{i1}}{2V_t}\right) \tag{3.23}$$

$$v_o = v_{om} = -\frac{R_C I_{EE}}{4V_t^2} v_{i1} v_{i2} \tag{3.25}$$

The magnitude restriction on the input signals for linearity remains the same now for both v_{i1} and v_{i2}. The final circuit of this section in fig (3.2b) is often referred to as a fully balanced multiplier and as a four-quadrant multiplier. The latter is the result of the output of the multiplier having the same relative behavior in all of the four quadrants of the v_{i1}–v_{i2} plane, dependent only on the sign of the input signals.

3.4 Predistortion and Linearity Improvement in the ECP

B. Gilbert first proposed a scheme to predistort the input signal to an emitter coupled pair, at the expense of gain, which greatly extends the linearity range of the circuit . This is of particular importance for analog multipliers, but also has application for other large-signal uses of the ECP. In the Gilbert predistortion scheme, diodes (diode connected transistor) are introduced at the input of

$$Va = V_B - V_t \ln\left(\frac{I_a}{I_S}\right) \tag{3.26}$$

$$V_b = V_E - V_t \ln\left(\frac{I_b}{I_S}\right) \tag{3.27}$$

where I_S is the saturation current of the bipolar device. The difference voltage, $V_a - V_b$, is taken as the differential input voltage to an ECP.

$$v_{i1} = V_a - V_b = -V_t \ln\left(\frac{I_a}{I_b}\right) = V_t \ln\left(\frac{I_b}{I_a}\right) \tag{3.28}$$

For the pair shown in Figure (3.3b), the collector currents, from (3.1) and (3.2) are

$$I_{C1} = \frac{I_{EE}}{1 + \exp(-d)} = \frac{I_{EE}}{2}\left[1 + \tanh\left(\frac{d}{2}\right)\right] \tag{3.29}$$

$$I_{C2} = \frac{I_{EE}}{1+\exp(d)} = \frac{I_{EE}}{2}\left[1 - \tanh\left(\frac{d}{2}\right)\right] \tag{3.30}$$

where $d = v_{i1}/V_t$. The difference of the two currents and the ratio of the two are

$$I_{C1} - I_{C2} = I_{EE} \tanh\left(\frac{d}{2}\right) \tag{3.31}$$

$$\frac{I_{C1}}{I_{C2}} = \exp(d) \tag{3.32}$$

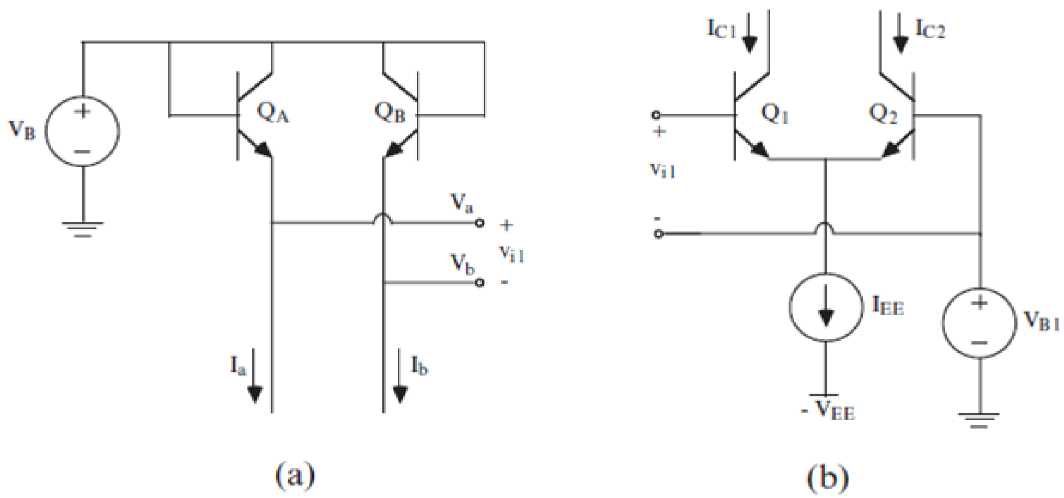


Figure 3.3: (a) Circuit with currents as inputs. (b) An EC pair circuit. with reference[20]

$$\frac{I_{C1}}{I_{C2}} = \frac{I_b}{I_a} \tag{3.33}$$

Next recognize that IEE = IC1+IC2 (assuming that the base currents can be neglected). In addition, (3.21) is introduced into (3.19) to obtain

$$I_b - I_a = (I_a + I_b)\tanh\left(\frac{d}{2}\right) \tag{3.34}$$

This is solved for the tanh function which is used in (3.19).

$$I_{C1} - I_{c2} = \frac{I_{EE}}{I_a + I_b}(I_b - I_a) \tag{3.35}$$

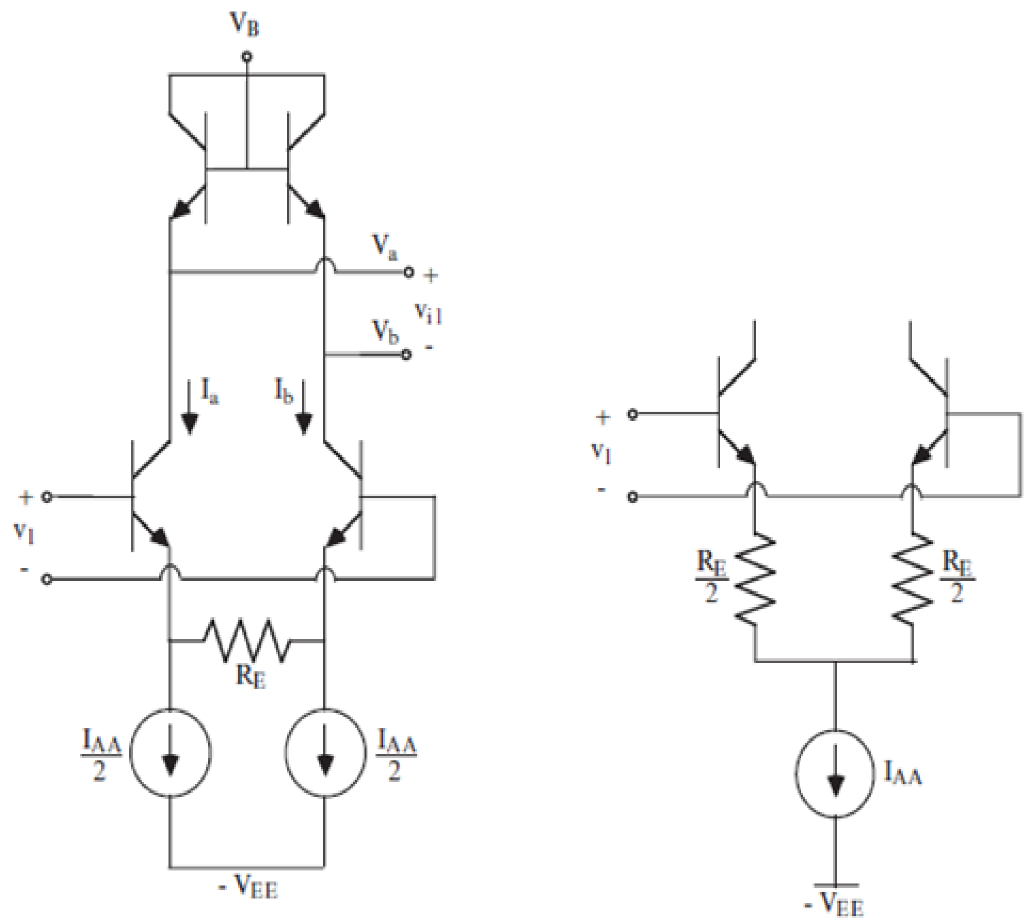


Figure 3.3: (c) An input voltage-to-current transducer. (d) An alternate arrangement to linearize the transfer characteristics. **with reference[20]**

We therefore have a linear relationship between the differential input currents,($I_b - I_a$) and the differential output currents, ($I_{C1} - I_{C2}$), of the pair. Figure(3.3c) is an input voltage-to-current ‘transducer. Here common-emitter resistor is used to linearise the transfer characteristic of an ECP. as given below R_E.

$R_E >> V_t / I_a$ and V_t / I_b

$$I_a = \frac{\frac{v_1}{2}}{\frac{R_E}{2}} + \frac{I_{AA}}{2} \tag{3.36}$$

$$I_b = \frac{\frac{-v_1}{2}}{\frac{R_E}{2}} + \frac{I_{AA}}{2} \tag{3.37}$$

Where v_1 is the differential input voltage to the transducer pair. The difference output current of the transducer is

$$I_a + I_b = I_{AA} \tag{3.38}$$

Since (I_a +I_b) is constant in equ (3.23) The complete predistorted pair is shown in Figure(3.4a). The differential output voltage is

$$v_O \approx -R_C(I_{C1} - I_{C2}) = +2\left(\frac{R_C}{R_E}\right)\left(\frac{I_{EE}}{I_{AA}}\right)v_i \tag{3.39}$$

The improvement in linearity with R_E is clear, although the voltage gain suffers.

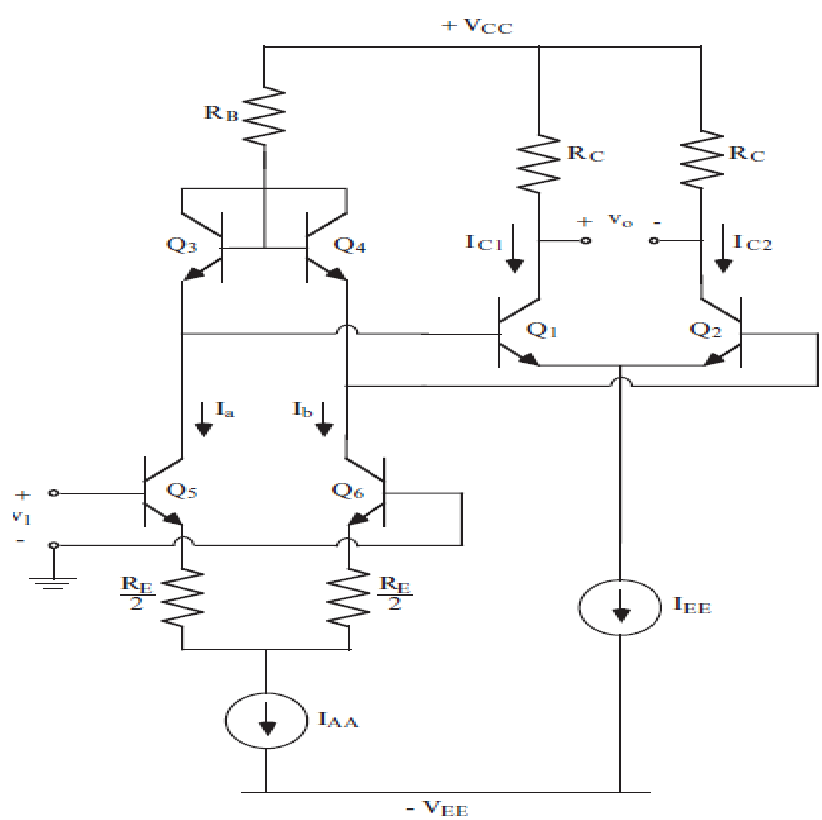


Figure 3.4: (a) The complete predistorted pair. with reference[20]

This predistortion scheme can be used with the simple analog multiplierof the last section by also introducing a second input signal into the current source, I_{EE}.

3.5 The Gilbert Cell

Four-quadrant multiplier is obtained when two simple analog multipliers of a single pair each are arranged in parallel

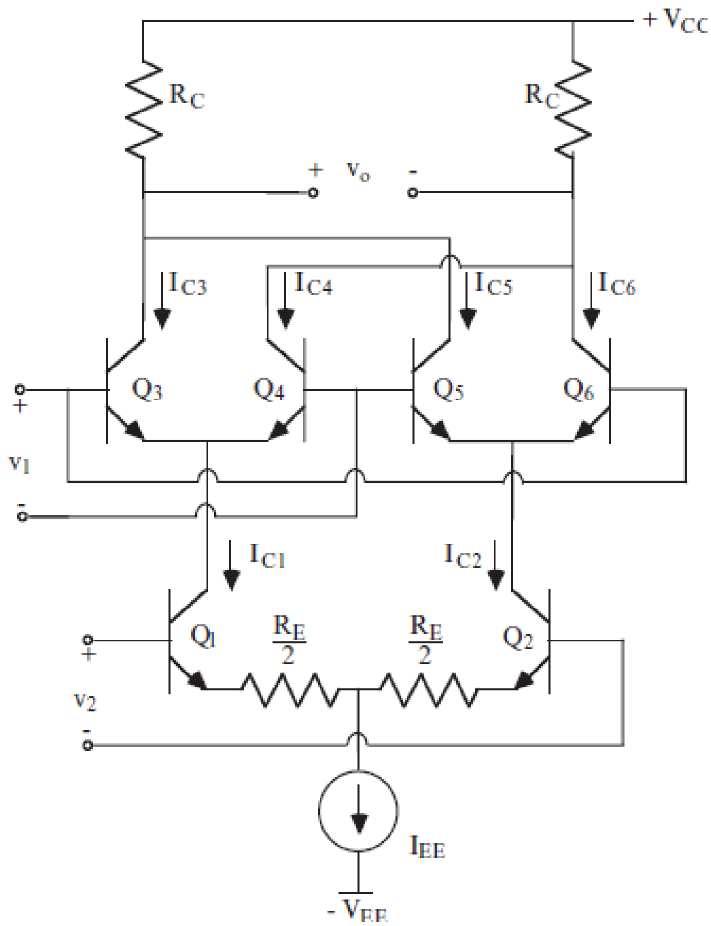


Figure 3.5: (a) A four-quadrant multiplier core. with reference[20]

$$I_{C3} - I_{C4} = I_{C1} \tanh\left(\frac{v_1}{2V_t}\right) \tag{3.40}$$

$$I_{C5} - I_{C6} = I_{C2} \tanh\left(\frac{-v_1}{2V_t}\right) = -I_{C2} \tanh\left(\frac{v_1}{2V_t}\right) \tag{3.41}$$

$$i_o = (I_{C3} + I_{C5}) - (I_{C4} + I_{C6}) \tag{3.42}$$

$$=(I_{C1} - I_{C2})\, tanh\left(\frac{v_1}{2V_t}\right) \tag{3.43}$$

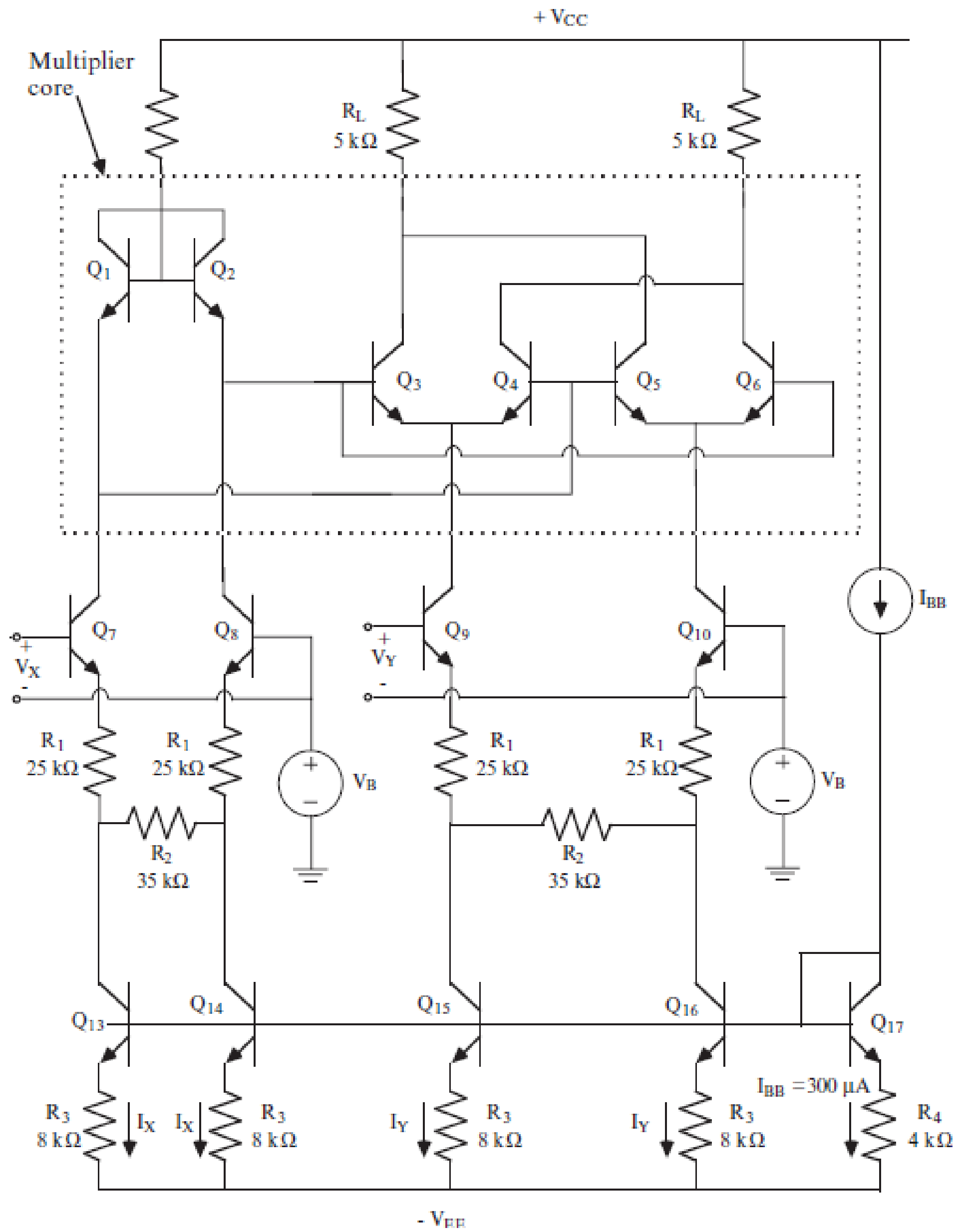


Figure 3.5. (b) Complete circuit of the multiplier. with reference[20]

For large values of the emitter feedback resistors,

$$I_{C1} - I_{C2} \approx \frac{2V_2}{R_E} \tag{3.44}$$

The differential-output voltage is

$$v_O = [V_{CC} - R_C(I_{C3} + I_{C5})] - [V_{CC} - R_C(I_{C4} + I_{C6})] \quad (3.45)$$

$$= -R_C i_0 = -kv_2 \tanh\left(\frac{v_1}{2V_t}\right)$$

Where

$$K = \frac{2R_C}{R_E} \quad (3.46)$$

The complete circuit becomes that of fig (3.5b).

$$v_O = -Kv_1v_2 \quad (3.47)$$

3.6 MOS Analog Multipliers

MOS devices can also be used to produce an analog multiplier because the different gain properties of the new devices, and the differing nonlinearities of the input and transfer characteristics may lead to modified performance .For designing of analog multiplier in BJT we use emitter coupled pair(ecp) while in MOSFET we use source coupled pair(scp). For MOS SCPs, a closed-form transfer function can be obtained only for operation in the MOS saturation region. the expressions for SCPs are not convenient to work with. It can be shown that linear multiplication is obtained for typical input voltage ranges Input predistortion circuitry and linear voltage-to-current converter sources can also be added to the MOS analog multiplier.

3.6.1 Gilbert cell using MOSFET (Two Quadrant Multiplier)

$$\frac{V_o}{V_i} = -g_m R_d \quad (3.48)$$

$$V_o = g_m R_d V_i \quad (3.49)$$

$$V_o = -f(V_c)\, R_d V_i \quad (3.50)$$

$$V_o = -\alpha V_c R_d V_i \quad (3.51)$$

Assuming $g_m = \alpha V_c$

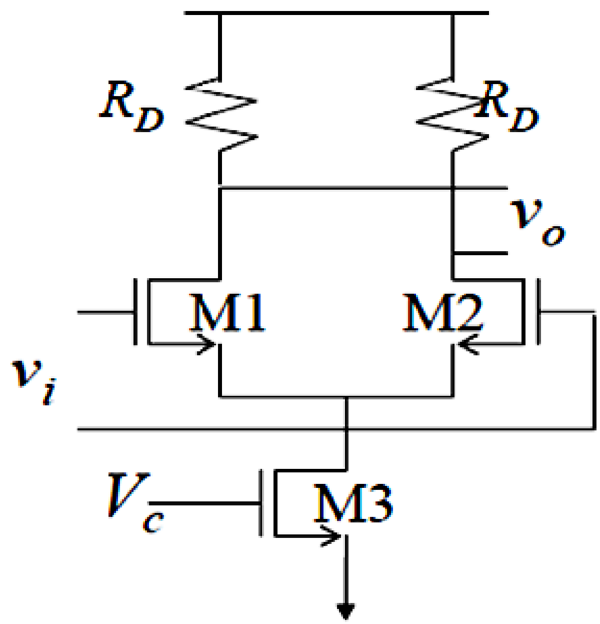


Fig 3.6 : Two Quadrant Multiplier using MOSFET

Above circuit also functions as Variable Gain Amplifier (VGA).

Transfer Function

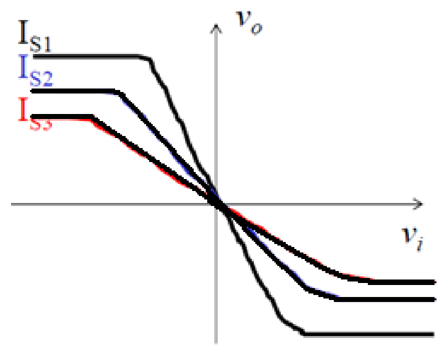


Fig 3.7 : Two Quadrant Multiplier Transfer Function

$$V_o = -\alpha V_c R_d V_i \tag{3.52}$$

It is two quadrant multiplier because V_c can't be negative.

Note: that V_c is the DC voltage and not the AC small signal voltage In order to build the 4 quadrant multiplier v_c should be AC voltage.

3.6.2 Gilbert Multiplier(Four Quadrant)

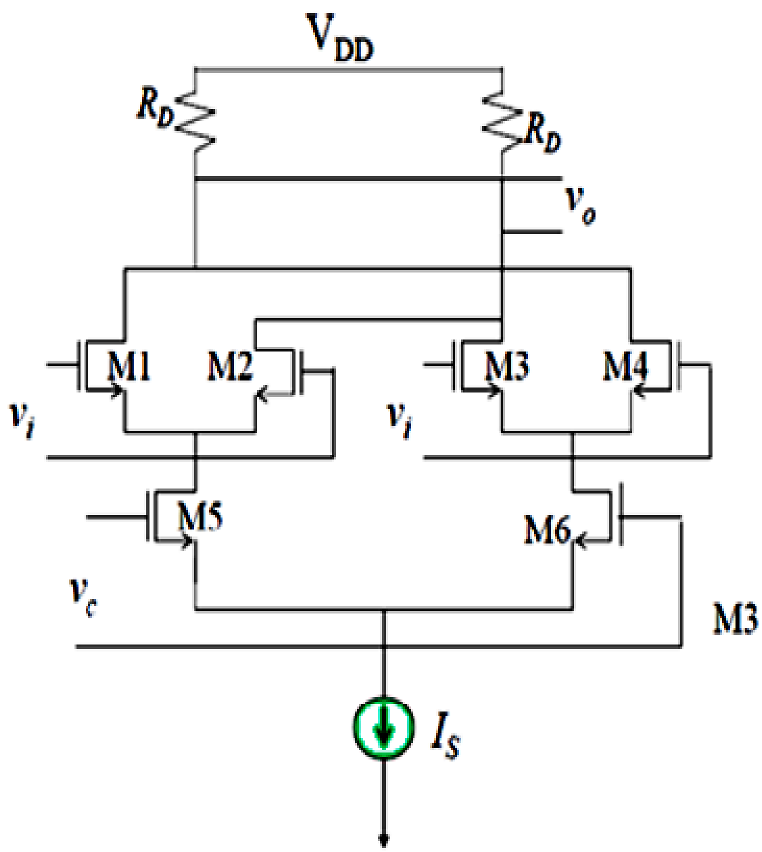


Figure 3.8 : Four Quadrant Multiplier using Gilbert cell

3.5 The Circuit Analysis

$$V_o = R_d(i_{d1} + i_{d4}) - R_d(i_{d2} + i_{d3}) \tag{3.53}$$

Case 1: $V_c = 0, V_i \neq 0; then\ i_{d1} = -i_{d4} and\ i_{d2} = -i_{d3} hence\ V_o = 0$

Case 2: $V_i - 0, V_c \neq 0; then\ i_{d1} - i_{d2} und\ i_{d3} - i_{d4} hence\ V_o - 0$

Case 3: $V_i \neq 0$, $V_c \neq 0$; then

$$\Delta g_{m1} = \Delta g_{m2} = \propto \frac{V_c}{2} \tag{3.54}$$

$$\Delta g_{m3} = \Delta g_{m4} = -\propto \frac{V_c}{2} \tag{3.55}$$

$$i_{d1} + i_{d4} = \frac{V_i}{2}(\Delta g_{m1} - \Delta g_{m4}) = \frac{V_i}{2}\left\{\frac{\propto V_c}{2} + \frac{\propto V_c}{2}\right\} = \frac{\propto V_i V_c}{2} \tag{3.56}$$

$$i_{d2} + i_{d3} = -\frac{V_i}{2}(\Delta g_{m2} - \Delta g_{m3}) = -\frac{V_i}{2}\left\{\frac{\propto V_c}{2} + \frac{\propto V_c}{2}\right\} = \frac{-\propto V_i V_c}{2} \tag{3.57}$$

$$V_o = -\alpha V_c R_d V_i \tag{3.58}$$

The circuit acts as four quadrant multiplier for small signal v_i, v_c **Error! Reference source not found.**.

Transfer Curves

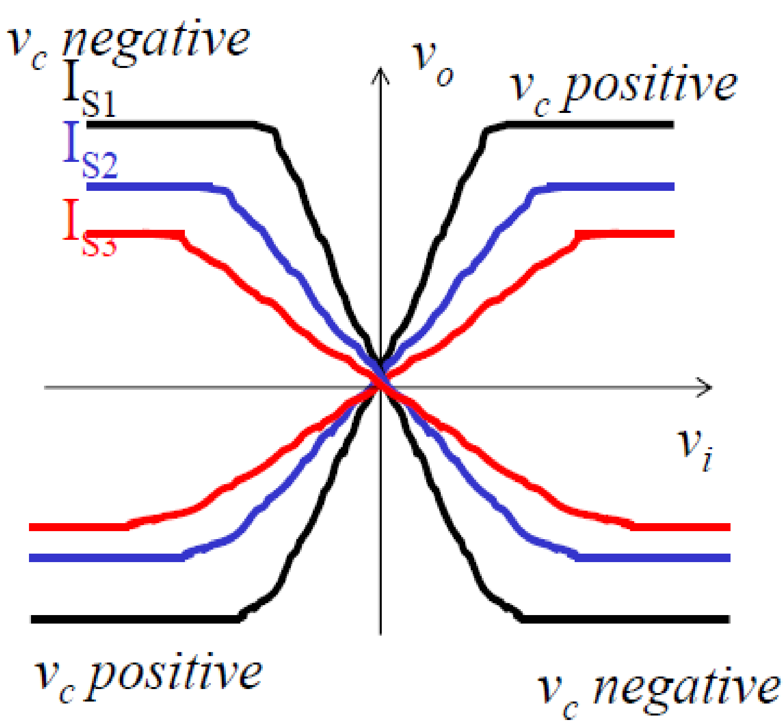


Figure 3.9 : four Quadrant Multiplier Transfer Function

3.7 A MOS Four-Quadrant Analog Multiplier Using the Quarter Square Technique

3.7.1 INTRODUCTION

The multiplier of this invention, including theoretical analysis, simulations experimental test results are disclosed in detail in a doctoral thesis by PenaFinol, "Analog Four-Quadrant Multiplier Using NMOS Integrated Circuit Technology," presented to the Georgia Institute of Technology on June 4, 1982. This circuit configuration for a four-quadrant analog multiplier in MOS integrated circnit technology is described. It is based on the “quarter-square algebraic identity” and uses differential summer and differential sqnaring stages. A 3-dB bandwidth of 5 MHz, a dynamic range of 87 dB, Typicaf power consumption is 10 mW. ANALOG multipliers are key building blocks in adaptive equalization, frequency translation, waveform generation, and other signal processing circuits. In the past, high-performance analog functions, such as multiplication, have been difficult to implement in MOS and VLSI technologies. In most applications, high accuracy and large dynamic range over a wide range of frequencies are required. In addition, small chip area and low power consumption are necessary for integration as part of a larger circuit. Here we discuss a MOS four-quadrant analog multiplier based upon the quarter-square algebraic identity.This circuit was fabricated in standard CMOS technology and achieves a better combination of linearity, bandwidth, and dynamic range than previous MOS multipliers. This circuit is suitable for fabrication as a stand-alone unit or as a building block for a more complex signal processor.

3.7.2 PRINCIPLE OF QUARTER-SQUARE MULTIPLIERS

The quarter-square algebraic identity can be written as

$$V_O = \frac{1}{4}[(V_1 + V_2)^2 - (V_1 - V_2)^2] = V_1 V_2 \quad (3.59)$$

The block diagram of a four-quadrant multiplier based on the quarter-square algebraic identity is shown above. In this technique multiplication is achieved in three steps.

1. The sum and differences of the two input signals are formed.
2. Then these results are squared.

3. Finally the difference of squares is obtained and scaled to get the desired result. Before MOS bipolar technology quarter-square multipliers made use of operational

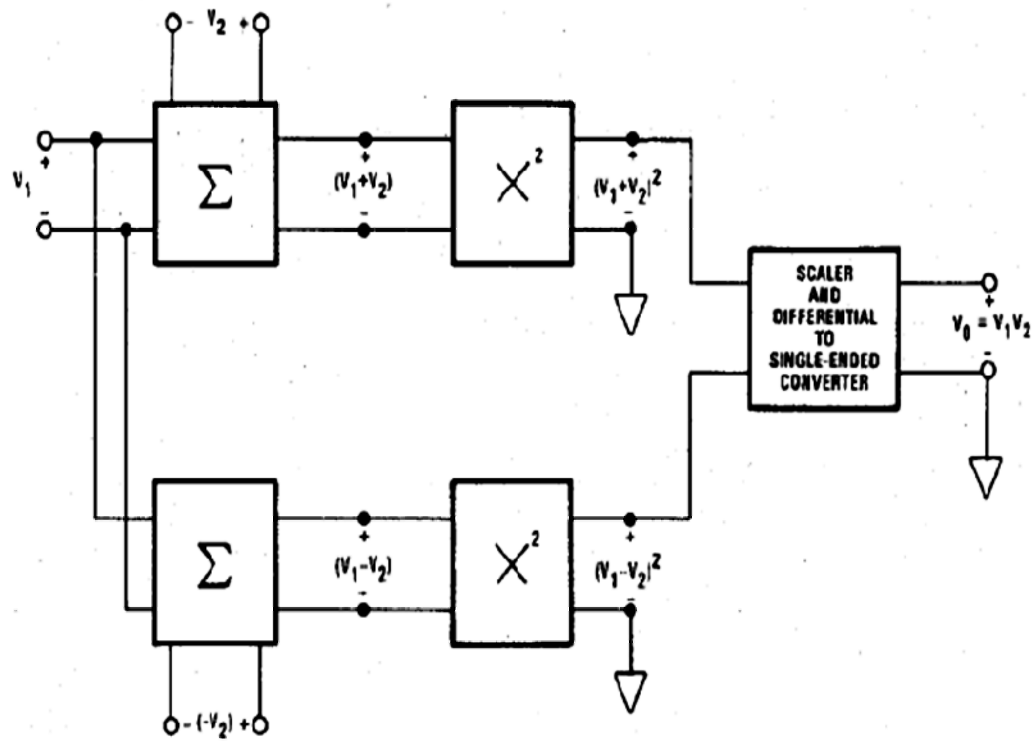


Figure.3.10: Block diagram of the quarter square based multiplication technique. with reference[5]

amplifiers to perform the sum and difference operations. A significant source of error was due to the discontinuities in a segmented parabolic transfer characteristic used to perform the squaring operation. Usually this square characteristic was realized by means of piecewise linear resistor-diode networks. For low errors, a large number of segments were required making this approach bulky and costly. Typical performance specifications were 2-MHz bandwidth and full-scale 10V. The quarter-square technique was replaced by the well known variable transconductance technique (which we already discuss it is devolped by B. gilbert) capable of providing bandwidths at least five times larger with the same order of magnitude accuracy.

At the present time, the variable transconductance multiplier is the dominant multiplying approach in bipolar integrated circuits but MOS technology is well suited for the realization of quarter-square based analog multipliers is due to the inherent square-law characteristic of the MOS device when operated in the saturation region. In implementing a MOS quarter-square multiplier, differential summing and differential squaring circuits have been devised. The differential squaring stage provides the needed parabolic transfer characteristic and the differential summing stage realizes the summing operations. The summing circuit is not limited by the gain-bandwidth product as would be the case if operational amplifiers were used. This results in much improved bandwidth compared to that of previous bipolar quarter-square multipliers

3.7.3 DIFFERENTIAL SUMMER CIRCUIT

A simplified version of the summer circuit is shown in Figure 3.11. It consists of two simple NMOS inverter stages M_l, M_2 and M_3, M_4. Input V_1 is applied to the driver device M_l, having M_2 as ac load, and appears inverted at the output. Input V_2 is applied to the inverter stage M_3, M_4 and appears at the output through M_2 acting as source follower. The sum of $V_1$and V_2occurring due to these two inverters appears then at the output. The drain current of the MOS device in saturation is given by equation (3.59)

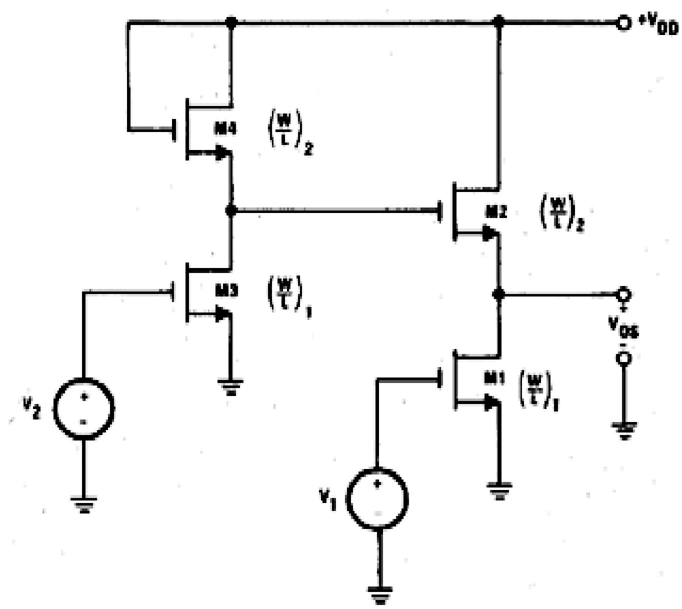


Figure 3.11: Simplified single ended summing circuit. with reference[5]

$$I_D = \frac{1}{2} K_P \left(\frac{W}{L}\right) (V_{GS} - V_{TH})^2 \quad (3.60)$$

Assume transistor as a long channel device where ,

$$K_p = \mu_0 C_{ox} \quad (3.61)$$

Considering the single NMOS inverter shown in Figure 3.11 and assuming that devices Ml and M2 are properly biased in the saturation region, it follows by using (3.11) that since $I_2 = I_1$

$$(w/l)_2(v_{gs2}-v_{th})^2=(w/l)_1(v_{gs1}-v_{th})^2 \tag{3.62}$$

$$v_2 = v_{gs2} = v_{th} + \left(v_{gs1} - v_{th}\right)\sqrt{\frac{\left(\frac{w}{l}\right)_1}{\left(\frac{w}{l}\right)_2}} \tag{3.63}$$

$$v_{gs2} = v_{th} + (v_1 - v_{th})\sqrt{\frac{\left(\frac{w}{l}\right)_1}{\left(\frac{w}{l}\right)_2}} \tag{3.64}$$

In fig(a) we can say that

$$V_{os} = v_{dd}-v_{gs4}-v_{gs2} \tag{3.65}$$

Since $v_{gs1}= v_1$, $v_{gs3} = v_2$ (3.66)

$$v_{os} = v_{dd} - v_{gs4} - \left[v_{th} + (v_1 - v_{th})\sqrt{\frac{\left(\frac{w}{l}\right)_1}{\left(\frac{w}{l}\right)_2}}\right] \tag{3.67}$$

As from single NMOS inverter circuit

$$v_{gs2} - v_{th} + (v_1 - v_{th})\sqrt{\frac{\left(\frac{w}{l}\right)_1}{\left(\frac{w}{l}\right)_2}} \tag{3.68}$$

Similarly, in Figure(3.11)

$$v_{gs4} = v_{th} + \left(v_{gs3} - v_{th}\right)\sqrt{\frac{\left(\frac{w}{l}\right)_1}{\left(\frac{w}{l}\right)_2}} \tag{3.69}$$

$$v_{gs4} = v_{th} + (v_2 - v_{th})\sqrt{\frac{\left(\frac{w}{l}\right)_1}{\left(\frac{w}{l}\right)_2}} \tag{3.70}$$

By eq. (3.67) and (3.70) we get

$$v_{os} - v_{dd} - v_{th} - \left(v_{gs3} - v_{th}\right)\sqrt{\frac{\left(\frac{w}{l}\right)_1}{\left(\frac{w}{l}\right)_2}} - \left[v_{th} + (v_1 - v_{th})\sqrt{\frac{\left(\frac{w}{l}\right)_1}{\left(\frac{w}{l}\right)_2}}\right]$$

$$v_{os} = v_{dd} + 2v_{th}\left[\sqrt{\frac{\left(\frac{w}{l}\right)_1}{\left(\frac{w}{l}\right)_2}} - 1\right] - \sqrt{\frac{\left(\frac{w}{l}\right)_1}{\left(\frac{w}{l}\right)_2}}(v_1 + v_2) \qquad (3.71)$$

$$v_{dcs} = v_{dd} + 2v_{th}\left[\sqrt{\frac{\left(\frac{w}{l}\right)_1}{\left(\frac{w}{l}\right)_2}} - 1\right] \qquad (3.72)$$

by equation (3.71) and (3.72)

$$v_{os} = v_{dcs} - \sqrt{\frac{\left(\frac{w}{l}\right)_1}{\left(\frac{w}{l}\right)_2}}(v_1 + v_2) \qquad (3.73)$$

The complete summer circuit is shown in above figure. It is fully differential version of the circuit shown in fig3.1 2that allow the cancellation of the DC voltage given by eq.(3.74)

$$v_{os-} = v_{dcs} - \sqrt{\frac{\left(\frac{w}{l}\right)_1}{\left(\frac{w}{l}\right)_2}}(v_1 + v_2) \qquad (3.74)$$

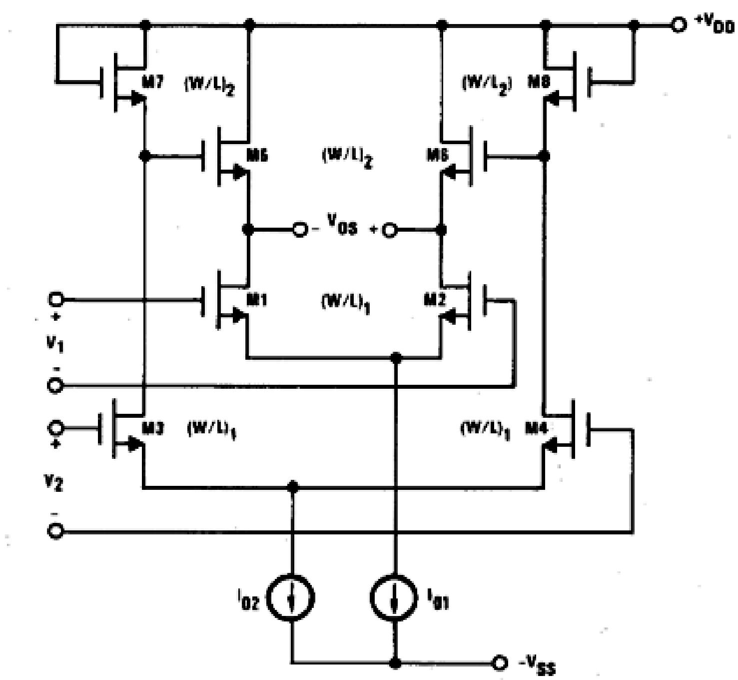


Figure 3.12: Complete fully differential summer circuit. with reference[5]

$$v_{os+} = v_{dcs} - \sqrt{\frac{\left(\frac{W}{l}\right)_1}{\left(\frac{W}{l}\right)_2}}(v_1 - v_2) \tag{3.75}$$

the differential output voltage V_{os}, as a function of the inputs $v_1$and v_2, is given by

$$v_{os} = v_{os+} - v_{os-}$$

$$v_{os} = 2\sqrt{\frac{\left(\frac{W}{l}\right)_1}{\left(\frac{W}{l}\right)_2}}(v_1 + v_2) \tag{3.76}$$

3.7.4 DIFFERENTIAL SQUARING CIRCUIT

The differential squaring circuit is shown in Figure 3.13. This configuration is basically a two-input NOR gate used in a differential pair fashion. When both devices M9 and M10 are biased in the saturation region, it can be shown that this circuit performs the squaring operation. The resistance R_p is used as a biasing resistor to insure that both transistors remain in their saturation regions over the maximum common-mode dynamic range. From the circuit shown in shown in Figure 5. the Single ended Output is related to the drain current of devices M9 and M10 by the loop equation

$$V_{osq} = V_{DD} - [I_9 + I_{10}]R_L \tag{3.77}$$

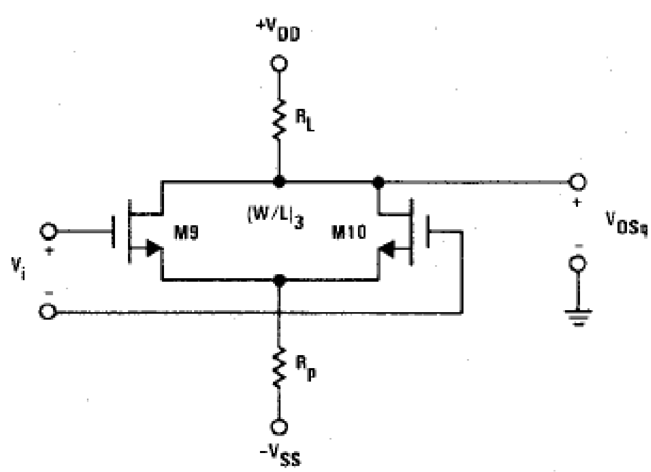


Figure 3.13: Single ended output, differential input squaring circuit. with reference[5]

Using (2), the single-ended output is related to differential input V_{in}

$$I_9 = \frac{1}{2} K_P \left(\frac{W}{L}\right)_3 \left(V_{gs9} - V_{th}\right)^2 \tag{3.78}$$

$$I_{10} = \frac{1}{2} K_P \left(\frac{W}{L}\right)_3 \left(-V_{gs9} - V_{th}\right)^2 \tag{3.79}$$

$$V_{osq} = V_{DD} - \frac{1}{2} K_P \left(\frac{W}{L}\right)_3 R_L \left[2V_{gs9}^2 + 2V_{th}^2\right] \tag{3.80}$$

$$V_{osq} = V_{DD} - \frac{2}{2} K_P \left(\frac{W}{L}\right)_3 R_L \left[V_{gs9}^2 + V_{th}^2\right] \tag{3.81}$$

$$V_{gs9} = \frac{V_i}{2} - V_s \tag{3.82}$$

V_s is the voltage at the common-source node.

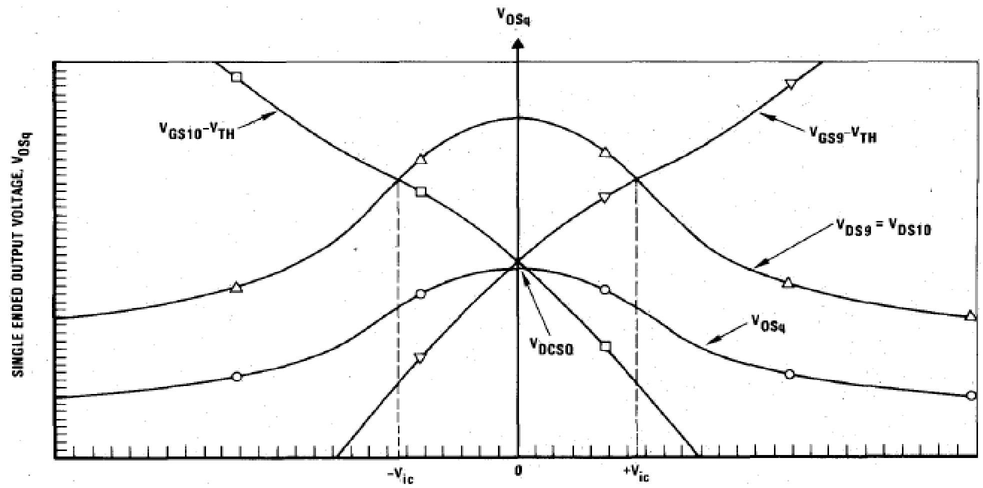
$$V_{osq} = V_{DD} - K_P \left(\frac{W}{L}\right)_3 R_L \left[\frac{V_i^2}{4} + V_{th}^2\right] \tag{3.83}$$

$$V_{osq} = -\frac{1}{4} K_P \left(\frac{W}{L}\right)_3 R_L V_i^2 + V_{DD} - K_P \left(\frac{W}{L}\right)_3 R_L V_{th}^2 \tag{3.84}$$

$$V_{osq} = -\frac{1}{4} K_P \left(\frac{W}{L}\right)_3 R_L V_i^2 + V_{DCSQ} \tag{3.85}$$

Where dc term is

$$V_{DCSQ} = V_{DD} - K_P R_L \left(\frac{W}{L}\right)_3 (V_S + V_{th})^2 \tag{3.86}$$



Differential input voltage, v_i

Figure 3.14.(a) spice simulation of the dc transfer characteristics for the squaring circuit. with reference[5]

Equation (3.86) is valid only for a ‘limited range of input voltages. It was derived assuming that both devices M9 and M10are biased in the saturation region. As $|V_i|$ increases, one device enters the triode region while the other is turned off. Figure 3.14 shows a SPICE simulation of V_{osq} for a wide range of V_i. The critical input voltage, designated as V_{ic} represents the maximum differential input voltage that can be applied to the circuit

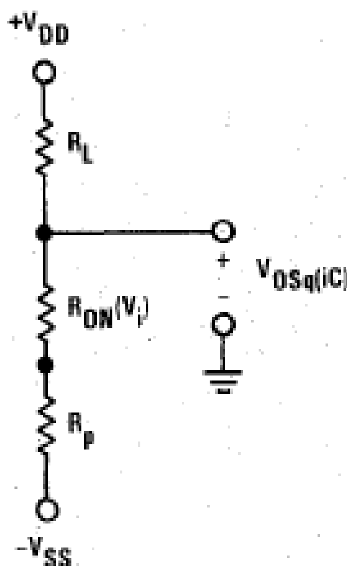


Figure 3.14(b):. resulting squaring circuit for $V_i > V_{ic}$with reference[5]

Whenever $|V_i| \geq |V_{ic}|$ the squaring circuit no longer performs the squaring operation, and it can be modeled by the simple resistive voltage divider. circuit shown in Figure 3.14. The output voltage for $|V_i| \geq |V_{ic}|$ can be obtained from Figure 3.14(b) and is given by

$$V_{OS(IC)} = \frac{(R_{ON}(V_i)+R_P)V_{DD}-R_L V_{SS}}{(R_{ON}(V_i)+R_P+R_L)} \quad (3.87)$$

where, depending on the polarity of V_i , $R_{ON}(V_i)$ represents the triode resistance of either device M9 or M10. $R_{ON}(V_i)$ decrease nonlinearity as $|V_i|$ is increase causing the nonlinear behavior of V_{Osq} for $|V_i| \geq |V_{ic}|$ as was shown in Figure 3.14(b). A first-order expression for ~c can be obtained from the circuit shown in Figure 3.12. Using the triode region defining inequality $V_{ds} > V_{gs} - V_{th}$ [3.89], it follows that

$$V_{ic} = \pm 2[V_{dd} + V_{th} - R_L I_{ic}] \quad (3.88)$$

where the quantity l_{ic} is given by

$$I_{ic} = \frac{\left[K_P\left(\frac{W}{L}\right)_3 (V_{SS}+V_{DD})(R_L+R_P)+1\right] - \sqrt{2K_P\left(\frac{W}{L}\right)_3 (V_{SS}+V_{DD})(R_L+R_P)+1}}{K_P\left(\frac{W}{L}\right)_3 (R_L+R_P)^2} \quad (3.89)$$

3.7.5 QUARTER-SQUARE MOS ANLOG MULTIPLIER

The output voltage given by (3.89) is the single-ended square of the differential input . Since two squaring circuits are needed in order to obtain the square of the sum and difference of the input signals, two mirror image squaring circuits are used as shown in Figure 3.15. Here the same biasing resistor Rp is used for both circuits to insure effective cancellation of the dc term, V_{DCSQ}, present at both single-ended outputs. Since the output voltages of each squaring circuit are single-ended, (1) is realized because the differential signal between their outputs will be the difference of the squared sums. Thus, for the circuit shown in Figure 3.15, the differential output is related to the

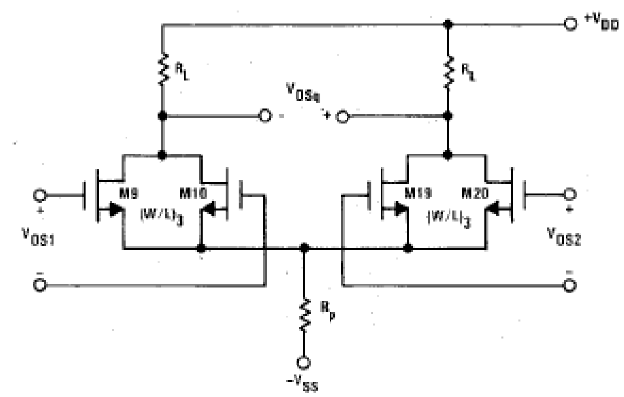


Figure 3.15: Double differential input, differential output squaring circuit. with reference[5]

Devices M9, M10 and M19, M20 together with resistors R_L form the squaring circuits corresponding to Figure 3.15. The sum and difference outputs from the summer stages are then applied to the squaring circuits. The differential output signal VO is thus the product of inputs VI and V2times a scaling factor. The analytic expression for the transfer characteristic of this circuit can be obtained as follows.The outputs from the summers are given by (6) and by

$$V_{osq} = V_{osq+} - V_{osq-}$$

From eq(3.85) we put the value of V_{osq}

$$V_{osq} = V_{DCSQ} - \frac{1}{4}K_P\left(\frac{W}{L}\right)_3 R_L V_{OS1}^2 - \left[V_{DCSQ} - \frac{1}{4}K_P\left(\frac{W}{L}\right)_3 R_L V_{OS2}^2\right]$$

$$V_{osq} = \frac{1}{4}K_P\left(\frac{W}{L}\right)_3 R_L\left[V_{OS2}^2 - V_{OS1}^2\right] \quad (3.90)$$

$$V_{OS1} = \sqrt{\frac{\left(\frac{W}{L}\right)_1}{\left(\frac{W}{L}\right)_2}(V_1 + V_2)^2} \quad (3.91)$$

$$V_{OS2} = \sqrt{\frac{\left(\frac{W}{L}\right)_1}{\left(\frac{W}{L}\right)_2}(V_1 - V_2)^2} \quad (3.92)$$

By(3.90)(3.91)and(3.92)we get

$$V_{osq} = K_p R_L \left(\frac{W}{L}\right)_3 \frac{\left(\frac{W}{L}\right)_1}{\left(\frac{W}{L}\right)_2} V_1 V_2 \tag{3.93}$$

The complete multipliers shown in Figure 3.16. Devices Ml – M8 and M11 – M18 form the two differential summing pairs, corresponding to Figure 4, and are biased by current sinks M24, M25 and M21, M22, respectively .Input V2 is applied simultaneously to the input of one of the summing circuits and to the input of an inverting unity gain differential stage formed by devices M29- M32 and biased by M33 which is needed to realize the difference operation.

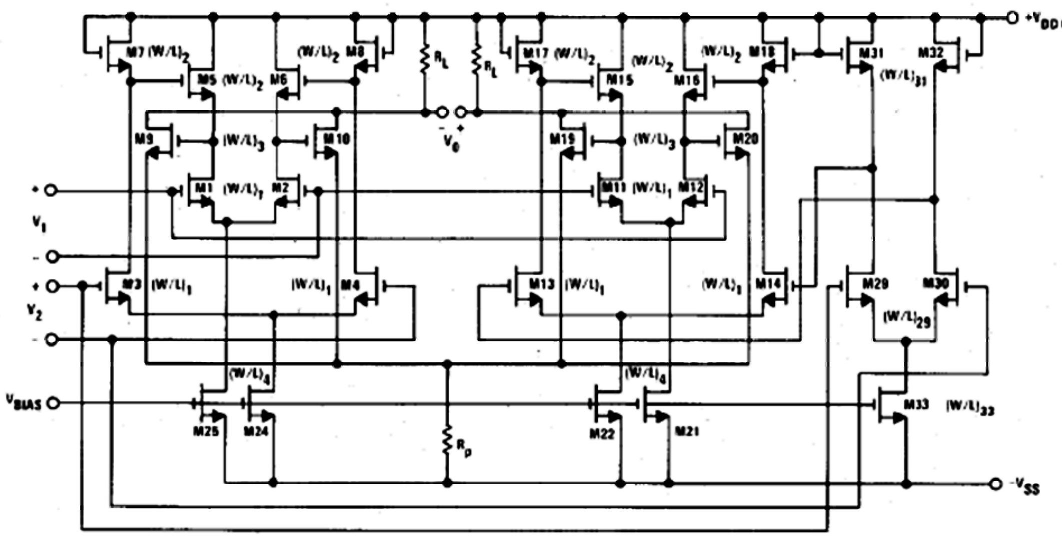


Figure 3.16: complete circuit schematic for the MOS quarter square analog multiplier. with reference[5]

$$V_{osq} = K_p R_L \left(\frac{W}{L}\right)_3 \frac{\left(\frac{W}{L}\right)_1}{\left(\frac{W}{L}\right)_2} V_1 V_2$$

The range of input voltages over which multiplication is achieved is determined by the squaring circuit and is given by

$$|V_{ic} \pm V_{ic}| \leq \frac{V_{ic}}{\left(\frac{\left(\frac{W}{L}\right)_1}{\left(\frac{W}{L}\right)_2}\right)^{1/2}} \tag{3.94}$$

where V_{ic} is given by (3.94). A central objective in the design of the circuit is to keep all devices biased in saturation for the largest possible range of input voltages. Care must be exercised in the design of both the biasing current sinks for the summing stages and the biasing resistor R_P for the squaring stage. Typically, common-mode and gain-stage considerations limit the voltage drop across load devices M5– M8 and M15– M18of the summing stages. The usual requirement of a large biasing current for improved bandwidth would severely restrict the design of the stage. However, gain is not a dominant design parameter of the summing stage, and it can be adjusted elsewhere. The gain of the summing circuits is less than 1. Thus, a large aspect ratio can be used for the load devices. This permits a large biasing current for increased bandwidth and a low voltage drop across the load devices, reducing the sensitivity of the stage to common-mode signals.

3.8 CAMPARISION BETWEEN QUARTER SQUARE AND VARIABLE TRANSCONDUCTANCE TECHNIQUES

This invention generally relates to an analog four quadrant multiplier using MOS integrated circuit technology, and more particularly relates to such an analog multiplier based on the quarter-square algebraic identity and utilizing low-gain differential summer and differential squaring circuits.

3.8.1 Description of the Prior Art

1. There are several prior art methods used to perform analog multiplcation, namely electromechanical, magnetic (magnetoresistance, Hall effect), time-division, triangle averaging, log/antilog, quarter-square, variable transconductance and those based on A/D and D/A conversion techniques. Of these techniques, only the quarter-square and variable transconductance techniques having bandwidths above 1 MHz as does the invention disclosed herein. The quarter-square is the more accurate method. The variable transconductance has a larger bandwidth, but the quarter-square possesses one-half an order of magnitude more accuracy, typically 0.25%. At the present time, the 0.25% accuracy is obtained only through the use of expensive discrete circuitry. The design of a monolithic quarter-square multiplier with comparable or better accuracy to bandwidth ratio, would represent a significant contribution in the area of analog signal processing.

2. Traditionally, these multipliers have been implemented using bipolar technology. This technology has been the dominant one in the analog domain. Higher levels of monolithic integration are combining analog and digital circuits on the same MOS/LSI chip. Currently, analog integrated circuits are being fabricated using the same MOS technology employed in the realization of digital circuits. This circuit was fabricated in standard CMOS technology and achieves a better combination of linearity, bandwidth, and dynamic range than previous MOS multipliers.
3. The conventional method of performing the multiplication function based on the variable transconductance technique so far has been the only one which has been integrated in monolithic form. This method uses the inherent close matching and variable transconductance of bipolar junction transistor monolithic differential amplifiers. The circuit configuration for this method is the well-known Gilbert multiplier cell
4. $I_2/I_1=I_6/I_8=I_5/I_7$ (3.95)
5. Equation (3.95) is obtained assuming perfectly matching transistors and resistors and infinite common emitter current gain (β) of the transistors. Thus, monolithic integrated circuit technology should be used in the fabrication of the variable transconductance multiplier. However, a small but finite mismatching will exist in the emitter areas, ohmic resistances, and β's. This mismatch introduces nonlinearities and offset voltages and ultimately limits the accuracy of this compensated variable transconductance multiplier. Improved processing of device matching and laser trimming thin film resistors has produced high accuracies of about 1%. However, the extra processing steps increase considerably the cost.
6. Because of these small-signal level constraints, the useful range for good linearity is severely limited. A nonlinear cancellation approach similar to that used for the bipolar multiplier is not suitable for MOSFET multiplier because of the different type of nonlinearity associated with MOSFETs. MOSFETs have a square law current-voltage dependency while bipolar junction transistors (BJTs) have an exponential relationship. Another shortcoming associated with the NMOS multiplier is that large values of transconductance are required for proper operation of the circuit. The transconductance of a MOS transistor operating in the saturation region is derived as shown above where I_D is the drain current. Thus, in order to significantly increase the transconductance of the MOS devices, the

aspect ratio (W/L) will have to be greatly increased as well as the drain current, I_D . However, increasing these two variables causes new problems.

3.8.2 Over edge of Quarter square multiplier using NMOS over Variable transconductance multiplier

1. Accordingly, one object of this invention is to provide a new and improved NMOS IC quarter-square multiplier wherein the performance of the NMOS quarter square multiplier is at least comparable to that of its bipolar variable transconductance counterpart.
2. Another object is to provide an NMOS multiplier which compensates for the nonlinearities of the basic cell and low values of the MOS transistor transconductances
3. Yet another object is to provide an all-NMOS four-quadrant multiplier which can easily be integrated to achieve low cost in quantity production.
4. The body effect can be explained as follows. In discrete MOS transistors the source and substrate are tied together causing zero substrate-to-source voltage. However, in a monolithic circuit, all of the devices share the same substrate. Thus, in designing NMOS circuits a tradeoff must be made between the minimum allowable body effect and the required threshold voltage for proper circuit operation.
5. Instead of above advantages there is one main disadvantage associated with the all-NMOS circuit is their smaller dynamic range .

VOLTAGE-MODE VERSUS CURRENT-MODE

The information processed by lumped electric networks can be represented by either the nodal voltages or branch currents of the networks. The different design focuses of voltage-mode and current-mode circuits, arising from the intrinsic characteristics of nodal voltages and branch currents, result in distinct design principles. The former are referred to as voltage-mode circuits whereas the latter are known as current-mode circuits. Voltage-mode circuits have received a much broader attention The reasons for such a popularity of voltage mode are

1. The nodal voltage of electric networks can be measured conveniently using voltmeters without modifying the topology and affecting the operation of the networks. On the contrary, the measurement of the branch current of the networks are less convenient and often requires a change of the configuration of the networks or additional circuitry,

2. The infinite impedance looking into the gate of MOS transistors makes these devices an ideal choice for the realization of voltage-mode circuits, especially in cascade configurations, such as multi-stage voltage amplifiers,

3. The ease to obtain a high voltage gain of voltage-mode circuits using techniques such as cascodes and regulated cascodes.
4. But now a day's current mode designing is more prefer current-mode circuits offer comparable bandwidth to that of high bandwidth voltage-mode circuits .The usefulness of CMOS current-mode circuits in combating the difficulties arising from the reduction of the supply voltage and the increase in the operation speed.

Chapter4

DESIGN OF MULTIPLIER

4.1 INTRODUCTION

In this chapter a new approach to designing a differential input multiplier configuration is presented. This multiplier works in all four quadrants; i.e., both the inputs can be positive or negative. The approach here is unique in that we attempt to use an all NMOS voltage-mode four quadrant analog multiplier based on a basic NMOS differential amplifier that can produce the output signal in voltage form without using resistors is presented**.** Usually, the variable transconductance technique which operates on Gilbert's translinear circuit is widely used for the design of multiplier circuits in Bipolar and CMOS technologies region [1], [2], [3], The other approaches in CMOS technology are that based on square-law characteristics of MOS transistor which are biased in saturation region [4], [5], [6], and that based on the current voltage characteristics of MOS transistor in the nonsaturation region [7]. Unfortunately, all the mention techniques require resistors to obtain the output signal in voltage form. The use of resistors may require external resistors, or occupy large chip area to implement in IC form and also cause of the multiplier frequency degradation . The multiplier proposed here uses the non-linear characteristic of the NMOS differential amplifier based upon the quarter square algebraic identity. But, however, the proposed circuit also does not require resistors to obtain the output signal in voltage form. quarter square technique without resistor differential pair for multiplier implementation.. This voltage mode analog multiplier has many application , for examples, automatic gain control, frequency translation, waveform generation, linear modulation, neural networks, and other signal processing circuits.

4.2 CIRCUIT DESCRIPTIONS

The basic principle of the proposed multiplier is based on the quarter-square algebraic identity, For this operation, the multiplier needs the summing and squarer circuits. The multiplier is achieved in three steps. First, the sum and difference of the two input voltages are formed.

$$(V_1+V_2)^2-(V_1-V_2)^2 = 4V_1V_2 \quad (4.1)$$

Then, these summing and differencing results are squared. Finally, the multiplication is obtained by subtracting the square of the difference from the square of the sum of the two inputs.

4.2.1 Summing Circuit

Figure (4.1) shows the fully differential summing circuit that based on basic MOS differential pairs M_1-M_4 and the active loads M_5-M_6. Assuming that transistors M_1-M_4 are matched with transconductance parameter K_1 and transistors M_5-M_6 are matched with K_5. If all devices operate in saturation region, applying the differential input voltages V_1 and

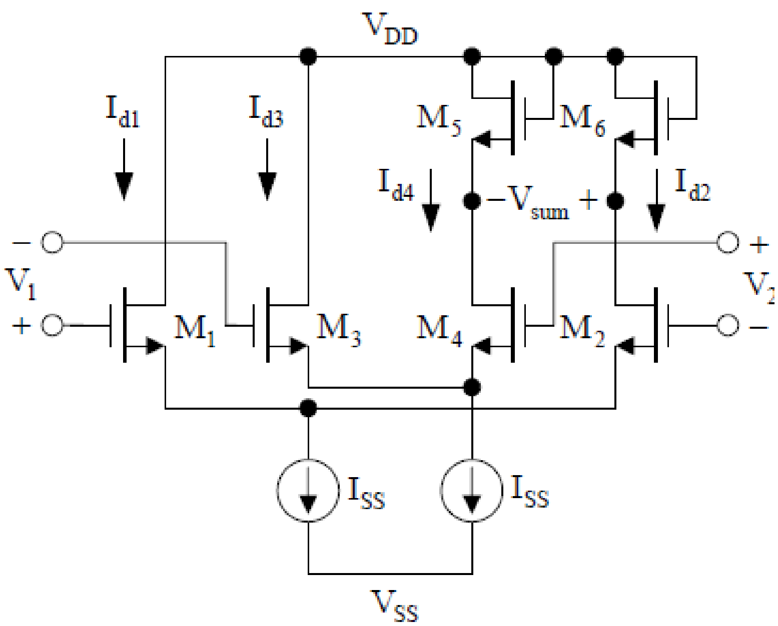


Figure 4.1: Fully differential summing circuit. with reference[13]

V_2, the loop equation of the gate-to-source voltages of the two differential amplifiers M_1-M_2 and M_3-M_4 can be written as

$$V_{gs1} - V_{gs2} = V_{g1} - V_S - V_{g2} + V_S \tag{4.2}$$

$$= V_{g1} - V_{g2} \tag{4.3}$$

$$V_{gs1} - V_{gs2} = \frac{V_1}{2} - \left(\frac{-V_2}{2}\right) \tag{4.4}$$

$$V_{gs1} - V_{gs2} = \left(\frac{V_1}{2} + \frac{V_2}{2}\right) \quad (4.5)$$

$$V_{gs3} - V_{gs4} = V_{g3} - V_{g4} \quad (4.6)$$

$$V_{gs3} - V_{gs4} = \frac{-V_1}{2} - \left(\frac{V_2}{2}\right) \quad (4.7)$$

$$V_{gs3} - V_{gs4} = -\left(\frac{V_1}{2} + \frac{V_2}{2}\right) \quad (4.8)$$

Where V_{gs1} and V_{gs4} are the gate to source voltage of the transistors respectively $M_1$and M_4. So our input of each differential pair is$+\left(\frac{V_1}{2} + \frac{V_2}{2}\right)$ and $-\left(\frac{V_1}{2} + \frac{V_2}{2}\right)$. Since all transistors are in saturation so voltage and current equation can be written in this form

$$I_d = K(V_{gs} - V_{th})^2, V_{gs} = V_{th} + \sqrt{\frac{I_d}{K}}$$

Replace V_{gs} value in above equation. We can write

$$\left(\frac{V_1}{2} + \frac{V_2}{2}\right) - \sqrt{\frac{I_{d1}}{K_1}} - \sqrt{\frac{I_{d2}}{K_1}} \quad (4.9)$$

$$-\left(\frac{V_1}{2} + \frac{V_2}{2}\right) = \sqrt{\frac{I_{d3}}{K_1}} - \sqrt{\frac{I_{d4}}{K_1}} \quad (4.10)$$

Subtracting (4.9) by (4.10) we get

$$(V_1 + V_2) = \frac{1}{\sqrt{K_1}}\left(\sqrt{I_{d1}} - \sqrt{I_{d2}} - \sqrt{I_{d3}} + \sqrt{I_{d4}}\right) \quad (4.11)$$

$$(V_1 + V_2) = \frac{1}{\sqrt{K_1}}\left[\left(\sqrt{I_{d1}} + \sqrt{I_{d4}}\right) - \left(\sqrt{I_{d2}} + \sqrt{I_{d3}}\right)\right] \quad (4.12)$$

Considering from the two differential amplifiers M_1-M_2 and M_3-M_4 in Figure(4.1), we can see that $I_{d1}=I_{d4}$ and $I_{d2}=I_{d3}$ then, equ. (4.5) can be rearranged and rewritten in the form of

$$(V_1 + V_2) = \frac{2}{\sqrt{K_1}}\left(\sqrt{I_{d4}} - \sqrt{I_{d2}}\right) \quad (4.13)$$

$$\sqrt{I_{d4}} - \sqrt{I_{d2}} = \sqrt{K_1}\left(\frac{V_1}{2} + \frac{V_2}{2}\right) \quad (4.14)$$

From the output loop equation

$$V_{sum} = V_{gs5} - V_{gs6} \tag{4.15}$$

$$V_{sum} = V_{g5} - V_{s5} - V_{g6} + V_{s6} \tag{4.16}$$

Since $V_{g5} = V_{g6}$ (4.17)

$$V_{sum} = V_{s6} - V_{s5} = V_{sum+} - V_{ssum-} \tag{4.18}$$

We can write current voltage relation for transistor M_5, M_6 from equation (4.9) and (4.10)

$$V_{gs5} - V_{gs6} = \sqrt{\frac{I_{d5}}{K_5}} - \sqrt{\frac{I_{d6}}{K_6}} \tag{4.19}$$

As we already mentioned transistor M_5 and M_6 are matched transistors therefore $K_5 = K_6$. From the output loop equation

$$V_{sum} = V_{gs5} - V_{gs6} = \frac{\sqrt{I_{d5}} - \sqrt{I_{d6}}}{\sqrt{K_5}} \tag{4.20}$$

Drain current $I_{d5} = I_{d4}$ and $I_{d2} = I_{d6}$ the output voltage Vsum is given by

$$V_{sum} = \left(\frac{\sqrt{I_{d4}} - \sqrt{I_{d2}}}{\sqrt{K_5}}\right) \tag{4.15}$$

By substituting (4.7) into (4.6) we get

$$V_{sum} = \sqrt{\frac{K_1}{4K_5}}(V_1 + V_2) \tag{4.21}$$

Maximum input Voltage range of circuit is

$$\left(\frac{V_1}{2} + \frac{V_2}{2}\right) \leq \sqrt{\frac{I_{ss}}{K}} \tag{4.22}$$

4.2.2 Squaring Circuit

Figure(4.2) shows the configuration of the differential-input voltage squaring circuit that modified from a basic NMOS differential pair, where the transistors M_7-M_9 are bias in saturation region. If the differential voltage V_d with the same common – mode V_c is applied, the drain currents of the transistors can be given by

$$I_{d7} = K_7\left(V_c + \frac{V_d}{2} - V_{sq} - V_{th}\right)^2 \tag{4.23}$$

$$I_{d8} = K_8\left(V_c - \frac{V_d}{2} - V_{sq} - V_{th}\right)^2 \tag{4.24}$$

$$I_{d9} = K_9\left(V_{g9} - V_{ss} - V_{th}\right)^2 \tag{4.25}$$

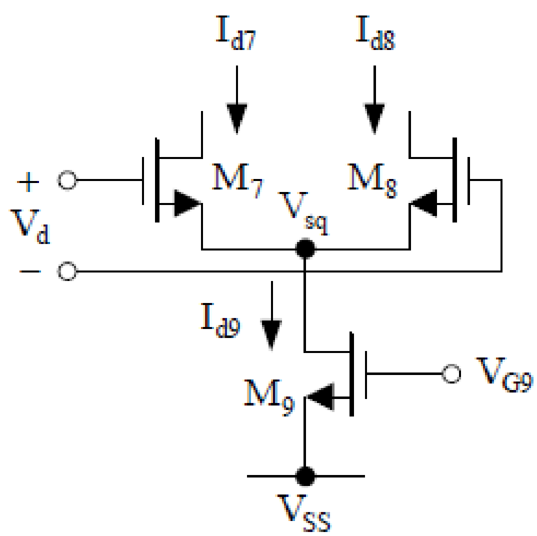


Figure 4.2: Squaring circuit based on differential pair. with reference[13]

$$I_{d7} + I_{d8} = I_{d9} \tag{4.26}$$

Where K_7, K_8 and K_9 are transconductance parameter of the transistor M_7 – M_9, and V_{th} is threshold voltage of the transistor, respectively. Let M_7 and M_8 are identical, and the aspect ratio of M_9 is twice that of M_7 and M_8. Substituting (23), (24), (25) into (26), as

$$I_{d7} + I_{d8} = I_{d9} \tag{4.27}$$

$$K_7\left(V_c+\frac{V_d}{2}-V_{sq}-V_{th}\right)^2+K_8\left(V_c-\frac{V_d}{2}-V_{sq}-V_{th}\right)^2$$

$$=K_9\left(V_{g9}-V_{th}\right)^2 \quad (4.28)$$

Where $K_7=K_8=\frac{K_9}{2}$ according to our assumption so above equation reduced as

$$\left(V_c+\frac{V_d}{2}-V_{sq}-V_{th}\right)^2+\left(V_c-\frac{V_d}{2}-V_{sq}-V_{th}\right)^2=2\left(V_{g9}-V_{th}\right)^2 \quad (4.29)$$

$$V_{sq}=V_c-V_{th}-\sqrt{\left(V_{g9}-V_{th}\right)^2-\left(\frac{V_d}{2}\right)^2} \quad (4.30)$$

If the approximation of the form $\sqrt{1+x}\cong\left(1+\frac{x}{2}\right)$ for mod(x) <<1 is employed, (4.14) can be written as

$$V_{sq}=V_c-V_{th}-\left(V_{g9}-V_{th}\right)\sqrt{1-\frac{\left(\frac{V_d}{2}\right)^2}{\left(V_{g9}-V_{th}\right)^2}} \quad (4.31)$$

$$V_{sq}=V_c-V_{th}-\left(V_{g9}-V_{th}\right)\left(1-\frac{\left(\frac{V_d}{2}\right)^2}{2\left(V_{g9}-V_{th}\right)^2}\right) \quad (4.32)$$

$$V_{sq}=V_c-V_{g9}+\frac{V_d^2}{8\left(V_{g9}-V_{th}\right)} \quad (4.33)$$

Equation (4.33) indicated that the output voltage V_{sq} is related to the square of the differential input voltage V_d. Therefore, the source-coupled pair circuit as shown in Figure (4.2) can be used as a squaring circuit for quarter-square multiplier. However, this relation is valid for the case that all transistors are operated in the saturation region.

DC transfer characteristics of squaring circuit

For testing squaring circuit if we apply DC voltage at differential input port which is vary

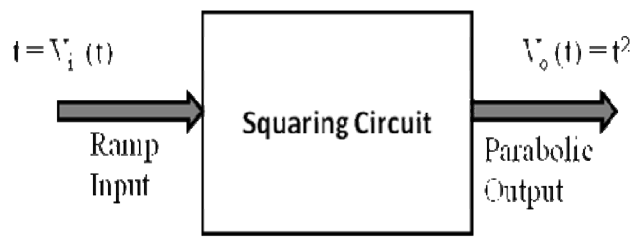


Figure 4.3: squaring circuit

in ramp form with respect to time then we get parabola type waveform at output port as shown in Figure(4.3).

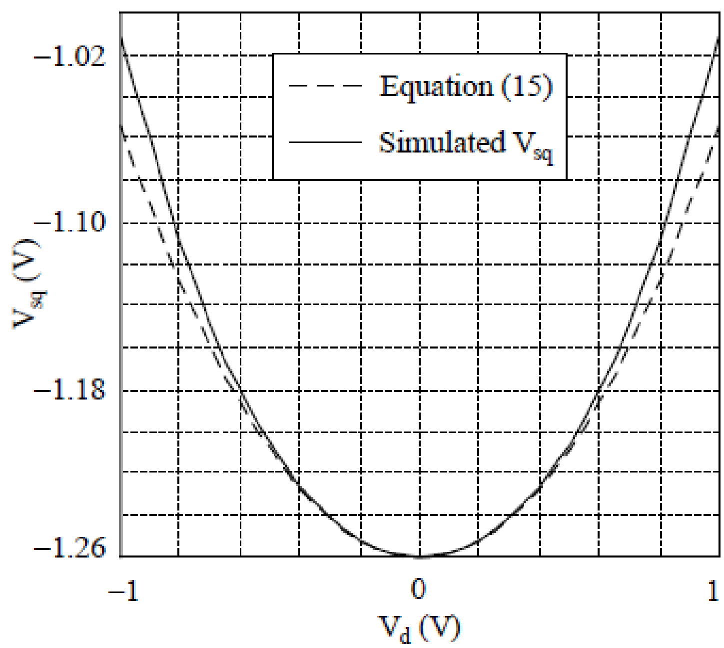


Fig 4.4: DC characteristic of the circuit. with reference[13]

4.2.3 Fully Differential Amplifier

By employing the squaring circuit of Figure (4.2) and the summing circuit of Figure (4.3), the fully differential all NMOS four-quadrant analog multiplier can be realized. From (8) and (15), the output voltage V_o of the multiplier can be derived as

$$V_d = V_{sum} = \sqrt{\frac{K_1}{4K_5}}(V_1 + V_2) \tag{4.33}$$

$$V_{sq} = V_c - V_{g9} + \frac{V_d^2}{8(V_{g9}-V_{th})} \tag{4.34}$$

by (4.33) and (4.34) we get

$$V_{sq} = V_c - V_{g9} + \frac{\frac{K_1}{4K_5}(V_1+V_2)^2}{8(V_{g9}-V_{th})} \tag{4.35}$$

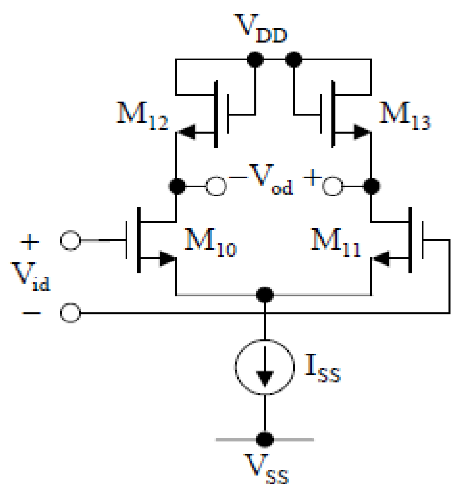


Figure 4.5: NMOS voltage amplifier. with reference[13]

$$V_o = V_{sq+} - V_{sq-} \tag{4.36}$$

by equation (4.35) and (4.36) the output voltage V_o of the multiplier can be expressed as

$$V_0 = \frac{\frac{K_1}{4K_5}}{8(V_{g9}-V_{th})}\left[(V_1+V_2)^2 - (V_1-V_2)^2\right] \tag{4.37}$$

$$V_0 = \frac{\frac{K_1}{K_5}}{8(V_{g9}-V_{th})} V_1 V_2 \tag{4.38}$$

Equation (4.38) shows that the output voltage V_o is in the form of multiplication of the two input voltages and it should be noted that while other multiplier need resistors to obtain an output in voltage form, but this circuit achieves the output voltage without resistors from (4.38), the gain factor of multiplier can be controlled by the transconductance parameters K_1, K_5 and the gate voltage V_{G9}.

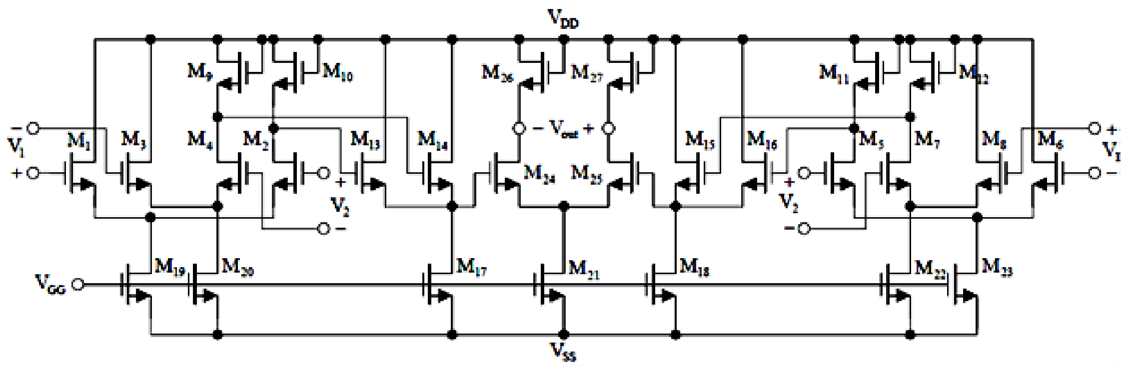


Figure 4.6: NMOS voltage mode multiplier. with reference[13]

Figure (4.6) shows the complete voltage-mode multiplier circuit. Transistors M_1- M_{12} form the summing circuits that produce the output voltage in term of the sum and difference of input signals. The sum and difference outputs from these stages are applied to the squarer circuits formed by M_{13}-M_{18} and M_{24}- M_{27} form NMOS voltage amplifier, where the transistors M_{19}-M_{23} provide bias currents ISS for summing stages and amplifier circuit. Finally, the output voltage of the multiplier can be written as

$$V_{out} = \left[\frac{\frac{K_1 K_{24}}{K_9 K_{26}}}{o(V_{g9}\ \ V_{th})} \right] V_1 V_2 \qquad (4.39)$$

Table 4.1: Transistor Sizing

S.No.	Transistor Name	Size
1.	$(MN)_1 - (MN)_8$	W=4.35,L=1.4
2.	$(MN)_9 - (MN)_{12}$	W=0.86772,L=1.4
3.	$(MN)_{13} - (MN)_{16}$	W=32,L=1.4
4.	$(MN)_{17} - (MN)_{18}$	W=64,L=1.4
5.	$(MN)_{19}$,$(MN)_{20}$, $(MN)_{22}$	W=80,L=1.4
6.	$(MN)_{24}$– $(MN)_{25}$	W=7,L=1.4
7.	$(MN)_{26} - (MN)_{27}$	W=1.9,L=21
8.	$(MN)_{17} - (MN)_{18}$	W=64,L=1.4
9.	$(MN)_{21}$	W=64,L=1.4

Chapter 5

Simulation Results and Layout

5.1 Introduction

In this chapter the schematic of the analog multiplier circuit has been tested for DC, AC and transient response. The simulations of this differential multiplier were done using **ELDO** simulator in Mentor Graphics with 0.35μm technology parameters. The simulated NMOS multiplier schematic is shown in **figure 4.6.** A higher value of input voltage gives better bandwidth to analog multiplier but at the expense of power consumption. Therefore an optimum value of input voltage range (±.66V) is chosen to give good bandwidth as well as low power consumption. Analog Multiplier is divided into three parts

- Summing circuit
- Squaring circuit
- Differential amplifier

5.2 Analog Multiplier Schematic Simulations

This chapter divides simulation results into four parts and shows the comparison with the ideal results.

5.2.1 Differential Summing Circuit

This section includes the transient and AC response for Differential Summing Circuit.

5.2.1.1 Transient Response for Differential Summing Circuit

Simulated transient response of differential summing circuit for input voltage ranging from -0.66V to 0.66V in 4 steps. Equation 5.1 signifies calculated value of sum which helps to get ideal waveform. Output of summing circuit is compared with ideal sum to confirm the correctness of the result.

$$V_{sum} = \sqrt{\frac{K_1}{4K_5}}(V_1 + V_2) \tag{5.1}$$

Figure (5.1) shows test setup for transient response of summing circuit.

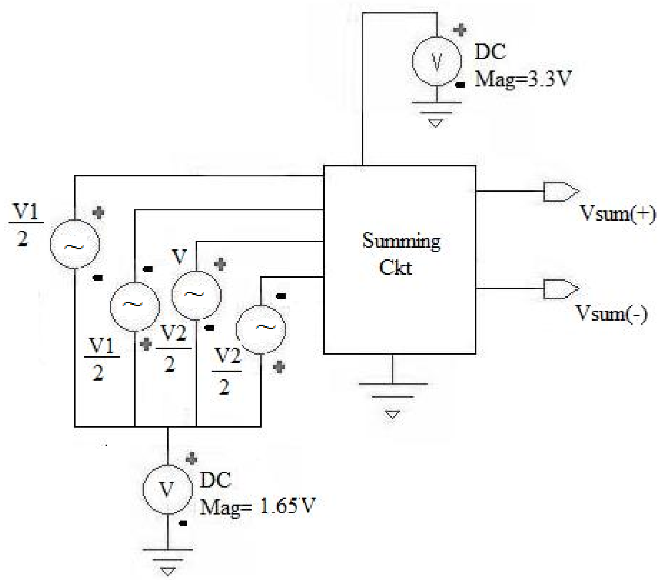


Figure 5.1: Test Setup for Transient Response of Summing Circuit.

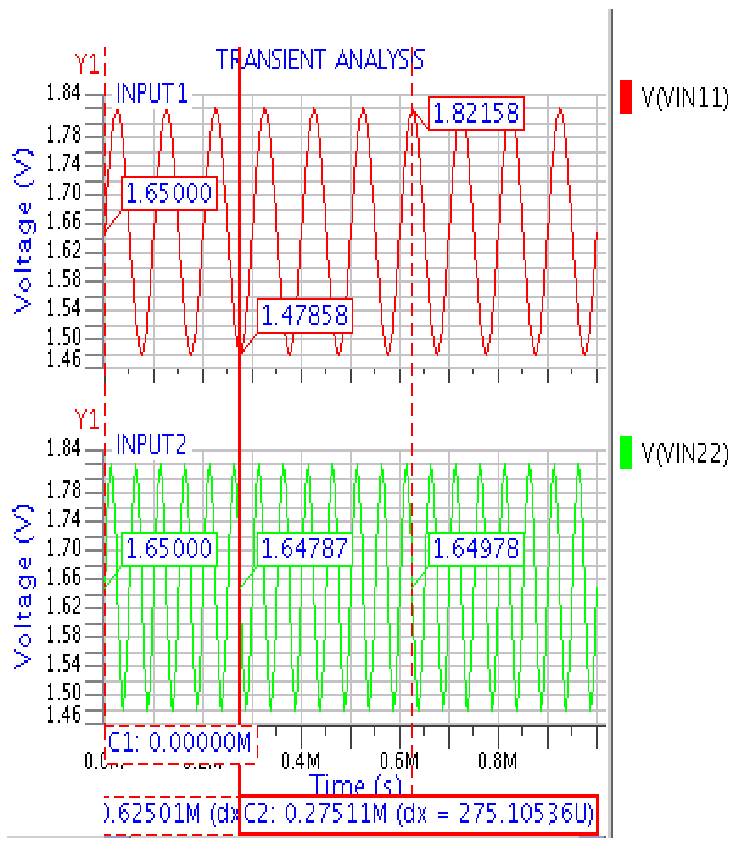


Figure 5.2: $V_1/2$ and $V_2/2$ with DC offset.

Figure (5.2) shows input waveforms for $V_1/2$ and $V_2/2$ with DC offset of 1.65V .

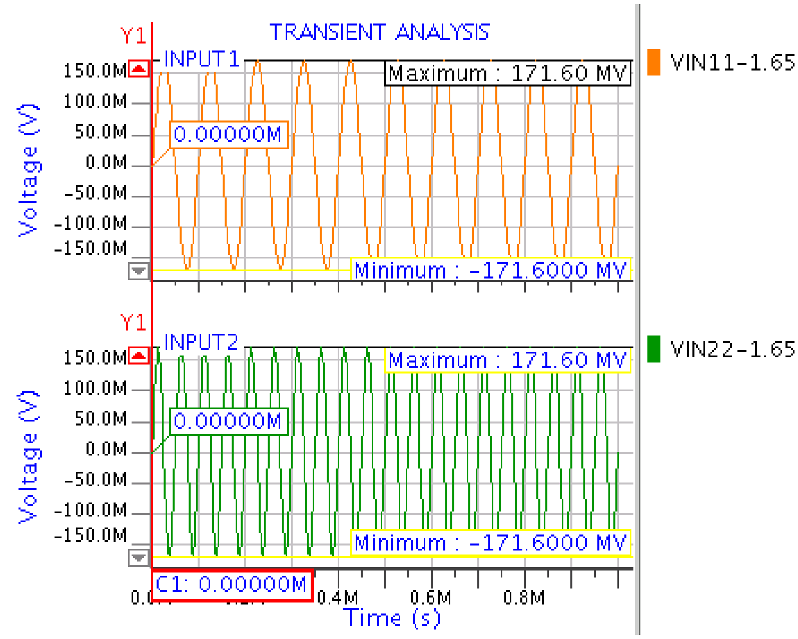


Figure 5.3: $V_1/2$ and $V_2/2$ without DC offset.

Figure (5.3) shows input waveforms for $V_1/2$ and $V_2/2$ without DC offset.

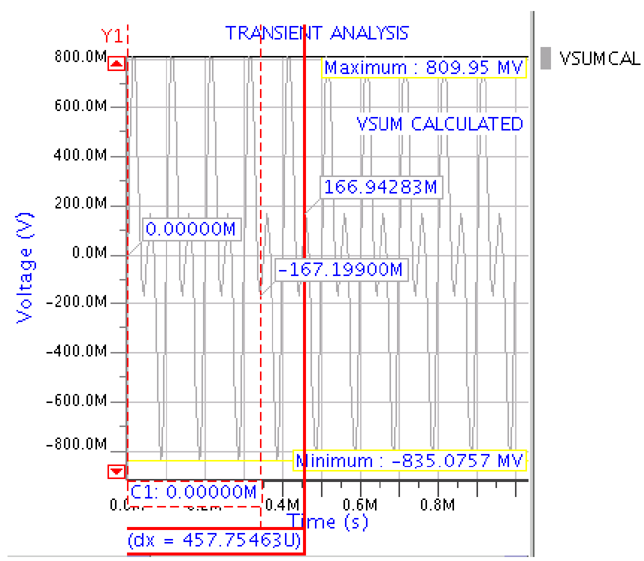


Figure 5.4: Calculated value of V_{sum}

Figure 5.4 shows the calculated V_{sum}.

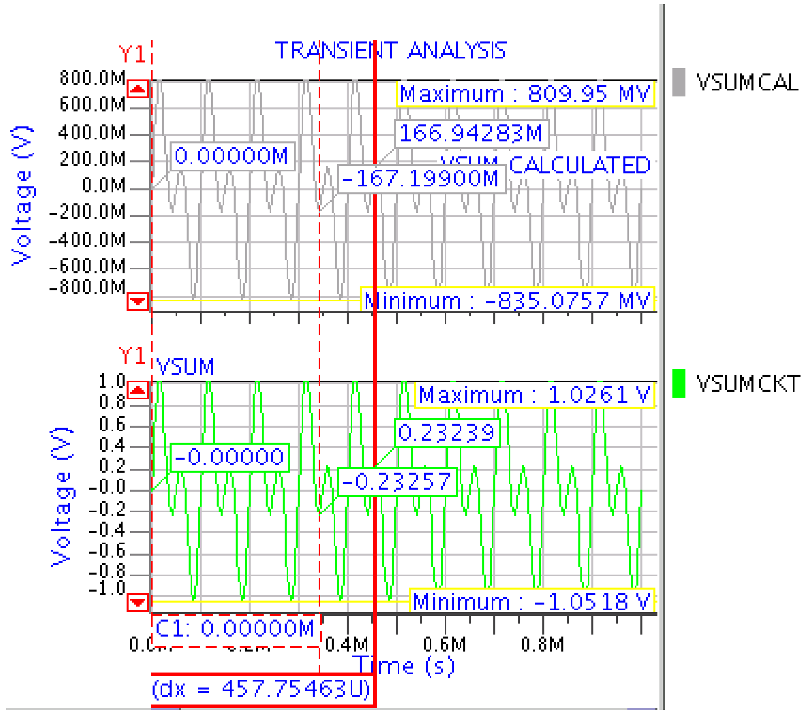


Figure 5.5: Comparison of V_{sum} Circuit and V_{sum} Calculated

5.2.1.2 AC Response for Differential Summing Circuit

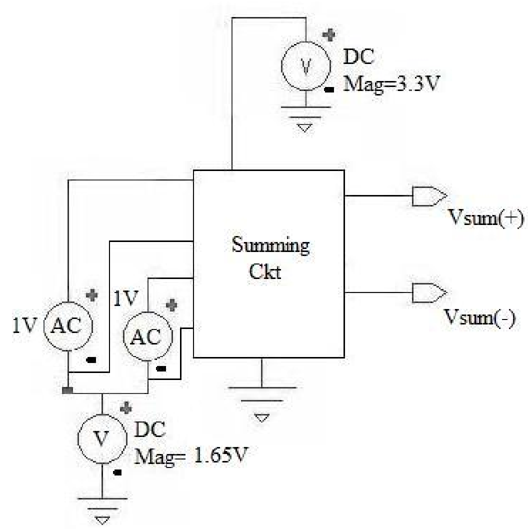


Figure 5.6: Test Setup for AC Response of Summing Circuit.

The output frequency response of differential summing circuit is shown in Figure (5.7). Band width deteriorates in later stages of analog multiplier so very large bandwidth is required in summing circuit. 2-dB bandwidth is achieved at $5.8x10^6$ MHz as shown in a figure 5.6.

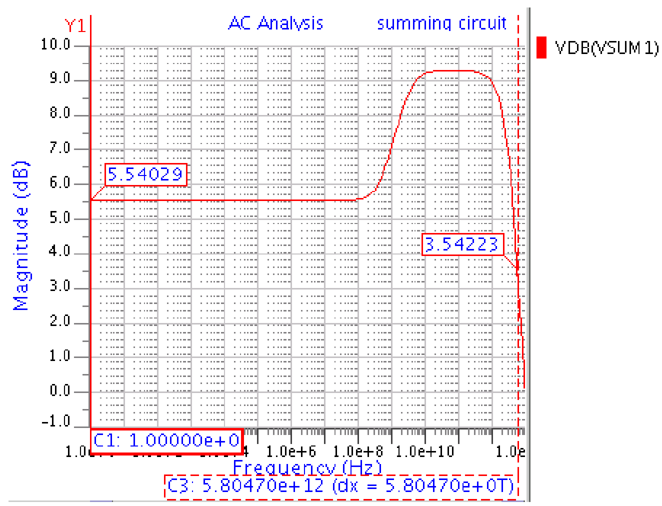


Figure 5.7: AC Analysis of Differential Summing Circuit

Gain of 5.52 db has been achieved as shown in a Figure (5.6) in contrast to ideal value of 0 db.

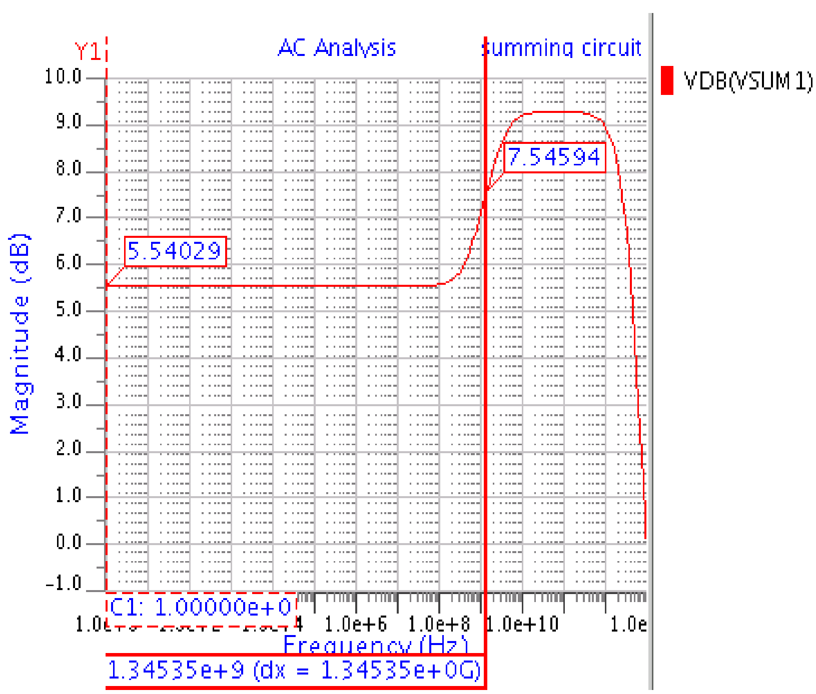


Figure 5.8: AC Analysis of Differential Summing Circuit

Due to the presence of zero in the transfer function of summing circuit, bandwidth is enhanced as shown in a figure 5.7.

5.2.2 Differential Squaring Circuit

This section includes the DC, transient and AC response for Differential Summing Circuit.

5.2.2.1 DC analysis for Differential Squaring Circuit

Figure (5.9) shows the DC characteristic of the differential squaring circuit shown in below.

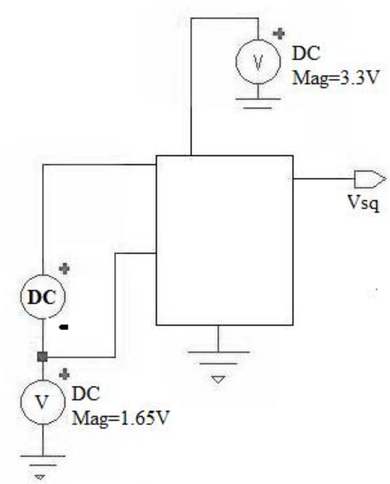


Figure 5.9: DC Analysis of Differential Squaring Circuit

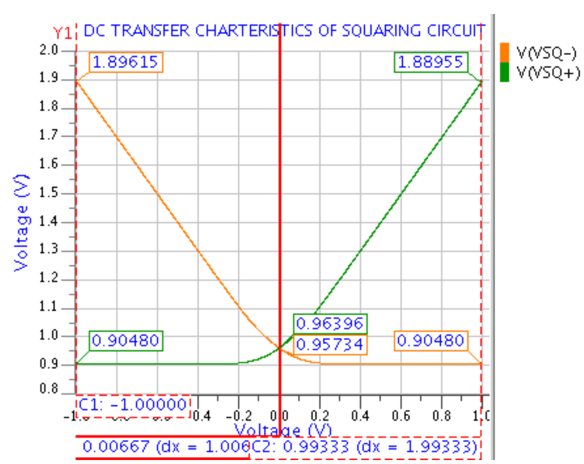


Figure 5.10: DC Analysis of Differential Squaring Circuit

Output voltage of the circuit match with equation 3.25.

5.2.2.2 Transient Response for Differential Squaring Circuit

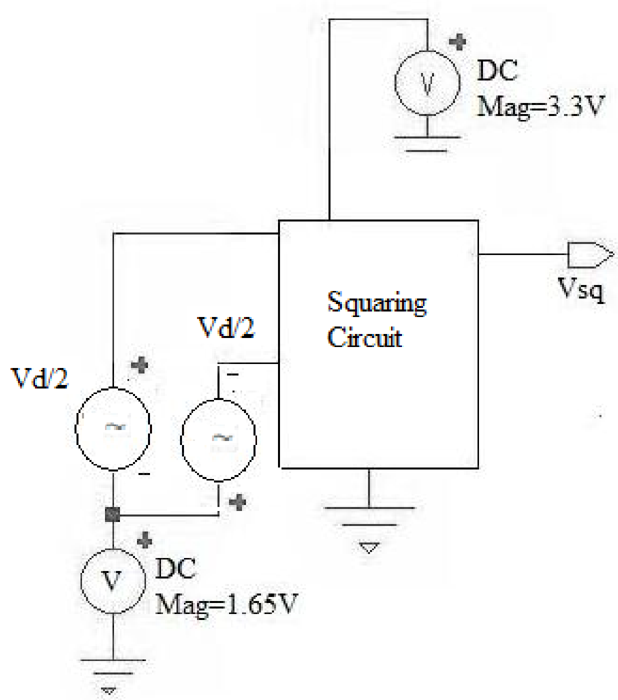


Figure 5.11 – Transient Analysis of Differential Squaring Circuit

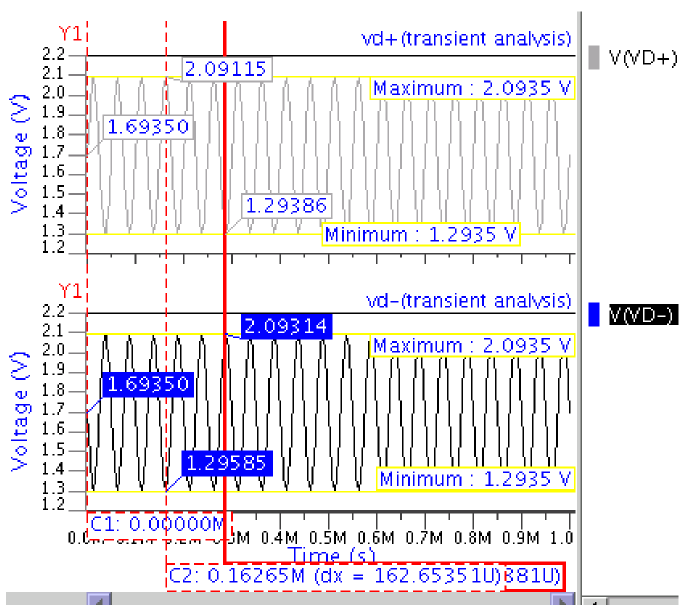


Figure 5.12 – $V_{D+}/2$ and $V_{D-}/2$ with DC offset.

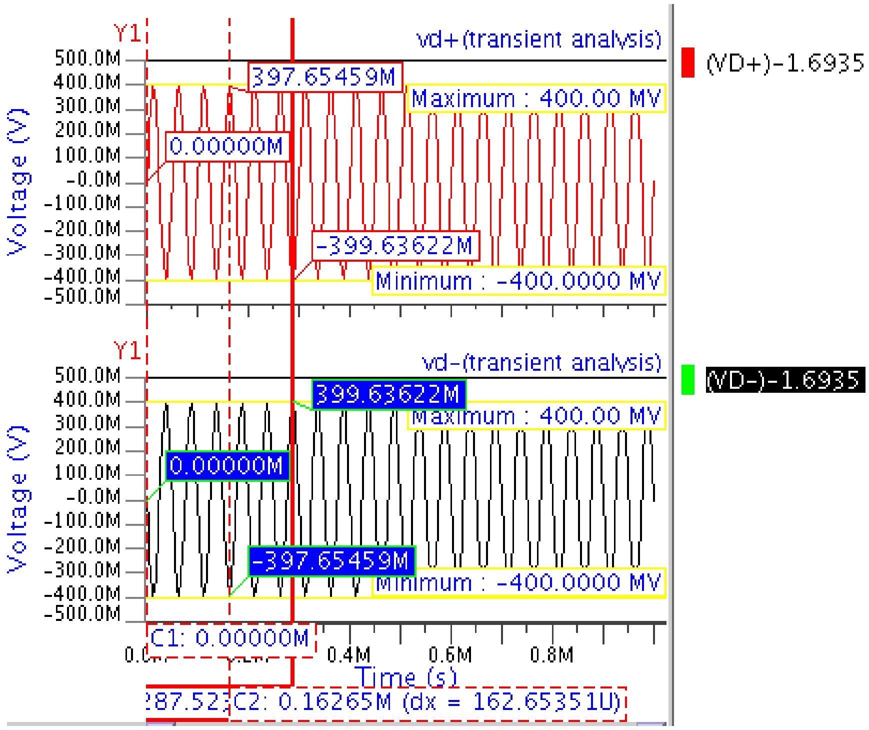


Figure 5.13 – $V_{D+}/2$ and $V_{D-}/2$ without DC offset.

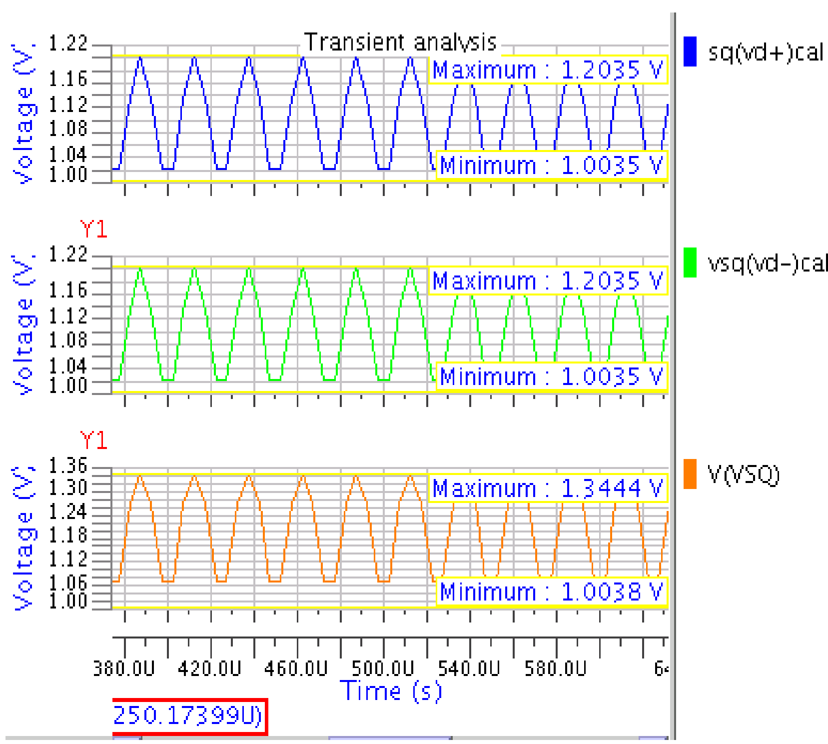


Figure 5.14: Comparison of V_{sq} Circuit and $V_{sq}(V_{d+})$ calculated and $V_{sq}(V_{d-})$ Calculated

5.2.2.3 AC Response for Differential Squaring Circuit

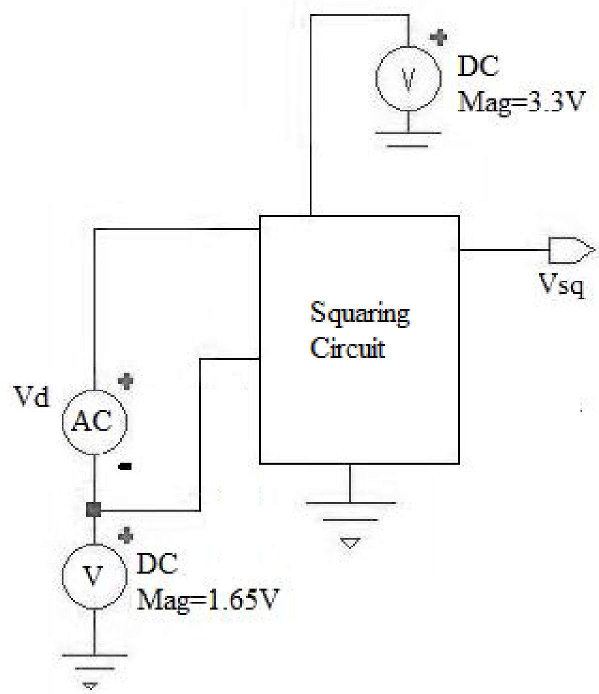


Figure 5.15: AC Analysis of Differential Squaring Circuit

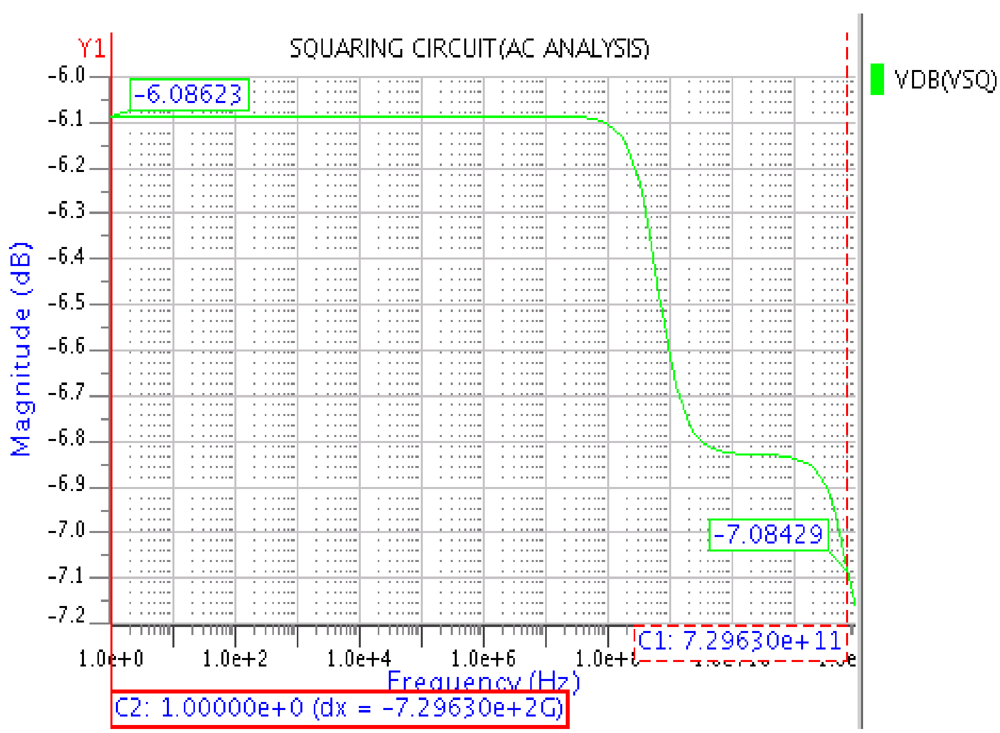


Figure 5.16: AC Analysis of Differential Squaring Circuit

5.2.3 Cascading of Summing and Squaring Circuit

5.2.3.1 Transient Response for cascaded Differential summing and Squaring Circuit

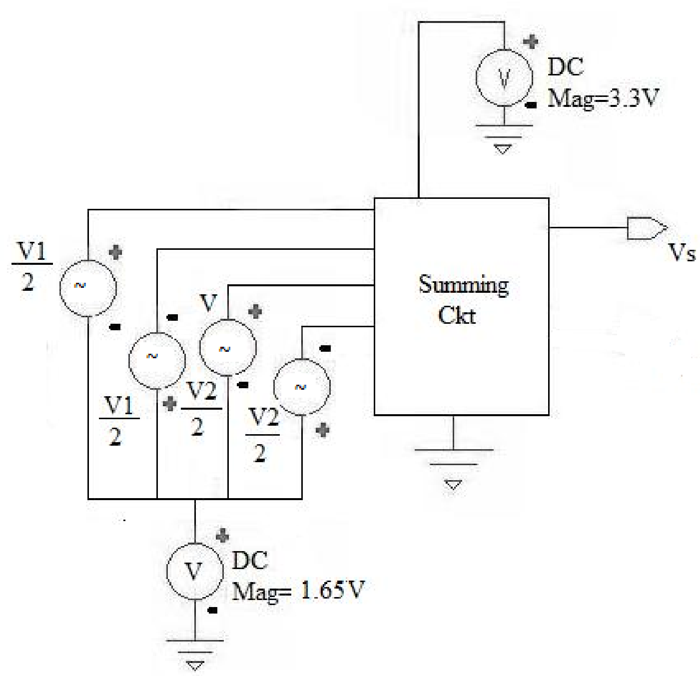


Figure 5.17: Test Setup for Transient Analysis of Cascaded Summing and Squaring Circuit

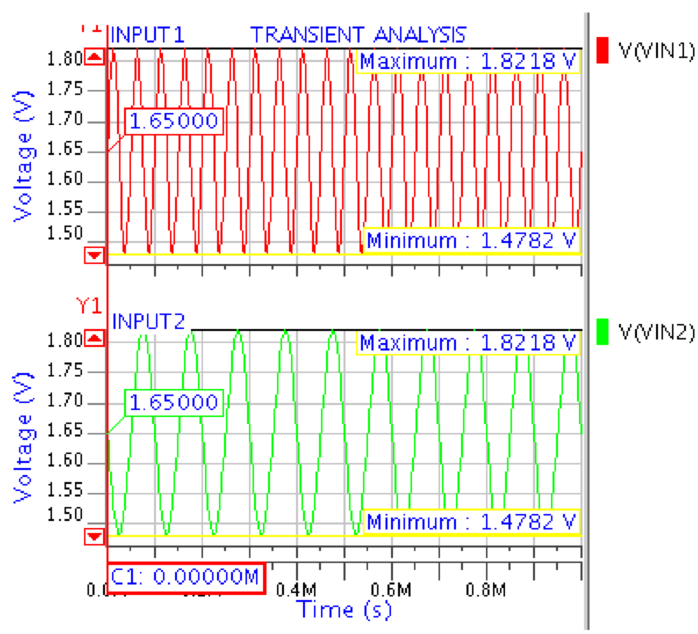


Figure 5.18:Vin$_1$/2 and Vin$_2$/2 with DC offset of Cascaded Summing and Squaring Circuit

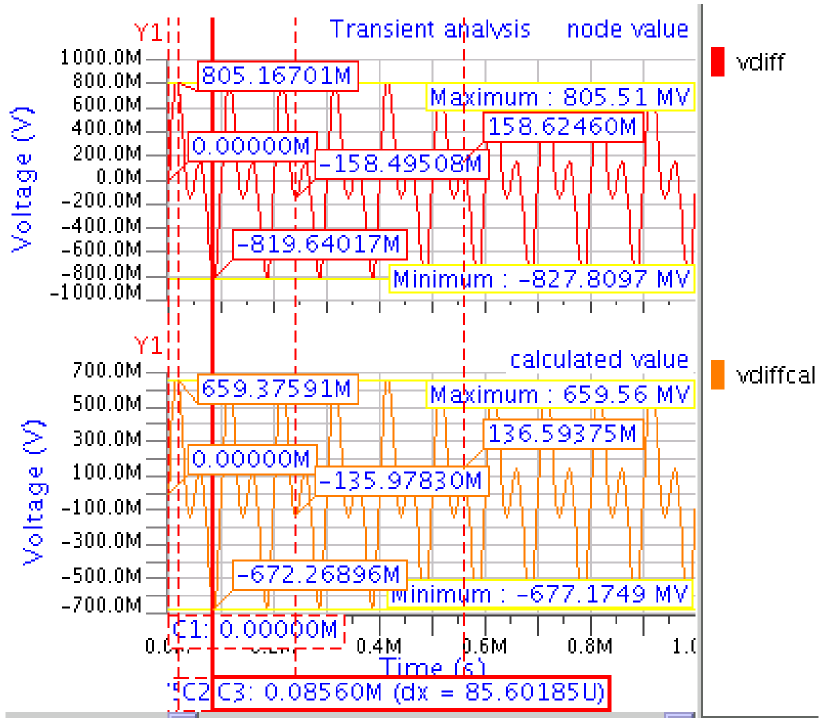


Figure 5.19: Comparison of $V_{diff.}$ Circuit and $V_{diff.}$ Calculated

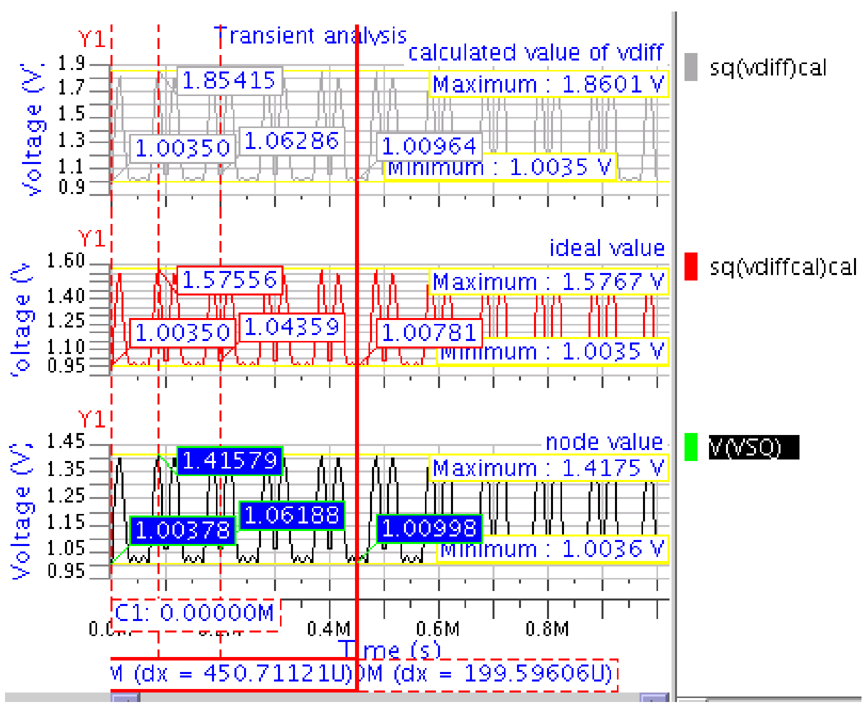


Figure 5.20: Comparison of V_{sq} Circuit and V_{sq} calculated

5.2.3.2 AC Response for Differential Squaring Circuit

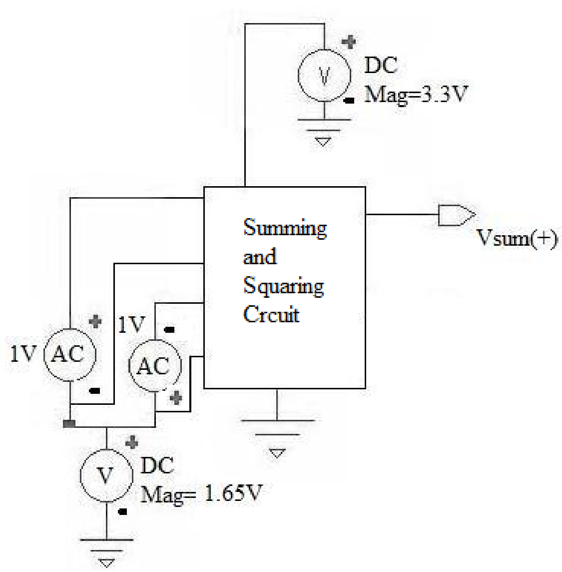


Figure 5.21: Test Setup for AC analysis of Cascaded Summing and Squaring Circuit

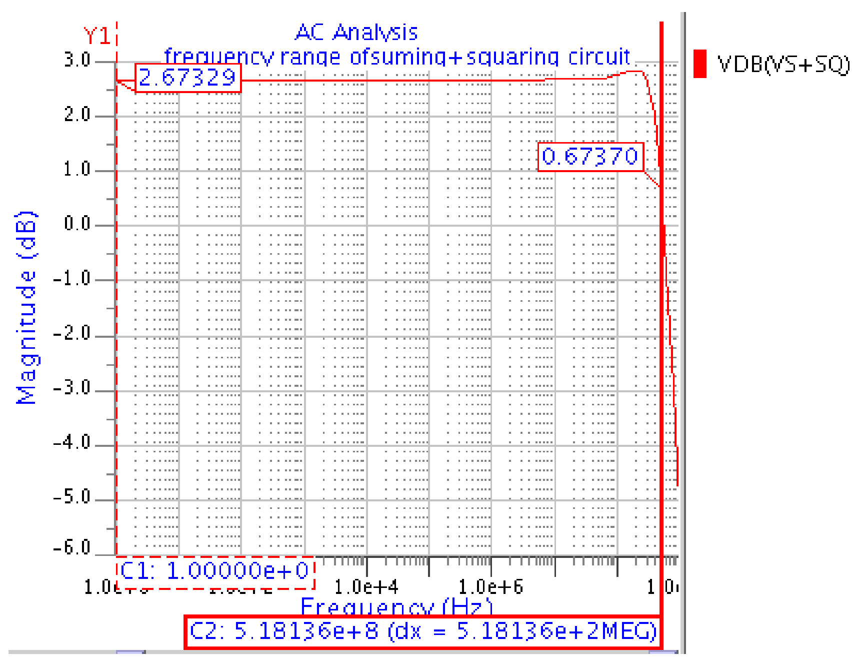


Figure 5.22: – AC Analysis of cascaded summing and squaring circuit

5.2.4 A complete NMOS voltage mode Analog Multiplier

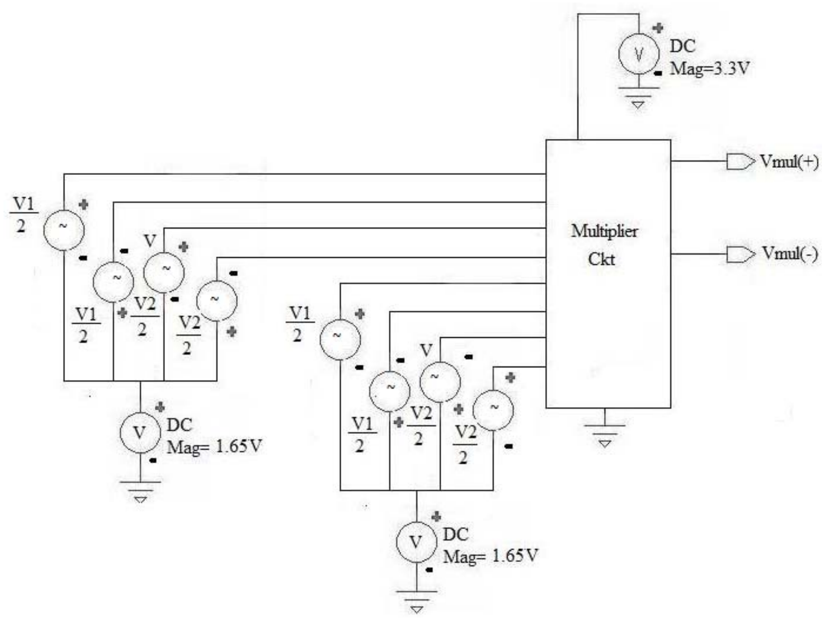


Figure 5.23: Test setup for Complete NMOS voltage mode Multiplier

5.2.4.1 Transient Response for Differential Squaring Circuit

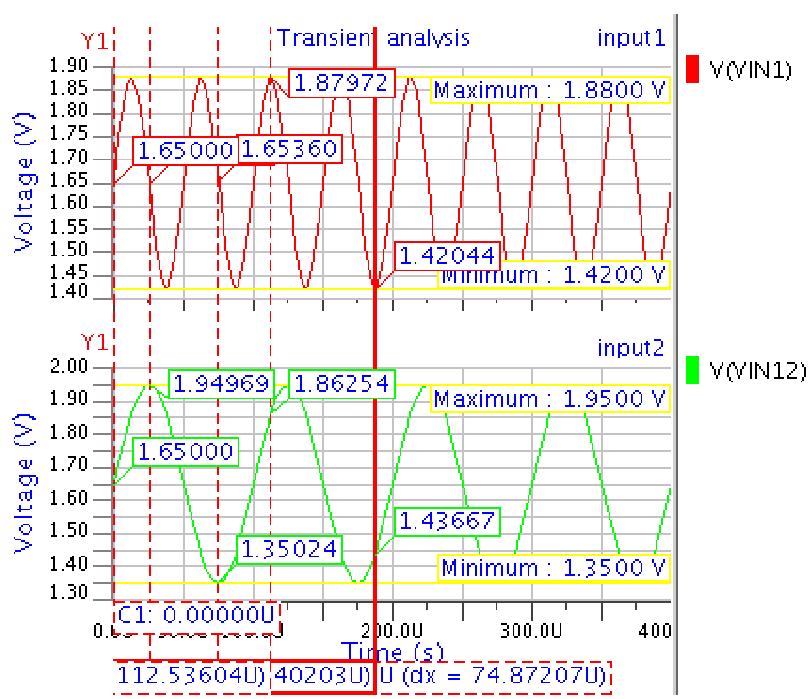


Figure 5.24: V_1(20 KHz) and V_2(10 KHz) inputs with offset

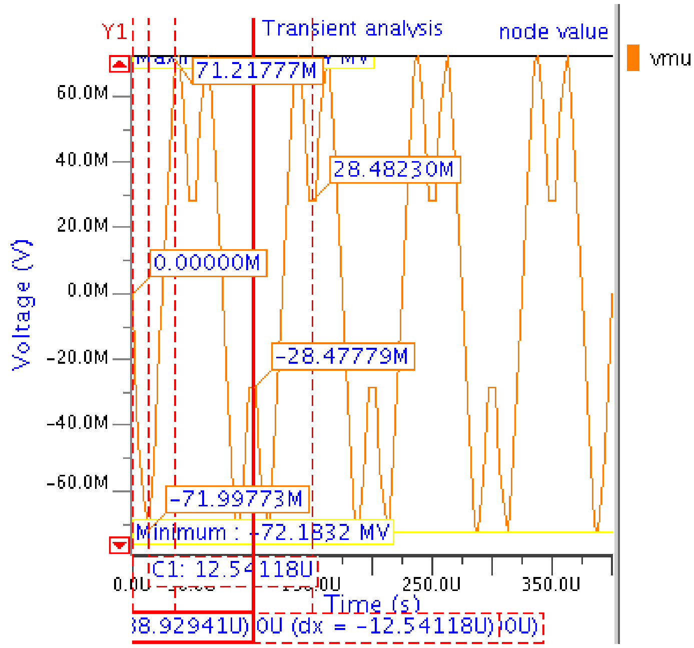


Figure 5.25: Multiplication of V_1 (10 KHz) and V_2(20 KHz) Signals

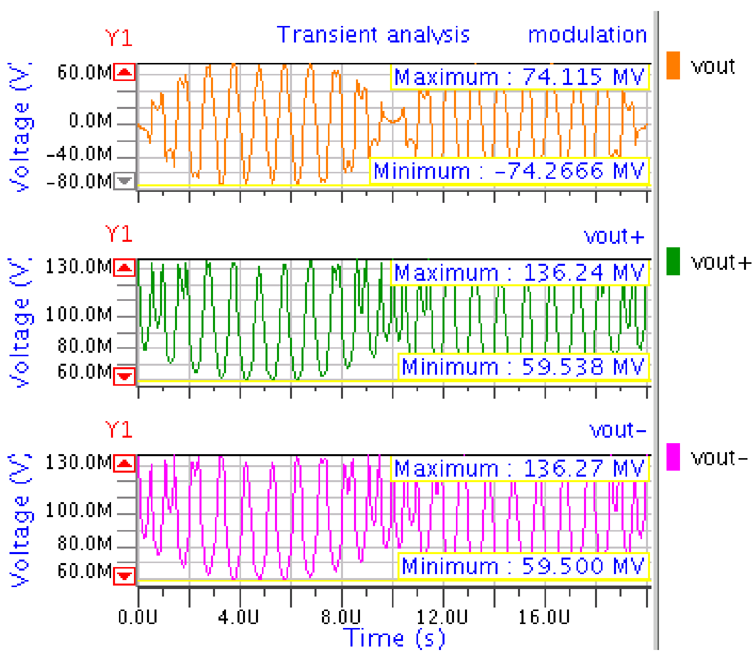


Figure 5.26: Multiplication of V_1 (50 KHz) and V_2 (1 MHz)

In figure5.26 trying to test this multiplier as a modulator with input V_1 /2=.33v and V_2 /2=.23v where V_1 act as information signal with input frequency of 50khz and V_2 act as carrier frequency with 1MHZ frequency.

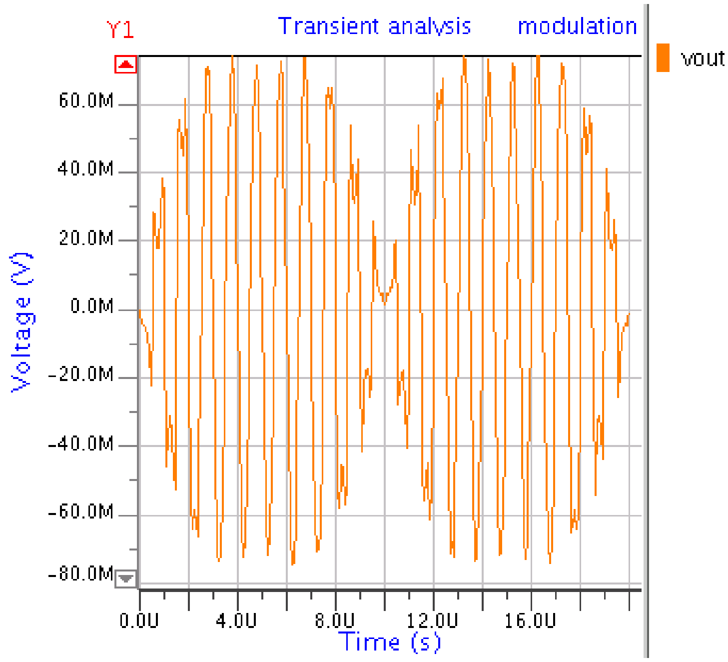


Figure 5.27: Amplitude Modulated V_1(50 Khz) with V_2(1 MHz)

Figure(5.27) shows the successful simulation of analog multiplier as a modulator .

Table 5.1 Comparison between paper results and simulation results

S.No.	Parameters	IEEE Paper Results	Simulated Results
1.	Input Voltage Range	±1V	±0.66V
2.	Frequency	120 MHz	67.779 MHz
3.	Power Dissipation	3.23 mW	1.51 mW

Hence results showing the success in designing analog multiplier with reduced power.

5.3 Layout of N-MOS Four Quadrant Voltage Mode Analog Multiplier

5.3.1 INTRODUCTION:

The layout of analog integrated circuits is often driven by several issues that are generally not important in digital circuits. Therefore it is important for the layout engineer and designer to be aware of these issues.

5.3.2 IMPORTANT ANALOG ISSUES:

1. Matching of Devices:

Matching of individual devices is of paramount concern in analog circuit design. In fact almost all of the 'analog layout techniques' are actually methods for improving matching between different devices on a chip. Matching is important because most analog circuit designs use a ratio based design technique (e.g. current mirrors). Some common techniques that help improve device matching are Multi-gate Finger Layout and Common-Centroid Layout [23].

2. Noise:

Noise is important in all analog circuits because it limits dynamic range. In general there are two types of noise, random noise and environmental noise. Random noise refers to noise generated by resistors and active devices in an integrated circuit; environmental noise refers to unwanted signals that are generated by humans. Two common examples of environmental noise are switching of digital circuits and 60 Hz 'hum'. In general, random noise is dealt with at the circuit design level. However they are some layout techniques which can help to reduce random noise. Multi-gate finger layout reduces the gate resistance of the poly-silicon and the neutral body region, which are both random noise sources. Generous use of Substrate plugs will help to reduce the resistance of the neutral body region, and thus will minimize the noise contributed by this resistance.

Environmental noise is also dealt with at the circuit level. One common design technique used to minimize the effects of environmental noise is to employ a 'fully-differential' circuit design, since environmental noise generally appears as a common-mode signal. However Substrate plugs is also very useful for reducing substrate noise, which is a particularly troublesome form of environmental noise encountered in highly integrated mixed-signal systems and Systems-On-a-Chip (SOC). Substrate noise occurs when large amount digital circuits are present on a chip. The switching of a large number of circuits discharges large dynamic currents to the substrate, which cause the substrate voltage to 'bounce'. The modulation of the substrate voltage can then couple into analog circuits via the body effect or parasitic capacitances. Substrate plugs minimizes substrate noise because it provides a low impedance path to ground for the noise current.

Issues that are important in digital circuits are still important in analog layout. Foremost among these is parasitic aware layout. It is important to minimize series resistance in digital circuits because it slows switching speed. Series resistance also slows analog circuits, plus it introduces unwanted noise. Parasitic capacitance is avoided in digital circuits because it slows switching speed and/or increases dynamic power dissipation. Stray capacitance has the same effect in analog circuits (bias current must be increased to maintain bandwidth and/or slew rate when extra load capacitance is present) plus it can lead to instability in high gain feedback systems.

5.3.3 Definition of Important Terms:

1. **Multi-gate Finger Layout** refers to implementing a single, wide transistor as several narrow transistors in parallel. This minimizes the gate resistance and it also makes it easier to match the transistor with other devices. When referring to a multiple gate finger device one usually uses the term ‘M-factor' to refer to the number of gate fingers.

Therefore an M=4 device has 4 gate fingers. When trying to ratio two or more devices you should always use the same unit transistor size for each device and then include multiple gate fingers to achieve the desired ratio. For instance, a current mirror containing a 10/2 and 5/2 device is NOT a perfect ratio of two because of oxide encroachment. However a 5/2 M=2 device and a 5/2 M=1 device is a perfect ratio of two.

2. Common-Centroid Layout refers to a layout style in which a set of devices has a common center point. This is used to minimize the effect of linear process gradients (e.g. oxide thickness) in a circuit.

Example: Consider that a transistor 'A' has 'M' fingers and can be represented by 'M' instances of the letter 'A'. For example 'AAAA' represents a transistor 'A' that has 4 fingers. Now consider the layout of two transistor, ‘A’ and ‘B’. One structure is

AABB

The problem with this structure is that the transistor 'A' will have a different oxide capacitance (which affects transconductance, Ft) than 'B' because of oxide gradients. For instance, if the oxide thickness at the center of the structure is Tox, and there is an oxide gradient DEL, the average oxide thickness for 'A' and 'B' is

$$Tox(A, average) = [Tox - 2DEL]/2 + [Tox - DEL]/2 = Tox - 3DEL/2$$

$$Tox(B, average) = [Tox + 2DEL]/2 + [Tox + DEL]/2 = Tox + 3DEL/2$$

Now consider the following layout:

ABBA

The average oxide thickness will now be:

$$Tox(A, average) = [Tox - 2DEL]/2 + [Tox + 2DEL]/2 = Tox$$

$$Tox(B, average) = [Tox - DEL]/2 + [Tox + DEL]/2 = Tox.$$

Many other common centroid layout structures are possible:

ABCCBA, ABBBBA, ...

Also in two dimensions:

AB

BA

ABAB

BABA

ABAB

BABA

3. Substrate plugging simply refers to making an ohmic contact to the substrate. This technique is used in digital circuits to minimize latch-up. In analog circuits it is used to minimize latch-up and for the reasons discussed above.

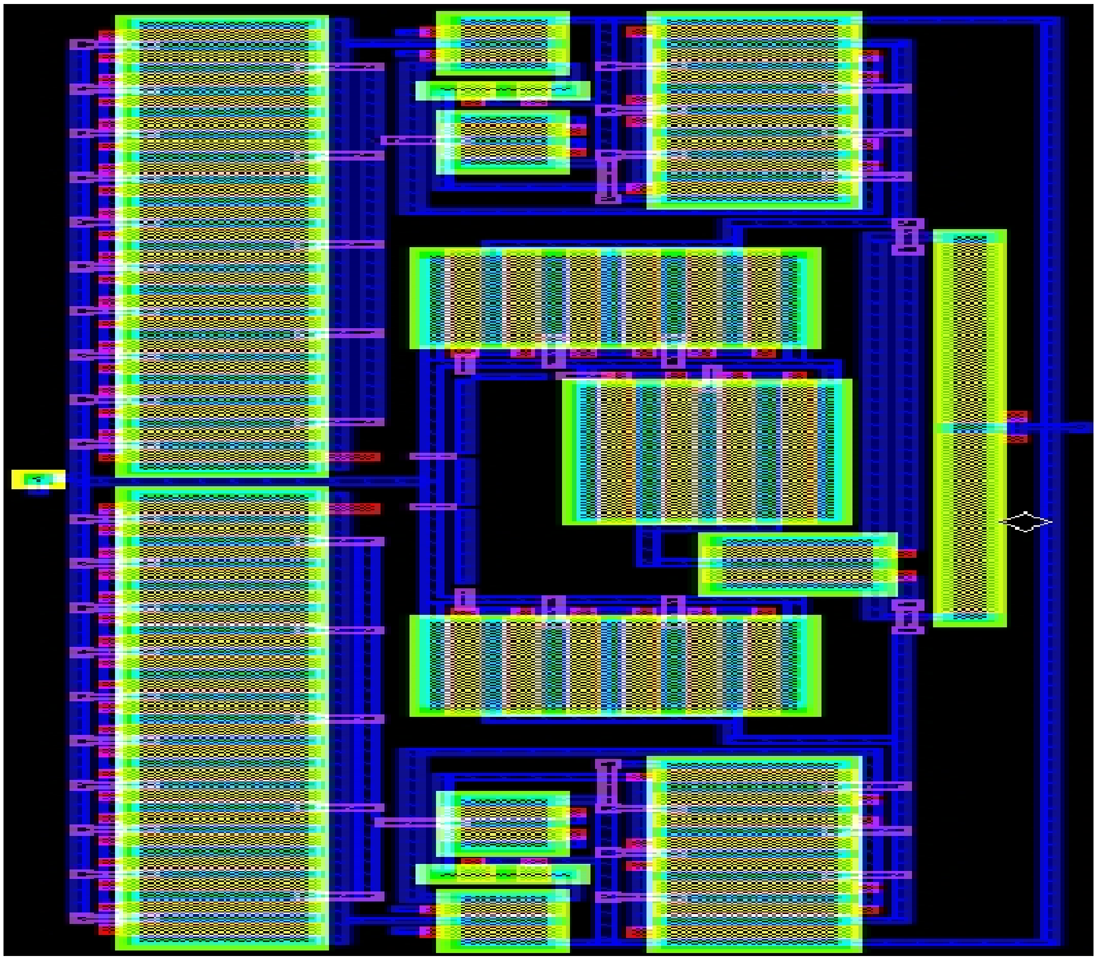


Fig. 5.25: Layout of the N-MOS Four Quadrant Voltage Mode Analog Multiplier

Chapter 6

Conclusions

In this work, NMOS voltage mode four quadrant analog multiplier is designed and simulated for DC, transient and AC analysis. The limited frequency and large IC area requirement of multiplier based on quarter square technique are analyzed by means of simulation results. A better approach for differential input four-quadrant multiplier is designed and verified by means simulations to provide better results for input range, linearity and low power dissipation by eliminating resistors. High operating frequency and area are the prime issues resolved by eliminating resistors.

This multiplier as an amplitude modulator can modulate a low frequency signal by high frequency carrier. The design is able to achieve ±0.66V input range, 67.79 MHz bandwidth with low power dissipation. For bias voltage of 0.691V, the power consumption was 1.51mW. The design layout was done using 0.35µm technology using Eldo simulator in Mentor Graphics's design architect integrated circuit environment.

The layout of final design is verified by means of Mentor Graphics's IC station (Verification tool) without any design kit. The design is cleared with respect to Design Rule Check (DRC) and Layout Versus Schematic (LVS) check. The process of designing the chip from start to finish was quite valuable to enhance my designing skills.

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