PERFORMANCE ANALYSIS OF A DC-DC MULTILEVEL BOOST CONVERTER

A dissertation submitted in partial fulfillment of the requirements for the degree of

MASTER OF ENGINEERING

in

Power Electronics and Drives

Submitted by

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DECLARATION

I hereby declare that the work which I have presented in dissertation entitled, "***Performance Analysis A DC-DC Multilevel Boost converter***", in partial fulfillment of the requirements for the award of degree of Master in Engineering in Power Electronics and Drives, submitted to Electrical & Instrumentation Engineering Department of Thapar Institute of Engineering & Technology University, Patiala is an authentic record of my own work carried under the supervision of Dr. Santosh Sonar. It refers to other researcher's work which is duly listed in the reference section. The matter contained in this dissertation has not been submitted, neither in part nor in full to any other degree to any other university or institute except as reported in text and references.

Place: PATIALA

Date: 17/7/2017

(Julakanti Santhosh Reddy)

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CERTIFICATE

Certified that the dissertation entitled, "***Performance Analysis of A DC-DC Multilevel Boost converter***", which is being submitted by Julakanti Santosh Reddy in partial fulfillment of the requirements for the award of the Master of Engineering in Power Electronics and Drives, to Thapar University, Patiala, is a bonafide record of the candidates own work carried out by his under my supervision and guidance. The matter contained in this dissertation has not been submitted, neither in part nor in full to any other university or institute for the award of any degree.

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ACKNOWLEDGEMENT

I feel honored in expressing my profound sense of gratitude and indebtedness to **Dr. Santosh Sonar**, Asst. Professor, Electrical and Instrumentation Engineering Department, Thapar University, Patiala for his guidance, meticulous effort, constructive criticism, inspiring encouragement, unflinching support and invaluable co-operation which help me to enrich my knowledge and reproduce it in the present form.

İ also like to extend my gratefulness to **Dr. Ravinder Agarwal**, Professor and Head, Electrical and Instrumentation Engineering Department, Thapar University, Patiala for his perpetual encouragement, generous help, and inspiring guidance. İ am thankful for kind coordination through M.E to **Ms. Manbir Kaur**, PG coordinator, Associate Professor, Electrical, and Instrumentation Engineering Department, Thapar University, Patiala.

I am also very thankful to the entire faculty and staff members of Electrical and Instrumentation Engineering Department for their direct-indirect help, co-operation, love, and affection, which made my stay at Thapar University memorable.

İ am very thankful to **Mr. Satwant Singh** Ph.D. scholar and staff of Power Electronics Lab Electrical and Instrumentation Engineering Department, Thapar University, Patiala for developing prototype of thesis work.

I wish to thank all my classmates for their time-to-time suggestions and cooperation without which İ would not able to complete my work.

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ABSTRACT

The core contribution in this thesis is mathematical, simulation and experimental analysis of a DC-DC multilevel boost converter (MBC). MBC is derived from the conventional boost converter by adding 2N-1 capacitors, 2N-1 diodes, with on driven switch and one inductor without changing the main conventional boost converter, to obtain N levels of output voltage. The proposed topology is a non-isolating circuit operated at high switching frequency.As a result the size of inductor and capacitor as well as ripple across it reduces. The structure of the circuit is multimodular to convert low input dc voltage to high output dc voltage with low rating devices at low duty cycle. This marks the circuit more suitable for various applications as Photovoltaic (PV) system, fuel cell etc. The open loop and closed loop analysis of the converter is done. A detailed mathematical analysis to select suitable value of Inductor and capacitor to meet output requirement is given. Non-linear dynamic analysis of full order MBC, reduced order MBC and small signal modeling of the converter is presented. To verify the mathematical results, simulations are done in Matlab Simulink. Finally, to demonstrate the validity of proposed theory and simulation results, a prototype was developed in the lab.

Index Terms: - Multilevel Boost converter (MBC), PV system, Multilevel Inverters (MLIs), Pulse width modulation (PWM).

TABLE OF CONTENTS

NOMENCLATURE

Symbol	Description	Units
V_s	Source Voltage	Volts
V_o	Output Voltage	Volts
I_s	Source Current	Ampere
I_o	Output Current	Ampere
D	Duty Cycle	No units
N	Number of levls	No units
V_c	Voltage across Capacitor	Volts
T_s	Switching time period	seconds
I_L	Inductor Current	Ampere
V_L	Voltage across Inductor	Volts
f_s	Switching Frequency	Hertz
L_c	Critical Value of Inductance	Henry
C_c	Critical Value of Capacitence	Farad
ΔI	Ripple Current	Ampere
ΔV	Ripple Voltage	Volts
Q	Charge	Coulomb
C_{eq}	Equivalent Capacitence	Farad
$\hat{x}$	Small change in x	No units
$\hat{I}_z$	Small change in Output current (Iz)	Ampere
τ	Time Constant	Seconds
N	Speed	rpm
Tem	Electromagentic Torque	N-m
Ia	Armature Current	Ampere
Hz	Frequency	Cycles/second
K_m	Motor constant	N-m/A (or) V-sec/rad

LIST OF FIGURES

LIST OF ABBREVIATIONS

ACRONYMS	FULL FORM
AC	Alternating Current
DC	Direct Current
MOSFET	Metal Oxide Semiconductor Field Effect Transistor
IGBT	Insulated Gate Bipolar Transistor
HVDC	High Voltage Direct Current
MBC	Multilevel Boost Converter
CBC	Conventional Boost Converter
PV	Photovoltaic System
MLI	Multilevel Inverter
STATCOM	Static Compensator
PWM	Pulse Width Modulation
FACTS	Flexible AC Transmission System
CHB	Cascaded H-bridge
kV	Kilo Volt
EV	Electric Vehicle
T.H.D.	Total Harmonic Distortion
RPM	Revolutions per minute
VSC	Voltage Source Converter
VSI	Voltage Source Inverter
DC-MLC	Diode Clamped Multilevel Converter
FC-MLC	Flying Capacitor Multilevel Converter
IEEE	Institute of Electrical and Electronics Engineers
MATLAB	Matrix Laboratory
RMS	Root-mean-square
DTC	Direct Torque Control
PID	Proportional Integral and Differential
SDCSs	Separate DC sources
mH	Milli henry

LIST OF TABLES

ORGANIZATION OF THESIS WORK

The thesis is organized in six chapters as follows,

- **CHAPTER-1,** discusses about different conventional topologies of DC-DC converter and its features
- **CHAPTER-2,** in this chapter, literature survey of DC-DC converter is presented. Literature review regarding classification, applications, modelling, controlling design considerations, efficiency and recent developments is discussed
- **CHAPTER-3,** this chapter, presents detailed analysis of the proposed topology, multilevel dc-dc boost converter. The principal of operation of the circuit, the effect of parasitic resistance, switch and diode voltage drops, state space and stability analysis, settling time of converter responses for variable resistance load, and applications.
- **CHAPTER-4,** here discussion about all results regarding converter, root locus, bode for reduced order model of two level MBC is presented.
- **CHAPTER-5,** validation of simulation results with prototype of MBC developed in the lab is presented.
- **CHAPTER-6,** Conclusion and future scope of the work is presented.

CHAPTER-1
INTRODUCTION

1.1 BACKGROUND: -

In nature basically two electrical signals exist, namely AC and DC. AC power can't be stored. It needs transformer for processing. DC power can be stored, but it uses various converters to meet load end requirement. The converters are classified as (AC-DC), choppers (DC-DC), inverters (DC-AC), voltage controllers (AC-AC), cyclo converters(AC-AC). These converters consist of passive components like inductors, capacitors and active components like semiconductor switches. DC-DC converters are gaining popularity nowadays. These converters are generally used in applications like digital systems, renewable power applications, hybrid electric vehicle system, regulators, etc. The grid system requirement is high power converters at low frequency operation. buck converters are generally used in the digital system, microelectronic systems because these devices required less than 5V DC. The best example of the buck converter is mobile adaptors having AC input of 110V to 220V.Boost converters finds its applications in X-ray, hybrid electric vehicle, DC drive system, renewable applications like PV system, fuel cell, micro-grid applications and HVDC system.

In high gain converters transformers are not feasible as it produces non-linarites in the output. Transformers used in the resonant(isolated) converters like push-pull, fly back, half-bridge DC-DC converter, Full-Bridge DC-DC converter etc. These converters preferably operate at high-frequency as it redues passive component requirement in tern lesser inductor current and capacitor voltage ripple.

1.2 CLASSIFICATION OF DC-DC CONVERTERS: -

DC-DC converters can be categorized as follows,

a) Buck converter
b) Boost converter
c) Buck-boost converter
d) Cuk converter
e) Sepic converter etc.

1.2.1 BUCK CONVERTER: -

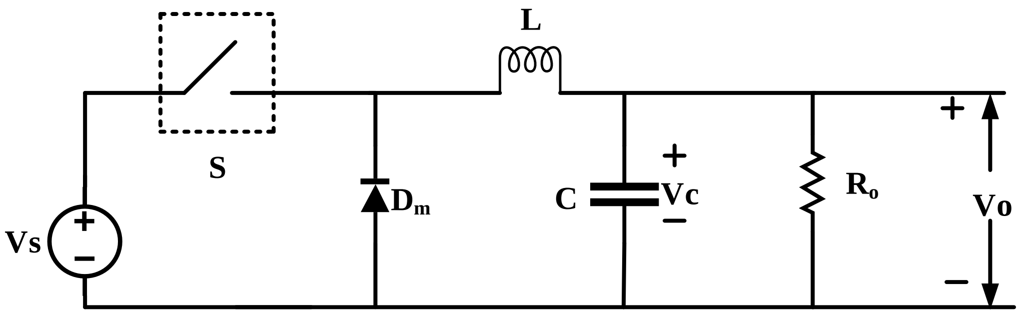

Fig 1.1 Buck converter

Fig1.1 represents a simple buck converter. Inductor and capacitor acts as energy storing element. Switch (S) can be any switch like BJT, MOSFET, IGBT depending upon switching frequency. During switch on (DT_s) condition inductor stores energy, during switch off condition (1-D) T_s stored inductor energy is transfer to load through diode (D_m). Output voltage and source current equations are given below.

$$\text{Output voltage } V_o = DV_s \tag{1.1}$$

$$\text{Input current } I_s = DI_o \tag{1.2}$$

1.2.2 BOOST CONVERTER: -

The boost converter is shown in Fig 1.2. Capacitor at load side is to maintain a constant voltage across the load. During ON period inductor stores energy and during switch off period inductor stored energy transfer to load resistance through the diode (D_m).

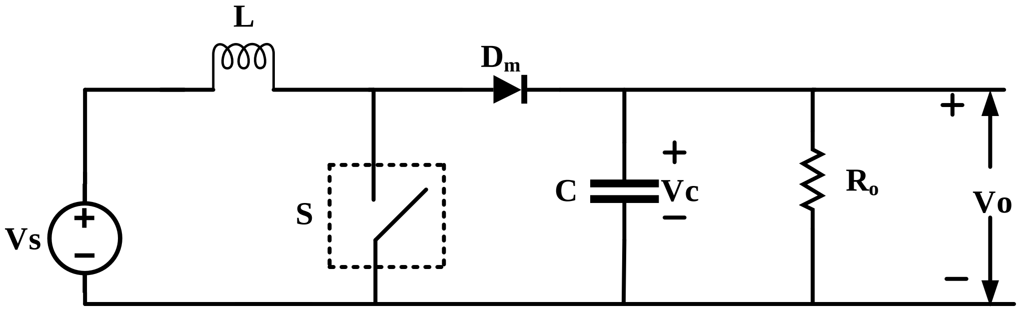

Fig 1.2. Boost converter

$$\text{Output voltage } V_o = \frac{V_s}{(1-D)} \tag{1.3}$$

$$\text{Source current } I_s = \frac{I_o}{(1-D)} \tag{1.4}$$

1.2.3 BUCK-BOOST CONVERTER: -

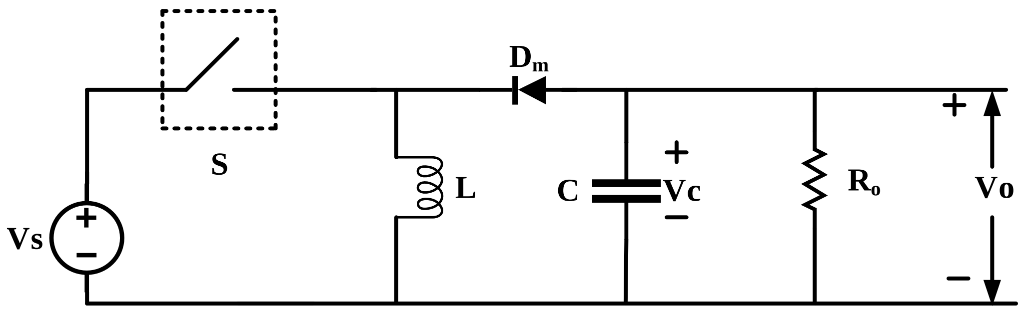

Fig 1.3. Buck-boost converter

Buck-boost converter is shown in Fig 1.3. During ON period inductor stores energy and in off period it discharges. In this converter output voltage is more or less depends on duty cycle given in equation (1.5).

$$\text{Output voltage } V_o = \frac{DV_s}{(1-D)},\ D \le 0.5 \text{ buck converter, } D \ge 0.5 \text{ boost converter} \tag{1.5}$$

$$\text{Source current } I_s = \frac{-DI_o}{(1-D)} \tag{1.6}$$

1.2.4 CÚK CONVERTER: -

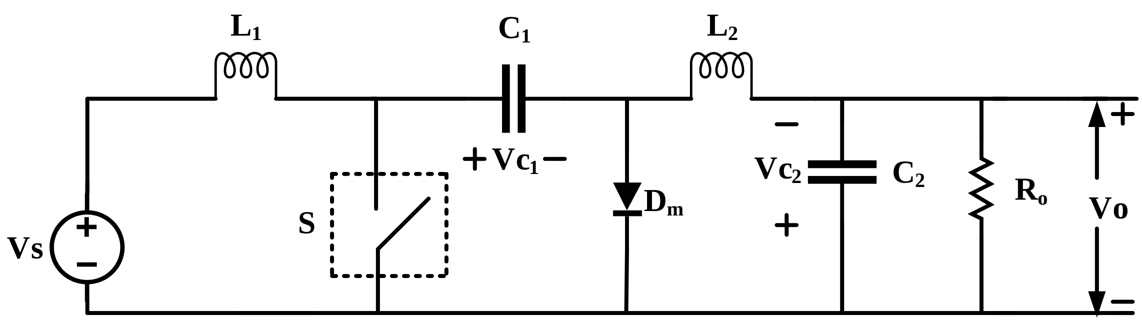

Fig 1.4. CÚK converter

CÚK converter is shown in Fig 1.4. It consists of two inductors and two capacitors. During S on condition, inductor(L_1) and capacitor(C_2) gets charged and in off condition inductor(L_2) and capacitor(C_1) gets charged. It operates as both buck and boost mode depending upon duty cycle. output voltage and output current equations (1.7,1.8) written below. It is suitable up to 100W load .

$$\text{Output voltage } V_o = \frac{-DV_s}{(1-D)} \tag{1.7}$$

$$\text{Source current } I_s = \frac{DI_o}{(1-D)} \tag{1.8}$$

1.2.5 SEPIC CONVERTER: -

SEPIC converter is presented in Fig 1.5. As in CUK converter, sepic converter also consist of two inductors and two capacitors. During switch (S) on (DT_S) condition both inductors are charging and both capacitors are discharging, during off condition both capacitors charging inductor are discharging through the diode (D_m) shown in Fig 1.5. output voltage maintains constant always by a capacitor(C_2) shown in Fig 1.5. output voltage and input current equations (1.9, 1.10) are written below.

$$\text{Output voltage } V_o = \frac{-DV_s}{(1-D)} \tag{1.9}$$

$$\text{Source current } I_s = \frac{DI_o}{(1-D)} \tag{1.10}$$

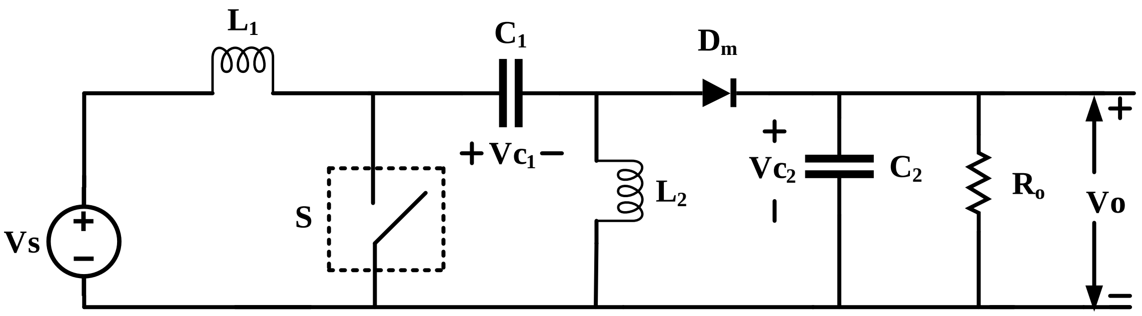

Fig1.5. SEPIC converter

1.2.6 FEATURES OF DC-DC CONVERTERS: -

Table 1.1 Features of dc-dc converters

Converter	Features
Buck	• Output voltage less than the input voltage. • Discontinuous input current. • Continuous output current.
Boost	• Output voltage more than the input voltage.

	• Continuous input and output currents
Buck-boost	• This converter operates as both modes like buck or boost mode. • High switching stress in boost mode.
CÚK	• two inductors and two capacitors • Used for low power applications (up to 100W) • High switching stress
SEPIC	• SEPIC converter required two inductors and two capacitors • High switching stress

CHAPTER-2
LITERATURE REVIEW

2.1 CLASSIFICATION OF DC-DC CONVERTERS: -

[1] DC-DC converters are of two types, isolated and non-isolated. Non-isolated converters operated at the high-frequency. These converters don't have transformers. To get high output voltage larger value of passive component is needed.

[2] In conventional dc-dc converter topologies, to reduce the size of passive component, it is to be operated at high frequency.

[3] Many electrical loads like LCD TV, electric pumps and SAI instruments operate at high voltage and low current. For all these applications a converter is proposed. It consists of three switches, three diodes and an isolating transformer. It operates at high frequency. It produces high output voltage with low ripple content. But the converter has more number of switches and capacitors with more complex gate driver circuit.

[4] Basic dc-dc converter is not suitable for high power applications. A new topology is derived from basic dc-dc converter. It increases the output voltage magnitude by adding capacitors and diodes without changing the conventional boost converter.

[5] Multilevel dc-dc boost converter consists of one switch, one inductor with N number of capacitors and diodes. Inductor is connected in series with dc source. The proposed topology can give any output voltage by adding capacitors and diodes in the basic circuit. The main demerit of the proposed topology is requirement of large inductor.

[6] In DC-DC converter inductors and capacitors are main components for bucking or boosting the voltage. In Capacitor-switching only capacitors and diodes serve the purpose. It is done by only inductors and diodes in inductor switching. Merits include reduced ripple current, reduced ripple voltage reduces and a single switch operates at high frequency.

[7] In DC-DC converters passive elements like inductor, capacitor and resistors are present. Inductor maintains a constant current and capacitor maintain a constant voltage across the load. The presented topology has constant input current and high output voltage. Demerits of the topology are high value of tapped inductance and EMI. It makes the converter bulky.

[8,9] Nowadays, requirement of power is increasing day by day. With conventional energy sources we can't meet demand. The renewable energy source like photovoltaic (PV) system, fuel cell system, wind system etc. is an alternative choice. For all these renewable applications converters are needed. For high power applications, single input with multi output like MBC is found to be more suitable. Merits of the presented work are high output voltage, no requirement of transformers and operate at high switching frequency. Demerits in MBC topology are more number of capacitors and diodes requirements to produce high output voltage.

2.2 DESIGN CONSIDERATIONS: -

[10] In dc-dc converters appropriate size of inductor and capacitor selection is necessary. The paper describes process to design a multilevel inverter optimally.

2.3 MODELLING AND CONTROL OF DC-DC CONVERTERS: -

[12] Due to sudden change in load, output parameters also changes. In order to maintain constant output, controller design becomes necessary. The paper presents state space modelling of converter for full circuit model. Analysis of full circuit model for MBC is difficult. A reduced order model analysis for MBC is also explained.

[13-16] DC-DC converters are highly non-linear. Small signal modelling of DC-DC converter along with its controller design is presented.

[12,14] DC-DC converters plays important role in PV system. Shadow effect in solar system reduces its power generation. It is eliminated by designing a suitable controller. MPPT controller design along with small signal dynamic modelling is examined.

2.4 EFFICIENCY OF DC-DC CONVERTER: -

[17] DC-DC converter consists components like inductor, capacitors and semiconductor devices like diodes, MOSFET, IGBT. The components don't operate ideally. A proper selection of components for modelling is described.

2.5 DC-DC CONVERTER APPLICATIONS: -

[18] Single fuel cell voltage output is roughly 1.5V. To increase the voltage, fuel cells are arranged in a stacked manner. The voltage is then fed to DC-DC boost converter. Further the boosted voltage is fed to an inverter to achieve desired ac voltage and frequency for utility grid.

[19] Conventional boost converter operates at high duty period for higher gain. At high duty cycle, inductor may get saturates. Multilevel dc-dc boost converter operates at low duty cycle. Multilevel converter for Fuel cell application is presented.

[20] The need of recent days is to reduce the uses of non-renewable sources. The transformation of petroleum based vehicles to hybrid electrical vehicles and then to electric vehicles has been seen. Recent developments in DC-DC converters mark them suitable for electric vehicles. Number of dc supplies is needed to charge electrical vehicles. A multilevel DC-DC converter is derived to serve the purpose.

[21] Single fuel cell voltage output is roughly 1.5V. To increase the voltage, fuel cells are arranged in a stacked manner. The voltage is then fed to DC-DC boost converter. Further the boosted voltage is fed to an inverter to achieve desired ac voltage and frequency for utility grid.

CHAPTER-3

ANALYSIS OF MBC AND APPLICATIONS

3.1 MULTILEVEL DC-DC BOOST CONVERTER: -

Fig3.1 represents Multilevel DC-DC boost converter. It generates the boosted voltage at various levels using a single inductor and a single switch. The main advantage of the proposed topology is that it can produce any number of output voltage levels by adding capacitor and diodes. To get N number of output voltage levels, "2N-1" no of capacitors and same number of diodes is to be connected in the basic circuit.

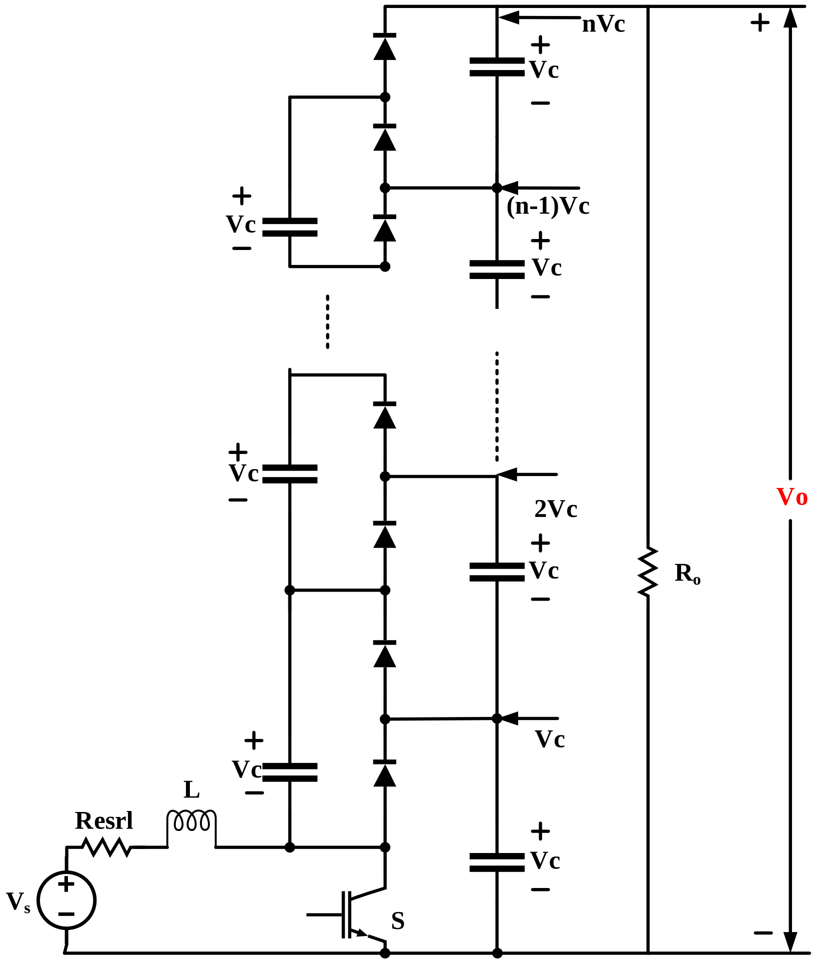

Fig 3.1. Multilevel boost converter

The MBC can be analysed in two different modes of operation, (i) on condition (T_1=DT_S) and (ii) off condition (T_2 = (1-D) Ts. Both on and off conditions for 4 level boost converter is given below.

DURING ON CONDITION (T_1=DT_s)

During on condition, inductor is connected to source voltage as shown in Fig 3.2. If the voltage across capacitor C_7 is more than voltage across C_6 then C_6 gets charged from C_7 through D_6 and switch(S) as shown in Fig 3.3. If sum of voltage across C_7 and C_5 is more than sum of voltage across C_6 and C_4 then both the capacitors C_6 and C_4 gets charged from C_7 and C_5 through D_4 and switch(S) as shown in Fig 3.4. In case the sum of voltage across C_7, C_5 and C_3 is more than sum of voltage across C_6 , C_4 and C_2 then the capacitors C_6, C_4 and C_2 gets charged from C_7 , C_5 and C_3 through D_2 and switch(S) as shown in Fig 3.5.

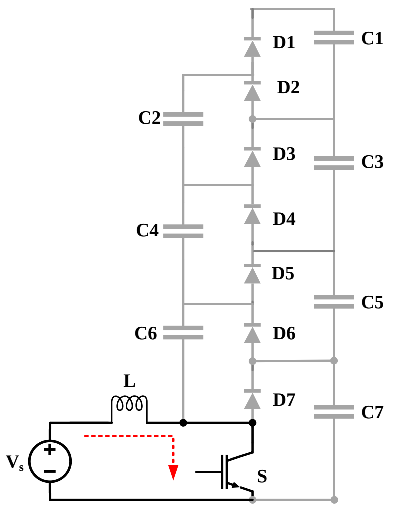

Fig 3.2 Inductor charging from source

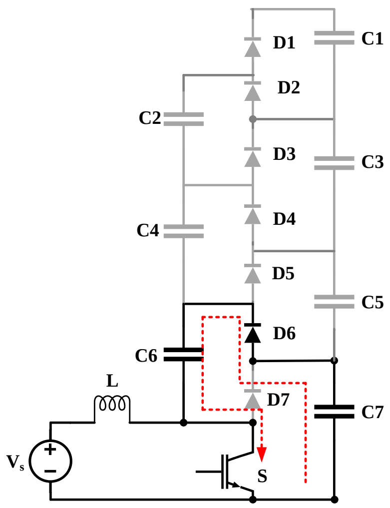

Fig 3.3 C6 is charging from C7

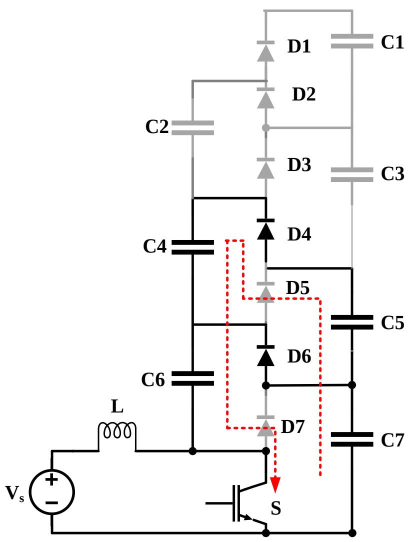

Fig 3.4 C4, C6 charging from C5, C7

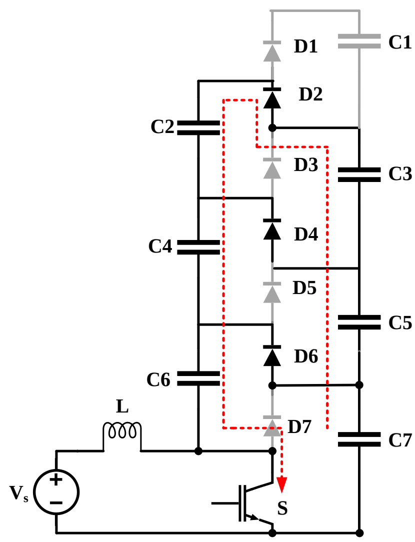

Fig 3.5 C2, C4, C6 charging from C3, C5, C7

DURING OFF CONDITION (T_2=(1-D) Ts): -

During off condition, inductor voltage adds up with the source voltage to charge the capacitor C_7 through D_7 as shown in Fig 3.6. If the voltage across C_6 is more than the voltage across capacitor C_5, D_5 conducts and the capacitors C5 and C7 gets charged as shown in Fig 3.7. Similar approach is adopted to explain the charging of capacitors C_1, C_3, C_5 and C_7 as shown in Fig 3.8 and Fig.3.9.

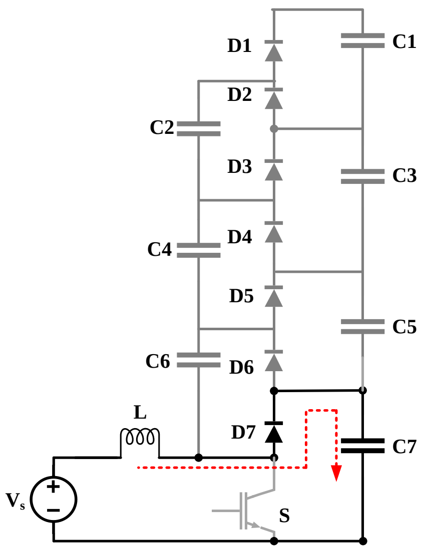

Fig 3.6 Charging of capacitor C_7

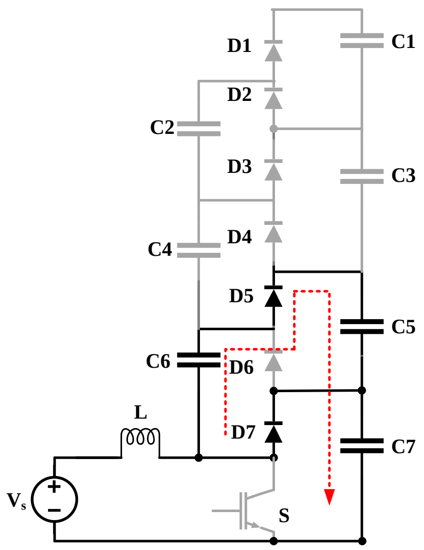

Fig 3.7 Charging of capacitor C5, C7.

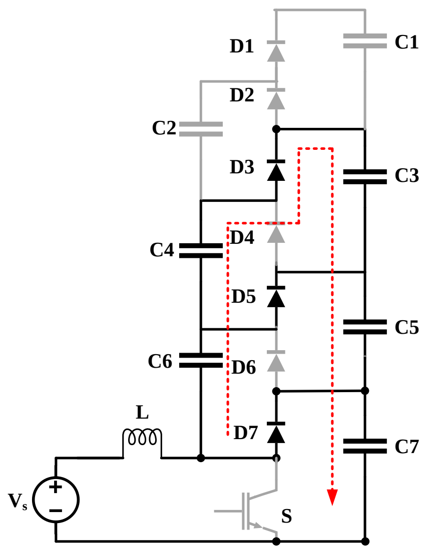

Fig 3.8. Charging of capacitors C3, C5, C7.

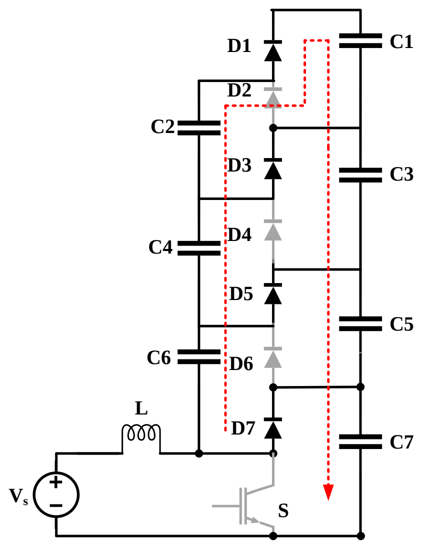

Fig 3.9. Charging of capacitors C_1, C_3, C_5, C_7

3.2 EFFECT OF PARASITIC RESISTANCE (Resrl): -

Simple boost converter at ideal condition has maximum boost ratio, but actual scenario is different in practical. Inductor resistance, called parasitic resistance is responsible for the limitation in boost factor. DC-DC converters operate at high switching frequency. At high frequency inductor size and resistance reduces. At different parasitic resistance, gain of the converter is different at various duty period is presented below.

3.2.1 ANALYTICAL EXPRESSIONS FOR OUTPUT VOLTAGE AND SOURCE CURRENT WITHOUT PARASITIC RESISTANCE: -

From Fig 3.1, output voltage of the converter is equal to sum of the capacitor voltages. For N number of output side capacitors,

$$V_o = N \times V_c, I_L = I_s \tag{3.1}$$

During on condition,

$$V_L = V_s \tag{3.2}$$

During off condition,

$$V_L = (V_s - V_c) \tag{3.3}$$

Averaging the voltage across the inductor,

$$V_L\big|_{on} + V_L\big|_{off} = 0 \tag{3.4}$$

Using equations (3.2, 3.3, 3.4) obtained equation (3.5)

$$DV_s\big|_{on} + (1-D)(V_s - V_c)\big|_{off} = 0 \tag{3.5}$$

$$V_s = V_c(1-D) \tag{3.6}$$

From (3.6) and (3.1)

$$V_o = \frac{N \times V_s}{(1-D)} \tag{3.7}$$

Equation (3.7) represents voltage equation of N level boost converter.

Considering the lossless system,

$$V_s \times I_s = V_o \times I_o \tag{3.8}$$

From (3.7) and (3.8)

$$V_s \times I_s = \frac{N \times V_s}{(1-D)} \times I_o \tag{3.9}$$

$$I_s = \frac{N \times I_0}{(1-D)} \tag{3.10}$$

Equation (3.10) represents source current equation for N level boost converter. Equation (3.9) represents the multilevel dc-dc boost converter output voltage. For N = 1, output voltage represents the conventional boost converter output voltage. Example: - if input voltage(V_s) = 50V, Duty cycle(D) = 0.5 then conventional boost converter output voltage is 100V, same input parameters for MBC also then output voltage is according to equation (3.10) is 300V.

The above example justifies the following,

Multilevel boost converter output voltage = N* conventional boost converter output voltage

3.2.2 ANALYTICAL EXPRESSIONS FOR OUTPUT VOLTAGE AND SOURCE CURRENT WITH PARASITIC RESISTANCE: -

The voltage drop across the parasitic resistance is considered for analysis.
During on condition inductor voltage,

$$V_L = (V_s - I_L \times R_{esrl}) \tag{3.11}$$

During off condition inductor voltage,

$$V_L = (V_s - V_c - I_L \times R_{esrl}) \tag{3.12}$$

$$V_L|_{on} + V_L|_{off} = 0$$

$$D(V_s - I_L \times R_{esrl}) + (1-D)(V_s - V_c - I_L \times R_{esrl}) = 0 \tag{3.13}$$

From (3.13)

$$V_s = V_c \times (1-D) + I_L \times R_{esrl} \tag{3.14}$$

Substituting (3.1), (3.10) in eq. (3.14)

$$V_s = \frac{V_0 \times (1-D)}{N} + \frac{V_0 \times N \times R_{esrl}}{(1-D) \times R_0} \tag{3.15}$$

Equation (3.15) represents the output voltage of N*MBC with Resrl. A graph is plotted between gain and duty cycle for various values of Resrl/Ro is shown in Fig 3.9 and Fig 3.10 for conventional and multilevel boost converter respectively. It will help to select duty cycle to achieve desired output voltage.

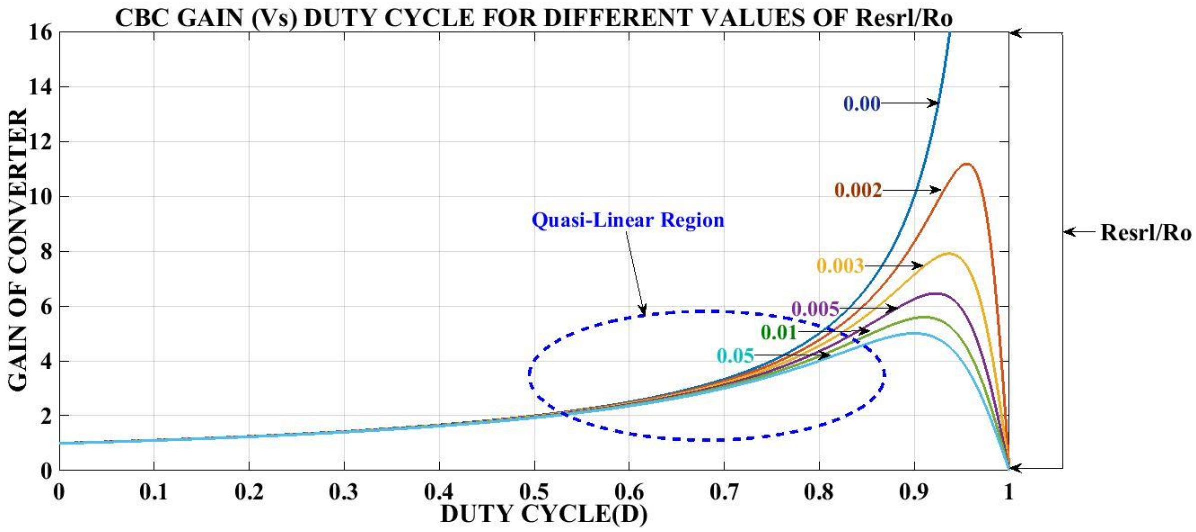

Fig 3.10 CBC voltage gain (Vs) duty cycle for different value of Resrl/Ro

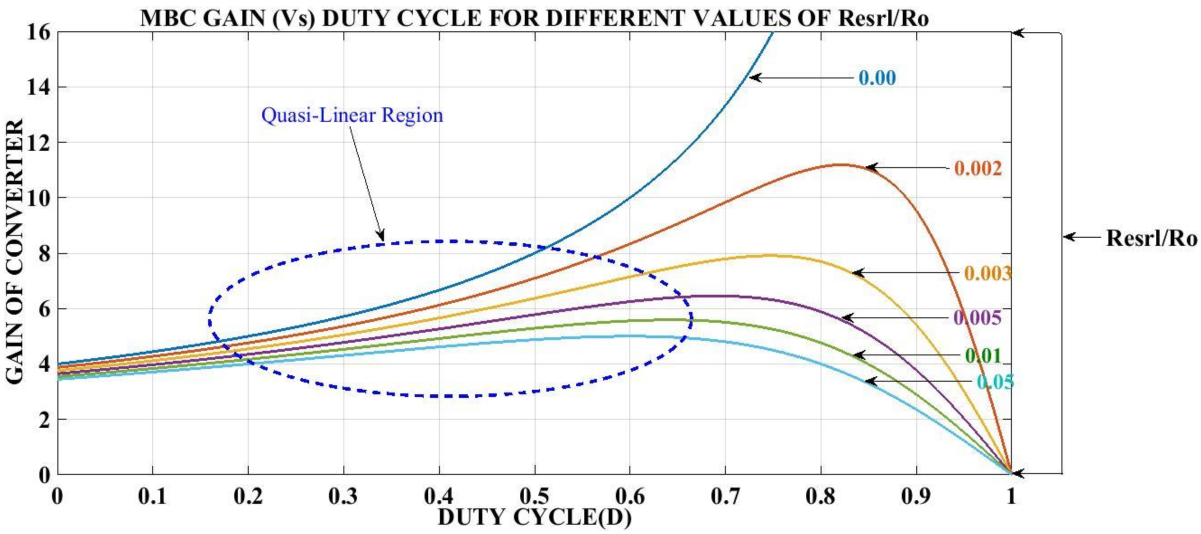

Fig 3.11 MBC voltage gain (Vs) duty cycle for different value of Resrl/Ro

The encircled region in the graph is quasi-linear region because of the linear relation between gain and duty cycle. It is observed that the multilevel boost converter output voltage is more at any duty cycle than conventional one.

3.3 CONVERTER SEMICONDUCTOR DEVICES DROPS: -

Power electronic switches are not ideal. During on as well as switching condition, voltage drop across it reduces conversion efficiency. This drop is negligible in high or medium power application, but becomes prominent in low power application.

From Fig 3.12, voltage across capacitor C6 is written as,

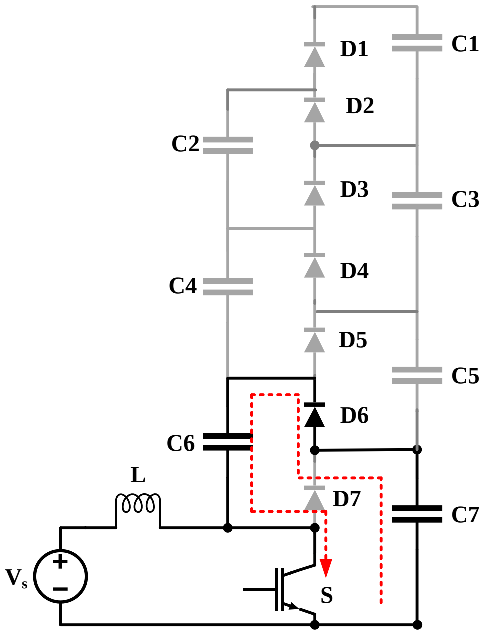

Fig 3.12 Capacitor (C6) charging through diode (D6)

$V_{C6} = V_{C7} - 2V_d$, Where, $2V_d$ is the voltage drops across switch(S) and diode D6.

From Fig 3.4, voltage across capacitor C5 is,

$V_{C5} = 2V_{C7} - 2V_d$, $2V_{C7}$ is the output voltage for 2 level inverter,

From fig 3.12, voltage across the capacitor during off condition,

$V_{C7} = V_{C6} - 2V_d$

$V_{C7} = 2V_{C5} - 2V_d$, $2V_{C7}$ is the output voltage for 2 level inverter,

Ideally, $V_o = NV_c$. Considering the drops across the switches and diodes,

$$\text{Total drop} = \text{During switch}|_{on} + \text{During switch}|_{off} \text{ for N*MBC.}$$

$$V_o = NV_c - (N-1)4V_d \tag{3.16}$$

3.4 DESIGN CONSIDERATIONS OF MBC: -

Inductor design (Resrl =0): -

Output voltage,

$$V_0 = N \times V_c, I_L = I_s \tag{3.17}$$

During on condition inductor voltage,

$$V_L = V_s \tag{3.18}$$

During off condition inductor voltage,

$$-V_L = (V_s - V_c) \tag{3.19}$$

$$V_L = (V_c - V_s) \tag{3.20}$$

Inductor voltage can be represented as, $V_L = \frac{L \times \Delta I}{\Delta T}$ (3.21)

$$T_1 = \frac{L \times \Delta I}{Vs} \tag{3.22}$$

$$T_2 = \frac{L \times \Delta I}{\left(V_c - V_s\right)} \tag{3.23}$$

From equation 3.22 $\Delta I = \frac{T_1 \times V_s}{L}$ (3.24)

From equation 3.23 $\Delta I = \frac{T_2 \times \left(V_c - V_s\right)}{L}$ (3.25)

Equate equations 3.24 and 3.25

$$\frac{T_1 \times V_s}{L} = \frac{T_2 \times \left(V_c - V_s\right)}{L} \tag{3.26}$$

By substituting T_1 = DTs and T_2 = (1-D) Ts in equation 3.26

$$\frac{DT_s \times V_s}{L} = \frac{(1-D)T_s \times (V_c - V_s)}{L} \tag{3.27}$$

From Equation (3.27) capacitor voltage of Multilevel DC-DC boost converter

$$V_s = \left(1 - D\right) \times V_c \tag{3.28}$$

Substitute equation (3.17) Vc in equation (3.28) then equation (3.28) modified as

$$\boxed{V_0 = \frac{N \times V_s}{\left(1 - D\right)}} \tag{3.29}$$

Equation (3.29) represents the output voltage equation for N level MBC with Resrl = 0.

For lossless converter, input power = output power

$$V_s \times I_s = V_o \times I_o \tag{3.30}$$

From (3.29) and (3.30),

$$V_s \times I_s = \frac{N \times V_s}{(1-D)} \times I_o \tag{3.31}$$

From (3.31), source current of converter

$$\boxed{I_s = \frac{N \times I_o}{(1-D)}} \tag{3.32}$$

Total time
$$T_s = T_1 + T_2 = \frac{L \times \Delta I}{Vs} + \frac{L \times \Delta I}{(V_c - V_s)} \tag{3.33}$$

From equation (3.33) the ripple current of inductor can be written as.

$$\frac{1}{f_s} = \frac{\Delta I \times L \times V_c}{V_s \times (V_c - V_s)} \tag{3.34}$$

Substitute $V_0 = N \times V_c$ in equation (3.34)

$$\boxed{\Delta I_L = \frac{V_s \times (V_o - N \times V_s)}{f_s \times L \times V_o}} \tag{3.35}$$

Equation (3.35) represents ripple current of the inductor for N level MBC with Resrl = 0

3.5(A) CRITICAL VALUE OF INDUCTANCE ((L_C)) WITHOUT PARASITIC RESISTANCE: -

The converter inductor current is continuous and to reduce the ripple content proper selection of inductor is required. Critical value of inductance (L_C) is derived below.

$$\Delta I_L = \frac{V_s \times (V_o - N \times V_s)}{f_s \times L \times V_o} = 2I_L = 2I_o \tag{3.36}$$

$$I_o = \frac{V_o}{R} \tag{3.37}$$

Equation 3.37 substitute in equation 3.36

$$\Delta I_L = \frac{V_s \times \left(V_o - N \times V_s\right)}{f_s \times L \times V_0} = 2 \times \frac{V_o}{R} \qquad (3.38)$$

Substituting output voltage equation in equation 3.38,

$$\boxed{L_c = \frac{(1-D) \times (V_o - N \times V_s) \times R}{2 \times N \times f_s \times V_o}} \qquad (3.39)$$

Equation (3.39) represents the critical value of inductance for N level MBC with Resrl = 0. It is clear that the critical value of inductance is directly proportional to load resistance and inversely proportional to the switching frequency.so for high frequency, the value of inductance decreases.

3.5 (B) CRITICAL VALUE OF INDUCTANCE CONSIDERING PARASITIC RESISTANCE

During on condition, inductor voltage

$$V_L = (V_s - I_L \times R_{esrl}) \qquad (3.40)$$

During off condition, inductor voltage

$$-V_L = (V_s - V_c - I_L \times R_{esrl}) \qquad (3.41)$$

$$V_L = (V_c + I_L \times R_{esrl} - V_s) \qquad (3.42)$$

Inductor voltage can be written as, $V_L = \dfrac{L \times \Delta I_L}{\Delta T}$ (3.43)

during on condition, $T_1 = \dfrac{\Delta I_L \times L}{(V_s - I_L \times R_{esrl})}$ (3.44)

during off condition $T_2 = \dfrac{\Delta I \times L}{(V_c + I_L \times R_{esrl} - V_s)}$ (3.45)

$$\Delta I_L = \frac{T_1 \times (V_s - I_L \times R_{esrl})}{L} \qquad (3.46)$$

$$\Delta I_L = \frac{T_2 \times (V_c + I_L \times R_{esrl} - V_s)}{L} \qquad (3.47)$$

From (3.47) and (3.48)

$$\frac{T_1 \times (V_s - I_L \times R_{esrl})}{L} = \frac{T_2 \times (V_c + I_L \times R_{esrl} - V_s)}{L} \tag{3.48}$$

By substituting T_1 = DTs and T_2 = (1-D) Ts in equation (3.48)

$$\frac{DT_s \times (V_s - I_L \times R_{esrl})}{L} = \frac{(1-D)T_s \times (V_c + I_L \times R_{esrl} - V_s)}{L} \tag{3.49}$$

Substituting $V_o = N \times V_c, I_L = I_s = \frac{N \times I_0}{(1-D)}, I_o = \frac{V_o}{R}$

$$V_s = V_c \times (1-D) + I_L \times R_{esrl} \tag{3.50}$$

$$V_s = \frac{V_o \times (1-D)}{N} + \frac{V_o \times N \times R_{esrl}}{(1-D) \times R_o} \tag{3.51}$$

Total time $T_s = T_1 + T_2 = \frac{\Delta I_L \times L}{(V_s - I_L \times R_{esrl})} + \frac{\Delta I_L \times L}{(V_c + I_L \times R_{esrl} - V_s)}$ (3.52)

The ripple current of inductor with some parasitic resistance

$$\Delta I_L = \frac{(V_s - I_L \times R_{esrl}) \times (V_0 + N \times I_L \times R_{esrl} - N \times V_s)}{f_s \times L \times V_0} \tag{3.53}$$

If I_L is the average inductor current, the inductor ripple current $\Delta I = 2I_L$

$$\Delta I_L = \frac{(V_s - I_L \times R_{esrl}) \times (V_0 + N \times I_L \times R_{esrl} - N \times V_s)}{f_s \times L \times V_0} = 2I_0 \tag{3.54}$$

Again equation 3.53 modified to get critical value of inductance,

$$L_c = \frac{(V_s - I_L \times R_{esrl}) \times (V_0 + N \times I_L \times R_{esrl} - N \times V_s)}{2I_0 \times f_s \times V_0} \tag{3.55}$$

The following inequalities decide the boundary for conduction.

$\Delta I_L < 2I_L$, continuous mode of conduction

$\Delta I_L > 2I_L$, discontinuous mode of conduction

3.6 CAPACITOR DESIGN CONSIDERATIONS: -

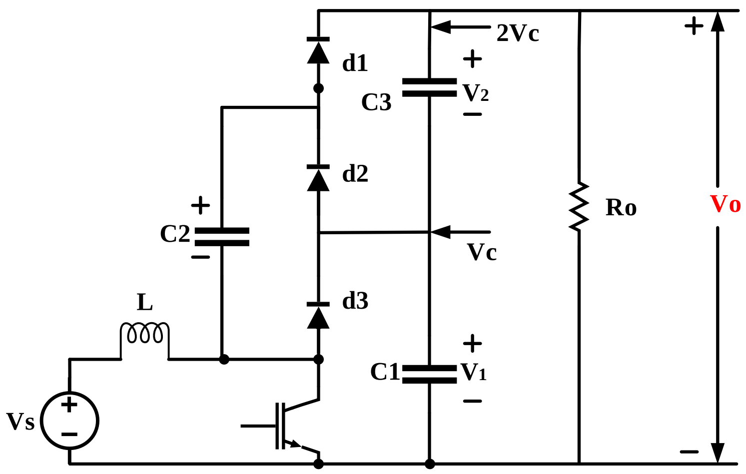

Fig 3.13 Two level MBC

The output voltage depends upon the two capacitor voltages V_1 and V_2. $V_0 = V_1 + V_2 = 2V_c$. The output voltage has some ripple content. It can be reduced by proper selection of capacitance. The critical value of capacitance is derived.

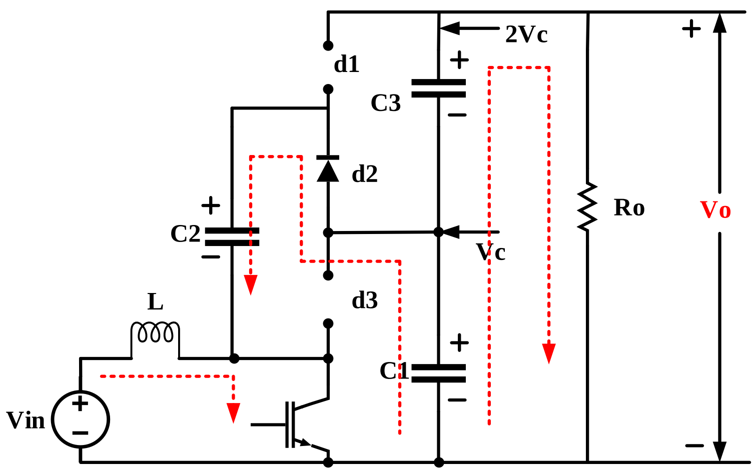

Fig 3.14 Two level MBC during on condition

The following notations are used to derive equations.

V_{1ac} = Voltage after closing switch, capacitor1 is discharging

V_{2ac} = Voltage after closing switch, capacitor2 is charging

Q_{1ac} = The charge of capacitor1 after closing the switch

Q_{2ac} = The charge of capacitor2 after closing the switch

During switch on condition, capacitor1 is discharging and capacitor2 is charging up to the source voltage.

2 LEVEL MBC DURING OFF CONDITION: -

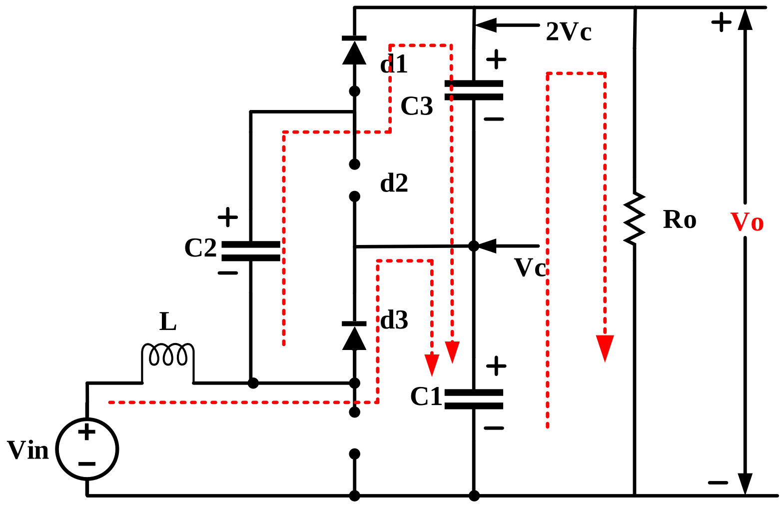

Fig 3.15 Two level boost converter during off condition

V_{1bc} = Voltage before closing the switch, capacitor1 is discharging

V_{2bc} = Voltage before closing the switch, capacitor2 is charging

Q_{1bc} = The charge of capacitor1 before closing the switch

Q_{2bc} = The charge of capacitor2 before closing the switch

During switch off condition, capacitor1 is charging and capacitor2 is discharging so capacitor2 is supplying to capacitor1 and capacitor3.

$$\begin{aligned} V_{1ac} &= V_{1bc} = V_1 \\ V_{2ac} &= V_{2bc} = V_2 \end{aligned} \tag{3.56}$$

In two level MBC, if all capacitors are of same value, then the voltage across capacitor1 V_1 and voltage across capacitor2 V_2 are equal. Voltage across the capacitors can be synthesised as (3.56). Here charge is exchanged between both capacitors as well as it is transferred to load.

Three levels MBC consist of 5 capacitors, but charge exchanged between four capacitors.

For N level MBC consist of "$2N-1$", but charge is transferred between "$2N-2$" no of capacitors.

$$V_{1ac} = V_{2ac} = \frac{V_{1bc}C_1 + V_{2bc}C_2}{C_1 + C_2} = \frac{Q_{1bc} + Q_{2bc}}{C_1 + C_2} \quad (3.57)$$

$$V_{1bc} = V_{2bc} = \frac{V_{1ac}C_1 + V_{2ac}C_2}{C_1 + C_2} \text{ (or) } \frac{Q_{1ac} + Q_{2ac}}{C_1 + C_2} \quad (3.58)$$

Similarly, for N level MBC can be synthesised as,

$$V_{1ac} = V_{2ac} = V_{3ac} = \text{..........}V_{(2N-2)ac} = \frac{V_{1bc}C_1 + V_{2bc}C_2 + V_{3bc}C_3 + \text{..................}V_{(2N-2)bc}C_{2N-2}}{C_1 + C_2 + C_3 + \text{................}C_{2N-2}}$$

(or)

$$V_{1ac} = V_{2ac} = V_{3ac} = \text{..........}V_{(2N-2)ac} = \frac{Q_{1bc} + Q_{2bc} + Q_{3bc} + \text{..................}Q_{(2N-2)bc}}{C_1 + C_2 + C_3 + \text{................}C_{2N-2}}$$

$$V_{1bc} = V_{2bc} = V_{3bc} = \text{..........}V_{(2N-2)bc} = \frac{V_{1ac}C_1 + V_{2ac}C_2 + V_{3ac}C_3 + \text{..................}V_{(2N-2)ac}C_{2N-2}}{C_1 + C_2 + C_3 + \text{................}C_{2N-2}}$$

(or)

$$V_{1bc} = V_{2bc} = V_{3bc} = \text{..........}V_{(2N-2)bc} = \frac{Q_{1ac} + Q_{2ac} + Q_{3ac} + \text{..................}Q_{(2N-2)ac}}{C_1 + C_2 + C_3 + \text{................}C_{2N-2}}$$

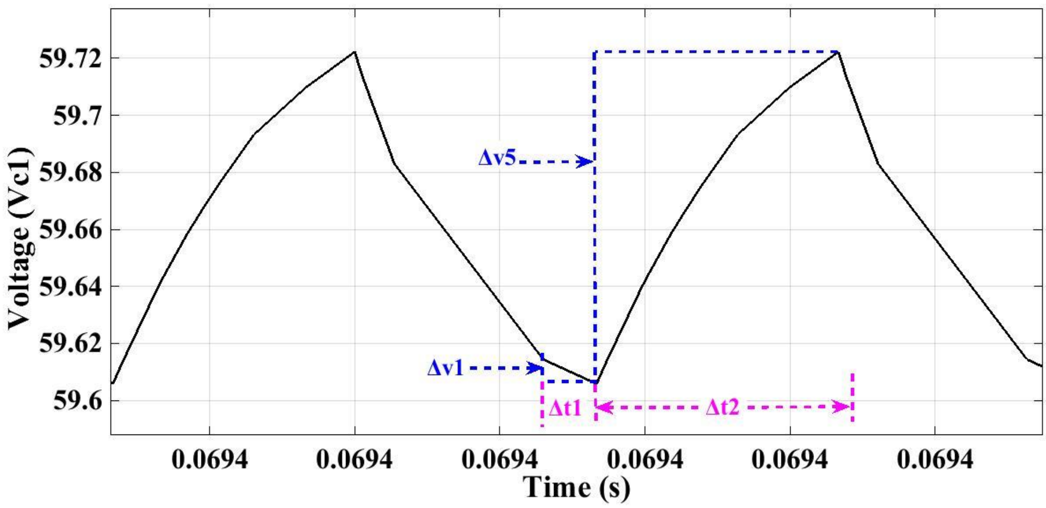

Fig 3.16 Voltage across capacitor 1

During on period the capacitor C_1 charges C_2, the Voltage drop is shown as ΔV_1 and in the off period the capacitor gets charged from the source, the change in voltage is shown as ΔV5.Here Δt_1 indicate switch on condition, and $\Delta t_3 + \Delta t_4 = \Delta t_2$ indicates switch off condition. The change in voltage across capacitor1 during on and off periods is ΔV_1, ΔV_5 respectively. It can be synthesised as,

$$\Delta V_1 = -\frac{1}{C_1}(Ic_2 + I_{out})\Delta t_1 \tag{3.59}$$

$$\Delta V_5 = \frac{1}{C_1}(I_L - I_{out})\Delta t_2 \tag{3.60}$$

The negative sign in (3.59) is due to the fact that the current through the capacitor is opposite during on and off period.

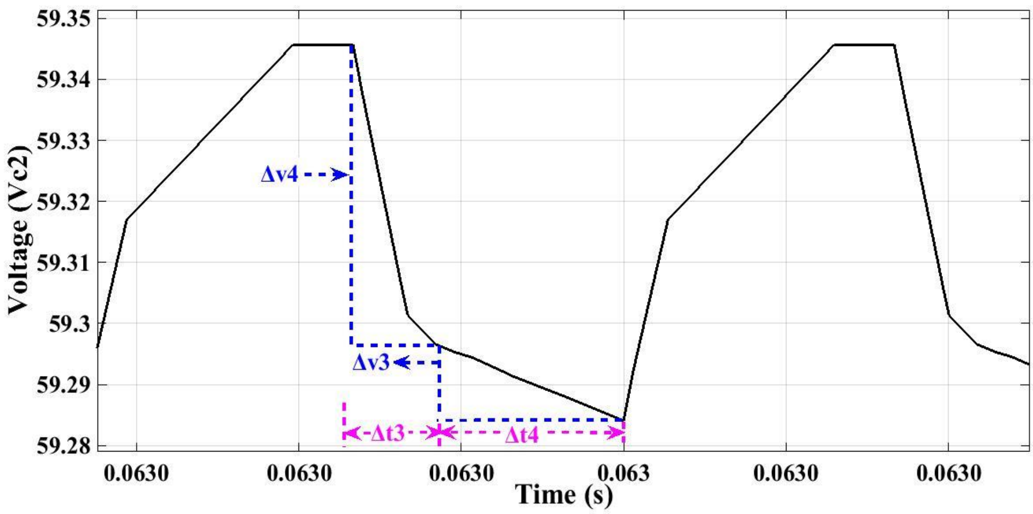

Fig 3.17 Voltage across capacitor 2

During on period ,the capacitor charges up to Vc_1 ($Vc_1 = Vc_2$). During off period, Vc_2 decreases. The drop in voltage can be splitted in two parts as shown in Fig 3.17. In first part capacitor C_2 charges capacitor C_3, the drop in voltage is shown as ΔV_4.In second part capacitor C_2 and C_3 along with C_1 supply the load, the drop in voltage across C_2 is shown as ΔV_3 .

Similarly, for capacitor C_2

$$\Delta V_4 = \frac{1}{C_2}(I_L - I_{out})\Delta t_3 \tag{3.61}$$

$$\Delta V_3 = \frac{1}{C_2}(I_L)\Delta t_4 \tag{3.62}$$

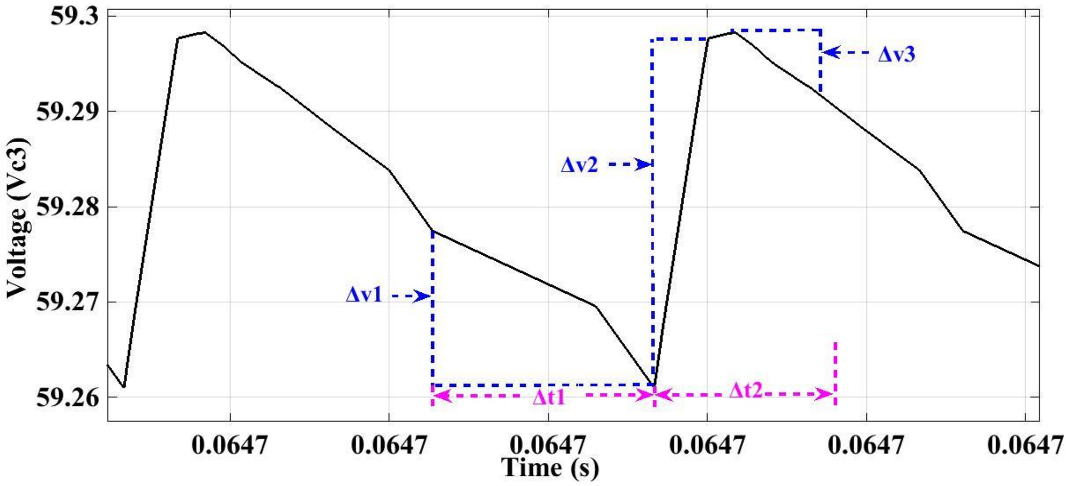

Fig 3.18 Voltage across capactior3

The voltage across capacitor (Vc_3) is shown in Fig 3.18. The capacitor has voltage drops as (ΔV_1), (ΔV_2) and (ΔV_3). These drops are due to switching action. During on condition capacitor(C_3) discharges through load, drop is (ΔV_1). During switch off condition, initially capacitor (C_3) charges(ΔV_2) and then discharges (ΔV_3) as shown in Fig 3.18.

For capacitor C_3,

$$\Delta V_1 = \frac{1}{C_3}(I_{out})\Delta t_1 \tag{3.63}$$

$$\Delta V_3 = \Delta V_2 = \frac{1}{C_3}(I_L - I_{out})\Delta t_5 \tag{3.64}$$

3.6.1 CRITICAL VALUE OF CAPACITANCE: -

To reduce the ripple across capacitors as well as to get desired conduction mode , suitable value of capacitor selection is necessary. Critical value of capacitor is derived below.

$$\text{Change in voltage across capacitor1} = \text{Voltage}\Big|_{\text{during on period}} + \text{Voltage}\Big|_{\text{during off period}}$$

In this critical capacitance calculation derived for capacitance1 (C_1) equation written below.

Capacitance1(C_1) has two voltage drops during on-state voltage drop1 (ΔV_1) and during off-state voltage drops5 (ΔV_5) is shown in Fig 3.16.

$$\Delta V_{C1} = \frac{1}{C_1}\left(-\int_0^{T_{on}} (I_{C2} + I_{out})dt + \int_{T_{on}}^{T} (I_S - I_{out})dt \right) \tag{3.65}$$

From (3.65),

$$\mathbf{\Delta V_{C1}} = \left(\left(\frac{(1-D)\times T\times I_s}{C_1}\right)-\left(\frac{T\times I_{out}}{C_1}\right)\right) \tag{3.66}$$

Capacitor   have two voltage levels, maximum and minimum voltage.

Ripple voltage, ΔV_C = maximum voltage – minimum voltage

Average voltage across capacitor, Va = (maximum voltage level – minimum voltage level)/2

the ripple voltage,

$$\Delta V_C = 2Va \qquad (\therefore V_a = I_a \times R) \tag{3.67}$$

Equation (3.66) substitute in equation (3.67)

$$\mathbf{\Delta V_{C1}} = \left(\left(\frac{(1-D)\times T\times I_s}{C_1}\right)-\left(\frac{T\times I_{out}}{C_1}\right)\right) = \frac{2V_a}{N} \tag{3.68}$$

Equation ($\therefore V_a = I_a \times R$) substitute in equation (3.68)

$$\mathbf{\Delta V_{C1}} = \left(\left(\frac{(1-D)\times T\times I_s}{C_1}\right)-\left(\frac{T\times I_{out}}{C_1}\right)\right) = \frac{2(I_a \times R)}{N} \tag{3.69}$$

From Fig (3.13), each capacitor voltage is load voltage divided by N level, so drop of particular capacitor is equal to two times of average voltage divided by N level.

After modifying equation (3.69)

$$\boxed{C_c = \frac{N\times\left((1\text{-}D)\times T\times I_s\text{-}T\times I_{out}\right)}{2(I_a\times R)}} \tag{3.70}$$

Equation (3.70) indicates the critical capacitance (C_C).

3.7 STATE SPACE MODELLING AND CONTROL OF A DC–DC MBC:

Multilevel DC-DC boost converter consisting of (2N-1) capacitors and one inductor is a 2Nth order system. For 2 level MBC consisting of 3 capacitors and one inductor has a fourth order representation. Two level MBC topology is shown in Fig 3.13. Full order state space matrices for two level is derived below. (Assumption, the capacitor C1 and C2 don't have any transient when they are connected in parallel)

DURING ON CONDITION ($T_1 = DT_s$): -

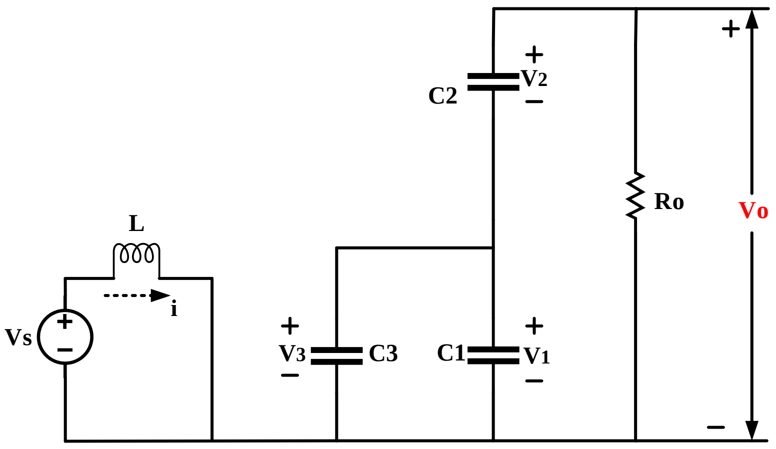

Fig 3.19 Equivalent circuit of two level MBC during on condition

$$\frac{di_L}{dt} = \frac{V_s}{L} \tag{3.71}$$

$$\frac{dV_1}{dt} = -\frac{V_1}{R(C_1 + C_3)} - \frac{V_2}{R(C_1 + C_3)} \tag{3.72}$$

$$\frac{dV_1}{dt} = -\frac{V_1}{RC_2} - \frac{V_2}{RC_2} \tag{3.73}$$

$$\frac{dV_3}{dt} = -\frac{V_1}{R(C_1 + C_3)} - \frac{V_2}{R(C_1 + C_3)} \tag{3.74}$$

From (3.71-3.74),

$$\begin{bmatrix} \frac{di_L}{dt} \\ \frac{dv_1}{dt} \\ \frac{dv_2}{dt} \\ \frac{dv_3}{dt} \end{bmatrix} = \begin{bmatrix} 0 & 0 & 0 & 0 \\ 0 & -\frac{1}{R(C_1+C_3)} & -\frac{1}{R(C_1+C_3)} & 0 \\ 0 & -\frac{1}{RC_2} & -\frac{1}{RC_2} & 0 \\ 0 & -\frac{1}{R(C_1+C_3)} & -\frac{1}{R(C_1+C_3)} & 0 \end{bmatrix} \begin{bmatrix} i_L \\ v_1 \\ v_2 \\ v_3 \end{bmatrix} + \begin{bmatrix} \frac{1}{L} \\ 0 \\ 0 \\ 0 \end{bmatrix} V_s$$

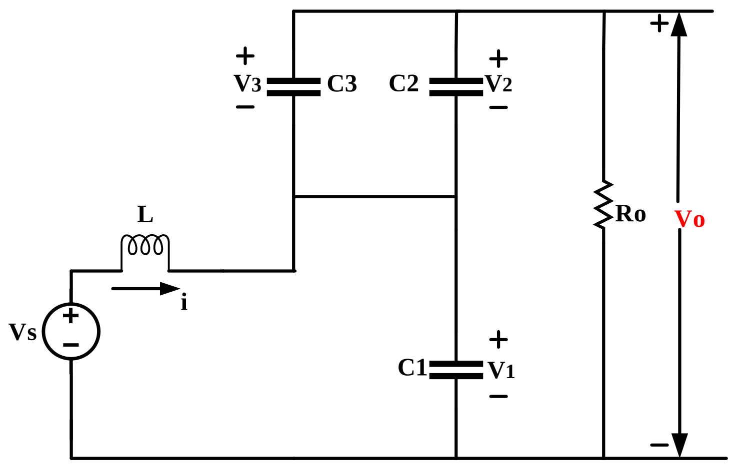

Fig 3.20 Equivalent circuit of two level MBC during off condition

From Fig3.19 and Fig3.20,

$$\frac{di_L}{dt} = -\frac{V_1}{L} + \frac{V_s}{L} \tag{3.75}$$

$$\frac{dV_1}{dt} = \frac{i}{C_1} - \frac{V_1}{RC_1} - \frac{V_2}{RC_1} \tag{3.76}$$

$$\frac{dV_2}{dt} = -\frac{V_1}{R(C_1 + C_2)} - \frac{V_2}{R(C_1 + C_2)} \tag{3.77}$$

$$\frac{dV_3}{dt} = -\frac{V_1}{R(C_2 + C_3)} - \frac{V_2}{R(C_2 + C_3)} \tag{3.78}$$

From (3.75-3.78),

$$\begin{bmatrix} \frac{di_L}{dt} \\ \frac{dv_1}{dt} \\ \frac{dv_2}{dt} \\ \frac{dv_3}{dt} \end{bmatrix} = \begin{bmatrix} 0 & -\frac{1}{L} & 0 & 0 \\ \frac{1}{C_1} & -\frac{1}{RC_1} & -\frac{1}{RC_1} & 0 \\ 0 & -\frac{1}{R(C_1+C_2)} & -\frac{1}{R(C_1+C_2)} & 0 \\ 0 & -\frac{1}{R(C_2+C_3)} & -\frac{1}{R(C_2+C_3)} & 0 \end{bmatrix} \begin{bmatrix} i_L \\ v_1 \\ v_2 \\ v_3 \end{bmatrix} + \begin{bmatrix} \frac{1}{L} \\ 0 \\ 0 \\ 0 \end{bmatrix} V_s$$

Output equation can be written as,

$$V_o = V_c, \; I_g = i_L$$

$$\begin{bmatrix} V_o \\ I_g \end{bmatrix} = \begin{bmatrix} 0 & 1 \\ 1 & 0 \end{bmatrix} \begin{bmatrix} i_L \\ V_c = v_1 + v_2 \end{bmatrix}$$

Average large signal modelling: - Average large signal modelling of full order dc-dc converter is presented below.

$$A = A_1 d + A_2 (1-d)$$

$$B = B_1 d + B_2 (1-d)$$

$$C = C_1 d + C_2 (1-d)$$

$$D = D_1 d + D_2 (1-d)$$

In above equations A_1, B_1, C_1, D_1 are on state matrices and A_2, B_2, C_2, D_2 are off state matrices. A, B, C, D state space matrices are found out for particular dc-dc converter, but large signal modelling for MBC full order circuit is very complex. A two level MBC considering equivalent capacitance is discussed below.

3.7.1 Reduced Order Non-Linear Dynamic Modelling of Two Level MBC: -

In full order modelling, the order of the system increases with the increase of output levels. The steady state as well as small signal modelling for higher order system is very complex. For simplicity, a reduced order model, considering equivalent capacitance during on and off period is presented.

During ON condition (DTs): -

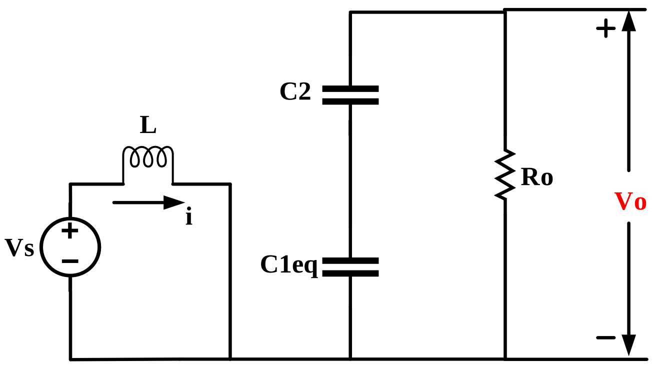

Fig 3.21 Equivalent circuit of reduced order model of two-level MBC (On period)

From Fig 3.21,

$$L\frac{di_L}{dt}=V_s \tag{3.79}$$

$$C_{1eq}\frac{dv}{dt}=-\frac{N}{R}\times V \tag{3.80}$$

During OFF condition,

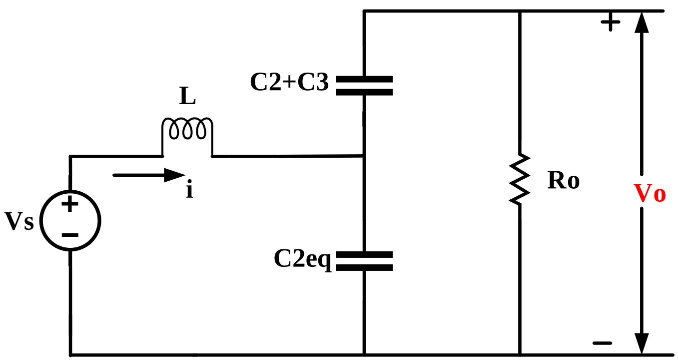

Fig 3.22 Equivalent circuit of reduced order model of two-level MBC (Off period)

From Fig 3.22,

$$L\frac{di_L}{dt}=-\frac{V}{N}+V_s \tag{3.81}$$

$$C_{2eq}\frac{dv}{dt}=i-\frac{N}{R}\times V \tag{3.82}$$

From (3.79-3.82),

$$L\frac{di_L}{dt}=-(1-D)\frac{V}{N}+V_s \tag{3.83}$$

$$C_{eq}\frac{dv}{dt}=(1-D)i-\frac{N}{R}\times V \quad \{\therefore C_{eq}=C_{1eq}+C_{2eq}\} \tag{3.84}$$

From (3.83, 3.84), resultant state space matrix is given as

$$\begin{bmatrix}\frac{di_L}{dt}\\ \frac{dv_c}{dt}\end{bmatrix}=\begin{bmatrix}0 & -\frac{(1-D)}{N\times L}\\ \frac{(1-D)}{C_{eq}} & -\frac{N}{R\times C_{eq}}\end{bmatrix}\begin{bmatrix}i_L\\ v_c\end{bmatrix}+\begin{bmatrix}\frac{1}{L}\\ 0\end{bmatrix}V_s \tag{3.85}$$

Output equations of reduced order model for two level MBC.

$$V_0 = V_c$$

$$I_g = i_L$$

$$\begin{bmatrix} V_0 \\ I_g \end{bmatrix} = \begin{bmatrix} 0 & 1 \\ 1 & 0 \end{bmatrix} \begin{bmatrix} i_L \\ V_c \end{bmatrix}$$

3.7.2 STEADY STATE MODELLING OF REDUCED ORDER 2 LEVEL MBC

Steady state condition is represented as, $\frac{di_L}{dt} = 0$, $\frac{dv_c}{dt} = 0$.

From (3.86), the steady state representation is

$$\begin{bmatrix} 0 \\ 0 \end{bmatrix} = \begin{bmatrix} 0 & -\frac{(1-D)}{N \times L} \\ \frac{(1-D)}{C_{eq}} & -\frac{N}{R \times C_{eq}} \end{bmatrix} \begin{bmatrix} i_L \\ v_c \end{bmatrix} + \begin{bmatrix} \frac{1}{L} \\ 0 \end{bmatrix} V_s \tag{3.86}$$

$$\begin{bmatrix} V_0 \\ I_g \end{bmatrix} = \begin{bmatrix} 0 & 1 \\ 1 & 0 \end{bmatrix} \begin{bmatrix} i_L \\ V_c \end{bmatrix} \tag{3.87}$$

$$\frac{dx}{dt} = 0 = Ax + Bu \Longrightarrow X = -A^{-1}BU \tag{3.88}$$

$$y = Cx \Longrightarrow Y = -CA^{-1}BU \Longrightarrow \frac{Y}{U} = -CA^{-1}B \tag{3.89}$$

From (3.88, 3.89) we can write,

$$V_o = \begin{bmatrix} 0 & 1 \end{bmatrix} \begin{bmatrix} i_L \\ V_c \end{bmatrix}$$

From (3.89),

$$V_o = -CA^{-1} \begin{bmatrix} \frac{1}{L} \\ 0 \end{bmatrix} V_s \tag{3.90}$$

$$C = \begin{bmatrix} 0 & 1 \end{bmatrix},\ A = \begin{bmatrix} 0 & -\frac{(1-D)}{N \times L} \\ \frac{(1-D)}{C_{eq}} & -\frac{N}{R \times C_{eq}} \end{bmatrix}$$

$$Vo = -\begin{bmatrix} 0 & 1 \end{bmatrix} \begin{bmatrix} 0 & -\frac{(1-D)}{N \times L} \\ \frac{(1-D)}{C_{eq}} & -\frac{N}{R \times C_{eq}} \end{bmatrix}^{-1} \begin{bmatrix} \frac{1}{L} \\ 0 \end{bmatrix} V_s \tag{3.91}$$

$$Vo = -\begin{bmatrix} 0 & 1 \end{bmatrix} \left(\frac{N \times L \times C_{eq}}{(1-d)^2}\right) \begin{bmatrix} \frac{N}{RC_{eq}} & -\frac{(1-D)}{N \times L} \\ -\frac{(1-D)}{C_{eq}} & 0 \end{bmatrix} \begin{bmatrix} \frac{1}{L} \\ 0 \end{bmatrix} V_s \tag{3.92}$$

From (3.92), the gain of the converter is synthesised as

$$V_o = \frac{N \times V_s}{(1-D)}$$

3.7.3 SMALL-SIGNAL MODELLING OF REDUCED ORDER TWO LEVEL MBC

Multilevel DC-DC converter is a non-linear system. To linearize the system, a small change in variable quantity is inserted like $d = D + \hat{d}$, $v_0 = V_0 + \hat{v}_0$, $i_L = I_L + \hat{i}_L$, $v_c = V_c + \hat{v}_c$, $v_s = V_s + \hat{v}_s$, $i_g = I_g + \hat{i}_g$, substituting all in below matrices.

$$\begin{bmatrix} \frac{di_L}{dt} \\ \frac{dv_c}{dt} \end{bmatrix} = \begin{bmatrix} 0 & -\frac{(1-d)}{N \times L} \\ \frac{(1-d)}{C_{eq}} & -\frac{N}{R \times C_{eq}} \end{bmatrix} \begin{bmatrix} i_L \\ v_c \end{bmatrix} + \begin{bmatrix} \frac{1}{L} \\ 0 \end{bmatrix} V_s \tag{3.93}$$

$$\begin{bmatrix} V_0 \\ I_g \end{bmatrix} = \begin{bmatrix} 0 & 1 \\ 1 & 0 \end{bmatrix} \begin{bmatrix} i_L \\ V_c \end{bmatrix} \tag{3.94}$$

Substituting the all small perturbations in above state space matrices shown above (3.93, 3.94).

$$\begin{bmatrix} \dfrac{d(I_L+\hat{i}_L)}{dt} \\ \dfrac{d(V_c+\hat{v}_c)}{dt} \end{bmatrix} = \begin{bmatrix} 0 & -\dfrac{(1-D-\hat{d})}{N\times L} \\ \dfrac{(1-D-\hat{d})}{C_{eq}} & -\dfrac{N}{R\times C_{eq}} \end{bmatrix} \begin{bmatrix} I_L+\hat{i}_L \\ V_c+\hat{v}_c \end{bmatrix} + \begin{bmatrix} \dfrac{1}{L} \\ 0 \end{bmatrix} (V_s+\hat{v}_s) \quad (3.95)$$

$$\begin{bmatrix} V_0+\hat{v}_0 \\ I_g+\hat{i}_g \end{bmatrix} = \begin{bmatrix} 0 & 1 \\ 1 & 0 \end{bmatrix} \begin{bmatrix} I_L+\hat{i}_L \\ V_c+\hat{v}_c \end{bmatrix} \quad (3.96)$$

A small signal based state space matrices are shown above (3.95, 3.96). From these matrices separate steady state and small signal quantities are derived.

$$\begin{bmatrix} \dfrac{d(I_L+\hat{i}_L)}{dt} \\ \dfrac{d(V_c+\hat{v}_c)}{dt} \end{bmatrix} = \begin{bmatrix} 0 & -\dfrac{(1-D)}{N\times L} \\ \dfrac{(1-D)}{C_{eq}} & -\dfrac{N}{R\times C_{eq}} \end{bmatrix} \begin{bmatrix} i_L \\ v_c \end{bmatrix} + \begin{bmatrix} 0 & -\dfrac{(1-D)}{N\times L} \\ \dfrac{(1-D)}{C_{eq}} & -\dfrac{N}{R\times C_{eq}} \end{bmatrix} \begin{bmatrix} \hat{i}_L \\ \hat{v}_c \end{bmatrix}$$

$$+ \begin{bmatrix} 0 & \dfrac{\hat{d}}{N\times L} \\ -\dfrac{\hat{d}}{C_{eq}} & 0 \end{bmatrix} \begin{bmatrix} I_L \\ V_c \end{bmatrix} + \begin{bmatrix} \dfrac{1}{L} \\ 0 \end{bmatrix} (V_s+\hat{v}_s) + \begin{bmatrix} 0 \\ -\dfrac{1}{C_{eq}} \end{bmatrix} (I_z+\hat{i}_z) \quad (3.97)$$

$$\begin{bmatrix} V_0+\hat{v}_0 \\ I_g+\hat{i}_g \end{bmatrix} = \begin{bmatrix} 0 & 1 \\ 1 & 0 \end{bmatrix} \begin{bmatrix} I_L+\hat{i}_L \\ V_c+\hat{v}_c \end{bmatrix} \quad (3.98)$$

In above small signal state space matrix shown in (3.97) in that blue colour matrix becomes zero, because blue colour matrix is a steady state matrix.

$$\begin{bmatrix} \dfrac{d(\hat{i}_L)}{dt} \\ \dfrac{d(\hat{v}_c)}{dt} \end{bmatrix} = \begin{bmatrix} 0 & -\dfrac{(1-D)}{N\times L} \\ \dfrac{(1-D)}{C_{eq}} & -\dfrac{N}{R\times C_{eq}} \end{bmatrix} \begin{bmatrix} \hat{i}_L \\ \hat{v}_c \end{bmatrix} + \begin{bmatrix} 0 & \dfrac{\hat{d}}{N\times L} \\ -\dfrac{\hat{d}}{C_{eq}} & 0 \end{bmatrix} \begin{bmatrix} I_L \\ V_c \end{bmatrix} + \begin{bmatrix} \dfrac{1}{L} \\ 0 \end{bmatrix} (\hat{v}_s) + \begin{bmatrix} 0 \\ -\dfrac{1}{C_{eq}} \end{bmatrix} (\hat{i}_z)$$

$$\begin{bmatrix} \hat{v}_0 \\ \hat{i}_g \end{bmatrix} = \begin{bmatrix} 0 & 1 \\ 1 & 0 \end{bmatrix} \begin{bmatrix} \hat{i}_L \\ \hat{v}_c \end{bmatrix}$$

Combining above matrices, B_1 B_2 B_3

$$\begin{bmatrix} \frac{d(\hat{i}_L)}{dt} \\ \frac{d(\hat{v}_c)}{dt} \end{bmatrix} = \begin{bmatrix} 0 & -\frac{(1-D)}{N \times L} \\ \frac{(1-D)}{C_{eq}} & -\frac{N}{R \times C_{eq}} \end{bmatrix} \begin{bmatrix} \hat{i}_L \\ \hat{v}_c \end{bmatrix} + \begin{bmatrix} \frac{1}{L} & 0 & \frac{V_c}{N \times L} \\ 0 & -\frac{1}{C_{eq}} & -\frac{I_L}{C_{eq}} \end{bmatrix} \begin{bmatrix} \hat{v}_s \\ \hat{i}_z \\ \hat{d} \end{bmatrix} \quad (3.99)$$

$$\begin{bmatrix} \hat{v}_0 \\ \hat{i}_g \end{bmatrix} = \begin{bmatrix} 0 & 1 \\ 1 & 0 \end{bmatrix} \begin{bmatrix} \hat{i}_L \\ \hat{v}_c \end{bmatrix} \quad (3.100)$$

Transfer function model from the state space representation: -

$$\frac{dx}{dt} = Ax + Bu \Longrightarrow SX(S) = AX(S) + BU(S)$$

$$y = cx \Longrightarrow Y(S) = CX(S)$$

$$X(S) = (SI - A)^{-1} BU(S)$$

$$Y(S) = C(SI - A)^{-1} BU(S) \text{ \{transfer function between input and output\}}$$

In below all transfer functions depends on the columns of B_1, B_2, B_3 of (B) state space matrix (3.99).

$$\frac{\hat{v}_0}{\hat{d}} = C(SI - A)^{-1} B_3 \text{ \{control output voltage gain @ } \hat{v}_s = 0,\ \hat{i}_z = 0 \text{\}}$$

$$\frac{\hat{v}_0}{\hat{v}_s} = C(SI - A)^{-1} B_1 \text{\{audio susceptibility @ } \hat{d} = 0,\ \hat{i}_z = 0 \text{\}}$$

$$\frac{\hat{v}_0}{\hat{i}_z} = C(SI - A)^{-1}B_2 \text{ \{output impedance @ } \hat{d} = 0,\ \hat{v}_s = 0\text{ \}}$$

$$\frac{\hat{v}_s}{\hat{i}_g} \text{ \{input impedance @ } \hat{d} = 0,\ \hat{i}_z = 0\text{ \}}$$

$$\hat{i}_g = \begin{bmatrix} 0 & 1 \end{bmatrix} x$$

$$\hat{i}_g = \begin{bmatrix} 0 & 1 \end{bmatrix} (SI - A)^{-1} B_2 \hat{v}_s$$

$$\frac{\hat{i}_g}{\hat{d}} \text{ \{control current gain @ } \hat{v}_s = 0,\ \hat{i}_z = 0\text{ \}}$$

$$\hat{i}_g = \begin{bmatrix} 0 & 1 \end{bmatrix} x$$

$$\hat{i}_g = \begin{bmatrix} 0 & 1 \end{bmatrix} (SI - A)^{-1} B_3 \hat{d}$$

This small signal model is used to find transfer functions of the converter. These are useful for stability analysis. Stability of this converter can be explained by Bode plot, root locus, Nyquist plot etc. Bode plots of the transfer functions are shown in chapter (4).

The transfer function of the output voltage ($\hat{v}_0$) and duty cycle($\hat{d}$): -

This transfer function between the output voltage ($\hat{v}_0$) and duty cycle ($\hat{d}$) according to the equation $\frac{\hat{v}_0}{\hat{d}} = C(SI - A)^{-1}B_3$.

$$\hat{v}_0 = C(SI - A)^{-1} B_3 \hat{d} \qquad (3.101)$$

$$C = \begin{bmatrix} 0 & 1 \end{bmatrix},\ A = \begin{bmatrix} 0 & -\frac{(1-D)}{N \times L} \\ \frac{(1-D)}{C_{eq}} & -\frac{N}{R \times C_{eq}} \end{bmatrix},\ B_3 = \begin{bmatrix} \frac{V_c}{N \times L} \\ -\frac{I_L}{C_{eq}} \end{bmatrix}$$

$$\hat{v}_0 = \begin{bmatrix} 0 & 1 \end{bmatrix} \begin{bmatrix} S & \frac{(1-D)}{N \times L} \\ -\frac{(1-D)}{C_{eq}} & S + \frac{N}{R \times C_{eq}} \end{bmatrix}^{-1} \begin{bmatrix} \frac{V_c}{N \times L} \\ -\frac{I_L}{C_{eq}} \end{bmatrix} \hat{d}$$

The transfer function between the output voltage and duty cycle is,

$$\frac{\hat{v}_0}{\hat{d}} = \frac{\frac{(1-D)V_c}{N \times L} - \frac{S \times I_L}{C_{eq}}}{S^2 + \frac{S \times N}{RC_{eq}} + \frac{(1-D)^2}{N \times L \times C_{eq}}} \quad (3.102)$$

$V_c = V_o, I_L = I_s$ are steady-state quantities substitute in (3.102)

$$\frac{\hat{v}_0}{\hat{d}} = \frac{\frac{(1-D)V_o}{N \times L} - \frac{S \times I_s}{C_{eq}}}{S^2 + \frac{S \times N}{RC_{eq}} + \frac{(1-D)^2}{N \times L \times C_{eq}}} \quad (3.103)$$

(3.103) represents the small signal non-linear dynamic modelling theoretical transfer function between the output voltage and duty cycle of reduced order model of 2 level MBC. Transfer function (3.103) is a non-minimum phase system because one zero at right-hand side and two poles at left-hand side, so this transfer function is stable but bode plot doesn't exist because it is non-minimum phase system, while the phase angle of non-minimum phase system is more than minimum phase system.

The transfer function of the output voltage ($\hat{v}_0$) and the input voltage($\hat{v}_s$): -

This transfer function between small signal output voltage to small signal input voltage according to the equation $\frac{\hat{v}_0}{\hat{v}_s} = C(SI - A)^{-1}B_1$.

$$\frac{\hat{v}_0}{\hat{v}_s} = C(SI - A)^{-1}B_1 \quad (3.104)$$

$$C = \begin{bmatrix} 0 & 1 \end{bmatrix},\ A = \begin{bmatrix} 0 & -\dfrac{(1-D)}{N \times L} \\ \dfrac{(1-D)}{C_{eq}} & -\dfrac{N}{R \times C_{eq}} \end{bmatrix},\ B_1 = \begin{bmatrix} \dfrac{1}{L} \\ 0 \end{bmatrix}$$

$$\hat{v}_0 = \begin{bmatrix} 0 & 1 \end{bmatrix} \begin{bmatrix} S & \dfrac{(1-D)}{N \times L} \\ -\dfrac{(1-D)}{C_{eq}} & S + \dfrac{N}{R \times C_{eq}} \end{bmatrix}^{-1} \begin{bmatrix} \dfrac{1}{L} \\ 0 \end{bmatrix} \hat{v}_s$$

The transfer function between the output and input voltage is obtained as,

$$\frac{\hat{v}_0}{\hat{v}_s} = \frac{\dfrac{(1-D)}{C_{eq}} \times \dfrac{1}{L}}{S^2 + \dfrac{S \times N}{RC_{eq}} + \dfrac{(1-D)^2}{N \times L \times C_{eq}}} \tag{3.105}$$

Equation (3.105) represents the small signal non-linear dynamic modelling theoretical transfer function between the output voltage and input voltage of reduced order model of 2 level MBC. Transfer function (3.105), we can observe that it is minimum phase system because no zeros and poles on right hand side all poles in left hand side, so it is a stable.

3.8 THREE LEVEL MBC OPEN AND CLOSED LOOP CIRCUIT MODEL

Open loop model for three levels MBC is shown in Fig.3.23.

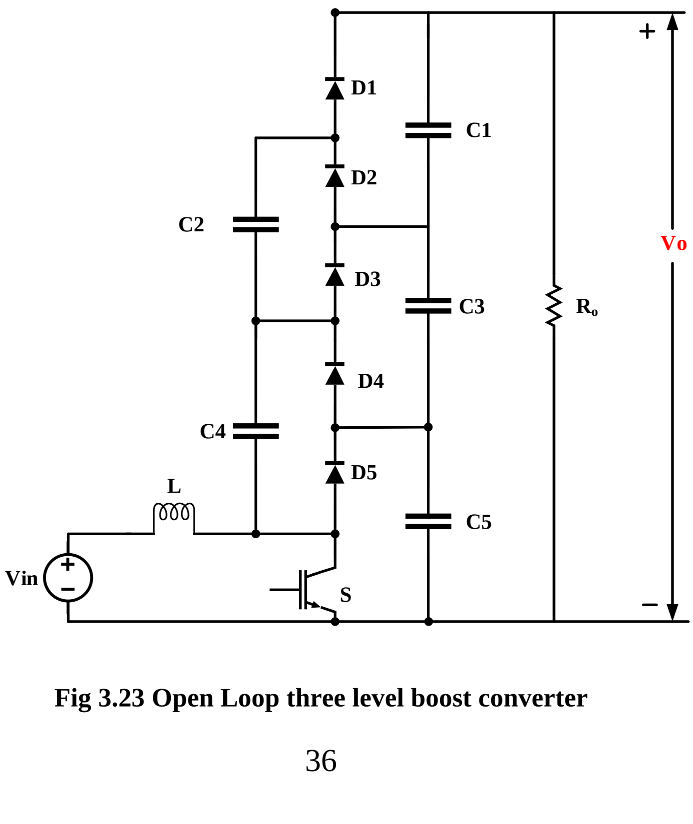

Fig 3.23 Open Loop three level boost converter

Fig 3.24 represents 3 level boost converter closed loop model. This model mainly concerns for the ratio between load and source resistance. The proposed closed loop system is basically to obtain constant output voltage. In case of any load or source side variation, the output changes. Output depends on duty cycle. So a suitable integral controller is designed to change the duty cycle, keeping output constant.

$$V_s = \frac{V_0 \times (1-D)}{N} + \frac{V_0 \times N \times R_{esrl}}{(1-D) \times R_0}$$

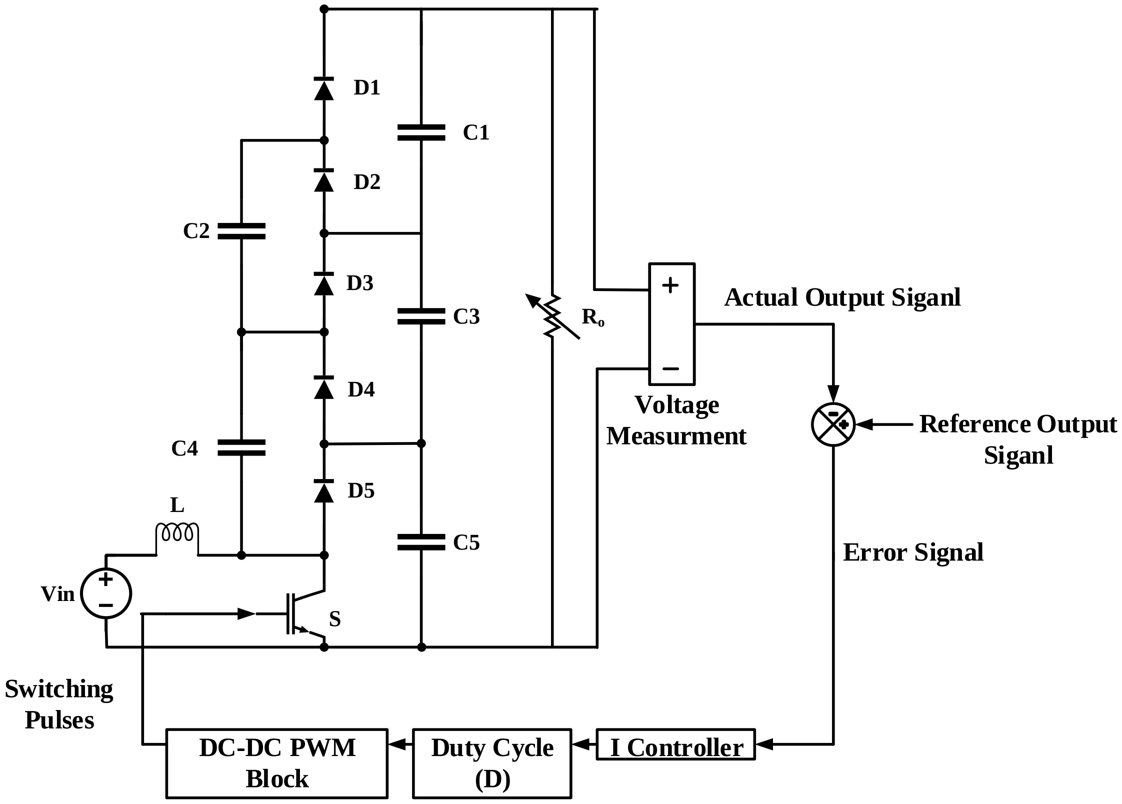

Fig 3.24 Closed loop three level boost converter

The boost converter responses like output current, input current, output voltage changes with the change of load or source resistance.

a. As the load resistance increases keeping source resistance constant, the settling time as well as oscillations increases,
b. As the load resistance decreases, the settling time and oscillations decreases.

Settling time of converter for MBC converter as the load resistance increases, keeping source resistance constant is shown in the chapter (4).

To find the efficiency of the proposed converter.

For loss less converter system,

$$V_s \times I_s = V_o \times I_o$$

$$\eta = \frac{\text{output power}}{\text{Input power}}$$

$$\eta \times \text{Input power} = \text{output power}$$

$$\eta \times V_s \times I_s = V_o \times I_o \qquad (3.106)$$

From (3.7, 3.10,3.105)

$$\eta = \frac{V_o(1-D)}{N \times V_s} \qquad (3.107)$$

Other way of calculating the efficiency of MBC converter, equations are written below.

$$\eta = \frac{V_{out}}{NV_c} = \frac{NV_c - (N-1) \times 4\,V_d}{NV_c} \qquad (3.108)$$

Equations (3.106) and (3.107) represent efficiency of MBC converter.

The actual efficiency of MBC converter is obtained considering all power loss calculations across all components.

$$\eta = \frac{\text{output power}}{\text{Input power}}$$

$$\eta = \frac{(\text{Input power}) - (\text{power loss})}{\text{Input power}} \qquad (3.109)$$

Power losses of MBC,

$$P_{switch} = V_{switch} \times I_{(switch,\ avg)} + R_{switch} \times (I^2_{sw,rms}) \qquad (3.110)$$

$$P_{inductor} = R_L \times I^2_{s,rms} \qquad (3.111)$$

$$P_{diode} = R_d \times (I_o)^2 + V_F \times I_o \qquad (3.112)$$

Equation (3.109) represents power loss in switch during only on state. Equation (3.110) represents power loss in inductor and (3.111) is power loss across the diode due to internal resistance

Substituting equations (3.109, 3.110, 3.111) in equation (3.108), the actual efficiency of converter written below.

$$\eta = \frac{P_{in} - (P_{switch} + P_{inductor} + (2N-1) \times P_{diode})}{P_{in}} \qquad (3.113)$$

3.9 APPLICATIONS OF MBC CONVERTER

The proposed converter is expected to be much more dominating in the following areas.

a) Motor drive
b) Hybrid electric vehicle
c) Multilevel inverters (MLI)
d) uninterruptible power supply (UPS)
e) High voltage DC (HVDC)
f) Magnetic traction
g) Renewable energy sources
h) Automotive applications.

CHAPTER-4

SIMULATION RESULTS AND DISCUSSION

4.1 THREE LEVEL DC-DC BOOST CONVERTER

Three level open loop MBC is shown in Fig 4.1. Simulation parameters are chosen as,

Table 4.1 Open loop three level boost converter model specifications

Parameter	Specification
Input Voltage (Vs)	50V
Switching Frequency	30kHz
Capacitance (C)	200µF
Load Resistance (R_L)	30Ω
Inductance (L)	1.33mH
Duty Cycle (D)	0.5

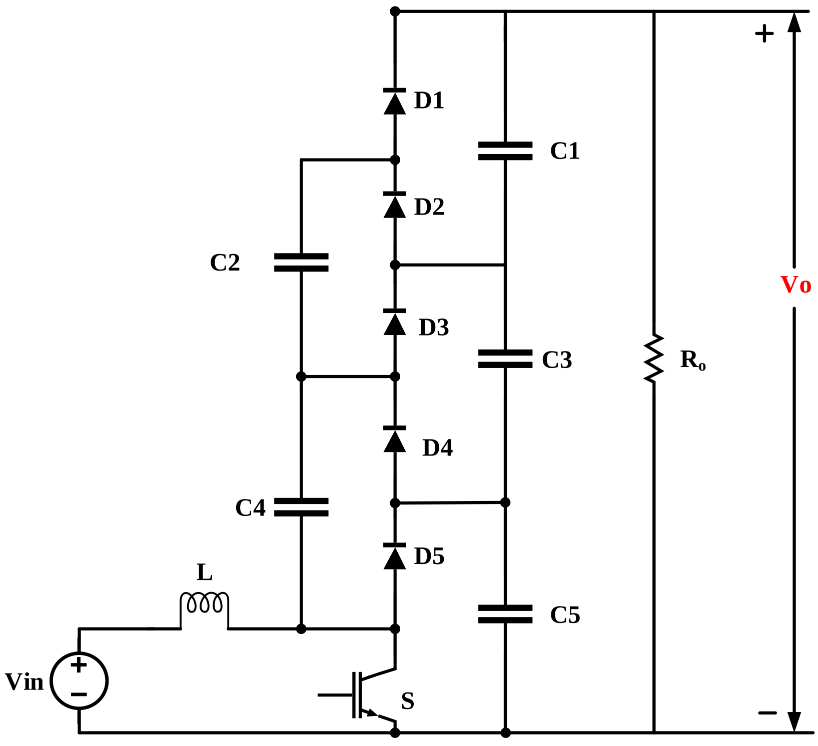

Fig 4.1 Three level boost converter

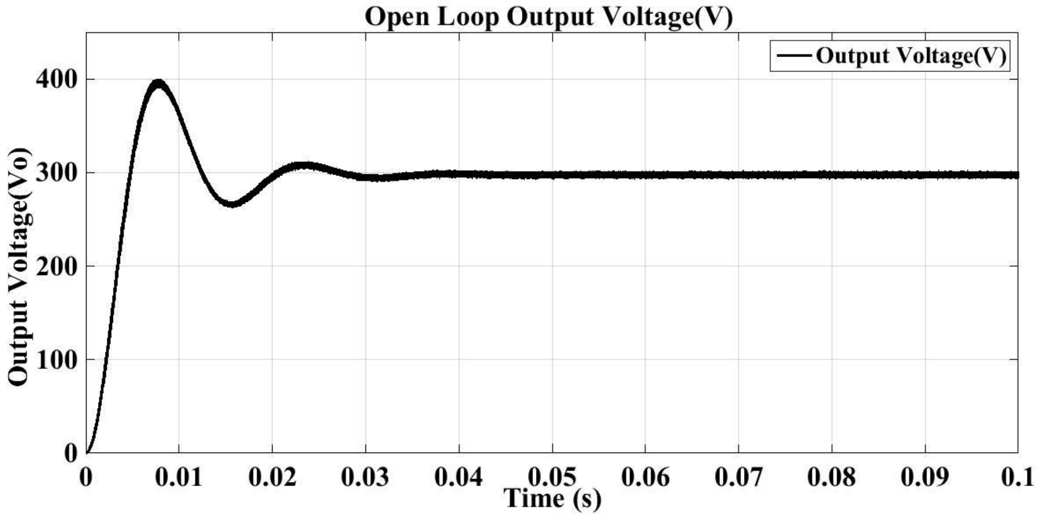

Fig 4.2 Open Loop three level boost converter output voltage(V)

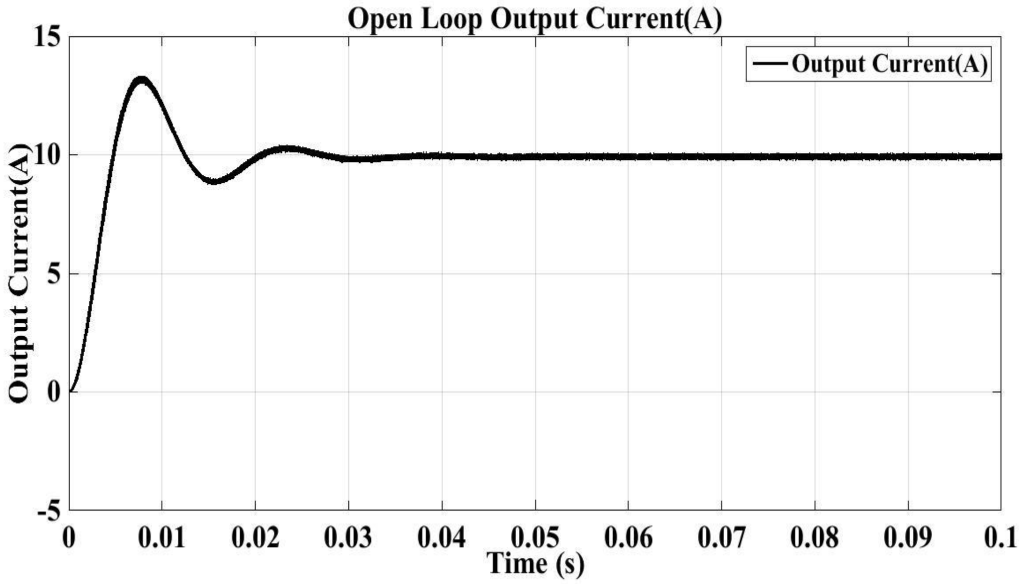

Fig 4.3 Open Loop three level boost converter output current (A)

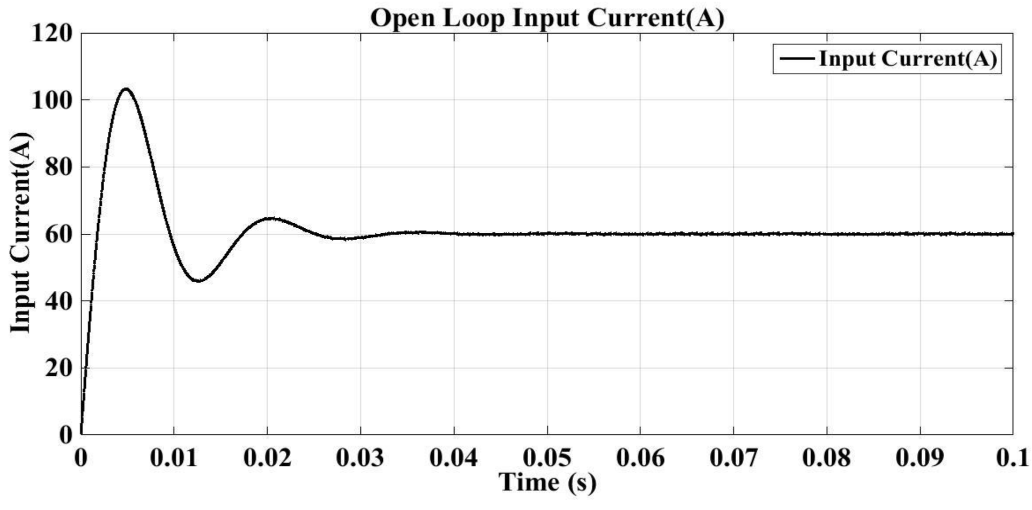

Fig 4.4 Open Loop three level boost converter output current (A)

Figs (4.3) and (4.4) represent the open loop output and input current.

Substituting table 4.1 specification in output voltage $V_o = \frac{N \times V_s}{(1-D)}$

Theoretical output voltage (Vo) = 300V verified with simulation result.

Substituting table 4.1 specification in output voltage $I_s = \frac{N \times I_o}{(1-D)}$

Theoretical input current (Is) = 60A verified with simulation result.

4.2 THREE LEVEL CLOSED LOOP MBC RESULTS

Fig. (4.5) represents a closed loop system of MBC. Here the output voltage is sensed and fed to an integral control to vary the duty cycle of the switch. Simulation is done on Matlab Simulink with the following parameters

Table 4.2 Closed Loop Three Level Boost Converter Model Specifications

Components	Specification
Source Voltage	50V
Switching frequency (fs)	100kHz
capacitance (C)	100µF
Change in Load Resistance (R_L)	10Ω to 20Ω
Inductance (L)	1.33mH
Integral controller constant(I)	0.55.

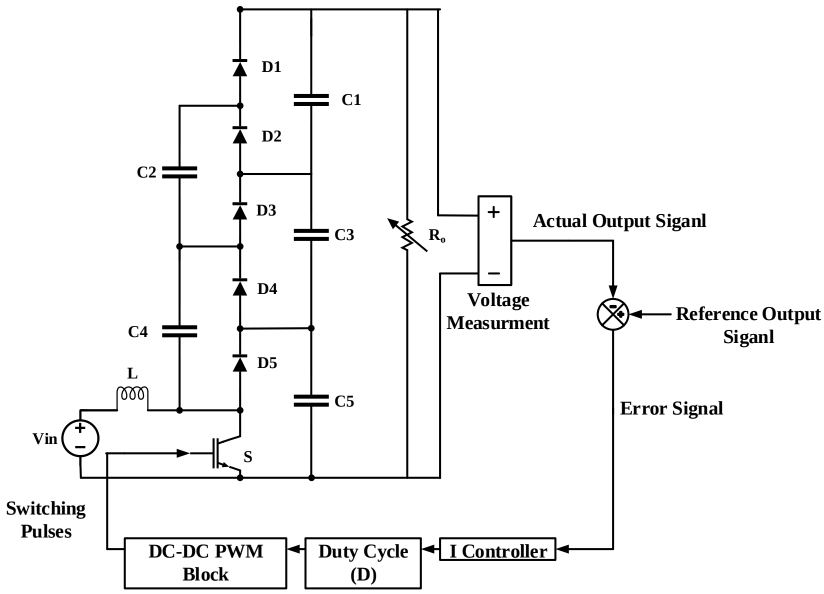

Fig 4.5 Closed loop MBC circuit model

To track the performance of the controller a step change in load resistance from 10Ω to 20 Ω is given as shown in Fig4.5.

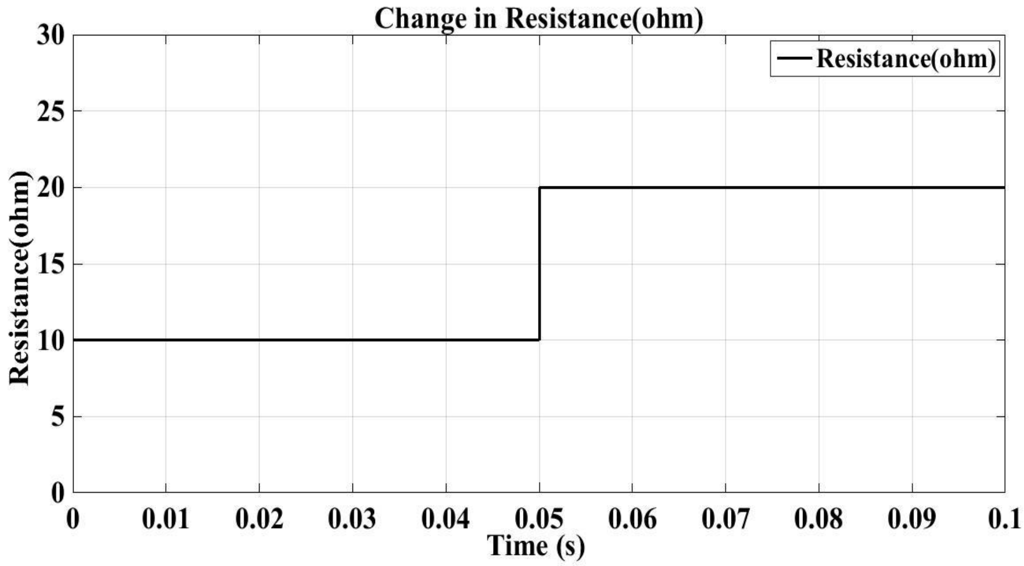

Fig 4.6 Change in load resistance

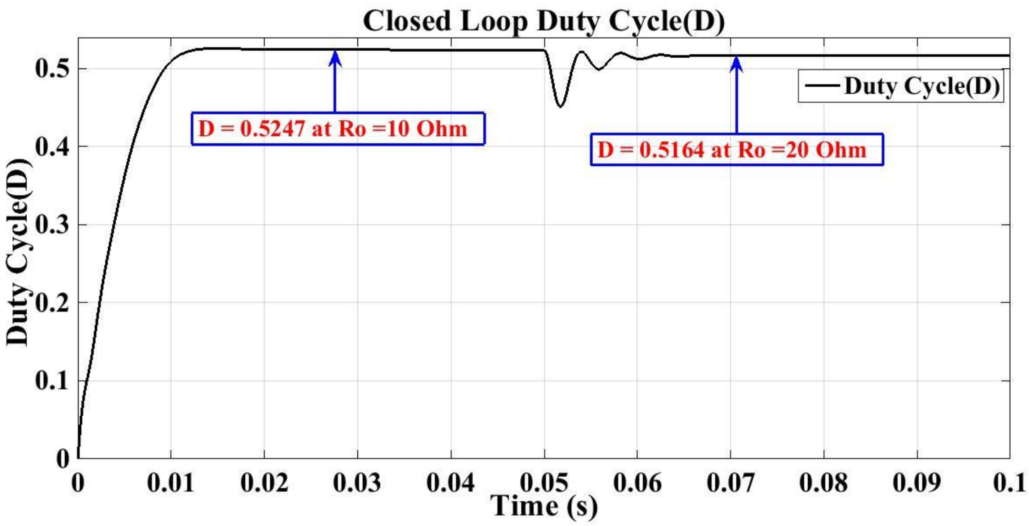

Fig 4.7 Closed loop three level boost converter duty cycle

Fig 4.7 represents the corresponding change in output voltage due to change in duty cycle. It is observed that the integral controller takes care the changes in load resistance. It results constant output voltage.

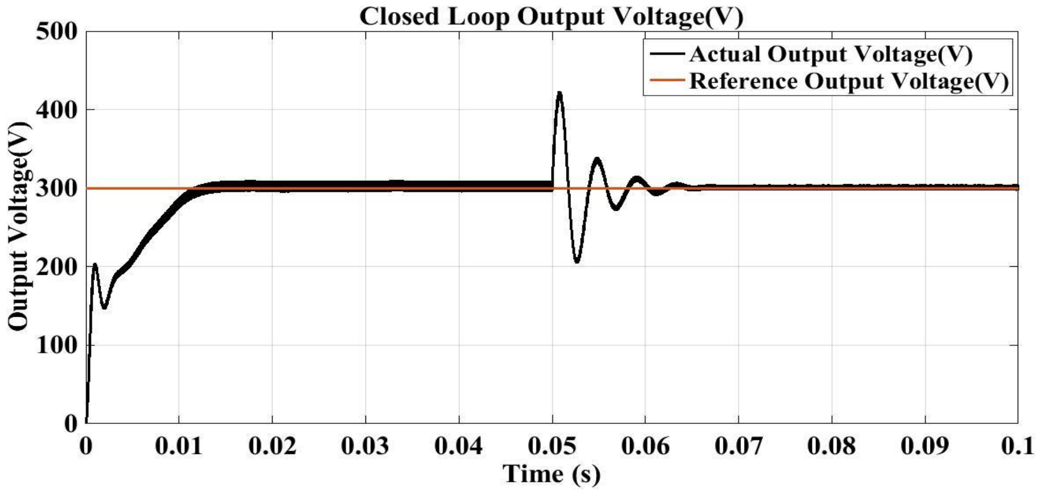

Fig 4.8 Closed loop three level boost converter output voltage(V)

To maintain the output voltage constant a drop in output current is shown in Fig4.8

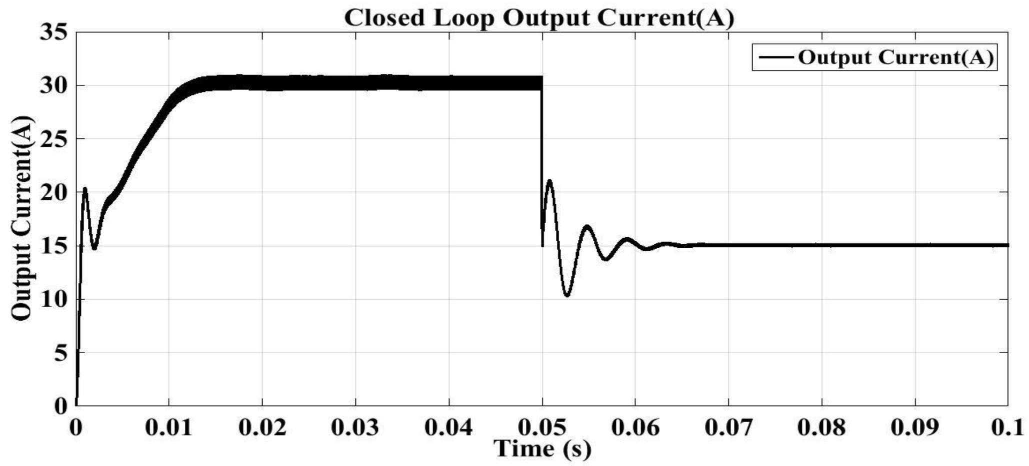

Fig 4.9 Closed loop three level boost converter output current (A)

A corresponding change in input current due to change in duty cycle is shown in Fig4.9.

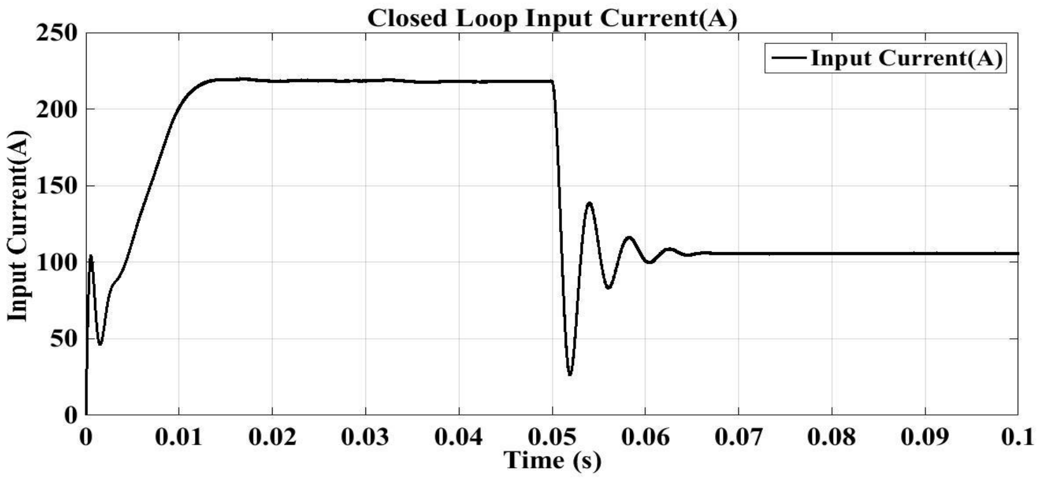

Fig 4.10 Closed loop three level boost converter input current (A)

It is observed that the converter stabilizes within short time. Settling time of different performance parameter at different load resistance is shown in table 4.1.

Table 4.3 Settling time of converter responses at different load resistances

R-Load(ohm)	Input Current settling time(ms)	output Current settling time(ms)	Output voltage settling time (ms)
20	2	2	2
50	6.5	4.5	4.5
70	8	6	6
100	10	9.5	9.5

4.3 STABILITY ANALYSIS OF REDUCED ORDER TWO LEVEL MBC (Open loop)

Transfer function between output voltage and duty cycle

$$\frac{\hat{v}_0}{\hat{d}} = \frac{\frac{(1-D)V_o}{N \times L} - \frac{S \times I_s}{C_{eq}}}{S^2 + \frac{S \times N}{RC_{eq}} + \frac{(1-D)^2}{N \times L \times C_{eq}}} \tag{4.1}$$

In (4.1) substituting the parameters, Vin = 50V, D = 0.5, L = 100(μH) C = 100(μF), R = 10, number of levels (N) = 2, we get

$$\frac{\hat{v}_o}{\hat{d}} = \frac{(-8 \times 10^{12} \times S) + (10^{18})}{S^2 + 2000S + 0.125} \tag{4.2}$$

Equation (4.1) and (4.2) transfer functions are non-minimum phase function, because one zero on right hand side. But From equation (4.2) observed converter stable because all poles in left of s-plane.

Transfer function between output voltage and Input voltage

$$\frac{\hat{v}_0}{\hat{v}_s} = \frac{\frac{(1-D)}{C_{eq}} \times \frac{1}{L}}{S^2 + \frac{S \times N}{RC_{eq}} + \frac{(1-D)^2}{N \times L \times C_{eq}}} \tag{4.3}$$

$$\frac{\hat{v}_o}{\hat{v}_s} = \frac{(5\times 10^7)}{S^2 + 2000S + 0.125} \tag{4.4}$$

Equation (4.3) and (4.4) transfer functions are minimum phase function, because no zero and poles on right hand side. But From equation (4.4) observed converter stable because all poles in left of s-plane.

CHAPTER-5

MBC PROTOTYPE RESULTS

Fig 5.1 shows a three level boost converter. simulation is carried out in Matlab Simulink. To validate the simulation results, a prototype was built in Power Electronics Lab. To track the performance as well as the authentication of the proposed topology, simulation and prototype parameters are chosen same and with MOSFET switch IRFP250.

Simulation and experimental results carried with the parameters shown in Table 5.1

Table 5.1 Open loop three level boost converter model specifications

Parameter	Specification
Input Voltage (Vs)	15V
Switching Frequency	10kHz
Capacitance (C)	100µF
Load Resistance (R_L)	400Ω
Inductance (L)	2mH
Duty Cycle (D)	0.5

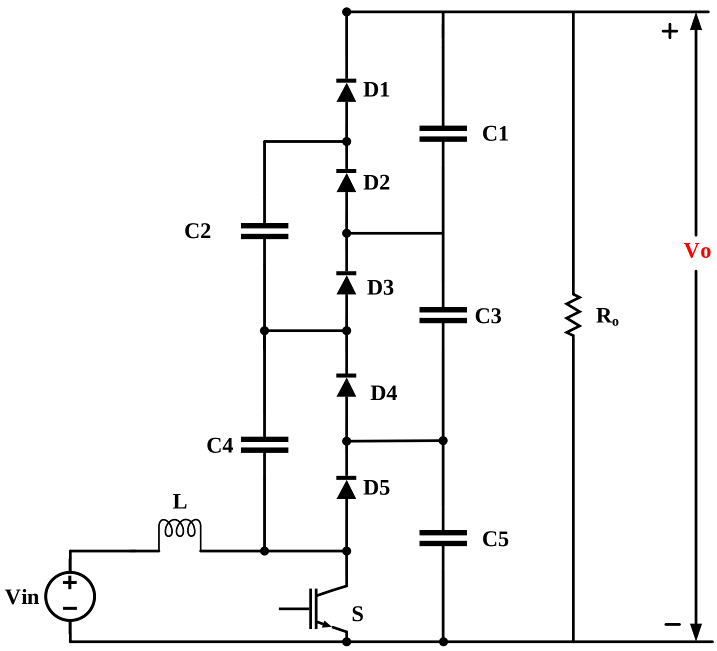

Fig 5.1 Three level boost converter

5.1 SIMULATION RESULTS

Fig 5.2 and Fig 5.3 represents the output voltage and inductor current respectively. Fig 5.4 and Fig 5.5 depicts the voltage across capacitor 5 and sum of voltage across capacitor5 and capacitor3.

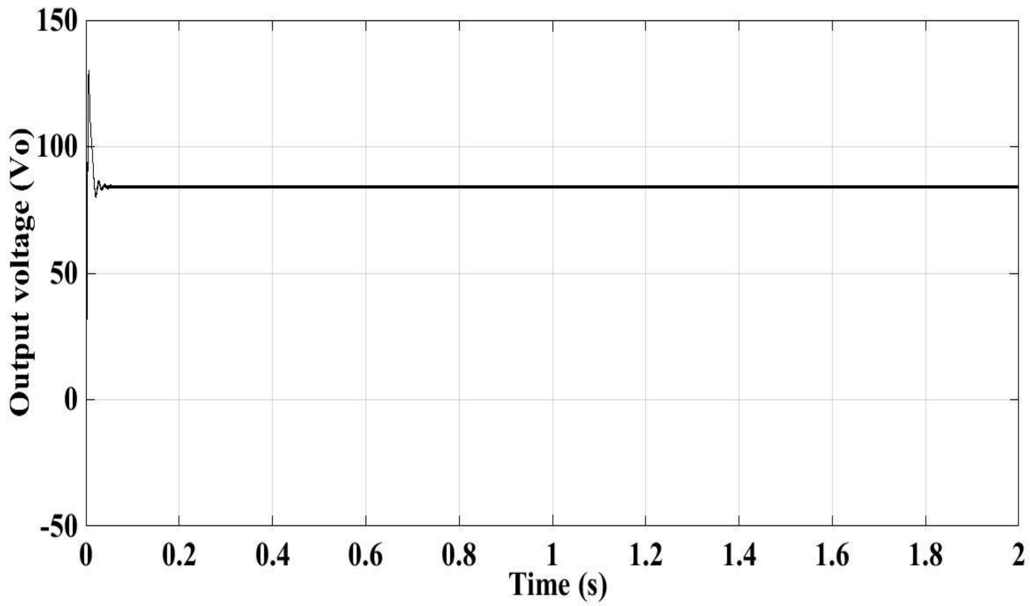

Fig 5.2 Simulated output voltage (V)

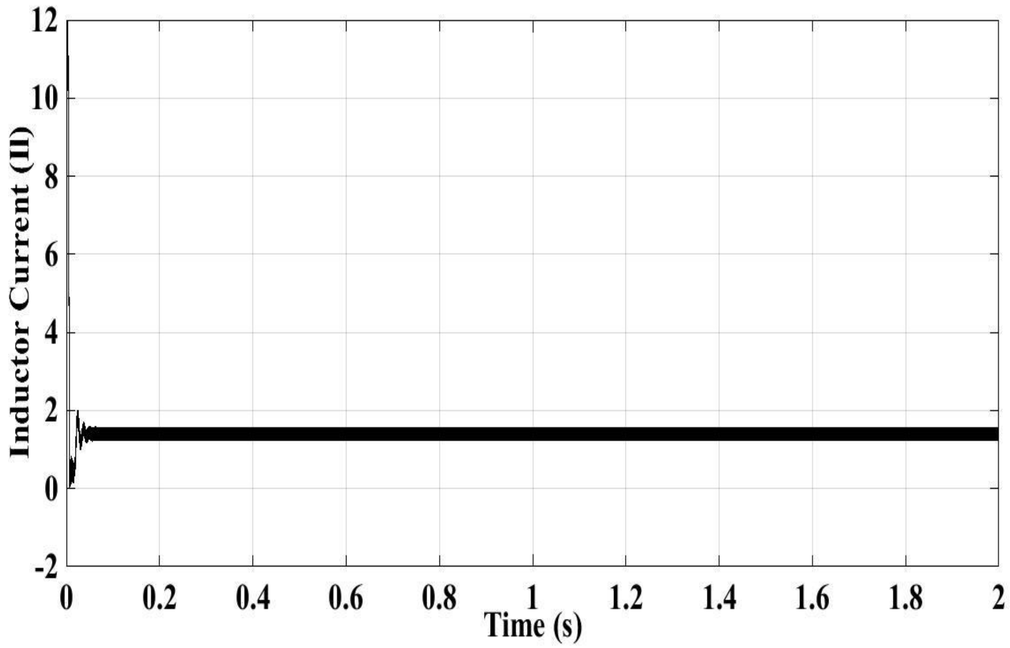

Fig 5.3 Simulated inductor current (A)

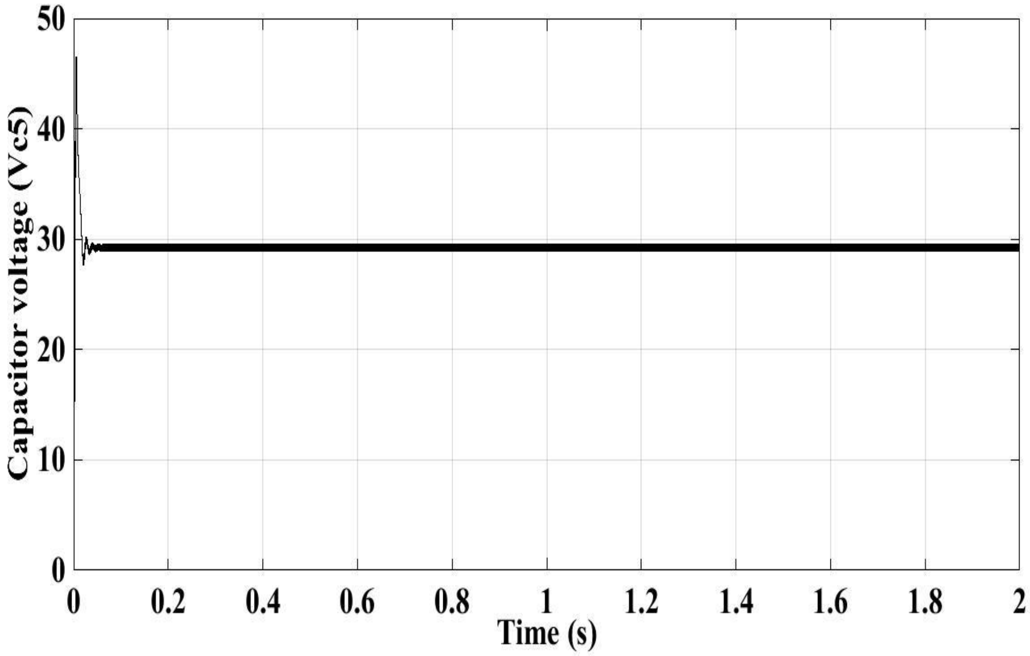

Fig 5.4 simulated capacitor voltage (Vc5)

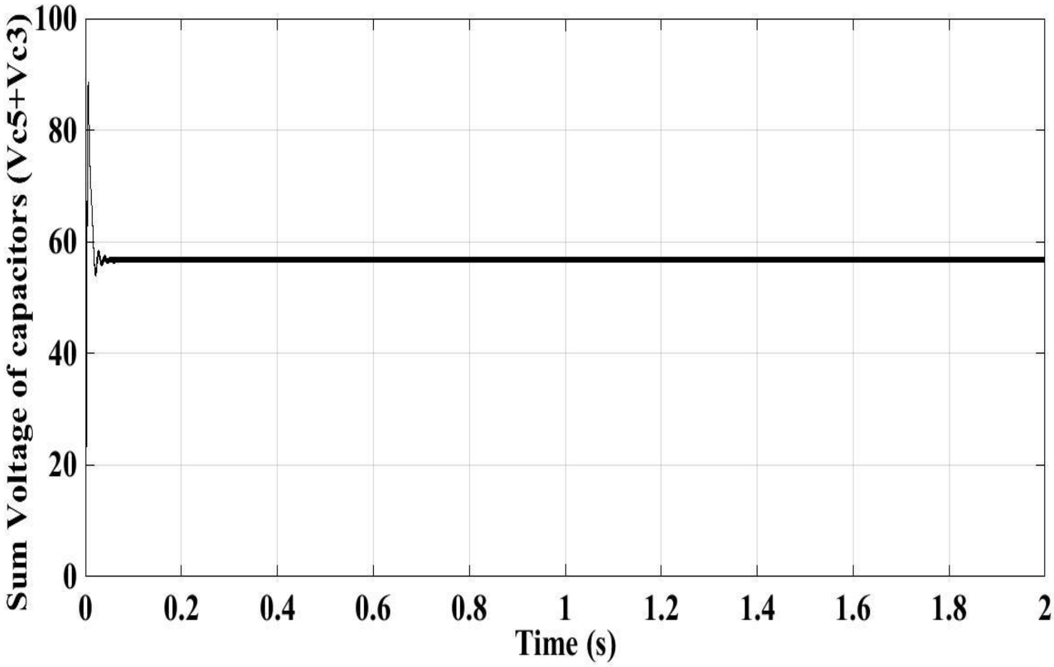

Fig 5.5 Sum voltage of capacitors (Vc5+Vc3)

5.2 PROTOTYPE RESULTS

To demonstrate the validation of proposed theory and results an experimental setup is developed in the lab is shown in Fig5.6.

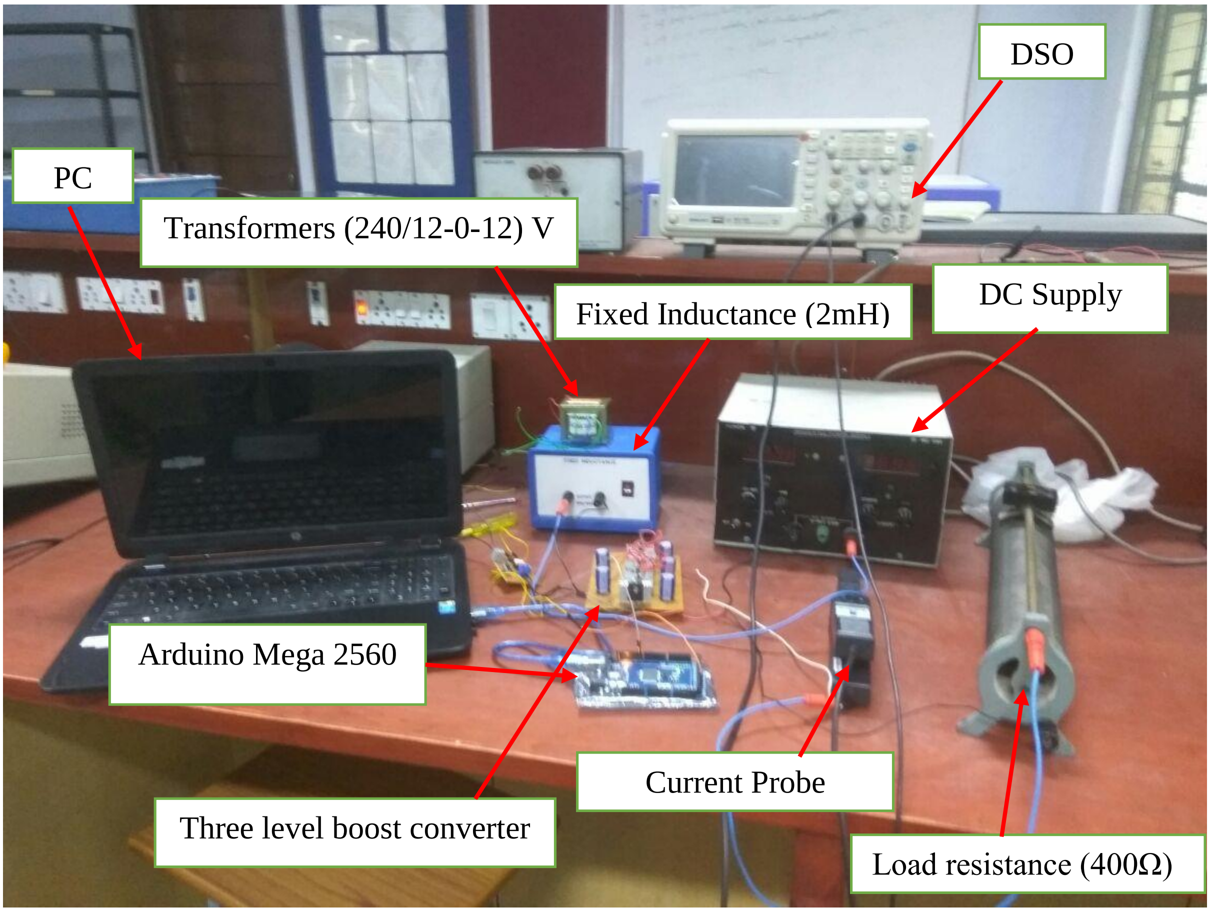

Fig 5.6 Prototype of three level boost converter

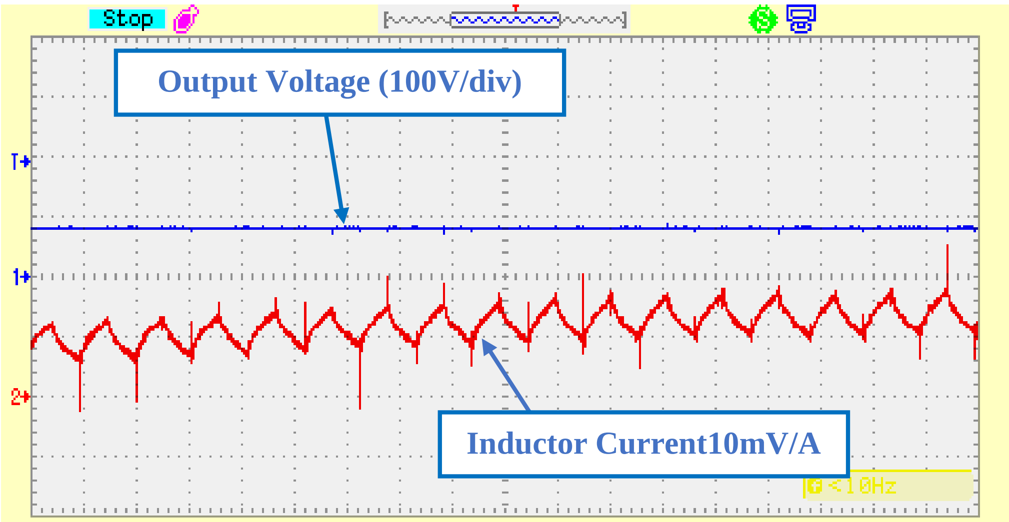

Fig 5.7 Output voltage (V) and inductor current (A)

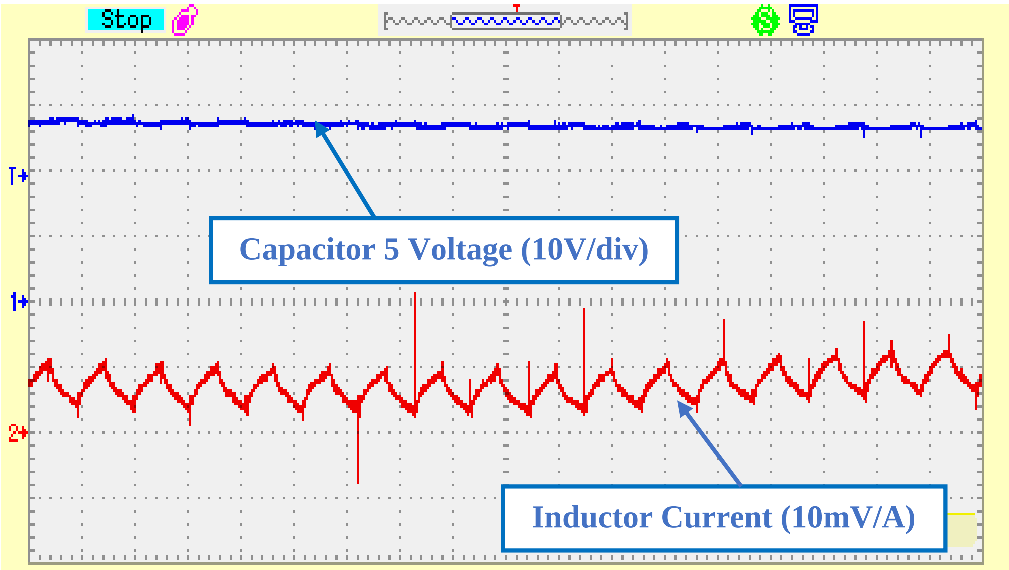

Fig 5.8 capacitor voltage (Vc5) and inductor current

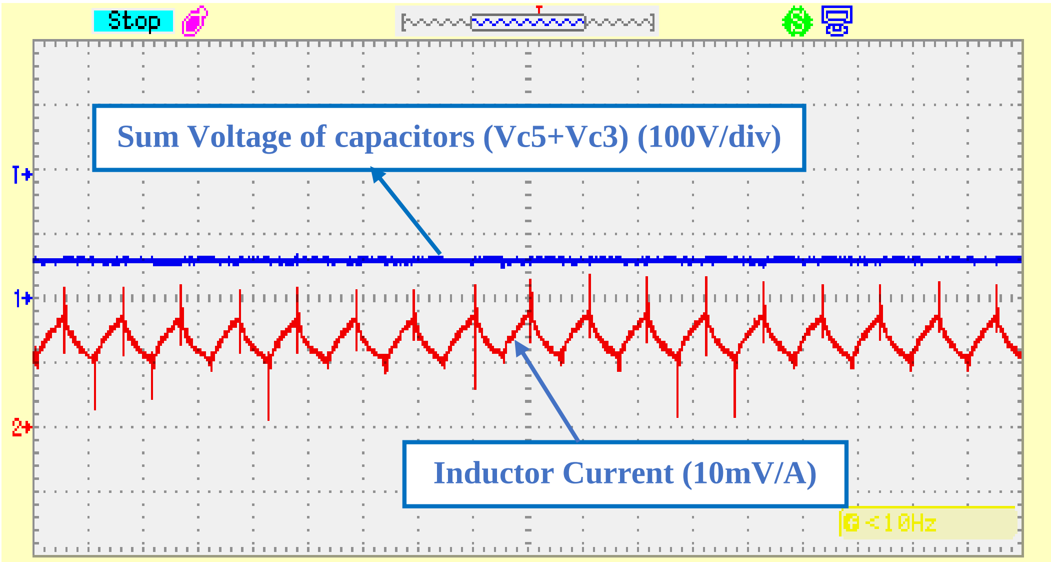

Fig 5.9 Voltage(Vc5+Vc3) and inductor current

Table 5.2 Simulation and prototype parameter specifications

Specification	Theoretical value	Practical value	Simulated value
Inductor L (mH)	1.667	2	2
Capacitance C (μF)	10.5	100	100
Ripple Current ΔI (A)	0.3	1	0.315
Ripple Voltage ΔV (V)	1.058	0.85	0.7
Efficiency η (%)	94.6	90	96.70

CHAPTER-6

CONCLUSION AND FUTURE SCOPE

6.1 CONCLUSION

Multilevel dc-dc boost converter is derived from conventional boost converter just by adding (2N-1) capacitors, (2N-1) diodes to obtain N level output voltage. Here the conventional topology remains unchanged. Multilevel converter output voltage is more than conventional boost converter is justified with the mathematical, simulation and experimental results. Analytical design for practical value of inductor and capacitor for three level boost converter is presented. The continuous conduction mode of inductor current is verified experimentally. Higher gain can be achieved at low duty cycle compared to conventional one. Another important advantage of the converter is that no external circuitry is needed to balance the capacitor voltage. The converter operates at high switching frequency to meet less space requirement. Ripple in the inductor current and capacitor voltage is examined experimentally. It marks the converter as a suitable candidate for various applications like PV system, fuel cell system, traction system, HVDC system etc..

6.2 FUTURE SCOPE OF WORK

Power demand is increasing day by day. To meet the demands conventional energy sources are not sufficient because of environmental concern. We need to depend on renewable energy sources. It is well known from the literature that the processing of power from renewable energy sources is a challenging issue. It is observed and synthesised from the thesis work that the proposed converter can extend its contribution to solve the issue. As an example Fuel cell-based grid connected system is shown Fig (6.1) .

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APPENDIX-A

CLOSED LOOP MBC FED DC MOTOR DRIVE

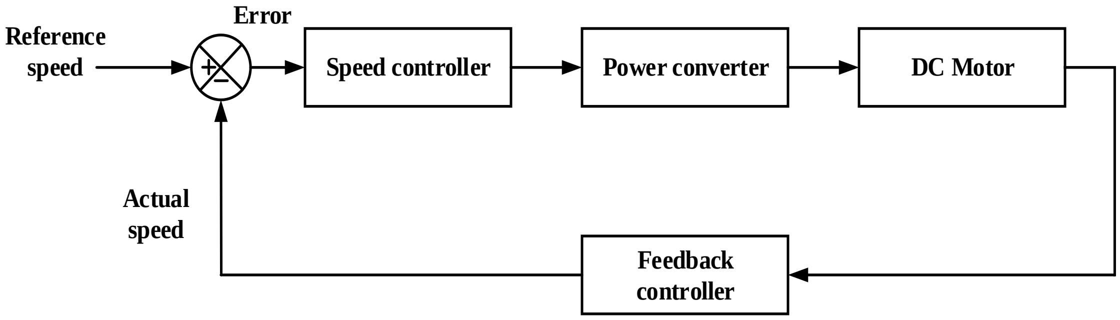

Fig-A1 Closed loop fed DC motor drive

Fig A1 presents a closed loop MBC fed DC motor drive. Here the speed is sensed and compared with the reference speed, the resulting error is fed to a speed controller. The speed controller then changes the duty cycle to give the desired speed. MBC output is fed to a separately excited DC Motor. Simulation parameters for closed loop system is given in Table A1

Table A1 Closed loop MBC fed DC motor drive specifications

Parameter	Specification
Input Voltage (Vs)	50V
Switching Frequency	1kHz
Capacitance (C)	100µF
Inductance (L)	160µH
Duty Cycle (D)	0.5 to 0.6
PI controller	P = 0.003, I = 0.03
Separately excited DC motor	50HP, Vt = 240V, 1750rpm, Vf = 300V

Table A2 Input drive cycle

Time (sec)	Reference Speed(rpm)	Actual Speed(rpm)
0-1	1000	980
1-1.5	850	848
1.5-2.2	1500	1475
2.2-3	500	450

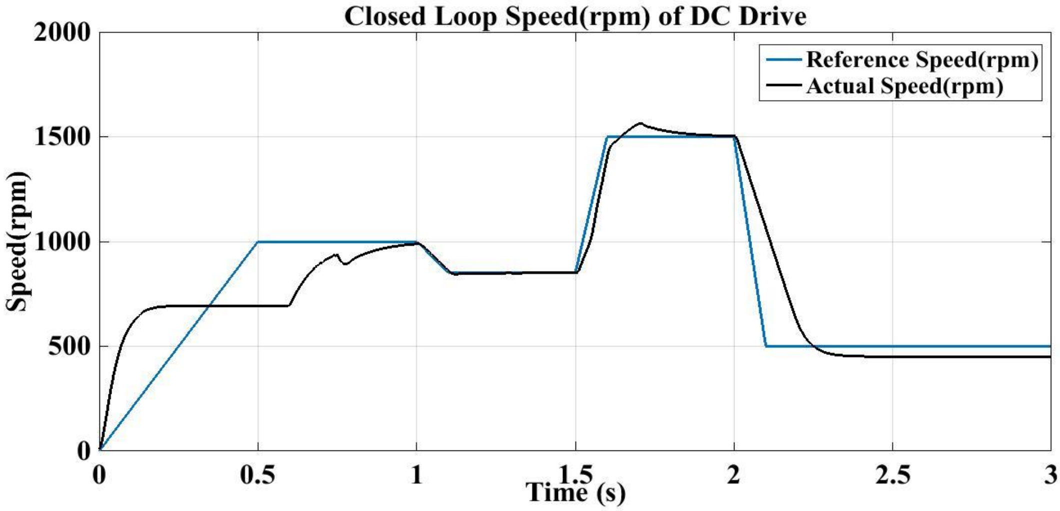

Fig A2 Closed loop speed of dc motor

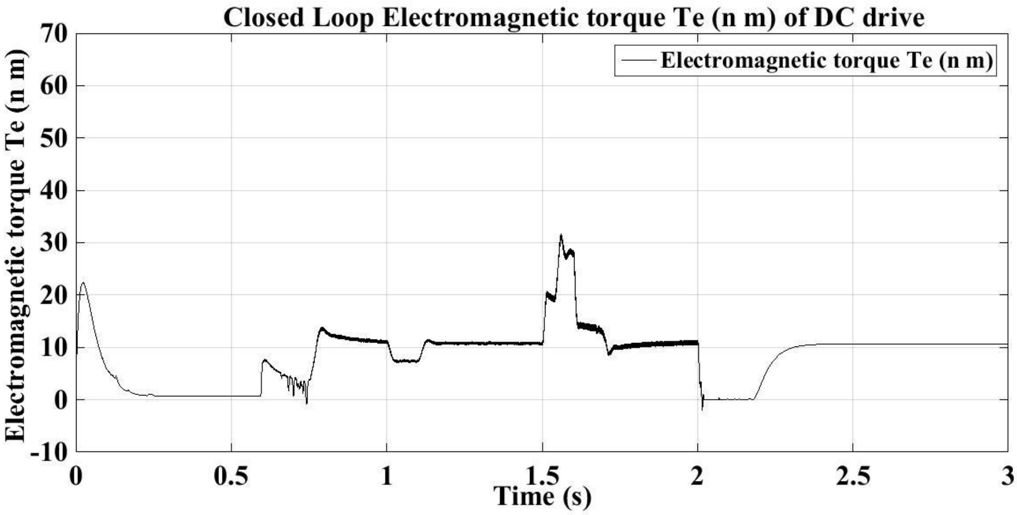

Fig A3 Closed loop electromagnetic torque

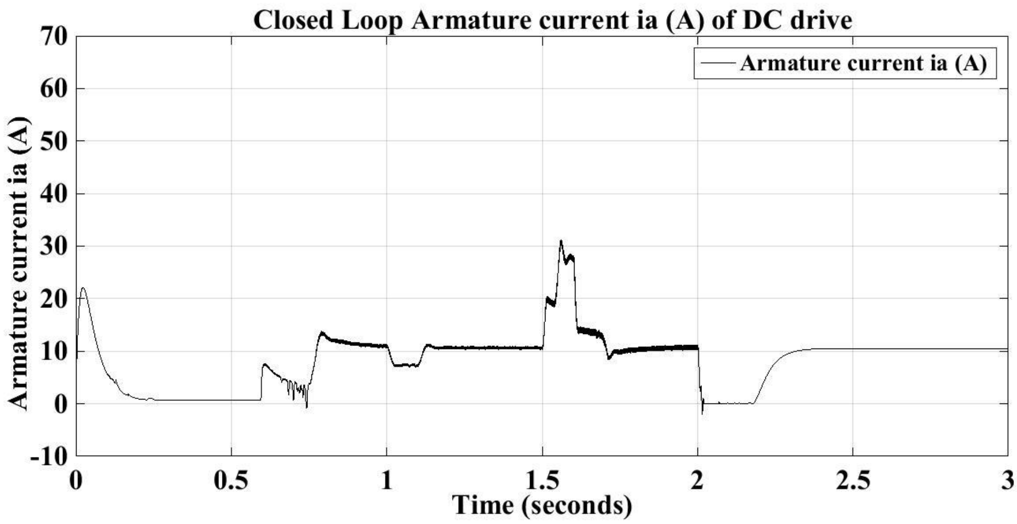

Fig A4 Closed loop armature current

CURRICULUM VITAE

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Certificate/Degree	Board/University	School/College	Duration of study
Master of Engineering, Specialization: Power Electronics & Drives	Thapar University (TIET) Patiala, Punjab	Thapar University (TIET) Patiala, Punjab	2015-2017
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"*Performance Analysis and Design of of DC-DC Multilevel Boost Converter*"----------- to be communicated in international journal.

Thesis: - Performance analysis of a DC - DC multilevel boost converter

PLAGIARISM CERTIFICATE

Santosh_Reddy_ME_PED_Multi_Level_Converter

ORIGINALITY REPORT

%10	%4	%9	%0
SIMILARITY INDEX	INTERNET SOURCES	PUBLICATIONS	STUDENT PAPERS

PRIMARY SOURCES

1	Zhou, Haihua, Ashwin M. Khambadkone, and Xin Kong. "Passivity-Based Control for an Interleaved Current-Fed Full-Bridge Converter With a Wide Operating Range Using the Brayton–Moser Form", IEEE Transactions on Power Electronics, 2009. Publication	%1
2	Can, F.. "Efficiency and effectiveness of query processing in cluster-based retrieval", Information Systems, 200412 Publication	%1
3	maxwellsci.com Internet Source	<%1
4	Diedenhofen, M.. "Tetracyclo[3.1.0.0(1.3).0(3.5)]hexane: a new C"6H"6 isomer with an unusual bonding situation", Journal of Molecular Structure, 20001212 Publication	<%1