A COMPARATIVE STUDY OF DELAY ANALYSIS FOR CARBON NANOTUBE AND COPPER BASED VLSI INTERCONNECT MODELS

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Submitted by

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JULY, 2011

CERTIFICATE

I hereby declare that the work which is being presented in the thesis entitled, **"A Comparative Study of Delay Analysis for Carbon Nanotube and Copper based VLSI Interconnect models"** in partial fulfillment of the requirement for the award of degree of M.Tech. (VLSI Design & CAD) at electronics and Communication Engineering Department of Thapar University, Patiala, is an authentic record of my own work carried out under the supervision of Mr. Mayank K. Rai, Assistant Professor, ECED.

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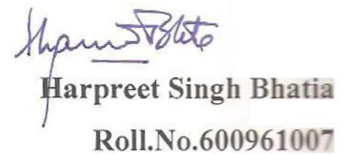

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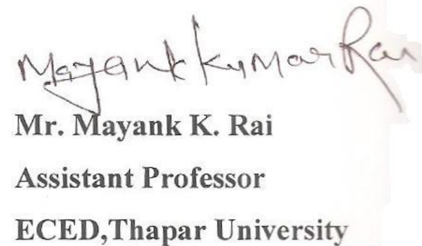

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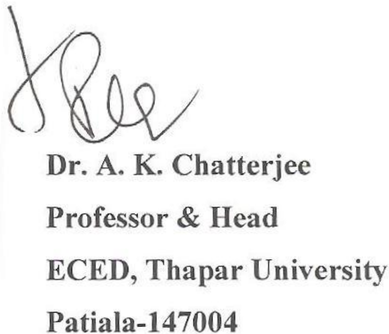

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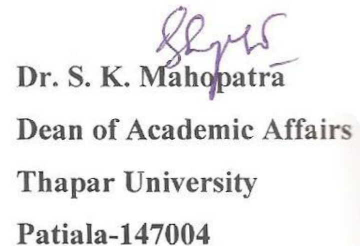

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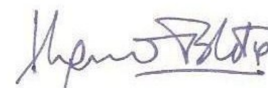

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ABSTRACT

On-chip global interconnect is perceived to be a bottleneck in present and future high-performance designs because wire delays are not scaling from generation to generation at the same rate as logic delays. To counteract these detrimental effects, various measures are used such as use of wide wires, insertion of repeaters and employing distributed interconnects. In future development of nanoscale ICs, new materials for interconnects are utilized such as low-*k* material or low resistivity metals such as copper. However as the diameters of conventional metallic interconnection wires reach the mean free path for electrons, surface scattering from the boundaries of ultra-narrow conductors as well as grain boundary scattering would inhibit electronic conduction in the copper wires to an unacceptable level. Consequently, alternative solutions such as metallic carbon nanotube (CNT) interconnects have been proposed in order to avoid the problems associated with global on-chip wires altogether.

This thesis work analyses the efficacy of using single-walled carbon nanotube bundle instead of copper as an interconnect material for the 45 nm technology node. Various analytical models for equalized on-chip interconnect are used to calculate theoretical delay for these interconnects. SPICE simulations using PTM level 54 model were carried out to validate the findings. A number of parameters such as interconnect length, pitch, repeater size and number of repeaters were optimized to determine the delay performance of these interconnects. The results reflect that CNT show more than 36% time delay saving than copper for less number of inserted repeaters in global interconnects.

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ABBREVIATIONS

AR	Aspect Ratio
IC	Integrated Circuit
LSI	Large Scale Integration
CMOS	Complementary Metal Oxide Semiconductor
CNT	Carbon Nanotube
EM	Electo-Magnetism
FET	Field Effect Transistor
GaAs	Gallium Arsenide
GHz	Giga Hertz
MFP	Mean Free Path
MSI	Medium Scale Integration
MWCNT	Multi Walled Carbon Nanotube
RC	Resistance-Capacitance
RLC	Resistance-Inductance-Capacitance
SPICE	Simulation Program with Integrated Circuit Emphasis
SWCNT	Single Walled Carbon Nanotube
VLSI	Very Large Scale Integration

LIST OF SYMBOLS

A	Area of Interconnect (cm^2)
c_{fringe}	Capacitance of interconnect due to fringing field (F/cm^2)
c_{int}	Capacitance of interconnect (F/cm^2)
C_N	Capacitance of subsection of interconnect (F/cm^2)
C_o	Input capacitance of the minimum size inverter (F/cm^2)
c_{pp}	Capacitance of interconnect due to parallel field (F/cm^2)
d'	distance between grain boundaries
h	Plank's constant ($6.626 X10^{-34}$ Js)
i	current (A)
k	dielectric constant
l	length of interconnect (nm)
L	length of MOS channel (nm)
R	Resistance of interconnect (Ω/cm^2)
R_N	Resistance of subsection of interconnect (Ω/cm^2)
R_o	Output resistance of the minimum size inverter (Ω/cm^2)
R_s	sheet resistance (Ω/cm^2)
s	spacing between interconnects (nm)
t	time of flight (s)
V	Voltage (V)
w	width of interconnect (nm)
W	width of MOS channel (nm)
X_{ox}	dielectric thickness between interconnects (nm)
$\varepsilon_{dielectric}$	permittivity of dielectric (F/cm)
ε_o	permittivity of free space (8.85×10^{-14} F/cm)
μ	permeability ($4 X10^{-9}$ H/cm)
ρ	Resistivity (Ω-cm)
ρ_g	resistivity due to Grain Boundary effect (Ω-cm)
ρ_o	bulk resistivity (Ω-cm)

CHAPTER 1 INTRODUCTION

1.1 Motivation

The rapid growth of the VLSI technology is mainly due to the constant reduction of the feature size of VLSI devices. Feature size is the minimum transistor size. With the rapid developments in VLSI technology, design, and CAD techniques, the central processor cycle times are reaching the vicinity of 1 ns and communication switches are being designed to transmit data that have frequency greater than 1 GHz. The ever-increasing quest for high-speed applications is placing higher demands on interconnect performance and highlights the previously negligible effects of interconnects such as ringing, signal delay, distortion, reflections, and crosstalk [1].

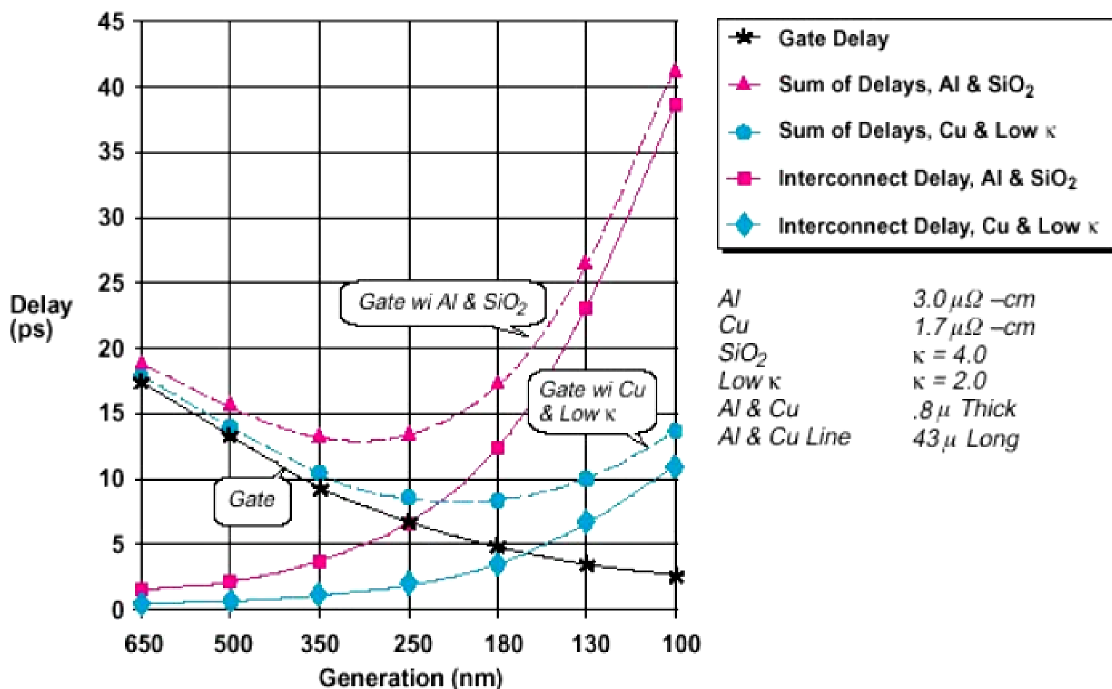

Fig. 1.1 Impact of scaling on signal delay in high speed systems [3]

Fig. 1.1 describes the effect of scaling of chip on the global interconnect delay. As seen, the global interconnect delay grows as a cubic power of the scaling factor [1]. It is predicted that interconnects will be responsible for nearly 70 to 80% of the signal delay in high-speed systems. If not considered during the design stage, these interconnect effects can cause logic glitches that render a fabricated digital circuit inoperable, or they can distort an analog signal such that it fails to meet specifications. Since extra iterations in the design cycle are costly, accurate prediction of these effects is a necessity in high-speed designs. Hence, It becomes extremely important for designers to simulate the entire design along with interconnect sub circuits as efficiently as possible while retaining the accuracy of simulation.

1.2 What Is High Speed?

Speaking on a broader perspective, a "high-speed interconnect" is the one in which the time taken by the propagating signal to travel between its end points cannot be neglected. ·An obvious factor that influences this definition is the physical extent of the interconnect - the longer the interconnect, the more time the signal takes to travel between its end points. Smoothness of signal propagation suffers once the line becomes long enough for the signal's rise/fall times to roughly match its propagation time through the line. Then, the interconnect electrically isolates the driver from the receivers, which no longer function directly as load to the driver. Instead, within the time of the signal's transition between its high and low voltage levels, the impedance of the interconnect becomes the load for the driver and also the input impedance to the receivers. This leads to various transmission line effects, such as reflections.

Alternatively, the term "high-speed" can be defined in terms of the frequency content of the signal. At low frequencies, an ordinary wire (i.e., an interconnect) will effectively short two connected circuits. However, this is not the case at higher frequencies. For the same wire, which is so effective at lower frequencies for connection purposes, has too much inductive/capacitive effect to function as a short at higher frequencies. Faster clock speeds and sharper slew rates tend to add more and more high-frequency contents.

An important criterion used for classifying interconnects is the *electrical length* of an interconnect. An interconnect is considered to be electrically short if at the highest frequency, the interconnect length is physically shorter than one-tenth of the wavelength (i.e., length of

the interconnect ($\lambda < 0.1,\ \lambda = v/f$). Otherwise the interconnect is referred as electrically long [4]. In most digital applications, the desired highest operating frequency (which corresponds to the minimum wavelength) of interest is governed by the rise/fall time of the propagating signal. For all practical purposes, the width of the spectrum can be assumed to be finite and f_{max} can be defined as corresponding to 3-dB bandwidth point [5]

$$f_{\,max} = \frac{0.35}{t_r} \tag{1.1}$$

where t_r is the rise/fall time of the signal.

Electrically short interconnects can be represented by lumped models, whereas electrically long interconnects need distributed or full-wave models.

1.3 Delay analysis

High-speed system designers are driven by the motivation to have signals with higher clock and slew rates while at the same time to innovate on reducing the wiring cross-section as well as packing the lines together. Reducing the wiring dimensions results in appreciably resistive lines. Depending on the operating frequency, signal rise times, and the nature of the structure, interconnects can be modeled as lumped (RC or RLC), distributed (frequency-independent/dependent RLCG parameters, lossy, coupled), full-wave models, or measured linear sub networks.

In the past, interconnect models have been generally restricted to ***RC tree models***. RC trees are RC circuits with capacitors from all nodes to ground, no floating capacitors, and no resistors to ground. The signal delay were estimated using a form of Elmore delay [5] through RC ,which provided a dominant time constant approximation for monotonic step responses.

At relatively higher speeds, the electrical lengths of interconnect becomes a significant fraction of the operating wavelength, giving rise to signal-distorting effects that do not exist at lower frequencies [4]. Consequently, the conventional lumped impedance interconnect models become inadequate, and transmission line models such as RLC trees are needed. In the super GHz range, inductance starts to play a role even on a chip. The lumped-RC model,

is no longer adequate, and a ***RLC*** (resistive-inductive-capacitive) model has to be adopted [19].

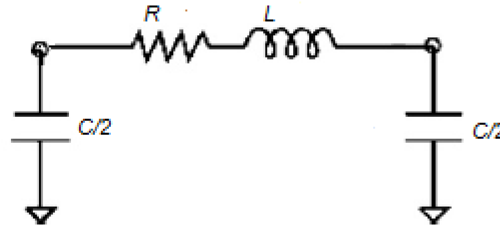

Fig. 1.2: RLC Interconnect model [4]

Unfortunately, Elmore delay cannot accurately estimate the delay for RLC interconnect lines and trees [5]. This is primarily due to the fact that the Elmore delay does not cover non-monotonic responses [7] which can occur in RLC circuits. During the course of time various Closed-form analytical formulas for delay prediction of RLC trees were proposed, viz. Sakurai Delay Model [5], Kahng and Muddu analytical delay model [7], Ismail et al. analytical delay model [5] and Meindl et al. delay model [8-11]. Other variants of delay model are derived from the Modified Nodal Analysis method given by Ruehli et al [12].

1.4 Methods for improving Interconnect delay

It is not possible for interconnect to grow millions of transistors on VLSI chip using only one level of copper; moreover even copper will introduce excessive delay when chips get larger and minimum size is reduced.

Multilayers of interconnections are partial solutions to this problem. First, layers of copper in the x- and y- directions interconnected through vias between the levels enable global communication without the need for polysilicon or diffusion wires. Second, the cross-sectional dimensions of the upper layers can be optimized to reduce their RC constants. The local interconnects can use the upper levels with thicker lines that yield shorter propagation delays. Because much of the chip area is occupied by interconnections, mulilayers of metal can also reduce the chip size and further improve the time delay because the average interconnect length is inversely proportional to the number of levels [1]

When the resistance of the interconnection is comparable to or larger than the on- resistance of the driver, propagation delay increases quadratically with its length because both

capacitance and resistances increase linearly with length. The signal delay of long (global) wires therefore tends to be dominated by the *RC* effect.

Repeaters are regularly inserted to minimize the interconnect response time by mitigating the effect of resistance and capacitance. The use of repeaters makes time delay linear with length by dividing the interconnection into smaller subsections [2].

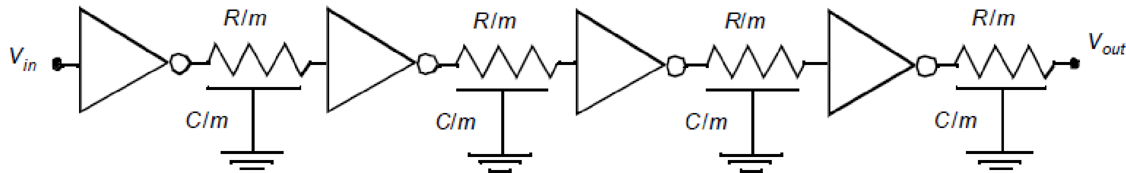

Fig. 1.3: Distributed RC Interconnect with Repeaters (Buffers) inserted in between [2].

Various models of delay estimation have been derived by Ismail et al. [13-14], Meindl et al. [8-11] and Sakurai-Newton's alpha low power model [15] for repeater inserted RLC interconnect lines.

1.5 Factors affecting Interconnect Delay

Various factors defining the shape and structure of interconnect that affect its performance in terms of delay and power. Replacing aluminium and silicon–dioxide (SiO_2) with copper and low *dielectric* constant (low-k) materials, respectively can reduce the interconnect delay. But, low-k materials are more prone to dielectric breakdown due to increasing current densities [28].

To improve signal speed, there is a trend to increase the line width, leading to reduction of spacing between two lines (smaller *pitch*) [25]. This leads to a continuous increase in resistance and capacitance, negating improvement in interconnect delays, even forcing longer RC interconnect delays with each generation.

In deep-submicron, designers tend to keep a high aspect ratio (ratio of interconnect thickness/width) since higher interconnect thickness/width decreases the inter-line capacitance. But, as the aspect ratio get larger, the two-dimensional fringing fields and capacitances between neighbouring lines become important and, after a certain point, larger aspect ratios yield no additional advantage [28].

1.6 Future Interconnections

Resistivity of copper is increasing rapidly under the combined effects of enhanced grain boundary [26], surface scattering [26] and the presence of a highly resistive diffusion barrier layer [27] in deep-submicron technology nodes. These are the most important parameters that limit the efficiency of copper in future.

In order to alleviate such problems, changes in the material used for on-chip interconnections have been sought even in earlier technology generations, for example the transition from aluminium to copper some years back. Carbon nanotubes have recently been proposed as a possible replacement for metal interconnects in future technologies [29]. Carbon nanotubes (CNTs) are graphene sheets rolled up into cylinders with diameter of the order of a nanometer. Depending on the direction in which CNTs are rolled up (chirality), they demonstrate either metallic or semi-conducting properties. Because of their extremely desirable properties of high mechanical and thermal stability, high thermal conductivity and large current carrying capacity [30], CNTs have aroused a lot of research interest in their applicability as VLSI interconnects of the future. However, a singlewall nanotube results in a very high contact resistance (greater than 6.45 KΩ) [32] and hence a bundle of closely packed parallel CNT *bundle* is preferably used above a ground plane.

The potential performance of CNT interconnections and their relative comparison to copper interconnections can be studied using physical models [32]. Nanotube bundles offer better performance than single nanotubes in which wave propagation is relatively slower. As the interconnection size decreases, the performance of copper interconnections goes down due to the increased resistivity as well as electromigration problems, and CNTs have been proposed to be effective replacements due to the ballistic flow of electrons with electron mean free path of several micrometers.

1.7 Thesis Organization

Chapter 2 starts with a literature review of interconnect technologies, starting from basics to the advancement towards the carbon nanotube interconnects. A bibliographic survey of the various analytical approaches for delay prediction and waveform analysis is given. Along with that, the current research in modeling carbon nanotube interconnects is presented.

Chapter 3 briefly introduces the basic concepts of interconnect analysis and its delay evaluation. The major repeater insertion techniques for improving signal delay are also included. The factors affecting metal interconnects and challenges faced by Cu Interconnects in deep sub-micron technologies are explained. In the concluding part, the unique properties of the CNTs that make it prime choice for the photonic applications are given.

Chapter 4 is mainly concerned with the analytical delay estimation techniques of VLSI interconnects. In this chapter interconnect delay calculation using three models are shown- the Modified Nodal Analysis method given by Ruehli et al [12]. The alpha low power model [15] was used to obtain Driver Interconnect Model (DIL) to estimate delay of an RLC interconnect without repeaters.

Chapter 5 compares the result of copper as well as CNT based interconnect at 45 nm technology. Impedances are calculated for top global layer interconnect lines with coupling above one metal ground [31], [32]. The signal delays for GHz waveforms are plotted and analyzed using SPICE in Tanner EDA. In the end the comparison of copper and CNT interconnect delays are summarized that gives the range of the length and pitch variations for which CNT gives a better delay performance.

Finally, a conclusion and future scope of the thesis is given in **Chapter 6.**

CHAPTER

2

LITERATURE SURVEY

2.1 Introduction

With continuously decreasing device dimensions, the effect of the interconnect lines on the overall performance of digital integrated circuits is becoming increasingly significant. The increased die size makes long interconnect lines to be common features in VLSI chips. The long interconnections lead to prohibitively high propagation delays. As it has been extensively pointed out (Sakurai, 1983[6]), when the resistive component of the interconnect load becomes comparable to the gate output impedance, a single capacitor is no longer a valid gate load model. The line resistance R acts as capacitance "shielding," and as it increases this "shielding" becomes significant and the output waveform presents an RC tail. Therefore, more accurate load models have to be used for taking into account the increased role of the resistance in the determination of the load behaviour and consequently the propagation delay of the driving CMOS gates.

For a single transistor that drives many clock lines, the network of clock lines produces excessive clock skew and sets an upper limit on clock frequency (Bakoglu and Mendl, 1986[2]). Clock frequency determines the overall performance of the chip (cycle time, access time, instructions per second) because, despite its fast switching speed, a transistor must normally wait until the next clock cycle before it can change its state.

2.2 Interconnect Delay Models

As the feature size decreases to the submicron dimension, the transmission-line effects now play an important role in determining interconnect delays and system performance (Ismail, et al., [4]). Various techniques have been proposed for the delay analysis of interconnects

In order to find analytical expressions for the propagation delay and the output waveform shape, an interconnect line may be modeled in different ways. An expression for the propagation delay when a load is modeled simply by a resistor in series with a capacitor (RC

model) was derived by Adler and E. G. Friedman (1998 [14]) utilizing Elmore (1948 [16]) delay model. Elmore delay approximation represents the first moment of the transfer function. Elmore's expression approximates the mid-point of the *monotonic step response* waveform by the mean of the impulse response as [14]

$$\tau_{Di} = \int_0^\infty t.v(t)dt \tag{1.1}$$

For the general topology of this *RC* tree network, this formula can be modified as [16]:

$$\tau_{Di} = \sum_{j=1}^{N} C_j \sum_{\substack{for\ all \\ k\epsilon j}} R_k \tag{1.2}$$

which is the Elmore delay at node *i* of this *RC* tree, which has the following path definitions:

- P_i denotes the unique path from the input node to node *i, i* = 1,2,3, ... , N.
- $P_{ij} = P_i \cap P_j$ denotes the portion of the path between the input and the node *i*, which is common to the path between the input and node *j*.

Unfortunately. Elmore delay cannot accurately estimate the delay for RLC interconnects, i.e. those interconnects whose inductive impedance cannot be neglected (Kahng and Muddu, 1996[7]). This is primarily due to the fact that the Elmore delay does not cover non-monotonic responses which can occur in RLC circuits. This inaccuracy of Elmore delay is harmful to current performance-driven routing methods which try to optimize interconnect segment lengths and widths as well as driver and buffer sizes.

Consequently in Friedman's model, the driving transistor was considered to operate always in linear mode and only the simplified case of step input was examined. Pillage et al. (1994 [18]) replaced the RC output load by an "effective" capacitance, which was calculated by an iteration procedure based on simplified assumptions for the shape of the output response. The real output waveform was approximated by the charging/discharging of the effective capacitance up to a point and capturing of the remaining portion of the output response is achieved by a simple resistive model.

Sakurai (1993, [17]) provided the response and delay calculation for the distributed RC line. He calculated the time-domain response from the transfer function using the Heaviside

expression over poles of the transfer function. He then approximated the response using a single pole and observes the variation of delay with respect to source and load parameters. His heuristic delay formula is almost identical to the Elmore delay equation. Hence, it buffers of the same constraints related to Elmore delay model mentioned above.

Krauter et al. (1995, [19]) proposed to improve the Elmore delay model by using higher order moments; this work led to a heuristic net delay model equal to the sum of the first moment (M 1) and its standard deviation $\sqrt{|M_1^2 - M_2|}$. Kahng et al. (2000, [21]) used Krauter et al. delay model; however, they realized that it is not accurate for various source and load parameters.

Another approach was proposed by Dartu, Menezes, Pileggi (1997[20]) where a time-varying Thevenin equivalent model is used for the estimation of the gate delays. The gate is replaced by an equivalent circuit model consisting of a linear voltage source and a linear resistor where their values are determined using empirical factors thus reducing the accuracy. In case the output load is not purely capacitive, an effective capacitance for the RC load is used. But the RC models present significantly lower accuracy mainly because they are based on simplified assumptions for the transistor operation and use simple load models for the representation of the interconnect lines.

A good and simple approximation of an interconnect line is obtained by Kahng et al. (1996, [21]) who studied various combinations of first and second moments, from which they developed their first delay analytical model of RLC interconnects, incorporating inductance effects while assuming step input. The solutions developed by Kahng et al. showed that Elmore delay (1948 [16]) estimates can vary as much as 50% from the SPICE-computed delays, while their proposed analytical delay model estimates are within 15% of the SPICE delays. Also, they found that an RLC model achieves an accuracy better than 3% in delay calculations in case a π- model is employed. In comparison, L-model needs 100 segments for same accuracy. Therefore, π-model is often used in Spice instead of large number of segments as a reasonable approximation of distributed RC.

A first attempt to model the interconnect line by a π-circuit was made by Sakurai (1993)[], however the driving transistor was replaced by a simple resistor. More accurate analytical expressions for the propagation delay and the output waveform can be found if the corresponding system equations of an inverter driving a circuit are solved.

Ismail and Friedman (2000 [22]) introduced a simple tractable delay formula for RLC trees. They tried to preserve the useful characteristics of the Elmore delay model while maintaining the same accuracy characteristics. This delay model with the closed-form expressions considers all damping conditions of an RLC circuit including the under damped response, which was not considered by the Elmore delay due to the non-monotonic nature of the response. They have given an empirical relationship for the propagation delay of a CMOS gate driving a distributed resistive inductive capacitive load, which gives an error within 5 percent of AS/X simulations. These solutions are presented for the 50% delay. rise time. overshoots. and settling time of signals in an RLC tree.They have shown that neglecting inductance in on-chip interconnects can cause errors over 35 percent in propagation delay and use much larger area. The CMOS devices are modeled as discrete RC components.

2.3 Repeaters for long interconnects and their delay models.

The increase in load in VLSI circuits especially due to large fanouts and the long interconnects, emphasize the need for effective driver circuits that can discharge capacitances with sufficient speed, thus helping in delay minimization. The insertion of repeaters is used to minimize the interconnect response time by mitigating the effect of resistance and capacitance (Bakoglu, 1990 [1]). Chapter 3 explains the role of repeaters in minimizing the RC constant, and with it the cumulative signal delay. However, the additional delay due to repeaters has to be taken into account.

Bakoglu and Meindl ([2]) proposed various types of repeaters viz. uniform cascaded and cascaded tapered repeaters to optimally drive resistive-capacitive interconnect to reduce the delay. They utilized Elmore approach to evaluate delay in interconnections loaded with such repeaters. They have shown that delay of a repeater loaded interconnect becomes a linear function of line length. MOSFETs have been modeled as discrete resistance and capacitance depending upon the geometric dimensions. They derived the optimum value of tapering factor for the cascaded buffer to be “e” the base of natural logarithm. However, this method is useful for capacitive loads as well as when interconnect resistance is small and driver resistance is dominant; but it is not adequate when interconnect resistance is comparable to or larger than driver resistance. Another important advantage of inserting repeaters within

interconnect trees is to decouple a large capacitance from the critical path in order to minimize the total overall delay of the critical path.

In 2001 Venkutesan, Davis and Meindl (2001 [8]) presented novel compact expressions for: (1) the time delay, (2) the peak crosstalk for coupled lines, (3) the optimum number and size of repeaters, and (4) the time delay for repeater-inserted distributed RC and RLC lines. For practical ranges of line parameters, the maximum error for time delay and crosstalk, and SPICE simulations are 2% and 10% respectively. These expressions that describe rigorously derived the transient response of a high-speed interconnect with on-chip global interconnect boundary conditions in a series of four papers [8-11]. Simplified expressions enable physical insight and accurate estimation of transient response, time delay, and overshoot for high-speed global interconnects with the inclusion of inductance.

Much research effort has been devoted during the last few years to model CMOS gates driving simple capacitive loads, especially *CMOS inverter/repeater*. The CMOS inverter is the simplest buffer or repeater in VLSI interconnects. Sakurai and Newton (1990 [15]) gave alpha-power MOS model for current voltage characteristics for short channel MOSFETs. They included input waveform slope effects and parasitic drain/source resistance effects. The short channel CMOS inverter delay becomes less sensitive to the input waveform slope and to the V_{DD} variation as compared to the conventional classic MOSFETs based on square law model given by Shockley.

Adler and Friedman (1998 [14]) dealt with repeater design to reduce both delay and power in interconnects using (Sakurai and Newton, 1990 [15]) α-power law model for short channel devices and the current voltage characteristics of MOSFETs. They reported that uniform repeaters outperform tapered buffers and tapered buffer repeaters when driving even relatively low RC loads. They demonstrated that 4 percent decrease in input to output delay can be traded off for a 40 percent saving in area and 15 percent saving in power.

Chatzigeorgiou and Nikolaidis (2001 [23]) modeled the short circuit power and the propagation delay by single equivalent transistor primitive of complex CMOS gates. They too used the α-power law MOS model. It was found that on an average, the execution speed of their method was 70 times faster than SPICE simulation for 0.5mm technology and 300times faster compared to SPICE for a 0.35mm technology.

Recently, Kaushik, et al. (2007 [24]) presented an analytical method with emphasis on the short-circuit power dissipation has been presented for an inverter driving an π-RLC load. The model shows an impressive accuracy. However, the proposed analysis is far too complex to be integrated into a CAD timing analysis system in spite of the simplified assumptions that are made for the short-circuit current.

2.4 Parameters limiting interconnect performance

With the advancement of technology, as the dimension of Cu interconnect are scaled down, the resistivity of copper is increasing rapidly under the combined effects of enhanced grain boundary scattering, surface scattering and the presence of a highly resistive diffusion barrier layer in deep-submicron technology nodes. These are the most important parameters that limit the efficiency of copper in future.

Saraswat et al. (2002 [26]) showed that Copper barrier oxide layer increases its effective resistivity to a high value, especially in case of local and semiglobal interconnects. As far as comparison between Copper and Aluminium is concerned, since Al does not need a four-sided barrier, this effect would degrade Cu resistivity a lot more.

It was found out that Al resistivity rises slower than Cu. This may lead to a higher copper effective resistivity than that of aluminum in the future. The cross over, where copper effective resistivity is higher occurs faster for local and semiglobal interconnects.

W. Steinhogl (2002 [25]) further characterized the increase in copper resistivity with decrease in line width, due to surface scattering and grain-boundary scattering. They proposed a model for copper taking into effect the surface scattering and grain-boundary scattering, which depended on various parameters included line width.The complete model and its effects are presented in [25] and its effects are summarised in Chapter 3.

In deep-submicron, designers tend to keep a high Aspect Ratio (ratio of interconnect thickness/height) since higher interconnect thickness/height decreases the inter-line capacitance. But, the two-dimensional fringing fields and capacitances between neighbouring lines become important and, after a certain point, larger aspect ratios yield no additional advantage

Schaper, et al. (1983, [27]) determined that as the AR get larger, the two-dimensional fringing fields and capacitances between neighbouring lines become important and, after a

certain point, larger aspect ratios yield no additional advantage. As a result, the capacitance per unit length of the wires in a multilevel interconnectional scheme approaches a lower limit of 2 pF/cm with SiO_2 as the dielectric material.

To improve signal speed, there is a trend to increase the line width, leading to reduction of spacing between two lines (smaller *pitch*). But Deodhar and Davis (2005 [25]) showed that this leads to a continuous increase in resistance and capacitance, negating improvement in interconnect delays, even forcing longer RC interconnect delays with each generation.

Due to the above issues, research is being carried out for new interconnect materials which could solve these problems and that potential candidate is CNT.

2.5 CNT as the future interconnect material

With the advent of high performance requirement, such as high current density and low interconnect delay of advanced integrated circuits, metallic carbon nanotube with its long mean free path (several micrometers) is seen as the viable candidate for future interconnect. There are two types of carbon nanotubes, namely, single-walled nanotubes (SWCNTs) and multi-walled nanotubes (MWCNTs).

F. Kreupl et al. (2002 [29]) showed that due to the strong sp^2 bonding (like graphite), carbon nanotubes are much less susceptible to electro migration (EM) Problems that plague the copper interconnects. They can also carry very high current densities. Metallic single walled CNT bundles are able to carry extremely high current densities of the order of 10^9 A./cm^2 . Cu interconnects on the other hand, have a current carrying capacity of 10^6 A./cm^2 due to M effect. However, F. Kreupl et al. (2002 [29]) and J. Li et al. (2003 [30]) pointed out that a singlewall nanotube results in a very high contact resistance and high characteristic impedance, and hence a bundle of closely packed parallel CNTs is preferably used above a ground plane.

P. Burke et al. (2002 [32]) proposed a CNT interconnect model where they observed that resistance for CNTs has typically been in the range of 10 KΩ. Their equivalent model had two capacitances associated with it- electrostatic capacitance (≈ femto farads) and quantum capacitance (≈100 af/μm). Furthermore, there is associated magnetic inductance and kinetic inductance. For obtaining the resistance and inductance of a bundle, the resistance and capacitance of an individual CNT can be divided by the number of CNTs in the bundle.

Srivastava et al. (2005 [33], [35]), Li et al. (2006 [30], [34]) and Massoud, et al. (2009 [36]) compared the performance of the CNT bundle interconnect and Cu interconnect for local, semiglobal and global interconnects. It was seen that the propagation delay ration of CNT and Cu interconnect is very high at the local level, but undergoes a steep decreases as it is moved to the semi global level where it first decreases to a minimum value and then increases by a slight amount finally becoming constant at lengths of global level.

It is also reported by K. Banerjee and N. Srivastava. (2005 [35]) that pitch influences semi global and global relative performance of CNT as it does in case of local lengths. For the local interconnects, the influence of pitch on delay of CNT bundle is quite significant. It can be seen that the delay ratio of CNT bundle to Cu interconnect is increased when the pitch increases.

Li et al. (2007 [39]) have proposed to use bundles of CNTs with large migration tolerance as vias to get enough current for ultra large-scale integrated (ULSI) interconnections. They suggest that the total resistance of the CNT via is about three orders of magnitude lower than that of a single CNT and that there is no visible degradation of the via current with time. It is expected that CNT bundle vias will prove to be effective replacements for copper vias for future ULSI interconnections.

Thiruvenkatesan et al. (2009 [40]) used a carry-save-adder-array multiplier to study the effects of copper interconnect and carbon nanotube interconnect. The performance of critical delay with respect to device technology is presented it also showed that the ratio of the delay of CNT bundle to that of Cu wire reaches its minimum interconnect length exists for CNT in the semi- global level.

Vivo et al. (2010 [41]) described a new model based on Multi Wall CNTs, suitable for the 32 and 22 nm technology, where they evaluated the upper and lower bounds of the time-delay due to the variations of some physical and geometrical characteristics of a nano-interconnects. The obtained results are compared with those of scaled down copper-based structures where it indicates that the CNT interconnect has better performance.

Mayank Kumar Rai and Sankar Sarkar (2011 [51]) addressed the influence of tube diameter on single walled carbon nanotube (CNT) bundle interconnect delay and power output in VLSI application. They found that single-walled carbon nanotube (SWCNT) bundle interconnects

are of lower delay than copper interconnect due to low resistance and inductance. Power dissipation decreases with increase in tube diameter of the constituent SWCNT. CNT interconnect resistance and inductance increases with increase in tube diameter. On the other hand, with increase in tube diameter interconnect capacitance decreases. There is a trade off between delay and power dependence on tube diameter.

Recent research in the study of metallic carbon nanotube by S. Sarkar et al. (2011 [52]) show that in 32 nm and 22 nm nodes, CNT shows better relative performance for longer interconnects. They have reviewed all the possible parameters to explore the applicability of CNTs as future interconnects. Thus, as technology nodes shrink in the future, CNT has become the most prospective material of future.

In summary, a bibliographic survey of the works carried out to explore the design methodologies and delay analysis techniques for VLSI interconnect. A viable option for reducing delays is to use better interconnect material with lower resistivity (higher conductivity).

CHAPTER

3

INFLUENCE OF VARIOUS PARAMETERS ON INTER-CONNECT PERFORMANCE

3.1 Introduction

Interconnects are wires connecting gates in VLSI circuits. They can either be global or local. In general, local interconnects are the lowest level of interconnects, used to connect nearby cells. At the next level comes Intermediate/semiglobal interconnects which are used to connect devices within a block. Global interconnects are generally all of the interconnect levels above the local interconnect level. They often travel over large distances, between different devices including power, ground and clocks.

An interconnect, shown in Fig. 3.1 with length L, width *w*, space *s* and placed at height X_{ox} from the ground plane.

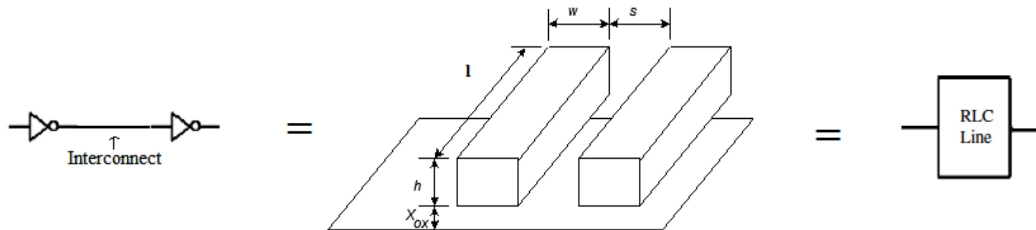

Fig. 3.1: Interconnection and its 3-D view signifying its RLC parasitics

With the introduction of deep-submicron semiconductor technologies, the typical channel length in a transistor has shrunk to a nominal value of less than 0.1 micron [42]. With this type of resolution, both die size and device density of the VLSI circuits are on the increase. The increased die size makes long interconnect lines to be common features in VLSI chips. The long interconnections lead to prohibitively high propagation delays. The footprint area required for an FET has shrunk to the point where it is almost insignificant when compared with the surface area needed for contacts, vias, and interconnect routing. Thus leads to the conclusion that modern CMOS chip design is interconnect-limited such that they have started to dominate some of the relevant metrics of digital integrated circuits such as speed, energy-

consumption, and reliability. A careful and in-depth analysis of the role and the behaviour of the interconnect wire in a semiconductor technology is therefore not only desirable, but even essential. Accurate modeling of on-chip wiring is important to the circuit designer which takes into consideration the parasitic-induced delays and stray coupling.

The Parasitics effects introduced by the interconnection wires display a scaling behaviour that differs from the active devices such as transistors, and tend to gain in importance as device dimensions are reduced and circuit speed is increased. This situation is aggravated by the fact that improvements in technology make the production of ever larger die sizes economically feasible, which results in an increase in the average length of an interconnect wire and in the associated parasitic effects.

It is predicted that interconnects will be responsible for nearly 70 to 80% of the signal delay in high-speed systems. If not considered during the design stage, these interconnect effects can cause logic glitches that render a fabricated digital circuit inoperable, or they can distort an analog signal such that it fails to meet specifications. Since extra iterations in the design cycle are costly, accurate prediction of these effects is a necessity in high-speed designs.

3.2 Interconnect Parasitics

Interconnect introduces three types of parasitic effects—capacitive, resistive, and inductive—all of which influence the signal integrity and degrade the performance of the circuit. The basic geometry is shown below. This is representative of an interconnect line that is described by a width ‘w’, and has a length of *l*. The material layer itself has a height (or thickness) *h*.

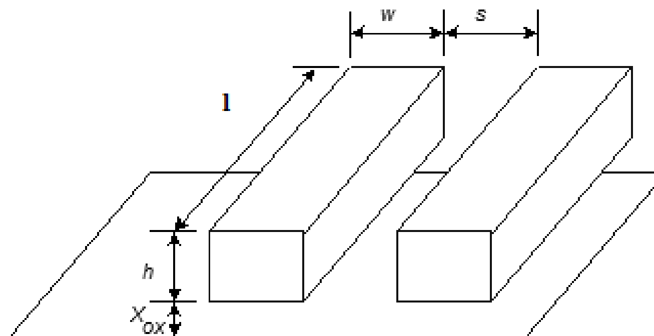

Fig. 3.2: Interconnection dimensions

Line Resistance

The resistance of the line from one end to the other is computed by using the standard equation

$$R = {}^{\rho l}/_{A} = \frac{\rho}{h}\left({}^{l}/_{w} \right) = R_s\left({}^{l}/_{w} \right) \tag{3.1}$$

where ρ is the resistivity in units of [Ω-cm] and $A = hw$ is the cross-sectional area of the line. Every material is characterized by a value of ρ. When choosing interconnect lines, metals dominate due to their small values of resistivity. Although this expression can be used directly, a more useful formulation for use in chip design is based on the use of the sheet resistance which has units of ohms for the layer. This is defined by

$$R_s = {}^{\rho}/_{h} \tag{3.2}$$

and is the end-to-end resistance of a square section of material with $d = w$ as seen from the top. The sheet resistance is useful as it can be directly measured on a test structure in the laboratory. Once $\boldsymbol{R_s}$ is known, then the total resistance R of a line that has a width w and spans a distance d is given by

$$R = R_s . n \tag{3.3}$$

where $n = l/w$ is the **number of squares** of dimensions ($w \times w$) encountered by the current. Owing to this observation, $\boldsymbol{R_s}$ has units of "ohms per square". This can be seen by the top view of the interconnect shown below.

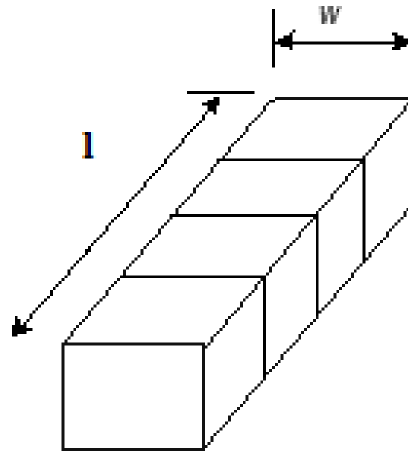

Fig. 3.3: Calculation of line resistance from sheet resistance (R_s)

Line Capacitance

The capacitance of an interconnect line can be the limiting factor in high-speed signal transmission. Consider the cross-sectional geometry shown below

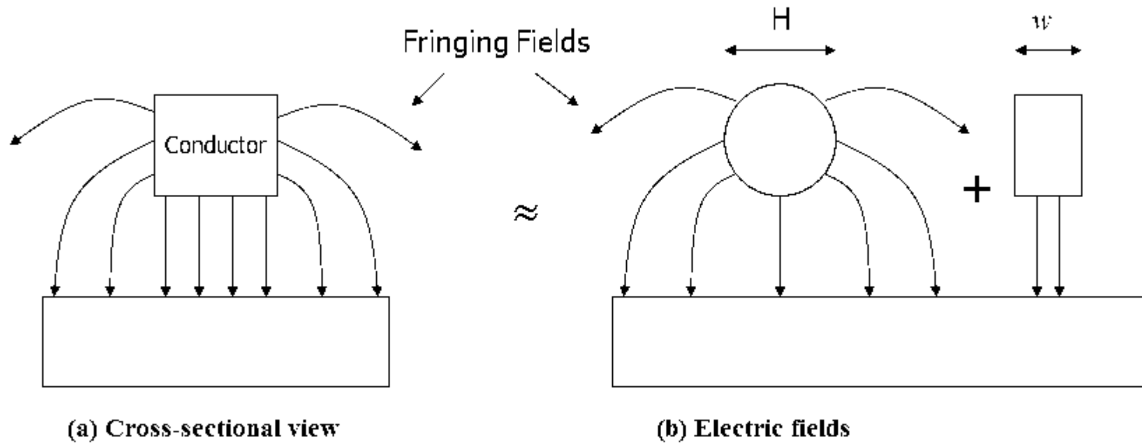

Fig. 3.4: Interconnection capacitance: (a) shows the parallel plate capacitance only (C_{pp}) and (b) shows the additional effect of fringing fields (C_{fringe}) [44]

The total capacitance of the line in farads is given by

$$c_{int} = c^{'}L \tag{3.4}$$

where *c'* (farads per centimeter) is obtained from the parallel-plate capacitor as

$$c^{'} = \varepsilon_{dielectric} \, . w/X_{ox} \tag{3.5}$$

However, this formula ignores the existence of fringing electric fields at the edges (shown in Figure (b), and is therefore too small. A more accurate empirical expression is

$$c_{wire} = c_{pp} + c_{fringe} = \frac{\varepsilon_{dielectric}}{X_{ox}} w + \frac{2\pi\varepsilon_{dielectric}}{\log(X_{ox}/h)} \tag{3.6}$$

The first term is the standard parallel plate formula while the second term accounts for fringing field lines that originate from the side of the layer with a height *h*.

Line Inductance

With the adoption of low-resistive interconnect materials and the increase of switching frequencies to the super GHz range, inductance starts to play a role even on a chip.

The inductance of a section of a circuit can always be evaluated with the aid of its definition, which states that a changing current passing through an inductor generates a voltage drop ΔV:

$$\Delta V = L \, {}^{di}/_{dt} \quad (3.7)$$

The importance of inductance in high-performance very large scale integration (VLSI) design methodologies will increase as technologies scale. It is imperative that inductance be included in the interconnect impedance model when inserting repeaters to drive RLC trees in high speed circuits.

3.3 Interconnect Models

To study the parasitic effects described above requires the introduction of electrical models that estimate and approximate the real behaviour of the wire as a function of its parameters. These models vary from very simple to very complex depending upon the effects that are being studied and the required accuracy.

3.3.1 The Lumped Model

The circuit Parasitics of a wire are distributed along its length and are not lumped into a single position. Yet, for fast observation of the effects of Parasitics, or when looking at only one aspect of the circuit behaviour, it is often useful to lump the different fractions into a single circuit element. As long as the inductive component of the wire is small and the switching frequencies are in the low to medium range, it is meaningful to consider only the resistance and capacitive component of the wire, and to lump the distributed capacitance into a single RC model as described below.

3.3.1(a) The Lumped RC model

There are different configurations of RC Interconnect models [45] as shown below

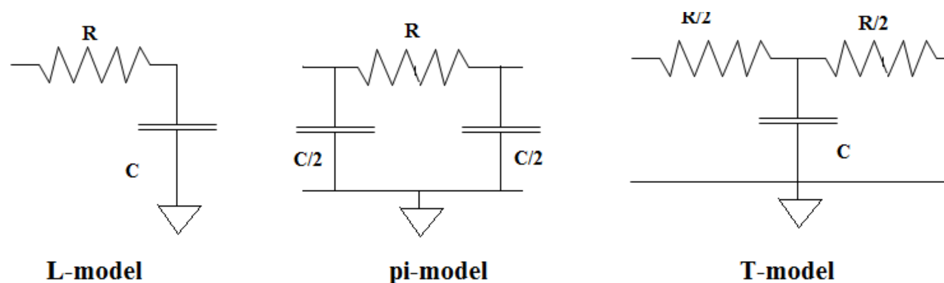

Fig. 3.5: Different configurations of RC Interconnect models [18]

Kahng and Muddu [21] proposed a pi-model for distributed RLC interconnects to estimate the driving point admittance at the output of a CMOS gate. A good and simple approximation of an interconnect line is obtained with the pi-model, achieving better accuracy in estimating output waveform and delay calculations.

3.3.1(b) The Lumped RLC model

With the adoption of low-resistive interconnect materials and the increase of switching frequencies to the super GHz range, inductance starts to play a role even on a chip. Global interconnects are often wide wires. These wires are low resistance lines that can exhibit significant inductive effects. The lumped-RC model, is no longer adequate, and a resistive-inductive-capacitive model has to be adopted [22].

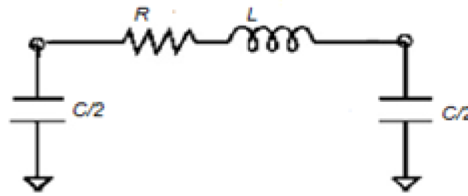

Fig. 3.6: RLC Interconnect model [22]

3.3.2 The Distributed *rc* Line

The lumped *RC* model is a highly inaccurate model, and for a resistive-capacitive wire a distributed *rc* model is more appropriate. As before, *L* represents the total length of the wire, while *r* and *c* stand for the resistance and capacitance per unit length.

The distributed *rc* line can be approximated by a lumped multi-stage *RC* ladder network (that has *m* rungs), which can be easily used in computer-aided analysis. Defining the individual element values by

$$R_N = R/N \quad \text{and} \quad C_N = C/N \tag{3.9}$$

allows us to construct the desired ladder network. Figure below shows the equivalent circuits for the cases of *m*. With m=3,

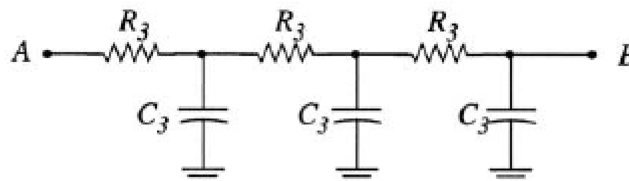

Fig. 3.7: Distributed RC Interconnect model divided into 3 parts

It is observed that the distributed *rc* ladder will yield more accurate results. However, since the introduction of additional nodes into a circuit simulation program increases the CPU time, the ladder simulation will take longer to execute. For example, SPICE models an *N*-node circuit by using matrices of dimensions $N \times N$, so that using ladders with large values of m increases the matrix size quadratic ally. This results in increased computer time for the simulations.

3.4 Scaling of device and interconnection lines

The area occupied by an MOS transistor can be made smaller by shortening its channel width and length leading to a faster device. Based on Constant Field device scaling, in Table 3.1 has been suggested.

Table 3.1: MOS device scaling for a Constant Field

Device/Circuit Parameter	Scaling Factor (S)
Device dimensions L, W_c, X_{gox}	$1/S$
Voltage	$1/S$
Field	1
Gate Delay	$1/S$

According to Table 3.1, as the average feature size drops by a scaling factor of 1/S, gate delay is reduced by a factor of 1/S.

As device dimensions are miniaturized, the interconnection dimensions must also be reduced. A straightforward approach to satisfying the processing and layout constraints is to scale all cross-sectional interconnection dimensions (w, L, h, s) by the same factor as used for transistors (**Ideal Scaling**).

The effects of scaling on local and long distance interconnections are listed in Tables 3.2 and 3.3. The dimensions can be referred from Fig. 3.2.

Table 3.2: Scaling of local interconnection lines for Constant Field (S =Scaling Factor)

Interconnection Parameter	**Ideal Scaling**	**Quasi-Ideal Scaling**	**Constant-R Scaling**
Interconnection dimensions (Horizontal) w, h, L, s	$1/S$	$1/S$	$1/\sqrt{S}$
Interconnection dimensions (Vertical) h, X_{ox}	$1/S$	$1/\sqrt{S}$	$1/\sqrt{S}$
Line resistance $R = \rho L/w.h$	S	$1/\sqrt{S}$	1
Line capacitance $C_{int} = k_{ox}\ \varepsilon_o\ s.w/X_{ox}$	$1/S$	$1/S^{3/2}$	$1/S$
RC Delay	1	$1/\sqrt{S}$	$1/S$
Line current density	S	$\sqrt{S}$	$1/S$

It can be seen in Table 3.2 that, after scaling, the line response time remains constant and the line voltage drop stays the same; however, current density increases which can introduce severe device-performance problems, such as electro migration.

Deviation from ideal scaling can be advantageous. Scaling interconnections and field-oxide thickness by factors smaller than $\boldsymbol{S}$ will lower RC delay. Two alternative approaches to minimizing propagation delay are also presented in Tables 3.2 and 3.3. In "quasi-ideal" scaling of local interconnections, the horizontal dimensions are scaled by $1/S$ (like transistors) to improve overall packing density by a factor S. On the other hand, the vertical dimensions are reduced only by $1/S$ to maintain a small RC time constant and, as a result, delay decreases by $1/\sqrt{S}$. In "constant-R" scaling, all cross-sectional dimensions are reduced only by $1/\sqrt{S}$ and, consequently, propagation delay is lowered by $1/S$.

Long-distance interconnections are more difficult because of the additional burden introduced by their increasing chip size. The effect of long-distance interconnection lines on total delay time for the transmission of signals from block to block is discussed below:

Table 3.3: Scaling of Long distance interconnection lines for Constant Field (S =Scaling Factor, S_c = die-size Scaling factor)

Interconnection Parameter	**Ideal Scaling**	**Constant Dimension**	**Constant Delay**
Long-distance interconnection dimensions w, L, h, s, X_{ox}	$1/S$	1	S_c
Long-distance interconnection dimension L_{max}	S_c	S_c	S_c
Line resistance $R = \rho L/w.h$	$S^2.S_c$	S_c	$1/S_c$
Line capacitance $C_{int} = k_{ox}\ \varepsilon_o\ s.w/X_{ox}$	S_c	S_c	S_c
RC Delay	$S^2.S_c^2$	S_c^2	1

The results of Ideal scaling are summarized in Table 3.3 where it is assumed that the maximum long-distance or block-to-block interconnection line increases by a factor of $S_c > 3$. Because the long-distance line response time rises drastically as a result of scaling, a substantial amount of delay and the performance of the circuits cap suffer from technological advancement,

In “constant-dimension” scaling of long-distance interconnections, all cross-sectional dimensions are held constant, and propagation delay rises by S_c^2 because of the growth in chip size. In "constant-delay" scaling, the cross-sectional interconnection dimensions are increased such that the improvement in the RC delay per unit length cancels the effect of increasing chip size and total delay remains constant.

3.5 Role of Repeaters

Repeaters are intermediate buffers in the interconnect line. They are effectively driver circuits that can discharge capacitances with sufficient speed, thus helping in delay minimization. The use of repeaters makes time delay linear with length by dividing the interconnection into smaller subsections.

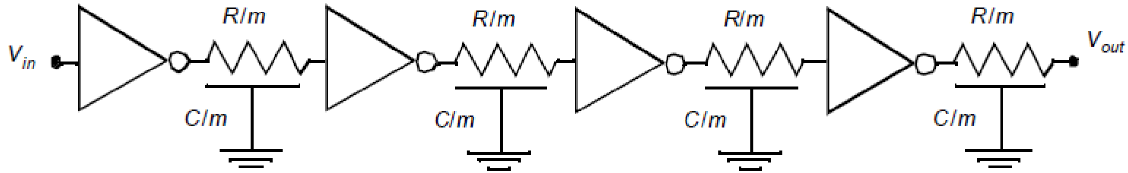

Fig. 3.8: Distributed RC Interconnect with Repeaters (Buffers) inserted in between [14].

The insertion of repeaters is used to minimize the interconnect response time by mitigating the effect of resistance and capacitance. The delay of a wire grows quadratically with its length. The signal delay of long (global) wires therefore tends to be dominated by the *RC* effect. This is becoming an ever larger problem in modern technologies, which feature an increasing average length of the global wires at the same time that the average delay of the individual gates is going down. This leads to the rather bizarre situation that it may take multiple clock cycles to get a signal from one side of a chip to its opposite end. Providing accurate synchronization and correct operation becomes a major challenge under these circumstances.

Repeater Design

The repeaters can be of different types viz.

(a) uniform 'Minimum' sized

$$(W/L)_{driver} = 1, (W/L)_{load} = 3 \tag{3.10}$$

(b) Optimum sized; - Increasing size of repeaters to improve propagation time

(c) Variable tapered repeaters

- Sequence of drivers that increase gradually in size
- Used to drive large capacitive loads;
- tapered cascaded buffers, consisting of optimum number of repeaters in one stage and an appropriate tapering factor

As shown in Fig. 3(j)(c), when applied to interconnections this method optimizes the sum of the delay caused by charging the input capacitances of the cascaded drivers and the interconnection propagation delay. Total delay is then expressed as

$$T = 2.3(n-1)fR_oC_o + \left(\frac{2.3R_o}{f^{n-1}} + R_{int}\right)C_{int} \qquad (3.11)$$

where f is the 'optimum value' of tapering factor for the cascaded buffer.

By setting $\boldsymbol{dT/dn}$ to zero, we derive the optimum value of tapering factor $= \boldsymbol{e}$, the base of natural logarithm.

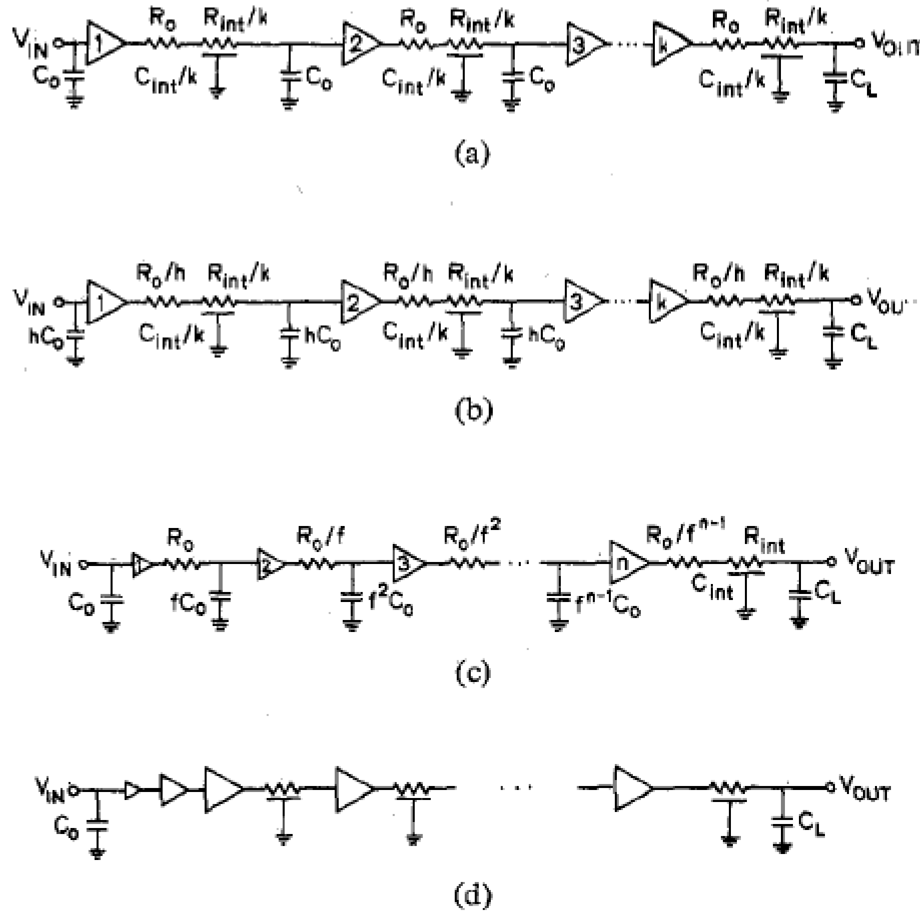

Fig. 3.9: Different types of Repeater Design: (a) Minimum size repeaters. (b) Optimal repeaters. (c) Cascaded drivers. (d) Optimal repeaters with a cascaded first stage [2].

3.5.1 Repeater model (Bakoglu and Mendl model)

According to Bakoglu and Mendl [2], the propagation delay of an interconnection with k minimum-size inverters as repeaters can be expressed as:

$$T = k\left[0.7\ \frac{R_o}{h}\left(\frac{C_{\text{int}}}{k} + hC_o\right) + \frac{R_{\text{int}}}{k}\left(0.4\frac{C_{\text{int}}}{k} + 0.7hC_o\right)\right] \qquad (3.12)$$

where C_o and R_o are the input capacitance and output resistance of the minimum size inverter. The *W/L* ratios of the transistors are increased by a factor *h* to improve the propagation time can be further improved, the output resistance and input capacitance become R_o/h and hC_o.

The optimal number of repeaters (k) that minimizes the overall delay can be found by setting *dT/dk* to zero.

$$k = \sqrt{\frac{R_{\text{int}}C_{\text{int}}}{2.3R_oC_o}} \tag{3.13}$$

By setting and *dT/dh* to zero, optimal value of transister sizing (h) is obtained as

$$h = \sqrt{\frac{R_oC_{\text{int}}}{R_{\text{int}}C_o}} \tag{3.14}$$

yielding a minimum delay of

$$T = 2.3\sqrt{R_oC_oR_{\text{int}}C_{\text{int}}} \tag{3.15}$$

and is obtained when the delay of the individual wire segments is made equal to that of a repeater. For long-distance interconnections, C_{int} is on the order of pico farads and C_o is on the order of femptofarads, and R_{int} and R, have values around kilo ohms; therefore, RoCint>>RintCo, and the delay expression can be further simplified to

$$T = 2.3R_oC_{\text{int}} \tag{3.16}$$

As a result, repeaters can effectively "transform" the interconnection into a capacitive load.

When the resistance of the interconnection is comparable or larger than the on-resistance of the driver, propagation delay increases as the square of the interconnection length because both capacitance and resistance increase linearly will length.

RC Delay $$t_{int} = (RL)(CL) = RC.L^2 \tag{3.17}$$

For Local interconnects:

$$t_{int} = (R.S^2)(C)\left(\frac{L}{S}\right)^2 = RC.L^2 \tag{3.18}$$

So, Local interconnect delay unchanged (compared to faster devices)

For Global interconnects:

$$t_{int} = (R.S^2)(C)(L.S_c)^2 = (RC.L^2).(S.S_c)^2 \qquad (3.19)$$

So, Global interconnect delay grows quadratically.

Since repeaters have turned the interconnection into a capacitive load:

$$t_{int} = (CS)(L.\ S_c) = (CL).(S.S_c\ ) \qquad (3.20)$$

Thus, the use of repeaters makes time variation of delay 'linear' with length.

3.6 Effect of various parameters in interconnect performance

3.6.1 Dielectric effect

Inter-line capacitance of interconnects is given by the parallel-plate equation:

$$C = \varepsilon_{dielectric}\ .wL/X_{ox} \qquad (3.21)$$

The Dielectric constant (k) of the dielectric materials between interconnections affects the capacitance.

$$\varepsilon_{dielectric} = k\varepsilon_0 \text{ (where } \varepsilon_0 = 8.85\ x\ 10^{-14}\ F/cm) \qquad (3.22)$$

The prominent oxide layer is silicon–dioxide (SiO_2), which has k = 3.9 .Replacing aluminium and silicon–dioxide (SiO_2) with copper and low dielectric constant (low-k) materials, respectively can reduce the interconnect delay. This material set replacement helps increase the speed of interconnects by reducing resistance and capacitance per unit length. But, low-k materials are more prone to dielectric breakdown due to increasing current densities.

3.6.2 Pitch of Interconnect

Pitch is defined as the sum of interconnect width (w) and the spacing between two lines (s). The width as well as the spacing between two lines is labelled below.

$$Pitch = w + s \qquad (3.23)$$

To improve signal speed, there is a trend to increase the line width, w. As the width of interconnect increases, line-resistance decreases as seen in the line resistance equation:

$$R = R_s\ {}^{l}/_{w} \qquad (3.24)$$

But the inter-line Capacitance (due to coupling C_c) increases on reduction of spacing between two lines (s) as seen from the capacitive coupling equation:

$$C_{pp} = \varepsilon_{dielectric}\ .h.L/s \qquad (3.25)$$

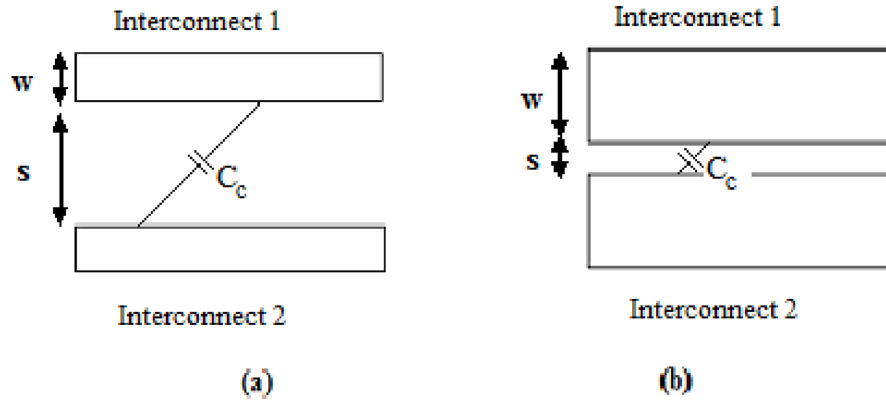

Fig. 3.10: Variation of width between two coupled interconnects; C_c shows the coupling capacitance between interconnects: (a) wires with small widths, *w* and large spacing, *s* (b) wires with larger widths, *w* and smaller spacing, *s*.

Thus, more closely packed interconnects (smaller pitch) leads to a continuous increase in resistance and capacitance, negating improvement in interconnect delays, even forcing longer RC interconnect delays with each generation [25]. Another adverse effect of smaller pitch is the increase in signal noise.

3.6.3 Length of Interconnect

As the length of interconnect increases, line resistance increases.

$$R = R_s \, {}^{l}\!/_{w} \tag{3.26}$$

This severely increases the interconnect delay. In lower technology nodes, this problem is particularly severe in Global interconnects [27]. Scaling effects further aggravate this problem, as discussed in Chapter 3.

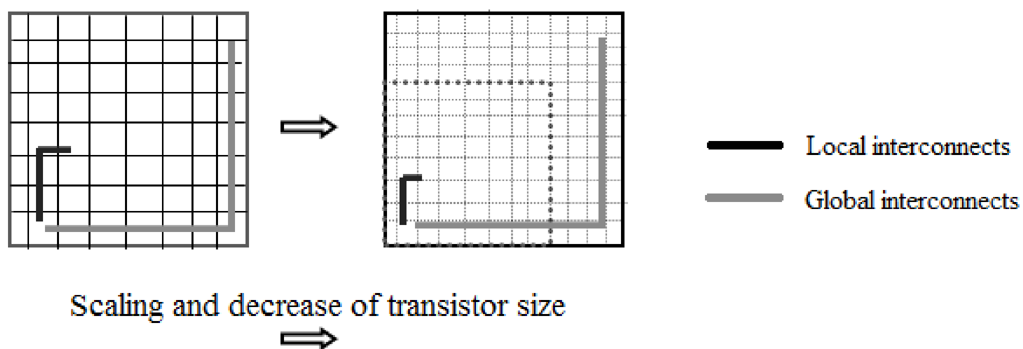

Fig. 3.11: Relative scaling of Global and Local interconnect with technology advancement.

Also, in deep-submicron, designers tend to keep a high AR (AR ≈ 2) since higher interconnect thickness/height decreases the inter-line capacitance. This further depreciates performance.

It was observed in Chapter 1 that Global interconnect lengths are not shrunk, whereas Local interconnect lengths shrink by scaling factor, S [27].

3.6.4 Aspect Ratio

For an interconnect, Aspect Ratio is defined as the ratio of interconnect thickness/height, h and width, w

$$AR = h/w \tag{3.27}$$

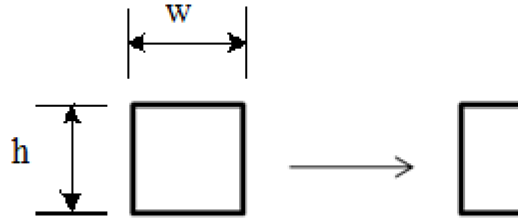

Fig. 3.12: Increase in AR with the increase of interconnect thickness/height, *h* with respect to width, *w*.

In older technologies (1 micron and above), interconnect thickness/height was scaled down so that AR << 3. But in deep-submicron, designers tend to keep a high AR (AR ≈ 2) since higher interconnect thickness/height decreases the inter-line capacitance. Since $h >> w$, C_{pp} decreases

$$C_{pp} = \varepsilon_{dielectric} \, .h.L/s \tag{3.28}$$

But, as the AR get larger, the two-dimensional fringing fields and capacitances between neighbouring lines become important and, after a certain point, larger aspect ratios yield no additional advantage. As a result, the capacitance per unit length of the wires in a multilevel interconnection scheme approaches a lower limit of 2 pF/cm [28].

3.7 Challenges of Cu Interconnects in Deep Sub-micron technologies

Resistivity of copper is increasing rapidly under the combined effects of enhanced grain boundary scattering, surface scattering and the presence of a highly resistive diffusion barrier layer in deep-submicron technology nodes. These are the most important parameters that limit the efficiency of copper in future.

3.7.1 Grain Boundary effect

Grain Boundaries are the internal interfaces that separate neighbouring disoriented single crystals in a polycrystalline solid [26]. Copper has a crystalline structure, but when engineered for use they become polycrystalline in nature in that they are made of many small single crystals which are disoriented with respect to each other. Grain boundaries are interfaces where crystals of different orientations meet. Grain boundary areas contain those atoms that have been perturbed from their original lattice sites, dislocations, and impurities that have migrated to the lower energy grain boundary.

Grain boundaries cause electron scattering leading to reduction in mobility. The least resistive Cu film is composed of the larger grained Cu. The smaller the grains, the higher the resistance, and slower the electrons will travel through interconnect.

The mathematical formulation governing the theory of scattering results in the following equation for scattering of electrons at Grain-boundaries ρ_g. [26].

$$\frac{\rho_g}{\rho_o} = \frac{1}{3\left[\frac{1}{3} - \frac{\alpha}{2} + \alpha^2 - \alpha^3 ln\left(1 + \frac{1}{\alpha}\right)\right]} \tag{3.29}$$

where

$$\alpha = \frac{1}{d'}\left(\frac{R}{1-R}\right)$$

Here, ρ_o is the bulk resistivity at a given temperature, d' is the smallest film thickness (distance between grain boundaries), and R is the reflectivity coefficient that denotes the fraction of electrons that are not scattered by the potential barrier at a grain boundary, and

From, the equation it can be seen that reduction in d' (width of the wire) increases α, which further increases the resistivity $\boldsymbol{\rho_g}$ and hence the resistance of Copper.

3.7.2 Surface Scattering

With dimensional shrinkage, the bulk mean free path of electrons will become comparable to the wire dimensions, leading to a non negligible scattering rate from the interface. Electron surface scattering: resistivity increases in future. Electron mobility reduces as dimensions decrease. Copper/barrier interface quality further reduces the mobility of electrons (Fig 3.13)

Fig. 3.13 Schematic showing electron surface scattering [27]

The mathematical formulation governing the theory of scattering results in the following equation for surface-scattering-dependent resistivity ρ_s. [26].

$$\frac{\rho_s}{\rho_o} = 1 + \frac{3}{4}(1-p)\frac{l}{d}$$

(3.30)

Here, p is the fraction of electrons scattered specularly at the surface, d is width of the wire, l is mean free path.

From, the equation it is clear that an increase in p (scattered electrons) or a reduction in d (width of the wire) increases the resistivity ρ_s and hence the resistance of Copper.

3.7.3 Diffusion Barrier Width

Copper is very mobile in SiO_2 , it diffuses into neighbouring dielectric silicon .This leads to contamination to Si Devices and damage of FETs, Therefore, copper wires must be surrounded by a diffusion barrier. Due to high resistivity of the diffusion barrier accompanying Cu, the effective resistivity of Copper wires, $\boldsymbol{\rho}$ increases.

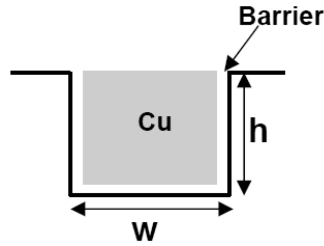

Fig. 3.14: Interconnect cross section, depicting the effect of barrier deposition technology on profile [26].

With the introduction of lower semiconductor technologies, copper cross-sectional area is scaled down (reduced). But the barrier does not scale as rapidly as the interconnect dimensions because of reliability constraints. This will lead to a progressively larger fraction of the cross section area being occupied by the high resistivity barrier, thus, an increase in effective resistivity of the interconnect stack. On the other hand, with dimensional shrinkage, the bulk mean free path of electrons will become comparable to the wire dimensions, leading to a non-negligible scattering rate from the interface. To compound the problem, the operational temperature is also likely to rise owing to a larger chip power density in the future.

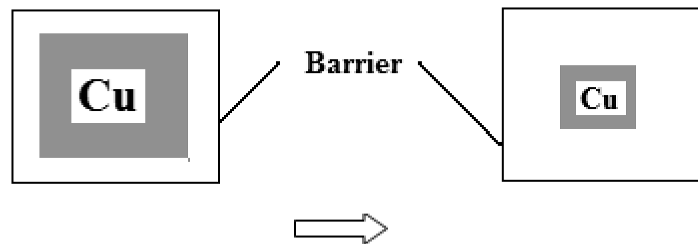

Fig. 3.15: Relative variation of barrier width with the decrease of Copper width due to scaling effects.

3.8 CNT – a future candidate for VLSI Interconnect

A viable option for reducing *RC* delays is to use better interconnect. The introduction of wires with lower resistivity (higher conductivity) reduces delay, while the adoption of dielectric materials with a lower permittivity lowers the capacitance. Both Copper and low-permittivity dielectrics have become common in advanced CMOS technologies (starting from the 0.18 mm technology generation). Yet, with the advent of deep-submicron technology nodes there are several disadvantages in Copper as mentioned above. So, we need

a potential candidate for interconnect material that is compatible with lower technologies. This potential candidate is Carbon Nanotube (CNT).

A Carbon Nanotube is a Graphene sheet rolled into a tube. These tubes have a diameter of the order of nm, hence the name. The process of nanotube formation eliminates all dangling bonds which immensely aids conduction of electrons within the tube. According to their chirality (during nanotube formation) CNT are of either metallic nature or semiconducting, known as Metallic CNT or Semi-conducting CNT respectively.

3.8.1 Classification on the basis of CNT structure

Carbon nanotubes can be classified into two types on the basis of their structure:

(1) Single-walled Carbon Nanotubes (SWCNTs)

(2) Multi-walled Carbon Nanotubes (MWCNTs)

(1) Single-walled carbon nanotubes

Single Wall CNT (SWCNT) consists of a single layer of graphene sheet seamlessly wrapped into a cylindrical tube. They are generated when a two dimensional graphene sheet of a certain size that is wrapped in a certain direction. SWCNTs have only one layer of graphene sheet with diameters of 0.7 to 10 nm (Figure.3).

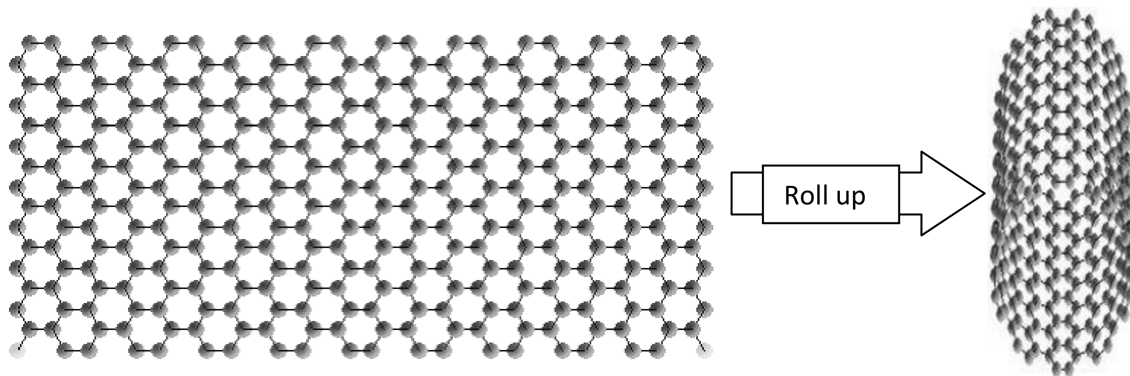

Fig. 3.16: A graphene layer folded in to SWCNT [33]

(2) Multi-walled carbon nanotubes

Multi walled carbon nanotubes (MWCNT) consist of concentric CNT cylinders held within each other by vander Waals forces. The distance between shells is approximately 3.4Å, which is the vander Waals distance for two graphite carbon lattices [33]. An example of a MWCNT is shown in Figure 1-2.

There are two models which can be used to describe the structures of multi-walled nanotubes. In the *Russian Doll* model, sheets of graphite are arranged in concentric cylinders. In the *Parchment* model, a single sheet of graphite is rolled in around itself, resembling a scroll of parchment or a rolled up newspaper.

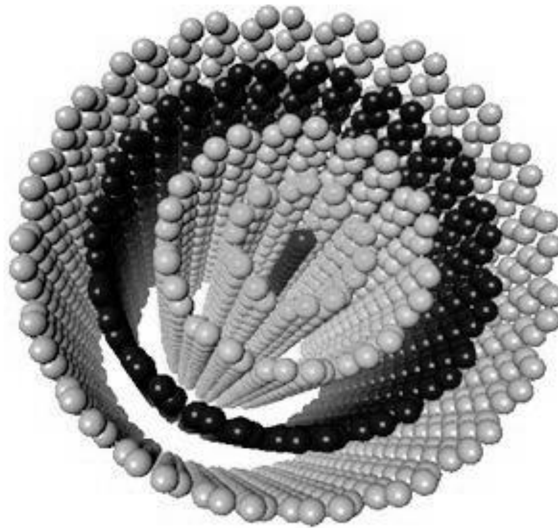

Fig. 3.17: Multiwalled carbon nanotube (MWCNT) [33]

While SWCNTs can be either metallic or semiconducting depending on their chirality, MWCNTs are always metallic and easier to fabricate. However, they are less favourable for interconnects because

- they typically exhibit ballistic conductance over very short lengths as compared to SWCNTs which have typical mean free paths of the order of a micron.
- The concentric shells of MWCNTs can differ in their chirality and can consist of both semiconducting and metallic nanotubes. This translates to different MFPs and the resistances of different shells cannot be assumed to be equal as in the case of SWCNT bundles. This coupling resistance will be dependent on the point of contact of wire and conducting shell, and in turn can be very large.

3.8.2 CNT as an Interconnect

Both SWCNTs and MWCNTs are usually many micrometers long and hence can fit well as components in sub-micrometer-scale devices and nanocomposite structures that may play an important role in emerging technologies. IBM has recently been able to manipulate the nanotubes in a controlled way. It has developed the capability of changing a nanotube’s position, shape, and orientation as well as cutting it by using an atomic force microscope. NASA researchers have reported a new method for producing ICs using CNTs instead of copper for interconnections. This technology may extend the life of the silicon chip industry by 10 years.

To a large extent, the unique electrical properties of CNTs such as their extremely low electric resistance are derived from their 1D character and the unique electronic structure of graphite. Resistance primarily occurs due to defects in crystal structure, impurity atoms, or an atom vibrating about its position in the crystal. In the case of a CNT, the electrons are not so easily scattered. Due to their small diameter and huge aspect ratio (length to width), nanotubes are essentially 1D systems and therefore electrons have a low chance of scattering, giving rise to very low resistance. The electronic properties of perfect MWCNTs are rather similar to those of perfect SWCNTs because the coupling between the cylinders is weak in MWCNTs.

Electrical transport in metallic SWCNTs and MWCNTs is ballistic, that is, without scattering over long nanotube lengths, enabling them to carry high currents with essentially no heating. In contrast, electrons in copper travel only 40–50 nm before they scatter. The low resistance ensures that the energy dissipated in CNTs is very small, thereby solving the problem of dissipated power density that adversely affects silicon circuits. Current densities of more than $10^{10}\,\mathrm{A/cm^2}$ have been reported for the metallic CNTs without any signs of damage even at an elevated temperature of 250°C, thereby eliminating EM reliability concerns that plague Cu interconnects. Since CNTs do not have any leftover bonds, there is no need to grow a film on the surface in order to tie up the free bonds and there is no need to restrict the gate insulator to silicon dioxide. This fact implies the use of other superior materials to insulate the gate terminal in a transistor which can result in a much faster device.

However, the high resistance associated with an isolated CNT (greater than 6.45 KΩ) [] necessitates the use of a *bundle* (rope) of CNTs conducting current in parallel to form an interconnection. A singlewall nanotube results in a very high contact resistance and high characteristic impedance, and hence a bundle of closely packed parallel CNTs is preferably used above a ground plane.

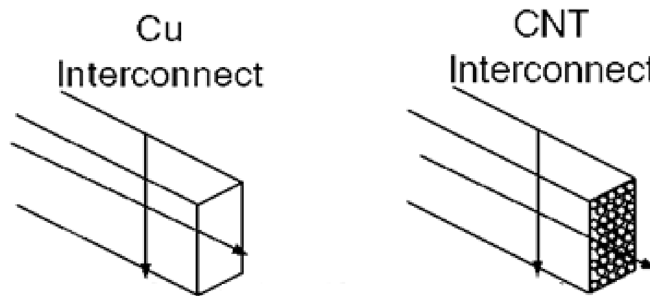

Fig. 3.18: Schematic showing the comparison of a Copper interconnect and a CNT interconnect bundle [33].

Moreover, due to the lack of control on *chirality*, any bundle of CNTs consists of metallic as well as semi-conducting nanotubes (the semi-conducting CNTs do not contribute to current conduction in an interconnect). Furthermore, the observed resistance of a CNT is much higher than the resistance derived due to the presence of imperfect metal-nanotube contacts which give rise to an additional contact resistance. The resistance arising from these imperfect contacts is often so high that it masks the observation of intrinsic transport properties. The observed resistance for CNTs has typically been in the range of 100 KΩ.

The properties of CNTs as well as the advantages of CNTs over Copper Interconnections can be summarized as follows:

3. The carrier transport is 1D, resulting in ballistic transport with no scattering and much less power dissipation. Scattering-free current transport allows high current densities and improved signal delays.

2. All chemical bonds of the carbon atoms are satisfied and there is no need for chemical passivation of free bonds as in silicon.

3. The strong C–C covalent bonding gives the CNTs high mechanical and thermal stability and resistance to electromigration. Current densities as high as 1010 A/cm2 can be sustained in metallic CNTs.

4. The diameter of a CNT is controlled by chemistry, not by fabrication.

5. Both active devices and interconnections can be made of semiconducting and metallic nanotubes.

But the occurrence of imperfect metal-nanotube contacts has the following implications:

- For small lengths (L), especially for L < MFP, the large contact resistance dominates the overall CNT resistance. Resistance is higher than that of a Cu interconnect.
- However, for long interconnect lengths L > MFP (global wires), the impact of imperfect contacts diminishes, because R_c is a constant resistance. Hence long CNT bundle interconnects will have smaller resistance than their Cu counterparts.

3.8.3 RLC circuit model for CNT

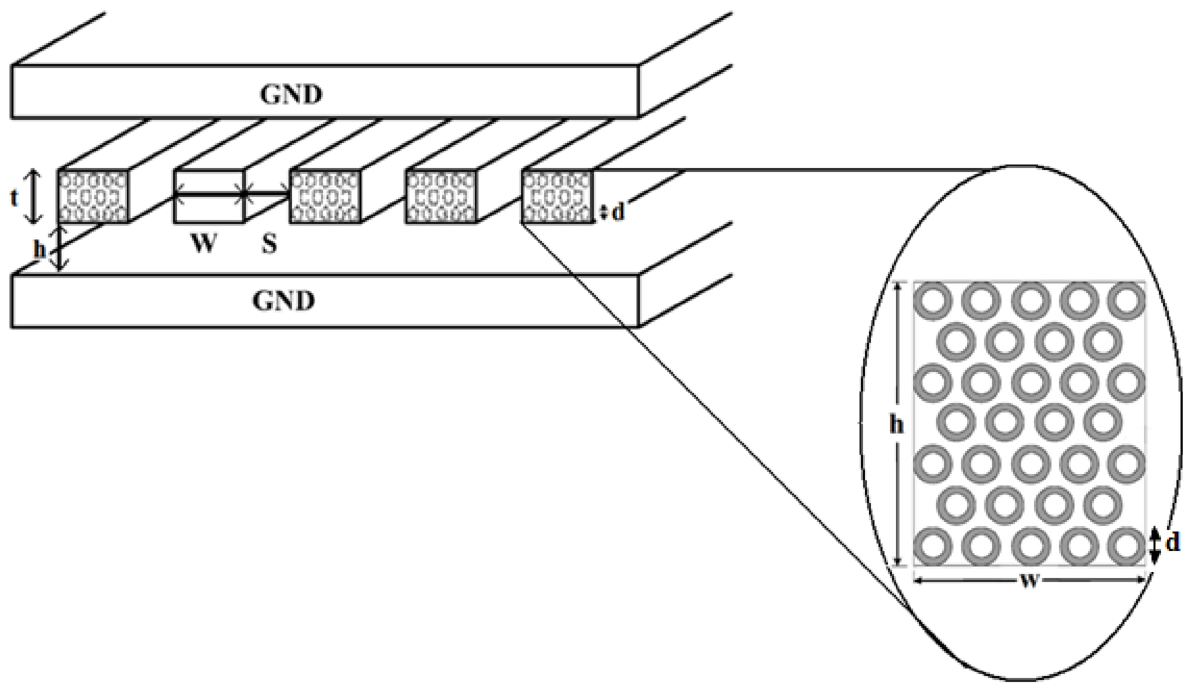

Fig. 3.19: The 2-D structural model of SWCNT bundle interconnect with the inset showing the nanotubes within its bundle

An isolated SWCNT interconnect is equivalent to a tandem of RLC circuits, each comprising a resistance, an inductance and a capacitance as shown in Fig. (3.20). A SWCNT bundle is formed by parallel combination of a large number of such nanotubes Fig. (3.19). Similar RLC equivalent circuits were proposed for SWCNT-bundle interconnects Fig. (3.20 [32]).

P. J. Burke proposed a Luttinger Liquid Theory based equivalent circuit model to obtain expressions for resistances, inductances and capacitances of a bundle. The tube diameter of the SWCNT is d, its thickness is h, the width of CNT bundle is w interconnect and n_{CNT} is the total number of CNT tubes in the bundle Fig. (3.19).

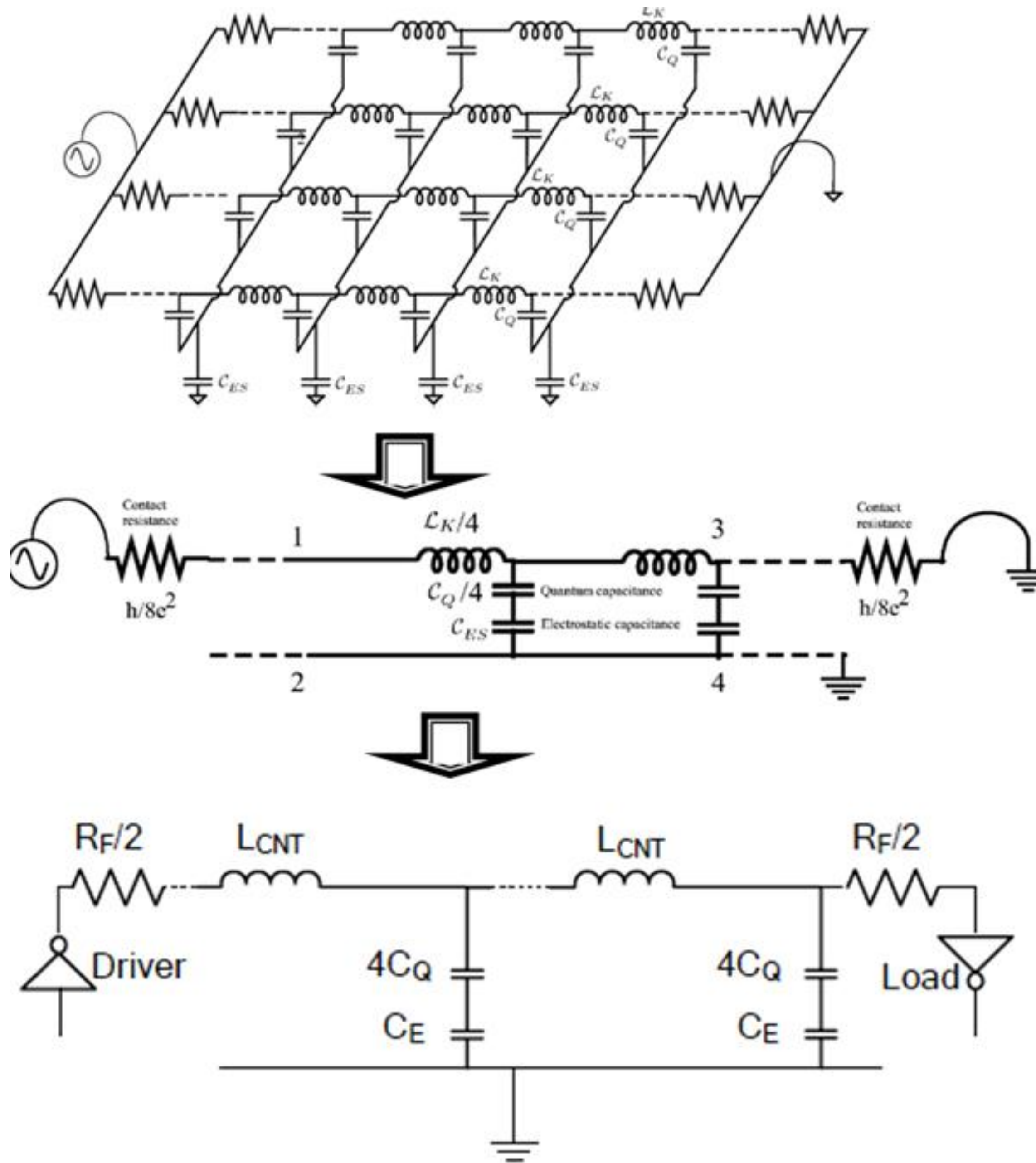

Fig. 3.20 **(a)** Circuit diagram for an SWNT with tandem of RLC circuits, **(b)** *Effective* circuit diagram for a SWNT ([32]), **(c)** equivalent circuit for SWCNT Bundle

Based on this model, the resistance of a CNT bundle of length L is given by Eq. (3.30) where h is Planck's constant, λ_0 is the mean free path of electron in a CNT,

$$R_{bundle} = \frac{R_{isolated}}{n_{CNT}} = \frac{\left[\left(\frac{h}{4e^2}\right)\frac{l}{\lambda_o}\right]}{n_{CNT}} = \frac{\left(\frac{6.45\ k\Omega}{1\mu m}\right)l}{n_{CNT}} \tag{3.30}$$

where, $n_{CNT} = n_w n_H - n_H/2$ if the number of rows in the bundle n_H is even,

otherwise $n_{CNT} = n_w n_H - (n_H - 1)/2$

Here, the number of rows in the bundle is given by

$$n_H = \frac{H - d}{\left(\sqrt{3/2}\right)x} + 1 \tag{3.31}$$

where x is the separation between the centres of two neighbouring tubes. Assuming a parallel structure, $x = d$.

The total effective capacitance of a bundle of SWCNTs is given by.

$$C_{bundle} = \frac{C_{E_{bundle}} \cdot C_{Q_{bundle}}}{C_{E_{bundle}} + C_{Q_{bundle}}} \tag{3.32}$$

where $C_{E_{bundle}}$ and $C_{Q_{bundle}}$ are the total electrostatic capacitance and total quantum capacitance of bundle of SWNT and can be calculated by equations below:

$$C_{E_{bundle}} = 2C_{E_n} + \left(\frac{n_w - 2}{2}\right)C_{E_f} + \frac{3}{5}(n_H - 2)C_{E_n} \tag{3.33}$$

and

$$C_{Q_{bundle}} = \frac{2e^2}{hv_F} \tag{3.34}$$

where,

$$C_{E_n} = \frac{2\pi\varepsilon}{ln\left(\frac{s}{d}\right)} \tag{3.35}$$

and

$$C_{E_f} = \frac{2\pi\varepsilon}{ln\left(\frac{s+w}{d}\right)} \tag{3.36}$$

Here, v_F is the Fermi velocity ($v_F = 8X10^5\ m/s$) and s is the separation between adjacent bundles.

The inductance of CNT bundle is given by the parallel combination of the inductances corresponding to each CNT forming the bundle, as shown below

$$L_{bundle} = \frac{L_m + L_K}{4n_{CNT}} \tag{3.37}$$

L_m and L_K are the magnetic and kinetic inductances. These components of isolated CNT inductance are calculated as:

$$L_m = \frac{\mu_o}{2\pi} \times ln\left(\frac{y}{d}\right) = 2 \times 10^{-7} \times ln\left(\frac{y}{d}\right) \tag{3.38}$$

$$L_K = \frac{h}{2e^2 v_F} \tag{3.39}$$

y being the separation between a CNT tube and ground.

Burke's Luttinger Liquid Theory based equivalent circuit for SWCNT [32] is well accepted and forms the basis for many useful analyses.

3.8.4 Nanotube Vias

The ability to grow nanotubes at specific sites has helped researchers to design CNT vias [35]. Vias are defined as interconnections between wiring layers in chips and are prone to deterioration due to current crowding and electromigration. Carbon nanotubes have been proposed as the alternative for metal plugs to overcome these problems. Ultra-large-scale integrated (ULSI) circuits have problems that originate from stress and electromigration of copper interconnections, particularly the vias.

One proposed solution for this problem is to use CNTs with large migration tolerance as vias. Bundles of CNTs must be used as vias to get enough current for large-scale integrated (LSI) interconnections. Hot-filament chemical vapor phase deposition (HF-CVD) can be used to grow CNT bundles in the via holes. Mechanical polishing with diamond slurry can be done to control the length of the CNT vias after their growth.

[39] suggests that the total resistance of the CNT via is about three orders of magnitude lower than that of a single CNT and that there is no visible degradation of the via current with time.

It is expected that CNT bundle vias will prove to be effective replacements for copper vias for future ULSI interconnections.

Carbon nanotubes have shown great promise for use as interconnections in nanotechnology circuit applications. This is particularly because they can conduct large currents of the order of a $10^6 \mathrm{A/cm^2}$ without any deterioration and without any scattering, thus avoiding the electromigration problems characteristic of metallic interconnections. On the other hand, the reduction in the thickness of conventional metallic (Cu, Al) or polycrystalline interconnections leads to additional scattering at the surfaces and grain boundaries, thereby deteriorating the interconnection resistance.

CHAPTER

4

ANALYTICAL RESULTS

4.1 Interconnect Models

Chapter 3 emphasized the importance of on-chip inductance in the deep submicron VLSI technology, thus implying the necessity to model the interconnects as transmission lines [13]. This means that more accurate RLC transmission line models are becoming necessary in the analysis of VLSI-based interconnect. The RC model can be viewed as a limiting case of the RLC transmission line model where the inductance is considered to be negligible. This case has been thoroughly investigated in [14].

Various techniques have been proposed for the delay analysis of interconnects. These techniques are based on either one of the following.

(1) Simulation through SPICE to calculate 90% delay. Such techniques give the most accurate insight into arbitrary interconnect structures but are computationally expensive. These transient simulation methods of lossy interconnect are presented in Appendix A.

(2) Closed-form analytical formulas.

Faster techniques based on moment computations were proposed [16] in the performance-driven design of clock distribution and global routing topologies. In the following subsections, some of the delay models which were developed for RLC interconnects were described in Chapter 2.

However Elmore delay cannot accurately estimate the delay for interconnect lines whose inductive impedance cannot be neglected [21].This inaccuracy of Elmore delay is not useful to current performance-driven routing methods where frequency is on the rise resulting in the increase in inductive impedance.

Ismail et al. [14] introduced a simple tractable delay formula for RLC trees. They tried to preserve the useful characteristics of the Elmore delay model while maintaining the same accuracy characteristics. This delay model with the closed-form expressions considers all damping conditions of an RLC circuit including the under-damped response, which was not considered by the Elmore delay due to the non-monotonic nature of the response. These solutions are presented for the 50% delay. rise time. overshoots. and settling time of signals in an RLC tree.

But these models present significantly lower accuracy mainly because they are based on simplified assumptions for the transistor operation and use simple load models for the representation of the interconnect lines.

4.2 Driver Interconnect Model (DIL)

Much research effort has been devoted during the last few years to model CMOS gates driving simple capacitive loads, especially CMOS inverter/repeater. The CMOS inverter is the simplest buffer or repeater in VLSI interconnects. Sakurai and Newton (1990 [15]) gave alpha-power MOS model for current voltage characteristics for short channel MOSFETs.

Chatzigeorgiou and Nikolaidis (2001[23]) modeled the propagation delay of RLC interconnect (Cu) using a CMOS driver using the α-power law MOS model. Kaushik, et al. (2007 [24]) presented an analytical method for an inverter driving a π-RLC load.

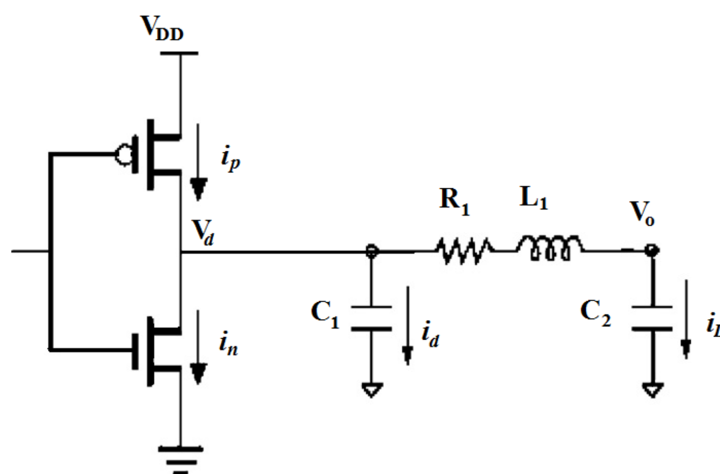

Fig. 4.1 Delay prediction for RLC interconnect (Cu) driven by a CMOS driver

In our work, we used the α-power law MOS model to derive the delay performance of a CMOS inverter which is driving an RLC interconnect load (Fig. 4.1). We have used a π-RLC interconnect model of both copper as well as CNT material in 45nm technology to calculate delay. We considered the case for fast input ramps since our transition time (rise time and fall time) is within 10% of the pulse period.

We showed that this method accurately calculates the delay for both the interconnects with an impressive accuracy of less than 30%.

The CMOS driver characteristics are governed by the Alpha Power law model given in Eq.(4.1) below,

$I_D = 0; \quad V_{GS} \leq V_{T0}$: cutoff region

$I_D = k_1 \, (V_{GS} - V_{T0})^{\alpha/2} . V_{DS}; \quad V_{DS} < V_{DS-sat}$: linear region

$I_D = k_s \, (V_{GS} - V_{T0})^{\alpha} \quad V_{DS} \geq V_{DS-sat}$: saturation region

(4.1)

where V_{GS}, V_{DS} and I_D are the gate-source potential, drain-source potential and the drain current respectively, V_{DS-sat} is the drain saturation voltage, k_1, k_s the transconductance parameters in linear and saturation regions, respectively; α the velocity saturation index and V_{T0} the zero bias threshold voltage.

Applying KCL at drain of nMOS:

$$i_n + i_d + i_L - i_p = 0$$

where i_n, i_p, i_d and i_L are nMOS drain current, pMOS drain current, current through C_1 and C_2 respectively, as shown in Fig. 4.1.

4.2.1 Delay expressions for fast input ramps

Since we have considered the case for fast input ramps, the equations defining time delay period are given below:

Region 1 $(0 < t < t_1)$: During this region, the nMOS transistor is cut off.

$$i_d + i_L = 0 \tag{4.2}$$

where

$$i_d = C_1 \frac{dV_d}{dt} \quad \text{and} \quad i_L = C_2 \frac{dV_0}{dt} \tag{4.3}$$

where V_d is drain-source voltage across nMOS (near-end voltage of the interconnect) and V_0 is output voltage at far end of the interconnect.

Substituting value of $V_d = LC_2 \frac{d^2V_0}{dt^2} + RC_2 \frac{dV_0}{dt} + V_0$, we get: (4.4)

$$C_1 \frac{d}{dt}\left(LC_2 \frac{d^2V_0}{dt^2} + RC_2 \frac{dV_0}{dt} + V_0\right) + C_2 \frac{dV_0}{dt} = 0 \quad (4.5)$$

Solving,

$$a \frac{d^3V_0}{dt^3} + b \frac{d^2V_0}{dt^2} + \frac{dV_0}{dt} = 0 \quad (4.6)$$

where

$$a = \frac{C_1C_2L}{C_1 + C_2} \quad (4.7)$$

$$b = \frac{C_1C_2R}{C_1 + C_2} \quad (4.8)$$

$$t_1 = \frac{V_{T0}}{V_{DD}}\tau \quad (4.9)$$

Here initial conditions are

$$V_0(0) = V_{DD}, \left(\frac{dV_0}{dt}\right)(0) = 0 \quad \text{and} \left(\frac{d^2V_0}{dt^2}\right)(0) = 0 \quad (4.10)$$

Solving the differential equation, we get $V_0 = V_{DD}$ $\quad (0 < t < t_1)$ (4.11)

Region 2 $(t_1 < t < \tau)$: During this region, the nMOS device operates in saturation and

$$V_{in} = \frac{V_{DD}}{\tau} t \quad (4.12)$$

Apply KVL,

$$i_n + i_d + i_L = 0 \quad (4.13)$$

$$C_1 \frac{d}{dt}\left(LC_2 \frac{d^2V_0}{dt^2} + RC_2 \frac{dV_0}{dt} + V_0\right) + C_2 \frac{dV_0}{dt} + k_s(V_{GS} - V_{T0})^{\alpha} = 0$$

(4.14)

Re-arranging, we get

$$a\,\frac{d^3V_0}{dt^3} + b\,\frac{d^2V_0}{dt^2} + \frac{dV_0}{dt} + \frac{K_S}{(C_1 + C_2)}\left(\frac{V_{DD}}{\tau}t - V_{T0}\right)^{\alpha} = 0 \tag{4.15}$$

This equation cannot be solved analytically. To obtain an analytical expression for the output, i_n is approximated by a second-order Taylor series at $t = \tau/2$ (where $V_{in} = V_{DD}/2$) as:

$$\frac{i_n}{(C_1 + C_2)} = A_0 + A_1 t + A_2 t^2 \tag{4.16}$$

Taking the initial conditions $V_0(0) = V_{DD}$, $\left(\frac{dV_0}{dt}\right)(0) = 0$, $\left(\frac{d^2V_0}{dt^2}\right)(0) = 0$ (4.17)

and solving the differential equation, we get

$$V_0(t) = K_1 t^3 + K_2 t^2 + K_3 t - K_4 e^{-(b-M)t/2a} - K_5 e^{-(b+M)t/2a} + C[3] \tag{4.18}$$

where

$$M = \sqrt{b^2 + 4a} \tag{4.19}$$

$$K_1 = -A_2/3 \tag{4.20}$$

$$K_2 = A_2 b - A_1/2 \tag{4.21}$$

$$K_3 = 2aA_2 - 2b^2A_2 - A_0 + bA_1 \tag{4.22}$$

$$K_4 = 2a\ C[2]/b - M \tag{4.23}$$

$$K_5 = 2a\ C[1]/b + M \tag{4.24}$$

C[1], C[2], C[3] are integration constants

Region 3 $(\tau < t < t_2)$: During this region, $V_{in} = V_{DD}$ and the nMOS transistor is still in saturation

$$a\,\frac{d^3V_0}{dt^3} + b\,\frac{d^2V_0}{dt^2} + \frac{dV_0}{dt} + \frac{k_S}{(C_1 + C_2)}(V_{DD} - V_{T0})^{\alpha} = 0 \tag{4.25}$$

or,

$$a\,\frac{d^3V_0}{dt^3} + b\,\frac{d^2V_0}{dt^2} + \frac{dV_0}{dt} + A_3 = 0 \quad (4.26)$$

where

$$k_s = \frac{I_{D0}}{(V_{DD} - V_{TH})^{\alpha}} \quad (4.27)$$

Taking the initial conditions $V_0(0) = V_{DD}$, $\left(\frac{dV_0}{dt}\right)(0) = 0$, $\left(\frac{d^2V_0}{dt^2}\right)(0) = 0$ (4.28)

and solving the differential equation, we get

$$V_0(t) = C[6] - A_3 t - K_6 e^{-(b-M)t/2a} - K_7 e^{-(b+M)t/2a} \quad (4.29)$$

where

$$K_6 = 2a\ C[5]/b - M \quad (4.30)$$

$$K_7 = 2a\ C[4]/b + M \quad (4.31)$$

C[4], C[5], C[6] are integration constants.

Region 4 $(t > t_2)$: During this region, $V_{in} = V_{DD}$ and nMOS transistor operates in linear region.

$$a\,\frac{d^3V_0}{dt^3} + K_8\frac{d^2V_0}{dt^2} + K_9\frac{dV_0}{dt} + K_{10}V_0 = 0 \quad (4.32)$$

where

$$K_8 = \frac{nLC_2}{C_1 + C_2} + b \quad (4.33)$$

$$K_9 = \frac{nRC_2}{C_1 + C_2} + 1 \tag{4.34}$$

$$K_{10} = \frac{n}{C_1 + C_2} \tag{4.35}$$

$$n = k_1(V_{DD} - V_{T0})^{\alpha/2} \tag{4.36}$$

$$k_1 = \frac{I_{D0}}{V_{DD}(V_{DD} - V_{TH})^{\alpha/2}} \tag{4.37}$$

Solving the differential equation, we get

$$V_0(t) = C[7]e^{\left(-1/12(\beta^{2/3} - 12a\,K_9 + 4K_8{}^2 + 4K_8\beta^{1/3} + i\sqrt{3}\beta^{2/3} + i12\sqrt{3}aK_9 - i4\sqrt{3}K_8{}^2)\frac{t}{a\beta^{1/3}}\right)} + C[8]e^{\left(1/12(-\beta^{2/3} + 12a\,K_9 - 4K_8{}^2 - 4K_8\beta^{1/3} + i\sqrt{3}\beta^{2/3} + i12\sqrt{3}aK_9 - i4\sqrt{3}K_8{}^2)\frac{t}{a\beta^{1/3}}\right)} + C[9]e^{\left(-1/6(-\beta^{2/3} + 12a\,K_9 - 4K_8{}^2 + 2K_8\beta^{1/3})\frac{t}{a\beta^{1/3}}\right)} \tag{4.38}$$

where

$$\beta = 36aK_8K_9 - 108a^2K_{10} - 8K^3{}_8 + 12a(12aK^3{}_9 - 3K^2{}_8K^2{}_9 - 54aK_8K_9K_{10} + 81a^2K^2{}_{10} + 12K^3{}_8K_{10})^{1/2} \tag{4.39}$$

C[7], C[8], C[9] are integration constants.

4.2.2 Analytical Delay prediction for Copper interconnect

The total input time of ramp(t_{rise}) is 2ns. The total time of output t_{fall} is 2.2ns.

The copper interconnect parasitics were calculated by Shyh-Chyi Wong's TSM model [31] which is described in Appendix A. Using this model interconnect resistance *R*, capacitance *C* and inductance *L* were calculated for a wire of length 1mm (global).

The following parameters were used in the calculation-

	Copper	CNT
technology	45 nm	45 nm
V_{DD}	1V	1V
length (L) of interconnect	1000 um (global)	1000 um (global)

width (w) of interconnect	102.5 nm	102.5 nm
spacing (s) between interconnects	102.5 nm	102.5 nm
thickness (h) of global interconnect	235.75 nm	235.75 nm
resistivity (relative)	2.45 Ω-cm	-
oxide thickness (t_{OX})	215.25 nm	215.25 nm
ε_{OX} (relative)	2.45	2.45
Load capacitance	50fF	50fF
$(W/L)_{driver}$	110	110
$V_{TO_{(N-MOSFET)}}$	0.3558V	0.3558V
velocity saturation index (α)	1	1
drain saturation current, I_{D0}	1.91 mA	1.91 mA
drain saturation voltage V_{D0}	0.6442 V	0.6442 V

Region 1 (t = 0 to 0.7116ns)

$$V_0(t) = V_{DD} = 1 \tag{4.40}$$

Region 2 (t = 0.7116ns to 1ns)

$$V_0(t) = (0.0666)e^{-1.1039*10^{10}*t} - (1.7986*10^{-5})e^{-6.0135*10^{11}*t} - (8.09*10^{17})t^2 + (7.2495*10^8)t + 0.8438 \tag{4.41}$$

Region 3 (t = 1ns to 1.2ns)

$$V_0(t) = -(0.1069)*e^{-1.1039*10^{10}*t} + (3.6015*10^{-5})e^{-6.0135*10^{11}*t} - (1.1581*10^9)t + 1.9565 \tag{4.42}$$

Region 4 (t = 1.2ns to 2ns)

$$V_0(t) = -(2.33)*e^{(-3.0551*10^{10} - 7.3922*10^{-4}i)*t} + (0.0055*10^{-4})e^{(-5.9829*10^{11} - 5.3158*10^{-5}i)*t} + (22.3240)e^{(-3.0406*10^9 - 7.1908*10^{-4}i)*t} \tag{4.43}$$

Plotting $V_0(t)$ against time for different regions, we get the analytical waveform for output voltage. This is given in Fig. 4.2.

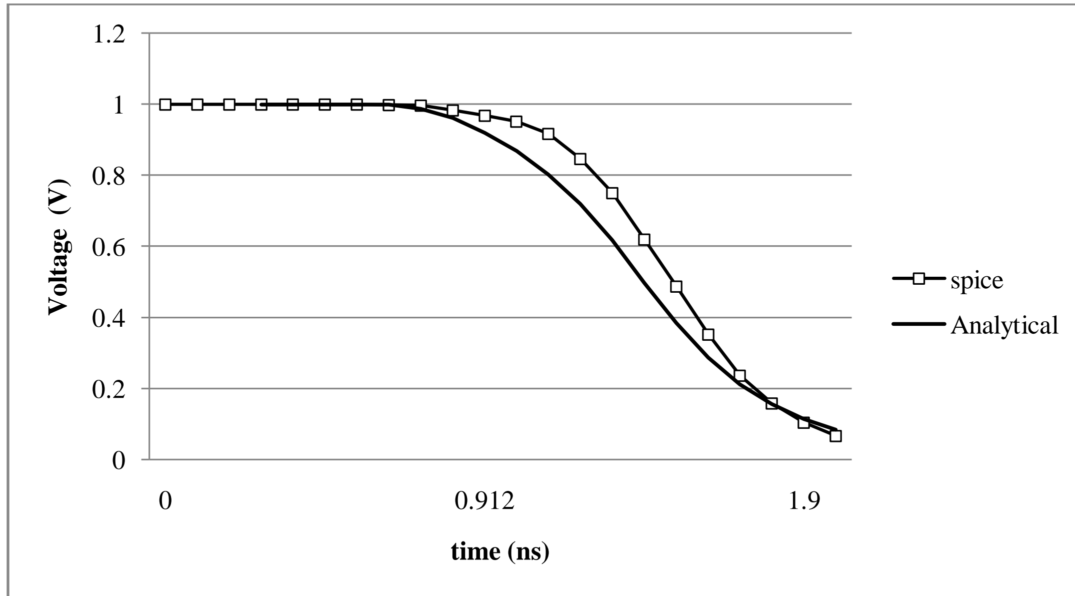

Fig. 4.2 Analytical v/s SPICE delay for Cu interconnect (α-power law)

The SPICE simulated waveform using a PTM 54 model is also shown in Fig. 4.2 for comparison. The difference in analytical and SPICE simulated data is shown in Table 4.1. The table shows that the maximum percentage error in analytical waveform is 32.23% while the average error is 10.04%.

Table 4.1: Comparison of Analytical (α-power law) and SPICE delay for Cu interconnect

time (ns)	SPICE	Analytical	Percentage error (%)
0	1	0.9996	-0.04
0.1	1	0.9996	-0.04
0.2	1	0.9996	-0.04
0.3	1	0.9996	-0.04
0.4	1	0.999	-0.1
0.5	1	0.999	-0.1
0.6	1	0.999	-0.1
0.7	1	0.998	-0.2

0.7116	0.95	0.997	4.7
0.8116	0.8993	0.983	8.37
0.9116	0.8323	0.968	13.57
1	0.7984	0.951	15.26
1.1	0.6826	0.917	23.44
1.2	0.5668	0.846	27.92
1.3	0.4287	0.751	32.23
1.4	0.3163	0.619	30.27
1.5	0.2334	0.487	25.36
1.6	0.1722	0.353	18.08
1.7	0.127	0.236	10.9
1.8	0.0937	0.158	6.43
1.9	0.0692	0.104	3.48
2	0.051	0.067	1.6

4.2.3 Analytical Delay prediction for CNT bundle

The total input time of ramp, t_{rise} is 2ns. The total time of output t_{fall} is 3.4 ns.

The copper interconnect parasitics were calculated using Burke's Luttinger Liquid Theory [32] which is described in Chapter 3. Using this model interconnect resistance *R*, capacitance *C* and inductance *L* were calculated for a wire of length 1mm (global).

The parameters used for calculation are already showed in 4.2.2.

After solving for $V_0(t)$, the following equations were obtained:

Region 1 (t = 0 to 0.7116ns)

$$V_0(t) = V_{DD} = 1 \tag{4.44}$$

Region 2 (t = 0.7116ns to 1ns)

$$V_0(t) = (0.0338)e^{-1.8608*10^{10}*t} - (3.3102*10^{-13})e^{-5.5436*10^{15}*t} - (7.6825*10^{17})t^2 + (6.2925*10^{8})t + 0.9412 \tag{4.45}$$

Region 3 (t = 1ns to 1.2ns)

$$V_0(t) = -(0.0431) * e^{-1.1039*10^{10}*t} + (1.4519 * 10^{-5})e^{-6.0135*10^{11}*t} - (4.6691 * 10^{8})t + 1.2614 \tag{4.46}$$

Region 4 (t = 1.2ns to 2ns)

$$V_0(t) = -(0.4358) * e^{(-2.0836*10^{10}+17.379i)*t} - \left(10^{-9} * (1.3001 + 2.1856i)\right)e^{(-5.5436*10^{15}-0.51466i)*t} + (5.3550)e^{(-1.6953*10^{9}-17.383i)*t} \tag{4.47}$$

Plotting $V_0(t)$ against time for different regions, we get the analytical waveform for output voltage. This is given in Fig. 4.3.

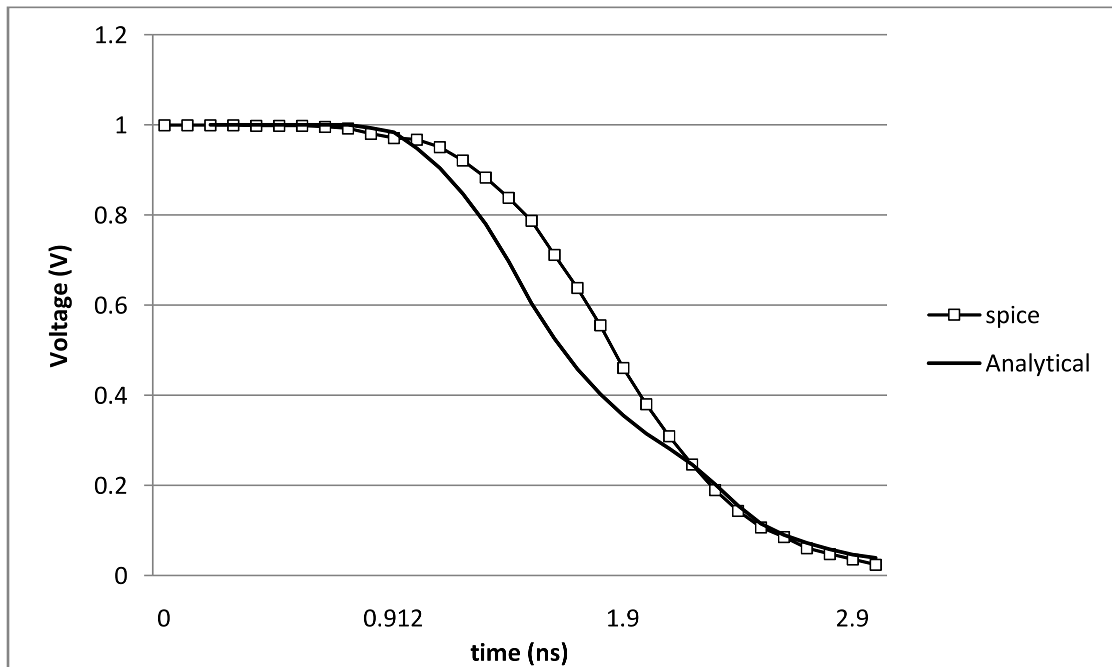

Fig. 4.3 Analytical v/s SPICE delay for CNT bundle interconnect (α-power law)

The SPICE simulated waveform using a PTM 54 model is also shown in Fig. 4.3 for comparison. The difference in analytical and SPICE simulated data is shown in Table 4.2. The table shows that the maximum percentage error in analytical waveform is 26.69% while the average error is 6.63%.

Table 4.2: Comparison of Analytical (α-power law) and SPICE delay for CNT bundle interconnect

time (ns)	SPICE	Analytical	Percentage error (%)
0	0.9996	1	-0.04
0.1	0.9996	1	-0.04
0.2	0.9996	1	-0.04
0.3	0.9996	1	-0.04
0.4	0.999	1	-0.1
0.5	0.999	1	-0.1
0.6	0.998	1	-0.2
0.7	0.996	1	-0.4
0.712	0.993	0.9999	-0.69
0.812	0.981	0.98	0.1
0.912	0.971	0.97	0.1
1	0.968	0.8945	7.35
1.1	0.951	0.8478	10.32
1.2	0.922	0.8002	12.18
1.3	0.883	0.6911	19.19
1.4	0.839	0.5989	24.01
1.5	0.788	0.5211	26.69
1.6	0.712	0.4554	25.66
1.7	0.639	0.4	23.9
1.8	0.556	0.3532	20.28
1.9	0.461	0.3137	14.73
2	0.38	0.2804	9.96
2.1	0.309	0.2523	5.67

2.2	0.246	0.2085	3.75
2.3	0.19	0.1485	4.15
2.4	0.144	0.1096	3.44
2.5	0.107	0.0873	1.97
2.6	0.085	0.0752	0.98
2.7	0.061	0.0551	0.59
2.8	0.048	0.0465	0.15
2.9	0.036	0.0392	-0.32
3	0.024	0.0331	-0.91

4.3 Modified Nodal Analysis and Moment Matching

To accurately model the interconnect's electrical characteristics, a parasitic circuit with tens of RLC segments has to be used. We use the s domain and time domain analysis to calculate the delay of an interconnect with several RLC segments. For this, we use a circuit reduction technique known as **moment-matching reduction via Padé approximation**.

4.3.1 Approximation of CMOS Inverter Delay

The first step is to estimate the on-resistance, input capacitance and load capacitance of a CMOS inverter. Since the CMOS inverter is the preferred repeater circuit, its delay estimation is of utmost importance. On the other hand, as there may be several repeaters in a circuit their exact analysis is cumbersome and lengthens the RLC delay analysis. In SPICE, the CMOS circuits are generally found to conduct in a state where either the N-MOSFET or the P-MOSFET is in saturation. Using this general assumption, a rough approximation of CMOS resistance and capacitance was made. The inverter was in turn replaced by a *RC* circuit, as shown below.

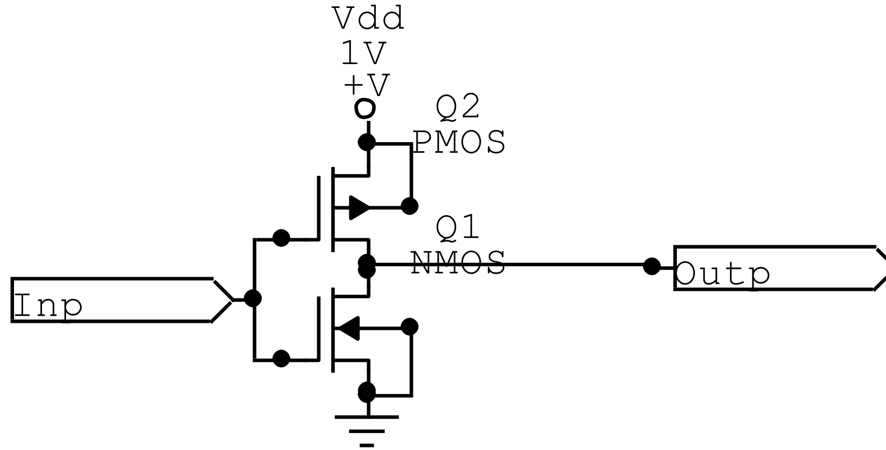

Fig. 4.4 Schematic of a CMOS inverter

The CMOS inverter capacitance, C_L is calculated as :

$$C_L = C_{DB_n} + C_{GD_n} + C_{DB_p} + C_{GD_p} \quad (4.48)$$

where- $$C_{DB} = C_{SB} = WEC_j + 2(W + E)C_{jsw} = (AD)C_j + 2(PD)C_{jsw} \quad (4.49)$$

and, $$C_{GD} = C_{GS} \approx \frac{1}{2}(WLC_{OX}) + WC_{ov} \text{ in linear} \quad (4.50)$$

or, $$C_{GD} \approx C_{ov}W \quad \text{in saturation} \quad (4.51)$$

Also, the input capacitance is given by $C_{in} = C_{GS}$ (4.52)

where- $$C_{GS} = C_{GD} \approx \frac{1}{2}(WLC_{OX}) + WC_{ov} \quad \text{in linear} \quad (4.53)$$

or, $$C_{GS} = \frac{2}{3}(WL_{eff}C_{OX}) + WC_{ov} \quad \text{in saturation} \quad (4.53)$$

The net capacitance of inverter is given by,

$$C_{total} = (C_{in} + C_L) \quad (4.54)$$

For the CMOS inverter in 45nm technology with repeater driver transistor (N-MOSFET) size $(W/L)_{driver}$= 400) of 30, the capacitance, C_{total} was calculated as in eq. (4.55).

$$C_{DBn} = 3.6e * 10-16$$
$$C_{GD_n} = 4.05 * 10^{-17}$$
$$\rightarrow C_{L_n} = 4.005 * 10^{-16}$$

$$C_{DB_p} = 7.75 * 10^{-16}$$
$$C_{GD_p} = 9.215 * 10^{-16}$$
$$\rightarrow C_{L_p} = 9.215 * 10^{-16}$$

$$C_{L_n},\ C_{L_p} \rightarrow C_L = 2.1 * 10^{-15}$$

$$C_{GS_n} = 6.623e * 10^{-16}$$
$$C_{GS_p} = 1.9376 * 10^{-15}$$
$$\rightarrow C_{in} = C_{GS} = 2.6 * 10^{-15}$$

$$C_L,\ C_{in} \rightarrow C_{total} = 4.6e * 10^{-15}$$

(4.55)

At the end, the C_{total} was found to be 4.6 femto-farads.

The CMOS inverter resistance is calculated as

$$R_{in} = \frac{L/W}{\mu C_{OX} V_{DD}} \tag{4.56}$$

For N-MOSFET, the resistance is R_{in_n} ; and for P-MOSFET the resistance is R_{in_p}

$$R_{in_n} = 9.1198\ k\Omega$$
$$R_{in_p} = 24.3\ k\Omega$$
$$\rightarrow R_{in} = R_{in_n} \parallel R_{in_p} = 6.631\ k\Omega$$

(4.57)

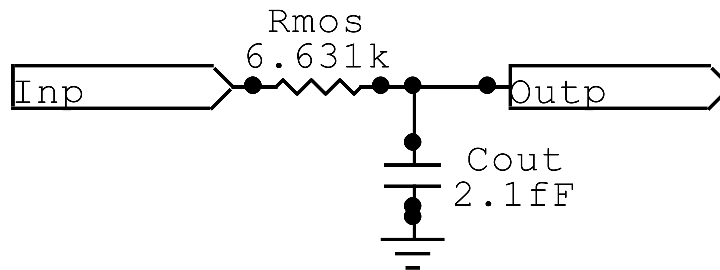

Fig. 4.5 RC equivalent of the CMOS inverter

In the end the approximate delay of CMOS is calculated as [42]:

$$\tau_{inv} = 0.69 R_{in} C_L \tag{4.58}$$

Using, this τ_{inv} was found to be 11.316ns. The SPICE Simulation Results show this to be 9.59 ns as shown in Fig. 4.5 and Fig. 4.6.

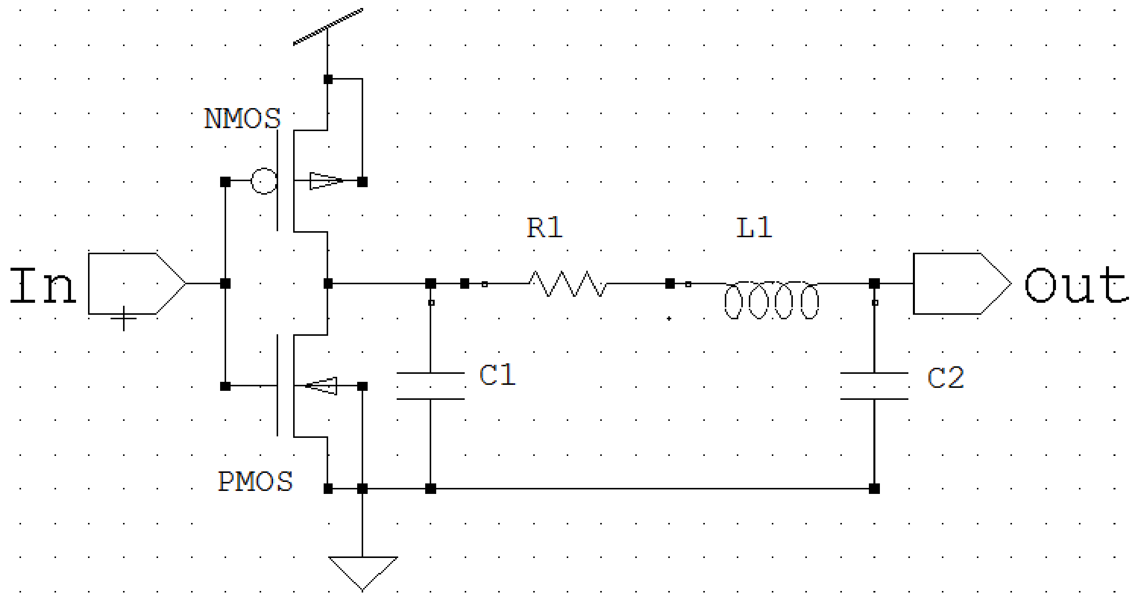

Fig. 4.6 Schematic of a CMOS inverter in S-Edit of Tanner EDA

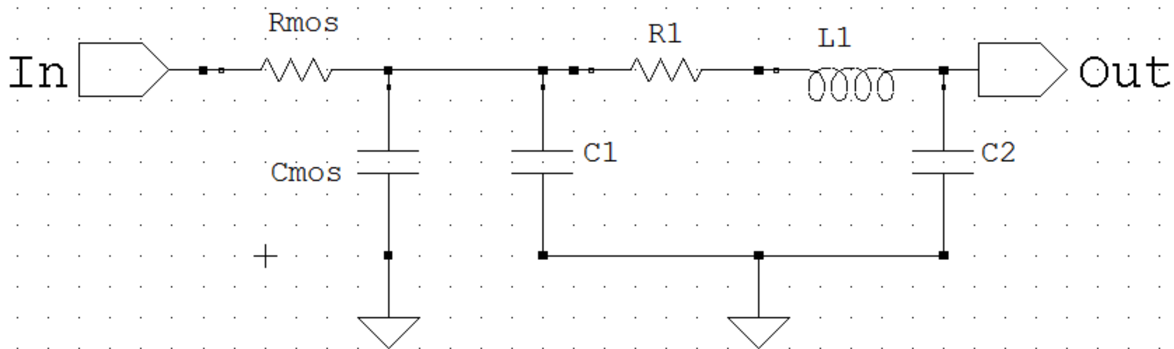

Fig. 4.7 RC equivalent of the CMOS inverter in Tanner EDA

4.3.2 Formulation of the Circuit Equations

The first step is to RLC circuits with a certain general structure. In SPICE, the circuits are represented by a system of ordinary differential equations. These equations are then solved using several different numerical techniques. The equations are constructed using Kirchoff's voltage and current laws. The first system of equations pertains to the currents flowing into each node.

One equation is written for each node in the circuit (except for the ground node), so the following equation is really a system of N equations for the N nodes in the circuit.

Modified Nodal Analysis [12]

Normal nodal analysis that uses only Kirchoff s current law, cannot be used to represent ideal voltage sources or inductors. This is so because the branch current in these elements cannot be expressed as a function of the branch voltage. To resolve this problem, Ruehli et al. [12] suggested a technique known as Modified Nodal Analysis (MNA) where KVL is used to write a loop equation around each inductor or voltage source.

The use of modified nodal analysis does have the disadvantage of requiring that an additional equation be included for each inductor or voltage source, but has the advantage that ideal voltage sources can be used. The total number of equations to be solved is therefore the number of nodes plus the number of voltages sources and inductors.

In this scenario, a transfer function of the linear network was obtained from the MNA formulation in s-domain. The analytical model for delay of an interconnect with 2 RLC-segments is summarized below and calculations from this analytical expression are compared with those from PTM level 54 models [46] for verification.

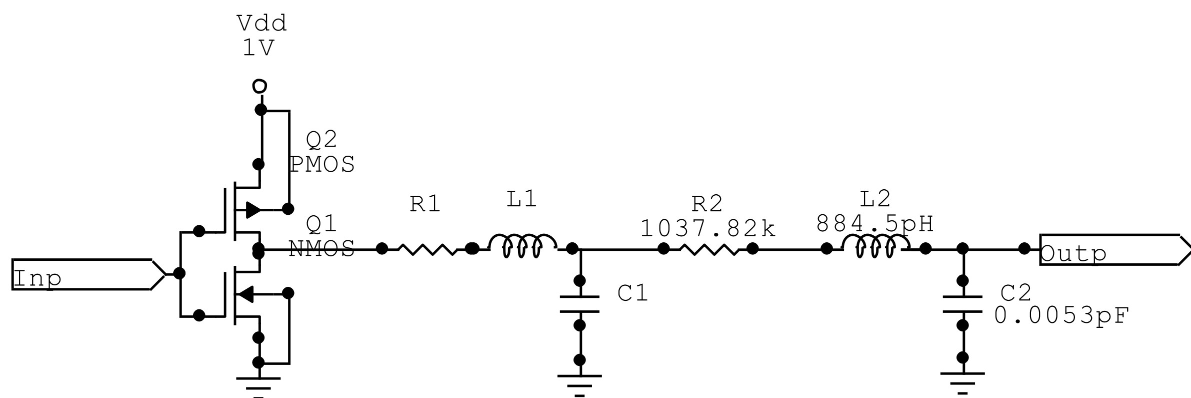

Fig. 4.8 Schematic of a 2 segment RLC-interconnect with CMOS inverter driver

Subsequently the driver (CMOS inverter) was replaced with an equivalent RC circuit obtained from Section 4.2.1. This is shown in Fig. 4.9.

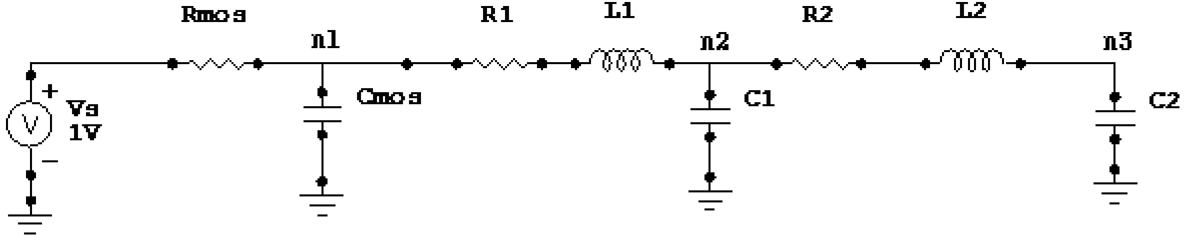

Fig. 4.9 Schematic of a 2 segments RLC-interconnect with RC-equivalent driver

Using Modified Nodal Analysis (MNA) the following matrix was formed:

$$\begin{bmatrix} C_{mos} & & & 0 & 0 \\ & C_1 & & 0 & 0 \\ & & C_2 & 0 & 0 \\ 0 & 0 & 0 & L_1 & \\ 0 & 0 & 0 & & L_1 \end{bmatrix} \begin{bmatrix} \dot{v}_1 \\ \dot{v}_2 \\ \dot{v}_3 \\ \dot{i}_1 \\ \dot{i}_2 \end{bmatrix} = - \begin{bmatrix} G_{mos} & 0 & 0 & 1 & 0 \\ 0 & 0 & 0 & -1 & 1 \\ 0 & 0 & 0 & 0 & -1 \\ -1 & 1 & 0 & R_1 & 0 \\ 0 & -1 & 1 & 0 & R_2 \end{bmatrix} \begin{bmatrix} v_1 \\ v_2 \\ v_3 \\ i_1 \\ i_2 \end{bmatrix} + \begin{bmatrix} G_{mos}\, v_s \\ 0 \\ 0 \\ 0 \\ 0 \end{bmatrix}$$

(4.59)

which corresponds to this equation-

$$\mathbf{M} \cdot \dot{\mathbf{x}}(t) = -\mathbf{G} \cdot \mathbf{x}(t) + \mathbf{P} \cdot \mathbf{u}(t) \tag{4.60}$$

where

$$\mathbf{M} = \begin{bmatrix} \mathbf{C} & 0 \\ 0 & \mathbf{L} \end{bmatrix}, \ \mathbf{x}(t) = \begin{bmatrix} \mathbf{v_c}(t) \\ \mathbf{i_L}(t) \end{bmatrix} \text{ and } \mathbf{G} = \begin{bmatrix} \mathbf{Y} & \mathbf{E} \\ -\mathbf{E}^T & \mathbf{R} \end{bmatrix} \tag{4.61}$$

The output is $v_3 = V_{0utp}$ which is given by-

$$V_{0utp} = \begin{bmatrix} 0 & 0 & 1 & 0 & 0 \end{bmatrix} \begin{bmatrix} v_1 \\ v_2 \\ v_3 \\ i_1 \\ i_2 \end{bmatrix} \tag{4.62}$$

which corresponds to this equation- $\mathbf{y}(t) = \mathbf{Q} \cdot \mathbf{x}(t)$ (4.63)

Using Laplace transform to represent the equations in s-Domain

$$s\mathbf{Mx}(s) - \mathbf{mx}_0 = -\mathbf{Gx}(s) + \mathbf{Pu}(s) \tag{4.64}$$

$$\mathbf{y}(s) = \mathbf{Qx}(s) \tag{4.65}$$

Assuming initial conditions $\mathbf{x}_0 = 0$, and multiplying both sides of the equations by $\mathbf{G}^{-1}$ eq. (4.66) is obtained-

$$s\mathbf{G}^{-1}\,\mathbf{Mx}(s) = -\mathbf{x}(s) + \mathbf{G}^{-1}\,\mathbf{Pu}(s) \tag{4.66}$$

Denoting $\mathbf{A} \equiv \mathbf{G}^{-1}\mathbf{M}$ (4.67)

and $\mathbf{B} \equiv \mathbf{G}^{-1}\,\mathbf{P}$, (4.68)

eq. (4.68) becomes –

$$s\mathbf{A}\mathbf{x}(s) = -\mathbf{x}(s) + \mathbf{B}\mathbf{u}(s) \quad (4.69)$$

Solve for $\mathbf{x}(s)$-

$$\mathbf{x}(s) = (1 + s\mathbf{A})^{-1}\mathbf{B}\mathbf{u}(s) \quad (4.70)$$

The output $\mathbf{y}(s)$is found as- $\mathbf{y}(s) = \mathbf{Q}\mathbf{x}(s) = \mathbf{Q}(\mathbf{1} + s\mathbf{A})^{-1}\mathbf{B}\mathbf{u}(s)$

Finally, the transfer function $\mathbf{H}(s)$ is found as-

$$\mathbf{H}(s) = \frac{\mathbf{y}(s)}{\mathbf{u}(s)} = \mathbf{Q}(\mathbf{1} + s\mathbf{A})^{-1}\mathbf{B} \quad (4.71)$$

4.3.3 Matrix Approximation (PVL and Arnoldi approximation) [47]

In eq. 4.71 there is a need to invert$(\mathbf{1} + s\mathbf{A})$. However this term contains a variable *s*. Performing the inversion on such a matrix is complicated (There are 3 methods but they are much too involved). Furthermore, the complexity increases as the matrix dimension increases.

Reduction of the matrix $(\mathbf{1} + s\mathbf{A})$ is done by multiplication of two matrices $\mathbf{W}_{n,q}$ and $\mathbf{X}_{n,q}$ from the left and right respectively. Here, *n* is the dimension of $\mathbf{x}(s)$ and *q* is the dimension of the reduced matrix. The matrices $\mathbf{X}_{n,q}$ and $\mathbf{W}_{n,q}$ are chosen such that they are bi-orthogonal, i.e., $\mathbf{W}_{n,q}^T\mathbf{X}_{n,q} = \mathbf{1}_{q,q}$. (4.72)

Construction of $\mathbf{X}_{n,q}$

Since $(\mathbf{1} + s\mathbf{A})^{-1}$ needs to be multiplied by $\mathbf{B}$ on the right, $\mathbf{X}_{n,q}$ is constructed using the columns spanned by Krylov space-

$$[\mathbf{B} \quad \mathbf{AB} \quad \mathbf{A^2B} \quad \ldots \quad \mathbf{A}^{q/u}\,\mathbf{B}] \quad (4.73)$$

If matrix **B** has *u* columns, we expand Krylov space into *q/u* powers of **A** , where *u* is the dimension of the input $\mathbf{u}(s)$.

Construction of $\mathbf{W}_{n,q}$

1. Pade approximation via Lanczos (PVL) - Since $(\mathbf{1}+s\mathbf{A})^{-1}$ needs to be multiplied by $\mathbf{Q}$ on the left, PVL process constructs $\mathbf{W}_{n,q}$ using the columns spanned by Krylov space

$$[\mathbf{Q} \quad \mathbf{A}^T\mathbf{Q} \quad (\mathbf{A}^T)^2\mathbf{Q} \quad \ldots \quad (\mathbf{A}^T)^{q/y}\mathbf{Q}]. \tag{4.74}$$

If matrix $\mathbf{Q}$ has *y* columns, we expand Krylov space into *q/y* powers of $\mathbf{Q}$, where *y* is the dimension of the output $\mathbf{y}(s)$.This algorithm utilizes the input and output. Therefore, the precision is very good. However, the matrix transformation is not symmetric , i.e., $\mathbf{W}_{n,q} \neq \mathbf{X}_{n,q}$. So the transformation may lead to some positive poles in the reduced transfer function and reduce its stability.

2. Arnoldi approximation- $\mathbf{W}_{n,q}$ is set to be equal to $\mathbf{X}_{n,q}$. The matrix will be bi-orthogonal, i.e., $\mathbf{W}_{n,q}^T\mathbf{X}_{n,q} = \boldsymbol{X}_{n,q}^T\boldsymbol{X}_{n,q} = \mathbf{1}_{q,q}$ and the output will be stable.

However the Arnoldi approximation will be less accurate than PVL approximation since the output structure is ignored.

The **reduced transfer function** is formed and substituted in eq. 4.71.

The equation $s\mathbf{A}\mathbf{x}(s) = -\mathbf{x}(s) + \mathbf{B}\mathbf{u}(s)$ becomes-

$$s\mathbf{A}_{q,q}\mathbf{z}_q = -\mathbf{z}_q + \mathbf{B}_{q,u}\mathbf{u}(s) \tag{4.75}$$

where

$$\mathbf{x}_n(s) = \mathbf{X}_{n,q}\mathbf{z}_q(s) \tag{4.76}$$

$$\mathbf{A}_{q,q} \equiv \mathbf{W}_{n,q}^T\mathbf{A}\mathbf{X}_{n,q} \tag{4.77}$$

$$\mathbf{B}_{q,u} \equiv \mathbf{W}_{\boldsymbol{n},\boldsymbol{q}}^{\boldsymbol{T}}\mathbf{B} \tag{4.78}$$

$$\mathbf{Q}_{y,q} \equiv \mathbf{Q}\mathbf{X}_{n,q} \tag{4.79}$$

and *u* is the dimension of the input $\mathbf{u}(s)$ and *y* is the dimension of the output $\mathbf{y}(s)$.

Consequently, the reduced transfer function is expressed by-

$$\mathbf{H}(s) = \mathbf{Q}_{y,q}\left(\mathbf{1}_{q,q} + s\mathbf{A}_{q,q}\right)^{-1}\mathbf{B}_{q,u} \tag{4.80}$$

4.3.4 Analysis using Moment Matching

Maclaurin expansion of the transfer function (Taylor's expansion around *s*=0)

$$H(s) = H_0 + s\frac{dH}{ds}_{|s=0} + \frac{s^2}{2!}\frac{d^2H}{ds^2}_{|s=0} + \cdots \tag{4.81}$$

The coefficients of this expansion are known as central **moments** $m^{(j)}$ defined as

$$m^{(j)} = \frac{1}{j!}\frac{d^j H}{ds^j}\Big|_{s=0} \tag{4.82}$$

$$\therefore\ H(s) = m^{(0)} + sm^{(1)} + s^2 m^{(2)} + \cdots = \sum_{j=0}^{\infty} s^j m^{(j)} \tag{4.83}$$

Characteristics of moments w.r.t output waveform

$$H(s) = \int_0^{\infty} H(t)e^{-st}dt = \int_0^{\infty} H(t)\left[1 - st + \frac{s^2}{2!}t^2 + \frac{s^3}{3!}t^3 + \cdots\right]dt$$
$$= \sum_{j=0}^{\infty} s^j \frac{(-1)^j}{j!}\int_0^{\infty} t^j H(t)dt \tag{4.84}$$

Comparing the above two equations, we get that moment $m^{(j)}$ is integration of $H(t)$ with t^j in time t.

$$m^{(j)} = \frac{(-1)^j}{j!}\int_0^{\infty} t^j H(t)dt \tag{4.85}$$

Focusing on moment $m^{(1)}$

$$-m^{(1)} = \int_0^{\infty} t\frac{dy(t)}{dx}dt \tag{4.86}$$

This is the voltage-time area of step input response between output curve $y(t)$ and vertical voltage axis. If $y(t)$ is a step function, then this voltage-time area is equal to its **delay**. In case of a ramp function, the voltage-time area is also equal to the signal delay.

4.3.5 Calculation

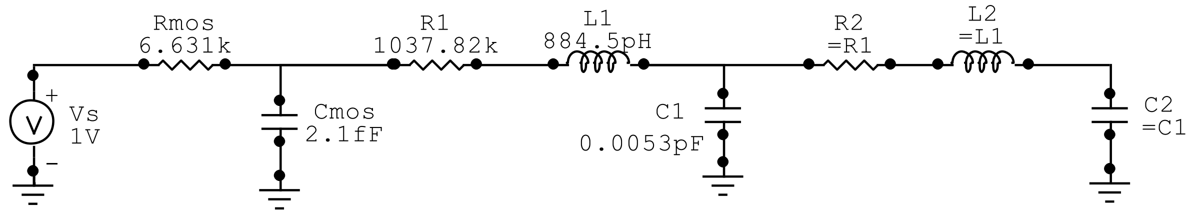

Fig. 4.10 Schematic of a 2 segments RLC-interconnect with copper R, L, C values

As in the previous case, copper interconnect parasitics were calculated by Shyh-Chyi Wong's TSM model [31] which is described in Appendix A. Using this model, interconnect resistance *R*, capacitance *C* and inductance *L* were calculated for a 2-segment wire of length 1mm (global).

The parasitic resistance was found to be 1037.82 Ω, interconnect capacitances C_1 and C_2 is 0.0053 pF, and the interconnect inductance was found to be 884.5pH. The driver (CMOS inverter) was replaced with an equivalent RC circuit of resistance 6.631k Ω and capacitance 2.1 fF.

Putting values in the circuit shown in Fig. 4.10, the following matrices 4.87 to 4.90 were found-

$$\mathbf{M} = \begin{bmatrix} 2.1e-15 & & & & \\ & 5.3e-15 & & & \\ & & 5.3e-15 & & \\ & & & 8.84e-10 & \\ & & & & 8.84e-10 \end{bmatrix} \tag{4.87}$$

$$\mathbf{G} = \begin{bmatrix} 1.5e-4 & 0 & 0 & 1 & 0 \\ 0 & 0 & 0 & -1 & 1 \\ 0 & 0 & 0 & 0 & -1 \\ -1 & 1 & 0 & 1.03e6 & 0 \\ 0 & -1 & 1 & 0 & 1.03e6 \end{bmatrix} \tag{4.88}$$

$$\mathbf{P} \cdot \mathbf{u}(\mathrm{t}) = \begin{bmatrix} 1.5e-4 \cdot \mathrm{v_s} \\ 0 \\ 0 \\ 0 \\ 0 \end{bmatrix} \tag{4.89}$$

$$\mathbf{Q} = [0 \quad 0 \quad 1 \quad 0 \quad 0] \tag{4.90}$$

Solving for $\mathbf{A}$, we get-

$$\mathbf{A} \equiv \mathbf{G}^{-1}\,\mathbf{P} = \begin{bmatrix} 1.39e-11 & 3.5e-11 & 3.5e-11 & -2.7e-26 & -2.7e-26 \\ 1.39e-11 & 5.5e-9 & 5.5e-9 & 8.84e-10 & -2.7e-26 \\ 1.39e-11 & 5.5e-9 & 1.1e-8 & 8.84e-10 & 8.84e-10 \\ 0 & -5.3e-15 & -5.3e-15 & 0 & 0 \\ 0 & 0 & -5.3e-15 & 0 & 0 \end{bmatrix} \tag{4.91}$$

$$\mathbf{B} \equiv \mathbf{G}^{-1}\,\mathbf{P} = \begin{bmatrix} 1 \\ 1 \\ 1 \\ 0 \\ 0 \end{bmatrix} \tag{4.92}$$

Reducing the transfer function from dimension 5 to dimension 1

$$\mathbf{X}_{5,1} = [\mathbf{B}] = \begin{bmatrix} 1 \\ 1 \\ 1 \\ 0 \\ 0 \end{bmatrix} \tag{4.93}$$

Using PVL approximation, $\mathbf{W}_{5,1} = [\mathbf{Q}]^T = \begin{bmatrix} 0 \\ 0 \\ 1 \\ 0 \\ 0 \end{bmatrix}$ (4.94)

$$\mathbf{A}_{1,1} = \mathbf{W}_{5,1}^T\mathbf{A}\mathbf{X}_{5,1} = 1.6562e-008 \tag{4.95}$$

$$\mathbf{B}_{1,1} = \mathbf{W}_{5,1}^T\mathbf{B} = 1 \tag{4.96}$$

$$\mathbf{Q}_{1,1} = \mathbf{Q}\mathbf{X}_{5,1} = 1 \tag{4.97}$$

$$\therefore \mathbf{H}(s) = \mathbf{Q}_{1,1}\left(\mathbf{1}_{1,1} + s\mathbf{A}_{1,1}\right)^{-1}\mathbf{B}_{1,1} = \frac{1}{1 + (1.65e-8)s} \tag{4.98}$$

Analysis using Moment Matching

Obtaining the Maclaurin expansion of $\mathbf{H}(s)$ upto 3 terms, eq.(4.99) is obtained

$$\mathbf{H}(s) = 1 - (1.656\ \times 10^{-8})s + (2.743 \times 10^{-16})s^2 \tag{4.99}$$

The first moment $-m^{(1)} = 1.656\ \times 10^{-8}$seconds

Thus using MNA, the time delay was found to be 16.56 ns. The SPICE Simulation Results show this to be 13.59 ns, resulting in an error of 21.86 %.

4.4 Unified Time Delay Model

Meindl et al. [8-11] presented novel compact expressions for: (1) the time delay for distributed RLC lines and (2) the time delay for *repeater-inserted* distributed RLC lines. They are simplified expressions that enable physical insight and estimation of transient response, time delay, and overshoot for high-speed global interconnects with the inclusion of inductance. But the model is technology dependent. These expressions were rigorously high-speed interconnect of 180nm technology. For this thesis work, this model proved to be highly inaccurate.

4.4.1 Unified Time Delay (t_d) for distributed RLC lines,

In [11], it was seen that the time delay model that will reduce to the RC delay if resistance dominates or to the RLC delay if inductance dominates. The time delay of an interconnect is the greater of the RC and RLC model delay i.e.

$$t_d = max(t_{d,rlc}, t_{d,rc}) \tag{4.100}$$

The time for signal propagation through the interconnect is dictated by time of flight, t_f for RLC lines and by time to charge up the distributed line capacitance in RC lines. Therefore, in the "max" function, if time of flight dominates, then the line behavior is inductive. Otherwise, it is a resistive line.

Therefore, the eq. 4.100 becomes-

$$t_d = \left[max\ \left(t_f, 0.377rcL^2 + 0.693R_{tr}cL\right)\right] + [0.693.C_L(rL + 0.65R_{tr} + 0.36Z_c)] \tag{4.101}$$

where-

l = wire inductance/m, c = wire capacitance/m, r = wire resistance/m, L = length of wire, R_{tr}= driver output resistance, t_f= time of flight, Z_c= characteristic impedence, C_L = load capacitance

$$t_f = L\sqrt{lc} \tag{4.102}$$

$$Z_c = \sqrt{l/c} \quad \text{for a lossless line} \tag{4.103}$$

Here, $t_d = max\ (a, b)$ means that if $a > b$ then $t_d = a$; else $t_d = b$

4.4.2 Unified Time Delay for repeater insertion ($t_{d,rep}$)

Similar to eq. 4.101, if the time of flight, t_f for an interconnect segment is greater than the RC charging time for its distributed line capacitance the line behaviour is inductive; otherwise, it is resistive, as is borne out by the " max" function in eq. 4.104.

$$t_{d,rep} = max(t_{d,rlc_rep}, t_{d,rc_rep}) \tag{4.104}$$

$$t_d = \left[max\left(t_f, 0.377\frac{rcL^2}{\boldsymbol{k}} + 0.693\frac{R_c cL}{\boldsymbol{h}}\right)\right] + [0.693.C_c(\boldsymbol{h}rL + 0.65\,\boldsymbol{k}R_c + 0.36\,\boldsymbol{hk}Z_c)] \tag{4.105}$$

where-

l = wire inductance/m, c = wire capacitance/m, r = wire resistance/m, L= length of wire, R_c = output resistance of a minimum size inverter, t_f= time of flight, Z_c= characteristic impedence, C_c= input capacitance of a minimum size inverter, $\boldsymbol{k}$ = no. of repeaters, $\boldsymbol{h}$= width of repeaters w.r.t. a minimum size inverter

To obtain the R_c and C_c of a minimum size inverter, we use eqs. 4.106 to 4.109

$$R_c = \left[\frac{1}{C_{ox}(V_{DD}\mu_n)}\right]\frac{\boldsymbol{L}}{\boldsymbol{W}} = \left[\left(\frac{t_{ox}}{\varepsilon_{ox}}\right)\frac{1}{(V_{DD}\mu_n)}\right]\frac{\boldsymbol{L}}{\boldsymbol{W}} \tag{4.106}$$

The input capacitance, $C_c = C_{g\boldsymbol{s},n} + C_{g\boldsymbol{s},p}$ (4.107)

where,

$$C_{g\boldsymbol{s},n} = C_{ox}W(L + 2L_D) = \left(\frac{t_{ox}}{\varepsilon_{ox}}\right)W(L + 2L_D) \tag{4.108}$$

So,

$$C_c \approx 2 \times \left[\left(\frac{t_{ox}}{\varepsilon_{ox}}\right)\boldsymbol{WL}\right] \tag{4.109}$$

Meanwhile, the load capacitance of a minimum size inverter is given by eq. 4.110

$$C_L = \left(C_{g\boldsymbol{d},n} + C_{g\boldsymbol{d},p}\right) + \left(C_{db,n} + C_{db,p}\right) \tag{4.110}$$

4.4.3 Results and Comparison

Deriving the copper interconnect parasitics from Shyh-Chyi Wong's TSM model [31] (described in Appendix A), we obtain the resistance *R*, capacitance *C* and inductance *L* were calculated for a wire of length 1mm (global). The parasitics for CNT bundle are derived from Burke's Luttinger Liquid Theory based equivalent circuit for SWCNT(described in Chapter 3). The dimensions are same as that of copper wire.

Fig. 5.6 to Fig. 5.11 compares the analytical and SPICE simulated delay for varying number of repeaters and a fixed repeater driver transistor (N-MOSFET) sizing.

The SPICE simulated waveform using a PTM 54 model is compared with Unified Time Delay model in Fig. 4.11. The repeater driver transistor (N-MOSFET) sizing has a fixed ratio of 10.

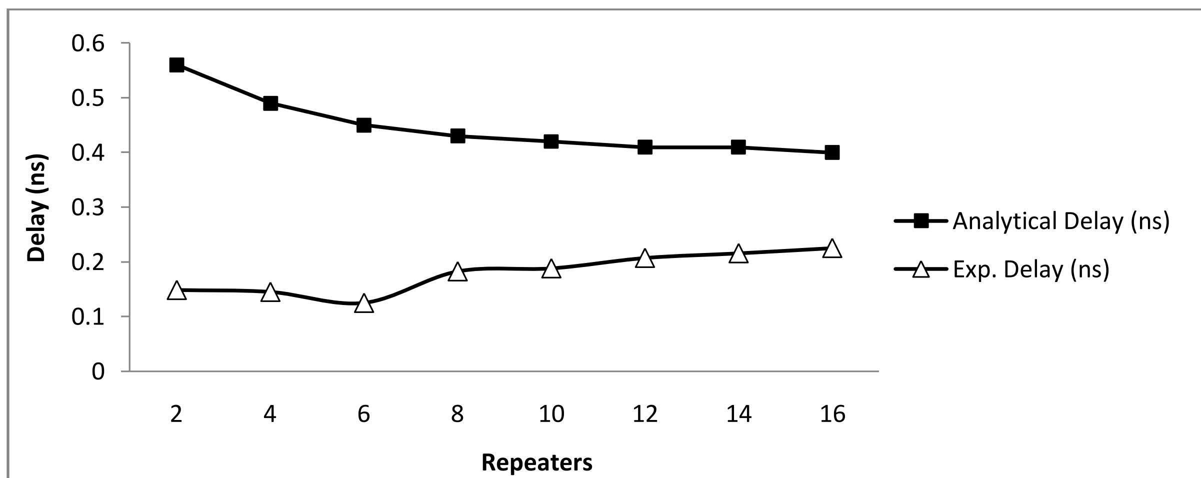

Fig. 4.11 Analytical v/s SPICE delay for Cu interconnect (Unified Time Delay) w.r.t. number of repeaters (for $(W/L)_{driver} = 10$)

The difference in the analytical and SPICE simulated data is shown in Table 4.3. The table shows that the maximum percentage error in analytical waveform is 41.15% while the average error is 27%.

Table 4.3 Comparison of Analytical (Unified Time Delay) and SPICE delay for CNT bundle interconnect

Repeaters	Exp. Delay (ns)	Analytical Delay (ns)	Percentage error (%)
2	0.1485	0.56	41.15
4	0.145	0.49	34.5
6	0.125	0.45	32.5
8	0.1825	0.43	24.75
10	0.188	0.42	23.2
12	0.207	0.41	20.3
14	0.2155	0.41	19.45
16	0.225	0.4	17.5

In Fig. 4.12, the SPICE simulated waveform is compared with Unified Time Delay model for copper interconnect. The repeater driver transistor (N-MOSFET) sizing has a fixed ratio of 40 while the number of repeaters is varied.

The procedure is repeated for CNT bundle interconnect with the repeater driver transistor (N-MOSFET) sizing having a fixed ratio of 40.

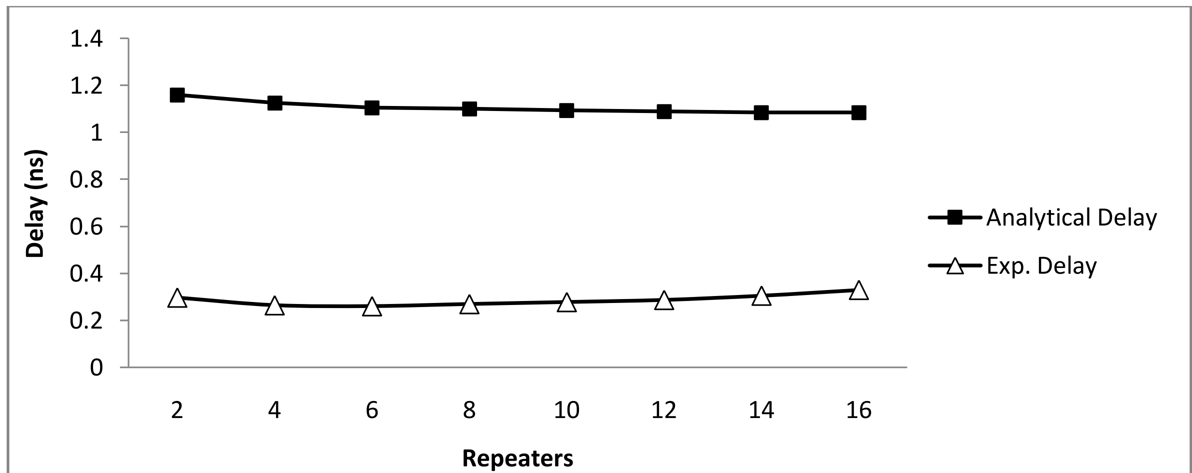

Fig. 4.12 Analytical v/s SPICE delay for Cu interconnect (Unified Time Delay) w.r.t. number of repeaters (for $(W/L)_{driver} = 40$)

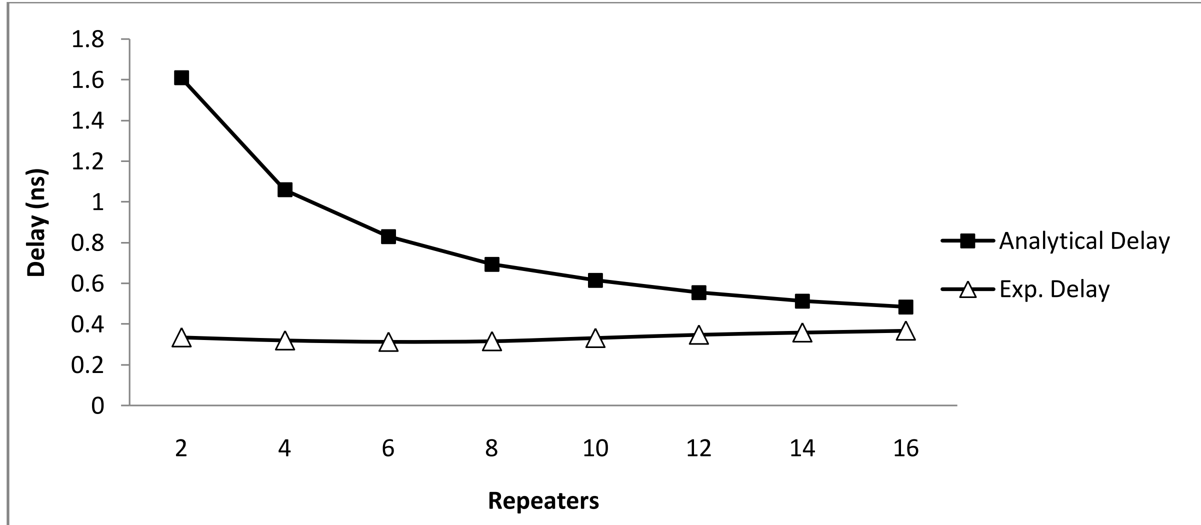

Fig. 4.13 Analytical v/s SPICE delay for CNT bundle interconnect (Unified Time Delay) w.r.t. number of repeaters (for $(W/L)_{driver}$= 40)

The difference in the analytical and SPICE simulated data for both copper and CNT bundle is shown in Table 4.4. The table shows that the maximum percentage error in analytical waveform is 127% for CNT bundle and it is 86.3% for copper.

Table 4.4 Comparison of Analytical (Unified Time Delay) and SPICE delay for Cu and CNT bundle interconnect (for $(W/L)_{driver}$= 40)

	Cu			CNT		
Repeaters	**Exp. Delay (ns)**	**Analytical Delay (ns)**	**Percentage error (%)**	**Exp. Delay**	**Analytical Delay**	**Percentage error (%)**
2	0.297	1.16	86.3	0.335	1.61	127.5
4	0.2645	1.125	86.05	0.32	1.06	74
6	0.2605	1.105	84.45	0.313	0.83	51.7
8	0.2695	1.1	83.05	0.316	0.695	37.9
10	0.278	1.095	81.7	0.332	0.615	28.3
12	0.287	1.09	80.3	0.348	0.555	20.7
14	0.305	1.085	78	0.359	0.515	15.6
16	0.3295	1.085	75.55	0.368	0.485	11.7

In Fig. 4.14 and fig. 4.15, the SPICE simulated waveform is again compared with the Unified Time Delay model for copper and CNT bundle respectively. The repeater driver transistor (N-MOSFET) sizing has a fixed ratio of 80 while the number of repeaters is varied.

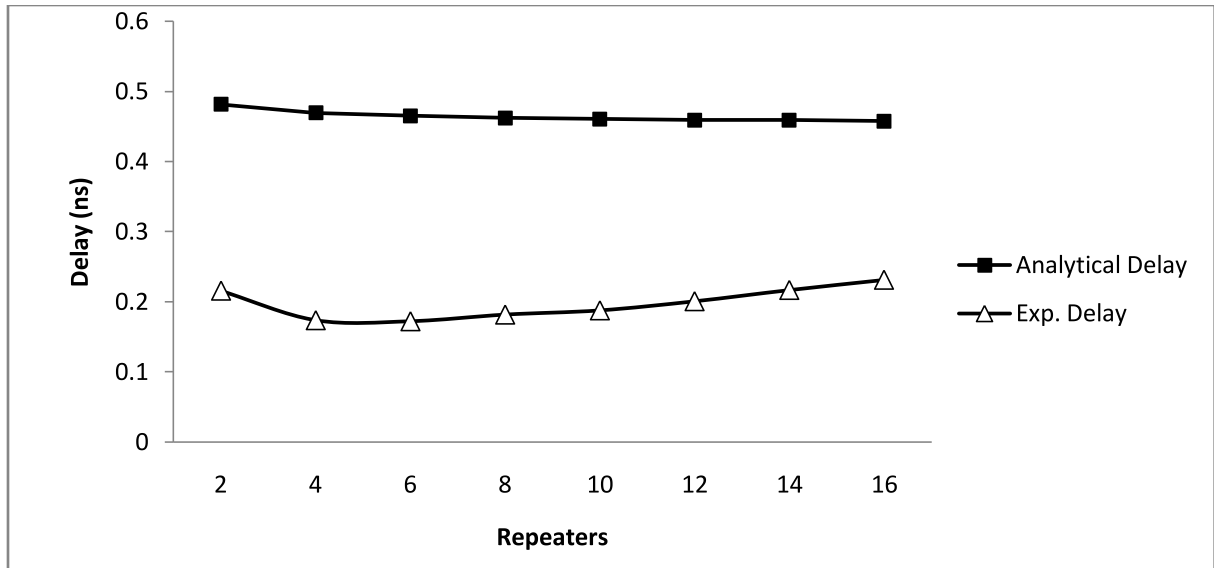

Fig. 4.14: Analytical v/s SPICE delay for Cu interconnect (Unified Time Delay) w.r.t. number of repeaters (for $(W/L)_{driver}= 80$)

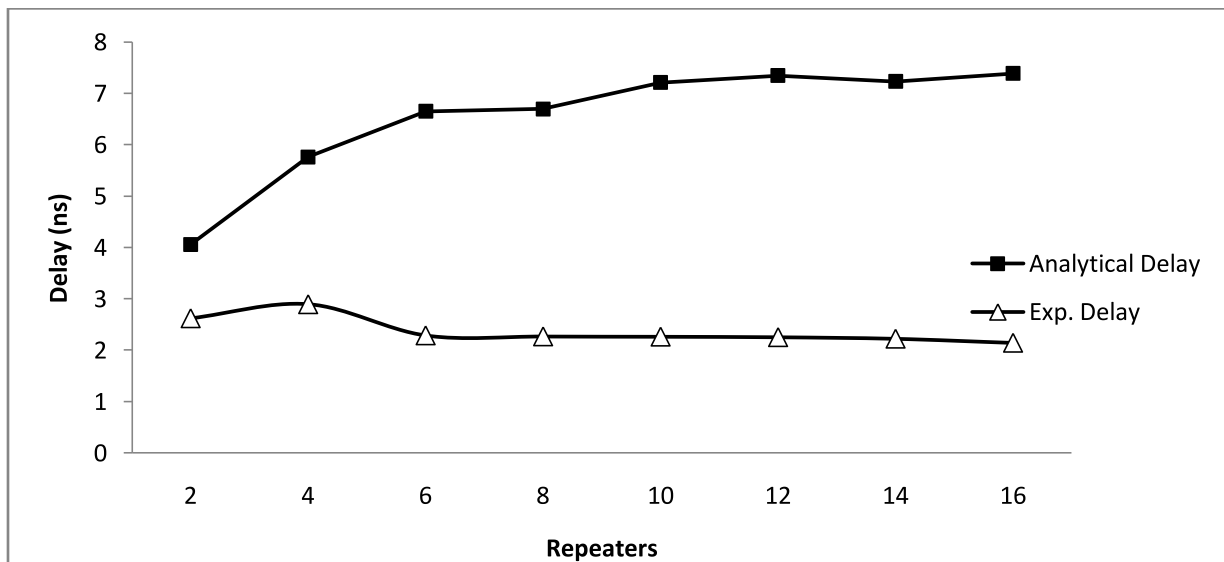

Fig. 4.15 Analytical v/s SPICE delay for CNT bundle interconnect (Unified Time Delay) w.r.t. number of repeaters (for $(W/L)_{driver}= 80$)

The difference in the analytical and SPICE simulated data for both copper and CNT bundle is shown in Table 4.4. The table shows that the maximum percentage error in analytical waveform is 509.33% for CNT bundle and it is 28.4% for copper.

Table 4.5: Comparison of Analytical (Unified Time Delay) and SPICE delay for Cu and CNT bundle interconnect (for $(W/L)_{driver}= 80$)

	Cu			CNT		
Repeaters	**Exp. Delay (ns)**	**Analytical Delay (ns)**	**Percentage error (%)**	**Exp. Delay (ns)**	**Analytical Delay (ns)**	**Percentage error (%)**
2	0.22	0.48	26.55	2.63	4.06	143.52
4	0.17	0.47	29.55	2.90	5.76	286.44
6	0.17	0.47	29.25	2.29	6.65	436.22
8	0.18	0.46	28.00	2.27	6.70	442.78
10	0.19	0.46	27.25	2.27	7.21	494.78
12	0.20	0.46	25.80	2.26	7.35	509.33
14	0.22	0.46	24.20	2.23	7.23	500.54
16	0.23	0.46	22.60	2.15	7.39	524.38

4.5 Comparative study of the three analytical models

Table 4.6: Comparison of Analytical delay errors for the three analytical models

S.no.	Analytical Model	Percentage error (%)	
		CNT interconnect	**Copper interconnect**
1.	α-power	6.63%	10.04%
2.	moment matching	20.86%	21.86%
3.	Unified Time Delay	127%	86.30%

It is observed that in the Driver Interconnect Model (DIL) delay estimation using α-power MOS model, the output waveforms generated by the SPICE and the analytical equations closely match each other (6.63% error). This is because different delay expressions are obtained for linear as well as saturation regions. However, the proposed analysis is far too complex and has lower computational efficiency. In the modified nodal analysis, the driver CMOS inverter was replaced by an "effective" RC load, assuming that it always operates in saturation region. Therefore, its accuracy is less. The Unified Time Delay Model uses a exceedingly simplified expressions for interconnect delay for both segmented RLC lines and for *repeater-inserted* RLC lines. But this model was technology dependent and therefore very inaccurate. This method can only be used to determine the trend for interconnect delay.

CHAPTER

5

SIMULATIONS AND RESULTS

5.1 Introduction

In this chapter, one dimensional CNT bundle and Copper interconnect have been designed and modeled. An analytical model for parasitic impedances RLC interconnect of Copper and CNT is given below and using equations the equivalent resistances, capacitances and inductances were calculated. The model is for top global layer interconnect lines with coupling above one metal ground [31]. After finding these values, they were fitted in the equivalent circuit model to find the delay performance of the interconnect material. Tanner EDA tool package is used to simulate the equivalent circuit SPICE files.

Inductance cannot be ignored based on [21] which states that the exclusion of inductance for an interconnect with repeaters gives less than 10% error in the results if the ratio $T_{L/R}$ is less than or equal to 3. The ratio $T_{L/R}$ is defined as

$$T_{L/R} = \sqrt{\frac{L_{seg}/R_{seg}}{R_t C_t}} \tag{5.1}$$

where L_{seg} and R_{seg} are the inductance and resistance of an interconnect segment and R_t and C_t are the driver resistance and capacitance respectively. For the applications studied in this paper, this criterion of $T_{L/R} >> 3$ is easily met. So an RLC model is used in the analysis. A π- model is employed since it was shown that it was more accurate in delay calculations [21].

RLC circuit model for copper interconnects

Shyh-Chyi Wong [31] proposed the Winbond TSM model for copper interconnect resistance, capacitance and inductance (Appendix A). These equations are valid for the 45nm technology node. In the derivation of a closed-form expression for throughput, a distributed RLC interconnect line with coupling above one ground is assumed.

RLC circuit model for carbon nanotubes

P. J. Burke proposed a Luttinger Liquid Theory based equivalent circuit model [32] to obtain expressions for resistances, inductances and capacitances of a bundle (Chapter 3). This model is well accepted and forms the basis for many useful analyses (shown in Fig. 5.3).

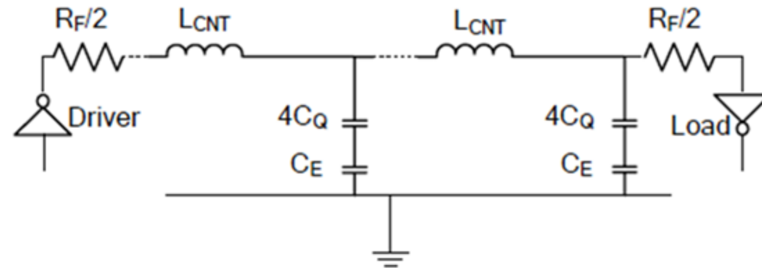

Fig. 5.3 Equivalent RLC circuit for SWCNT Bundle

5.2 Simulation Results

5.2.1 Effect of Repeater sizing

The parameters used in simulation of CNT and Copper interconnects are given below-

Simulation parameters

	Copper	CNT
technology	45 nm	45 nm
V_{DD}	1V	1V
length (L) of interconnect	1000 um (global)	1000 um (global)
width (w) of interconnect	102.5 nm	102.5 nm
spacing (s) between interconnects	102.5 nm	102.5 nm
thickness (h) of global interconnect	235.75 nm	235.75 nm
resistivity (relative)	2.45 Ω-cm	-
oxide thickness (t_{OX})	215.25 nm	215.25 nm
ε_{OX} (relative)	2.45	2.45
Load capacitance	50fF	50fF
frequency	0.1 GHz	0.1 GHz

A schematic for a CMOS inverter driving a 1mm long CNT interconnect with 4 repeaters is given in Fig. 5.4. The corresponding waveforms of input voltage and output, indicating the delay is shown in Fig. 5.5. The circuit was simulated using Tanner EDA tools.

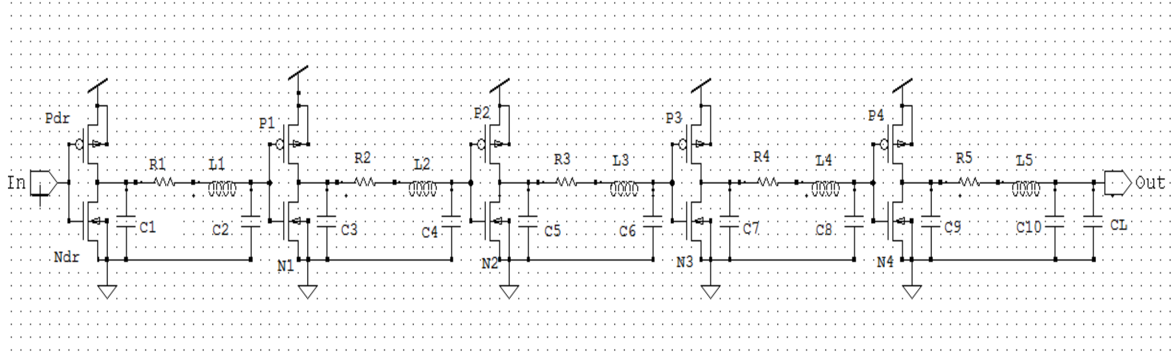

Fig. 5.4 Schematic of a global CNT interconnect with 4 repeaters

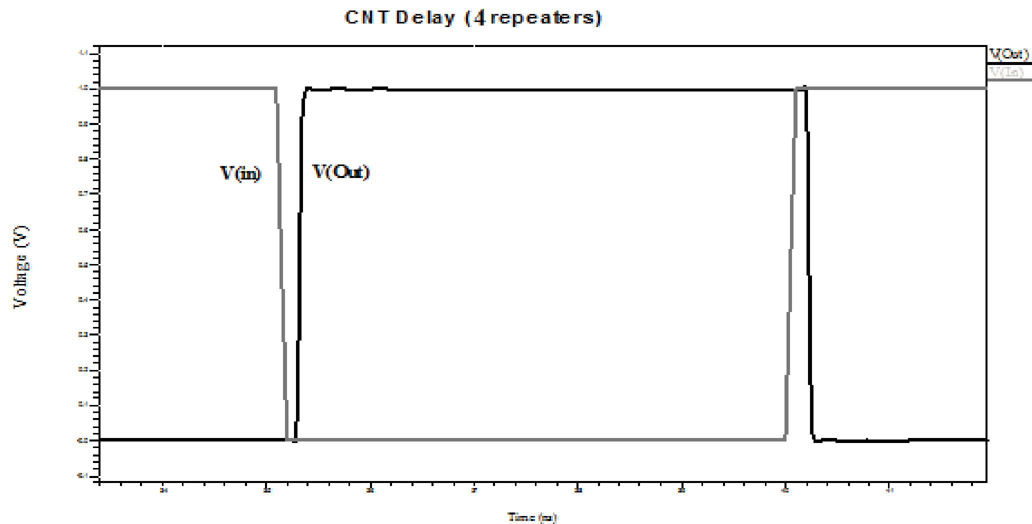

Fig. 5.5 Waveforms of input voltage V(In) and output V(Out) for the circuit shown in Fig. 5.4

Fig. 5.6 to Fig. 5.11 compares the delay between the CNT and Copper interconnect simulations for varying number of repeaters and a fixed repeater driver transistor (N-MOSFET) sizing. The delay first reduces with increasing number of repeaters and then increases again due to the additional load of the repeaters.

The cumulative results of figures from Fig. 5.6 to Fig. 5.11 is shown in Fig. 5.12, and described in Table 5.1 and 5.2. They show the influence of repeater driver transistor (N-

MOSFET) sizing on delay performance. As the repeater size increases, delay reduces since current capacity increases.

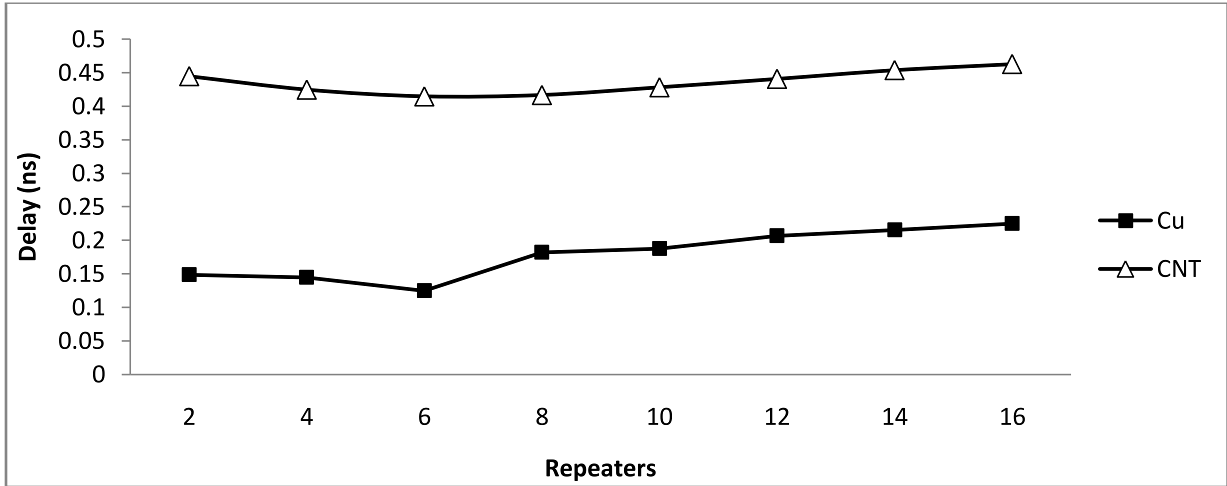

Fig. 5.6 CNT and Cu delay variation w.r.t. number of repeaters (for $(W/L)_{driver}$= 10)

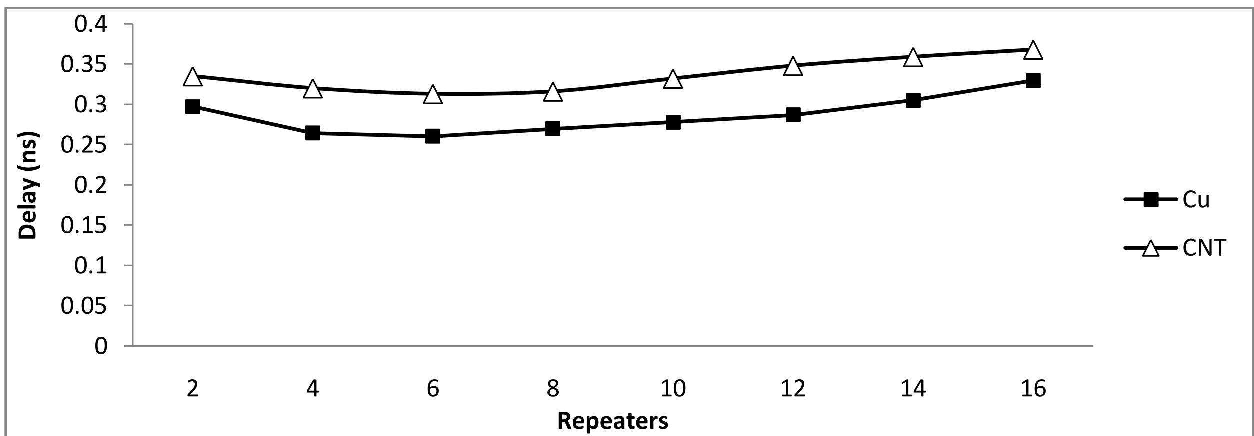

Fig. 5.7 CNT and Cu delay variation w.r.t. number of repeaters (for $(W/L)_{driver}$= 40)

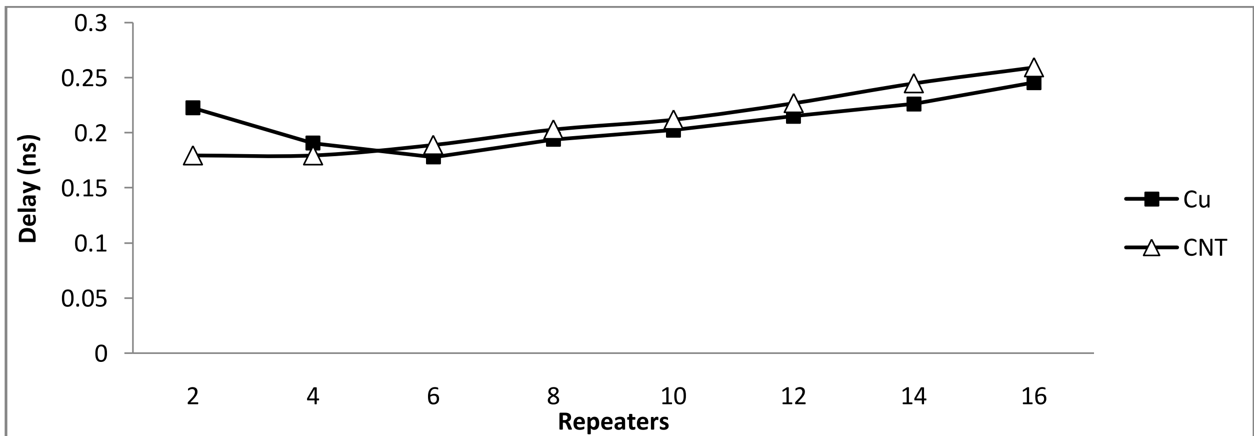

Fig. 5.8 CNT and Cu delay variation w.r.t. number of repeaters (for $(W/L)_{driver=}$ 80)

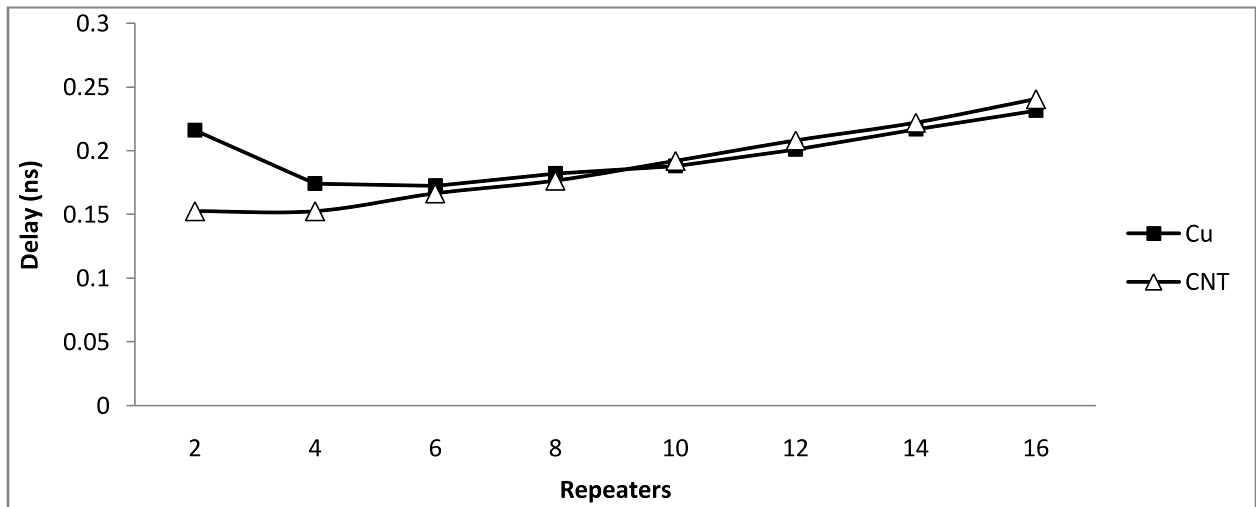

Fig. 5.9 CNT and Cu delay variation w.r.t. number of repeaters (for $(W/L)_{driver}$= 100)

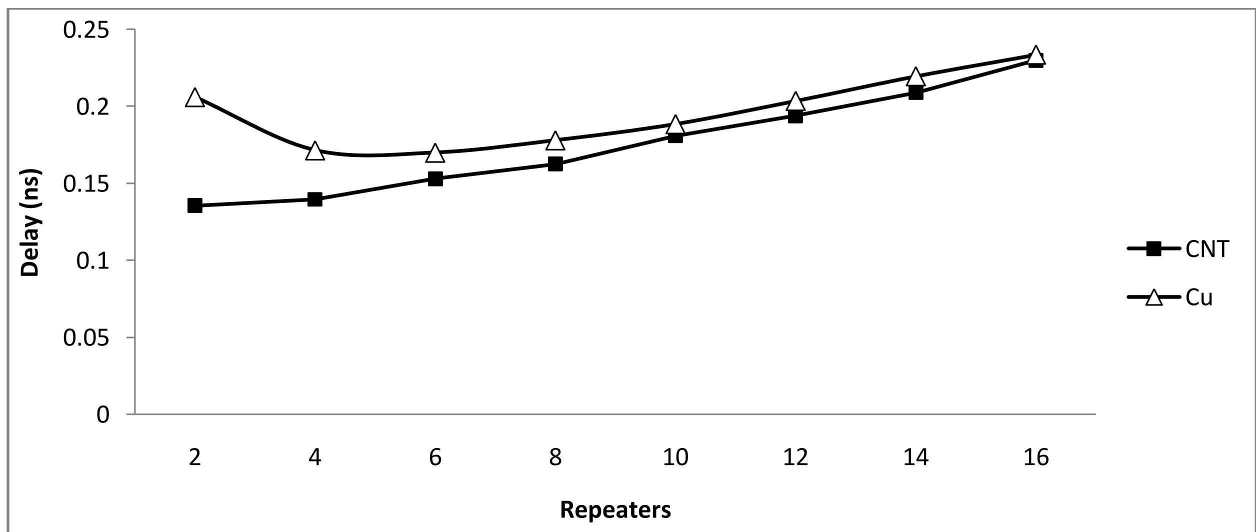

Fig. 5.10 CNT and Cu delay variation w.r.t. number of repeaters (for $(W/L)_{driver}$= 110)

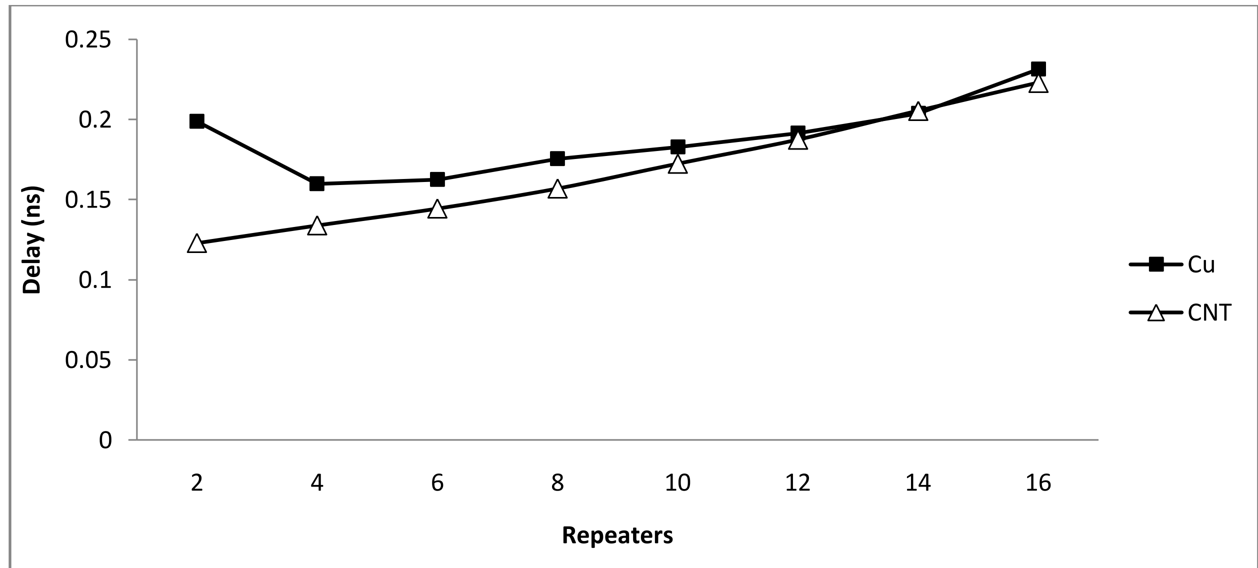

Fig. 5.11 CNT and Cu delay variation w.r.t. number of repeaters (for $(W/L)_{driver}$= 120)

It is seen in Table 5.1 and Table 5.2 that CNT offers a better reduction in delay when increasing the repeater driver transistor W/L ratio above 80. Fig 5.12 illustrates this comparison of CNT delay improvement for different repeater driver widths ($(W/L)_{driver}$).

Table 5.1 Comparison of CNT delay over Copper delay (Delay CNT/Cu) for different repeater driver widths (W/L (n)) and number of repeaters.

	Delay CNT/Cu				
$(W/L)_{driver}$	40	80	100	110	120
Repeaters					
2	1.13	0.81	0.71	0.66	0.64
4	1.21	0.94	0.88	0.81	0.84
6	1.20	1.06	0.97	0.90	0.89
8	1.17	1.05	0.97	0.91	0.89
10	1.19	1.05	1.02	0.96	0.94
12	1.21	1.06	1.03	0.95	0.98
14	1.18	1.08	1.02	0.95	1.01
16	1.12	1.06	1.04	0.99	0.96

Table 5.2: Delay Reduction by CNT (in percentage) over Copper for different repeater driver widths (W/L (n)) and number of repeaters.

	Delay Reduction by CNT (in percentage)				
W/L (n)	40	80	100	110	120
Repeaters					
2	-12.79 %	19.33 %	29.40 %	34.22 %	36.43 %
4	-20.98 %	5.77 %	12.36 %	18.66 %	16.25 %
6	-20.15 %	-6.18 %	3.48 %	10.00 %	11.08 %
8	-17.25 %	-4.64 %	3.02 %	8.71 %	10.54 %
10	-19.42 %	-4.69 %	-2.13 %	3.98 %	5.74 %
12	-21.25 %	-5.58 %	-3.48 %	4.67 %	2.09 %
14	-17.70 %	-8.41 %	-2.30 %	4.78 %	-0.74 %
16	-11.68 %	-5.70 %	-3.89 %	1.50 %	3.67 %

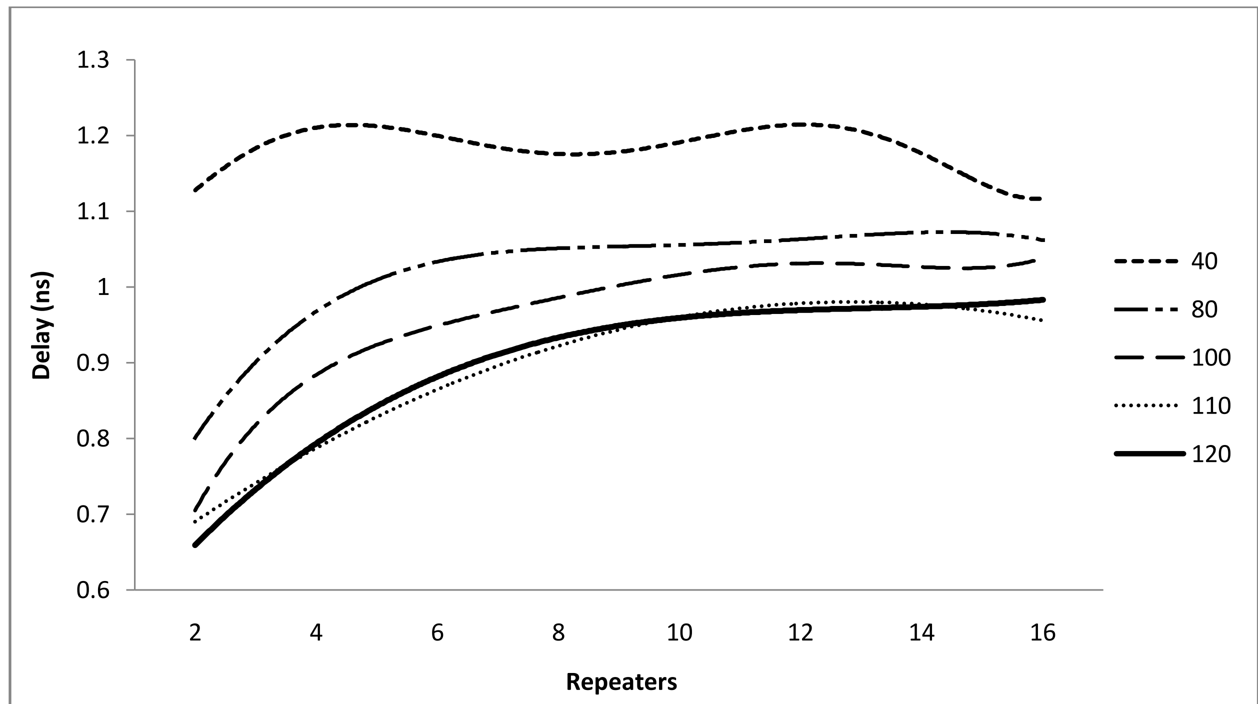

Fig. 5.12 Comparison of CNT/Cu delays for different repeater driver widths W/L(n)

From these results it is verified through SPICE simulations that in the 45 nm technology node, CNT gives a better delay reduction than copper for less number of inserted repeaters in global interconnects. In the lower technology nodes similar superior performance of CNT w.r.t. copper is observed as seen in [52].

5.2.2 Effect of Pitch sizing

The parameters used in simulation of CNT and Copper interconnects are given below-

	Copper	CNT
technology	45 nm	45 nm
V_{DD}	1V	1V
length (L) of interconnect	1000 um (global)	1000 um (global)
thickness (H) of global interconnect	235.75 nm	235.75 nm
resistivity (relative)	2.45 Ω-cm	-
oxide thickness (t_{OX})	215.25 nm	215.25 nm
ε_{OX} (relative)	2.45	2.45
Load capacitance	50fF	50fF
frequency	0.1 GHz	0.1 GHz
$(W/L)_{driver}$	110	110

Fig. 5.13 to Fig. 5.15 compares the delay between the CNT and Copper interconnect simulations for varying number of repeaters and a fixed pitch (ratio of width *w* and spacing *s*). The simulations in Fig. 5.13 to Fig. 5.15 are done using a fixed repeater driver transistor (N-MOSFET) W/L ratio of 110. In agreement with the above simulations, the delay first reduces with increasing number of repeaters and then increases again due to the additional load of the repeaters.

Table 5.3 and 5.4 describes the cumulative results of figures from Fig. 5.13 to Fig. 5.15. The results are illustrated in Fig. 5.17 which shows the influence of pitch (w:s ratio) sizing on delay performance.

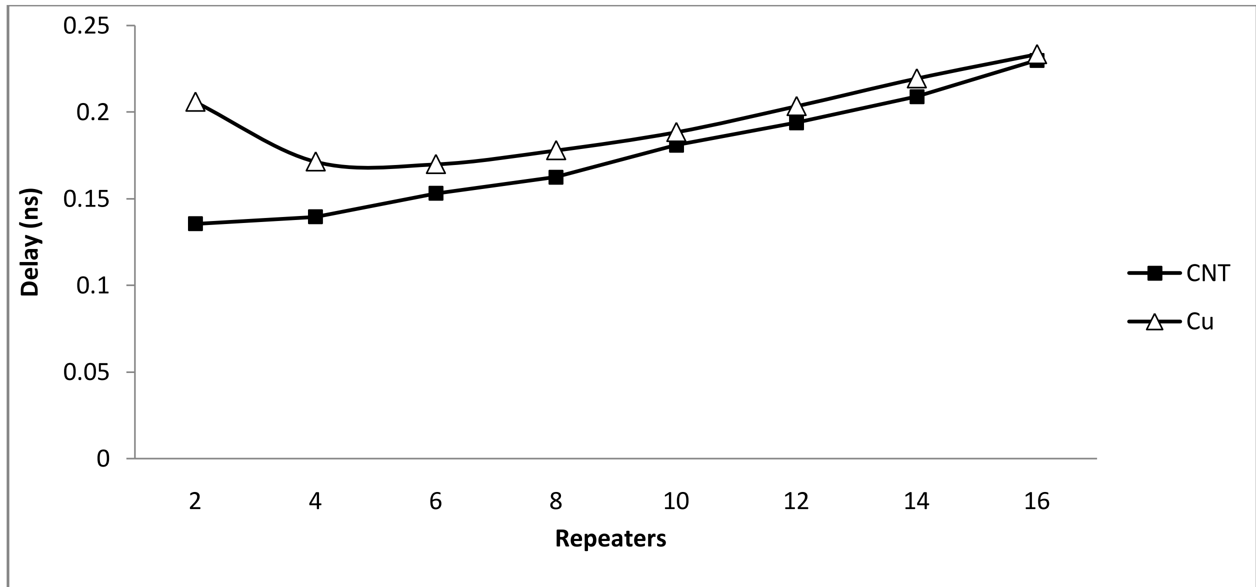

Fig. 5.13 CNT and Cu delay variation w.r.t. number of repeaters (for w:s = 1:1)

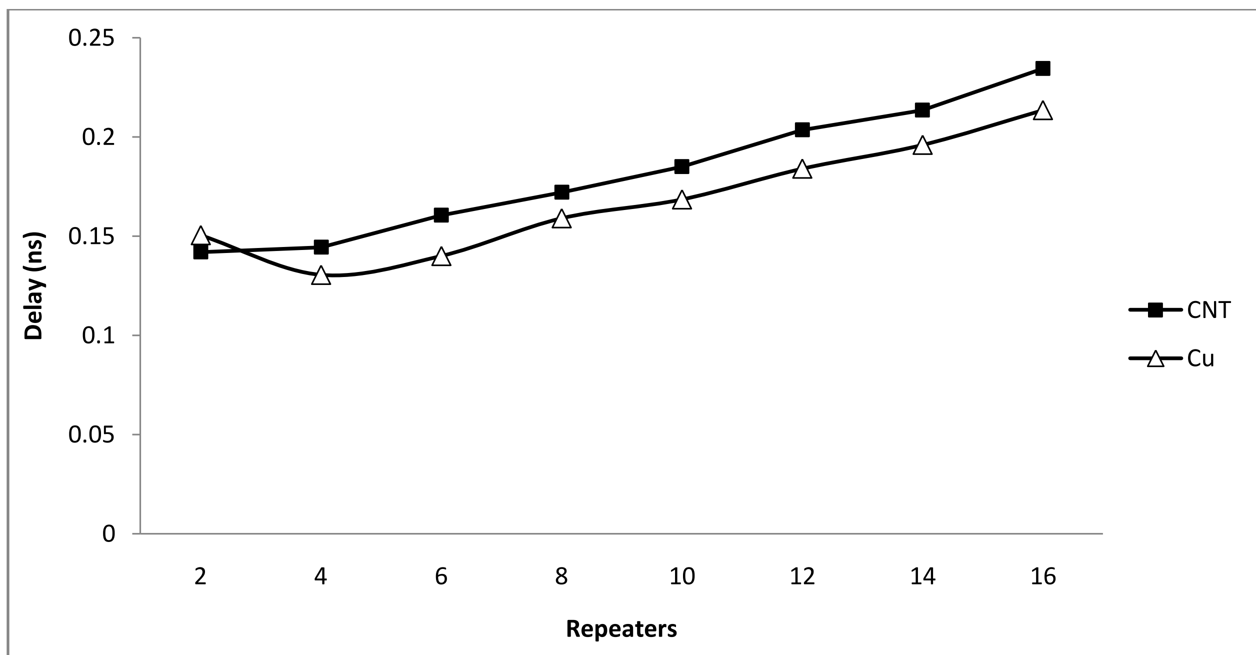

Fig. 5.14 CNT and Cu delay variation w.r.t. number of repeaters (for w:s = 0.5:1.5)

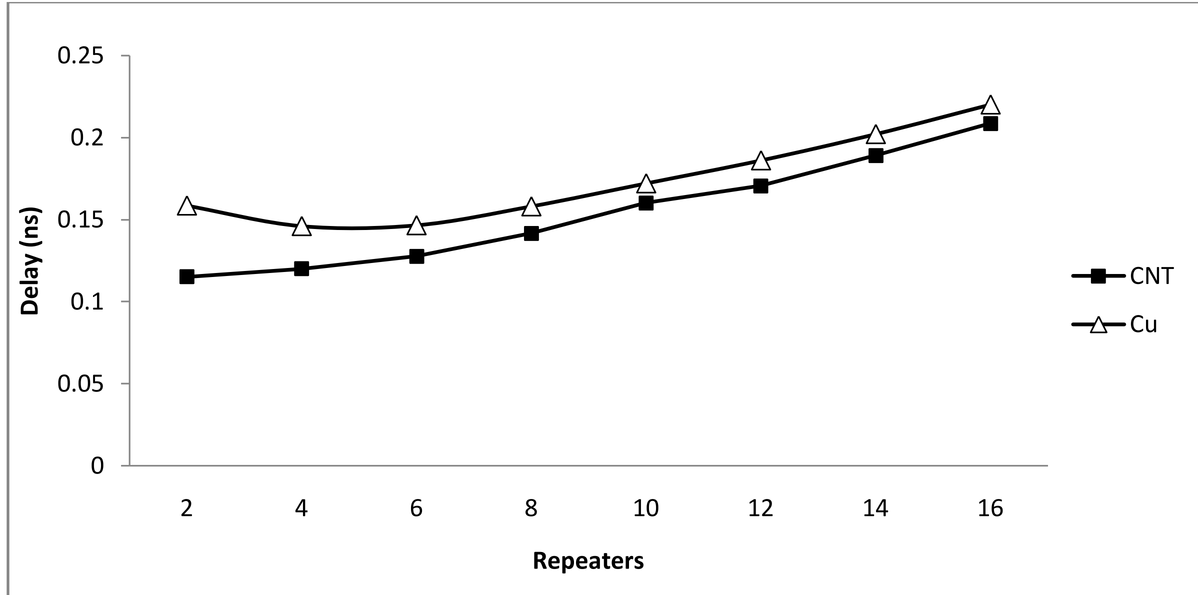

Fig. 5.15 CNT and Cu delay variation w.r.t. number of repeaters (for w:s = 1.5:0.5)

It is seen in Table 5.3 and Table 5.4 that CNT offers a better reduction in delay when the pitch is 1:1 (Fig. 5.16 (a)). Increasing the width to 1.5 times reduces the spacing between interconnects by half (Fig. 5.16 (b)). Thus, the decrease in resistance, owing to increase in *w* is negated by the increase of coupling capacitance between two interconnects due to decrease in spacing *s*.

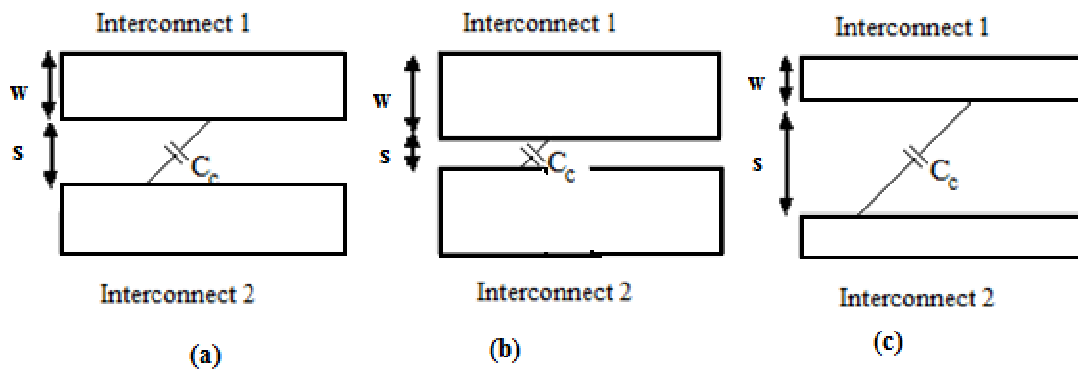

Fig. 5.16 Variation of width, and in turn Pitch in interconnects; C_c shows the coupling capacitance between interconnects: **(a)** wire with width, *w*=spacing, *s* **(b)** wires with larger widths, 1.5w and smaller spacing, 0.5s. **(c)** wires with small widths , 0.5w and large spacing, 1.5s

Similarly, increasing the spacing between interconnects reduces the width of interconnects by half (Fig. 5.16 (c)). Thus, interconnect resistance increases, owing to decrease in *w* which negates the reduction of coupling capacitance between two interconnects (due to increase in spacing *s*). Fig 5.17 further illustrates this comparison of delay variation for different pitch (w:s ratio) .

Table 5.3 Comparison of CNT delay over Copper delay (Delay CNT/Cu) for different pitch (w:s ratio) and number of repeaters.

	Delay CNT/Cu		
w:s ratio	1.5:0.5	1:1	0.5:1.5
Repeaters			
2	0.73	0.36	0.94
4	0.82	0.21	1.11
6	0.87	0.15	1.15
8	0.90	0.11	1.08
10	0.93	0.09	1.10
12	0.92	0.08	1.11
14	0.94	0.07	1.09
16	0.95	0.06	1.10

Table 5.4: Delay Reduction by CNT (in percentage) over Copper for different pitch (w:s ratio) and number of repeaters.

	Delay Reduction by CNT (in percentage)		
w:s ratio	1.5:0.5	1: 1	0.5:1.5
Repeaters			
2	27.44	63.72	5.65
4	17.81	79.45	-10.73
6	12.97	85.49	-14.64
8	10.44	88.81	-8.18
10	6.98	90.70	-9.79
12	8.33	92.36	-10.60
14	6.44	93.32	-8.93
16	5.23	94.08	-9.84

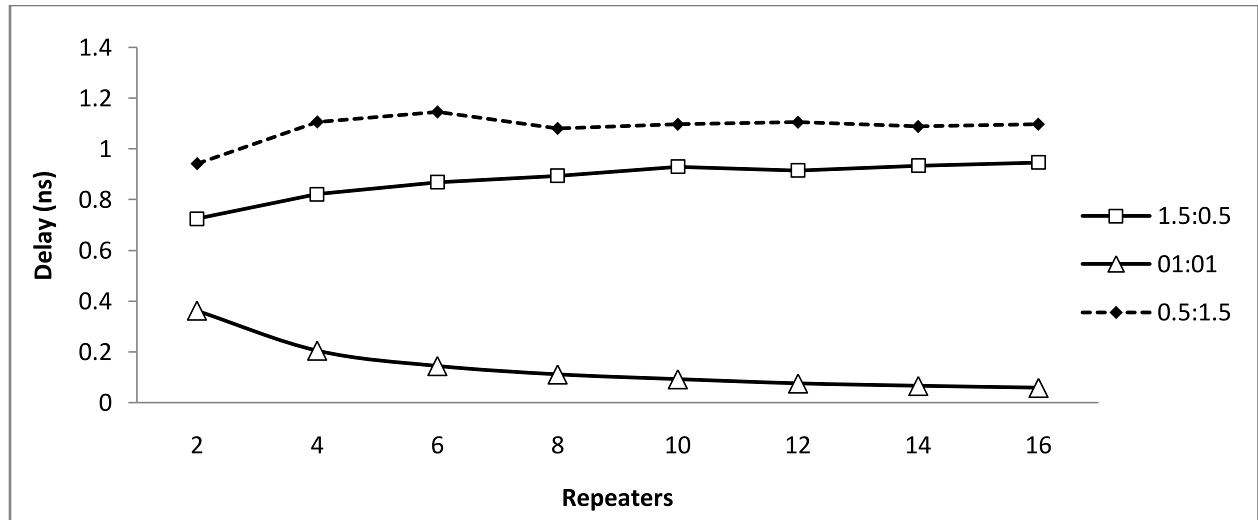

Fig. 5.16 CNT/Cu ratio for different pitch (w:s ratio)

Thus, the increase of either the width or spacing between interconnects leads to the reduction in the other, increasing either the resistance or capacitance. This led to an increase in delay of 36.28% or 58.07% for the two cases respectively. Therefore the layout designers should be very careful while adjusting the width or spacing of interconnect.

In addition, Fig. (5.13) reveal that CNT requires far less number of inserted repeaters (2 against 6 for copper) to achieve the same delay reduction.

CHAPTER

6

CONCLUSION

6.1 Conclusion

In this thesis, the delay performance of CNT-bundle interconnects has been compared to that of copper interconnects. SPICE simulation is used to compare SWCNT interconnect delay with that of copper interconnects for the 45nm technology node. In the case of long global interconnects of 1mm length, densely packed CNT bundle interconnects show significant improvement in performance as compared to copper interconnects, in spite of imperfect metal-nanotube contacts. It is shown that CNT bundle interconnects can greatly reduce signal delay (about 36%).

The effect of simultaneous application of pitch sizing, repeater insertion and repeater sizing on the delay is shown to optimize the delay performance of these interconnects. Comparison the delay between the CNT and Copper interconnect simulations for varying pitch (ratio of width *w* and spacing *s*) and a fixed length show that CNT offers a better reduction in delay when the pitch ratio is 1:1. Thus, the increase of either the width or spacing between interconnects leads to increase of either the resistance (delay increase of 36.28%) or capacitance (delay increase of 58.07%).

In another case it is found that CNT requires less number of inserted repeaters (2 against 6 for copper) to achieve the same delay reduction. Furthermore, it is seen that the delay performance of Copper becomes worse when increasing the repeater driver transistor W/L ratio above 80. CNT gives a better delay reduction than copper in this scenario (29.4 % to 36.43 %).

Besides SPICE simulation, the delay performance of copper and CNT-bundle interconnects were compared using three analytical models. In the Driver Interconnect Model (DIL) using α-power MOS model delay, it is found that the percentage error was found to be 6.63 % for CNT interconnect and 10.04% for Copper interconnect. On the other hand, the modified

nodal analysis and moment matching has a higher percentage error of 21.86% for Copper interconnect. In the Unified Time Delay Model, the error was massive. It was found to be 127% for CNT bundle and 86.3% for copper. Although the Unified Time Delay Model offers very simplified expressions and faster techniques for delay computations, its inaccuracy cannot be ignored. This method can only be used to determine the trend for interconnect delay. Driver Interconnect Model (DIL) is very accurate, but far too complex and has lower computational efficiency. Thus, a tradeoff needs to be made between the computational efficiency and accuracy.

6.2 Future Scope

In this thesis, it was seen that single-walled carbon nanotube bundle can be used instead of copper as an interconnect material for the 45 nm technology node due to high mean free path and high current density. In this technology, the resistivity of copper is large under the combined effects of enhanced grain boundary scattering, surface scattering and the presence of a highly resistive diffusion barrier layer in deep-submicron technology nodes. These are the most important parameters that limit the efficiency of copper in future technology nodes. Thus, as the resistivity of copper is on the rise, there is a need to find a replacement for copper. From this thesis, it can be seen that Carbon Nanotubes can be the viable candidate for future interconnect.

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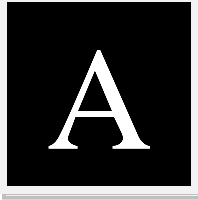

APPENDIX A

A.1 RLC circuit model for copper interconnects

Shyh-Chyi Wong [31] proposed the closed-form expressions for copper interconnect resistance, capacitance and inductance. These equations are valid for the 45nm technology node.

The Winbond TSM model is for top global layer interconnect lines with coupling above one ground. According to the model, the thickness of the interconnect is *t,* the width of CNT bundle is *w*, and *h* is the height of the interconnect above the ground. The spacing between the interconnects *s* is assumed to be equal to the interconnect width, i.e. $s = w$

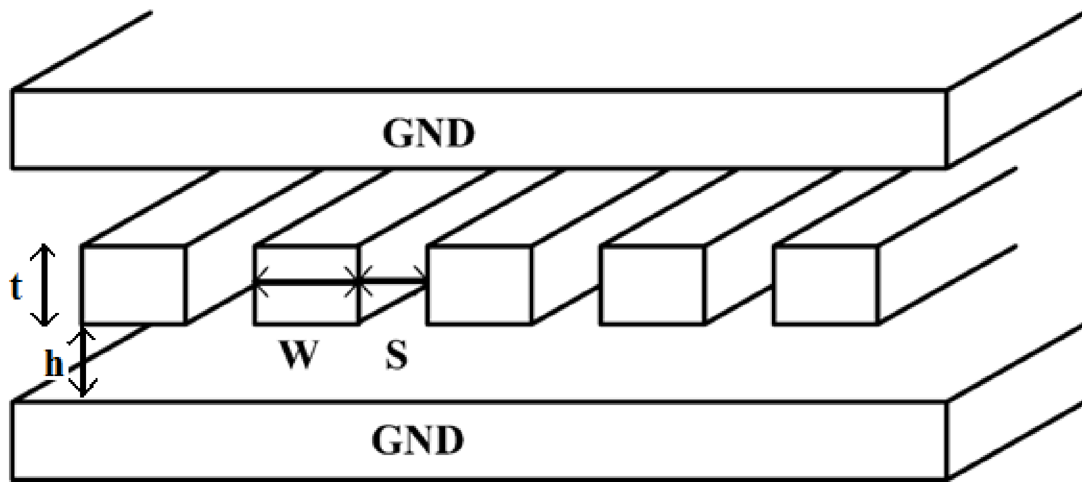

Fig. 5.1: The 2-D structural model of copper interconnect showing its dimensions

.

Based on this model, the resistance of a CNT bundle of length L is given by Eq. (5.2) where ρ is resistivity of copper,

$$R = \frac{\rho l}{wt} \tag{5.2}$$

The total effective capacitance of the copper interconnect is given by

$$C_g = \varepsilon\left[\frac{w}{h} + \left\{2.22\left(\frac{s}{s + 0.7h}\right)^{3.19}\right\} + \left\{1.17\left(\frac{s}{s + 1.51h}\right)^{0.76}\left(\frac{t}{t + 4.53h}\right)^{0.12}\right\}\right]$$

(5.3)

where ε_o is the dielectric permittivity ; and ε_r is the relative dielectric permittivity of copper

$$\varepsilon = \varepsilon_r \times 8.86 \times 10^{-12} \quad (5.4)$$

There are two inductances assscociated with copper interconnect Ls and M. They are given by the Eqs. () shown below

$$L_s = \frac{\mu_o l}{2\pi}\left[ln\left(\frac{2l}{w+t}\right) + \frac{1}{2} + \frac{0.22(w+t)}{l}\right] \quad (5.5)$$

$$M = \frac{\mu_o l}{2\pi}\left[ln\left(\frac{2l}{d}\right) - 1 + \frac{d}{l}\right] \quad (5.6)$$

where μ_o is the permeability, $\mu_o = 4\pi \times 10^{-7}$

Here, we have assumed that the spacing between interconnects *s* is equal to the interconnect width, i.e. $s = w$. Also the distance between two layers of interconnects *d* is assumed to be equal to the twice the interconnect width, i.e.$d = 2$.

Furthermore, the thickness of the interconnect *t* can be changed according to the aspect ratio, AR

$$t = AR \times w \quad (5.7)$$

A.2 BSIM 3v3 Level 49 SPICE File

.MODEL NMOS NMOS (LEVEL = 49 +VERSION = 3.1

```
TNOM    = 27           TOX     = 7.7E-9
+XJ     = 1E-7         NCH     = 2.2E17         VTH0    = 0.5244477
+K1     = 0.5715897    K2      = 0.0141559      K3      = 79.4813719
+K3B    = -9.584785    W0      = 2.801236E-5    NLX     = 1.814988E-7
+DVT0W  = 0            DVT1W   = 0              DVT2W   = 0
+DVT0   = 5.5178257    DVT1    = 0.777727       DVT2    = -0.0308743
+U0     = 400.6658093  UA      = -2.52294E-10   UB      = 1.849095E-18
+UC     = 3.586835E-11 VSAT    = 1.670969E5     A0      = 1.3495812
+AGS    = 0.2113616    B0      = 9.509772E-7    B1      = 5E-6
+KETA   = 4.145053E-3  A1      = 0              A2      = 0.4031612
+RDSW   = 953.621599   PRWG    = -9.422186E-3   PRWB    = -0.0838438
+WR     = 1            WINT    = 1.522385E-7    LINT    = 4.056535E-9
+XL     = -5E-8        XW      = 1.5E-7         DWG     = -5.989391E-9
+DWB    = 4.817166E-9  VOFF    = -0.1038934     NFACTOR = 0.6391361
+CIT    = 0            CDSC    = 2.4E-4         CDSCD   = 0
+CDSCB  = 0            ETA0    = 0.5012862      ETAB    = -0.0206888
```

```
+DSUB    = 0.8486731      PCLM    = 1.4937207      PDIBLC1 = 2.088589E-3
+PDIBLC2 = 4.759795E-3    PDIBLCB = 0.0677132      DROUT   = 0.1009912
+PSCBE1  = 7.37409E8      PSCBE2  = 9.609802E-4    PVAG    = 0
+DELTA   = 0.01           RSH     = 3.4            MOBMOD  = 1
+PRT     = 0              UTE     = -1.5           KT1     = -0.11
+KT1L    = 0              KT2     = 0.022          UA1     = 4.31E-9
+UB1     = -7.61E-18      UC1     = -5.6E-11       AT      = 3.3E4
+WL      = 0              WLN     = 1              WW      = 0
+WWN     = 1              WWL     = 0              LL      = 0
+LLN     = 1              LW      = 0              LWN     = 1
+LWL     = 0              CAPMOD  = 2              XPART   = 0.5
+CGDO    = 3.24E-10       CGSO    = 3.24E-10       CGBO    = 1E-12
+CJ      = 1.004428E-3    PB      = 0.8            MJ      = 0.33289
+CJSW    = 3.16922E-10    PBSW    = 0.7            MJSW    = 0.2004559
+CJSWG   = 1.82E-10       PBSWG   = 0.7            MJSWG   = 0.2004559
+CF      = 0              PVTH0   = -0.0191254     PRDSW   = -77.8978772
+PK2     = 1.363802E-3    WKETA   = -6.966301E-3   LKETA   = -4.253867E-3    )
*
.MODEL PMOS PMOS (                                 LEVEL   = 49
+VERSION = 3.1            TNOM    = 27             TOX     = 7.7E-9
+XJ      = 1E-7           NCH     = 8.52E16        VTH0    = -0.6293205
+K1      = 0.442207       K2      = -0.0115433     K3      = 81.6279615
+K3B     = -5             W0      = 6.381874E-6    NLX     = 3.084152E-7
+DVT0W   = 0              DVT1W   = 0              DVT2W   = 0
+DVT0    = 0.7885721      DVT1    = 0.5436265      DVT2    = -0.0818278
+U0      = 156.8387812    UA      = 1.000775E-10   UB      = 2.010512E-18
+UC      = -1.18858E-11   VSAT    = 2E5            A0      = 1.1637791
+AGS     = 0.375441       B0      = 2.444752E-6    B1      = 5E-6
+KETA    = -7.924167E-3   A1      = 0              A2      = 0.3059919
+RDSW    = 4E3            PRWG    = -0.1126488     PRWB    = -0.0251834
+WR      = 1              WINT    = 1.55303E-7     LINT    = 0
+XL      = -5E-8          XW      = 1.5E-7         DWG     = -1.634839E-8
+DWB     = 8.887067E-9    VOFF    = -0.1375077     NFACTOR = 2
+CIT     = 0              CDSC    = 2.4E-4         CDSCD   = 0
+CDSCB   = 0              ETA0    = 1.321073E-3    ETAB    = -3.315168E-3
+DSUB    = 0.0123957      PCLM    = 3.0840812      PDIBLC1 = 0.0812069
+PDIBLC2 = 5.303088E-3    PDIBLCB = -1E-3          DROUT   = 0.4090848
+PSCBE1  = 7.762632E10    PSCBE2  = 5.04699E-10    PVAG    = 1.5324968
+DELTA   = 0.01           RSH     = 2.7            MOBMOD  = 1
+PRT     = 0              UTE     = -1.5           KT1     = -0.11
+KT1L    = 0              KT2     = 0.022          UA1     = 4.31E-9
+UB1     = -7.61E-18      UC1     = -5.6E-11       AT      = 3.3E4
+WL      = 0              WLN     = 1              WW      = 0
+WWN     = 1              WWL     = 0              LL      = 0
+LLN     = 1              LW      = 0              LWN     = 1
+LWL     = 0              CAPMOD  = 2              XPART   = 0.5
```

```
+CGDO    = 2.8E-10       CGSO    = 2.8E-10       CGBO    = 1E-12
+CJ      = 1.443723E-3    PB      = 0.99          MJ      = 0.5499545
+CJSW    = 3.859203E-10   PBSW    = 0.9877815     MJSW    = 0.3654842)
```

A.3 PTM Level 54 Model

```
.model  NMOS  NMOS level = 54  +version = 4.0
 binunit = 1             paramchk= 1             mobmod  = 0
+capmod  = 2             igcmod  = 1             igbmod  = 1             geomod  = 1
+diomod  = 1             rdsmod  = 0             rbodymod= 1             rgatemod= 1
+permod  = 1             acnqsmod= 0             trnqsmod= 0

+tnom    = 27            toxe    = 7.5e-010      toxp    = 5e-010        toxm    = 7.5e-010
+dtox    = 2.5e-010      epsrox  = 3.9           wint    = 5e-009        lint    = 1.95e-009
+ll      = 0             wl      = 0             lln     = 1             wln     = 1
+lw      = 0             ww      = 0             lwn     = 1             wwn     = 1
+lwl     = 0             wwl     = 0             xpart   = 0             toxref  = 7.5e-010       xl      = -
14e-9
+dlcig   = 1.95e-009
+vth0    = 0.3558        k1      = 0.2           k2      = 0             k3      = 0
+k3b     = 0             w0      = 2.5e-006      dvt0    = 1             dvt1    = 2
+dvt2    = 0             dvt0w   = 0             dvt1w   = 0             dvt2w   = 0
+dsub    = 0.078         minv    = 0.05          voffl   = 0             dvtp0   = 1e-011
+dvtp1   = 0.1           lpe0    = 0             lpeb    = 0             xj      = 1e-008
+ngate   = 1e+023        ndep    = 8.7e+018      nsd     = 2e+020        phin    = 0
+cdsc    = 0             cdscb   = 0             cdscd   = 0             cit     = 0
+voff    = -0.13         nfactor = 2.1           eta0    = 0.005         etab    = 0
+vfb     = -1.058        u0      = 0.0238        ua      = -5e-010       ub      = 1.7e-018
+uc      = 0             vsat    = 182130        a0      = 1             ags     = 0
+a1      = 0             a2      = 1             b0      = 0             b1      = 0
+keta    = 0.04          dwg     = 0             dwb     = 0             pclm    = 0.06
+pdiblc1 = 0.001         pdiblc2 = 0.001         pdiblcb = -0.005        drout   = 0.5
+pvag    = 1e-020        delta   = 0.01          pscbe1  = 2.0e+009      pscbe2  = 1e-007
+fprout  = 0.2           pdits   = 0.01          pditsd  = 0.23          pditsl  = 2300000
+rsh     = 5             rdsw    = 80            rsw     = 40            rdw     = 40
+rdswmin = 0             rdwmin  = 0             rswmin  = 0             prwg    = 0
+prwb    = 0             wr      = 1             alpha0  = 0.074         alpha1  = 0.005
+beta0   = 30            agidl   = 0.0002        bgidl   = 2.1e+009      cgidl   = 0.0002
+egidl   = 0.8           aigbacc = 0.012         bigbacc = 0.0028        cigbacc = 0.002
+nigbacc = 1             aigbinv = 0.014         bigbinv = 0.004         cigbinv = 0.004
+eigbinv = 1.1           nigbinv = 3             aigc    = 0.020014      bigc    = 0.0027432
+cigc    = 0.002         aigsd   = 0.020014      bigsd   = 0.0027432     cigsd   = 0.002
+nigc    = 1             poxedge = 1             pigcd   = 1             ntox    = 1
+xrcrg1  = 12            xrcrg2  = 5
+cgso    = 9e-011        cgdo    = 9e-011        cgbo    = 0             cgdl    = 7.5e-013
```

```
+cgsl    = 7.5e-013       clc     = 1e-007        cle     = 0.6          cf      = 1.1e-010
+ckappas = 0.6            ckappad = 0.6           vfbcv   = -1           acde    = 1
+moin    = 15             noff    = 1             voffcv  = 0

+kt1     = -0.154         kt1l    = 0             kt2     = 0.022        ute     = -1.1
+ua1     = 1e-009         ub1     = -1e-018       uc1     = -5.6e-011    prt     = 0
+at      = 33000
+fnoimod = 1              tnoimod = 0             noia    = 6.25e+041    noib    = 3.125e+026
+noic    = 8.75e+009      em      = 41000000      af      = 1            ef      = 1
+kf      = 0              tnoia   = 1.5           tnoib   = 3.5          ntnoi   = 1
+jss     = 1.2e-006       jsws    = 2.4e-013      jswgs   = 2.4e-013     njs     = 1
+ijthsfwd= 0.1            ijthsrev= 0.1           bvs     = 10           xjbvs   = 1
+jsd     = 1.2e-006       jswd    = 2.4e-013      jswgd   = 2.4e-013     xjbvd   = 1
+pbs     = 1              cjs     = 0.0018        mjs     = 0.5          pbsws   = 1
+cjsws   = 1.2e-010       mjsws   = 0.33          cjswgs  = 2.1e-010     cjd     = 0.0018
+cjswd   = 1.2e-010       mjswd   = 0.33          pbswgd  = 1            cjswgd  = 2.1e-010
+mjswgd  = 0.33           tpb     = 0             tcj     = 0            tpbsw   = 0
+tcjsw   = 0              tpbswg  = 0             tcjswg  = 0            xtis    = 3
+dmcg    = 0              dmci    = 0             dmdg    = 0            dmcgt   = 0
+dwj     = 0              xgw     = 0             xgl     = 0
+rshg    = 0.4            gbmin   = 1e-010        rbpb    = 5            rbpd    = 15
+rbps    = 15             rbdb    = 15            rbsb    = 15           ngcon   = 1
```

.model PMOS PMOS level = 54

```
+version = 4.0            binunit = 1             paramchk= 1            mobmod  = 0
+capmod  = 2              igcmod  = 1             igbmod  = 1            geomod  = 1
+diomod  = 1              rdsmod  = 0             rbodymod= 1            rgatemod= 1
+permod  = 1              acnqsmod= 0             trnqsmod= 0
+tnom    = 27             toxe    = 7.7e-010      toxp    = 5e-010       toxm    = 7.7e-010
+dtox    = 2.7e-010       epsrox  = 3.9           wint    = 5e-009       lint    = 1.95e-009
+ll      = 0              wl      = 0             lln     = 1            wln     = 1
+lw      = 0              ww      = 0             lwn     = 1            wwn     = 1
+lwl     = 0              wwl     = 0             xpart   = 0            toxref  = 7.7e-010       xl      = -
14e-9
+dlcig   = 1.95e-009
+vth0    = -0.24123       k1      = 0.2           k2      = -0.01        k3      = 0
+k3b     = 0              w0      = 2.5e-006      dvt0    = 1            dvt1    = 2
+dvt2    = -0.032         dvt0w   = 0             dvt1w   = 0            dvt2w   = 0
+dsub    = 0.1            minv    = 0.05          voffl   = 0            dvtp0   = 1e-011
+dvtp1   = 0.05           lpe0    = 0             lpeb    = 0            xj      = 1.008e-008
+ngate   = 1e+023         ndep    = 3.5e+018      nsd     = 2e+020       phin    = 0
+cdsc    = 0              cdscb   = 0             cdscd   = 0            cit     = 0
+voff    = -0.13          nfactor = 2.1           eta0    = 0.0042       etab    = 0
+vfb     = -1.058         u0      = 0.00306       ua      = -5e-010      ub      = 1.6e-018
+uc      = 0              vsat    = 78000         a0      = 1            ags     = 1e-020
```

```
+a1      = 0              a2      = 1              b0      = 0              b1      = 0
+keta    = -0.047         dwg     = 0              dwb     = 0              pclm    = 0.1
+pdiblc1 = 0.001          pdiblc2 = 0.001          pdiblcb = 3.4e-008       drout   = 0.6
+pvag    = 1e-020         delta   = 0.01           pscbe1  = 2e+009         pscbe2  = 9.58e-007
+fprout  = 0.2            pdits   = 0.08           pditsd  = 0.23           pditsl  = 2300000
+rsh     = 5              rdsw    = 80             rsw     = 40             rdw     = 40
+rdswmin = 0              rdwmin  = 0              rswmin  = 0              prwg    = 0
+prwb    = 0              wr      = 1              alpha0  = 0.074          alpha1  = 0.005
+beta0   = 30             agidl   = 0.0002         bgidl   = 2.1e+009       cgidl   = 0.0002
+egidl   = 0.8            aigbacc = 0.012          bigbacc = 0.0028         cigbacc = 0.002
+nigbacc = 1              aigbinv = 0.014          bigbinv = 0.004          cigbinv = 0.004
+eigbinv = 1.1            nigbinv = 3              aigc    = 0.011942       bigc    = 0.0012217
+cigc    = 0.0008         aigsd   = 0.011942       bigsd   = 0.0012217      cigsd   = 0.0008
+nigc    = 1              poxedge = 1              pigcd   = 1              ntox    = 1
+xrcrg1  = 12             xrcrg2  = 5
+cgso    = 9e-011         cgdo    = 9e-011         cgbo    = 0              cgdl    = 3e-011
+cgsl    = 3e-011         clc     = 1e-007         cle     = 0.6            cf      = 1.1e-010
+ckappas = 0.6            ckappad = 0.6            vfbcv   = -1             acde    = 1
+moin    = 15             noff    = 1              voffcv  = 0
+kt1     = -0.14          kt1l    = 0              kt2     = 0.022          ute     = -1.1
+ua1     = 1e-009         ub1     = -1e-018        uc1     = -5.6e-011      prt     = 0
+at      = 33000
+fnoimod = 1              tnoimod = 0              noia    = 6.25e+041      noib    = 3.125e+026
+noic    = 8.75e+009      em      = 41000000       af      = 1              ef      = 1
+kf      = 0              tnoia   = 1.5            tnoib   = 3.5            ntnoi   = 1
+jss     = 2e-007         jsws    = 4e-013         jswgs   = 4e-013         njs     = 1
+ijthsfwd= 0.1            ijthsrev= 0.1            bvs     = 10             xjbvs   = 1
+jsd     = 2e-007         jswd    = 4e-013         jswgd   = 4e-013         xjbvd   = 1
+pbs     = 1              cjs     = 0.0015         mjs     = 0.5            pbsws   = 1
+cjsws   = 9.4e-011       mjsws   = 0.33           cjswgs  = 2e-010         cjd     = 0.0015
+cjswd   = 9.4e-011       mjswd   = 0.33           pbswgd  = 1              cjswgd  = 2e-010
+mjswgd  = 0.33           tpb     = 0              tcj     = 0              tpbsw   = 0
+tcjsw   = 0              tpbswg  = 0              tcjswg  = 0              xtis    = 3
+dmcg    = 0              dmdg    = 0              dmcgt   = 0              xgw     = 0
+xgl     = 0
+rshg    = 0.1            gbmin   = 1e-012         rbpb    = 50             rbpd    = 50
+rbps    = 50             rbdb    = 50             rbsb    = 50             ngcon   = 1
```

A.4 SPICE file for interconnect with 10 repeaters

Simulation parameters

	Copper	CNT
technology	45 nm	45 nm
V_{DD}	1V	1V
length (L) of interconnect	1000 um (global)	1000 um (global)
width (w) of interconnect	102.5 nm	102.5 nm
spacing (s) between interconnects	102.5 nm	102.5 nm
thickness (h) of global interconnect	235.75 nm	235.75 nm
resistivity (relative)	2.45 Ω-cm	-
oxide thickness (t_{OX})	215.25 nm	215.25 nm
ε_{OX} (relative)	2.45	2.45
Load capacitance	50fF	50fF
frequency	0.1 GHz	0.1 GHz
number of repeaters	10 repeaters	10 repeaters
$(W/L)_{driver}$	110	110

A.4.1 SPICE file for a CNT interconnect

```
CCapacitor_6 N_24 Gnd 0.034pF
CCapacitor_7 N_22 Gnd 0.034pF
CCapacitor_8 N_30 Gnd 0.034pF
RResistor_1 N_2 N_4 12.524 TC=0.0, 0.0
CCapacitor_9 N_28 Gnd 0.034pF
RResistor_2 N_10 N_5 12.524 TC=0.0, 0.0
RResistor_3 N_16 N_6 12.524 TC=0.0, 0.0
RResistor_4 N_22 N_7 12.524 TC=0.0, 0.0
RResistor_5 N_28 N_8 12.524 TC=0.0, 0.0
RResistor_6 N_34 N_9 12.524 TC=0.0, 0.0
RResistor_7 N_40 N_11 12.524 TC=0.0, 0.0
RResistor_8 N_3 N_14 12.524 TC=0.0, 0.0
RResistor_9 N_15 N_19 12.524 TC=0.0, 0.0
LInductor_1 N_4 N_12 0.0023p
LInductor_2 N_5 N_18 0.0023p
LInductor_3 N_6 N_24 0.0023p
LInductor_4 N_7 N_30 0.0023p
```

LInductor_5 N_8 N_36 0.0023p
MMOSFET_N_10 N_20 N_17 Gnd Gnd NMOS L=50n W=5.5u AD=0.6875p PD=11.25u AS=0.6875p PS=11.25u
LInductor_6 N_9 N_42 0.0023p
MMOSFET_N_11 N_25 N_21 Gnd Gnd NMOS L=50n W=5.5u AD=0.6875p PD=11.25u AS=0.6875p PS=11.25u
LInductor_7 N_11 N_1 0.0023p
LInductor_8 N_14 N_13 0.0023p
LInductor_9 N_19 N_17 0.0023p
RResistor_10 N_20 N_23 12.524 TC=0.0, 0.0
RResistor_11 N_25 N_26 12.524 TC=0.0, 0.0
LInductor_10 N_23 N_21 0.0023p
LInductor_11 N_26 Out 0.0023p
MMOSFET_P_1 N_2 In Vdd Vdd PMOS L=50n W=16.5u AD=2.0625p PD=33.25u AS=2.0625p PS=33.25u
MMOSFET_P_2 N_10 N_12 Vdd Vdd PMOS L=50n W=16.5u AD=2.0625p PD=33.25u AS=2.0625p PS=33.25u
MMOSFET_P_3 N_16 N_18 Vdd Vdd PMOS L=50n W=16.5u AD=2.0625p PD=33.25u AS=2.0625p PS=33.25u
MMOSFET_P_4 N_22 N_24 Vdd Vdd PMOS L=50n W=16.5u AD=2.0625p PD=33.25u AS=2.0625p PS=33.25u
MMOSFET_P_5 N_28 N_30 Vdd Vdd PMOS L=50n W=16.5u AD=2.0625p PD=33.25u AS=2.0625p PS=33.25u
MMOSFET_P_6 N_34 N_36 Vdd Vdd PMOS L=50n W=16.5u AD=2.0625p PD=33.25u AS=2.0625p PS=33.25u
MMOSFET_P_7 N_40 N_42 Vdd Vdd PMOS L=50n W=16.5u AD=2.0625p PD=33.25u AS=2.0625p PS=33.25u
MMOSFET_P_8 N_3 N_1 Vdd Vdd PMOS L=50n W=16.5u AD=2.0625p PD=33.25u AS=2.0625p PS=33.25u
MMOSFET_P_9 N_15 N_13 Vdd Vdd PMOS L=50n W=16.5u AD=2.0625p PD=33.25u AS=2.0625p PS=33.25u
CCapacitor_10 N_36 Gnd 0.034pF
CCapacitor_11 N_34 Gnd 0.034pF
CCapacitor_12 N_42 Gnd 0.034pF
CCapacitor_13 N_40 Gnd 0.034pF
CCapacitor_14 N_1 Gnd 0.034pF
CCapacitor_15 N_3 Gnd 0.034pF
CCapacitor_16 N_13 Gnd 0.034pF
CCapacitor_17 N_15 Gnd 0.034pF
CCapacitor_18 N_17 Gnd 0.034pF
CCapacitor_19 N_20 Gnd 0.034pF
CCapacitor_20 N_21 Gnd 0.034pF
CCapacitor_21 N_25 Gnd 0.034pF
CCapacitor_22 Out Gnd 0.034pF
MMOSFET_N_1 N_2 In Gnd Gnd NMOS L=50n W=5.5u AD=0.6875p PD=11.25u AS=0.6875p PS=11.25u

MMOSFET_N_2 N_10 N_12 Gnd Gnd NMOS L=50n W=5.5u AD=0.6875p PD=11.25u AS=0.6875p PS=11.25u
MMOSFET_N_3 N_16 N_18 Gnd Gnd NMOS L=50n W=5.5u AD=0.6875p PD=11.25u AS=0.6875p PS=11.25u
MMOSFET_N_4 N_22 N_24 Gnd Gnd NMOS L=50n W=5.5u AD=0.6875p PD=11.25u AS=0.6875p PS=11.25u
MMOSFET_N_5 N_28 N_30 Gnd Gnd NMOS L=50n W=5.5u AD=0.6875p PD=11.25u AS=0.6875p PS=11.25u
MMOSFET_N_6 N_34 N_36 Gnd Gnd NMOS L=50n W=5.5u AD=0.6875p PD=11.25u AS=0.6875p PS=11.25u
MMOSFET_N_7 N_40 N_42 Gnd Gnd NMOS L=50n W=5.5u AD=0.6875p PD=11.25u AS=0.6875p PS=11.25u
MMOSFET_N_8 N_3 N_1 Gnd Gnd NMOS L=50n W=5.5u AD=0.6875p PD=11.25u AS=0.6875p PS=11.25u
MMOSFET_N_9 N_15 N_13 Gnd Gnd NMOS L=50n W=5.5u AD=0.6875p PD=11.25u AS=0.6875p PS=11.25u
MMOSFET_P_10 N_20 N_17 Vdd Vdd PMOS L=50n W=16.5u AD=2.0625p PD=33.25u AS=2.0625p PS=33.25u
MMOSFET_P_11 N_25 N_21 Vdd Vdd PMOS L=50n W=16.5u AD=2.0625p PD=33.25u AS=2.0625p PS=33.25u
CCapacitor_1 N_2 Gnd 0.034pF
CCapacitor_2 N_12 Gnd 0.034pF
CCapacitor_3 N_10 Gnd 0.034pF
CCapacitor_4 N_18 Gnd 0.034pF
CCapacitor_5 N_16 Gnd 0.034pF
CCapacitor_23 Out Gnd 50fF

A.4.1 SPICE file for a Copper interconnect

CCapacitor_6 N_24 Gnd 0.018pF
CCapacitor_7 N_22 Gnd 0.018pF
CCapacitor_8 N_30 Gnd 0.018pF
RResistor_1 N_2 N_4 97 TC=0.0, 0.0
CCapacitor_9 N_28 Gnd 0.018pF
RResistor_2 N_10 N_5 97 TC=0.0, 0.0
RResistor_3 N_16 N_6 97 TC=0.0, 0.0
RResistor_4 N_22 N_7 97 TC=0.0, 0.0
RResistor_5 N_28 N_8 97 TC=0.0, 0.0
RResistor_6 N_34 N_9 97 TC=0.0, 0.0
RResistor_7 N_40 N_11 97 TC=0.0, 0.0
RResistor_8 N_3 N_14 97 TC=0.0, 0.0
RResistor_9 N_15 N_19 97 TC=0.0, 0.0
LInductor_1 N_4 N_12 158p
LInductor_2 N_5 N_18 158p
LInductor_3 N_6 N_24 158p
LInductor_4 N_7 N_30 158p

LInductor_5 N_8 N_36 158p
MMOSFET_N_10 N_20 N_17 Gnd Gnd NMOS L=50n W=5.5u AD=0.6875p PD=11.25u AS=0.6875p PS=11.25u
LInductor_6 N_9 N_42 158p
MMOSFET_N_11 N_25 N_21 Gnd Gnd NMOS L=50n W=5.5u AD=0.6875p PD=11.25u AS=0.6875p PS=11.25u
LInductor_7 N_11 N_1 158p
LInductor_8 N_14 N_13 158p
LInductor_9 N_19 N_17 158p
RResistor_10 N_20 N_23 97 TC=0.0, 0.0
RResistor_11 N_25 N_26 97 TC=0.0, 0.0
LInductor_10 N_23 N_21 158p
LInductor_11 N_26 Out 158p
MMOSFET_P_1 N_2 In Vdd Vdd PMOS L=50n W=16.5u AD=2.0625p PD=33.25u AS=2.0625p PS=33.25u
MMOSFET_P_2 N_10 N_12 Vdd Vdd PMOS L=50n W=16.5u AD=2.0625p PD=33.25u AS=2.0625p PS=33.25u
MMOSFET_P_3 N_16 N_18 Vdd Vdd PMOS L=50n W=16.5u AD=2.0625p PD=33.25u AS=2.0625p PS=33.25u
MMOSFET_P_4 N_22 N_24 Vdd Vdd PMOS L=50n W=16.5u AD=2.0625p PD=33.25u AS=2.0625p PS=33.25u
MMOSFET_P_5 N_28 N_30 Vdd Vdd PMOS L=50n W=16.5u AD=2.0625p PD=33.25u AS=2.0625p PS=33.25u
MMOSFET_P_6 N_34 N_36 Vdd Vdd PMOS L=50n W=16.5u AD=2.0625p PD=33.25u AS=2.0625p PS=33.25u
MMOSFET_P_7 N_40 N_42 Vdd Vdd PMOS L=50n W=16.5u AD=2.0625p PD=33.25u AS=2.0625p PS=33.25u
MMOSFET_P_8 N_3 N_1 Vdd Vdd PMOS L=50n W=16.5u AD=2.0625p PD=33.25u AS=2.0625p PS=33.25u
MMOSFET_P_9 N_15 N_13 Vdd Vdd PMOS L=50n W=16.5u AD=2.0625p PD=33.25u AS=2.0625p PS=33.25u
CCapacitor_10 N_36 Gnd 0.018pF
CCapacitor_11 N_34 Gnd 0.018pF
CCapacitor_12 N_42 Gnd 0.018pF
CCapacitor_13 N_40 Gnd 0.018pF
CCapacitor_14 N_1 Gnd 0.018pF
CCapacitor_15 N_3 Gnd 0.018pF
CCapacitor_16 N_13 Gnd 0.018pF
CCapacitor_17 N_15 Gnd 0.018pF
CCapacitor_18 N_17 Gnd 0.018pF
CCapacitor_19 N_20 Gnd 0.018pF
CCapacitor_20 N_21 Gnd 0.018pF
CCapacitor_21 N_25 Gnd 0.018pF
CCapacitor_22 Out Gnd 0.018pF
MMOSFET_N_1 N_2 In Gnd Gnd NMOS L=50n W=5.5u AD=0.6875p PD=11.25u AS=0.6875p PS=11.25u

```
MMOSFET_N_2 N_10 N_12 Gnd Gnd NMOS L=50n W=5.5u AD=0.6875p PD=11.25u
AS=0.6875p PS=11.25u
MMOSFET_N_3 N_16 N_18 Gnd Gnd NMOS L=50n W=5.5u AD=0.6875p PD=11.25u
AS=0.6875p PS=11.25u
MMOSFET_N_4 N_22 N_24 Gnd Gnd NMOS L=50n W=5.5u AD=0.6875p PD=11.25u
AS=0.6875p PS=11.25u
MMOSFET_N_5 N_28 N_30 Gnd Gnd NMOS L=50n W=5.5u AD=0.6875p PD=11.25u
AS=0.6875p PS=11.25u
MMOSFET_N_6 N_34 N_36 Gnd Gnd NMOS L=50n W=5.5u AD=0.6875p PD=11.25u
AS=0.6875p PS=11.25u
MMOSFET_N_7 N_40 N_42 Gnd Gnd NMOS L=50n W=5.5u AD=0.6875p PD=11.25u
AS=0.6875p PS=11.25u
MMOSFET_N_8 N_3 N_1 Gnd Gnd NMOS L=50n W=5.5u AD=0.6875p PD=11.25u
AS=0.6875p PS=11.25u
MMOSFET_N_9 N_15 N_13 Gnd Gnd NMOS L=50n W=5.5u AD=0.6875p PD=11.25u
AS=0.6875p PS=11.25u
MMOSFET_P_10 N_20 N_17 Vdd Vdd PMOS L=50n W=16.5u AD=2.0625p PD=33.25u
AS=2.0625p PS=33.25u
MMOSFET_P_11 N_25 N_21 Vdd Vdd PMOS L=50n W=16.5u AD=2.0625p PD=33.25u
AS=2.0625p PS=33.25u
CCapacitor_1 N_2 Gnd 0.018pF
CCapacitor_2 N_12 Gnd 0.018pF
CCapacitor_3 N_10 Gnd 0.018pF
CCapacitor_4 N_18 Gnd 0.018pF
CCapacitor_5 N_16 Gnd 0.018pF
CCapacitor_23 Out Gnd 50fF
Vdd Vdd Gnd 1V
VIn In Gnd PULSE (0 1 0 .1n .1n 5n 10n)
.tran .1n 60ns
.print V(In) V(Out)

.end
```

APPENDIX B

B.1 T-Spice 12 — Simulation commands

1 .ac

Syntax

.ac list f1 f2 …fn [sweep swinfo] [analysisname=name]

2 .acmodel

Syntax

.acmodel [output file] { [device [[,] device ...]]}

3 .dc

Syntax

.dc swinfo [[sweep] swinfo [[sweep] swinfo]]

4 .end

Syntax

.end [comment]

5 .include

Syntax

.include filename

filename The file to be included. It must exist in the current directory or in the T-Spice search path.

6 .lib

Syntax

Library File Format I:

The first T-Spice library file format is a sequence of library sections. Each library section begins with a .lib command and ends with a .endl command. The .lib command assigns a name to each section.

8 .model

Syntax

.model modelname type [level=L][parameter=value [parameter=value [...]]] [ako: akomodel]

type is one of the following:

modelname Model name.

type Device type (see below).

L Model level, required for device models with multiple levels.

Parameter The parameter list is predefined for each standard device model.

c Capacitor

Csw Current-controlled switch element.

nmos N-type MOSFET.

9 .op

Syntax

.op [noprint]

noprint Turns off automatic .op output.

10 .param

Syntax

.param funcname([arg1 [, arg2 [, arg3 [...]]]])='body'

parameter Parameter name.

funcname The name of the user function, which may not be the same as a built in.

11 .print

Syntax

.print [mode] ["filename"] [arguments]

filename Output filename. Must be enclosed by double quotes.

arguments Information to be printed (see below). arguments may include valid expressions involving other arguments or global parameters.

12 .probe

Syntax

.probe [mode] ["filename"] [arguments]

mode Analysis type (see below). If mode is omitted, the .probe command applies to all analysis types.

ac Print results from AC analysis.

13 .step

Syntax

.step sweep [[sweep] sweep [[sweep] sweep]]

14 .tf

Syntax

.tf arguments source

arguments Any arguments appropriate for the ".print" (page 106) dc command.

source Voltage or current input source.

15 .tran

Syntax

.tran[/mode] S L [start=A] [UIC] [sweep sweep]

B.2 Calculation of interconnect parasitics for 45nm

The parameters used in calculation of CNT and Copper parasitics are given below-

	Copper	CNT
length (L) of interconnect	1000 um (global)	1000 um (global)
thickness (H) of global interconnect	235.75 nm	235.75 nm
resistivity (relative)	2.45 Ω-cm	-
oxide thickness (t_{OX})	215.25 nm	215.25 nm

ε_{OX} (relative)	2.45	2.45

Based on these parameters, the following value of parasitic R, C, L were calculated.

Table. B.1 CNT and Cu delay parasitics

Repeaters	0					
	Cu			CNT		
	R	C	L	R	C	L
w:s						
1.5:0.5	1594.70	0.15	1753.31	208.68	0.61	0.04
01:01	1063.13	0.39	1736.00	137.76	0.76	0.02
0.5:1.5	531.56	0.41	1717.55	66.84	0.88	0.01

Repeaters	2					
	Cu			CNT		
	R	C	L	R	C	L
w:s						
1.5:0.5	531.565	0.0245	584.435	69.561	0.101	0.0127
01:01	354.377	0.0655	578.667	45.92	0.126	0.0083
0.5:1.5	177.187	0.068	572.518	22.28	0.1475	0.004

Repeaters	4					
	Cu			CNT		
	R	C	L	R	C	L
w:s						
1.5:0.5	318.939	0.0147	350.661	41.737	0.0606	0.0076
01:01	212.626	0.0393	347.2	27.552	0.0756	0.005
0.5:1.5	106.312	0.0408	343.511	13.368	0.0885	0.0024

Repeaters	6					
	Cu			CNT		
	R	C	L	R	C	L
w:s						
1.5:0.5	227.814	0.0105	250.472	29.812	0.0433	0.0054
01:01	151.876	0.0281	248	19.68	0.054	0.0036
0.5:1.5	75.9375	0.0291	245.365	9.5484	0.0632	0.0017

Repeaters	8					
	Cu			CNT		
	R	C	L	R	C	L
w:s						
1.5:0.5	177.188	0.0082	194.812	23.187	0.0337	0.0042
01:01	118.126	0.0218	192.889	15.307	0.042	0.0028
0.5:1.5	59.0625	0.0227	190.839	7.4266	0.0492	0.0013

Repeaters	10					
	Cu			CNT		
	R	C	L	R	C	L
w:s						
1.5:0.5	144.972	0.0067	159.391	18.971	0.0275	0.0035
01:01	96.6482	0.0179	157.818	12.524	0.0344	0.0023
0.5:1.5	48.3239	0.0185	156.141	6.0763	0.0402	0.0011

Repeaters	12					
	Cu			CNT		
	R	C	L	R	C	L
w:s						
1.5:0.5	122.669	0.0057	134.87	16.053	0.0233	0.0029
01:01	81.7792	0.0151	133.538	10.597	0.0291	0.0019
0.5:1.5	40.8894	0.0157	132.119	5.1415	0.034	0.0009

Repeaters	14					
	Cu			CNT		
	R	C	L	R	C	L
w:s						
1.5:0.5	106.313	0.0049	116.887	13.912	0.0202	0.0025
01:01	70.8753	0.0131	115.733	9.184	0.0252	0.0017
0.5:1.5	35.4375	0.0136	114.504	4.4559	0.0295	0.0008

Repeaters	16					
	Cu			CNT		
	R	C	L	R	C	L
w:s						
1.5:0.5	93.8056	0.0043	103.136	12.276	0.0178	0.0022
01:01	62.5371	0.0116	102.118	8.1035	0.0222	0.0015
0.5:1.5	31.2684	0.012	101.033	3.9317	0.026	0.0007

B.3 Simulated values of CNT and Copper delay

B.3.1 Variation of Repeater width

Simulated values of CNT and Copper delay were found using SPICE Simulation for 45 nm. The comparative study is shown in Chapter 5.

Table. B.2 CNT and Cu delay variation w.r.t. number of repeaters (for $(W/L)_{driver}$= 40)

Repeaters	Delay Cu	Delay CNT	Delay CNT/Cu
2	0.297	0.335	1.13
4	0.2645	0.32	1.21
6	0.2605	0.313	1.20
8	0.2695	0.316	1.17
10	0.278	0.332	1.19
12	0.287	0.348	1.21
14	0.305	0.359	1.18
16	0.3295	0.368	1.12

Table. B.3 CNT and Cu delay variation w.r.t. number of repeaters (for $(W/L)_{driver}$= 80)

Repeaters	Delay Cu	Delay CNT	Delay CNT/Cu
2	0.2225	0.1795	0.81
4	0.1905	0.180	0.94
6	0.178	0.189	1.06
8	0.194	0.203	1.05
10	0.2025	0.212	1.05
12	0.215	0.227	1.06
14	0.226	0.245	1.08
16	0.2455	0.2595	1.06

Table. B.4 CNT and Cu delay variation w.r.t. number of repeaters (for $(W/L)_{driver}$= 100)

Repeaters	Delay Cu	Delay CNT	Delay CNT/Cu
2	0.216	0.1525	0.71
4	0.174	0.153	0.88
6	0.1725	0.167	0.97
8	0.182	0.177	0.97
10	0.188	0.192	1.02
12	0.201	0.208	1.03

14	0.217	0.222	1.02

Table. B.5 CNT and Cu delay variation w.r.t. number of repeaters (for $(W/L)_{driver}$= 110)

Repeaters	Delay Cu	Delay CNT	Delay CNT/Cu
2	0.206	0.1355	0.66
4	0.1715	0.140	0.81
6	0.17	0.153	0.90
8	0.178	0.163	0.91
10	0.1885	0.181	0.96
12	0.2035	0.194	0.95
14	0.2195	0.209	0.95
16	0.2335	0.23	0.99

Table. B.6 CNT and Cu delay variation w.r.t. number of repeaters (for $(W/L)_{driver}$= 120)

Repeaters	Delay Cu	Delay CNT	Delay CNT/Cu
2	0.199	0.1265	0.64
4	0.16	0.134	0.84
6	0.1625	0.145	0.89
8	0.1755	0.157	0.89
10	0.183	0.173	0.94
12	0.1915	0.1875	0.98
14	0.204	0.206	1.01
16	0.2315	0.223	0.96

B.3.2 Variation of Pitch

Table. B.7 CNT and Cu delay variation w.r.t. number of repeaters (for w:s = 1:1)

Repeaters	Delay Cu	Delay CNT	Delay CNT/Cu
2	0.206	0.1355	0.66
4	0.1715	0.140	0.81
6	0.17	0.153	0.90
8	0.178	0.163	0.91
10	0.1885	0.181	0.96
12	0.2035	0.194	0.95
14	0.2195	0.209	0.95
16	0.2335	0.23	0.99

Table. B.2 CNT and Cu delay variation w.r.t. number of repeaters (for w:s = 0.5:1.5)

Repeaters	Delay Cu	Delay CNT	Delay CNT/Cu
2	0.1505	0.142	0.94
4	0.1305	0.145	1.11
6	0.14	0.161	1.15
8	0.159	0.172	1.08
10	0.1685	0.185	1.10
12	0.184	0.2035	1.11
14	0.196	0.214	1.09
16	0.2135	0.2345	1.10

Table. B.2 CNT and Cu delay variation w.r.t. number of repeaters (for w:s = 1.5:0.5)

Repeaters	Delay Cu	Delay CNT	Delay CNT/Cu
2	0.1585	0.115	0.73
4	0.146	0.120	0.82
6	0.1465	0.128	0.87
8	0.158	0.142	0.90
10	0.172	0.160	0.93
12	0.186	0.1705	0.92
14	0.202	0.189	0.94
16	0.22	0.2085	0.95