Thesis

On

"Design of a Low Power, 8- Bit, 5MS/s Digital to Analog Converter for Successive Approximation ADC"

Submitted in the partial fulfillment for the
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In
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Submitted by:

Amandeep Kaur

Roll No. 601061003

Under the supervision of:

Dr. Alpana Agarwal

Associate Professor

Department of Electronics & Communication Engineering

Thapar University, Patiala-147004 (Punjab)

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DECLARATION

I hereby certify that the work, which is being presented in this thesis entitled **"Design of a Low Power, 8- Bit, 5MS/s Digital to Analog Converter for Successive Approximation ADC"** , in partial fulfillment of the requirement for the award of Master of Technology in VLSI Design at Thapar University, Patiala is an authentic record of my own work carried out under the supervision of Dr. Alpana Agarwal, Associate Professor, ECED and refers other researcher's work which are duly listed in reference section.

The matter embodied in this thesis has not been submitted for the award of any other degree of this or any other university.

Amandeep Kaur

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It is certified that the above statement made by the candidate is correct to the best of my knowledge and belief.

08/06/12

Dr. Alpana Agarwal

Associate Professor

Countersigned by:

Head

ECE Department

Dean of Academic Affairs

Thapar University, Patiala

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ABSTRACT

Digital-to-Analog converters (DACs) help bridge the digital domain with the everyday analog world. A DAC occupying small area capable of high resolution is of use in many applications. A monotonic DAC always has an increasing analog output with increasing digital input. This behavior is essential in many applications. These applications can tolerate non-linearities but cannot tolerate non-monotonicity. In this thesis, a simple switched capacitor DAC is presented that exhibits monotonicity while occupying a small area. The proposed DAC starts its conversion from the MSB instead of the traditional approach of starting from LSB making it suitable for use in cyclic or successive approximation analog-to-digital converters (ADCs). For an N-bit digital input sequence, the proposed DAC starts conversion with the MSB and takes N cycles to finish conversion. The DAC samples the reference voltage only once and transfers appropriate charge to an output capacitor. Some issues relevant to the design and their possible solutions are presented. The DAC is designed for a resolution of 8-bit. Sampling speed is chosen to be 5MS/s and the main emphasis is on low power. This DAC consumes power in the order of microwatts(μW), compare with previous DACs which consume more power, generally in the order of milliwatts. Switched capacitor DAC is designed and simulated in Cadence® Virtuoso Analog Design Environment using UMC 180nm technology to validate its performance. Layouts of op amp and DAC are made in Cadence® Virtuoso Layout XL Environment. The post layout and process corner simulations with 1.8V supply voltage have been done for the output DAC characteristics and power dissipation.

The output 8-bits along with power dissipation of 493.8 μW have been achieved.

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ABRREVIATIONS

SAR:	**Successive Approximation Register**
ADC:	**Analog-to-Digital Converter**
DAC:	**Digital to Analog Converter**
CMOS:	**Complementary Metal Oxide Semiconductor**
FF:	**Fast NMOS Fast PMOS**
FS:	**Fast NMOS Slow PMOS**
ICMR:	**Input Common Mode Range**
MOS:	**Metal Oxide Semiconductor**
MOSFET:	**Metal Oxide Semiconductor Field Effect Transistor**
NMOS:	**Negative-Channel Metal-Oxide Semiconductor**
PMOS:	**Positive-Channel Metal-Oxide Semiconductor**
SS:	**Slow NMOS Slow PMOS**
SF:	**Slow NMOS Fast PMOS**
TT:	**Typical NMOS Typical PMOS**
VLSI:	**Very Large Scale Integration.**

CHAPTER 1

INTRODUCTION

1.1 Background

Most of real world signals are analog in nature, they are continuous-time, continuous-valued signals. Compared to analog signals, digital signals have the following advantages:

a) It is immune to electrical noise.

b) It can be manipulated easily (DSP processing).

c) It is easy to store.

d) It is easy to copy and transfer.

Thus, there is a trend to move signal processing from the analog domain to the digital one such as digital signal processing, which, besides above advantages allow for a higher level of accuracy, provides savings in power consumption and silicon area, increases robustness, speeds up the design process, brings flexibility and programmability, and increases the possibilities for design reuse. Because of above benefits of working in digital domain, there is a need to convert the analog real world signals to digital discrete-time, discrete-value signals. Analog to digital converters (ADC) convert the analog signals to digital signals for DSP processors to process. Although the analog input signal can be represented in several domains (for example voltage, current, charge), input is taken in the voltage domain in the present work. Also, digital codes are described in the binary domain. The analog input signal *is* V_{in}(t) defined for each moment in time, and it is supposed that it can take any value within a certain range. To represent this signal in a limited amount of digital data, the input signal is sampled on fixed time intervals and quantized in the amplitude domain. The sample frequency f_s of the converter determines the time interval T_s between two consecutive sample moments, according to$f_s = \frac{1}{T_s}$.

1.2 Successive Approximation ADC

Successive Approximation Register ADC represents the majority of the ADC market for medium to high resolution. This topology requires just one comparator; an N-bit SAR ADC will require N comparison periods and will not be ready for the next conversion until the current one is complete. This topology is expected to allow the lowest power dissipation, but

at the same time paying the price with the slowest sampling rate.

The successive approximation ADC is by far the most popular architecture for data-acquisition applications, especially when multiple channels require input multiplexing. The overall accuracy and linearity of the SAR ADC are determined primarily by the internal DAC's characteristics. Switched-capacitor (or charge-redistribution) DACs have become popular in newer CMOS-based SAR ADCs, as their accuracy and linearity are primarily determined by high-accuracy photolithography. Among the existing ADC architectures, successive approximation (SA) ADC is widely known for processing accurate and medium-speed conversion. By nature, SA ADC is preferred for biomedical applications because of its low power consumption. However, though the low-power characteristic guarantees long-term use, it constrains the circuits' performance, including required speed and signal-to-noise ratio (SNR). Fortunately, the bio-signals are low-frequency by nature. The required specifications are not as strict in such biomedical systems. Hence, the degraded performance due to the low-power design considerations for analog circuits is not a critical point for the proposed SA ADC Design. The bio-signals' bandwidth is usually below 10 kHz, thus an ADC with high operation speed is not required.

1.2.1 Building blocks

Following are the building blocks of SAR ADC:

Sample-and-Hold Stage (S/H)

Digital-to-Analog Converter (DAC)

Comparator

Successive Approximation Register (SAR)

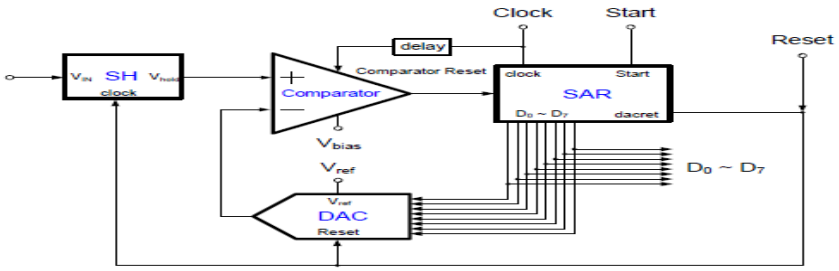


Figure 1.1 SAR ADC Building blocks [34].

1.2.2 Basic principle

The basic functionality of a SAR ADC is very simple. The analog input voltage V_i is sampled by the Sampled & Hold block. Here the output of sampled and hold circuit is represented by$V_{in}{}^{*}$. To implement the binary search algorithm, the N-bit register is first set to midscale setting the MSB to '1' and all other bits to '0'. This forces the DAC output, V_{dac}, to be half of the reference voltage,$\frac{V_{ref}}{2}$. V_i is then compared with V_{dac}, if V_i is greater than V_{dac}, the comparator output is logic 1 and MSB of N-bit register remains at 1. Conversely, if V_i is less thanV_{dac}, the comparator output is logic 0 and the MSB of the register is cleared to 0. The SAR control logic then moves to the next bit down, forces that bit high, and does another comparison. The sequence continues all the way down to the LSB. Once this is done, the conversion is completed, and the N-bit digital word is available in the register and the MSB of the N-bit register remains at 1. SAR ADC works with two different clock frequencies. The first clock is an input of the chip, and its frequency, f_i, is the one at which the internal circuit works. The second clock drives the Sample and Hold in order to sample the analog input value. This second clock is internally created by a frequency divider; it should be X times slower the first one, where X is the number of comparison periods needed from the control logic to complete a conversion. The conversion rate is determined by this second clock, an N-bit SAR ADC will require minimum N periods and will not be ready for the next conversion until the current one is complete.

As increased numbers of ADCs are being integrated with complex digital circuitry on a single chip, such as bio-systems, in such systems on chips (SOCs), the requirements for energy consumption are particularly stringent because majority of these systems are portable devices. The power consumption must remain as low as possible for long term use. Compared with other types of ADC, the SA ADC's structure is not complicated,. The converter consists of an S/H circuit, a comparator, a successive approximation register (SAR) controller, and an 8- bit DAC. Using a binary searching algorithm, the input sample voltage can be successively approximated by the DAC output voltage. For an N-bit SA ADC, N cycles are required to convert the analog signals into digital codes. Obviously, the DAC dominates the accuracy and the speed of the SA ADC. The successive approximation register is initialized so that the most significant bit (MSB) is equal to a digital 1. This code is fed

into the DAC, which then supplies the analog equivalent of this digital code $\frac{V_{ref}}{2}$ into the comparator circuit for comparison with the sampled input voltage. If this analog voltage exceeds V_{in} , the comparator causes the SAR to reset this bit; otherwise, the bit is left a 1. Then the next bit is set to 1 and the same test is done, continuing this binary search until every bit in the SAR has been tested. The resulting code is the digital approximation of the sampled input voltage and is finally output by the DAC at the end of the conversion (EOC).

1.3 Requirement of DAC

The operation of communication and entertainment systems is increasingly based on digital signal processing (DSP), while the physical signals needed to be handled at the input and output nodes of these systems remain continuous time analog ones. Hence, such a system typically needs an analog-to-digital converter (ADC) at its input end, and a digital- to-analog converter (DAC) at its output end. Digital-to-Analog converters (DACs) help bridge the digital domain with the everyday analog world. A DAC occupying small area capable of high resolution is of use in many applications. A monotonic DAC always has an increasing analog output with increasing digital input. This behavior is essential in many applications. These applications can tolerate non-linearities but cannot tolerate non-monotonicity. Digital to analog converters operating at moderate speeds and moderate resolutions are used in many applications. These DACs often have a small footprint and consume low power. In this work on Successive Approximation Analog-to-Digital Converters, a new Digital-to-Analog Converter is introduced. This new converter is based on charge redistribution and it can easily be operated at very high sampling rates. Furthermore the matching accuracy of integrated capacitors is excellent. The key issues for such a DAC are the integral non linearity (INL) and the power consumption. Switched Capacitor DACs (SCDAC) is well suited to meet these requirements.

1.4 DAC specifications

A block diagram of a DAC is shown in Fig. 1.2. Here an N-bit digital word is mapped into a single analog voltage. Typically, the output of the DAC is a voltage that is some fraction of a reference voltage (or current), such that

$$V_{out} = KV_{ref}D \tag{1.1}$$

where K is a scaling factor and the digital word D is given as

$$D = \frac{D_0}{2^1} + \frac{D_1}{2^2} + \frac{D_2}{2^3} + \cdots + \frac{D_{N-1}}{2^N} \quad (1.2)$$

N is the total number of bits of the digital word and D_{i-1} is the ith-bit coefficient and is either 0 or 1. Therefore, the output of a DAC can be expressed by combining equations (1.1) and (1.2) to get

$$V_{out} = KV_{ref}\left(\frac{D_0}{2^1} + \frac{D_1}{2^2} + \frac{D_2}{2^3} \ldots\ldots + \frac{D_{N-1}}{2^N}\right) \quad (1.3)$$

where V_{out} is the analog voltage output, V_{ref} is the reference voltage, and K is the scaling factor and the input word, D, that is N bits wide.

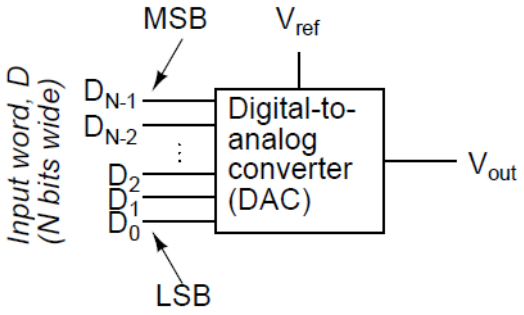


Figure 1.2 Block diagram of Digital to Analog Converter [2].

1.4.1 Transfer curve

By plotting the input word, D, versus V_{out} as D is incremented from 000 to 111 for 3 bits, the transfer curve seen in Fig. 1.3 would be generated. The y-axis has been normalized to V_{ref}. Some important characteristics need to be discussed here. First, notice that the transfer curve is not continuous. Since the input is a digital signal, which is inherently discrete, the input signal can only have eight values that must correspondingly produce eight output voltages. If a straight line connected each of the output values, the slope of the line would ideally be one increment/input code value. Also note that the maximum value of the output is 7/8. Since the case where D = 000 has to result in an analog voltage of 0V, and a 3-bit DAC has eight possible analog output voltages, then the analog output will increase from 0V to only $7/8V_{ref}$. This maximum analog output voltage that can be generated is known as full-scale voltage, V_{FS}, and can be generalized to any N-bit DAC as

$$V_{FS} = \frac{2^N - 1}{2^N} . V_{ref} \quad (1.4)$$

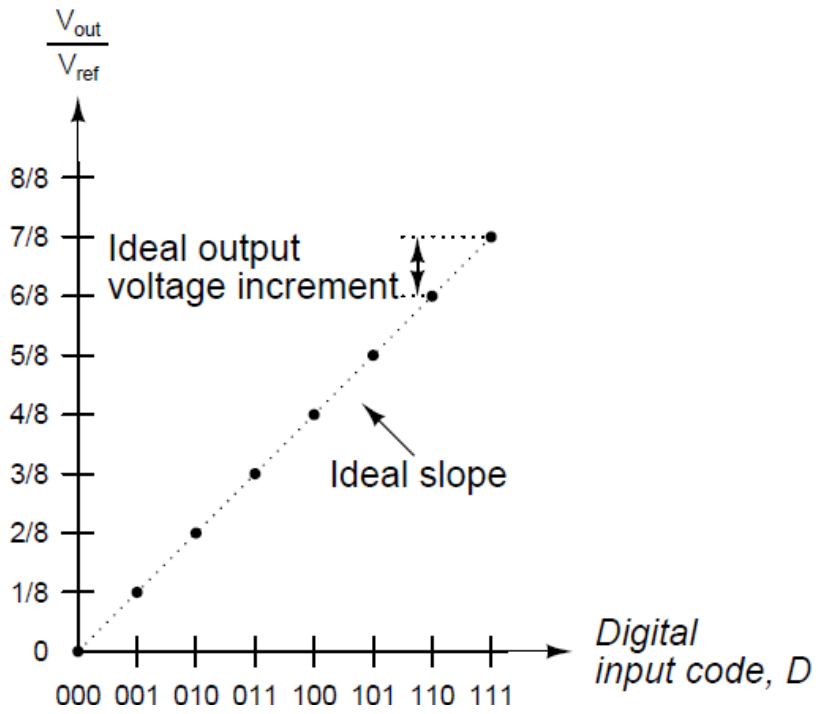


Figure 1.3 Ideal transfer curves for a 3-bit DAC [2].

1.4.2 Least Significant Bit (LSB)

The least significant bit (LSB) refers to the rightmost bit in the digital input word. The LSB defines the smallest possible change in the analog output voltage. The LSB will always be denoted as D0. One LSB can be defined as

$$1\text{LSB} = \frac{V_{ref}}{2^N} \tag{1.5}$$

1.4.3 Most significant Bit (MSB)

The most significant bit (MSB) refers to the leftmost bit of the digital word, D. Generalizing to the N-bit DAC, the MSB would be denoted as D_{N-1}. The MSB causes the output to change by $\frac{V_{ref}}{2}$.

1.4.4 Resolution

The term resolution describes the smallest change in the analog output with respect to the value of the reference voltage V_{ref}. Resolution is typically given in terms of bits and represents the number of unique output voltage levels *.i.e.,* 2^N where N is the resolution.

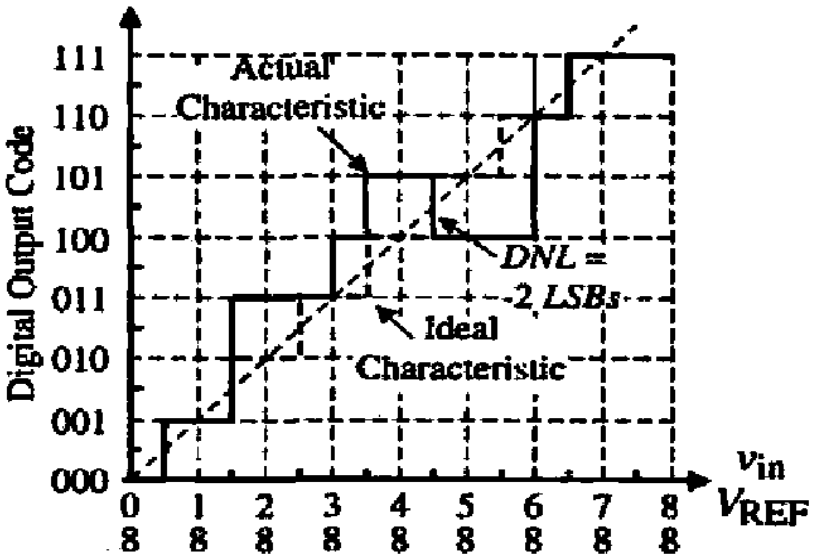
1.4.5 Differential nonlinearity

Non-ideal components cause the analog increments to differ from their ideal values. The

difference between the ideal and non-ideal values is known as differential nonlinearity, or DNL and is defined as

$$DNL = max\left|\frac{V(i+1)-V(i)}{V_{LSB}} - 1\right| \quad (1.6)$$

The DNL specification measures how well a DAC can generate uniform analog LSB multiples at its output. Generally, a DAC will have less than ±½LSB of DNL if it is to be N-bit accurate. If the DNL for a DAC is more than ±½LSB, then the DAC is said to be non-monotonic, which means that the analog output voltage does not always increase as the digital input code is incremented. A DAC should always exhibit monotonicity if it is to



function without error. DNL error is shown in Fig. 1.4.

Figure 1.4 DNL Error[2].

1.4.6 Integral Nonlinearity

Another important static characteristic of DACs is called integral nonlinearity (INL). It is defined as the difference between the data converter output values and a reference straight line drawn through the first and last output values. INL defines the linearity of the overall transfer curve and can be described as

$$INL = max\left|\frac{V(i)-i.V_{LSB}}{V_{LSB}}\right| \quad (1.7)$$

It is common practice to assume that a converter with N-bit resolution will have less than

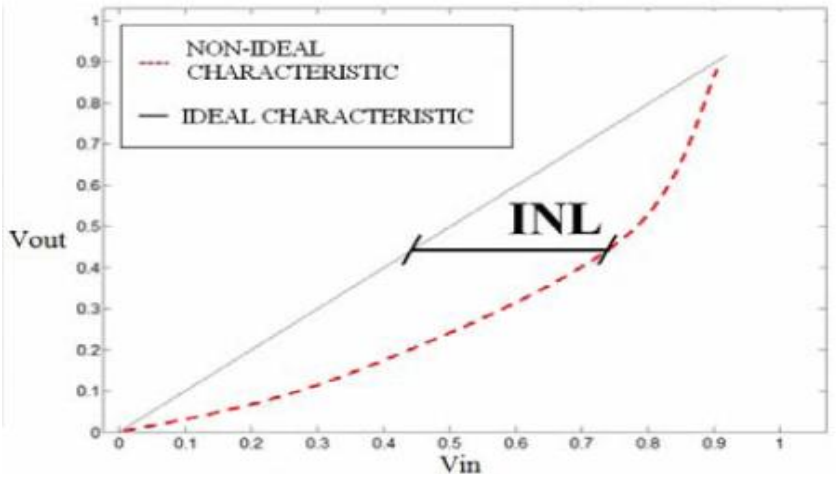


Figure 1.5 INL Error[2].

±½LSB of DNL and INL. INL Error is shown in Fig. 1.5.

1.4.7 Signal-to-Noise Ratio (SNR)

Signal-to-Noise Ratio (SNR) is defined as the ratio of the signal power to the noise at the analog output. In amplifier applications, this specification is typically measured using a sine wave input. For the DAC, a sampled sine wave is generated through an A/D. The SNR can reveal the true resolution of a data converter as the effective number of bits can be quantified mathematically.

$$\text{Error energy: } {e_{rms}}^2 = \frac{{V_{LSB}}^2}{12} \tag{1.8}$$

$$\text{Signal energy: } {s_{rms}}^2 = \frac{1}{T}\int_{t=0}^{t=T} A^2 \sin^2(\omega t)dt = \frac{A^2}{2} = \frac{2^{2N}{V_{LSB}}^2}{8} \tag{1.9}$$

$$SNR = \frac{\frac{2^{2N}{V_{LSB}}^2}{8}}{\frac{{V_{LSB}}^2}{12}} = \frac{3}{2}2^{2N} \approx 6.02.N + 1.76[dB] \tag{1.10}$$

1.4.8 Total harmonic Distortion (THD)

The total harmonic distortion is given by

$$THD = 10log\frac{{A_{2f}}^2+{A_{3f}}^2+{A_{4f}}^2+\cdots{A_{nf}}^2}{{A_{1f}}^2}\ [dB] \tag{1.11}$$

Five to ten harmonics are included in the THD, the rest is considered “noise”

1.4.9 Signal-to-Noise-and-Distortion (SINAD)

Signal-to-Noise-and-Distortion (SINAD) is the ratio of the root-mean-square (rms) signal amplitude to the mean value of the root-sum-square of all other spectral components, including harmonics, but excluding dc. SINAD is a good indication of the overall dynamic performance of a DAC because it includes all components which make up noise and distortion.

$$SINAD = \frac{S}{N+D} \tag{1.12}$$

1.4.10 Effective-Number-of-Bits (ENOB)

SINAD is often converted to effective-number-of-bits (ENOB) using the relationship for the theoretical SNR of an ideal N-bit DAC: SNR = 6.02N + 1.76[dB]. The equation is solved for N, and the value of SINAD is substituted for SNR:

$$ENOB = \frac{SINAD - 1.76dB}{6.02} \tag{1.13}$$

1.5 Types of DACs

The most common types of DACs are:

1.5.1 Oversampling DAC

Oversampling DACs such as the Sigma-Delta DAC use a pulse density conversion technique. The oversampling technique allows for the use of a lower resolution DAC internally. A simple 1-bit DAC is often chosen because the oversampled result is inherently linear. The DAC is driven with a pulse density modulated signal, created with the use of a low-pass filter, step nonlinearity (the actual 1-bit DAC), and negative feedback loop, in a technique called sigma-delta modulation. This results in an effective high-pass filter acting on the quantization (signal processing) noise, thus steering this noise out of the low frequencies of interest into the high frequencies of little interest, which is called noise shaping. The quantization noise at these high frequencies is removed or greatly attenuated by use of an analog low-pass filter at the output (sometimes a simple RC low-pass circuit is sufficient). Most very high resolution DACs (greater than 16 bits) are of this type due to its high linearity and low cost. Higher oversampling rates can either relax the specifications of the output low-pass filter or enable further suppression of quantization noise. Speeds of greater than 100 thousand samples per second (for example, 192kHz) and resolutions of 24

bits are attainable with Delta-Sigma DACs.

1.5.2 Binary Weighted DAC

The Binary Weighted DAC contains one resistor or current source for each bit of the DAC connected to a summing point. These precise voltages or currents sum to the correct output value. This is one of the fastest conversion methods but suffers from poor accuracy because of the high precision required for each individual voltage or current. Such high-precision resistors and current sources are expensive, so this type of converter is usually limited to 8-bit resolution or less. Binary weighted DAC is shown in Fig. 1.6.

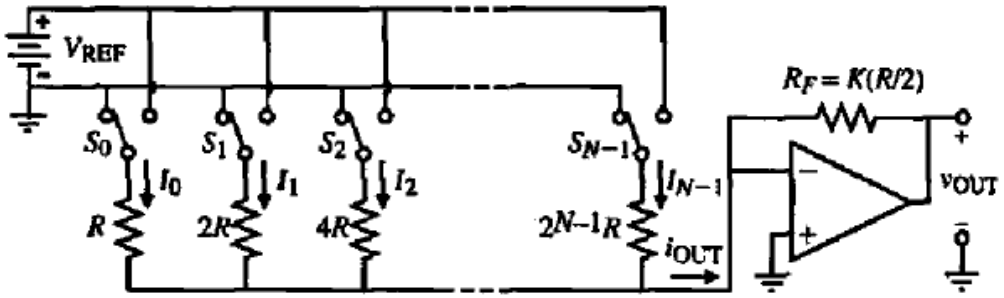


Figure 1.6 Binary-weighted resistor DAC implementation [2] .

The analog output voltage is expressed as

$$v_{out} = -K\left(\frac{b_0}{2^1} + \frac{b_1}{2^2} + \frac{b_2}{2^3} + \cdots + \frac{b_s}{2^N}\right)V_{REF} \tag{1.14}$$

1.5.3 R-2R Ladder DAC

This type of DAC is a binary weighted DAC that uses a repeating cascaded structure of resistor values R and 2R. This improves the precision due to the relative ease of producing equal valued matched resistors (or current sources). However, wide converters perform slowly due to increasingly large RC-constants for each added R-2R link. R-2R Ladder DAC is shown in Fig. 1.7.

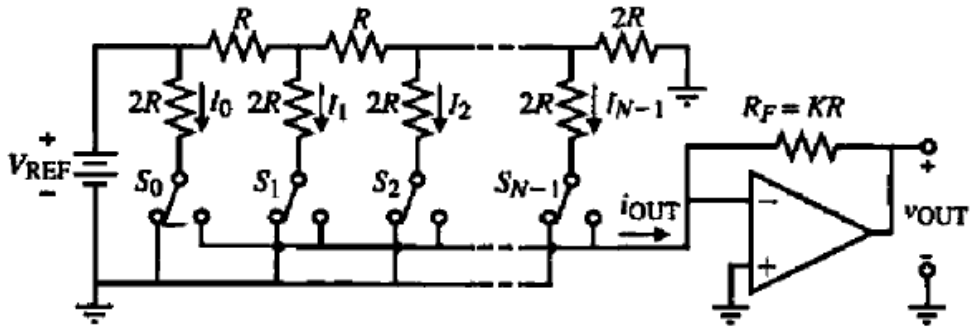


Figure 1.7 R-2R Ladders DAC [2].

1.5.4 Charge Scaling DAC

Charge scaling DACs operate by binarily dividing the total charge applied to a capacitor array. This process is implemented by using capacitors to attenuate the reference voltage. The configuration is extremely simple and is in effect a digitally controlled voltage attenuator. Another advantage of the charge scaling DAC is that it is compatible with switched capacitor circuits. Fig. 1.8 shows the general implementation of a charge scaling DAC. A two-phase, non-overlapping clock is used for this converter. Duringφ_1, the top and bottom plates of all capacitors in the array are grounded. Next, duringφ_2, the capacitors associated with bits that are 1 are connected to V_{REF} and those with bits that are 0 are connected to ground. The output of DAC is valid duringφ_2. The resulting situation can be described by equating the charge in the capacitors connected to $V_{REF}(C_{eq})$ to the charge in the total capacitors (C_{tot}). This is expressed as

$$V_{REF}C_{eq} = V_{REF}(b_0C + \frac{b_1}{2}C + \frac{b_2}{2^2}C + \cdots + \frac{b_{N-1}}{2^{N-1}}) = C_{tot}V_{OUT} = 2CV_{OUT} \quad (1.15)$$

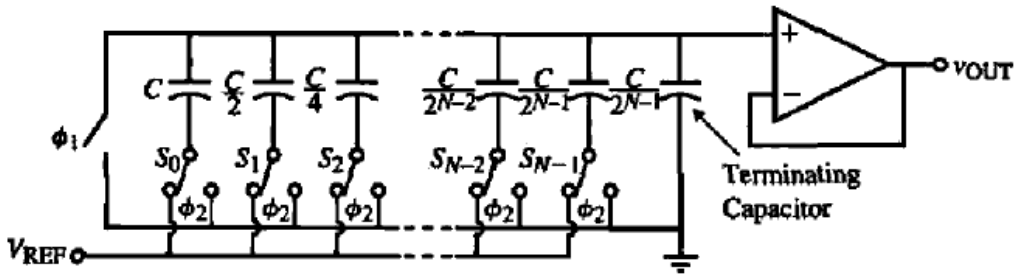


Figure 1.8 Charge scaling DAC [2].

1.5.5 Thermometer coded DAC

The thermometer coded DAC contains an equal resistor or current source segment for each possible value of DAC output. An 8-bit thermometer DAC would have 255 segments, and a 16-bit thermometer DAC would have 65,535 segments. This is perhaps the fastest and highest precision DAC architecture but at the expense of high cost. Conversion speeds of over 1 billion samples per second have been reached with this type of DAC. The advantage of a binary-weighted DAC is its simplicity, as no decoding logic is required. There are several major drawbacks, however, which are all associated with major bit transitions. At the mid-code transition (011 111 111 111 → 100 000 000 000), the most significant bit (MSB) capacitor needs to be matched to the sum of all the other capacitors to within ±½LSB. This is difficult to achieve. Because of statistical spread, such matching can never be guaranteed. Therefore this architecture is not guaranteed monotonic. Matching is an issue for all bit transitions, but the severity of the problem is proportional to the weight of the bit, resulting in a typical differential nonlinearity (DNL). Fig. 1.9 shows an example of a 3-bit thermometer-coded DAC. There are 2^3 = 8 unit capacitors. Each unit capacitor is connected to a switch controlled by the signal coming from the binary-to-thermometer decoder.

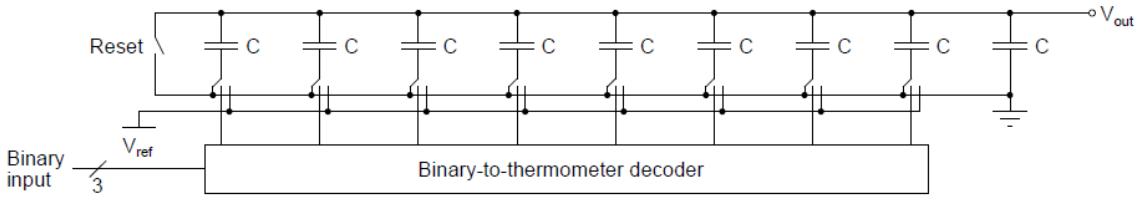


Figure 1.9 3-bit thermometer coded DAC.

When the digital input increases by 1LSB, one more capacitor is charged. The analog output is always increasing as the digital input increases. Hence, monotonicity is guaranteed using this architecture. In addition, there are several other advantages for a thermometer-coded DAC compared to its binary-weighted counterpart. First, the matching requirement is much relaxed: 50% matching of the unit capacitor is good enough for a DNL of 0.5 LSB. At the mid-code, a 1LSB transition (011 111 111 111 → 100 000 000 000), causes only one capacitor to charge as the digital input only increases by one. This greatly reduces the glitch problem. On top of that, glitches hardly contribute to nonlinearity in the thermometer coded

architectures. This is because the magnitude of a glitch is proportional to the number of switches that are actually switching. So for small steps, the glitch is small, and for a large step, the glitch is large. Since the number of switches that switch is proportional to the signal step between two consecutive clock cycles, the magnitude of the glitch is directly proportional to the amplitude of the signal step. Table 1.1 shows the conversion Table from decimal to binary to thermometer code.

Table 1.1 Conversion Table

Decimal	Binary			Thermometer Code						
	b_1	b_2	b_3	d_1	d_2	d_3	d_4	d_5	d_6	d_7
0	0	0	0	0	0	0	0	0	0	0
1	0	0	1	0	0	0	0	0	0	1
2	0	1	0	0	0	0	0	0	1	1
3	0	1	1	0	0	0	0	1	1	1
4	1	0	0	0	0	0	1	1	1	1
5	1	0	1	0	0	1	1	1	1	1
6	1	1	0	0	1	1	1	1	1	1
7	1	1	1	1	1	1	1	1	1	1

One major drawback of the thermometer coded DAC is area consumption, since for every LSB this architecture needs a capacitor, a switch, and a decoding circuit, as well as the binary to thermometer decoder.

1.5.6 Segmented DAC

The segmented DAC combines the thermometer coded principle for the most significant bits and the binary weighted principle for the least significant bits. In this way, a compromise is obtained between precision (by the use of the thermometer coded principle) and number of resistors or current sources (by the use of the binary weighted principle). The full binary weighted design means 0% segmentation; the full thermometer coded design means 100% segmentation.

1.5.7 Hybrid DAC

The hybrid DAC uses a combination of the above techniques in a single converter. Most DAC integrated circuits are of this type due to the difficulty of getting low cost, high speed

and high precision in one device.

1.5.8 Charge redistribution DAC

Shown in Fig. 1.10, charge redistribution DAC is a parallel array of binary-weighted capacitors, $2^N C$ in number. After initially being discharged, the digital signal switches each capacitor to either V_{REF} or ground, causing the output voltage,V_{out}, to be a function of the voltage division between the capacitors.

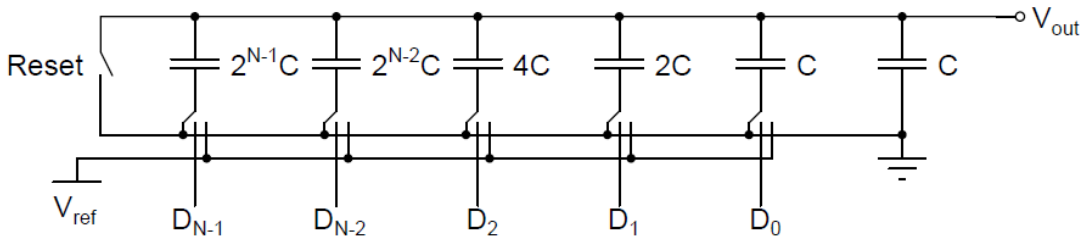


Figure 1.10 Charge Redistribution DAC [25]

The capacitor array totals$2^N C$. Therefore, if the MSB is high and the remaining bits are low, then a voltage divider occurs between the MSB capacitor and the rest of the array. The analog output voltage, V_{out}, becomes

$$V_{out} = V_{ref} \cdot \frac{2^{N-1}C}{(2^{N-1}+2^{N-2}+2^{N-3}+\cdots+4+2+1+1)C} = V_{ref} \cdot \frac{2^{N-1}C}{2^N C} = \frac{V_{ref}}{2} \tag{1.16}$$

which confirms the fact that the MSB changes the output of a DAC by ½Vref. Fig. 1.11 shows the equivalent circuit under this condition.

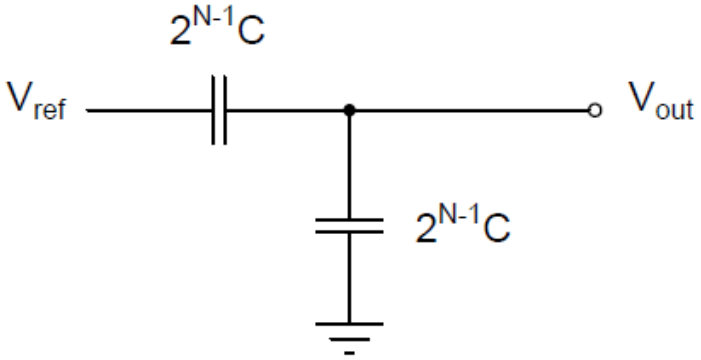


Figure 1.11 Equivalent circuit when MSB = 1 and all other bits set to zero[25].

The ratio between V_{out} and V_{ref} due to each capacitor can be generalized to

$$V_{out} = \frac{2^k C}{2^N C} . V_{ref} = 2^{k-N} . V_{ref} \quad (1.17)$$

where it is assumed that the k-th bit, D_k, is one and all other bits are zero. Superposition can then be used to find the value of V_{out} for any input word by

$$V_{out} = \sum_{k=0}^{N-1} D_k . 2^{k-N} . V_{ref} \quad (1.18)$$

1.5.9 The Split Array

The charge-redistribution architecture is very popular because of its simplicity and relative good accuracy. Although a linear capacitor is required, high resolution in the 10- to 12-bit range can be achieved. However, as the resolution increases, the size of the MSB capacitor becomes a major concern. For example if the unit capacitor, C, were 100fF, and a 12-bit DAC were to be designed, the MSB capacitor would need to be

$$C_{MSB} = 2^{N-1} . 100fF = 204.8pF \quad (1.19)$$

One method of reducing the size of the capacitors is to use a split array. A 6-bit example of the array is pictured in Fig. 1.13. This architecture is slightly different from the charge-redistribution DAC pictured in Fig. 1.11, because in that the output is taken off a different node and an additional attenuation capacitor is used to separate the array into a LSB array and a MSB array. Note that the LSB, D_0, now corresponds to the leftmost switch and that the MSB, D_5, corresponds to the rightmost switch.

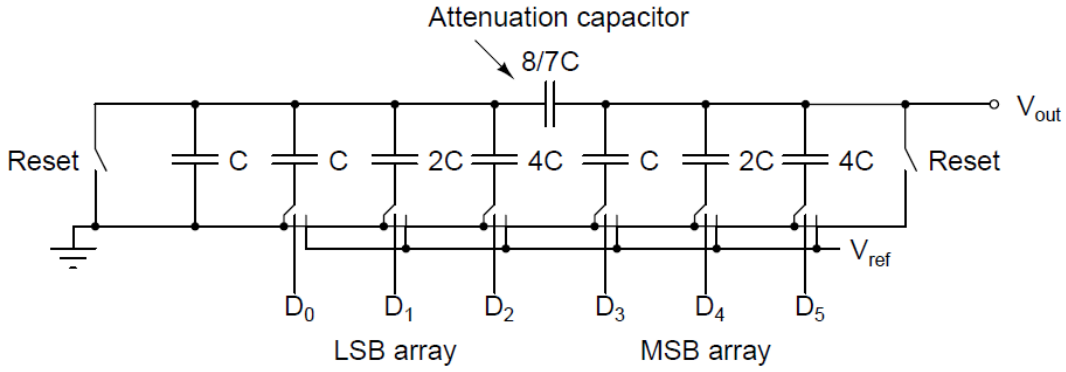


Figure 1.13 A charge-redistribution DAC using a split array [28]

The value of the attenuation capacitor can be found by

$$C_{att} = \frac{sum\ of\ the\ LSB\ array\ capacitors}{sum\ of\ the\ MSB\ array\ capacitors} . C \quad (1.20)$$

where the sum of the MSB array equals the sum of LSB capacitor array minus C. The value

of the attenuation capacitor should be such that the series combination of the attenuation capacitor and the LSB array, assuming all bits are zero, equals C. A drawback of the split array is that spreading in the attenuation capacitor affects all the capacitors after the attenuation capacitor. Therefore, care in the layout should be taken.

1.5.10 Switched capacitor DAC

Switched capacitor DAC is a serial DAC in which the conversion is done sequentially. Typically, one clock pulse is required to convert 1-bit. Thus, N clock pulses would be required for the typical serial N-bit DAC. Since, Successive Approximation analog to digital converter (SAR ADC) also requires N clock pulses for the conversion to take place, hence switched capacitor DAC is widely used as one of the essential component in SAR ADC.

Fig. 1.13 shows conventional method of DAC implementation.

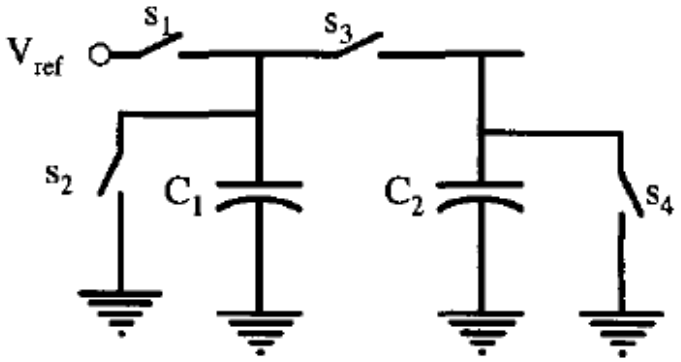


Figure 1.13 Conventional DAC implementation [26].

The operation of conventional DAC is as follows. The capacitors are designed to be of equal value. The conversion starts with the LSB. The capacitorC_1, is charged toV_{ref}, or connected to ground, depending on the value of the bit to be converted. At the same time, capacitor C_2 is discharged by turning on the switchs_4**.** In the second phase, switches s_1, s_2 *and* s_4 are turned off and the switch s_3 is turned on. This puts the capacitors C_1 and C_2 in a parallel configuration forcing the charge on C_1 to be shared equally acrossC_2. The procedure is repeated for all the bits except that the switch s_4 is kept open resulting in the voltage across C_2 converge towards the analog equivalent of the input digital word. Notice that the capacitor C_1 has to be charged to V_{ref} or discharged to ground during each iteration. The conversion starts from the LSB. As a consequence of this latter observation, if this DAC is used as a sub-DAC in an ADC, the ADC will need to convert the input completely before the LSB becomes

available for processing by the DAC. This can slow down the operation of the ADC considerably. Fig. 1.14 shows a new concept of DAC implementation that does not suffer from these drawbacks. C_1 and C_2 are the same size nominally. φ_1 and φ_2 are non-overlapping clocks enabled only when φ_{start} is low. The conversion process starts with φ_{start} going high. This charges the capacitor C_1 to the reference voltage, V_{ref}. Once φ_{start} goes low, φ_1 and φ_2 are enabled. φ_1 turns on first resulting in charge sharing between C_1 and C_2 resulting in C_2 getting charged to $\frac{V_{ref}}{2}$. The data stream is fed to the DAC starting with the MSB. If the current bit, b, is a 1, the charge held by C_2 is transferred to the integrator. If the bit is a 0, the capacitor C_2 is discharged to ground. The process continues until the LSB is reached. In each cycle, charge is transferred in quantities corresponding to the bit under conversion from the "master" capacitor C_1 to C_2 and either integrated with output or discarded to ground.

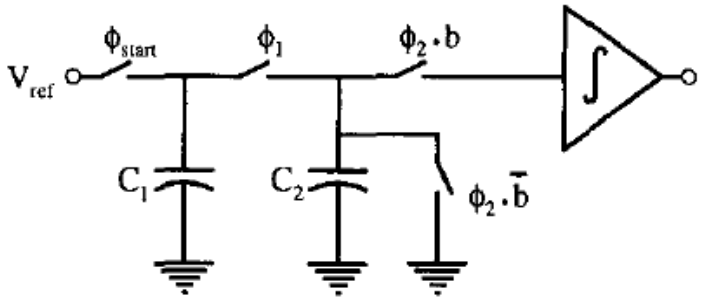


Figure 1.14 Concept of the proposed DAC [26]

There are two benefits of this approach: First, the intermediate output of the DAC either increases (for an input of 1) or stays the same (for an input of 0). Therefore, the output will always be monotonic. Second, the conversion of the digital input starts with the MSB. The benefit of this becomes clear when this DAC is used as part of an ADC. The sub DAC can start its conversion as soon as the MSB from the ADC becomes available. If the DAC was designed to start the conversion starting from the LSB, the ADC would have to finish conversion first before the DAC can start processing its input. The savings in time can be significant.

CHAPTER 2

LITERATURE SURVEY

2.1 Literature Survey of SAR ADC

In a biomedical signal processing system, an ADC is an important circuit that successively converts biomedical signals from analog into digital signals. Analyzing and processing digital signals are dependent on specific demands. However, the ADC operates continuously. Therefore, the power consumption is a very important factor in the ADC circuit design. Moreover, the key components of a successive approximation analog to digital converter (SA-ADC) include a comparator and a DAC. Hence, more stress had given to reducing power of comparator and DAC. A lot of research has been done to reduce power. In [35], 1-V 8-bit 50-kS/s successive approximation analog-to-digital converter (ADC) implemented in a conventional 1.2µm CMOS process is presented. Low voltage, large signal swing sample-and-hold, and digital-to-analog conversion are realized based on inverting op-amp configurations with biasing currents added to the op-amp negative input terminal so that the op-amp input common-mode voltages can be biased near ground to minimize the supply voltage. At the same time, the input and output quiescent voltages can be set at half of the supply rails. Low-voltage latched comparator is realized based on current-mode approach. The entire ADC including all the digital circuits consumes less than 0.34 mW. An effective number of bits of 7.9 were obtained for a 1-kHz 850- mW peak-to-peak input signal. In [7], A new method for switching the capacitors in the DAC capacitor array of a successive approximation register (SAR) ADC is presented. By splitting the MSB capacitor into $b-1$ binary scaled sub-capacitors, the average switching energy of the array can be reduced by 37% compared to a conventional switching method. A formal solution of the switching energy in four different switching methods is included, and the equations are verified using HSPICE simulations of a 10b capacitor array in a 0.18μm CMOS process. In [9], a new self-timed timing control and WRV (Without Reference Voltage) algorithm based on the conventional SA-ADC architecture to detect biomedical signals is proposed in this paper. Using the new self-timed control method, the conversion time could be shortened to turn off the analog circuit earlier to lower the power consumption. In addition, a new WRV algorithm

is introduced to remove the circuits of reference voltage sources in the DAC sub-circuit inside the SA-ADC. By this way, both INL and DNL errors of this SA-ADC are well controlled in 0.33LSB from simulation results. Also, the input range of this proposed SA-ADC can be extended to rail-to-rail. Here, power consumption was 0.3*mW*. In latest research on SAR ADC for biomedical applications, power consumption is reduced to very few µW. [36]. A low power 1V 10-bit successive approximation analog-to-digital converter (SA-ADC) is presented for biomedical applications. In the DAC capacitor arrays of this SA-ADC a charge-recycling method for switching the capacitors is used. Besides, a 1V rail-to-rail input comparator with both current driven bulk technique and offset cancellation is proposed. The complete 1V ADC implemented in TSMC 0.18um CMOS process has a signal-to-noise ratio of 58.5dB and its effective number of bits is 9.4 based on post-layout simulations. The entire ADC power consumption is 32.6uW for normal signals and 29.5uW for ECG applications. 1V 8-bit 10 *kS/s* successive approximation (SA) analog-to-digital converter (ADC) with low power characteristic is implemented for bio-signal acquisition systems. To decrease power consumption, a passive sample-and-hold (SH) circuit and an op-amp-free, capacitor-based digital-to-analog converter (DAC) are utilized. The only active circuit, a comparator, is implemented in the sub-threshold region to preserve the required bias current. According to the measured results, the ADC has a signal-to-noise distortion ratio (SNDR) of 45.2 dB, and peak spurious free dynamic range (SFDR) of 54 dB for a 1 kHz 500 mVpp input sine wave. The effective number of bits (ENOB) is 7.2. Its differential nonlinearity (DNL) and integral nonlinearity (INL) are -0.41/+0.38 and -0.89/+0.6 LSB, respectively**.** The total power consumption is 950*nW*, and the figure of merit (FOM) is 3230 *fJ* per conversion-step. The active area, which is 0.93 x 0.93 mm2, is determined by using TSMC 0.18µm CMOS Process.Table-1 shows performance comparison among above discussed SAR ADC.

Table 2.1 Performance comparison

	[9]	[10]	[11]	[12]	Objective
Process	1.2μm	0.18μm	0.18μm	0.18μm	0.18μm
Resolution	8bits	9bits	10bits	10bits	8bits
Supply voltage	1V	1V	1.8V	1V	1.8V
Sampling rate	50KS/s	150KS/s	70KS/s	40KS/s	10K
DNL	0.47LSB	0.7LSB	0.33LSB	0.25LSB	-0.41/+0.38LSB
INL	1.14LSB	0.75LSB	0.24LSB	0.45LSB	-0.89/+0.6LSB
SNR	49.31dB	51.6dB	59.55dB	58.5dB	45.2dB
ENOB	7.9bits	8.27bits	9.6bits	9.4bits	7.2
Power	0.34mW	30μW	0.3mW	32.6μW	0.95μW

2.2 Literature Survey of DAC

Digital-to-analog converters (DAC's) are very useful blocks in telecommunication and many other applications where the digital and analog worlds meet. In this chapter, a survey of some of the techniques that have been used over the past 15years in achieving low power (LP) DAC's and the techniques that have been employed to reduce the power consumption of this important block. The advantages and disadvantages of each approach are given and the low power limitations are presented. From a study of several published architectures, it is clear that the most power efficient DAC is switched capacitor DAC. Driven by advancement in technology and communication application demands, analog as well as digital circuits are experiencing a trend geared towards low power. The definition or requirement for low power depends on the application where for example, a sensor network will require power consumption of a few tens of microwatts in order to function for a reasonably long time. Two identically designed devices do not necessarily exhibit exactly the same properties. Uncertainties in device fabrication and other technological limits cause the dimensions and doping of the devices to differ by some amount. This is the mismatch problem. Mismatch causes offsets which may introduce inaccuracy problems in operational amplifiers and comparators of DACs. While increasing the sizes of the devices will result in reduced

mismatch, the capacitances will be increased affecting the speed of the circuit. To maintain a comparable speed under increased mismatch, the current consumption must be increased [3, 4]. Following this analysis, it is clear that there exist a trade-off known as the speed-accuracy-power trade-off.

2.2 Various DAC Architectures

2.2.1 High Speed DAC

MARCEL J. M. PELGROM 1988[5]

The integrated circuit implementation of high frequency analogue signal processing applications demands the development of new basic and simple circuits which should avoid using active components to realize high precision operations. In particular, the development of low cost high-speed digital-to-analogue convertors (DACs) is of the special interest for the rapidly expanding market of video processing applications. Because of the simplicity and ease of implementation, algorithmic DACs are widely used for such applications. However, available algorithmic DACs usually utilize an operational amplifier (OA) to implement the desired signal conversion function, which reduces the operating speed and performance accuracy. The next new idea is a two-step operation DAC [5] which overcomes the speed limitations of traditional algorithmic DACs. The first step of the operation always occurs in the charge domain, where a purely passive parasitic-compensated SC circuit implements a simple conversion algorithm consisting of a simple charge division between equal valued capacitors. Then, during the second step, the circuit produces a voltage signal which is directly related to the equivalent charge of the converted digital word. For this purpose, a novel technique has also been developed to eliminate the errors due to the input offset voltage and finite DC gain associated with the charge-voltage conversion circuit. The signal conversion speed of the proposed algorithmic DAC is only limited by RC poles determined by the finite on resistance of the switches and the low capacitance values of the corresponding SC branches, thus rendering it particularly suitable for high-frequency signal processing applications. Since, a purely parasitic-compensated switched-capacitor circuit was chosen to implement a simple signal conversion algorithm; hence the main problem was that appropriate design conditions need to be established to render the circuit insensitive to the input offset voltage and finite DC gain errors of the amplifier. Next, the integration of large

systems on chip requires that digital to- analog converters (DAC's) are realized in CMOS technology. So much attention was focused on waveform coders for analog-to-digital and digital-to-analog conversion. These realizations require an extensive digital filter operation and the converters still suffer from problems at extremely small and large signal levels. For low-cost and low-power applications other principles can present an attractive alternative. Several attempts have been made to design DAC's by means of algorithmic principles with interpolation. So, digital-to-analog converter (DAC) was designed which uses an algorithm based on interpolation. The algorithm ensures monotonicity and differential linearity despite offset voltages and hence eliminates the need for trimming. The technique has been used to design a 15-bit DAC in a 2.5-pm CMOS technology. The converter features S/ (N+THD) of 74 dB with a dynamic range of 87 dB and a power consumption of 22 *mW* at 44-kHz sample frequency. The major problem which has to be solved in these high-resolution converters is non-monotonicity due to circuit offset or mismatching in capacitor values. The 15-bit DAC based on an algorithm which ensures monotonicity and differential linearity despite offset and capacitor mismatch. It has been designed for low-cost digital audio application, but the principle can be used in other applications as well. The main problem in this implementation is low sample frequency and high power consumption. So, low power techniques have to be used.

K. Khanoyan, F. Behbahani, and *el at* .1999 [16]

Recent reports on high-speed CMOS D/A Converters (DACs) demonstrate clock rates and effective bandwidths of the well-known current-steering DAC architecture of l00’s of MHz. In this work, new circuit design and layout methods are applied to a glitch-free 10-bit DAC based on the pipelined charge redistribution architecture. Transients in the output current as codes change are called glitches, and because glitch characteristics depend nonlinearly on codes, they result in spurious tones in the output frequency spectrum. In the glitch-free DAC, on the other hand, the analog voltages are sampled and held at each clock cycle. The 0.6-pm CMOS prototype described here clocks at up to 400 MS/s, and delivers a superior spurious-free dynamic range (SFDR) over the Nyquist band compared to other CMOS DACs. This circuit is part of digitally based agile frequency synthesizer for a fast-frequency hopping

wireless transmitter, and is intended to drive on-chip capacitor loads. The core of the DAC successively bisects charge in an array of equal unit capacitors. Switches driven by a three-phase clock force charge to move from the LSB towards the MSB capacitors. Each data bit pre-charges the corresponding capacitor to one of two reference voltages, and in the next clock cycle the charge is bisected. The charge on the MSB capacitor constitutes the final converted value. An op amp at the end of the capacitor array converts this into a buffered voltage. Latches with appropriate pipeline delays supply data to the cells.

Seung-Chul Lee, Min-Hyung Cho and *et al.* 2002 [17]

A 10 bit 200 MS/s CMOS current-steering digital to analog converter (DAC) employing a new voltage limiter to reduce the feed through of the control signals is presented. At 200 MS/s, a spurious free dynamic range of *65* dB for a 40 MHz output signal has been achieved from the proposed DAC. With rapid progress in such fields as digital synthesis and communication systems, high-speed and high-resolution digital to- analogue converters (DACs) are considered to be the key component completing integrated system design. Most conventional high speed, high-resolution DACs employ segmented current-steering architecture, which combines binary and unary current sources, since it trades off glitch energy, linearity, and overall chip area appropriately. At high-speed operation, there are two main factors that limit the dynamic performance of the DAC. The first factor is output impedance reduction of a current source according to output signal frequency due to the parasitic capacitance in the current source. However, even if the parasitic capacitance is optimized to obtain a level of output impedance high enough to satisfy the specification of the dynamic performance for a given output signal, the expected results may not be achieved, since glitches periodically caused by the feed through of the switch control signals degrade the linearity. Therefore, the current-cell driving circuit, which generates the switch control signals, has been designed carefully to minimize glitches.

Ritu Raj Singh, Roman Genov 2008 [29] .

In this, a capacitive digital-to-analog converter (DAC) architecture combining properties of

the binary-weighted and serial charge-redistribution DACs is presented to yield high integration density and high accuracy. The architecture provides the flexibility to trade area with conversion speed based on a set of area-speed-linearity constraints. We validate the architecture using a 10-bit two-step DAC example, simulated in a standard 0.35μm CMOS technology. The 10-bit DAC occupies 32 times less area than the conventional 10-bit binary-weighted DAC, has low INL, good matching, and high tolerance to parasitic capacitance. Charge-redistribution digital-to-analog converters (DACs) are commonly employed in successive approximation register (SAR) analog-to-digital converter (ADC) designs. In distributed sensory applications, several hundred of such ADCs may be placed on a single chip. This leads to tight area constraints for the data converter block. Low capacitance densities and matching requirements make it difficult to reduce the large area occupied by the DAC capacitors. Common approaches to reduce the capacitor area in charge-redistribution DACs trade area with linearity, speed and complexity. The binary-weighted DAC (BDAC) and the serial DAC (SDAC) , offer a fast conversion speed and use small area respectively. The BDAC occupies large chip area, with a high capacitance spread and cannot achieve resolutions above eight to 10 bits. The SDAC is slow as the conversion time scales linearly with the resolution. It also suffers from linearity errors due to excessive switching. To overcome the large area constraint of the BDAC, while maintaining high speed, several architectures have been proposed. The two-stage buffer DAC occupies significantly less area but requires a unity gain buffer, increasing the complexity and power consumption. The two stage capacitor network assumes the top plate parasitics to be negligible and requires a transconductance amplifier to remove the nonlinearities.

RICARDO E. SUAREZ 1975, [11]

This two-part paper describes two different techniques for performing analog-to-digital (A/D) conversion compatibly with standard single-channel MOS technology. In the first paper, the use of a binary weighted capacitor array to perform a high-speed successive approximation conversion was discussed. Titis second paper describes a two-capacitor successive approximation technique, which, in contrast to the first, requires considerably less die area, is inherently monotonic in the presence of capacitor ratio errors, and which operates

at somewhat lower conversion rate. Factors affecting accuracy and conversion rate are considered analytically. Experimental results from a monolithic prototype are presented; a resolution of eight bits was achieved with an A/D conversion time of 100 p.s. Used as a digital-to-analog (D/A) converter, a settling time of 13.5 μs was achieved. The estimated total die size for a completely monolithic version including logic is 5000mil^2. Traditional approaches to A/D conversion have required the simultaneous implementation of high-performance analog circuits, such as operational amplifiers, and of digital circuitry for counting, control, and data storage. Consequently, current A/D converter realizations have tended to be multiple-chip approaches wherein the advantages offered by bipolar and MOS fabrication technologies are separately exploited. In contrast, the charge-redistribution A/D conversion technique to be described in this paper requires a minimum number of precision components and is realizable on a single low cost

MOS chip. Compared with the weighted capacitor technique described in Part I, the technique requires only two equal grounded capacitors of moderate value. As a result, it can be realized in a relatively small die area compared with the weighted capacitor approach. On the other hand, ultimate resolution of this technique is sensitive to parasitic capacitances associated with the switch transistors, and the conversion rate is lower for a given clock rate because of the conversion algorithm required. The technique is thus most suitable when moderate conversion rate and moderate resolution are required in a small die area.

S.H. Yang, K.S. Lee, S. Kim and Y.M. Lee 2011 [15]

An 8-bit charge-redistribution DAC with double bit processing in a single capacitor is proposed. The proposed DAC requires only four binary weighted capacitors where each capacitor converts 2-bit digital data into an analogue value in a single conversion step. Therefore, capacitor area can be effectively reduced without affecting the conversion time. The proposed 8-bit DAC is fabricated using CMOS 0.18 mm technology with a core area of 0.0934mm^2. In mobile display drivers, low power and small area are very important requirements. In addition, the conversion time has to be fast since high resolution and high data rate are required. Conventionally, resistor-based DACs have been mostly used in column drivers for LCDs and LEDs. However, since resistor-based DACs consume more power and

occupy large area as the DAC resolution increases, charge-redistribution DACs such as cyclic and binary weighted DACs are commonly employed nowadays. Cyclic DACs can be a good solution for small area since they only use two or three capacitors. However, the conversion time increases with the resolution, which can be a limitation for large-sized display panels. On the other hand, binary-weighted DACs have fast conversion speed, yet size is still a burden owing to the large capacitor area. As a result, there is a trade-off between capacitor area and the conversion speed for charge-redistribution DACs. In this Letter, we propose a double bit processing 8-bit charge-redistribution DAC that can reduce capacitor area to 1/16 of the conventional 8-bit binary-weighted DAC, while maintaining conversion speed.

2.2.2 Switched Capacitor DAC

Mezyad M. Amourah, Saqib *Q.* Malik and *et al*. 2002 [26]

A monotonic DAC using switched capacitor integrator is presented. For an N-bit digital input sequence, the proposed DAC starts conversion with the MSB and takes N cycles to finish conversion. The DAC samples the reference voltage only once and transfers appropriate charge to an output capacitor. Some issues relevant to the design and their possible solutions are presented. Digital-to-Analog converters (DACs) help bridge the digital domain with the everyday analog world. A DAC occupying small area capable of high resolution is of use in many applications. A monotonic DAC always has an increasing analog output with increasing digital input. This behavior is essential in many applications. These applications can tolerate non-linearities but cannot tolerate non-monotonicity. In this paper, a simple switched capacitor DAC is presented that exhibits monotonicity while occupying a small area. The proposed DAC starts its conversion from the MSB instead of the traditional approach of starting from LSB [31].making it suitable for use in cyclic or successive approximation analog-to-digital converters (ADCs).

Zhiheng Cao and Shouli Yan 2006 [30]

A multi-bit switched-capacitor DAC with robust analog background calibration intended to

be used as feedback DAC for multi-bit pipeline ADCs or broadband sigma delta ADCs with low oversampling ratio is presented in this paper. The accuracy of calibration is not limited by mismatch of charge injections. A multi-bit switched capacitor DAC whose linearity is only limited by op amp DC gain is realized. Multi-bit feedback DACs are used in delta-sigma modulators or pipelined ADCs to reduce op amp output swing thus linearity requirement of the integrators or inter-stage gain accuracy requirement in case of pipeline ADC. Since CMOS process can only match capacitor up to 10-12 bit and the matching degrades for smaller capacitors, some kind of linearization of the multi-bit DAC is necessary if more than 10 bit resolution is desired for the entire ADC. When the oversampling ratio (OSR) is high, first order mismatch shaping techniques such as data weighted averaging (DWA) are usually the best choice. However, when OSR is low or in case of pipelined ADC , first order mismatch shaping is no longer effective and much more complicated linearization techniques such as higher order mismatch shaping or digital noise cancellation (DNC) must be used. Such techniques require much design complexity and have potential stability problems (in the case of higher order mismatch shaping) or long convergence time (in the case of DNC). In this paper, an improved technique is proposed that is fully implemented in discrete-time, switched-capacitor circuits. Therefore the circuit can work with any clock frequency, improving flexibility of the system. Furthermore, by an improved switching sequence, charge injection mismatch that limits the accuracy of many existing analog calibration techniques have been eliminated. The DAC element matching becomes only limited by the calibration loop gain. In this thesis, 8-bit DAC is simulated in 0.18 μm technology. Previous architectures use either binary weighted or segmented current steering architectures which although provides high speed to the DAC, but at the same time consumes very high power. Since, here the main emphasis is on low power; hence switched capacitor technique is preferred. Power consumed in this architecture is very less as compared to previous architectures. This decrease in power makes the DAC to be used in SAR ADC for various applications.

Table 2.2 Performance Comparison

	[32]	[17]	[16]	[29]	[28]
Technology	0.18μm	0.35 μm	0.5 μm	0.35 μm	0.35 μm
Resolution	6	10	10	10	14
Conversion speed	1.3GS/s	200MS/s	400MS/s	25MS/s	5MS/s
Input range	600mV_{pp}	-	0.5V_{pp}	-	-
Supply voltage	1.8V	3V	3.3V	3V	3V
Power consumption	64mW	61mW	90mW	-	7mW
Gain	40dB	65dB	-	-	90dB
Load capacitance	-	50pF	0.5pF	3.2pF	-

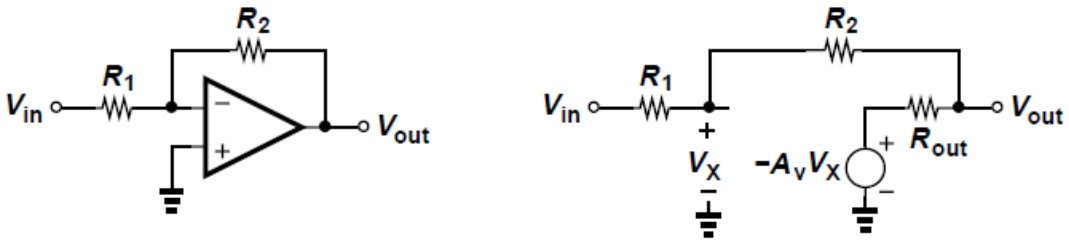
CHAPTER 3

SWITCHED CAPACITOR CIRCUITS

There are two types of circuits: Continuous-time circuits and Discrete-time circuits. There are amplifiers where the input signal is continuously available and applied to the circuit and the output signal is continuously observed. These circuits are called “continuous-time” circuits. Such amplifiers find wide application in audio, video, and high-speed analog systems. In many situations, however the input is required to be sensed at periodic instants of time, ignoring its value at other times. The circuit then processes each “sample” producing a valid output at the end of each period. Such circuits are called “discrete-time” or “sampled-data” systems. Here, a common class of discrete-time systems called “switched-capacitor circuits” is discussed. The objective is to provide the foundation for more advanced topics such as filters, comparators, ADCs and DACs. Beginning with a general view of SC circuits, sampling switches and their speed and precision issues are also described.

3.1 General Considerations

In order to understand the motivation for sampled-data circuits, let us first consider the simple continuous-time amplifier shown in Fig. 3.1(a). Used extensively with bipolar op amps, this circuit presents a difficult issue if implemented in CMOS technology. Recall that, to achieve a high voltage gain, the open-loop output resistance of CMOS op amps is maximized, typically approaching hundreds of kilo-ohms. So R_2 heavily drops the open-loop gain, degrading the precision of the circuit.



(a) (b)

Figure 3.1 (a) Continuous-time feedback amplifier, (b) equivalent circuit of (a).[1]

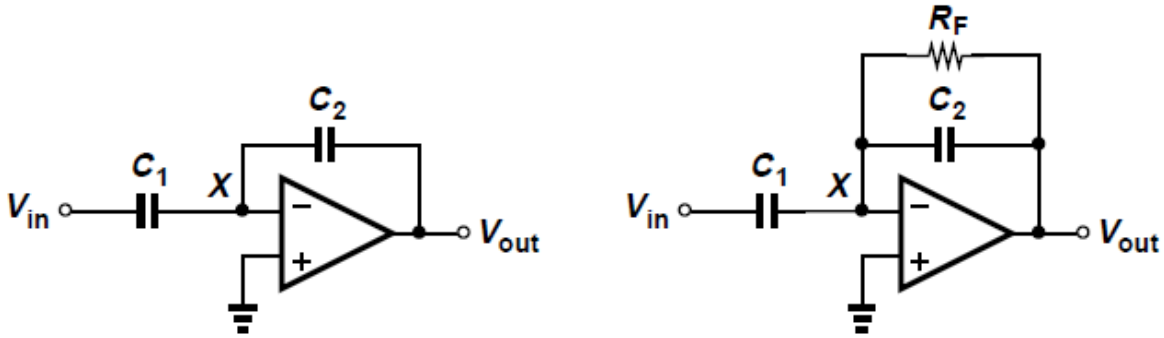
In fact, with the aid of the simple equivalent circuit shown in Fig. 3.1(b), we can write:

$$-A_v\left(\frac{V_{out}-V_{in}}{R_1+R_2}R_1+V_{in}\right)-R_{out}\frac{V_{out}-V_{in}}{R_1+R_2}=V_{out} \quad (3.1)$$

and hence

$$\frac{V_{out}}{V_{in}}=-\frac{R_2}{R_1}\cdot\frac{A_v-\frac{R_{out}}{R_2}}{1+\frac{R_{out}}{R_1}+A_v+\frac{R_2}{R_1}} \quad (3.2)$$

Equation (3.2) implies that, compared to the case where R_{out} = 0, the closed-loop gain suffers from inaccuracies in both the numerator and the denominator. Also, the input resistance of the amplifier, approximately equal to R_1, loads the preceding stage while introducing thermal noise. In the circuit of Fig. 3.1(a), the closed-loop gain is set by the ratio of R_2 and R_1. In order to avoid reducing the open-loop gain of the op amp, we postulate that the resistors can be replaced by capacitors [Fig. 3.2(a)]. But, to set the bias voltage at node X a large feedback resistor as in Fig. 3.2(b), providing dc feedback while negligibly affecting the ac behavior of the amplifier in the frequency band of interest. Such an arrangement is indeed practical if the circuit senses only high-frequency signals.



(a) (b)

Figure 3.2 (a) Continuous-time feedback amplifier using capacitors, (b) use of resistor to define bias point [1].

Illustrated in Fig. 3.3, the response contains a step change due to the initial amplification by the circuit consisting of $C_1 and\ C_2$, and the op amp, followed by a "tail" resulting from the loss of charge on C_2 throughR_F. From another point of view, the circuit may not be suited to amplify wideband signals because it exhibits a high-pass transfer function.

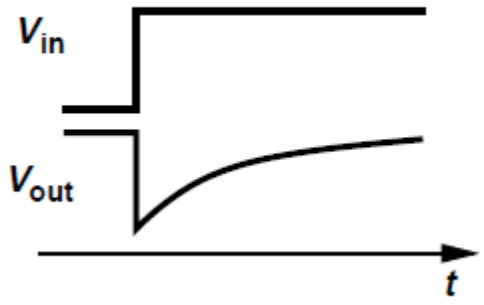


Figure 3.3 Step response of amplifier of Figure 3.2(b)[1].

In fact, the transfer function is given by

$$\frac{V_{out}}{V_{in}}(s) \approx \frac{R_F \frac{1}{C_2 s}}{R_F + \frac{1}{C_2 s+1}} \div \frac{1}{C_1 s} \tag{3.3}$$

$$= -\frac{R_F C_1 s}{R_F C_2 s+1} \tag{3.4}$$

The above difficulty can be remedied by increasing$R_F C_2$, but in many applications the required value of the two components becomes prohibitively large. Let us now consider the switched-capacitor circuit depicted in Fig. 3.4, where three switches control the operation: S_1 and S_3 connect the left plate of C_1 to V_{in} and ground, respectively, and

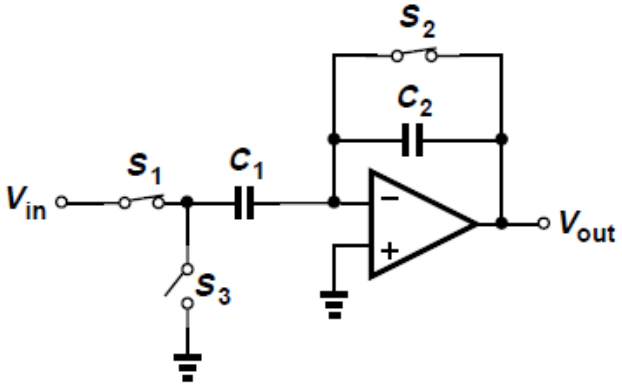
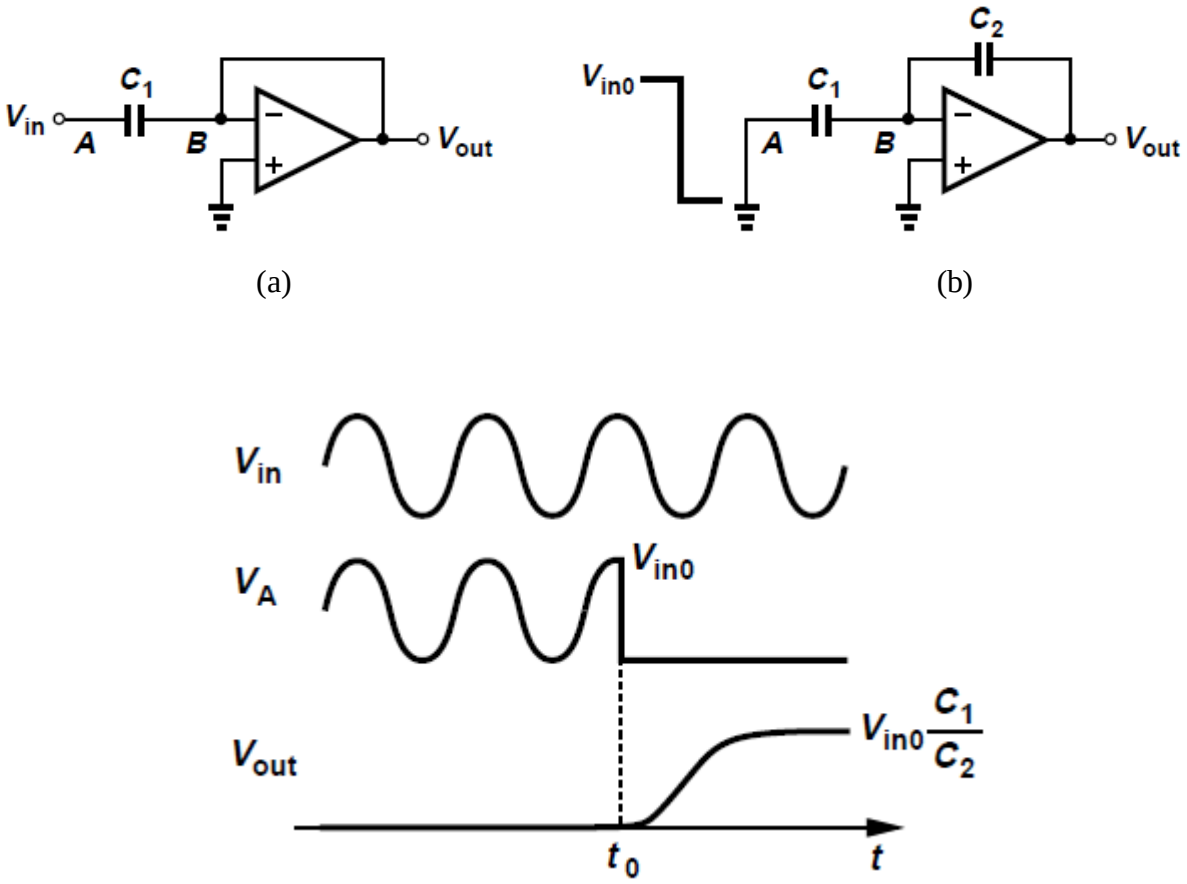


Figure 3.4 Switched-capacitor amplifiers [1].

S_2 Provide unity-gain feedback. It is assumed that the open-loop gain of the op amp is very large. The circuit is studied in two phases. First, S_1 and S_2 are on and S_3 is off, yielding the equivalent circuit of Fig. 3.5(a).



(a) (b)

Figure 3.5 Circuit of Fig. 3.4 in (a) Sampling mode, (b) Amplification mode [1].

For a high-gain op amp, $V_B = V_{out} \approx 0$, and hence the voltage across C_1 is approximately equal to V_{in}. Next, at $t = t_0$, S_1 and S_2 turn off and S_3 turns on, pulling node *A* to ground. Since V_A changes from V_{in} to 0, the output voltage must change from zero to$V_{in0}C_1/C_2$. The output voltage change can also be calculated by examining the transfer of charge. Note that the charge stored on C_1 just before t_0 is equal to$V_{in0}C_1$. After $t = t_0$, the negative feedback through C_2 drives the op amp input differential voltage and hence the voltage across C_1 to zero (Fig. 3.6). The charge stored on C_1 at $t = t_0$ must then be transferred to C_2, producing an output voltage equal to $V_{in0}C_1/C_2$. Thus, the circuit amplifies V_{in0} by a factor of C_1/C_2. Several attributes of the circuit of Fig. 3.4 distinguish it from continuous-time implementations. First, the circuit devotes some time to "sample" the input, setting the output to zero and providing no amplification during this period. Second, after sampling, for $t > t_0$, the circuit ignores the input voltage V_{in} amplifying the sampled voltage. Third, the

circuit configuration changes considerably from one phase to another, as seen in Fig. 3.5(a) and (b), raising concern about its stability.

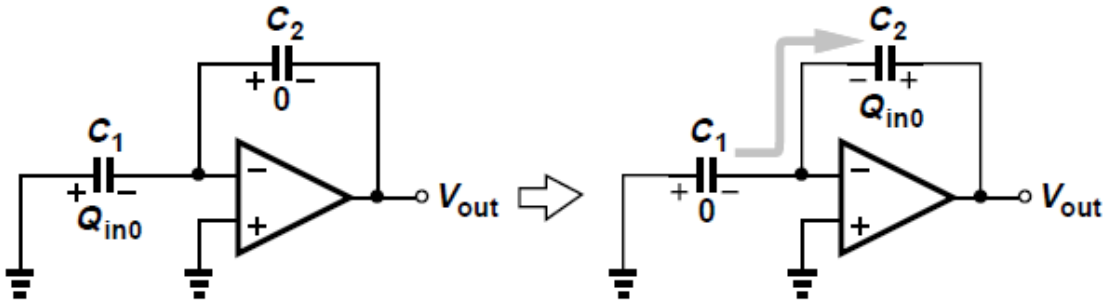


Figure 3.6. Transfer of charge from C_1 to C_2[1].

In addition to sampling capability, we note from the waveforms depicted in Fig. 3.5 that after V_{out} settles, the current through C_2 approaches zero. That is, the feedback capacitor does not reduce the open-loop gain of the amplifier if the output voltage is given enough time to settle. In Fig. 3.1, on the other hand, R_2 continuously loads the amplifier.

In the simplest case, the operation takes place in two phases: sampling and amplification. Thus, in addition to the analog input, V_{in}, the circuit requires a clock to define each phase as shown in Fig. 3.7. The study of SC amplifiers proceeds according to these two phases.

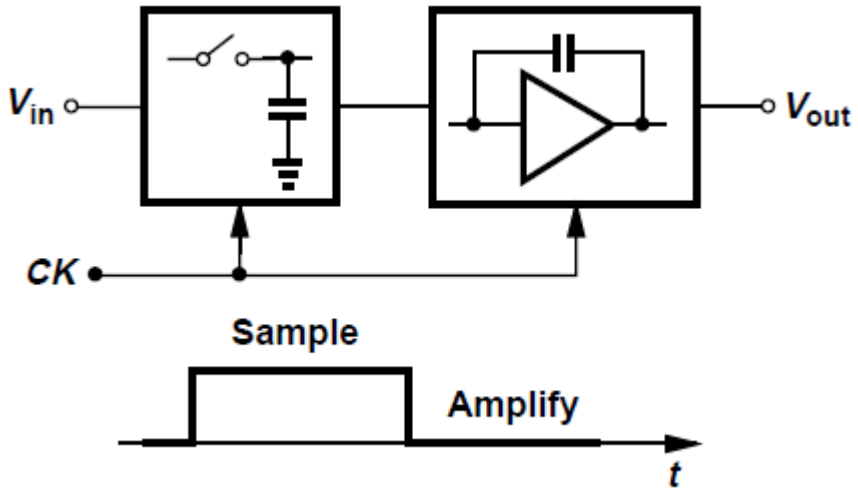
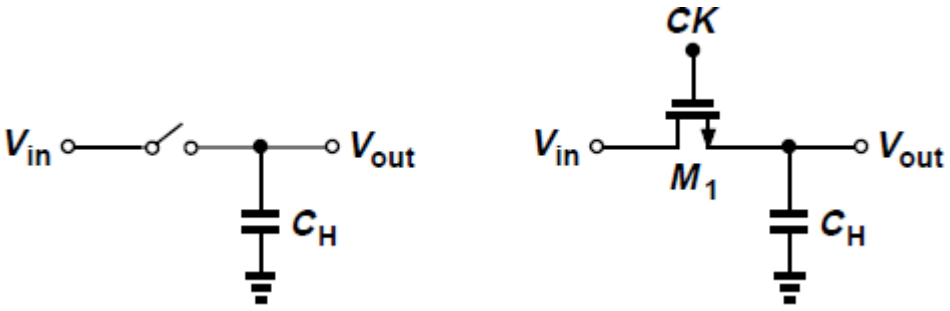


Figure 3.7. General view of switched-capacitor amplifier[1].

3.2 Sampling Switches

3.2.1 MOSFETS as Switches

A simple sampling circuit consists of a switch and a capacitor [Fig. 3.8(a)]. A MOS transistor acts as a switch [Fig. 3.8(b)] because (a) it can be on while carrying zero current, and (b) its

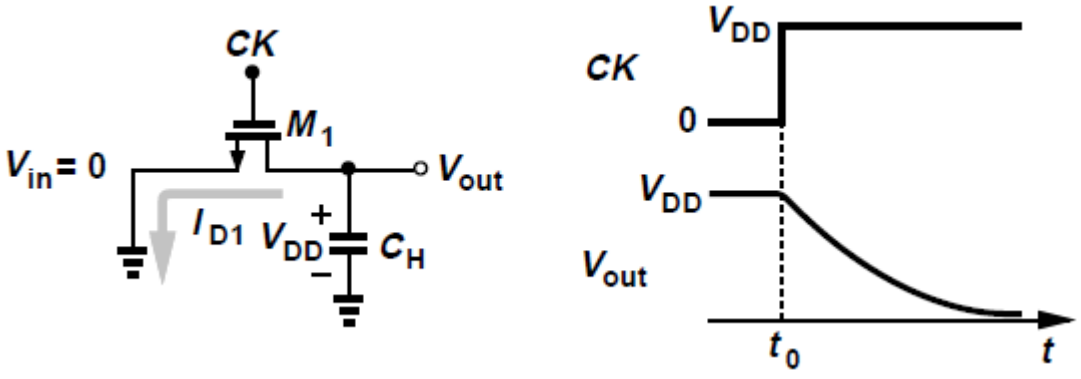


(a) (b)

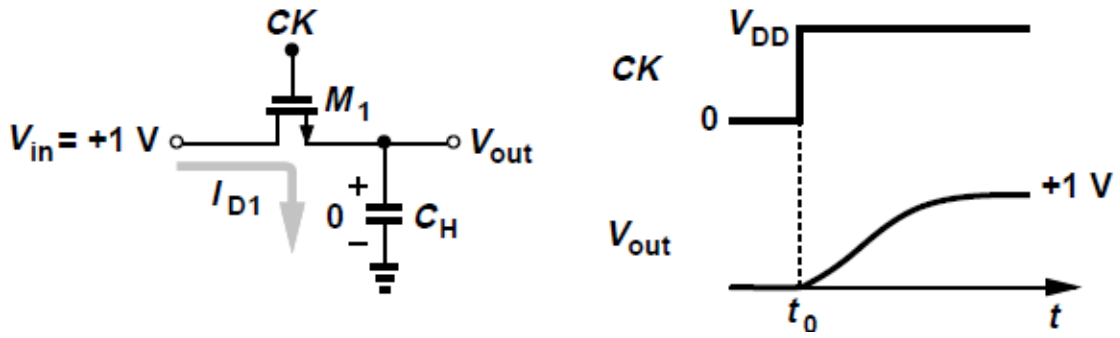
Figure 3.8 (a) Simple sampling circuit, (b) implementation of the switch by a MOS device [1].

Source and drain voltages are not "pinned" to the gate voltage, i.e., if the gate voltage varies, the source or drain voltage need not follow that variation. By contrast, bipolar transistors lack both of these properties, typically necessitating complex circuits to perform sampling.

To understand how the circuit of Fig. 3.8(b) samples the input, first consider the simple cases depicted in Fig. 3.9, where the gate command, CK, goes high at $t = t_0$. In Fig. 3.9(a), we assume that V_{in} = 0 for $t \geq t_0$ and the capacitor has an initial voltage equal to V_{DD}. Thus, at $t = t_0$. , M1 senses a gate-source voltage equal to V_{DD} while its drain voltage is also equal to V_{DD}. The transistor therefore operates in saturation, drawing a current of $I_{D1} = (\mu_n C_{ox}/2)\frac{W}{L}(V_{DD} - V_{TH})^2$ from the capacitor.



(a)

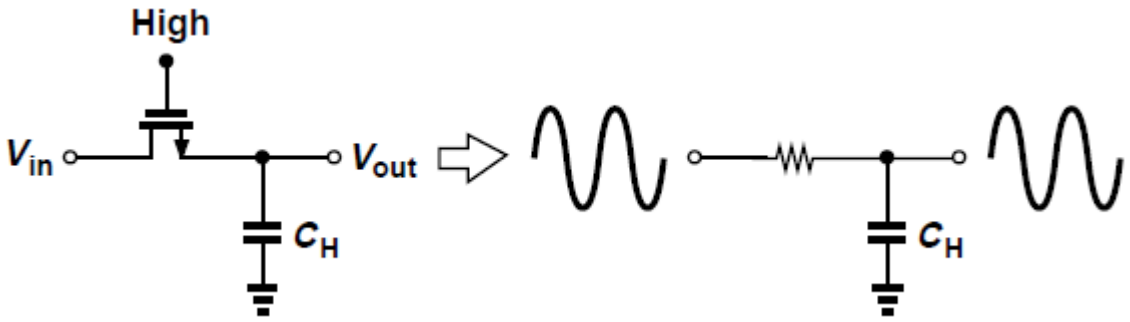


(b)

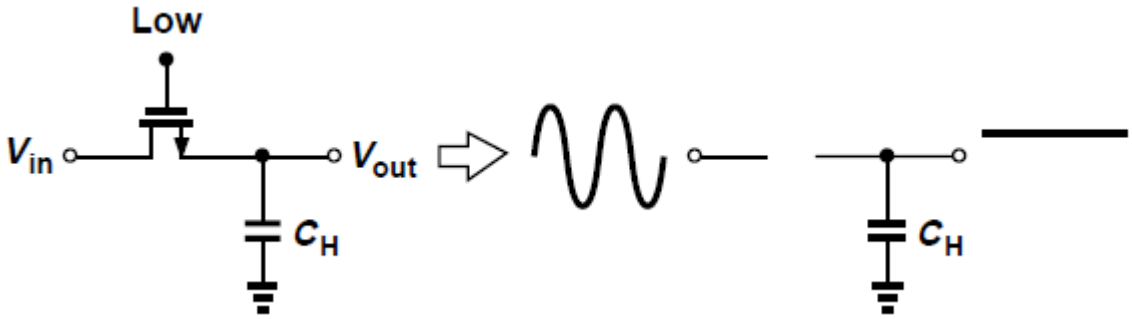
Figure 3.9 Response of a sampling circuit to different input levels and initial conditions [1].

As V_{out} falls, at some point, $V_{out} = V_{DD} - V_{TH}$, driving M_1 into the triode region. The device nevertheless continues to discharge C_H until V_{out} approaches zero. Note that for $V_{out} \ll 2(V_{DD} - V_{TH})$, the transistor can be viewed as a resistor equal to $R_{on} = \mu_n C_{ox} \frac{W}{L} (V_{DD} - V_{TH})^{-1}$

Now consider the case in Fig. 3.9(b), where V_{in}= +1 V, V_{out} $t = t_0$= 0 V, and V_{DD} = 3 V. Here, the terminal of M_1 connected to C_H acts as the source, and the transistor turns on with V_{GS} = +3 V, but V_{DS} = +1 V. Thus, M1 operates in the triode region, charging C_H until V_{out} approaches+1V.For $V_{out} = +1V$, M1 exhibits an on-resistance of $R_{on} = \mu_n C_{ox} \frac{W}{L} (V_{DD} - V_{TH})^{-1}$. The above observations reveal two important points. First, a MOS switch can conduct current in either direction simply by exchanging the role of its source and drain terminals. Second, as shown in Fig. 3.10, when the switch is on, V_{out} follows V_{in} and when the switch is off, V_{out} remains constant. Thus, the circuit “tracks” the signal when CK is high and “freezes” the instantaneous value of V_{in} across C_H when CK goes low.



(a)

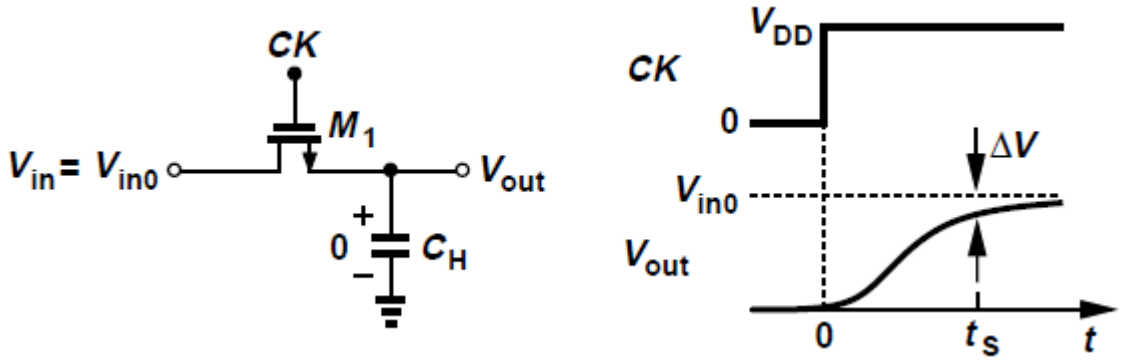


(b)

Figure 3.10 Track and hold capabilities of a sampling circuit [1].

3.2.2 Speed considerations

Illustrated in Fig. 3.11, a simple, but versatile measure of speed is the time required for the output voltage to go from zero to the maximum input level after the switch turns on. Since V_{out} would take infinite time to become equal to V_{in0}, let us consider that the output to get settled when it is within a certain "error band," ΔV, , around the final value. For example, if the output settles to 0.1% accuracy after t_s seconds, meaning that in Fig. 3.11, $\frac{\Delta V}{V_{ino}} = 0.1\%$. Thus, the speed specification must be accompanied by an accuracy specification as well. Note that after $t = t_s$ we can consider the source and drain voltages to be approximately equal.



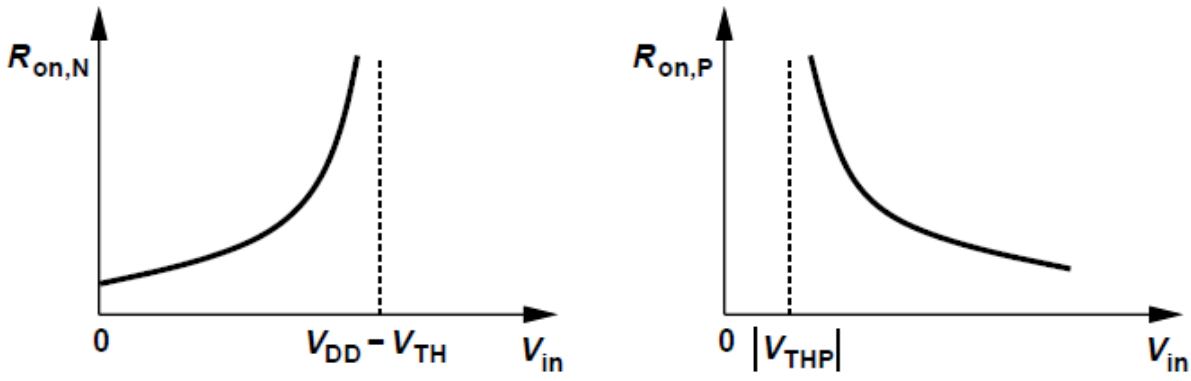
(a) (b)

Figure 3.11 Definition of speed in a sampling circuit [1].

From the circuit of Fig. 3.11, we surmise that the sampling speed is given by two factors: the on-resistance of the switch and the value of the sampling capacitor. Thus, to achieve a higher speed, a large aspect ratio and a small capacitor must be used. As R_{on} i.e. the on-resistance is given by

$$R_{on} = \mu_n C_{ox} \frac{W}{L} (V_{DD} - V_{TH})^{-1} \tag{3.5}$$

using equation (3.5), the plot of on-resistance of the switch as a function of the input level is made. This plot is shown in Fig. 3.12 notice that there is a sharp rise as V_{in} approaches$V_{DD} - V_{TH}$.



(a) (b)

Figure 3.12 On-resistances of (a) NMOS and (b) PMOS devices as a function of input voltage.

For example, if we restrict the variation of R_{on} to a range of 4 to 1, then the maximum input

level is given by

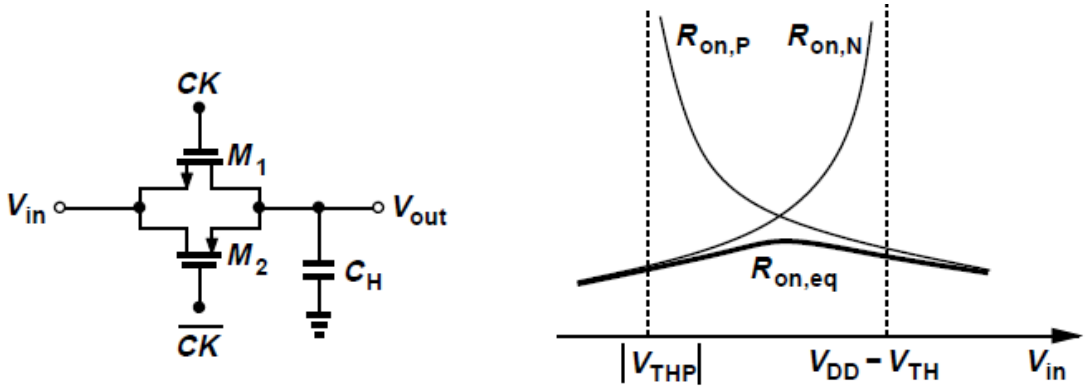
$$\frac{1}{\mu_n C_{ox}\frac{W(V_{DD}-V_{in,max}-V_{TH})}{L}} = \frac{4}{\mu_n C_{ox}\frac{W}{L}(V_{DD}-V_{TH})} \tag{3.6}$$

This value falls around $V_{DD}/2$, translating to severe swing limitations. Note that the device threshold voltage directly limits the voltage swings. In order to accommodate greater voltage swings in a sampling circuit, we first observe that a PMOS switch exhibits an on-resistance that decreases as the input voltage becomes more positive [Fig. 3.12(b)]. It is then possible to employ "complementary" switches so as to allow rail-to-tail swings. Shown in Fig. 3.13(a), such a combination requires complementary clocks, producing an equivalent resistance equal to

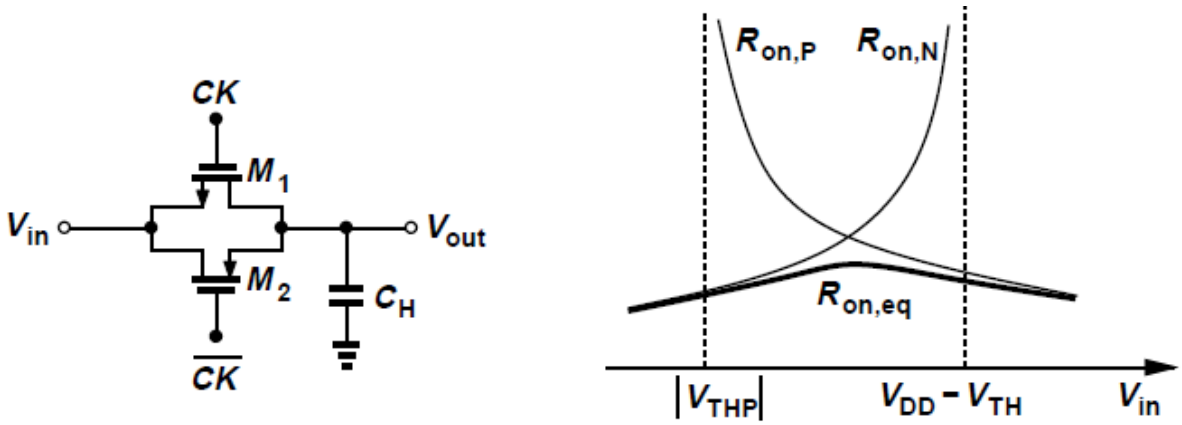
$$R_{on,eq} = R_{on,N} \parallel R_{on,P} \tag{3.7}$$

$$\frac{1}{\mu_n C_{ox}\frac{W_n(V_{DD}-V_{in}-V_{THN})}{L_n}} = \frac{1}{\mu_p C_{ox}\frac{W_n(V_{in}-V_{THP})}{L_n}} \tag{3.8}$$

Interestingly, if $\mu_n C_{ox}(\frac{W}{L})_n = \mu_p C_{ox}(\frac{W}{L})_p$ (3.9)



(a)



(b)

Figure 3.13(a) Complementary switch, (b) on-resistance of the complementary switch [1].

Fig. 3.13(b) plots the behavior of $R_{on,eq}$ in the general case, revealing much less variation than that corresponding to each switch alone. For high-speed input signals, it is critical that the NMOS and PMOS switches in Fig. 3.13(a) turn off simultaneously so as to avoid ambiguity in the sampled value. If, for example, the NMOS device turns off Δt seconds earlier than the PMOS device, then the output voltage tends to track the input for the remaining Δt seconds, but with a large, input-dependent time constant (Fig. 3.14). This effect gives rise to distortion in the sampled value. For moderate precision, the simple circuit shown in Fig. 3.15 provides complementary clocks by duplicating the delay of inverter I_1 through the gateG_2.

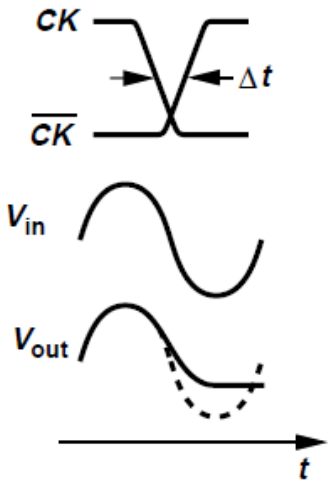


Figure 3.14 Distortion generated if complementary switches do not turn off simultaneously.

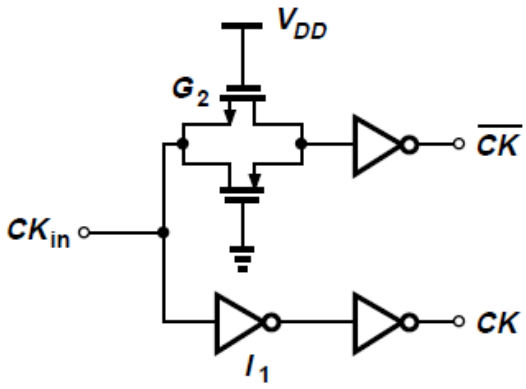


Figure 3.15 Simple circuit generating complementary clocks [1].

3.2.3 Settling time

The charging of every individual capacitor that represents a bit value should occur within a certain time, the settling time. The settling time depends on the ON-resistance of the inverter, the capacitive load of the inverter (deglitch- and charging capacitor) and the accuracy demand. The accuracy is determined by the required resolution, which is 8 bits. The charging of a capacitor is defined by formula

$$V_c = V_{ref}\left(1 - e^{\frac{-t}{RC}}\right) \tag{3.10}$$

Because of the 8-bit resolution the smallest step that can be made at the output is

$$V_{LSB} = \frac{V_{ref}}{2^N} \tag{3.11}$$

To settle within the required accuracy the minimal time needed will be

$$V_{ref}\left(1 - e^{\frac{-t}{RC}}\right) = V_{ref} - V_{LSB} = V_{ref} - \frac{V_{ref}}{2^N} = V_{ref}\left(1 - \frac{1}{2^N}\right) \tag{3.12}$$

$$e^{\frac{-t}{RC}} = \frac{1}{2^N} \tag{3.13}$$

or $$t = RC\ln(2^N) \tag{3.14}$$

For a 8-bit DAC, the settling time is

$$t = 5.545\ RC \tag{3.15}$$

The product of the ON-resistance and the capacitive load of the transistor determine the bandwidth. So if the sampling frequency is 5*Ms/s* then the time to charge and discharge the charging capacitor is equal to 0.2μs. Formula (3.10) describes only the charging of a capacitor, therefore the settling time has to occur in only half the period, in 0.1μs.

Substituting the settling time in formula (3.15) results in an expression for the RC-product

$$RC = \frac{0.1\mu s}{5.545} = 0.018\ \mu s$$

Or $RC = 18ns$ (3.16)

3.2.4 Precision Considerations

The foregoing study of MOS switches indicates that a larger W/L or a smaller sampling capacitor results in a higher speed. This section shows that the method of increasing the speed degrades the precision with which the signal is sampled.

Three mechanisms in MOS transistor operation introduce error at the instant the switch turns off. Let us study each effect individually.

Channel Charge Injection: Consider the sampling circuit of Fig. 3.17 and recall that for a MOSFET to be on, a channel must exist at the oxide-silicon interface. Assuming $V_{in} \approx V_{out}$, the total charge in the inversion layer is given by:

$$Q_{ch} = WLC_{ox}(V_{DD} - V_{in}\text{-}V_{TH}), \quad (3.17)$$

where L denotes the effective channel length. When the switch turns off, Q_{ch} exits through the source and drain terminals, a phenomenon called "channel charge injection."

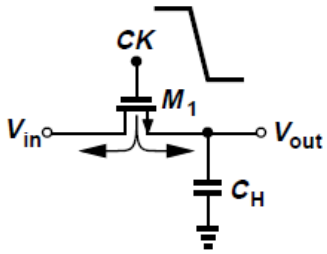


Figure 3.16 Charge injection when a switch turns off[1].

The charge injected to the left side on Fig. 3.16 is absorbed by the input source, creating no error. On the other hand, the charge injected to the right side is deposited on C_H, introducing an error in the voltage stored on the capacitor. For example, if half of Q_{ch} is injected onto C_H, the resulting error equals

$$\Delta V = \frac{WLC_{ox}(V_{DD} - V_{in} - V_{TH})}{2C_H} \quad (3.18)$$

Illustrated in Fig. 3.17, the error for a NMOS switch appears as a negative "pedestal" at the output.

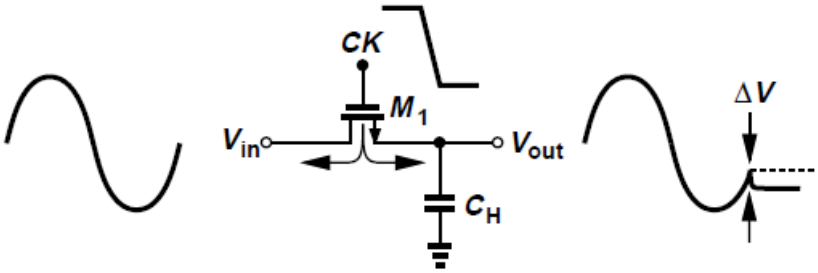


Figure 3.17 Effect of charge injection [1].

Note that the error is directly proportional to WLC_{ox}ox and inversely proportional toC_H. In reality, the fraction of charge that exits through the source and drain terminals is a relatively complex function of various parameters such as the impedance seen at each terminal to ground and the transition time of the clock. Investigations of this effect have not yielded any rule of thumb that can predict the charge splitting in terms of such parameters. Furthermore, in many cases, these parameters, e.g., the clock transition time, are poorly controlled. Also, most circuit simulation programs model charge injection quite inaccurately. As a worst-case estimate, we can assume that the entire channel charge is injected onto the sampling capacitor.

How does charge injection affect the precision? Assuming all of the charge is deposited on the capacitor, we express the sampled output voltage as

$$V_{out} \approx V_{in} - \frac{WLC_{ox}(V_{DD} - V_{in} - V_{TH})}{C_H} \tag{3.19}$$

where the phase shift between the input and output is neglected. Thus,

$$V_{out} = V_{in}\left(1 + \frac{WLC_{ox}}{C_H}\right) - \frac{WLC_{ox}}{C_H}(V_{DD} - V_{TH}) \tag{3.20}$$

suggesting that the output deviates from the ideal value through two effects: a non-unity gain equal to $1 + \frac{WLC_{ox}}{C_H}$ and a constant offset voltage $\frac{WLC_{ox}}{C_H}(V_{DD} - V_{TH})$ (Figure. 3.18). In other words, since it is assumed that channel charge is a linear function of the input voltage, the circuit exhibits only gain error and dc offset.

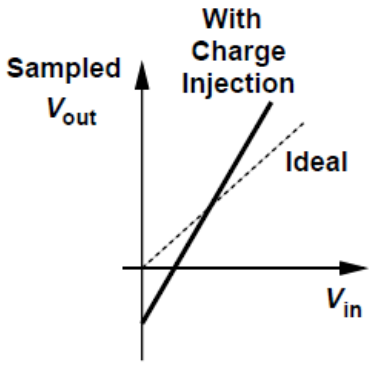


Figure 3.18 Input/output characteristic of sampling circuit in the presence of charge injection.

In the foregoing discussion, it is assumed that V_{TH} is constant. However for NMOS switches (in an n-well technology) body effect must be taken into account. Since V_{TH}= $V_{TH0} + \gamma(\sqrt{2\varphi_B + V_{BS}} - \gamma\sqrt{2\varphi_B})$, and $V_{BS} \approx -V_{in}$, it gives

$$V_{out} = V_{in} - \frac{WLC_{ox}}{C_H}\left(V_{DD} - V_{in} - V_{TH0} - \gamma\sqrt{2\varphi_B + V_{in}} - \gamma\sqrt{2\varphi_B}\right) \quad (3.21)$$

It follows that the nonlinear dependence of V_{TH} upon V_{in} introduces nonlinearity in the input/output characteristic. In summary, charge injection contributes three types of errors in MOS sampling circuits: gain error, dc offsets, and nonlinearity. In many applications, the first two can be tolerated or corrected whereas the last cannot. It is instructive to consider the speed-precision trade-off resulting from charge injection. Representing the speed by a simple time constant τ and the precision by the error ΔV due to charge injection, the figure of merit is defined as $F = (\tau\Delta V)^{-1}$. Writing

$$\tau = R_{on}C_H \quad (3.22)$$

$$= \frac{1}{\mu_n C_{ox}\left(\frac{W}{L}\right)(V_{DD} - V_{in} - V_{TH})}.C_H \quad (3.23)$$

And

$$\Delta V = \frac{WLC_{ox}}{C_H}(V_{DD} - V_{in} - V_{TH}) \quad (3.24)$$

$$F = \frac{\mu_n}{L^2} \quad (3.25)$$

Thus, to the first order, the trade-off is independent of the switch width and the sampling

capacitor.

Clock Feedthrough: In addition to channel charge injection, a MOS switch couples the clock transitions to the sampling capacitor through its gate-drain or gate-source overlap capacitance. Depicted in Fig. 3.19, the effect introduces an error in the sampled output voltage. Assuming

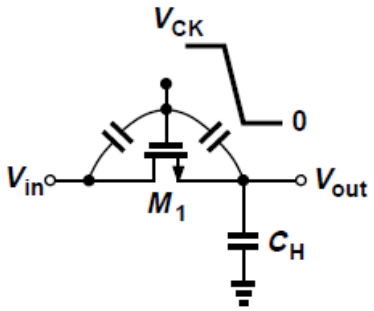


Figure 3.19 Clock feed-through in a sampling circuit [1].

overlap capacitance is constant, we express the error as

$$\Delta V = V_{CK} \frac{WC_{ov}}{WC_{ov}+C_H} \tag{3.26}$$

Where C_{ov} the overlap capacitance per unit width.The error is ΔV is independent of the input level, manifesting itself as a constant offset in the input/output characteristic. As with charge injection, clock feed through leads to a trade-off between speed and precision as well. Also notice that a resistor charging a capacitor gives rise to a total rms noise voltage of $\sqrt{\frac{kT}{C}}$. as shown in Figure. 3.20; a similar effect occurs in sampling circuits.

Figure 3.20 Thermal noise in a sampling circuit [1].

The on-resistance of the switch introduces thermal noise at the output and, when the switch turns off, this noise is stored on the capacitor along with the instantaneous value of the input voltage. It can be proved that the rms voltage of the sampled noise in this case is still

approximately equal to $\sqrt{\frac{kT}{C}}$. the problem of kT/C noise limits the performance in many high-precision applications. In order to achieve a low noise, the sampling capacitor must be sufficiently large, thus loading other circuits and degrading the speed.

3.2.5 Charge Injection Cancellation

The dependence of charge injection upon the input level and the trade-off expressed by equation(3.26) make it necessary to seek methods of cancelling the effect of charge injection so as to achieve a higher F. Let us consider a few such techniques here. To arrive at the first technique, the idea is that the charge injected by the main transistor can be removed by means of a second transistor. As shown in Fig. 3.20, a "dummy" switch, M_2, driven by $\overline{CK}$ is added to the circuit such that after M_1 turns off and M_2 turns on, the channel charge deposited by the former on C_H is absorbed by the latter to create a channel. Note that both the source and drain of M_2 are connected to the output node. It is ensured that the charge injected by M_1, Δq_1, is equal to that absorbed by M_2, Δq_1. Suppose half of the channel of M_1 is injected onto C_H, i.e.,

$$\Delta q_1 = \frac{W_1 L_1 C_{ox}}{2}(V_{CK} - V_{in} - V_{TH1}) \tag{3.28}$$

Since $\Delta q_2 = W_2 L_2 C_{ox}(V_{CK} - V_{in} - V_{TH1})$, if it is supposed that $W_2 = 0.5W_1$ and $L_2 = L_1$, then $\Delta q_2 = \Delta q_1$.

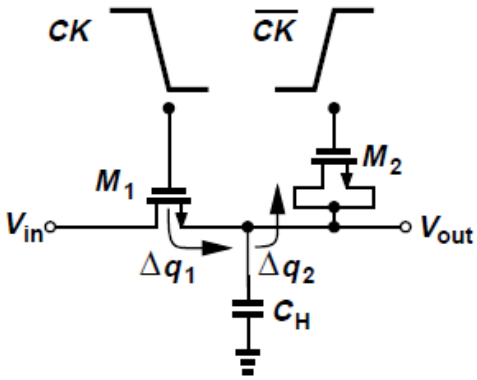


Figure 3.21. Addition of dummy device to reduce charge injection and clock feed-through [1].

Unfortunately, the assumption of equal splitting of charge between source and drain is generally invalid, making this approach less attractive. Interestingly, with the choice

$W_2 = 0.5W_1$ and $L_2 = L_1$, the effect of clock feedthrough is suppressed. As depicted in Fig. 3.22, the total charge in V_{out} is zero because

$$-V_{CK}\frac{W_1 C_{ov}}{W_1 C_{ov} + C_H + 2W_2 C_{ov}} + V_{CK}\frac{2W_2 C_{ov}}{W_1 C_{ov} + C_H + 2W_2 C_{ov}} = 0 \quad (3.29)$$

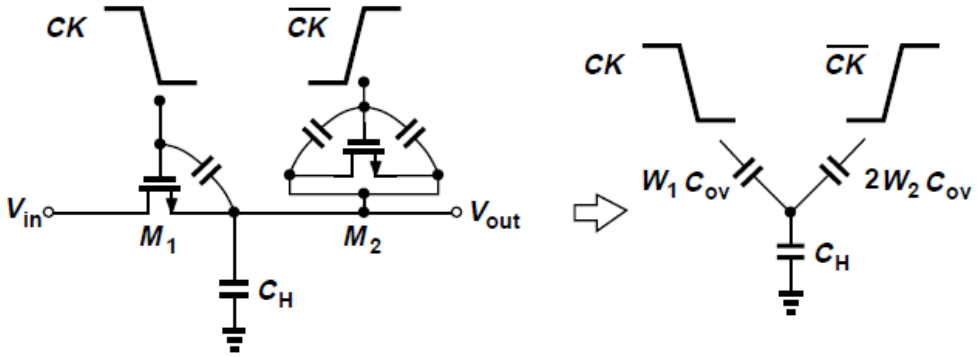


Figure 3.22 Clock feed-through suppression by dummy switch [1].

Another approach to lowering the effect of charge injection incorporates both PMOS and NMOS devices such that the opposite charge packets injected by the two cancel each other (Fig. 3.22).

For Δq_1 to cancelΔq_2, the following values need to be equal. i.e.,

$$W_1 L_1 C_{ox}(V_{CK} - V_{in} - V_{THN}) = W_2 L_2 C_{ox}(V_{in} - V_{THP})$$

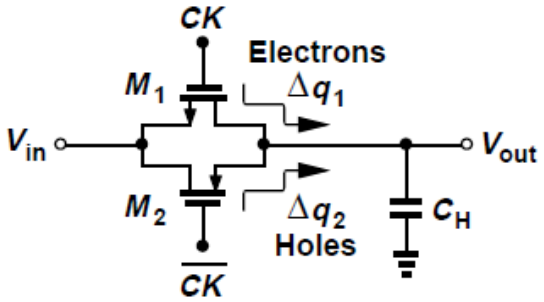


Figure 3.23 Use of complementary switches to reduce charge injection [1].

Thus, the cancellation occurs for only one input level. Even for clock feed through, the circuit does not provide complete cancellation because the gate-drain overlap capacitance of

NFETs is not equal to that of PFETs.

The knowledge of the advantages of differential circuits suggests that the problem of charge injection may be relieved through differential operation. As shown in Fig. 3.24, it is surmised that the charge injection appears as a common-mode disturbance. But, writing$\Delta q_1 = WLC_{ox}(V_{CK} - V_{in1} - V_{TH1})$ and $\Delta q_2 = WLC_{ox}(V_{CK} - V_{in2} - V_{TH2})$, it is clear that $\Delta q_1 = \Delta q_2$ only if $V_{in1} = V_{in2}$.

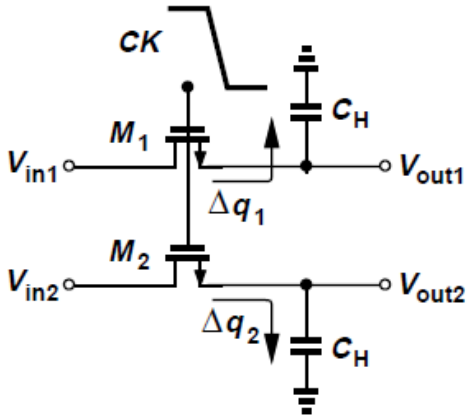


Figure 3.24 Differential sampling circuits [1].

In other words, the overall error is not suppressed for differential signals. Nevertheless, this technique removes the constant offset and lowers the nonlinear component.

CHAPTER4

Design of Operational Amplifier

Operational amplifiers (op-amps) are an integral part of many analog and mixed-signal systems. Op amps with vastly different levels of complexity are used to realize functions ranging from dc bias generation to high-speed amplification or filtering. The design of op amps continues to pose a challenge as the supply voltage and transistor channel lengths scale down with each generation of CMOS technologies.

4.1 General Considerations

Op amp is defined as a "high-gain differential amplifier". By the term "high" it means a value that is adequate for the application, typically10^1 to 10^5. Since op amps are usually employed to implement a feedback system, their open-loop gain is chosen according to the precision required of the closed-loop circuit.

4.2 Performance parameters

This section describes a number of op amp design parameters, providing an understanding of why and where each may become important. Various design parameters are:

Gain: The open-loop gain of an op-amp determines the precision of the feedback system employing the op amp. The required gain may vary by four orders of magnitude according to the application. Trading with parameters like speed and output voltage swings, the minimum required gain must therefore be known. High open-loop gain may also be necessary to suppress nonlinearity.

Small-Signal Bandwidth: The high-frequency behavior of op amps plays a critical role in many applications. For example, as the frequency of operation increases, the open loop gain begins to drop (Fig. 4.1), creating large errors in the feedback system. The small-signal bandwidth is usually defined as the "unity-gain" frequency, f_u , which 1 GHz in today's CMOS op amps. The 3-dB frequency, f_{3-dB}, may also be specified to allow easier prediction of the closed-loop frequency response.

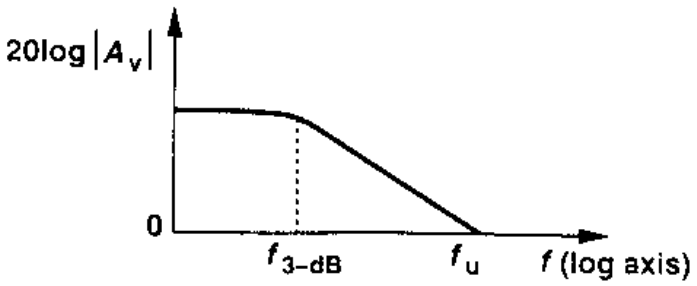


Figure 4.1 Gain roll off with frequency [1].

Output Swing: Most systems employing op amps require large voltage swings to accommodate a wide range of signal amplitudes. The need for large output swings has made fully differential op amps quite popular. The maximum voltage swing trades with device size and bias currents and hence speeds. Achieving large swings is the principal challenge in today's op amp design.

Linearity: Open-loop op amps suffer from substantial nonlinearity. In the circuit of Fig. 3.2, for example, the input pair $M_1 - M_2$ exhibits a non linear relationship between its differential drain

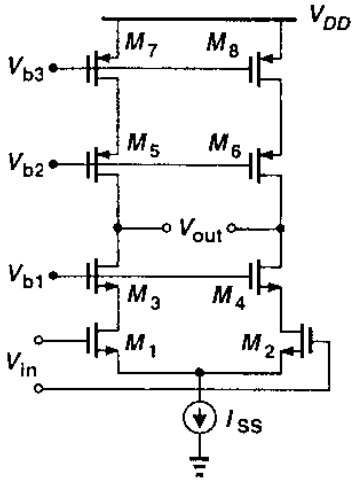


Figure 3.2 Cascode op amps [1].

current and input voltage. The issue of non linearity is tackled by two approaches: using fully differential implementations to suppress even-order harmonics and allowing sufficient open-loop gain such that the closed-loop feedback system achieves adequate linearity. It is interesting to note that in many feedback circuits, linearity requirement, rather than the gain error requirement, governs the choice of the open-loop gain.

Noise and offset: The input noise and offset of op amps determine the minimum signal level that can be processed with reasonable quality. In a typical op amp topology, several devices contribute noise and offset, necessitating large dimensions or bias currents. For example, in the circuit of Fig. 4.2, $M_1 - M_2$and $M_7 - M_8$ contribute the most. There is a trade-off between noise and output swing. For a given bias current, as the overdrive voltage of M_7 and M_8 in Fig. 4.2 is lowered to allow larger swings at the output, their trans-conductance increases and so does their drain noise current.

4.3 Types of Op amps.

Op amps are classified as:

1). One stage op amp.

2). Two- stage op amp

1). One stage op amp:

All the differential amplifiers can be considered as op amps. Fig 4.3 shows two such topologies with single-ended and differential outputs. The small signal, low frequency gain of both circuits is equal to$g_{mN}(r_{ON} \parallel r_{OP})$, where the subscripts $N\ and\ P$ denote NMOS and PMOS respectively. Note that the circuit of Fig. 4.3(a) exhibits a mirror pole whereas that of Fig. 4.3(b) does not, a critical difference in terms of the stability of feedback systems using these topologies. The circuits of Fig. 4.3 suffer from noise contributions of$M_1 - M_4$. In all op amp topologies, at least four devices contribute to the input noise: two input transistors and two load transistors. In order to achieve a high gain, differential cascode topologies can be used.

Telescopic op amp: Shown in Fig. 4.4(a) and (b) for single-ended and differential output generation, respectively, such circuits display a gain on the order of$g_{mN}[(g_{mN}{r_{ON}}^2) \parallel (g_{mP}{r_{OP}}^2)]$, but at the cost of output swing and additional poles. These configurations are also called “telescopic” cascade op amps to distinguish from another cascade op amp.

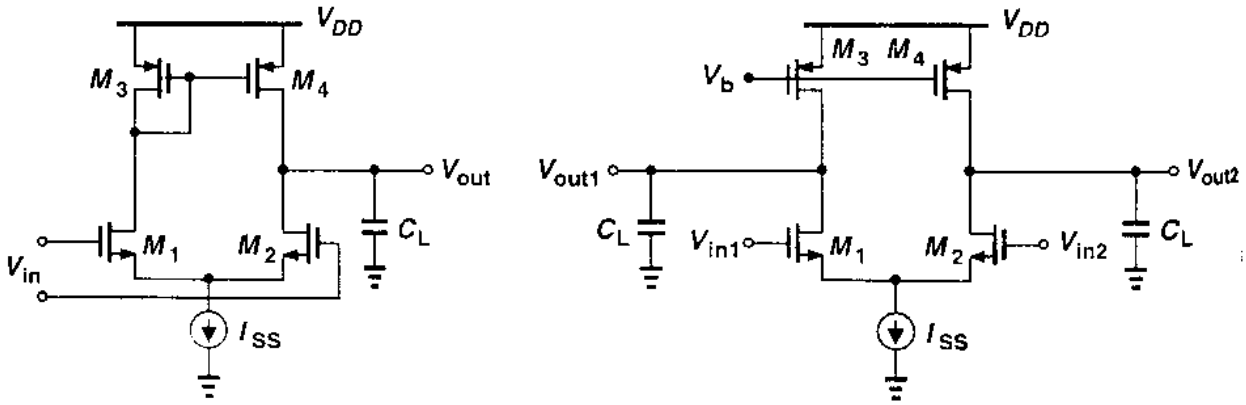
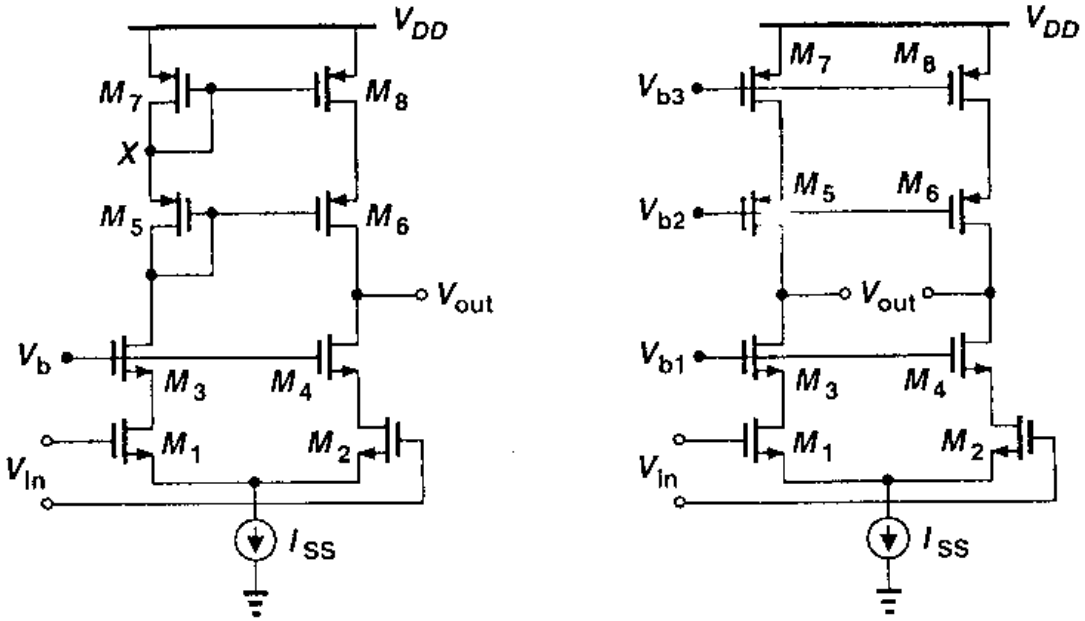


Figure 4.3 Simple op amp topologies [1].

The output swings of telescopic op amps are relatively limited. In the fully differential version of Fig. 4.4(b), the output swing is given by $2[V_{DD} - (V_{OD1} + V_{OD3} + V_{CSS} + |V_{OD5}| + |V_{OD7}|)]$, where V_{ODj} denotes the overdrive voltage of M_j.



(a) (b)

Figure 4.4 Cascode op amps [1].

Another major drawback of telescopic cascades is the difficulty in shorting their inputs and outputs. i.e., it is not possible to implement a unity gain buffer using this op amp topology. To understand this issue, let us consider the unity gain feedback topology shown in Fig. 4.5

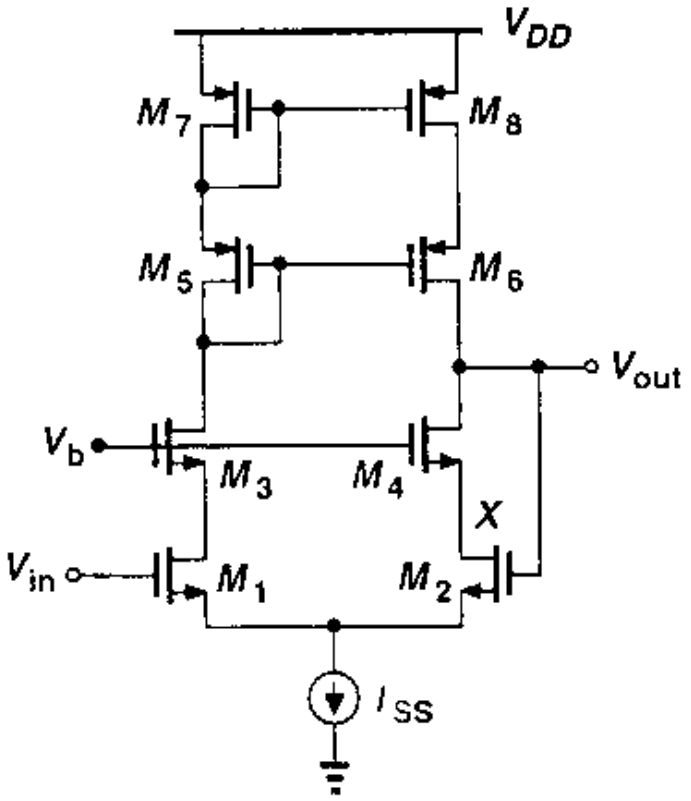


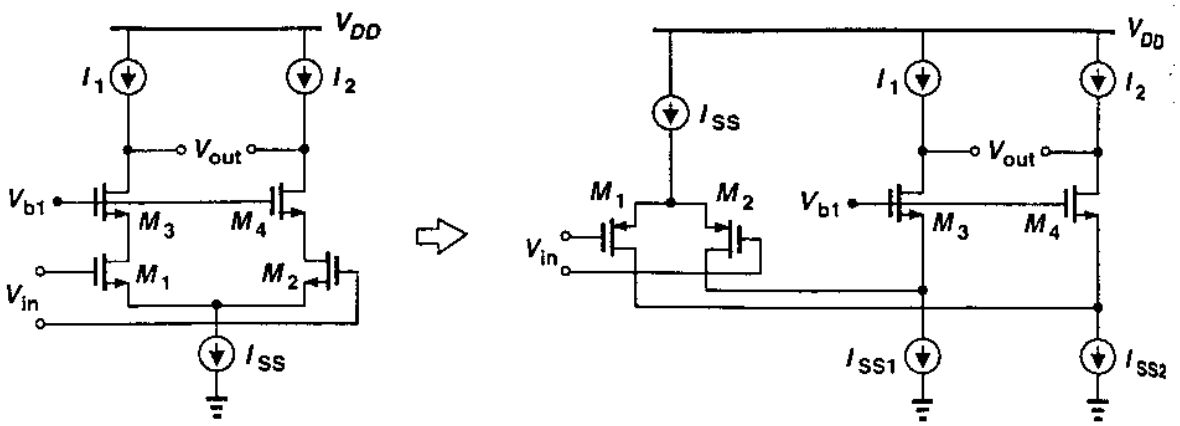
Figure 4.5 Cascode op amp with input and output shorted [1].

Let us find out the conditions when both M_2 and M_4 are in saturation. We must have $V_{out} \leq V_X + V_{TH2}$ and $V_{out} \geq V_b - V_{TH4}$.

Since, $V_X = V_b - V_{GS4}, V_b - V_{TH4} \leq V_{out} \leq V_b - V_{GS4} + V_{TH2}$. This voltage range is simply equal to $V_{max} - V_{min} = V_{TH4} - (V_{GS4} - V_{TH2})$, maximized by minimizing the overdrive of M_4 but always less than V_{TH2}.

Since, switched capacitor circuits require input and output to be shorted for a part of operation period; hence this configuration is not preferred for such applications.

Folded cascode op amp: In order to alleviate the drawbacks of telescopic op amps, namely limited output swings and difficulty in shorting the inputs and outputs, a "folded cascode" op amp is used. Folded cascade structure is formed by replacing the input device by the opposite type i.e. NMOS by PMOS and vice-versa while still converting the input voltage to a current. This folding is easily applied to differential pairs and hence op amps as well. Shown in Fig. 4.6, the resulting circuit replaces the input NMOS pair with a PMOS counterpart. Note the important difference between the two circuits.



(a) (b)

Figure 4.6 Folded cascode op amp topology [1]

(1). In Fig. 4.6(a), one bias current, I_{SS}, provides the drain current of both the input transistors and the cascode devices whereas in Fig. 4.6(b) the input pair requires an additional bias current. In other words, $I_{SS1} = \frac{I_{ss}}{2} + I_{D3}$. Thus, the folded cascode structure generally consumes higher power.

(2). In Fig. 4.6(a), the input CM level cannot exceed $V_{b1} - V_{GS3} + V_{TH1}$, whereas in Fig. 4.6(b), it cannot be less than $V_{b1} - V_{GS3} + |V_{THP}|$. It is therefore possible to design the latter to allow shorting its input and output terminals with negligible swing limitation. Hence, this op amp configuration is widely used for switched capacitor applications as folded cascode also behaves as a unity gain buffer.

The gain of folded cascode op amp is given by:

$$|A_v| \approx \{[(g_{m1} + g_{mb3})r_{o3}(r_{o1} \parallel r_{o5})] \parallel [(g_{m7} + g_{mb7})r_{o7}r_{o9}]\}. \quad (4.1)$$

(2). Two-stage op amp

The op amps studied above exhibit a “one-stage” nature in that they allow the small signal current produced by the input pair to flow directly through the output impedance. The gain of these topologies is therefore limited to the product of input pair tranconductance and the output impedance. Also, it is clear that cascoding in such circuits increases the gain while limiting the output swings. In some applications, gain and the output swing provided by cascode op amps are not adequate, in such cases two-stage op amps are preferred. Here, the first stage is designed to provide high gain and second stage provides large swing.

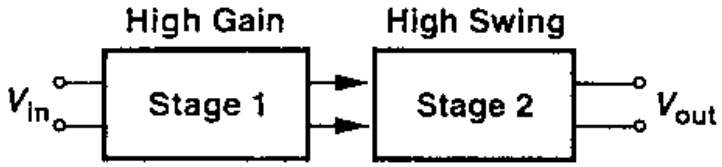


Figure 4.7 Two-stage op amp[1].

Since it provides high gain and high swing, but problem here is use of compensating capacitor in between the two stages. This compensating capacitor creates problem in terms of stability and hence compensating techniques are required.

Hence among above op amp topologies, folded cascode op amp is chosen for the design of switched capacitor based digital to analog converter.

Table 4.1 Comparison of performance of various op amp topologies.

Type of op amp	Gain	Output swing	Speed	Power dissipation	Noise
Telescopic	Medium	Medium	Highest	Low	Low
Folded-cascode	Medium	Medium	High	Medium	Medium
Two-stage	High	Highest	Low	Medium	Low

4.4 Op amp design for DAC

Out of various op amp architectures discussed above, folded cascode op amp is best suited for switched capacitor applications because it has advantages over both telescopic and two-stage op-amp.

In telescopic, there is a disadvantage that input and output cannot be shorted together, which is the basic requirement in switched-capacitor applications, but in folded cascode do, hence folded cascode is preferred.

In two-stage op-amp, various compensation techniques are required to increase the stability, which is not required in folded-cascode op-amp.

Because of above reasons, folded cascode op-amp is used in switched capacitor applications.

4.4.1 Designing of Folded cascode

Designing of folded cascode begins with the power budget. Folded cascode is designed by beginning with total power consumption of DAC to be 500μW. This power is divided between op-amp and switches. Since, folded cascode is used, it consumes more power than the other two configurations, hence this power is divided as 400 μW + 100 μW respectively. Op amps with high gain consume more power and hence, high gain op amps have power range in the order of few milli-watts. But in this thesis, the main emphasis is on low power, hence op amp with power consumption in the order of few microwatts is designed. Beginning with this given power, and using supply voltage of 1.8V in 0.18 μm n-well CMOS technology, value of total current flowing through the op amp is calculated. Input transistors are designed so that maximum current flows through them, as the input transistors decide the gain of op amp. Assuming overdrive voltage to be 0.2V, and using $\mu_n C_{ox} = 170.4 \mu A/V^2$ and $\mu_p C_{ox} = 40.5 \mu A/V^2$, the values of W/L of all transistors are calculated. Designed folded cascode is shown in Fig. 3.8. This folded cascode op amp is an important component in digital to analog converter (DAC). Since, digital to analog converter is designed for 8-bit resolution; hence, minimum op amp gain required is given by $2^N + 1$ i.e. 54.18 dB. Folded cascode shown in Fig. 3.8 is providing gain of 62.61 dB; hence it meets the minimum requirement of DAC. This op amp provides the phase margin of 82.7°.

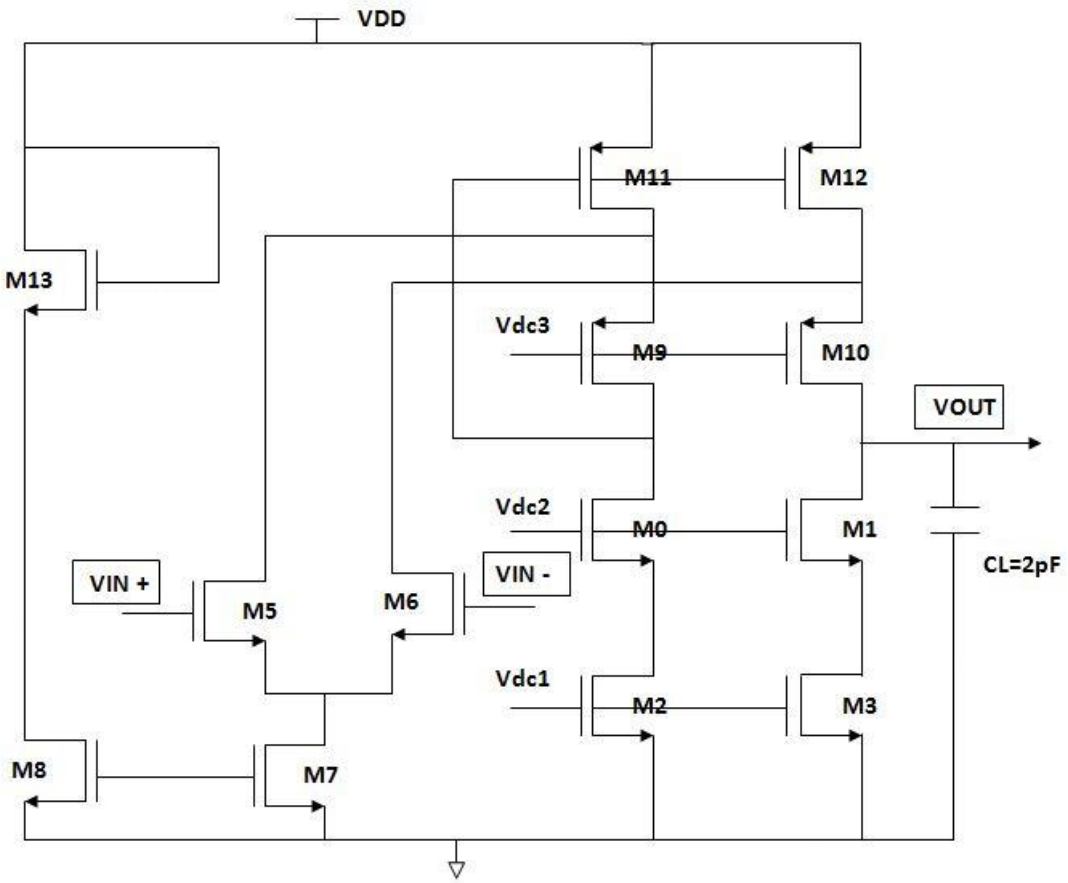


Figure 4.8 Schematic of Folded cascode op amps.

4.5 AC analysis of op amp

AC analysis of op amp is done by applying ac or sinusoidal signal at the input MOS terminal of op amp. The amplitude of this ac signal is set to '1' so that output when selected, directly gives the value of gain. And its operating point is set to 0.9V as this voltage keeps the input transistor in saturation and hence provides maximum gain.

The initial op-amp design begins with power even half of 400 μW. Though its power consumption is less, but it produces a gain which is not sufficient for 8-bit DAC. Hence, iterations are done on values of W/L to improve gain which meets the minimum DAC requirement as shown in Table 4.2. This increase in gain increases the power consumption too. The selected W/L values along with other obtained parameters are shown in Table 4.3.

Table 4.2 Variations of Op amp parameters

$(\frac{W}{L})_{0,1}$	$(\frac{W}{L})_{9,10}$	Gain(dB)	Phase margin(degrees)	Power(μW)
0.79/0.18	1.66/0.18	44.79	89	264.9
2.37/0.54	4.98/0.54	47	87.12	294.2
3.95/0.90	8.3/0.90	57.39	86	306.3
9.96/1.08	4.74/1.08	62.61	82.7	306.5

Table 4.3 Op amp obtained parameters

MOS	$\frac{W}{L}$	$g_m(\mu\Omega^{-1})$	$g_{ds}(\mu\Omega^{-1})$	$g_{mbs}(\mu\Omega^{-1})$	$r_{on}(\Omega)$	$V_{TH}(V)$	$V_{gs}(V)$	$V_{dsat}(V)$
M_0, M_1	9.96/1.08	147.9	1.748	26.04	65	425.9	550.3	136.8
M_2,M_3	1.58/0.36	144.5	7.629	26.02	19.47	486.5	600	140.4
M_5	7.08/0.54	434.2	6.233	67.05	35.77	482.4	590.3	134
M_6	7.08/0.54	434.2	6.233	67.05	35.77	482.4	590.3	134
M_7	3.16/0.18	676.5	52.83	101	4.672	514	638.3	152.7
M_8	3.16/0.18	783.9	36.32	115.8	7.98	502.7	638.3	159
M_9, M_{10}	4.74/1/08	101.5	762.1	31.21	40.08	-491.9	-695.1	-198.7
M_{11}, M_{12}	6.66/0.36	269.3	24.22	82.234	6.753	-513.4	-786	-277.2
M_{30}	0.28/0.18	153.1	12.69	14.57	14.52	485.8	1.162	421.8

Gain plot and phase plot of op amp at all process corners is shown from Fig. 4.9 to 4.14. This op amp is subjected to process variations. Gain, phase and 3-dB frequency obtained after corner analysis meets the minimum required specifications. Table 4.4 shows gain, phase and 3-dB frequency of an op amp at different corners.

Value of minimum gain required is given by

$$Gain = 2^{N+1} \qquad 4.2$$

where N is resolution of DAC in bits.

These values satisfy the minimum specifications: like minimum gain required is 54.18dB, minimum 3-dB of 5MHz as assumed. Hence the designed op amp performs well at all process corners.

Table 4.4 Op amp parameter variations at process corners.

Process corner	Gain(decibels)	Phase(degrees)	3-dB frequency(MHz)
TT	62.61	82.74	18.409
SS	68.65	81.40	14.856
FF	55.14	84.818	19.047
SF	55.14	84.818	19.047
FS	55.14	84.818	19.047

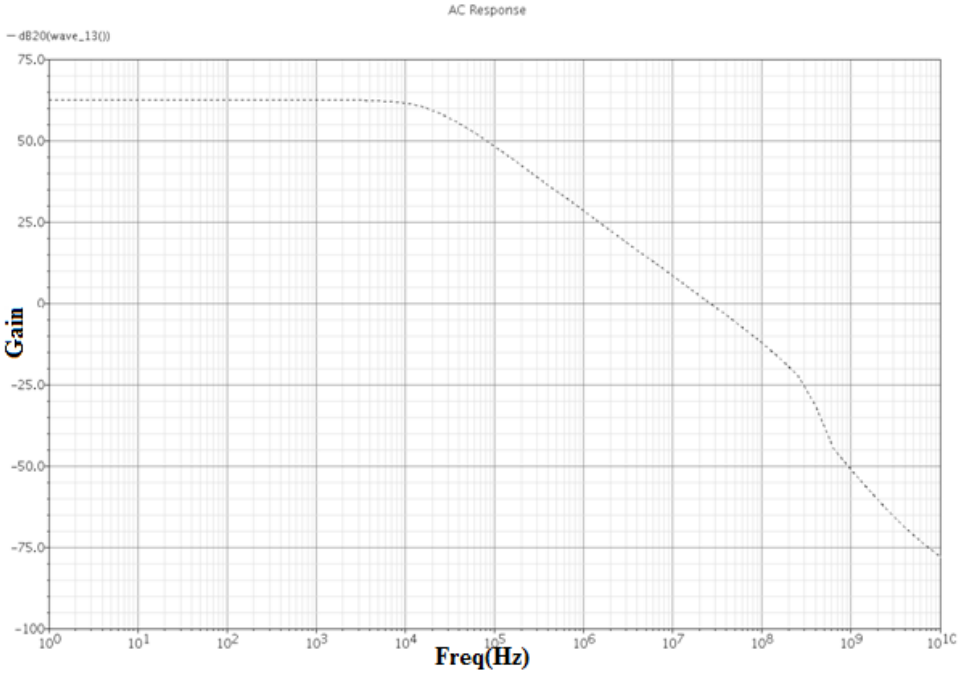


Figure 3.9 Gain plot of an op amp

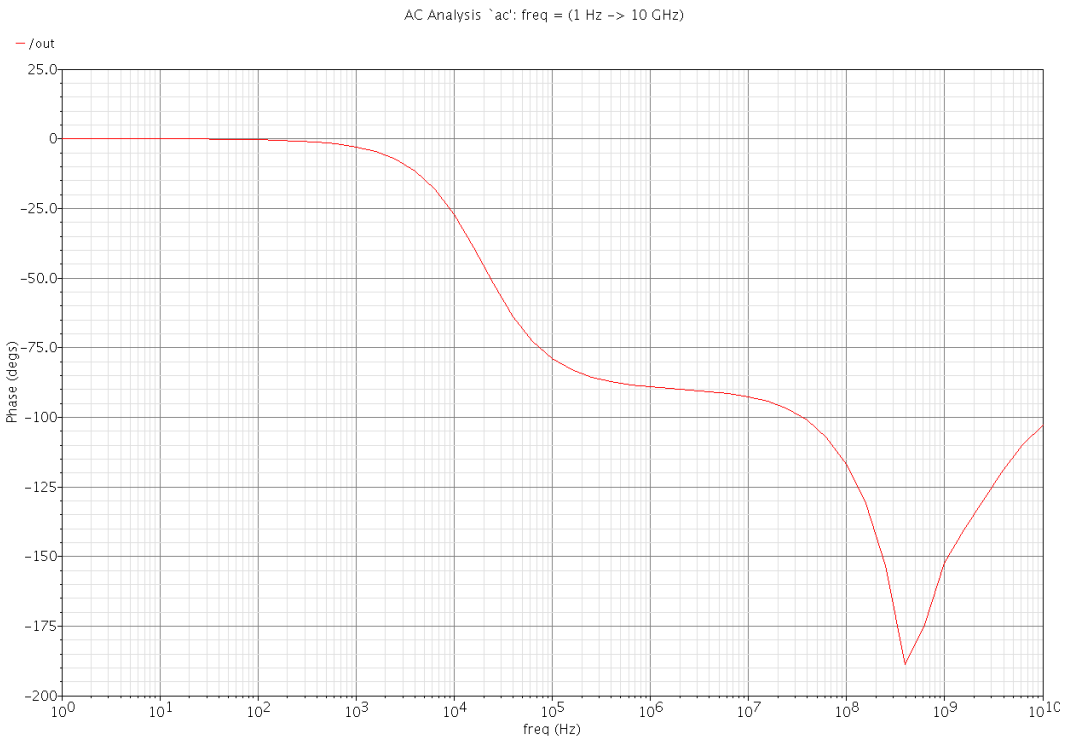


Figure 4.10 Phase plot of op amp.

4.6 DC analysis of op amp

DC analysis of op amp is done by replacing ac sinusoidal input only with fix dc bias voltage (common mode). The value of this voltage is also decided so as to keep transistors in saturation. DC analysis of op amp is shown in Fig. 4.15.

Fig. 4.15 shows variation of output voltage of op amp when subjected to common mode input voltage

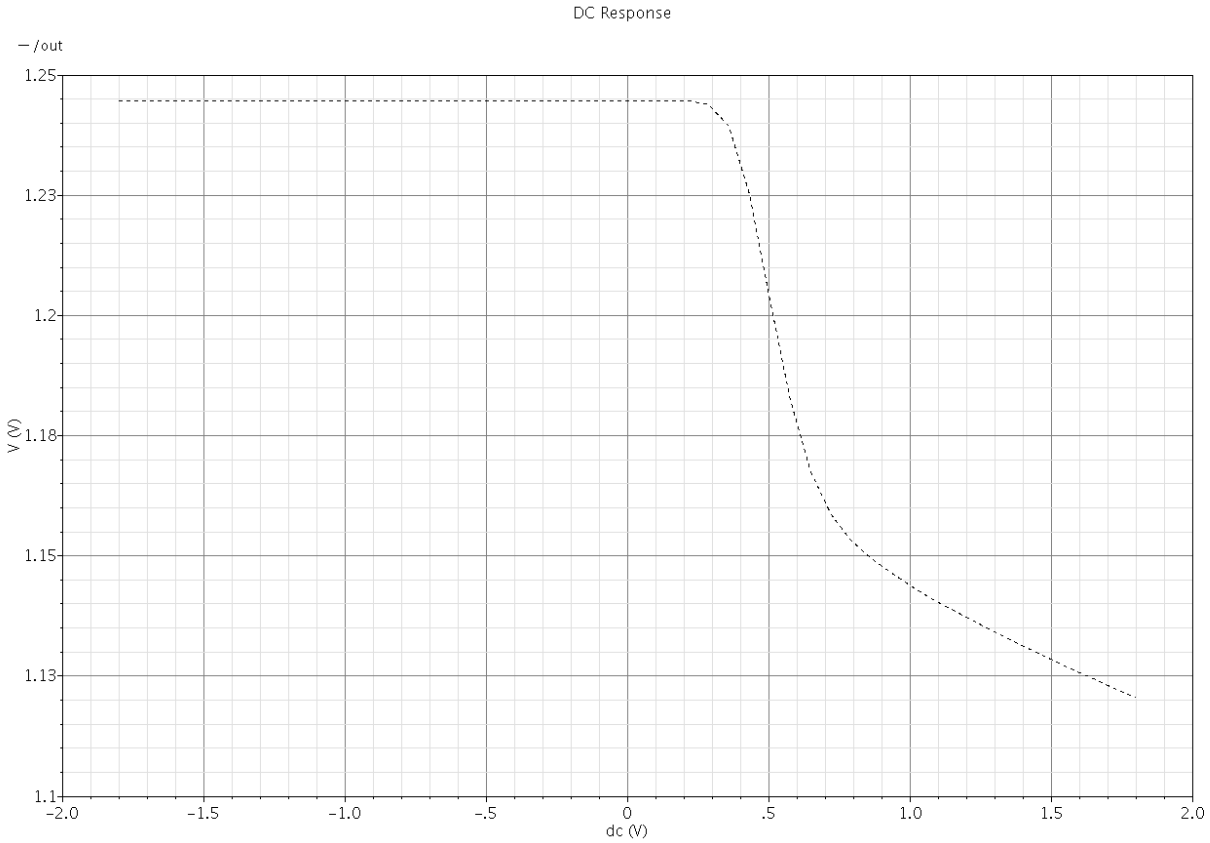


Figure 4.15 DC analysis of op amp.

Op amp symbol is generated and is shown in Fig. 4.16. This symbol is created from the schematic and it shows the same results as that shown by op amp schematic.

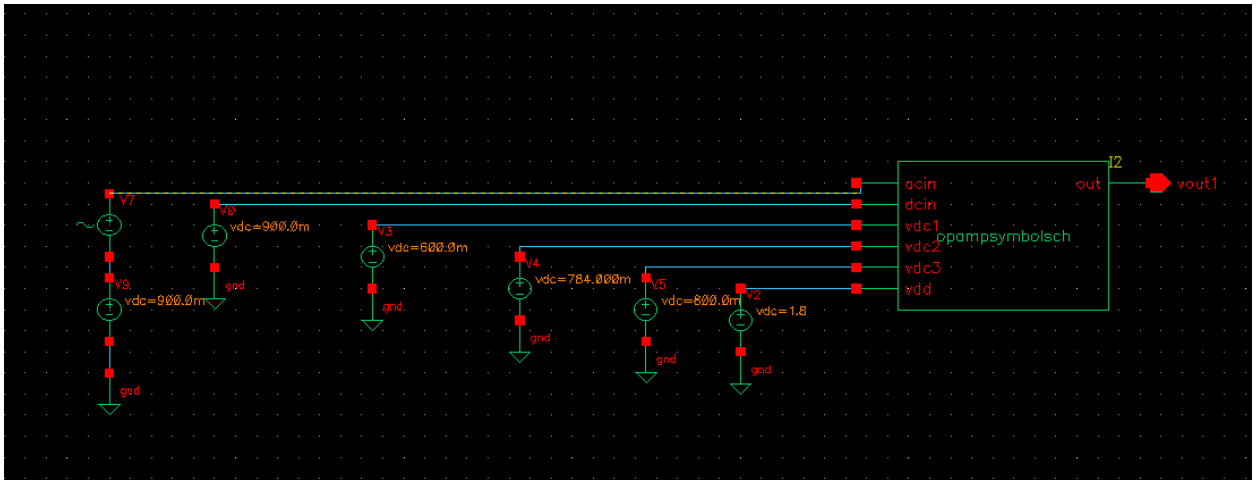


Figure 4.16 Op amp symbol.

4.7 Op amp layout

Layout of op amp is shown in Fig. 4.17.

Cadence Virtuoso XL Layout Editing Software is used for the layout design and DRC, LVS and RCX have been performed by using Cadence Assura.

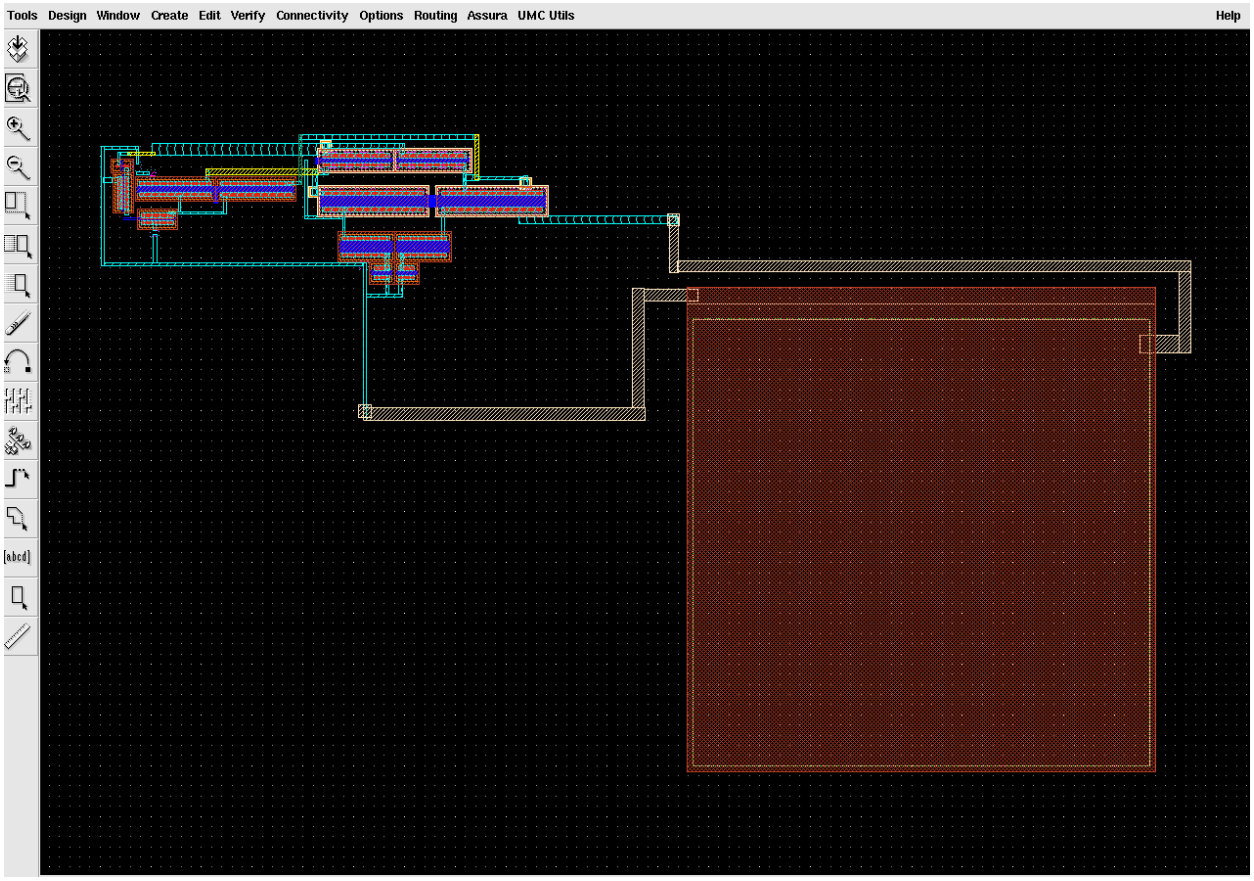


Figure 4.17 Op amp layouts.

CHAPTER 5

DIGITAL TO ANALOG CONVERTER (DAC) DESIGN

A low power 5MS/s switched capacitor DAC has been designed in 0.18μm CMOS n-well process. The resolution of DAC is taken to be 8-bit. The proposed DAC structure is shown in Fig. 1.13. Its practical implementation is shown in Fig. 5.1.

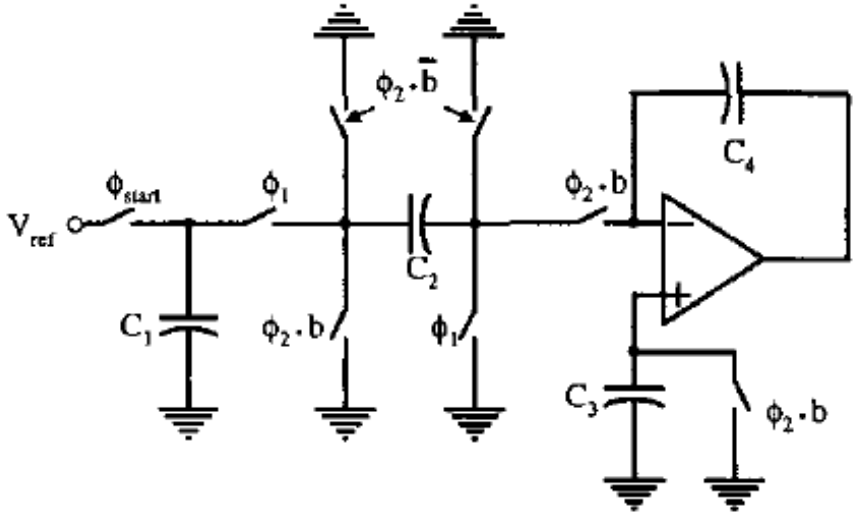


Figure 5.1 Practical implementation of proposed DAC.

All the switches are implemented by using transmission gate. Some switches are not shown for simplicity, like a switch connected between input and output of op amp etc.

5.1 Operation of DAC

Capacitors C_1 and C_2 are of the same size nominally. φ_1 and φ_2 are the two non- overlapping clocks enabled only when φ_{start} is low. The conversion process begins when φ_{start} is going high. This charges the capacitor C_1 to the reference voltage, V_{ref}. Once φ_{start} goes low, φ_1 and φ_2 are enabled. C_1 and C_2 forms capacitive divider network when φ_1 is on. The charge sampled on C_1 earlier during φ_{start} is equally divided between the two capacitors. During φ_2 , depending on the value of input digital bit b, the charge on C_2 is either transferred to C_4 or discarded. For an N-bit DAC, it takes N clock cycles to finish the conversion. At the end of N cycles, the output is available at the output of op amp. The output converging to its final value for an input of all 1's is shown in Fig. 5.2.

5.2 Design Specifications

Table 5.1 Various design parameters of DAC.

Parameters	Values
Technology	**Cadence UMC_180nm Technology**
Supply voltage	**1.8V**
Power	**< 500μW**
Resolution	**8-bits**
Sampling speed	**5MS/s**

CAD tools:

Schematic Entry: Cadence Schematic Entry Analog Design Environment

Simulator: Cadence SPECTRE

5.2 Design issues

Several factors can degrade the performance of the proposed design considerably. These design issues are:

5.2.1 Charge Injection

Charge injection from the switches limit the achievable accuracy from this architecture. To alleviate the problems associated with charge injection, the extra capacitor C_3 is added to the circuit. C_3 is made the same size as C_2. With the addition of this capacitor, charge injection effects are presented as common mode to the op amp and are removed by the common mode rejection ratio(CMRR) of op amp. Additionally, using fully differential architecture and dummy switches can also reduce the non linearities caused by charge injection.

5.2.2 Capacitor Sizing and Mismatch

The capacitor sizes will affect the total power consumption of the DAC. To minimize the power, it is desirable to minimize the size of the capacitors$C_1 - C_4$. However, the kT/C noise due to the capacitors considered along with the target resolution will dictate the size of the capacitors. Increasing the size of the capacitors will not only help with reducing the effects of charge injection but will also improve the matching of the critical capacitors. For higher resolution, the conversion can be done at half the speed with capacitor swap algorithm to eliminate capacitor mismatch effect.

5.2.3 Charge Leakage from the "Master" Capacitor

As explained earlier, the reference voltage is sampled on the "master" capacitor C_1 before the start of the conversion process. This capacitor can be viewed as a "bucket" from which charge is siphoned off for processing by the rest of the circuit. Any leakage of charge from this capacitor will show up directly as error in the output. Repeated charge injection from neighboring switches can also change the charge held by this capacitor. One way to reduce these errors is to make C_1 very large. However, this will require increasing the size of C_2 and C_3 as well resulting in increased power dissipation.

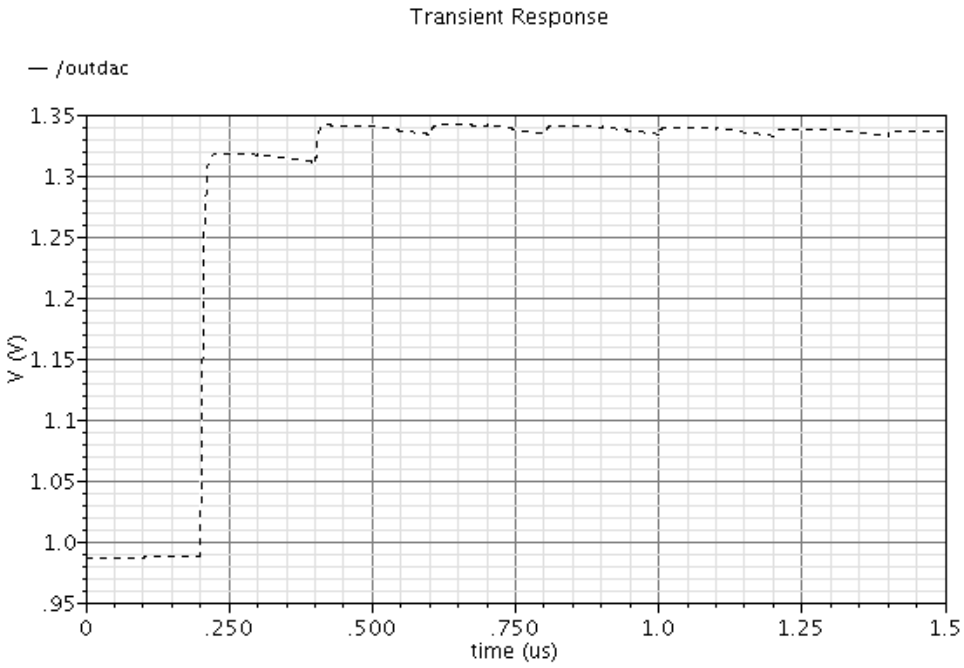


Figure 5.2 Charge leakage problem in DAC.

An alternate approach that does not require increasing the size of $C_1$is shown in Fig. 5.3. The capacitor C_1 of Fig. 5.1 is replaced by the network shown in Fig. 5. 3.

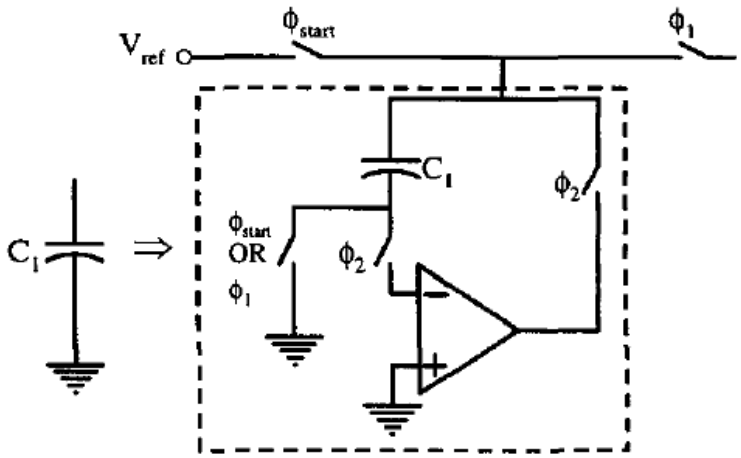


Figure 5.3 Schematic to hold charge accurately.

Duringφ_{start} , the reference voltage V_{ref} is sampled as before. Similarly, the circuit looks the same duringφ_1 . However, during φ_2 when the voltage on C_2 is being processed, the master capacitorC_1, is placed in the feedback loop of an opamp forcing the voltage acrossC_1, to remain constant. Any perturbations due to charge injection of charge loss from C_1 are compensated by the op amp. As a result, the charge corresponding to the reference voltage sampled acrossC_1, at the start of the conversion process can be held more accurately.

The output of DAC after replacing capacitor C_1 with the circuit given in Fig. 5.3 is shown in Fig. 5.4.

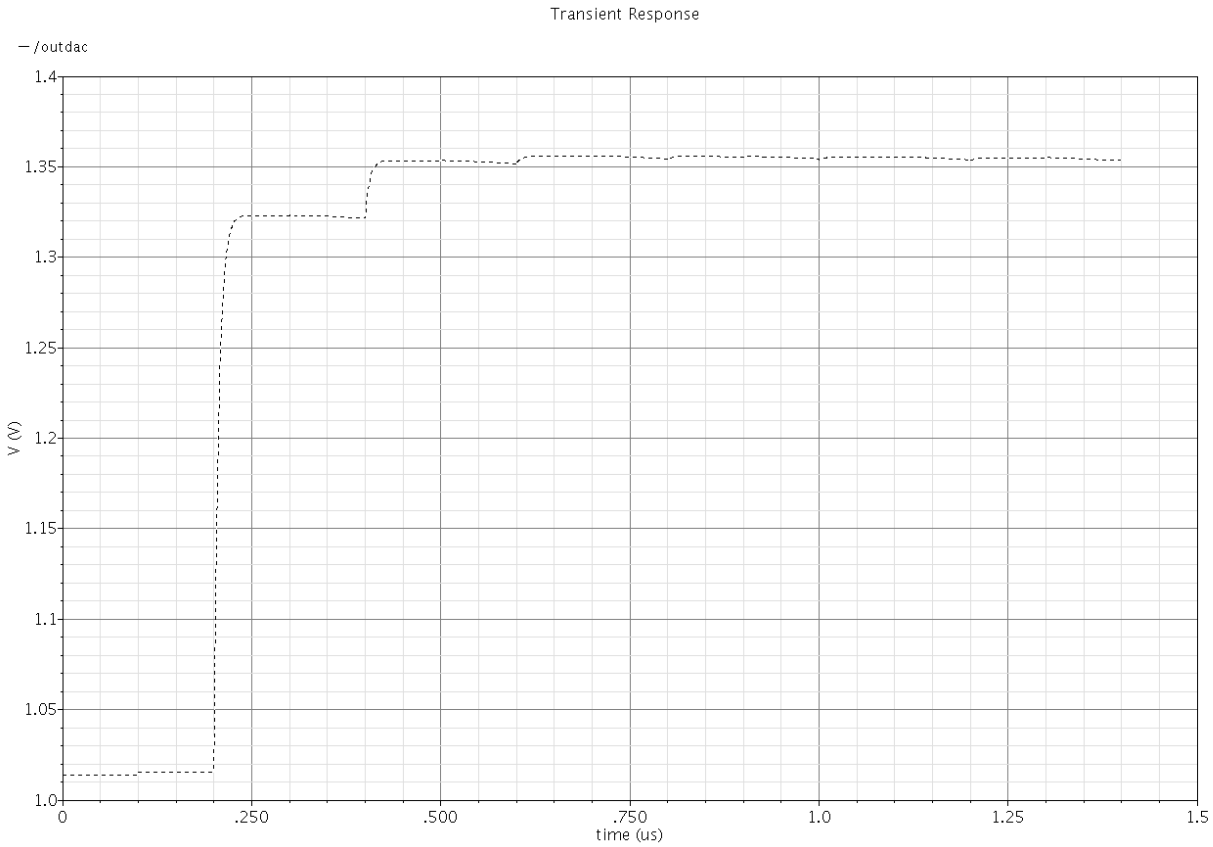


Figure 5.4 Typical DAC characteristics.

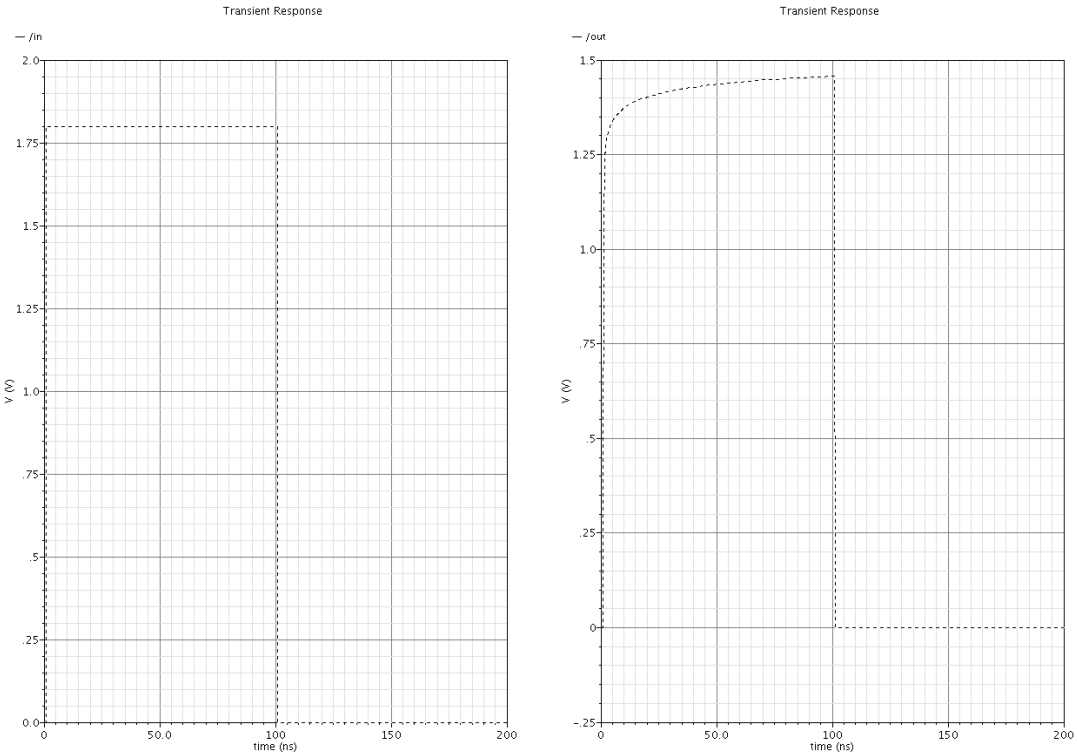
5.2.4 Switch Designing

The switches are designed using transmission gate. On resistance of switch is calculated and further, using the equation 3.16, we have

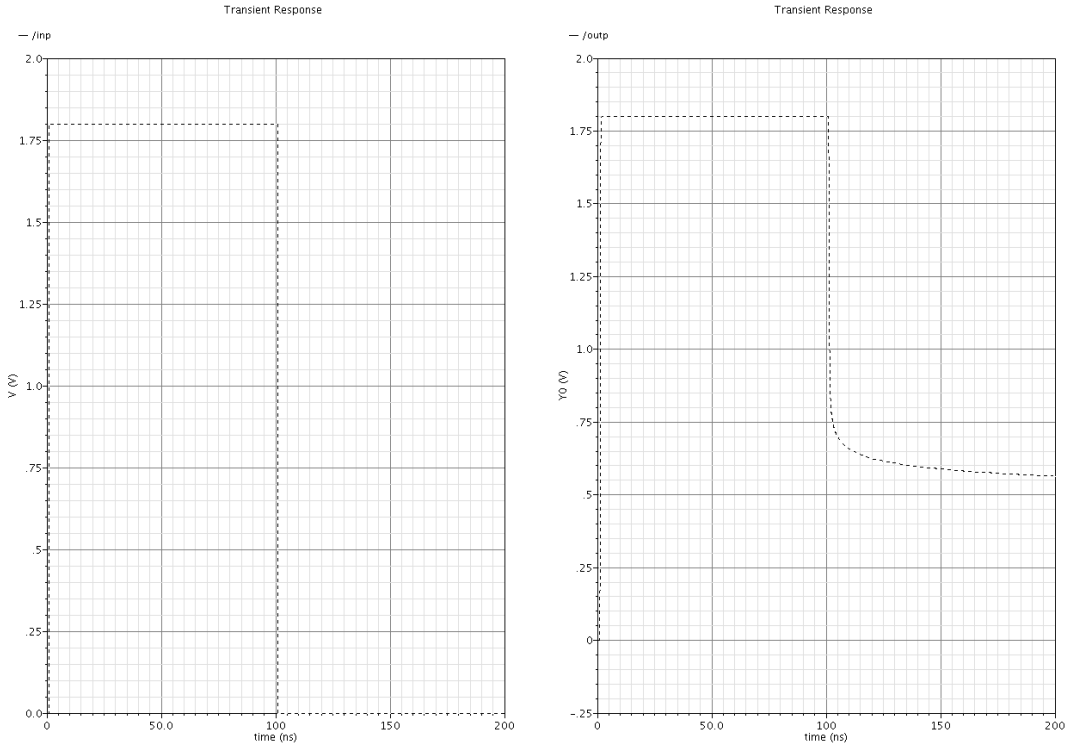
$$RC = 18ns$$

value of capacitor "C" is determined.

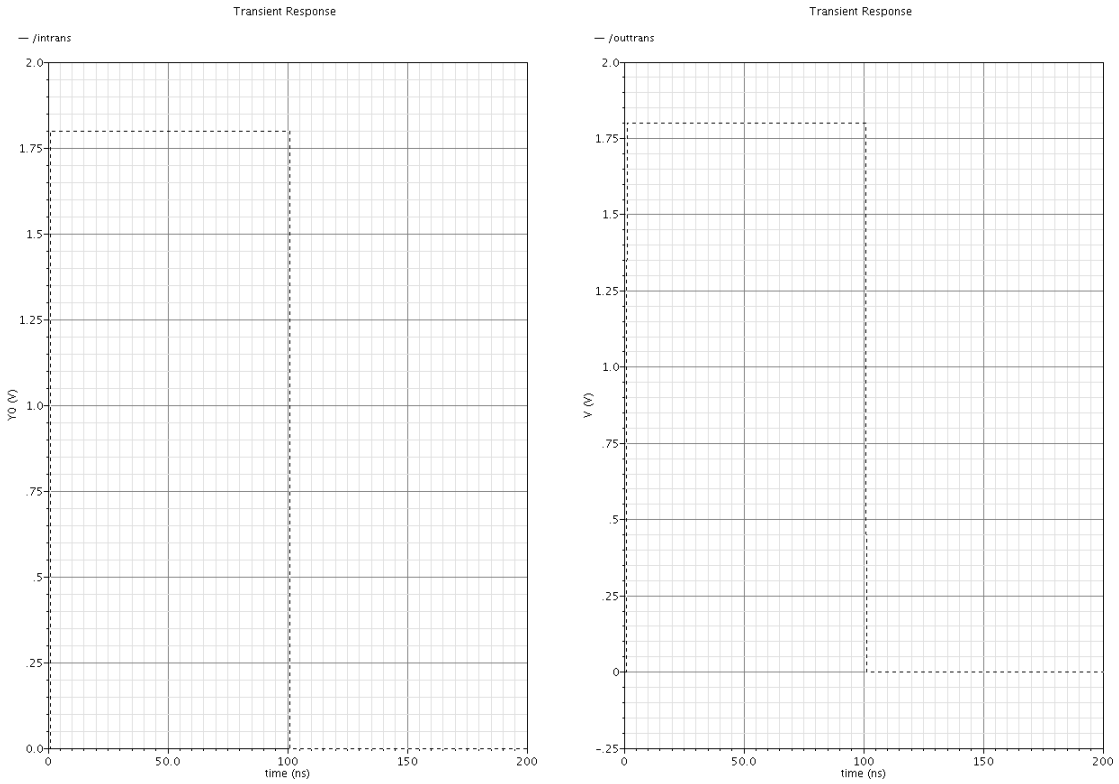
The switches are implemented using transmission gates as discussed earlier. The outputs of PMOS, NMOS and transmission gates as switch is shown in Fig. 5.5(a), (b) and (c).


Transient Response
— /in
V (V)
time (ns)
Transient Response
— /out
V (V)
time (ns)

(a)


Transient Response
— /inp
V (V)
time (ns)
Transient Response
— /outp
YO (V)
time (ns)

(b)



(c)

Figure 5.5 Outputs of PMOS, NMOS, Transmission gate acting as a switch.

Hence, from Fig 5.5(c), it is clear that in transmission gate, when switch is on, the output resembles the input. Hence, transmission gate is preferred for switched capacitor DAC.

Switch φ_{start} is implemented using PMOS, because it is turned on in the beginning for 100ns to reset all switches, but after this time period, it is turned off. Hence logic '1' is required at the beginning, so PMOS is preferred. Remaining switches are implemented using transmission gate. The W/L ratios of switches along with their equivalent resistance is shown in Table 5.2

Table 5.2 Various switch parameters.

Components	$(W/L)_p$	$(W/L)_n$	Resistance(r_{on})
φ_{start}	900/180	-	2.887K
φ_1	900/180	270/180	2.073K
φ_2	900/180	270/180	2.073K

Table 5.3 Various Capacitor parameters.

Component	Value (in *p*F)	Width(in μm)	Length(in μm)
C_1	6.92	71	28.8
C_2	6.92	71	28.8
C_3	3.075	12.6	28.8
C_4	3.075	12.6	28.8

5.2.5 Amplifier gain and offset errors

The amplifier used in the proposed DAC can become the performance bottleneck. The maximum DAC accuracy that can be reached is limited by the amplifier's open loop gain. The maximum gain error allowed should always be less than half least significant bit(LSB) value .i.e,

$$G_{error} = \frac{1}{A_0 . \beta} < \frac{1}{2} LSB \qquad (5.1)$$

where A_0 is the amplifier DC gain and β is the feedback factor. A more strict condition is justified if there are many sources of errors in the switching scheme. The overall DAC offset will depend on the amplifier's offset. However, these offset issues can be resolved by the external switched capacitor circuit. In this design, the amplifier used is a folded cascode as discussed earlier with a gain of 62.71dB, which means that the maximum accuracy that can be achieved is 9-bit. Gain and phase plot of folded cascode op amp is shown in Fig. 5.5.

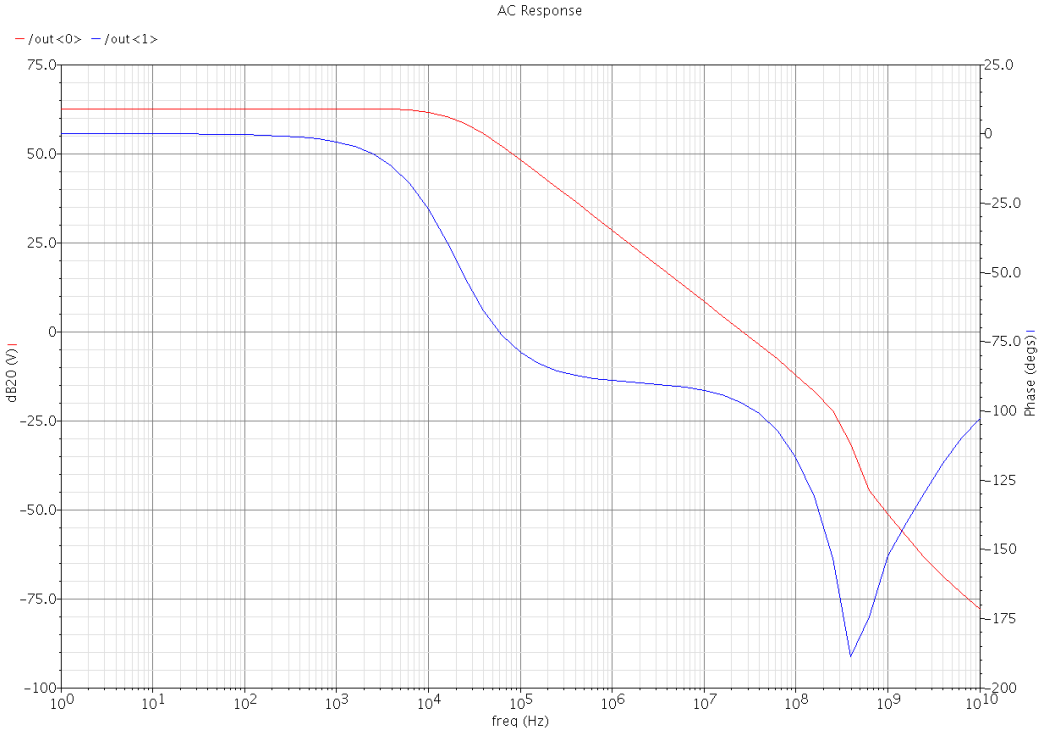


Figure 5.6 Gain and phase plot of op amp.

5.2.5 Corner Analysis of DAC

Designed DAC is made to run at all process corners and the given DAC fulfils the minimum requirements. Clock used in the circuit is shown in Fig. 5.7. The transient analysis of DAC at different corners is shown in Fig. 5.8 (a), (b) and (c).

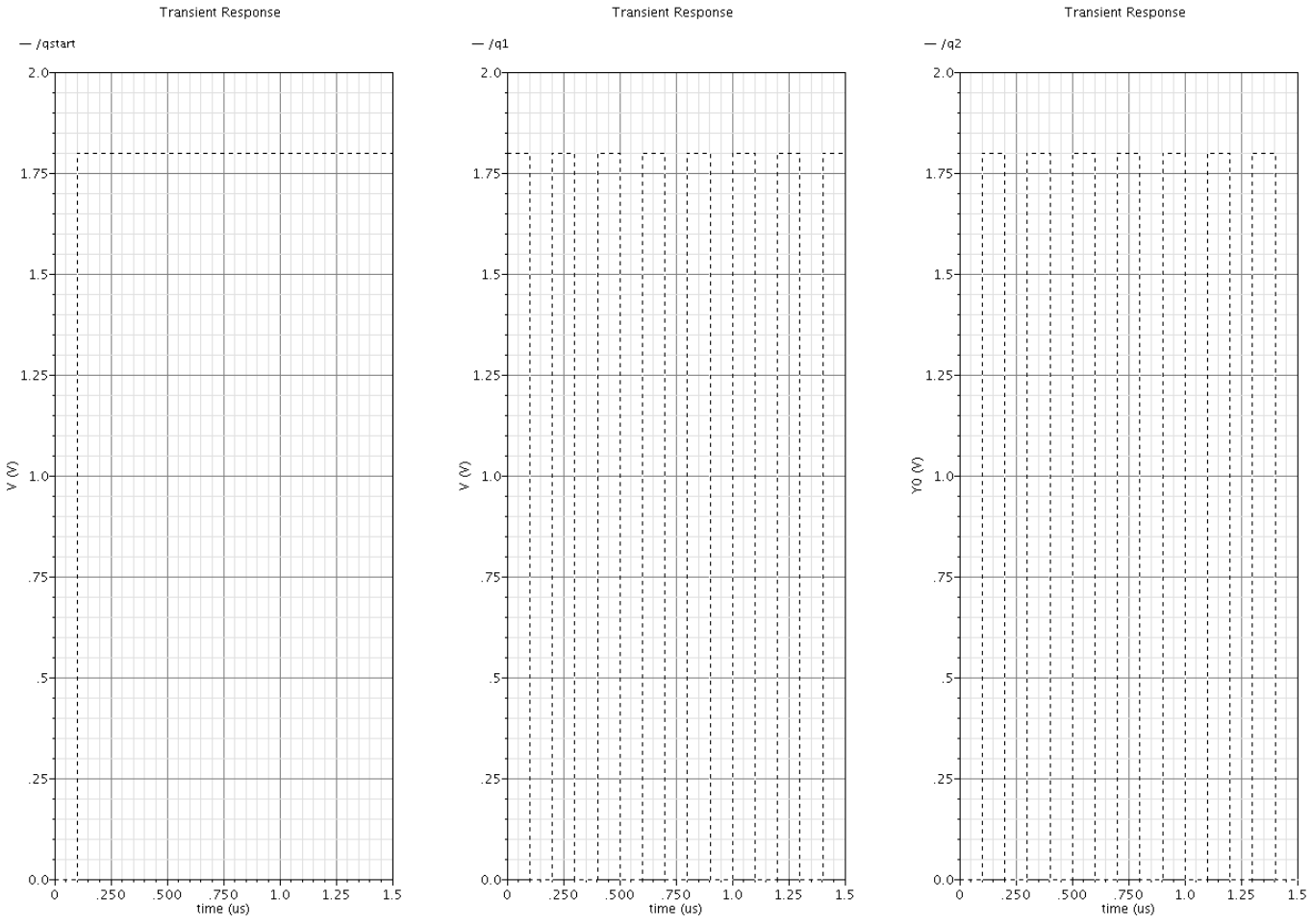


Figure 5.7 Circuit clocks.

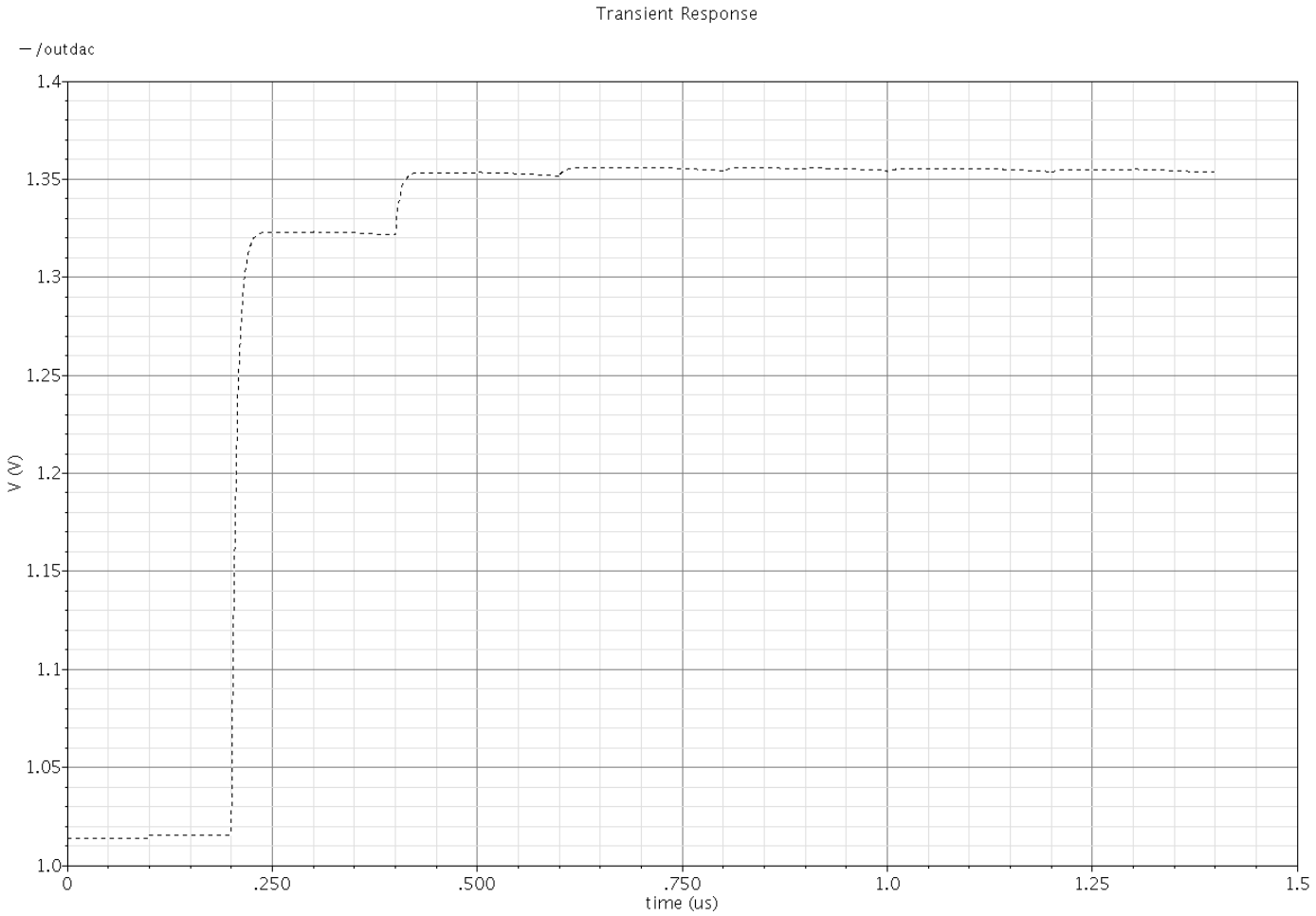


Figure 5.8 (a) DAC characteristic at TT corner.

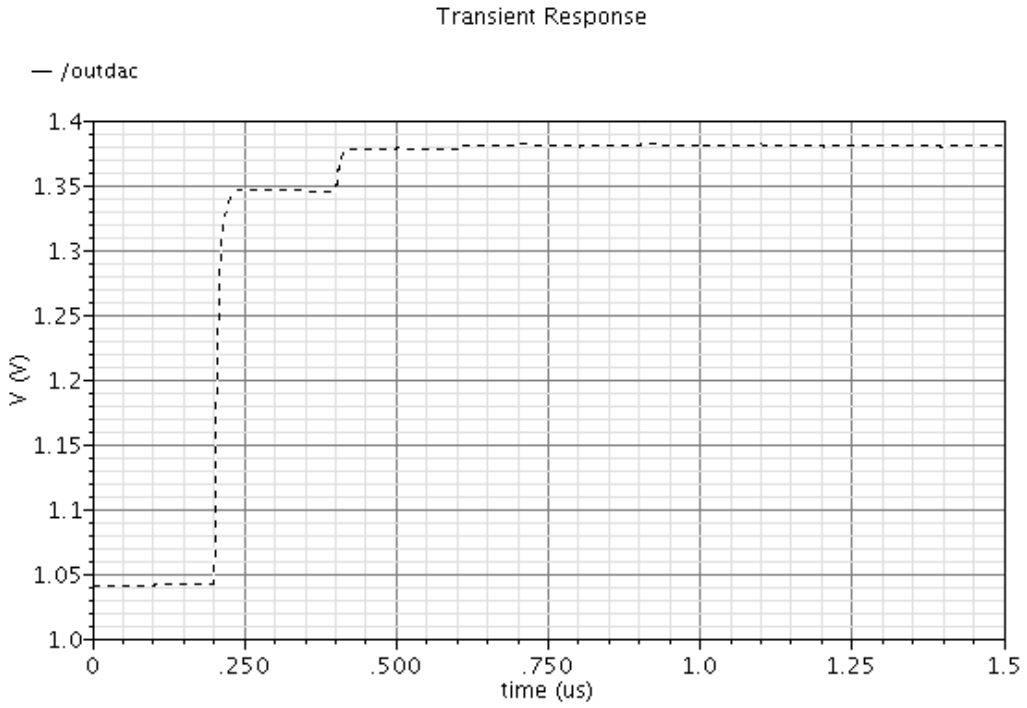


Figure 5.8 (b) DAC characteristics at SS corner

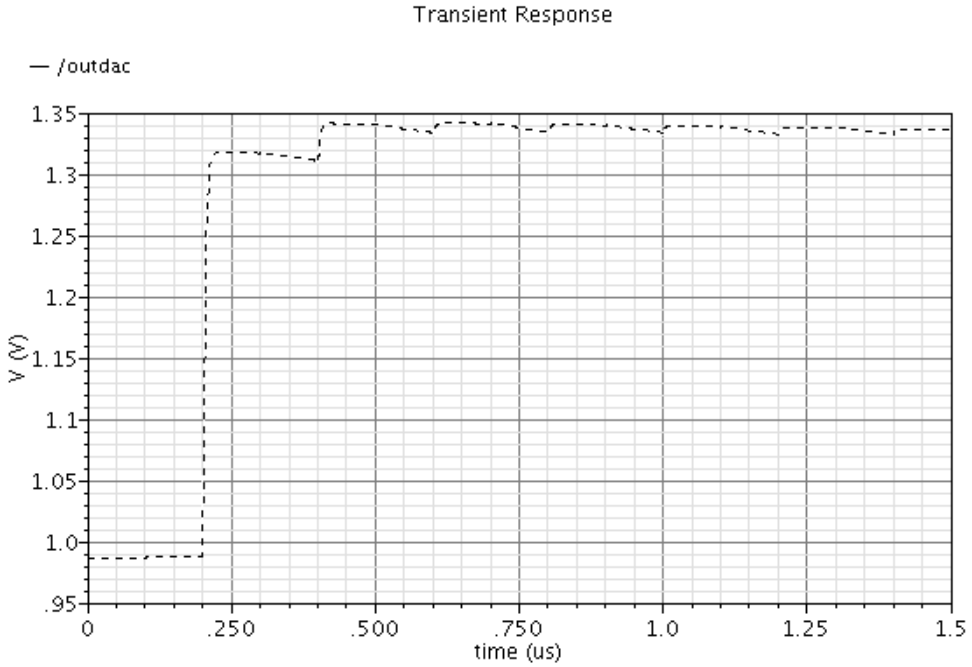


Figure 5.8 (c) DAC characteristics at FF corner.

5.2.6 Power consumption of DAC

The DAC is designed for low power consumption. Previous work on DAC consumes the

power in the order of milli-watts, but this DAC consumes very low power of 493.8uW.

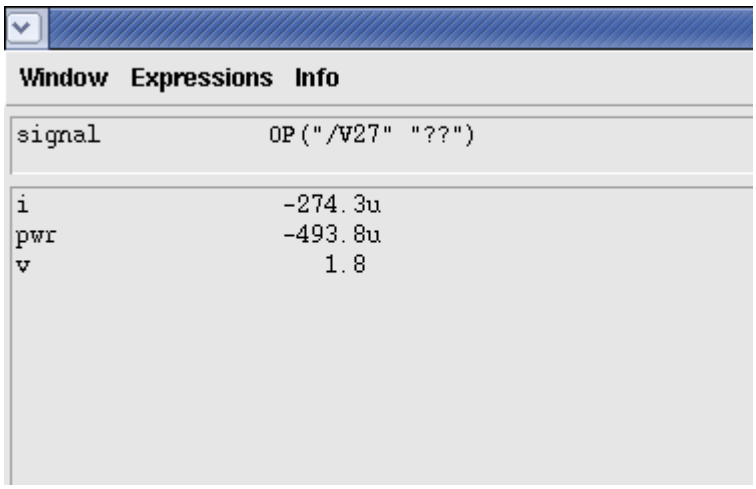


Figure 5.9 Power consumption of DAC.

5.4 DAC Layout

Cadence Virtuoso XL Layout Editing Software is used for the layout design and DRC, LVS and RCX have been performed by using Cadence Assura.

The layout of DAC satisfies the minimum design rules. The designed layout is free from DRC errors. Layout of DAC is as shown in Fig. 5.10

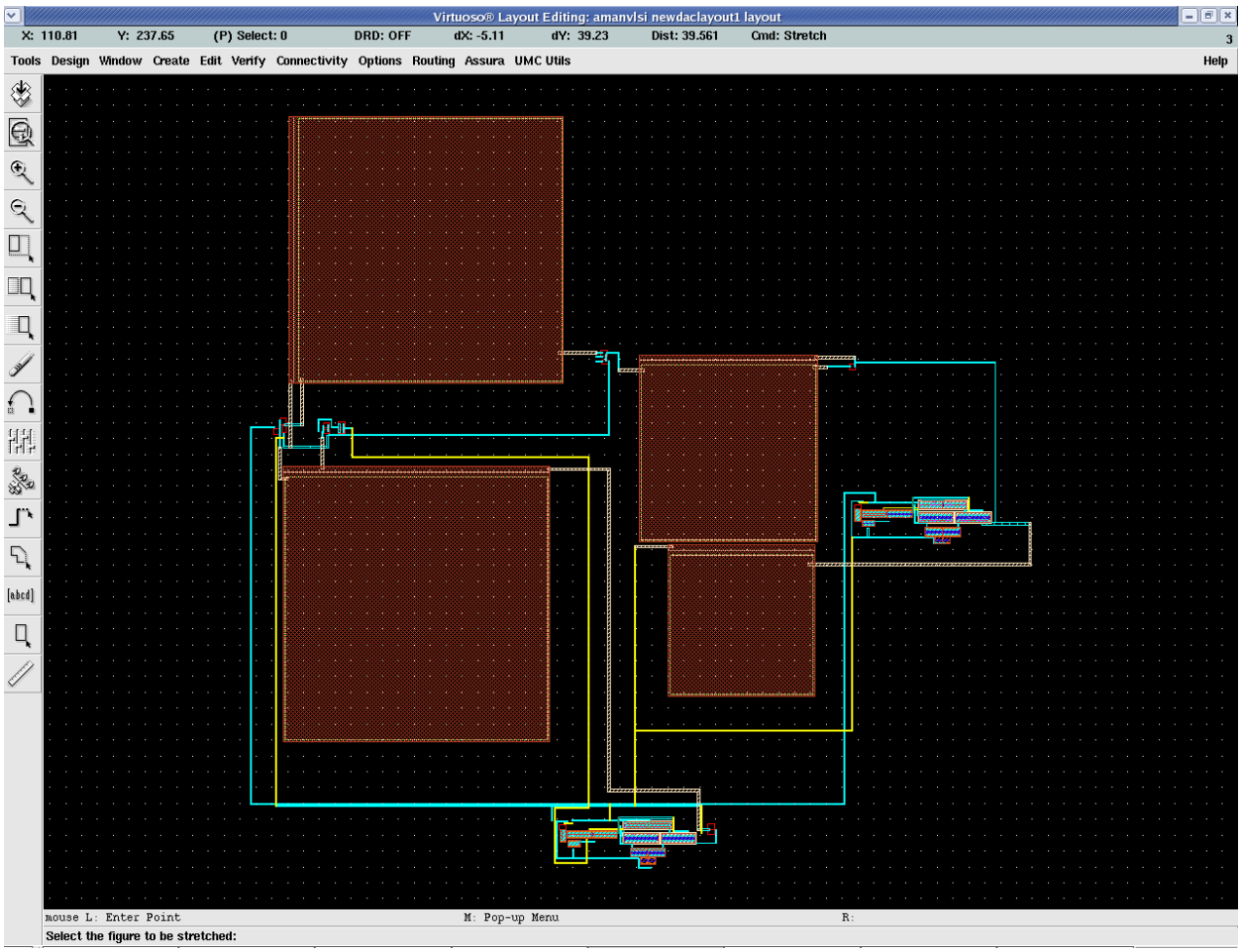


Figure 5.10 Layout of DAC

5.5 DAC Parameter extraction.

DAC extracted view is shown in Fig. 5.11.

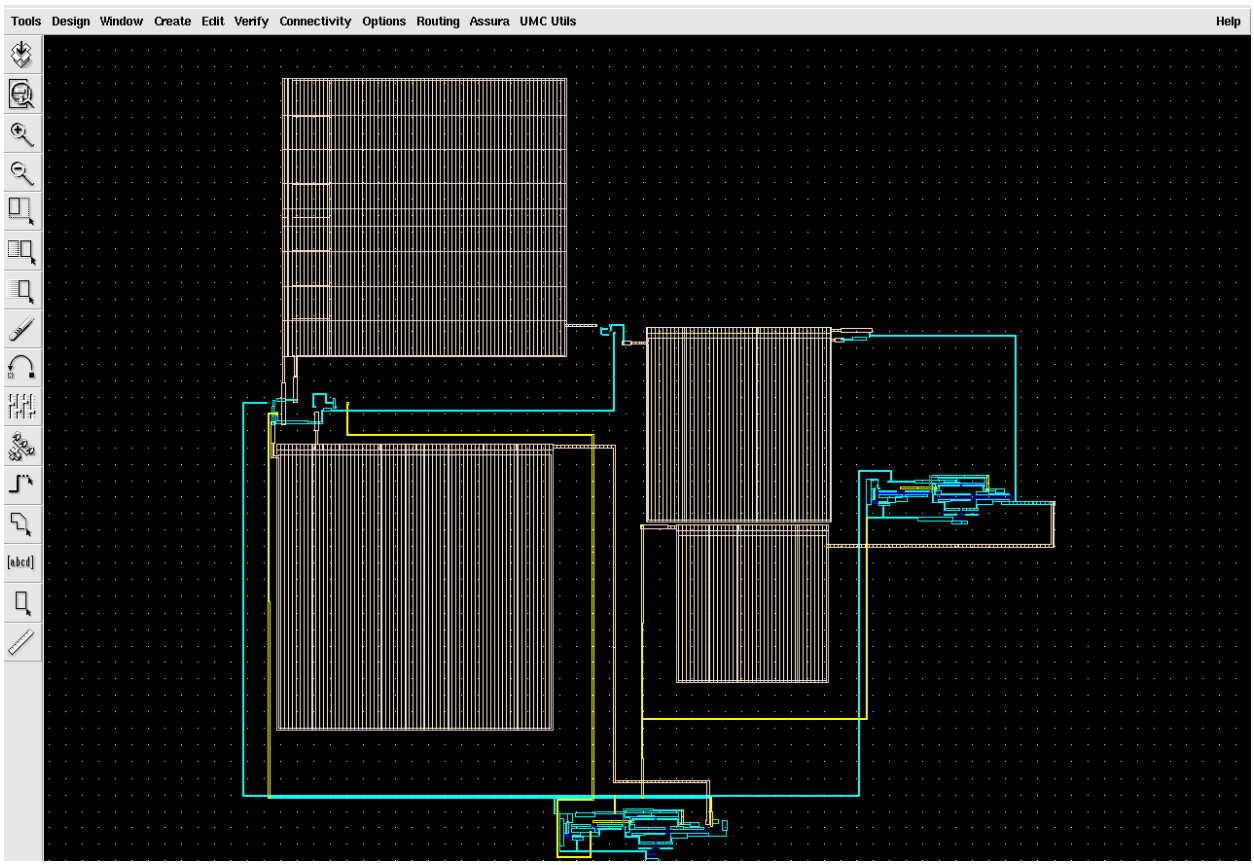


Figure 5.11 DAC extracted view.

CHAPTER 6

CONCLUSION AND FUTURE SCOPE

6.1 Conclusion

In this thesis, a digital to analog converter (DAC) for Successive Approximation Analog to Digital Converter (SAR ADC) has been investigated and designed. The design is mainly optimized for the low power, moderate resolution and moderate speed. Folded cascode op amp is chosen as a basic component because of its advantages over other amplifiers. Switched capacitor based DAC is simulated with UMC 180nm CMOS technology.

The DAC is designed for resolution of 8-bit. Sampling speed is taken to be 5MS/s and power dissipation achieved is 493.8 μW. The output of DAC converges to the final value without decreasing from its previous analog value.

6.2 Future Scope of Work

Simulation results shows that DAC dissipates power of 493.8 μW and output of DAC increases for input'1'. The conversion starts from MSB and the output voltage is obtained using a switched capacitor integrator. Few of design issues that limit its performance have been discussed. Although no concern on linearity is specifically addressed, various techniques can be used for its improvement also. Such enhancements as well as the design of the improved DAC can be included in the future work. Since the designed DAC failed at SF corner and FS corner because the output of DAC decreases even for "1" input. This problem may be due to charge leakage through capacitor C_1 , hence improved charge storage circuit need to be designed to extend this work in future. Further scaling of technology will also led to change in calculated parameters. Hence, technology scaling can also be the future scope of this work.

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