ESTIMATION OF NOISE IN HIGH PERFORMANCE VLSI CIRCUITS

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CERTIFICATE

I, **Pawan Kumar Singh,** hereby declare that the thesis entitled, **"Estimation of Noise in High Performance VLSI Circuits,"** submitted to Thapar University, Patiala, in partial fulfillment of the requirement for the award of the Degree of **Doctor of Philosophy** in **the Electronics and Communication Engineering** is and authentic record of my original and independent research work carried out under the supervision and guidance of **Prof. (Dr.) Sanjay Sharma,** Head, ECED, Thapar University, Patiala and refers other researcher's work which are duly listed in the reference section.

The matter embodied in this thesis has not been formed the basis for the award of any Degree/Diploma/Associate-ship/Fellowship or other similar title to any candidate of this or any other university.

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ABSTRACT

Integrated circuit manufacturing industries are striving for cost effective, compact and handheld products in recent years. Therefore, the integration of digital circuits and analog/RF circuits over a common substrate is a viable solution. The system in which the digital and analog/RF block are sharing a common substrate, experiences an unwanted interaction amongst the various blocks. The switching activities in digital circuits inject noise in the substrate which is propagated through the common substrate to the sensitive analog circuits. This substrate noise coupling can therefore degrade the performance of the entire chip. Therefore, the accurate substrate modeling technique is a prime requirement for the analysis of substrate coupling in complex VLSI circuits. Existing substrate modeling techniques were either based on two dimensional simulations which are not sufficient since the substrate problem is inherently three dimensional, or required extraction of empirical parameters which make the models less predictable.

In this thesis, a compact and more accurate substrate macromodel is proposed for the estimation of the substrate noise which encapsulates interactions amongst various types of circuits integrated on a System-on-Chip (SoC). This substrate macromodel is mainly dealing with resistive behavior of the substrate and by using the same resistive behavior of the substrate, the macromodel for the uniformly doped substrate as well as for multilayer substrate is developed to analyze the substrate noise coupling between the source and sensor circuits. These macromodels can further be used in complex VLSI circuits to estimate their performance in the presence of substrate noise coupling. The macromodel for the substrate is generics for all types of substrates, but the circuit macromodel is unique for every circuit. The variation in the performance of MOSFET devices in the presence of substrate coupling is presented to discerning the effect of substrate coupling in the MOSFET operation.

The complex VLSI circuits are decomposed in small sections (standard cells) for their truthful analysis of substrate noise coupling and these small sections are further combined to develop the original circuit. To estimate the noise in the standard cell, a gate-level circuit macromodel is developed and is further simplified by combining the effects of parasitics. This simplified gate-level circuit macromodel is combined with the substrate macromodel and is then used in circuit simulator to estimate the substrate noise. The validation of this approach is done by applying it on a chain of five CMOS inverters, which are integrated over a high resistive substrate and the overall system is simulated for substrate noise potential which is varying from – 0.6 mV to + 0.6 mV with a capacitive load of 0.6 nH. The above performed technique is further used for the simulation of substrate current in a CMOS inverter which is integrated over a high resistive substrate. A pulse shaped signal with rise and fall delay of 1 ns is applied at the input of the inverter and substrate current is observed at each high-to-low and low-to-high transitions of the input signal. It is observed that as there is advancement in down scaling technology, the substrate current and hence the substrate potential will be more prominent.

Furthermore, a novel methodology is proposed to estimate the spectral response of substrate noise generated from the digital section of SoC which is integrated on the high resistive substrate. In this context two contacts are integrated over the top of the substrate, out of which one is considered as source contact (digital section) while the other as sensor contact (analog/RF section). The system is simulated and it is observed that the transmission coefficient S (2, 1) is varying from -40 dB to -80 dB over the entire frequency range, the substrate noise potential is varying from -1.5 mV to +1.5 mV and power spectral density of substrate noise is also estimated. The design and analysis of the inductively source degenerated low noise amplifier (LNA) is also presented in this research work. The

minimum noise figure is obtained using the simulation which is observed to be 1.5dB at the resonance frequency of 1GHz.

To demonstrate the substrate coupling phenomenon in a complex VLSI system, two different inverter circuits are considered. Out of these two inverter circuits, one is a saturated load NMOS inverter and is assumed as analog part of the SoC, while the other is CMOS inverter and is considered as digital part of SoC. Both are integrated over a common multi-layered substrate. The substrate network is assumed to be pure resistive network and both the inverter circuits are operating on two different frequencies of 10 MHz (analog) and 25 MHz (digital). The substrate noise coupling between these circuits is analyzed through simulation and it is observed that the noise coupling between the circuits exists only when the distance between circuits is of the order of 10 µm to 15 µm. It is further observed that when the input is applied only at analog inverter then no noise coupling between two types of circuits is present and a peak is observed at 10 MHz. But when the inputs at both the inverter circuits are applied, the noise coupling between the circuits exists and two peaks are observed at 10 MHz and 25 MHz.

The statistical behavior of the substrate noise is also studied in this research work. The non-Gaussian cyclostationary substrate noise is modeled using a non-Gaussian mixture density and the probability density function (PDF) of non-Gaussian cyclostationary noise (substrate noise) is estimated by maximizing the log likelihood function and using the priori and post-priori updates. To validate this PDF estimation method, the PDF of substrate noise is again obtained by modeling of non-Gaussian noise using the Gaussian mixture density and a comparison between probability density functions (PDF) is also presented in this study.

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LIST OF ACRONYMS

ADC	:	Analog to Digital Converter
BiCMOS	:	Bipolar Complementary Metal Oxide Semiconductor
BEM	:	Boundary Element Method
CMOS	:	Complementary Metal Oxide Semiconductor
CAD	:	Computer Aided Design
f_c	:	Cut-Off Frequency
ξ	:	Constant
DAC	:	Digital to Analog Converter
V_{ds}	:	Drain to Source Voltage
EDA	:	Electronic Design and Automation
R_{sn}	:	Equivalent Substrate Resistance
FEM	:	Finite Element Mesh
FDM	:	Finite Difference Method
ggs	:	Gate to Source Admittance
V_{gs}	:	Gate to Source Voltage
L_g	:	Gate Inductance
$\overline{E^2{}_{n1}}$	:	Intrinsic Thermal Noise

I_{impact} : Impact Ionization Current

LNA : Low Noise Amplifier

γ : Lagrange Multiplier

F_m : Minimum Noise Figure

PLL : Phase Locked Loop

$Sv\Delta f$: Power Spectral Density of Thermal Noise

PDF : Probability Density Function

$P_{sn}(f)$: PSD of Substrate Noise

RF : Radio Frequency

SOI : Silicon on Insulator

Σ-Δ Modulator : Sigma Delta Modulator

L_s : Source Inductance

R_{Su} : Substrate Resistance

$\overline{E^2{}_{n2}}$: Substrate Noise

L_{sub} : Substrate Inductance

SoC : System-On-Chip

V_T : Threshold Voltage

TSV : Through Silicon Via

I_S : Total Swathing Current

VCO	:	Voltage Controlled Oscillator
C_{wel}	:	Well Capacitance
WLAN	:	Wireless Local Area Network

CHAPTER 1

INTRODUCTION

1.1 INTRODUCTION AND MOTIVATION

In 1958, Kilby and Noyce invented the integrated circuit and since then, technology is striving to integrate smaller devices. The evolution of down-scaling technology created a possibility to integrate digital and analog/RF circuits on a single substrate. This concept is termed as system-on-chip (SoC) or microchips that are capable to operate in the radio frequency range. Along with a number of advantages of integrating complex systems on a single substrate, it also faces the number of challenges. These challenges are raised because of the interaction amongst the blocks and interconnects. This interaction in the functional parts of SoC is due to the substrate noise coupling. A typical mixed signal system is shown in figure. 1.1, where the substrate noise coupling through common substrate has been represented.

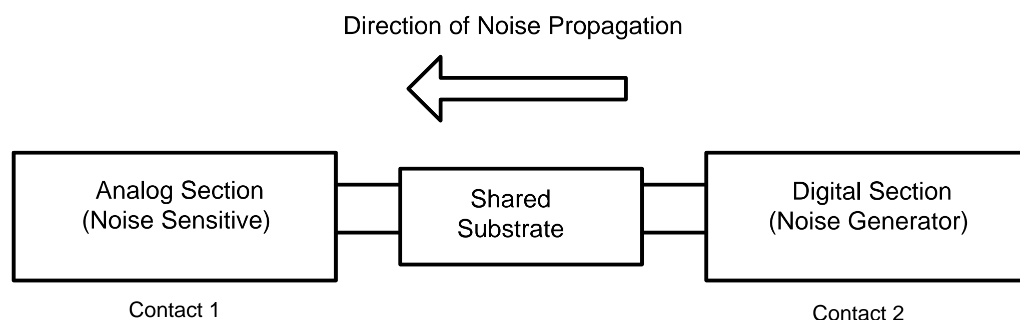


Figure. 1.1: Propagation of substrate noise from digital section to analog section in System-on-Chip (SoC)

Since, the high-speed digital circuits integrate with sensitive analog /RF blocks, the noise produced by the switching activities in digital block and by impact ionization transmits

through the common substrate and power distribution network to sensitive analog/RF blocks. The noise generated by the digital section ultimately degrades the performance of analog/RF blocks. Since the down-scaling technology provides the opportunity to integrate a large number of components and more functions of digital part. Therefore, the digital part has become more complex and hence more noise injection occurs in substrate and power distribution network.

A closer look of device scaling reflects that in order to reduce the transistor threshold voltage, the doping concentration increases and leading to the rise of conductivity in the substrate. This high conductive substrate allows noise coupling through a low resistive path. Since, the transistor dimensions are reduced, therefore the challenges of substrate noise coupling phenomenon are predicted to be aggravated in high performance SoC implementation. It is to be verified that whether a design which encapsulates some functional blocks and are integrated on a single substrate behaves within the performance specifications? In SoC implementation, the dominating noise source is digital block and hence the noise injected into the substrate by the digital block is an important factor to be considered. In the initial stage of SoC designs the noise injected by the digital part must be predicted precisely. The development of truthful substrate coupling minimization technique and circuits, which are less sensitive to noise are essentials for the progress of SoC implementation. The design is to be passed through a noise verification test along with the performance check in order to confirm whether, it meets the design specification.

In the last decades the semiconductor industry has enriched through down scaling technology. The down scaling technology is used to reduce device size and to attain the goal of low cost production and good performance of the devices. The International Technology Roadmap for Semiconductors (ITRS, 2003) [1] presented that the gate length

of logic device will be reduced up to 18 nm by the year 2012. It will enable the integration of more and more transistor in digital block and a single chip with multiple functionality. The down-scaling technology also allows integration of multiple functions on a single chip, i.e. analog, digital and RF parts. The researches in the last few years have mainly focused to reduce the length of connection paths in the different parts of the SoC to improve the performance and to reduce the production cost [2]. Scaling technology offers the implementation of a large number of functions and subsystems on a single substrate, higher transistor packaging density, lesser supply voltage requirement and higher frequency of operation. The innovations in technology have reduced the cost of production, but it creates a trade-off between the benefits of SoC and the resources used in design. SoC integrated circuit itself inherits these types of issues.

The integration of analog/RF circuits with high performance digital circuits as the parts of SoC has been reported in the International Solid-State Circuit Conference (ISSCC) [2-5]. Alcatel has provided the Bluetooth solution which encapsulates many analog/RF parts with memory and signal processing core [2]. Power amplifier performance is not specifically limited to the all other applications within Bluetooth specifications; while the implementation of digital parts and RF parts are made separately in the case of GSM application. The implementation of the above said functional blocks persist in the same manner for the IEEE 802.11 as it was in the case of Bluetooth application. The signal integrity issue, arisen due to putting the analog/RF parts with noisy digital part on a single substrate is demanding more attention to limit it [3], [4]. In this way it is confirmed that, the interaction among the analog/RF and digital parts through the common substrate and the signal integrity issues are the fundamental limitations in the SoC implementation. The International Solid State Circuit Conference [2-8] reported that some integrated circuit manufacturing industries put analog/RF parts and high performance digital parts together

to produce their high end system-on-chip. The different functional parts of SoCs are provided in table 1.1.

Table 1.1: System-on-Chip (SoC) application announced at ISSCC

Company	Year	Application	LNA	VCO	ADC DAC	PA	μP DSP	Memory
Alcatel	2001	Bluetooth	X	X	X	X	X	X
Conexant	2002	GSM/GPRS	X	X	X		X	
Toshiba	2003	IEEE802.11 a		X	X		X	X
AMD	2003	IEEE802.11 b	X	X	X	X		
TI	2004	Bluetooth	X	X	X			
Broadcom	2005	IEEE802.11 b	X	X	X	X		
Atheros	2005	IEEE802.11 g		X	X			X
TI	2005	GPS	X	X	X		X	
Atheros	2008	Transceiver	X	X	X	X		
Media Tek	2011	GPS		X	X		X	
Atheros	2013	IEEE802.11 ad		X	X			X

1.2 NOISE IN MOS DEVICES

Initially, when the MOS devices are come in picture for applications in digital circuits, there was no clear understanding about noise in MOS devices. Moreover, the MOS devices are found suitable for the single chip high performance application. However, when the

performance of the MOS devices was measured, it was noticed that the clear noise behavior of MOS devices is needed for its high performance applications. This issue exposed a new research trend in the field of noise associated with MOS devices. Each of the noise sources in MOS devices become a subject of research across the globe. In this section, there is brief information about the noise sources in MOS devices and their causes are represented and provided in table 1.2.

Table 1.2: Different noise phenomenon in semiconductor devices

S.No.	Noise in semiconductor devices	Cause	Representation
1.	Thermal Noise in Electron Devices [26, 28, 29]	Particle moving in resistive medium as Brownian motion, first reported by the Nyquist	$\overline{v_n^2} = S_v \Delta f = 4kT\Delta f R$ $\overline{i_n^2} = S_i \Delta f = 4kT\Delta f / R$
2.	Thermal Noise in MOSFET [32, 33, 34]	MOSFET thermal noise is developed by Van der Ziel	$\overline{i_d^2} \triangleq 4kT\Delta f \gamma g_{d0}$ $\overline{i_g^2} \triangleq 4kT\Delta f \delta g_{gs}$
3.	Induced gate current noise [26]	Due to the instabilities in the channel	Phenomenon is represented in figure. 1.1
4.	Shot Noise [26]	When the quantize carriers cross the barriers of random	$\overline{i_n^2} = 2qI_{dc}\Delta f$

		spacing, investigated by Schottky in 1918	Where; $I_{dc}$is the amount of current flowing through the device
5.	**I**nduced Gate Noise [36, 37, 38]	Channel thermal noise in MOSFET is obtained by solving the foremost factors of the Bessel's function	$S_{I_g}(f) = \frac{64}{135}\omega^2 kT\frac{C^2}{g_{d0}}$ Where; *T* is temperature, *C* is the gate capacitance, k is Boltzmann's constant and *ω* is the frequency of operation.
6.	Gate Resistance Noise [26, 41, 42]	Any fluctuation in parameters which are used to control the channel resistance	$R_n = \frac{1}{g_{mT}^2}\left[\sum_{j=1}^{p}\left(\sum_{i=1}^{p} g_{mi}A_{vij}\right)^2 R_j \sum_{i=1}^{p}\frac{g_{mi}^2}{12}R_i\right]$ Phenomenon is represented in figure. 1.2
7.	Substrate Resistance Noise [26, 29]	The resistance developed between the substrate and channel is responsible for the voltage fluctuation across it and generates a thermal noise	$S(f) = 4k_B T R_{sub} g_{mb}^2$ Where; R_{sub} is the resistance between the substrate and channel andg_{mb} be the transconductance of substrate.
8.	Substrate Current Supershot Noise	The impact ionization raptures the bonds and initiates the	$I_{eq} = I_{sub}\left(\frac{I_{sub}}{I_{sub0}}\right)^{1/2}$

	[26, 44, 45]	generation of extra electron-hole pair. The generated electron-hole pairs are generated the current in substrate as a noise and collected by the terminal of MOSFET	$S\ (f) = 2qI_{eq}R_{sub}^2 g_{mb}^2$ Where; Substrate current I_{sub} is I_{sub0}(maximum values)and qis the charge of electron.

Here, the induced gate current noise, is due to the instabilities in the channel. This fluctuation further capacitively coupled to gate through the gate oxide. The phenomenon of the generation of induced gate current noise is depicted in figure. 1.2.

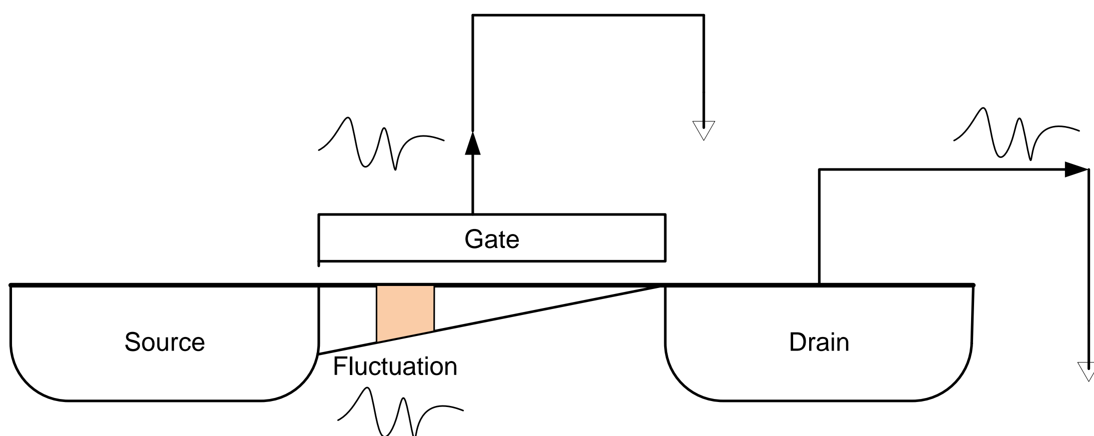


Figure. 1.2: Generation of Induced gate noise in MOS device

Any fluctuation in parameters which is used to control the channel resistance will definitely appear at the device output. The gate terminal of MOS device has the major responsibility for this kind of behavior. The typical layout of resistive gate matrix is shown figure. 1.3. There are two types of resistances, the first one is gate resistance and the second is contact resistance. The effects of all these resistances are taken into account and noise is formulated

[42].

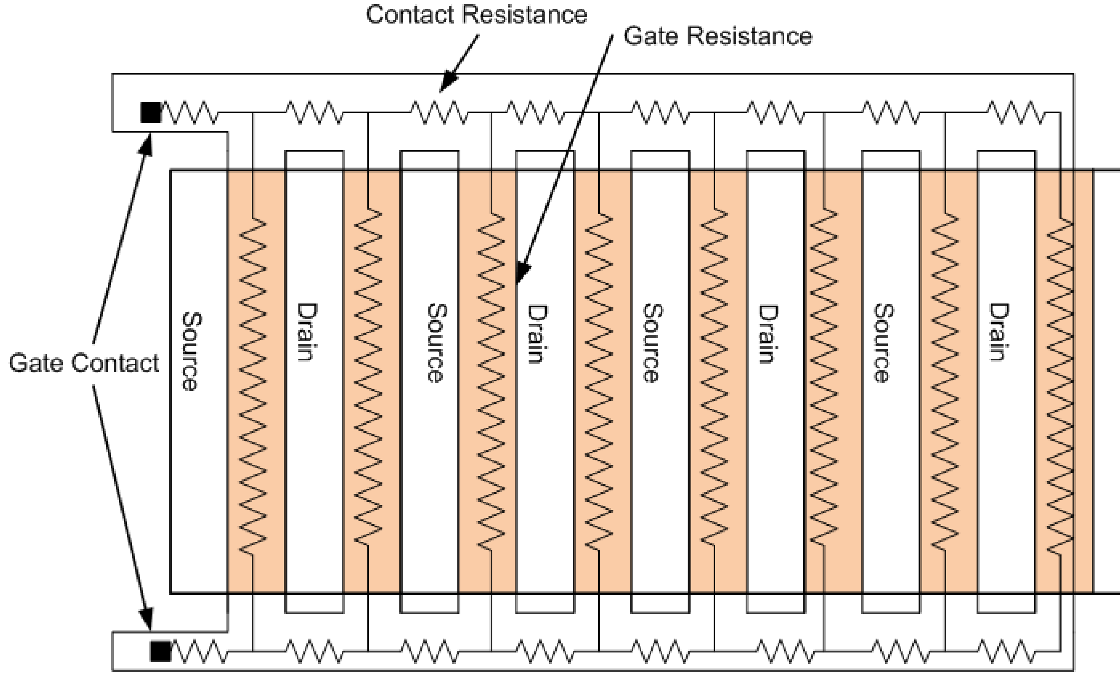


Figure. 1.3: Typical resistive gate matrix layout

1.3 DIGITAL SWITCHING NOISE

The system-on-chip encapsulates the multiple digital blocks of different spectral noise signatures [54]. Digital switching noise $Sw(t)$ is the group effect of stochastic $S(t)$and deterministic $D(t)$ component. This noise can be propagated through the substrate or power supply lines and given as in eq. (1.1),

$$Sw(t) = S(t) + D(t)$$

$$= \sum_{i=1}^{N} A_i \cos(2\pi.\omega_i.t + \theta_i) + S(t) \quad (1.1)$$

Where A is amplitude, ω is frequency and θ is the phase of the deterministic signal using the cosine transform. The values of amplitude, frequency, phase and $S(t)$ are affected by

the frequency, timing, digital switching activity and transistor count of the digital block. Ultimately, the switching noise affects the performance of the analog/RF system.

1.4 SUBSTRATE NOISE

Improvement in down scaling technology provided the feasibility to implement the digital, analog and RF block on a common substrate. The dark side of integration of the mixed signal blocks on the single substrate is the interaction amongst the different functional blocks through the parasitics of common substrate. Even a large physical separation amongst the blocks is provided, but still all the blocks are connected through the common substrate on which the system is implemented. A prototype of mixed signal system is shown in the figure. 1.4. Since the substrate is considered as a multilayered conductive medium, the noise generated from the switching activities in digital circuits is injected in substrate and conductive substrate plays a vital role to propagate this noise to the sensitive analog section [55].

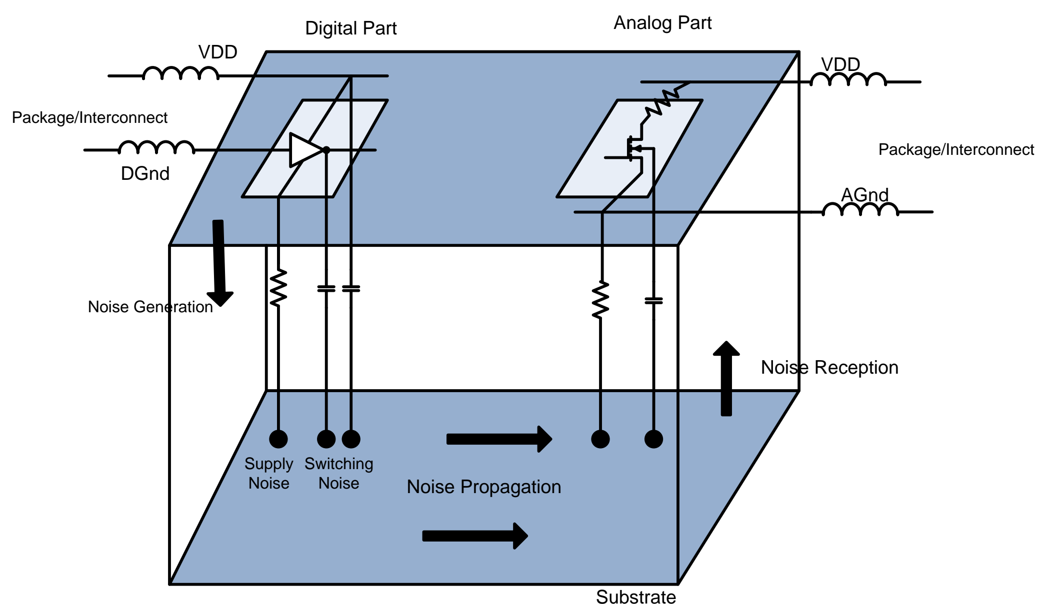


Figure. 1.4: Illustration of substrate noise mechanism in SoC

Since, the noise immunity of the analog section is lesser in comparison to digital, part therefor, this noise is severely affecting the performance of the analog section. The overall substrate noise mechanism comprises three basic mechanisms, generation of noise, its propagation and its reception in analog circuits. All these mechanisms are thoroughly discussed in sections 1.5, 1.6 and 1.7. The substrate parasitics are the major cause of the substrate noise coupling in SoC implementation. The parasitics in the supply lines provides a medium to couple the switching noise into the substrate. There are some other causes of noise injection into the substrate such as; the contact which connects the power supply lines to substrate, fluctuations in supply lines and ground lines current which are injected in substrate through the supply line inductances. As noise injects into the substrate, it travels to the noise sensitive analog circuits through the common substrate and thus degrades the performance of the sensitive analog/RF parts.

1.4.1 Sources of Substrate Noise

There are several relevant noise sources in the design of the digital CMOS system. The first important and relevant source is noise coupling or cross talk noise, which occurs due to the coupling between the power supply and substrate through parasitic capacitances, the second is the supply line noise which occurs due to the fluctuation in the supply lines and is injected into the substrate, and the third is charge sharing noise and is the most important substrate noise [54, 55, 57]. The various sources of noise in digital CMOS are shown in the figure. 1.5.

Digital part of the SoC is the noisy part and is responsible for the production of noise. There are three basic reasons for the generation of noise in the digital section. Firstly, supply line coupling with substrate through the parasitic inductance and resistance, secondly, coupling from the switching nodes and thirdly, the impact ionization in the substrate. The dI/dt

noise and drop in on-chip inductance and resistance of supply lines are the components of noise in digital power supply lines. The inductance and parasitic capacitance of supply and ground lines are responsible for the generation of simultaneous switching noise. The coupling of supply line noise is shown in figure. 1.6.

In the digital circuit design, typically the ground is connected to the substrate, which provides a very low resistive path between the substrate and the ground. The capacitive coupling between the source and the drain node of the MOSFET is yet again a cause of the substrate noise. In this case, the switching signal on the drain and source node have the same characteristic as the substrate voltage waveform [54, 68].

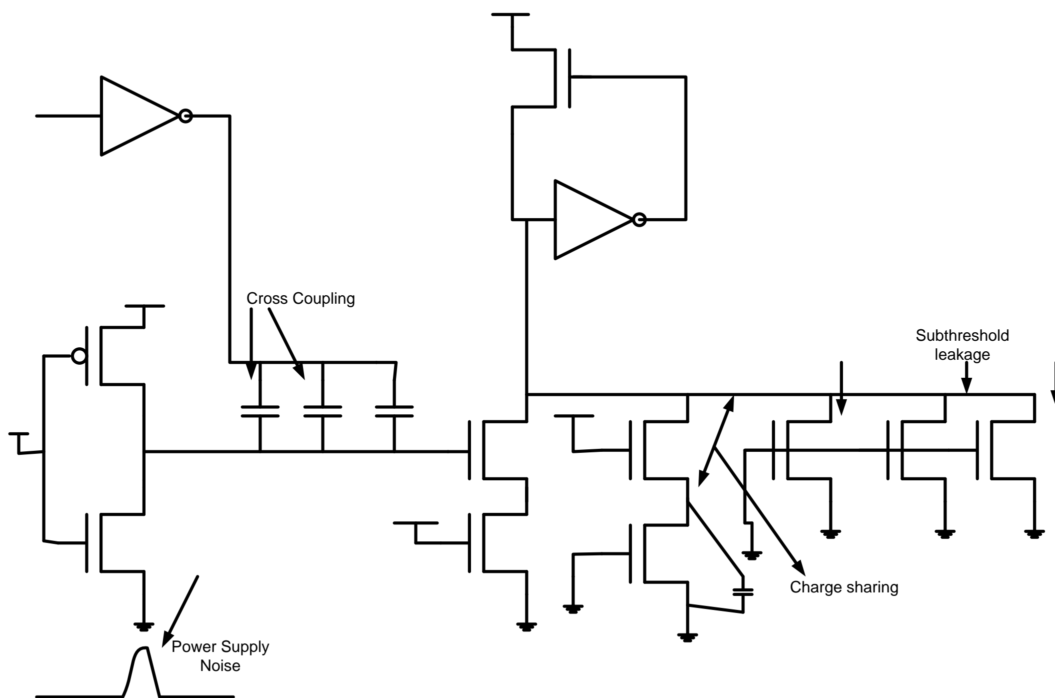


Figure. 1.5: Illustration of different sources of noise in digital CMOS system

As the switching activity increases, the substrate potential peak also increases. A current is injected into the substrate through the capacitance of source/drain junction, when there is switching in the digital circuit, as shown in figure. 1.7. This current is directly proportional

to switching or the Slew rate of switching voltage i.e. dV_{sw}/dt. With a rise in the frequency of switching in the digital circuit the coupling also increases

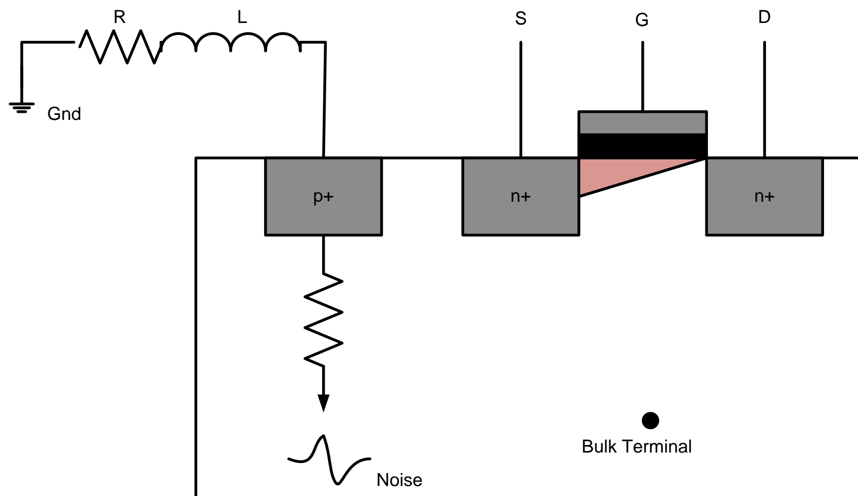


Figure. 1.6: Illustration of coupling of supply noise (inductive $L * di/dt$ noise) into substrate of NMOSFET

This is also dependent on the number of on-chip transistors and junction capacitance and is given by eq. (1.2);

$$i = C. dV_{sw}/dt \tag{1.2}$$

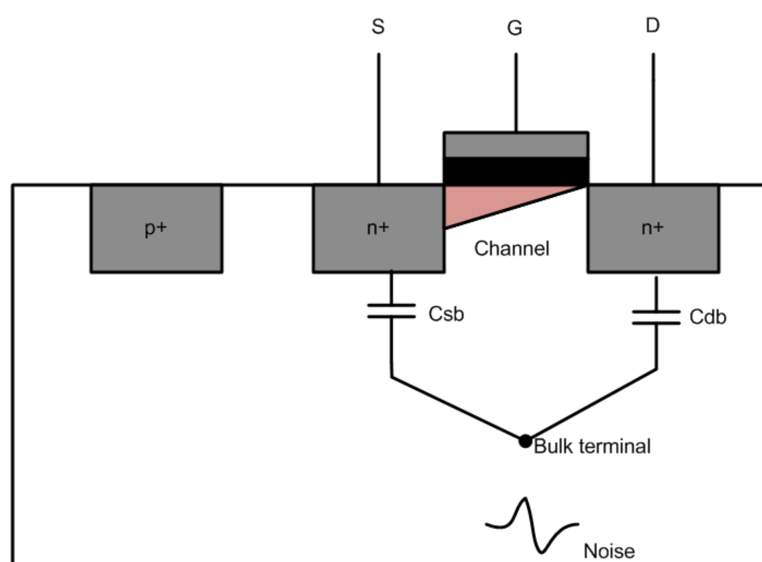


Figure. 1.7: Substrate noise coupling through the junction capacitances

The Impact ionization is another source of substrate noise and is dependent on the design technology. When high velocity electrons due to the high electric field at channel and substrate collide with carriers of substrate, an electron-hole pair generates and hence current in the substrate generates.

1.4.2 Substrate Noise Coupling Mechanism

The digital circuits, which share the substrate with analog circuits of the SoC severely degrade the performance of analog circuits in many ways. But, the analog circuits are mainly interfered by the switching activities in digital circuits (called as simultaneous switching noise, SSN). The substrate noise coupling mechanism in SoC is depicted in figure. 1.8.

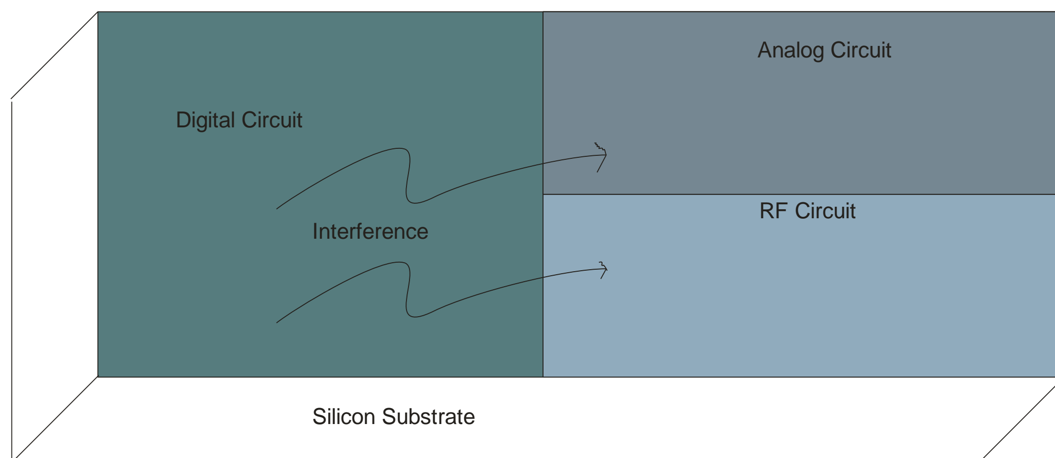


Figure. 1.8: Illustration of Substrate noise coupling in analog/ RF circuits

The noise coupling in the circuits through the parasitics is basically of two types i.e. thermal and electrical. When the excessive heat which is generated in substrate due to operation and this temperature deviates the performance of the other on-chip parts. The electrical coupling can be resistive, capacitive, or inductive in nature. The common substrate is responsible for another electrical coupling which is known as the substrate noise coupling. The noise generated in the substrate (substrate noise) is entirely different from the intrinsic

device noise (thermal noise) and has a random nature. Any undesirable potential variation of substrate over time, falls under the substrate noise which has a magnitude larger than the intrinsic device noise and this is the major concern of SoC design.

1.5 SUBSTRATE NOISE GENERATION MECHANISMS

The substrate noise generated by the digital part is injected into the other on-chip devices through common substrate in many ways which are symbolically represented and shown in figure. 1.8.

(1) Power grid fluctuation

(2) Capacitive coupling through the source (drain) to substrate junction and the gate substrate junction

(3) Resistive coupling (IR drop) through impact ionization.

There are three basic mechanisms for the generation of substrate noise; impact ionization [57], capacitive coupling and supply line bounce [58, 59]. Under the high electric field when the freely moving carriers get energized, then the phenomenon of impact ionization occurs, which generates a heavy number of electron-hole pair and due to impact ionization it generates current. The current generated by the impact ionization gets accumulated by the substrate contacts and produces a substrate current (I_{sub}) [57]. The IR drop produced by the substrate current is seen as the fluctuating current at supply rail and a dynamic voltage change is noticed at substrate contact. In a CMOS system the generation of substrate noise due to impact ionization is labeled as 3 and shown in the figure. 1.9. Due to switching signals a displacement current is produced, which, coupled through the parasitic capacitances (which encapsulates source/drain to substrate, gate capacitance and well to substrate capacitance). The capacitive coupling is labeled as 2 and shown in figure. 1.9.

When the supply line bounce concerns the coupling, it is dominated by the inductive effect followed by the capacitive and resistive effects. Therefore, supply bounce noise $(L\ {di}/{dt})$ is due to the interaction between parasitic inductance and the switching current at the supply lines [60, 62, 63, 64], this is labeled as 1 and shown in figure. 1.9.

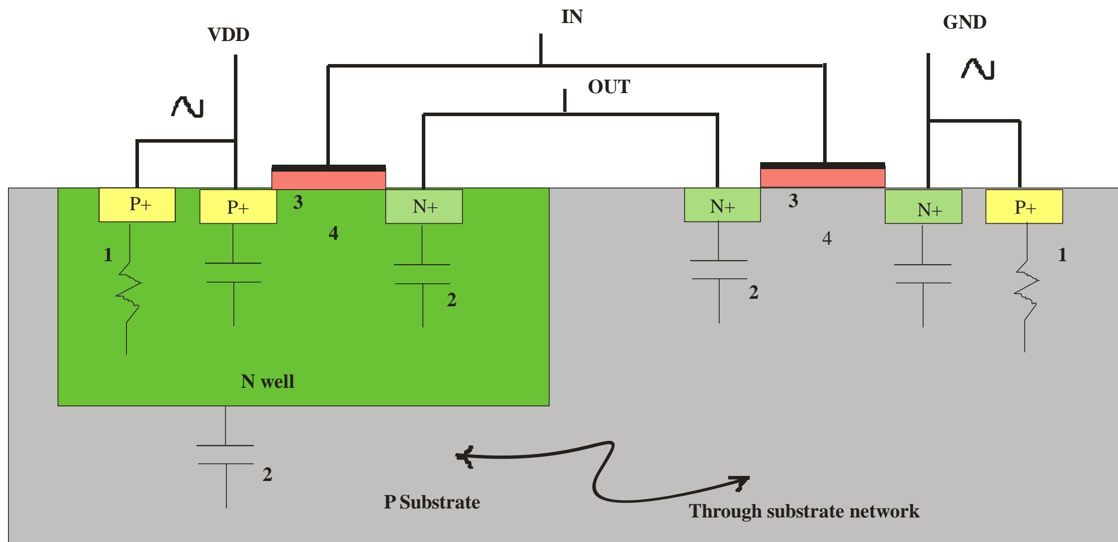


Figure. 1.9: Coupling in CMOS cell (1) Power grid fluctuation (2) Junction capacitance and Gate capacitance (3) Impact ionization

1.5.1 Power Supply Fluctuations

Since the current is drawn by the switching in digital circuits from the power supply line, the parasitic effect associated with this line become noisy. When current is induced due to large voltage fluctuation on switching of digital circuits, a$(L.dI/dt)$ noise is produced at the substrate and well contacts [65]. This noise is dependent on the switching speed and is capacitively coupled through the substrate parasitic capacitance.

1.5.2 Capacitive Coupling

Since the substrate and diffusion region are capacitively coupled the junction capacitance $C_{js}$of p-n junction plays the role of medium for noise injection into the substrate. The junction capacitance/unit area [57] is given by eq. (1.3);

$$C_{js} = \sqrt{\frac{q\varepsilon}{2(\psi+V_b)}}\left(\sqrt{\frac{N1N2}{N1+N2}}\right) \tag{1.3}$$

Where; p-n junction capacitance/unit area is represented as C_{js}, electronic charge as q, dielectric constant of Silicon material as ε, p and n material doping concentration as $N1$ and $N2$, applied reverse bias as V_b and barrier potential of junction is represented as ψ. As the device size reduces, the doping concentration increases and the higher doping concentration leads towards more coupling effects.

1.5.3 Impact Ionization

When the electric field in the substrate increases up to a certain level (critical field $\simeq 10^6\ V/m$ for normally doped semiconductor) due to the applied voltage [57], the excess electron-hole pairs are generated in the substrate region and are known as the impact ionization. Impact ionization current is given by eq. (1.4),

$$I_{impact} = \int_{E_s}^{E_m} I_d A e^{-B/E(x)} dx \tag{1.4}$$

Where, E_m is maximum electric field, E_s is source electric field and Id is drain current. A and B are material related Constants. Since $E_m \gg E_s$ eq. (1.4) will take a form as in eq. (1.5)

$$I_{impact} \simeq \frac{A}{B} l E_m I_d e^{-B/E_m} = C_1(V_{ds} + V_{dsat}) I_d e^{-\frac{C_2}{(V_{ds}+V_{dsat})}} \tag{1.5}$$

Where l is channel length, Vds is drain source voltage and Vd_{sat} is saturation voltage. C_1 and C_2 are material constant. Since holes have lower ionization coefficient Impact ionization currents in p-type substrate is lower than in n-type substrate.

Since the substrate behavior is as a dielectric medium, it can be described by a derivative of Maxwell's equation as in eq. (1.6),

$$J = (\sigma + j\omega\varepsilon_{si})E \quad (1.6)$$

Where; the substrate current density is J, Electric field is E, conductivity is σ, frequency is ω and the dielectric permittivity of silicon is ε_{si} (ε_o 8.854e-14 $*\varepsilon_r$11.7F/cm). Substrate will act as a medium of coupling between the devices fabricated over the common substrate and frequency of the operation has a significant impact on it as the transmission media. As long as $\sigma \gg \omega.\varepsilon_{si}$ the capacitive behavior of substrate is insignificant and assumed as resistive medium.

1.6 NOISE INJECTION IN SUBSTRATE

A typical view of the SoC is depicted in figure. 1.4, in addition to it, the noise generation, injection and propagation are also represented. The digital and the analog sections are shown separately in the figure. The digital part is represented by the inverter and the analog part is represented by the NMOS transistor. The generated noise is injected into the substrate by the three basic means; the first injection mechanism is through substrate contacts. The NMOS consists the p+ contact and PMOS consists the n+ contact are connected to either VDD or GND depending on the device type. The substrate and source terminal are connected together to prevent the threshold voltage variation [58]. The parasitic inductance and capacitance associated with the connection lines picks the spikes in supply and charge the load. Since, the substrate is connected to the ground the major portion of this voltage is discharged to ground through the substrate. This is a cyclic process and causes a ringing in the supply lines and the order of this is tens of millivolts. The second injection mechanism is through coupling capacitances. In the MOS transistor the source and drain of the transistor forms p-n junction and hence the existence of the parasitic capacitances has come into the picture. These parasitic capacitances are the mean of coupling between the source/drain and substrate. When any switching appears at these

nodes the noise gets capacitively coupled into the substrate. As the capacitance increases the noise coupled becomes significant and it is also dependent on the length of routing lines. The third and last noise injection mechanism is the impact ionization current. The carrier, which moves under the high electric field obtains sufficient energy and collision starts with the carriers of substrate. Therefore, excessive electron-hole pair generation is there in substrate [58, 64, 66]. Thus, there is current due to impact ionization which flows in the resistive network of the substrate and fluctuates the substrate potential. The noise injection through impact ionization and the capacitive coupling are very much expected because the diffusion area will surely be there in physical design and cannot be eliminated. However the injection from the supply can be reduced by using the better packaging technique.

1.7 NOISE PROPAGATION THROUGH SUBSTRATE

The Silicon substrate behaves like conducting as well as dielectric medium. The noise generated from the digital part of the SoC is propagated to the entire system through the substrate over which the system is integrated. The nature of the substrate is frequency dependent and its behavior changes at different frequency range. Up to 12 to 15 GHz frequency, substrate behaves as a resistive medium and if any node gets perturbed there, it will cause the fluctuation at other associated nodes. The impedance of substrate path plays a major role in the propagation of the noise into the substrate. The behavior of noise propagation in lightly doped as well as heavily doped substrate and effects of these substrates are different [56, 66, 68, 69, 70].

Typically, the lightly doped substrate provides a better and heavily doped substrate provides the poor noise propagation medium. A better noise rejection quality is expected from the advance systems, such as SoC and SOI. In the propagation of noise, it is distinctly noted that the low operating frequency is not suitable for the noise propagation in the

substrate. Once the higher operating frequency requirement is fulfilled, this advantage is neglected in the design of SoC because due to its nature substrate become capacitive at higher frequency [97]. There are basically two governing parts in the noise propagation, first the Maxwell's equations, in which the substrate effect is characterized by the full wave Maxwell equation. A substrate may behave like pure resistive medium and it can be modeled by R or substrate under quasi-static condition that can be modeled by R and C or substrate under non quasi-static condition which can be modeled by the R, C and L. The all above are dependent on the frequency of operation and material property. As it has been discussed that the substrate has dual nature, conductive and dielectric which is dependent on the frequency of operation. When the operating frequency increases the conductive nature of the substrate become less prominent. A homogeneous substrate is shown in the figure. 1.10. A unit of this homogeneous substrate is taken into account and the cut-off frequency for the substrate is given by the eq. (1.7), (1.8) and (1.9).

$$j = \sigma E = q(n\mu_n + p\mu_p)E \tag{1.7}$$

$$Y = \frac{1 + R\,C}{R} = \frac{1 + j\omega T}{R}$$

$$T = R\,C = \frac{\rho\,dl}{dA}\frac{\epsilon\,dA}{dl} = \frac{\epsilon}{q(n\mu_n + p\mu_p)} \tag{1.8}$$

$$j = \sigma E = q(n\mu_n + p\mu_p)E \tag{1.7}$$

$$Y = \frac{1 + R\,C}{R} = \frac{1 + j\omega T}{R}$$

$$T = R\,C = \frac{\rho\,dl}{dA}\frac{\epsilon\,dA}{dl} = \frac{\epsilon}{q(n\mu_n + p\mu_p)} \tag{1.8}$$

$$f_{c=}\frac{1}{2\pi T} = \frac{q(n\mu_n + p\mu_p)}{2\pi\epsilon}$$

$$f_c = \frac{1}{2\pi\epsilon\rho} \tag{1.9}$$

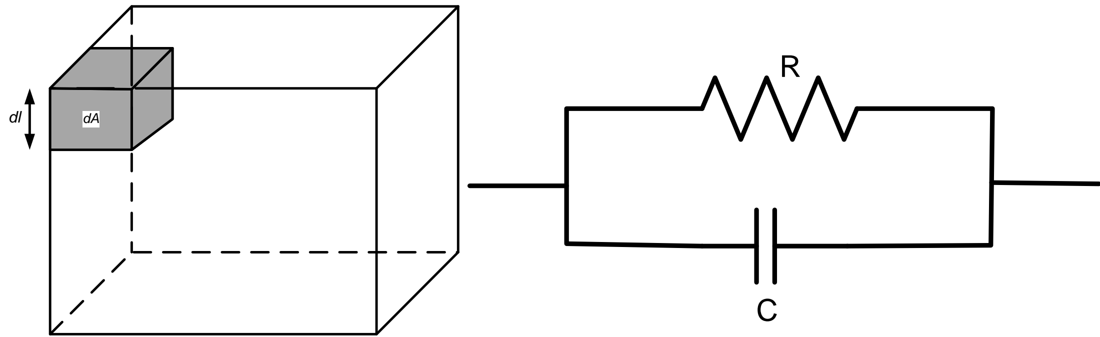


Figure. 1.10: RC model of a homogeneous substrate

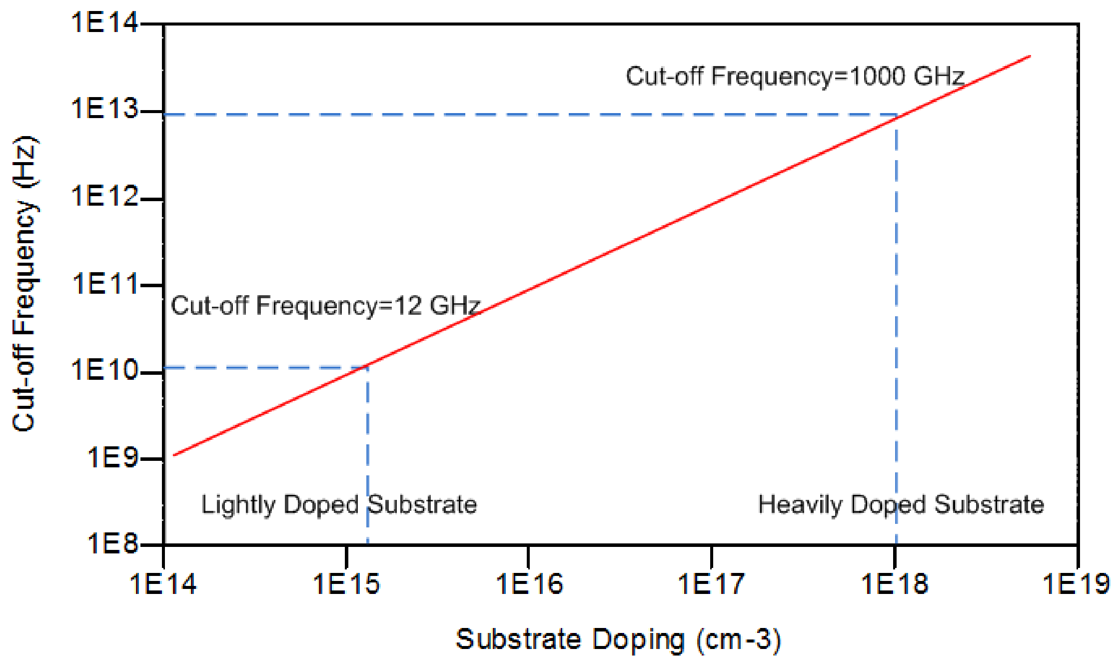


Figure. 1.11: Analytical plot of substrate doping v/s cut-off frequency for silicon substrate

The cut-off frequency given in eq. (1.9) depends on the doping of the substrate. In heavily doped substrate the cut-off frequency is more than the lightly doped substrate. Up to the cut-off frequency the substrate can be modeled as a pure resistive network and for the frequency above the cut-off frequency the dielectric behavior cannot be neglected anymore. Hence, the substrate will behave as the mesh of resistive and capacitive components at high

frequency [102]. The analytical plot of substrate doping v/s cut-off frequency for silicon substrate is shown in figure. 1.11.

1.8 NOISE RECEPTION AT SUBSTRATE

The noise reception mechanism has the same analogy as that of noise injection mechanism, i.e. both the phenomenon are due to the parasitics of the substrate as well as the device integrated. Signal fluctuation at the contact terminal will directly couples trough parasitic capacitance of the drain and source terminals. Noise can couple by another means, through the channel which is basically due to the parasitics depletion capacitances and this noise will be injected again in the source/drain. The on-chip component can also work as the receptor of the substrate noise. The on-chip components may be passive resistor, capacitor and inductor or it may be the active device [117]. Since the substrate is connected to the supply or to the ground, any noise in the substrate will automatically appear at the supply rail. The performance of the analog circuit will be altered whenever there is change in small signal behavior of the MOSFET. The small signal behavior of the MOSFET will only be changed when there body effect exists, which is a kind of noise reception mechanism and it can be described by the well-known eq. (1.10);

$$V_T = V_{T0} + \frac{\sqrt{2q\epsilon_s N_A}}{C_{ox}}\left(\sqrt{|2\varphi| + V_{SB}} - \sqrt{|2\varphi|}\right) \tag{1.10}$$

Since the substrate behavior can be modeled as a pure resistive network below the cut-off frequency the noise due to capacitive coupling is there at higher frequency while the noise due to the body effect is there for the entire frequency range.

1.9 IMPACT OF SUBSTRATE NOISE ON SOC PERFORMANCE

In the design of SoC, the digital part is the noisy part and responsible for the generation of substrate noise which significantly affects the performance of the sensitive analog/RF

circuits. The analysis of the impact of the substrate noise on performance of analog/RF circuits is done at three different levels, i.e. device level, circuit level, and system level [59, 72, 86, 132].

1.9.1 Device Level

The substrate bias effect comes into picture during the study of the impact of the substrate noise on the performance of the sensitive analog/RF circuits of SoC. The MOSFET performance deviates due to the variation in the threshold voltage of the MOSFET. Here n-channel MOSFET is taken as an example and the drain current of the MOSFET is given by eq. (1.11);

$$I_D = \frac{\mu C_{ox\,W}}{2L} \cdot \left(V_{gs} - V_t\right)^2 \tag{1.11}$$

Where V_t is threshold voltage of the MOSFET and expressed by the eq. (1.10) and V_{SB} is source to body potential and is assumed to be constant. The substrate noise, as already been discussed affects the substrate contact voltage due to the resistive path between the substrate and substrate contact and causes supply rail bounce.

1.9.2 Circuit Level

When the effect of substrate noise is examined at the circuit level, the circuit topology, supply scheme, and the parasitics are the major factors on which performance of device degradation depends. In this work, the effect of substrate noise on RF MOSFET, Adder and LNA is analyzed. The performance degradation of analog circuits such as LNA (low noise amplifier), VCO [73] and operational amplifier were examined in the past research. In the communication system, the performance of the band limited LNA is only degraded by such noise component which appears in a specific frequency range.

1.9.3 System Level

The substrate noise is one of the major challenge in the integration of the analog circuits such as PLL, LNA, VCO and RF blocks with large digital blocks such as memory [132], DSP block etc. RF blocks which have the large dynamic range are more sensitive to the digital substrate noise. The researcher has proposed the substrate noise reduction techniques in the past, including the isolation between the noise generator and noise receptor, low parasitic packaging etc. [133]. Keeping substrate noise in mind and on the basis of the spacing between blocks, closely placed substrate contacts and decoupling capacitance, the designs were proposed in the past to reduce the substrate noise [13].

1.10 CHALLENGES IN SYSTEM-ON-CHIP DESIGN

Mounting of the different ICs over the single board cannot be said an analogy of integrating different functional blocks on the substrate. Researchers are facing many problems during SoC implementation like substrate noise coupling, poor signal integrity, power supply integrity issue and the support of EDA tool is not sufficient for high level synthesis and verification. Amongst the above discussed issues the substrate noise coupling through the common substrate is a major challenge in SoC design, which can significantly degrade the performance of SoC and may lead to the system failure because of a breakdown in analog/RF parts [141]. Researchers have even reported that the integration of communication system on a single chip in the presence of substrate noise coupling is impractical [141]. With an advancement in scaling technology, the SoCs has become more realizable and attractive for high volume products [8, 9]. Figure. 1.12 depicts the typical SoC architecture reported in [10]. This chip contains DAC and ADC as analog/RF parts, CPU and memory unit as digital parts, WLAN as communication unit and IEEE 802.11g as media access controller.

The Scaling technology has a great impact on substrate noise coupling phenomenon. As the scaling technology improves, the substrate coupling problem becomes more powerful due to the closer integration of digital parts and analog/RF parts at high packaging density. Therefore, the integration of system-on-chip needed more efforts of designers to remodel the SoC integration for the minimization of substrate coupling effects. Since more functions are implemented in the digital section of the SoC involves more number of transistors and hence the noise generated by this section become more intense. Moreover, the higher clock frequency leads to faster switching in digital circuit which generates more noise.

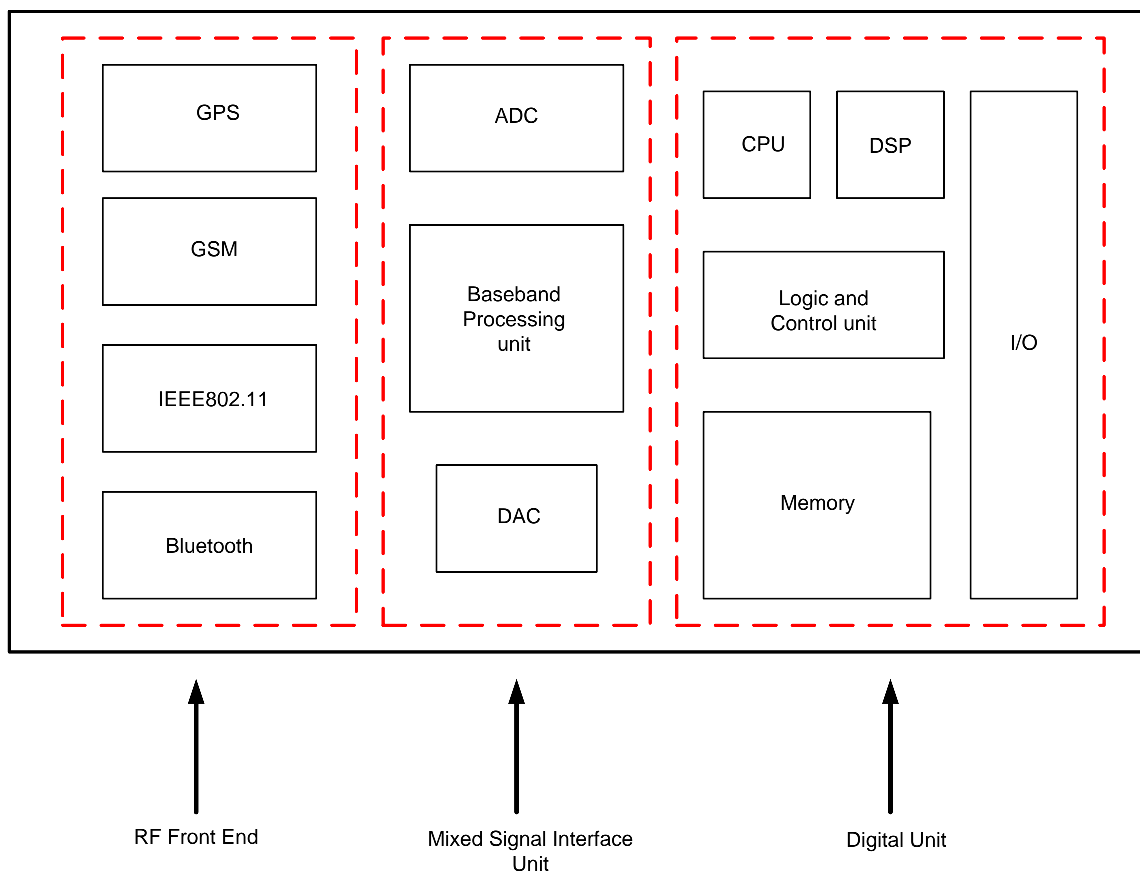


Figure. 1.12: Typical System-on-Chip (SoC) Architecture

The doping concentration of the substrate increases for a good command over the threshold voltage. The higher doping concentration offers more conductive/less resistive top surface region of the substrate. Hence, it becomes a favorable medium for noise to propagate

through the surface of substrate. Apart from this, beyond certain substrate potential, the substrate itself generates noise current due to the impact ionization and this is an addition to the noise generated by the digital section. Since, the analog/RF circuits are very less noise tolerant, it picks up the noise that propagates through the substrate. The performance of the analog/RF sections is now affected due to this picked noise. Thus, a number of challenges are imposed on the designers by the substrate noise coupling in the design of system-on-chip. In the future, with the advancement of technology the substrate noise coupling phenomenon will become more complicated and substrate noise will become tough to estimate and minimize.

1.11 PROBLEM FORMULATION

For the last three decades, the device performance has improved and the production cost has significantly reduced due to improvement in the scaling technology. The designers are looking forward towards the implementation of analog/RF blocks using the CMOS technology unlike the use of BiCMOS technology in previous years [14]. Since, the implementation of digital circuits as well as analog/RF circuits using the CMOS technology has been augmented, even though the CMOS technologies are not very much convenient for the implementation of the analog/RF circuits due to their limitations like lower drive capabilities of active devices and bad quality of on chip passive component. The implementation of analog/RF circuits using CMOS technology has enhanced possibilities for the designer to integrate digital, analog, and RF circuits on a single chip. As discussed in previous sections the SoC design will put more challenges for the designers, especially in wireless application where the clock speed and switching activity of digital section is very high. Immediate complication like substrate noise coupling effects and signal integrity [16, 18] which have aroused as a problem and is responsible for the dilapidation in the

performance of analog/RF block integrated neighboring to the digital block. The substrate noise coupling issue became more important when many of researchers focused on it and presented substrate noise coupling as their key challenge for single chip SoC integration. Many more contributions are there on the degradation of performances of individual analog blocks like Low-noise amplifiers (LNAs) [151,152] and Voltage controlled Oscillators (VCOs) [4, 131].This can be predicted that substrate noise issue will be aggravated in the design of SoC with a higher package density of digital circuit and with a higher switching speed. These issues and overall complications in analog CMOS design, necessitate an understanding of substrate noise coupling.

As discussed in the previous sections that, to understand the substrate noise coupling a suitable substrate model is a prime requirement. Without a clear picture of the substrate behavior, the substrate noise cannot be accurately estimated in high performance VLSI circuit design. The statistical characteristics of the substrate noise are essential, if the wireless communication is targeted for the SoC application. Therefore, a suitable substrate model, efficient substrate noise estimation technique and exact substrate noise characteristics are intensely required for high performance SoC design in future.

1.11.1 Thesis Objectives

1. To determine the relevant device parasitics that should be included in a circuit noise macro-model.

2. To propose and verify a circuit noise macro-model for standard cells and to implement a procedure to evaluate the substrate noise.

3. Estimation of statistical characteristics of the substrate noise in VLSI circuit.

1.12 THESIS OUTLINE

The thesis will be organized in six chapters. The details of the contents of each chapter of the thesis are as follows;

- Chapter one presents the introduction and motivation of the entire thesis, problem formulation, the objectives of the thesis and thesis organization.
- Chapter two gives a brief review of literatures regarding the substrate modeling techniques for the estimation of substrate noise, Substrate noise estimation methods, impact of substrate coupling on the analog/RF circuits and the technique for the estimation of probability density function (PDF) of noise is also presented.
- Chapter three mainly deals with the substrate modeling techniques and a comparison among the previous modeling techniques and proposed techniques is also presented in this chapter.
- Chapter four is oriented towards the substrate noise estimation and its analysis in VLSI circuits. In this context, the performance variation of MOSFET in the presence of digital substrate noise has been studied, substrate noise in CMOS inverter and in a chain of five CMOS inverters is estimated and substrate noise analysis is also presented for some other high performance VLSI circuits.
- Chapter five is related with the estimation of the probability density function of substrate noise. The PDF parameters are modeled and the PDF of the substrate noise is estimated in this chapter.
- Finally, the chapter six sums up the research work. Further, a brief description about the future work/scope has been presented as a motivational seed for the germination of research work.

CHAPTER 2

LITERATURE REVIEW

2.1 INTRODUCTION

The estimation and analysis of substrate noise have attracted the researcher for many years at different level of system of chip (SoC) design. With the increase in packaging density, the device size decreases, resulting in the integration of more transistors on a single chip. Thus, the substrate noise has become more intensive in the designing of SoC. Hence, the substrate noise coupling issue is a major concern in the design of high performance integrated circuits. The excessive heating of a chip is responsible for the thermal coupling, whereas the electrical coupling is due to the parasitic capacitances of the substrate and the inductances in supply lines.

The issue of substrate noise coupling at different level in design of mixed signal system is discussed and reported by many researchers in the last decades. Many research outputs in recent years are based on the substrate modeling techniques, substrate noise estimation methods, and reduction techniques. Apart from this, commercial as well as educational CAD tools have been developed which are based on substrate modeling, and are helpful in the analysis of the mixed signal circuits.

A significant focus on research has also been put forth by the industries, research groups and academia for the substrate noise analysis specifically for the RF integrated circuit design. A review of the literatures of previous researches on noise in semiconductor devices, substrate modeling, parameter extraction, substrate noise estimation methods and probability density function estimation of substrate noise is presented in this chapter.

2.2 LITERATURE REVIEW

2.2.1 Substrate noise Issue in System on Chip (SoC) Design

The MOS transistor possesses different noise sources as well as different types of noises. Intrinsic and extrinsic noise mechanism in MOSFET is to be studied well to understand noise in a MOSFET. A compact noise model of the MOSFET is developed and discussed by R. P. Jindal in [42, 44, 71]. The intrinsic and extrinsic noises are categorized as; the intrinsic noise is an encapsulated thermal noise, induced gate and induced substrate noise, while the extrinsic noise covers the noise because of scaling in device size, noise from substrate charge effects, noise due to substrate current and noise due to the distributed substrate resistance. The compact noise model for all the mentioned noises are discussed and the validation of model for different regions of operation of the MOSFET is explained.

A physics based simple noise model for MOSFET is explained by A Arnaud et al. [79] and the validity of the model for the usual operation as well as subthreshold operation is explained by K Fobelets et al. [109], it is discussed as an approach to analyze noise performance of MOSFET which uses the hydrodynamic model and an impedance field method. The impact of gate scaling and oxide layer scaling on minimum noise figure (NF_{min}) is separately discussed. The discussion is concluded as the gate scaling has negative impact on NF_{min} in subthreshold operation, while the NF_{min} is not been affected by the oxide thickness in subthreshold operation. The major concern of this work is substrate noise and above mentioned researches are not oriented towards the substrate noise. The substrate noise in the design of SoC includes the physical phenomenon responsible for the generation of substrate noise, the transmission of substrate noise through the common substrate, parasitics responsible for substrate coupling and the performance of the mixed signal system in the presence of substrate noise is explained by Ali Afzali-Kusha

et al. [96]. The direction to minimize the substrate coupling, modeling methods and simulation techniques are also discussed. Mustafa Badaroglu et al. [69, 84] discusses the impact of device size scaling on the coupling mechanism. The literature described that when the device is down-scaled and substrate is connected to ground, then the substrate coupling become more intensive in mixed signal integrated circuits. The source-drain capacitive coupling is the dominant coupling when the substrate is biased to ground. Further, the literature described the effect of down-scaling on the supply noise coupling and explains that it is more dependent on the ratio of switching and non-switching capacitance than the $L \, {di}/{dt}$ noise. The quantitative analysis has proven to be more useful in the design of low noise CMOS systems. The generation of substrate noise by digital circuits and spectral analysis of substrate noise is presented by Marc van Heijningen et al. [85]. The simulation of the generation of substrate noise by the digital circuits is done using a SPICE model and the correctness of this model is validated by measurement of substrate noise sensor. When switching noise is dominating source of substrate noise coupling, a new concept of virtual separation is proposed to analyze the substrate noise in SoC design by Shuching Hsu et al. [97]. The existing p-contact to p-contact model is used and the virtual separation concept is applied; the model is validated with 3D device simulator for 0.35 µm CMOS process. Brian E. Owens et al. [145, 156] have proposed a scalable macromodel for the analysis of substrate noise coupling. The analog and digital circuit are integrated with a scalable separation between them over a common substrate. The effect of the adding the grounded guard rings around noisy circuits on substrate coupling is also analyzed. The modeling of MOS transistor using the sub-circuits is presented by Christian C. Enz et al. [106], which encapsulates the substrate network responsible for the noise coupling between diffused regions at high frequency. This sub-circuits model is further lead towards the derivation of a scalable model. Again a physics based approach by Charif Mohamed et al.

[146] for the analysis of substrate noise due to movement of free carriers generated in the n-well and p-well region of digital circuits has been explained.

2.2.2 Substrate Modeling Techniques

To analyze the substrate coupling, it is important to have an accurate substrate model/macromodel. It is also required for analog circuit simulation. It has explained by Zhuoxiang Ren et al. [83] that, in the lightly doped substrate, the capacitive effect becomes prominent and the substrate impedance become frequency dependent at a higher frequency of operation. For both high resistive as well as low resistive substrate, the consideration of dynamic behavior of substrate is needed. The dynamic behavior of the substrate macromodel is studied on these two traditional substrates. A macromodel based simulation approach is presented by Luis Elvira et al. [74], where one macromodel for each standard cell is developed and the whole chip network is a combination of these macromodels and this approach can be used to construct the macromodel for both EPI type and bulk-type substrates, which has also discussed by Mustafa Badaroglu et al. [84]. This macromodel based approach can be adopted for both heavily doped as well as lightly doped type substrates. The digital injecting blocks and sensing analog blocks are assumed as two separate contact and substrate noise analysis is made. The spacing between the contacts are kept variable for further analysis. The comparison of obtained substrate noise using substrate waveform analysis with SPICE simulation clearly indicated 10% error in time domain and 2 dB relative error. A scalable macromodel for substrate noise coupling in low resistive substrates is discussed in Anil Samavedam et al. [20]. This model can be used for different spacing between the source-sensor contacts and for different contact geometries. The scalable separation and width of this model provided an insight into substrate coupling regarding the optimization issues prior to and during the physical design. Another scalable

macromodel by Brian E. Owens et al. [145] is presented, which demonstrates the noise coupling with the effectiveness of inclusion of grounded guard bands and separating bulk and supply pins to reduce the coupling effects. As the complexity of the digital core increases the propagation network also increases. An acceptable frequency range of the lumped element models is identified by Chenggang Xu et al. [106] for the frequency dependent substrate parasitic. Lossy substrate is modeled by the frequency dependent coupling parameter and extraction of substrate resistance using the direct boundary element method and revise resistance into parameter has been done by Xiren Wang et al. [112]. Since, the designs are extending into the multiple tens of Gigahertz, the Giorgos Manetas et al. [82] has suggested that, an Electro-quasi-static RC model analysis will be a better approach for analysis of substrate noise coupling. At higher frequency of operation is increased the capacitive effect has become prominent and the substrate impedance has become frequency dependent for the lightly doped substrate as discussed by Zhuoxiang Ren et al. [83]. The studies on substrate noise modeling in recent years have only considered the parasitic elements of substrate and the parasitics of the bonding wires. Olivier Valorge et al. [89] has considered all the sections which are responsible for substrate noise coupling to model the substrate for substrate coupling analysis. The considered sections are supply rail bounces, board and package parasitics, bonding wire parasitics, input/output rings, supply distribution and core digital section of SoC. The transient substrate potential by digital part of SoC is simulated with integrated power supply model. The high resistive as well as low resistive substrate are having the frequency dependent lumped components. A lumped element model of the substrate is analyzed by Chenggang Xu et al. [106] and the validity of lumped model at very high frequency has also been authenticated. Since, the dominant substrate coupling mechanism is needed to be identified at a very early stage of the SoC design process. A macromodel is proposed by Emre Salman

et al. [60] to find the dominant substrate noise coupling mechanism and a macromodel is discussed which purview the multiple parameters. The dependency of substrate noise in these considered parameters is also examined which depicts the non-monotonic dependency of substrate noise on the rise time of the signal. Since, performance improvement of the analog / RF system in terms of low power and high packaging density of passive with digital active devices is required. The device integrated on silicon substrate has a major challenge of coupling through capacitance to the resistive substrate. Power dissipation, cross talk and injection of thermal noise are the major problem raised due to this coupling mechanism. Ronald Dekker et al. [117] has developed a cost effective post processing technology to transfer the circuits for glass substrate. This technique meets the challenges of the Silicon substrate and effectively removed the cross talk between the different parts of SoC. The structural macromodel for the special analog circuits such as, two stage operational amplifier and operational transconductance amplifier is demonstrated by Ying Wei et al. [119]. In this method, the behavioral concept of building block is applied to two algorithms and the structural macromodel of analog circuits are generated.

2.2.3 Parasitic Extraction of Substrate

The prime techniques applied for the parameter extraction from the transient, static and dynamic behavior of MOSFET are reviewed by D Bauza et al. [141]. The method to extract the key parameters like series resistance of source and drain, channel resistance etc. from the transfer characteristics are discussed. A method to examine the trapped charge at the interface, substrate densities using the subthreshold slope and low frequency noise is also explained. Kow-Ming Chang et al. [121] has discussed a simple and precise small signal model for RF MOS transistor, which considers the parasitic elements of substrate, effect of gate distributed network and conservation of charge. The linear regression is used in

accurate extraction method for the parameter extraction of the MOSFET. The propose model and extraction method are validated using experiments and concluded that ignorance of important parameter like charge conservation will be headed towards erroneous transistor performance. The silicon substrate behaves as lossy dielectric and this kind of substrate is modeled using the frequency dependent circuit elements by Xiren Wang et al. [117]. Substrate parasitics at different frequencies are extracted in two steps. The first step is time taking process, which uses the direct Boundary Element Method to extract the coupling resistance. In the second step, the resistances are revised into parameter at different frequency in a rapid manner. This step is needed to be repeated at all frequencies of interest. The method can be applied to the substrate of any doping profile and is proven faster and more accurate than Green's function based techniques. An improved small signal equivalent circuit model of MOSFET which is equivalent to non-quasi small signal with direct extraction method is discussed by Yang Tang et al. [122]. A shunt gate drain branch is appended in traditional small signal equivalent circuit model to define the gate to drain at very high frequency where the effect of substrate loss, contact resistances and inductances are considered. The z-parameter at ground bias and y-parameter at supply bias is used for extraction of extrinsic parasitic elements and intrinsic component respectively. The proposed technique is further used in large signal application to develop a nonlinear model. Germán Álvarez-Botero et al. [160] has proposed a parameter extraction method in which the parameters, threshold voltage, gain factor and mobility degradation factor are determined from the s-parameter. The substrate effect is considered in the discussed technique and for the parameter extraction, data regression and DC measurement are not required in this method. Apart from the method proposed, the substrate impedance analysis suggested that the parasitics are not only altered the transistor performance also the parasitics are needed to be considered at high frequency. Jiong-Guang Su et al. [125] has

considered the substrate resistance in series and gate conductance in parallel in the proposed method for extraction of gate capacitance using s-parameter at high frequency

A noble method to extract the gate resistance from s-parameter in CMOS system is discussed by R. Torres-Torres et al. [161]. In the previous gate resistance extraction techniques the impact of intrinsic channel resistance was not considered. This method allows the extraction of the gate resistance when the impact of the intrinsic channel resistance is considered. This method is validated for the 0.18μm CMOS process. The combination of a noble method and the traditional method of threshold voltage determination used for the extraction of the series resistance, effective channel length and effective mobility for a MOSFET. A comparative study of these methods is presented by Yue Hao et al. [124] and depicted that at high gate voltage, these techniques maintained an accuracy in threshold voltage extraction, restricted the gate voltage range selection and eradicated the parameters of interdependence impact. Based on the conclusion of comparative study, an optimization technique for the extraction of the threshold voltage of the MOSFET is discussed which minimizes the variance of extraction techniques.

2.2.4 Substrate Noise Analysis and Estimation

The switching activities in digital circuits of system-on-chip are a prime source of generation of substrate noise. The complete representation of the injected substrate noise current by the digital part of the SoC is done using the technique proposed by Edoardo Charbon et al. [58]. This technique is taken as an advantage to model the gate by signal injected into the substrate which is dependent to input transition. To represent the noise contributed by each gate is calculated using the switching activity and the injection made by each gate. Ultimately, the addition of contributed noise from each gate provides the total injected noise from the digital section of the SoC. The substrate noise coupling analysis is made by Anil Samavedam et al. [20] using a macromodel technique for low resistive

substrate. The macromodel discussed provides the facility to scale the separation between the injector and receptor contacts. The issue of substrate noise coupling and optimization is also being taken care using the scalable separation between the contacts. Adil Koukab et al. [90] has exaggerated the extraction of substrate model and eliminated large storage of matrix by combining the substrate noise impact information and enhanced BEM. This method provides an accurate, fast extraction and demanded less computational complexity. An appropriate phase noise analysis in CMOS ring oscillator is discussed by Liang Dai et al. [103]. To analyze the phase noise, this method used the device noise as well as the switching activities of digital circuits coupled through the supply rail and the substrate in linear and nonlinear operation. It is shown that the phase noise can be reduced by the fast supply switching. Kamel Benaissa et al. [103] has explained the effect of resistivity of the substrate on the performance of the SoC and recommended the use of high resistive substrate to integrate the high performance RF CMOS systems. The recommendation is made on the basis of the comparative study that is comprised on-chip T-line, parasitic capacitors, inductor and s-parameter. The substrate and package analysis is made by Wen Kung Chu et al. [165] to analyze the inductive coupling between supply switching node and ground node because of the return of substrate current between them. The discussed analysis method explains the substrate noise simulation technique at the sensitive node of the SoC. The s-parameter based brief examination of substrate coupling is presented by Wen-Kuan Yeh et al. [107]. This analysis explains the dependency of isolation on the physical design dimensions. The substrate coupling is minimized by using guard bands and deep n-well, also, the substrate noise analysis is done for the mixed signal power system. The sensitivity of digital circuits is characterized and noise behavior of digital circuits is analyzed using the theoretical data. To estimate the substrate noise accurately in mixed signal system, a method is presented by Husni Habal et al. [54], which combines the

compressed switching information with the signature of cell library. A practical approach is obtained from this method for switching noise generation to simulate the substrate noise. Elad Alon et al. [110] has presented a technique to describe the statistical behavior of supply noise in VCO, which includes cyclostationary behavior; and this method is validated on 0.13 μm CMOS system. Another substrate noise estimation technique is proposed by Golnar Khodabandehloo et al. [131] which first extracted the substrate model using Green's function and then the substrate noise is simulated for the VCO with extraction model. The effectiveness of the extraction model explained by the simulated substrate noise along with the recommendation to use the p+ guard band to minimize the substrate noise. The substrate noise estimation techniques reviewed, accurately estimated the substrate noise, but demanded computational complexity for modeling of substrate noise.

A substrate noise detector is proposed by Byung-tae Kang et al. [170] which is integrated with SoC to detect the level of substrate noise in real time. The comparators and the counters are integrated with the detector to determine the errors and error repetition. This method used probabilistic line for the accurate estimation of substrate noise. The functioning of the detector and substrate noise estimation is validated for the adaptive digital to analog converter. The electro-dynamic model is used in Giorgos Manetas et al. [82] for the analysis of substrate noise unlike the electro-quasistatic model, which was a dominant method to analyze the substrate noise in past recent years. The electro-quasistatic model is valid for the frequencies over which the substrate coupling is assumed to be not dependent on the frequency. To examine the inductive coupling in the propagation of substrate noise, the electro-dynamics model is used and provided the electromagnetic analysis of coupling for the frequency range of interest. A block preference directed graph based technique to estimate the substrate noise in the early stage of floorplanning is presented by Minsik Cho et al. [148]. This technique used the noise characteristics of a set

of digital blocks to find the best possible location for the minimization of substrate coupling. This method is used for the physical design and floorplanning optimization for design of SoC. A voltage domain identification based substrate noise estimation technique is presented by Emre Salman et al. [55, 60]. In this method, the ground distribution network of the digital circuit possesses a small spatial potential difference and this potential difference is used in identifying the voltage domain on the substrate. In the same manner, the biased regions which were connected to ground network on a substrate can also be obtained, and an input equivalent port corresponding to each individual region is represented on substrate ignoring all other ports in the domain. The substrate noise in this method is estimated and analyzed for the reduced port with adequate accuracy at the sensor node and obtained a reduction of the order of four folds compared to the full extraction of digital circuit. A practical approach to solving the substrate noise issue in the design of SoC is presented by Hazem Hegazy et al. [91], which considered the substrate noise problem in parts instead of a whole. The generation of substrate noise, its transmission and reception are three different marked sections in which the generation is treated as the most sensitive section. In this technique, a top-down approach for noise generation with suitable macromodel is presented, it isolates the noise generator from noise sensor first and then combines the effect of noise generators at the sensor. The substrate noise is simulated at chip level by combining these two models. Stephane Bronckers et al. [66] explored the dominant substrate noise coupling mechanism with simulation in high resistive CMOS system. The results explained that the ground resistance plays an important role in substrate and coupling is dependent to the grounding resistant. It is also shown that the best isolation is obtained for the 0.8 Ω grounding resistance. A physics base substrate noise modeling and estimation method is discussed by Charif Mohamed et al. [146]. This method depicted that, the well regions of digital section of SoC owns free carriers and the substrate noise

generation occurs due to the impulsive movement of these free carriers. A high cut-off frequency is introduced by the transit time of carriers from well region to substrate and this frequency is directly dependent to the switching of digital circuits.

2.2.5 Performance of Analog/RF Circuits in Presence Substrate Noise

The digital substrate noise significantly affects the performance of the analog/RF circuits integrated with digital circuit over a common substrate, irrespective of substrate profiles. Mark Shane Peng et al. [145] explained the impact of substrate noise on the performance of analog/RF circuits and a substrate noise shaping technique is proposed. Almost a 20 dB of reduction in signal to noise ratio of delta-sigma modulator in the presence of digital inverters and about 10 dB improvement is observed in signal to noise ratio, by implementing the noise shaping technique on the same chip. First of all, Yo-Sheng Lin [120] has discussed how source to body resistance of the MOSFET has affected its RF performances. The results depicted that, as the reverse bias of substrate increased due to decreased transconductance, the isolation and transmission parameter become more imprecise and as separation between source-substrate increases, an improvement is observed at a cost of cut-off frequency at the maximum oscillation frequency. Yann Zinzius et al. [171] has discussed the effect of substrate noise on the performance of regenerative comparator and analog to digital converter. The results obtained from analog to digital converter fabricated on a low resistive substrate using of 0.35 µm CMOS process are revealed that 20% reduction in signal to noise ratio is observed. Since the analysis of the impact of substrate coupling in terms of isolation is insufficient due to the fact it does not provide the information regarding the actually affected parameters. Yongho Oh et al. [86] has analyzed the performance of RF MOSFET in the presence of digital substrate noise in terms of noise figure. A significant degradation in noise figure is observed as the drain to

source voltage become small or the device is functioning under weak inversion and is suggested to use of a dual guard band instead of the single guard band as it improves the noise figure. Stephane Bronckers et al. [59] addressed the analysis and impact of substrate noise coupling by a method on LC voltage controlled oscillator and wideband receiver designed with 90 nm and 0.13 μm CMOS technology respectively. The method is validated with 1-2 dB of accuracy.

2.2.6 Reduction Methods of Substrate Noise

The substrate noise coupling has severely degraded the performance of analog/RF circuits in the design of mixed signal SoC. The substrate noise must be reduced to improve the performance of the analog/RF circuits in mixed signal design. The substrate noise injection is mainly due to the supply bounce and is dependent to the switching of digital circuits. Makoto Nagata et al. [164] discussed an estimator to simulate and reduce the substrate noise based on the divided parasitic capacitance model. The discussed technique is implemented in CMOS circuits to reduce the supply bounce and achieved a 90 % reduction in comparison to the general CMOS circuit. Kamel Benaissa et al. [78] has discussed the effect of resistivity of substrate on the performance of RF CMOS for SoC application and recommended the use of high resistive substrate to reduce the substrate coupling and T Wen-Kuan Yeh et al. [107] suggested to use of active guard band for the reduction of substrate coupling. The recommendation to integrate substrate guard band with the traditional guard band is made for the reduction of substrate noise by Sun-Lai Hsu et al. [97]. The analysis depicted that when substrate guard bands are integrated in the traditional guard band the isolation of a p+ guard band is improved by -15 dB irrespective of substrate materials and profiles. Edgar Francisco Monteiro Albuquerque et al. [126] has introduced two logic families as current steering logic and current balance logic for the reduction

substrate noise in mixed signal SoC design. A small reduction in substrate noise is obtained using these logic families for the low power cell as well as a high power cell with low value power supply inductance. Current balance logic cell offered a significant reduction with higher value of power supply inductance than current steering logic cell. Toru Nakura et al. [172] discussed a substrate noise cancellation method using the feed forward power supply $di/_{dt}$detector. A triple well shielding technique is used by Roberto Rossi et al. [173] for the substrate noise reduction and Yongho Oh et al. [134] has examined the deviation in RF performance of MOSFET in the presence of substrate noise. A noise of certain level is injected to port and a variation up to 20% is observed in performance parameters as it deviated the threshold voltage. Substrate fluctuation takes place due to the injection of substrate noise, which is responsible for the variation in threshold voltage. Syed Muhammad Yasser Sherazi et al. [128] has proposed a technique to reduce the substrate noise, where digital circuit is designed to generate a supply current whose period is equal to clock period and reduced data dependency is obtained by using return to zero signaling. Stanley S. K. Ho et al. [174] discussed noise cancellation technique to reduce the substrate noise in the design of low noise mixer. An isolation method in oppose of substrate noise coupling and is discussed by Shinichiro Uemura et al. [87] using the existing through silicon via (TSV) technique and observed that it improved the isolation by 40 dB at 1 GHz frequency between different blocks of SoC. Jim Le et al. [165] has explained the null convention logic and with conventional Boolean clock logic estimated the substrate noise using both the techniques. It is advantageous in reference to substrate noise due to the switching, to use the digital circuits those are not sensitive to the delay. The method of null convention logic is validated using 0.25 μm CMOS random sequence generator and shown 23 dB reduction in substrate noise compared to the traditional CMOS logic. The nature of substrate noise is other than Gaussian nature, i.e. it is a non-Gaussian in nature and since

on time domain, its characteristics in any time slot repeats itself over the full time scale. The substrate noise is said to be a Non-Gaussian and cyclostationary noise process. Miguel A. Méndez et al. [129] has discussed the derivation of the substrate noise spectrum characteristics using an analytical model. The correntropy is defined and the difference between the kernel method and defined term correntropy is explained by Weifeng Liu et al. [168]. The assumption of Gaussian leads to the optimal second order statistics. It is suggested that the property of correntropy is entirely different to the second order statistics and very advantageous in the PDF estimation of non-Gaussian noise. Arpita Mukherjee et al. [166] estimated the probability density function of non-Gaussian non stationary noise. The modeling of non-Gaussian noise has done using the Gaussian mixture densities and an algorithm is developed for PDF estimation by maximizing the log likelihood function and is used priori and post priori updates.

CHAPTER 3

SUBSTRATE MODELING METHODOLOGIES

3.1 INTRODUCTION

The objectives of SoC design are the integration of a large number of transistors, high speed and compact size with multiple functionality on a single chip. It is needed to integrate the digital, analog and RF system on the single die on common substrate to fulfill the design objectives. Such system consists of the dissimilar functioning and the unwanted signal because of the integration of the heterogeneous block on a single die. Due to these constraints, the modeling of the substrate has become a need and it is difficult to model the substrate for exact estimation of substrate noise. The substrate noise coupling is an issue to be considered because of its impact on the performance of the mixed signal system [59]. In this chapter various substrate modeling techniques are studied and compared, and also substrate macromodels for various substrate profiles have been developed for the analysis of the substrate noise coupling. The electromagnetic behavior of the substrate is studied and the nature of the substrate is examined on the basis of the substrate parasitics [80, 81, 86]. The behavior of low resistive and high resistive substrate at lower and higher frequencies is studied to develop exact substrate macromodel. Owing to increase in operating frequency, the need of substrate modeling and its equivalent circuit at high as well as low frequencies are demanded in modern SoC design [100, 102, 104, 106]. The substrate modeling is needed for the analysis of substrate coupling in SoC and substrate coupling analysis is preferred before the layout extraction to limit the redesign time. Since, the substrate coupling has become an issue in complex and compact mixed signal system design. Therefore, the identification of substrate parasitics and substrate modeling have become a major concern in the SoC design [82, 89, 93, 96, 99].

3.2 SUBSTRATE PHYSICS

To simplify the substrate modeling and to study the substrate behavior, some assumption are made as hereunder; (i) Surface inversion will not be considered, (ii) The well and substrate junction is reversed biased, (iii) No Latch-up phenomenon occurs during the normal operation and (iv) negligence of coupling through inductance.

3.2.1 Resistive Effect

The equation of the conductivity of the doped semiconductor material is represented as:

$$\sigma = q\left(p\mu_p + n\mu_n\right) \tag{3.1}$$

Where q represents the electronic charge, n-type and p-type semiconductor has the mobility as μ_n andμ_p. The mobility of semiconductor is dependent to temperature and doping concentration. The limitation of the mobility occurs at high electric field and for normal operation it should not be considered while the limitation of mobility is due to the saturation velocity of charge carriers.

3.2.2 Capacitive Effect

The relative dielectric constant of Silicon material is given by:

$$\varepsilon_{rel_{Si}} = 11.7 \tag{3.2}$$

Then the absolute dielectric constant is:

$$\varepsilon_{Si} = \varepsilon_{rel_{Si}}.\varepsilon_0 \tag{3.3}$$

And the unit ofϵ_{Si} is $\left[\frac{\mathrm{pF}}{\mathrm{cm}}\right]$.

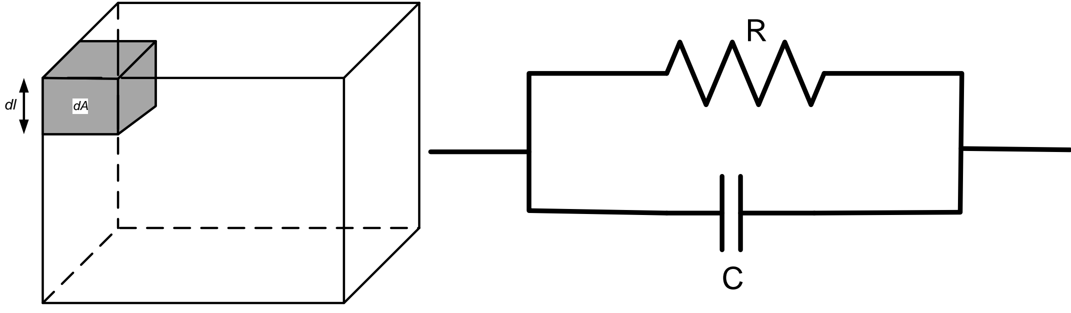


Figure. 3.1: R-C model of a homogeneous substrate

The admittance Y for a cube of substrate as depicted in the figure. 3.1 is given by:

$$Y = \frac{1+R\ C}{R} = \frac{1+j\omega T}{R} \tag{3.4}$$

Therefore, eq. (3.1) and (3.3) provides the time constant of substrate

$$T = R\ C = \frac{\rho\ dl}{dA}\frac{\epsilon\ dA}{dl} = \frac{\epsilon}{q(n\mu_n+p\mu_p)} \tag{3.5}$$

Time constant T in eq. (3.5) is not dependent on the dimensions of the piece of the substrate. For particular operating frequency and in case of homogeneously doped substrate parasitics capacitance can be neglected and substrate can be assumed as pure resistive in nature. For lower frequencies, resistance of substrate R (resistive nature) is more prominent and parasitic capacitance C will not have any significant impact. As the frequency of operation increase, the capacitive nature of the substrate will start impacting and the capacitive effect rises to become equal to the resistive effect which will be at cut-off frequency $f_{c,}$ which is defined as:

$$f_{c=} \frac{1}{2\pi T} = \frac{q(n\mu_n+p\mu_p)}{2\pi\epsilon} = \frac{1}{2\pi\epsilon\rho} \tag{3.6}$$

The f_c will be minimum for a high resistive and even for p-type substrate because, the electron mobility is greater than the hole mobility. The dependency of cut-off frequency on substrate doping for a homogeneous Silicon substrate is shown in figure. 3.10.

3.2.3 Effect of Substrate Parasitics

The impact of parasitics on the performance of the mixed signal integrated circuits will be more significant with an increase in the complexity of the system [82, 83, 84]. The substrate parasitics are complex in nature and have a negative impact on integrated circuit performance through the different medium as depicted in the figure. 3.2. In the SoC, the substrate works as a medium of current to flow to the ground and develops a voltage drop that ultimately affected the performance of SoC [132, 133].

The parasitic capacitance between wires and substrate introduces delay in signal transmission to the different part of the SoC. Most importantly, the various part of SoC are integrated over a common substrate which are not properly isolated and resulting into substrate coupling and crosstalk issues in the system. The substrate over which SoC is integrated affects the performance of SoC by introducing parasitic capacitance and resistance. A general structure is shown in figure. 3.3, which illustrates the formation of RLC structure by the substrate and bonding wires. For example, a capacitor of certain value is combined with bonding wire having a certain inductance will defiantly have a finite resonance frequency, which actually added the oscillation and make the system unstable.

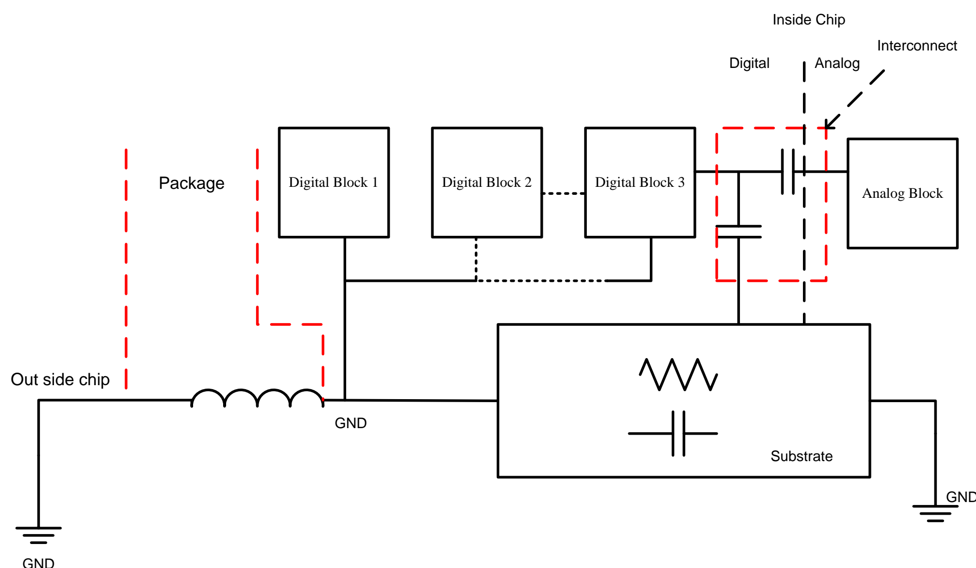


Figure. 3.2: Representation of parasitic effect in integrated Circuits

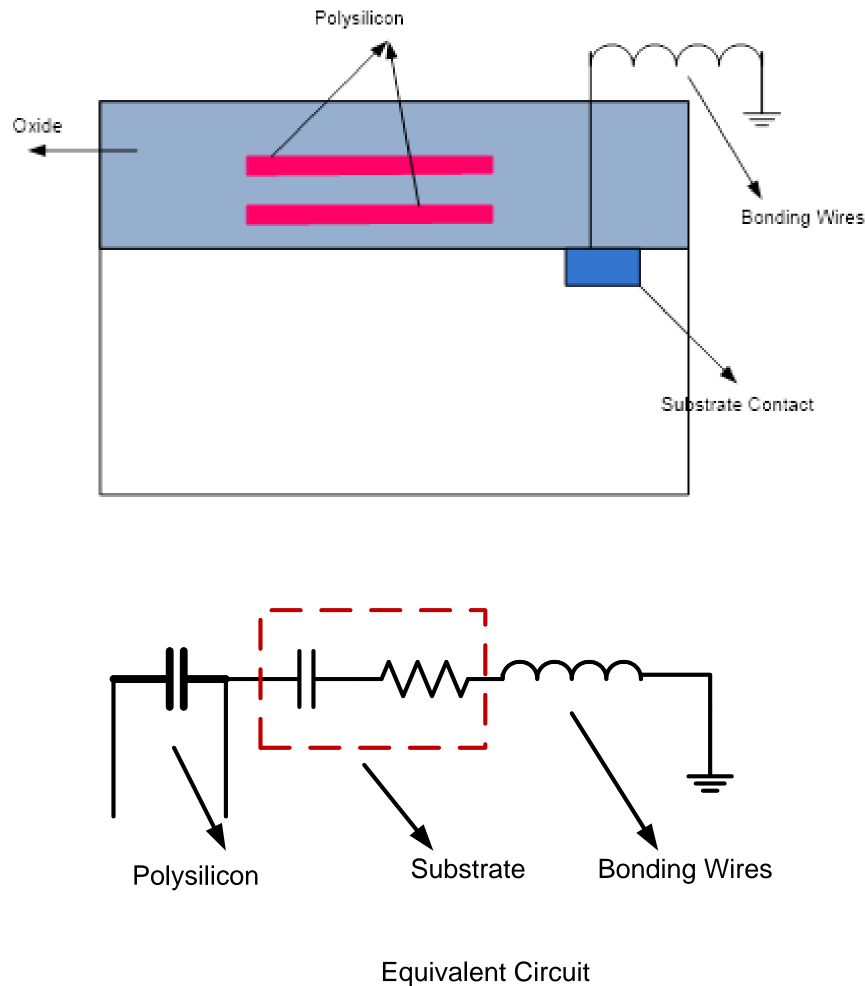


Figure. 3.3: Effect of parasitic capacitance formed by the Poly-silicon layer and its equivalent circuit

3.3 SUBSTRATE PROFILES: LOW RESISTIVE AND HIGH RESISTIVE

High resistive substrate and low resistive substrate are the basic types of substrate which are commonly used in the integrated circuit design [56, 66, 90]. The high resistive substrate is a combination of two layers of uniform doping and certain width. The resistivity of a bulk layer of high resistive substrate varies from 20 Ω-cm to 50 Ω-cm, and resistivity of the surface layer is having the resistivity of the order of 0.1 Ω-cm [115]. Since the resistivity of the surface layer is low, then the coupling between the substrate contact exists, because signal propagation occurs through the surface only [97, 103, 117]. The substrate noise reduction circuitry basically limits the coupling between the noise generator and noise

sensitive circuits. Thus the use of guard rings to reduce the coupling is very much popular in high resistive substrates. Separating the circuits with some distance will certainly reduce the crosstalk between noisy and sensitive circuitry.

The cross-section view of the high resistive substrate is given in the figure. 3.4. The integration of mixed signal integrated circuit over high resistive substrate faces one major challenge is Latch-up, which arises due to the formation of the parasitic bipolar transistors. These parasitic bipolar transistors provide a path between power supply and ground during the CMOS implementation which ultimately leads towards system failure.

The low resistive substrate is a combination of three different layers of even doping concentration and widths came into the picture for the better removal of Latch-up phenomenon. A low resistive substrate has the resistivity of its bulk layer of the order of 1 mΩ-cm to 2 mΩ-cm.

There a high resistive thin epitaxial layer between the bulk layer and the surface layer is patterned and has the resistivity of the order of 10 Ω-cm to 15 Ω-cm. The cross sectional view of a low resistive substrate is given in the figure. 3.5.

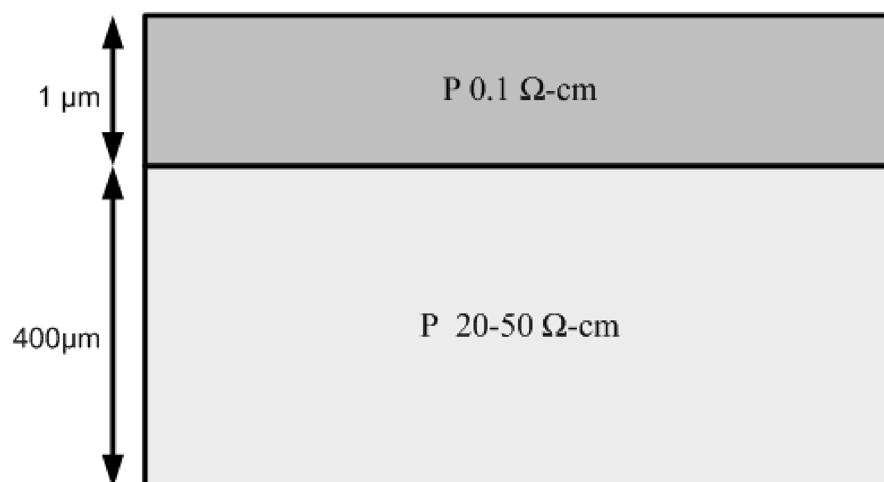


Figure. 3.4: Sectional view of a high resistive substrate

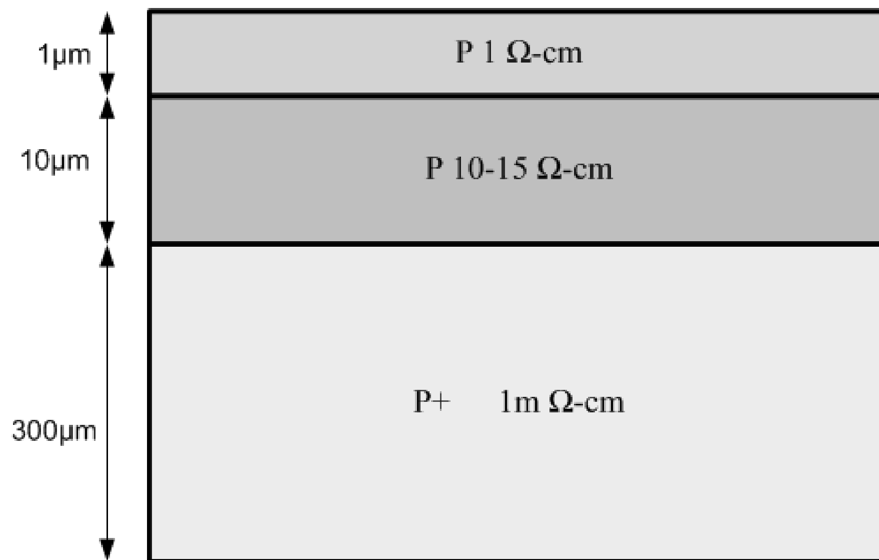


Figure. 3.5: Sectional view of a low resistive substrate

Since, there is a high resistance epitaxial layer between the surface and bulk layer, a low impedance path is formed from the surface layer down to the backplane. When the substrate contacts are fabricated with large separation, the impedance between them is larger than the impedance to the backplane. The high impedance between the contacts due to the large separation forces the substrate noise to travel downward to the backplane and then travels through the low resistive bulk and again back to the surface [115]. In low resistive substrate, the substrate noise coupling takes place through the low resistive bulk when the contacts are fabricated at larger separation e.g. 40 µm to 90 µm. Substrate coupling in mixed signal SoC has become independent of separation between the contacts after a certain distance. The large contact separation has enabled the implementation of noisy digital part and noise sensitive analog/RF part over a single substrate [97]. The only guard rings which are placed very close to the digital circuit are able to limit the substrate noise coupling between the circuits, otherwise, they are not very effective to reduce the substrate noise coupling. As discussed earlier, the substrate noise signal is able to affect the performance of circuits which are separated by a large distance, by travelling through the low resistive bulk of low resistive substrate. In high resistive substrate the coupling between the contacts occurs due

to the noise propagation on the surface, while coupling between the contacts reduces as the separation increases between them [56, 66]. Whereas, in low resistive substrate the noise coupling between the contacts is due to the noise travelling through the low resistive bulk even when the contacts are separated by a large distance and noise coupling become independent of distance after a certain distance between the contacts which is validated in section 3.5.

3.4 OVERVIEW OF PREVIOUS SUBSTRATE MODELING TECHNIQUES

Modelling of the substrate is the primary requirement to analyze the substrate noise coupling in the mixed signal SoC design. After considerable research efforts on substrate modeling, some analytical substrate modeling techniques have been proposed and categorized as Mesh-based modeling technique [135], Boundary-based modeling technique [136, 137] and compact macromodeling [74, 83]. The mesh-based and boundary-based techniques involves complex mathematical computation and led towards accurate mesh extraction. The involvement of complex mathematical computation actually reduces the scope of these modeling techniques even after accurate mesh extraction. These modeling techniques have limited the scope for small scale problems. This is actually a trade-off between the modeling complexity and modeling accuracy. The compact macromodeling has less analytical and mathematical complexity at a cost of accuracy. The brief details about some of the modeling techniques and parameters based comparison among them have been presented in this chapter.

3.4.1 Finite Difference Mesh Method

The substrate is assumed to be a conducting medium uniformly doped semiconductor layers of different doping concentration and a discretization technique is adopted in this assumption [135]. The node definition of whole substrate volume is done using the

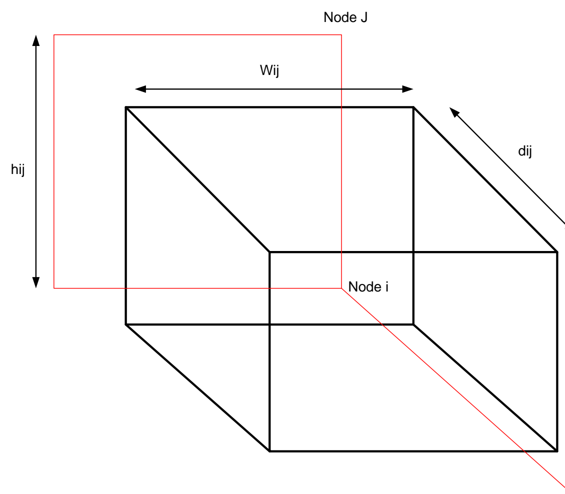
Maxwell's equation as shown in figure. 3.6 (a) and the electric field vector between the nodes is formulated. On the discretization of entire substrate volume, a mesh circuit is generated and this is a parallel combination of resistance and capacitance of nodes as shown in figure. 3.6 (b). The value of these elements has a dependency on process parameters (carrier concentration or dielectric constant) and can be determined by the extraction. The close form solution of Maxwell's equation does not hold if the different layer of substrate are doped with different doping concentration [56, 66, 138, 139]. So, to solve the Maxwell's equation substrate is further sectioned in elements of fixed resistivity and permittivity. Maxwell's equation becomes simplified when no magnetic field is considered. Starting from the continuity equation

$$\varepsilon \frac{\partial}{\partial t}(\nabla.E) + \frac{1}{\rho}\nabla.E = 0 \qquad (3.7)$$

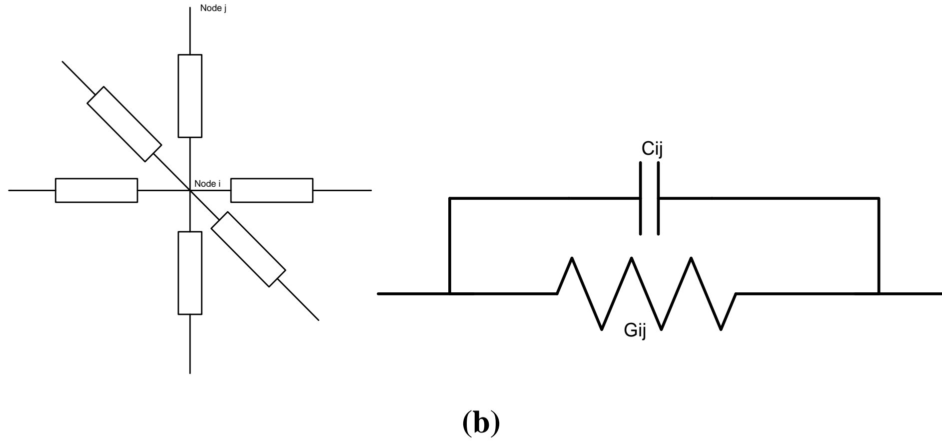
Or $\nabla.\left(\sigma\nabla\phi\left(x, y, z, t\right)\right) + \frac{\partial}{\partial t}\left(\nabla.\left(\varepsilon\nabla\phi\left(x, y, z, t\right)\right)\right) = 0$

If this continuity equation is solved for multidimensional cube and consider the substrate as a region of uniform material in electrostatic then this equation reduced to Laplace equation [6].

$$\nabla^2\phi = 0 \qquad (3.8)$$



(a)



(b)

Figure. 3.6: Representation of substrate (a) mesh and (b) electrical equivalent around mesh of the substrate

A cube shape substrate of close surface S, ofside $2d$, the Gauss's law gives a fixed electric field divergence at any indigenous point. So, at node i of cube, the electric field divergence is

$$\nabla . E = k \tag{3.9}$$

If the $\nabla . E$ is integrated for the entire cube volume V, the equation (3.3) can be written as;

$$\int \nabla . E dV = \int_{v} k dV = 8d^3 k \tag{3.10}$$

The divergence theorem gives that

$$\int_{V} \nabla . E dV = \int_{S} E dS \tag{3.11}$$

Hence, (3.11) can be rewritten as

$$\frac{1}{8d^3} \int_{S} E dS = k \tag{3.12}$$

Therefore,

$$\nabla . E = \frac{1}{8d^3} \int_{S} E dS \tag{3.13}$$

The integral in (3.11) can be approximated as

$$\int_s EdS = \sum_{j=1}^{6} Eij4d^2 \tag{3.14}$$

From the *j* node, the electric field to the node *i* is being approximated as;

$$Eij = \frac{Vi - Vj}{d/2} \tag{3.15}$$

Hence,

$$\nabla.E = \frac{1}{8d^3}\sum_{j=1}^{6}\frac{Vi - Vj}{d/2}4d^2 = \sum_{j=1}^{6}\frac{Vi - Vj}{d^2} \tag{3.16}$$

Using (3.16)

$$\sum_{j=1}^{6}\left[\frac{\left(V_i - V_j\right)}{R} + C\left(\frac{\partial V_i}{dt} - \frac{\partial V_j}{dt}\right)\right] = 0 \tag{3.17}$$

Where $R = \rho / 2d$ and $c = 2\varepsilon d$.

As it has been already mentioned that there is a trade-off between the accuracy and complexity in Finite Difference Mesh (FDM) Method. The number of grids are large enough to solve, then there are some suggestions which can be adopted for the reduction of RC networks. First, use a moment-matching method to reduce an RC mesh model, second use a coarse grid to reduce the overall number of grids, and third, ignore substrate capacitances and consider the substrate as a purely resistive mesh.

3.4.2 Boundary Element Method

When the unit current is injected to any point under suitable boundary conditions the potential at that point is defined by the Green’s function. In Boundary Element Method

(BEM), the Green's function is used for the substrate modeling in the mixed signal integrated circuit design and the macromodel developed by this method can be used in the circuit simulator for the analysis, impact and reduction of substrate coupling [136, 137].

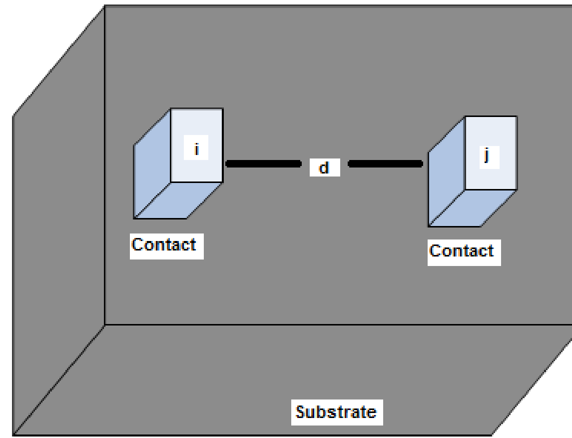


Figure. 3.7: A multilayer substrate view over which two equipotential contacts are placed

To formulate the Green's function for the structure given in the figure. 3.7, it has considered as electrostatic case and the capacitance between the contacts i and j is defined as

$$C_{ij} = \frac{Q_j}{\varphi} \tag{3.18}$$

Where; Q_j is charge at contact j and φ is potential of contact i, and by the Stoke's theorem, the capacitance between the contacts i and j is

$$C_{ij} = \frac{1}{\varepsilon} \oint_S E \cdot \hat{n} \, ds \tag{3.19}$$

Where; capacitance C_{ij} is surface integral of electric field E and outward normal vector $\hat{n}$ in medium. In the same manner the resistance between contacts i and j can be defined in medium of conductivity σas

$$R_{ij} = Y_{ij}^{-1} = \left[-\sigma \oint_s E \cdot \hat{n} \, ds \right]^{-1} = -\frac{1}{\sigma\varepsilon} \frac{\phi_i}{Q_j} \tag{3.20}$$

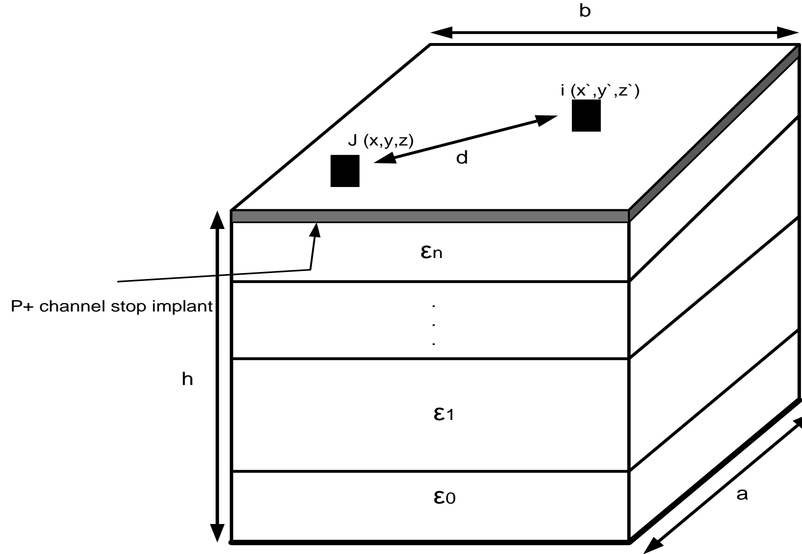


Figure. 3.8: Geometry of multilayer doping substrate over which two equi-potential contacts are placed

Since, the Laplace equation satisfies both the capacitive and resistive cases, therefore, it can be concluded that both the cases are interchangeable and can be interchanged. For the substrate taken under consideration, the susceptance of substrate is very much less than the conductance of the substrate up to the 15 GHz frequency. Then the substrate behavior will be governed by the resistances only and can be treated as pure resistive, since the susceptance of substrate can be ignored. For the electrostatic potential φ, the Poisson's equation can be re-written as;

$$\nabla^2\phi = -\frac{\rho}{\varepsilon} = 0 \tag{3.21}$$

If the r` is a point at which the current density is injected then the observed electrostatic potent at an observer point r can be obtained by applying the Green's function on eq. (3.21) and is defined as;

$$\phi(r) = \int_V \rho(r')G(r,r')d^3r' \tag{3.22}$$

Where; the boundary condition of the substrate is being satisfied by the Green's function G (r, r`) and V of the entire chip volume on the substrate. The potential at each contact is estimated and after averaging the potential at each contact, the electrostatic potential at a contact can be calculated. Using the eq. (3.22) the electrostatic potential of contact i can be approximated as;

$$\phi_i = \frac{1}{V_i \int_{V_i} \int_{V_j} \rho_j G dv_j dv_i} \tag{3.23}$$

Where; the volume of contact i and contact j is V_i and V_j respectively, $p_j$is charge distribution at contact j and is defined as $p_j = {Q_j}/{V_j}$. By putting this charge distribution in eq. (3.23) the potential at electrostatic potential at contact i is given as;

$$\phi_i = \frac{Q_j}{V_i V_j} \int_{V_i} \int_{V_j} G dv_j dv_i \tag{3.24}$$

A potential coefficient matrix [M] can be derived by taking eq. (3.24) in consideration and solving eq. (3.22) for each pair of contacts as;

$$[\Phi] = [M][Q] \qquad \text{And} \qquad [Q] = [p][\Phi] \tag{3.25}$$

Where; $p = M^{-1}$ and is induction coefficient matrix. A ground capacitance C_i for contact i and mutual capacitance is defined as;

$$C_i = \sum_{j=1}^{N} c_{ij}$$

Where; $C_{ij} = c_{ij}$and N is the size of matrix c. These are the basic boundary conditions using these the Green's function in a multilayer substrate as given in figure. 3.8 can be derived. The figure. 3.8 depicts the multilayer substrate of dielectric constants ε_n, where n

is the number of layers in multilayer substrate. If the substrate is assumed to be pure resistive lossy dielectric and backplane of substrate is grounded then the Green's function for the multilayer substrate consists of a series of sinusoidal function as;

$$G(r,r') = G_0 |_{z=z'=0} + \sum_{p=0}^{\infty}\sum_{q=0}^{\infty} f_{pq} C_{pq} \cos(\frac{p\pi x}{a})\cos(\frac{p\pi x'}{a})\cos(\frac{q\pi y}{b})\cos(\frac{q\pi y'}{b}) \quad (3.26)$$

Where; f_{pq} is given by

$$f_{pq} = \frac{1}{ab\gamma\varepsilon_N} \frac{\beta_N \tanh(\gamma_{pq} d) + \Gamma_N}{\beta_N + \Gamma_N \tanh(\gamma_{pq} d)} \quad (3.27)$$

And $\gamma_{pq} = \sqrt{(p\pi/a)^2 + (q\pi/b)^2}$

3.4.3 Resistive Macromodel Method

The substrate modeling techniques discussed earlier have a complex mathematical computation to develop a model of substrate for the analysis of substrate noise coupling in mixed signal SoC design. After rigorous effort of researching towards the simplification of the substrate modeling, a simple resistive macromodeling has come into the picture [74, 83]. Substrate macromodeling shows the fair visualization of substrate coupling at an early stage of design for the researchers, moreover, this technique is accurate and simple in modeling and required only three parameters based on the signal propagation path [127, 130].

This macromodeling method provides a more accurate result for the low resistive substrate. Since the cut-off frequency is dependent on the doping concentration, thus the lower resistive substrate is having the higher cut-off frequency than the high resistive substrate and is given in the equation (3.6). The variation of cut-off frequency with the substrate resistivity is shown in figure. 3.9.

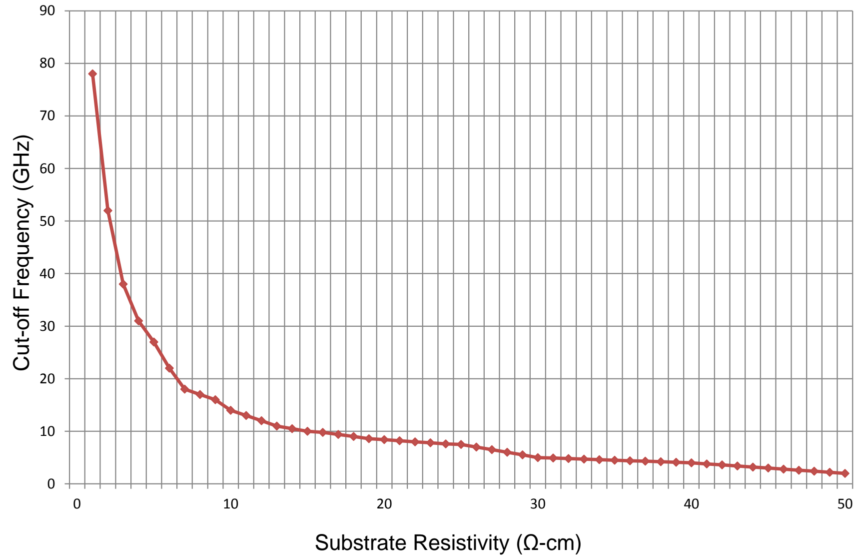


Figure. 3.9: Analytical variation of cut-off frequency with substrate resistivity

This method is based on the signal propagation line, as already discussed. Thus, two contact are placed over top of the substrate, one of which works as source contact and other as sensor contact and are separated by a distance d. Based on signal propagation lines, a substrate can be modeled as resistive network as shown in figure. 3.10, and it is best suited for the low resistive substrate.

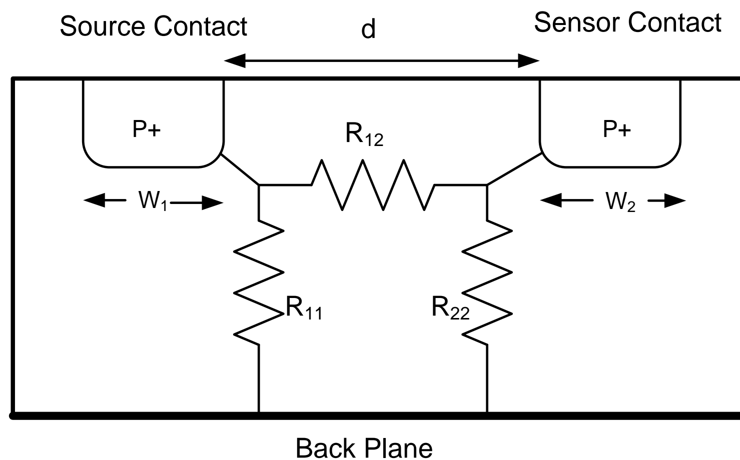


Figure. 3.10: Pure resistive macromodel for the substrate with grounded backplane

The conductance for the circuit in figure. 3.10 are given as,

$$G_{11} = \frac{1}{R_{11}}$$

$$G_{22} = \frac{1}{R_{22}}$$

And

$$G_{12} = \frac{1}{R_{12}}$$

Where, G_{11} is conductance from source, G_{22} are conductance for the sensor and G_{12} is cross coupling conductance between the substrate contacts. The resistive macromodel method can be used for the modeling of the different parts of the SoC, the macromodel for the different part of the SoC is given in the figure. 3.11.

Considering the figure. 3.10, the cross coupling resistance R_{12}between the contacts show variation in its value with variation in the distance between them. The analysis clearly explains this variation, when the value of d decreases the value of R_{12} also decreases and a rapid increment is noticed in the value of R_{12} with an increase in the distance d.

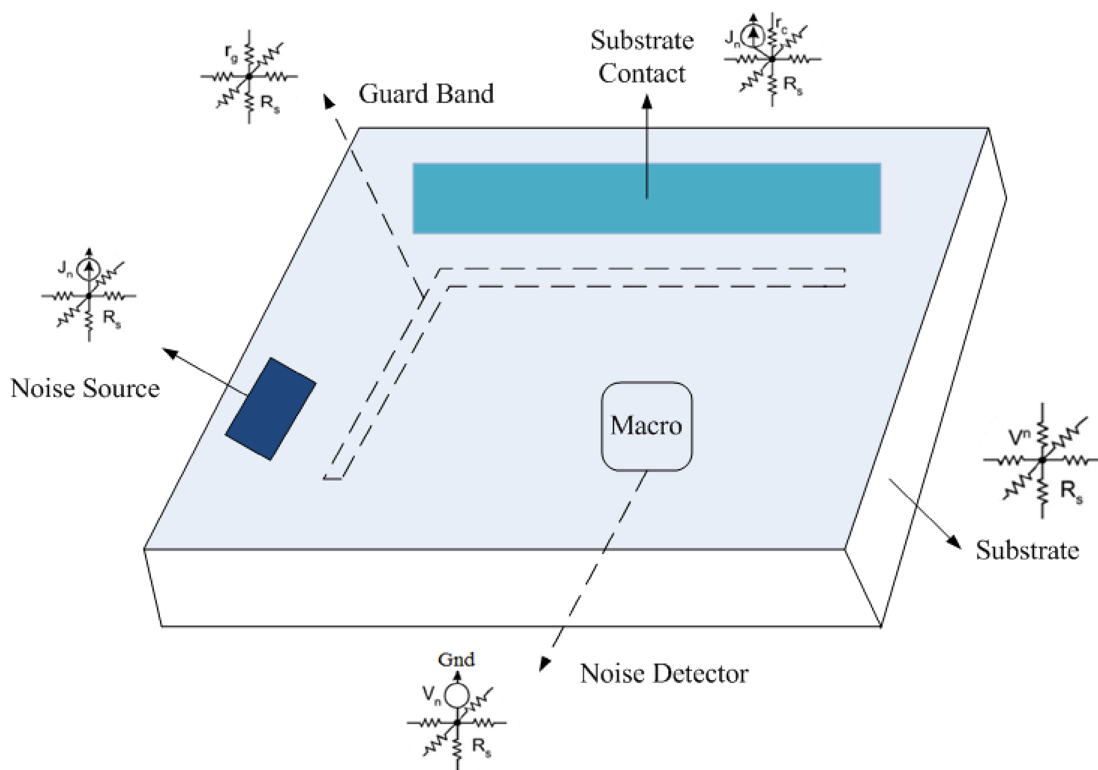


Figure. 3.11: Representation of resistive macromodel for the different part of the SoC

The values of R_{11} and R_{22} remains constant for any variation in distance d and show the independent behavior. The values of R_{11} and R_{22} are same, i.e. $R_{11} = R_{22} = R_2$ and conductance $G_{22} = {}^{1}/_{R_{22}}$ for the contacts having matched shape and size. A signal is applied to source port and currents is observed on the sensor port connected to ground. The Y-parameter of macromodel circuit in figure. 3.10 is given as;

$$Y = \begin{bmatrix} y_{11} & y_{12} \\ y_{21} & y_{22} \end{bmatrix} = \begin{bmatrix} G_{12} + G_{22} & -G_{22} \\ -G_{22} & G_{12} + G_{22} \end{bmatrix} \tag{3.28}$$

$$Z = \begin{bmatrix} z_{11} & z_{12} \\ z_{21} & z_{22} \end{bmatrix} = Y^{-1} = \frac{1}{G_{12}^2 + 2G_{12}G_{22}} \begin{bmatrix} G_{12} + G_{22} & G_{22} \\ G_{22} & G_{12} + G_{22} \end{bmatrix} \tag{3.29}$$

The determinant of the Y-parameter matrix is $\Delta = (G_{12}^2 + 2G_{12}G_{22})$. The impedance of source contact to substrate is z_{11} with all other contacts and is given by;

$$\begin{aligned} z_{11} &= \frac{G_{12} + G_{22}}{G_{12}^2 + 2G_{12}G_{22}} = \xi \\ => \quad & G_{12}^2 + 2G_{12}G_{22} - \frac{1}{\xi}(G_{12} + G_{22}) = 0 \end{aligned} \tag{3.30}$$

Where; ξ is constant and eq. (3.30) can be written as,

$$G_{12}(d) = \frac{1}{2\xi} - G_{22}(x) + \frac{1}{2\xi}\sqrt{1 + 4\xi^2 G_{22}^2(d))} \tag{3.31}$$

Where the simulation provides the value of conductance $G_{11}$and G_{22}, the relation between the $G_{22}$and distance d can ultimately be derived as,

$$G_{22}(x) = \alpha e^{-\beta x} \tag{3.32}$$

Where; the value of the constants α and β can be obtained from the simulation data.

Here, only two contacts are considered for the macromodel circuit and are sufficient to provide the result with accuracy, more accurate result can be drawn with more data.

The more data consideration provides the more accurate α and β [20, 114, 140]. The low resistive substrate can only be modeled as in the figure. 3.10, if and only if the operating frequency is not exceeding to 12-15 GHz. The comparison among the discussed modeling methods is given in the table 3.1.

Table 3.1: Comparison among the different substrate modeling techniques

Techniques	Accuracy	Difficulty	Simulation Time	Generality	Assumption made
Finite Difference Method	**Good** Depends Highly On The Resolution Of Discretization	**Hard** Large Mesh Matrix Size	**Long** Huge Matrix Sparse Size	Lightly and Heavily Doped Substrate	Consisting of Purely Resistive Mesh
Boundary Element Method	**Excellent** Within 10% Of The Actual Answer	**Hard** Cumbersome Mathematics	**Quite Long** DCT Can Be Used as an Efficient Solver	Lightly and Heavily Doped Substrate	Constant Current Density Across a Port
Resistive Macromodel Method	**Good** Improved By More Input Data	**Simple** Only 3 Parameters (α, β, ξ) Required	**Short**	Heavily Doped Substrate	Treated As a Resistive Network Up to some GHz Frequency

3.5 VALIDATION OF RESISTIVE MACROMODEL METHOD

3.5.1 Admittance between the Contacts:

As already discussed that the capacitive effect in mixed signal integrated circuits becomes prominent with the increasing operating frequency. To analyze the interaction amongst the various parts of SoC and estimate the impedance between them, two contacts are fabricated over both types of the substrate profiles. Since the substrate consists of different layers of different conductivities, therefore, the impedance has the dependency on the operating frequency. The contacts placed over the top of the substrate have a certain size and spacing between them. The dimension of the each contact is $10\mu m\ X\ 10\ \mu m\ X\ 0.25\ \mu m$, and the separation between them is $50\mu m$. The back-plane of the substrate is grounded and both contacts are representing the noisy digital and sensitive analog block of SoC respectively.

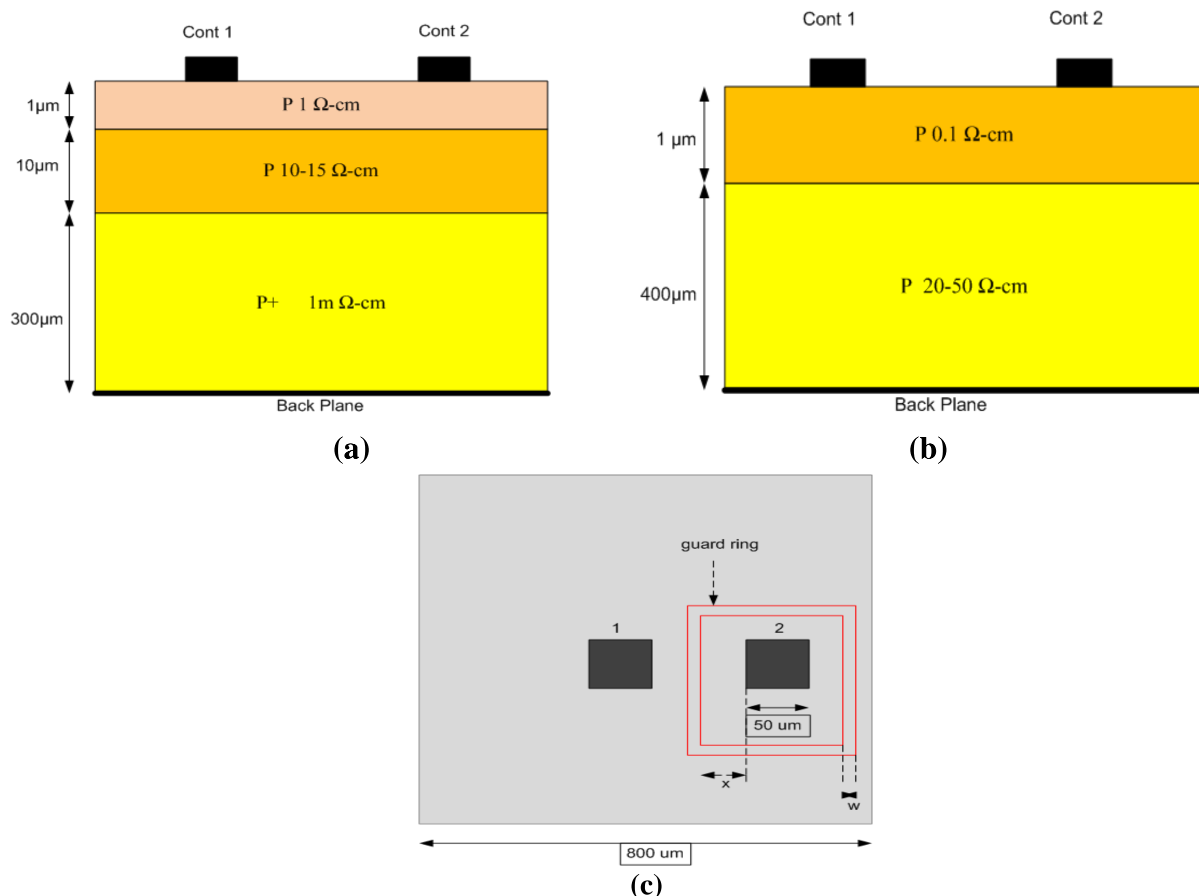


Figure. 3.12: Representation of substrate profiles with contact on top (a) for low resistive substrate (b) for high resistive substrate (c) guard ring placed around contact 2

The impedance between the contacts provides truthful information about substrate coupling which can further be used for full integrated circuit simulation. In advance step a guard ring of width 4μm is placed around one of the contacts (digital contact) and the analysis is made for low resistive substrate as well as high resistive substrate as shown in figure. 3.12 (a), (b) and (c).

In this section, the admittance between the contacts for low resistive substrate and for high resistive substrate is simulated at the same operating frequency range. The same analysis and simulation are done for both substrate profiles when the guard ring is fabricated around the noisy digital contact and sensitive (analog) contact is left open [83, 115, 117].

In case of low resistive substrate when no guard ring is placed around any contact, the admittance behavior with operating frequency is observed and is depicted in figure. 3.13. The observation shows that, the admittance is independent of frequency up to 6 GHz and the impact of frequency on admittance between the contacts starts significantly after 10 GHz. It is also noticed that the admittance values between the contacts is of the order of 10^{-6} mho and the admittance between the contact 1 and backplane is less than the admittance between the contacts, which is of the order of 10^{-3} mho.

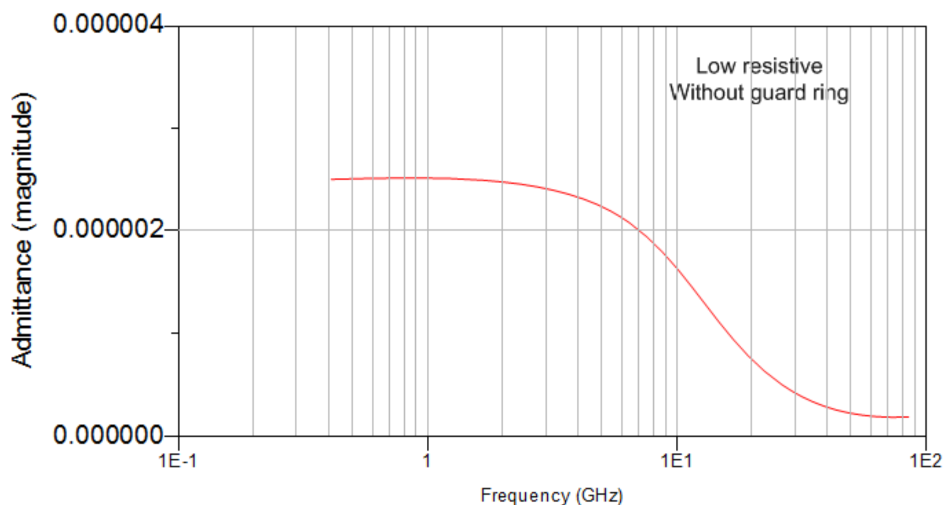


Figure. 3.13: Admittance between $cont_1$ and $cont_2$ without a guard ring in low resistive substrate without guard ring

In case of low resistive substrate when the guard ring is placed around the contact, the admittance behavior with operating frequency is observed and depicted in figure. 3.14. The observation shows that, the admittance is independent of frequency around 10 GHz and the impact of frequency on admittance between the contacts starts significantly after 15 GHz. It is also noticed that the admittance values between the contacts is of the order of 10^{-8} mho and the admittance is frequency independent for the longer operating frequency.

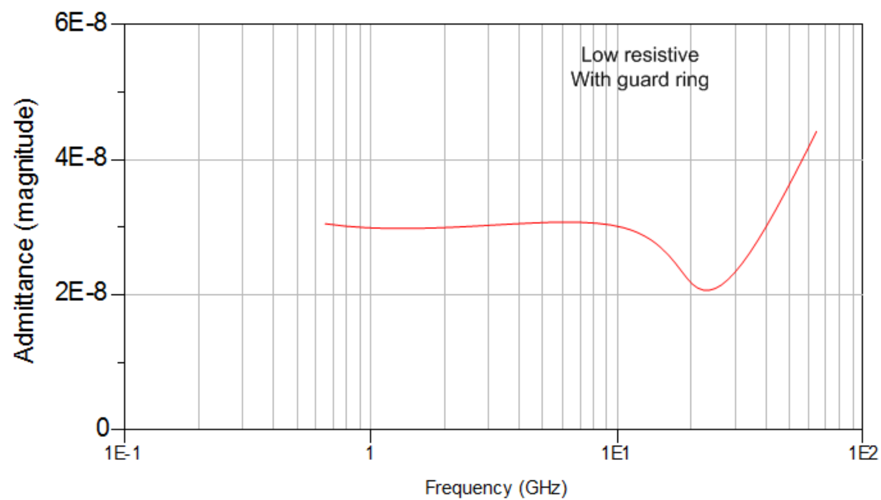


Figure. 3.14: Admittance between $cont_1$ and $cont_2$ without a guard ring in low resistive substrate with guard ring

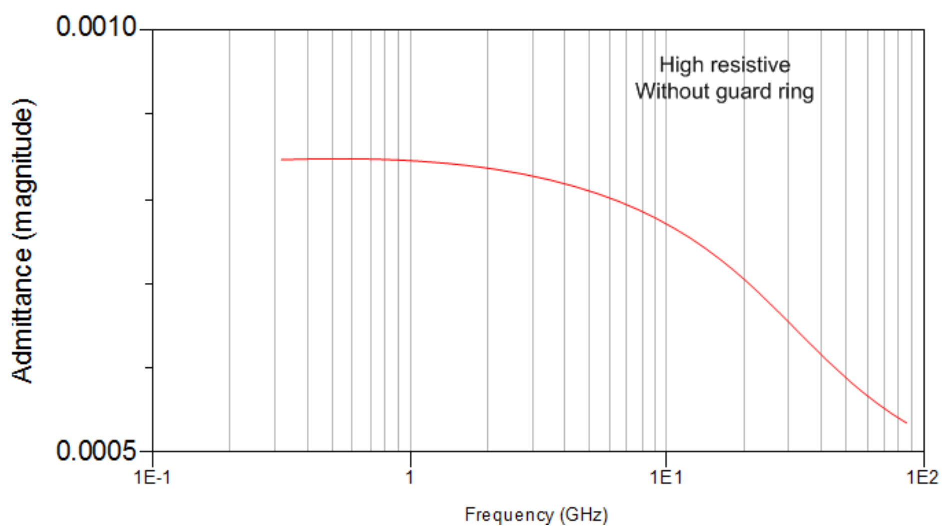


Figure. 3.15: Admittance between $cont_1$ and $cont_2$ without a guard ring in the high resistive substrate without guard ring

In case of high resistive substrate the analysis is made in the same way as in case of low resistive substrate.

The nature of admittance with frequency in high resistive substrate when no guard ring is placed between the contacts is observed and is shown in figure. 3.15. It is observed that the admittance between the contacts is independent of frequency up to few GHz and the admittance is significantly shown its dependency on frequency after 8 GHz.

The nature of admittance with frequency in high resistive substrate when the guard ring is placed between the contacts is observed and shown in figure. 3.16. It is observed that admittance between the contacts is independent of frequency up to few GHz and admittance is significantly shown its dependency on frequency after 10 GHz.

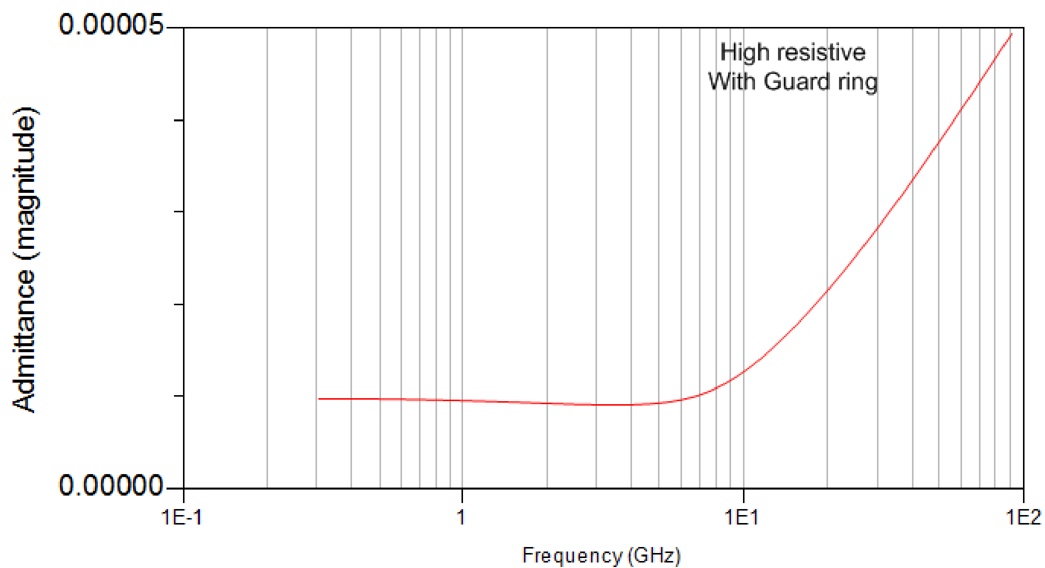


Figure. 3.16: Admittance between $cont_1$ and $cont_2$ without a guard ring in high resistive substrate with guard ring

It is very clear from the observation, that in a high resistive substrate with guard rings, the significant impact of frequency on admittance is seen after 10 GHz. Since, the resistivity of surface of low resistive substrate is higher than that of the resistivity of surface of high resistive substrate, the admittance between the contacts in low resistive substrate is having

a lower value than high resistive substrate; whereas the admittance is remains frequency independent for larger operating frequency in the high resistive than in low resistive substrate. As the frequency of operation keeps on increasing beyond 15 GHz, the substrate behavior will not be pure resistive but will also needed capacitance to model the substrate for the analysis of substrate noise coupling.

3.5.2 Isolation between the Contacts

In this section of the study, the isolation is observed between the contacts placed on the surface of the low resistive substrate and high resistive substrate. The two contact configuration over the surface of substrate is given by the figure. 3.17. Each contact has a size of 50 µm and is separated by scalable distance d. The isolation is observed by keeping one contact at a fixed position and moving other contact away from fixed contact. Observation is made on the basis of simulation result of the electrical set-up of low resistive substrate provided in the figure. 3.18. For the low resistive substrate profile figure. 3.12 (a) is referred and the specification is as $\rho_{surface}$ is 1Ω cm, $\rho_{epitaxy}$ is 15Ω cm and ρ_{bulk} is 10mΩ cm.

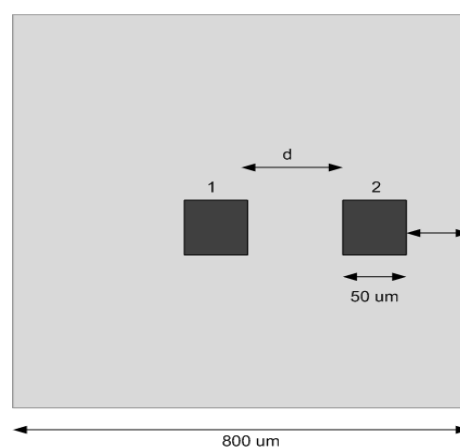


Figure. 3.17: Two contact configuration for both types of substrate

Considering the figure. 3.18 and simulation is done for the different values of grounding inductance L. The value of L is taken $0\ nH, 1\ nH\ and\ 3\ nH$ for three different simulations;

while the values of C_{S1} and C_{S2} are kept fixed and is equal to 0.3 pF and frequency is set to be 1 GHz. The signal is applied at the injection port and the observation for isolation is made at the reception port for the different backplane inductance, which is shown in figure. 3.19. When the value of back-plane inductance L is 3 nH, then it is observed that the isolation becomes independent of separation between the contacts d. The reason behind this is the value of resistance R_{12} become very less than the reactance of C_{S1} and C_{S2}. In the second case when the value of back-plane inductance L is 1 nH, then the isolation is almost showing the same nature as discussed in the previous case as when $L = 3\ nH$, the isolation becomes independent of separation after a certain distance and the reason is again as explained.

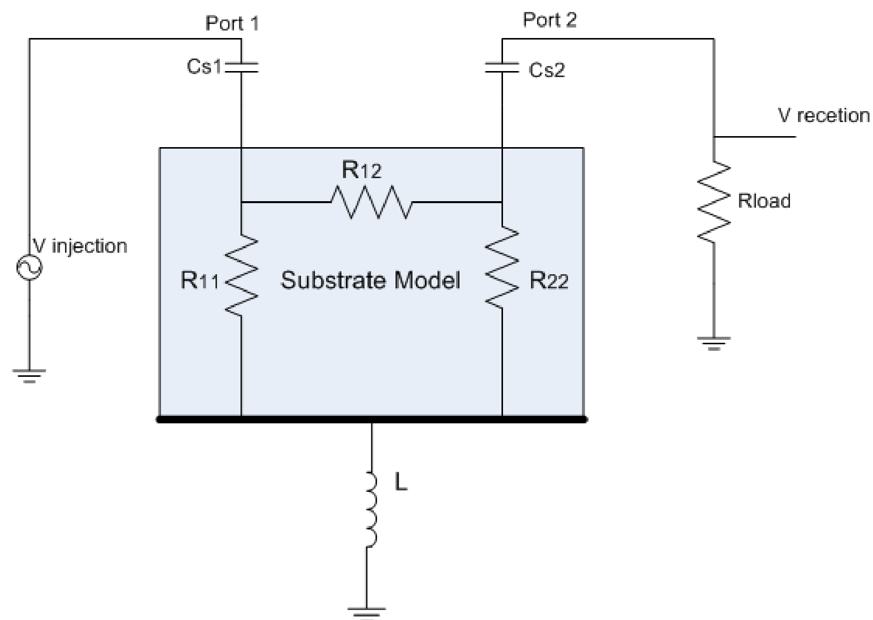


Figure. 3.18: Electrical set-up to simulate the isolation for low resistive substrate

As it is expected that isolation must increase with increasing distance, so these above discussed cases cannot be said as a helpful and favorable condition. Now the value of back-plane inductance L is taken 0 nH, in this particular case, as the separation increases the isolation between the contacts is also increases.

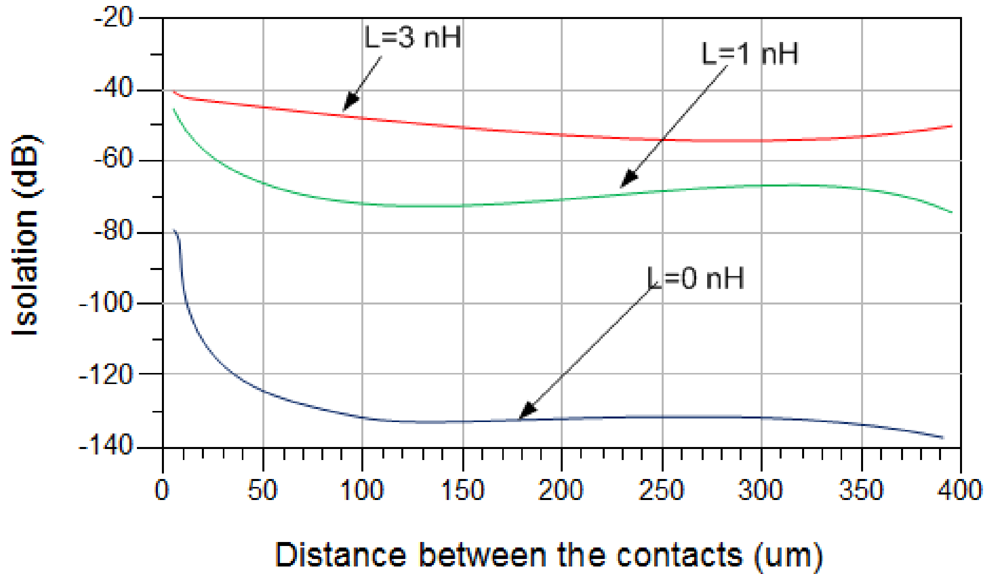


Figure. 3.19: The isolation between the contacts at different values of *L* for low resistive substrate

The backplane impedance plays an important role for isolation in both low resistive and high resistive substrate, since the isolation is sensitive to the backplane impedance.

All the above discussed exercises to simulate the isolation between two surface contacts is done again, to observe the isolation in high-resistivity substrate. To simulate the isolation in high resistive substrate, the substrate profile given in the figure. 3.12 (b) is referred and the specifications are as $\rho_{epitaxy}$ is equal to $0.1\ \Omega\ cm$ and ρ_{bulk} is equal to $20\ \Omega\ cm$. The electrical setup to simulate the isolation between the surface contacts is provided in the figure. 3.20. The signal is applied at the injection port and the observation for isolation is made at the reception port for the different back-plane inductance, which is shown in figure. 3.21. Considering the figure. 3.20 and simulation is done for the different values of back-plane inductance L. The value of L is left floating, $0\ nH\ and\ 3\ nH$ for three different simulations; while the values of $C_{S1}\ and\ C_{S2}$ are kept fixed and is equal to $0.8\ pF$ and frequency is set to be 1 GHz. When the back-plane inductance L is left floating, it is observed that the isolation is weakly dependent or independent to separation between the

contacts; the reason behind this is the value of resistance R_{12} is having the comparable value of reactance of C_{S1} and C_{S2} at this particular operating frequency.

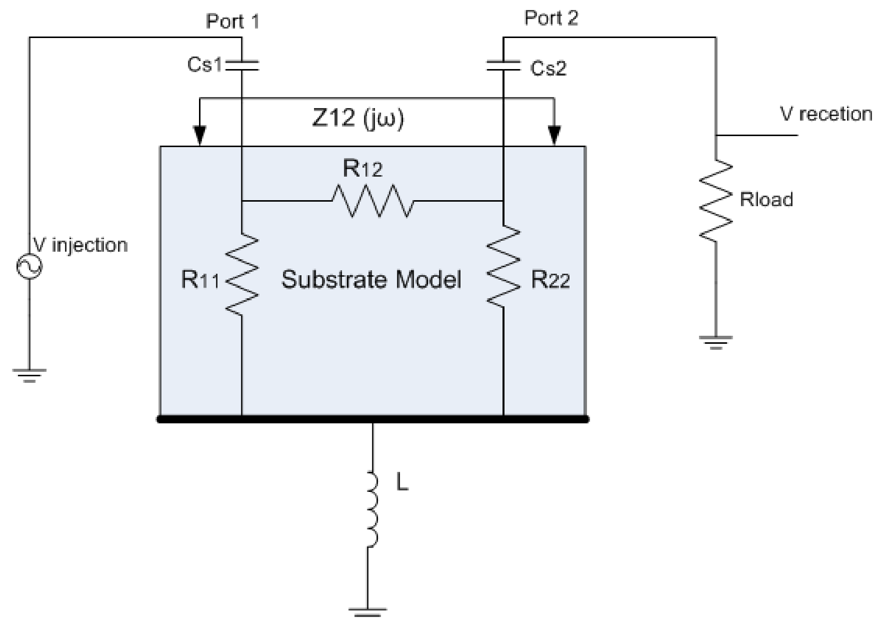


Figure. 3.20: Electrical set-up to simulate the isolation for high resistive substrate

When the back-plane inductance L is $3\ nH$, then it is observed that the isolation is not dependent upon the separation between the contacts after a certain distance d. This is again a case of weakly dependency or independency. Now in this case, when the back-plane inductance L is $0\ nH$, in this particular case, as the separation increases the isolation between the contacts also increases. As discussed in the case of low resistive substrate that the isolation is very sensitive to the backplane impedance, but here in case of high resistive substrate isolation is not very much sensitive to backplane impedance and said to have weakly dependent to the backplane impedance.

In the case of high resistive substrate most of the signal propagation takes place through the surface of the substrate unlike in low resistive substrate where propagation is vertically downward and then back to the surface of substrate. Observation depicts that the surface layer is responsible for the coupling between the contacts or different part of SoC integrated

over it, so the substrate taps will be more efficient and helpful in the high resistive substrate than low resistive substrate.

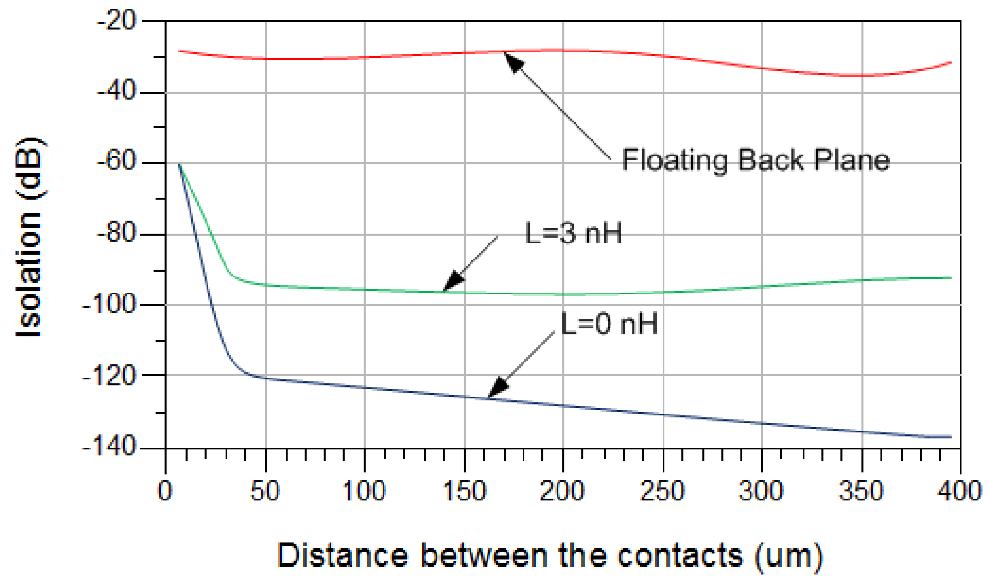


Figure. 3.21: The isolation between the contacts at different values of *L* for low resistive substrate

CHAPTER 4

ESTIMATION OF SUBSTRATE NOISE IN VLSI CIRCUITS

4.1 INTRODUCTION

The fundamental components in SoC design or analog/RF circuit design are the transistors therefore, before studying the performance of SoC in the presence of substrate noise and how substrate noise has affected the performance of SoC, it is important to study the behavior of transistors in the presence of substrate noise. The primary requirement is to understand the generation of substrate noise, injection of substrate noise into the substrate, propagation of substrate noise through the substrate and its impact on analog/RF circuits. In this chapter, a noble methodology is proposed for the estimation of substrate noise spectrum and also the behavior of high performance analog/RF circuits are discussed in the presence of substrate noise. The substrate noise coupling is mainly due to the parasitics in the substrate which are frequency dependent and even different substrate profiles have shown different parasitics behavior with frequency. Thus, the substrate model is again a matter of concern for the analysis of substrate noise coupling. Various substrate modeling techniques have been explained in the previous chapter. The macromodeling of the substrate is also discussed in the last chapter with its limitation, referring to the frequency of operation. This chapter completely focuses on the estimation of substrate noise in transistor and high performance analog circuits using the macromodeling and proposed methodology. The circuit macromodeling is used to estimate the substrate noise in CMOS system and the in chain CMOS inverter. The MOSFET performance in the presence of substrate noise along with the substrate noise estimation in full adder and in Low noise amplifier (LNA) with the simulation results are explained in this chapter. A practical case is also discussed with power spectral density of substrate noise and validated with the

simulation results. Two amplifiers are integrated on a common high resistive substrate, the first one is digital CMOS inverter while the second is a saturated load NMOS inverting amplifier. These amplifiers are operating on two different frequencies and are separated by a variable distance. The input at analog amplifier is applied first and the coupling between these two transistors is analyzed from the power spectral density of substrate noise. Again the input signals are applied at both the analog as well as digital amplifier and the coupling is analyzed by providing the different separation between them.

4.1.1 Simulation Methodology for Substrate Noise Spectrum

The spectrum of substrate noise provides clearer information about the substrate noise coupling. A noble and efficient methodology is proposed to obtain the spectrum of the substrate noise. This methodology suggests that the input noise current signal from the digital section and is applied to the probabilistic analysis block where the statistical characteristics of the noise signal is obtained and the output of this block is applied to current waveform characteristics and to the substrate noise generation block simultaneously. This provides the transfer function of substrate noise and finally the substrate noise spectrum is obtained. The package and board parasitics are not taken into account in this method. A detailed discussion on the methodology is provided in section 4.6 and existing estimation methods are detailed in [59, 60, 84, 100, 132].

4.2 EFFECT OF SUBSTRATE NOISE ON MOSFET PERFORMANCE

This section elaborates the effect of substrate noise on the DC performances of MOSFET and the variation in the parameters of the MOSFET as well. The MOSFET structure which is considered in the analysis is given in the figure. 4.1. In this analysis various substrate noise injection levels are applied and the performance of the MOSFET is observed for a fixed drain to source voltage of 0.8 V. The plot between V_{gs} and I_d is shown in Figure. 4.2,

which clearly depicts the variation in drain current with a variation in noise injection level. When the noise injection level increases the drain current is also increased, i.e. curve shifts upward for a fixed drain to source voltage. The change in the amplitude of the drain currents is observed due the variation in the threshold voltage V_T and the variation in threshold voltage is because of the injected noise.

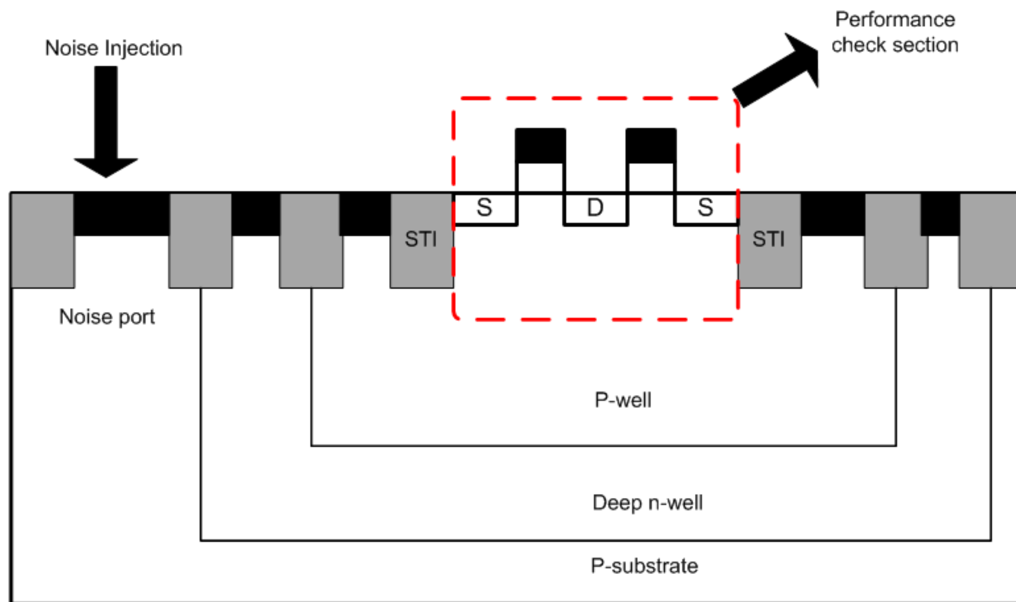


Figure. 4.1: Structure of MOSFET used in analysis

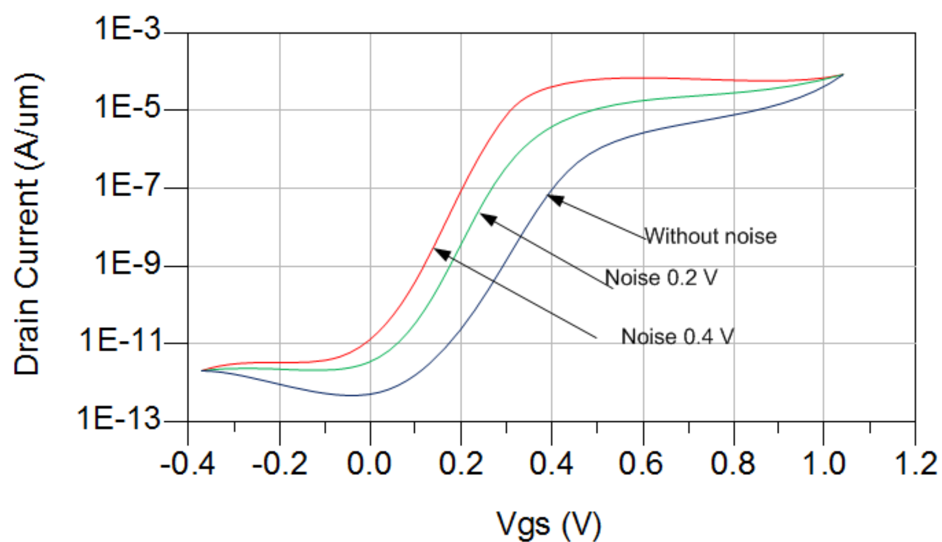


Figure. 4.2: Plot between V_{gs} and I_d with different noise injection level

The threshold voltage variation will definitely be affected by the MOSFET conduction and hence the variation is observed in the amplitude of the drain current. The variation of threshold voltage V_T with the different level of injected noise is shown in figure. 4.4 and it is observed that the threshold voltage V_T is decreased with the increased injection level of the substrate noise. This shift in threshold voltage V_T is enabled the variation in other RF parameters of the MOSFET and these are shown is in the table 4.1.

A variation in the substrate potential is seen when the substrate noise couples through the substrate. For the analysis of this variation in substrate potential a pulse shaped noise of 0.6 V is applied and the potential of the substrate is observed and shown in figure. 4.4. The injected noise signal varies between level 0 to 0.6 V and after simulation substrate potential signal is observed to be a deformed pulse shaped with reduced amplitude. The signal level varies between the -0.4 V to -0.2 V. The reason behind the deformation in shape and reduction in voltage level is an RC delay in the substrate and attenuation in the propagation path.

Table 4.1: Observed variation in performance of MOSFET

Parameter	Unit	Without Noise Injection	With Noise Injection		
			0.2 V	0.4 V	0.6 V
f_T	*GHz*	47.4	51.8	53	54.1
f_{max}	*GHz*	144.0	153.3	158.2	160.2
g_m	*mS*	19.7	21.8	23.3	24.0
g_{ds}	*mS*	1.14	1.24	1.33	1.38

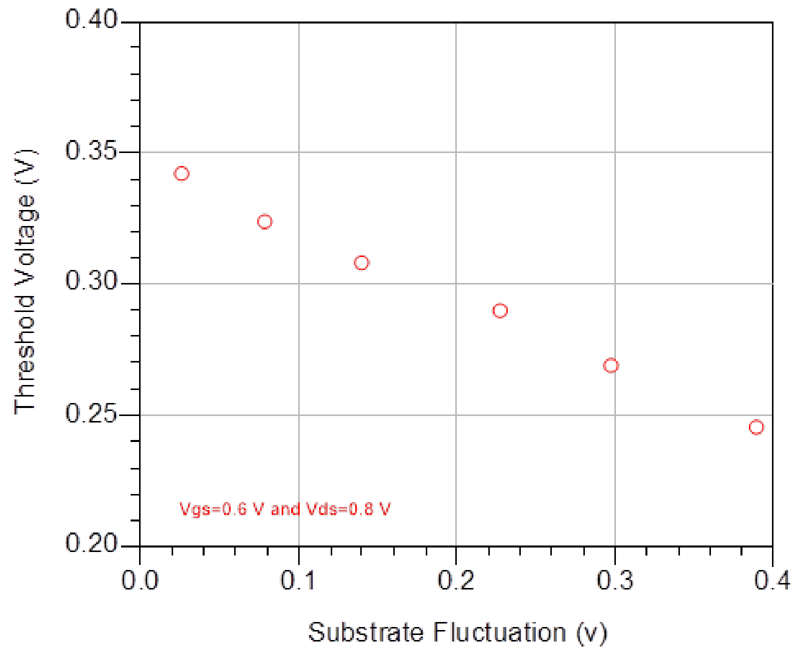


Figure. 4.3: Threshold voltage variation due to the substrate noise injection

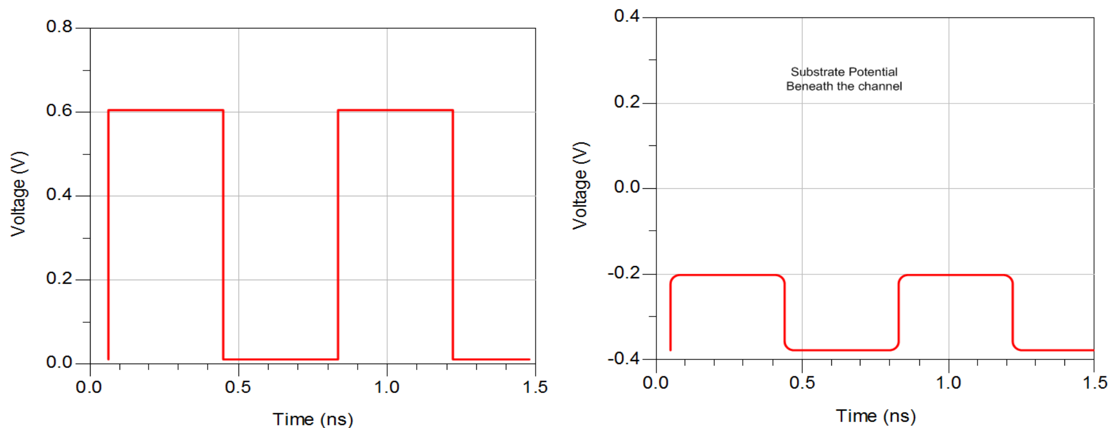


Figure. 4.4: Injected noise to the MOSFET and simulated substrate potential beneath the channel of MOSFET

4.2.1 Noise Figure Analysis of MOSFET

The noise figure is an important parameter to be analyzed to understand the noise behavior of a MOSFET. In this section the noise figure for the MOSFET is analytically derived. The small signal model of the MOSFET is shown in figure. 4.5. The analysis of the noise figure is based on two assumptions. Firstly, when the thermal noise is greater than substrate noise

and secondly, when the substrate noise is greater than thermal noise of the MOSFET. The presence of substrate noiseV_{sn} and equivalent resistance for substrate noise R_{sn} is shown in the MOSFET small signal model which indicates the presence of noise. The input and output ports are shorted one by one, of the given circuit (figure. 4.6) to obtain the noise figure and the assumptions are applied [144]. The assumptions are given as; first, when$\overline{E^2{}_{n2}} \gg \overline{E^2{}_{n1}}$, i.e. substrate noise is much greater the MOSFET thermal noise, second, when $\overline{E^2{}_{n1}} \gg \overline{E^2{}_{n2}}$ i.e. MOSFET thermal noise is greater than substrate noise and third, when$\overline{E^2{}_{n1}} \sim \overline{E^2{}_{n2}}$ i.e. MOSFET thermal noise is comparable to substrate noise.

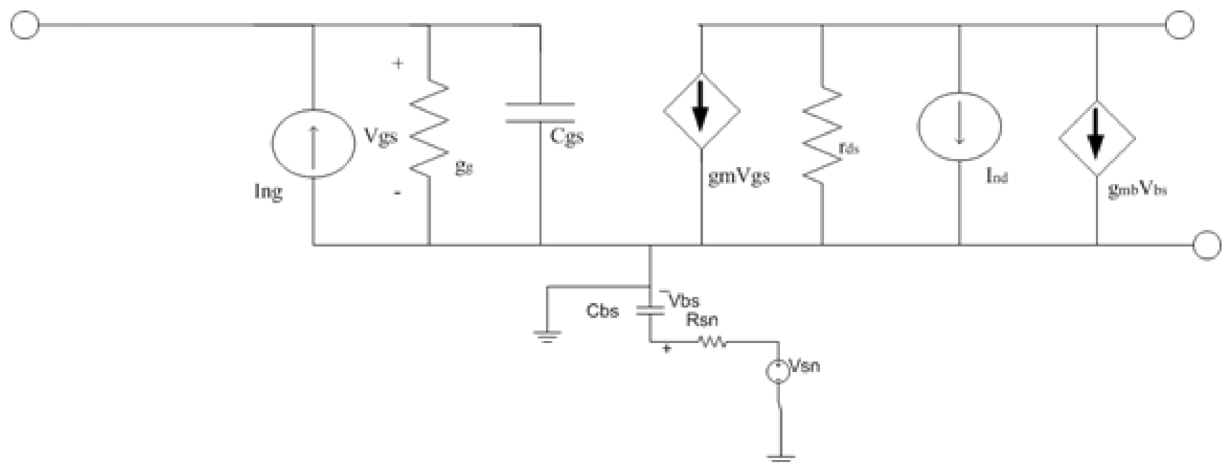


Figure. 4.5: Small signal equivalent of MOSFET with substrate noise

1) With shorted input and output ports,

$$E_n = E_{n1} + E_{n2}$$

Where; $E_{n1} \equiv i_{nd}/g_m$, $E_{n2} \equiv (g_{mb}/g_m)\, v_{sn}/(1+ \tau s)$, and $\tau \equiv R_{sn}C_{bs}$

Where; i_{nd} is uncorrelated input current noise.

2) the correlated admittance for the open input port and shorted output port,

$$Y_C = Y_{c1} \frac{\overline{E^2{}_{n1}}}{\overline{E^2{}_{n1}} + \overline{E^2{}_{n2}}} + j\omega C_{gs} \frac{\overline{E^2{}_{n2}}}{\overline{E^2{}_{n1}} + \overline{E^2{}_{n2}}} \quad (4.1)$$

If $\overline{E^2{}_{n2}} \gg \overline{E^2{}_{n1}}$, then$Y_c \simeq j\omega C_{gs}$. On the other hand, for $\overline{E^2{}_{n1}} \gg \overline{E^2{}_{n2}}$, $Y_c \simeq Y_{c1}$

A. When $\overline{E^2{}_{n2}} \gg \overline{E^2{}_{n1}}$ If $\overline{E^2{}_{n2}} \gg \overline{E^2{}_{n1}}$, i.e., $\overline{v^2{}_{sn}}$ is greatly larger than the thermal noise of MOSFET

$$G_u \equiv \frac{\overline{\overline{i^2{}_u}}}{4kT\Delta f} = \frac{\delta\omega^2 C^2{}_{gs}(1-|c|^2)}{5g_{do}} \quad (4.2)$$

$$R_n \equiv \frac{\overline{E^2{}_u}}{4kT\Delta f} \simeq \left(\frac{g_{mb}}{g_m}\right)^2 \frac{P_{sn}(f)}{(1+ \omega^2\tau^2)\, 4kT} \quad (4.3)$$

The minimum noise figure $F_{min} = 1 + 2R_n\left(G_{opt} + G_c\right)$ of noisy two port is found to be

$$F = F_m + \frac{R_n}{G_s}\left[\left(G_s - G_{opt}\right)^2 + \left(B_s - B_{opt}\right)^2\right]$$

Where; G_s and B_s are source admittance.

Thus,

$$F = 1 + \frac{g_{mb}}{g_m}\sqrt{\frac{P_{sn}(f)}{(1+ \omega^2\tau^2)kT}\frac{\delta\omega^2 C^2{}_{gs}(1-|c|^2)}{5g_{do}}} + \frac{\left(\frac{g_{mb}}{g_m}\right)^2 \frac{P_{sn}(f)}{(1+\omega^2\tau^2)}}{4kTG_s}\left[\left(G_s - G_{opt}\right)^2 + \left(B_s + \omega C_{gs}\right)^2\right] \quad (4.4)$$

Where; G_{opt}, B_{opt} are representing their optimal values, $P_{sn}(f)$ is representing the power spectral density of substrate noise, F is noise figure and F_m is minimum noise figure.

B. When $\overline{E^2{}_{n1}} \gg \overline{E^2{}_{n2}}$ i.e. the intrinsic thermal noise of the MOSFET, $\overline{E^2{}_{n1}}$ is greatly larger than the Substrate noise,

$$F_m = 1 + \frac{2}{\sqrt{5}}\frac{\omega}{\omega_T}\sqrt{\gamma\delta(1-|c|^2)} \quad (4.5)$$

$$F = F_m + \frac{R_n}{G_s}[(G_s - G_{ot})^2 + (B_s - B_{ot})^2] \quad (4.6)$$

Where $R_n = \alpha\omega C_{gs}\sqrt{(\delta/5\gamma)(1-|c|^2)}$ (4.7)

C. In Case of $\overline{E^2{}_{n1}} \sim \overline{E^2{}_{n2}}$

When $\overline{E^2{}_{n1}}$ and $\overline{E^2{}_{n2}}$ are having the equivalent magnitude, the expression of Y_c can further be written as;

$$Y_c = Y_{c1}\left(\frac{4kT\gamma g_{d0}}{4kT\gamma g_{d0} + g^2{}_{mb}\frac{P_{sn}(f)}{(1+\omega^2\tau^2)}}\right) + j\omega C_{gs}\left(\frac{g^2{}_{mb}P_{sn}(f)/(1+\omega^2\tau^2)}{4kT\gamma g_{d0} + g^2{}_{mb}\frac{P_{sn}(f)}{(1+\omega^2\tau^2)}}\right)$$

(4.8)

Now the fundamental noise figure parameters are $R_n, B_{opt}, G_{opt},$ and F_m becomes

$$R_n = \frac{4kT\gamma g_{d0} + g^2{}_{mb}P_{sn}(f)/(1+\omega^2\tau^2)}{4kTg^2{}_m} \quad (4.9)$$

$$B_{opt} = -B_c$$

$$G_{opt} = \sqrt{\frac{\delta\omega^2 C^2{}_{gs}(1-|c|^2)}{5g_{d0}}\frac{4kTg^2{}_m}{4kT\gamma g_{d0} + g^2{}_{mb}\frac{P_{sn}(f)}{(1+\omega^2\tau^2)}}} \quad (4.10)$$

$$F_m = 1 + 2\sqrt{\frac{4kT\gamma g_{d0} + g^2{}_{mb}\frac{P_{sn}(f)}{(1+\omega^2\tau^2)}}{4kTg^2{}_m}\frac{\delta\omega^2 C^2{}_{gs}(1-|c|^2)}{5g_{d0}}} \quad (4.11)$$

Where; $P_{sn}(f)$ is representing the power spectral density of substrate noise and F_m is minimum noise figure.

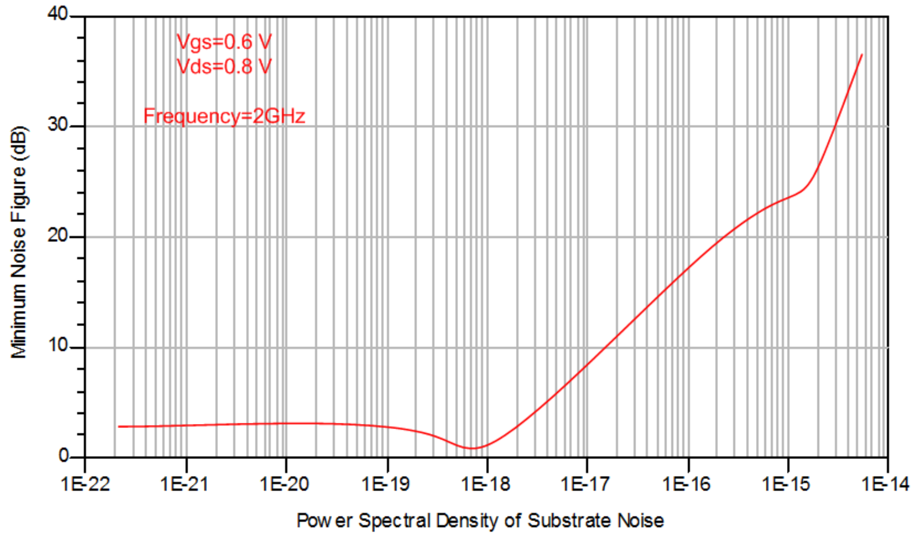


Figure. 4.6: Simulation of minimum noise figure with PSD of substrate noise at fixed V_{gs} and V_{ds}

The simulation for the minimum noise figure is done for the 0.18 µm NMOS transistor at a fixed gate to source voltage 0.6 V and drain to source voltage 0.8 V. The minimum noise figure v/s power spectral density of substrate noise is given in the figure. 4.6 and the minimum noise figure v/s frequency plot is shown in figure. 4.7. The minimum noise figure is decreasing in nature with increasing operating frequency and minimum value is obtained at maximum limit of the operating frequency range.

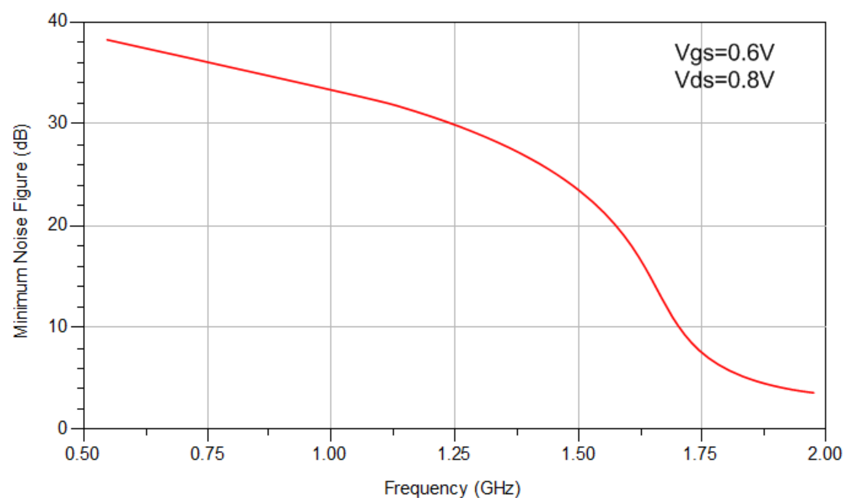


Figure. 4.7: Simulation of minimum noise figure with frequency at fixed V_{gs} and V_{ds}

4.3 GATE LEVEL MACROMODEL

The gate level macromodeling is used for the substrate noise estimation and hence the gate level macromodeling is described in this section and also discussed in [74, 83]. To develop the macromodel for entire system these individual macromodels of the gates are combined together and simulation for the system is done using circuit simulator. For more detail a fundamental digital cell (CMOS inverter) is driven by a same kind of cell and its circuit macromodel are shown in figure. 4.8 (a) and (b). The four important parts of this circuit noise macromodel are; first, the switching current I_S, second, the capacitance of well C_{Wel}, third, the substrate resistance R_{Su} and fourth, capacitance at the output of the cell C_{out}. To form the macromodel for the entire system the individual circuit macromodel are combined and equivalent macromodel is shown in figure. 4.8 (c). The overall values of the elements are given by the eq. (4.12), (4.13) and (4.14).

$$C_{out} = \sum C_{outi} \tag{4.12}$$

$$\frac{1}{R_{Su} + {}^{1}/_{j\omega C_{Wel}}} = \sum \frac{1}{R_{Sui} + {}^{1}/_{j\omega C_{Weli}}} \tag{4.13}$$

$$I_S = \sum I_{Si} \tag{4.14}$$

These equations represent the values after the superposition of individuals and most importantly the switching current of individual cells are added at their exact transition time. Two fundamental assumptions are taken in consideration for the macromodel discussed in this section. The first assumption which is to be taken into account is, the dominant substrate noise is that which is being introduced by the power supply rail and second, all the contacts of the digital part of the SoC which are connected to the ground is treated as a single node. As a result of which the fundamental assumption, $L\,{}^{di}/_{dt}$ is said to be dominant substrate noise generation source available at ground rail.

4.3.1 Parasitic Extraction of Macromodel

A circuit macromodel is said to be a meaningful macromodel only when it provides the relation amongst the elements which are contributed in the generation of substrate noise and active as well as passive elements of the digital part of SoC along with the clear information about those elements which are responsible for the generation of substrate noise.

Also a macromodel should be as simple so that its parameters can easily be extracted. The macromodel parameter extraction methods are given in [121, 122, 123, 124, 125].

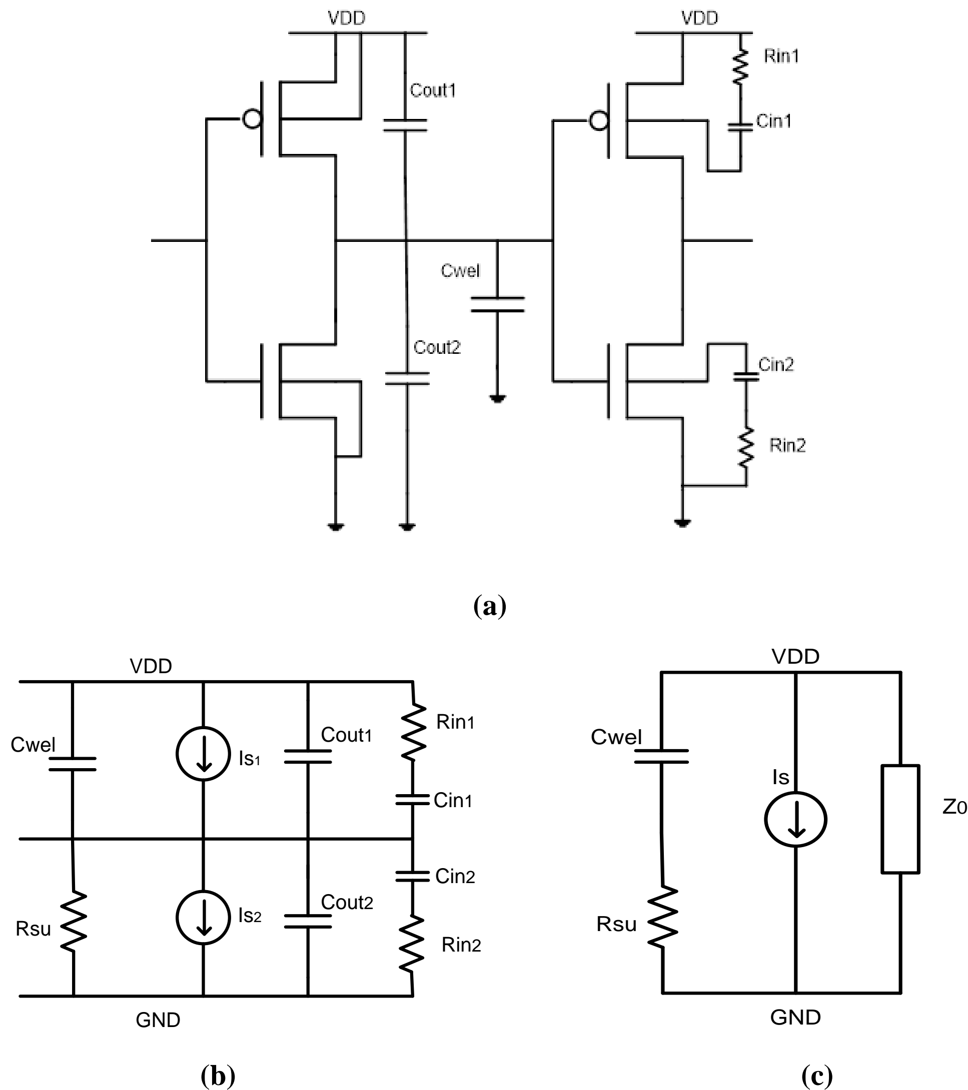


Figure. 4.8: (a) Basic digital gate circuit driven by another gate, (b) noise equivalent macromodel circuit, and (c) simplified macromodel

The physical design of the circuit is able to provide information about the well capacitance C_{wel} and substrate resistance R_{sub}. The output capacitances in figure. 4.8 (b), between diffusion and GND can be analytically obtained from the device geometry. The switching currents I_{s1} and I_{s2} is measured at the Supply nodes. The input resistances and capacitances at input of gate of the circuit ($C_{in1}, C_{in2}, R_{in1} and R_{in2}$) can easily be extracted.

4.3.2 Substrate Noise in CMOS Inverter

The circuit macromodel discussed in the previous section is used in this section to develop the circuit macromodel for a CMOS inverter. The CMOS inerter shown in figure. 4.9 is considered for the validation of the circuit macromodel and it is integrated over a lightly doped substrate on 0.18 µm technology. The combined macromodel for the circuit and substrate is shown in figure. 4.11.

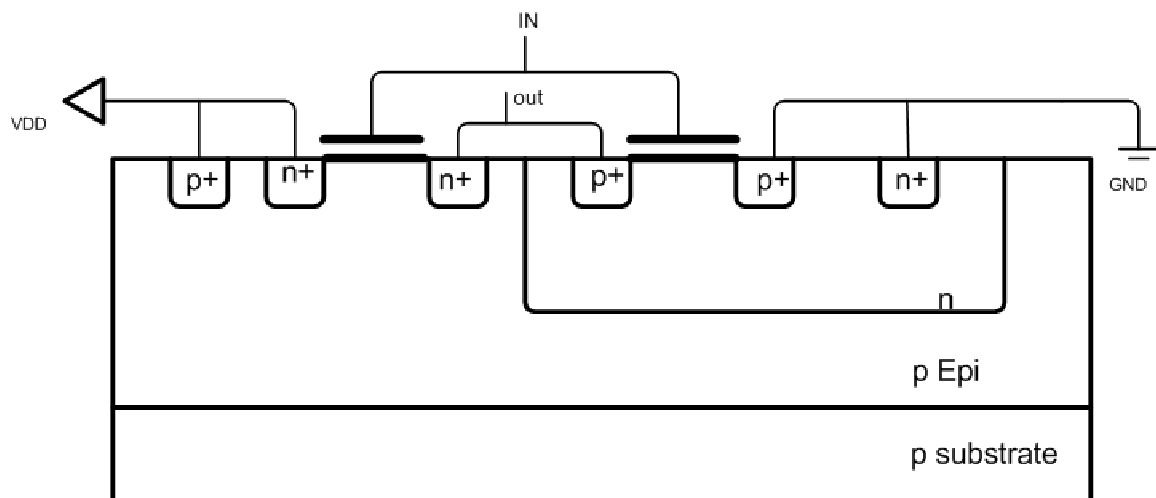


Figure. 4.9: CMOS inverter for macromodel validation

The input waveform is shown in figure. 4.10 (a), which is applied to the input of the CMOS inverter. A SPICE simulator is used to simulate the injected current in substrate at every transition of input for both types either High-to-Low or Low-to-High, is shown in figure. 4.10 (b). The impact ionization and its varying nature are responsible for the generation of

large false current at input transitions and it is positive for most of the cases. The substrate current is also dependent on the integration technology. The higher is the fabrication technology greater is the substrate noise current. The glitches and the switching phenomenon in complex circuits generate the high frequency components. Also the substrate noise generated from the chain of five inverters is shown in figure. 4.12.

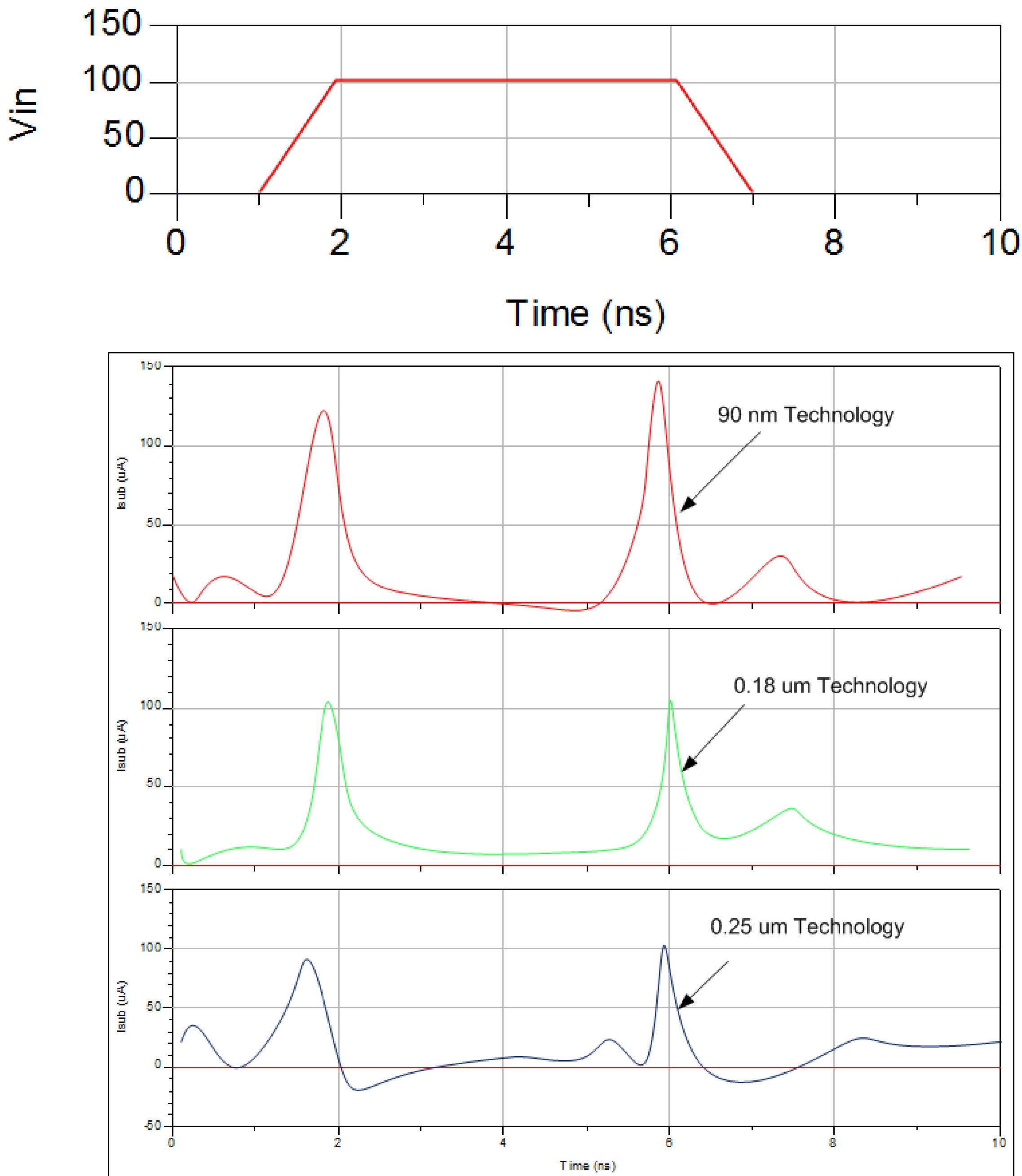


Figure. 4.10: Input waveform and resulting substrate current waveform injected into the substrate on different transitions of input

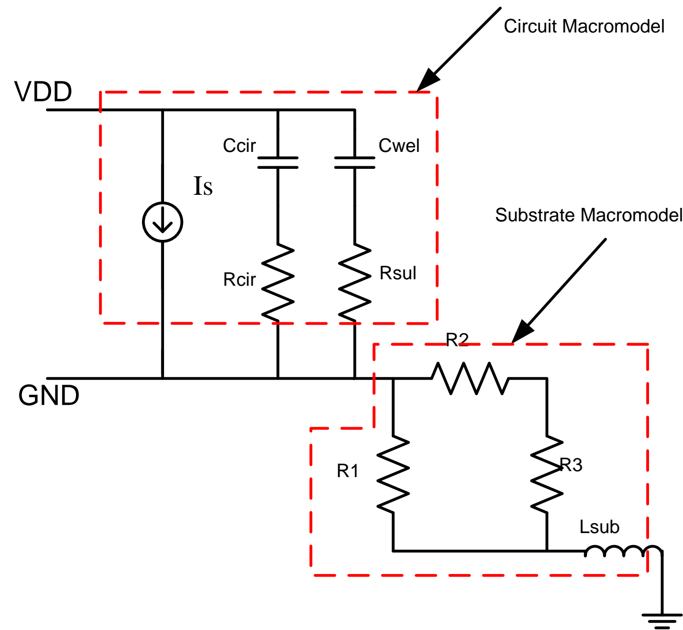


Figure. 4.11: Simplified combined macromodel for the substrate and circuit

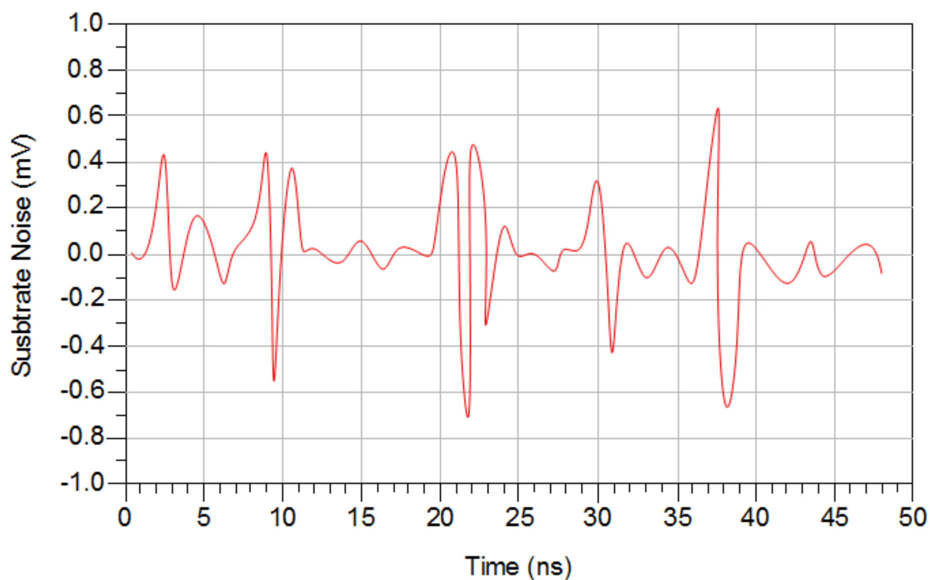


Figure. 4.12. Substrate noise voltage for the chain of five inverters, when ground inductor is of 0.6 nH

4.4 SUBSTRATE NOISE ANALYSIS IN FULL ADDER

In this section, a 16-transistor static 1-bit CMOS full-adder cell is implemented and the same is considered in the analysis of substrate noise. The static and pass transistor principle is used for the implementation of the full adder and is implemented over high resistive

substrate on 0.18 μm technology. Since the inverters are eliminated from the critical path, therefore, the speed of the full adder is higher and the power consumption is lower than the standard 1-bit full-adder cell. Elimination of short circuit power component offers low power consumption. Using the 0.18 μm technology design rules, layout is designed first and then the substrate noise is estimated.

4.4.1 Design Implementation and Simulation

The full adder circuit in figure. 4.13 is taken for the substrate noise analysis. The estimation of the substrate noise for CMOS inverter is done in the previous section. Now a complex digital circuit is taken under consideration and layout for the full adder using 0.18 μm technology is designed as shown in figure. 4.14.

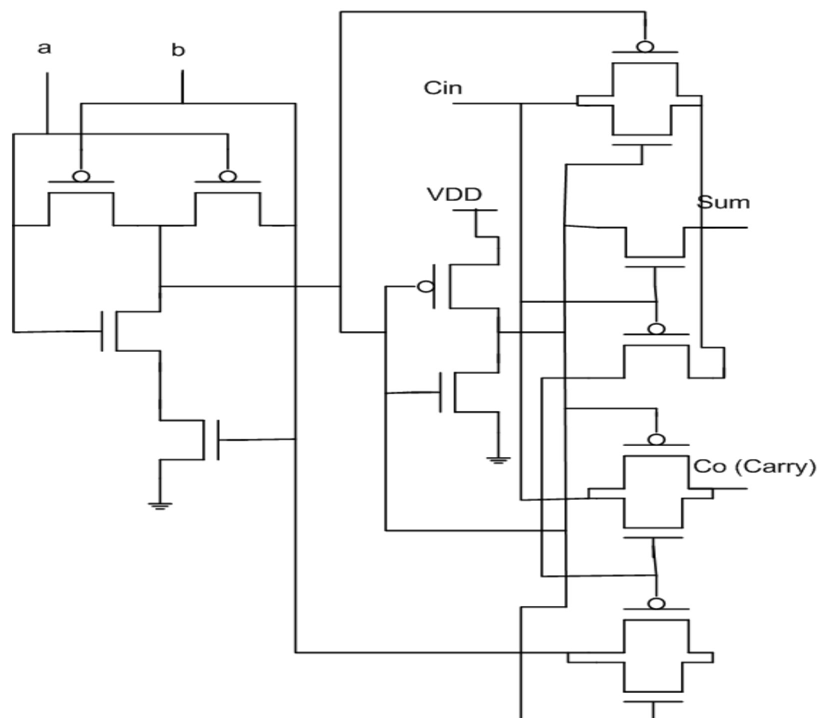


Figure. 4.13: The schematic of one bit full adder cell which is used in analysis

The highly resistive substrate is used here, so it cannot be considered as a single node because its complex mesh with lots of internal nodes. It still need a control contact on the substrate and after minute modification in the layout it is added in the middle of the cell view as shown in figure 4.15.

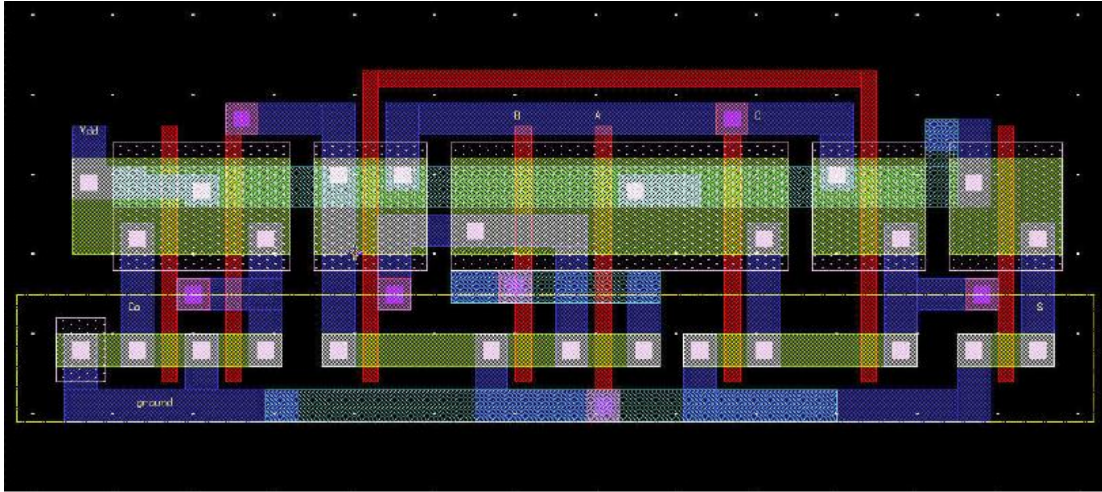


Figure. 4.14: Layout of one bit full adder (0.18 μm technology)

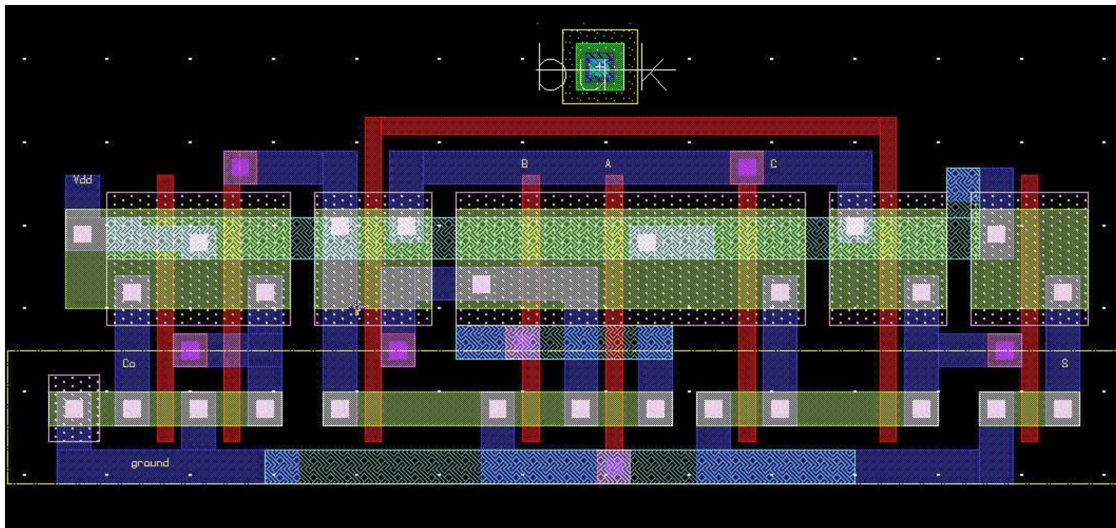


Figure. 4.15: A bulk contact is added to the layout in order to have a controlled substrate node

The layout of the full adder circuit is developed in Cadence EDA tool following the 0.18 μm CMOS technology design rules. The discussed full adder design is simulated and substrate noise current and voltage are observed for all the input combinations.

The analog as well as digital simulations for full adder is done and output bits are checked in all cases of inputs. The analog simulation results are verified and found that the full voltage swing is of the order of 2.5V for both the outputs.

The analog simulation is performed with a capacitive load of 0.03 pF at both the outputs of full adder. The simulation result shows a **0.2ns** propagation delay for carry output and **0.38ns** propagation delay for sun output. The average propagation is observed to be 0.23 ns**.** The analog simulation report is given in table 4.2.

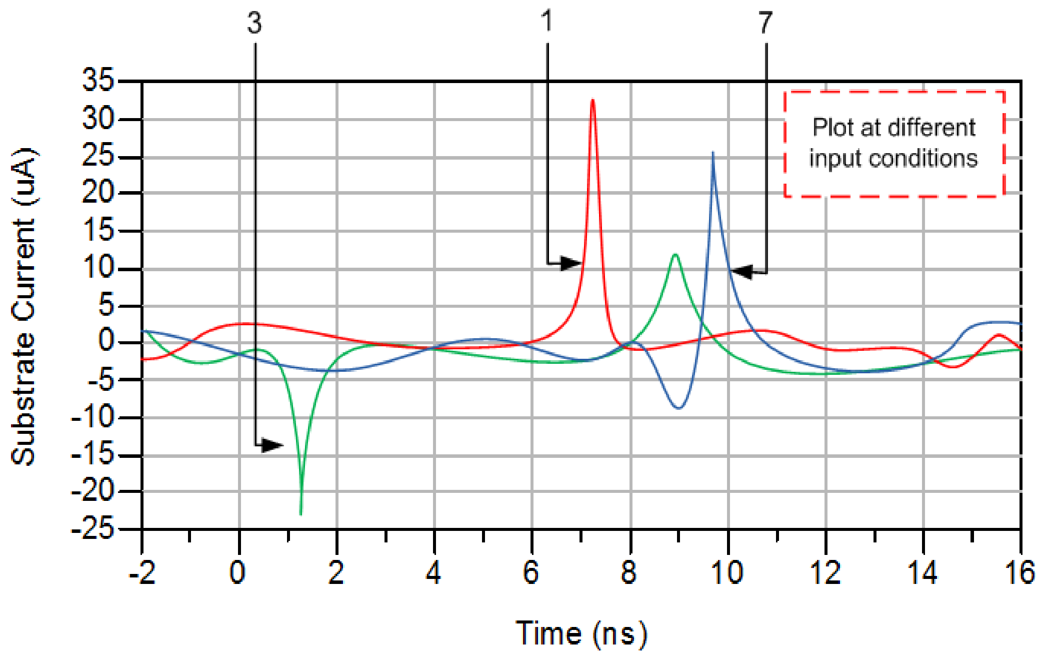


Figure. 4.16: Noise current waveform without power supply noise coupling for the full adder at different input conditions

Table 4.2: Performance of one bit full adder at different input combinations

A	B	C	Co		S	
Logic	**Logic**	**Logic**	**Logic**	**tp (ns)**	**Logic**	**tp(ns)**
0	0	0	0	-	0	-
0	0	1	0	-	1	0.20
0	1	0	0	-	1	0.38
0	1	1	1	0.20	0	-
1	0	0	0	-	1	0.38
1	0	1	1	0.18	0	-
1	1	0	1	0.20	0	-
1	1	1	1	0.16	1	0.16

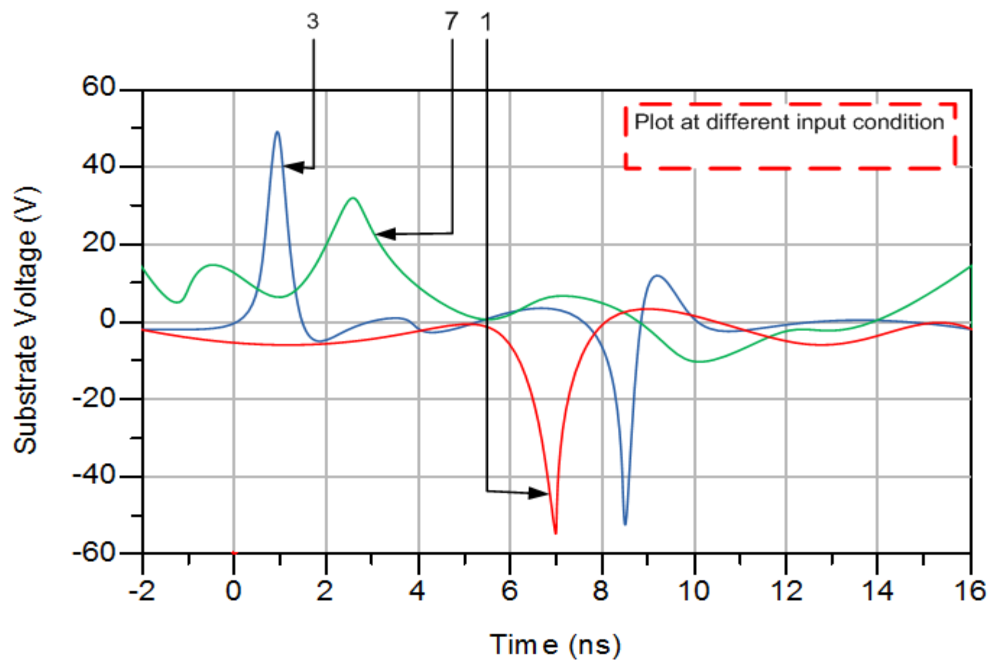


Figure. 4.17: Substrate noise voltage without power supply noise coupling for full adder circuit at different input conditions

If the two contacts are separated by a distance there is a possibility of path for current as well as for voltage to propagate. These voltages and currents are not associated with circuit performance rather they are actually related to the internal mechanism in the substrate like impact ionization. These current and voltage is now estimated at the substrate contact and is shown in figure 4.16 and figure 4.17. The current at the substrate contact is plotted with time at the different possible combination of the input to the full adder in figure 4.16. The maximum value is 30uA, at the input 1 and 5. The substrate voltage is plotted with time in figure 4.17, at the different possible combination of the inputs. The maximum value is 45mV at input combination 3.

4.5 SUBSTRATE COUPLING ANALYSIS IN LOW NOISE AMPLIFIER (LNA)

The research focus on the ultra-wideband radio receiver is growing and the very first signal processing block of the radio receiver is Low Noise Amplifier (LNA). The main purpose of the LNA is to amplify the received signal to the acceptable level with minimum self-generated noise. An inductively source degenerated low noise amplifier [43], its design and

analysis for the ultra-wideband application is discussed in this section. The linearization and the current MOSFET model is used for analytical calculation of noise figure for the LNA. The gain, noise figure, nonlinearity and impedance matching are the most important parameters of the LNA design. The large signal must be accommodated by the low noise amplifier without distortion and present a specific impedance of 50Ω to the input source. The inductively source degeneration is having an advantage that inductor can potentially ease the difficulty in LNA design. The inductor based LNA are having a good performance in terms of noise figure and power consumption, but the use of inductor consumed more area on the chip. The schematic of inductively source degenerated low noise amplifier is given in figure 4.18 (a) and the small signal equivalent circuit is shown in figure 4.18 (b). The impedance and the noise figure are the most important parameters among the four parameters of the LNA. The noise figure for LNA can analytically be calculated in the same way as discussed in section 4.2.1. The body bias effect and the gate-substrate capacitance are generally neglected and it is assumed that the transistor operates in the strong inversion for the analysis of the LNA. Considering these assumption analysis led to better results. When the transistor is operating in weak inversion the gate-substrate capacitance $(C_{gb})$and body bias effect must be considered.

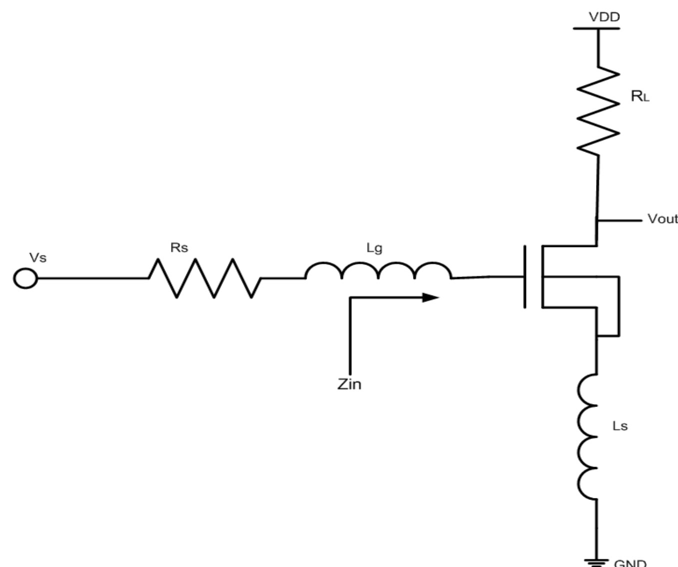


Figure. 4.18: (a) Inductively source degenerated Low Noise Amplifier

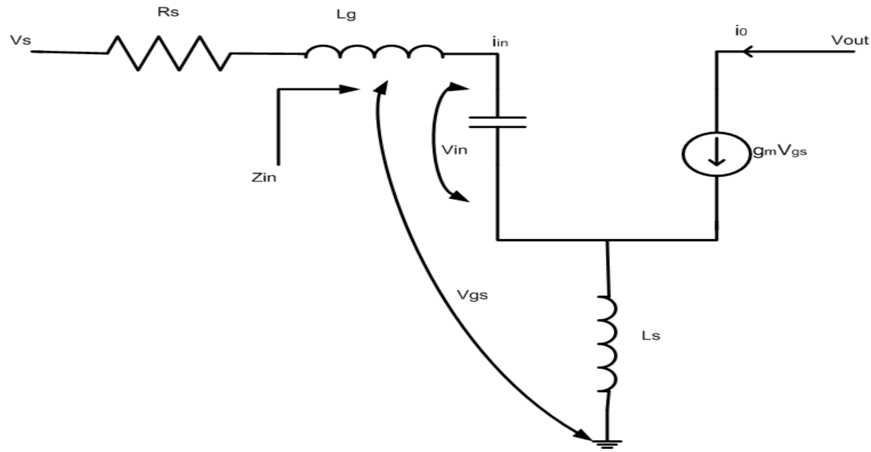


Figure. 4.18: (b) small signal equivalent inductively source degenerated LNA and

The proper choice of L_g and L_s can set the matching condition, and L_g is used to set he resonance frequency. For the narrow band application L_g and L_s can be approximated as;

$$L_s = \frac{R_s}{\omega_T} \cdot \frac{(C_{gs}+C_{gb})}{C_{gs}} \tag{4.15}$$

$$L_g = \frac{1}{\omega_0^2 (C_{gs}+C_{gb})} \tag{4.16}$$

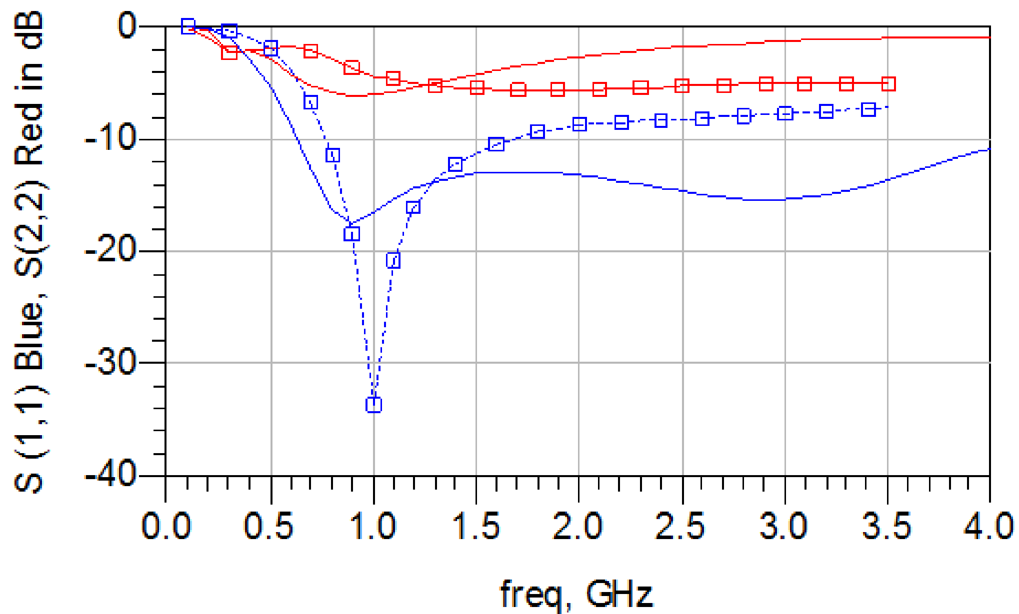


Figure. 4.19: Comparison of Simulated S (1, 1) and S (2, 2) in for the presented LNA at different frequency of operation (solid lines for the ideal component and squares from Layout)

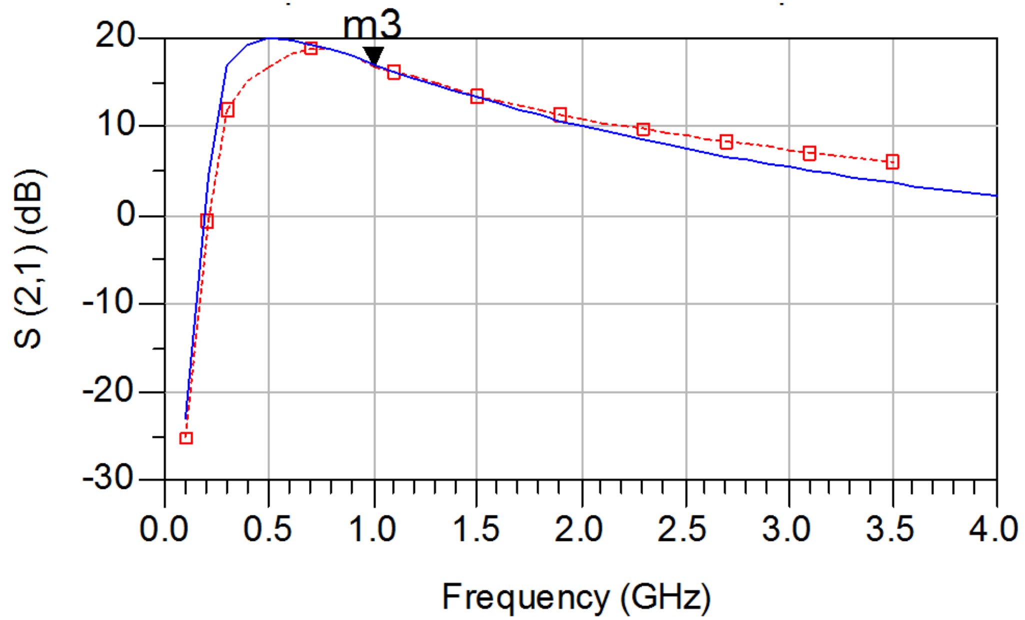


Figure. 4.20: Simulated isolation S (1, 2) in red for the presented LNA at different frequency of operation (solid lines for the ideal component and squares from Layout)

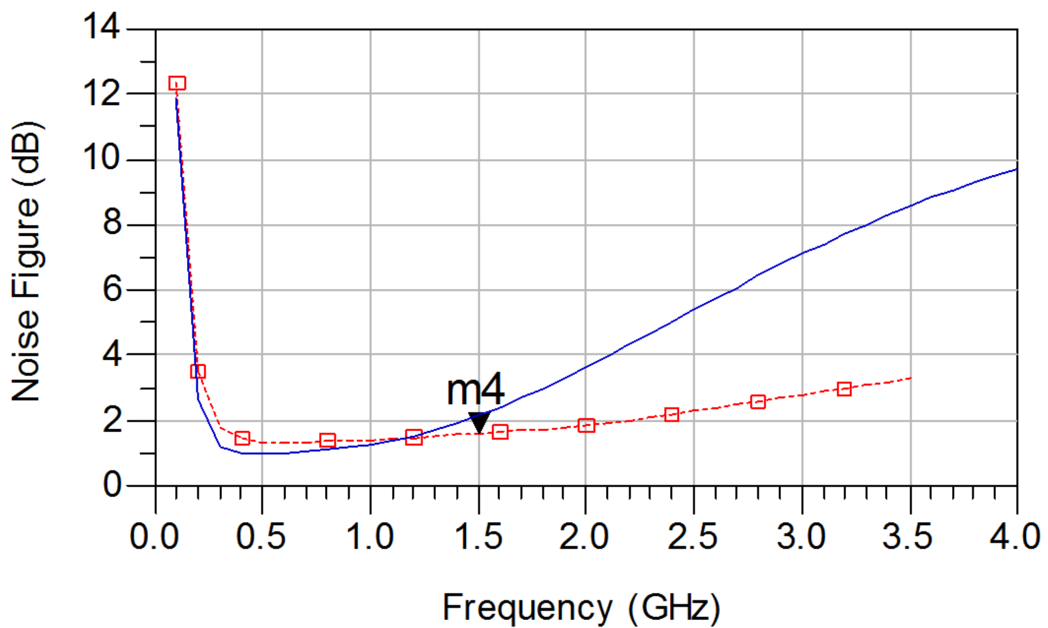


Figure. 4.21: Simulated minimum noise figure for the Low Noise Amplifier at different frequency of operation (ideal for solid lines and square for the layout)

The simulated S (1, 1) and S (2, 2) and the comparison with layout results is done, which is shown in the figure 4.19, the resonance frequency for the designed LNA is observed to be 1GHz. The parameter S (2, 1) is depicted in the figure 4.20 and the marker m3 showing that at 1GHz the isolation is 15dB. Figure 4.21 shows the simulated noise figure and at

resonance frequency the minimum noise figure is 1.5 dB and it can be verified from the figure 4.22, the marker m1 is at 1 GHz. It is also noted from figure 4.22, that some of the noise circles will be disappearing when the frequency will be increased this is because of the minimum noise figure will increase with increasing frequency and there cannot be circles corresponding the noise figure below the minimum noise figure.

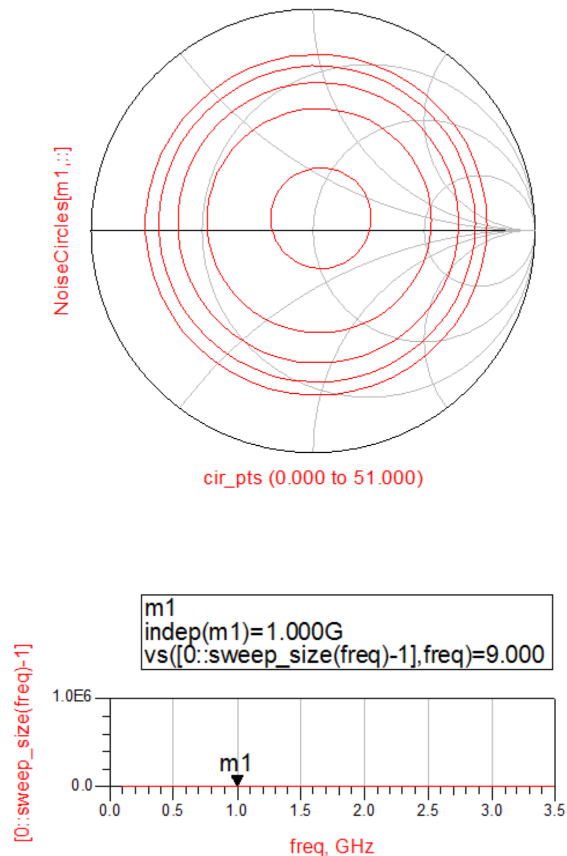


Figure. 4.22: Simulated noise figure in Smith chart at resonance frequency 1 GHz

The Low noise amplifier is designed for the narrow band application (0.5 to 3.5) GHz and the results are also validated by comparing with the results obtained from layout design. The values of the source inductor and the gate inductor to obtain matching condition are given and in that particular condition the resonance frequency is defined. The results clearly depict that the resonance frequency is 1GHz and the minimum noise figure is 1.5dB for the designed LNA.

4.6 SUBSTRATE NOISE SPECTRUM OF RF CMOS

The propagation of the substrate noise from the digital section of the SoC to the analog and RF section is a problem to be considered. Mainly this noise is due to the high speed switching of blocks and signal propagation through common substrate. A pulse shaped waveform produces across the supply rail due to the switching activity. When the number of the gates increases the amplitude of this waveform becomes greater and when the speed increases the waveform become sharper. This means if the digital circuit will be faster and complex, the result will be a larger noise in the parasitic inductances of the supply rail of the integrated circuit. The RF CMOS for the System-on-Chip application is analyzed and substrate noise is estimated using a simple analytical model. The analysis includes substrate noise due to digital circuit of the System-on-Chip excluding the packaging and board parasitic inductances. To extend the capability of the standard CMOS, in terms of integration of high performance radio frequency passive component substrate of high resistivity is used.

Substrate noise spectrum, mainly consists of two parts; first is a Dirac delta, which is due to the periodic mean of current and noise signal, and the second is cycle to cycle fluctuation of the current noise signal [129]. In this work a noble methodology is proposed to estimate substrate noise spectrum; where board and packaging parasitic inductances are not considered, i.e. the analysis is done only by taking the digital section and substrate parasitics in the account. The flowchart of the methodology is given in figure 4.23. Using the statistical analysis the current waveform of the digital section is obtained at the source, and by using the simple lumped model the coupling mechanism in source and substrate is derived and finally the analytical transfer function is obtained. To fulfill the performance requirements for radio frequency application CMOS is a well suited technology. Here, the

high resistive (lightly doped) substrate is used, since the low resistive (heavily doped) substrate limits the integration of high quality passive elements. For the better removal of substrate noise and to increase the quality factor of the passive components, the high resistive substrate is used. It's a challenge to keep the characteristics of the CMOS same to make reusable of lower design cost digital library.

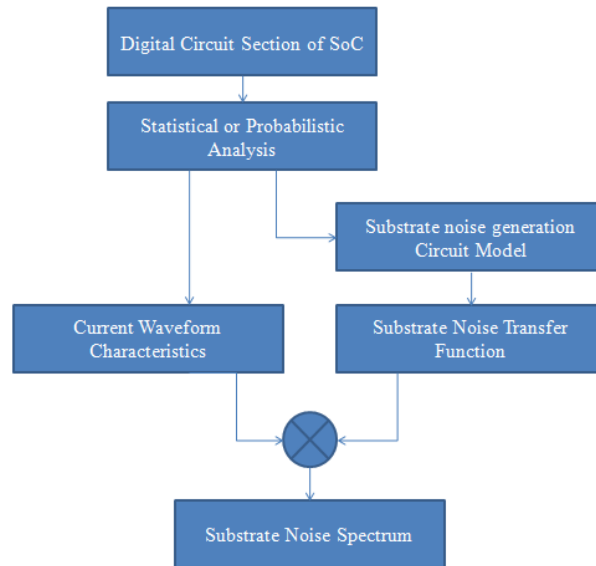


Figure. 4.23: Flow diagram of the proposed methodology to estimate the substrate noise

The flow diagram of the proposed methodology suggests that the input noise current signal from the digital section and is applied to the probabilistic analysis block where the statistical characteristics of the noise signal is obtained. The output of this block is applied to current wave form characteristics and substrate noise generation block. Simultaneously, after this the transfer function is evaluated and finally the substrate noise spectrum is found. In some cases, the board and package parasitics are also considered for the same.

4.6.1 Simulation of Substrate Noise Spectrum

The two port noise isolation structure is shown in figure 4.24, the port 1 is source port and the port 2 is the sensor port. Simulation is done by injecting an AC signal through port 1

and the transmitted signal is obtained by EM simulator. The parameter S (2, 1) is simulated for the given test structure at different frequencies. The macromodel shown in figure 4.11 is being used here for the SPICE simulation. The parasitics shown in the figure 4.11 are the responsible for the coupling between port 1 and port 2; and coupling between the substrate to the ground. Substrate resistance and substrate capacitance are dependents on the thickness of the substrate, thinner will be the substrate better will be isolation.

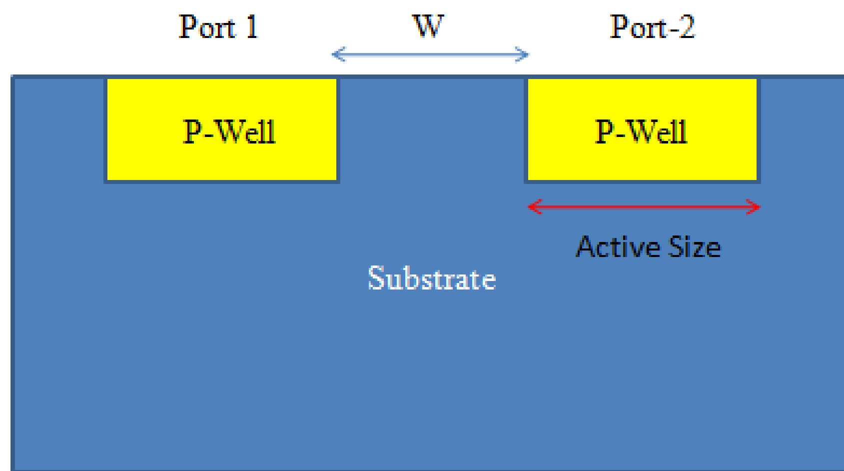


Figure. 4.24: Structure for the EM simulation of RF CMOS

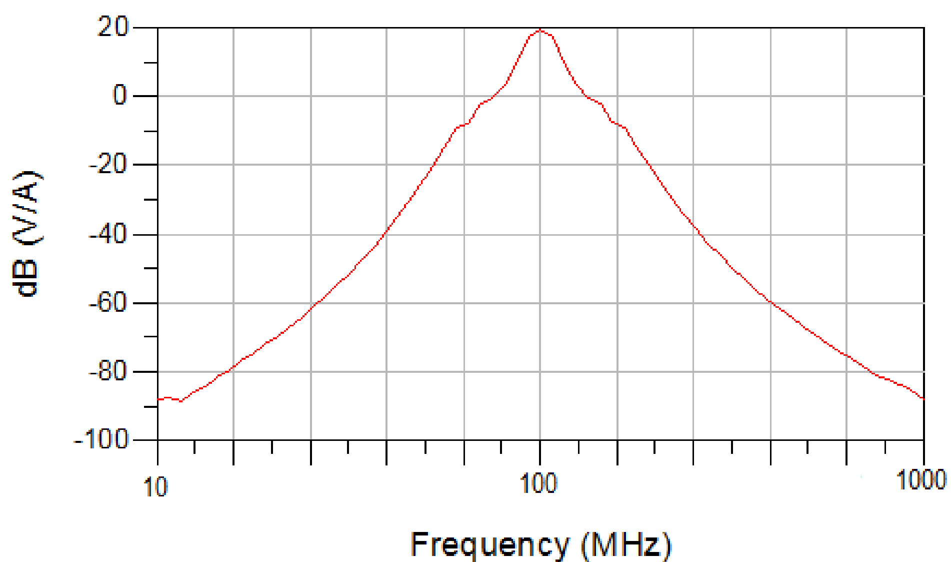
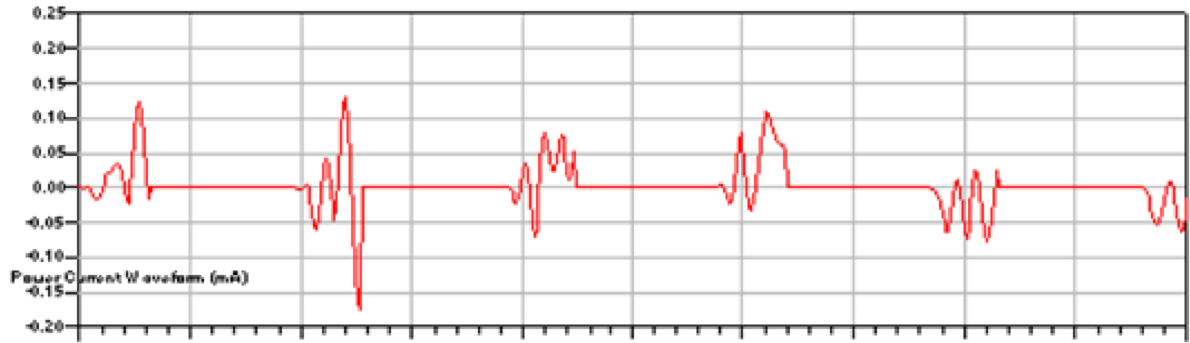
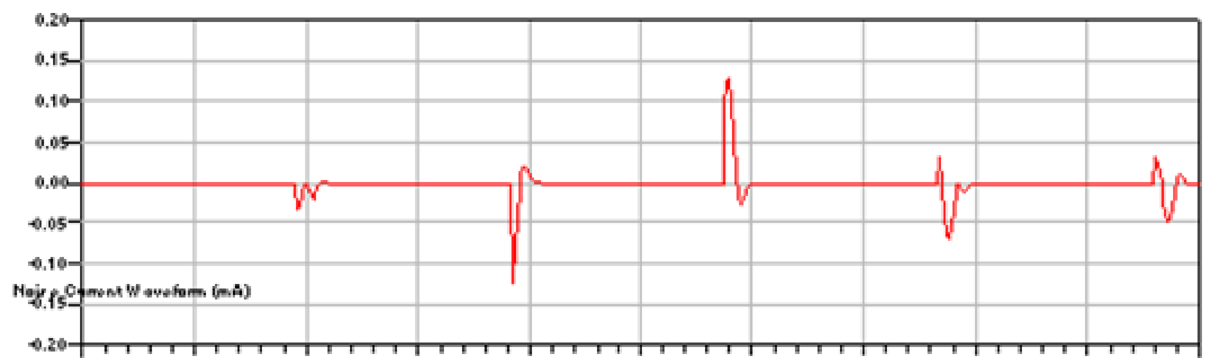


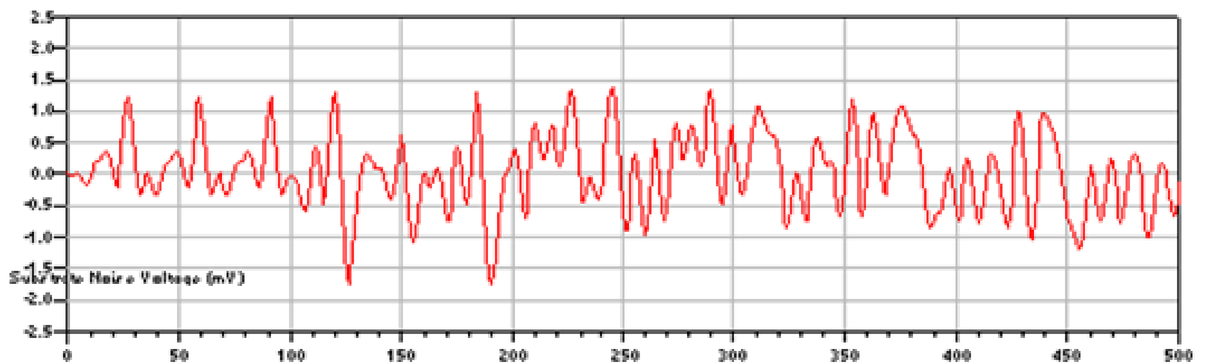
Figure. 4.25: Transfer function of the substrate noise for simplified mesh



(a)



(b)



(c)

Figure. 4.26: Simulated waveform of (a) power supply current, (b) noise current and (c) substrate noise potential for RF CMOS.

The simulation is done for the RF CMOS, the simulated waveform of power supply current, noise current and substrate noise potential at different time of simulation is given in the figure 4.26 (a), (b) and (c).

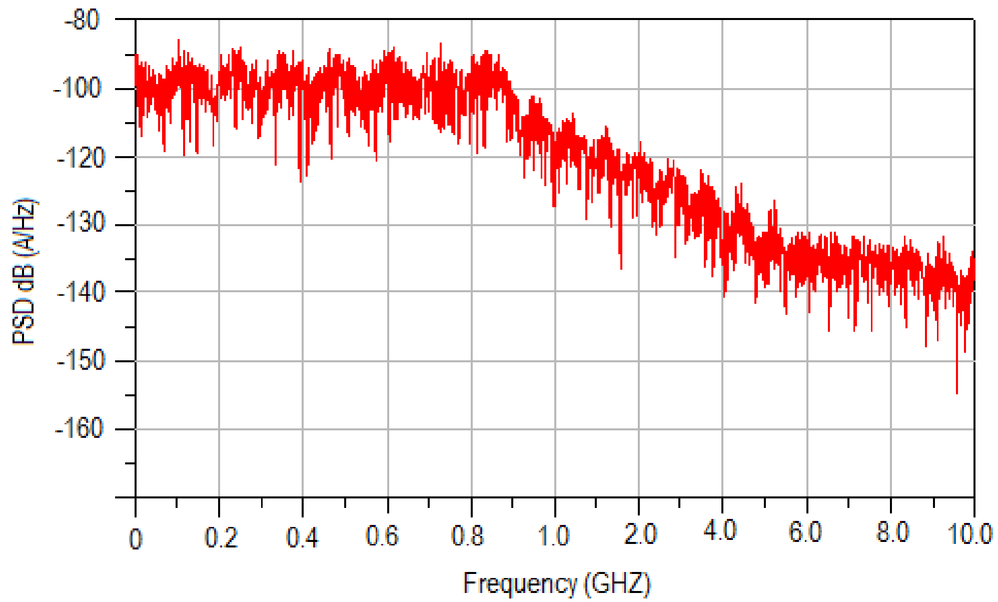


Figure. 4.27: Simulated continuous term power spectral density of substrate current

It is visualized from the figure 5.26 that, the potential at the substrate contact is varying from 1.5 mV to -1.5 mV and the power supply current waveform varies from the 0.12 mA to -0.17 mA.

The PSD of the substrate current using the proposed methodology for RF CMOS is obtained and its plot is shown in figure 4.27.

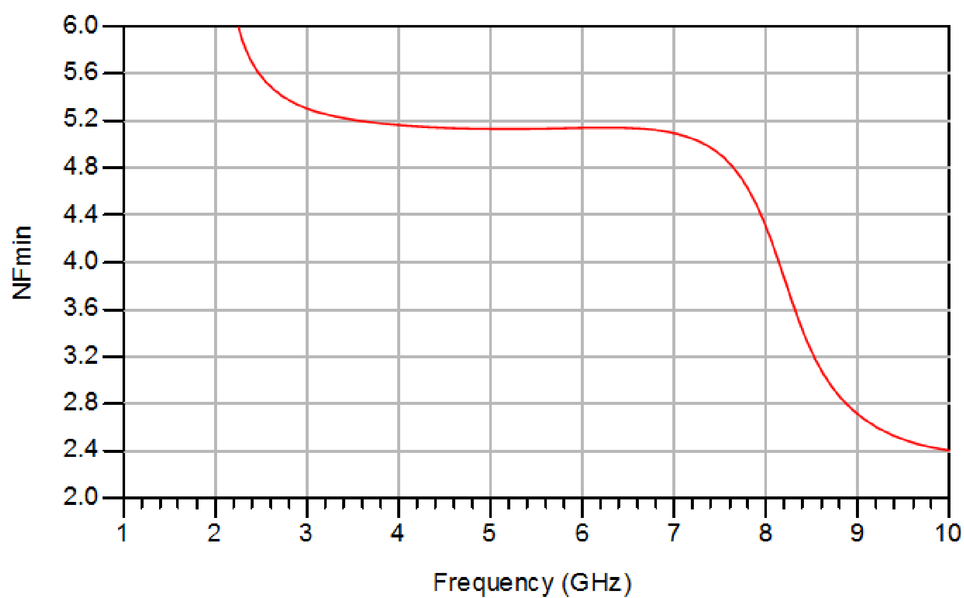


Figure. 4.28: Simulated minimum noise figure at different frequency of operation

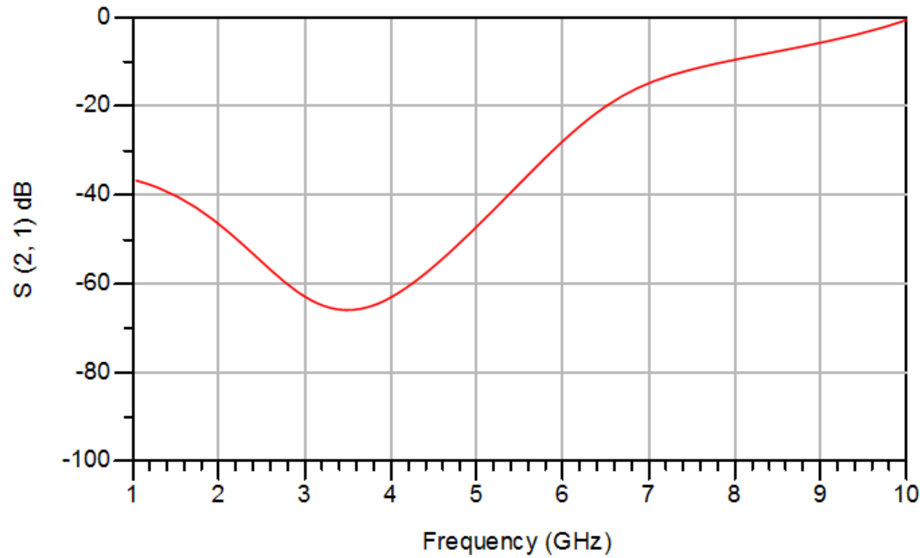


Figure. 4.29: Simulation of isolation (S (2, 1) Parameter) between port1 and port 2

There may be slight variation from the exact because the package and board parasitics are not taken into the account. The substrate noise transfer function is shown in figure 4.25. The minimum noise figure can analytically be estimated as in section 4.2.1. The minimum noise figure for different frequency of operation is given in figure 4.28, and it is observed that the noise figure decreases with increasing frequency. Now, to analyze the coupling between the contacts (between $port_1$ and $port_2$) of structure considered in figure 4.26, the s-parameter is obtained. The simulation is done for S (2, 1) and result is shown in figure 4.29; result clearly depicts that isolation between the source and sensor contacts gets poorer when frequency of operation increases.

4.7 ANALYSIS OF SUBSTRATE COUPLING IN HIGH PERFORMACE SOC

In the previous chapter, it has already been discussed that the accurate substrate model plays important role in the analysis of substrate noise coupling. Since, the capacitive effect becomes significant at a higher frequency of operation and the impedance of the high resistive substrate becomes frequency dependent. Therefore, the capacitive effect is needed to be considered for high resistive substrate at high frequency. To overcome this snag of

high resistive substrate, the analysis is done for a low resistive substrate and substrate network is assumed to possess purely resistive nature. A CMOS inverter and a saturated load n-MOS inverting amplifier are integrated on the common substrate of purely resistive nature to demonstrate substrate noise coupling in a mixed signal system. The system is designed on 0.18 μm CMOS technology and is depicted in figure 4.30. Since, the behavior of low resistive substrate changes at different frequency of operation, therefore, a frequency of interest is the need to model the substrate and simulate the system.

It has already discussed that, the behavior of substrate is purely resistive up to 15 GHz and substrate can be modeled as a pure resistive network with multiple ports. If the frequency of operation increases, the capacitive effect on substrate arises and the impedance of the substrate become dependent on the frequency because of the varying conductivities of different doping layers.

4.7.1 Description of Systems and its Simulation

A CMOS inverter and a saturated load n-MOS inverter are integrated on a common substrate to demonstrate a practical mixed signal system-on-chip. Out of these two, CMOS inverter is considered as digital part and saturated load n-MOS inverter is considered as the analog part of SoC. These two circuits are assumed as two different contacts integrated at certain separation on a common purely resistive substrate.

The CMOS inverter and the saturated n-MOS inverter are separated by a fixed distance and the resistive macromodel for the represented system is derived. First, a two port impedance matrix is constructed to construct an n-port impedance matrix for the system and then the values of resistances are obtained. The mixed signal circuit setup for simulation is represented in figure 4.30 and the resulting resistive substrate network with values of resistances is shown in figure 4.31.

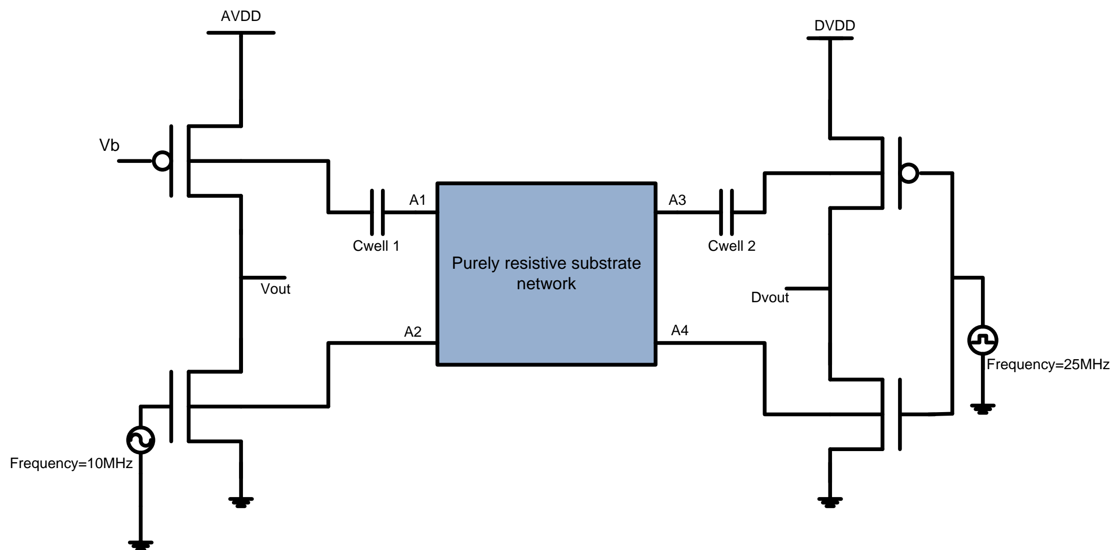


Figure. 4.30: Representation of mixed signal SoC for substrate noise coupling analysis

The n-well–capacitances C_{well1} and C_{well2} represented in figure 4.30, are not considered in circuit simulation. The resistances of the substrate network shown in figure 4.31 and the resistors R_{12}, R_{13}, R_{14}, R_{23}, R_{24} and R_{34} are the resistances amongst the contacts, while resistances R_{11}, R_{22}, R_{33} and R_{44} represent the resistances amongst the contacts and the back-plane.

The layout design rules and the size of transistor is used for the calculation of the values of resistances, moreover, the separation between the contacts is also significant for the calculation of values of resistances. Since, noise coupling through the substrate has been only the matter of concern, therefore, inductances associated with supply lines are not considered in the simulation.

A digital pulse signal of 25 MHz frequency is applied as input to the CMOS inverter and an analog sinusoidal signal of 10 MHz frequency is applied as input to the saturated load NMOS inverter, for the analysis of substrate noise coupling between the circuits shown in figure 4.30.

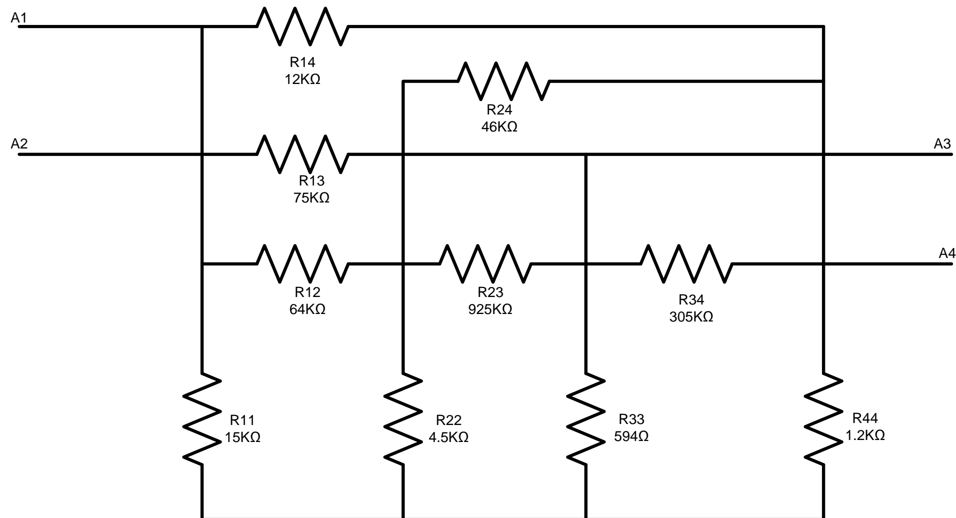


Figure. 4.31: Resistance network of substrate for the mixed signal system

To eliminate the harmonics associated with analog sinusoidal signal those lies in spectrum of digital signal, the frequency of the analog signal is chosen lesser than that of the digital signal. The substrate noise is obtained by the time domain simulation of the system, and substrate noise waveform at the output of the saturated load inverting amplifier is shown in figure 4.32.

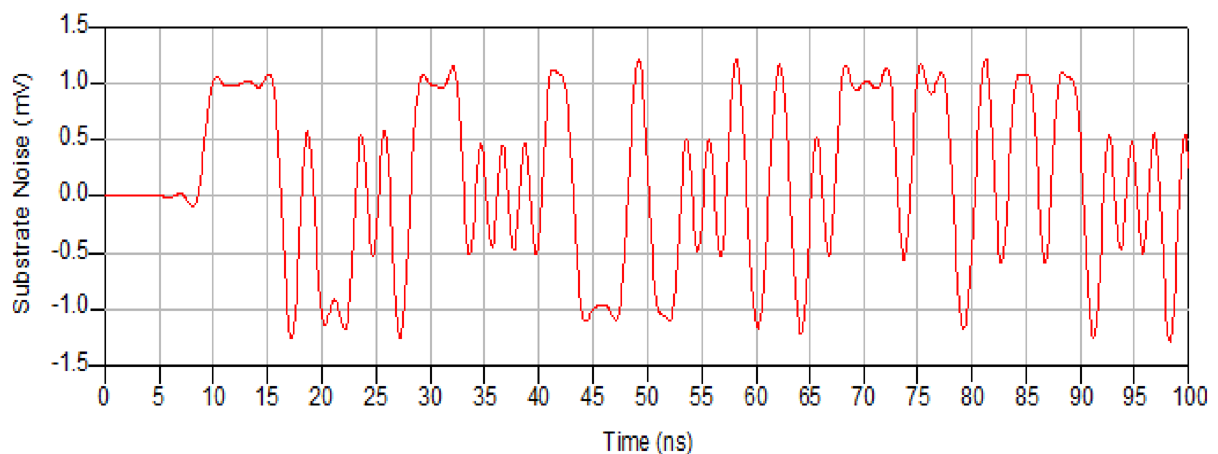


Figure. 4.32: Waveform of substrate noise obtained from the time domain simulation

When the analog input of 10 MHz is applied to the saturated load n-MOS inverter and CMOS inverter is not triggered with any input, then no coupling is observed between the circuits and a peak at 10 MHz appears in output power spectral density. The peak in the

output spectrum at 10 MHz is due to the input signal and some harmonics resulting from the amplifier design, which is shown in figure 4.33. If there is no input signal at CMOS inverter, the coupling between he circuits is not seen, though, the separation between the circuits is of the order of 10 µm.

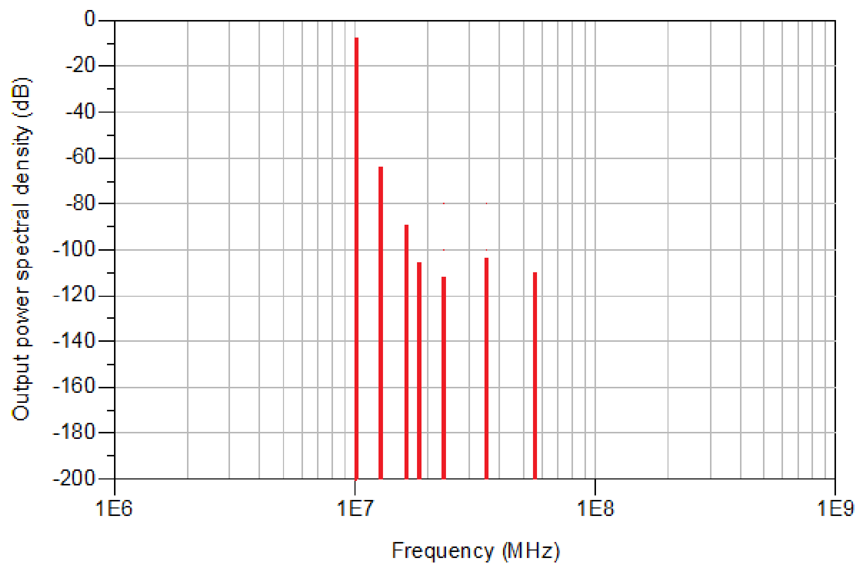


Figure. 4.33: Power spectral density at the output of the amplifier when analog input of 10 MHZ frequency is applied at saturated load n-MOS inverter

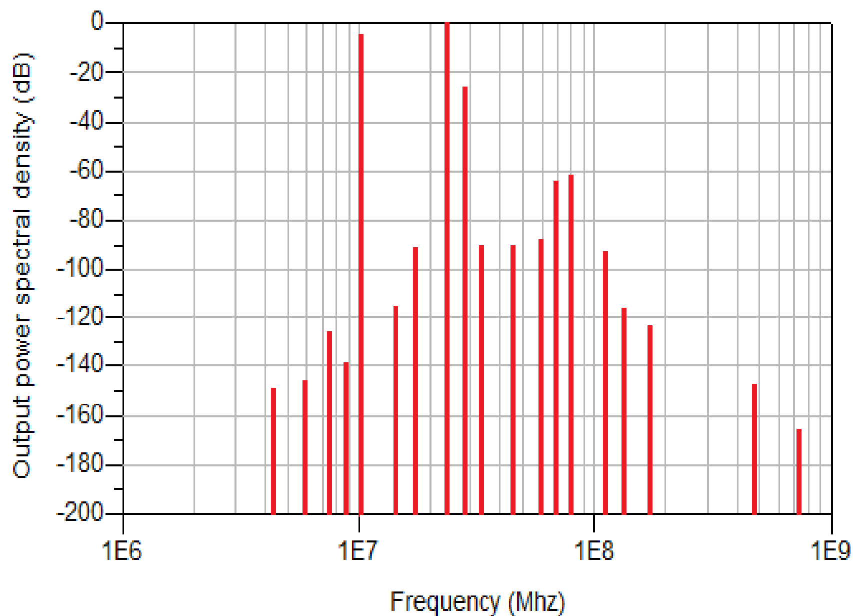


Figure. 4.34: Power spectral density at the output of the amplifier when analog input of 10 MHZ frequency and digital input of 25 MHz frequency is applied at saturated load n-MOS inverter and CMOS inverter respectively

Again, the separation between the CMOS inverter and saturated load n-MOS inverter is of the order of 15μm, and a square pulse of 25 MHz frequency is applied to CMOS inverter. In such a case, one peak at 10 MHz and another peak at 25 MHz with associated harmonics are appeared in the output power spectral density at the output of the amplifier, which is shown in the figure 4.34.

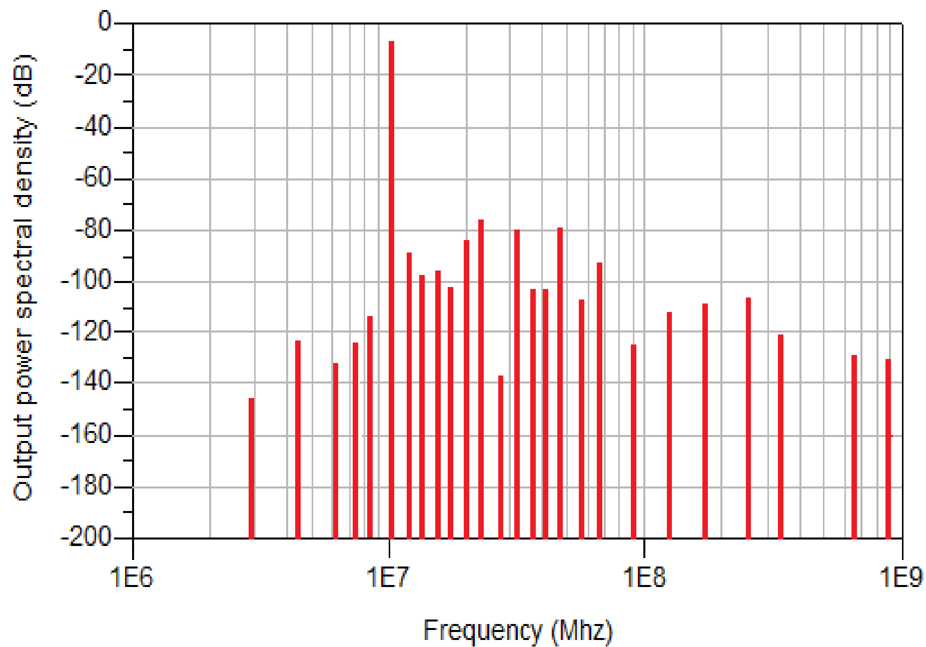


Figure. 4.35: Power spectral density at the output of the amplifier when analog input of the 10 MHZ frequency and digital input of 25 MHz frequency is applied at saturated load n-MOS inverter and CMOS inverter respectively and separation between them is 90 μm

This is the clear indication of the substrate noise coupling between the circuits and the amplifier output is dominated by the substrate noise coupling for a small separation of 15μm to 20μm. The substrate noise coupling between the circuits appears only if, the separation between the circuits is of the order of 15μm to 20μm and input is applied to both the circuits.

In the same system, the separation between the circuits is now increased up to the 90 μm and the system is simulated. A significant attenuation at 25 MHz is observed in output

power spectral density. It depicts that, when the separation between the circuits increases, the isolation between the circuits increases. The output power spectral density of the system is shown in figure 4.35. The analysis of substrate noise coupling in low resistive substrate is done using the simulation up to the 15 GHz frequency using the substrate resistive macromodel. The impact of the substrate noise coupling on analog circuits is demonstrated at different separations between the circuits. The small separation between the circuits allows the substrate noise coupling to dominate the performance of analog circuit. While, at large separation the substrate noise coupling becomes insignificant and the substrate noise coupling will no longer dominate the performance of analog circuit.

CHAPTER 5

STATISTICAL ANALYSIS OF SUBSTRATE NOISE

5.1 INTRODUCTION

The nature of substrate noise is other than Gaussian nature, i.e. it is non-Gaussian in nature. Since on the time domain its characteristics at any time slot get repeated itself over the entire time scale. The substrate noise is now said to be a non-Gaussian and cyclostationary noise process. Since, all the existing approaches relating to the probability density function (PDF) estimation of non-Gaussian noise are now applicable to non-Gaussian stationary noise sequences only. The non-Gaussian PDF is defined by some parameters and are assumed to be fixed for the case. These methods cannot be used to estimate the probability density function of non-Gaussian cyclostationary noise process. The approach discussed in [166] is taken as a non-Gaussian and non-stationary process for PDF estimation and a general algorithm is also presented in the same. In this method, the non-Gaussian mixtures are defined using the Gaussian mixture densities. The algorithm discussed in [166] is used the Gaussian mixtures to define the non-Gaussian sequences, maximized the log likelihood function [167] and priori as well as post-priori updates are applied for estimation of PDF parameters of non-Gaussian nonstationary noise. This algorithm is useful for those cases where the distribution may be a kind of Gaussian or non-Gaussian, may be a kind of stationary or nonstationary and may be a kind of unimodal or multimodal. The algorithm also has the capacity to estimate PDF of non-Gaussian nonstationary noise with zero or non-zero mean. The estimation of probability density function of substrate noise which is a kind of non-Gaussian cyclostationary noise is discussed in this work. The algorithm discussed in [166] is used for the estimation of PDF of non-Gaussian noise, but, the non-Gaussian samples with non-zero mean are modeled by the non-Gaussian mixture density.

The estimation of parameters of non-Gaussian sample are done by priori and post-priori updates over time. The maximum log likelihood function is used to estimate the post-priori parameters of non-Gaussian cyclostationary noise as in [167, 168, 169]. The substrate noise is taken as an example to estimate the PDF using the algorithm referred above. Since, the Cauchy's distribution function is able to characterize the noise generated in electronic circuits and photo diodes. Therefore, the substrate noise is modeled by the Cauchy's distribution function in this work. The application of Cauchy's distribution function and some other distribution function are given the table 5.1.

Table 5.1: Applications of Some Distribution Functions

S. No.	Distribution Function	Application
1	Gaussian Distribution	Characterization of electronic circuit noise and sensor noise
2	Rayleigh Distribution	Characterization of noise phenomena in range imaging
3	Cauchy's Distribution	Characterization of noise phenomena in electronic circuit and photo devices
4	Exponential and Gamma Distribution	Used in LASER imaging
5	Uniform Distribution	Used in basis for numerous random number generators

5.2 PROBABILITY DENSITY FUNCTION OF NON-GAUSSIAN CYCLOSTATIONARY NOISE

Consider a Non-Gaussian cyclostationary sequence $f(x_t)$, denotes the PDF of x_t which is characterized by Cauchy's mixture density of size m. The estimation of noise parameter at each time instant is done by using the maximum log likelihood function.

Let $f(x_t)$, the pdf of $x_t$at time t, is being given by a Cauchy's mixture density of size *m* as;

$$f(x_t) = \sum_{i=0}^{m} p_i\,(t) f_i(x_t)$$

Where $f_i(x_t)$ is Cauchy's distribution function and given by;

$$f_i(x_t) = \frac{\alpha_{i/\pi}}{(x_t - \mu_i)^2 + \alpha_i^2}$$

$$(x_t) = \sum_{i=0}^{m} p_i\,(t) \frac{\alpha_i(t)}{[\{x_t - \mu_i(t)\}^2 - \alpha_i^2(t)]} \tag{5.1}$$

Where; $\mu_i(t)$represents the mean and $\alpha_i(t)$ represents the spreading nature of the Cauchy's distribution function.

Where; $f_i(x_t)$is representing the PDF of$x_t$fori^{th}Cauchy's density. $\mu_i(t)$ =$[\mu_1(t), \mu_2(t), \dots \dots . \mu_m(t)]$ and $\alpha_i(t) = [\alpha_1(t), \alpha_2(t), \dots \dots \dots \alpha_m(t)]$ represents the mean and spreading nature of distribution function respectively. The total probability can be given as;

$$\textstyle\sum_{i=0}^{m} p_i\,(t) = 1 \tag{5.2}$$

It is assumed that i^{th}component of $x_t$is distributed normally with mean $\mu_i(t)$with a spreading $\alpha_i^2(t)$ is denoted by $N\{\alpha_i(t), \mu_i(t)\}$ at the tth time step which is being related with the event as;

$$A_i(t) = [x \sim N\{\alpha_i(t), \mu_i(t)\}] \tag{5.3}$$

Where $A_i(t)$, is mutually exclusive and exhaustive event, and the probability of the event$A_i(t)$for$(i = 1 \dots\dots\dots..m)$can be written as;

$$P\{A_i(t)\} = p_i(t) \tag{5.4}$$

If the i^{th}component of Cauchy's distribution is inured on signal x_t^l, then using the Baye's rule the post prior probability can be given as;

$$P\{f_i(x_t^l)|x_t^l\} = \frac{p\{x_t^l|f_i(x_t^l)\}\, P\{f_i(x_t^l)\}}{\sum_{j=1}^{m} p\{x_t^l|f_i(x_t^l)\}\, P\{f_i(x_t^l)\}}$$

The conditional probability density function of x_t^l at t^{th}time instant is $p\{x_t^l|f_i(x_t^l)\}$ gives $f_i(x_t^l)$ and x_t^l represents the lth specific data set from total of m data sets. The $f_i(x_t^l)$ is i^{th} Cauchy's distribution component is related to the event $A_i(t)$ as in eq. (5.3). Using the value of $A_i(t)$ with $f_i(x_t^l)$ in eq. (5.4), then $P\{A_i(t)\}$ is given as;

$$P\{A_i(t)\} = P\{f_i(x_t^l)\} = p_i(t) \tag{5.5}$$

Since relation in eq. (5.6) defined as

$$p\{x_t^l|f_i(x_t^l)\} = f_i\{x_t^l|\alpha_i(t), \mu_i(t)\} \tag{5.6}$$

Then $P\{f_i(x_t^l)|x_t^l\}$can be written as;

$$P\{f_i(x_t^l)|x_t^l\} = \frac{p_i(t).\, f_i\{x_t^l|\alpha_i(t), \mu_i(t)\}}{\sum_{j=1}^{m} p_i\,(t) f_i\{x_t^l|\alpha_i(t), \mu_i(t)\}} \tag{5.7}$$

and, the total probability is given as;

$$\sum_{i=1}^{m} P\{f_i(x_t^l)|x_t^l\} = 1 \tag{5.8}$$

Here, using the priori updates of parameter and maximizing log likelihood function w.r.t. variables of function $p_i(t)$, $\mu_i(t)$ and $\alpha_i(t)$, the parameters $p_i(t)$, $\mu_i(t)$and $\alpha_i(t)$ are being estimated. The exact likelihood function is not used here but log likelihood function is used

because the log likelihood function enables simpler formulation and at the same point it gets maximum likelihood function. Using the model parameters, the log likelihood function for n independent samples is given as;

$$L(t) = \sum_{l=1}^{n} \log_e \sum_{i=1}^{m} p_i(t).f_i\{x_t^l|\alpha_i(t), \mu_i(t)\} \tag{5.9}$$

Now, as per the condition mentioned in eq. (5.2), and if γ considered to be Lagrange multiplier, the equation will take a form as;

$$L(t) = \sum_{l=1}^{n} \log_e \sum_{i=1}^{m} p_i(t).f_i\{x_t^l|\alpha_i(t), \mu_i(t)\} - \gamma \left\{\sum_{i=1}^{m} p_i(t) - 1\right\} \tag{5.10}$$

The parameter $\mu_i(t)$can be estimated only when $L(t)$is assumed to maximum for $\mu_i(t)$and it can be obtained by;

$$\frac{\partial L(t)}{\partial \mu_i(t)} = 0 \tag{5.11}$$

The eq. (5.11) can be written as;

$$\frac{\partial L(t)}{\partial \mu_i(t)} = \sum_{l=1}^{n} \frac{p_i(t)\frac{\partial}{\partial \mu_i(t)}\left[\frac{\alpha_i(t)/\pi}{\{x_t^l - \mu_i(t)\}^2 + \alpha_i^2(t)\}}\right]}{\sum_{i=1}^{m} p_i(t).f_i\{x_t^l|\alpha_i(t), \mu_i(t)\}}$$

$$\frac{\partial L(t)}{\partial \mu_i(t)} = \sum_{l=1}^{n} \frac{p_i(t)\frac{\left[\frac{\alpha_{i(t)}}{\pi}.2(x_t^l - \mu_i(t)\right]}{[\{x_t^l - \mu_i(t)\}^2 + \alpha_i^2(t)\}]^2}}{\sum_{i=1}^{m} p_i(t).f_i\{x_t^l|\alpha_i(t), \mu_i(t)\}}$$

$$\frac{\partial L(t)}{\partial \mu_i(t)} = \sum_{l=1}^{n} \frac{p_i(t)\frac{\left[\frac{\alpha_{i(t)}}{\pi}.2(x_t^l - \mu_i(t)\right]}{\{x_t^l - \mu_i(t)\}^2 + \alpha_i^2(t)\}\{x_t^l - \mu_i(t)\}^2 + \alpha_i^2(t)\}}}{\sum_{i=1}^{m} p_i(t).f_i\{x_t^l|\alpha_i(t), \mu_i(t)\}}$$

Since, it is known that

$$f_i\{x_t^l|\alpha_i(t),\mu_i(t)\} = \frac{\frac{\alpha_{i(t)}}{\pi}}{\{x_t^l-\mu_i(t)\}^2+\alpha_i^2(t)\}}$$

Using above function in eq. (5.11), the equation will take a form as;

$$\frac{\partial L(t)}{\partial \mu_i(t)} = \sum_{l=1}^{n} \frac{p_i(t) f_i\{x_t^l|\alpha_i(t),\mu_i(t)\} \frac{[2(x_t^l-\mu_i(t)]}{[\{x_t^l-\mu_i(t)\}^2+\alpha_i^2(t)\}}}{\sum_{i=1}^{m} p_i(t).\, f_i\{x_t^l|\alpha_i(t),\mu_i(t)\}}$$

And it is mentioned in eq. (5.7) that,

$$\frac{p_i(t) f_i\{x_t^l|\alpha_i(t),\mu_i(t)\}}{\sum_{i=1}^{m} p_i(t).\, f_i\{x_t^l|\alpha_i(t),\mu_i(t)\}} = P\{f_i(x_t^l)|x_t^l\}$$

Putting the eq. (5.7) in eq. (5.11),

$$\sum_{l=1}^{n} \frac{P\{f_i(x_t^l)|x_t^l\}.\,[2(x_t^l-\mu_i(t)]}{\sum_{i=1}^{m} p_i(t).\, f_i\{x_t^l|\alpha_i(t),\mu_i(t)\}} = 0$$

$$\sum_{l=1}^{n} P\{f_i(x_t^l)|x_t^l\}.\,[2(x_t^l-\mu_i(t)] = 0$$

The parameter $\mu_i(t)$, is then estimated in eq. (5.12) as;

$$\mu_i(t) = \frac{\sum_{l=1}^{n} x_t^l.\, P\{f_i(x_t^l)|x_t^l\}}{\sum_{l=1}^{n} P\{f_i(x_t^l)|x_t^l\}}$$

(5.12)

Similarly, the parameter $\alpha_i(t)$ can be estimated only when $L(t)$ is assumed to maximum for$\alpha_i(t)$ and it can be obtained by;

$$\frac{\partial L(t)}{\partial \alpha_i(t)} = 0$$

(5.13)

$$\frac{\partial L(t)}{\partial \alpha_i(t)} = \sum_{l=1}^{n} \frac{p_i(t)\frac{\partial}{\partial \alpha_i(t)}\left[\frac{\alpha_i(t)/\pi}{\{x_t^l - \mu_i(t)\}^2 + \alpha_i^2(t)\}}\right]}{\sum_{i=1}^{m} p_i(t).f_i\{x_t^l|\alpha_i(t), \mu_i(t)\}}$$

$$\frac{\partial L(t)}{\partial \alpha_i(t)} = \sum_{l=1}^{n} \frac{\frac{p_i(t)\{x_t^l - \mu_i(t)\}^2 + \alpha_i^2(t)\}.1/\pi - \left\{\frac{\alpha_i(t)}{\pi}.2\alpha_i(t)\right\}}{[\{x_t^l - \mu_i(t)\}^2 + \alpha_i^2(t)\}]^2}}{\sum_{i=1}^{m} p_i(t).f_i\{x_t^l|\alpha_i(t), \mu_i(t)\}}$$

$$\frac{\partial L(t)}{\partial \alpha_i(t)} = \sum_{l=1}^{n} \frac{\frac{p_i(t)[\{x_t^l - \mu_i(t)\}^2/\pi - \alpha_i^2(t)/\pi\}]}{[\{x_t^l - \mu_i(t)\}^2 + \alpha_i^2(t)\}]^2}}{\sum_{i=1}^{m} p_i(t).f_i\{x_t^l|\alpha_i(t), \mu_i(t)\}}$$

Taking $\alpha_i(t)/\pi$ as common

$$\frac{\partial L(t)}{\partial \alpha_i(t)} = \sum_{l=1}^{n} \frac{\frac{p_i(t)\alpha_i(t)/\pi[\{x_t^l - \mu_i(t)\}^2/\alpha_i(t) - \alpha_i(t)]}{\{x_t^l - \mu_i(t)\}^2 + \alpha_i^2(t)\}\{x_t^l - \mu_i(t)\}^2 + \alpha_i^2(t)\}}}{\sum_{i=1}^{m} p_i(t).f_i\{x_t^l|\alpha_i(t), \mu_i(t)\}}$$

(5.14)

Since, it is known that;

$$f_i\{x_t^l|\alpha_i(t), \mu_i(t)\} = \frac{\frac{\alpha_{i(t)}}{\pi}}{\{x_t^l - \mu_i(t)\}^2 + \alpha_i^2(t)\}}$$

And using this expression in eq. (5.14), the equation will take form as given;

$$\frac{\partial L(t)}{\partial \alpha_i(t)} = \sum_{l=1}^{n} \frac{\frac{p_i(t)f_i\{x_t^l|\alpha_i(t), \mu_i(t)\}[\{x_t^l - \mu_i(t)\}^2/\alpha_i(t) - \alpha_i(t)]}{[\{x_t^l - \mu_i(t)\}^2/\alpha_i(t) - \alpha_i(t)]}}{\sum_{i=1}^{m} p_i(t).f_i\{x_t^l|\alpha_i(t), \mu_i(t)\}}$$

(5.15)

And it is mentioned in eq. (5.7) that,

$$\frac{p_i(t)f_i\{x_t^l|\alpha_i(t), \mu_i(t)\}}{\sum_{i=1}^{m} p_i(t).f_i\{x_t^l|\alpha_i(t), \mu_i(t)\}} = P\{f_i(x_t^l)|x_t^l\}$$

Using eq. (5.7) in eq. (5.15), then

$$\frac{\partial L(t)}{\partial \alpha_i(t)} = \sum_{l=1}^{n} \frac{P\{f_i(x_t^l)|x_t^l\}.[\{x_t^l - \mu_i(t)\}^2/\alpha_i(t) - \alpha_i(t)]}{[\{x_t^l - \mu_i(t)\}^2/\alpha_i(t) - \alpha_i(t)]}$$

$$\sum_{l=1}^{n} \frac{P\{f_i(x_t^l)|x_t^l\}.[\{x_t^l - \mu_i(t)\}^2/\alpha_i(t) - \alpha_i(t)]}{[\{x_t^l - \mu_i(t)\}^2/\alpha_i(t) - \alpha_i(t)]} = 0$$

$$\alpha_i^2(t) = \frac{\sum_{l=1}^{n} P\{f_i(x_t^l)|x_t^l\}.\{x_t^l - \mu_i(t)\}^2}{\sum_{l=1}^{n} P\{f_i(x_t^l)|x_t^l\}}$$

(5.16)

Now, the parameter $p_i(t)$ can be estimated only when $L(t)$ is assumed to maximum for $p_i(t)$ and it can be obtained by;

$$\frac{\partial L(t)}{\partial p_i(t)} = 0$$

$$\frac{\partial L(t)}{\partial p_i(t)} = \sum_{l=1}^{n} \frac{p_i(t) f_i\{x_t^l|\alpha_i(t), \mu_i(t)\}}{\sum_{i=1}^{m} p_i(t).f_i\{x_t^l|\alpha_i(t), \mu_i(t)\}} - \gamma$$

$$\sum_{l=1}^{n} \frac{p_i(t) f_i\{x_t^l|\alpha_i(t), \mu_i(t)\}}{\sum_{i=1}^{m} p_i(t).f_i\{x_t^l|\alpha_i(t), \mu_i(t)\}} - \gamma = 0$$

(5.17)

Using eq. (5.7) in eq. (5.17), then

$$\sum_{l=1}^{n} \frac{P\{f_i(x_t^l)|x_t^l\}}{p_i(t)} - \gamma = 0$$

$$p_i(t) = \frac{1}{\gamma} \sum_{l=1}^{n} P\{f_i(x_t^l)|x_t^l\}$$

(5.18)

Now, the total probability for m independent samples can be written as;

$$\sum_{i=1}^{m} p_i(t) = \sum_{i=1}^{m} \frac{1}{\gamma} \sum_{l=1}^{n} P\{f_i(x_t^l)|x_t^l\}$$

Then the parameter γ is being estimated as;

$$\gamma = \sum_{l=1}^{n}\sum_{i=1}^{m} P\{f_i(x_t^l)|x_t^l\}$$

(5.19)

Now from eq. (5.8), it is clear that total probability equal to 1, using this condition in eq. (5.19),

$\gamma = n$

Using the value of γ in eq. (5.18), the parameter $p_i(t)$, is now

$$p_i(t) = \frac{1}{n}\sum_{l=1}^{n} P\{f_i(x_t^l)|x_t^l\}$$

(5.20)

Putting the value of parameters $p_i(t)$, $\mu_i(t)$ and $\alpha_i(t)$,

$f(x_t)$

$$= \sum_{i=0}^{m}\frac{1}{n}\sum_{l=1}^{n} P\{f_i(x_t^l)|x_t^l\} \quad \frac{\left[\frac{\sum_{l=1}^{n} P\{f_i(x_t^l)|x_t^l\}.\{x_t^l - \mu_i(t)\}^2}{\sum_{l=1}^{n} P\{f_i(x_t^l)|x_t^l\}}\right]^{1/2} /\pi}{\left[\left\{x - \frac{\sum_{l=1}^{n} x_t^l.P\{f_i(x_t^l)|x_t^l\}}{\sum_{l=1}^{n} P\{f_i(x_t^l)|x_t^l\}}_i\right\}^2 - \frac{\sum_{l=1}^{n} P\{f_i(x_t^l)|x_t^l\}.\{x_t^l - \mu_i(t)\}^2}{\sum_{l=1}^{n} P\{f_i(x_t^l)|x_t^l\}}\right]}$$

(5.21)

The parameters and weight of Non-Gaussian cyclostationary noise, which is assumed to be the Cauchy's distribution i.e. $\mu_i(t), \alpha_i(t)$ and $p_i(t)$ is estimated using the discussed algorithm in two stages i.e. priori updates and post priori updates. The priori updates are used to set the values of parameters of Cauchy's function at each time instant and the final values are estimated using the post priori updates as given in eq. (5.12), (5.16) and (5.20). The priori values of parameters are set as;

The priori probability is set for m independent samples as;

$$p_{0i}(t) = \frac{1}{m}$$

(5.21)

The priori value for the $\alpha_i(t)$ is set as;

$$\alpha_{0i}^2(t) = \alpha_{01}^2(t-1) \tag{5.22}$$

Whereas the priori value of mean $\mu_i(t)$ is set for m independent samples as;

When m is odd,

$$\mu_{0i}(t) = \mu(t-1)\left(1 + \left(\frac{m+1}{2} - i\right)\frac{1}{m}\right) \tag{5.23}$$

And for even value of m and when $i = 1\ to\ m/2$

$$\mu_{0i}(t) = \mu(t-1)\left(1 + \left(\frac{m+2}{2} - i\right)\frac{1}{m}\right) \tag{5.24}$$

For even value of m and when $i = m/2\ to\ 1$

$$\mu_{0i}(t) = \mu(t-1)\left(1 + \left(\frac{m}{2} - i\right)\frac{1}{m}\right) \tag{5.25}$$

Where

$$\mu(t-1) = p_1(t-1)\mu_1(t-1) + \cdots p_m(t-1)\mu_m(t-1) \tag{5.26}$$

5.3 SIMULATION OF PROBABILITY DENSITY FUNCTION

The probability density function of the substrate noise using the discussed algorithm is simulated. The priori updates values are set and post priori updates values for the each parameter is evaluated, on the basis of these updates the PDF is estimated. The substrate noise shown in figure 5.1 is considered as an example for the estimation of probability density function.

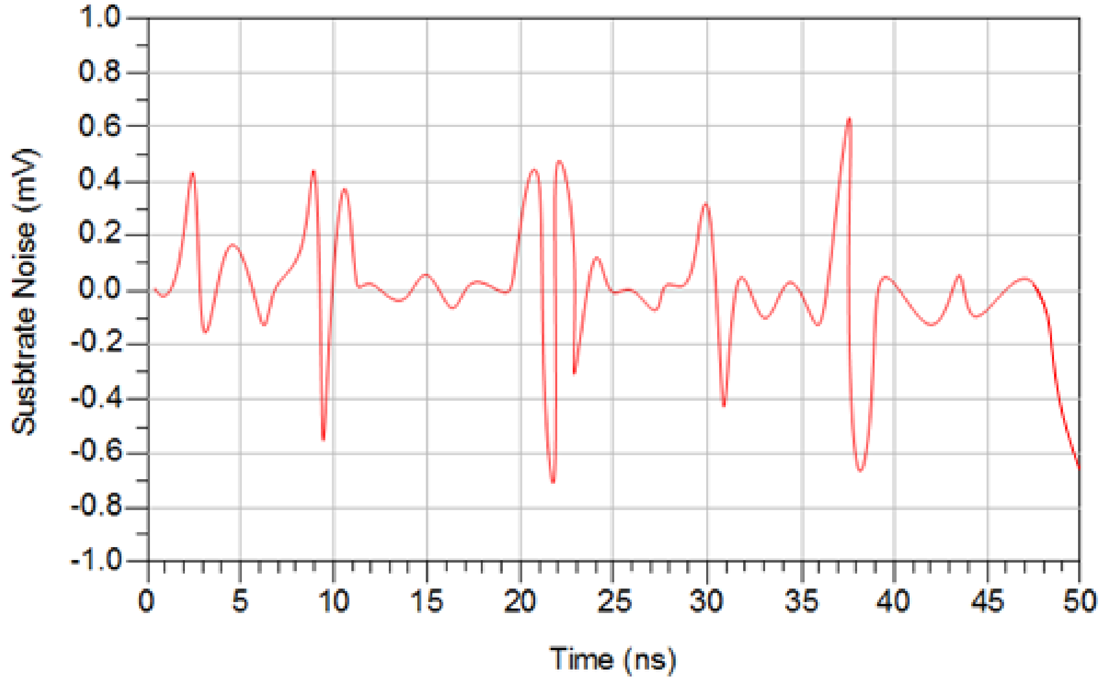


Figure. 5.1: Substrate noise considered as an example for substrate noise estimation

The substrate noise is a Non-Gaussian cyclostationary noise and assumed to have Cauchy's distribution, so; it is modeled by Cauchy's density function. For simulation setup total time is divided into five equal bins and each time bin is contained 1000 samples. For each of time bins the parameters $\mu_i(t), {\alpha_i}^2(t)$ and $p_i(t)$ are estimated. For example considered in figure 5.1, the priori updates values of $\mu_i(t), {\alpha_i}^2(t)$ and$p_i(t)$ for different time bin and a particular time instant (say 5th time instant) are set for $i = 1\ to\ 5$ (so, $m = 5$) and given as; $\mu_{0i}(t)$= [0.3629 0.3110 0.2592 0.2074 0.1555], $\alpha_{0i}^2(t)$= [0.45 0.4 0.3 0.35 0.25]and $p_{0i}(t)$= [0.2, 0.2, 0.2, 0.2, 0.2].

These priori updated values are again used to estimate post priori updated values. The PDF of substrate noise for the mentioned updates at the 5th time instant is estimated and is shown in figure 5.2. The same example of substrate noise is again modelled with a Gaussian distribution, the same priori updates values are taken and the post priori updates are evaluated for the Gaussian assumption. The Probability density function obtained from the modeling of non-Gaussian cyclostationary substrate noise using the Gaussian distribution

function and modeling of same using Cauchy's distribution function are plotted together as shown in figure 5.3. The probability density function of substrate noise by modeling using Gaussian distribution and Cauchy's distribution is estimated and compared in figure 5.3. The comparison of PDF obtained by both the modeling suggests that if the substrate noise is modeled by the Gaussian distribution, the probability density function will be bimodal instead of unimodal.

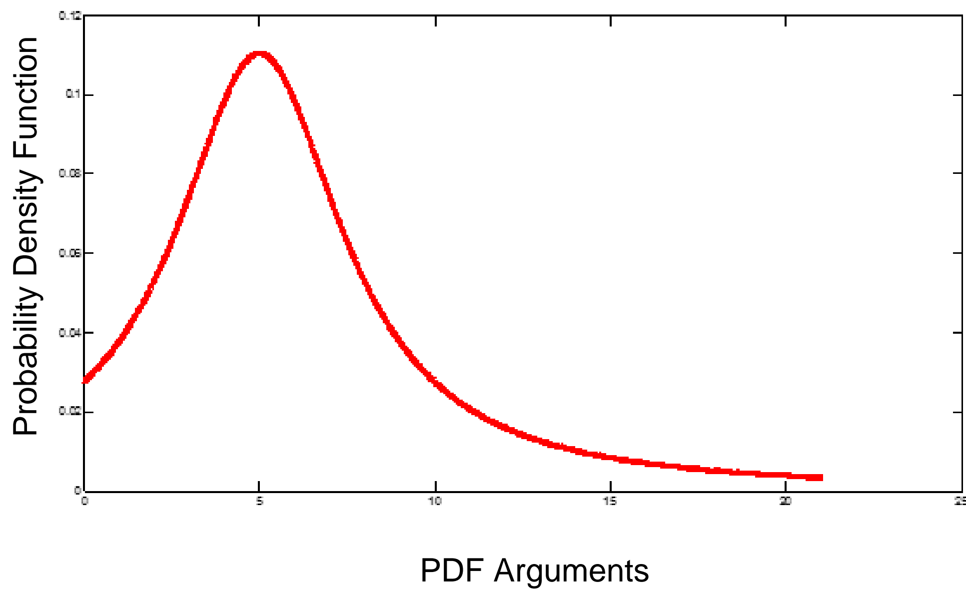


Figure. 5.2: Probability density function of Substrate noise at 5th time instant

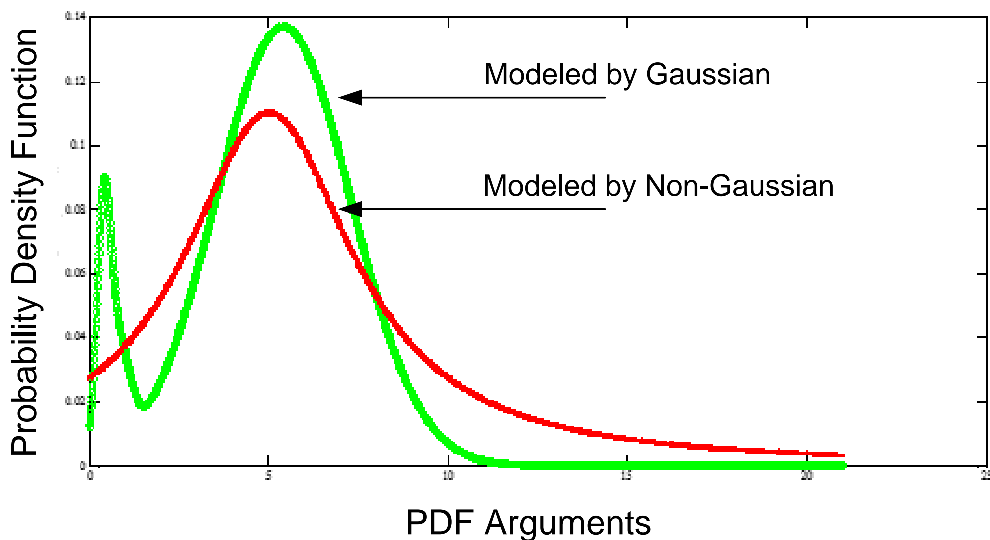


Figure. 5.3: Comparison of probability density function obtained by Gaussian and Non-Gaussian modeling

Therefore, the algorithm shows its capability, which is an efficient way to estimate the probability density function of non-Gaussian cyclostationary noise. The PDF estimation through the discussed algorithm is applicable to practical cases where the acquisition of noise data is possible through the simulation. In the PDF estimation of noise, if the noise is modeled by Cauchy's distribution, following the discussed technique and used in noise suppression circuits, it may increase the noise suppression capability of the circuit.

CHAPTER 6

CONCLUDING REMARKS AND FUTURE SCOPE

6.1 CONCLUDING REMARKS

In recent years, many research efforts have been put towards the estimation of substrate noise and to diminish the substrate coupling effects in analog/RF circuits. In this research work, an accurate substrate modeling technique has been proposed to apply during the substrate modeling for the estimation of substrate noise. Furthermore, an improved methodology for the estimation of substrate noise spectrum has also been proposed in this research work. The generation of substrate noise, the injection of substrate noise into the substrate and its propagation through the common substrate have been presented for better understanding of substrate noise coupling phenomenon. The performance of the mixed signal system in the presence of the substrate noise at device level, circuit level and system level has also been covered in this research work.

The substrate noise will not accurately be estimated without the clear understanding of substrate behavior on the different frequencies of operation. The exact substrate behavior can only be adjudged by using the proper substrate model. Since, the substrate profile plays a key role in the high frequency integrated circuit design. Therefore, the profiles of low resistive substrate as well as high resistive substrate along with their models and behaviors have been discussed in this work.

An accurate substrate modeling methodology has been proposed in this research work, which is the substrate resistive macromodeling method. In this method, the substrate network has been assumed as a pure resistive network up to the 12 GHz to 15 GHz frequency. A comparison between the proposed substrate modeling technique with other existing substrate modeling techniques has also been presented. The comparison has clearly

depicted that, the resistive macromodel method is the most suitable method which offers better accuracy, requires less parameter in modeling and needs lesser simulation time.

The substrate resistive macromodel has been validated by integrating two contacts over the top of the low resistive as well as the high resistive substrates. Out of these two contacts, one is assumed as the digital circuit while the other is assumed as analog circuit of a SoC. The simulation for the admittance between these two contacts on different frequencies is done for both types of the substrates. Further, a guard ring is placed around the digital contact and again the simulation for the admittance between the contacts at different frequencies has been done. It is observed from the simulation that, the magnitude of the admittance between the contacts for the low resistive substrate is of the order of 10^{-6} mho and is independent of frequency up to 6 GHz, whereas, the significant effect of frequency on the admittance has been started after 10 GHz. When a guard band is placed around the digital contact, then the magnitude of the admittance between contacts is now of the order of 10^{-8} mho and it is independent of frequency up to 10 GHz, while, the impact of frequency on admittance is now started after 15 GHz. Further, the simulation has done for the high resistive substrate and it is observed that the admittance between the contacts is independent of frequency up 5 GHz, while, the effect of frequency has been started after 8 GHz. When a guard band is placed around digital contact, the impact of frequency on admittance has been started after 10 GHz for the high resistive substrate.

The substrate resistive macromodel is again validated by simulating the isolation between the contacts. In this case, the separation between the contacts is kept variable and the isolation between the contacts has been simulated at different separations between the contacts. The substrate resistive macromodel is applied to model the low resistive as well as for the high resistive substrates and a back-plane inductance is used for grounding purpose. When a zero value of grounding inductance is used in the low resistive substrate,

it is observed that, the isolation between the contacts is increasing with increasing separation between contacts. But, when the values of grounding inductance is increased, the isolation has become independent of separation between the contacts. The same phenomenon is observed for the high resistive substrate also, except, when the backplane is left floating the isolation has become independent of separation between the contacts.

The substrate noise estimation and analysis in high performance VLSI circuits have also been presented in the research work. First of all, the variation in performances of the MOSFET in the presence of the substrate noise has been discussed. The curve between the gate to source voltage and drain current is potted for different values of injected noise at a fixed drain to source voltage of 0.8V. It is observed from the simulation that, the drain current is increasing when the level of noise injection is increasing, i.e., the drain current curve is shifting upward when the level of noise injection is increasing. Further, the variation in threshold voltage of the MOSFET is also simulated at fixed drain to source voltage of 0.8 V and fixed gate to source voltage of 0.6 V. The simulation result has depicted that, the threshold voltage decreases when the noise injection level increases. Furthermore, a pulse shaped noise signal of amplitude 0.6 V has been injected into the substrate and the potential underneath the channel has been simulated. It is observed from the simulation that, the shape of injected signal is deformed and amplitude is attenuated to -0.4 V to -0.2 V due to RC delay in the substrate.

A technique to develop circuit macromodel for high performance VLSI circuits has also been discussed in this research work. The circuit macromodel, which is developed using this technique is further simplified by combining the effect of parasitics. The components of the simplified circuit macromodel are, an equivalent well capacitance, an equivalent substrate resistance and switching current. The circuit macromodel has been validated for a CMOS inverter and substrate noise in the CMOS inverter is estimated. A pulse of 100

mV with rise and fall time of 1 ns is applied to the input of CMOS inverter and the substrate current peaks have been observed at both the high-to-low and the low-to-high transitions. The substrate current is observed to be of the order of 140 μA for 90 nm CMOS technology, while, the substrate current is 100 μA for 0.18 μm CMOS technology and 95 μA for 0.25 μm CMOS technology. This circuit macromodel has also been validated for a chain of five CMOS inverters.

The design and analysis of inductively source degenerated narrow band (0.5 to 3.5 GHz) low noise amplifier (LNA) has also been discussed in this research work. The schematics and layout of designed LNA are simulated for S (1, 1) and S (2, 2) and a comparison of results is presented. It is observed from the results that, the minimum noise figure of narrow band low noise amplifier (LNA) is 1.5 dB at resonance frequency of 1 GHz. Further, the smith chart of noise figure has also simulated and it is observed that, some of the noise circles have been disappeared when the frequency is increased, i.e., there cannot be the circles corresponding the noise figure below the minimum noise figure.

The substrate noise spectrum for RF CMOS using the proposed methodology has also been estimated in this research work. The substrate noise transfer function, substrate noise current, substrate noise voltage and power spectral density of substrate noise of RF CMOS are simulated and it is observed that, the substrate noise voltage is varying from -1.5 mV to 1.5 mV while the substrate current is varying from the -0.17 mA to 0.12 mA.

To demonstrate the substrate coupling phenomenon in a complex VLSI system, two different inverter circuits are taken into consideration. Out of these two inverter circuits, one is a saturated load NMOS inverter and it is considered as analog part of the SoC, while the other is a CMOS inverter and it is considered as digital part of SoC. Both the inverter circuits are integrated over a common multi-layered substrate and both the inverter circuits are operating on two different frequencies of 10 MHz (analog) and 25 MHz (digital). The

substrate network is assumed to be a pure resistive network. The substrate noise coupling between these circuits is analyzed through simulation and it is observed that, the noise coupling between the circuits exists only when the separation between circuits is of the order of 10 μm to 15 μm. It is further observed that when the input is applied at analog inverter only, then no noise coupling between two types of circuits is present and a peak at only 10MHz is observed. But, when the inputs at both the inverter circuits are applied, the noise coupling between the circuits exists and two peaks are observed at 10 MHz and 25 MHz.

The statistical behavior of the substrate noise is also studied in this research work. The substrate noise is assumed to possess the non-Gaussian cyclostationary nature. The non-Gaussian cyclostationary noise is modeled using a non-Gaussian mixture density and the probability density function (PDF) of non-Gaussian cyclostationary noise (substrate noise) is estimated by maximizing the log likelihood function and using the priori and post-priori updates. To validate this PDF estimation method, the PDF of substrate noise is further estimated by modeling of non-Gaussian noise using the Gaussian mixture density and a comparison between probability density functions (PDF) is also presented in this work.

6.2 FUTURE SCOPE

The issues those have been covered in this work and several other related issues which have not been covered in this work, may be explored in future. The substrate behavior in the radio frequency range changes when the frequency of operation changes. Therefore, the issue of substrate modeling technique with the board and supply line parasitics is needed to be considered. Though, this work has covered some substrate modeling techniques, but these are having some limitations. The substrate resistive macromodel is used to model the high resistive as well as low resistive substrates, and their behavior on different frequency of operation is studied. The substrate resistive macromodel is valid up to 10-15 GHz and

also depends on the substrate profile. Therefore, to meet the design challenges, a suitable substrate model technique is still to be explored where all the substrate parasitics should be well involved in substrate modeling and must be valid for the entire radio frequency range. The substrate noise estimation method is another critical issue, which is an attraction of research in recent years. Since, the substrate noise is not only a problem of on-chip design, but also the board level design. Therefore, the substrate noise estimation in on-chip design not only requires the accurate information of substrate parasitics and substrate model, but the board parasitics, the package parasitics, the supply switching ($L\, {di}/{dt}\ noise$) and switching in digital circuit are also vigorously required. In this research work, substrate noise in high performance VLSI circuits has been estimated without considering the package and board parasitics. Practically, an accurate substrate noise estimation method is recommended where the board parasitics and package parasitics must be considered during the estimation of substrate noise at the system level.

The substrate noise is assumed to possess the non-Gaussian cyclostationary behavior. The estimation of probability density function (PDF) of substrate noise is explained in this research work. The non-Gaussian cyclostationary noise is modeled using the non-Gaussian mixture density. Further, the probability density function is estimated by maximizing the log likelihood function and using priori and post-priori updates. It is recommended that, if the non-Gaussian cyclostationary noise (substrate noise) is modeled by non-Gaussian mixture density, and used in noise suppression circuit, it may increase the noise suppression capability of the circuit.