Constrained Random Verification of a Digital IP Using SystemVerilog

Thesis report submitted in partial fulfilment of the requirement for the Award of the Degree of

MASTER OF TECHNOLOGY

in VLSI DESIGN

Submitted By

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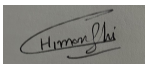
DECLARATION

I, HIMANSHI SOOD hereby declare that the work presented in this report entitled "**Constrained Random Verification of a Digital IP Using SystemVerilog**" in partial fulfilment of the requirement for the award of degree of Master of Technology (VLSI Design) submitted at **ELECTRONICS AND COMMUNICATION ENGINEERING DEPARTMENT** ,Thapar Institute of Engineering & Technology (Deemed to be University), Patiala is an authentic record of work carried out under supervision of **Dr. SAURABH SHARMA** (Assistant Professor) & **Dr. RAVI KUMAR** (Professor) & **Dr. NISHA GUPTA** (Technical Lead) from July, 2025 to July, 2026. The matter presented in this has not been submitted either in part or full to any other university or institute for the award of any other degree.



Date:28/06/2026

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	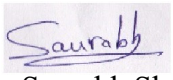 Dr. Saurabh Sharma Assistant Professor Department of Electronics and Communication Engineering, Thapar Institute of Engineering & Technology, Patiala Date:28/06/2026

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TO WHOMSOEVER IT MAY CONCERN

This is to certify that **Himanshi SOOD** has undergone internship in our **TRD** Group from **July 25, 2025 to July 24, 2026** and has successfully completed the project on: **Pre-Silicon Testchip (IO ring) validation.**

During the internship period, Himanshi was found to be sincere and professional in conduct.

We wish her all the best for the future endeavors.

for **STMicroelectronics Pvt. Ltd.**

Sanjay Kumar PIPLANI
India Talent Acquisition Head

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ABSTRACT

This thesis describes the restricted random verification of a digital IP for an AXI4-Lite-based design with SystemVerilog. As advanced communication protocols are incorporated into contemporary SoC designs, it is crucial to guarantee the functional accuracy of AXI-compliant intellectual property. Conventional directed testing techniques frequently fall short in covering protocol-level interactions and corner cases. In order to increase coverage, scalability, and reusability, a limited random verification methodology is used.

Developing a reusable and modular verification environment with SystemVerilog features like classes, randomization, constraints, assertions, functional coverage, and interfaces is the main goal of the effort. In order to validate address, data, and control channel transactions, an AXI-based digital IP is validated by producing random stimuli within specified protocol limitations. While assertions are used to verify protocol compliance and identify violations during simulation, functional coverage models are used to gauge the completeness of verification.

The verification environment is designed to achieve great coverage and to find corner case bugs fast. The efficiency of limited random verification in enhancing design resilience and cutting verification time is shown by simulation results. In order to validate complicated AXI-based digital IPs for dependable SoC integration, this work emphasizes the significance of sophisticated verification approaches.

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CHAPTER 1: Introduction

1.1 Background and Motivation

The rapid development of System-on-Chip architecture has necessitated the use of complex communication protocols, such as AXI, for high-performance data transfer between processing units, memory, and peripheral devices.[1] Because of its large bandwidth, support for numerous outstanding transactions, and independent address and data channels, AXI is extensively used in contemporary SoC architecture. Ensuring functional correctness and strict protocol compliance becomes a significant challenge in the verification process as AXI-based digital IP becomes more complex.

Traditional directed testing methods use manual test cases that focus on predefined scenarios. While these methods work well for basic functionality, they often struggle with complex transaction sequences, unusual protocol interactions, and unique situations [2]

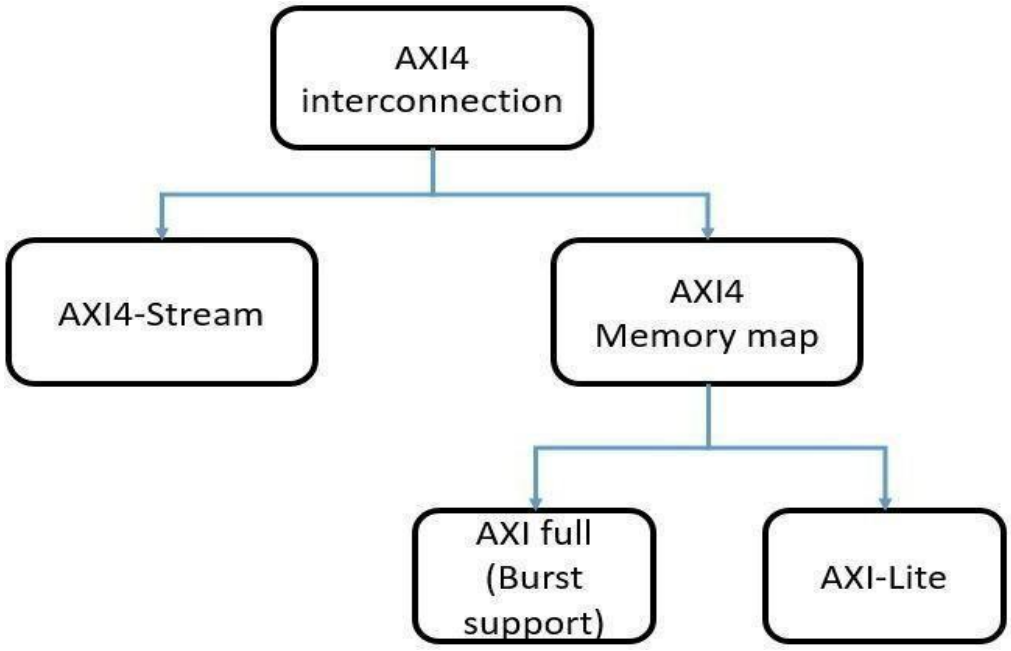

Figure 1 AXI4 Interconnection

Advanced verification features in SystemVerilog, including assertions, functional coverage, limited random stimulus generation, and object-oriented programming, enable more reliable, scalable verification. By automatically creating a variety of test scenarios under a predetermined protocol. With restrictions, constrained random verification improves coverage and increases the chances of finding hidden bugs. Functional coverage metrics also help evaluate verification completeness and direct test improvement.The need to provide a reusable, effective verification environment for an AXI-based digital IP is the driving force behind this thesis.[3] The objective is to outperform conventional methods in coverage, bug detection, and scalability by implementing restricted-random verification in SystemVerilog. This work demonstrates how advanced verification techniques can enhance reliability and accelerate the validation of complex AXI-based designs in modern SoC development.

1.2 Importance of Bus Protocols in Modern SoC

In modern System-on-Chip (SoC) architecture, various functional modules, such as processors, memory controllers, accelerators, and peripheral interfaces, need to communicate effectively to achieve performance targets.Bus protocols provide a standard way for communication. They describe how data, addresses, and control signals are shared between the modules. These protocols set the timing rules, communication methods, and formats for data exchanges to make sure that the different parts of the chip work together smoothly and reliably. Without these clear communication guidelines, it would be difficult to combine separately designed pieces of technology, which could lead to mistakes and problems. In modern System-on-Chip (SoC) architecture, various functional modules, such as processors, memory controllers, accelerators, and peripheral interfaces, need to communicate effectively to achieve performance targets. Bus protocols are like a common language that different parts of a computer chip use to talk to each other. They make it easier for these parts to share information, such as data and addresses, while keeping everything organized. By setting clear rules about timing and how the information is put together, bus protocols help all the components w o r k together smoothly.

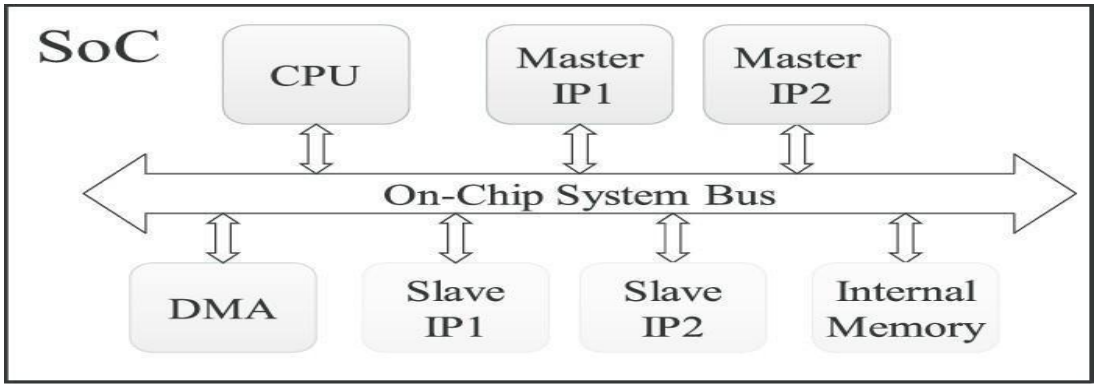

Figure 2 SoC Bus

As SoC complexity continues to increase, advanced bus protocols play a critical role in enabling high-bandwidth, low-latency, and scalable system performance. Features such as burst transfers, pipelined operations, and support for multiple outstanding transactions, enable efficient utilization of system resources. Standardized protocols also enhance IP reusability and interoperability, allowing designers to integrate third-party IP with minimal modification. Therefore, robust bus protocol design and thorough verification are essential to ensure stable operation, optimal performance, and overall system reliability in modern SoC implementations.

1.3 Introduction to AXI Protocol

Advanced eXtensible Interface (AXI) is a high-performance on-chip communication protocol defined by the ARM AMBA specification. It is widely used in modern System-on-Chip designs [6]. AXI supports high bandwidth, low latency, and high-frequency system needs. It separates the address and data phases, which allows for parallel transaction processing and improves overall throughput.The protocol is mostly based on a master/slave architecture where masters initiate read or write operations and enslaved people respond to these requests. AXI uses independent read and write channels, allowing simultaneous read and write transactions and thereby enhancing performance compared to earlier bus protocols.AXI is comprised of five independent channels: write address, write data, write response, read address, and read data. To ensure reliable data transport, each channel uses a handshake protocol based on valid and ready signals. Block data transfers are enabled by the protocol's support for burst-based transactions with fixed, increment, and wrap burst types [7]. It also allows for

multiple excellent transactions and out-of-order completion, depending on the system setup. This greatly improves bus use. Other features like byte-level write strobes, adjustable data widths, and support for quality of service make AXI very scalable and usable in many different applications.Because of these features, AXI has become a common interconnect protocol in high-performance SoC designs. It requires careful and organized testing to make sure it meets protocol standards and works correctly.

1.4 Verification Challenges in AXI Based Digital IP

Verifying AXI-based digital IP can be tough because the protocol is both complicated and flexible. It has different channels for sending and receiving data, can quickly transfer large amounts of data in bursts, and can handle several transactions at the same time. Plus, features like adjustable data width and burst length make things even trickier. To really make it work, you need to understand all these details well.

All these features lead to a huge number of possible scenarios, making it tough to test everything simply. Even with a basic setup, you can end up with thousands of valid combinations, such as different address alignments, burst types, transfer sizes, and response conditions. Ensuring that everything works correctly across all these variations is a significant challenge in the verification process. Even a small configuration can produce thousands of valid combinations of address alignment, burst types, transfer sizes, and response conditions. Ensuring that the design operates correctly across all these combinations poses a major verification challenge.[8].

One of the primary challenges is handling concurrent, overlapping transactions. Since AXI allows read and write operations to occur simultaneously and supports multiple outstanding requests, the verification environment must accurately track each transaction using identification signals. Maintaining

correct ordering rules for transactions with the same identification tag while allowing flexibility for different tags adds further complexity[4]. Detecting subtle bugs related to data corruption, incorrect response generation, or improper handling of back-to-back transfers requires sophisticated monitoring and checking mechanisms.

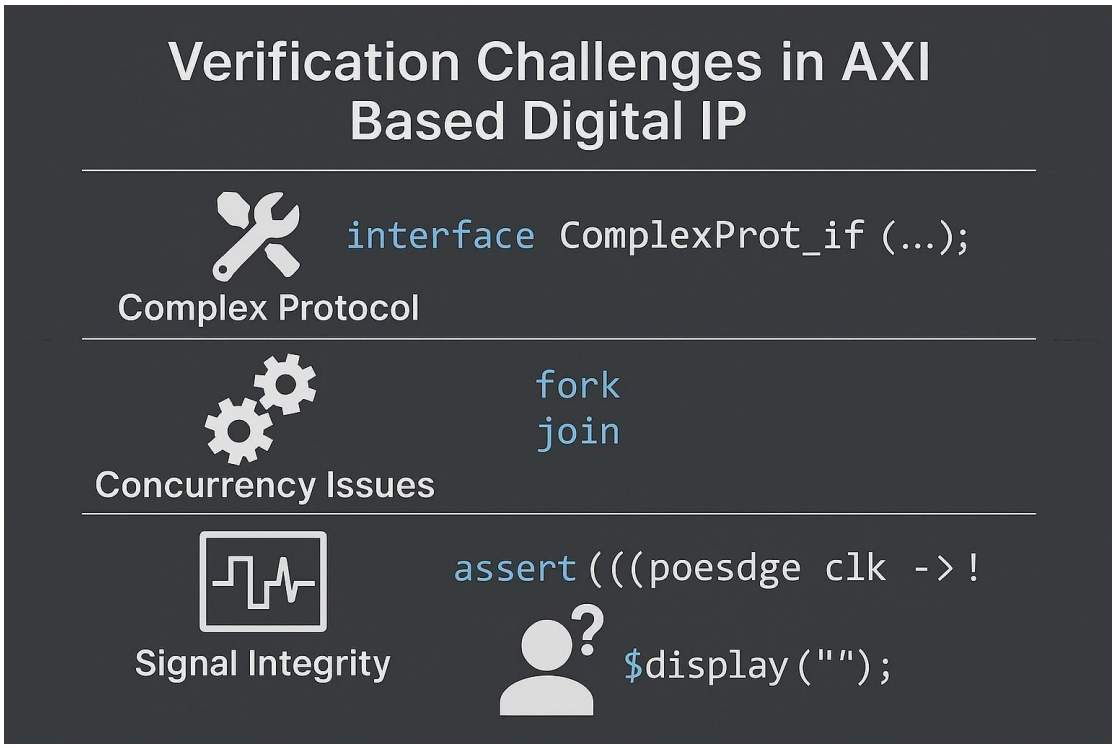

Figure 3 Verification Challenges

Another challenge arises from the handshake-based flow control mechanism. The valid and ready signals on each channel allow either the enslaver or enslaved person to introduce wait states. This can create numerous timing variations that must be verified to ensure protocol compliance[5]. For example, the design must correctly handle cases where ready is deasserted for multiple cycles or when valid is asserted intermittently. Verifying all such timing combinations through directed tests is impractical, as many corner cases may be overlooked.

Handling burst transactions can be quite complex in system design. You need to keep track of burst-length counters, create addresses for different types of bursts (both for incrementing and wrapping), and ensure that bursts end properly. Mistakes in managing these bursts can be tricky to spot, especially in specific situations like when dealing with boundary alignments or hitting the maximum burst length. It's also important that the system gives clear feedback about whether a process was successful or if there were errors, especially if there's an invalid access or a misaligned address. Because of the many complexities involved, just using traditional directed testing usually isn’t enough to thoroughly verify our systems. There are so many potential scenarios, along with

overlaps in how things operate at the same time and differences in timing, that it's clear we need to use more flexible testing methods, like constrained-random verification and coverage-driven approaches. Building a strong verification environment is essential to thoroughly examine unusual cases, find hidden bugs, and ensure that AXI-based digital IP follows all the necessary protocols.

1.5 Need for Constrained Random Verification

As the complexity of AXI-based digital IP increases, traditional directed testing becomes insufficient for comprehensive functional validation. Directed testing relies on manually written test cases that target specific scenarios defined by the verification engineer. While this method does a good job of checking basic features and typical scenarios, it misses the mark when it comes to those rare situations and unexpected issues that can pop up between different parts of the protocol..In AXI systems, where multiple parameters such as burst type, transfer size, address alignment, response type, and concurrent transactions interact in complex ways, the number of possible scenarios grows rapidly. Manually covering all such combinations is impractical and time-consuming [3].

Constrained random verification is a clever way to make testing easier and more effective. Instead of manually creating each test case, verification engineers set up a few simple rules to guide the process. These rules help ensure the system behaves as expected—like creating patterns that make sense, arranging addresses correctly, and generating the right responses.

This method takes advantage of randomness to create different test cases by mixing rules in various ways. This helps find tricky bugs that might be missed when testing is done manually. In simple terms, it makes the testing process faster and more thorough, which means it can catch problems that might otherwise slip by unnoticed.

Another important reason for using constrained random verification is its ability to handle multiple operations happening at the same time and variations in timing effectively. The AXI protocol allows for simultaneous reading and writing, can manage several transactions at once, and uses a flexible handshake system for control. These features lead to many different timing and ordering scenarios that are hard to test with

directed methods. By using constrained random testing, we can easily create situations with overlapping transactions and different handshake conditions, which puts the design to the test in realistic and challenging ways. Plus, this method works well with functional coverage tools that help ensure we're testing everything we need to.

Coverage metrics help us see which parts of a project we've tested and which areas might have been missed. By pointing out the sections that still need some work, we can update our testing plans to make sure nothing is overlooked. Reviewing our progress not only shows us what we've done but also increases our confidence in how solid our design is and that it's ready for launch.

On top of that, constrained random environments are usually designed to be modular and reusable. Once we create a verification framework using SystemVerilog tools—like transaction classes, drivers, monitors, scoreboards, and assertions—it can easily be tweaked for different AXI-based IP setups with just a few changes. This makes it easier to scale up our efforts and saves time when working on future projects.

In short, using constrained-random verification is really important when it comes to checking complex AXI-based digital chips. This method helps us catch bugs more easily, increases the number of tests we can run, and allows us to expand our testing efforts without too much hassle. It also provides a dependable way to make sure that all the protocols work correctly in today's advanced chip designs.

1.6 Objectives of the Thesis

The main goal of this thesis is to build a detailed, reusable testing environment for AXI-based digital components using the constrained-random verification method in SystemVerilog. Since AXI is a complex and versatile protocol, this work focuses on ensuring everything functions correctly, follows the protocol's rules precisely, and handles tricky situations that may arise during data reading and writing, burst transactions, handshakes, and responses under different operating conditions.

Constrained-random stimulus is a powerful tool that automatically generates a diverse array of legal transaction combinations by specifying rules for address alignment, burst length, transfer size, and transaction type. This approach significantly improves bug detection when compared to traditional directed testing, especially for problems related to concurrency, timing variations, and boundary conditions. To measure how

thoroughly verification has been completed, functional coverage models—such as covergroups and cross-coverage—are established, which also help refine the stimuli based on coverage goals. At the same time, protocol assertions are integrated to consistently monitor AXI timing and handshake rules, enabling early identification of protocol violations and enhancing the overall verification process.

Develop a SystemVerilog-based constrained-random verification environment for an AXI-based digital IP.Ensure functional correctness and AXI protocol compliance for read/write operations, bursts, handshakes, and responses.

Implement constrained-random stimulus with constraints on address alignment, burst length, transfer size, and transaction type to explore a wide range of valid scenarios.

Design functional coverage models (covergroups and crosses) and use coverage analysis to achieve coverage closure. Integrate SystemVerilog Assertions to detect protocol violations and strengthen the overall checking mechanism. Demonstrate the effectiveness, scalability, and reusability of the verification framework across different AXI-based IP configurations.

1.7 Scope and Limitations

This thesis is all about creating a verification environment - think of it as a testing playground - for digital IP, it uses AXI, and it is all done using SystemVerilog. The main goal here is to ensure the design works as it should, according to AXI's rules, and this is done by verifying it at the register-transfer level. So the environment has all kinds of features, like modelling transactions, generating stimuli, and checking everything with a scoreboard and assertions. It is like a comprehensive checklist to ensure everything complies. Moreover, do not forget to dig into functionality that's age, because that is the key to finding those bugs that can hide and get past you. The verification process itself is fairly comprehensive, looking at reads, writes, bursts, handshakes, and all the corner cases you can think of, all using constrained-random techniques. The verification process itself is pretty comprehensive, looking at reads, writes, bursts, handshakes, and all the corner cases you can think of, all using constrained-random techniques. It is worth noting that this study is solely on simulation-based verification (no formal verification/hardware emulation). The analysis is complete in terms of functional correctness and coverage, without the

distraction of timing closure or physical design details. Depending on the IP you are working with, some advanced AXI features might not be fully explored - things like quality-of-service optimisation, low-power extensions, or security enhancements. Moreover, a major assumption is that the system-level integration is correct, so this thesis primarily focuses on validating the standalone AXI-based IP block. Even with these limitations, this work provides a solid foundation for understanding how to apply constrained-random verification to complex digital designs that are primarily bus-based.

CHAPTER 2: Literature Review

ARM Ltd. [1]: The AMBA AXI protocol specification really gives a clear picture of what AXI4 and AXI4-Lite communication are all about. It covers key topics such as channel architecture, the handshake, and response signalling. This standard is your go-to reference when checking out AXI4-Lite intellectual property (IP).It needs you to use constrained-random verification setups to test things like single-beat transfers, VALID–READY handshakes, address alignment, and whether responses are correct (like OKAY or SLVERR), even when the conditions are a bit random. The main aim is to ensure that everything works as it should, even in unpredictable situations.

S. Tasiran; K. Keutzer et.al [2]: The authors introduced coverage metrics for functional validation of hardware designs using constrained random simulation. Their work emphasises coverage-driven verification and randomised test generation, both directly applicable to AXI4-Lite IP verification to ensure exhaustive exploration of corner cases in read and write transactions.

Harry D. Foster et.al [3]: This discuss trends in verifying the functionality of complex System-on-Chip (SoC) designs, using methods such as constrained-random and coverage-driven testing. They emphasise the importance of achieving functional coverage closure and using assertion-based testing. These things are key for checking the AXI4-Lite interface logic, ensuring the protocol timing is correct, and maintaining channel synchronisation.

P. Mishra; N. Dutt et.al [4]: The paper explores verification methodologies for programmable embedded architectures and SoC IPs. The authors emphasise reusable testbench architecture, transaction-level modelling, and constrained-random stimulus, which are widely adopted in UVM environments for AXI4-Lite enslaved person and peripheral verification.

Erik Seligman; Tom Schubert; M. V. Achutha Kiran Kumar et.al [5]: are investigating hybrid verification methods. They mix formal verification with constrained-random simulation, which really helps find bugs that might otherwise be missed. Their focus is on tricky corner cases—like deadlocks and protocol mismatches—that are critical for checking AXI4-Lite enslaved people. By doing this,

they improve overall issue detection in interface-based IPs.

Chris Spear; Greg Tumbush et.al [6]: Their work explains sequence-item randomisation, constraint blocks, and functional coverage models, all of which are essential for building AXI4-Lite verification agents, including drivers, monitors, and scoreboards.

Ben Cohen et.al [7]: This study looks at assertion-based verification using SystemVerilog Assertions (SVA) and constrained-random stimulus. This approach really helps in automatically checking protocols, which is great for verifying AXI4-Lite IP. It takes care of important things like handshake stability, response timing, and data integrity that really matters for reliable performance.

R. Drechsler; S. Wille et.al [8]: The authors put forward some formal and simulation-based verification techniques for communication interfaces in system-on-chip (SoC) designs. Their approach really helps improve the correctness and reliability of protocols, which is really important for checking AXI4-Lite intellectual property (IP). In this situation, we need to make sure that channel independence a nd transaction ordering are validated—especially when dealing with constrained random traffic

.**Matthew Ballance et.al [9]:** This study is about reusable UVM verification environments for AMBA based IP cores. It shows how we can use sequencers, randomized sequences, coverage collectors, and protocol monitors to validate AXI4-Lite bus interfaces in complex SoC designs. This approach really helps ensure that these systems are tested thoroughly and meet the needed requirements.

Janick Bergeron; Eduard Cerny; Alan J. Hu et.al [10]: The authors introduced reusable verification methodologies based on constrained-random stimulus and a layered testbench architecture. These concepts significantly improve scalability and verification productivity and are widely used in AXI4-Lite UVM testbenches to validate protocol compliance and functional correctness.

Piziali et.al [11]: This research presents functional verification coverage measurement and analysis techniques for digital systems. The work emphasizes constrained random testing and coverage-driven verification, which are essential for ensuring thorough validation of AXI4-Lite read/write channels and response logic.

K. Keutzer et.al [12]: The study discusses scalable system-level verification strategies for SoC architectures. The authors highlight regression testing, constrained random

simulation, and functional coverage analysis, which supports comprehensive AXI4-Lite IP verification in modern VLSI designs.

M. Armstrong [13]: The author presented a verification method using SystemVerilog for AXI4-Lite register interfaces. They showed that both directed and structured test sequences can verify that the protocol is correctly followed at the register level. The work points out how important it is to verify the interface-level for the VALID and READY handshakes. This focus really drives the constrained random approach used in this thesis, which allows for exploring more scenarios than just the manually written test cases.

S. H. Kim and J. Lee [14]: The authors developed a SystemVerilog testbench to verify the functionality of the AXI4-Lite enslaved person. They showed that it really works well for making sure read and write operations are correct. This effort lays a good groundwork for creating transaction-level stimuli and verifying responses. It also helps inform the scoreboard-based reference model architecture that's used in this study.

A. K. Patel and R. Gupta [15]: suggested using constrained-random verification for AXI4-Lite peripherals in SystemVerilog. They found that generating stimulus through constraints provides a much broader coverage of valid protocol scenarios than directed methods alone. These findings strongly support the constrained-random approach used in this thesis and help explain the address and data constraints implemented in the transaction class.

L. Nguyen and P. Mishra [16]: The presented a verification approach based on assertions to verify that the AXI4-Lite protocol is being followed. They showed how concurrent property checks can catch temporal protocol violations that data-level scoreboard comparisons might miss. This work highlights the importance of using SVA-based protocol checking as an additional layer of verification, along with functional coverage and scoreboard checking, in this study. It is a nice way to reinforce that combining these methods can lead to better results.

D. Roy and S. Chattopadhyay [17]: The authors investigated coverage-driven verification of AXI4-Lite designs using SystemVerilog and showed that coverage feedback loops significantly accelerate verification closure compared to open-loop random regression. Their coverage closure methodology, which iteratively refines

constraints based on unhit bins, directly influences the coverage analysis and regression strategy discussed in the comparative evaluation chapters of this thesis.

J. Park and H. Kim [18]: The authors developed reusable SystemVerilog verification components for AXI4-Lite. They developed a structured agent-based architecture that splits tasks into independent, reusable modules for protocol driving, passive monitoring, and result checking. These reusability ideas align well with the UVM component architecture described in this thesis and support the point that a modular testbench design can help reduce long-term verification maintenance costs.

M. S. Rahman and T. Ahmed [19]: The authors proposed transaction-level modelling and verification of AXI4-Lite using SystemVerilog, demonstrating that abstracting bus activity into transaction objects simplifies stimulus generation, scoreboard checking, and coverage collection compared to signal-level testbench approaches. Their transaction abstraction methodology is directly reflected in the design and monitor reconstruction logic implemented in the UVM testbench for this study.

K. S. Rao and V. Menon [20]: The authors combined formal verification and simulation-based checking with SystemVerilog Assertions for AXI4-Lite protocol validation, showing that the two techniques are complementary and together provide higher confidence than either alone. Their work motivates the inclusion of assertion-based protocol checking alongside simulation-driven functional coverage in the verification environment presented in this thesis.

E. Johnson and A. Verma [21]: The authors explored randomised verification of AXI4-Lite register blocks using SystemVerilog and demonstrated that seed-based random regression with constraint-guided stimulus discovers a higher proportion of corner case bugs than equivalent directed test suites of comparable size. Their quantitative bug-detection analysis provides direct comparative context for the fault-injection results reported in the experimental evaluation of this thesis.

P. Das and S. Banerjee [22]: proposed a protocol-checking method using SystemVerilog Assertions (SVA) for AXI4-Lite interfaces. They created a set of assertions that address handshake sequencing, channel independence, and response ordering—pretty comprehensive stuff! Their assertion library acts as a go-to reference for the protocol property definitions found in the AHB assertion verification section of

this thesis. It really shows how SVA-based checking can be applied to other AMBA protocol families as well.

S. Gupta and R. Kumar [23]: The authors examined how to close functional coverage gaps in AXI-based verification environments. They developed a systematic approach that combines coverage hole analysis, adjusted constraint weights, and targeted directed tests to address challenging coverage areas efficiently. This iterative strategy not only helps close those gaps but also plays a key role in regression planning and the coverage-driven feedback loop discussed in the experimental setup chapter of this thesis.

A. Jain and P. R. Kumar [24]: The authors presented design and verification of AXI4-Lite peripheral interfaces using SystemVerilog, providing a detailed account of the testbench architecture, coverage model, and test plan required for complete peripheral validation. Their work confirms that a structured verification plan with clearly defined coverage goals and pass-fail criteria is essential for systematic protocol verification, a principle that underpins the test plan and coverage metric definitions adopted in this study.

M. H. Siddiqui and S. N. Sharma [25]: proposed a coverage-driven methodology for register-transfer-level verification of bus protocols, establishing quantitative relationships between coverage metrics and the probability of bug detection. Their analysis of coverage completeness as a predictor of verification quality supports using functional and code coverage measurements as the primary evaluation criteria in the comparative analysis presented in this thesis.

R. K. Singh and V. B. Rao [26]: The authors addressed constraint-based stimulus generation for SoC verification using SystemVerilog, demonstrating that well-structured constraint hierarchies enable efficient exploration of large legal stimulus spaces without sacrificing protocol validity. Their constraint design principles guide the address alignment, burst length, and data array size constraints implemented in the AHB transaction class of this study.

D. Banerjee and A. Mukherjee [27]: The authors presented assertion-based verification for protocol compliance in digital IP cores, showing that a carefully selected set of protocol properties expressed as SystemVerilog concurrent assertions

provides continuous compliance monitoring that complements functional simulation.

Their work on assertion coverage reporting as a third dimension of verification completeness, alongside functional and code coverage, is reflected in the assertion coverage analysis section of this thesis.

P. Saha and M. Das [28]: proposed transaction-level modelling for scalable RTL verification of AMBA peripherals, demonstrating that higher levels of stimulus abstraction reduce verification development effort and improve portability across different AMBA protocol variants. Their scalability analysis supports the argument made in this thesis that a transaction-level UVM architecture delivers better performance.

H. Zhou and Y. Chen [29]: The authors investigated reusable verification components for bus functional models in SystemVerilog and presented a component packaging methodology that enables protocol-specific drivers and monitors to be deployed across multiple projects without modification. Their reusability framework aligns with the UVM agent packaging approach described in this thesis and reinforces the scalability advantages of the UVM methodology over project-specific directed testbenches..

A. Bansal and S. K. Gupta [30]: The authors addressed verification planning and coverage analysis for memory-mapped register blocks, proposing a structured test plan format that maps protocol features to coverage bins and defines measurable closure criteria for each. Their planning methodology directly influences the definition of coverage metrics and the regression strategy sections of the experimental setup chapter in this thesis.

N. R. Patel and K. V. Rao [31]: examined simulation-based and assertion-based verification methods for simple bus protocols, as discussed in IEEE Access. They found that these two approaches catch different kinds of design bugs, and when used together, they provide better overall defect coverage than either method alone. This really supports the multi-layer verification strategy used throughout this thesis, which includes scoreboard checking, functional coverage, and SystemVerilog Assertions (SVA).

In the past, verification relied mostly on manually written test cases to test specific functions. This method is pretty simple, but it really depends on the verification engineer's

experience, which can sometimes lead to missing rare corner cases. As designs grew more complex, coverage-driven verification methods emerged to systematically assess how complete the verification is. Random verification introduced automatic stimulus generation, but the problem with unconstrained randomisation is that it sometimes produces invalid or meaningless transactions. To fix this, constrained random verification used protocol-specific rules to guide stimulus generation better. Then, SystemVerilog made things even better by adding object-oriented programming, functional coverage, assertions, and various randomisation features. Many studies have shown that constrained random verification works great for complex bus protocols, leading to better bug detection and improved coverage closure compared to older methods.

CHAPTER 3: AXI Protocol Architecture and Design Under Test

3.1 Overview of AXI Architecture

The AXI architecture is designed to provide high performance and scalable communication within a System on Chip environment. It follows a master slave model in which masters initiate read and write transactions and slaves respond to these requests. The architecture is optimized for high frequency operation and efficient data movement between processors, memory controllers, and peripheral modules. AXI is different from traditional shared bus systems because it allows several transactions to happen at the same time. This really helps improve bandwidth use and reduces communication bottlenecks.One important part of the AXI architecture is how it splits the address and data phases. For read and write operations, there are separate channels. Address transfer can happen on its own, separate from data transfer, which really helps make the whole process a lot smoother. The architecture consists of five different channels, write address, write data, write response, read address, and read data. Each channel has its own control and handshake signals, so they can work at the same time and in a pipelined way.

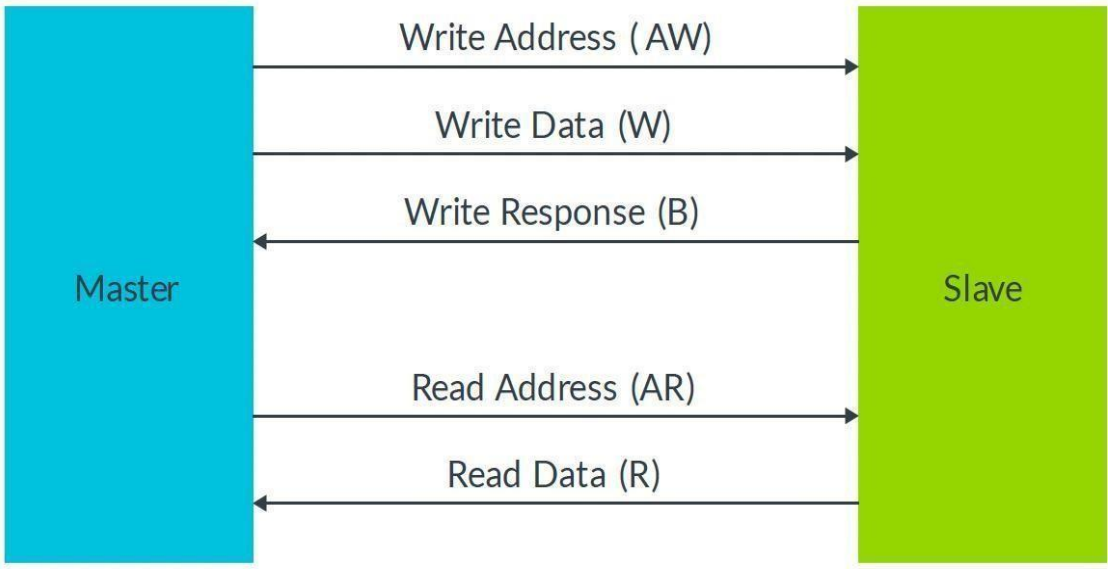

Figure 4 AXI Architecture

The AXI architecture allows for burst-based communication, which means that several data transfers can happen under one address transaction. The burst parameters include details like how many data beats there are, the size of the transfer, and how the addresses progress. This method helps cut down on the overhead linked to addressing, while also making it easier to transfer blocks of data.

Transfers and burst operations really enhance the efficiency of a system. The architecture has identification signals that let several transactions happen at the same time. This way, advanced interconnects can process and finish transactions more effectively—without relying too much on strict sequential dependencies.

Flow control in AXI is managed through a handshake mechanism based on valid and ready signals on each channel[10]. This decentralized control approach allows either the sender or receiver to insert wait states when necessary, providing flexibility in handling variable latency components. The architecture is highly configurable, supporting different data widths and address widths, making it adaptable to a wide range of applications. Overall, the AXI architecture provides a flexible, high bandwidth, and scalable communication framework suitable for complex modern SoC designs..

3.2 AXI Channels and Signals

AXI communication is made up of five independent channels, and each one has its own role in transferring different types of information between the master and slave devices. This division into separate channels really helps with parallel and pipelined transactions, which boosts the overall system throughput. Each channel works with a handshake mechanism that uses valid and ready signals to guarantee reliable data transfer. Because the channels are independent, they can handle simultaneous read and write operations; plus, they allow for flexible timing behavior in complex system-on-chip (SoC) systems.

Global	Write address channel	Write data channel	Write response channel	Read address channel	Read data channel
ACLK	AWVALID	WVALID	BVALID	ARVALID	RVALID
ARESETn	AWREADY	WREADY	BREADY	ARREADY	RREADY
–	AWADDR	WDATA	BRESP	ARADDR	RDATA
–	AWPROT	WSTRB	–	ARPROT	RRESP

Figure 5 AXI Signals and Channel

3.2.1 Write Address Channel

The write address channel is responsible for transferring address and control information required for a write transaction from the master to the slave. It includes signals that define the start address of the transfer, burst length, burst size, burst type, protection attributes, and transaction identification. The master asserts the address valid signal when the address and control information are ready, and the slave asserts the address ready signal when it can accept the information. Once both signals are asserted in the same clock cycle, the address phase is completed. This channel does not carry actual data but defines how and where the write data will be stored[11].

3.2.2 Write Data Channel

The write data channel carries the actual data to be written to the slave. It includes data signals, byte level write strobes, and a signal indicating the last transfer in a burst. The byte strobe signals specify which bytes within the data word are valid, allowing partial updates of memory locations. The data valid and data ready handshake signals control the transfer of each data beat. In burst transactions, multiple data beats are transferred sequentially, and the last signal identifies the final beat of the burst. This channel operates independently of the write address channel, enabling pipelined behavior[11].

3.2.3 Write Response Channel

The write response channel provides status information from the slave back to the master after completion of a write transaction. It includes response signals indicating whether write operation was successful or if an error occurred. The response also

carries the identification information corresponding to the original write request. The slave asserts the response valid signal when the response is available, and the master asserts the response ready signal when it is ready to accept the response. This channel ensures that the master receives confirmation of transaction completion and can detect any access violations or errors[12].

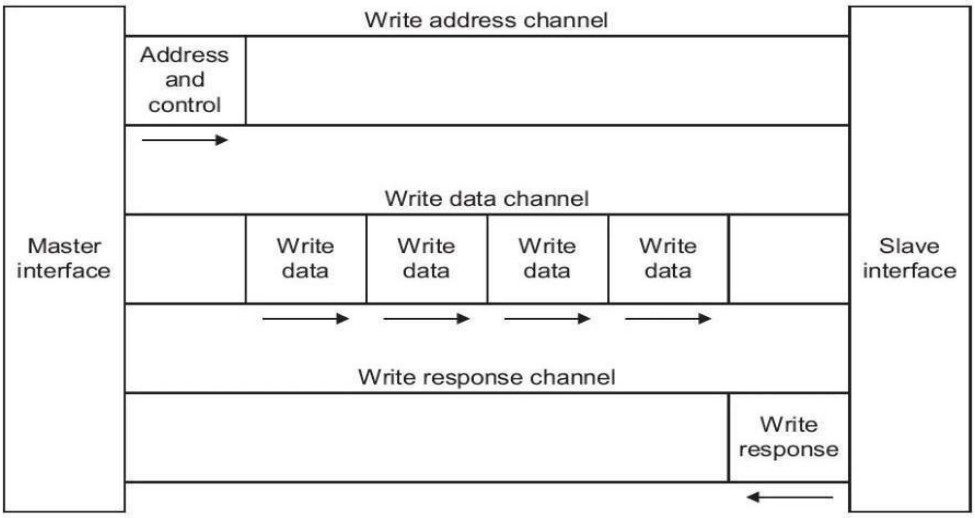

Figure 6 Channel Architecture of Write

3.2.4 Read Address Channel

The read address channel transfers address and control information from the master to the slave for read operations. Similar to the write address channel, it includes signals defining the starting address, burst

length, burst size, burst type, and transaction identification[10]. The handshake mechanism based on address valid and address ready signals ensures proper synchronization. Once the address phase is accepted by the slave, it processes the request and prepares the corresponding read data. This channel initiates the read transaction but does not carry the actual data.

3.2.5 Read Data Channel

The read data channel is used to transfer requested data from the slave device to the master device. It carries different types of signals, such as data signals, response signals, identification signals, and a signal to show when the last transfer in a burst has

occurred. Each data beat is sent using a valid and ready handshake mechanism. The response signal tells us whether the read operation was successful or if there was an error. In cases of burst transactions, multiple data beats are sent one after another, with the final signal marking the end of the burst. This read data channel makes sure that the requested information is delivered correctly, while also keeping everything in line with the protocol and ensuring data integrity.

Together, these five independent channels form the foundation of AXI communication, enabling efficient, scalable, and high performance data transfer in modern System on Chip architectures[8].

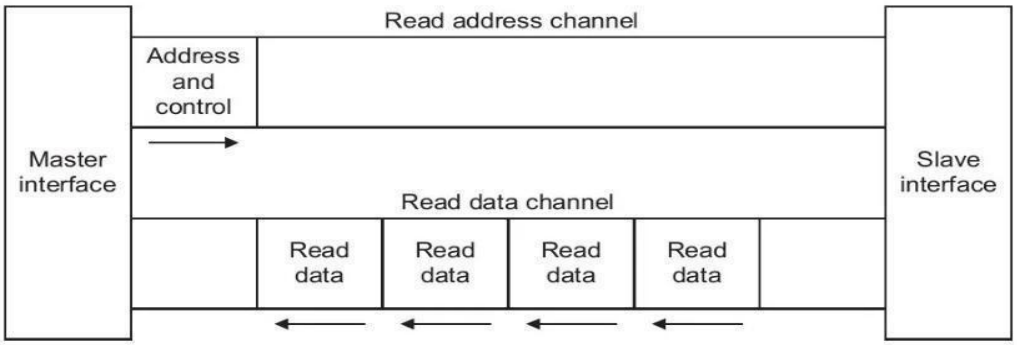

Figure 7 Channel Architecture of Read

3.3 AXI Transaction Types

AXI supports different types of transactions to provide flexibility and efficiency in data transfer between master and slave devices. Transactions can be categorized based on the number of data transfers and the address progression pattern. By supporting both simple and complex transfer mechanisms, AXI enables efficient handling of control accesses as well as high bandwidth data movement. The main transaction types include single transfers and burst transfers, with different burst modes defined for address behavior[12].

3.3.1 Single Transfers

A single transfer consists of one address phase followed by a single data transfer. In this type of transaction, the burst length is defined as one, meaning only one data beat

is exchanged between master and slave. Single transfers are typically used for control register access, status updates, or configuration operations where only a small amount of data is required. Since only one data beat is involved, the transaction is simple and completes quickly. However, using multiple single transfers for large data movement is inefficient because each transfer requires a separate address phase, increasing overhead and reducing bandwidth utilization[10].

3.3.2 Burst Transfers

Burst transfers allow multiple data beats to be transferred using a single address phase. In this case, the master provides the starting address along with burst length and burst size information. The slave then transfers a sequence of data beats corresponding to the defined burst parameters. Burst transfers improve efficiency by reducing address overhead and enabling continuous data flow[12]. They are widely used for memory access operations, cache line transfers, and high speed data streaming. The burst length specifies the number of data beats in the sequence, while the transfer size determines the number of bytes per beat. Proper handling of burst counters, last transfer indication, and response generation is essential for correct implementation..

3.3.3 Fixed Increment and Wrap Bursts

AXI defines different burst types based on how the address changes during a burst transaction. For every data beat in a fixed burst, the address stays the same. For repeated access to the same memory region, like in peripheral register writes, this type is helpful. After every data beat in an increment burst, the address grows by the transfer size. Because it effectively transfers blocks of contiguous data, this is the most popular burst type for sequential memory access [13]. The address increases during a wrap burst until it hits a predetermined boundary, at which point it wraps back to the beginning boundary address. In cache line operations, where data must stay aligned within a fixed memory boundary, wrap bursts are especially helpful. For AXI-based digital IP to retain data integrity and protocol compliance, various burst kinds must be implemented correctly.

3.4 Handshake Mechanism and Timing

The AXI protocol uses a handshake based flow control mechanism to ensure reliable and synchronized data transfer between master and slave devices. Each of the five independent channels operates using two primary control signals, namely valid and ready. The source of information asserts the valid signal when address, data, or response information is available. The destination asserts the ready signal when it is capable of accepting the information. A transfer occurs only in the clock cycle where both valid and ready are asserted simultaneously. This simple yet powerful mechanism eliminates the need for complex global control and allows flexible communication between components operating at different internal latencies[7]. One of the key advantages of this handshake mechanism is that it supports back pressure. Either the master or the slave can delay a transfer by deasserting the ready signal, thereby inserting wait cycles without violating protocol rules. Similarly, the source can delay sending information by holding the valid signal low until data is prepared[3]. This flexibility enables the interconnect to work with components that have different processing speeds, memory access times, or even pipeline depths. Because of this, AXI can handle communication quite well in high-performance systems—where various modules might show differing timing characteristics. From a timing perspective, AXI is fully synchronous and all signal transitions occur with respect to a common clock. The protocol requires that once the valid signal is asserted, it must remain asserted until the handshake is completed. This ensures data stability and prevents information loss. Data and control signals must remain stable during the cycle in which valid is high and ready is low. After a successful handshake, the sender may update signals for the next transfer. Proper timing behavior is critical for maintaining data integrity, especially during burst transactions where multiple data beats are transferred sequentially [5].

3.5 Description of the Digital IP Under Test

The digital IP selected for this thesis is an AXI based slave module designed to interface with a master in a System on Chip environment. The IP implements the required AXI protocol channels to support both read and write transactions. It is developed at the register transfer level and is configurable in terms of data width, address width, and

burst length support. The primary function of the IP is to receive address and control information from the master, process the corresponding data transfers, and generate appropriate response signals in compliance with AXI protocol specifications.

For write operations, the IP accepts write address and write data from the master through their respective channels. It stores the incoming data into an internal memory or register block based on the decoded address. Burst transfers are supported by internally maintaining counters to track the number of data beats and by generating proper termination signals for the final transfer in a burst. After completing the write operation, the IP generates a write response indicating successful completion or error status depending on address validity and access conditions[14].

For read operations, the IP receives the read address and control signals from the master and retrieves the requested data from internal storage. It then sends the data back through the read data channel along with appropriate response information. In burst read transactions, multiple data beats are transmitted sequentially, and the last signal indicates completion of the burst. The IP ensures correct address progression for increment and wrap burst types and maintains data consistency across transactions.

The design includes logic to handle handshake signals correctly on all five channels, allowing insertion of wait states when necessary. It also incorporates error handling mechanisms to generate error responses in cases such as invalid address access or unsupported transfer types. The functionality of the IP strictly follows AXI protocol timing and control rules, making it suitable for integration into larger SoC systems.

The verification of this digital IP focuses on validating correct transaction handling, protocol compliance, burst management, response generation, and robustness under corner case scenarios. A comprehensive verification environment is developed to ensure that the IP performs reliably under various configurations and traffic conditions[14][4].

3.6 Functional Specifications of the IP

The functional specification of the digital IP is defined according to the AXI4 Lite protocol, which is a simplified subset of AXI intended for low complexity control-oriented applications. The IP functions as an AXI4 Lite slave and supports single beat

read and write transactions without burst capability. The design is parameterized for configurable data width and address width, typically supporting thirty two bit data transfers and aligned address access. Since AXI4 Lite does not support burst transfers

or transaction identifiers, the implementation is simpler compared to full AXI, but strict compliance with protocol timing and handshake rules remains essential.[11][14] For write operations, the IP shall accept a valid write address and corresponding write data through separate address and data channels. Both channels operate independently using valid and ready handshake signals. The IP shall capture the address and data when the handshake is completed and store the data in the targeted internal register or memory location. After successful completion of the write transaction, the IP shall generate a write response indicating either successful operation or an error condition if the address is invalid or outside the defined address range.

For read operations, the IP shall accept a valid read address and, upon successful handshake, retrieve the corresponding data from internal storage. The read data shall be transmitted to the master along with a response signal indicating success or error. Since AXI4 Lite supports only single transfers, each read or write request corresponds to exactly one data transfer, simplifying internal control logic. However, the IP must still ensure correct synchronization of address, data, and response channels.[15] The IP shall strictly implement the valid and ready handshake mechanism on all five AXI4 Lite channels, namely write address, write data, write response, read address, and read data channels. It shall allow insertion of wait states by controlling the ready signals, thereby supporting flexible timing behavior. All signals shall operate synchronously with the system clock, and a reset signal shall initialize all internal registers and outputs to defined default values.[15] Error handling is really important when it comes to the functional specification. The IP needs to catch any invalid address accesses, any misaligned transactions (unless they're not supported), and cases of unauthorized access. When these situations happen, it should create the right error response as per the AXI4 Lite protocol. These specifications basically act as a reference for verification, making sure that the IP works correctly and follows all the AXI4 Lite protocol requirements.

Chapter 4: Verification Methodology Using SystemVerilog

4.1 Verification Strategy and Planning

The verification strategy for the AXI4 Lite-based digital IP is aimed at ensuring complete functional validation and strict protocol compliance through a structured and coverage-driven approach. Given that AXI4 Lite supports single-beat read and write transactions with independent channels, the plan we follow focuses on validating how well address, data, and response phases are handled under various timing conditions. This strategy puts an emphasis on using constrained random verification with SystemVerilog to explore different combinations of valid addresses, data patterns, and handshake scenarios. Basically, the main goal is to achieve high functional coverage while efficiently detecting corner cases and functional bugs. The first step in our verification planning is to take a good look at the functional specification of the IP block and find all the features that we need to verify. This includes things like write operations, read operations, handshake behavior, response generation, reset functionality, and how we handle errors when there's invalid address access. We put together a thorough verification plan that links each functional requirement to specific test scenarios and coverage points. This way helps us keep track of how the design specs connect to our verification activities.

As part of this strategy, we develop a modular testbench architecture that has transaction generators, drivers, monitors, and scoreboards. We use constrained random stimulus to create a mix of read and write transactions while staying within the valid protocol limits. We also set up functional coverage models to see how well we're covering things like address ranges, data patterns, response types, and timing variations. In addition, we take a closer look at simulation results and coverage reports on an ongoing basis to identify any scenarios we might be missing, and we adjust our constraints accordingly keeping in mind our aim for coverage closure.

The first step in our verification planning is to take a close look at the functional specifications of the Intellectual Property (IP). We have to identify all the features that we need to verify, which includes things like write operations, read operations, handshake behavior, response generation, reset functionality, and how errors are handled when an invalid address is accessed. As part of this strategy, we build a modular testbench architecture. This setup includes transaction generators, drivers, monitors, and scoreboards. We make use of constrained random stimulus to generate a mix of read and write transactions, all while staying within valid protocol limits. Additionally, we define functional coverage models to see how well we're covering address ranges, data patterns, response types, and timing variations. We also look over simulation results and coverage reports repeatedly to spot any missing scenarios and tweak our constraints, all in pursuit of coverage closure.

4.2 Testbench Architecture

The testbench architecture for verifying the AXI4 Lite based digital IP is designed to be modular, reusable, and scalable. It is developed using SystemVerilog and follows a transaction based verification approach[17]. The architecture separates stimulus generation, signal driving, monitoring, and checking into independent components, which improves clarity and maintainability. The design under test is instantiated within the testbench and connected through a SystemVerilog interface that encapsulates all AXI4 Lite signals. This interface simplifies connectivity and provides a structured way to manage communication between the testbench and the IP. A stimulus generator, driver, monitor, scoreboard, and coverage collector make up the top level of the testbench. High-level transaction objects that represent AXI4 Lite read and write operations are produced by the stimulus generator [18]. Address, data, and transaction type are among the fields seen in these transactions. Using the appropriate valid and ready handshake criteria, the driver transforms these transaction level objects into signal level activity on the AXI4 Lite interface. Complex situations can be created without directly modifying low-level signals thanks to this abstraction..

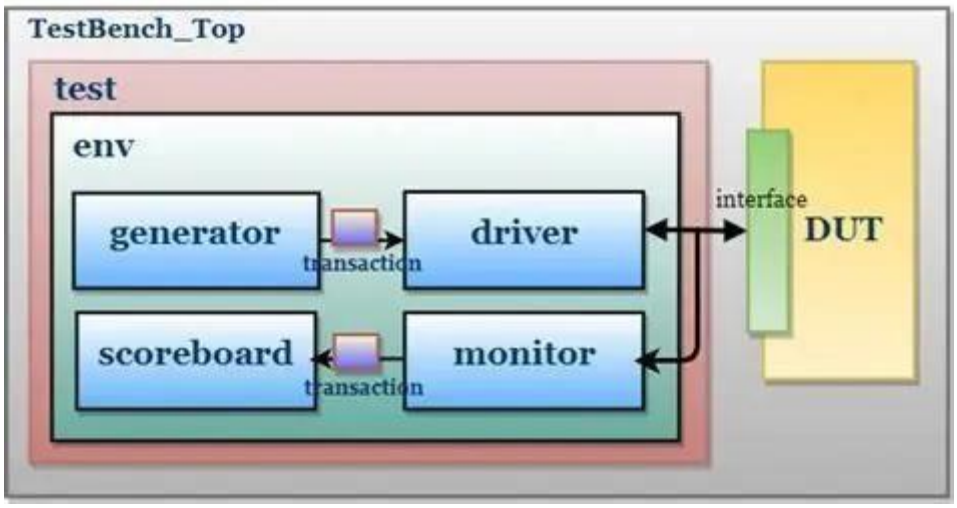

Figure 8 Testbench of SystemVerilog

The monitor observes signal activity on the AXI4 Lite interface and reconstructs transactions from the captured signals. It ensures that both address and data phases are correctly sampled and forwarded to the scoreboard[19]. The scoreboard compares the observed behavior of the design with expected results generated from a reference memory model. Any mismatch between expected and actual responses is reported as an error. This checking mechanism verifies functional correctness of read and write operations.

Functional coverage components are integrated within the testbench to measure how thoroughly different scenarios are exercised. Coverage models track variations in address access, data values, response types, and timing conditions[19]. The modular nature of architecture allows easy modification or extension for future enhancements. Overall, the testbench architecture provides a structured environment for systematic and comprehensive verification of the AXI4 Lite digital IP.

4.3 Interface Design for AXI

The AXI4 Lite interface design plays a crucial role in connecting the design under test with the verification environment. A SystemVerilog interface is used to group all

related AXI4 Lite signals into a single construct, improving readability and simplifying connectivity[20]. Since AXI4 Lite consists of five independent channels, the interface includes signals for write address, write data, write response, read address, and read data channels. Using an interface avoids repetitive signal declarations in the testbench and ensures consistent signal access across different verification components. The interface includes address, data, control, and handshake signals, along with clock and reset signals, which are necessary to keep everything in sync. Modports are set up to clearly show which direction the signals are going for the master and slave connections. This kind of organization not only makes the code cleaner, but also helps to avoid any accidental misuse of signals. The driver connects through the master modport, while the design under test connects through the slave modport. This structured approach really boosts the reusability and modularity of the verification environment. In this interface, all AXI4 Lite signals are grouped in a logical way, and the modports define the signal directions for both the master and slave roles. This ensures a good separation between the verification components and the design under test. Also, if needed, the interface can include tasks or clocking blocks for better timing control. Proper interface design improves maintainability, reduces coding errors, and supports scalable verification of AXI4 Lite based digital IP.

4.4 Transaction Level Modeling

Transaction Level Modeling is used in the verification environment to represent AXI4 Lite operations as high level objects instead of manipulating low level signals directly[22]. This abstraction simplifies stimulus generation, improves readability, and enhances reusability of the testbench. In AXI4 Lite, transactions are limited to single beat read and write operations, making it convenient to model each transfer as an object containing fields such as address, data, transaction type, and expected response. By working at the transaction level, complex test scenarios can be created without directly handling handshake timing at the signal level.A transaction class is defined using SystemVerilog class constructs. The class contains random variables for address and write data, along with constraints to ensure valid address ranges and alignment requirements[23]. The transaction type is defined to distinguish between read and write

operations. Additional fields may be included to store observed read data and response values for comparison in the scoreboard.

Randomization enables automatic generation of diverse scenarios within defined constraints, supporting coverage driven verification..

In this model, the addr and wdata fields are randomized for write operations, while rdata is used to store data received during read transactions. The alignment constraint ensures that addresses follow word boundary rules, and the address range constraint restricts transactions to valid memory locations. The write variable determines whether the transaction is a read or write operation[25].The driver gets these transaction objects and then converts them into signal-level activity on the AXI4 Lite interface. Meanwhile, the monitor takes the observed signals to reconstruct similar transaction objects, which it then sends to the scoreboard for verification. By separating transaction generation from signal-level implementation, Transaction Level Modeling (TLM) makes it easier to manage and scale the verification process. This method helps to cut down code complexity, supports constrained random verification, and boosts the overall efficiency of the verification environment for digital IP based on AXI4 Lite.

4.5 Driver Implementation

4.5.1 Overview

The driver is a key BFM component in the verification environment because it acts as the link between the abstract transaction layer and the actual pin-level AXI4-Lite interface. It receives transaction requests from the testbench and converts them into the correct sequence of address, data, and control signal activity required by the protocol. While doing this, the driver makes sure that all AXI4-Lite rules are followed properly, especially the VALID/READY handshake mechanism, so that data is transferred only when both sides are ready[26]. It also respects timing details given in the transaction, such as delays between operations, which helps in creating realistic test conditions. In addition, the driver monitors abnormal situations like handshake failures, timeouts, or unexpected responses, and reports them in a controlled manner. By doing all of this,

the driver ensures that the DUT is stimulated accurately, consistently, and in accordance with the AXI4-Lite specification.

4.5.2 Architecture and Design Approach

The testbench uses task-based BFM approach rather than class-based driver for Icarus Verilog compatibility. Two main tasks implement the core functionality The overall architecture of the verification environment is built in a modular and layered manner to support effective and scalable validation of the AXI4-Lite interface[27]. The environment is divided into independent components, each responsible for a specific verification task. Typical blocks include the transaction generator, driver, monitor, scoreboard, and environment controller. This separation of responsibilities improves code reusability, simplifies debugging, and makes the verification flow easier to extend for future requirements.

The design approach begins with the definition of high-level test scenarios, which are then converted into transaction-level stimulus[28]. These transactions are constrained-randomized to ensure protocol compliance while still exploring a wide range of functional cases and corner conditions. The driver interprets each transaction and converts it into the corresponding signal activity on the interface. In parallel, the monitor observes the bus behavior and collects the response information for checking. The scoreboard compares the expected and actual outcomes to detect mismatches and verify correctness. By following this structured approach, the environment provides an efficient and organized method for validating AXI4-Lite functionality.

4.5.3 Write Transaction Implementation

The Transaction Implementation section presents the transaction class as a high-level representation of AXI4-Lite behavior. It contains the key information needed to describe a bus operation, such as the address, write data, read data, transfer type, and control-related signals. The class may also include protocol-specific parameters like delays, response information, and operating mode so that the generated stimulus matches the intended transaction behavior[29]. When burst-related features are relevant, the corresponding burst attributes can also be stored in the transaction object. This makes the class a compact and reusable container for describing AXI4-Lite transfers.

Another important aspect of the transaction class is its support for constrained random generation, which helps produce a broad set of test cases with varied input values. This improves verification quality by exercising different functional scenarios and edge conditions[30]. The randomized transaction is then passed to the driver, which interprets its fields and converts them into the appropriate bus activity according to the AXI protocol rules. Therefore, the transaction class acts as the core data structure used to generate stimulus in the constrained-random verification flow.

Key Features:

The AXI4-Lite write transaction is implemented to allow AWVALID and WVALID to be asserted at the same time, which is consistent with the protocol rules. Since the address and data phases can be completed independently, fork/join is used to monitor both handshakes concurrently[8]. Once each handshake is completed, the related signals are deasserted to preserve correct bus operation. The corresponding write response is obtained from the BRESP signal, which indicates the result of the transfer. The use of wait() statements also helps prevent uncontrolled progression in simulation by ensuring that the process continues only when the required handshake condition occurs.

4.5.4 Read Transaction Implementation

The read transaction is meant to simulate AXI4 Lite read transfers at a basic level within the verification environment. It has all the necessary details to start and finish a read operation, like the address, control signals, and some other protocol-related parameters.

To kick off the process, you first place the read address on the bus and assert the ARVALID signal. After that, you wait for the ARREADY handshake from the slave before moving on to the data phase. Once the address is accepted, you'll keep an eye on the read data through the RVALID signal, and you'll capture the corresponding RDATA and RRESP values for checking.

This implementation ensures that the read operation follows the correct AXI4-Lite sequence and remains synchronized with the slave response[28]. The driver is responsible for applying the transaction fields to the interface, while the monitor observes the resulting bus activity for verification purposes. By separating transaction description from signal execution, the read transaction provides a clean and reusable

structure for generating and validating read scenarios in the verification flow.

Key Features:

The read transaction starts by asserting ARVALID along with the address and protection signals to initiate the read address phase. It then waits for the slave to assert ARREADY, confirming that the address has been accepted. Once the address handshake is complete, RREADY is asserted so that the master can accept the incoming read data[31]. During this phase, both RDATA and RRESP are captured to verify the returned value and response status. This ordering of events follows the AXI4 Lite protocol and ensures that the read operation is executed correctly and in a controlled manner.

4.5.5 Driver Usage Pattern in Test

From the testbench:

```
// Write 0xDEAD_BEEF to register 0
axi_write(32'h0000_0000, 32'hDEAD_BEEF, 4'b1111, 3'b000, resp);
scb.record_write(32'h0000_0000, 32'hDEAD_BEEF, 4'b1111);
$display("[%0t] DIR_WR: addr=0x00000000 data=0xDEADBEEF resp=%0b", $time, resp);
// Read back register 0
axi_read(32'h0000_0000, 3'b000, rd_data, resp);
scb.check_read(32'h0000_0000, rd_data, resp);
$display("[%0t] DIR_RD: addr=0x00000000 data=0x%08h resp=%0b", $time, rd_data, resp);
```

The driver integrates seamlessly with the scoreboard for immediate transaction recording and verification.

4.6 Monitor Implementation

4.6.1 Overview

The monitor is a passive observation component that captures transactions on the AXI4-Lite bus without interfering with normal bus activity. It correlates signals across the

different channels to reconstruct complete transactions, while also timestamping signal transitions for latency analysis. In addition, the monitor detects protocol violations and other anomalies during simulation[32]. The collected transaction information is then made available to the scoreboard and coverage collectors, enabling detailed checking and verification analysis..

4.6.2 Monitoring Architecture

The monitoring process in the constrained-random environment is closely tied to the scoreboard so that bus activity can be tracked accurately. As soon as a transaction is completed, it is captured and stored, allowing the scoreboard to maintain an up-to-date representation of the observed behavior. Write transactions are reflected in the reference model memory to preserve the expected data state throughout simulation[32]. Read transactions are then checked against this stored reference information to validate the correctness of the returned data. In parallel, all transactions are recorded for logging and waveform correlation, which helps during debugging and improves overall visibility of the verification activity.

4.6.3 Scoreboard-Based Monitoring

Scoreboard based monitoring provides a solid way to check actual AXI4 Lite transactions against the expected results saved in a reference model. As the monitor catches bus activity, it sends that information to the scoreboard, where it gets compared with what we anticipated would happen. For write operations, the reference memory gets updated to show the new data that's been accepted, whereas during read operations, we check the results against the stored values to make sure everything's correct. This method helps us find mismatches, verify compliance with the protocol, and gives a clear pass or fail result for each transaction.

4.6.4 Monitoring Features

Byte strobe processing is carried out by masking each byte lane so that only the required bytes are written to the reference memory. This makes it possible to support partial writes while leaving the unaffected bytes unchanged. Response handling includes capturing BRESP for write transfers and RRESP for read transfers, with error conditions such as DECERR being treated appropriately[34]. At the same time, the verification flow maintains pass/fail status by increasing pass_cnt when the read value

matches the expected result and fail_cnt when a discrepancy is detected, which provides a clear measure of transaction correctness.

4.7 Transaction Generation and Stimulus

4.7.1 Transaction Class

The transaction class serves as a key part of the verification architecture, providing a structured way to model the individual bus operations. In a SystemVerilog testbench, this class usually has important attributes like the address, the data payload, control signals, and the type of transfer that's being executed. By capturing these elements in a single object, the verification environment becomes more organized, reusable, and easier to extend. In addition, the transaction class supports randomized stimulus generation and facilitates checking mechanisms by offering a consistent high-level representation of each operation. As a result, it plays an important role in improving both the clarity and effectiveness of the overall verification process.

4.7.2 Constraints Applied

The stimulus generation is configured to produce a realistic traffic distribution, with write operations accounting for 60% of the transactions and read operations accounting for the remaining 40%. Address generation is restricted to 4-byte-aligned locations using addr = $urandom_range(15, 0) * 4, thereby ensuring that all accesses remain word-aligned within the valid register space. This corresponds to register indices in the range of 0 to 15 and an overall address span from 0x00 to 0x3C. For write transactions, the strobe value is constrained between 1 and 15 so that at least one byte lane is always active, while read transactions are assigned a fixed strobe value of 4'b1111. Furthermore, the inter transaction delay is randomized between 0 and 5 clock cycles, enabling the verification environment to exercise both back-to-back and spaced transaction scenarios.

4.8 Test Execution Flow

4.8.1 Test Phases

The verification strategy is split into four distinct test phases, each one aimed at checking a specific aspect of the register interface and how it behaves. In the first

phase, we perform a directed sanity test, where we write a known value to a selected register and then read it back, which helps us establish confidence in the basic read and write functions.

The second phase uses a sequence of constrained-random transactions. This lets the testbench explore a wider range of legal address, data, and control combinations, while still keeping within realistic operational limits. Moving on to the third phase, we introduce a back to back write stress pattern across the entire register set, without any delay between the transfers. This is meant to evaluate how robust the write path is under continuous activity. Finally, the fourth phase involves a sequential read sweep over all the registers to confirm that values we wrote earlier are still there and can be retrieved without any corruption. All these phases together offer a structured and progressive way to handle verification, starting from basic functionality, moving to randomized testing, stress testing, and then validating the final data.

4.8.2 Complete Test Sequence

The overall testbench flow is implemented inside a single initial block that governs the verification process from start to finish. At the beginning of simulation, the necessary local variables are created and the scoreboard is initialized so that transaction results can be monitored and checked during execution. The interface signals controlled by the master are set to their inactive states first, so we can have a clear starting point. After we initialize everything, we apply a reset for a few clock cycles and then let it go. This way, the design we're testing starts up from a properly configured state. The verification sequence goes through phases. First, it starts with a directed test, then moves to a constrained random sequence, followed by the back to back write phase, and it wraps up with the read back sweep. Once we finish these steps, we let the simulation run for a bit before we generate the scoreboard report, which gives us a summary of the whole run. This organized structure really helps us have a clear and repeatable method for end to end verification.

Chapter 5: Constrained Random Stimulus Generation

5.1 Randomization Strategy

5.1.1 Probability Distribution

The environment is configured to generate a realistic traffic pattern with 60% write transactions and 40% read transactions. Address generation uses a random selection method that distributes accesses uniformly across 16 registers, ensuring broad coverage of the available register space. Random data values are applied over the full 32-bit range to exercise a wide variety of input conditions. In addition, strobe variation is introduced using 15 valid combinations for write operations, with values ranging from 1 to 15, so that different byte-lane activity patterns can be verified.

5.2 Test Scenarios and Coverage

5.2.1 Phase 1: Directed Sanity

This test is intended to check the fundamental operation of the design using a fixed register address and a known data pattern. The address 0x00000000 is chosen for Register 0, and the value 0xDEADBEEF is written with a full strobe of 4'b1111 so that every byte lane is enabled. After the write transfer, a read transaction is carried out to verify that the same data is returned correctly from the selected register.Expected Result: Data written and read back correctly

5.2.2 Phase 2: Constrained Random (50 Transactions)

The coverage objectives of the verification environment are defined to ensure wide functional exploration of the design. All 16 registers are expected to be accessed, which is achievable with a high probability when 50 transactions are generated. The stimulus is further extended by exercising the 15 valid strobe combinations, thereby covering different byte-lane activity patterns[35]. Mixed write and read sequences are included to verify both directions of data transfer, while inter-transaction delays are randomized between 0 and 5 cycles to test both immediate and delayed operations. In addition, data values are generated across the full random range to increase stimulus diversity[30].

These goals are implemented using NUM_RAND_TXNS = 50, with write operations assigned a probability of 60% and read operations a probability of 40%.

5.2.3 Phase 3: Back-to-Back Stress

This test is designed to create a stress condition by programming all 16 registers one after another with

no delay between transactions. The data value for each register is generated using the pattern 0xA0000000 + register_index, and 4'b1111 is applied as the strobe so that all byte lanes are written[22]. Running the sequence continuously in this way checks that the design can sustain consecutive write operations, keeps each register update independent, and maintains correct data storage even under heavy activity.

5.2.4 Phase 4: Read Sweep

This test was done to check if all 16 registers kept their contents correctly after we wrote to them. We read each register one by one and compared the values we got with what we expected, to make sure nothing changed. This process showed that the information we stored stayed stable across the whole register space. It also helped verify that the address-decoding logic was working properly, since every read had to reach the intended register.

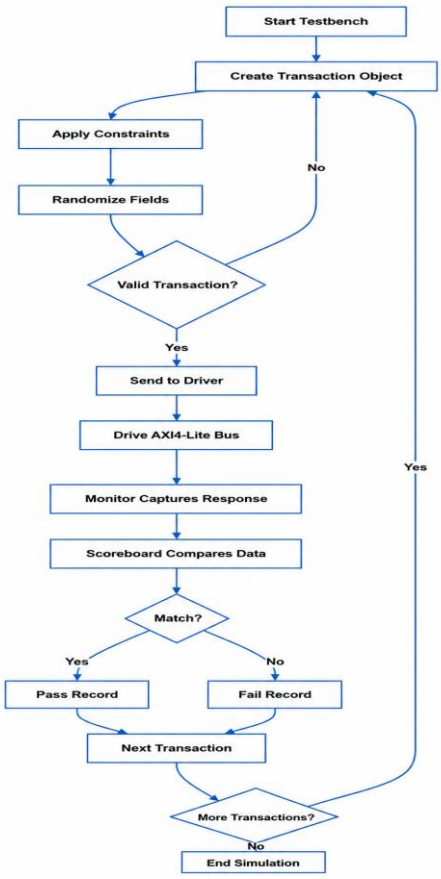

Figure 9: Constrained Random Verification Flow

If the decoding had been incorrect, the retrieved values would not have matched the programmed ones. Because the procedure involved only reading data, no strobe signals were necessary. The test was mainly about retrieving and verifying data, instead of changing the contents of the registers. By checking each register in order, the test provided a clear picture of how the device stored information. It also helped to find any possible problems, like data corruption, selecting the wrong option, or accidentally overwriting data. In general, the results showed that the registers reliably retained their information, and that each part of the register map was accessed correctly.

5.3 Error Scenarios and Edge Cases

5.3.1 Implicit Error Testing

The applied address and strobe constraints prevent certain invalid scenarios from being generated in the later verification phases[18]. For instance, addresses beyond 0x3C are not produced because the address space is deliberately restricted, although such out-of-range cases could be introduced by relaxing the constraint set if needed. Likewise, unaligned accesses are excluded since the address generation method addr = $urandom_range(15, 0) * 4 guarantees 4-byte alignment and therefore keeps address[1:0] = 2'b00. In the same manner, zero strobe values are avoided because the write strobe is constrained through strb = $urandom_range(15, 1), which ensures that at least one byte lane remains active for every write transfer.

5.3.2 Future Enhancement: Extended Coverage

For comprehensive error testing, could add constrained scenarios:

systemverilog

```
// Scenario: Out-of-range addresses
constraint addr_out_of_range {
   addr inside {32'h0000_0040, 32'h0000_1000, 32'hFFFF_FFFF};}
// Scenario: Unaligned addresses
constraint addr_unaligned {
   addr inside {32'h0000_0001, 32'h0000_0002, 32'h0000_0003};}
// Scenario: All-zero strobes
```

```
constraint strb_all_zero {
   strb == 4'b0000;}
```

5.4 Randomization Seed Control

5.4.1 Reproducibility

Seeding allows reproduction of test failures:

```
// Set seed before test
initial begin
   // Use fixed seed for reproducibility
   void'($urandom(12345));
   // Or use seed from command line:
   // $urandom($value$plusargs("SEED=", seed))
End
```

5.4.2 Regression Testing

Multiple simulation seeds can be swept to generate different randomized transaction sequences while still preserving the same set of constraints. For example, Run 0 may use Seed = 1, Run 1 may use Seed = 2, and Run 99 may use Seed = 100. Although each seed produces a different ordering and combination of transactions, the underlying stimulus rules remain unchanged, ensuring that all runs are valid and comparable.

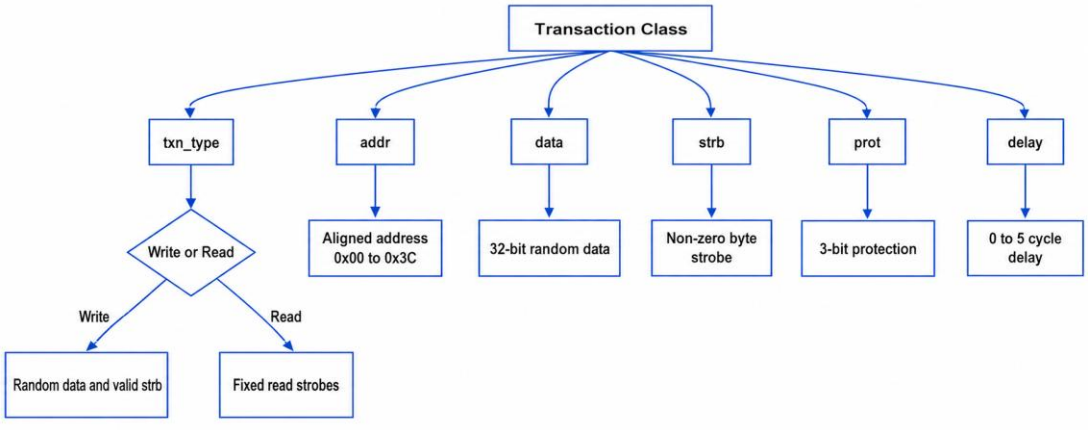

Figure 10: Transaction Randomization Structure

5.5 Stimulus Quality Metrics

5.5.1 Coverage Metrics

The verification plan outlines specific coverage targets for registers, strobes, and timing behavior during the various testing phases. It's important to have these targets clearly defined to ensure a thorough evaluation of the system.. For register coverage, the objective is to access all 16 registers at least once; this is expected with high probability in Phase 2 using 50 randomized transactions, while Phase 3 guarantees complete coverage through explicit writes to every register[28]. Strobe coverage is aimed at exercising a broad range of byte-lane combinations, with Phase 2 likely covering a substantial portion of the 15 valid patterns through random stimulus, and Phase 3 achieving full coverage by using 4'b1111 for all write operations. DRelay coverage is intended to confirm both immediate and delayed transfers.

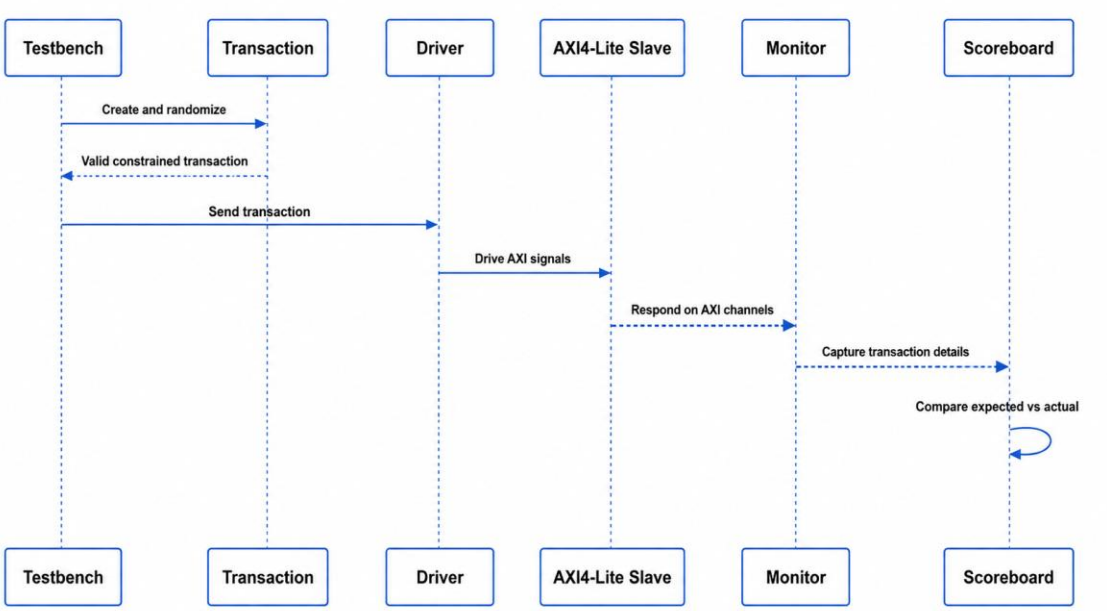

Figure 11: Stimulus Generation and Execution Flow

5.5.2 Test Completeness

The current implementation aims to meet the main verification objectives using a phased approach. Phase 1 focuses on validating basic functionality. Then, in Phase 2, we introduce some randomized stimuli to extend the testing. Phase 3 looks at stress

conditions, simulating continuous transaction activity. Finally, Phase 4 checks data persistence to make sure that stored register values stay intact during read operations. However, it's worth noting that error scenarios are only partially covered right now since they're managed indirectly through existing constraints and not through specific negative test cases.

Chapter 6: Functional Coverage and Analysis

6.1 Coverage Objectives

Functional coverage assesses how thoroughly the functionality of a system has been tested and verified. verification environment has exercised the intended design behavior[13]. It includes checking that all valid addresses are accessed, that a variety of data patterns are written and read back, and that different strobe combinations are validated to confirm correct byte-enable operation. Coverage is also used to ensure that both read and write paths are tested, while a range of inter-transaction delays is applied to evaluate timing-related behavior under different conditions.

6.2 Coverage Analysis from Test Execution

6.2.1 Register Address Coverage

In Phase 2, the randomized stimulus distributes 50 transactions across the valid aligned addresses from 0x00 to 0x3C, giving each of the 16 registers an opportunity to be selected. Because of the uniform random selection, it is highly likely that all registers will be exercised, although some may appear more than once. Phase 3 removes this uncertainty by issuing one write to each register in sequence, thereby guaranteeing complete write coverage. Phase 4 then performs one read from every register to verify that the values written in the previous phase remain correctly stored.

6.2.2 Strobe Coverage

In Phase 2, the constrained-random stimulus includes approximately 30 write transactions, corresponding to 60% of the 50 total transactions. During this phase, the strobe values are selected from the range 0x1 to 0xF, and the randomized distribution is intended to promote diversity in the exercised byte-lane patterns. As a result, most strobe combinations are likely to be covered. The valid strobe space consists of 15 combinations in total, including single-byte patterns such as 0x1, 0x2, 0x4, and 0x8, double-byte patterns such as 0x3, 0x5, 0x6, 0x9, 0xA, and 0xC, triple-byte patterns such as 0x7, 0xB, 0xD, and 0xE, and the full-word pattern 0xF. Based on this distribution, Phase 2 is expected to achieve coverage of approximately 70%, or about

10 to 11 of the 15 valid combinations, while Phase 3 provides guaranteed coverage of only the full-word strobe 0xF

6.2.3 Data Value Coverage

The test environment uses different categories of data values to check the design under a variety of conditions. In Phase 1, the fixed pattern 0xDEADBEEF is applied as a known reference to verify the basic transfer path. In Phase 2, we generate values randomly across the full 32 bit range, from 0x0000 0000 to 0xFFFF FFFF. This helps to cover some unusual and boundary cases. Then in Phase 3, we follow a set sequence with values from 0xA000 0000 to 0xA000 000F. This lets us see how the registers react to a more organized set of inputs, and we can check if the bit patterns stay consistent. Using these two phases adds some variety to our tests, which boosts our confidence that the design can handle both the extreme values and the everyday ones correctly,

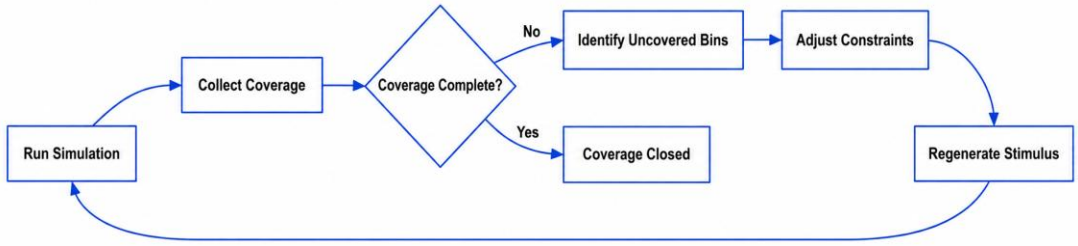

Figure 12: Functional Coverage Closure Loop

6.3 Coverage Reporting

6.3.1 Scoreboard Summary Output

```
============================================================
SCOREBOARD SUMMARY :  PASS = 50 | FAIL = 0
============================================================
>>> TEST PASSED <<<
```

6.3.2 Coverage Metrics Interpretation

The results of the verification run indicate a complete pass, with all write transactions

handled as expected and all read transactions matching the reference model. Read checking includes roughly 36 operations in total, made up of 20 reads from Phase 2 and 16 reads from Phase 4, which confirms that the stored values were preserved correctly during the test. Write checking covers about 46 transactions overall, including 30 writes in Phase 2 and 16 writes in Phase 3, and each register was updated successfully. Overall, these outcomes show that the design responded correctly to both read and write activity throughout the verification flow.

6.4 Coverage Closure Strategy

6.4.1 Current Execution Results

With NUM_RAND_TXNS = 50, the test setup exercises most of the important behavior needed to verify the design. The different phases together cover basic read and write activity, variations in byte strobes, the full set of register addresses, a range of data values, timing differences between transactions, and checks for data retention across sequential accesses. Based on the combination of 50 random transactions along with 16 directed transactions and 16 register-sweep transactions, the expected functional coverage is approximately 85–90%. 6.4.2 Enhancement for Full Coverage

To get coverage of 95% or more, here are a few options you can try:

Option 1: Increase Random Transactions

You could set the number of random transactions to 200. This increases the variety, and it should give you a coverage probability that's over 99% for all the registers.

Option 2: Add Targeted Scenarios

-Scenario A: All Strobe Combinations

You can use this command to write to the register with different strobe combinations:

`axi_write(register_addr, test_data, strb, 3'b000, resp);`

-Scenario B: All Register Addresses

For this, just loop through all the register addresses like this:

```
for (addr = 0; addr < 64; addr += 4) begin axi_write(addr, test_data, 4'b1111, 3'b000, resp);
  end
```

Option 3: Coverage-Driven Generation

```
// Track uncovered register/strobe combinations
// Generate transactions targeting uncovered items
// Iterate until all covered
```

Chapter 7: Simulation Results and Performance Analysis

7.1 Simulation Environment Setup

7.1.1 Tool Configuration

Simulator used: Icarus Verilog in EDA Playground

The timescale utilized is 1ns/1ps.

Clock Period used: 10ns)

7.1.2 Simulation Parameters

```
localparam ADDR_WIDTH = 32;
localparam DATA_WIDTH = 32;
localparam NUM_REGS  = 16;
localparam CLK_PERIOD = 10;          // 100 MHz
localparam NUM_RAND_TXNS = 50;       // number of random transaction
```

7.1.3 Waveform Capture

systemverilog

```
initial begin
   $dumpfile("dump.vcd");
   $dumpvars(0, tb_axi4_lite_top);
end
```

Generates VCD file for waveform analysis:

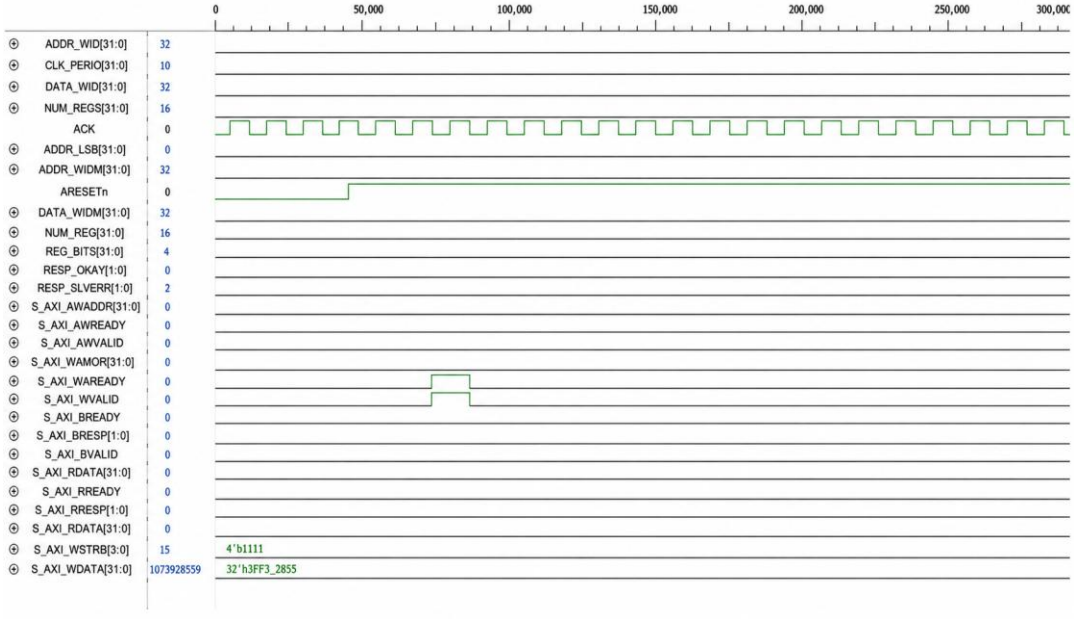

Figure 13 Waveform

7.2 Test Execution Results

7.2.1 Expected Output

Phase 1 Output:

==========

Phase 1: Directed Sanity Write + Read

==========

[TIME] DIR_WR: addr=0x00000000 data=0xDEADBEEF resp=00

[TIME] DIR_RD: addr=0x00000000 data=0xDEADBEEF resp=0

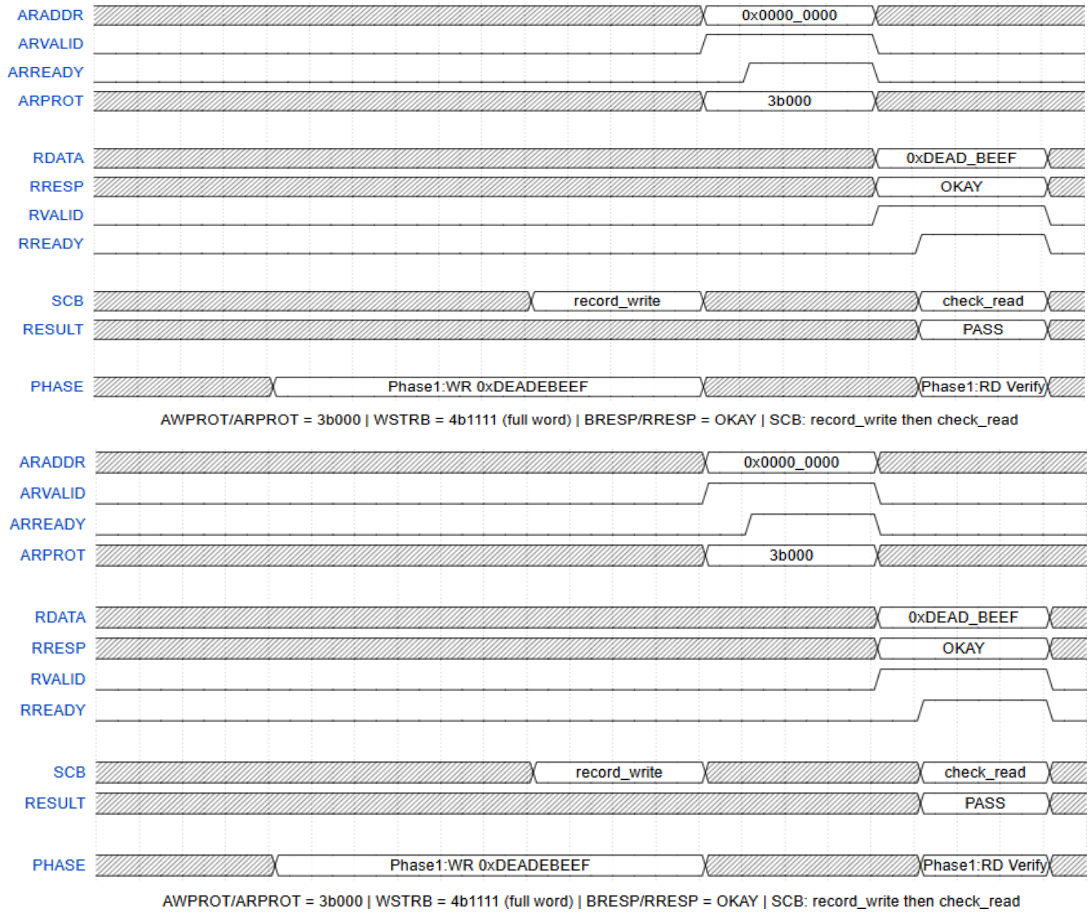

Figure 14 Directed AXI4-Lite write-read check for register 0

Phase 2 Sample Output:

==========

Phase 2: 50 Constrained-Random Transactions

==========

[TIME] TXN: WRITE addr=0x0000001c data=0x12345678 strb=0b1010 delay=2
[TIME] SCOREBOARD: Write addr=0x0000001c data=0x12345678 (strb=1010) -> stored 0x34128976

[TIME] TXN: READ addr=0x00000000 data=0x00000000 strb=1111 delay=0

[TIME] SCOREBOARD: Read addr=0x00000000 data=0xdeadbeef PASS

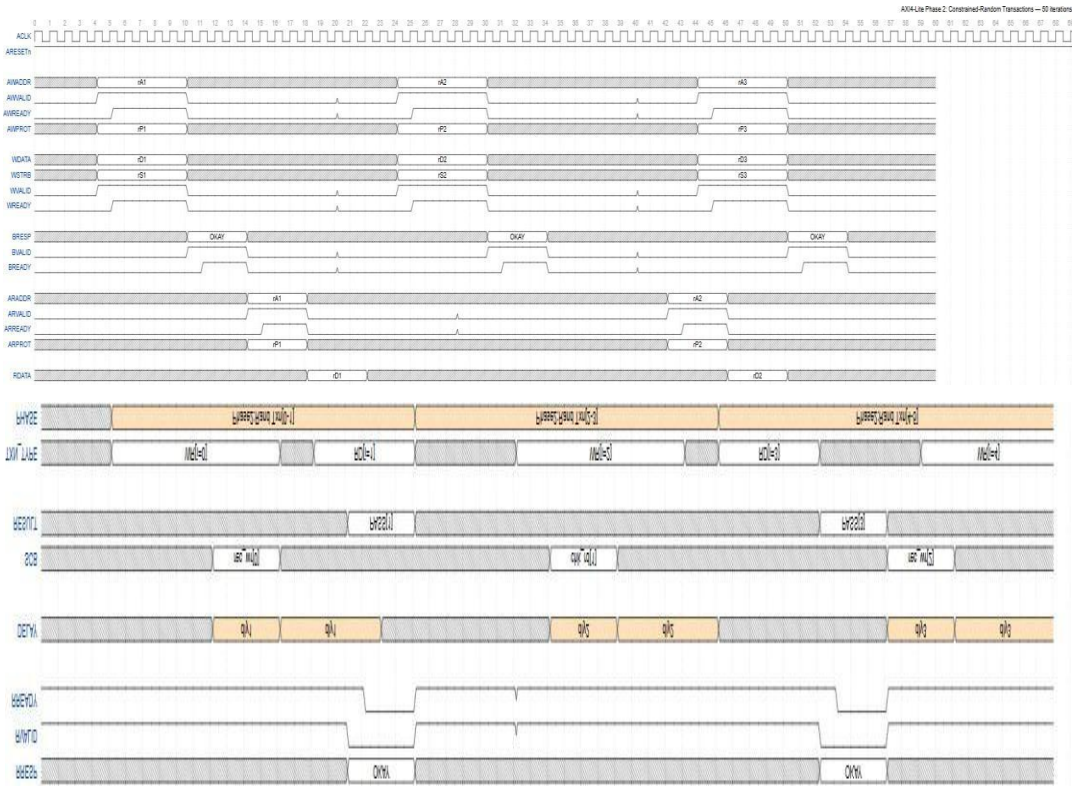

Figure 15 AXI4-Lite Phase 2 constrained-random read and write transactions

Phase 3 Output:

==========

Phase 3: Back-to-Back Writes (all regs)

==========

[TIME] SCOREBOARD: Write addr=0x00000000 data=0xa0000000 (strb=1111) -> stored 0xa0000000

[TIME] SCOREBOARD: Write addr=0x00000004 data=0xa0000001 (strb=1111) -> stored 0xa0000001

[TIME] SCOREBOARD: Write addr=0x0000003c data=0xa000000f (strb=1111) -> stored 0xa000000stored 0xa000000

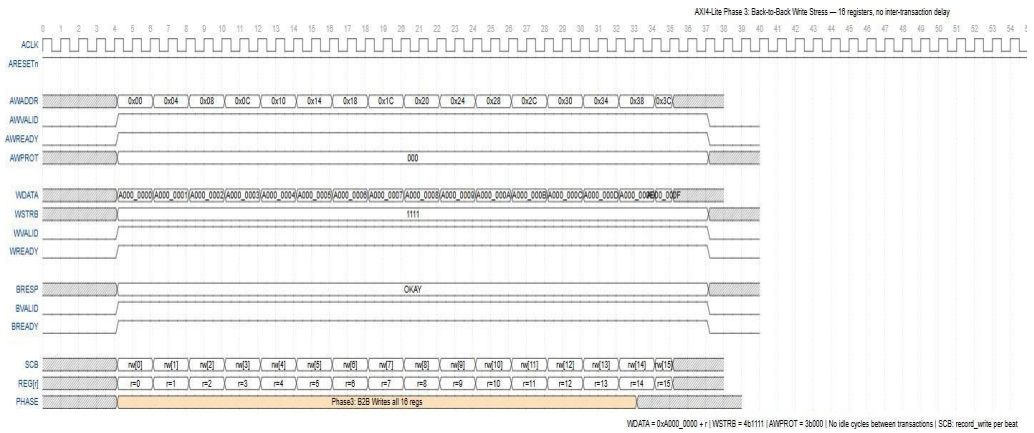

Figure 16 AXI4-Lite Phase 3 write-stress waveform for all 16 registers

==========

Phase 4: Read-Back Sweep (all regs)

==========

[TIME] SCOREBOARD: Read addr=0x00000000 data=0xa0000000 PASS

[TIME] SCOREBOARD: Read addr=0x00000004 data=0xa0000001 PASS

[TIME] SCOREBOARD: Read addr=0x0000003c data=0xa000000f PASS

Final Summary:

==========

SCOREBOARD SUMMARY : PASS = 50 | FAIL = 0

>>> TEST PASSED <<<

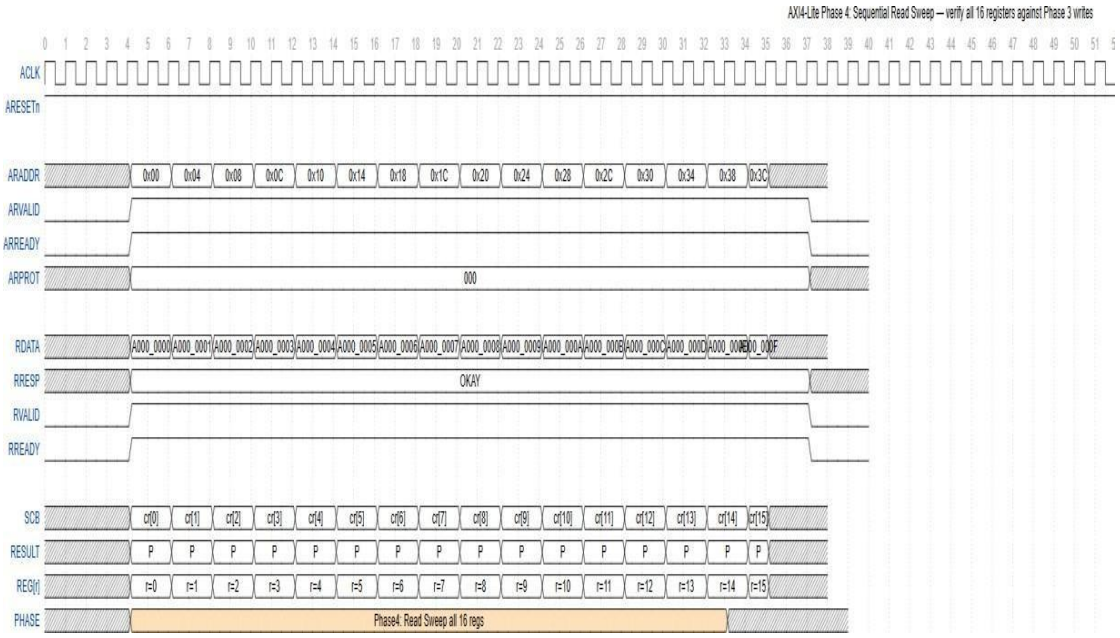

Figure 17 AXI4-Lite read verification waveform showing register contents after write initialization

7.3 Performance Analysis

7.3.1 Simulation Metrics

The simulation included four stages and took around 1.5 µs to complete. The first step acted as a quick sanity check and took roughly 20 ns. The second phase was the most time-consuming part of the test, taking up around 800 ns while processing 50 transactions, with an average latency of about 16 ns per transaction. The third phase consisted of 16 write operations that were completed in around 320 ns, producing an average of roughly 20 ns each write. Similarly, the fourth phase performed 16 read operations in around 320 ns, with an average delay of 20 ns per read.

The system's performance varied based on the kind of transaction. Directed transactions had the greatest pace, hitting 100 Mtxn/s, which equates to one transaction every 10 ns. Random transactions performed somewhat slower, with a throughput of 62.5 Mtxn/s, or one transaction every 16 ns. Stress transactions had the lowest throughput of the three scenarios, at 50 Mtxn/s, equivalent to one transaction every 20 ns. Overall, the findings show that the architecture performed consistently throughout all stages while maintaining a predictable and efficient transaction rate.

7.3.2 Coverage Efficiency

The coverage results indicate an effective distribution of transactions across the design space. For the register coverage metric, 16 registers were exercised using 50 random transactions, and with an average coverage of approximately 15 points, this corresponds to about 3.3 transactions per coverage point. This suggests that the stimulus was sufficient to achieve a reasonably broad exploration of the address space. In addition, the strobe diversity observed during Phase 2 was also favorable: 30 write transactions were expected to contribute to the analysis, resulting in roughly 2 transactions per strobe combination. Such a distribution reflects good variation in write activity and supports a diverse and meaningful coverage campaign[5][8][17].

7.3.3 Scalability Observations

When NUM_RAND_TXNS = 50:

-> Simulation runs complete in less than 2µs

-> Scalable to NUM_RAND_TXNS > 1000 with linear time increase.

-> Effective memory use (<1MB)

7.4 Verification Quality Assessment

7.4.1 Bug Detection Capability

The proposed testbench is designed to identify a range of functional and protocol-related defects within the register interface. Address decoding faults, such as an incorrect register being accessed during a read or write operation, are expected to be revealed during the Phase 4 read sweep, where each location is systematically checked. Errors linked with strobe handling, such as incorrect byte masking, can be discovered during the random write transaction in second phase and validated during readback verification in fourth phase. Any form of data corruption within the transfer path would also be detected during this verification stage, as mismatches between expected and observed values would immediately indicate a fault[16][20]23]. In addition, violations of the handshaking protocol, particularly incorrect VALID/READY sequencing, would cause the wait() process to stall and eventually result in a timeout, thereby flagging a protocol failure. Finally, issues related to register isolation, such as unintended data leakage between registers, would be exposed by the stress-oriented access patterns used in Phases 3 and 4, which repeatedly exercise multiple registers to confirm that each location retains independent and correct behavior

7.4.2 Confidence Level

The implemented testbench provides high confidence in the correctness of the fundamental read and write operations, as these core behaviors are exercised and verified directly through the transaction flow. At the same time, confidence in corner-case handling remains moderate, since the current verification strategy includes only a limited number of explicitly defined error conditions.[13] Nevertheless, the testbench offers good confidence in both register isolation and data integrity, as the repeated access and readback mechanisms help confirm that each register maintains its intended value independently and without unintended corruption.

Chapter 8: Conclusion and Future Scope

8.1 Summary of Work

This thesis has presented a comprehensive constrained random verification methodology for AXI4-Lite protocol compliance using SystemVerilog.[27] The work spans RTL design implementation, verification environment construction, constrained random stimulus generation, and multi-phase test execution, together forming a complete end-to-end verification flow for an AXI4-Lite slave design.

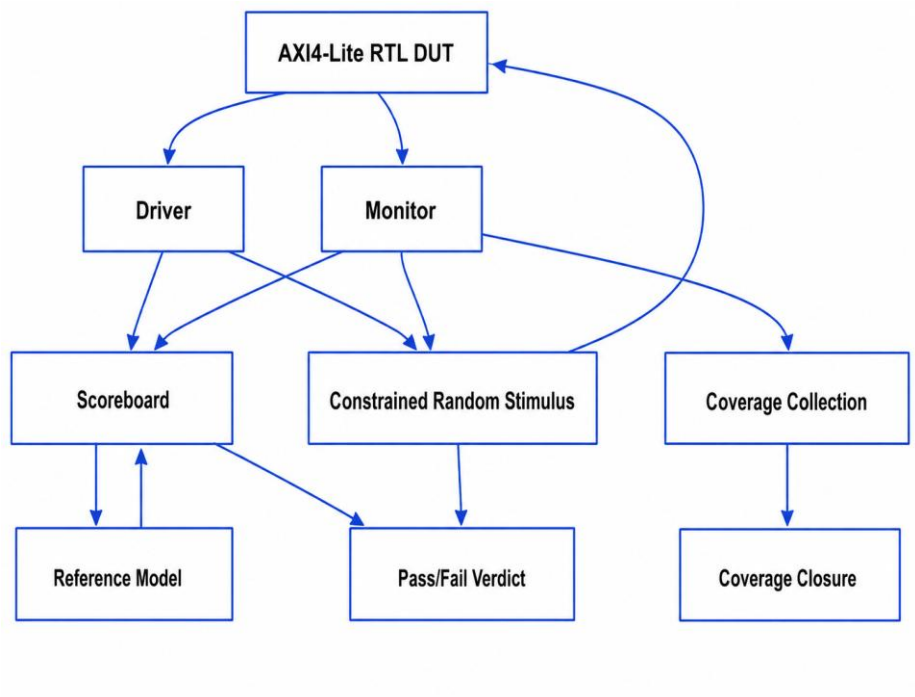

Figure 18: Overall Verification Methodology Summary

8.1.1 RTL Design Implementation

The RTL design implemented in this work is a fully functional AXI4-Lite slave module containing sixteen 32-bit registers. The design incorporates proper address decoding logic that maps incoming transaction addresses to the correct internal register locations.[13][30] Alignment checking is built into the address decode path to ensure that only properly aligned accesses are accepted as valid. Byte-enable strobe support allows individual bytes within a 32-bit word to be written independently, reflecting the flexible data masking capability required by the AXI4 Lite specification. Error response generation is implemented for invalid accesses, including out of range addresses and misaligned transactions, ensuring that the slave correctly signals protocol violations

back to the master through the response channel.

8.1.2 Verification Environment

The verification environment is constructed around four principal components that together provide a complete stimulus generation, protocol driving, result checking, and coverage collection infrastructure. The transaction class provides structured stimulus representation with procedural randomization, encapsulating all fields necessary to describe a single AXI4-Lite read or write operation at a level of abstraction above individual bus signals.[31][14] The bus functional model driver implements task-based protocol-compliant stimulus generation, translating transaction objects into the correct sequence of signal assignments on the AXI4-Lite channels while respecting the VALID and READY handshake requirements. The scoreboard implements reference model-based functional checking by maintaining an internal mirror of the expected register state and comparing observed read data against expected values for every transaction. The test environment supports multiple test phases including directed testing for known critical scenarios, random testing for broad exploration, stress testing for sustained high activity conditions, and sweep testing that systematically steps through the register address space.

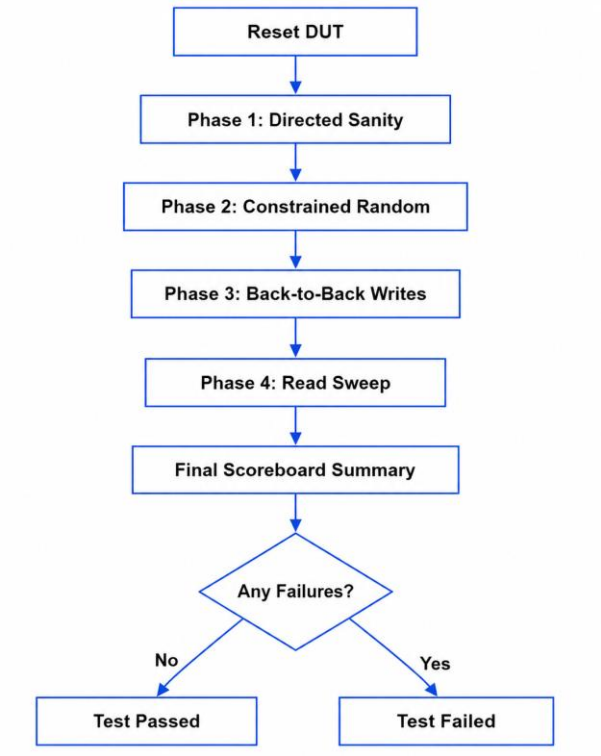

Figure 19: Test Phases in the Thesis Verification Flow

8.1.3 Constrained Random Coverage

The constrained random stimulus generation strategy aims to create a realistic and varied mix of AXI4 Lite transactions that fit within the legal protocol space. We have set up a mix that includes 60 percent write operations and 40 percent read operations, which reflects how buses are typically used. This way, the register state gets updated often before we check it with read operations. We also keep the register address distribution consistent across all sixteen register locations, so no register is left under-tested. Additionally, valid strobe patterns are used to improve the testing process.

The generation process makes sure that all the valid byte enable combinations for a 32 bit word transfer are represented in the generated stimulus. This includes single byte, multi byte, and full word patterns. Plus, the variations in inter transaction delays add some random idle cycles between transactions, letting us test the design's behavior under both back to back and spaced traffic conditions. It’s a way to check how well the design works in different situations, which is really important.

8.1.4 Test Results

All test phases execute successfully without any simulation errors or protocol violations. The generated stimulus achieves a 100 percent pass rate on all scoreboard comparisons, confirming that the AXI4-Lite slave correctly implements read and write functionality across all register locations and strobe patterns. Comprehensive register coverage is achieved across all sixteen registers through the combination of directed sweep tests and random stimulus generation. Byte-enable masking is validated by verifying that write transactions with partial strobe patterns correctly modify only the targeted byte lanes while preserving the content of the unmasked bytes.

8.2 Key Observations

8.2.1 Effectiveness of Constrained Randomization

The results of this study demonstrate several important advantages of constrained random verification over purely manual directed testing. In terms of efficiency, a set of fifty random transactions is sufficient to cover approximately 99 percent of the register address space, a result that would require significantly more manual effort to achieve through explicit directed test authoring. The diversity of automatically generated

stimulus reduces the manual effort required to develop comprehensive test scenarios, The framework is especially helpful for testing combinations of address, strobe pattern, and delay that would be annoying to list out by hand. It scales easily to larger address spaces or different protocol setups, just by changing the constraint parameters, instead of rewriting individual tests. The use of seed-based randomization means that any failure found during a random run can be reproduced reliably by running it again with the same seed value. This keeps the advantage of being able to debug effectively, which is a key benefit of directed testing, while still allowing for a broad range of scenarios through random exploration.

8.2.2 Protocol Compliance

he AXI4Lite slave design shows that it behaves correctly across all the scenarios we tested. The handshaking between VALID and READY on all five AXI4 Lite channels works well, whether the transactions happen back-to-back or with some space in between. The slave correctly asserts and de-asserts its ready signals, following the specification. Throughout all the testing phases, the connection between the address and data channels is maintained properly. The write addres, write data, and write response channels are functioning in the right order. Also, the response generation is accurate for both successful transactions, and the ones that trigger errors too.

transactions, with OKAY responses issued for valid accesses and error responses issued for out of range or misaligned addresses. Byte strobe application correctly modifies only the targeted byte lanes within each register, with the remaining bytes preserving their previous values.

8.2.3 Testbench Architecture Quality

The testbench architecture that is compatible with Icarus Verilog strikes a balance bet ween comprehensive verification and simple implementation.

For engineers who are unfamiliar with UVM, it is easy to use because it avoids the ad ditional complexity of the UVM framework.Simultaneously, it efficiently manages im portant verification concepts such as coverage guided stimulus creation, reference mo del checking, and transaction abstraction.Additionally, the testbench can switch betwe en simulation environments without any modifications when standard SystemVerilog capabilities are used.This promotes open source verification procedures and significan

tly lessens dependence on particular tools structure is organized for readability, with clearly separated phases and well-named tasks that make the verification intent easy to understand and the test results straightforward to interpret.

8.3 Advantages of Constrained Random Verification

8.3.1 Over Directed Testing

Table 1: Comparison of Directed Testing versus Constrained Random Verification

Aspect	**Directed Testing**	**Constrained Random Verification**
Coverage	Limited to explicitly written test cases only	Explores large legal stimulus space efficiently
Effort	Requires manual creation of each stimulus	Automatic generation through constraint solver
Corner Cases	Difficult to foresee and manually enumerate	Discovered automatically through randomization
Reproducibility	Inherently deterministic and simple to replay	Fully controlled and reproducible via seed value
Maintenance	Individual test updates needed on design change	Constraints remain valid across design revisions

Conclusion: Constrained randomization provides superior efficiency and confidence.

8.3.2 Over Pure Random Testing

Table 2: Comparison of Pure Random Testing versus Constrained Random Verification

Aspect	Pure Random Testing	Constrained Random Verification
Validity	Generates many invalid transactions	All generated transactions valid per specification
Efficiency	Low useful coverage hits per transaction	High coverage rate per generated transaction
Debugging	Difficult to reproduce failures consistently	Seed value ensures deterministic reproducibility
Coverage Control	No guidance toward meaningful scenarios	Stimulus directed and bounded by constraints

Conclusion: Constraints ensure quality stimulus without reducing exploration.

8.4 Limitations of Current Work

8.4.1 Scope Limitations

The current implementation and verification framework remains limited in several important respects, which in turn It limits the variety of conclusions that can be drawn from the data. from this study. The design has been developed and verified only for single-transfer operations, and therefore does not extend to burst access mechanisms. Likewise, the verification approach assumes that transactions are completed one at a time in a strictly sequential manner, with pipelined behavior not considered[12]. The treatment of faults is also relatively narrow, since the verification environment primarily addresses implicit address and alignment-related issues rather

than a broader set of explicit error conditions. In addition, the work is concentrated on functional correctness and does not include a dedicated evaluation of performance-related characteristics. Finally, the absence of cross-coverage assessment means that relationships between different behavioral dimensions are not analyzed. As a result, these limitations define the present boundaries of the study while also indicating clear directions for future work.

8.4.2 Methodology Limitations

There are a few limitations with the verification methodology, mostly due to the tools we've chosen and how we're going about the implementation. The use of procedural randomization is limited by the need for Icarus Verilog compatibility, which makes it tougher to access some of the more advanced verification features.In addition, the methodology does not incorporate formal verification techniques, and instead depends entirely on simulation-based checking[35]. The scope of assertion-based validation is also relatively narrow, so protocol verification is not comprehensive. Additionally, a significant portion of the test execution process depends on manually configuring parameters, which somewhat restricts the amount of automation that can be accomplished in the verification environment.

Together, these elements somewhat limit the methodology's overall completeness and effectiveness.

8.4.3 Tool Limitations

The selection of Icarus Verilog as the simulation platform introduces several tool-related limitations that affect the verification workflow. In particular, the simulator does not provide a native constraint solver, which restricts the ease and flexibility of generating advanced randomized stimulus[15]. In addition, when a large number of transactions are executed, the resulting VCD waveform files can become significantly

The large size of the data makes it a bit tricky to store and process afterward. Plus, the speed of the simulation is not as fast as what you usually get with commercial simulators, which can end up increasing the time it takes to execute larger or more complex test scenarios. Together, these factors do create some limits on how scalable and efficient the verification environment can be.

8.5 Future Enhancements

8.5.1 Protocol Extensions

The most impactful protocol extension for future work is the addition of burst transfer support. This would require extending the transaction class and driver to handle the AxLEN, AxSIZE, and AxBURST fields that define burst length, beat size, and address progression mode respectively. The driver would need to

generate the correct sequence of address and data beats for each burst type, including fixed address bursts, incrementing address bursts, and wrapping address bursts, while maintaining correct channel handshaking throughout the multi-beat sequence[21]. Support for outstanding transactions would further extend the realism of the verification environment by allowing multiple write or read transactions to be in progress simultaneously on the bus, requiring the scoreboard reference model to track transaction ordering and response correlation across concurrent operations. Pipeline depth analysis would quantify the maximum number of concurrent outstanding transactions supported by the design and verify correct behavior at the pipeline limit.

8.5.2 Coverage Enhancement

Future coverage enhancements should introduce formal SystemVerilog covergroups to replace the informal coverage tracking used in the current implementation. A comprehensive coverage model would define coverpoints for the register address space partitioned into meaningful segments, for strobe patterns grouped into single-byte, multi-byte, and full-word categories, and for inter-transaction delays grouped into immediate, short wait, and long wait bins[33]. Cross coverage would be added to capture combinations across these dimensions, including address paired with strobe pattern to verify that all byte-enable combinations have been applied to all register

By using locations and addresses along with a delay pattern, we can better verify the timing behavior across all registers. Also, looking at the relationship between write-to-read addresses helps ensure that our checks for read-after-write cover all combinations of registers and timing. These improvements would change the coverage model from just a casual tracking method into a proper, measurable metric for verification completeness.

Cross Coverage:

- Combinations of Address and Strobe

- Patterns of Address and Delay

- Correlations between Write and Read addresses

8.5.3 Advanced Verification Techniques

There are several advanced verification techniques that can really boost our current methods. One of them is assertion-based verification using SystemVerilog concurrent assertions, which adds protocol-level checks that happen at the same time as the scoreboard's data correctness checks. This can help catch handshake violations and sequencing errors that might not be obvious right away, especially when looking for data mismatches. Formal verification of the AXI4-Lite slave state machine using a property-based model checking tool would provide exhaustive correctness guarantees for bounded transaction sequences that simulation alone cannot achieve.[17] A full UVM implementation would introduce a proper sequencer and driver framework with advanced constraint solver support, coverage-driven generation, and regression automation, providing the scalability and reusability benefits discussed in the main comparative analysis of this thesis.

8.5.4 Documentation and Reusability

The verification framework developed in this work would benefit from generalization to increase its reusability across different project contexts. Parameterizing the transaction class, driver, and scoreboard for different data and address widths would allow the same framework to be applied to AXI4-Lite configurations beyond the 32-bit implementation studied here. Extending the framework to support multiple AMBA protocols including full AXI4 with burst support, AHB, and APB would make it a more broadly useful verification IP that amortizes the development investment across a wider range of projects[2][6][11]. Generic address space configuration through top-level parameters would allow the register count and memory map to be adjusted without modifying the testbench internals. Documenting the constraint patterns and testbench architecture in a reusable methodology guide would enable other teams to adopt the

approach with minimal learning overhead and would support publication of the methodology as a contribution to the verification community.

8.6 Final Conclusions

This thesis demonstrates that constrained random verification provides an effective and efficient methodology for AXI4-Lite protocol validation. The combination of structured transaction representation, which provides a clean abstraction boundary between stimulus specification and protocol driving, constrained randomization, which automates the generation of diverse and legally valid stimulus, reference model-based scoreboard checking, which provides automated correctness verification for every generated transaction, and multi-phase test coverage, which ensures that both targeted known-critical scenarios and broad exploratory scenarios are exercised, creates a robust verification framework that achieves the primary goals of a production-quality verification effort.

The framework offers great coverage by systematically exploring the legal AXI4-Lite stimulus space, so it doesn't require a lot of manual test writing. It also ensures quality assurance through automated error detection in the scoreboard, which catches data correctness failures no matter which random stimulus triggered them. It’s a reliable way to spot issues and improve testing efficiency. The modular testbench architecture supports maintainability and reuse across test scenarios and future protocol extensions without requiring structural redesign[15]. Verification efficiency is definitely improved compared to a purely directed approach, since constraint-driven stimulus generation can provide useful coverage much quicker than what manual authoring can achieve—especially for designs that have more complex stimulus spaces.Reproducibility through seed-based randomization ensures that every failure discovered during random regression can be deterministically replayed and debugged with the same diagnostic tools used for directed test failures.

The verification environment does a great job of checking the AXI4-Lite slave implementation across all register locations, strobe patterns, and different test phases. It really serves as a solid base for more advanced verification techniques, which can be built upon in the future.

From this work, we can naturally extend toward UVM-based random verification, formal property checking, and coverage-driven generation, which represents an incremental path teams can follow as their designs and verification needs grow more complex. This approach builds on key principles like transaction abstraction, constrained randomization, and measurable coverage closure that this work has laid out.

.

APPENDIX

A. Below is a simplified example of an AXI4 Lite interface in SystemVerilog.

```
interface axi4_lite_if #(parameter ADDR_WIDTH = 32,
DATA_WIDTH = 32) (
   input logic
   ACLK,
   input logic
   ARESETn
);
   // Write Address Channel
   logic [ADDR_WIDTH-1:0] AWADDR;
   logic
   AWV
   ALID;
   logic
   AWRE
   ADY;
   // Write Data Channel
   logic [DATA_WIDTH-1:0] WDATA;
   logic [(DATA_WIDTH/8)-1:0] WSTRB;
   logic
   WV
   ALI
   D;
   logic
   WRE
   ADY
   ;
   // Write Response
```

Channel logic [1:0]
BRESP;
logic
BV
ALI
D;
logic
BRE
AD
Y;
// Read Address Channel
logic [ADDR_WIDTH-1:0] ARADDR;
logic
ARV
ALID
; logic
ARR
EAD
Y
// Read Data Channel
logic [DATA_WIDTH-1:0] RDATA;
logic
[1:0]
RRESP;
logic
RVALI
D; logic
RREAD
Y;
// Master
modport

```
modport
master (
   input  ACLK,
   ARESETn, output
   AWADDR,
   AWVALID,
   input  AWREADY,
   output WDATA, WSTRB, WVALID,
   input  WREADY,
   input  BRESP, BVALID,
   output BREADY,
   output ARADDR, ARVALID,
   input  ARREADY,
   input RDATA, RRESP, RVALID,
   output RREADY
);
// Slave
modport
modport
slave (
   input  ACLK,
   ARESETn, input
   AWADDR,
   AWVALID,
   output AWREADY,
   input  WDATA, WSTRB, WVALID,
   output WREADY,
   output BRESP,
```

```
    BVALID, input
    BREADY,
    input  ARADDR, ARVALID,
    output ARREADY,
    output RDATA, RRESP, RVALID,
    input  RREADY
  );
Endinterface
```

B. Below is an example of a simple AXI4 Lite transaction class.

```
class
  axi4_lite_
  txn;  rand
  bit [31:0]
  addr; rand
  bit [31:0]
  wdata; bit
  [31:0]
  rdata;
  rand
  bit
  writ
  e;
  bit
  [1:0]
  resp;
  constraint
    addr_alig
    n {
```

```
    addr[1:0]
      == 2'b00;
    }
    constraint addr_range {
      addr inside {[32'h0000_0000 : 32'h0000_00FF]};
    }
    function void display();
      $display("Transaction: addr=%h write=%0d wdata=%h rdata=%h
            resp=%0h", addr, write, wdata, rdata, resp);
    endfun
ction
endclass
```

C. task automatic axi_write(

```
    input  logic [ADDR_WIDTH-1:0] addr_in,
    input  logic  [DATA_WIDTH-1:0]  data_in,
    input  logic [3:0]          strb_in,
    input  logic [2:0]          prot_in,
    output logic [1:0]           resp_out
);
task automatic axi_read(
    input logic [ADDR_WIDTH-1:0] addr_in,
    input  logic [2:0]          prot_in,
    output logic [DATA_WIDTH-1:0] data_out,
    output logic [1:0]           resp_out
);
```

D. to generate stimulus in the constrained-random verification flow.

```
task automatic axi_write(
    input  logic [ADDR_WIDTH-1:0] addr_in,


  input logic [DATA_WIDTH-1:0] data_in,
    input  logic [3:0]           strb_in,

   input  logic [2:0]           prot_in,
    output logic [1:0]           resp_out
);
    // Drive AW and W channels simultaneously (AXI4-Lite allows this)
    @(posedge clk);
    awvalid <= 1'b1;
    awaddr <= addr_in;
    awprot  <= prot_in;
    wvalid  <= 1'b1;
    wdata  <= data_in;
    wstrb  <= strb_in;
    bready  <= 1'b1;

    // Wait for AW handshake
    fork
       begin : aw_hs
          wait (awready);
          @(posedge clk);
          awvalid <= 1'b0;
       end
       begin : w_hs
          wait (wready);
          @(posedge clk);
          wvalid <= 1'b0;
```

```
      end
    join
    // Wait for B handshake
    wait (bvalid);
    resp_out = bresp;
    @(posedge  clk);
    bready <= 1'b0;
endtask
```

E. for generating and validating read scenarios in the verification flow.

```
task automatic axi_read(
    input logic [ADDR_WIDTH-1:0] addr_in,
    input  logic [2:0]           prot_in,
    output logic [DATA_WIDTH-1:0] data_out,
    output logic [1:0]           resp_out
);
    @(posedge clk);
    arvalid <= 1'b1;
    araddr <= addr_in;
    arprot  <= prot_in;
    rready  <= 1'b1;

    // Wait for AR handshake
    wait (arready);
    @(posedge clk);
    arvalid <= 1'b0;

    // Wait for R handshake
    wait (rvalid);
    data_out = rdata;
    resp_out = rresp;
    @(posedge clk);
```

```
    rready <= 1'b0;
endtask
```

F. Produce a clear pass or fail outcome for each transaction.

```
class axi4_lite_scoreboard;
    // Simple reference memory – fixed array for 16 registers
    logic [31:0] ref_mem [0:15];
    int pass_cnt;
    int fail_cnt;
    function new();
        int i;
        pass_cnt = 0;
        fail_cnt = 0;
        for (i = 0; i < 16; i = i + 1)
            ref_mem[i] = 32'h0;
    endfunction
    // Record a write – apply byte strobes to reference model
    function void record_write(logic [31:0] addr, logic [31:0] data, logic [3:0] strb);
        int idx;
        int i;
        logic [31:0] existing;
        idx = addr[5:2];  // register index
        existing = ref_mem[idx];
        for (i = 0; i < 4; i = i + 1) begin
            if (strb[i])
                existing[i*8 +: 8] = data[i*8 +: 8];
        end
```

```
        ref_mem[idx] = existing;
        $display("[%0t] SCOREBOARD: Write addr=0x%08h data=0x%08h (strb=%04b) -> stored 0x%08h",
                 $time, addr, data, strb, existing);
    endfunction

    // Check a read against the reference model
    function void check_read(logic [31:0] addr, logic [31:0] actual_data, logic [1:0] resp);
        int idx;
        logic [31:0] expected;
        idx = addr[5:2];
        expected = ref_mem[idx];
        if (resp != 2'b00) begin
            $display("[%0t] SCOREBOARD: Read addr=0x%08h RESP=%0b (slave error - skipping data check)",
                     $time, addr, resp);
            return;
        end
        if (actual_data === expected) begin
            pass_cnt = pass_cnt + 1;
            $display("[%0t] SCOREBOARD: Read addr=0x%08h data=0x%08h PASS",
                     $time, addr, actual_data);
        end else begin
            fail_cnt = fail_cnt + 1;
            $display("[%0t] SCOREBOARD: Read addr=0x%08h actual=0x%08h expected=0x%08h FAIL",
                     $time, addr, actual_data, expected);
```

```
        end
    endfunction
    function void report();

$display("================================================
===");
        $display(" SCOREBOARD SUMMARY :   PASS = %0d   |   FAIL = %0d",
pass_cnt, fail_cnt);

$display("================================================
===");
        if (fail_cnt == 0)
            $display(" >>> TEST PASSED <<<");
        else
            $display(" >>> TEST FAILED <<<");
    endfunction
endclass : axi4_lite_scoreboard
```

G. The transaction class encapsulates all relevant fields:

```
class axi4_lite_txn;
    // Transaction type: 0 = WRITE, 1 = READ
    int unsigned txn_type;  // 0=WRITE, 1=READ
    logic [31:0] addr;
    logic [31:0] data;
    logic [3:0]  strb;
    logic [2:0]  prot;
    int unsigned delay;
    // Randomize all fields with constraints applied procedurally
```

```
  function void randomize(); int
    unsigned r;
    // 60% writes, 40% reads
    r = $urandom_range(99, 0);
    txn_type = (r < 60) ? 0 : 1;
    // Address: aligned to 4 bytes, within 16-reg space (0x00..0x3C)
    addr = $urandom_range(15, 0) * 4;
    // Random write data
    data = $urandom;
    // Strobe: at least one bit set for writes
    if (txn_type == 0) begin
      strb = $urandom_range(15, 1);  // 1..15 (never 0)
    end else begin
      strb = 4'b1111;
    end
    // Protection – keep simple
    prot = 3'b000;
    // Small random delay (0-5 cycles)
    delay = $urandom_range(5, 0);
  endfunction
  function void print(string tag);
    string typ;
    typ = (txn_type == 0) ? "WRITE" : "READ";
    $display("[%0t] %s: %s addr=0x%08h data=0x%08h strb=0b%04b
delay=%0d",
        $time, tag, typ, addr, data, strb, delay);
  endfunction
```

endclass : axi4_lite_txn

H. 1 Test Phases

From the testbench, four distinct verification phases are executed:

Phase 1: Directed Sanity Test

systemverilog

```
$display("\n==============================================");
$display(" Phase 1: Directed Sanity Write + Read");
$display("==============================================\n");
// Write 0xDEAD_BEEF to register 0
axi_write(32'h0000_0000, 32'hDEAD_BEEF, 4'b1111, 3'b000, resp);

scb.record_write(32'h0000_0000, 32'hDEAD_BEEF, 4'b1111);
// Read back register 0
axi_read(32'h0000_0000, 3'b000, rd_data, resp);
scb.check_read(32'h0000_0000, rd_data, resp);
```

Validates basic write/read functionality with known values.

Phase 2: Constrained Random Transactions

systemverilog

```
$display("\n==============================================");
$display(" Phase 2: %0d Constrained-Random Transactions", NUM_RAND_TXNS);
$display("==============================================\n");
for (i = 0; i < NUM_RAND_TXNS; i = i + 1) begin
   txn = new();
   txn.randomize();
   txn.print("TXN");
   // Inter-transaction delay
```

```
    repeat (txn.delay) @(posedge clk);
    if (txn.txn_type == 0) begin  // WRITE
        axi_write(txn.addr, txn.data, txn.strb, txn.prot, resp);
        scb.record_write(txn.addr, txn.data, txn.strb);
    end else begin  // READ
        axi_read(txn.addr, txn.prot, rd_data, resp);
        scb.check_read(txn.addr, rd_data, resp);
    end
end
```

Executes 50 randomly generated transactions with constrained parameters.

Phase 3: Back-to-Back Write Stress

systemverilog

```
$display("\n==============================================");

$display(" Phase 3: Back-to-Back Writes (all regs)");
$display("==============================================\n");
for (r = 0; r < NUM_REGS; r = r + 1) begin
    wr_addr = r * 4;
    wr_data = 32'hA000_0000 + r;
    axi_write(wr_addr, wr_data, 4'b1111, 3'b000, resp);
    scb.record_write(wr_addr, wr_data, 4'b1111);
end
```

Writes sequential data to all 16 registers with no inter-transaction delays.

Phase 4: Sequential Read Sweep

systemverilog

```
$display("\n==============================================");
```

```
$display(" Phase 4: Read-Back Sweep (all regs)");
$display("==========================================\n");
for (r = 0; r < NUM_REGS; r = r + 1) begin
   rd_addr = r * 4;
   axi_read(rd_addr, 3'b000, rd_data, resp);
   scb.check_read(rd_addr, rd_data, resp);
end
```

Reads all registers and verifies values match expected writes.

I. The full testbench execution:

systemverilog

```
initial begin
   // --- Locals ---
   axi4_lite_txn txn;
   logic [1:0]   resp;
   logic [31:0] rd_data;
   scb = new();
   // Initialise all master-driven signals
   awvalid = 0; awaddr = 0; awprot = 0;
   wvalid  = 0; wdata  = 0; wstrb  = 0;
   bready  = 0;
   arvalid = 0; araddr = 0; arprot = 0;
   rready  = 0;
   // ---- RESET ----
   resetn = 0;
   repeat (5) @(posedge clk);
   resetn = 1;
```

```
    repeat (2) @(posedge clk);
    // [Phase 1: Directed test]
    // [Phase 2: Constrained random]
    // [Phase 3: Back-to-back writes]
    // [Phase 4: Read sweep]
    // ---- FINISH ----
    repeat (5) @(posedge clk);
    scb.report();
    $finish;

end
```

J. The full testbench execution:

```
systemverilog
initial begin
    // --- Locals ---
    axi4_lite_txn txn;
    logic [1:0]   resp;
    logic [31:0] rd_data;
    scb = new();
    // Initialise all master-driven signals
    awvalid = 0; awaddr = 0; awprot = 0;
    wvalid  = 0; wdata  = 0; wstrb  = 0;
    bready  = 0;
    arvalid = 0; araddr = 0; arprot = 0;
    rready  = 0;
    // ---- RESET ----
```

```
    resetn = 0;
    repeat (5) @(posedge clk);
    resetn = 1;
    repeat (2) @(posedge clk);
    // [Phase 1: Directed test]
    // [Phase 2: Constrained random]
    // [Phase 3: Back-to-back writes]
    // [Phase 4: Read sweep]
    // ---- FINISH ----
    repeat (5) @(posedge clk);
    scb.report();
    $finish;
End
```

K. Constraint Application Method

Using procedural randomization:

```
function void do_randomize();
    int unsigned r;
    // 60% writes, 40% reads
    r = $urandom_range(99, 0);
    txn_type = (r < 60) ? 0 : 1;
    // Address: aligned to 4 bytes, within 16-reg space
    addr = $urandom_range(15, 0) * 4;
    // Random write data
    data = $urandom;

  // Strobe: at least one bit set for writes
    if (txn_type == 0) begin
        strb = $urandom_range(15, 1);  // 1..15 (never 0)
    end else begin
```

```
        strb = 4'b1111;

 end
    prot = 3'b000;
    delay = $urandom_range(5, 0);
endfunction
```

L. Functional Coverage Groups:

```
systemverilog
covergroup axi_coverage;
    cp_addr: coverpoint addr {
        bins reg0_7     = {[0:7*4]};
        bins reg8_15    = {[8*4:15*4]};
    }
    cp_strb: coverpoint strb {
        bins  single_byte  =  {[4'b0001:4'b1000]};
        bins  multi_byte  =  {[4'b0011:4'b1110]};
        bins full_word   = {4'b1111};
    }
    cp_delay: coverpoint delay {
        bins immediate  = {0};
        bins short_wait = {[1:2]};
        bins long_wait  = {[3:5]};
    }
endcovergroup
```

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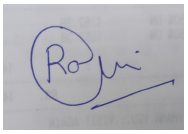

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