Thesis

on

Digitally Enhanced Smart Analog Circuits

submitted towards the partial fulfillment of the requirement for the award of the degree of

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in

VLSI Design

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DECLARATION

I hereby declare that the dissertation entitled "Digitally Enhanced Smart Analog Circuits" is an authentic record of my study carried out as partial requirement for the award of degree of M.Tech.(VLSI Design) at Thapar University, Patiala, under the supervision of Dr. Alpana Agarwal, Associate Professor, ECED.

The matter embodied in this thesis has not been submitted for award of any other degree at this or any other university

Date: 16/6/15

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It is certified that the above statement made by the student is correct to the best of my knowledge and belief.

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ABSTRACT

Today, analog and digital VLSI design has advanced to newer levels. The big challenge of VLSI design lies in minimizing the circuit overhead in terms of silicon area, power consumption and delay. Smart analog circuits are, thus, being looked into to derive the advantages of both, the digital as well as analog world. Smart data converters make use of auxiliary analog and digital circuitry to enhance the features and to eventually tailor the converter architecture for more efficient performance.

This work proposes an innovative, digital-in-concept prospective idea for designing smart analog circuits, operated on low voltage. The mixed signal circuit consists of both digital and analog circuit in which the CMOS digital circuit is easier to fabricate and it increases the speed of the circuit as most of the delay in the circuit comes from the analog circuitry. As a demonstration of the strength of smart analog circuits, a low power high speed digitally enhanced flash ADC has been designed. In present work, firstly, digitally enhanced analog voltage comparator has been designed using a pure digital differential circuit technique which is used as basic building block of flash ADC. The proposed digitally enhanced analog voltage comparator circuit has low power dissipation of 0.324μW, high resolution of 1.96 mV, low DC offset of 1 mV, full output swing of 0-1.8V and common mode input range of 0-1.8V. The circuit has been simulated using SPICE in TSMC 0.18μm CMOS technology at 1.8 V with load capacitance of 1 pf.

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ABBREVIATIONS

VLSI	Very Large Scale Integration
MOS	Metal Oxide Semiconductor
MOSFET	Metal Oxide Semiconductor Field Effect Transistor
CMOS	Complementary Metal Oxide Semiconductor
NMOS	Negative-Channel Metal-Oxide Semiconductor
PMOS	Positive-Channel Metal-Oxide Semiconductor
DP	Differential Pair
SAR	Successive Approximation Register
ADC	Analog to Digital Converter
INL	Integral Non Linearity
DNL	Differential Non Linearity
LSB	Least Significant Bit
MSB	Most Significant Bit
X-OR	Exclusive OR
LVDS	Low Voltage Differential Signaling
ICMR	Input Common Mode Range

MOTIVATION

Mixed signal circuit is a circuit that contains both analog and digital circuit in same semiconductor die. In real time applications mixed signal designs are everywhere for example smart phone. In mixed signal circuit analog to digital converter is used so that digital device can process the signal. However, Today's mixed signal circuit contains about 80 % of the digital circuit and only 20 % of the analog circuit and even then 80% of the design time is taken by analog circuits. Moreover, Geometrical and power supply scaling in recent CMOS technology have greatly improved the performance of digital integrated circuits (ICs) over the last decade. Nonetheless analog ICS have scarcely taken advantage of CMOS technology enhancements and on the contrary, reduced supply levels, short channel effects, increased process variability have made integration of analog blocks in the present day System-on-a-chips (SoCs) more and more challenging. An alternative approach to the challenges of the present day microelectronics is to rethink analog functions in digital terms so that they can be implemented by digital circuits and also about design methodologies which are as close as possible to digital world. This will lead to implementation of different analog circuit using IC fabrication technology.

CHAPTER 1 INTRODUCTION

Scaling in Geometrical parameter and power supply in recent CMOS technology have efficiently improved the performance of Integrated Circuit (IC) over last 10 years [1]. On the other hand reduced level of supply voltage, short channel effect, voltage swing reduction have made designing of analog IC more and more difficult [2]. In recent system-on-chip (SoC), digital topology is dominant although there are some analog circuits presents. Most devices are targeted for digital circuit enhancement if analog/mixed signal are taken into account. However, different topologies operating from low power supply voltages [3-7], current-mode techniques have been introduced [8] to replace standard CMOS operational amplifier [9] and voltage references [10]. However, most of proposed solutions, remove specific technology-related inconveniences at the cost of design complexity, large delay and/or reduced performance. To solve these challenges, microelectronics analog functionality has to be modified in digital term in such a manner that method of implementation is very close to digital world. By using this idea, working of voltage comparator, analog to digital (A/D) converters [11,12] class D amplifier [13] and phase lock loops (PLLs) [14] can be fully described in digital terms. Unfortunately, only a few analog circuits have been re-thought in pure digital [15] terms so far and traditional analog implementations are necessary for basic fundamental blocks like voltage comparators, op-amp and analog to digital converter circuits. For designing the digitally enhanced smart analog circuit which works same as analog circuit the understanding of different analog circuit is required.

1.1 AN ANALOG DIFFERENTIAL CIRCUIT

An analog differential-pair or differential circuit configuration is most widely used building block in analog IC design. Differential circuit is also an input stage of every operational amplifier. An analog differential circuit shown in Figure 1.1, is designed to provide an output signal that is related to the difference of two input voltages v^+ and v^- *i.e.,* to the differential mode input voltage $v_D = v^+ - v^-$, and that is not influenced by

the absolute value of input voltages with respect to reference voltage ,*i.e.*, which is insensitive to the common mode (CM) voltage, $v_{CM} = \frac{v^+ + v^-}{2}$.

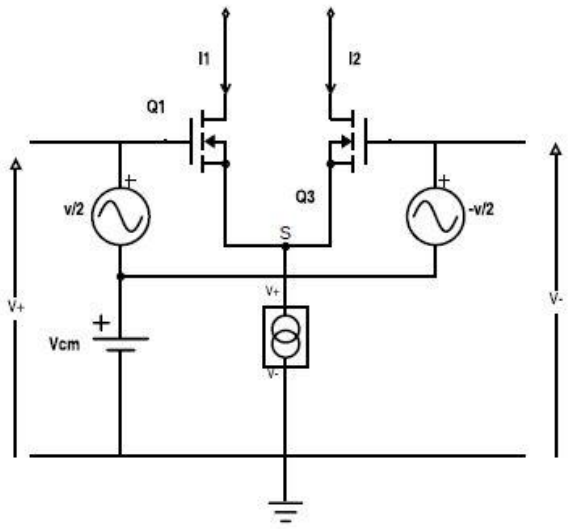


Figure 1.1 Analog differential circuit

An analog differential circuit is typically implemented in analog CMOS process as a DP including two identical source-coupled MOS transistors M1 and M2 biased in the saturation region by a constant current source, as depicted in Figure 1.1 In a CMOS DP, the voltage at the common-source node S, which ideally tracks the CM input voltage variations, is subtracted from the input voltages v^+ and v^- so that the gate-source voltages of M1 and M2 are not affected by the CM input. As a consequence, neglecting channel length modulation, the output currents i_1 and i_2 are independent of the CM input voltage in a differential circuit.

1.2 VOLTAGE COMPARATOR

A comparator is a device whose output is HIGH(‘1’) when the voltage on the positive (+) input is greater than the voltage on the negative (-) input and LOW(‘0’) when the positive input voltage is less than the negative input voltage. In other way of defining a comparator is to say that a comparator circuit is used to compare two input voltages and determine which is the larger of the two. This is true regardless whether the comparator is set up for inverting or non-inverting operation. Inputs into a comparator can be an analog voltage but the output is digital. Comparators, the devices, are designed to operate in

open loop configuration without any negative feedback. The speed (propagation delay) and slew rate (rise and fall time) are major parameter. Comparator overall gain is also usually higher.

1.3 ANALOG TO DIGITAL CONVERTER (ADC)

Analog to digital converter is an electronic integrated circuit which converts the analog signal into digital form (binary). However, most of device such as microprocessor, medical instruments, digital computers require signals to be in digital form whereas most instrumentation transducers have an output signal in analogue form so that there is need of analog to digital converter to convert the analog signal into digital form. Different types of ADCs are there according to requirement like speed, cost, power consumption, complexity.

Types of available ADCs are:

1. Flash

2. Successive Approximation

3. Pipelined

1.3.1 FLASH ADC

Flash analog to digital converters have a resistive ladder that divides the reference voltage in 2^N equal parts. A comparator compares the input signal with the voltage supplied by that part of the resistive ladder for each part. The output of all the comparators is like a thermometer code: the higher the input value, more comparators have their outputs high from bottom to top. A component called "Encoder" converts thermometer code into a binary code, which corresponds to the position of the last comparator with high output, counting from the bottom up.

- **STRENGTHS**
  - Very fast
  - converts analog signal instantly into bit form

- **WEAKNESSES**
  - For N bits 2^N-1 comparators require hence It doubles in size for each bit added to the representation.
  - It has a high input capacitance
  - It consumes a lot of power

In this thesis work our main focus is to design digitally enhanced flash analog to digital converter with high speed and low power consumption. Basically flash ADC has mainly 3 functional blocks which are voltage divider, voltage comparator and encoder. The basic block diagram of conventional flash ADC is shown below.

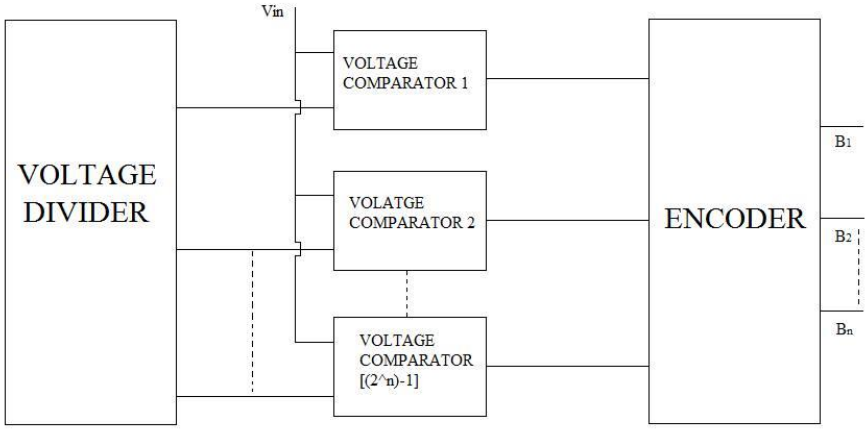


Figure 1.2 Basic block diagram of flash ADC

Parameters which are important to understand characteristic of flash ADC are explain here:

- **PERFORMANCE PARAMETERS OF FLASH ADC**
  - **Resolution**

    The resolution of the converter is the number of discrete values that flash ADC can produce over the full range of analog values. The resolution of ADC determines the magnitude of the quantization error. maximum possible average signal to noise ratio for an ideal ADC can be obtain by resolution without the use of oversampling. The values are usually stored in binary form, so the resolution is

usually expressed in bits. In consequence, the number of discrete values available, i.e. "levels", is assumed to be a power of two. For example, an ADC with a resolution of 4 bits can encode an analog input to one in 16 different levels (2^4= 16). Ideal graph for flash ADC is shown below.

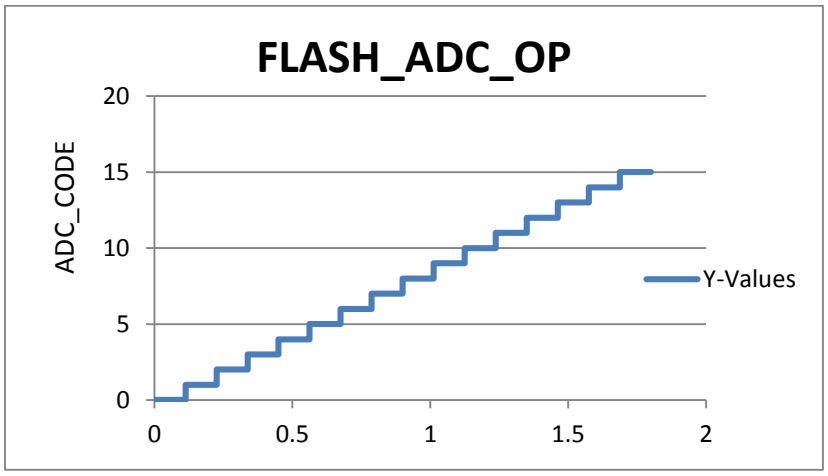


Figure 1.3 ideal flash ADC output

Resolution can also be expressed in volts. The minimum change in voltage required to assure a change in the output code level is called the least significant bit (LSB) voltage. The resolution R of the ADC is equal to the LSB voltage. The voltage resolution of a flash ADC is equal to the overall voltage range divided by the number of discrete values:

Resolution $R = \frac{V_{full}}{2^N}$

where N is the ADC's resolution in bits and V_{full} is the full scale voltage range

- **Propagation delay**

  Propagation delay of flash ADC can be determined by calculating acquisition time and settling time. In flash ADC sample and hold circuit is an important aspect. The acquisition time, denoted by T_{aq} is the time sample and hold circuit remain in the sampling mode to ensure that hold mode output will be in specific band of input level.

  Acquisition time can be obtained on assumption that the gain and offset effect has been removed. Now, Settling time T_s, is the time interval between the sample and

hold command and the time when the output transient has been settled to within a specified band. The figure for this is shown below.

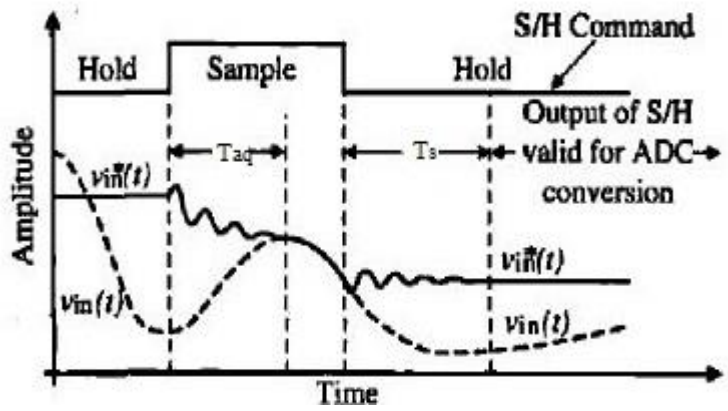


Figure 1.4 Waveform for sample and hold circuit

Hence the minimum conversation time for a flash ADC would be equal to T_{sample} is equal to

$T_{sample} = T_s + T_{aq}$

where T_s and T_{aq} is settling time and acquisition time respectively. Sampling frequency can be obtain by inverse of T_{sample}

$f_{sample} = \frac{1}{Tsample}$

- **Power consumption**

  In flash ADC there are mainly 3 components which are

  1. Voltage divider
  2. Voltage comparator
  3. Encoder

  Among all these component voltage comparator and encoder are play major role in power consumption. In conventional N bit flash ADC there are 2^N-1 comparators are required Hence, designing of voltage comparator must be in a such a way that minimum power can be consume. Now a days, different types of dynamic comparator is being used to reduce power also techniques in which number of comparator for flash ADC can be implemented for designing.

  Power = (2^N-1)*(power consume 1 comparator) + (power consume by encoder).

In this thesis a novel digitally enhanced voltage comparator is proposed which is used to design flash ADC so that power consumption is significantly reduced.

- **Gain Error**

  Gain error of flash ADC is a difference between the actual characteristic and infinite resolution characteristic. This difference is proportional to the input voltage. The gain error can be also thought as a change in slope of infinite resolution line above or below value of '1'.

- **Offset Error**

  The horizontal difference between horizontally shifted infinite resolution line until quantization noise is symmetrical and the infinite resolution characteristic that passes through the origin is offset error.

- **Differential nonlinearity**

  Definition of differential nonlinearity (DNL) is the Deviation of transition code width from the ideal one (1 LSB). For narrow code width, DNL is negative while for the wide one DNL is positive. In an ideal ADC the code width is always one, thus, DNL is zero.

- **Integral nonlinearity**

  The definition for integral nonlinearity (INL) of flash ADC is the maximum difference between the actual finite resolution characteristic and the ideal finite resolution characteristic measured vertically in percent or LSBs. INL can also be specified as the sum of DNLs. Additionally, INL can be defined as the distance of the code centers with the best fit line. Figure 1.5 depicts the maximum INL which is measured with the ideal one.

1.3.2 PIPELINED ADC

Pipelined analog to digital converter shown in Figure 1.6 is as fast as flash ADC. In pipelined ADC number stages are as per number of bits. Number of stages increased with increase in bits. Pipelined analog to digital converters convert the input in a number of steps proportional to the number of bits. Comparison of input signal can be made with half of

the reference value at each step. If signal value is higher than the half the reference value then signal is subtracted to the input and the bit value corresponding to that step is 1. Otherwise, bit value is 0. In either case, the remaining value is doubled and passed to the next stage. Note that one bit is being taken care by each stage, so a new value can be applied to the input in every cycle.

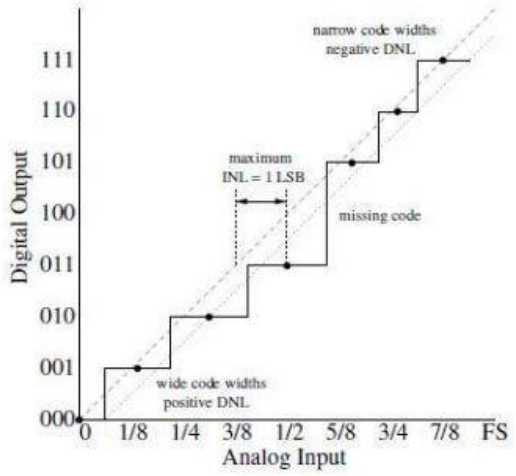


Figure 1.5 Example for INL and DNL for 3 bit ADC [21]

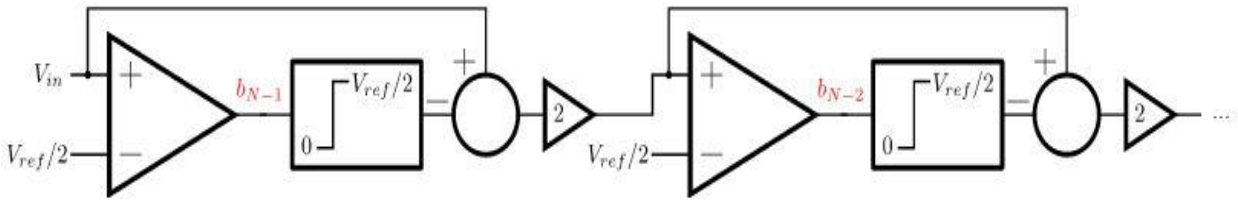


Figure 1.6 Pipeline ADC architecture [21]

- **STRENGTHS**
  - The number of stages increases only with the number of bits
  - As fast as the flash ADC

- **WEAKNESSES**
  - High latency - For any analog value, it takes N cycles to output the corresponding binary representation.

- Any error occur in the subtraction or doubling operations passes to the following stages.

1.3.3 SUCCESSIVE APPROXIMATION REGISTER (SAR) ADC

Successive approximation register converter is low power converter as it consist only one comparator in circuit. A Successive Approximation Register converter evaluates each bit at a time, from the most significant bit to the least significant bits. They successively approach the output of a digital-analog converter (DAC) in them to the applied input voltage. An N bit register is there for storing the input of the DAC, which is also the output of the ADC. Circuit for SAR ADC is shown in Figure 1.7

First, fixed input voltage is generated by using analog signal sampled and hold circuit. If the value of input signal is changed during the conversion then the result can be erroneous. Now, the bit N−1 of the register is set to '1' and all other bits of register are set to 0. Since the input reference voltage of the DAC is V_{ref}, its output is set to $\frac{V_{ref}}{2}$. The output of the comparator is latched to the most significant bit b_{N-1}, i.e., if the value of input voltage is less than the value of half of reference value ($V_{in} < \frac{V_{ref}}{2}$) then b_{N-1} is reset to 0, otherwise it stays 1. By successively setting the next bit to logic'1', comparing the output of the DAC with the applied input voltage and latching the output in the same bit, the converter generates a signal from the register that is successively approximating the input value.

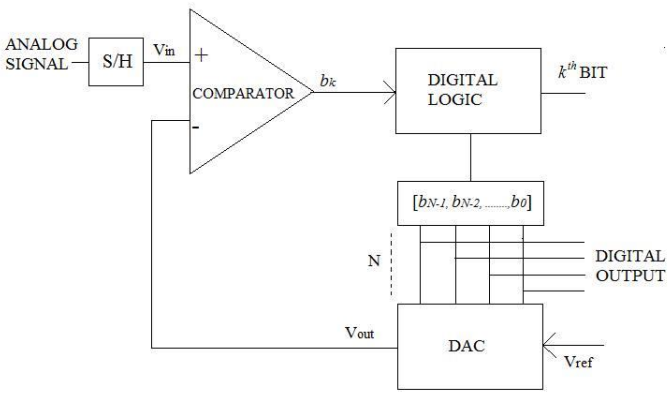


Figure 1.7 SAR ADC architecture [21]

- **STRENGTHS**
  - It uses only one comparator
  - Low power consumption

- **WEAKNESSES**
  - The DAC grows with the number of bits
  - They take as many cycles to convert the signal as the number of bits
  - Slow speed
  - The component mismatch in the DAC limits its linearity.

CHAPTER 2 LITERATURE REVIEW

2.1 FLASH ADC

The need for a high speed and low power ADC is veryessential for various applications. Flash ADCs are always thearchitecture choice where maximum sample rate and moderateresolution is needed.

2.1.1 I. L. Jong *et al.* [22]

A flash analog-to-digital converter (ADC) using multiplexers (MUXs) to reduce the number of preamplifiers and comparators is reported. For N-bit flash ADC requires 2^N-1 preamplifiers and comparators while the proposed ADC only needs $2^{(N-3)}$+2 preamplifiers and $2^{(N-2)}$+1 comparators. In this paper the proposed ADC with 6-bit resolution requires a reduce number of preamplifiers and comparators by 84% and 73%, respectively. Figure 2.1 shows 6-bit ADC consists of a resistive voltage divider , a track-and-hold circuit, 10 preamplifiers, 17 comparators, a (2x1)-MUX, 8 (4x1)-MUXs and logic gates for encoder and registers.

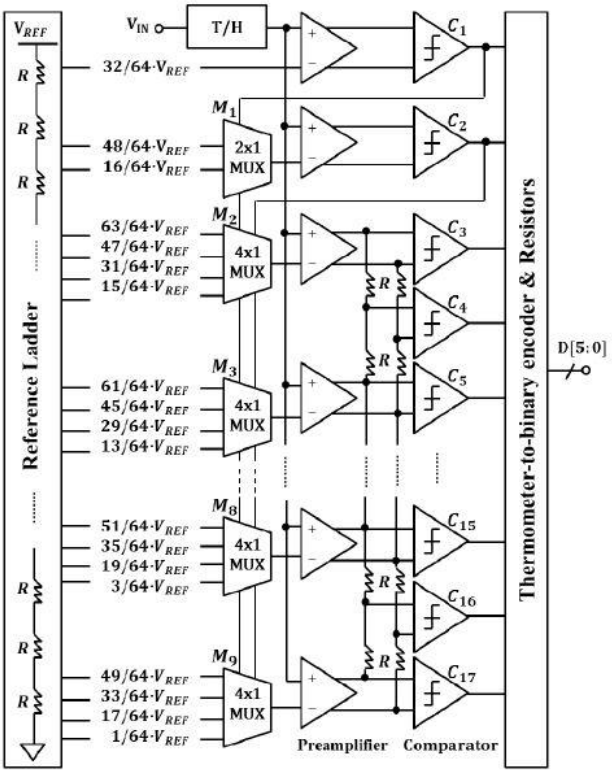


Figure 2.1Block diagram of the proposed 6-bit flash ADC [22]

2.1.2 O. S. Mohamed *et al.* [23]

In this paper, a new design for a low power CMOS flash Analog-to-Digital Converter (ADC) is proposed. A 6-bit flash ADC, with a maximum acquisition speed of 1 GHz, is implemented in a 1.2 V analog supply voltage. This design requires only 10 comparators and 9 multiplexers to generate the required binary code as shown in Figure 2.2.

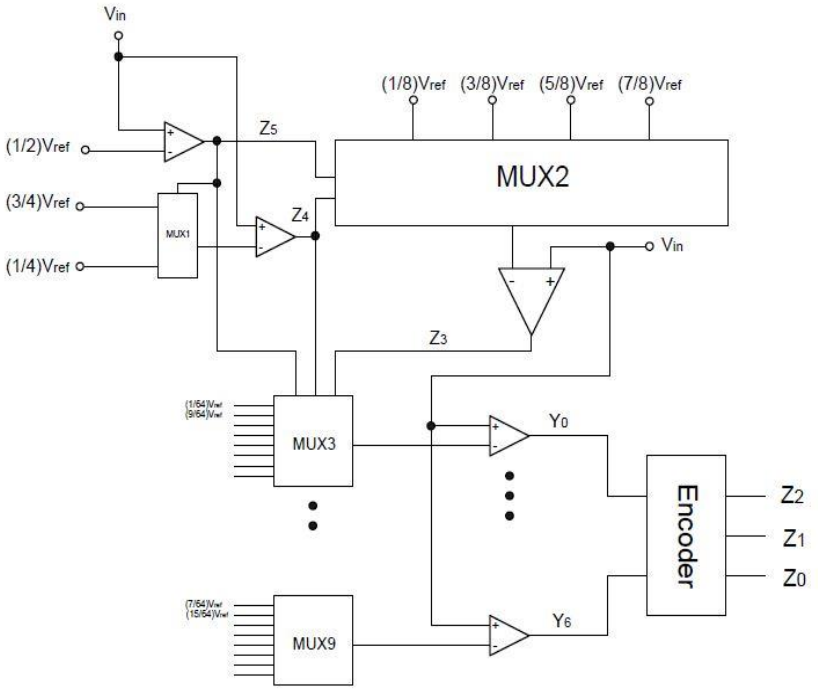


Figure 2.2The proposed 6-bit flash ADC architecture [23]

The new design offers lower number of comparators and lower power consumption compared with the conventional flashADC. The maximum sampling speed is 1 GHz and the analog supply voltage is only 1.2 V. This architecture can be extended to highresolution applications because of the simplicity of the circuit.

2.1.3 M. I. Titu *et al.* [24]

Dynamic Flash ADC has many applications in mixed signal systems in which analog signals are converted to bit form and then processed in circuit. In this paper, a new high performance dynamic Flash ADC is designed in which low power open loop comparator and fast thermometer encoder is used.

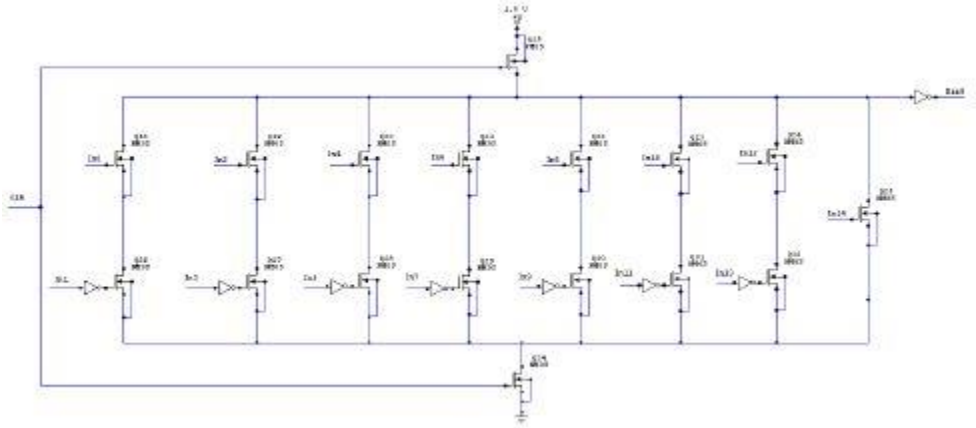


Figure2.3 Bit0 of a 4-Bit Dynamic Thermometer Encoder [24]

Subsequently, a dynamic Flash ADC using standard cells like NAND, NOR and INVERTER is also designed and implemented. The transistors count is reduced by 50%, which results efficient implementation of circuit with reduced area.

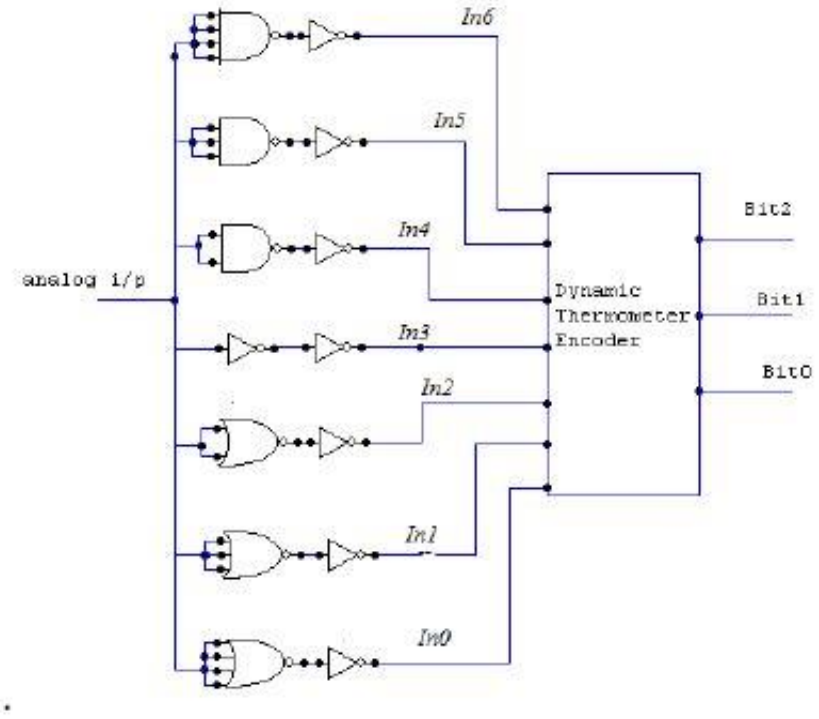


Figure 2.4 3-bit Dynamic Flash ADC using standard cells [24]

2.1.4 P. Senapati *et al.* [25]

Architectural level design of a low power Thermometer code to Binary code Encoder for a Flash ADC of 4 bit resolution is presented. Architecture for the thermometer code is initially converted into intermediate gray code using 2:1 multiplexers and then to the binary code using XOR gates. Various logic styles (CMOS, Transmission gate logic, DPL, SRPL, PPL) are studied for the design of 2:1 Multiplexers and XOR gate. The performance of proposed architecture is compared with other available architectures like multiplexer based direct conversion method, wallace tree encoder, intermediate gray code based encoder using basic gates and using 2:1 multiplexers.

2.2 VOLTAGE COMPARATOR

In flash ADC basic building block taken in consideration is the comparator. The main function of a comparator is to deliver an output voltage (high or low) which represents the results of a comparison between two voltages at its input.

2.2.1 K. N. Shesharaman *et al.* [16]

Voltage comparator circuit is used for Nuclear Magnetic Resonance (NMR) applications. Nuclear Magnetic resonance circuitry works at 1.5 Tesla magnetic field which corresponds to the resonance frequency of the nuclei around 64 MHz. This paper is based on designing of voltage comparator by using CMOS Operational Transconductance Amplifier (OTA) technique with reduced cascode current mirror circuit for proper biasing. For required frequency specification voltage comparator architecture include sampling circuit. The circuit is shown below:

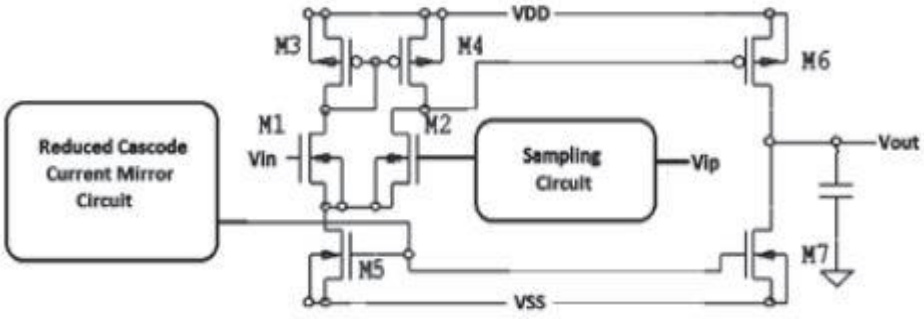


Figure 2.5 design of a CMOS comparator with modified current mirror and a sampling circuit [16].

The work presented in this paper deals with the design and implementation of CMOS latched comparator design for low power consumption and high speed application. This design achieves a high slew rate, which makes the useof OTA in high speed applications suitable.

2.2.2 S. Yewale *et al.* [19]

A CMOS voltage comparator based on a preamplifier-latch circuit driven by a clock is explored in this paper. Design is expected to be implemented in Sigma-delta Analog-to-Digital Converter (ADC). The proposed comparator is designed for high resolution sigma delta ADCs.The main advantage of this design is capable to reduce power dissipation and increase speed of an ADC. The design is simulated in 0.18 μm CMOS Technology with Cadence environment. The basic block diagram of circuit is shown in Figure 2.6.

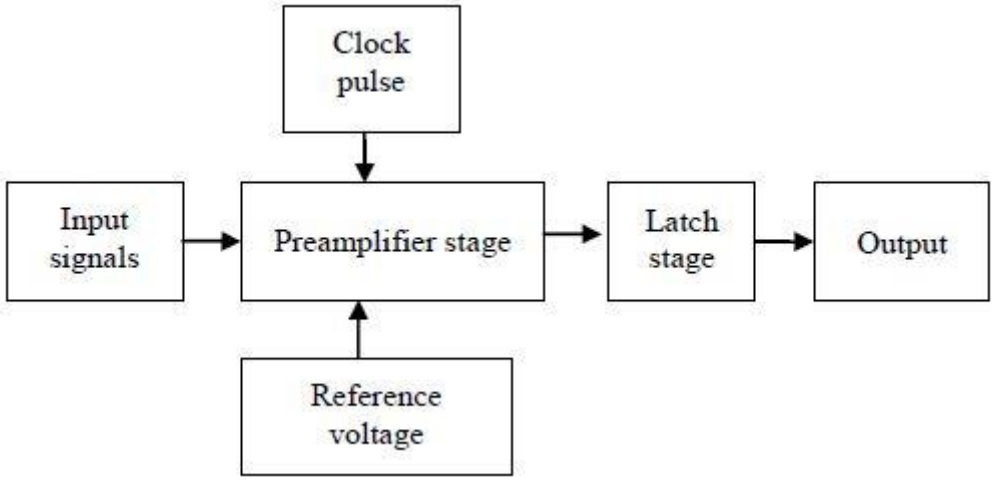


Figure 2.6 Preamplifier-latch comparator [19]

2.2.3 T. Jayachandran *et al.* [17]

In this paper a clocked comparator has been used to make fast decisions. The accuracy of voltage comparator is given by its input referred offset voltage and the resolution. Double tail comparator and pre-amplifier based comparators is used for reducing power and delay in dynamic latch comparator circuit. Double tail transistor is used to reduce the circuit delay so that transistor is included one at the top V_{dd} and other at the bottom V_{ss}. Due to this transistor positive feedback during regeneration is strengthened, which

reduces delay time. In the proposed comparator, power consumption and delay are reduced significantly to 7.4ns and 12 μw respectively.

2.2.4 S. Jayesh *et al.* [18]

Demands of the processing speeds and power efficient interconnections between the ICs is increasing. In order to meet the requirements of high speed, low noise communication between ICs, the Low Voltage Differential signaling (LVDS) protocol is used. This paper studies the design of comparator stage of LVDS receiver. Due to the differential transmission technique and the low voltage swing, LVDS allows high transmission speeds and low power consumption at the same time.

2.3 ANALOG AND DIGITAL DIFFERENTIAL CIRCUIT

Differential circuit is primary building block of op-amp or voltage comparator. Differential circuit amplifies the difference between 2 input voltage signals and suppresses common mode voltage.

2.3.1 B. Zeljko *et al.* [26]

This paper introduces the CMOS differential amplifier with active load and single ended output is one of the most popular circuits used in analog and mixed signal applications. The analysis of the differential amplifier is simplified and its behavior is properly explained. In this paper the facts that the gate to source voltages and the current changes of the output transistors in the differential mode are not of equal amount. Circuit diagram of CMOS differential circuit with active load is shown in Figure 2.7. The body effect is also included into the analysis.

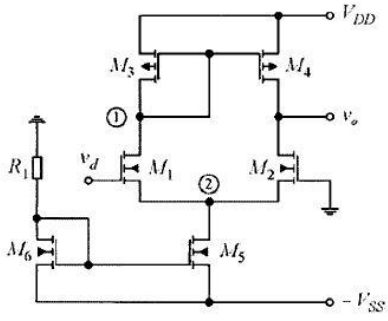


Figure 2.7 CMOS differential circuit with active load [26]

2.3.2 J. M. Redoute *et al.* [27]

This paper introduces the performances of CMOS differential input stageswith a high degree of immunity against electromagnetic interferences (EMIs). CMOS differential circuit also compares a source-buffered differential pair which is very resistant to EMI coupledat its inputs. TheEMI performance of this source-buffered differential- pair circuit hasbeen evaluated with a test chip in which EMI signal of 750 mV rms is injected at the input terminals and the measured maximal input offset voltage correspondsto 116mV for the source-buffered circuit is compared with 610mV for the classicdifferential pair, which suggests a major improvement.

2.3.3 P. S. Crovetti *et al.* [15]

Crovetti P.S used digital-in-concept approach for designing of analog differential circuits, suitable to very low voltage, scaled, pure digital integrated circuit technologies, is explained in this paper. A differential stage based on the proposed technique is presented and its operation as a voltage comparator and as an operational amplifier in negative feedback configurations is discussed and demonstrated on the basis of theory and simulations. The practical implementation of the proposed approach is finally verified by experiments carried out on a proof-of concept prototype.

2.4 VLSI TREND AND SCALING

The main requirement of VLSI integrated circuit is to improve performance of circuit by putting more and more number of transistor in small area. Speed and precision is also a major issue related to technology scaling.

2.4.1 G. E. Moore *et al.* [28]

Moore's law is the base of VLSI design. This paper is based on increase in the number of component in integrated circuits. Moore, G. E. gave a law for that which is stated as "The complexity for minimum number of component has increased at a rate of roughly a factor of two per year". If this rate does not increase, then certainly over the short period of time this rate can be expected to maintain. In this paper, cost reduction and yield increment is discussed. The cost per component is inversely proportional to the number of components on the integrated circuit so that the equivalent piece of semiconductor in the equivalent

package containing more components. For digital systems the integration will not change linear systems as radically as analog system. Still, a considerable degree of integration will be achieved with linear analog circuits. The limitation of large-value inductors and capacitors is the greatest fundamental bottleneck to integrated electronics in the linear area.

2.4.2 G. Gielen *et al.* [29]

The problems that are faced by designers while implementing analogand digital circuits in nanometer technologies are discussed in this paper. An introductory embedded tutorial willgive an overview of the design problems at hand the leakage power and processvariability and their implications for digital circuits and memories, and the reducingsupply voltages, the design productivity and signal integrity problems for embeddedanalog blocks. In this paper problem occur for digital and analog circuit at 65 nm technology is explored.

2.4.3 S. Borkar *et al.* [30]

Scaling advanced CMOS technology to the next generation improves performance, increases transistor density, and reduces power consumption. Technology scaling typically has three main goals: 1) reduce gate delay by 30%, resulting in an increase in operating frequency of about 43%; 2) double transistor density; and 3) reduce energy per transition by about 65%, saving 50% of power (at a 43% increase in frequency). These are not ad hoc goals; rather, they follow scaling theory. This article looks closely at past trends in technology scaling and how well microprocessor technology and products have met these goals. It also projects the challenges that lie ahead if these trends continue. This analysis uses data from various Intel microprocessors; however, this study is equally applicable to other types of logic designs.

CHAPTER 3 DIGITALLY ENHANCED SMART ANALOG CIRCUITS

In literature the limitation of analog integrated circuit fabrication in present day is being presented. Different techniques have been employed to analog circuit that is robust to noise also work on reduce supply voltage but all such improvement can get at the cost of increase design complexity or reduce performance. In this chapter rethinking of analog circuitry in digital term is discussed. Digital differential circuit is firstly discussed and digitally enhanced analog voltage comparator is also explored.

3.1 A Digital Differential Circuit

The circuit shown in Figure 3.1(a), which includes a pair of single-ended non-inverting digital buffers, is first considered as a possible fully digital implementation of a differential stage. Each buffer provides a high digital output signal OUT^+ = "1" an output voltage V_{OUT}= V_{OH}>V_{th} when input signal V_{IN}>V_{th} and each buffer provides a high digital output signal OUT^+ = "0" an output voltage V_{OUT}= V_{OL}<V_{th} when input signal V_{IN}<V_{th} where V_{th} is threshold voltage. The input terminals of the buffers in Figure3.1(a) are connected to the external inputs v^+ and v^- and their outputs are taken as the digital output (OUT^+, OUT^-) of differential circuit.

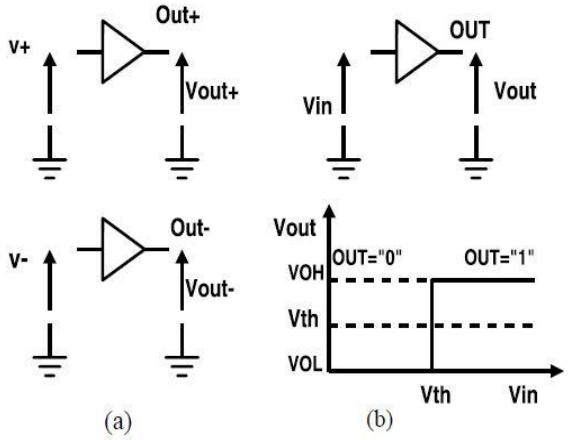


Figure 3.1. A pair of single-ended digital buffers as a +digital differential stage (a) and input/output characteristic of each digital buffer (b).

Depending on the input signals v^+ andv^-, it can be observed that output of the circuit in Figure 3.1(a) is related to the DM input voltage as in a differential circuit.

$$(v^+ > V_{th} \& v^- < V_{th}) \rightarrow v_D > 0 \tag{3.1}$$

It follows that

$$(OUT^+, OUT^-) = (1,0) \rightarrow v_D > 0 \tag{3.2}$$

Similarly

$$(v^+ < V_{th} \& v^- > V_{th}) \rightarrow v_D < 0 \tag{3.3}$$

It follows that

$$(OUT^+, OUT^-) = (0,1) \rightarrow v_D < 0) \tag{3.4}$$

Ideally, only two input configurations, $(v^+ > V_{th} \& v^- < V_{th})$ and $(v^+ < V_{th} \& v^- > V_{th})$ should be possible, i.e., in the above case inputs can be expressed as

$$\begin{cases} v^+ = V_{th} + \frac{v_D}{2} + v_{CM} \\ v^- = V_{th} - \frac{v_D}{2} + v_{CM} \end{cases} \tag{3.5}$$

With,

$$|v_{CM}| < \left|\frac{v_D}{2}\right| \tag{3.6}$$

So that,

$$v_D > 0 \rightarrow (OUT^+, OUT^-) = (1,0) \tag{3.7}$$

$$v_D < 0 \rightarrow (OUT^+, OUT^-) = (0,1) \tag{3.8}$$

However, this is not always the case as the configurations, ($v^+ > V_{th} \& v^- > V_{th}$) and ($v^+ < V_{th} \& v^- < V_{th}$) are also possible. When these inputs are applied, the buffer outputs are (OUT^+, OUT^-) = (1, 1) and (OUT^+, OUT^-) = (0, 0), respectively. Subsequently, they are no longer related to the DM input voltage v_D. In such configurations, in fact, the input voltages can be expressed as in (3.5), with $|v_{CM}| > \left|\frac{v_D}{2}\right|$ and the dominant CM component v_{CM} makes the circuit in Fig. 3.1(a) insensitive to the DM component.

In these last two cases, however, the digital outputs provide some information on the CM input voltage. Since

$$(v^+ > V_{th} \& v^- > V_{th}) \rightarrow v^+ + v^- > 2V_{th} \tag{3.9}$$

It follows that

$$(OUT^+, OUT^-) = (1,1) \rightarrow v_{CM} > V_{th} \tag{3.10}$$

And similarly

$$(v^+ < V_{th} \& v^- < V_{th}) \rightarrow v^+ + v^- < 2V_{th} \tag{3.11}$$

It follows that

$$(OUT^+, OUT^-) = (0,0) \rightarrow v_{CM} < V_{th} \tag{3.12}$$

The circuit in Fig. 3.1(a) operates like a differential stage only when condition (3.6) is satisfied by the external inputs. Nonetheless, it can be transformed into a real differential circuit, provided that the CM input of the digital buffers is corrected in real time so that condition (3.6) is verified independently of the external CM input voltage. A CM compensation analog signal v_{CMP} is generated by exploiting the information about the CM input provided by the configuration (3.10) and (3.12). This signal can be added to the external inputs v^+ and v^- so that condition (3.6) is enforced by negative feedback. Such a CM compensation method is analogous in concept to the CM rejection mechanism of

the standard CMOS DP in Figure1.1, where the S common source node voltage, which tracks the CM input, is subtracted from the external inputs and CM-independent gate-source voltages are applied to the input devices.

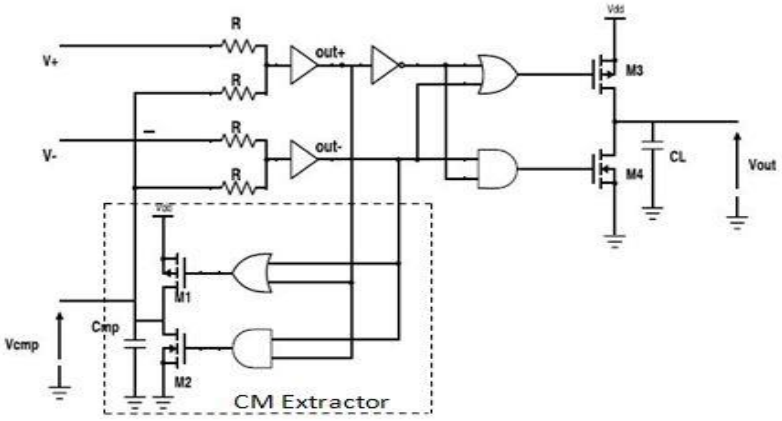


Figure 3.2 A digital-based differential circuit.

The idea that has been outlined above is exploited in the circuit in Figure 3.2 where some design specification is to be consider such as Supply Voltage of 1.8V, CM compensation capacitance of 2nf, load capacitance C_{OUT} of 1pf, large resistor R of 100K , propagation delay 8ns with feature size 0.18µ. Voltage compensation signal v_{CMP} is added to the external input signals v^+ and v^- by a summing network so that the actual input signals of the digital buffers v'^+ and v'^- can be expressed as,

$$v'^+ = \frac{v^+ + v_{CMP}}{2}, \; v'^- = \frac{v^- + v_{CMP}}{2} \tag{3.13}$$

and their DM and CM components are related to external DM and CM components as

$$v'_D = \frac{v_D}{2}, \; v'_{CM} = \frac{v_{CM} + v_{CMP}}{2} \tag{3.14}$$

The operation of the CM extractor block shown in Figure 3.2 can be described as follows: when(OUT^+, OUT^-) = (0, 0) i.e., $v_{CM} < V_{th}$ the pull-up pMOS transistor M1 is turned on to inject a positive current into the capacitor C_{CMP} so that to increase v_{CMP} and consequently v'_{CM}. The increase of v'_{CM} makes it closer to V_{th} to enforce the condition

(3.6). Following the same principle, if (OUT^+, OUT^-) = (1, 1), the pull-down nMOS device M2 is turned on so that to decrease v'_{CM} to enforce condition (3.6). For the (1,0) and the (0,1) configurations, both M1 and M2 are off, no current is injected into $C_{CMP}$and $v_{CMP}$is signal kept constant.

An output stage, including a three-state inverter M3–M4 loaded by a capacitor $C_L$and driven by the digital signals (OUT^+, OUT^-) completes the circuit of Figure 3.2 to get a single-ended DM output analog signal from the digital outputs (OUT^+, OUT^-). M3 is turned on when(OUT^+, OUT^-) = (1, 0), so that to increase the output voltage v_{OUT} whereas M4 is turned on when (OUT^+, OUT^-) = (0, 1), so that to decrease v_{OUT}. When configurations (1, 1) and (0,0) are applied, i.e., when the CM control is active, both M3 and M4 are off and $v_{OUT}$is kept constant.

3.2 ANALYTICAL MODEL OF DIGITAL DIFFERENTIAL CIRCUIT

A mathematical model of the digital-based differential circuit introduced in this paper is proposed to get further insight into its operation. To this purpose, the state variables v_{OUT} and $v_{CMP}$of the circuit in Figure 3.2 can be expressed in terms of the external inputs by the following delay differential equations [15]

$$\begin{cases} \frac{d_{vout}}{dt} = \frac{i_{out}}{C_{out}} \\ \frac{dv_{CMP}}{dt} = \frac{i_{CMP}}{C_{CMP}} \end{cases} \tag{3.15}$$

where ,

$$i_{OUT}(t) = \begin{cases} i_{NOUT} \text{ if } (v^+(t') < V_{th} \& v^-(t') > V_{th}) \\ i_{POUT} \text{ if } (v^+(t') > V_{th} \& v^-(t') < V_{th}) \\ 0 \text{ otherwise} \end{cases}$$

$$i_{CMP}(t) = \begin{cases} i_{NCMP} \text{ if } (v^+(t'') > V_{th} \& v^-(t'') > V_{th}) \\ i_{POUT} \text{ if } (v^+(t'') < V_{th} \& v^-(t'') < V_{th}) \\ 0 \text{ otherwise} \end{cases}$$

In which i_{POUT} and i_{NOUT} are the drain current of MOSFET M3 and M4 and $i_{NCMP} and i_{PCMP}$ drain current of CM extractor. Here $t^{"} = t - t_{Dcmp}$ and $t^{'} = t - t_{Dout}$.where $t_{Dcmp} is$ propagation delay of CM extractor and t_{Dout} is propagation delay of output. The operation of the differential circuit in Figure 3.2 as a voltage comparator is explained in this section on basis of model equation (3.15). In order to simplify the calculations the following assumptions are made.

$i_{POUT} = i_{NOUT} = i_{OUT}$ and $t_{Dcmp} = t_{Dout} = t_D$.

3.3 ANALOG VOLTAGE COMPARATOR USING DIGITAL DIFFERENTIAL CIRCUIT

An analog voltage comparator using digital differential circuit is depicted in Figure3.3a, the analysis is on the basis of the equation (3.15). For this purpose, a comparator threshold $V_A = 0.7$ V and a peak amplitude sine wave input are considered.

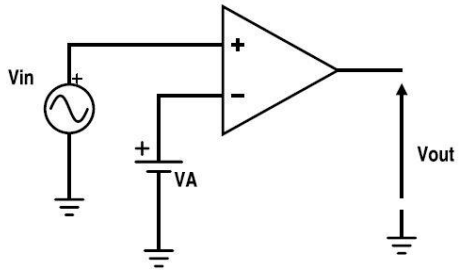


Figure 3.3a An analog voltage comparator using digital differential circuit

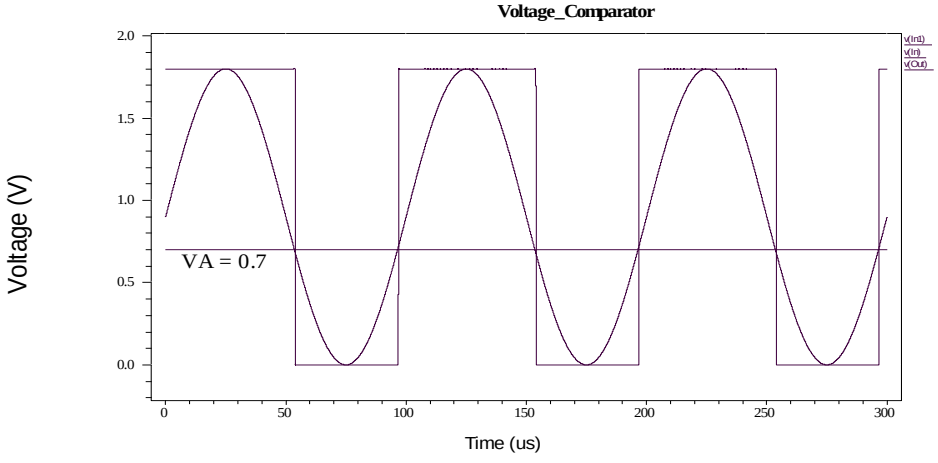


Figure 3.3b.voltage comparator circuit and simulation result.

The waveforms of the input and overall output, of the digital comparator are shown in Figure 3.3b. V_A is taken as reference voltage, with reference to the input signal output will be generated. As input $V_A > 0.7V$ output will be V_{dd}(1.8V) and $V_A < 0.7$V output will be 0v(ground). V_{CMP}Signal is generated in such a manner that the condition (3.6) will be enforced.

3.4 PERFORMANCE PARAMETER OF VOLTAGE COMPARATOR

Description of the performance of the proposed digitally enhanced analog voltage comparator circuit in terms of the some parameters such as the output voltage swing, slew rate, common mode range, offset voltage, power dissipation are to be discussed.

3.4.1 Output voltage swing

The output voltage is provided by the CMOS inverter stage in the differential circuit as shown in Fig 3. In the proposed circuit, it is shown that the rail to rail output voltage swing is obtained. Through M3 the output voltage $V_{dd}$and through M4 output voltage 0 v is obtain. So the range is ,

0 $<V_{OUT}<V_{dd}$

The simulation result is shown in Fig 4b.

3.4.2 Common Mode (CM) range

The CM input range of the differential circuit arises from the swing of the CM extractor stage in Figure 3.2.

where,

$$v'_{CM} = \frac{v_{CM}+v_{CMP}}{2} = V_{th} \quad (3.16)$$

So, $v_{CM} = 2V_T - v_{CMP}$

Now assuming $V_{th} = V_{dd}/2$ and $v_{CMP(max)} = V_{dd,} v_{CMP(min)} = 0$. so that the range of common mode is,

$0<V_{CM}<V_{dd}$

The simulation result is shown in Fig 3.3b.

3.4.3 Slew Rate

The slew rate of differential circuit is mainly limited by the Differential Mode output slew rate using equation(15), therefore related to the maximum current that can be delivered by the output stage (transistor M3 or M4 in Figure 3.2) and to the value of the output capacitance C_L give the value of slew rate. Maximum value of current is shown in Figure 3.4.

Slew rate = $\frac{i_{out}}{C_L}$

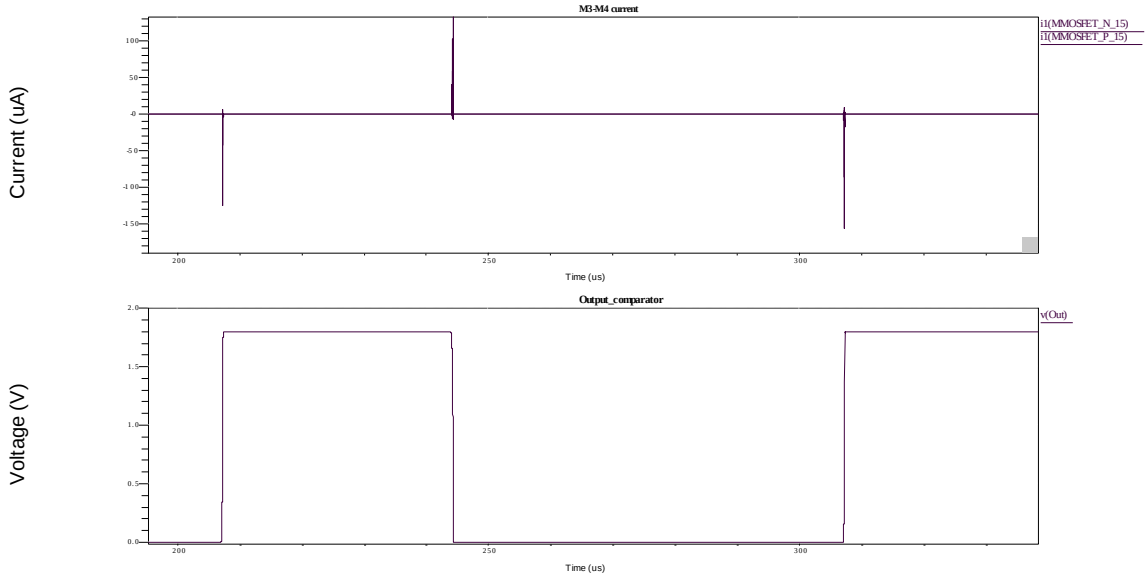


Figure 3.4 maximum current while switching in transistor M3

3.4.4 Input Offset Voltage

The proposed differential circuit in terms of DC offset can be examined with mismatch in the threshold voltages (V_{th}) and in the delays (t_D) of the buffers in Figure 3.2 It can be observed that a mismatch in the threshold voltages ($V_{th2} - V_{th1}$) gives rise to an input offset voltage. The rise time and fall time of buffer 1 and buffer 2 is shown in Figure 3.5a and Figure 3.5b respectively. On the basis of rise time and fall time value mismatch between rise time and fall time is calculated as

$$\Delta T_D = (|tr1 - tr2|) - (|tf1 - tf2|) \quad (3.17)$$

So the offset voltage can be given as

$$\text{Offset voltage } V_{off} = V_{th} + \frac{i_{out}}{C_L}\Delta T_D \quad (3.18)$$

where threshold voltage mismatch is assume to be 0.

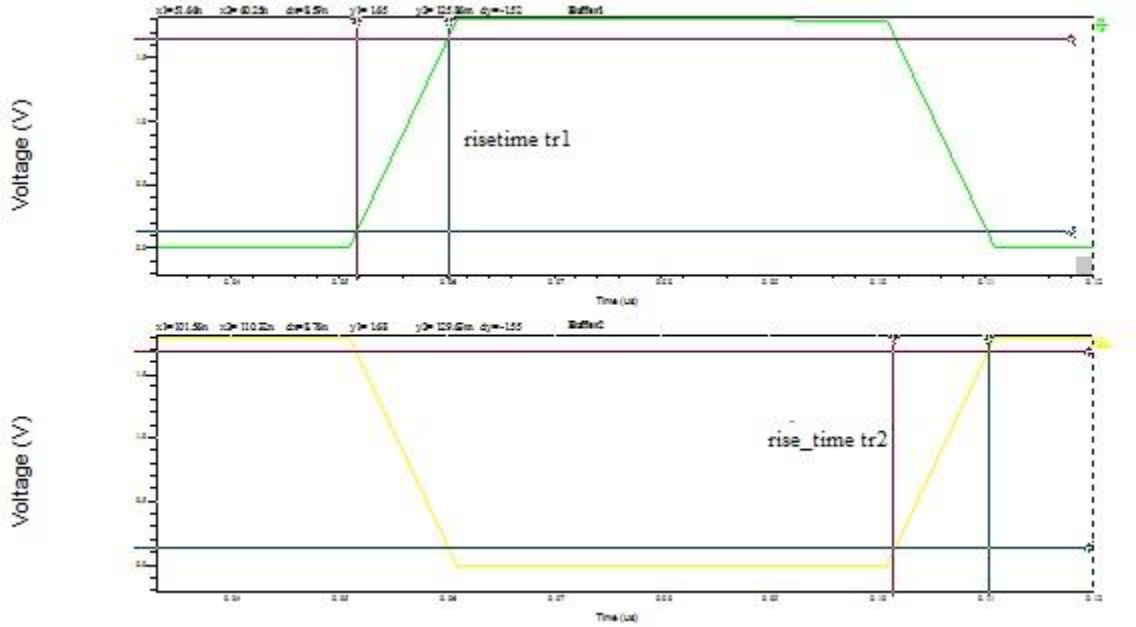


Fig. 3.5a Rise time of buffer1 and buffer2

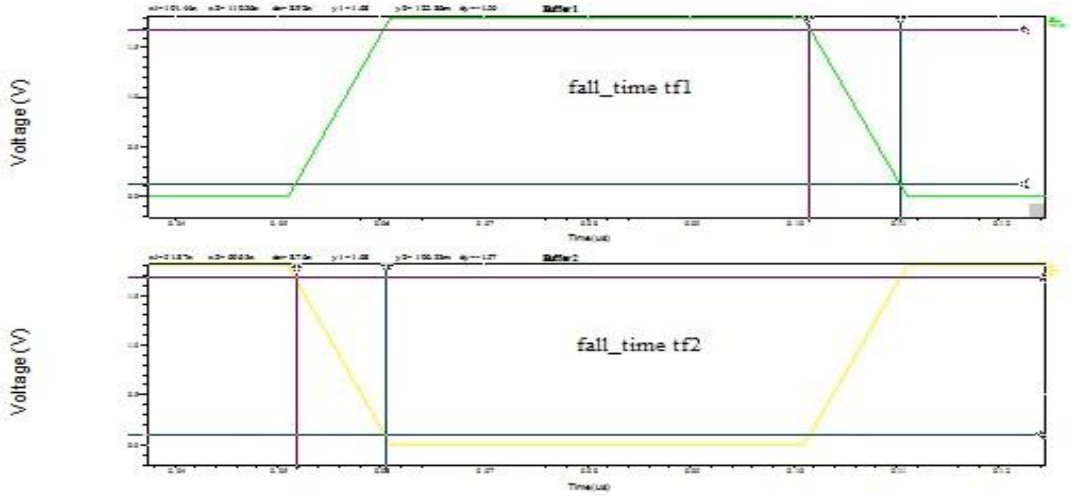


Fig. 3.5b Fall time of buffer1 and buffer2

3.4.5 Power Dissipation

In CMOS digital circuit static power dissipation is Zero therefore when there change in output signal (switching) occur the dynamic power will be dissipate. Dynamic power

depends on the value of load capacitance C_{Li} at each gate output node, square supply voltage and switching frequency used by the each gate. So that power dissipation in Fig 3 excluding driver M1-M4 can be estimated as

Dynamic power = $C_{Li}Vdd^2$ f

where $C_{Li} = C_{gs} + C_{gd} + C_{db} + C_w$ and f is the switching frequency of 10Khz.

Worst case of wiring capacitance is considered to be as 500fF [20].

$C_{gs} =$ gatetosourcecapacitance

$C_{gd} =$ gatetodraincapacitance

$C_{db} =$ drain to bulk capacitance

All these capacitance are shown in the Figure 3.6. Here bulk effect is not consider hence capacitance between source and bulk is equal to zero.

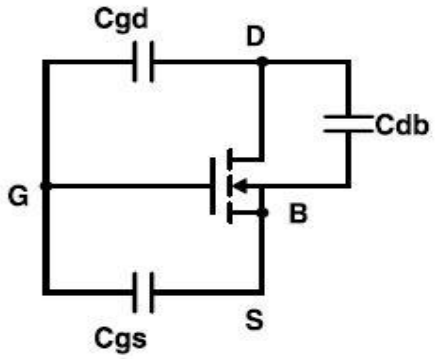


Figure 3.6 MOS capacitance

3.4.6 Resolution

Resolution of voltage comparator is the smallest difference between the input voltage and reference voltage that can be sensed. The resolution of digitally enhanced analog voltage comparator is shown in Figure3.7

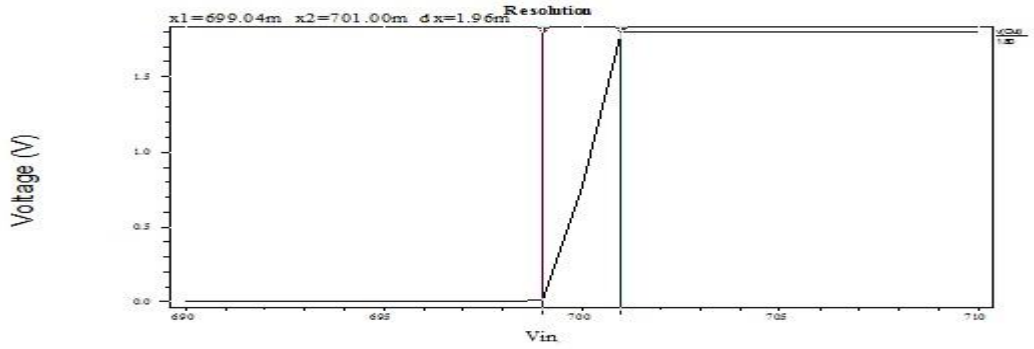


Figure3.7 Resolution of voltage comparator

From the above figure, it can be observed that the resolution of the comparator is 1.96mV.

The comparison between proposed digitally enhanced analog voltage comparator and traditional analog voltage comparator, is shown in Table 3.1.

Table 3.1. Comparison between proposed digitally enhanced analog voltage comparator and analog voltage comparators

Sr No.	Analog comparator							Digital Comparator	Proposed Work
	[16]	[17]				[18]	[19]	[15]	
		3 Stage Open Loop Comparator	Pre-amplifier based comparator	D-latch Dynamic comparator	Output buffer based comparator				
Technology (μm)	0.18	0.18	0.18	0.18	0.18	0.18	0.18	–	0.18
Supply Voltage (V)	1.5	1.8	1.8	1.8	1.8	3.3	1.8	5	1.8
Slew Rate (V/μs)	1750.87	–	–	–	–	33000	–	0.1	100
Power Dissipation (μW)	118.5	412.5	237	2.55	3.95	–	102	–	0.324
ICMR (V)	0-1.2	–		–	–	0-1.65	0-1.8	0-5	0-1.8
Offset Voltage (mV)	–	40.32	40	–	–	–	–	–	1
Resolution (mV)		486	0.0360	–	–	–	–	–	1.96
Current drawn from source (µA)	–	–	–	–	–	–	–	33000	1.2

3.5 Digitally Enhanced Differentiator

By introducing electrical reactance into the feedback loops of digital differential circuits, we can cause the output to respond to changes in the input voltage over time. The differentiator produces a voltage output proportional to the input voltage's rate of change. The digitally enhanced differentiator circuit is shown in Figure 3.8.

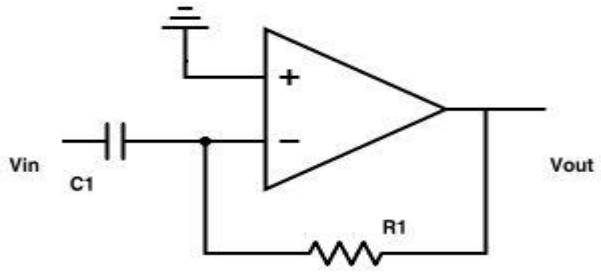


Figure 3.8 digitally Enhanced differentiator

Here, Capacitors oppose voltage change by creating current in the circuit: that is, they either charge or discharge in response to a change in applied voltage. The greater the capacitance, the more the opposition occur in a circuit. Hence if square wave is applied to the input V_{in} the output will be impulse also sine signal is converted into cosine. Simulation result of proposed digital differentiator is shown in Figure 3.9 and Figure 3.10.

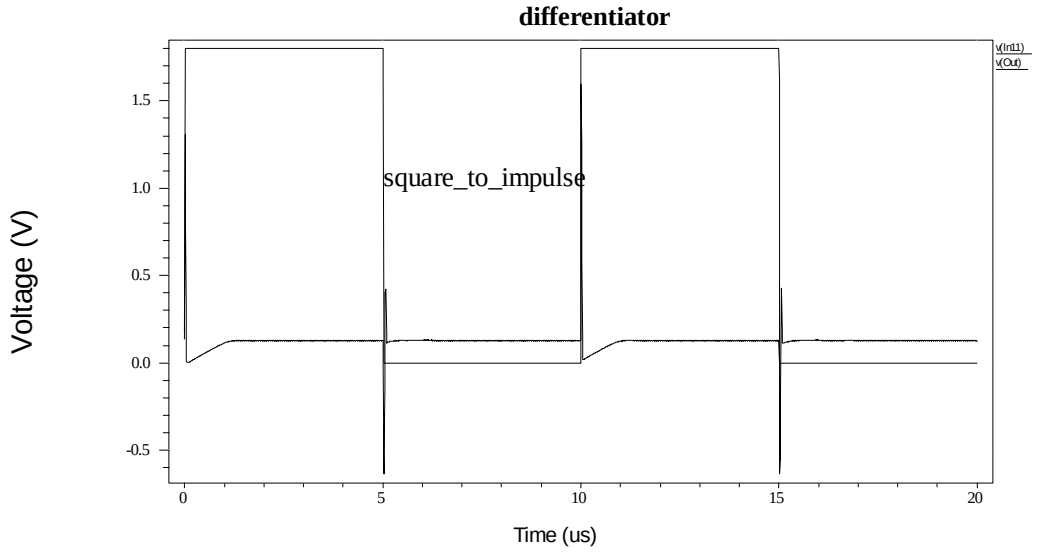


Figure 3.9 Differentiator (square to impulse)

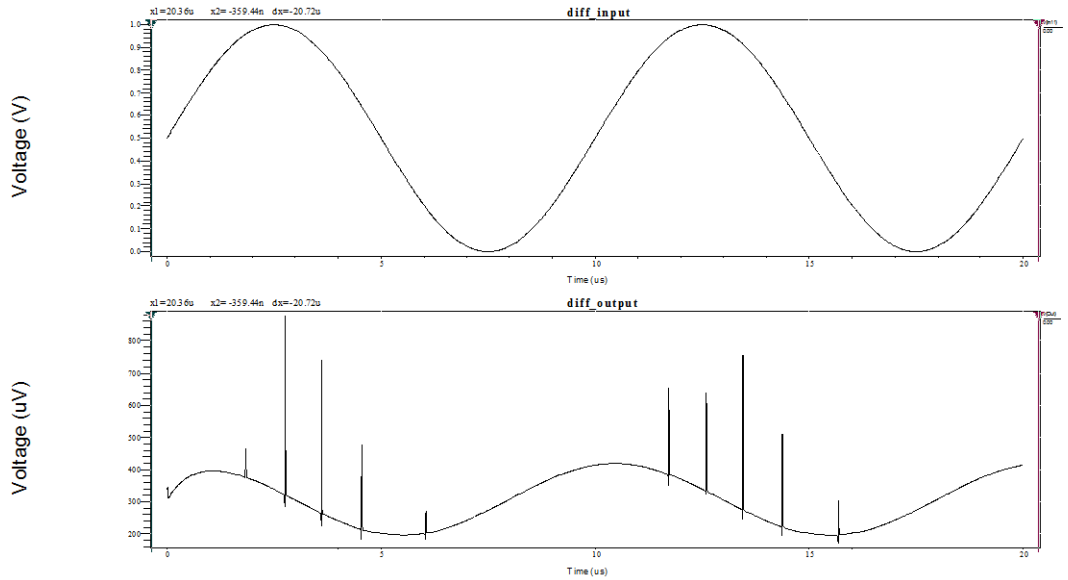


Figure 3.10 Differentiator (sine to cosine)

Due to delay in digital differential circuit phase shift error is introduced in output which is observed from Figure 3.10. This digitally enhanced differentiator can also used as square wave generator. If a triangular wave that has a steady positive going rate of change as the input voltage rises then it produces a steady positive voltage at the output. As the input voltage falls at a steady rate of change, a steady negative voltage appears at the output. The graph of the rate of change of a triangular wave is therefore a square wave. Simulation result for differentiator as square wave generator is Shown in Figure 3.11.

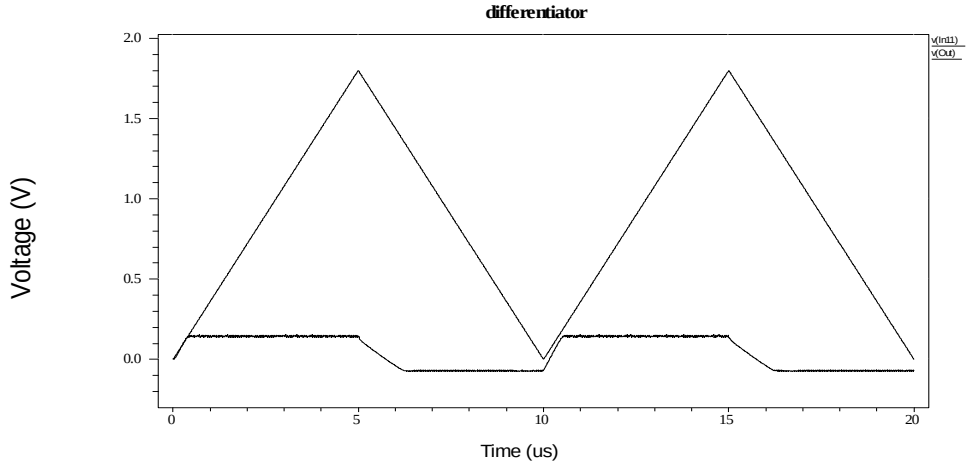


Figure 3.11 Digital Differentiator as square-wave generator

3.6 PROOF OF CONCEPT

For validation of the results discussed so far, a proof-of concept opamp circuit based on the digital differential stage in Figure 3.2 has been implemented using passive components (resistors) and has been connected in the voltage follower configuration in Figure 3.12.

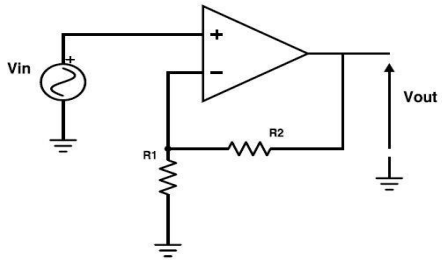


Figure 3.12. Digital differential circuit in Figure 3.2 employed as an opamp in a resistive negative feedback configuration and simulated with reference to the model (15) for β =1

Differential circuit is also used as voltage follower with value of $R_1 >> R_2$ and β = 1, result of this is shown in Figure 3.13.

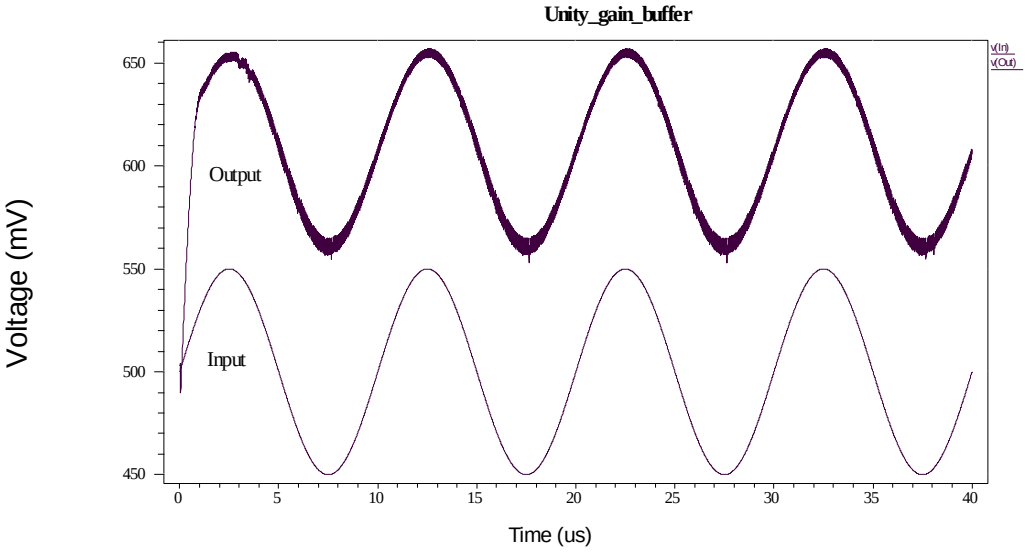


Figure 3.13. Simulation result for unity gain buffer

CHAPTER 4 FLASH ADC

In this chapter design and simulation result of digitally enhanced flash ADC is discuss. The proposed digitally enhanced analog voltage comparator is used as one of the building block of flash ADC. To design 4 bit flash ADC voltage divider, $2^4 - 1$, i.e. 15 comparators are required followed by one encoder block. In the proposed digitally enhanced flash ADC circuit sample and hold circuitry is not included as circuit is working on the assumption that the input V_{in} is available. According to applied voltage V_{in} 4 bit digital output is generated. Simulation result of digitally enhanced flash ADC in range of "0000" to "1111" is also shown.

4.1 INTRODUCTION

The need for a high speed and low power ADC is very essential for various applications. Flash ADCs are always the architecture choice where maximum sample rate and moderate resolution is needed. Even though flash ADC is the fastest type available it takes enormous amount of IC real estate to implement. The main disadvantage of flash ADC is that it need large area and dissipate large amount of power. Figure 4.1 illustrates the 4-bit flash ADC with digitally enhanced analog voltage comparator as discussed in section 3.3.

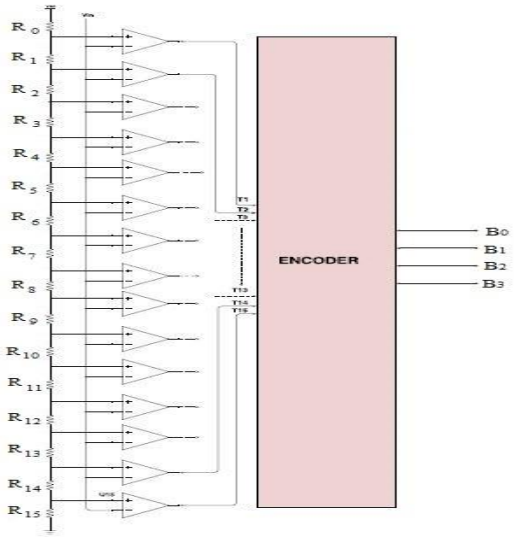


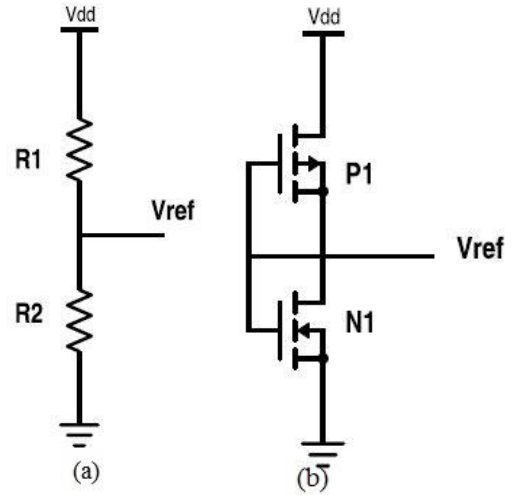
Figure 4.1 Block diagram of proposed 4 bit flash ADC

This proposed digitally enhanced flash ADC is divided into three main building blocks, which are:

1. Voltage divider
2. Digitally enhanced analog voltage comparator
3. Encoder

4.2 Voltage Divider

Reference voltages from the supply voltage can be generated by using the resistor and the MOSFET as seen in Figure 4.2(a) and Figure 4.2(b) respectively. The reference voltage formed by two resistors has the advantage of temperature insensitivity, simplicity and process insensitivity, i.e., reference voltage is not affected by sheet resistance. The circuit shown in Fig. 4.2(a) consist of two resistors which makes the circuit dissipate large amount power and also require large amount of area to fabricate. In proposed digitally enhanced 4 bit flash ADC require large number of resistors that are used to generate 15 different voltage reference levels. Due to input resistance of proposed digitally enhanced analog voltage comparator comes parallel with resistive voltage divider network there is significant voltage drop occur in reference voltage.



Resistive voltage divider Figure 4.2(a) CMOS voltage divider Figure 4.2(b)

To overcome this problem CMOS voltage divider circuit shown in Figure 4.2(b) has been designed. As output resistance of MOSFETs which are in saturation is depends on the

value of λI_D hence the reference voltages are generated by setting the ration of W/L of pMOS and nMOS. The value of output resistance can be expressed as,

$$R_o = \frac{V_A}{I_D} = \frac{1}{\lambda I_D} \tag{4.1}$$

Where λ is MOSFET device parameter which is also expressed as early voltage V_A, which is simply inverse of λ and drain current for nMOS N1 is,

$$I_D = K(V_{GS} - V_{th})^2 \tag{4.2}$$

where $K = \mu_n C_{ox} \frac{W}{L}$

μ_n = mobility of n type MOSFET

C_{ox} = oxide capacitance

Same way drain current of pMOS transistor P1 can also be expressed.

However, the problem of threshold voltage drop occurs in different CMOS circuit which is also occur in the circuit shown in Fig. Xb therefore the output level equal to V_{dd} or in between $V_{dd} - V_{th}$ cannot be achieved. To overcome this problem voltage bootstrapping technique is used to create reference voltage equal to 1.68 V also the same circuit is used to create low reference voltage of flash ADC equal to 0.12 V. Voltage levels between 1.56V to 0.24 is shown in Figure 4.3.

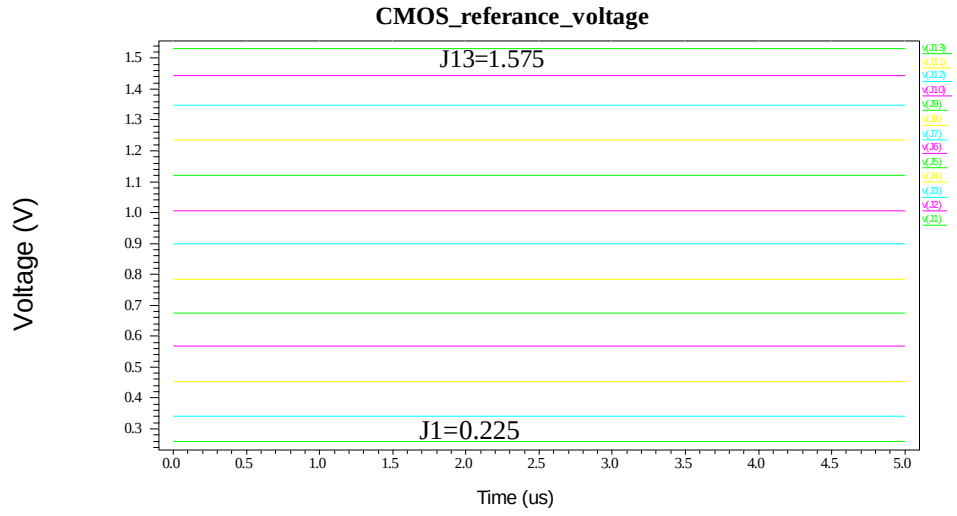


Figure 4.3 Simulation result of CMOS voltage divider (0.24V-1.56V)

The schematic view of CMOS voltage divider circuit in which 13 different voltage levels are generated is shown in Figure 4.4. J(n) is the reference voltage where 'n' varies from 1 to 13.

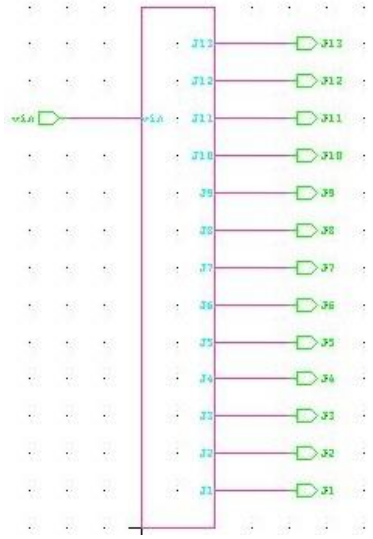


Figure 4.4 Schematic view of CMOS voltage divider

4.2.1 VOLTAGE BOOTSTRAPPING

In different digital circuits such as pass transistor gates, enhancement load inverter output level may suffer from threshold voltage drop. Voltage bootstrapping is the technique which is used to overcome the problem of threshold voltage drop. Voltage bootstrapping techniques offer a simple yet effective way to overcome threshold voltage drop which occur in most situation. Consider the circuit shown in Figure 4.5, where supply voltage V_x is smaller than the power supply voltage, $V_x \leq V_{dd}$. Consequently, the nMOS transistor M2 will remain in saturation so that the output voltage is limited by,

$$V_{out}(max) = V_x - V_{th2}(V_{out}) \tag{4.3}$$

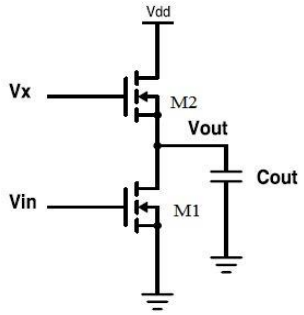


Figure 4.5 Enhancement type circuit in which outut node is weakly driven

To overcome the threshold voltage drop and to obtain a full logic-high level (V_{dd}) at the output node, the voltage V_x must be increased. For that, consider the circuit shown in Figure 4.6, where one transistor M3 is added to the circuit with 2 coupling capacitors C_s and C_{boot} which dynamically couple the output voltage V_x to the ground and to the output, respectively. Here, high voltage V_x is produce during switching, so that the threshold voltage drop can be overcome at the output node.

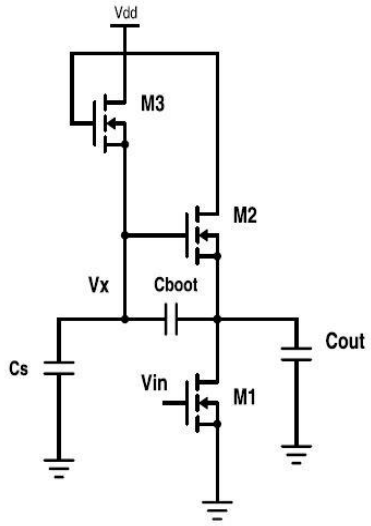


Figure 4.6 Dynamic voltage bootstrapping arrangement to boost V_x during switching

Operation of the circuit shown in Figure 4.6 is as follows:

Initially assume that the input voltage V_{in} is logic high, therefore M1 and M2 transistors have a nonzero drain current and that the output voltage is low. At this time, M1 is in the linear region and M2 is in saturation region. Since current through transistor M3 is zero, the initial condition for the voltage V_x can be found as

$$V_x = V_{dd} - V_{th3}(V_x) \quad (4.4)$$

Now, assume that the input voltage V_{in} is switching from logic high to 0 V at t=0, therefore the driver transistor M1 will turn off and output voltage will start to increase. During the charge up event, the bootstrap capacitor, i.e., C_{boot} will couple the change in output voltage level to V_x. Now, assuming two current components are approximately equal, proportional increase in the voltage V_x can be written by using equation,

$$V_x = (V_{dd} - V_{th3}) + \frac{Cboot}{(Cs + Cboot)} (V_{dd} - V_{ol}) \quad (4.5)$$

If the capacitor C_{boot} is much larger than C_s($C_{boot} \gg C_s$) , the maximum value of V_x can be approximated as,

$$V_x(\max) = 2V_{dd} - V_{th3} - V_{ol} \quad (4.6)$$

This proves that voltage bootstrapping can significantly boost the voltage level V_x. Now, in order to overcome the threshold voltage drop at the output, the minimum required voltage level V_x is,

$$V_x = V_{dd} + V_{th2} \mid V_{out} = V_{dd} \quad (4.7)$$

The result of voltage bootstrapping circuit is shown in the Figure 4.7.

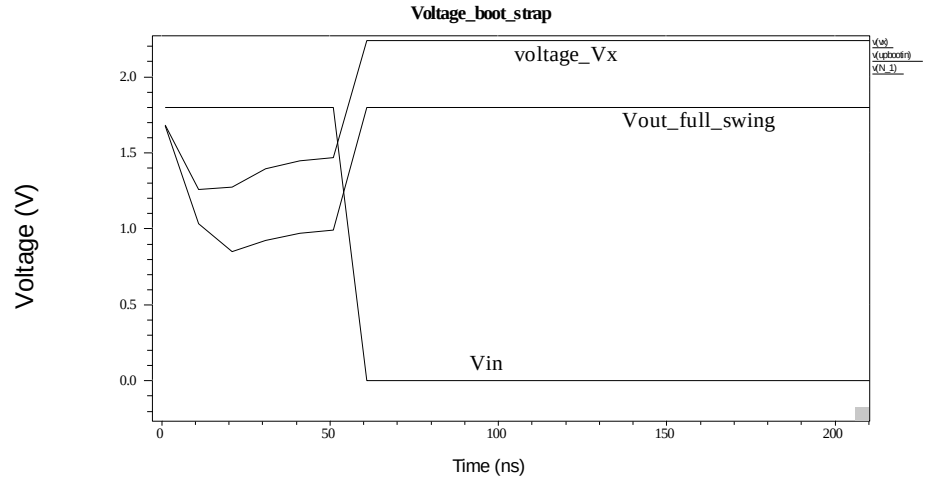


Figure 4.7 Simulation result of voltage bootstraping circuit at node V_x

From the Figure 4.7 it is observed that the full swing of output can be achieved by adjusting proper coupling between C_{boot} and C_s. The same concept is used to generate high voltage level of 1.68 V and low voltage 0.12 V which is not generated by CMOS voltage divider circuit. For generating high voltage level and low voltage level input pulse period of V_{in} is taken precisely. The high reference voltage of 1.68 V and low reference voltage of 0.12 V is shown in Figure 4.8(a) and Figure 4.8(b) respectively.

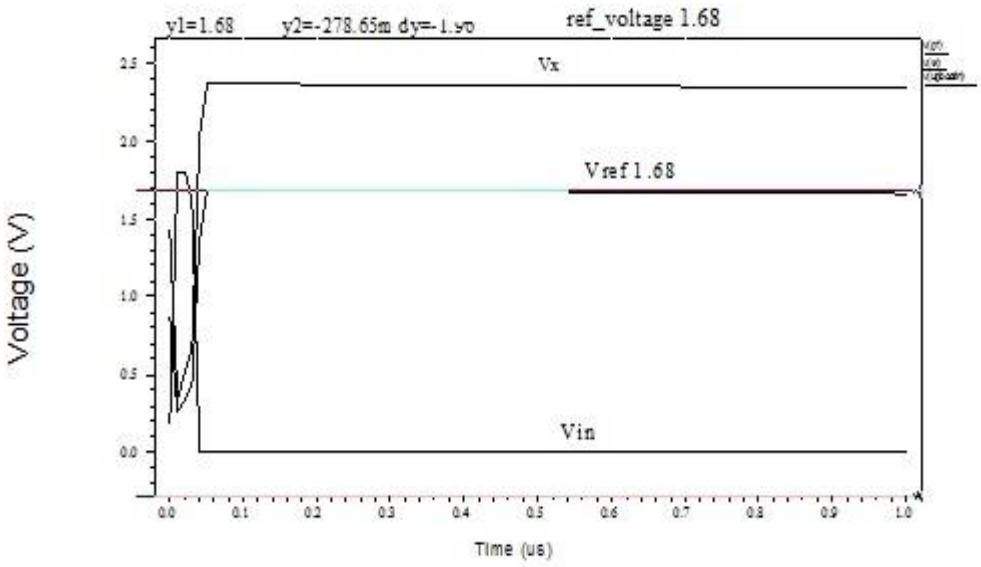


Figure4.8(a) generated reference voltage 1.68V

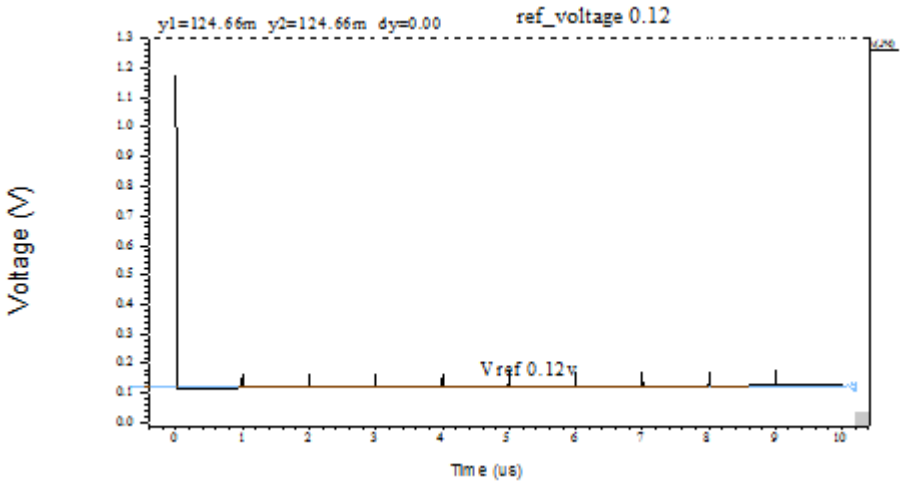


Figure 4.8(b) generated reference voltage 0.12V

4.3 DIGITALLY ENHANCED ANALOG VOLTAGE COMPARATOR

In the proposed digitally enhanced flash ADC circuit consists second important block, digitally enhanced analog voltage comparator which compares the input signal V_{in} with the value of reference voltage generated by CMOS voltage divider circuit applied at second node of comparator. Parallel connected 15 comparators generate 15 bit thermometer code which is given to encoder block which convert thermometer code into binary code. Here, voltage comparator whose behavior is discussed in chapter 2 is used hence power consumption of proposed circuit is reduced significantly. With value input

signal V_{in}=0.4 the corresponding thermometer code generated by is 15 comparator shown in Figure 4.9.

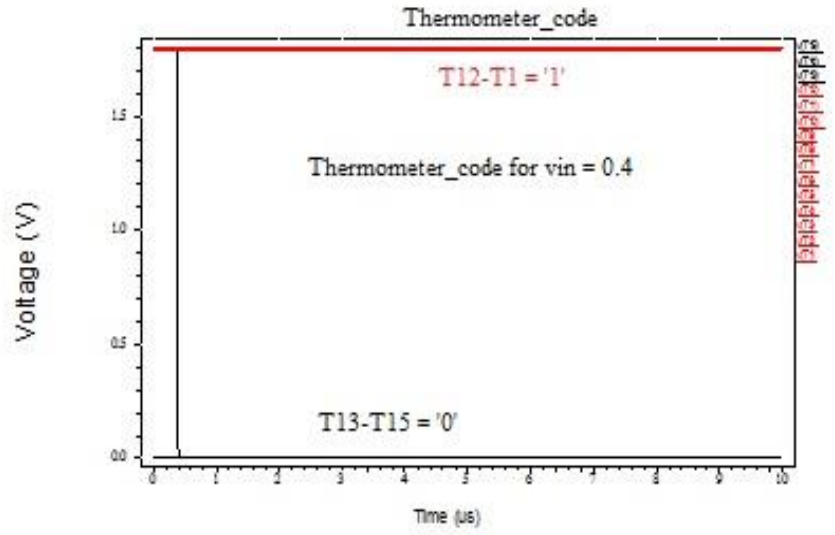


Figure 4.9 Thermometer code for V_{in}=0.4 V

4.4 ENCODER BLOCK

Flash ADC consists of combination of parallel structured comparators whose output will be in thermometer code format.The attained output in the form of mercury column in thermometer at comparator ends will be according to the signal strength at input ends. Flash ADC consists of $2^n - 1$ comparators where as each comparator produce one bit comparison output. Accordingly, the output of comparator array, thermometer code will be consisting of $2^n - 1$ bits.

Thermometer to binary code encoder is used to convertthermometer code into binary form. The encoder shown in Fig X plays an important role in the speed of proposed digitally enhanced flash ADC. For the conversion of thermometer code to binary code, various methods such as intermediate gray code based architecture using basic gates and direct conversion using multiplexers, have already been introduced. Truth table for thermometer code and its corresponding binary code is generated by using gray code based architecture is given in Table 4.1.

Table 4.1 Thermometer code to binary code

Sr No.	Thermometer Code															Binary Code			
	T 15	T 14	T 13	T 12	T 11	T 10	T 9	T 8	T 7	T 6	T 5	T 4	T 3	T 2	T 1				
1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
2	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0	0	0	1
3	0	0	0	0	0	0	0	0	0	0	0	0	0	1	1	0	0	1	0
4	0	0	0	0	0	0	0	0	0	0	0	0	1	1	1	0	0	1	1
5	0	0	0	0	0	0	0	0	0	0	0	1	1	1	1	0	1	0	0
6	0	0	0	0	0	0	0	0	0	0	1	1	1	1	1	0	1	0	1
7	0	0	0	0	0	0	0	0	0	1	1	1	1	1	1	0	1	1	0
8	0	0	0	0	0	0	0	0	1	1	1	1	1	1	1	0	1	1	1
9	0	0	0	0	0	0	0	1	1	1	1	1	1	1	1	1	0	0	0
10	0	0	0	0	0	0	1	1	1	1	1	1	1	1	1	1	0	0	1
11	0	0	0	0	0	1	1	1	1	1	1	1	1	1	1	1	0	1	0
12	0	0	0	0	1	1	1	1	1	1	1	1	1	1	1	1	0	1	1
13	0	0	0	1	1	1	1	1	1	1	1	1	1	1	1	1	1	0	0
14	0	0	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	0	1
15	0	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	0
16	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1

Thermometer code to Binary code conversion circuits are considered as the bottleneck in the design of Flash ADCs. Since the speed of the entire circuit is affected by this digital encoder of complete architecture, choosing a perfect design for encoder is become very important.

4.4.1 GRAY CODE BASED ENCODER USING BASIC GATES

In the proposed digitally enhanced flash ADC circuit the thermometer code is directly converted to its corresponding gray code and then the gray code is converted to binary. The corresponding thermometer code to gray code and gray code to binary code are shown in Table 4.2 and Table 4.3 respectively. This technique is highly power efficient. Other than power efficiency, conversion of thermometer code to gray code using gates will help in reducing the bubble errors. The conversion of gray code to binary code is done using the basic logic gates (AND, OR and INVERTER).

Table 4.2 Thermometer code to Gray code

Sr No.	Thermometer Code															Gray Code			
	T 15	T 14	T 13	T 12	T 11	T 10	T 9	T 8	T 7	T 6	T 5	T 4	T 3	T 2	T 1				
1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
2	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0	0	0	1
3	0	0	0	0	0	0	0	0	0	0	0	0	0	1	1	0	0	1	1
4	0	0	0	0	0	0	0	0	0	0	0	0	1	1	1	0	0	1	0
5	0	0	0	0	0	0	0	0	0	0	0	1	1	1	1	0	1	1	0
6	0	0	0	0	0	0	0	0	0	0	1	1	1	1	1	0	1	1	1
7	0	0	0	0	0	0	0	0	0	1	1	1	1	1	1	0	1	0	1
8	0	0	0	0	0	0	0	0	1	1	1	1	1	1	1	0	1	0	0
9	0	0	0	0	0	0	0	1	1	1	1	1	1	1	1	1	1	0	0
10	0	0	0	0	0	0	1	1	1	1	1	1	1	1	1	1	1	0	1
11	0	0	0	0	0	1	1	1	1	1	1	1	1	1	1	1	1	1	1
12	0	0	0	0	1	1	1	1	1	1	1	1	1	1	1	1	1	1	0
13	0	0	0	1	1	1	1	1	1	1	1	1	1	1	1	1	0	1	0
14	0	0	1	1	1	1	1	1	1	1	1	1	1	1	1	1	0	1	1
15	0	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	0	0	1
16	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	0	0	0

Table 4.3 Gray code to Binary code

Sr No.	Gray Code				Binary Code			
1	0	0	0	0	0	0	0	0
2	0	0	0	1	0	0	0	1
3	0	0	1	1	0	0	1	0
4	0	0	1	0	0	0	1	1
5	0	1	1	0	0	1	0	0
6	0	1	1	1	0	1	0	1
7	0	1	0	1	0	1	1	0
8	0	1	0	0	0	1	1	1
9	1	1	0	0	1	0	0	0
10	1	1	0	1	1	0	0	1
11	1	1	1	1	1	0	1	0
12	1	1	1	0	1	0	1	1
13	1	0	1	0	1	1	0	0
14	1	0	1	1	1	1	0	1
15	1	0	0	1	1	1	1	0
16	1	0	0	0	1	1	1	1

Here, firstly thermometer code generated by 15 digitally enhanced comparators is converted into gray code using basic gates (AND OR and NOT), the equations are shown below :

$$G_3 = T_8$$

$$G_2 = T_4\overline{T_{12}}$$

$$G_1 = T_2\overline{T_6} + T_{10}\overline{T_{14}}$$

$$G_0 = T_1\overline{T_3} + T_5\overline{T_7} + T_9\overline{T_{11}} + T_{13}\overline{T_{15}}$$

These gray codes are finally converted to Binary codes using the general gray to binary code converter equations using XOR gates.

$$B_3 = G_3$$

$$B_2 = B_3\ xor\ G_2$$

$$B_1 = B_2\ xor\ G_1$$

$$B_0 = B_1\ xor\ G_0$$

The circuit diagram for this architecture is shown in Figure 4.10.

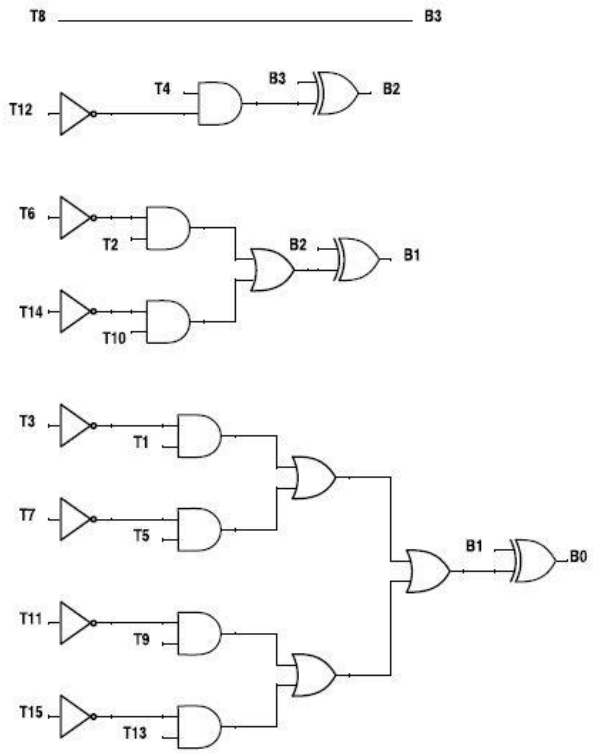


Figure 4.10 CMOS encoder using gates

By combining all the three blocks discussed in this chapter complete flash ADC has been designed. Here sample and hold circuitry is not designed to sample analog signal. Flash ADC is designed on the basis of assumption that sampled signal is available. More accurate flash ADC can be designed by using proper sample and hold circuitry to generate input voltageV_{in}.

4.5 SIMULATION RESULT

By combining three main building blocks, *i.e.* voltage divider, digitally enhanced analog voltage comparator and encoder, the flash ADC is designed.

4.5.1 Flash ADC

The simulation result of proposed digitally enhanced flash ADC circuit is seen in Figure 4.11. This figure clearly shows that as V_{in} increases, the output of the flash ADC goes from "0000" to "1111".

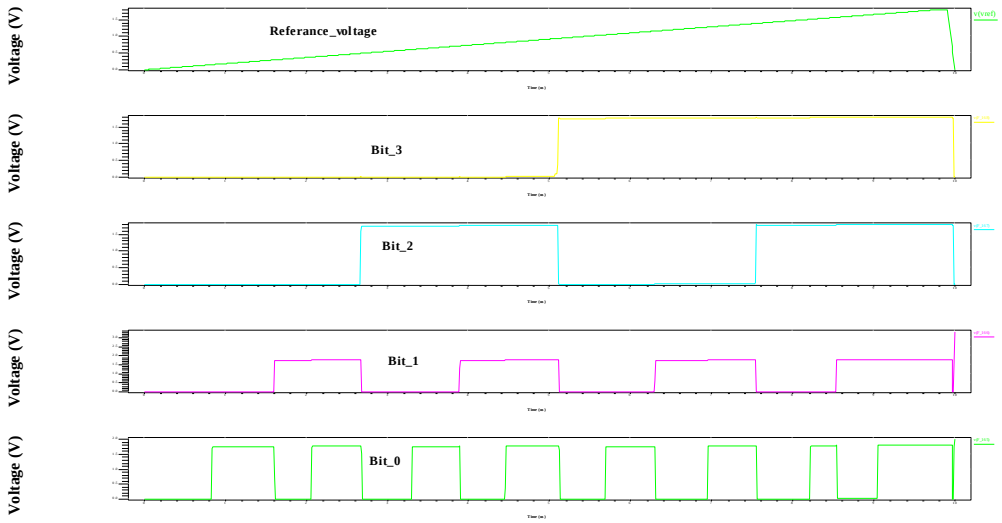


Figure 4.11 Flash ADC output ("0000"- "1111")

4.5.2 INL and DNL

By using result of proposed digitally enhanced flash ADCintegral nonlinearity and differential nonlinearity (DNL) is calculated. The result of INL and DNL is shown in Figure 4.12. It is observed that differential nonlinearity, i.e.,the Deviation of transition code width from the ideal one is 0 LSB also integral nonlinearity (INL) of flash ADC, *i.e.*, the maximum difference between the actual finite resolution characteristic and the ideal finite resolution characteristic is 0.5 LSB.

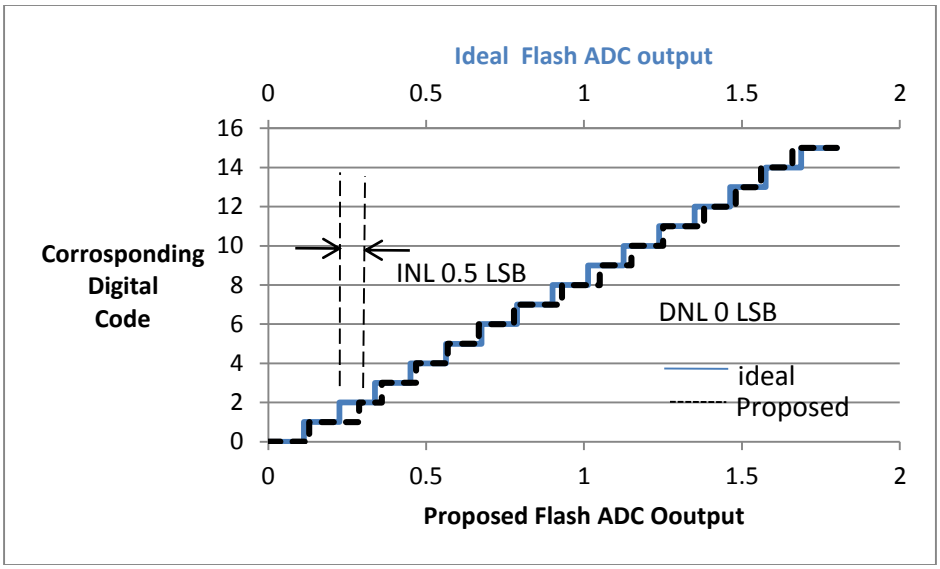


Figure 4.12 INL and DNL of propose flash ADC

Summary

The proposed, digitally enhanced flash ADC is compared with previously available flash ADC. For comparison, parameters such as resolution, propagation delay, power consumption, INL, DNL are used. All comparison of these parameter is shown in Table 4.4.

Table 4.4 Comparison of proposed flash ADC

Author	M. O. Shaker and S. Gosh	J. I. Lee and J. I. Song	M. I. Titu and J.K. Antony	This Work
Year	2009	2013	2014	
Design Methodology	Analog	Analog	Mixed	Digital
Technology (nm)	90	180	90	180
Resolution	6 bit	6 bit	4 bit	4bit
Power Consumption(mW)	72	0.4	23	0.02
Supply Voltage (V)	0.6	1	1.2	1.8
INL	-	-	-	0.5 LSB
DNL	-	-	-	0 LSB

CHAPTER 5 CONCLUSION AND FUTURE SCOPE

5.1 CONCLUSION

In this work, a novel smart analog circuit of flash ADC is designed in which digitally enhanced analog voltage comparator is deployed using digital differential circuit. Since the fabrication of pure CMOS digital circuit is easier and analog circuit produces more delay, therefore proposed design enhances the speed of the circuit. As proposed circuit implementation is purely digital, it is also seen that effect of noise in the circuit is minimized. The digitally enhanced analog voltage comparator has been found to have lower power dissipation, higher resolution, lower DC offset, fuller output swing and wider input common mode range (ICMR) than analog voltage comparators available in literature so that the overall power consumption of digitally enhanced flash ADC is significantly reduced. A digitally enhanced flash ADC with resolution of 4 bits and INL of 0.5 LSB is designed which consume less power at supply voltage 1.8V in 180nm technology. In this work, differentiator (square wave generator) is also designed by using digital differential circuit. The concept of digital differential circuit has also been proven by connecting the digital differential circuit in the unity gain configuration.

5.2 FUTURE SCOPE

In future, more precise digitally enhanced flash ADC can be designed.. High resolution flash ADC can also be designed by using digitally enhanced voltage comparator circuit. Layout of proposed circuit is also considered as future work. However, different types of ADC such as SAR ADC, pipelined ADC in which voltage comparator is being used are also designed by using same concept.

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