DESIGN AND ANALYSIS OF FULLY DIFFERENTIAL DOUBLE-TAIL DYNAMIC COMPARATOR USING CHARGE SHARING TECHNIQUE

A Thesis submitted in partial fulfillment of the requirement for the Award of the Degree of

MASTER OF TECHNOLOGY

in

VLSI Design

Submitted By

Sanchita Chaudhary

601762015

Under Supervision of

Dr. Rishikesh Pandey
Assistant Professor

THAPAR INSTITUTE
OF ENGINEERING & TECHNOLOGY
(Deemed to be University)

ELECTRONICS AND COMMUNICATION ENGINEERING DEPARTMENT
THAPAR INSTITUTE OF ENGINEERING & TECHNOLOGY
(A DEEMED TO BE UNIVERSITY), PATIALA, PUNJAB
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DECLARATION

I, **Sanchita Chaudhary** hereby declare that the work presented in this thesis entitled "**Design and Analysis of fully differential double-tail dynamic comparator using charge sharing technique**" in partial fulfillment of the requirement for the award of degree of **Master of Technology (VLSI Design)** submitted at **Department of Electronics And Communication Engineering**, Thapar Institute of Engineering & Technology (Deemed to be University), Patiala is an authentic record of work carried out under supervision of **Dr. Rishikesh Pandey** (**Assistant Professor, Department of Electronics And Communication Engineering, Thapar Institute of Engineering and Technology**) from August, 2017 to July, 2019. The matter presented in this has not been submitted either in part or full to any other university or institute for the award of any other degree.

Date: 8/8/19

(Sanchita Chaudhary)
(601762015)

It is certified that the above statement made by the candidate is correct to the best of my knowledge and belief.

Date: 8/8/19

Dr. Rishikesh Pandey
Assistant Professor
Department of Electronics and Communication Engineering
Thapar Institute of Engineering & Technology
(A deemed to be University), Patiala, Punjab.

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ABSTRACT

In today's fast moving digital world, it becomes necessary to come up with an innovation in digitization constantly. An important component in a semiconductor Integrated Circuit (IC) industry is an Analog-to-Digital Converter (ADC). Various portable devices which are used in communication systems, precision data acquisition systems, medical instruments, etc. require ADCs which consumes low power and provides high speed. The comparator is a pivotal building block in any ADC architecture. To meet the demand for low-voltage/low-power and high speed ADCs a new fully differential double-tail dynamic comparator using charge sharing technique (FDDCCST) is proposed in this research work. To lower the power consumption and speed up the comparison process, a charge sharing technique is employed in the latch stage of the proposed FDDCCST. In the proposed FDDCCST differential pair and double-tail comparator topologies are combined to minimize the offset voltage. Also, a detailed analysis of the proposed FDDCCST which includes delay analysis, power analysis and mismatch analysis is explained in this thesis. The proposed FDDCCST has been designed and simulated in 0.18μm CMOS technology with supply voltages of ± 0.75 V using Cadence Virtuoso Analog Design Environment. Simulation results verify that the proposed FDDCCST has worst case delay of 0.219 ns with power dissipation of 156.3 μW. The offset voltage is 0.184 mV with 1σ deviation of 7.65 mV. The proposed FDDCCST is faster, power efficient with low offset voltage than the existing dynamic comparator structures.

TABLE OF CONTENTS

LIST OF FIGURES

LIST OF TABLES

ABBREVIATIONS

ADC	Analog-to-Digital Converter
CMOS	Complementary Metal Oxide Semiconductor
DTDC	Double-Tail Dynamic Comparator
FDDCCST	Fully differential Double-tail Dynamic Comparator using Charge Sharing Technique
IC	Integrated Circuits
MOSFET	Metal Oxide Semiconductor Field Effect Transistor
MDTDC	Modified Double-Tail Dynamic Comparator
NMOS	n – type Metal Oxide Semiconductor
PMOS	p – type Metal Oxide Semiconductor
PDP	Power-Delay Product
STDC	Single-Tail Dynamic Comparator
VCCS	Voltage-Controlled Current Source

CHAPTER 1
INTRODUCTION

Since last few years, in semiconductor industry the number of functional and logical blocks integrated on a single chip gradually increases. Due to which the demand for low-power and high performance functional blocks increases. Data convertors such as analog-to-digital convertors (ADCs) that connect analog world with the digital systems become the constituent component. ADCs are widely acceptable in the industry as they provide low-power consumption, high speed and smaller area on a die. The comparator is the pivotal component in any ADC architecture as it has a strong relation with the accuracy of such convertors. A comparator is a device which takes two signals as an input, compares them and provides a digital output indicating which input signal is larger. This chapter presents conventional comparator architecture. Section 1.1 presents the functionality of the architecture and section 1.2 derives the time constant for latch stage. Section 1.3 presents the motivation behind the research work followed by organization of the thesis in section 1.4.

1.1 ARCHITECTURE OF CONVENTIONAL COMPARATOR

The symbol used for a comparator is shown in Figure 1.1 [1]. The comparator is a decision making device wherein whenever input signal V_p (positive terminal) of the comparator is larger than the input signal V_m (negative terminal) at that point the comparator gives output as logic 1 (V_{DD}) though whenever input signal V_p is not larger than V_m then the comparator gives output as logic 0 (ground).

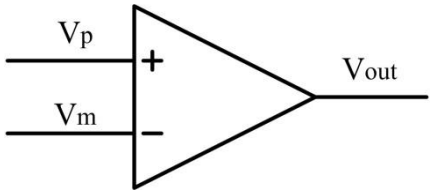

Figure 1.1 Symbol of comparator [1]

A block diagram of a conventional high speed comparator is diagrammatically presented in Figure 1.2 [1]. The comparator works in three stages namely (a) the input preamplifier circuit, (b) a positive feedback or a latch stage and (c) an output buffer. One or two preamplifier circuit stages are used in high speed comparators whose output is given to the latch circuit. The preamplifier circuit amplifies the input signal which improves the sensitivity of the comparator (i.e., increasing input signal to the voltage level so that the comparator can efficiently reach to a decision) and insulates the comparator input from a switching noise commonly known as kick-back noise which comes from the positive feedback stage. A latch stage or a positive feedback stage comprises of cross-coupled inverters used to determine the larger input signal. Finally, the output buffer amplifies the output coming from the latch stage and provides a digital signal as an output [1].

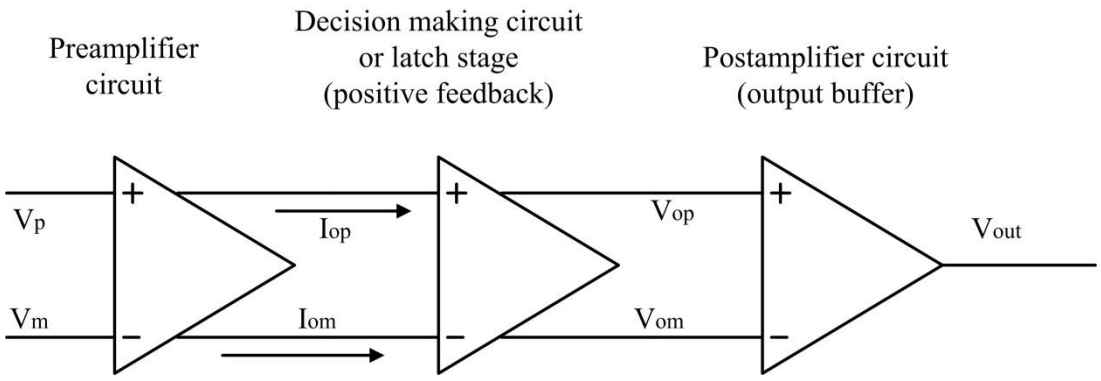

Figure 1.2 Block diagram of a voltage comparator [1]

1.1.1 Preamplifier circuit

The input signal is amplified at this stage to achieve high resolution and to minimize the effect of kick-back noise. The preamplifier circuit has the gain typically in the range of 4 to 10. Sometimes unity gain buffer can be used as preamplifier if high speed but moderate resolution is required. If the gain of the preamplifier becomes greater than 10, then its time constant becomes large which limits the speed of the circuit. Practically, it is not advised to eliminate the preamplifier because accuracy of the comparator is affected by the presence of kick-back noise. Kick-back noise is defined as the transferring of charge either in or out of the input whenever the latch circuit switches its mode from track to latch. Transferring of charge occurs because of the charge required to turn on the transistors in positive feedback circuit and by the removal of charge to turn off the transistors in tracking circuit. Without a preamplifier in the first stage, this kick-back noise will enter into the driving circuitry which causes large glitches [2].

1.1.2 Decision making circuit

The decision making circuit also known as latch stage is employed for comparing the two input voltages by the means of positive feedback and find which input voltage is larger. Although, the output of preamplifier circuit is more than the comparator input yet it is less than the demanded voltage to drive the digital circuitry. Latch stage amplifies this voltage level in track mode as well as in latch mode when the positive feedback in enabled. Analog signal is regenerated into full scale digital signal by the positive feedback circuitry. This stage reduces the total gain stages desired to obtain a good resolution which makes them faster than the multistage architectures [2].

1.1.3 Post amplification circuit

This stage uses output buffer circuit to amplify the signal and provides the final output as the valid logic levels (either V_{DD} or ground). The output buffer accepts differential input signal and it ought not to have any slew-rate limitations [1].

One important consideration while designing the comparator is to make sure that no memory is passed on from one decision cycle to next decision cycle. For this, different stages are reset before moving into the track mode. This can be achieved by joining the internal nodes of a comparator either to supply voltage or to ground. This can also be done by connecting differential nodes together with the help of switches before entering the track mode. It also helps to get the valid logic levels before the latch mode [2]. Another factor which influences the performance of a comparator is scaling down of the supply voltage to get low-power. As a result sub threshold leakage comes into consideration which reduces the rail voltage of a comparator if the threshold voltages of the transistors are not scaled according to the rail voltages. Furthermore, to obtain a low offset voltage in comparators, aspect ratios of the input transistors have to be increased. As a result, the area of the comparator is increased which will lead to more power consumption. Therefore, a trade-off between speed, power, offset and area is taken into consideration while designing a comparator. Speed and accuracy of the comparator is compromised if low-power and area is required whereas if high speed and low offset is the major concern, then more power and area are required.

1.2 TIME CONSTANT FOR LATCH STAGE

To calculate the time constant of the latch stage when it is used in positive feedback phase, a simplified circuit which comprises of two back-to-back inverters is used as shown in Figure 1.3 [2].

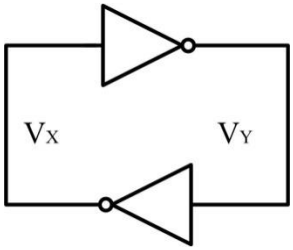

Figure 1.3 Circuit of latch stage [2]

At the beginning of the latch phase, it is assumed that the voltages at the output of both the inverters V_X and V_Y are close to each other. Thus, the inverters work in linear region and can be modelled as Voltage-Controlled Current Source (VCCS) which drives an RC load. A linearized model of latch stage is shown in Figure 1.4 [2].

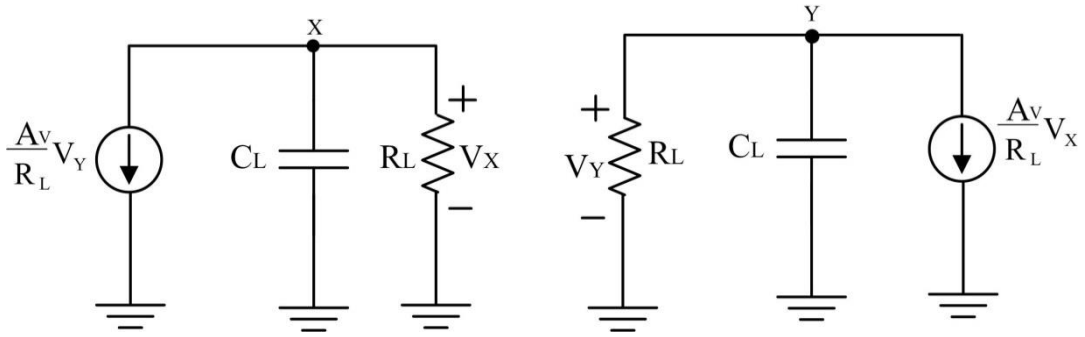

Figure 1.4 A linearized model of latch stage when it is working in latch phase [2]

Equations (1.1) and (1.2) can be obtained by applying KCL at node 'X' and 'Y' in the linearized model.

$$\frac{A_V}{R_L}V_Y = -C_L\frac{dV_X}{dt} - \frac{V_X}{R_L} \tag{1.1}$$

$$\frac{A_V}{R_L}V_X = -C_L\frac{dV_Y}{dt} - \frac{V_Y}{R_L} \tag{1.2}$$

where A_V is the gain of each inverter at low frequency having transconductance equal to $G_m = A_V / R_L$. Multiplying Equations (1.1) and (1.2) with R_L and rearranging gives

$$\tau\frac{dV_X}{dt} + V_X = -A_V V_Y \tag{1.3}$$

$$\tau\frac{dV_Y}{dt} + V_Y = -A_V V_X \tag{1.4}$$

where $\tau = R_L C_L$ is the time constant of each inverter at the output node.
Subtracting Equation (1.4) from Equation (1.3) gives

$$\left(\frac{\tau}{A_V - 1}\right)\left(\frac{d\Delta V}{dt}\right) = \Delta V \tag{1.5}$$

where ΔV denotes the difference between the two output voltages V_X and V_Y.
Equation (1.5) is in the form of first order differential equation and its solution can be obtained as

$$\Delta V = \Delta V_o e^{(A_V - 1)t/\tau} \tag{1.6}$$

where ΔV_0 represents the initial output difference voltage of the inverters at the starting of the latch phase.
Equation (1.6) depicts that ΔV_0 rises exponentially with respect to time. The time constant is defined as

$$\tau_{latch} = \frac{\tau}{A_V - 1} \cong \frac{R_L C_L}{A_V} = \frac{C_L}{G_m} \tag{1.7}$$

For MOS devices, output load capacitance is given by

$$C_L = K_1 W L C_{ox} \tag{1.8}$$

where C_{ox} is the gate-oxide capacitance and K_1 is the proportionality constant.
In addition, the transconductance of the inverter is given by

$$G_m = K_2 g_m = K_2 \mu_n C_{ox}\frac{W}{L}V_{eff} \tag{1.9}$$

where K_2 is in the range of 0.5 to 1.

Substituting the value of C_L and G_m from Equations (1.8) and (1.9) in Equation (1.7) gives

$$\tau_{latch} = \frac{K_1}{K_2}\frac{L^2}{\mu_n V_{eff}} = K_3\frac{L^2}{\mu_n V_{eff}} \tag{1.10}$$

where K_3 is the proportionality constant in the range of 2 to 4.

Equation (1.10) implies that τ_{latch} depends on the technology rather than design. This equation is very useful in determining the maximum clock frequency of the dynamic comparators.

It is required to attain a voltage difference of ΔV_{logic} so that the subsequent logic circuitry can safely identify the correct output value. So, Equations (1.6) becomes

$$\Delta V_{logic} = \Delta V_o e^{tG_m/C_L} \tag{1.11}$$

On solving Equation (1.11) latching delay of the dynamic comparator is computed as

$$t_{latch} = \frac{C_L}{G_m}\ln\left(\frac{\Delta V_{logic}}{\Delta V_o}\right) \tag{1.12}$$

1.3 MOTIVATION

The output of static comparators changes instantly whenever there is a change in the input signals. As a result, they consume more power. However, many applications only require comparator outputs at certain instances such as ADCs and memories. By only strobing a comparator output at certain intervals, higher accuracy, low offset and high speed can be achieved with a dynamic comparator structure also called as latched comparator. But dynamic comparators suffer from large offset voltage when compared with static comparators. Various offset cancellation techniques has been used in the dynamic comparator to minimize the offset voltage but they will increase other parameters like power consumption, area and delay. Therefore, the motivation behind this research work is to design a dynamic comparator which offers low offset voltage without affecting other performance parameters.

1.4 ORGANIZATION OF THE THESIS

The thesis is organized as follows:

Chapter 1 addresses the architecture of conventional comparators and discusses about the various design considerations for dynamic comparators. It also covers the motivation behind this research work.

Chapter 2 presents a brief description of various dynamic comparators that has been reported in the literature.

Chapter 3 focuses on two conventional structures of dynamic comparators namely single-tail and double-tail dynamic comparator. Delay and power analysis of these two structures are also discussed in this chapter.

Chapter 4 proposes fully differential double-tail dynamic comparator using charge sharing technique and its detailed analysis which includes delay, power and mismatch analysis.

Chapter 5 presents the simulation results of the proposed FDDCCST. The proposed FDDCCST is also compared with other dynamic comparators available in the literature in this chapter.

Chapter 6 concludes the thesis and also gives the future possibilities to carry forward the research work.

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CHAPTER 2
LITERATURE SURVEY

The need of area efficient, high speed and power optimized ADCs is compelling for the usage and exploration of the dynamic comparators to reduce the area, power and maximize the speed. The first DTDC was proposed by Schinkel *et al.* in [3-4]. In this structure, input and latch stage of the comparator is separated due to which it can be operated at very low supply voltage. Various other techniques have been proposed to meet these design specifications.

Elzakker *et al.* [5] presented the single-tail dynamic comparator having two stages which results in no DC quiescent current and low input equivalent noise. The presented dynamic comparator is also optimized to obtain high speed.

Jeon *et al.* [6] designed a dynamic comparator stems from the structures reported in [3, 5]. Several modification and two additional inverters are added in these structures to amplify the weak input dependent differential voltage in evaluation phase. These inverters allow the comparator to achieve low input referred offset voltage. This comparator uses single phase clock signal to drive the large capacitive load at the load.

Moni *et al.* [7] compared various CMOS comparators which includes preamplifier dynamic latch comparator, latch type voltage sense amplifier, preamplifier based comparator and dynamic latch comparator with inverter buffer. Comparison study shows that the consumed power of dynamic latch comparator with inverter is minimum.

To find an optimal design of dynamic comparator heuristic algorithm is used by Yaqubi *et al.* [8]. A multi-objective inclined planes optimization and HSPICE are linked together to get several set of solutions known as pareto-front. Now, from these pareto-front, a designer can select a suitable design depending on their requirements. Width of the transistors is used as the parameter which is varied to optimize the design.

Mashhadi *et al.* [9] proposed double-tail based structure for comparator. The positive feedback in the regeneration phase is reinforced by inserting few transistors to the design of DTDC [3-4], which results in reduced delay time. In addition, the comparator is operational at low supply voltage and has reduced power consumption. Additional NMOS switches are also added to the input transistors to overcome the problem of static power consumption in comparator during regeneration phase.

Vaijayanthi *et al.* [10] presented a bulk-driven dynamic comparator for low supply voltage and low-power capability which results in reduced delay. Another bulk-driven method to design DTDC is discussed by Dubey *et al.* [11]. The gain of the amplification stage (input stage) is improved by using bulk-driven PMOS load transistors. These loads operate in weak inversion region to improve the

speed and save considerable power. The limitation of bulk-driven technique is that it reduces the transconductance of transistors.

Bahmanyar *et al.* [12] designed a DTDC suitable for biomedical applications as it requires low-power devices. The vital signals do not change quickly, so the comparator having high speed is not required but the amount of consumed power is of major concern. This structure has three stages which allow the comparator to operate at low supply voltage and reduce the static leakage current.

To reduce the sub threshold leakage, CMOS inverter based preamplifier design for dynamic comparator is reported by Vemu *et al.* [13]. In this structure, inputs are given to the inverters and their outputs are applied to the latch stage which reduces the power consumption as well as delay of the comparator.

Double-tail structure is modified by inserting cross-coupled control transistors in input stage to increase the regeneration speed reported in [14-16]. To minimize the static power consumption due to these cross-coupled control transistors, another two transistors are added to the input transistors. These transistors break the path for current to flow from V_{DD} to ground if one of the control transistors turns ON during decision phase. This structure is termed as Modified Double-Tail Dynamic Comparator (MDTDC).

Dastagiri *et al.* [17] modified the exiting double-tail comparator structure [14-16] by adding domino logic circuit at the output side. By adding domino logic at the output, slew-rate of the comparator is increased than conventional DTDC.

Jain *et al.* [18] added two key transistors in the latch stage of MDTDC to enhance the effective transconductance of the intermediate stage transistors. Due to this, latch regeneration speed is increased as the initial output voltage difference is enhanced.

The new reset technique in which charge shared logic is provided between the output nodes is presented in [19-20]. In this reset technique, a pass transistor is added in between the two output terminals to share a charge between them during reset phase. As a result, output terminals are now charged to some intermediate level instead of ground and V_{DD}. Therefore, the input signals can be compared quickly during the comparison phase because the voltage at the output terminals will not drop below the threshold voltage of the transistor.

Rahmani *et al.* [21] presented a high speed DTDC with isomorphic latch preamplifier pairs. Supply voltage is enhanced in clock transition period with the help of supply boosting technique to reduce delay and power. SR latch comprise of NAND gates is used in evaluation phase instead to SR latch based on NOR gates as NAND gate is faster than NOR gate. Another structure that uses NAND latch circuit is reported in [22].

Fahmy *et al.* [23] transformed current steering technique by charge steering technique. Tail current is replaced with small capacitor and two NMOS switches. These two NMOS switches are driven by two clocks which are out of phase. In addition, charging and discharging time for the small capacitor used are less and equal. This modification reduces the power consumption and enhances the speed.

A two stage dynamic comparator designed for SAR ADC is presented by Hwang *et al.* [24]. It uses forward body bias scheme which helps the structure to operate at low supply voltage and reduces the power consumption. This structure also offers high speed performance with low offset voltage.

Bindra *et al.* [25] used dynamic biasing to reduce the energy consumption. Dynamic biasing is provided by replacing the input tail transistor with a capacitor and two transistors. One of the transistors is used to reset the capacitor to ground. Due to this, output nodes of preamplifier do not discharge to the ground at the end of comparison phase like other dynamic comparators. Partial discharging of the output nodes of preamplifier saves considerable power.

Various structures use differential pairs as the input transistors reported in [26-27]. Due to this, the offset voltage of the dynamic comparator is reduced significantly without affecting the speed and power of the comparator.

Another structure presented by Hassanpourghadi *et al.* [28] separate the preamplifier and latch. Both the circuits are operated using two different clock pulses which reduce the mismatch effects in inner devices. Therefore, the input referred offset voltage is significantly reduced.

Offset cancellation techniques are commonly used to decrease the offset voltage in dynamic comparators. One such technique is implemented for single stage latch comparator by Kazeminia *et al.* [29-30]. In this technique, analog control signals are applied to the circuit instead of digital control signals to resolve the unwanted coupling effect occurred in other offset cancellation techniques [31-32]. The comparison cycle consists of six different phases in which different operations are performed such as removal of previous latched data, increasing the gain of offset cancellation loop, amplification of main inputs, etc. The control signals of small amplitude are applied on the bulk terminal of frequently used PMOS transistors for positive and negative feedback to schedule the multiple operations.

A low-power rail-to-rail DTDC was proposed by Shahpari *et al.* [33]. In this structure, two parallel PMOS differential pairs with a DC level shifter are added in the input stage to increase the range of input common-mode voltage to rail-to-rail swing. Furthermore, to reduce the offset voltage, an offset cancellation circuit is also added to the structure which works on discrete time bulk-driven technique.

The second generation of dynamic comparators is presented by Khorami *et al.* [34]. In this structure, to minimize the power, two PMOS transistors are inserted as the input of the latch circuit and the PMOS preamplifier circuit is cascaded with PMOS latch circuit to get low-power and reduced delay.

The two stages get activated by different clock pulses generated by inverter based clock generator. NMOS version of the proposed structure is also presented which provides better performance than PMOS version in terms of speed.

Halim *et al.* [35] combines the differential pairs in input stage and charge sharing technique in latch stage to reduce delay. But, this structure suffers from stacking of transistors during comparison phase and hence it requires large supply voltage headroom for proper operation.

CHAPTER 3

CONVENTIONAL DYNAMIC COMPARATORS

Dynamic comparators are extensively used in many high speed ADCs because they have a strong positive feedback in regenerative latch due to which they can make fast decisions. The performance of dynamic comparators can be analyzed from different aspects such as offset [36-38], latching delay [2], power consumption [39], random decision error [40], kick-back noise [41], etc.

This chapter presents a broad analysis of two common conventional structures namely, Single-Tail Dynamic Comparator (STDC) and Double-Tail Dynamic Comparator (DTDC). In section 3.1 and 3.2 delay analysis of STDC and DTDC are presented whereas section 3.3 is used to analyze the power consumption of the dynamic comparator.

3.1 CONVENTIONAL SINGLE-TAIL DYNAMIC COMPARATOR

The circuit diagram of the conventional STDC is shown in Figure 3.1 [42]. It is widely used in many ADCs because it has high input impedance, full output swing and no static power consumption. The comparator works in two phases i.e, reset phase and comparison phase. In reset phase if clk = 0, then transistor M_{TAIL} is switched OFF whereas the transistors M_7 and M_8 are switched ON and now these two transistors will precharge the output nodes 'out-' and 'out+' to V_{DD}. A valid voltage level is obtained at the output nodes during reset phase which is defined as a starting condition for comparison phase.

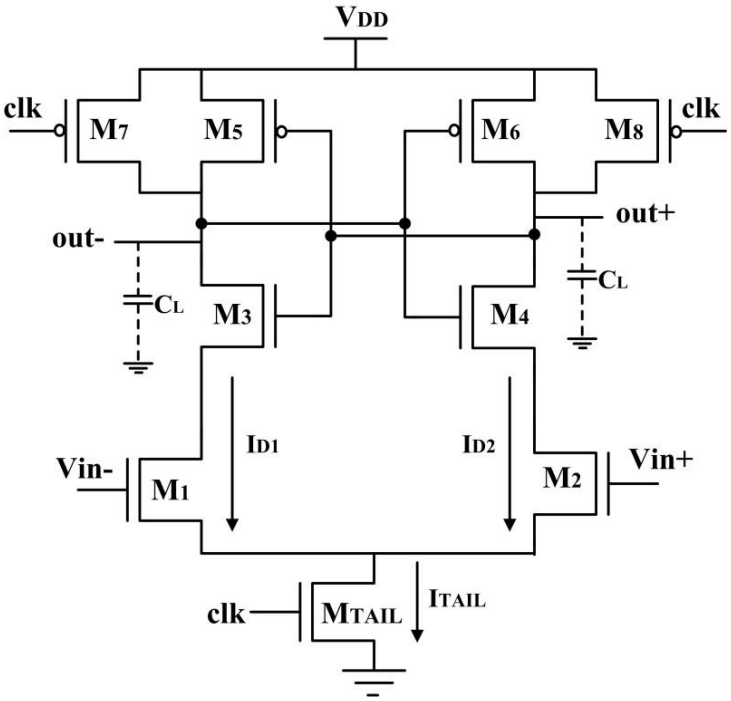

Figure 3.1 Circuit diagram of conventional STDC [42]

In comparison phase if clk = V_{DD}, then transistor M_{TAIL} is switched ON whereas transistors M_7 and M_8 gets switched OFF. Output nodes 'out-' and 'out+' start discharging from V_{DD} with different rates depending on the voltage at input nodes 'Vin-' and 'Vin+'. If Vin- > Vin+, output node 'out-' discharges at faster rate than output node 'out+'. As soon as the voltage at output node 'out-' falls below the threshold voltage V_{DD} - $|V_{thp}|$, the PMOS transistor M_6 will turn ON. Thus, output node 'out+' charges to V_{DD} whereas output node 'out-' discharges to ground. Similarly, if Vin+ > Vin-, then the output node 'out-' charges to V_{DD} and output node 'out+' discharges to ground. Thus, it can be concluded that if Vin-> Vin+, then output nodes 'out+' and 'out-' are at 'logic l' and 'logic 0 ' respectively. Similarly, if input Vin+ > Vin- then output nodes 'out-' and 'out+' are at 'logic l' and 'logic 0' respectively.

The total delay t_{total} of the comparator comprises of two delays t_0 and t_{latch} where t_0 represents the time period in which the load capacitor C_L discharges till the first PMOS transistor (either M_5 or M_6) turns ON and t_{latch} represents the latching delay of cross-coupled invertor pairs (M_3 – M_5 and M_4 – M_6). Consider when Vin- > Vin+, the drain current I_{D1} of transistor M_1 discharges the output node 'out-' faster than the output node 'out+' Thus, delay t_0 is given by

$$t_0 = \frac{C_L.|V_{thp}|}{I_{D1}} \tag{3.1}$$

where $I_{D1} = I_{TAIL}/2 + g_{m1,2}\ \Delta V_{in.}$ Since, the drain current I_{D1} can be approximated as a constant current ($I_{D1} = I_{TAIL}/2$) for small values of input differential voltage (ΔV_{in}). The delay t_0 reduces to

$$t_0 \approx 2.\frac{C_L.|V_{thp}|}{I_{TAIL}} \tag{3.2}$$

The delay t_{latch}, calculated using Equation (1.12) is given as

$$t_{latch} = \frac{C_L}{g_{m(eff)}}.\ln\left(\frac{\Delta V_{out}}{\Delta V_o}\right) \tag{3.3}$$

where $g_{m(eff)}$ represents the effective transconductance of two cross-coupled inverters (M_3 – M_5 and M_4 – M_6).

This delay depends on initial output difference voltage ΔV_0 at t = t_0 in logarithm manner. The final output ΔV_{out} is assumed to be $V_{DD}/2$ from the initial output difference voltage ΔV_0 and the delay t_{latch} is modified as

$$t_{latch} \approx \frac{C_L}{g_{m(eff)}}.\ln\left(\frac{V_{DD}/2}{\Delta V_o}\right) \tag{3.4}$$

The initial output difference voltage (ΔV_0) can be written as

$$\Delta V_o = |V_{out+}(t = t_o) - V_{out-}(t = t_o)| = \left|V_{thp}\right| - \frac{I_{D2}.t_o}{C_L} = \left|V_{thp}\right|\left(1 - \frac{I_{D2}}{I_{D1}}\right) \tag{3.5}$$

The current difference $\Delta I_{in} = |I_{D1} - I_{D2}|$ is much smaller than I_{D1} and I_{D2} between the branches and is equal to $g_{m1,2}\,\Delta V_{in}$. Thus, I_{D1} can be approximated to $I_{TAIL}/2$ and Equation (3.5) can be rewritten as

$$\Delta V_o = 2.|V_{thp}|\left(\frac{\Delta I_{in}}{I_{TAIL}}\right) = 2.|V_{thp}|.\sqrt{\frac{\beta_{1,2}}{I_{TAIL}}}\Delta V_{in} \tag{3.6}$$

where $\beta_{1,2}$ = transconductance parameter of input transistors and I_{TAIL} is the tail current which is a function of supply voltage and input common-mode voltage (V_{cm}).

By substituting the value of ΔV_0 in Equation (3.4) time period t_{latch} becomes

$$t_{latch} = \frac{C_L}{g_{m(eff)}}.\ln\left(\frac{V_{DD}.\sqrt{I_{TAIL}}}{4.|V_{thp}|.\sqrt{\beta_{1,2}}\,\Delta V_{in}}\right) \tag{3.7}$$

Using Equations (3.2) and (3.7), the total delay t_{total} (= t_0 + t_{latch}) is given as

$$t_{total} = 2.\frac{C_L.|V_{thp}|}{I_{TAIL}} + \frac{C_L}{g_{m(eff)}}.\ln\left(\frac{V_{DD}.\sqrt{I_{TAIL}}}{4.|V_{thp}|.\sqrt{\beta_{1,2}}\,\Delta V_{in}}\right) \tag{3.8}$$

From Equation (3.8), various parameters which affect the total delay t_{total} can be analysed. The total delay of the comparator is directly proportional to the C_L and inversely proportional to the ΔV_{in}. Moreover, the common-mode voltage (V_{cm}) indirectly affects the delay of the comparator. When V_{cm} is reduced, it causes smaller bias current i.e. I_{TAIL} which tends to increase the t_0 delay of the first sensing phase. Equation (3.6) shows that smaller I_{TAIL} increases the initial output difference voltage (ΔV_0) hence reducing t_{latch}. On reducing the value of V_{cm}, the delay t_0 increases linearly whereas the delay t_{latch} decreases logarithmically. Due to this, the total delay of the comparator increases. In [43], it has been shown that the optimal value for V_{cm} is 70% of the supply voltage regarding yield and speed. The switching speed of output nodes does not have a direct effect of the parasitic capacitances of input transistors. Therefore, to minimize the offset voltage of the comparator input transistors with large aspect ratio are used.

The disadvantage of STDC structure is high supply voltage requirement for proper delay time due to stacking of transistors. This happens because in comparison phase only transistors M_3 and M_4 are present in the positive feedback until the voltage at one of the output nodes dropped below the threshold value of transistors M_5 and M_6 to start the regeneration. At a lower supply voltage, this scenario is even worse as the delay of the latch increases due to reduction in transconductances. Another limitation of this structure is only one tail current, via transistor M_{TAIL}, which describes the current for differential amplifier. To keep the transistors of differential amplifier in weak inversion, small tail current is desired to have a better G_m/I_d ratio and long integration interval whereas to enable fast regeneration in latch stage, larger tail current is desired [3-4].

To plot the transient response of STDC, the various input parameters are chosen as ΔV_{in} = 20 mV, V_{cm} = 0.7 V, f_{clk} = 500 MHz, Vin- = 20mV and Vin+ = 0V. The power supply voltage is used as

V_{DD} = 1V. The transient response of STDC is shown in Figure 3.2 [9]. Figure shows that total delay is 0.594 ns, where t_0 = 0.31 ns and t_{latch} = 0.284 ns.

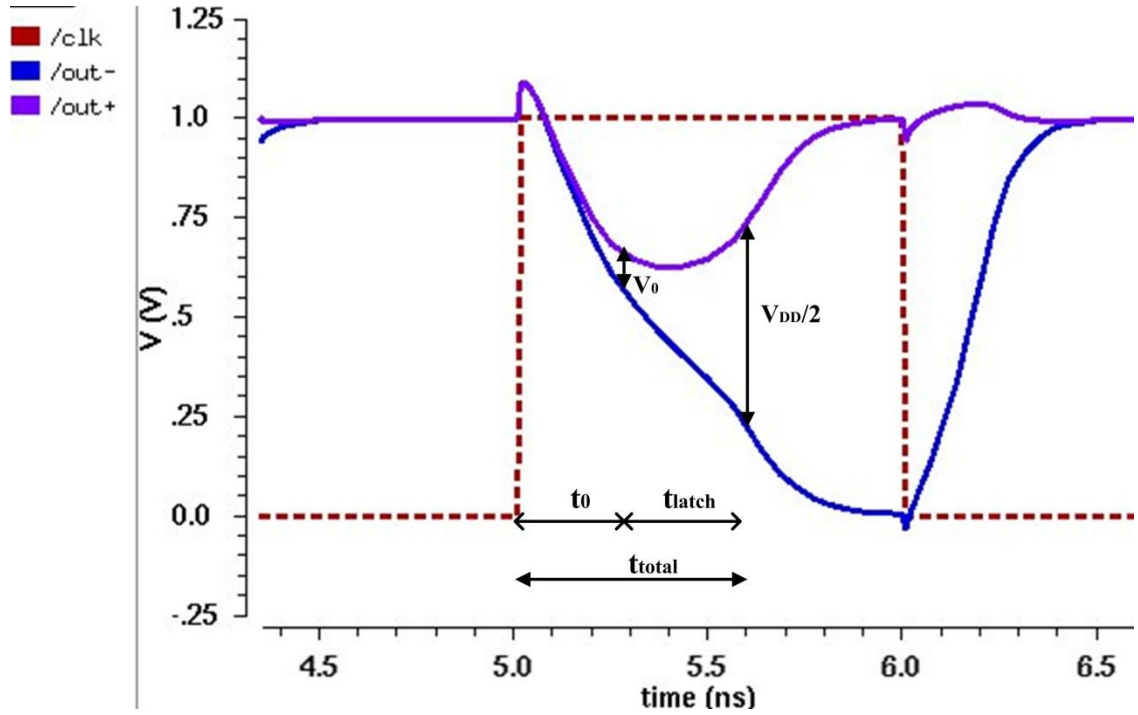

Figure 3.2 Transient response of the conventional STDC [9]

3.2 CONVENTIONAL DOUBLE-TAIL DYNAMIC COMPARATOR

The circuit diagram of the conventional DTDC is shown in Figure 3.3 [3]. This structure has two separate tail currents which enable large current in the latch stage for fast regeneration and small current in differential stage for low offset. Also, it has less stacking of transistors due to which it can be operated at lower supply voltages. Similar to STDC, this comparator also works in reset phase and comparison phase. In reset phase, if clk = 0, transistors M_{TAIL1} and M_{TAIL2} are switched OFF whereas transistors M_3 and M_4 are switched ON, which will precharge the nodes 'A' and 'B' to V_{DD}. As a result transistors M_{R1} and M_{R2} get switched ON and discharge the output nodes 'out-' and 'out+' to ground. In comparison phase, if clk = V_{DD}, then transistors M_{TAIL1} and M_{TAIL2} are switched ON whereas transistors M_3 and M_4 are switched OFF. The voltages at nodes 'A' and 'B' start to drop at different rates depending on the voltages (Vin- and Vin+) at input transistors M_1 and M_2. This builds an input dependent differential voltage (ΔV_{AB}) between 'A' and 'B' nodes. Intermediate transistors M_{R1} and M_{R2} pass this voltage difference to the cross-coupled inverters ($M_7 – M_9$ and $M_8 – M_{10}$) and also help to reduce kick-back noise by providing a good shield between input and output. If Vin- > Vin+ then node 'B' discharges faster than node 'A' due to which transistor M_{R1} turns OFF and output node 'out-' stops discharging whereas output node 'out+' is still discharging till its voltage reaches below the threshold of PMOS transistor M_7. The transistor M_7 charges the output node 'out-' to V_{DD} and discharge the output node 'out+' to ground. Therefore it can be concluded that if

Vin- > Vin+, then 'out+' is at 'logic 0' and 'out-' is at 'logic l'. Similarly, if input Vin+ > Vin-, then 'out-' is at 'logic 0' and 'out+' is at 'logic l'.

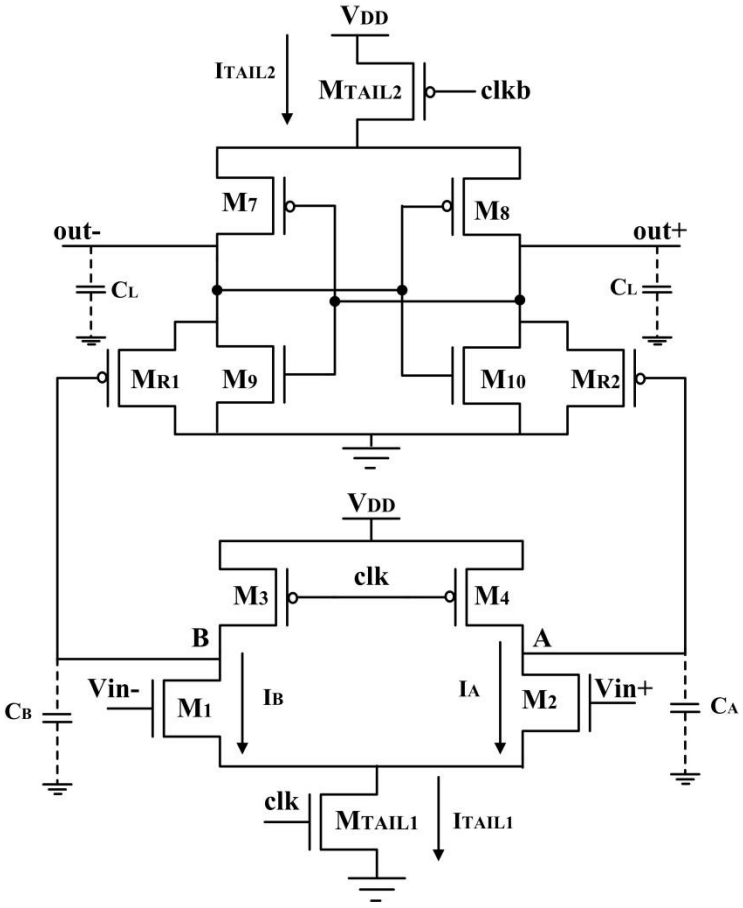

Figure 3.3 Circuit diagram of conventional DTDC [3]

Similar to STDC, the delay t_{total} of this comparator structure comprises of two delays t_0 and t_{latch}. Here, the delay t_0 represents the time period in which the load capacitance charges till the first NMOS transistor either M_9 or M_{10} gets switched ON to start the latch regeneration. Thus t_0 is obtained from

$$t_0 = \frac{C_L.V_{thn}}{I_{D10}} \tag{3.9}$$

where I_{D10} represents the drain current of transistor M_{10}.

The current I_{D10} can be approximated to $I_{TAIL2}/2$ for small values of ΔV_{in}. Thus, the delay t_0 is modified as

$$t_0 \approx 2\frac{C_L.V_{thn}}{I_{TAIL_2}} \tag{3.10}$$

When the first NMOS transistor of the latch (for example M_{10}) gets ON, the output node 'out+' starts discharging to ground which will turn ON the PMOS transistor M_7. The transistor M_7 charges the output node 'out-' to V_{DD}. Thus, the regeneration time t_{latch} is obtained by using Equation (3.3).

The initial output difference voltage (ΔV_0) at time t = t_0 is given as

$$\Delta V_o = |V_{out+}(t = t_o) - V_{out-}(t = t_o)| = |V_{thn}| - \frac{I_{D10}.t_o}{C_L} = V_{thn}\left(1 - \frac{I_{D9}}{I_{D10}}\right) \quad (3.11)$$

where I_{D10} and I_{D9} are the latch right and left side branches current, respectively and $\Delta I_{latch} = |I_{D10} - I_{D9}| = g_{mR1,2}\,\Delta V_{AB}$. Equation (3.11) is now rewritten as

$$\Delta V_o = V_{thn}\left(\frac{\Delta I_{latch}}{I_{D10}}\right) = 2.V_{thn}\frac{g_{mR1.2}}{I_{TAIL2}}.\Delta V_{AB} \quad (3.12)$$

where $g_{mR1,2}$ = transconductance of two intermediate transistors M_{R1} and M_{R2} and ΔV_{AB} is the voltage difference between nodes 'A' and 'B' at time t = t_0. Thus, it can be concluded that ΔV_0 as well as latch regeneration time is strongly influenced by transconductance ($g_{mR1,2}$) of two intermediate transistors M_{R1} and M_{R2} and the voltage difference between nodes 'A' and 'B' at time t_0 (ΔV_{AB}). The voltage difference ΔV_{AB} is amplified by intermediate transistors which causes latch to imbalance. The voltage difference between nodes 'A' and 'B' can be calculated as follows

$$\Delta V_{AB} = |V_A(t = t_o) - V_B(t = t_o)| = t_o.\frac{I_A - I_B}{C_{AB}} \quad (3.13)$$

where I_A and I_B refers to the discharging currents of transistors M_2 and M_1 respectively which depends on input differential voltage (ΔV_{in}) as $\Delta I = g_{m1,2}\,\Delta V_{in}$. Now ΔV_{AB} becomes

$$\Delta V_{AB} = t_o.\frac{g_{m1,2}.\Delta V_{in}}{C_{AB}} \quad (3.14)$$

Using Equations (3.10) and (3.14), ΔV_0 becomes is obtained as

$$\Delta V_o = \left(\frac{2.V_{thn}}{I_{TAIL2}}\right)^2.\frac{C_L}{C_{AB}}.g_{m1,2}.g_{mR1,2}\Delta V_{in} \quad (3.15)$$

The Equation (3.15) shows that the transconductance of the input and intermediate transistors, latch tail current, capacitive ratio C_L/C_{AB} and input differential voltage (ΔV_{in}) strongly affects the value of ΔV_0. The total delay of the comparator by substituting the value of ΔV_0 in Equation (3.4) and using Equation (3.10) is achieved as

$$t_{total} = 2.\frac{C_L.V_{thn}}{I_{TAIL2}} + \frac{C_L}{g_{m(eff)}}.\ln\left(\frac{V_{DD}.C_{AB}.I_{TAIL2}^2}{8{V_{thn}}^2 C_L.g_{m1,2}.g_{mR1,2}\Delta V_{in}}\right) \quad (3.16)$$

From the Equation (3.12), it can be concluded that the voltage difference between nodes 'A' and 'B' (ΔV_{AB}) at time t_0 strongly affects the initial output difference voltage ΔV_0 which in turns affects the latch delay. Therefore increasing ΔV_0 would finally reduce the total delay.

To plot the transient response of DTDC, the various input parameters are chosen as ΔV_{in} = 20 mV, V_{cm} = 0.7 V, clk = 500 MHz, Vin- = 20mV and Vin+ = 0V. The power supply voltage is used as

V_{DD} = 1V. The transient response of DTDC is shown in Figure 3.4 [3]. Figure shows that total delay is 0. 4415 ns, where t_0 = 0.3434 ns and t_{latch} = 0.09 ns.

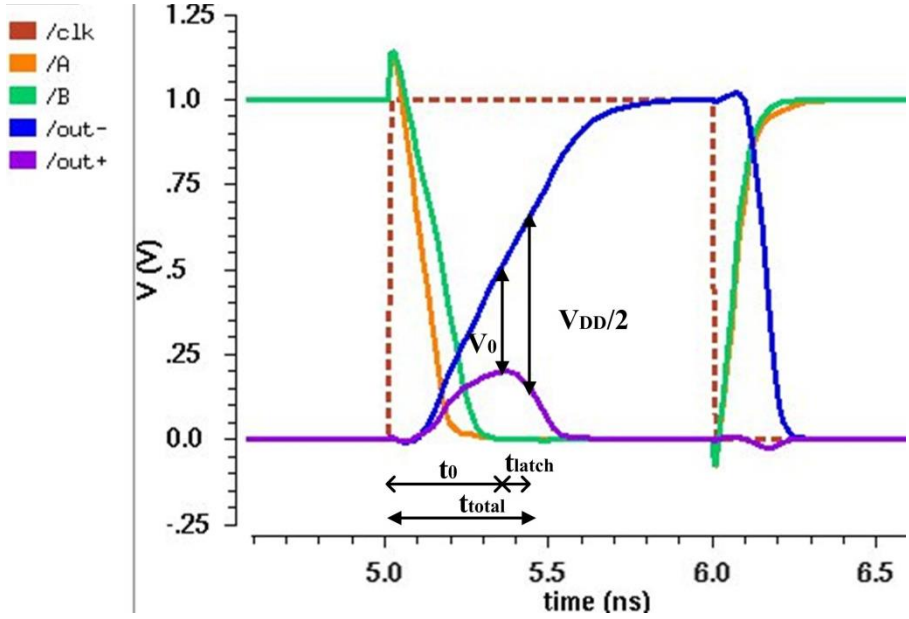

Figure 3.4 Transient response of the conventional DTDC [3]

3.3 POWER ANALYSIS OF DYNAMIC COMPARATOR

For power analysis of dynamic comparators the time variant model of transistor is used. Existing models of MOSFETs have distinct expressions for all operating region which is not accurate near or at the boundary between such regions [39]. So, the single expression for drain current of MOSFETs which is valid in all operating region is presented by Tsividis *et al.* [44]. The drain current is given as

$$I_D = I_Z\left\{\ln^2\left(1+\exp\left[\frac{V_p-V_{SB}}{2\phi_t}\right]\right)-\ln^2\left(1+\exp\left[\frac{V_p-V_{DB}}{2\phi_t}\right]\right)\right\} \tag{3.17}$$

where $I_Z = 2\mu C_{ox}\frac{W}{L}n\phi_t^2$, $n = \left[1-\frac{\gamma}{2\sqrt{V_{GB}-V_{TO}}+\left(\frac{\gamma}{2}+\sqrt{2\phi_t}\right)^2}\right]^{-1}$, ϕ_t = KT/q is the thermal voltage and V_p is the pinch off voltage which can be approximated as $(V_{GB} - V_{TO})/n$ [44].

Substituting the value of V_p in Equation (3.17), I_D becomes,

$$I_D = I_Z\left\{\ln^2\left(1+\exp\left[\frac{V_{GS}-V_T}{2n\phi_t}\right]\right)-\ln^2\left(1+\exp\left[\frac{V_{GS}-nV_{Ds}-V_T}{2n\phi_t}\right]\right)\right\} \tag{3.18}$$

This time variant model shows good accuracy for low voltage operations in all regions of inversion, which also include narrow or/and short channel effects and ion-implantation effects. Simple expression can also be derived from this model for each region of inversion [44].

The average power consumed during one period of conversion can be obtained as

$$P_{avg} = \frac{1}{T}\int_0^T V_{DD} I_{supply} dt = f_{clk} V_{DD} \int_0^T I_{supply} dt \quad (3.19)$$

where f_{clk} is the clock frequency of the comparator and I_{supply} is the total current drawn from the power supply.

Considering an example of STDC, during reset phase when clk = 0, a current is drawn from supply to charge the output nodes 'out-' and 'out+' to V_{DD}. In comparison phase when clk = V_{DD}, initially both the PMOS transistors M_5 and M_6 are OFF. As the operation continues, one of the output nodes get discharged enough to turn ON the PMOS transistor either M_5 or M_6. When Vin+ > Vin-, output node 'out+' discharges faster which will turn ON the transistor M_5. Thus, the output node 'out-' gets charge to V_{DD} whereas output node 'out+' discharges to ground and transistor M_6 will remain OFF. Transistor M_3 will get OFF and after some time no current will be drawn from supply. Therefore, the current is drawn for a short time from only one PMOS transistor (M_5) which is equal to I_{supply} and is given as

$$I_{supply} = I_{sp5}\left\{\ln^2\left(1+\exp\left[\frac{V_{DD}-V_{out+}(t)-|V_{thp}|}{2n\phi_t}\right]\right) - \ln^2\left(1+\exp\left[\frac{V_{DD}-V_{out+}(t)-|V_{thp}|-n(V_{DD}-V_{out-}(t))}{2n\phi_t}\right]\right)\right\} \quad (3.20)$$

To calculate the average power of the comparator during comparison phase, Equation (3.19) can be rewritten as

$$P_{avg} = f_{clk} V_{DD} I_{sp5} \int_{t0}^{tp}\left\{\ln^2\left(1+\exp\left[\frac{V_{DD}-V_{out+}(t)-|V_{thp}|}{2n\phi_t}\right]\right) - \ln^2\left(1+\exp\left[\frac{V_{DD}-V_{out+}(t)-|V_{thp}|-n(V_{DD}-V_{out-}(t))}{2n\phi_t}\right]\right)\right\} dt \quad (3.21)$$

The integration is performed from starting of regeneration (t_0) to the end of regeneration (t_p) equals to $\frac{C_{Load}}{G_m}\ln\left(\frac{V_{DD}}{\Delta V_{in}}\right)$. In Equation (3.21) output voltages 'V_{out+}' and 'V_{out-}' are functions of time. Using Equations (1.6) and (1.7), it can be seen that the difference of output voltages changes logarithmically as follows

$$\Delta V_{out} = |V_{out+} - V_{out-}| = \Delta V_0 \exp\left(\frac{G_m t}{C_{Load}}\right) \quad (3.22)$$

where G_m = effective transconductance of cross-coupled inverters, C_{Load} is the load capacitance at the output and ΔV_0 is initial output difference voltage given by Equation (3.4).

The output V_{out+} is discharged completely and it is given as

$$V_{out+} = (V_{DD} - |V_{thp}|[\exp(-(t-t_0)/\tau_{latch}] \quad (3.23)$$

where τ_{latch} is the ratio of G_m and C_{Load}.

Now, average power of STDC can be calculated by using Equations (3.21), (3.22) and (3.23) and given as

$$P_{avg} = f_{clk} V_{DD} I_{sp5} \int_{t0}^{tp} \left\{ \left(\frac{V_{DD} - V_{out+}(t) - |V_{thp}|}{2n\phi_t} \right)^2 - \left(\frac{V_{DD} - V_{out+}(t) - |V_{thp}| - n(V_{DD} - V_{out-}(t))}{2n\phi_t} \right)^2 \right\} dt \quad (3.24)$$

After simplification, Equation (3.24) is expressed as

$$P_{avg} = f_{clk} V_{DD} I_{sp5} \left(\frac{1}{8n{\phi_t}^2} \right) \tau_{latch} |V_{thp}| \times \left[2k - n|V_{thp}| + (2k + n|V_{thp}|) \exp\left(-2\frac{t_p - t_0}{\tau_{latch}} \right) - 4k \exp\left(-\frac{t_p - t_0}{\tau_{latch}} \right) \right] \quad (3.25)$$

where $k = V_{DD} - |V_{th}|$.

From Equation (3.25) it can be concluded that power of dynamic comparator depends on clock frequency, supply voltage, aspect ratio of input transistors and the time in which the comparator makes a decision ($t_p - t_o$).

CHAPTER 4

DESIGN OF PROPOSED FULLY DIFFERENTIAL DOUBLE-TAIL DYNAMIC COMPARATOR

This chapter discusses the design and operation of proposed FDDCCST in section 4.1. Delay, power and mismatch analysis of proposed FDDCCST is presented in section 4.2, 4.3 and 4.4 respectively.

4.1 OPERATION OF PROPOSED FULLY DIFFERENTIAL DOUBLE-TAIL DYNAMIC COMPARATOR

The fully differential double-tail dynamic comparator using charge sharing technique (FDDCCST) is presented in Figure 4.1. The features of differential pair and DTDC are combined to achieve low offset voltage in the proposed FDDCCST. Charge share technique suggested in [19-20] has been implemented using pass transistor logic which shares a charge between the two output nodes during reset phase. As a result, output nodes are now charged to some intermediate level instead of ground and V_{DD}.

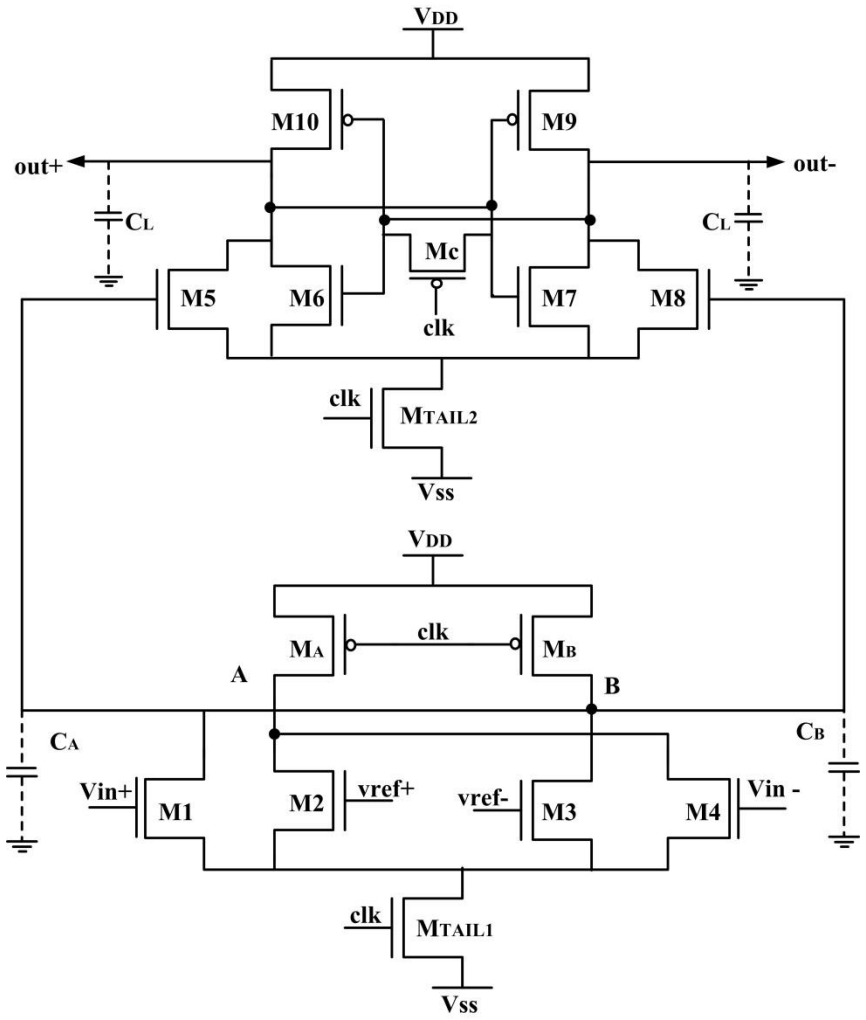

Figure 4.1 Proposed fully differential double-tail dynamic comparator using charge sharing technique

The proposed FDDCCST works in two different phases namely, reset phase and comparison phase. In reset phase, when clk = 0, transistors M_{TAIL1} and M_{TAIL2} are switched OFF and transistors M_A, M_B and M_C are switched ON and they will charge the nodes 'A' and 'B' to V_{DD} and therefore, transistors M_5 and M_8 get switched ON. Transistor M_C is used to share the charge between output nodes 'out+' and 'out-'. In comparison phase, when clk = V_{DD}, transistors M_{TAIL1} and M_{TAIL2} are switched ON and transistors M_A, M_B and M_C are switched OFF. Now, nodes 'A' and 'B' starts discharging through transistors M_1 to M_4 at different discharging rates depending upon the input voltages at transistors M_1 and M_4. When Vin+ > Vin-, node 'B' discharges faster than node 'A' which will turn OFF the transistor M_8 and output node 'out-' stops discharging. The output node 'out+' discharges below the threshold voltage, which will turn ON the transistor M_9. Therefore, output node 'out-' charges to V_{DD} and output node 'out+' discharges to V_{ss}. Similarly, when Vin- > Vin+, output node 'out+' charges to V_{DD} and output node 'out-' discharges to V_{ss}. At the end, depending upon the inputs to the comparator, output nodes 'out+' and 'out-' either charges to V_{DD} or discharges to V_{ss}.

4.2 DELAY ANALYSIS

The total time delay t_{total} of the proposed FDDCCST involves two delays t_0 and t_{latch} as $t_{total} = t_0 + t_{latch}$, where t_0 represents the time period in which the load capacitor C_L discharges till the first PMOS transistor (either M_9 or M_{10}) turns ON and t_{latch} represents the latching delay of cross-coupled invertor pairs (M_6 - M_{10} and M_7 - M_9). The drain current of the transistor M_7 which can be approximated to $I_{TAIL2}/2$ is given as

$$I_{D7} \approx \frac{I_{TAIL2}}{2} = C_L \frac{dV_{out-}}{dt} \tag{4.1}$$

Now, integrating both sides of Equation (4.1) from t = 0 to t = t_o gives

$$\int_0^{t_0} dt = \frac{C_L}{I_{D7}} \int_0^{V_{DD}-V_{thp}} dV; \qquad t_0 = \frac{2C_L(V_{DD}-V_{thp})}{I_{TAIL2}} \tag{4.2}$$

where C_L represents the load capacitance.

The delay t_{latch}, is calculated using Equation (1.12).

$$t_{latch} = \frac{C_L}{g_{m(eff)}} . \ln\left(\frac{\Delta V_{out}}{\Delta V_o}\right) \cong \frac{C_L}{g_{m(eff)}} . \ln\left(\frac{[V_{DD}-V_{SS}]/2}{\Delta V_o}\right) \tag{4.3}$$

The initial output difference voltage ΔV_0 is expressed as

$$\Delta V_0 = |V_{out+}(t = t_0) - V_{out-}(t = t_0)| = |(V_{DD} - V_{thp})(1 - \frac{I_{D6}}{I_{D7}})| \tag{4.4}$$

Assuming $\Delta I_{latch} = |I_{D7} - I_{D6}| = g_{m8,5}\Delta V_{AB}$ and $I_{D7} = I_{TAIL2}/2$, Equation (4.4) can be rewritten as

$$\Delta V_0 = \left|2(V_{DD} - V_{thp})\left(\frac{g_{m8,5}\Delta V_{AB}}{I_{TAIL2}}\right)\right| \tag{4.5}$$

where $g_{m8,5}$ is the transconductance of transistors M_5 and M_8 (intermediate stage transistors) and ΔV_{AB} is the voltage difference between nodes 'A' and 'B' at time $t = t_0$.

The voltage difference between nodes 'A' and 'B' ΔV_{AB} at time $t = t_0$ is given as

$$\Delta V_{AB} = |V_B(t = t_0) - V_A(t = t_0)| = \frac{t_0(I_B - I_A)}{C_{AB}} \tag{4.6}$$

where I_B and I_A represent the discharging currents of input transistors M_1 - M_3 and M_2 - M_4, which depend on input differential voltage (ΔV_{in}). Assuming $|I_B - I_A| = \Delta I = g_{m1,2}\Delta V_{in}$, the voltage difference ΔV_{AB} can be rewritten as

$$\Delta V_{AB} = \frac{t_0 g_{m1,2}\Delta V_{in}}{C_{AB}} \tag{4.7}$$

Using Equations (4.2), (4.5) and (4.7), ΔV_0 is modified as

$$\Delta V_0 = \left|2(V_{DD} - V_{thp})\left(\frac{g_{m8,5}g_{m1,2}\,\Delta V_{in} 2C_L(V_{DD} - V_{thp})}{{I_{TAIL2}}^2\, C_{AB}}\right)\right| \tag{4.8}$$

Now, the delay t_{latch} is given as

$$t_{latch} = \frac{C_L}{g_{m(eff)}}.\ln\left(\frac{[V_{DD} - V_{SS}]{I_{TAIL2}}^2\, C_{AB}}{8(V_{DD} - V_{thp})^2 g_{m8,5}g_{m1,2}\,\Delta V_{in} C_L}\right) \tag{4.9}$$

The total delay of proposed FDDCCST by substituting the values of t_0 and t_{latch} can be obtained as

$$t_{total} = \frac{2C_L(V_{DD} - V_{thp})}{I_{TAIL2}} + \frac{C_L}{g_{m(eff)}}.\ln\left(\frac{[V_{DD} - V_{SS}]{I_{TAIL2}}^2\, C_{AB}}{8(V_{DD} - V_{thp})^2 g_{m8,5}g_{m1,2}\,\Delta V_{in} C_L}\right) \tag{4.10}$$

4.3 POWER ANALYSIS

The average power of the proposed FDDCCST is calculated [39] as

$$P_{avg} = f_{clk}V_{DD}I_{sp5}\left(\frac{1}{8n{\phi_t}^2}\right)\tau_{latch}|V_{thp}| \times \left[2k - n|V_{thp}| + (2k + n|V_{thp}|)\exp\left(-2\frac{t_p - t_0}{\tau_{latch}}\right) - 4k\exp\left(-\frac{t_p - t_0}{\tau_{latch}}\right)\right] \tag{4.11}$$

where $k = V_{DD} - |V_{th}|$, $n = \left[1 - \frac{\gamma}{2\sqrt{V_{GB} - V_{TO}} + \left(\frac{\gamma}{2} + \sqrt{2\phi_t}\right)^2}\right]^{-1}$ and $I_{sp5} = 2\mu C_{ox}\frac{W}{L}n{\phi_t}^2$.

4.4 OFFSET VOLTAGE

The proposed FDDCCST is less sensitive to the mismatches present in the transistors because it uses fully differential pairs (M_1/M_3 and M_2/M_4) in the input stage. In the comparison phase, when clk = $V_{DD,}$ transistor M_{TAIL1} turns ON and moves to saturation region like transistors M_1 to M_4 of the two differential pairs. The drain voltage of transistors M_1 to M_4 is at V_{DD} due to transistors M_A and

M_B which charge the 'A' and 'B' nodes to V_{DD} during reset phase. Transistors M_A and M_B act like switches which are closed in comparison phase. The proposed FDDCCST has symmetry which results in identical pairing between the transistors. Mismatches in MOS transistors are categorized as threshold mismatch (ΔV_{th}) and transconductance parameter β mismatch (Δβ) [37]. These two random variables are assumed to have a normal distribution and variance given as

$$\sigma_{V_{th}}{}^2 = \frac{A_{V_{th}}^2}{WL}\ ; \qquad \sigma_{\beta}{}^2 = \frac{A_{\beta}^2}{WL} \tag{4.12}$$

where $A_{V_{th}}$ and A_{β} are the process-based parameters.

4.4.1 Input offset voltage

At the beginning of the comparison phase, transistors M_1 to M_4 and M_{TAIL1} are in the saturation region. The two discharging currents I_A and I_B are equal in the balanced state if the dimensions of all input transistors are same i.e $\beta_1 = \beta_2 = \beta_3 = \beta_4$. To calculate the input offset voltage of the proposed FDDCCST input stage is simplified as shown in Figure 4.2.

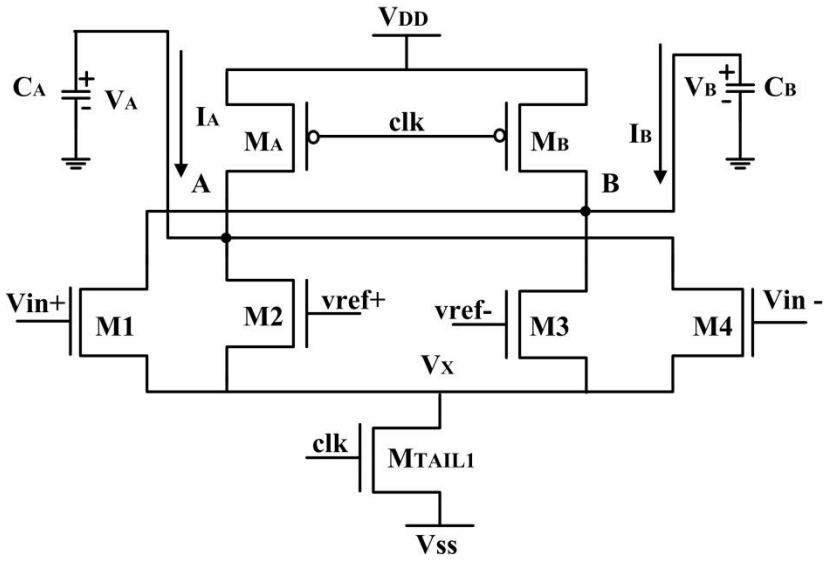

Figure 4.2 Simplified circuit diagram of input differential stage of proposed FDDCCST

Applying KCL at node 'A and 'B' (if there is no mismatch) the currents I_A and I_B are given as

$$I_A = I_{D2} + I_{D4} \tag{4.13}$$

$$I_B = I_{D1} + I_{D3} \tag{4.14}$$

Suppose the mismatch exists between the transistor pairs M_1 - M_3 and M_2 - M_4 which gives input offset voltage. Now, including mismatch effect the currents I_A and I_B are modified as

$$\frac{(\beta_2+\Delta\beta_2)}{2}(\mathrm{vref}^+ - \mathrm{V_X} - \mathrm{V_{thn2}} - \Delta\mathrm{V_{thn2}})^2 + \frac{(\beta_4+\Delta\beta_4)}{2}(\mathrm{Vin}^- - \mathrm{V_X} - \mathrm{V_{thn4}} - \Delta\mathrm{V_{thn4}})^2 =$$
$$\frac{(\beta_1+\Delta\beta_1)}{2}\left(\mathrm{Vin}^+ + \mathrm{V_{OS\_input}} - \mathrm{V_X} - \mathrm{V_{thn1}} - \Delta\mathrm{V_{thn1}}\right)^2 + \frac{(\beta_3+\Delta\beta_3)}{2}(\mathrm{vref}^- - \mathrm{V_X} - \mathrm{V_{thn3}} - \Delta\mathrm{V_{thn3}})^2 \quad (4.15)$$

Here an operator ($\overset{\Delta}{\rightarrow}$) is used to simplify the expression which is exemplified as

$$\Delta\mathrm{I} \overset{\Delta}{\rightarrow} \beta^*(V_{GS} - \mathrm{V_{thn3}}^*) = \beta(V_{GS} - \mathrm{V_{thn}}) + \Delta\beta(V_{GS} - \mathrm{V_{thn}}) - \beta\Delta\mathrm{V_{thn}} - \Delta\beta\Delta\mathrm{V_{thn}}$$
$$= \Delta\beta(V_{GS} - \mathrm{V_{thn}}) - \beta\Delta\mathrm{V_{thn}} \quad (4.16)$$

where $\beta^* = (\beta + \Delta\beta)$ and $\mathrm{V_{thn}}^* = \mathrm{V_{thn}} + \Delta\mathrm{V_{thn}}$.

Assuming all the variations is random in nature and variables are uncorrelated having normal distribution and zero mean. By using the above operator and solving for $\mathrm{V_{OS\_input}}$ by dividing the whole equation by β_1 Equation (4.15) becomes

$$\mathrm{V_{OS\_input}} =$$
$$\frac{(\mathrm{vref}^+-\mathrm{V_X}-\mathrm{V_{thn}})^2}{2(\mathrm{Vin}^+-\mathrm{V_X}-\mathrm{V_{thn}})}\frac{\Delta\beta_2}{\beta_1} - \frac{\mathrm{vref}^+-\mathrm{V_X}-\mathrm{V_{thn}}}{\mathrm{Vin}^+-\mathrm{V_X}-\mathrm{V_{thn}}}\Delta\mathrm{V_{thn2}} + \frac{(\mathrm{Vin}^--\mathrm{V_X}-\mathrm{V_{thn}})^2}{2(\mathrm{Vin}^+-\mathrm{V_X}-\mathrm{V_{thn}})}\frac{\Delta\beta_4}{\beta_1} - \frac{\mathrm{Vin}^--\mathrm{V_X}-\mathrm{V_{thn}}}{\mathrm{Vin}^+-\mathrm{V_X}-\mathrm{V_{thn}}}\Delta\mathrm{V_{thn4}} -$$
$$\frac{(\mathrm{vref}^--\mathrm{V_X}-\mathrm{V_{thn}})^2}{2(\mathrm{Vin}^+-\mathrm{V_X}-\mathrm{V_{thn}})}\frac{\Delta\beta_3}{\beta_1} + \frac{\mathrm{vref}^--\mathrm{V_X}-\mathrm{V_{thn}}}{\mathrm{Vin}^+-\mathrm{V_X}-\mathrm{V_{thn}}}\Delta\mathrm{V_{thn3}} - \frac{(\mathrm{Vin}^+-\mathrm{V_X}-\mathrm{V_{thn}})^2}{2}\frac{\Delta\beta_1}{\beta_1} + \Delta\mathrm{V_{thn1}} \quad (4.17)$$

Substituting $\mathrm{V_{ov1}} = (\mathrm{Vin}^+ - \mathrm{V_X} - \mathrm{V_{thn}})$, $\mathrm{V_{ov2}} = (\mathrm{vref}^+ - \mathrm{V_X} - \mathrm{V_{thn}})$, $\mathrm{V_{ov3}} = (\mathrm{vref}^- - \mathrm{V_X} - \mathrm{V_{thn}})$ and $\mathrm{V_{ov4}} = (\mathrm{Vin}^- - \mathrm{V_X} - \mathrm{V_{thn}})$, Equation (4.17) reduces to

$$\mathrm{V_{OS\_input}} = \frac{(\mathrm{V_{ov2}})^2}{2(\mathrm{V_{ov1}})}\frac{\Delta\beta_2}{\beta_1} - \frac{\mathrm{V_{ov2}}}{\mathrm{V_{ov1}}}\Delta\mathrm{V_{thn2}} + \frac{(\mathrm{V_{ov4}})^2}{2(\mathrm{V_{ov1}})}\frac{\Delta\beta_4}{\beta_1} - \frac{\mathrm{V_{ov4}}}{\mathrm{V_{ov1}}}\Delta\mathrm{V_{thn4}} - \frac{(\mathrm{V_{ov3}})^2}{2(\mathrm{V_{ov1}})}\frac{\Delta\beta_3}{\beta_1} + \frac{\mathrm{V_{ov3}}}{\mathrm{V_{ov1}}}\Delta\mathrm{V_{thn3}} -$$
$$\frac{\mathrm{V_{ov1}}}{2}\frac{\Delta\beta_1}{\beta_1} + \Delta\mathrm{V_{thn1}} \quad (4.18)$$

where $\mathrm{V_{ovi}}$ is the overdrive voltage of input transistors where i = 1, 2, 3 and 4.
Thus, the random input offset voltage $\sigma^2_{\mathrm{V_{OS\_input}}}$ is calculated from variance of Equation (4.18) as

$$\sigma^2_{\mathrm{V_{OS\_input}}} = \sum_{i=1}^{4}\left(\frac{v_{ovi}}{v_{ov1}}\right)^2\left(\sigma^2_{\mathrm{V_{thni}}} + \left[\frac{v_{ovi}}{2}\right]^2\sigma^2_{\beta\mathrm{i}}\right) \quad (4.19)$$

From Equation (4.19) it can be concluded that offset voltage is highly affected by the overdrive voltages, threshold voltage mismatch and transconductance parameter β mismatch of transistor $M_1 – M_4$.

4.4.2 Output offset voltage

To calculate the output offset voltage, output latch stage of proposed FDDCCST is simplified as shown in Figure 4.3. The inputs of the output latch stage are applied at the gate of transistors M_5 and M_8 which are connected to the ‘A’ and ‘B’ nodes. During comparison phase, when clk = $\mathrm{V_{DD}}$, nodes ‘A’ and ‘B’ start discharging at different rates if Vin+ ≠ Vin-. When Vin+ = Vin- and there is no

mismatch present in the transistors then both the nodes will discharge at equal rates. Therefore a balanced state is obtained at the output nodes ($V_{out+} = V_{out-}$). However, if a mismatch is present in the transistors of output latch stage, then the balanced state is disturbed ($V_{out+} \neq V_{out-}$). So, to maintain the circuit in balanced state, voltage V_{OS_output} should be applied at 'A' or 'B' node.

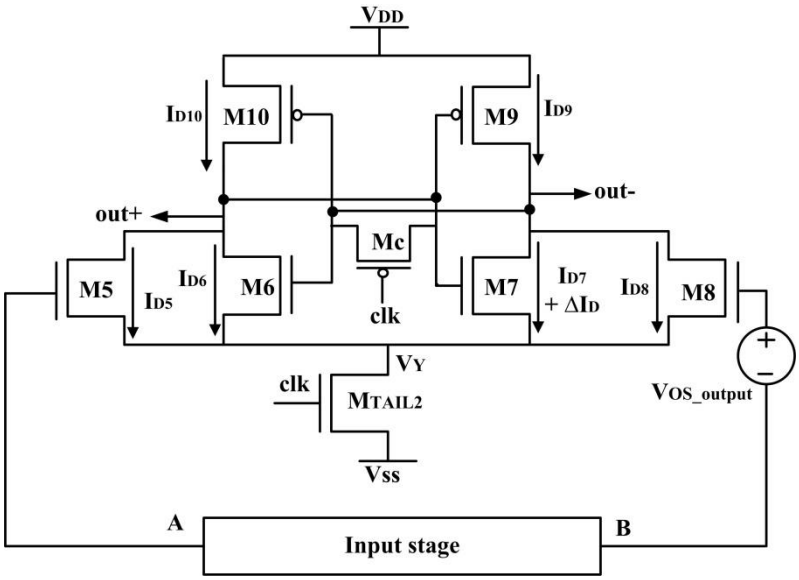

Figure 4.3 Simplified circuit of output latch stage of proposed FDDCCST

The operation regions of the transistors in the latch stage vary with time. Output nodes 'out+' and 'out-' discharge through transistors M_5 and M_8 and initially the voltage on the gate of these two transistors is V_{DD}, due to which they operate in saturation region. If Vin+ > Vin- then transistor M_9 and M_6 are in saturation region whereas transistors M_{10} and M_7 are in cut off region. The effect of mismatch in transistor pairs M_9 - M_{10} and M_6 - M_7 is ignored because during comparison phase, one of the transistors in each pair is in cut-off region and gets switched ON when the comparison is done, accelerating only the unbalanced process. So, the output offset voltage is affected by the mismatch exists between the transistors M_5 and M_8 only. To calculate the output offset voltage due to M_5 and M_8 mismatch is considered that,

Applying KCL at nodes 'out+' and 'out-', the currents I_{D9} and I_{D10} are given as

$$I_{D9} = I_{D7} + I_{D8} + \Delta I_D \tag{4.20}$$

$$I_{D10} = I_{D5} + I_{D6} \tag{4.21}$$

Since $I_{D9} = I_{D10}$, we get

$$\Delta I_D = I_{D5} - I_{D8} \tag{4.22}$$

The current difference ΔI_D after mismatch effect is given as

$$\Delta I_D = \frac{\beta_5}{2}(V_{G5} - V_Y - V_{thn5})^2 - \frac{(\beta_8+\Delta\beta_8)}{2}\left(V_{G8} + V_{OS\_output} - V_Y - V_{thn8} - \Delta V_{thn8}\right)^2 \tag{4.23}$$

Dividing by β_5 /2 and assuming that ΔI_D is very smaller than β_5, Equation (4.22) reduces to

$$V_{G5} - V_Y - V_{thn5} = \sqrt{\frac{1}{2}\left(1 + \frac{\Delta\beta_8}{\beta_5}\right)}\left(V_{G8} + V_{OS\_output} - V_Y - V_{thn8} - \Delta V_{thn8}\right) \quad (4.24)$$

From Equation (4.24), the output offset voltage V_{OS_output} is obtained as

$$V_{OS\_output} = \left(1 + \frac{1}{2}\left(1 + \frac{\Delta\beta_8}{\beta_5}\right)^{-2}\right)(V_{G5} - V_Y - V_{thn5}) + \Delta V_{thn8} \quad (4.25)$$

Assuming $\Delta\beta_8/\beta_5 << 1$, Equation (4.25) reduces to

$$V_{OS\_output} = \left(1.5 - \frac{\Delta\beta_8}{\beta_5}\right)(V_{G5} - V_Y - V_{thn5}) + \Delta V_{thn8} \quad (4.26)$$

Thus, the random output offset voltage $\sigma^2_{V_{OS\_output}}$ is calculated from variance of Equation (4.26) as

$$\sigma^2_{V_{OS\_output}} = {V_{ov5}}^2\sigma^2_{\beta 8} + \sigma^2_{V_{thn8}} \quad (4.27)$$

CHAPTER 5

SIMULATION RESULTS

The proposed FDDCCST has been designed and simulated in 0.18 μm CMOS technology with supply voltages of ± 0.75 V using Cadence Virtuoso Analog Design Environment. Figure 5.1 shows the transient response of the proposed FDDCCST during one clock cycle, when input signals Vin+ of 5mV and Vin- of 0V are applied having V_{cm} = 0.5 V, ΔV_{in} = 5mV, clk = 1.5 V_{p-p} and clock frequency (f_{clk}) of 500 MHz to calculate time period t_0 and t_{latch}. From the figure, it is observed that the total delay of the comparator is 0.219 ns where, t_0 = 0.11 ns and t_{latch} = 0.109 ns.

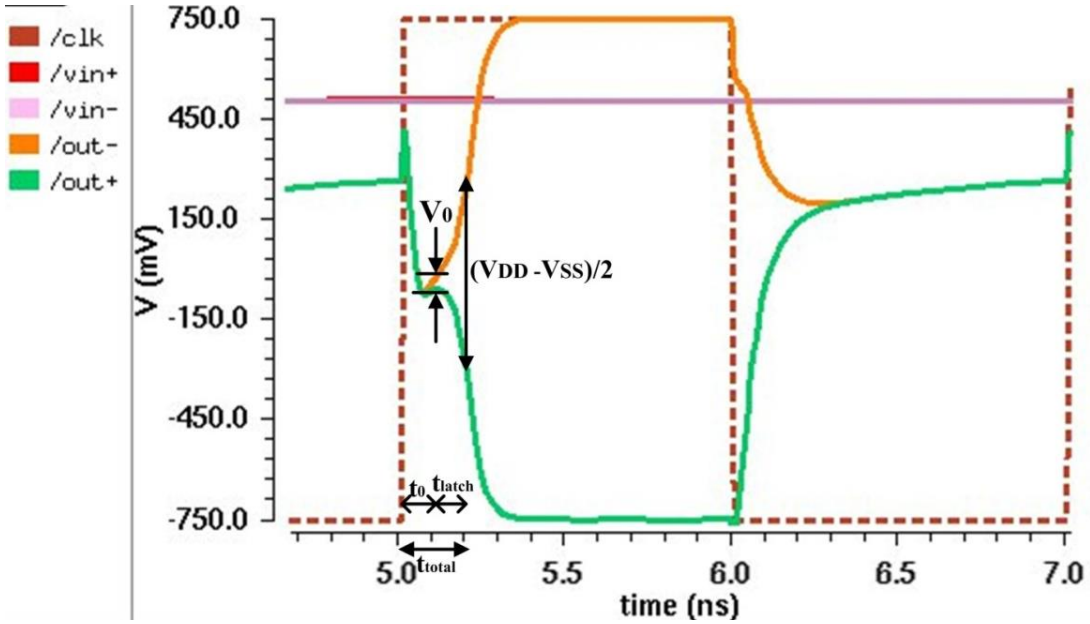

Figure 5.1 Transient response of the proposed FDDCCST during one clock cycle

The complete transient response of the proposed FDDCCST is shown in Figure 5.2, when two analog signals Vin+ and Vin- having amplitudes of 10 mV_{p-p} and 0 V_{p-p} respectively are applied. The common-mode voltage V_{cm} and f_{clk} are chosen as 0.5 V and 500 MHz respectively When Vin+ > Vin- , 'out-' node charges to V_{DD} whereas 'out+' node discharges to V_{SS}. Similarly, when Vin- > Vin+, 'out+' node charges to V_{DD} whereas 'out-' node discharges to V_{SS}.

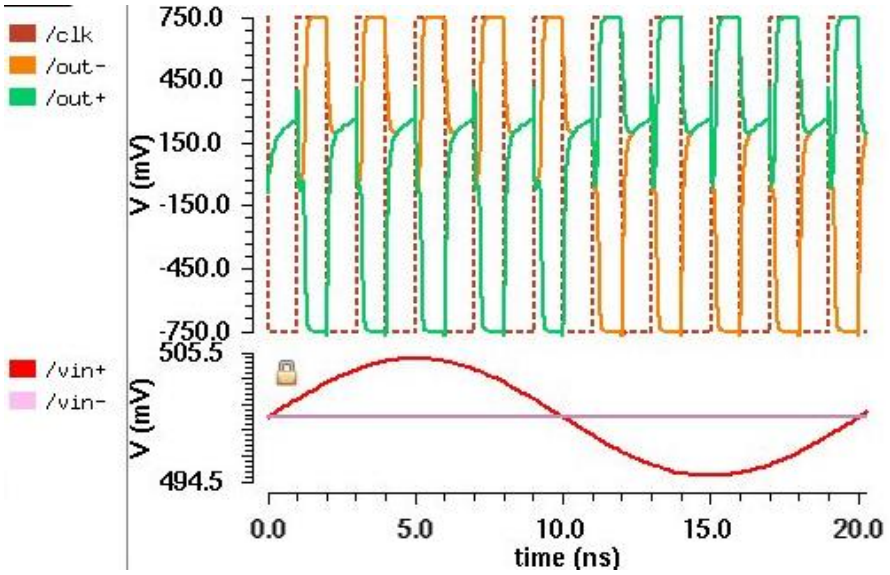

Figure 5.2 Transient response of the proposed FDDCCST for complete cycle of input waveform

The important parameters to determine the performance of the comparator are power dissipation, delay, area, PDP and offset. The effect of input differential voltage (ΔV_{in}) on delay of proposed FDDCCST at different common-mode voltages is shown in Figure 5.3. The delay of the comparator at ΔV_{in} = 5mV for V_{cm} = 0.5 is obtained as 0.219 ns. For the given value of common-mode voltage, the delay of the comparator decreases as input differential voltage increases. In addition, the delay also depends on the value of V_{cm}; it decreases as the V_{cm} increases. From the figure, it is clear that the delay is comparable for all the values of V_{cm} when ΔV_{in} > 10 mV.

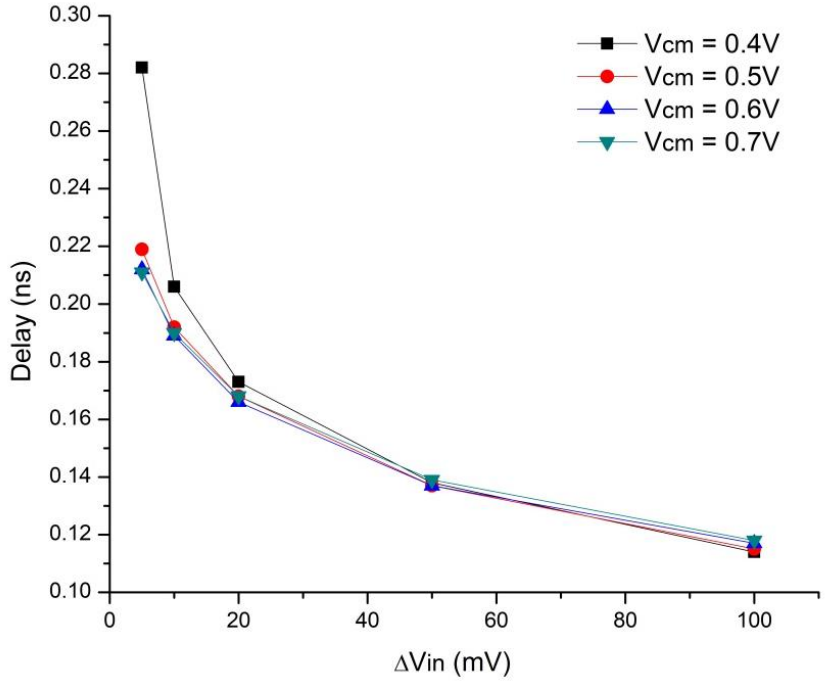

Figure 5.3 Delay versus input differential voltage (ΔV_{in}) at different common-mode voltages (V_{cm})

Figure 5.4 shows the dependence of input differential voltage (ΔV_{in}) on the PDP of the proposed FDDCCST at different V_{cm}. The delay and power reduces as input differential voltage increases due to which PDP also reduces. Similarly as delay, PDP is also less sensitive if the value of V_{cm} is more than 10mV.

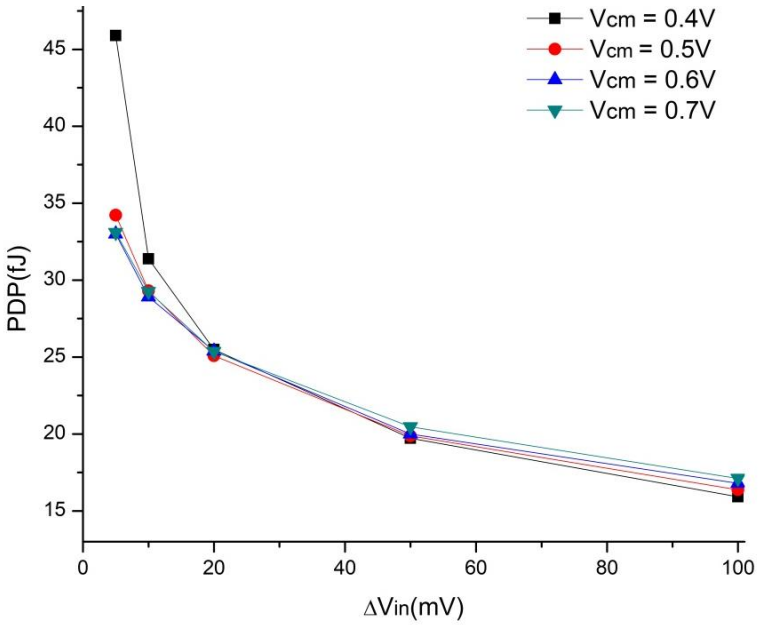

Figure 5.4 PDP versus input differential voltage (ΔV_{in}) at different common-mode voltages (V_{cm})

Figure 5.5 demonstrates the dependence of supply voltage on the power dissipation, delay and PDP of the proposed FDDCCST. The parameters are calculated at inputs having V_{cm} = 0.5 V, ΔV_{in} = 20 mV and f_{clk} = 500MHz. It shows that delay has inverse relationship whereas power has direct relationship with the supply voltage. PDP is calculated to find the optimum supply voltage for the best performance of the proposed FDDCCST.

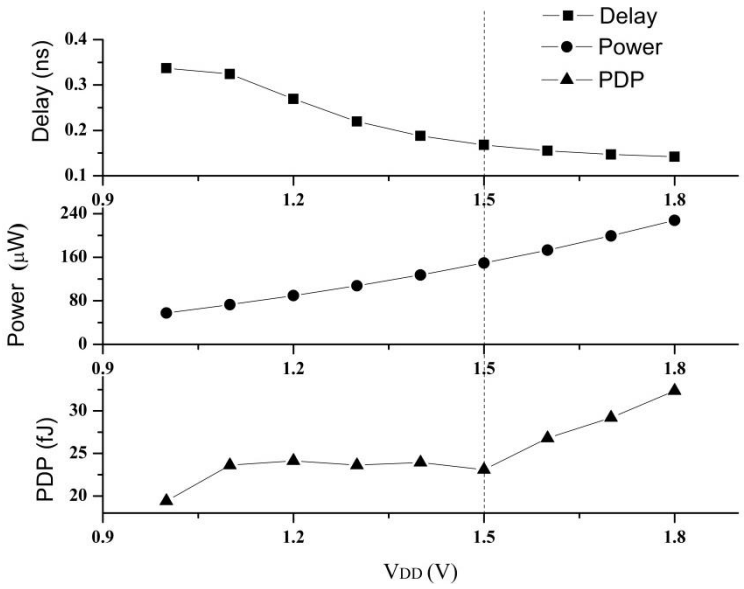

Figure 5.5 Effect of supply voltage on delay, power and PDP

Supply voltage of ± 0.75 V is chosen as the optimum value because at this value the PDP and offset voltage is low. Figure 5.6 shows the Monte-Carlo analysis for random offset voltage which is calculated by applying slow varying ramp signal (580 mV to 620 mV) on one of the input of the comparator keeping other input at a constant voltage of 0.6 V [31] [45-46] .

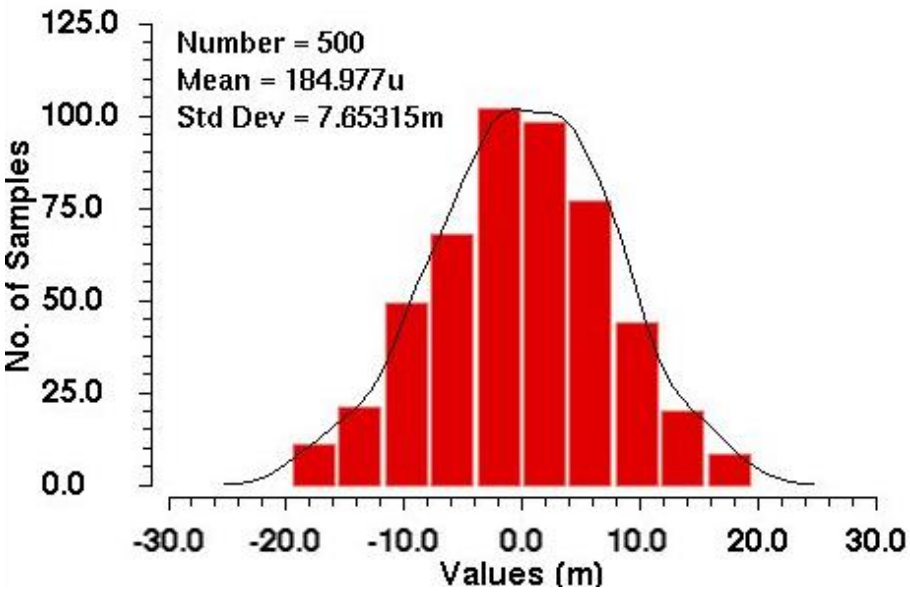

Figure 5.6 Histogram diagram of offset voltage using Monte Carlo simulation

From the figure it can be seen that the absolute offset voltage is 0.184 mV with 1σ deviation of 7.6 mV for the run of 500 samples. The proposed FDDCCST can successfully detect the difference of 4mV between the two inputs which results in 8 bit resolution.

The dependency of supply voltage on delay, power dissipation and PDP of the proposed FDDCCST at various input differential voltages are shown in Figures 5.7, 5.8 and 5.9 respectively.

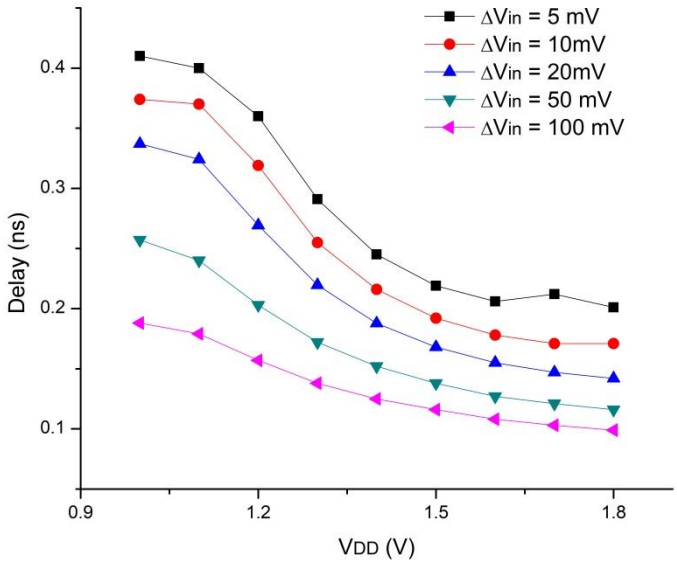

Figure 5.7 Delay versus supply voltage (V_{DD}) at different input differential voltages (ΔV_{in})

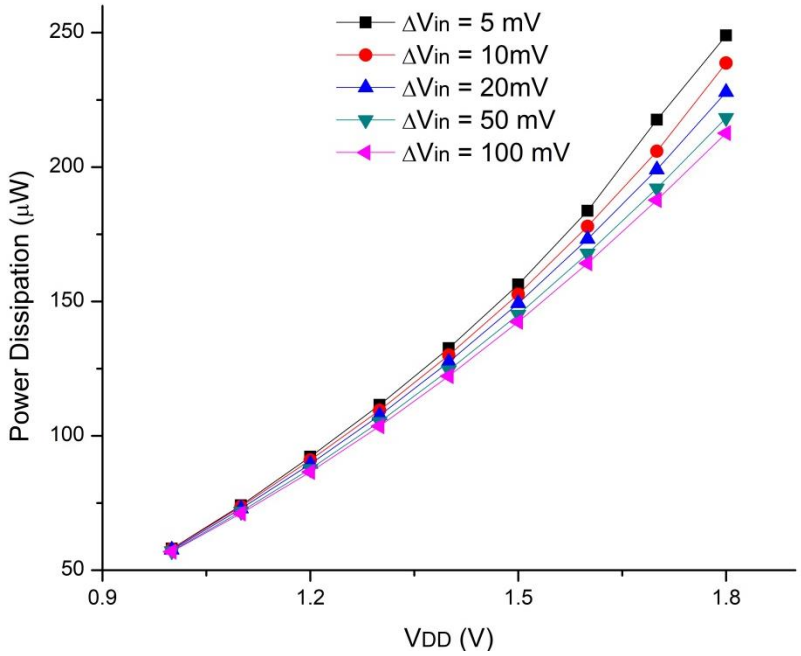

Figure 5.8 Power dissipation versus supply voltage (V_{DD}) at different input differential voltages (ΔV_{in})

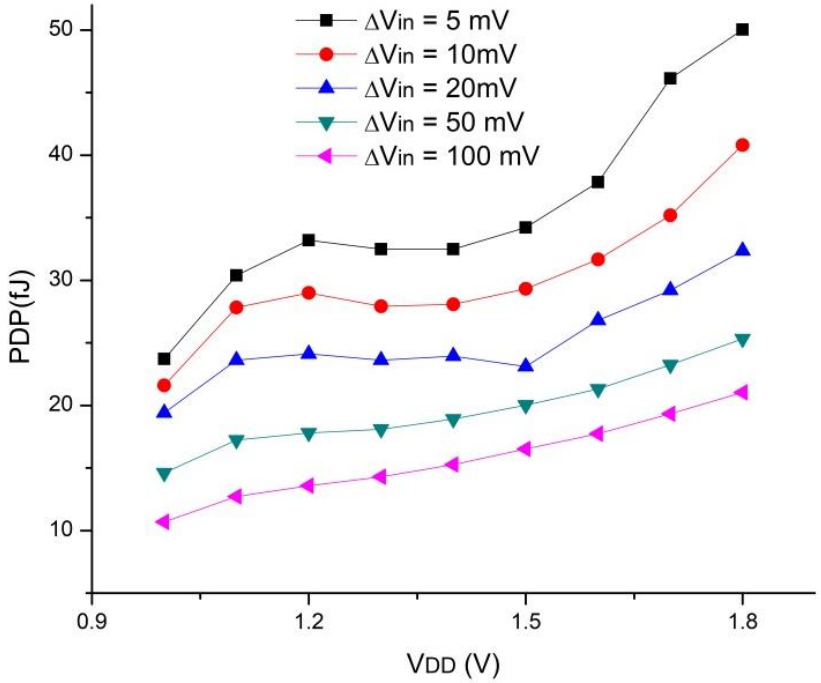

Figure 5.9 PDP versus supply voltage (V_{DD}) at different input differential voltages (ΔV_{in})

From Figure 5.7, if ΔV_{in} = 20 mV, the delay is obtained as 0.269 ns at V_{DD} = 1.2 V. This delay drops from 0.269 ns to 0.142 ns when V_{DD} changes from 1.2 V to 1.8 V. Similarly, in Figure 5.8 if ΔV_{in} = 20 mV, power dissipation is 89.5 μW at V_{DD} = 1.2 V which is increased to 228 μW at V_{DD} = 1.8 V. Furthermore, at a given V_{DD}, larger the value of input differential voltage the delay and power dissipation of the proposed FDDCCST decreases. As a result, PDP of the proposed FDDCCST also reduces as the value of input differential voltage increases at a constant V_{DD} as shown in Figure 5.9.

The layout of the proposed FDDCCST is designed using Cadence Virtuoso Layout XL editor is shown in Figure 5.10. To minimize the effect of parasitics and mismatchs all the transistors are positioned carefully which results in the layout area of 25.33 µm x 18.36 µm.

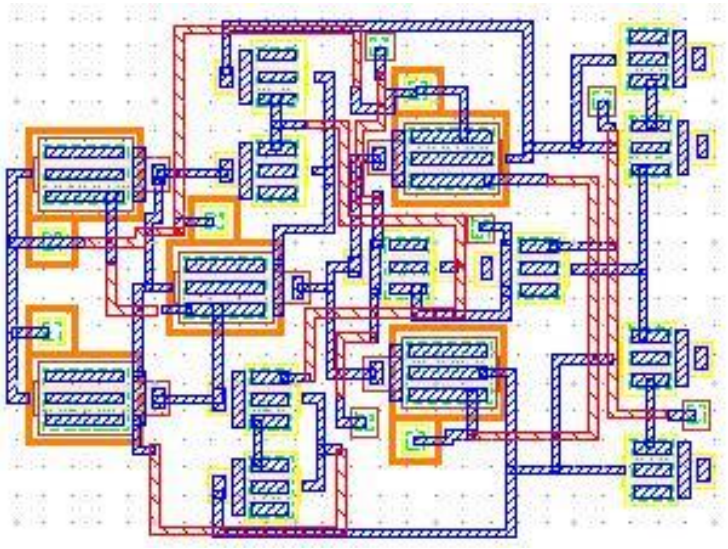

Figure 5.10 Layout of the proposed FDDCCST

To demonstrate the effectiveness of the proposed FDDCCST post-layout simulations for delay and PDP versus input differential voltage (ΔV_{in}) at various common-mode voltages (V_{cm}) are shown in Figures 5.11 and 5.12.

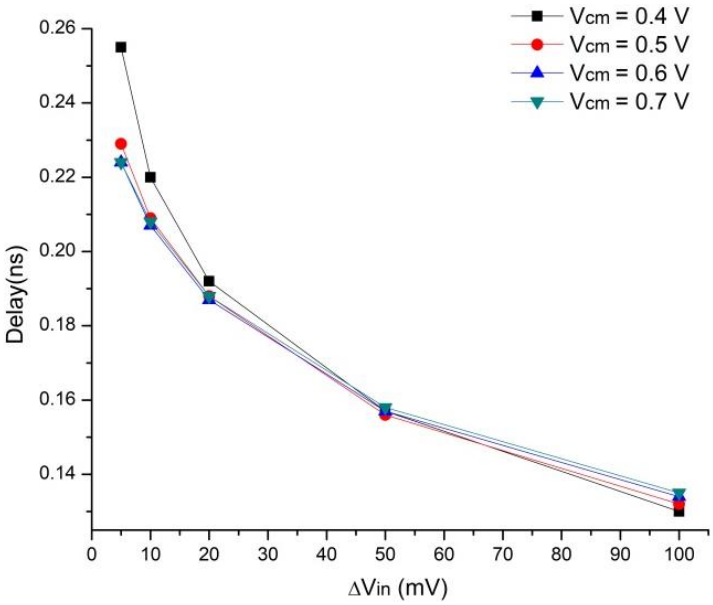

Figure 5.11 Post-layout delay versus input differential voltage (ΔV_{in}) at different common-mode voltages (V_{cm})

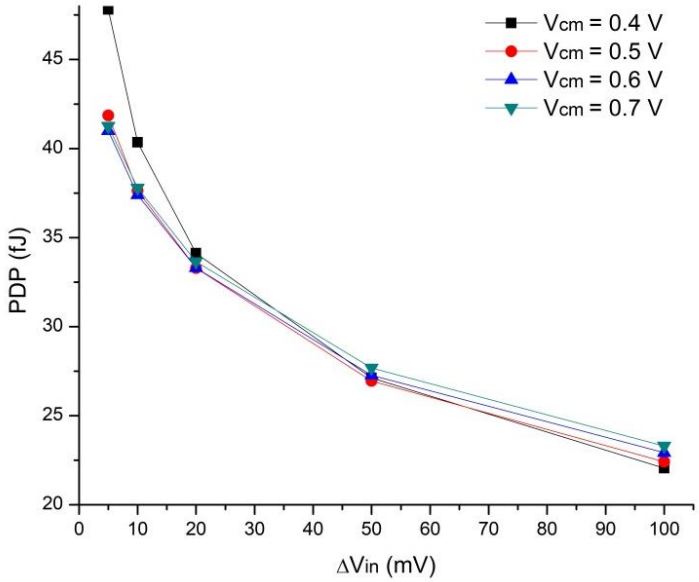

Figure 5.12 Post-layout PDP versus input differential voltage (ΔV_{in}) at different common-mode voltages (V_{cm})

From Figures 5.3, 5.4, 5.11 and 5.12, it is clear that post-layout simulation results are comparable to the pre-layout simulation results. To check the performance of the proposed FDDCCST in extreme conditions, corner analysis is performed with temperature as the design parameter. The comparator performance is observed at five different corners namely (a) Slow-Slow (SS), (b) Slow-Fast (SF), (c) Fast-Slow (FS), (d) Fast-Fast (FF) and (e) Nominal-Nominal (NN). The temperature value used at different corners is listed in Table 5.1.

Table 5.1 Different temperature values for corner analysis

Corners	Temperature (°C)
NN	27°
SS	85°
SF	27°
FS	27°
FF	0°

Figure 5.13 shows the transient response of the proposed FDDCCST when input signals are applied having input differential voltage ΔV_{in} = 5 mV, common- mode voltage V_{cm} = 0.5 V and f_{clk} = 500 MHz for different corners. The power supply voltage is chosen ± 0.75 V to perform the corner analysis. From the figure, it can be concluded that the comparator is fast at FF corner with the delay of 0.161 ns whereas it is slow at SS corner having delay of 0.31 ns.

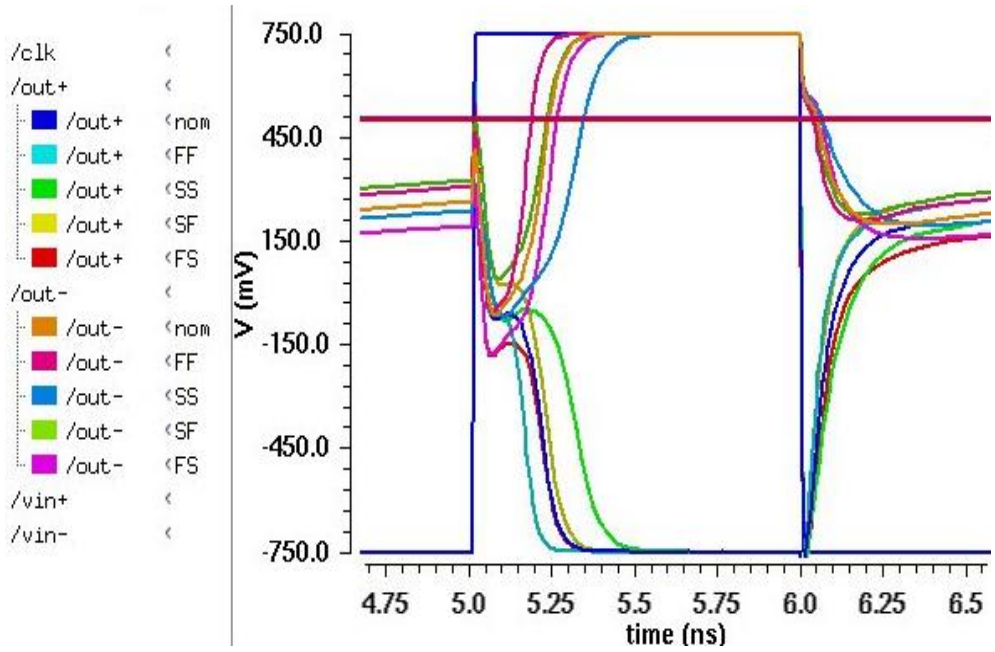

Figure 5.13 Transient response of the proposed FDDCCST at different corners

Pre-layout and Post-layout simulations results for various performance parameter i.e. delay, power and PDP at different corners considering inputs as V_{cm} = 0.5 V, ΔV_{in} = 5mV and f_{clk} = 500 MHz are shown in Figures 5.14, 5.15 and 5.16. From the Figure 5.14, it is observed that the post-layout delay of the proposed FDDCCST is comparable to pre-layout delay at all corners. Figure 5.15 shows that at FF corner proposed FDDCCST dissipate more power whereas at SS corner it dissipates less power. From the figures, it is evident that the proposed FDDCCST operates at all four corners within the acceptable range. From the Figures 5.14 and 5.15, it can also be concluded that the delay is comparable in post-layout simulation whereas power is slightly increased due to the presence of parasitic capacitances. With an increase in power, PDP also increases as shown in Figure 5.16.

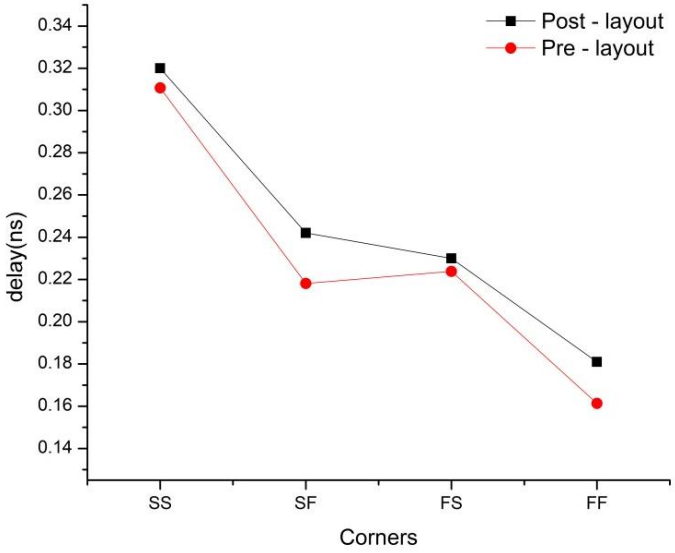

Figure 5.14 Pre-layout and post-layout delay at different corners

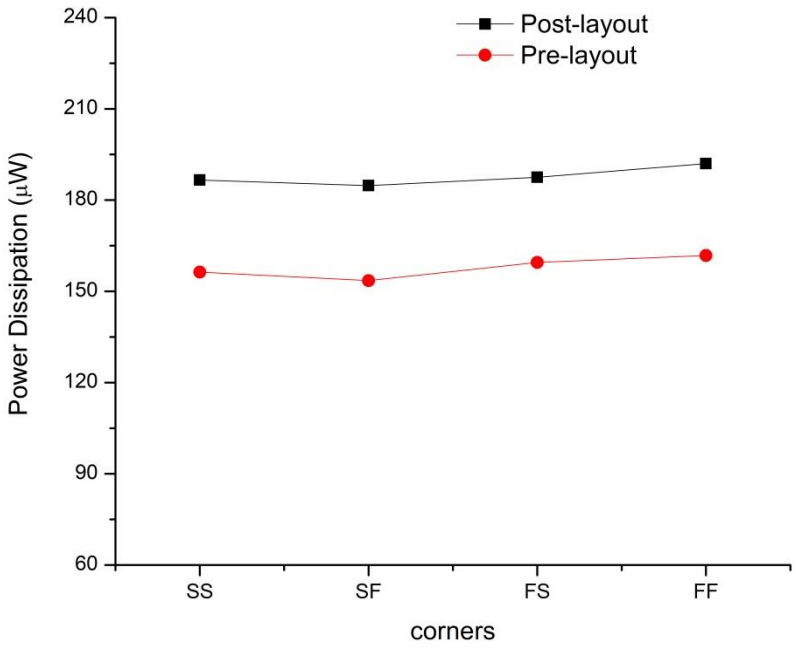

Figure 5.15 Pre-layout and post-layout power dissipation at different corners

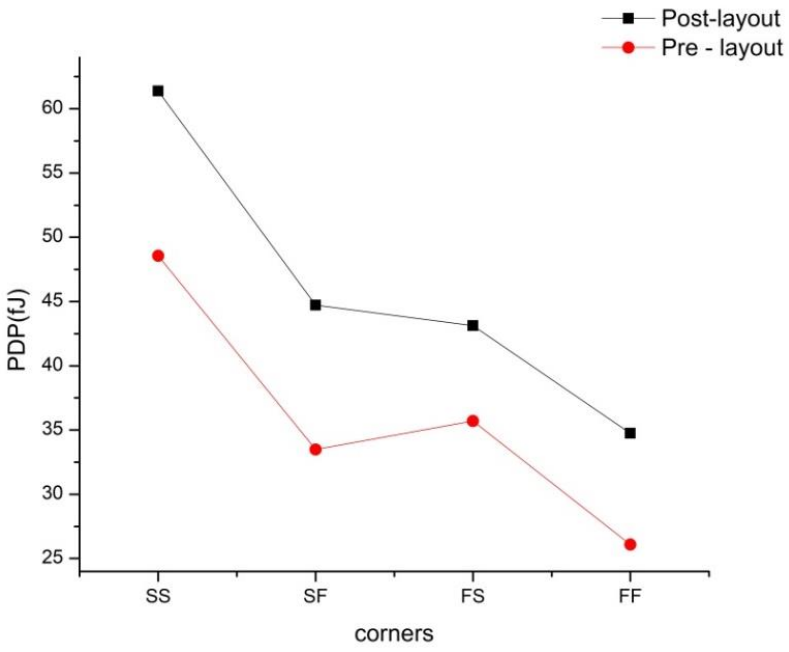

Figure 5.16 Pre-layout and post-layout PDP at different corners

Table 5.2 compares the performance parameters of the proposed FDDCCST with other comparator structures reported in the literature. As observed from the table, the proposed FDDCCST offers reduced delay and power for all values of input differential voltage when compared with other comparator structures discussed in the literature. It also provides low offset voltage of 0.18 mV.

Table 5.2 Comparison of proposed FDDCCST with different dynamic comparators reported in the literature

Parameters ↓ Comparator structures→	[9]	[21]	[35]	[29]	[30]	[47]	[27]	[34]	Proposed
Year	2014	2017	2011	2016	2016	2017	2018	2018	2019
Technology (nm)	180	180	180	180	180	180	180	180	180
Supply voltage (V)	1.2	1.2	1.8	---	---	1.8	± 0.9	---	± 0.75
Clock Frequency (GHz)	0.5	0.5	0.1	0.8	0.62	0.1	1.3	0.5	0.5
Delay (ns)	0.55	0.273	1.699	---	---	---	0.37	0.30	0.219
Power dissipation (μW)	329	196	460	780	1200	900	265.25	150	156.3
Power delay product (PDP) (fJ)	181	53.50	736	---	---	---	8.59* 98.14	45	34.22
Offset voltage (mV)	7.8	2.07	---	0.15	0.35	---	0.36	2.4	0.184
Bit resolution	---	---	---	---	9 - 10	11	10	---	8
Area (μm^2)	---	---	2220.45	---	---	---	256.8	430	465.05

*PDP is calculated using formula PDP = (delay) x (static power). All other PDPs are calculated using formula PDP = (delay) x (average power).

CHAPTER 6

CONCLUSION AND FUTURE SCOPE

6.1 CONCLUSION

A detailed analysis of proposed FDDCCST is presented in this thesis which is suitable for low-voltage and low-power applications due to its double stage structure. The proposed FDDCCST is less sensitive to the mismatches present in the MOSFETs because it has fully differential pairs in its input stage. Due to this, the proposed FDDCCST has the offset voltage of 0.18 mV. Pass transistor logic is used to share the charge between the output nodes allows the proposed FDDCCST to operate faster and consume less power making it suitable for high speed applications. From the simulation results, it is evident that the power, delay and PDP of the proposed FDDCCST are improved than the other structures reported in the literature. The corner analysis is also performed to show the performance of proposed FDDCCST in extreme conditions.

6.2 FUTURE SCOPE

The proposed FDDCCST presented in this thesis can also be used as a building block in various applications such as ADCs, memories, etc. Due to low-power and low-voltage operation of proposed FDDCCST it can also be used in biomedical applications.

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LIST OF PUBLICATION

1. Sanchita and R. Pandey, “Design and Analysis of low-power, low offset and high-speed fully differential double-tail dynamic comparator using charge sharing technique,” Communicated for the possible publication in Analog Integrated Circuits & Signal Processing journal. (SCI Index) (Under Review)