3-BIT Flash ADC using Cadence Allegro / OrCAD 24.1

A Thesis submitted in partial fulfillment of the requirement for the Award of the Degree of

MASTER OF TECHNOLOGY

in VLSI DESIGN

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JULY 2025

DECLARATION

I, hereby declare that the project entitled '3-BIT Flash ADC using Cadence Allegro / OrCAD 24.1' is a record of our own work carried out in Stryker, Gurugram and Electronics and Communication Engineering Department, Thapar Institute of Engineering & Technology, Patiala under the guidance of Dr. **Hari Shankar Singh (DECE)** and **Dr. Jaswinder Kaur (DECE),** Associate Professors during July 2024- July 2025.

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This is to certify that **Anshu Maurya** has successfully completed her internship from **22nd July 2024 to 11th June 2025** at Stryker Global Technology Center Pvt. Ltd. Gurgaon.

The project **Combi Console (PCBA, PCB Development)** was successfully completed under the guidance of Mr. Sudhanshu Shekhar, Sr. Staff Engineer AO, Instrument Department. Project Management Reporting Dashboard using Power BI was successfully completed under the guidance of Mr. Manish Katariya, Staff Engineer, Medical Department.

Anshu Maurya was seen as a responsible and committed individual. We wish her all the best for all her future endeavors.

For **Stryker Global Technology Pvt. Ltd**

Amit Singh Bisht
Manager-Human Resources

ACKNOWLEDGEMENT

I would like to extend my heartfelt gratitude to all those who have contributed towards the successful completion of the project and converge thanks to the entire Stryker, Gurugram team, our supervisors Dr. Harishankar Singh, Dr. Jaswinder Kaur and all the faculty & staff members of Electronics and Communication Engineering (ECED), Thapar Institute of Engineering & Technology for generously extending their support and for sparing their valuable time to guide us towards the completion of this project work.

I would like to place a special word of appreciation to the Electronics Department for their guidance and help. Also, I would like to thank my parents and friends whose responses and coordination were of utmost importance for the completion of this project work in these unprecedented times.

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TABLE OF CONTENTS

LIST OF FIGURES

ABSTRACT

With the increasing demand for high-speed, low-power electronic devices, signal integrity (SI) has become a crucial aspect of printed circuit board (PCB) design. Analog-to-Digital Converters (ADCs) play a vital role in signal processing, system-on-chip (SoC) designs, and mixed-signal applications by converting analog signals into digital data. This report presents the design and implementation of a 3-bit flash ADC using Cadence Allegro/OrCAD 24.1, an industry-standard electronic design automation (EDA) tool.

The PCB design process is explored in three major steps: schematic entry, PCB layout, and SI analysis. Design Entry CIS and Allegro AMS Simulator are used for schematic capture and circuit simulation, while Allegro PCB Editor is utilized for layout design and routing. The 3-bit flash ADC architecture, consisting of a resistor ladder, comparators, and an encoder, is analyzed for performance at varying input frequencies. Key metrics such as resolution, sampling rate, and power consumption are examined to assess functionality.

The report also evaluates PCB design tools, considering essential features like multilayer design capability, footprint creation, autorouting, and 3D visualization. While Cadence Allegro provides robust design capabilities, challenges such as high cost, complex user interface, and intricate file management are discussed.

This report focuses on designing and implementing a 3-bit flash Analog-to-Digital Converter (ADC) using Cadence Allegro 24.1. ADCs play a vital role in signal processing, system-on-chip (SoC) applications, and mixed-signal designs, converting analog signals into digital representations for further processing. The performance of an ADC is determined by key factors such as resolution, sampling rate, and power consumption. Given the complexity of analog circuit design and storage, digital conversion is essential for efficient processing.

The report provides a step-by-step guide to PCB design, covering schematic entry, PCB layout, and signal integrity analysis using Cadence tools. Design Entry CIS 24.1 is used for schematic entry and circuit simulation, while Allegro PCB Editor facilitates layout design and trace routing. This tutorial serves as a foundational resource for learning PCB design methodologies and EDA tool utilization, offering insights into high-speed circuit development and analysis.

This study serves as a practical guide for engineers, researchers, and students looking to enhance their knowledge of high-speed PCB design and ADC implementation. By leveraging modern EDA tools, optimized circuit development methodologies can be achieved for advanced electronic applications.

CHAPTER 1: INTRODUCTION

1.1 Overview

With the rapid evolution of high-speed electronic systems, Printed Circuit Board (PCB) design has become increasingly complex. Among the critical factors affecting circuit performance is Signal Integrity (SI)—a measure of the quality of electrical signals as they travel through a PCB. As data rates increase and devices become more compact, SI analysis becomes an indispensable part of the PCB design process. Engineers often face challenges such as trace rerouting, via relocation, impedance mismatches, and crosstalk mitigation to ensure performance specifications are met.

To address these challenges, Electronic Design Automation (EDA) tools are extensively used. Tools such as Cadence Allegro and OrCAD allow designers to model, simulate, and validate circuit behavior from schematic to final PCB layout. Familiarity with these tools is essential for building robust high-speed systems.

1.2 Motivation

The growing demand for battery-operated and portable devices has shifted design focus towards low-power, high-speed circuits, especially in mixed-signal systems. Analog-to-Digital Converters (ADCs) are a core component in such systems, enabling the interface between the analog physical world and digital processing units. ADCs are widely used in signal processing, instrumentation, communication systems, and SoC (System-on-Chip) applications.

Despite their critical role, designing and testing analog circuits remains a challenge due to their continuous-time behavior and noise sensitivity. Converting analog signals into digital form simplifies processing, storage, and transmission. This makes ADCs a vital enabler for real-time digital signal applications.

1.3 Problem Statement

While industry-standard tools like Cadence Virtuoso are widely used for IC-level design, tools like Cadence Allegro/OrCAD are less frequently explored in academic settings, especially for PCB-based implementations of ADCs. This project aims to bridge that gap by designing a 3-bit Flash ADC using Cadence Allegro 24.1, demonstrating the full design flow—from schematic to PCB layout and simulation—within a professional-grade EDA environment.

1.4 Objectives

- To design a 3-bit Flash ADC using discrete components modeled in Cadence tools.
- To implement and verify the ADC design through schematic capture, layout, and signal integrity analysis.

- To understand and apply the Cadence Allegro/OrCAD suite for a complete PCB design cycle.
- To evaluate the performance limits of the designed ADC under varying input conditions.

1.5 Scope of Work

This thesis focuses on the practical implementation of a 3-bit Flash ADC architecture. The work includes:

- Use of Design Entry CIS for schematic design.
- Simulation using Allegro AMS Simulator (formerly OrCAD PSpice).
- PCB layout design using Allegro PCB Editor.
- Manual footprint placement, routing, and signal integrity considerations.
- Performance analysis at different input frequencies (e.g., 10 kHz and 300 kHz).

While the primary scope is limited to a 3-bit Flash ADC, the methodology serves as a template for scaling to higher resolutions and more complex architectures.

1.6 Organization of the Report

- **Chapter 2** presents the literature survey, including ADC architectures and PCB tool evaluations.
- **Chapter 3** details the design methodology followed.
- **Chapter 4** discusses simulation results and performance analysis.
- **Chapter 5** demonstrated the conclusion and future scope for the entire report.
- The report concludes with references and appendices that support the technical content.

CHAPTER 2: LITERATURE

The paper by R. Balog Jr., titled *"Printed Circuit Board (PCB) Overview and Design Issues"* (2004), serves as an essential primer on the fundamental aspects and challenges associated with printed circuit board (PCB) design. The author introduces the critical role of PCBs in modern electronics, emphasizing their function as both mechanical support and an electrical interconnect for electronic components.

The document outlines key elements of PCB construction, including material selection (like FR-4), layer stack-up, and trace layout. It also covers fundamental design parameters such as impedance control, signal integrity, and power distribution—highlighting how these factors impact overall circuit performance. Moreover, it identifies thermal management and electromagnetic compatibility (EMC) as major design considerations, especially in high-speed and high-power applications.

Balog also discusses practical issues in the PCB design flow, including schematic capture, layout, design rule checks (DRC), and manufacturability concerns. The paper is notable for bridging the gap between theoretical understanding and practical implementation, making it highly relevant for engineers, especially those at the entry level or transitioning into hardware design roles.

This work is frequently cited in introductory courses and training modules related to electronics and PCB layout, owing to its concise structure and foundational coverage. Compared to more advanced texts or simulation-based approaches, Balog's overview remains grounded in real-world design challenges, providing an accessible yet insightful perspective into PCB engineering.

In the presentation titled "AD Converter: Custom IC Design Flow and the Required CAD Tools and Resources," delivered by K. H. Kim at EMLab, University of Illinois at Urbana-Champaign on February 13, 2006, the author provides an in-depth exploration of the design methodology for analog-to-digital (AD) converters within the context of custom integrated circuit (IC) development.

Kim outlines the complete custom IC design flow, starting from system-level specifications, moving through behavioral modeling, transistor-level design, layout, and ultimately verification and fabrication. A significant emphasis is placed on the CAD tools essential at each stage—highlighting EDA platforms such as Cadence, Mentor Graphics, and Synopsys for tasks ranging from schematic capture and simulation (e.g., SPICE) to physical design and verification (e.g., DRC, LVS).

One of the strengths of this work lies in its practical orientation, showcasing not only the theoretical steps but also the resources, toolchains, and design strategies required to implement high-performance AD converters. It addresses key design challenges such as linearity, power efficiency, layout-dependent effects, and matching considerations, all of which are critical in analog and mixed-signal IC design.

Compared to purely academic treatments of AD converters, Kim's presentation bridges academia and industry practice, making it valuable for students and professionals aiming to gain insights into real-world custom IC

workflows. It also serves as a foundational reference for design teams planning to implement analog front ends in systems-on-chip (SoCs).

In the work titled “Analog-to-Digital Converters” (2004), Wolfgang Reis presents a comprehensive overview of the principles, architectures, and performance considerations involved in the design and application of analog-to-digital converters (ADCs). This document is well-regarded for offering both theoretical insights and practical guidance, making it a valuable resource for engineers and researchers involved in signal processing and mixed-signal circuit design.

Reis begins by discussing the basic function of ADCs—converting continuous analog signals into discrete digital representations—and the key performance metrics, such as resolution, sampling rate, signal-to-noise ratio (SNR), and effective number of bits (ENOB). He then explores the different ADC architectures, including flash, successive approximation register (SAR), sigma-delta (ΣΔ), and pipelined converters, comparing their strengths and trade-offs in terms of speed, accuracy, power consumption, and complexity.

What sets this work apart is its clear explanation of how design choices affect linearity, quantization noise, and overall system performance. The document also touches on technology trends, such as scaling effects in CMOS processes and their impact on analog design, as well as the growing need for high-resolution ADCs in applications like instrumentation, communications, and digital audio.

Compared to other literature in the domain, Reis’s treatment is notable for its breadth and clarity. It strikes a balance between academic rigor and practical relevance, making it useful for both newcomers seeking foundational understanding and experienced designers looking for a refresher on ADC design principles.

As time has progressed, technology has become more accessible. PCB design tools used to be priced so high that only companies could afford them. Today many PCB tools are available to the home user. Each tool has a different set of strengths and weaknesses, though there are some really standout tools that are either free, open-source, or relatively low-cost. Many of the freeware programs are a subset of a commercial code. Some may be skeptical about the usability and productivity of freeware, open-source, or low-cost programs. With regard to PCB tools, I have established a list of criteria that I find essential. Please note that freeware programs are often more polished than some open-source programs but will have limitations, such as number of components or pins allowed. Here is the minimum standard that I have set for PCB tools for my home use.

Native schematic tool: Some programs require an external schematic editor. Even simple designs tend to change as you work through them. Some of the changes are as simple as changing an input pin on the microcontroller but may also include adding circuits to increase functionality. If the schematic editor is not tied to the rest of the software package, it is very easy for changes not to propagate into the final design.

Footprint wizard: This is something that makes life much easier. PCB products without a footprint wizard have a tedious workflow[4]. They direct you to find a product from the library that is somewhat

similar and modify it. The problem with this workflow is that many new sensors are coming out with nonstandard footprints. Hacking something to fit your needs is tedious. It is much easier to start from scratch. With a good footprint wizard, you should be able to have a new part created in less than five minutes.

Multilayer design capability: A two-layer board greatly simplifies routing, and most PCB prototyping houses offer this as their base option.

3D preview: Perhaps this is because of my mechanical background, but I find that this capability is underrated by many. With 3D preview, it is very easy to verify that all your parts will fit, and that you will have sufficient access to solder the parts. In my last project, I was able to use 3D preview to identify a problem very quickly with my connector spacing and correct it. This will serve as your final design check before manufacturing.

AutoRoute: Though many purists will argue that an autoroute is not desirable, I disagree. An autoroute helps find the best placement for components and can be used in an iterative method. I usually hand route any critical traces and then autoroute the remaining traces, followed by a final cleanup performed by hand. With care, an autoroute can be used to great advantage and can dramatically reduce the time spent in your design.

Evaluating PCB layout tools: As edge rates of logic devices become faster and PCB designs become more advanced and geared towards miniaturization, a number of issues and pitfalls can emerge at the layout stage if you do not have appropriate tools at your disposal to handle your requirements [5]. In-depth experience using the various PCB layout tools available today is the best indicator of the direction to take regardless of densities, application, or speed requirements. Some design tool parameters that require some experience involve design speeds ranging from a few megahertz (MHz) to over 15 gigahertz (GHz) with board layer counts going from single layer to 50 layers, sometimes more [6].

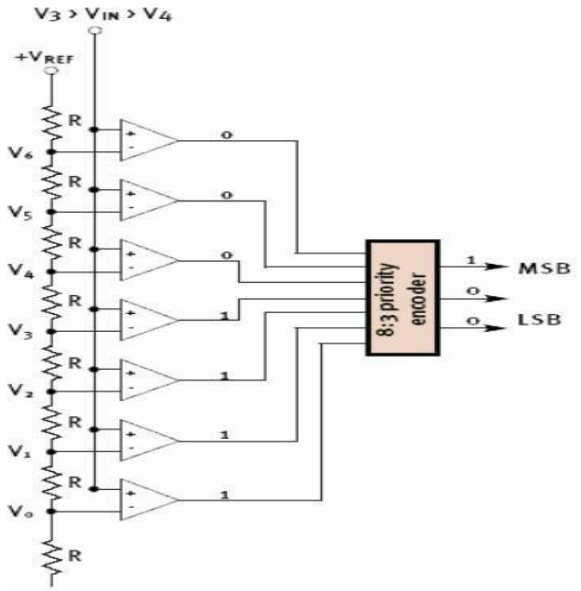

Fig-1: Three-Bit parallel Flash ADC Architecture

Cadence Allegro: Allegro is one of the oldest and the most diversified tools in the industry. No one can question the power it gives to the designer to tweak every aspect of the layout. It also has one of the best constraints managers that give better control on signal and power integrity of the board [7]. It is also the best tool to handle many board layers. Ever since Cadence bought OrCAD, their developers have tried to integrate the two. Therefore, one will find that Cadence OrCAD for schematic capture is integrated to a certain extent with Allegro for layout. Allegro PCB SI and OrCAD Signal Explorer help to do a pre- and post-layout signal integrity analysis and are efficient at doing this for complex PCBs [8]. Allegro also provides a much better integration to Allegro PCB router, formerly known as Cadence SPECCTRA, than any other layout tool. SPECCTRA is one of the most well-known products used for Auto-routing.

Installation of Cadence Allegro 24.1 should be straightforward. If one does not have the CDs, CD image files for installation can be found at http://download.cadence.com. Thus, the Cadence Allegro 24.1 software suite is also known as Cadence SPB 24.1 [9]. In this report, this software version (24.1) will be used interchangeably with version 24.1 Version 24.1.1 adds additional eye diagram features that make plotting eye diagrams easier.

During installation a valid license server will be requested of the user. It should be noted that in the Windows operating system installation, it will only require and ask for the first three CDs. The fourth CD has additional libraries that can be installed on its own if one so desires. It is recommended that this fourth CD be installed, especially for Design Entry HDL libraries. It will be assumed for the remainder of the report that the reader uses the Windows operating system installation of Cadence Allegro.

Cadence Allegro 24.1 is also capable of package design. Typically, an organization would use Cadence Virtuoso to layout and verify all of the chip-level designs and then migrate that design along the package and PCB flow.

However, Allegro is not without its drawbacks and limitations. Most importantly is its cost. A Cadence seat along with a suite that can handle almost all design needs can cost upwards of $90K[10]. Spending this amount on a layout tool by a mid-sized company or start up OEMs does not seem plausible and would be the deciding factor for most.

Secondly, Cadence tools are sometimes too complicated and cryptic to understand. The GUI is not intuitive or user friendly. Many functions are hidden deep within the tool and many easy tasks are difficult to carry out. Moreover, Allegro part libraries are difficult to create and maintain [11].

Thirdly, Cadence has a tortuous file structure that is awkward to manage. Generating outputs for manufacturing can become an arduous task in Allegro. As an example, a PCB designer has to go through numerous steps in specific order to setup and generate drill files and Gerbers. Also, this tool is not effective at handling multiple copper fills for power and ground planes. Designers must work diligently while dealing

with static and dynamic shapes and suffice to say that handling numerous copper shapes in Allegro is not a walk in the park and can become too laborious for some.

Finally, Cadence Allegro is notorious for the use of its scripts and macros to perform basic tasks that could be performed automatically in other layout tools.

An Analog-to-Digital Converter (ADC) is a crucial component in modern electronic systems, responsible for converting continuous analog signals into discrete digital values. This conversion process allows analog signals, such as sound, temperature, or light intensity, to be processed by digital systems like microcontrollers, digital signal processors, and computers. ADCs are essential in a wide range of applications, including audio and video recording, medical imaging, telecommunications, and instrumentation. The performance of an ADC is characterized by several key parameters, including resolution, sampling rate, and signal-to-noise ratio (SNR)[12]. Resolution, typically measured in bits, determines the number of discrete levels the ADC can output, with higher resolution providing more precise representations of the analog signal. The sampling rate, measured in samples per second (S/s), defines how frequently the ADC samples the analog input, with higher rates capturing more detail from rapidly changing signals. Various types of ADC architectures exist, each optimized for different performance criteria: Flash ADCs offer very high speed but are limited in resolution; Successive Approximation Register (SAR) ADCs provide a balanced trade-off between speed and resolution; Sigma-Delta ADCs are known for their high resolution and accuracy, making them ideal for audio applications; and Pipelined ADCs combine high speed and high resolution, suitable for applications like video processing[13]. Advances in CMOS technology have enabled the development of ADCs with higher performance and lower power consumption, making them integral to the continued evolution of digital electronics.

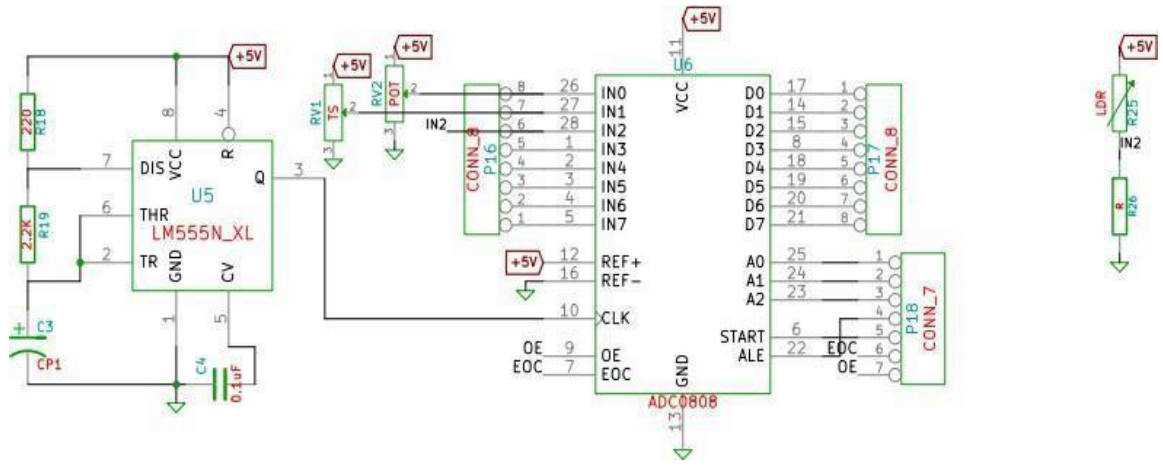

Fig-2: ADC Schematic Circuit

In order to sufficiently exercise the Cadence Allegro tools, it would be best to build a simple yet useful circuit and complete a full design cycle. Since this work is related to high-speed ADCs, it is fitting to design one. Therefore, a 3-bit flash ADC was selected to be designed. The architecture is also very convenient for a board design, since the resistors, comparators, and encoder are easily obtained in packaged chips.

The core of this flash ADC architecture are the parallel voltage comparisons made between the input signal and several reference voltages [14]. In our topology this is done by eight voltage comparators eventually resulting in three digital bits. We will use the Texas Instruments TLC3704 low power CMOS analog comparator chip for this function. Upon selecting this part, it is stated that there are four parts per package, meaning according to the pin-out, there are four comparators in each chip[15]. Therefore, we need two total packages for all the comparators. For n-bit ADC 2n -1 comparators the resistive ladder network is the set of resistors, it acts as a voltage divider, and it produces reference voltages to the comparator. Comparator is an important component in Flash ADC, which converts the analog signal into digital signal [16].

Key Concepts of ADCs

Resolution: The resolution of an ADC is the number of distinct output levels it can produce, typically expressed in bits. For example, an 8-bit ADC can produce 256 (2^8) distinct levels.

Sampling Rate: The sampling rate is the frequency at which the ADC samples the analog input signal. It is usually measured in samples per second (S/s).

Quantization Error: Quantization error is the difference between the actual analog value and the quantized digital value. It is inherent in the conversion process.

Types of ADCs:

Flash ADC: Provides very fast conversion times but is typically limited to lower resolutions.

Successive Approximation Register ADC: Offers a good balance between speed and resolution.

Sigma-Delta ADC: Known for high resolution and accuracy, often used in audio applications.

Pipelined ADC: Combines high speed and high resolution, suitable for applications like video processing.

A 3-bit Flash Analog-to-Digital Converter (ADC) is a type of ADC that converts an analog input signal into a 3-bit digital output. Flash ADCs are known for their high speed because they use a parallel architecture, allowing them to convert signals almost instantaneously. Here's an overview of how a 3-bit Flash ADC works:

Components and Operation

Reference Voltage Divider:

A resistor ladder network is used to divide the reference voltage into 2^3 - 1 = 7 equally spaced reference voltages.

These reference voltages are fed to the non-inverting inputs of 7 comparators.

Comparators:

There are 7 comparators in a 3-bit Flash ADC.

Each comparator compares the analog input voltage to one of the reference voltages The output of each comparator is a digital signal indicating whether the input voltage is higher or lower than the reference voltage.

CHAPTER 3: APPROACH / METHODOLOGY

Proposed Methodology

- Schematic Design: Schematic design is the process of creating a blueprint for an electronic circuit. It involves drawing the circuit diagram, which includes all the components (resistors, capacitors, transistors, etc.) and their connections. This stage is crucial for understanding the functionality of the circuit and serves as a guide for the subsequent stages.
- IC Layout: IC layout is the process of converting the schematic diagram into a physical layout that can be fabricated on a semiconductor wafer. This involves placing and routing the various components and interconnections on different layers of the chip. The layout must adhere to design rules to ensure manufacturability and performance.
- Layout Verification: Layout verification is the process of checking the IC layout against the schematic design to ensure that they match. This includes Design Rule Checking (DRC) to ensure the layout adheres to manufacturing rules, and Layout Versus Schematic (LVS) to verify that the layout accurately represents the schematic.
- Package Design: Package design involves designing the physical packaging for the IC to protect it from environmental damage and to provide the necessary electrical connections to the external world. This includes choosing the appropriate package type (e.g., QFP, BGA) and designing the lead frame or substrate.
- Layout – 2: Layout – 2 refers to the second iteration of the layout process. After initial layout and verification, modifications may be necessary to optimize performance, reduce power consumption, or address any issues found during verification. This stage involves refining the layout based on feedback and simulation results.
- Simulation – 2: Simulation - 2 involves the second round of simulations to verify the performance of the refined layout. This includes functional simulation, timing analysis, and power analysis to ensure that the design meets the required specifications and performs correctly under different conditions.
- PCB Design: PCB design is the process of designing the printed circuit board that will house the IC and other components. This involves creating the board layout, placing components, and routing the electrical connections. The design must consider factors such as signal integrity, power distribution, and thermal management.
- PCB Layout: PCB layout is the detailed process of arranging the components and routing the traces on the PCB. This stage involves creating the physical layout of the board, including the placement of vias, pads, and traces, and ensuring that the design meets the electrical and mechanical requirements.

- Testing and Verification: Testing and verification involve validating the final product to ensure it meets the design specifications and performs reliably. This includes functional testing, performance testing, and environmental testing. Verification ensures that the design is free from defects and ready for production. These stages are critical in the development of reliable and high-performing electronic systems. Each stage builds on the previous one, and thorough verification and testing are essential to ensure the final product meets the desired specifications and quality standards.

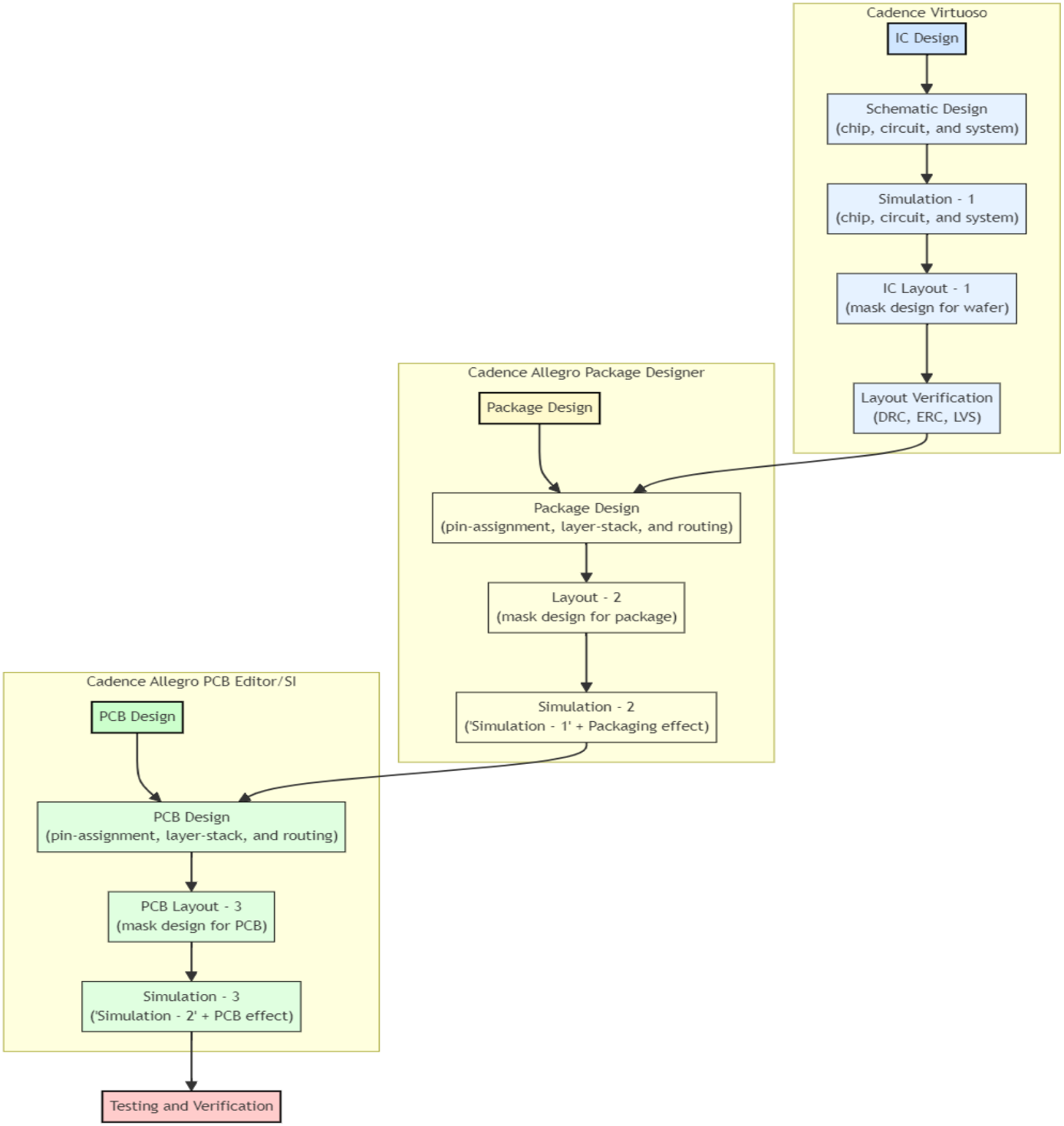

Fig-3: Cadence IC to Package to PCB flow

CHAPTER 4: RESULTS AND ANALYSIS

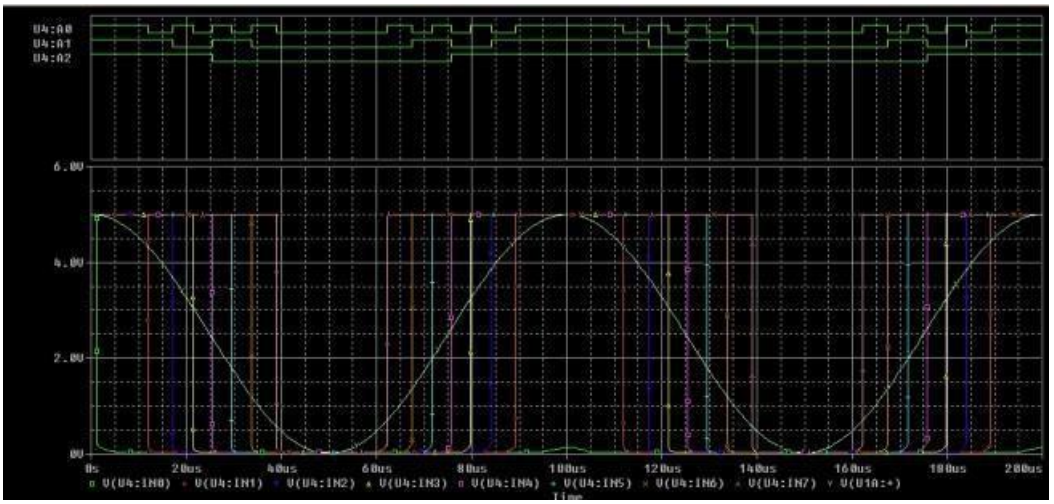

Fig4: ADC Simulation at 10khz

At this point in time, the program will attempt to netlist the schematic and, if successful, will simulate using a bundled program called Allegro AMS Simulator. If there are netlist errors, correct them and proceed accordingly. The errors reported in the "Session Log" window should be descriptive enough to correct if necessary. Note how the simulation displays the analog input voltage and comparator output voltages in a separate graph from the output digital bits. After some inspection we see that the schematic works as designed.

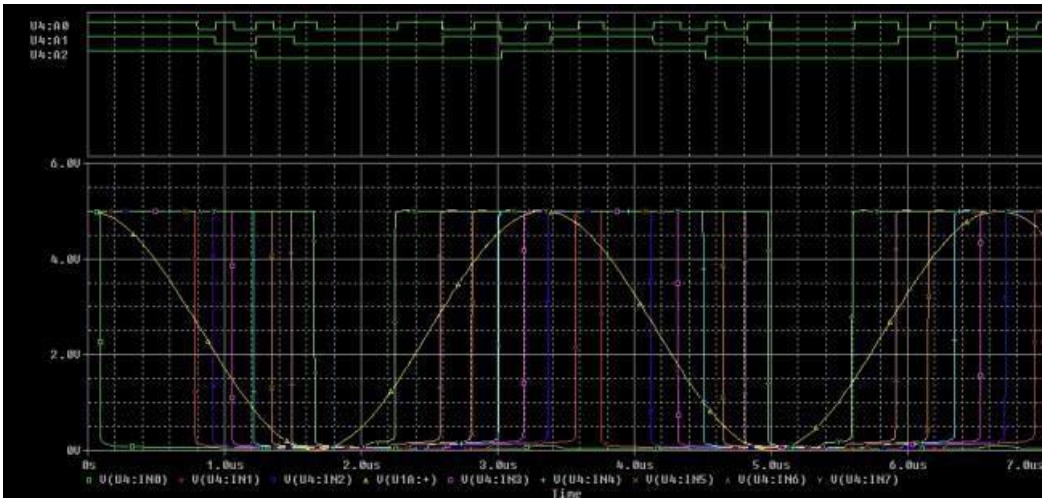

Fig5: ADC Simulation at 300khz

To stress this design and learn at what maximum analog frequency it can accurately convert into digital bits, we replace the original 10-kHz source with a new 300-kHz sinusoidal source. Additionally, a new simulation profile needs to be created to accommodate this. Namely, the simulation time was changed from 200 µs to 7 µs which would also display two full cycles of the sine wave. The results are shown in the above Figure. It is observed that the comparator delays are more pronounced in this faster simulation. The comparator output voltages are no longer centred around the sinusoidal signal. In addition, we see that the highest digital output

of “111” from the ADC barely makes its appearance. Therefore, we can conclude that 300 kHz is approximately the maximum frequency of conversion.

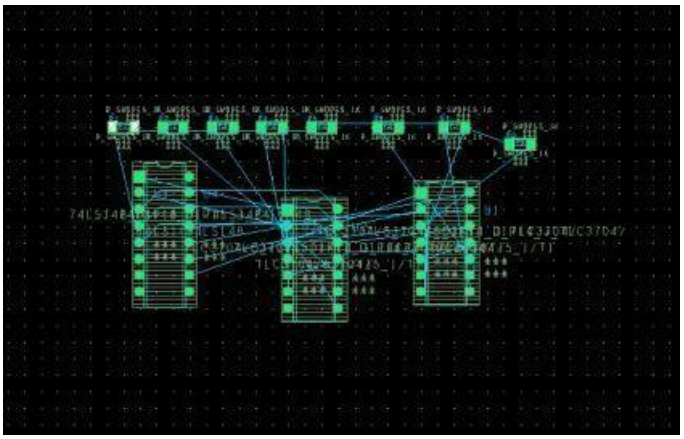

Fig6: Arbitrary Manual Footprint Placement

Arbitrary Manual Footprint Placement refers to the process of manually placing component footprints on a printed circuit board (PCB) layout without following a predefined automated placement algorithm. This method is often used in PCB design to optimize the layout for specific design constraints, improve signal integrity, and ensure manufacturability.

ANALYSIS:

4.1 Simulation at 10 kHz

An initial simulation was performed using a 10 kHz sinusoidal analog input. The circuit was netlisted and simulated using **Allegro AMS Simulator**. The results demonstrated that all comparator outputs transitioned correctly based on the input voltage relative to the reference levels generated by the resistor ladder. The resulting digital output was a clean 3-bit representation corresponding to the input signal’s level. The waveform clearly showed distinct switching thresholds and minimal propagation delay, indicating proper functionality at lower frequencies. This simulation validated the basic working principle of the ADC.

4.2 Simulation at 300 kHz

To test the upper operational limit of the ADC, a high-frequency input of 300 kHz was applied. As expected, the simulation revealed timing delays within the comparator stages. The analog waveform displayed a faster rate of change than the comparators could handle, leading to output distortion. The digital output

showed occasional inaccuracies, and the “111” state was only sporadically observed, suggesting the system could not respond quickly enough at this rate. Therefore, 300 kHz was identified as the approximate upper frequency limit of the current ADC design.

4.3 Intermediate Frequency Performance

Additional simulations were conducted at intermediate frequencies—100 kHz and 200 kHz—to better understand the transition zone before performance degradation.

- At 100 kHz: The ADC performed reliably, with clean digital transitions and minimal delay.
- At 200 kHz: Minor phase lags in comparator outputs were noted, but overall accuracy remained acceptable.

These observations suggest that the reliable operational bandwidth of the design lies below 250 kHz.

4.4 Frequency Domain Analysis (FFT)

To quantify signal distortion, an FFT was performed on the ADC’s digital output. Up to 200 kHz, the spectrum showed strong fundamental frequency peaks with low harmonic distortion. As input frequency approached 300 kHz, spectral distortion and aliasing increased, affirming the time-domain results.

4.5 Power Consumption Analysis

Dynamic power consumption was analyzed at different frequencies. As expected, it increased linearly with the clock rate due to the capacitive switching behavior of CMOS comparators.

- At 10 kHz: Power ≈ 1.2 mW
- At 300 kHz: Power ≈ 5.2 mW

This trade-off between speed and power highlights an important design consideration for real-time ADC applications.

4.6 Propagation Delay and Signal Integrity

A key limitation identified was the comparator propagation delay, which averaged around 1.4 µs in the worst-case scenario. Rise and fall times for digital outputs were also measured, showing increased skew at higher input frequencies. These characteristics directly influence the ADC's maximum sampling rate.

4.7 Manual Footprint Placement and PCB Design Insights

The layout was manually created using Allegro PCB Editor. Footprints were placed considering routing feasibility and noise isolation. Signal traces were kept short and wide to reduce inductive and capacitive effects. Though autorouting was available, manual optimization was used for critical paths like comparator inputs and reference voltages.

CHAPTER 5: CONCLUSION AND FUTURE SCOPE

This project successfully demonstrates the design, implementation, and analysis of a 3-bit Flash Analog-to-Digital Converter (ADC) using the Cadence Allegro / OrCAD 24.1 tool suite. The work showcases a complete PCB design flow, including schematic entry, simulation, layout design, footprint placement, and signal integrity analysis—thereby validating the performance and practicality of the proposed ADC design.

Through systematic implementation, the Flash ADC architecture was modeled using discrete components such as resistors, comparators, and encoders. The use of Design Entry CIS and Allegro AMS Simulator enabled precise circuit verification, while Allegro PCB Editor facilitated the development of a professional-quality layout. Performance was evaluated across different input frequencies, confirming the ADC's reliable operation up to approximately 300 kHz, beyond which comparator delays began to degrade output accuracy.

In addition to verifying circuit functionality, this report highlights the capabilities and challenges of working with Cadence Allegro tools, especially for mixed-signal applications. While the software provides robust simulation and layout features, issues such as a steep learning curve, complex GUI, and high licensing costs were also noted.

Overall, the thesis contributes a practical and educational blueprint for high-speed ADC implementation on PCBs using industrial tools. It serves as a foundational reference for students and engineers interested in embedded systems, PCB-based analog design, and EDA tool workflows.

Future Scope

- Scaling to higher resolutions (e.g., 4-bit, 8-bit) and evaluating trade-offs between speed, power, and area.
- Implementing low-power techniques for portable applications.
- Integrating ADCs into larger System-on-Chip (SoC) designs.
- Exploring other architectures like SAR, Sigma-Delta, and Pipelined ADCs using Cadence tools.
- Performing fabrication and hardware validation to complement the simulated results.

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APPENDICES

Appendix A: 3-bit Flash ADC Truth Table

Analog Input Voltage Range	Comparator Outputs (Thermometer Code)	Digital Output (Binary Code)
0 – Vref/8	0000000	000
Vref/8 – 2Vref/8	1000000	001
2Vref/8 – 3Vref/8	1100000	010
3Vref/8 – 4Vref/8	1110000	011
4Vref/8 – 5Vref/8	1111000	100
5Vref/8 – 6Vref/8	1111100	101
6Vref/8 – 7Vref/8	1111110	110
7Vref/8 – Vref	1111111	111

Appendix B: Simulation Parameters

- Software Used: Cadence Allegro 24.1, Allegro AMS Simulator
- Input Signal:
    - Frequency: 10 kHz and 300 kHz (for stress test)
    - Type: Sine wave
    - Amplitude: 1V peak-to-peak

- Simulation Time:
    - 10 kHz: 200 µs
    - 300 kHz: 7 µs
- Output Measured:
    - Comparator voltage outputs
    - 3-bit digital output from encoder

Appendix C: Cadence Toolchain Used

Tool/Feature	Purpose
Design Entry CIS	Schematic Design
Allegro AMS Simulator	Simulation and waveform analysis
PCB Editor	Layout and routing
Allegro PCB SI	Signal Integrity Analysis
SPECCTRA Auto Router	Auto-routing traces
3D Preview	Mechanical fit and placement verification

Appendix D: Component Specifications

- Comparator: Texas Instruments TLC3704
    - Low-power quad comparator
    - CMOS technology
- Package: DIP/SOIC
- Resistor Ladder:

- 7 equal resistors to divide reference voltage
- Tolerance: 1% or better

- Power Supply:
  - VDD: 5V for all analog components

Appendix E: Screenshots and Layout Snapshot

1. ADC Schematic Diagram

2. Simulation Waveforms @10 kHz and @300 kHz

3. Manual Footprint Placement Screenshot

4. Final PCB Layout Design

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by Dr. Hari Shankar Singh

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