ULTRA LOW POWER STANDARD CELLS LIBRARY DEVELOPMENT IN 90 nm TECHNOLOGY – OAI, CLKMUX, TLATCH, DFF, SDFF

A

THESIS

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Submitted by

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DECLARATION

I hereby declare that the work, which is being presented in the thesis, entitled **"Ultra Low Power Standard Cells Library Development in 90 nm Technology- OAI, CLKMUX, TLATCH, DFF, SDFF"** in partial fulfillment of the requirements for the award of degree of Master of Technology in VLSI Design & CAD at Electronics and Communication Engineering Department of Thapar University, Patiala, is an authentic record of my own work carried out under the guidance of Er. Smarti Kotwal.

This thesis work has been carried out in RF Silicon Pvt. Ltd., Noida, under the guidance of Mr. Rupesh Bartunia (Project Leader).

I have not submitted the matter presented in the thesis for the award of any other degree of this or any other university.

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ABSTRACT

Electronic products have long become an integral part of the modern lifestyle. Demand and supply of such products with smaller size, lower power consumption and better performance are ever increasing. Some of the driving factors include portability, mobility, accuracy and increased performance demands. This in turn impels the manufacturers to incorporate many methods such as decreasing the component sizes, making operations battery powered, choosing improved heat tolerant packaging materials and more. The field of electronics has made quite a leap and come a long way, starting with vacuum tubes, transistors, MOSFETS to the Integrated circuits. Today's electronic circuits carry thousands of systems all on a single chip.

The semiconductor industry grew from 3000 transistors in its nascent stages to about 50 million transistors in today's ICs. This doubling of the transistor count every 18 months manifested as decreased MOS dimensions. From 10um in the 1970's to the present day sizes of about 0.09um MOS dimensions have reduced from micron to sub-micron and now to nanometer technologies, being made possible by various techniques such as scaling of gate oxide thickness, source-drain extension(SDE) and newer process technologies. This technology migration has been relatively smooth until the sub-micron feature length for CMOS technologies. As we approach the rear end of deep sub micron technologies, the reliability of circuit performance has started facing serious challenges.

Creating an IC (Integrated Circuit) can be very time consuming if high flexibility of the construction is demanded. This thesis will try to solve this problem by creating own standard cell libraries, which in turn are more flexible since the user designs them. Having these libraries makes it possible to map VHDL or Verilog code to those libraries, using them instead of predefined cell libraries. The procedure of creating the libraries is quite time consuming, and thus the possibilities of making that procedure automatic, or as automatic as possible, has been examined.

This thesis reviews the forces that caused the power problem, the solutions that were applied, and what the solutions tell us about the problem. As systems became more power constrained, optimizing the power became more critical, viewing power reduction from an optimization perspective provides valuable insights.

Leakage due to scaling down CMOS device sizes will be the major power consumption source in cell based IC design in a few years. This work addresses the problem of this leakage, investigating the possibilities of utilizing alternative logic families instead of static CMOS for the creation of a low

leakage cell library. For this purpose, MTCMOS, CPL and Domino logic are investigated for leakage characteristics and are found unusable for low leakage design. Using cell libraries of small logic cells for IC design is found to be the major reason for much of the leakage.

In this thesis, a novel logic gate design with low leakage is proposed. Traditionally, the subthreshold leakage through a logic gate depends on the applied input vector. In order to reduce leakage power, we stack an extra transistor in the large leakage path and applying substrate biasing technique. The proposed structure induces low leakage current under all possible inputs. Compared to the conventional CMOS logic circuit design, the simulation results show that the proposed logic circuits not only reduce significant leakage power dissipation, but also keep similar circuit performance as conventional CMOS logic circuits.

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ABBREVIATIONS AND SYMBOLS

ASIC	Application Specific Integrated Circuit
CAD	Computer Aided Design
NMOS	N Type MOS Transistor
PMOS	P Type MOS Transistor
CMOS	Complementary Metal Oxide Semiconductor
V_{th}	Threshold voltage
LEF	Library Exchange Format
VTCMOS	Variable threshold CMOS
I_{SUB}	Sub-Threshold Leakage Current
DIBL	Drain-induced barrier-lowering
I_G	Gate Leakage Current
GIDL	Gate induced drain leakage
BTBT	Band-to-band tunneling
DRV	Data retention voltage
VRC	Virtual rail clamp
DFF	D-flip-flop
VDD	Supply voltage
VSS	Ground power
DSMT	Deep Sub-Micron technology
V_{gs}	Gate to source voltage

CHAPTER-1
INTRODUCTION

1.1 Background

IC development is nowadays a huge industry. There is an almost infinite amount of consumer products like mobile phones, processors, televisions, cameras, refrigerators, ovens and cars that in one way or another uses custom IC components. Integrated circuits can provide anything from analog-to-digital conversion to digital filtering and much more. A digital integrated circuit can be manufactured with a number of different approaches, but they all contain the same basic steps. It all starts with transistors, wiring and all the things that make up the circuit being placed in a layout, designed in a CAD (Computer Aided Design) tool and ends up with that layout being physically created on a chip. The way to create this layout differs depending on design requirements.

There are three basic ways to go about:

1.1.1 Full Custom

Full custom design is when everything in the layout is created manually. Every single transistor used can be set up as desired, optimized for speed, area or capacitive load etc. Every single wire in the layout is placed manually and the designer has total control over the layout. This is done when the design has very strict requirements and needs to be optimized in one way or another. The obvious advantage is that the layout can be created very carefully to fit the need. On the other hand, this requires a lot of work and time.

1.1.2 Semi Custom

Semi custom design is when the designer works on a logical gate level. This means that the designer can use gates like NAND, Inverters, Buffers, Flip-Flops etc. that have already been created and distributed as a cell library by a supplier. The idea is to reuse blocks of logic instead of creating them manually over and over again. Instead of placing every transistor and wire, the designer places logic blocks in the layout that corresponds to the desired function. The good thing with semi custom layout is that the required time is decreased and it is far less advanced compared to full custom layout. The downside is that the possibility to optimize the given gates is very limited, so the designer loses some control of the layout **[1]**. A combination of full and semi custom layout can often be a good approach, where the logical gates are created manually and optimized and then used in a semi custom layout instead of using gates created by a supplier.

1.1.3. Automatic Design

Automatic design is similar to semi custom design in that it uses pre-created standard cell libraries. The difference is that in the automatic design approach, the layout is created automatically. The work of the designer in this case, is to describe the design in a high level programming language like VHDL or Verilog. The high level description is then fed to the automatic design tools which create a layout that corresponds to the description. This is the fastest way to create a layout of a circuit, unless it's a very trivial one, like basic logical gates such as an Inverter or a NAND gate. The automatic design approach is also the one where the designer has least control of the layout. Although the design tools can be told to optimize the generated layout in certain ways, there is just no way for the designer to control exactly how it is generated. Automatic design therefore suffers from creating less optimized layouts compared to full custom design and even semi custom design. How ever, automatic design is a very useful tool when the design to be created does not have very strict requirements and when the time to market is more important than a fully optimized design. As mentioned, the automatic design process uses standard cell libraries created by some supplier, generally the one that has supplied the technology that is being used (90nm, 65nm, 45nm and so on). While these standard cell libraries are quite flexible they may not fit the requirements. A solution to this would be to create a standard cell library manually and use that in the automatic design. This would give the designer total control of the cells in the library and still make it possible to use automatic design tools when creating layouts, thus allowing both the optimization of the design building blocks and rapid layout creation.

1.2 The problem of leakage currents

Leaking devices will soon be the major concern of the IC design industry. As device sizes have been scaled down to keep up the exponential growth of device density and to enable lower supply voltages, reducing the dynamic power dissipation, MOSFET transistors are beginning to conduct current when they are in off mode. MOS transistors have always conducted a bit of current in their off mode, but until recent years the problem has not been big enough to get worried about. When the industry embraces the new sub-90nm technologies though, these currents will be the reason for almost half of the total power dissipation in an integrated circuit **[2].**

Lowering power consumption is critical for further improvements for operational speed in high-speed applications and for low-power consumption in battery-supplied applications such as cellular phones. Reducing the unwanted currents, called leakage currents or simply leakage, is vital for further growth in IC designs. Leakage has two components: Subthreshold leakage and gate-oxide leakage.

Subthreshold old leakage consists of source-drain currents when the transistor is supposed to be non-conducting. These currents are now flowing through the substrate of the transistors due to effects near the active regions of transistors that heavily depend on the length of the transistor gate. Gate-oxide leakage comes from currents tunneling through the very thin oxide layer between gate and source, drain or bulk. Clearly, both types of leakage depend on the device sizes, and also depend on the voltages at the terminals. Further, altering the doping of the substrate, the threshold voltage, V_{th}, can be changed enabling the design of low leakage transistors with higher V_{th} values. Though, high V_{th} have weaker drive and will deteriorate the speed of the circuitry.

1.3 Structure for creating a standard cell library

There are five major steps in creating and testing a standard cell library, and each of them is discussed thoroughly in their respective section. **[3]** Problems and solutions are also presented as well as a complete guideline on how to create a standard cell library and use that library in an automatic design process. The five major parts are:

1) Create a correct schematic and layout
2) Create abstract and LEF file (Library Exchange Format, used to describe the cells in a standard cell Library).
3) Create a TLF file (Timing Library Format, used to characterize the cells in a standard cell library)
4) Synthesis
5) Place and Route

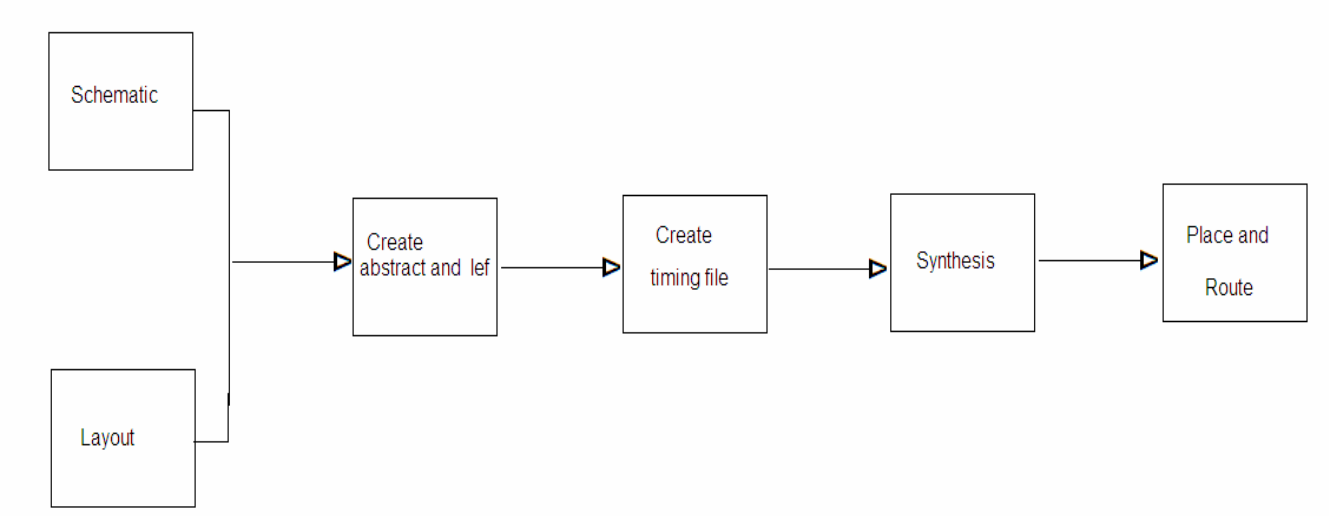


Figure 1.1 Overview flow chart for standard cell library

1.4 Objective

The purpose of this master thesis is to examine the possibility of making a standard cell library with low consumption, from which any given design can be created in an automatic design process. The main purpose is to manage to create a standard cell library manually and to integrate that library into a commercial tool for automatic design. This thesis will also discuss the possibility of creating the standard cell library itself automatically, hence delivering a solution that will be able to both optimize a design and have it created totally automatically.

This thesis is limited to describing the creation of a Ultra Low Power Standard Cell Library consisting of a many standard cells. This master thesis will only cover standard cell library construction using 90 nm technology. Many techniques for reducing leakage power are explained in this thesis but applying substrate biasing (VTMOS) and stacking technique with high V_{th} MOS cell. It is however possible to change the technology with only changes in the procedure minor. All the examples of locations of files, sizes etc. are with regard to the 90 nm technology supplied in the Cadence tool. This thesis also contains the layout of standard cell in 90 nm technology with Virtuoso (Cadence) tool.

1.5 Thesis Organization

Chapter 2 presents various power dissipation mechanisms in CMOS digital circuits. The increased subthreshold leakage, caused by technology scaling, is then discussed. For each subthreshold leakage reduction approach, the advantages and disadvantages are analyzed. This chapter provides different leakage reduction techniques for low power standard cell library. The required cells for standard cell are introduced in detail in the first Part of Chapter 3. Second part of the chapter contains layout guide lines for standard cells. Chapter 4 presents cells description in standard cell library for low power cell designing.

Chapter 5 shows results in terms of speed, leakage current with body bias and without body bias (using VTCMOS technique) and dynamic current with waveforms.

CHAPTER-2
LEAKAGE POWER AND SOURCES

Unlike bipolar technologies, where a majority of power dissipation is static, the bulk of power dissipation in properly-designed CMOS circuits is the dynamic charging and discharging of capacitances. Thus, a majority of the low power design methodology is dedicated to reducing this predominant factor of power dissipation. However, there are also other components of power dissipation in CMOS circuits as described in the following section. Most of them are negligible, but one component that can become significant in poorly-designed circuits is power dissipated by short-circuit currents. The magnitude of this component is determined by the design methodology used.

2.1 Sources of Power Dissipation

There are three main source of power dissipation:

1. Dynamic switching power due to the charging and discharging circuit capacitances.
2. Short-circuit current power due to finite signal rise/fall times.
3. Leakage current power from reverse-biased diodes and subthreshold conduction.

2.1.1 Dynamic Switching Power

When CMOS circuits switch, the output is either charged up to V, or discharged down to ground. In static logic design, the output only transitions on an input transition, while in dynamic logic, the output is precharged during half the clock cycle, and transitions can only occur in the second clock phase, depending upon the input values. **[4]** In both cases, the power dissipated during switching is proportional to the capacitive load; however, they have different transition frequencies.

For the simple inverter gate shown in Figure 2.1, it can be shown that a low-to-high output transition draws CV Joules (energy) from the power supply (V). The high-to-low output transition dissipates the energy stored on the capacitor into the NMOS device. Given a frequency *f* of low-to-high output transitions, the power drawn from the supply is CV *f*. This simple equation holds for more complex gates and other logic styles as well, given a periodic input. Since dynamic switching power is the major component of overall power dissipation, the low-power design methodology concentrates on minimizing total capacitance, supply

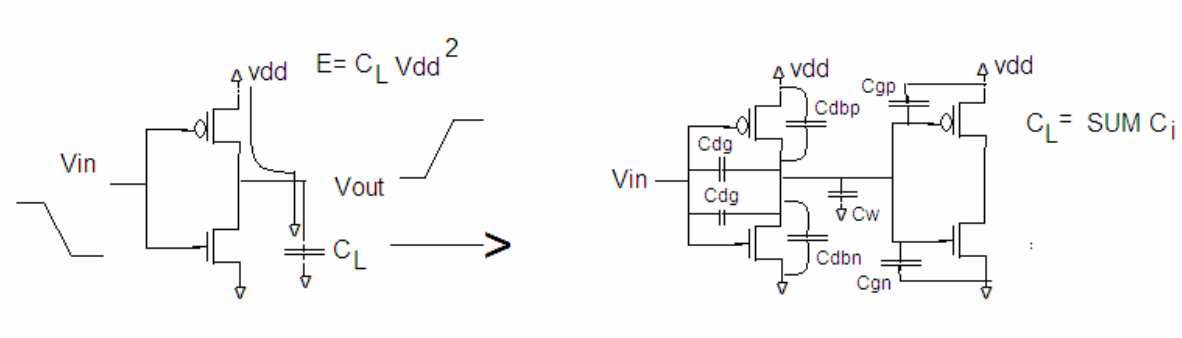


Figure 2.1 Dynamic switching power dissipation; Source of capacitance

voltage, and frequency of transitions.

2.1.2 Short-Circuit Current Power

Short circuit currents occur when the rise/fall time at the input of a gate is larger than the output rise/fall time. For the ideal case of a step input, the transistors change state immediately one turning on, one turning off. There is not a conductive path from the supply to ground. For real circuits, however, the input signal will have some finite rise/fall time. While the condition $V_{th} < V_{gs} < V_{gs} - |V_{th}|$ holds for the input voltage, there will be a conductive path open because both devices are on. The longer the input rise/fall time, the longer the short-circuit current will continue to flow and the average short-circuit current increases. Figure 2.2 plots the ratio of energy consumed by short-circuits current versus the ratio of input rise/fall time to output rise/fall time. The E increases dramatically with increasing input rise/fall time. To minimize the total average short-circuit current power, it is desirable to have equal input and output edge times**. [5]**

For most ICs, the short-circuit power dissipated is approximately 5-10% of the total dynamic power. If the supply is lowered to below the sum of the thresholds of the transistors, $Vdd < V_{tn} + |V_{tp}|$, however, short-circuit currents will be eliminated because both devices cannot be on at the same time for all values of input voltage.

2.1.3 Leakage Current Power

This section briefly describes each type of leakage current.

2.1.3.1 p-n Junction Reverse Bias Current

When building structures with layers of doped silicon and electrically charging them, currents will unavoidably leak through the silicon. From drain and source regions a reverse bias p-n junction leakage current flows into the well region (Figure 2.3, I_1).

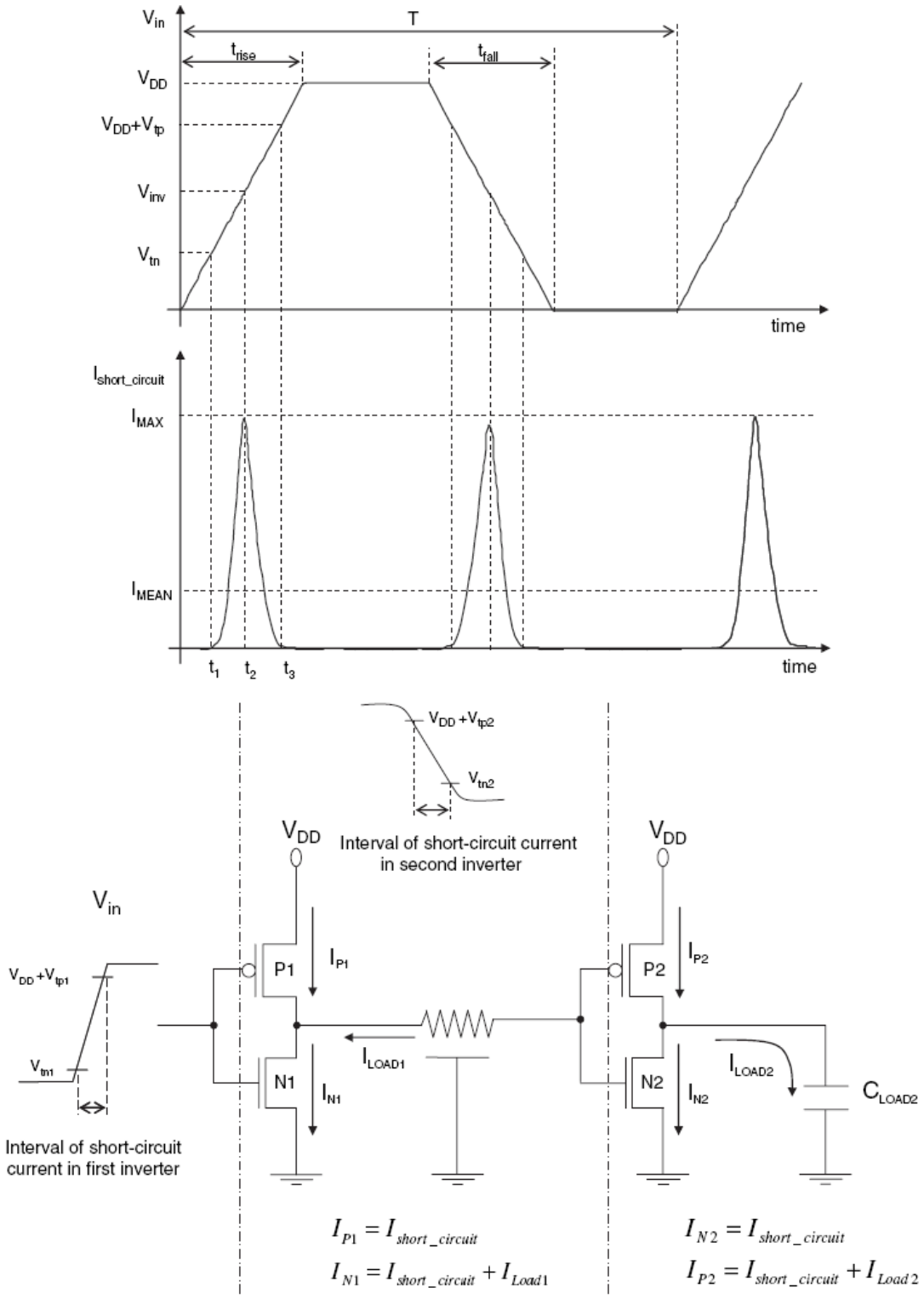


Figure 2.2 Short Circuit Power Dissipation **[5]**

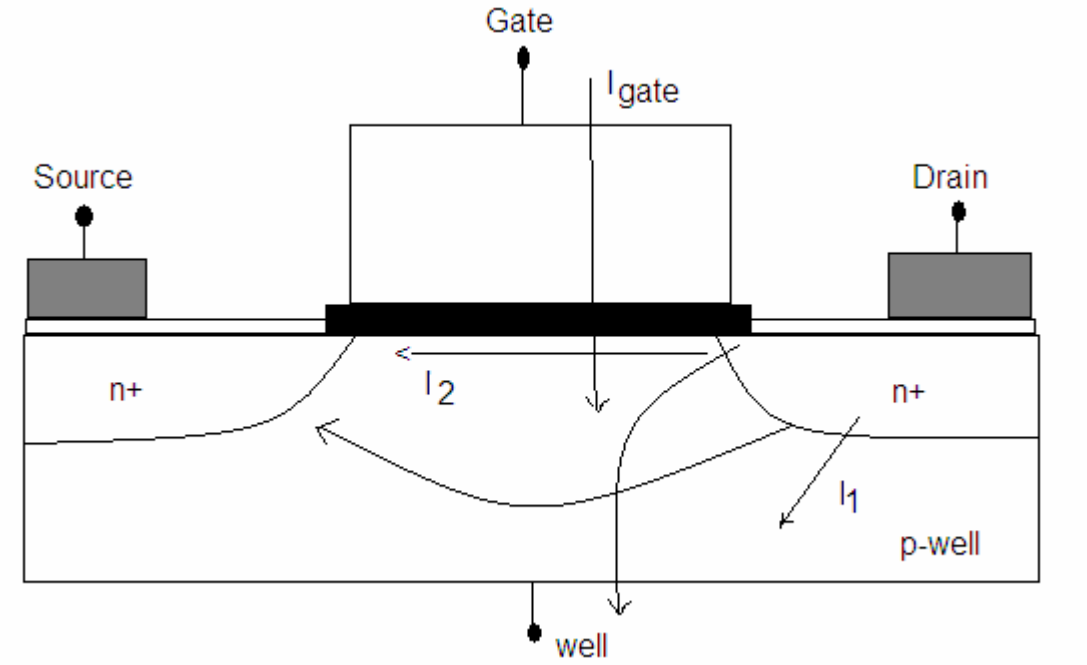


Figure 2.3 Leakage Current

This current has two main components: Firstly, the minority carrier drift near the edge of the depletion region and secondly the electron-hole pair generation in the depletion region. Both components are heavily dependent on the doping level of the source and drain regions. When heavily doped drain/source regions together with short-channel-effect enhancements, such as halo-doping are used, p-n junction reverse bias currents increase significantly **[6]**.

2.1.3.2 Sub-Threshold Leakage Current (I_{SUB})

Sub-threshold current is the most dominant among all sources of leakages. It is caused by minority carriers drifting across the channel from drain to source due to presence of weak inversion layer when the transistor is operating in cut-off region ($V_{GS} < V_{th}$). (Figure 2.3, I_2). The minority carrier concentration rises exponentially with gate voltage V_G and so the plot of log (I_{SUB}) versus V_G is a linear curve with typical slopes of 60-80mV per decade. I_{SUB} depends on the substrate doping concentration and halo implant, which modifies the threshold voltage V_{th}. I_{SUB} also rises exponentially with temperature.

$$I_{SUB} = I_0\left(1-\exp\left(\frac{-qV_{DS}}{kT}\right)\right)\exp\left(q\frac{V_{GS}-V_{th}-V_{OFF}}{nkT}\right) \qquad ..2.1$$

Where, V_{OFF} is the offset voltage in sub-threshold region and Io is given as:

$$I_0 = \mu \frac{W_{eff}}{L_{eff}} \left(\frac{kT}{q} \right)^2 \sqrt{\frac{q\varepsilon_{Si} NDEP}{2\phi_S}} \qquad ..2.2$$

Condition for I_{SUB} to occur in an NMOS transistor is shown below.

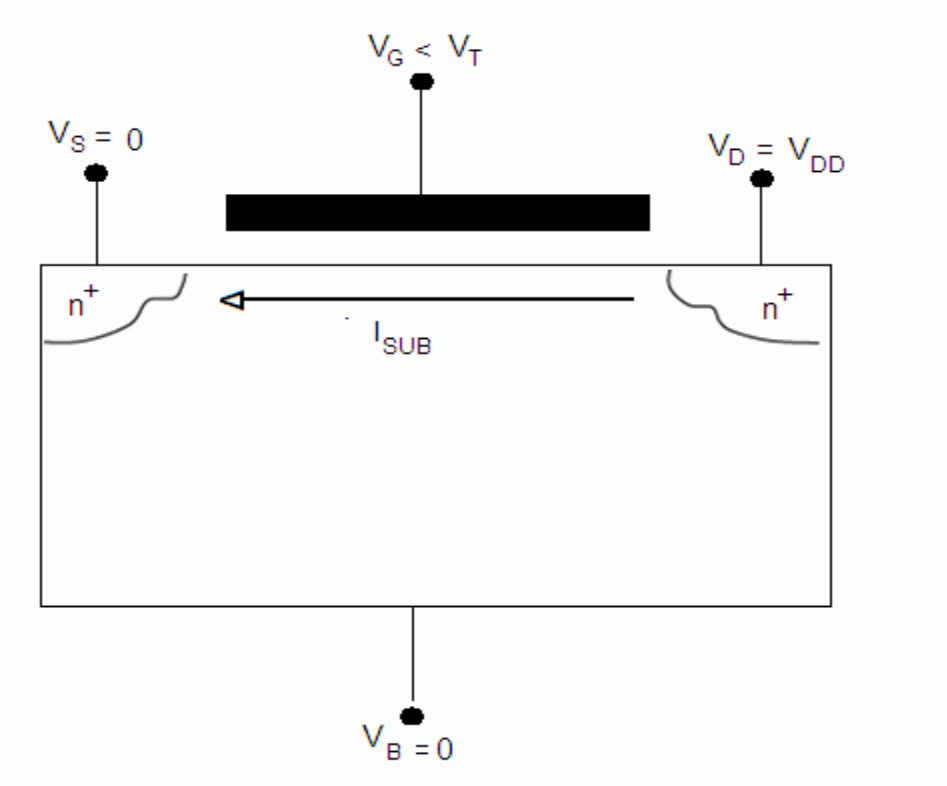


Figure 2.4 Subthreshold Leakage Current

2.1.3.2.1 Illustration of sub-threshold leakage in a NMOS

As the length of the channel is scaled, the capability of the gate to control the charge and potential distribution in the channel area degrades. The threshold voltage of a MOSFET is reduced with decreasing channel length. The effects of scaling the channel length on the threshold voltage and subthreshold leakage current characteristics of a MOSFET are called short-channel effects. While the gate loses some control of the channel region, the effect of the drain on the voltage potential distribution across the channel area increases with scaling of the gate length. The effect of the bias conditions of the drain on the threshold voltage and subthreshold leakage current characteristics of a MOSFET is called drain-induced barrier-

lowering (DIBL). The various parameters that characterize subthreshold leakage current in a deep submicrometer IC.

The subthreshold leakage current increases with temperature. Figure 2.5 shows the leakage current for several technologies for different temperatures. As I_{SUB} grows in each generation. Furthermore, in a given technology, the leakage current increases with the temperature. I_{SUB} has a temperature sensitivity of 8-12 x/100^{o}C **[7].**

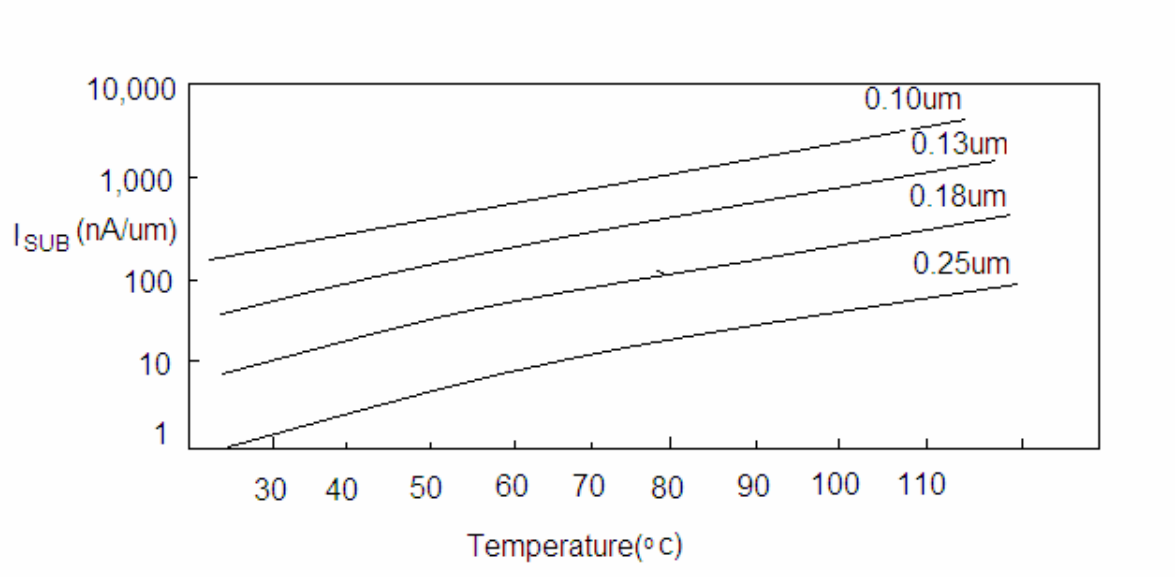


Figure 2.5 Subthreshold Current v/s Temperature

2.1.3.3 Drain-Induced Barrier Lowering

In long devices the drain and source regions are far enough apart for the electrical field and depletion regions induced into the device by these regions to have any impact in the threshold voltage. Hence the threshold voltage is almost independent of the channel length and drain bias. In a short-channel device, on the other hand, source and drain depletion width and source-drain potential have great effect on the energy band bending over a considerable portion of the device. Threshold voltage and thereby subthreshold currents of short-channel devices vary with the drain bias. This effect is called drain-induced barrier lowering (DIBL). and two short devices (B and C), charged by relative low drain-source voltage except (C) which is driven by higher voltage. The threshold voltage equals the maximum energy level a charge carrier has to achieve to move between the source and drain terminals. It is evident that decreasing channel lengths reduces the threshold voltage. Increasing drain voltage causes

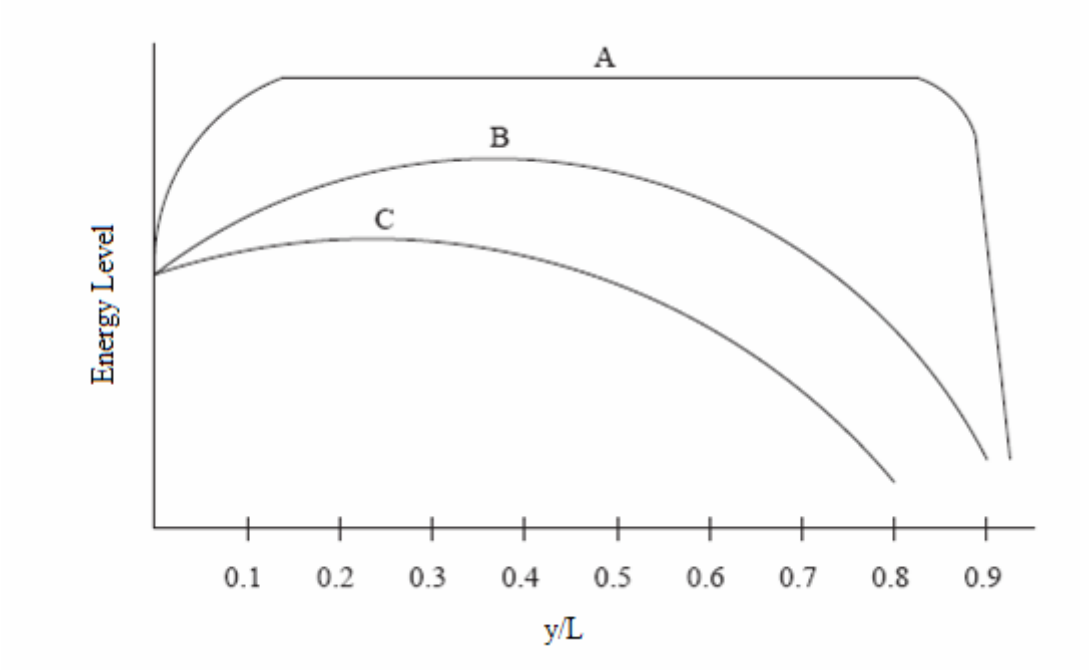


Figure 2.6 Depicts three different energy bands near the surface of a long device (A)

further Vth lowering in the short-channel device, but does not affect the long-channel device. This is due to the flatness of the curve in the middle (or the high slopes near drain and source), which originates from the extension of the non-affected area under the gate. Ideally DIBL does not change the slope, but it reduces V_{th}. Higher surface and channel doping can reduce the DIBL effect. DIBL certainly has to be taken into account when designing new technologies as supply voltage lowering not only slows the circuits down but counters the DIBL-effect and raises the threshold voltage which further slows circuits down. This is especially important when considering multi- V_{th} -designs. The effects of DIBL are shown on Figure 2.7.

2.1.3.4 Gate Leakage Current (I_G)

Gate leakage is a serious concern at gate oxide thicknesses below 2nm. With such thin gate oxide, fairly small potential difference across the gate oxide can induce high electric field, causing electrons to easily tunnel through the oxide. This process is called Fowler-Nordheim Tunneling. Gate leakage consists of three components: gate-to-channel (I_{GC}), gate-to-bulk (I_{GB}) and gate-to-source/drain diffusion (I_{GS} / I_{GD}) leakage **[8]**.

$$I_G = I_{GC} + I_{GB} + I_{GS} + I_{GD}$$

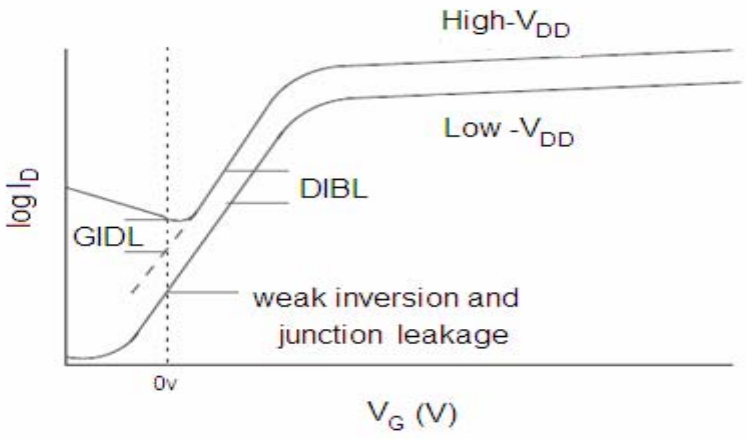


Figure 2.7 Effect of DIBL

2.1.3.5 Gate-Induced Drain Leakage

The gate induced drain leakage (GIDL) is caused by high field effect in the drain junction of MOS transistors. For an NMOS transistor with grounded gate and drain potential at VDD, significant band bending in the drain allows electron-hole pair generation through avalanche multiplication and band-to-band tunneling. A deep depletion condition is created since the holes are rapidly swept out to the substrate. At the same time, electrons are increased (Figure 2.9), while the channel doping is low. This is done mainly to control punch-through and drain-induced barrier lowering while having a low impact on the carrier mobility in the channel. The resulting steep doping profile at the drain edge increases band to band tunneling currents there, particularly as VDB is increased. Thinner oxide and higher supply voltage increase GIDL current. GIDL occurs from drain to body when D=1, G=0, S=X, B=0.

2.1.3.6 Hot-Carrier Injection

It occurs in short-channel transistors. Because of a strong electric field near the silicon, silicon oxide interface, electrons or holes can gain enough energy to cross the interface and enter the oxide layer. Injection of electrons is more likely to occur, since they have a lower effective mass and barrier height than holes **[9, 10]**.

2.1.3.7 Punch-Through Leakage

It occurs when there is decreased separation between depletion regions at the drain substrate and the source-substrate junctions. This occurs in short-channel devices, where this

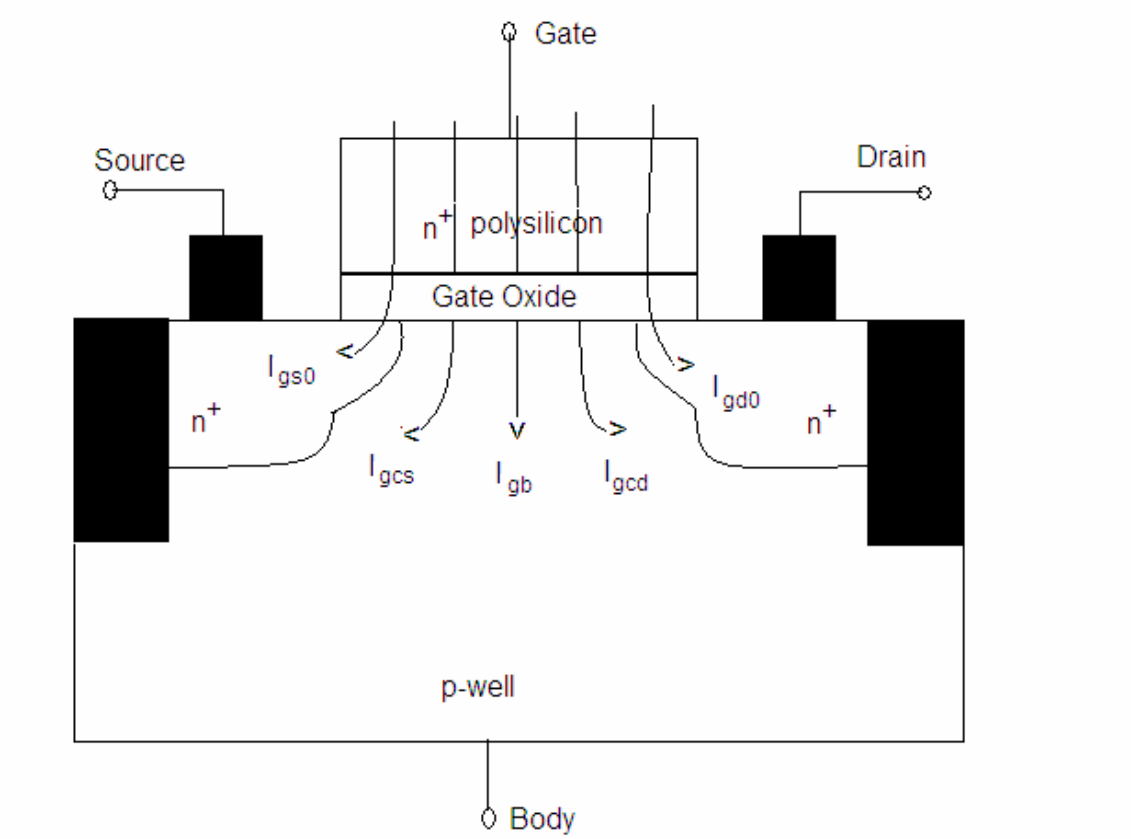


Figure 2.8 Components of Gate Current

separation is relatively small. Increased reverse bias across the junctions further decreases the separation. When the depletion regions merge, majority carriers in the source enter into the substrate and get collected by the drain, and punch-through takes place.

2.2 Leakage Power Model and Analysis for Nanometer CMOS circuits

In off-state, the main components of leakage current are subthreshold leakage (I_{Sub}), gate induced drain leakage (IGIDL), gate tunneling leakage (I_{GATE}), and band-to-band tunneling (I_{BTBT}) as shown in Figure 2.10(a). In on-state, gate tunneling leakage (I_{GATE}) is the major component as shown in Figure 2.10(b). The GIDL (Gate Induced Drain Leakage) is a current from drain to substrate caused by high electric field between gate and drain, and thin gate oxide thickness and high supply voltage increase the GIDL leakage. The gate tunneling

leakage is a current flowing into the gate of the transistor by tunneling effect, and thin gate oxide thickness and high supply voltage increase the gate tunneling leakage. The subthreshold leakage is a weak inversion conduction current of the CMOS transistor.

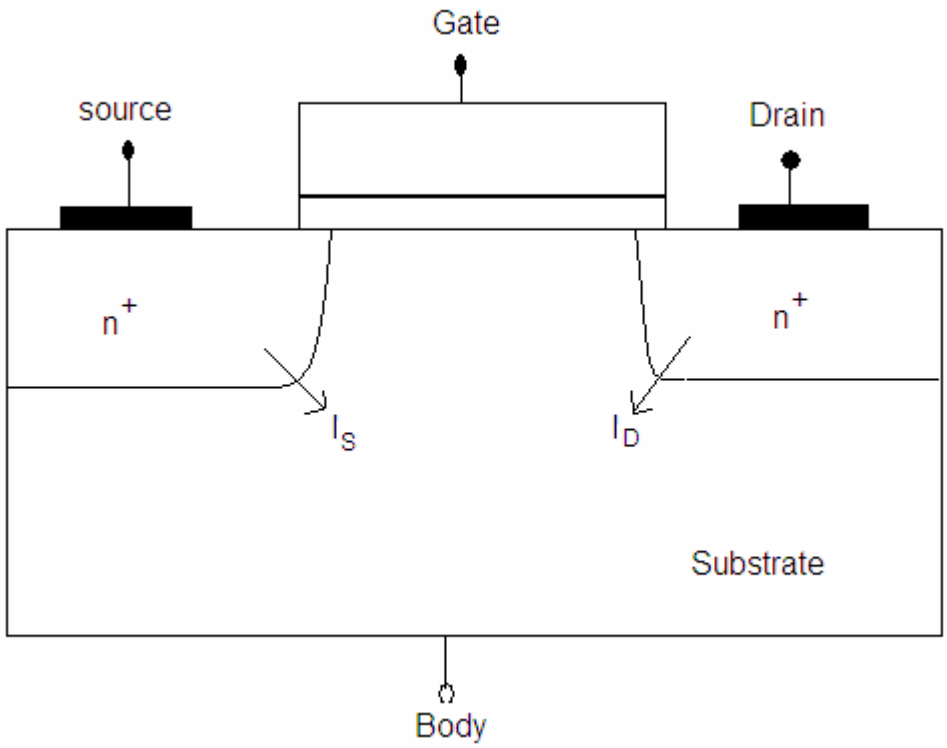


Figure 2.9 Gate Induced Drain Leakage

It increases exponentially due to reduced threshold voltage, and it is a main leakage component in high forward body bias. Finally, the BTBT leakage is a current by electron tunneling across the reverse biased p-n junction between drain/source and substrate of the CMOS transistor. Therefore, in high reverse body bias, the BTBT leakage becomes a major portion to the total leakage currents **[10]**. The subthreshold leakage current and the BTBT leakage are much more sensitive to the applied body bias than other two leakage components. The minimum leakage current is obtained when the subthreshold leakage current is equal to the BTBT leakage.

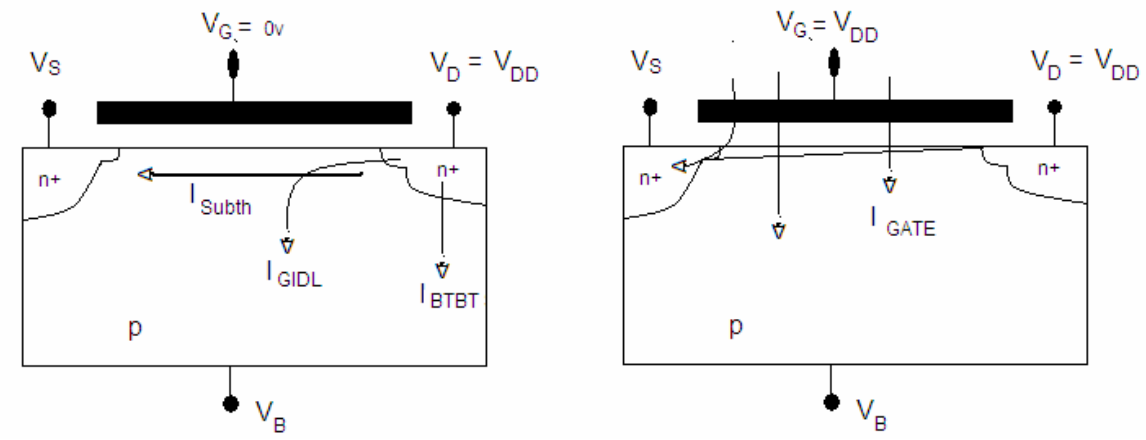
2.3 Leakage Reduction Techniques

2.3.1 Raising the Threshold Voltage

The three basic techniques to raise the threshold voltage are source biasing, body effect and changing the process. In most cases, raising the threshold voltage reduces the subthreshold leakage, but also significantly degrades the performance of the circuit in active mode. Usually, some localized performance loss is acceptable, since most circuit paths are not critical and additional logic delay on these paths will not change the overall performance.

2.3.1.1 Source Biasing and Stack Effect

Source biasing is the general term for several techniques that changes the voltage at the source of a transistor. The goal is to reduce V_{GS}, which has the effect of exponentially



(a) (b)

Figure 2.10 Leakage Current in Nanoscale CMOS Circuits (a) Off-State Leakage Components (b) On-State Leakage Components.

reducing the subthreshold current. Another result of raising the source is that it also reduces V_{BS} , resulting in a slightly higher threshold voltage due to the body effect. Circuits that directly manipulate the source voltage are rare, and those that exist usually use switched source impedance or a self-reversed biasing technique. Probably the simplest example of source biasing occurs when "off" transistors are stacked in series. Conceptually, the source voltage of the upper transistor will be a little higher than the source voltage of the lower transistor. Since the gates are driven identically, the upper transistor has a significantly lower current, as shown in Figure 2.11. **[11, 12]**

This reduction in leakage is commonly known as the stack effect. Clearly, it is advantageous

from a leakage perspective, but the trade-off is a significant degradation in performance. Figure 2.11 shows the effect of simply replacing each device in an inverter with two in series. In the case where the input capacitance is the same, i.e. each transistor in the stack has half the width of the baseline device. The reason is the significantly decreased drive current resulting from quadrupling the equivalent resistance.

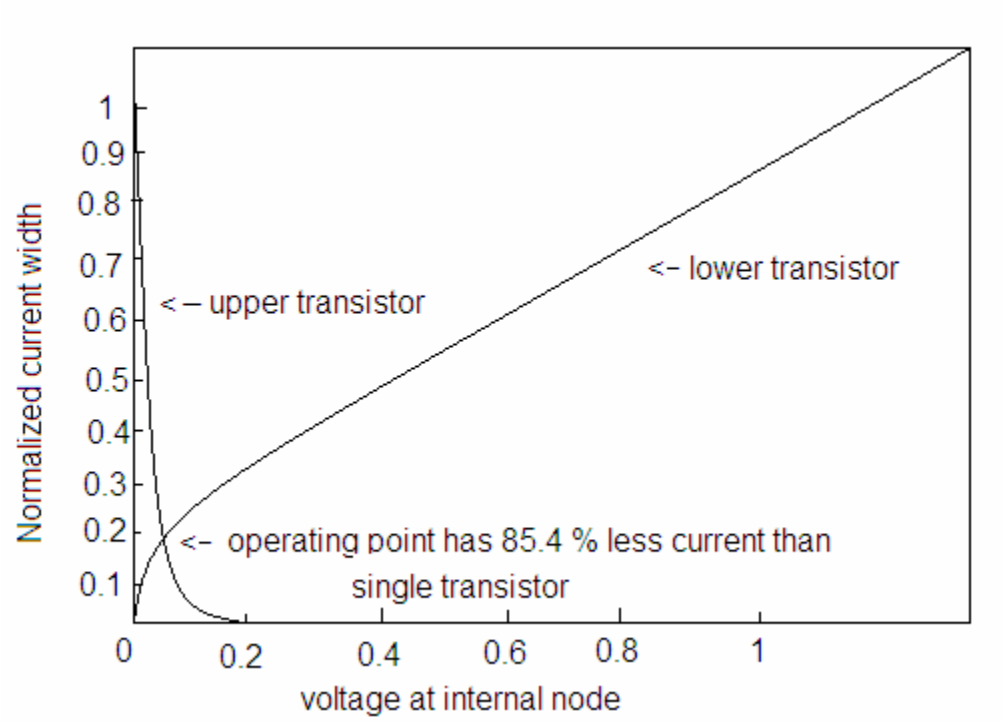


Figure 2.11 Load lines for upper and lower transistors illustrate the stack effect in 90nm Process **[11]**.

Increasing the width of the stacked devices does not significantly improve the performance because the input capacitance (and thus load capacitance) also increases. Further increasing the device size results in a larger leakage current that begins to exceed the baseline inverter. Since the leakage reduction comes at the expense of delay, one potential use of stacked devices is where delay is actually desired. It is not uncommon for designs to have a large number of minimum delay path violations, stemming from short logic paths like a scan path that directly chains registers together. The traditional approach is to add delay elements (typically inverters) to these paths, which results in large rise in leakage. Usage of "stack effect" inverters means that fewer gates are required for the same delay target, and each gate leaks less than an ordinary inverter. A second implicit use of the stack effect comes from the selection of more complex gates during technology mapping. In this way,

stacks are formed more naturally. The performance penalty still exists, but its effect is mitigated by the reduction in the number of gates required to implement the desired logic function. A third potential use is to exploit the natural stacks in logic gates by forcing a known input pattern during sleep mode. For example, a typical two-input NAND gate has a pull-down network with two NMOS transistors in series.

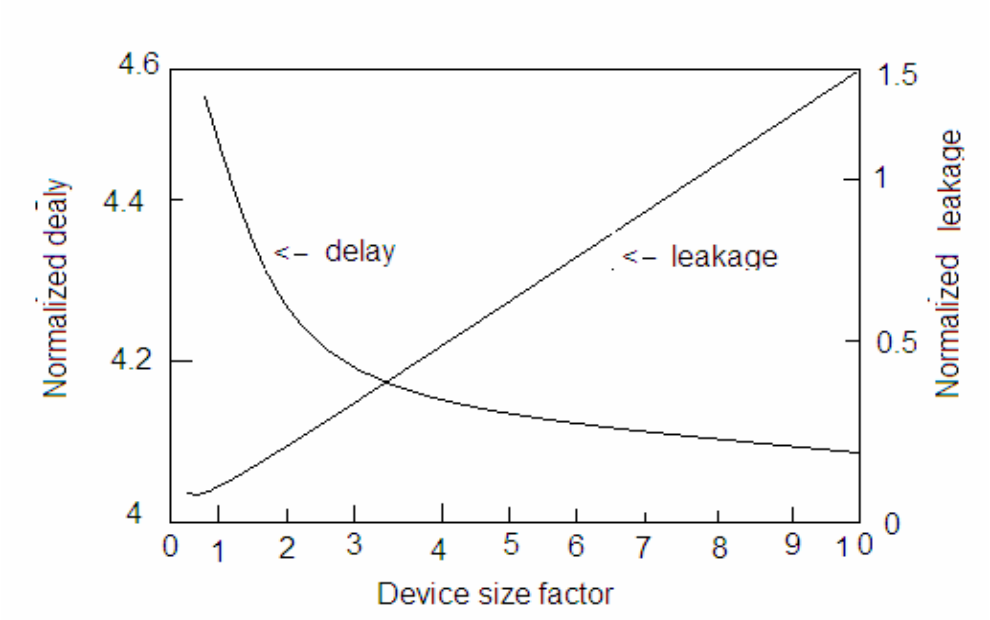


Figure 2.12 Simply stacking two identical NMOS transistors in an inverter significantly degrades the performance in 90nm process**[11]**.

When the inputs are both low, both these transistors are "off" minimizing the leakage. In all other configurations, the leakage current is higher.

2.3.1.2 Body Effect (VTCMOS)

The source biasing techniques described above decrease leakage by simultaneously reducing V_{GS} and V_{BS}, but another class of techniques focuses specifically on the term V_{BS}. The primary method is to manipulate the body voltage to modulate the threshold voltage. Since subthreshold leakage is inversely dependent upon the threshold voltage, increasing the threshold reduces the power consumption. However, the gate performance degrades with increasing V_t, so techniques that statically increase the body voltage are undesirable. Instead, by dynamically controlling the body voltage, the circuit can be tuned to the best trade-off

between power consumption and performance at any given time. This technique is typically called Variable Threshold CMOS (VTCMOS) **[13, 14].**

Although not always specifically called VTCMOS, schemes that modify the body bias to affect the threshold voltage have been proposed for older process generations. The self-adjusting threshold-voltage scheme (SATS) bounds the leakage regardless of the process corner and temperature using a sense stage that dynamically tunes the body voltage to the set the minimum Vt to meet the performance requirements. The intention is to switch between an active and a sleep mode. The VTCMOS approach depends on the ability to dynamically change the threshold voltage. For long-channel devices, the threshold voltage is calculated according to Eq. (2.3):

$$V_{t(long)} = V_{FB} + 2\left|\phi_p\right| + \frac{1}{C_{ox}}\sqrt{2\varepsilon_S qN_a\left(2\left|\Phi p\right| + V_{SB}\right)} \qquad ..2.3$$

In this formulation, V_{FB} is the gate voltage required to bring the silicon to a charge-neutral condition, Cox is the capacitance of the gate oxide, 2|φp | is the Fermi potential required to cause inversion in the channel, $\varepsilon_s q$ is a constant, Na is the dopant density, and V_{SB} is the potential between the source and the body. For ready-use, this formulation is usually transformed into the "body-effect" equation, Eq. (2.6), by separating it into two terms: the threshold voltage when $V_{SB} = 0$ (called V_{t0}) and the body-effect term (called ΔV_t):

$$V_{t0} = V_{FB} + 2\left|\Phi p\right| + \gamma\sqrt{2\left|\Phi p\right|} \qquad ..2.4$$

$$\Delta V_t = \gamma\left(\sqrt{\left|2\Phi p\right| + V_{SB}} - \sqrt{2\left|\Phi p\right|}\right) \qquad ..2.5$$

Equation (2.6) makes it seem that the threshold voltage can be raised to any value by just increasing $V_{BS.}$

$$\Delta V_{t(long)} = V_{t0} + \Delta V_t = V_{t0} + \gamma\left(\sqrt{\left|2\Phi p\right| + V_{SB}} - \sqrt{2\left|\Phi p\right|}\right) \qquad ..2.6$$

The parameter γ is called the body-effect coefficient and is defined as

$$\gamma = \frac{1}{C_{ox}}\sqrt{2\varepsilon_S qN_a} \qquad ..2.7$$

In reality this is not true, because this equation assumes a one dimensional model of the transistor that does not account for the depth of the channel. **[15]**For shorter channel lengths

and higher V_{BS} values, the depletion regions grow large enough that the channel appears to have a different length at the top and bottom.

The three primary complications with VTCMOS are that it must be dynamically controlled, the different body voltages must be generated, and they must be distributed throughout the chip. For designs that have a single set of body voltages to distribute throughout the entire logic, the additional wiring complexity is minor and can be handled similarly to the power rails. However, distribution can become significant if different sections of the logic must be controlled with different body voltages. In both cases, the appropriate bias voltage must be generated. The approach uses a self-substrate bias circuit (SSB) which employs a charge pump to produce a body voltage that is less than ground. The control issue can be more complicated, especially if more than two body voltages are permitted. For the case of two modes, the control case is similar to clock gating and subsystems can often be locally controlled. The situation becomes more complex if more power/performance points are permitted. In most cases, the controller must also handle any problems arising from the time it takes to charge or discharge the large well capacitances when changing modes.

2.3.2 Multiple Threshold Transistors

Another method to incorporate different thresholds on a chip is to simply use transistors with different intrinsic thresholds. Of course, this method requires the ability to choose the threshold voltage of a transistor during fabrication, thus the set of allowable threshold voltages is usually set by the foundry for a particular process. Although it is possible to have an arbitrary number of thresholds, most foundries provide two devices: a low threshold, high-leakage device for performance; and a high-threshold, low-leakage device for low power. This approach is commonly called a dual-V_t scheme, and the goal is to use as many low-leakage devices as possible while meeting the performance requirements. This approach fits well in standard cell design flows, because each gate can have a high speed and a low-leakage implementation. Although this doubles the size of the gate library, the resulting library is still feasible for use by commercial tools. Different approaches exist for the assignment of high-speed versus low-leakage gates. The most basic method maps to the high-speed library first, then replaces gates with low-leakage version wherever possible (or vice-versa). More advanced synthesis tools can incorporate power as part of the cost

function. [14] The dual-Vt method is widely used because there is no performance or area penalty, and the standby power consumption can be significantly decreased.

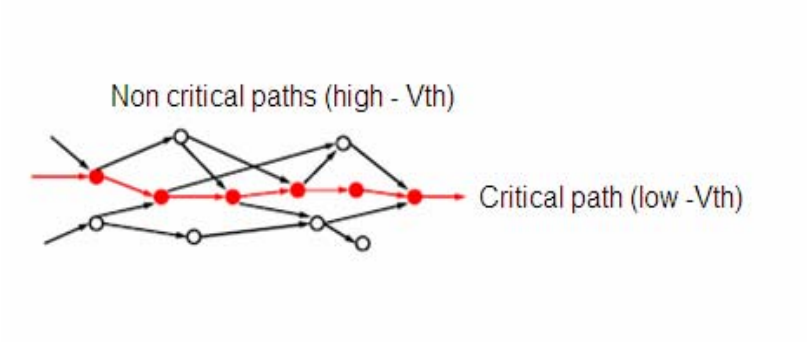


Figure 2.13 Dual V_{th} Scheme **[14]**

2.3.3 Power Rail Gating

Although leakage for non-critical paths can be reduced using high-Vt devices, devices still leak when the system is in standby. First, often a large number of low-Vt devices to be required to meet the timing requirements for a design. Second, even the "low-leakage" devices can have a large aggregate leakage current due to their large numbers. Thus, it is desirable to use a dynamic technique to reduce leakage further during a standby mode. The most promising approach is to gate the power supply rails as shown in Figure 2.14. This technique, called multi-threshold CMOS (MTCMOS), isolates the circuit from the supply rails using high-V_t power switches, called sleep transistors **[15]**. Although the Figure 2.14 shows sleep transistors on both the VDD and GND supplies, leakage currents are reduced even if only one polarity device is used. Probably the most obvious way to avoid losing the state is to prevent the virtual rails from degrading to the point that the state is lost. The minimum (maximum) voltage at which the state of the system is preserved is called the data retention voltage (DRV). One approach is to simply apply this voltage to the virtual supply rails using additional power switches, as shown in Figure 2.15a. The power switch transistors must be implemented using high-V_t devices to reduce the additional leakage current through the switches themselves. The DRV is determined through simulation of the various memory storage elements in the design, and the strictest constraint is typically used for all devices to reduce the number of voltages that must be generated and distributed.

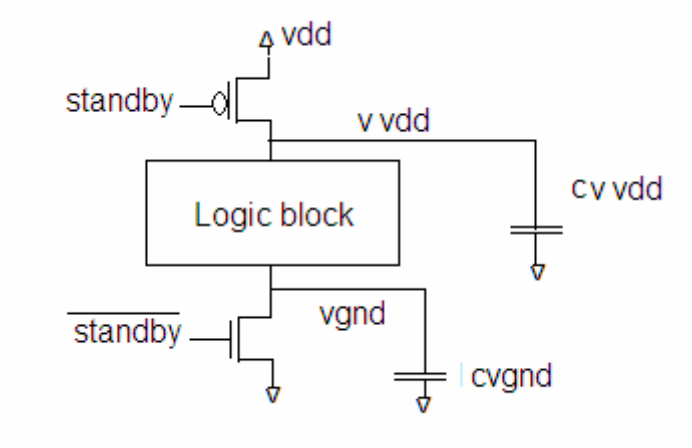
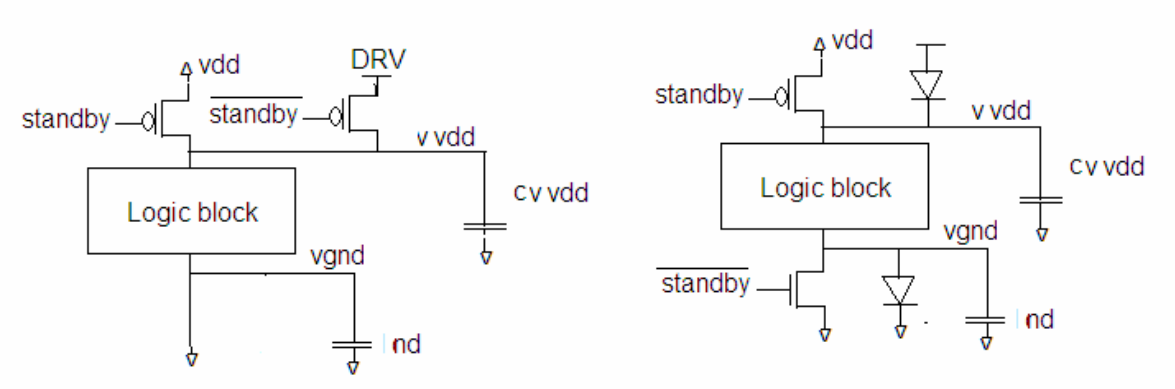


Figure 2.14 Circuit for multiple threshold CMOS (MTCMOS) using sleep transistors.

Although the DRV is the strict lower bound, a margin is usually reserved to improve reliability in the presence of noise. The DRV approach suffers from an increased area penalty to implement the second set of power switches. Also, a voltage converter is needed to generate the retention voltage, and it has an area and power overhead. Another approach to save the state clamps the virtual rails within a certain range. As shown in Figure 2.15b, this is the approach used in virtual rail clamp (VRC) logic, which employs small forward-biased diodes to ensure second set of power switches. Also, a voltage converter is needed to generate the retention voltage, and it has an area and power overhead. Another approach to save the state clamps the virtual rails within a certain range. As shown in Figure 2.15b, this is the approach used in virtual rail clamp (VRC) logic, which employs small forward biased diodes to ensure that the virtual supply does not float too far. When the sleep transistors turn off, the virtual supply rails are isolated until they reach the intrinsic potential barrier of the diode, at which point the diode clamps the virtual supply. Assuming the clamping voltage is higher than the DRV, the VRC Method avoids the problems caused by the loss of state. Since the clamps do not require the explicit generation of the retention voltage, VRC can be viewed as a "poor man's" DRV. The cost, of course, is the area required to implement the diodes, which can be significant and is in addition to the large sleep transistors. Both the DRV and VRC approaches have larger leakage than the basic MTCMOS approach, because the rails are not entirely isolated from the logic. **[16, 17]**



(a) Data retention voltage (DRV) (b) Virtual rail clamp(VRC)

Figure 2.15 Circuit variants of MTCMOS that retain the state

However, the time to restore the circuit is reduced, because the capacitance on the virtual supply does not need to be charged much to achieve a level acceptable for active operation. The major benefit of the DRV and VRC methods are that the state of the system is maintained, although both require area and power overhead to do so. The most important static parameter for an MTCMOS design is the size of the sleep transistor. The trade-off here is the area of the sleep transistor vs. the performance degradation of the circuit. As shown in Figure 2.16 for a MTCMOS test circuit with a PMOS

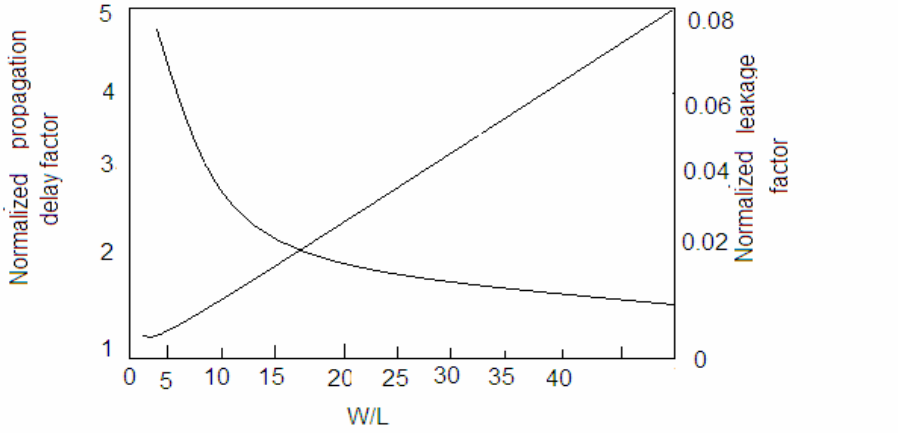


Figure 2.16 Graph of performance and leakage vs. power switch size for inverter chain. Values are normalized to the same basic circuit without the sleep transistor **[16]**.

sleep transistor, a larger transistor (higher W/L) has a lower equivalent resistance in series with the circuit, so the performance improves. Just the presence of the sleep transistor

increases the stack effect, which significantly reduces the leakage. As shown, sizing the sleep transistor has only a 6% effect on leakage over the sizing range, when compared to a baseline circuit with no sleep transistor. Also important for MTCMOS is amount of capacitance on the virtual supply. Current spikes cause the virtual voltage to temporarily degrade, since they increase the voltage drop across the sleep transistor. A larger capacitance on the virtual supply reduces the effects of current spikes by essentially forming a low-pass filter with the sleep transistor.

Figure 2.17 shows the lowest level the virtual supply rail V_{vdd} reaches for the test circuit. The more the virtual supply degrades, the lower the performance of the circuit. Some performance can be recovered by adding additional capacitance at the virtual supply node.

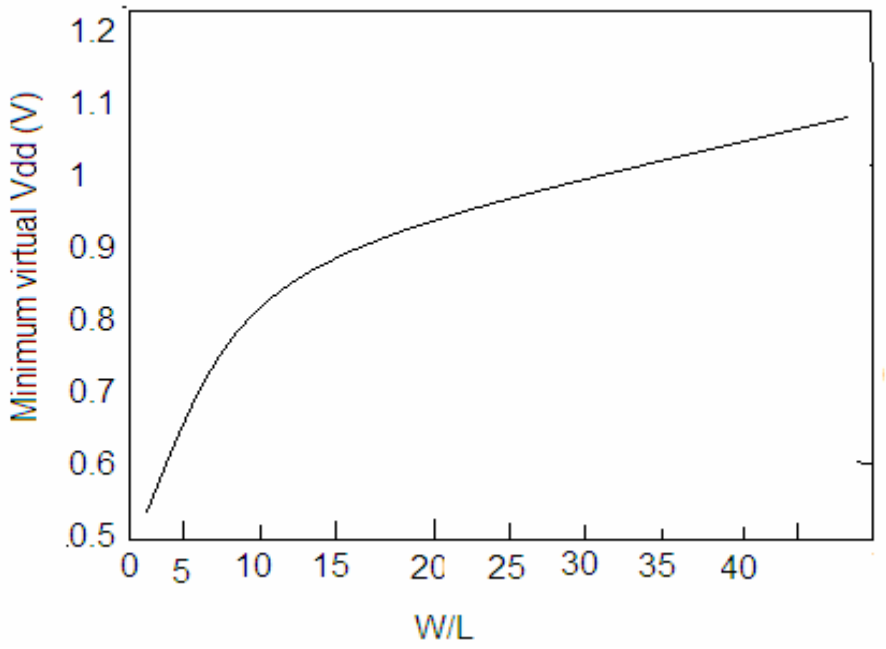


Figure 2.17 Graph of lowest virtual supply voltage vs. MTCMOS power switch size for inverter chain with VDD = 1.2V **[16]**

2.4 Comparison of Techniques

The effectiveness of various power saving devices and circuits is summarized in Table 2.1, simulated using a small test circuit in a 90nm process. The stack effect can be combined with any of the other techniques, as it is simply a choice of gate topology. The dual V_t technique can also be combined with other techniques, although it loses effectiveness at

lower VDD voltages because there will simply not be enough margin to separate the V_t voltages much. Similarly, VTCMOS is expected to lose effectiveness as L and V_t decrease, due to the described short channel effects. Thus, the most promising leakage reduction schemes are the MTCMOS variants, due to their high leakage reduction factor and tunable delay impact. The simplest MTCMOS implementation has a problem with state maintenance, which is addressed in the DRV and VRC variants, at the expense of additional overhead. Each of the techniques can be classified as either static or dynamic. Static techniques are those that are set at design time and do not require any time dependent controlling parameters. The dual- V_t and stack effect techniques fall into this category. Dynamic techniques require one or more controlling parameters to select the correct circuit mode. The clock gating, VTCMOS, and MTCMOS variants fall into the dynamic category. Dynamic techniques have additional concerns because the appropriate control signal(s)

Table 2.1 Summary of leakage reduction techniques (leakage factors for 90nm process) **[18]**

Technique	Leakage Saving	Delay Penalty	Outlook
Stack effect	8-40x	Free(natural) 2x(artificial)	Combinable with other techniques
Dual-Vt	1-38x	Tunable	Combinable; less at lower VDD
VTCMOS	4x (V_{SB} =0.5V)	None	Loses effect for smaller L and Vt
MTCMOS	2-1000x	Tunable	Most promising but loses state

must be generated so that power consumption is reduced. Even in a system with a simple control mechanism for each circuit, the situation quickly becomes more complicated when multiple modes are supported. Care must be taken that interacting circuits are active when necessary to ensure correct operation of the system. This is made more difficult if the transitions between modes take some time.

CHAPTER 3

STANDARD CELL LIBRARIES

Cadence works with several standard cell libraries. A cell library consists of different cells, such as logic gates, transistors and pads etc. Each cell in turn consists of different views. These views are used for different purposes. The schematic view, for instance, allows the designer to make a little less detailed construction before starting the layout. The construction on the schematic level can then be used for simulation, and once it is confirmed that the construction is correct, the layout can be constructed. This can be made at even a higher abstraction level by using Verilog.

3.1 Required Cells

This part describes what cells that are needed in a standard cell library and function of those cells.

3.1.1 Logical Cells

A cell library must be able to create any logical expression possible that might be needed in a synthesis of any design. To do this a number of cells with logical functions are needed. There are plenty of functions that can be implemented e.g. AND, NAND, OR, NOR, XOR and NOT. However, only a few of these are required in a minimum cell library since several functions can be created from a combination of other functions**. [19, 20]** For example:

Table 3.1 Truth Table for the function NOR

a	b	a NOR b	(NOT a) AND (NOT b)
0	0	1	1
0	1	0	0
1	0	0	0
1	1	0	0

As shown in Table 3.1, the function NOR can be replaced by a number of AND and NOT functions. Further, AND can be replaced with a NAND followed by a NOT etc. As described, all logical expressions can be created with a few logical cells, however, the construction will be much more complex and contain many more cells when just using a cell library consisting of a few cells. The minimum requirement for a standard cell library is simply enough cells to be able to create all logical expressions possible, which is fulfilled with just a NAND cell. It's even possible to create all possible expressions using nothing but a NOR-cell but as mentioned, it can be more area-effective to create a number of logical gates so that the place and route tool doesn't have to create them itself. It is also wise to create several different cells implementing the same function but with differently sized transistors so that their different fanout load limit, speed and area can be used by the synthesis tools when optimizing a design in respect of these different requirements. This however is not required for a minimum, working cell library **[21, 22]**.

3.1.2 Synchronous Cells

A cell library also needs synchronous cells so that counters, registers and other cells dependent on a clock signal can be created. Therefore a flip-flop must be created, for example a D-flip-flop (DFF). The DFF must have complementary output and support enable, reset and preset control signals so that all possible functionality is supported.

3.1.3 Buffers

At least one buffer has to be created in the cell library. This is required so that the synthesizer can amplify signals and also delay signals if there are timing constraints requiring that. The buffer should also be a tri-strate buffer so that several buffers can be attached to a data bus or similar. This is needed to be able to control the buffers to not output to the bus all at once but only one at a time. As with the other cells it is good to have several different buffers with different driving capabilities and delays to give the synthesizer the option to choose the buffer that is most suitable for the current design.

3.1.4 Optional Cells

There are a couple of types of cells that don't provide extra functionality of the cell library. These cells contribute in a way that makes the placed and routed design demand less manual work after it has been created. These cells are filler cells that help fill the unused area in the design and capacitance cells that add decaps to the design, which otherwise would

have had to be added manually.

3.1.5 Core Filler Cells

In the unused area in between the core cells that's left when the place and route tool has placed all the functional cells, filler cells can be placed to fill up the empty space. This is done to add as much coverage as possible automatically and avoid design rule violations. The filler cells also function as decaps. Several differently sized filler cells should be created so that the tool can place larger filler cells in large open spaces and smaller in the smaller open spaces, so that as few filler cells as possible are used, decreasing the complexity and amount of cells used in the final design. The sizes of the filler cells are technology dependent. The smallest filler cell should have the minimum width possible to still fulfill all the requirements of a layout. The width of the cells should be a multiple of the spacing in horizontal direction of the routing grid (Y-Pitch). The minimum multiple is 1, therefore the smallest filler cell should have the width of Y pitch **[23].**

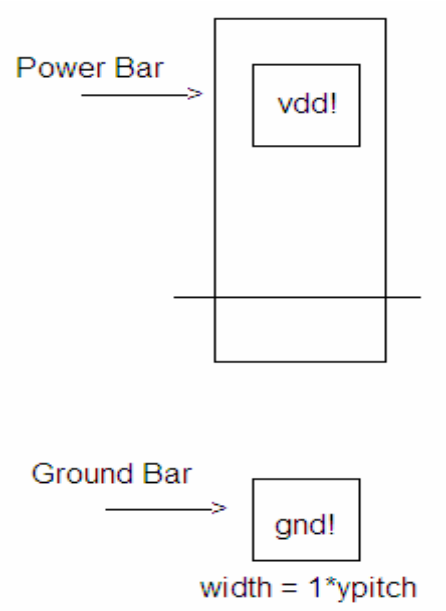


Figure 3.1 Minimum sized filler cell

The minimum sized filler cell in Figure 3.1 doesn't contain much, and its only function is to relay the ground and power bars in the spaces where it is placed. The only things in the minimum sized filler cell are a ground and power bar, not even n-well and p-substrate contacts. With only this filler cell no coverage at all would be added to the design

so more filler cells are needed. The next filler cell should be twice as wide as the minimum sized one and contain two transistors, adding coverage and capacitance. **[24, 25]** One pmos and one nmos transistor are used where the drain of each transistor is connected to the gate of the other one as the schematic in Figure 3.2 shows. However, there is no use in creating schematics of the filler cells unless it is desired to be able to import the final design back into Cadence and testing it with LVS (Layout Versus Schematic). If that is desired then schematics must be created so that the schematic and layout can match. It is desirable to make the filler cell as compact as possible without breaking any of the layout constraints.

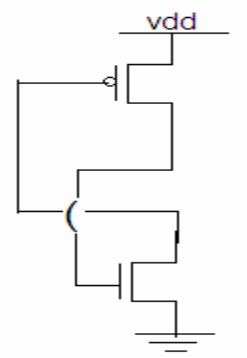


Figure 3.2 Schematic of a filler cell

3.2 Methodology of Characterization and Layout of cells

3.2.1 Physical Specifications

Table 3.2 The physical design specifications of this library **[26]**

Drawn Gate Length (μm)	0.10
Layers of Metal	6,7,8
Layout Grid (μm)	0.003
Vertical Pin Grid (μm)	0.30
Horizontal Pin Grid (μm)	0.30
Cell Power and Ground Rail Width (μm)	0.20
Cell Height (μm)	2.40

Table 3.3 The electrical specifications for this library **[26]**

Parameter	Minimum	Typical	Maximum
DC Supply Voltage(Vdd)	0.96V	1.20 V	1.44 V
Junction Temperature	-40^{o} C	25^{o} C	125^{o} C

3.2.2 Terms related to characterization of cells

3.2.2.1 Propagation Delay

The propagation delay through a cell is the sum of the intrinsic delay, the load-dependent delay, and the input-slew dependent delay. Delays are defined as the time interval between the input stimulus crossing 50% of Vdd and the output crossing 50% of Vdd. Figure 1 illustrates the propagation delay **[27].**

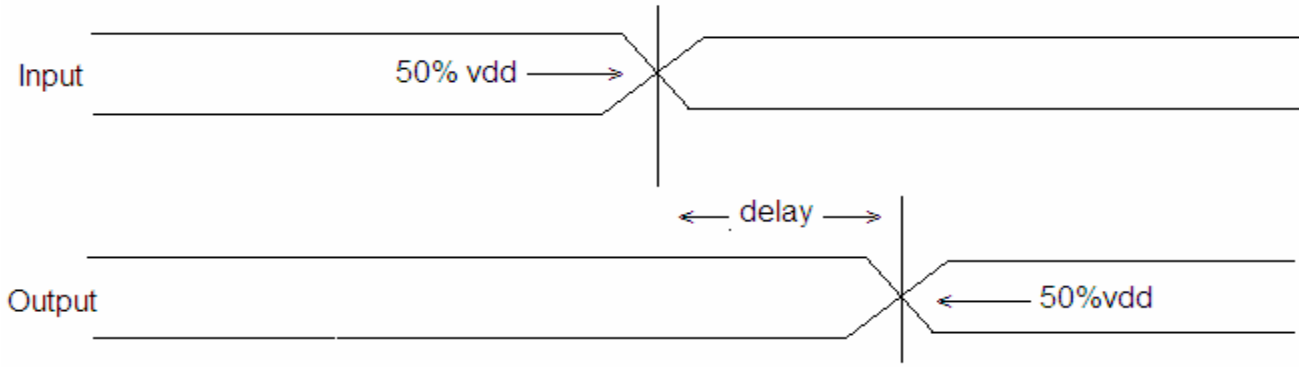


Figure 3.3 Propagation Delay

3.2.2.2 Output Slew (Transition) Time

The transition times (slews) on output pins are defined as the time interval between the signal crossing 10% of Vdd and 90% of Vdd . Figure 3.4 illustrates transition time measurements for rising and falling signals. Factors that affect propagation delays and transition time include: temperature, supply voltage, process variations, fanout loading, interconnect loading, input-transition time, input signal polarity, and timing constraints. The timing models provided with this library include the effects of input-transition time on propagation delays.

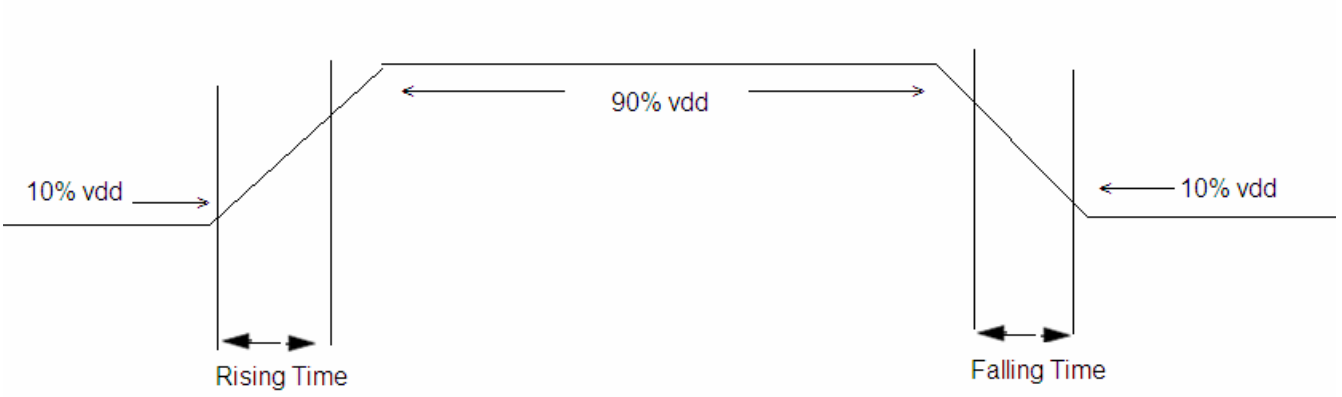


Figure 3.4 Transition Time

3.2.2.3 Timing Constraints

Timing constraints define minimum time intervals during which specific signals must be held steady in order to ensure the correct functioning of any given cell. Timing constraints include: setup time, hold time, recovery time, and minimum pulse width. Timing constraints can affect propagation delays. The intrinsic delays given in the datasheets are measured with relaxed timing constraints (longer than necessary setup times, hold times, recovery times, and pulse widths).The use of shorter timing constraint intervals may increase delay. Each cell is considered functional as long as the actual delay does not exceed the delay given in the datasheets by more than 10% **[27].**

3.2.2.3.1 Setup Time

The setup time for a sequential cell is the minimum length of time the data-input signal must remain stable before the active edge of the clock (or other specified signal) to ensure correct functioning of the cell. The cell is considered functional as long as the delay for the output reaching its expected value does not exceed the reference delay (measured with a large setup time) by more than 10%. **[28]** Setup constraint values are measured as the interval between the data signal crossing 50% of Vdd for rising data (or 50% of Vdd for falling data) and the clock signal crossing 50% of Vdd for rising clocks (or 50% of Vdd for falling clocks).

3.2.2.3.2 Hold Time

The hold time for a sequential cell is the minimum length of time the data-input signal must remain stable after the active edge of the clock (or other specified signal) to

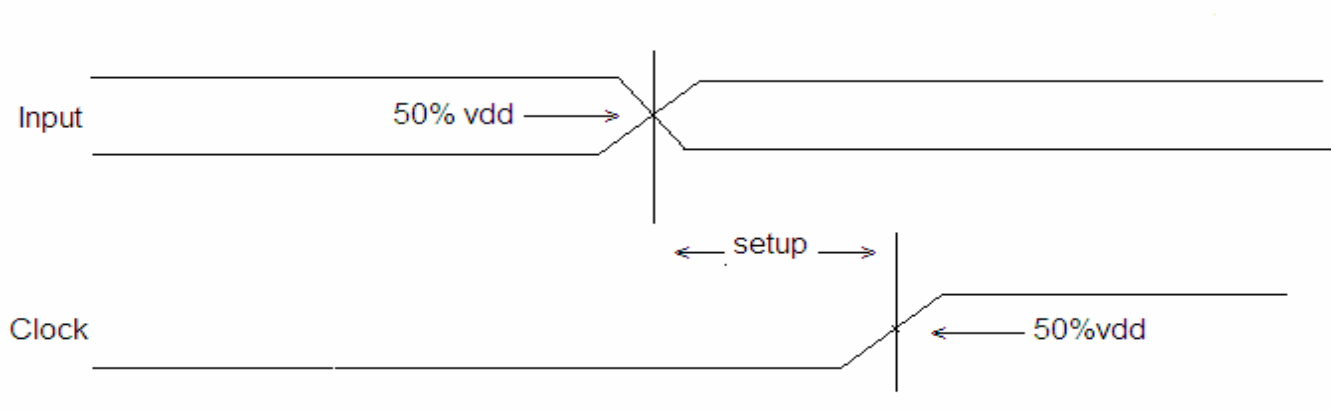


Figure 3.5 Setup Time

ensure correct functioning of the cell. The cell is considered functional as long as the delay for the output reaching its expected value does not exceed the reference delay (measured with a large hold time) by more than 10%. Hold-constraint values are measured as the interval between the data signal crossing 50% of Vdd for rising data (or 50% of Vdd for falling data) and the clock signal crossing 50% of Vdd for rising clocks (or 50% of Vdd for falling clocks). For the measurement of hold time, the data input signal is held stable before the active clock edge for an infinite setup time. Figure 3.6 illustrates hold time for a positive-edge-triggered sequential cell.

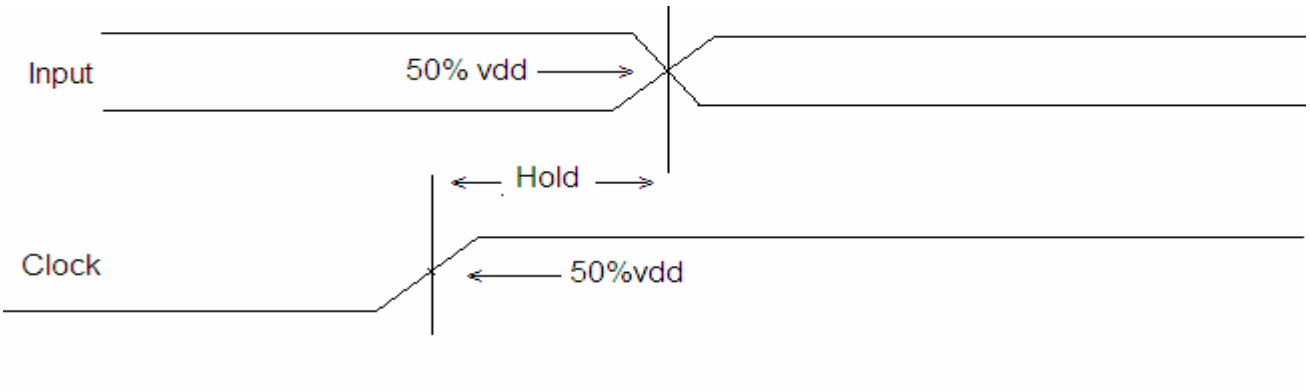


Figure 3.6 Hold Time

3.2.2.3.3 Recovery Time

Recovery time for sequential cells is the minimum length of time that the active-low set or reset signal must remain high before the active edge of the clock to ensure correct

functioning of the cell. The cell is considered functional as long as the delay for the output reaching its expected value does not exceed the reference delay (measured with a large recovery time) by more than 10%. Recovery constraint values are measured as the interval between the set or reset signal crossing 50% of Vdd and the clock signal crossing 50% of Vdd for rising clocks (or 50% of Vdd for falling clocks). For the measurement of recovery time, the set or reset signal is held stable after the active clock edge for an infinite hold time. Figure 3.7 illustrates recovery time.

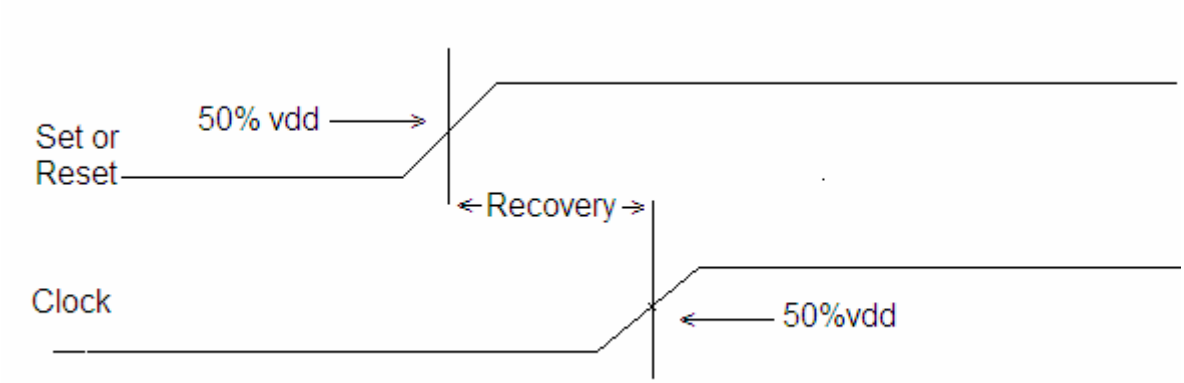


Figure 3.7 Recovery Time

3.2.2.3.4 Removal Time

Removal time for sequential cells is the minimum length of time that the active low set or reset signal must remain low after the active edge of the clock to ensure correct functioning of the cell. The cell is considered functional as long as the active clock edge does not latch in a new data value from that programmed by the asynchronous set or reset signal. Removal constraint values are measured as the interval between the set or reset signal crossing 50% of Vdd and the clock signal crossing 50% of Vdd for rising clocks (or 50% of Vdd for falling clocks). For the measurement of removal time, the set or reset signal is held stable before the active clock edge for an infinite setup time. Figure 3.6 illustrates removal time.

3.2.2.3.5 Minimum Pulse Width

Minimum pulse width is the minimum length of time between the leading and trailing edges of a pulse waveform. Minimum pulse width high (minpwh) is measured as the interval between the rising edge of the signal crossing 50% of Vdd and the falling edge of the signal

crossing 50% of Vdd.

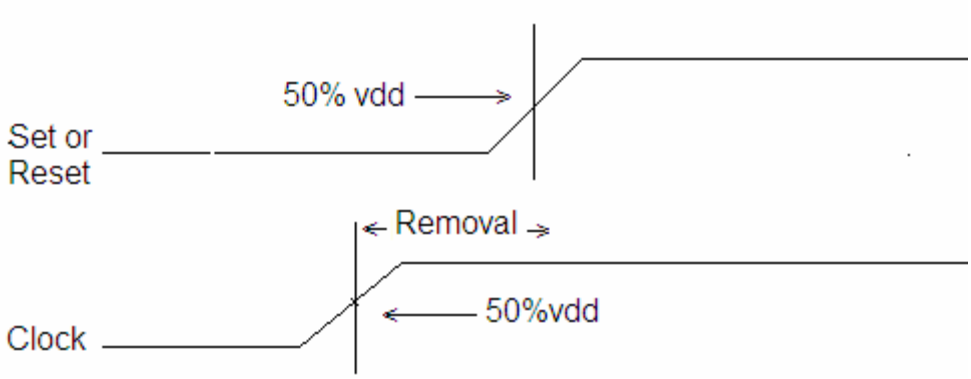


Figure 3.8 Removal Time

Minimum pulse width low (minpwl) is measured as the interval between the falling edge of the signal crossing 50% of Vdd and the rising edge of the signal crossing 50% of Vdd. Figure 7 illustrates minimum pulse width.

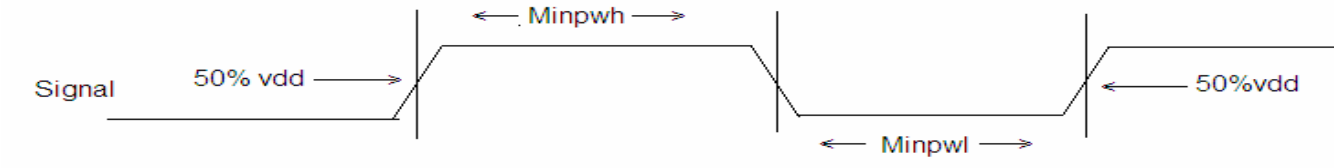


Figure 3.9 Minimum Pulse Widths

3.2.2.4 Logic Symbol

The logic symbol is a graphical representation of the cell, similar to the view in the schematic editor when the cell is instantiated. The symbol shows the name and location of the input and output pins.

3.2.2.5 Cell Size

This cell size table gives the height and width (μ m) for each drive strength of the cell.

3.2.2.6 Drive Strength

The drive strength of each cell is indicated by an "X" followed by the unit strength.

3.2.3 Electromigration

Electromigration (EM), the mass transport of a metal due to the momentum transfer between conducting electrons and diffusing metal atoms, exists wherever current flows

through metal wires. When electrons flow through wires on a chip, they collide with metal atoms, producing a force on the atoms that causes the wires to break over the chip's lifetime. Making wires thicker was easy when they were 10 microns wide, but, due to the difference in aspect ratio, it's not easy with today's 130 nanometer and 90 nanometer technologies. The conditions necessary for EM to be a significant problem continue to bear down on us with increasing speed and ferocity: high current densities, long narrow wires, logic hazards, and high operating frequencies. These conditions now occur on both power grids and signal lines. The transition from aluminum wires to copper wires was promoted as solving the EM problem. This is far from the case. Copper has in fact made EM analysis of chips more complex. Reduced wire size in both width and thickness and higher frequencies continue to push the envelope of current densities wires can handle. Wire slotting and via characteristics in copper also lead to more complex design rules for EM **[29]**.

3.2.3.1 Electromigration Guideline Compliance

Artisan standard cell libraries are designed to meet foundry electromigration guidelines for normal chip design usage; however, it is the chip designer's responsibility to ensure that electromigration guidelines are met at the chip level with regard to foundry guidelines for how the library will be used. The following three Electromigration guidelines must be met in order to ensure safe use of the standard cell library within the electromigration guidelines of the foundry.

1. The width of the Metal1VDD and VSS power buses in the standard cells has been sized to provide adequate current to the cells. Vertical power straps must be placed with sufficient frequency to provide adequate current distribution to the standard cell power buses.
2. The output pin metal for each standard cell has been sized to accommodate multiple vias necessary (for worst case electromigration conditions) to meet via electromigration guidelines, although oversized Metal1 output pins do not necessarily require multiple vias. The number of vias required to meet electromigration guidelines is design dependent, and the chip designer must use an appropriate number of vias and wire width when routing from an output pin.
3. The internal layouts of the standard cells have been designed and verified to comply with the manufacturer's electromigration guidelines under normal usage.

4. The current required by the cell does not exceed the maximum current that can be supplied by the Metal1 power buses.

5. The output transition times (measured using 10%90% thresholds), for a cell outside the clock tree network, must be no greater than 20% of the total cycle time, or must be no greater than 10% of the cycle time for any of the output pins of that particular cell. Limiting the output transition time has the effect of limiting the load driven by the cell which will reduce the cell's current draw, making it comply with electromigration guidelines. Ratios larger than 20% are not appropriate for commonly used design flows and are unlikely to be encountered in normal designs.

6. For a cell in the clock tree network, transition times must not exceed 10%of the total cycle time for that cell.

3.3 Layout Guide Lines For Standard Cells

1. Power connections between cells formed by abutment **[30, 31]**.
2. Regular Pins (not VDD VSS) should align at a grid point (aligned with both vertical and horizontal grids).
3. Rows are placed to align with vertical and horizontal routing grids.
4 .Grid spacing needs to be at least line-on-via and are usually via-on-via.

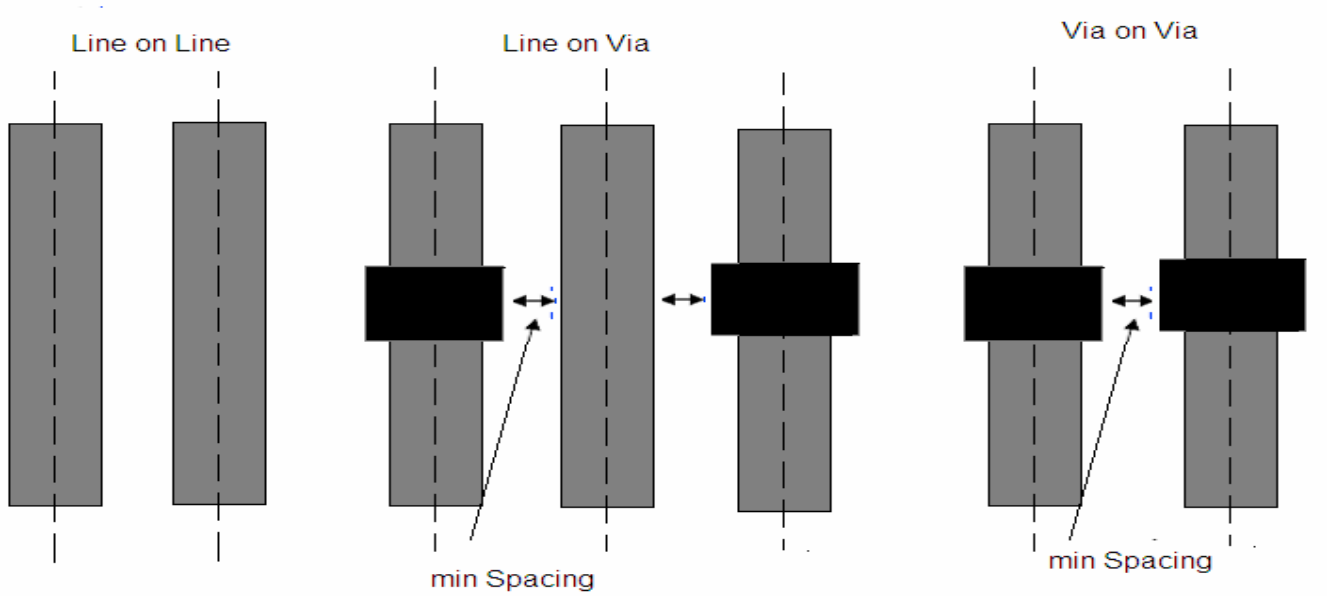


Figure 3.9 Grid spacing **[30, 31]**

5. Vertical PIN Grid(X) is based on via to via spacing with metal M1 and would be 0.30 um.

6. Horizontal PIN Grid(X) is based on via to via spacing with metal M1.
7. The cell height must be a multiple of the horizontal grid spacing and the cell width must be a multiple of the vertical grid spacing in our case both grid are same.
8. Preferred routing directions are poly, M2 vertical, M1 (and M3) horizontal.

CHAPTER 4

CELLS DESCRIPTION

4.1 OA21

The OA21cell provides the logical AND of one OR group and an additional input. The output (Y) is represented by the logic equation

$$Y = (A0 + A1) \bullet B \qquad ..4.1$$

Table 4.1 Function of OA21

A0	A1	B0	Y
X	X	0	0
0	0	X	0
X	1	1	1
1	X	1	1

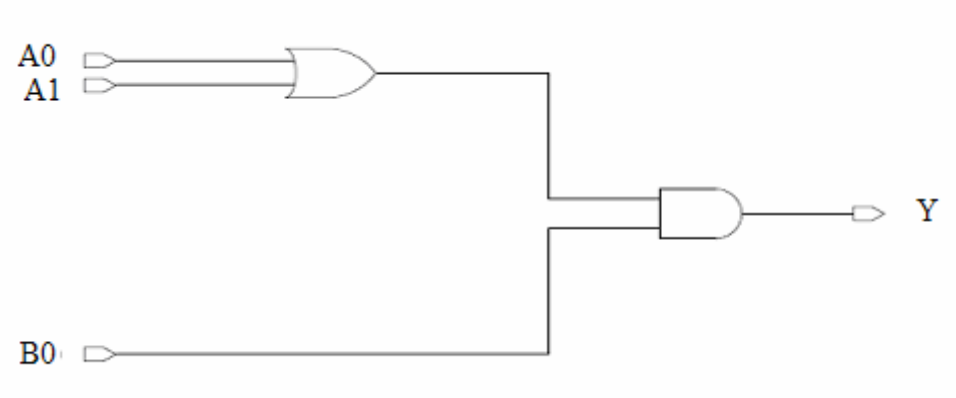


Figure 4.1 Functional Schematic of OA21

Table 4.2 Cell Size of OA21

Drive Strength	Height (μm)	Width (μm)
OA21XL	2.40	2.24
OA21X1	2.40	2.24
OA21X2	2.40	2.24
OA21X4	2.40	2.80
OA21X8	2.40	4.48

4.2 OA22

The OA22 cell provides the logical AND of two OR groups. The output (Y) is represented by the logic equation:

$$Y = (A0 + A1) \bullet (B0 + B1) \quad ..4.2$$

Table 4.3 Function of OA22

A0	A1	B0	Y
X	X	0	0
0	0	X	0
X	1	1	1
1	X	1	1

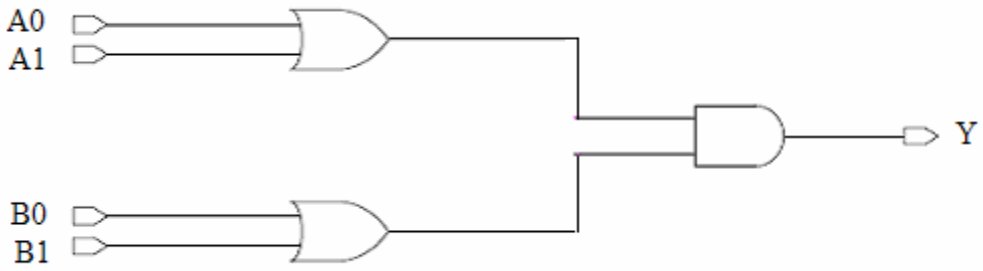


Figure 4.2 Functional Schematic of OA22

Table 4.4 Cell Size of OA22

Drive Strength	Height (μm)	Width (μm)
OA22XL	2.40	2.52
OA22X1	2.40	2.52
OA22X2	2.40	2.52
OA22X4	2.40	3.08
OA22X8	2.40	5.32

4.3 OAI21

The OAI21cell provides the logical inverted AND of one OR group and an additional input.The output (Y) is represented by the logic equation:

$$Y = \overline{(A0 + A1) \bullet B0} \qquad ..4.3$$

Table 4.5 Function of OAI21

A0	A1	B0	Y
0	0	X	1
X	X	0	1
X	1	1	0
1	X	1	0

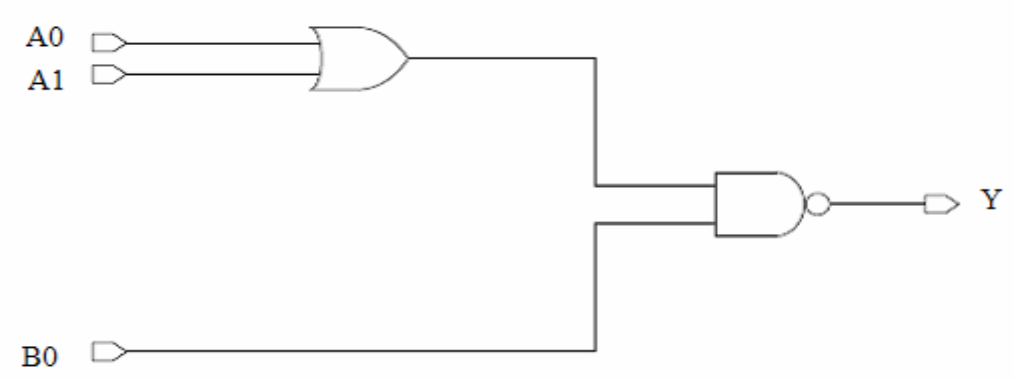


Figure 4.3 Functional Schematic of OAI21

Table 4.6 Cell Size of OAI21

Drive Strength	Height (μm)	Width (μm)
OAI21XL	2.40	1.68
OAI21X1	2.40	1.68
OAI21X2	2.40	1.68
OAI21X3	2.40	2.80
OAI21X4	2.40	2.80
OAI21X6	2.40	3.92

4.4 OAI222

The OAI222 cell provides the logical inverted AND of three OR groups. The output (Y) is represented by the logic equation:

$$Y = \overline{(A0 + A1) \bullet (B0 + B1) \bullet (C0 + C1)} \quad ..4.4$$

Table 4.7 Function of OAI222

A0	A1	B0	B1	C0	C1	Y
0	0	X	X	X	X	1
X	X	0	0	X	X	1
X	X	X	X	0	0	1
X	1	X	1	1	X	0
X	1	X	1	X	1	0
X	1	1	X	1	X	0
X	1	1	X	X	1	0
1	X	X	1	1	X	0
1	X	X	1	X	1	0
1	X	1	X	1	X	0
1	X	1	X	X	1	0

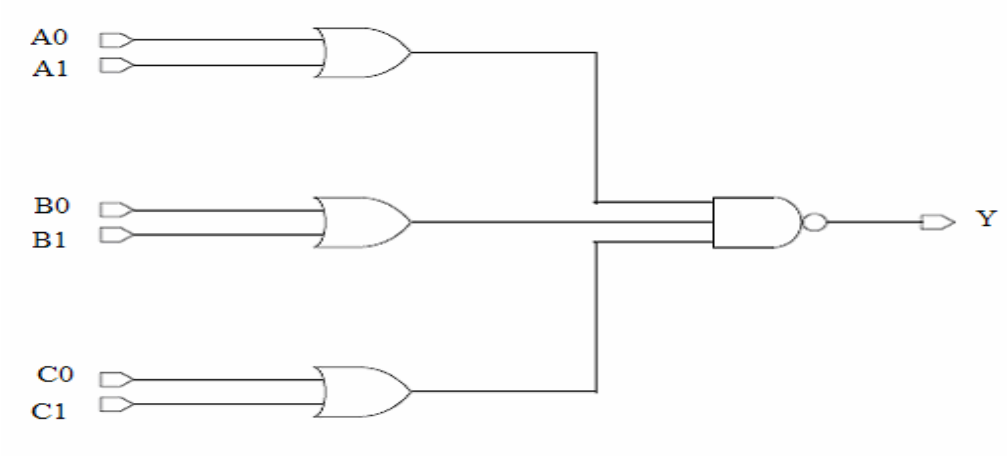


Figure 4.4 Functional Schematic of OAI222

Table 4.8 Cell Size of OAI222

Drive Strength	Height (µm)	Width (µm)
OAI222XL	2.40	3.08
OAI222X1	2.40	3.08
OAI222X2	2.40	3.08
OAI222X4	2.40	5.32

4.5 OAI2B1

The OAI2B1cell provides the logical inverted AND of one OR group and an additional input. The output (Y) is represented by the logic equation:

$$Y = \overline{\left(A0 + \overline{A1N}\right) \bullet B0} \qquad ..4.5$$

Table 4.9 Function of OAI2B1

A0	A1N	B0	Y
0	1	X	1
X	X	0	1
X	0	1	0
1	X	1	0

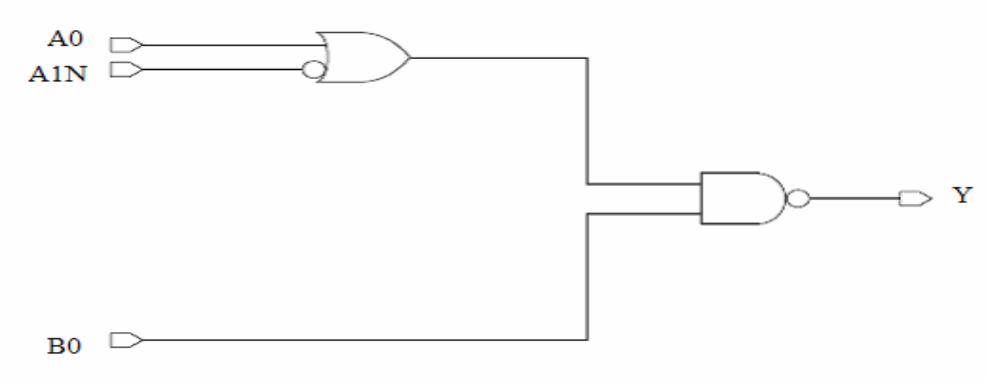


Figure 4.5 Functional Schematic of OAI2B1

Table 4.10 Cell Size of OAI2B1

Drive Strength	Height (µm)	Width (µm)
OAI2B1XL	2.40	2.24
OAI2B1X1	2.40	2.24
OAI2B1X2	2.40	2.24
OAI2B1X4	2.40	3.36
OA12B1X8	2.40	6.16

4.6 OAI2B11

The OAI2B11cell provides the logical inverted OR of one OR group and two additional inputs. The output (Y) is represented by the logic equation:

$$Y = \overline{\left(A0 + \overline{A1N}\right) \bullet B0 \bullet C0} \qquad ..4.6$$

Table 4.11 Function of OAI2B11

A0	A1N	B0	C0	Y
0	1	X	X	1
X	X	0	X	1
X	X	X	0	1
X	0	1	1	0
1	X	1	1	0

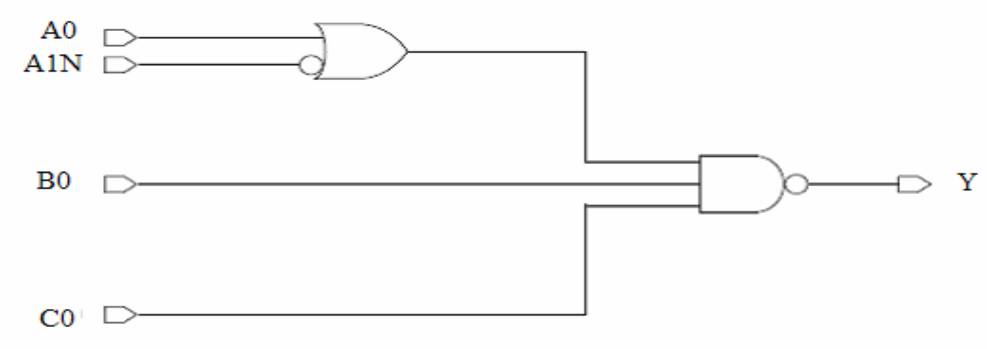


Figure 4.6 Functional Schematic of OAI2B11

Table 4.12 Cell Size of OAI2B11

Drive Strength	Height (µm)	Width (µm)
OAI2B11XL	2.40	2.52
OAI2B11X1	2.40	2.52
OAI2B11X2	2.40	2.52
OAI2B11X4	2.40	3.92

4.7 OAI2B2

The OAI2B2 cell provides the logical inverted AND of two OR groups. The output (Y) is represented by the logic equation:

$$Y = \overline{(A0 + \overline{A1N}) \bullet (B0 + B1)} \quad ..4.7$$

Table 4.13 Function of OAI2B2

A0	A1N	B0	B1	Y
0	1	X	X	1
X	X	0	0	1
X	0	X	1	0
X	0	1	X	0
1	X	X	1	0
1	X	1	X	0

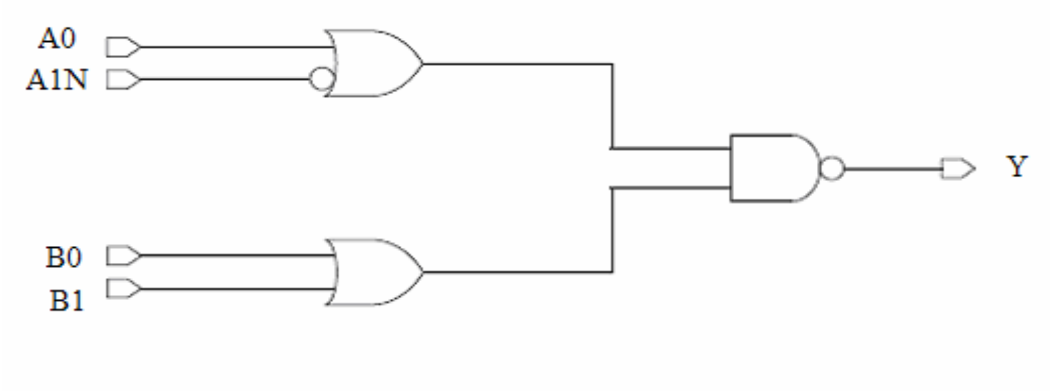


Figure 4.7 Functional Schematic of OAI2B2

Table 4.14 Cell Size of OAI2B2

Drive Strength	Height (μm)	Width (μm)
OAI2B2XL	2.40	2.52
OAI2B2X1	2.40	2.52
OAI2B2X2	2.40	2.52
OAI2B2X4	2.40	4.20
OAI2B2X8	2.40	7.84

4.8 OAI2BB1

The OAI2BB1cell provides the logical inverted AND of one OR group of two inverted inputs (A0N, A1N) and an additional non-inverted input (B0). The output (Y) is represented by the logic equation:

$$Y = \overline{\left(\overline{A0N} + \overline{A1N}\right) \bullet B0} \qquad ..4.8$$

Table 4.15 Function of OAI2BB1

A0N	A1N	B0	Y
1	1	X	1
X	X	0	1
X	0	1	0
0	X	1	0

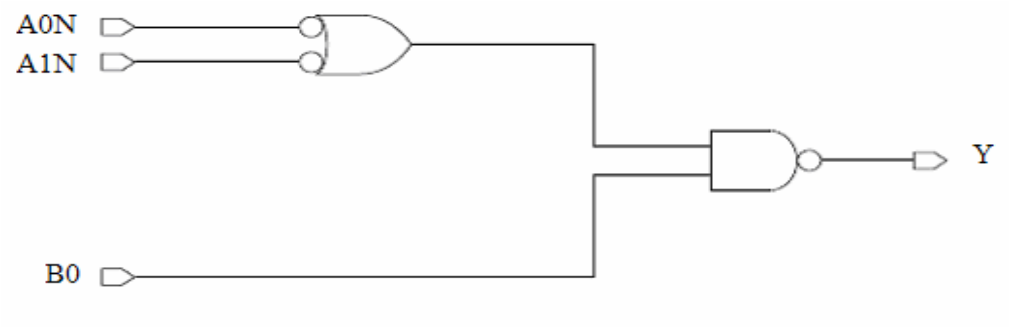


Figure 4.8 Functional Schematic of OAI2BB1

Table 4.16 Cell Size of OAI2BB1

Drive Strength	Height (μm)	Width (μm)
OAI2BB1XL	2.40	1.96
OAI2BB1X1	2.40	1.96
OAI2BB1X2	2.40	1.96
OAI2BB1X4	2.40	2.80

4.9 OAI2BB2

The OAI2BB2 cell provides the logical inverted AND of one OR group of two inverted inputs (A0N, A1N) and one OR group of two non-inverted inputs (B0, B1). The output (Y) is represented by the logic equation:

$$Y = \overline{\left(\overline{A0N} + \overline{A1N}\right) \bullet \left(B0 + B1\right)} \quad ..4.9$$

Table 4.17 Function of OAI2BB2

A0N	A1N	B0	B1	Y
1	1	X	X	1
X	X	0	0	1
X	0	X	1	0
X	0	1	X	0
0	X	X	1	0

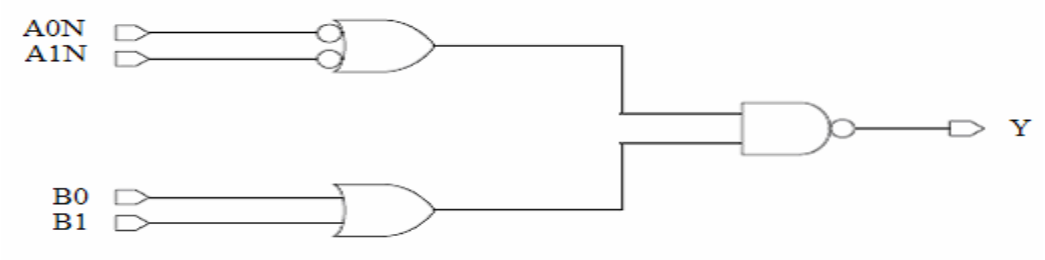


Figure 4.9 Functional Schematic of OAI2BB2

Table 4.18 Cell Size of OAI2BB2

Drive Strength	Height (μm)	Width (μm)
OAI2BB2XL	2.40	2.52
OAI2BB2X1	2.40	2.52
OAI2BB2X2	2.40	2.52
OAI2BB2X4	2.40	3.64
OAI2BB2X8	2.40	6.72

4.10 OAI21B

The OAI21B cell provides the logical inverted AND of one OR group and an additional input. The output (Y) is represented by the logic equation:

$$Y = \overline{(A0 + A1) \bullet \overline{B0N}} \qquad ..4.10$$

Table 4.19 Function of OAI21B

A0	A1	B0N	Y
0	0	X	1
X	X	1	1
X	1	0	0
1	X	0	0

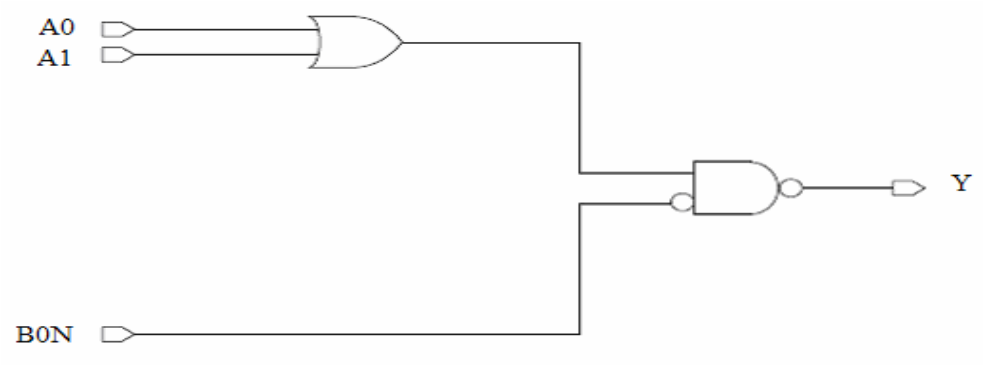


Figure 4.10 Functional Schematic of OAI21B

Table 4.20 Cell Size of OAI21B

Drive Strength	Height (µm)	Width (µm)
OAI21BXL	2.40	2.24
OAI21BX1	2.40	2.24
OAI21BX2	2.40	2.24
OAI21BX4	2.40	3.36
OAI21BX8	2.40	5.88

4.11 OR2

The OR2 cell provides the logical OR of two inputs (A,B). The output (Y) is represented by the logic equation:

$$Y = (A + B) \qquad ..4.11$$

Table 4.21 Function of OR2

A	B	Y
0	0	0
X	1	1
1	X	1

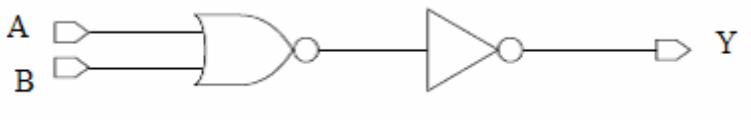


Figure 4.11 Functional Schematic of OR2

Table 4.22 Cell Size of OR2

Drive Strength	Height (μm)	Width (μm)
OR2X1	2.40	1.68
OR2X2	2.40	1.68
OR2X4	2.40	2.52
OR2X6	2.40	3.64
OR2X8	2.40	4.76
OR2X12	2.40	5.88

4.12 OR3

The OR3 cell provides the logical OR of three inputs (A,B,C).The output (Y) is represented by the logic equation:

$$Y = (A + B + C) \qquad ..4.12$$

Table 4.23 Function of OR3

A	B	C	Y
0	0	0	0
X	X	1	1
X	1	X	1
1	X	X	1

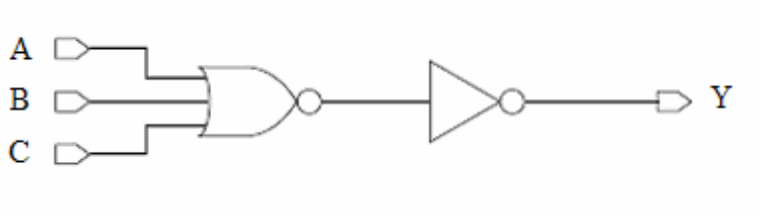


Figure 4.12 Functional Schematic of OR3

Table 4.24 Cell Size of OR3

Drive Strength	Height (µm)	Width (µm)
OR3X1	2.40	1.96
OR3X2	2.40	1.96
OR3X4	2.40	3.08
OR3X6	2.40	4.48
OR3X8	2.40	5.88

4.13 NOR2

The NOR2 cell provides a logical NOR of two inputs (A,B). The output (Y) is represented by the logic equation:

$$Y = \overline{(A + B)} \quad ..4.13$$

Table 4.25 Function of NOR2

A	B	Y
0	0	1
X	1	0
1	X	0

Figure 4.13 Functional Schematic of NOR2

Table 4.26 Cell Size of NOR2

Drive Strength	Height (μm)	Width (μm)
NOR2XL	2.40	1.12
NOR2X1	2.40	1.12
NOR2X2	2.40	1.12
NOR2X3	2.40	1.96
NOR2X4	2.40	1.96
NOR2X5	2.40	2.80
NOR2X6	2.40	2.80
NOR2X8	2.40	3.64
NOR2X12	2.40	5.60

4.14 MUX2

The MX2 cell is a 2-to-1multiplexer. The state of the select input (S0) determines which data input (A,B) is presented to the output (Y).The output (Y) is represented by the logic equation:

$$Y = \left(\overline{S0} \bullet A\right) + \left(S0 \bullet B\right) \qquad ..4.14$$

Table 4.27 Function of MUX2

S0	A	B	Y
0	0	X	0
0	1	X	1
1	X	0	0
1	X	1	1

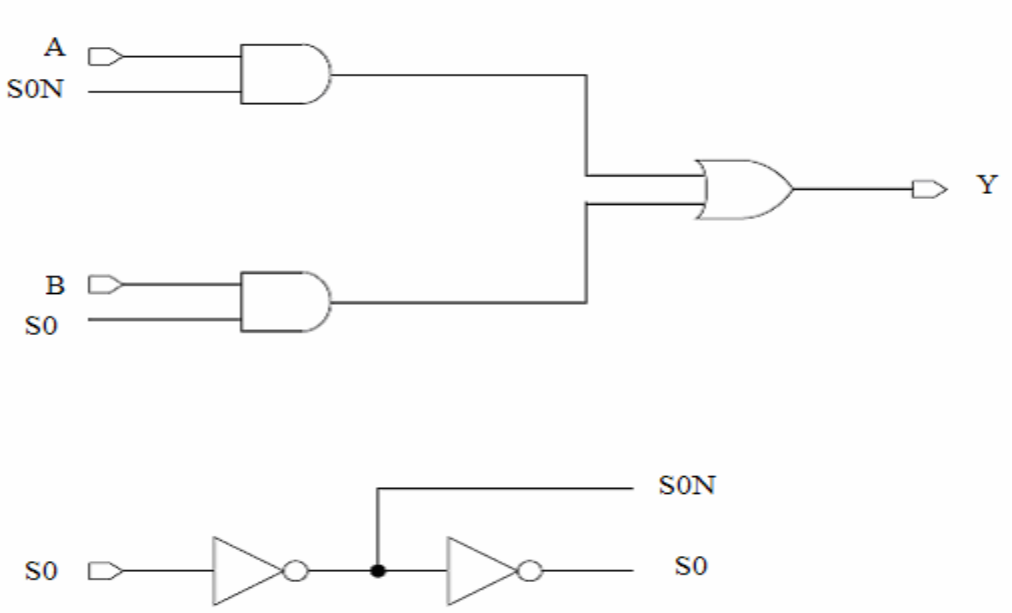


Figure 4.14 Functional Schematic of MUX2

Table 4.28 Cell Size of MUX2

Drive Strength	Height (µm)	Width (µm)
MX2XL	2.40	3.08
MX2X1	2.40	3.08
MX2X2	2.40	3.08
MX2X3	2.40	3.64
MX2X4	2.40	3.64
MX2X6	2.40	3.92
MX2X8	2.40	4.20
MX2X12	2.40	5.32

4.15 MUX3

The MX3 cell is a 3-to-1multiplexer. The state of the select inputs (S1,S0) determines which data input (A,B,C) is presented to the output (Y). The output (Y) is represented by the logic equation:

$$Y = \left(\overline{S0} \bullet \overline{S1} \bullet A\right) + \left(S0 \bullet \overline{S1} \bullet B\right) + \left(S1 \bullet C\right) \quad ..4.15$$

Table 4.29 Function of MUX3

S1	S0	A	B	C	Y
0	0	0	X	X	0
0	0	1	X	X	1
0	1	X	0	X	0
0	1	X	1	X	1
1	X	X	X	0	0
1	X	X	X	1	1

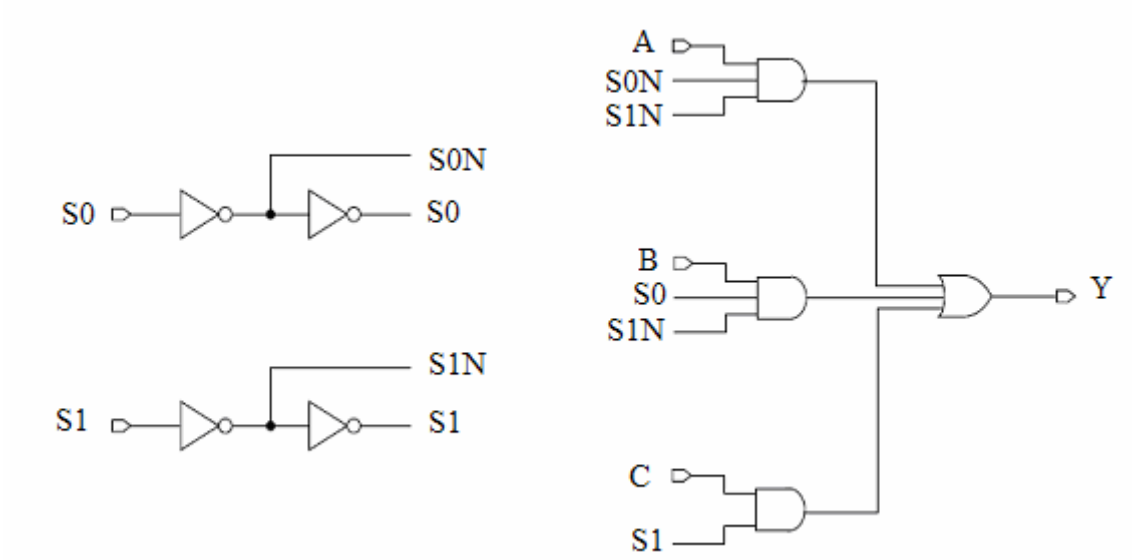


Figure 4.15 Functional Schematic of MUX3

Table 4.30 Cell Size of MUX3

Drive Strength	Height (μm)	Width (μm)
MX3XL	2.40	5.04
MX3X1	2.40	5.04
MX3X2	2.40	5.32
MX3X4	2.40	5.60
MX3X8	2.40	6.44

4.16 OAI31

The OAI31cell provides the logical inverted AND of one OR group and an additional input. The output (Y) is represented by the logic equation:

$$Y = \overline{(A0 + A1 + A2) \bullet B0} \qquad ..4.16$$

Table 4.31 Function of OAI31

A0	A1	A2	B0	Y
0	0	0	X	1
X	X	X	0	1
X	X	1	1	0
X	1	X	1	0
1	X	X	1	0

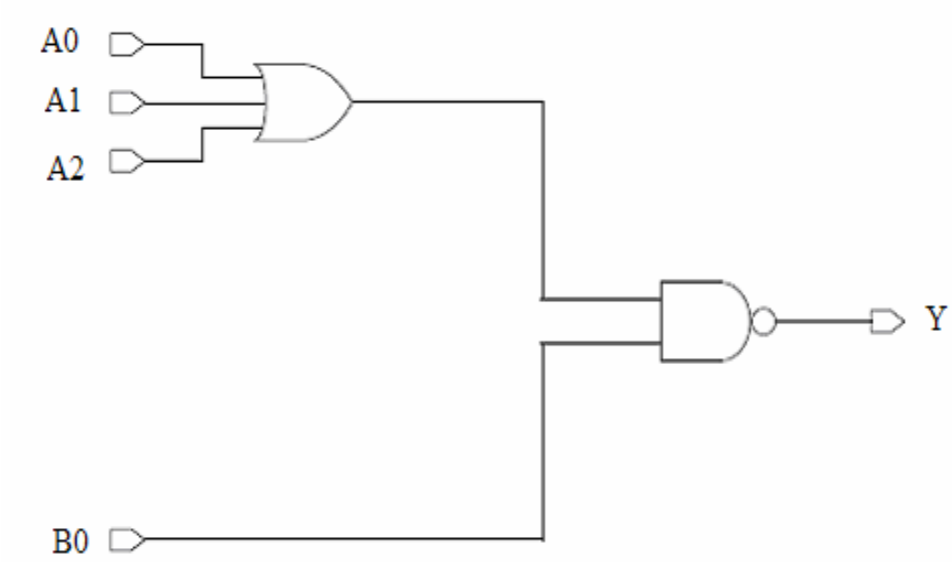


Figure 4.16 Functional Schematic of OAI31

Table 4.32 Cell Size of OAI31

Drive Strength	Height (μm)	Width (μm)
OAI31XL	2.40	5.04
OAI31X1	2.40	5.04
OAI31X2	2.40	5.32
OAI31X4	2.40	5.60

4.17 DFFH

The DFFH cell is a positive-edge triggered, static D-type flipflop and fast clock-to-Q-path.

Table 4.33 Function of DFFH

D	CK	Q[n+1]	QN[n+1]
0	0 -> 1	0	1
1	0 -> 1	1	0
X	1 -> 0	Q[n]	QN[n]

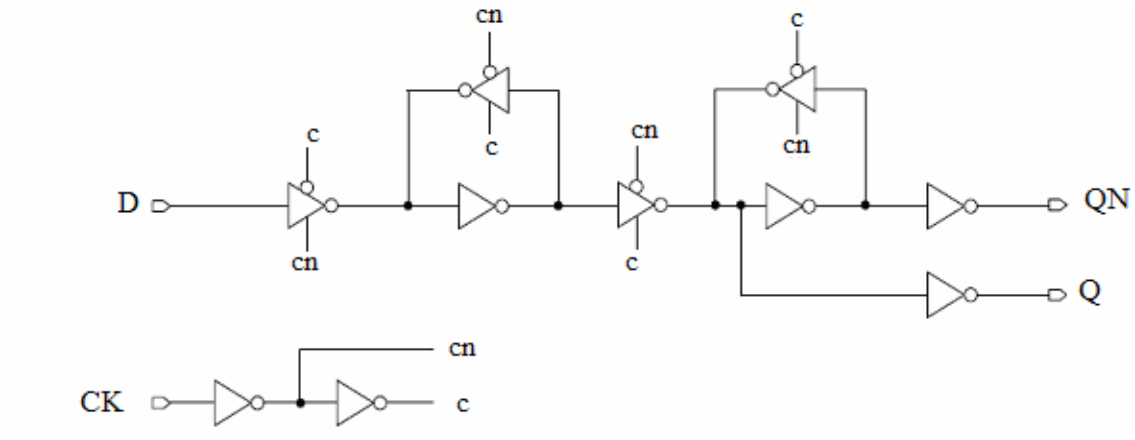


Figure 4.17 Functional Schematic of DFFH

Table 4.34 Cell Size of DFFH

Drive Strength	Height (μm)	Width (μm)
DFFHX1	2.40	8.12
DFFHX2	2.40	8.68
DFFHX4	2.40	11.48
DFFHX8	2.40	15.68

4.18 DFFHQ

The DFFHQ cell is a high-speed, positive-edge triggered, static D-type flip-flop. The cell has a single output (Q) and fast clock-to-out path.

Table 4.35 Function of DFFHQ

D	CK	Q[n+1]
0	0 -> 1	0
1	0 -> 1	1
X	1 -> 0	Q[n]

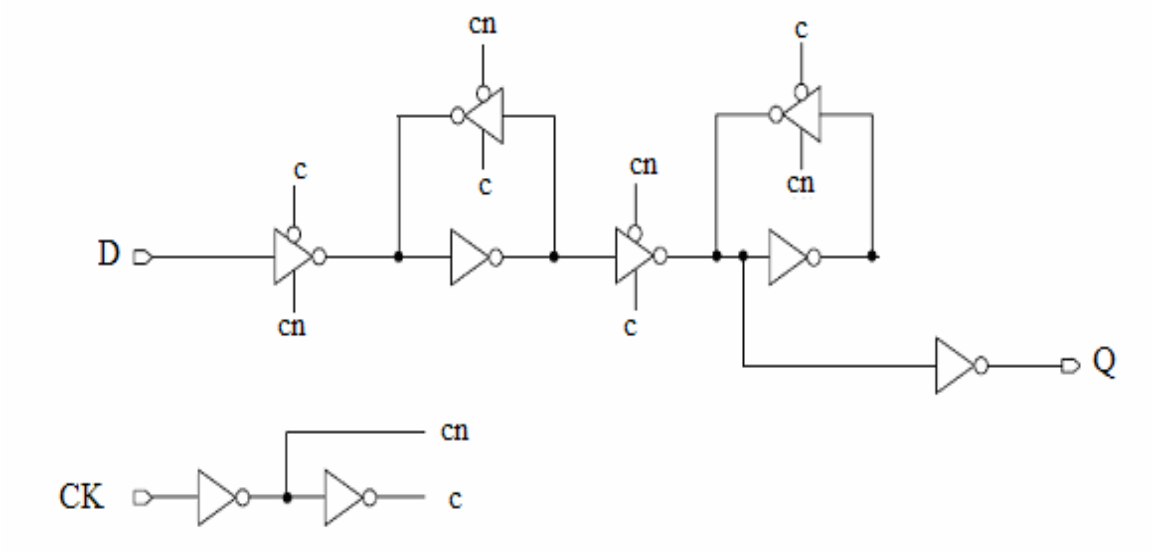


Figure 4.18 Functional Schematic of DFFHQ

Table 4.36 Cell Size of DFFHQ

Drive Strength	Height (μm)	Width (μm)
DFFHQX1	2.40	7.56
DFFHQX2	2.40	8.12
DFFHQX4	2.40	10.92
DFFHQX8	2.40	15.12

4.19 SDFFH

The SDFFH cell is a positive-edge triggered, static D-type flip-flop with scan input (SI), active-high scan enable (SE), and fast clock-to-Q-path.

Table 4.37 Function of SDFFH

D	SI	SE	CK	Q[n+1]	QN[n+1]
1	X	0	0 -> 1	1	0
0	X	0	0 -> 1	0	1
X	X	X	1 -> 0	Q[n]	QN[n]
X	1	1	0 -> 1	1	0
X	0	1	0 -> 1	0	1

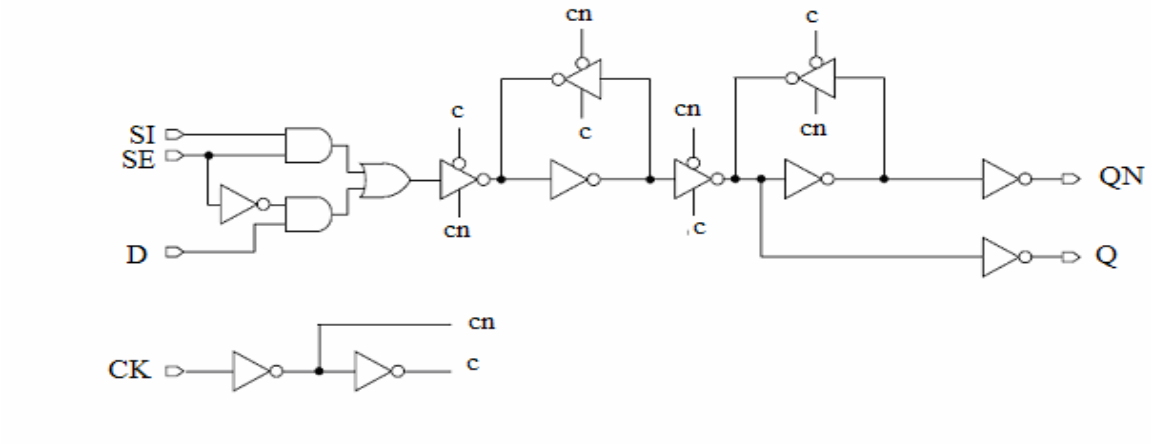


Figure 4.19 Functional Schematic of SDFFH

Table 4.38 Cell Size of SDFFH

Drive Strength	Height (μm)	Width (μm)
SDFFHX1	2.40	10.08
SDFFHX2	2.40	11.20
SDFFHX4	2.40	14.28
SDFFHX8	2.40	19.04

4.20 SDFFHQ

The SDFFHQ cell is a high-speed, positive-edge triggered, static D-type flip-flop with scan input (SI) and active-high scan enable (SE). The cell has a single output (Q) and fast clock to-out path.

Table 4.39 Function of SDFFHQ

D	SI	SE	CK	Q[n+1]
1	X	0	0 -> 1	1
0	X	0	0 -> 1	0
X	X	X	1 -> 0	Q[n]
X	1	1	0 -> 1	1
X	0	1	0 -> 1	0

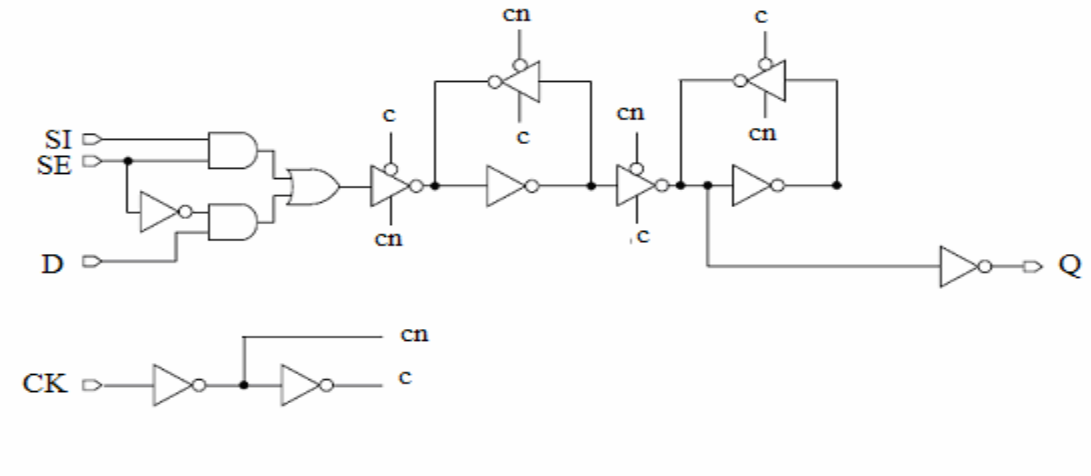


Figure 4.20 Functional Schematic of SDFFHQ

Table 4.40 Cell Size of SDFFHQ

Drive Strength	Height (μm)	Width (μm)
SDFFHQX1	2.40	9.80
SDFFHQX2	2.40	10.64
SDFFHQX4	2.40	13.72
SDFFHQX8	2.40	18.20

4.21 SDFFNH

The SDFFNH cell is a negative-edge triggered, static D-type flip-flop with scan input (SI), active high scan enable (SE), and fast clock-to-Q-path.

Table 4.41 Function of SDFFNH

D	SI	SE	CKN	Q[n+1]	QN[n+1]
1	X	0	1 -> 0	1	0
0	X	0	1 -> 0	0	1
X	X	X	0 -> 1	Q[n]	QN[n]
X	1	1	1 -> 0	1	0
X	0	1	1 -> 0	0	1

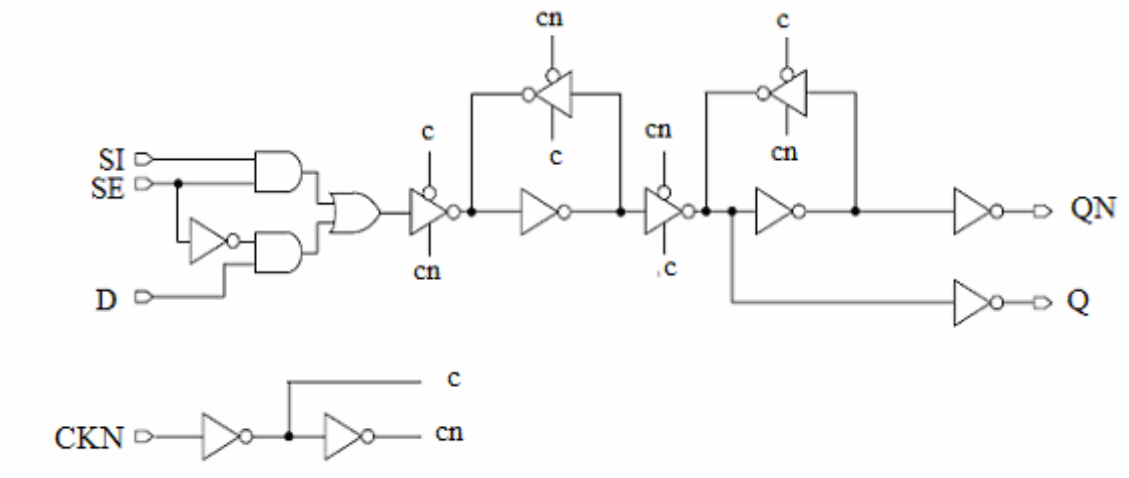


Figure 4.21 Functional Schematic of SDFFNH

Table 4.42 Cell Size of SDFFNH

Drive Strength	Height (μm)	Width (μm)
SDFFNHX1	2.40	10.80
SDFFNHX2	2.40	11.64
SDFFNHX4	2.40	14.00
SDFFNHX8	2.40	18.76

CHAPTER 5

Ultra Low Power Standard Cells Library Design Document

Results And Waveforms

5.1 OAI21

5.1.1 SPEED

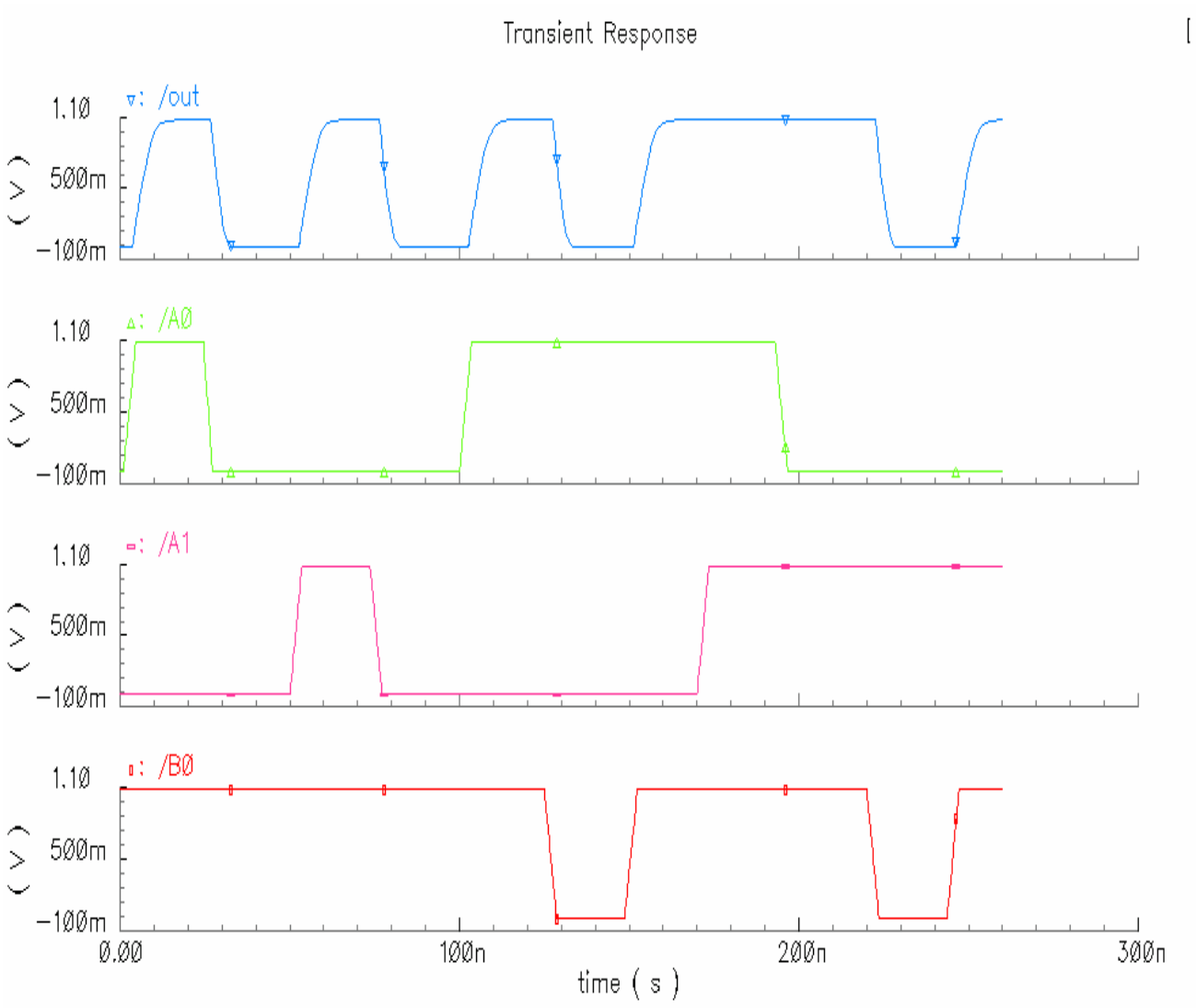


Figure 5.1 Waveform for OAI21

5.1.1.1 SPEED (50%Input to 50% Output)

Table 5.1 Delay 50% Input to 50% Output for OAI21 at SS, 0.96V, 125^{o}C

Delays	OLD	NEW	%change
A0(f) to Y(f)	2.45ns	2.71ns	10.6%
B0(f)_A0(1) to Y(f)	2.35ns	2.58ns	9.78%
B0(f)_A1(1) to Y(f)	2.45ns	2.68ns	**9.38%**
A1(f) to Y(f)	2.65ns	2.91ns	9.8%
A0(r) to Y(r)	3.47ns	3.75ns	8.06%
B0(r)_A0(1) to Y(r)	3.39ns	3.699ns	9.11%
B0(r)_A1(1) to Y(r)	3.41ns	3.69ns	8.21%
A1(r) to Y(r)	3.52ns	3.79ns	7.67%

5.1.1.2 SPEED (50%Input to 90% Output)

Table 5.2 Delay 50% Input to 90% Output for OAI21 at SS, 0.96V, 125^{o}C

Delays	OLD	NEW	%change
A0(f) to Y(f)	1.11ns	1.168ns	5.2%
B0(f)_A0(1) to Y(f)	1.02ns	1.04ns	1.9%
B0(f)_A1(1) to Y(f)	1.12ns	1.14ns	1.8%
A1(f) to Y(f)	1.31ns	1.37ns	4.6%
A0(r) to Y(r)	6.79ns	7.41ns	9.1%
B0(r)_A0(1) to Y(r)	6.695ns	7.34ns	9.7%
B0(r)_A1(1) to Y(r)	6.694ns	7.35ns	9.7%
A1(r) to Y(r)	6.82ns	7.46ns	9.3%

5.1.1.3 SLEW RATE (10% Input to 90% Output)

Table 5.3 Delay 10% Output to 90% Output for OAI21 at SS, 0.96V, 125^{o}C

Output(Y)	OLD	NEW	%Change
Rise	5.496 ns	6.075 ns	10.5%
Fall	3.347 ns	3.902 ns	11.5%

5.1.2 LEAKAGE CURRENT

Table 5.4 Leakage Current for OAI21 at FF, 1.44V, 125C

Inputs (A0 A1 B0)	OLD (nAmp.)	NEW (nAmp.)		X_change	
		Without Bias	With Bias	Without Bias	With Bias
000	1.944	1.738	0.212	1.11x	9.16x
001	2.603	2.39	0.344	1.08x	7.55x
010	2.42	2.21	0.308	1.09x	7.85x
011	2.62	2.50	0.360	1.04x	7.27x
100	2.42	2.21	0.308	1.09x	7.85x
101	2.87	2.72	0.396	1.05x	7.24x
110	2.41	2.20	0.302	1.09x	7.96x
111	1.91	1.836	0.271	1.04x	7.04x

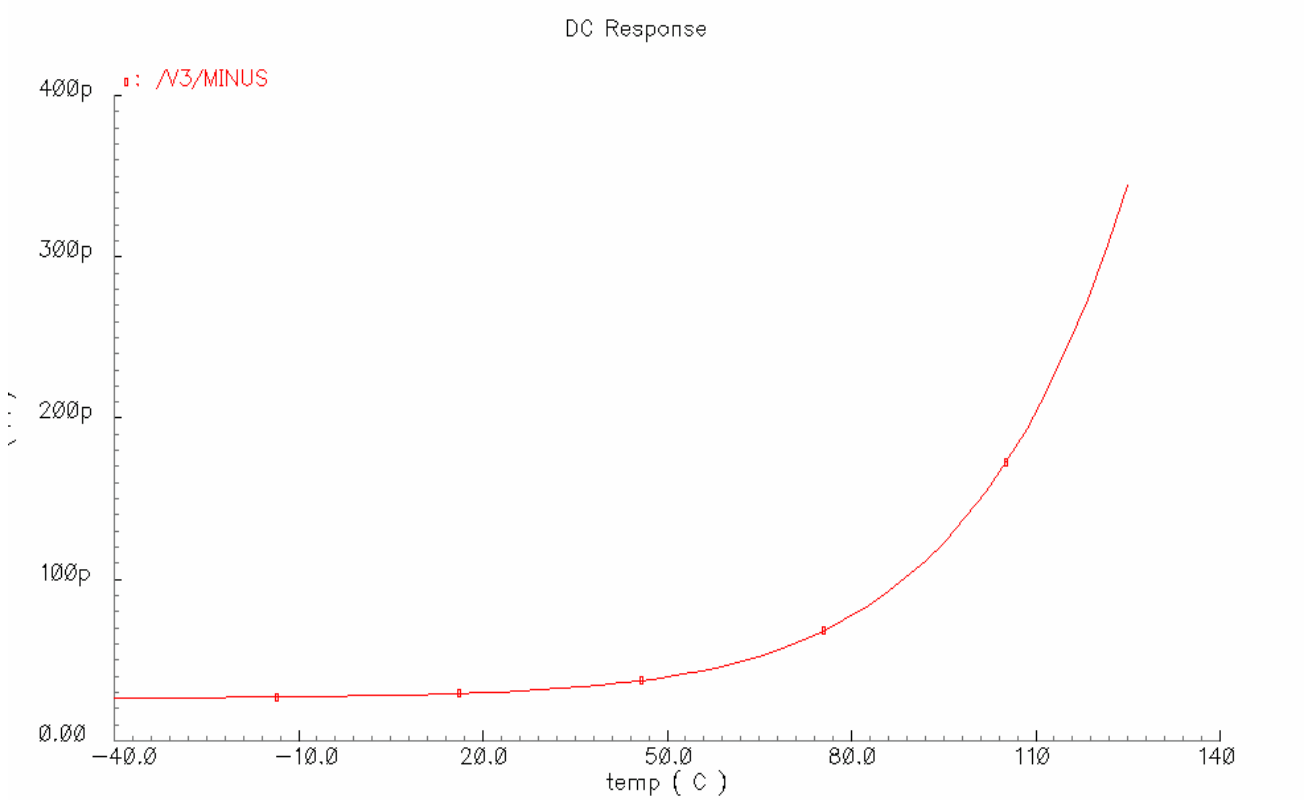


Figure 5.2 Leakage v/s Temperature for OAI21

5.1.3 DYNAMIC POWER (Maximum Load, Maximum Slope) Unit- uW/MHz

Table 5.5 Dynamic power for OAI21 at FF, 1.44V, -40C

Inputs	OLD	NEW	%Change
A0(r)_B0(r)_A1(r) to Y(r)	0.3752	0.374	0.32%
A0(f)_B0(f)_A1(f) to Y(f)	0.3754	0.375	0.1%

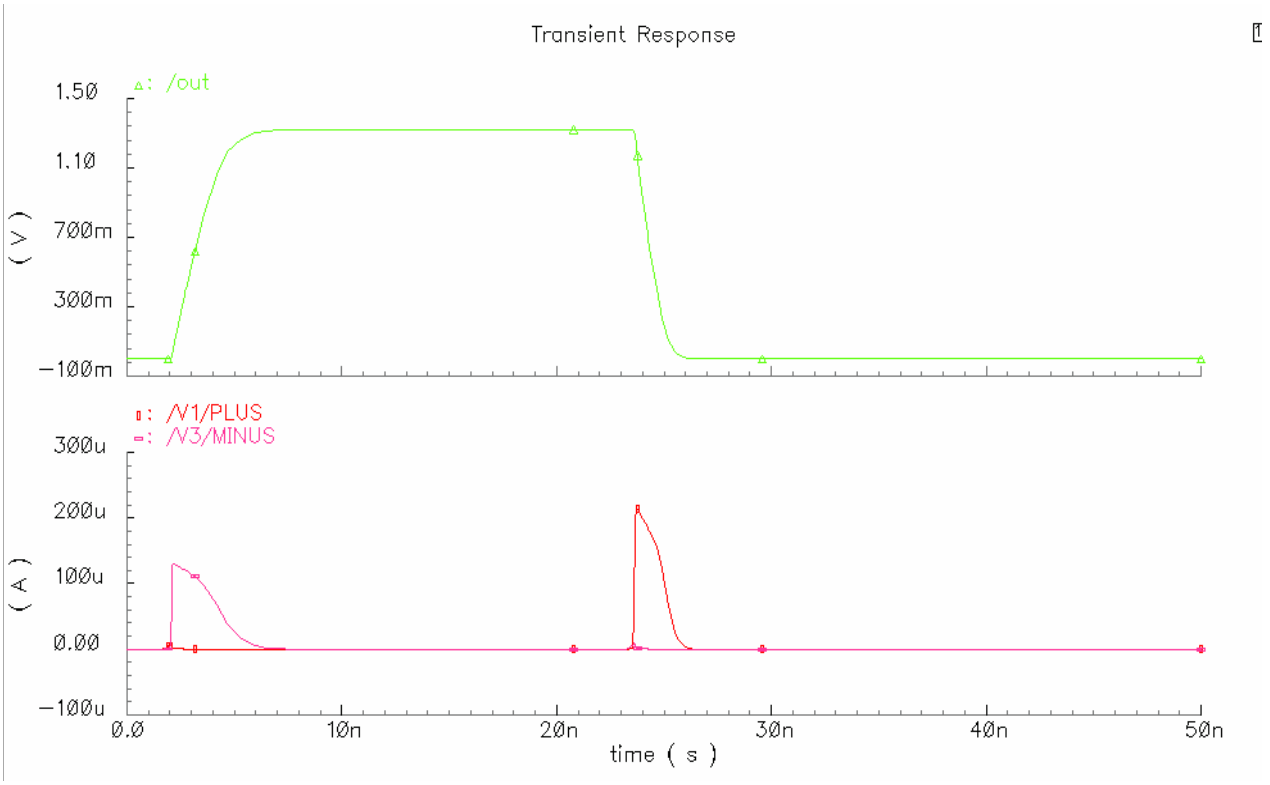


Figure 5.3 Dynamic Current for OAI21 at FF, 1.44V, -40C

5.1.4 DYNAMIC CURRENT (Maximum Load, Maximum Slope) Unit- uA

Table 5.6 Dynamic current for OAI21 at FF, 1.44V, -40C

Inputs	OLD	NEW	%Change
A0(r)_B0(r)_A1(r)_B1(r) to Y(r)	5.69	5.68	0.17%
A0(f)_B0(f)_A1(f)_B1(f) to Y(f)	5.698	5.688	0.17%

5.2 OAI22

5.2.1 SPEED

5.2.1.1 SPEED (50%Input to 50% Output)

Table 5.7 Delay 50% Input to 50% Output for OAI22 at SS, 0.96V, 125^{o}C

Delays	OLD	NEW	%change
A0(f) to Y(f)	2.62ns	2.88ns	9.92
B0(f) to Y(f)	2.67ns	2.95ns	10.4
A1(f) to Y(f)	2.65ns	2.78ns	4.90
B1(f) to Y(f)	2.74ns	2.99ns	9.12
A0(r) to Y(r)	3.5ns	3.69ns	5.42
B0(r) to Y(r)	3.61ns	3.80ns	5.26
A1(r) to Y(r)	3.56ns	3.69ns	3.65
B1(r) to Y(r)	3.67ns	3.86ns	5.17

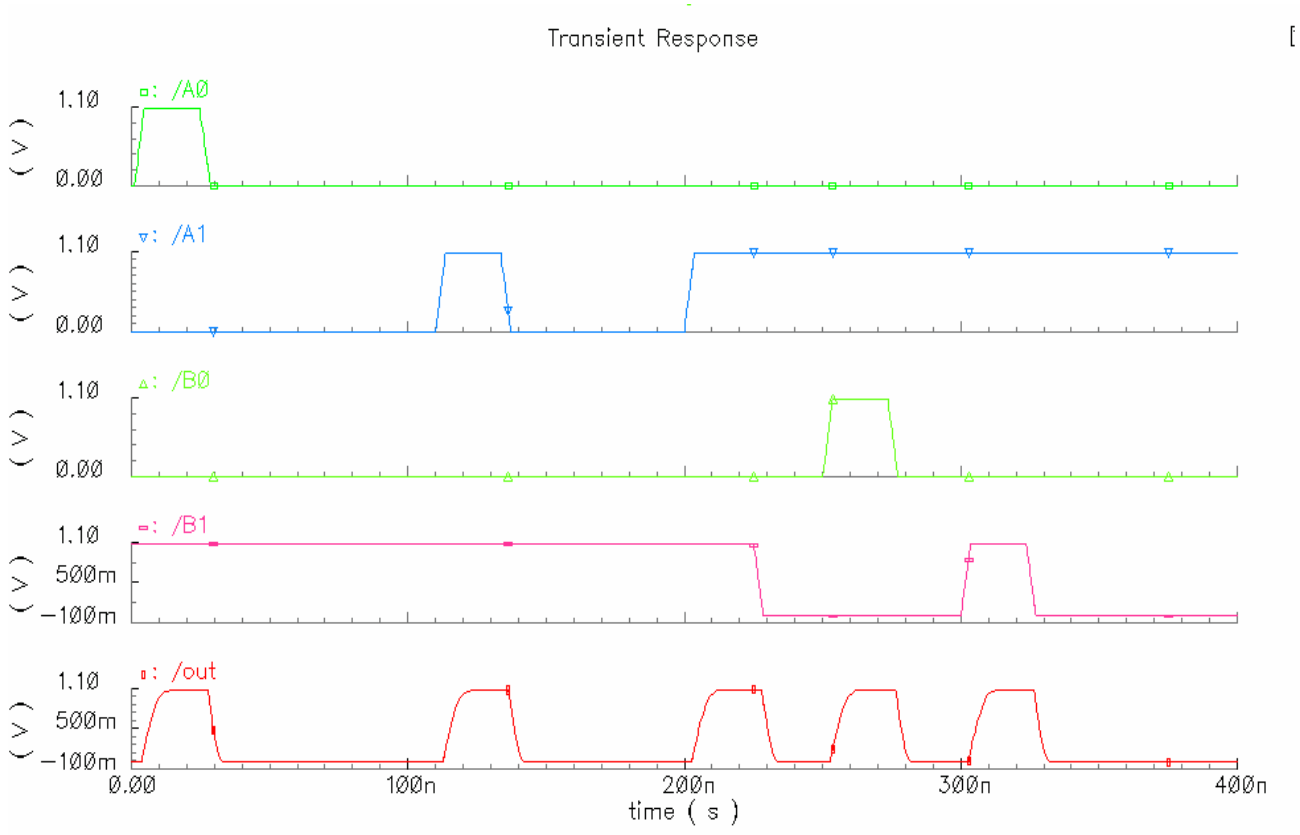


Figure 5.4 Waveform for OAI22

5.2.1.2 SPEED (50%Input to 90% Output)

Table 5.8 Delay 50% Input to 90% Output for OAI22 at SS, 0.96V, 125^{o}C

Delays	OLD	NEW	%change
A0(f) to Y(f)	1.285ns	1.39ns	8.2%
B0(f) to Y(f)	1.32ns	1.46ns	10.6%
A1(f) to Y(f)	1.31ns	1.39ns	6.1%
B1(f) to Y(f)	1.39ns	1.50ns	7.9%
A0(r) to Y(r)	6.72ns	7.31ns	8.6%
B0(r) to Y(r)	6.84ns	7.44ns	8.8%
A1(r) to Y(r)	6.87ns	7.40ns	7.7%
B1(r) to Y(r)	6.97ns	7.51ns	7.6%

5.2.1.3 SLEW RATE (10% Input to 90% Output)

Table 5.9 Delay 10% Output to 90% Output for OAI22 at SS, 0.96V, 125^{o}C

Output(Y)	OLD	NEW	%Change
Rise	5.435 ns	5.961 ns	9.6%
Fall	3.339 ns	3.686 ns	10.3%

5.2.2 LEAKAGE CURRENT

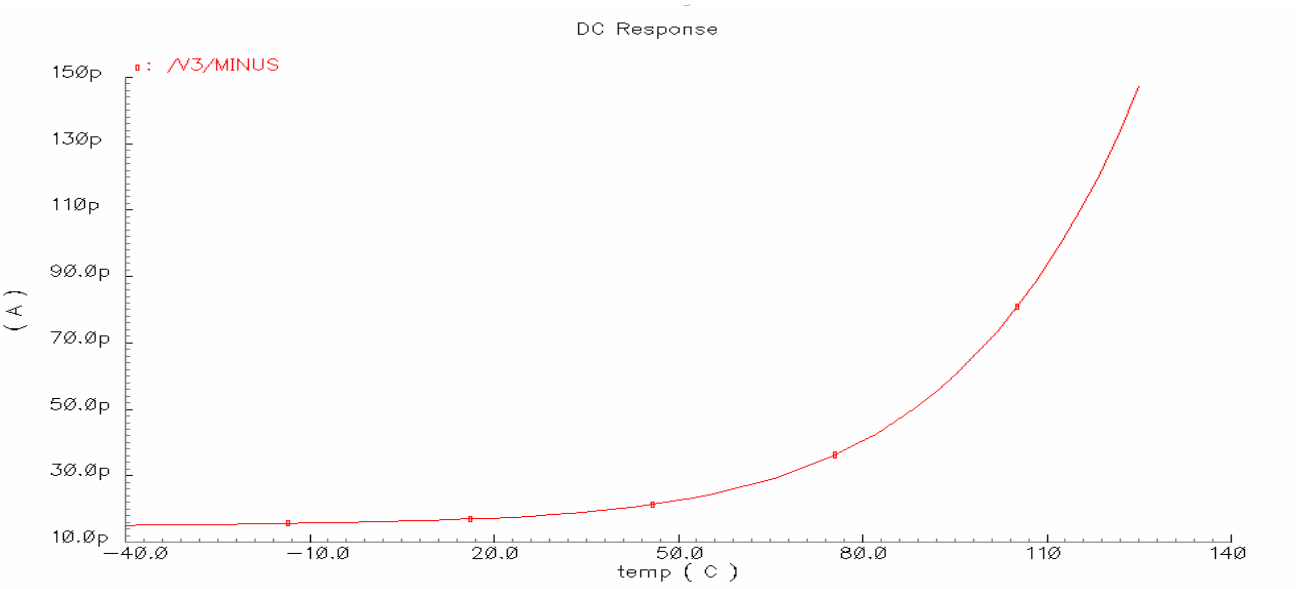


Figure 5.5 Leakage v/s Temperature for OAI22

Table 5.10 Leakage Current for OAI22 at FF, 1.44V, 125C

Input (A0 A1 B0 B1)	OLD (nAmp.)	NEW (nAmp.)		X_change	
		Without Bias	With Bias	Without Bias	With Bias
0000	1.971	1.722	0.224	1.14x	8.78x
0001	2.981	2.78	0.431	1.07x	6.92x
0010	2.981	2.78	0.431	1.07x	6.92x
0011	2.972	2.779	0.424	1.07x	6.99x
0100	2.619	2.423	0.357	1.08x	7.34x
0101	2.39	2.229	0.325	1.07x	7.34x
0110	2.68	2.45	0.361	1.09x	7.41x
0111	1.667	1.56	0.236	1.07x	7.06x
1000	2.619	2.423	0.357	1.08x	7.32x
1001	2.681	2.452	0.361	1.09x	7.42x
1010	2.97	2.675	0.397	1.11x	7.47x
1011	1.956	1.78	0.272	1.10x	7.19x
1100	2.642	2.449	0.357	1.08x	7.39x
1101	1.667	1.561	0.236	1.07x	7.05x
1110	1.956	1.784nA	0.272	1.09x	7.18x
1111	0.942	0.892nA	0.147	1.05x	6.40x

5.2.3 DYNAMIC POWER (Maximum Load, Maximum Slope) Unit- uW/MHz

Table 5.11 Dynamic power for OAI22 at FF, 1.44V, -40C

Inputs	OLD	NEW	%Change
A0(r)_B0(r)_A1(r)_B1(r) to Y(r)	0.3757	0.375	0.18%
A0(f)_B0(f)_A1(f)_B1(f) to Y(f)	0.3761	0.3754	0.18%

5.2.4 DYNAMIC CURRENT (Maximum Load, Maximum Slope) Unit- uA

Table 5.12 Dynamic leakage for OAI21 at FF, 1.44V, -40C

Inputs	OLD	NEW	%Change
A0(r)_B0(r)_A1(r)_B1(r) to Y(r)	5.69	5.68	0.17%
A0(f)_B0(f)_A1(f)_B1(f) to Y(f)	5.698	5.688	0.17%

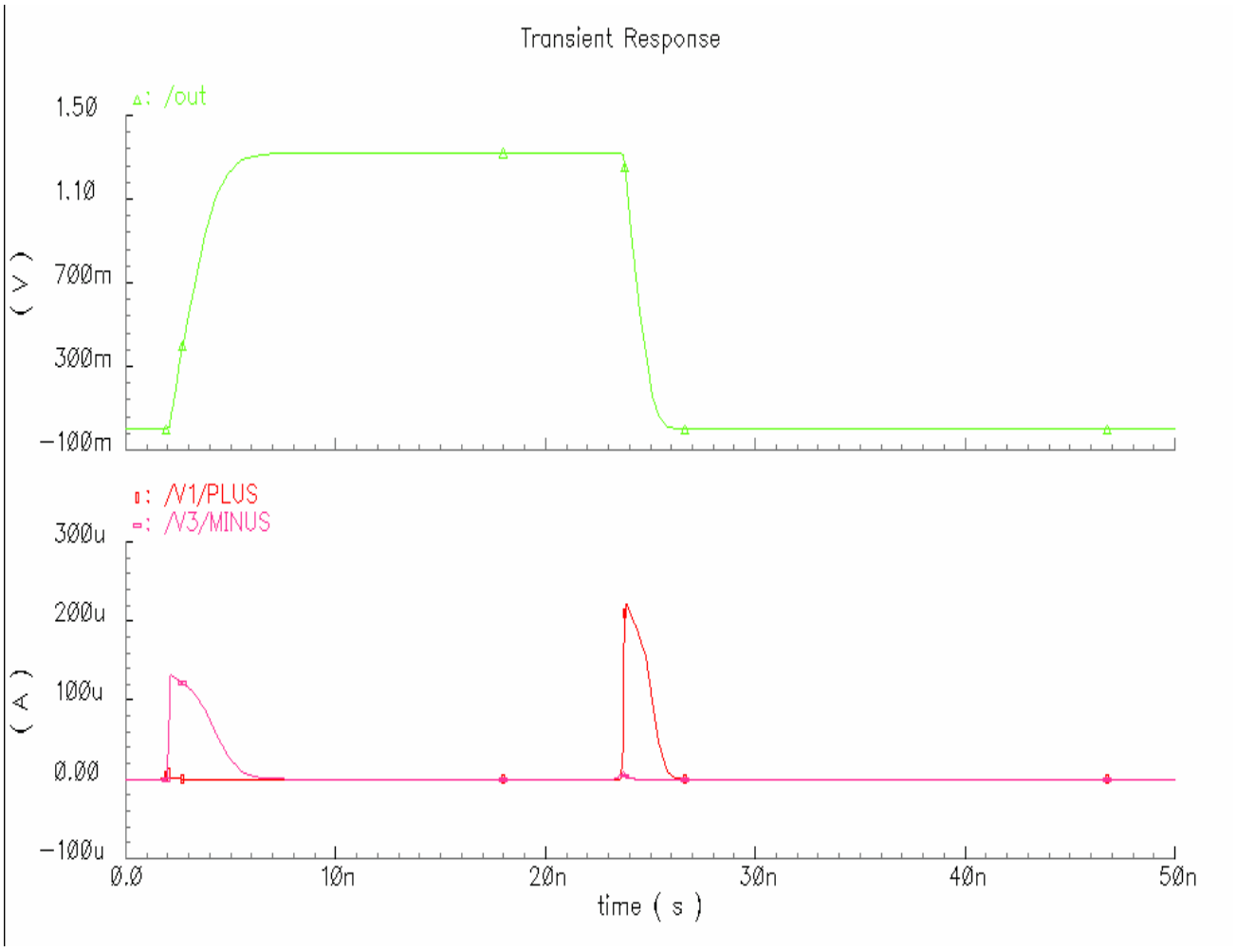


Figure 5.6 Dynamic Current for OAI22 at FF, 1.44V, -40C

5.3 OR2

5.3.1 SPEED

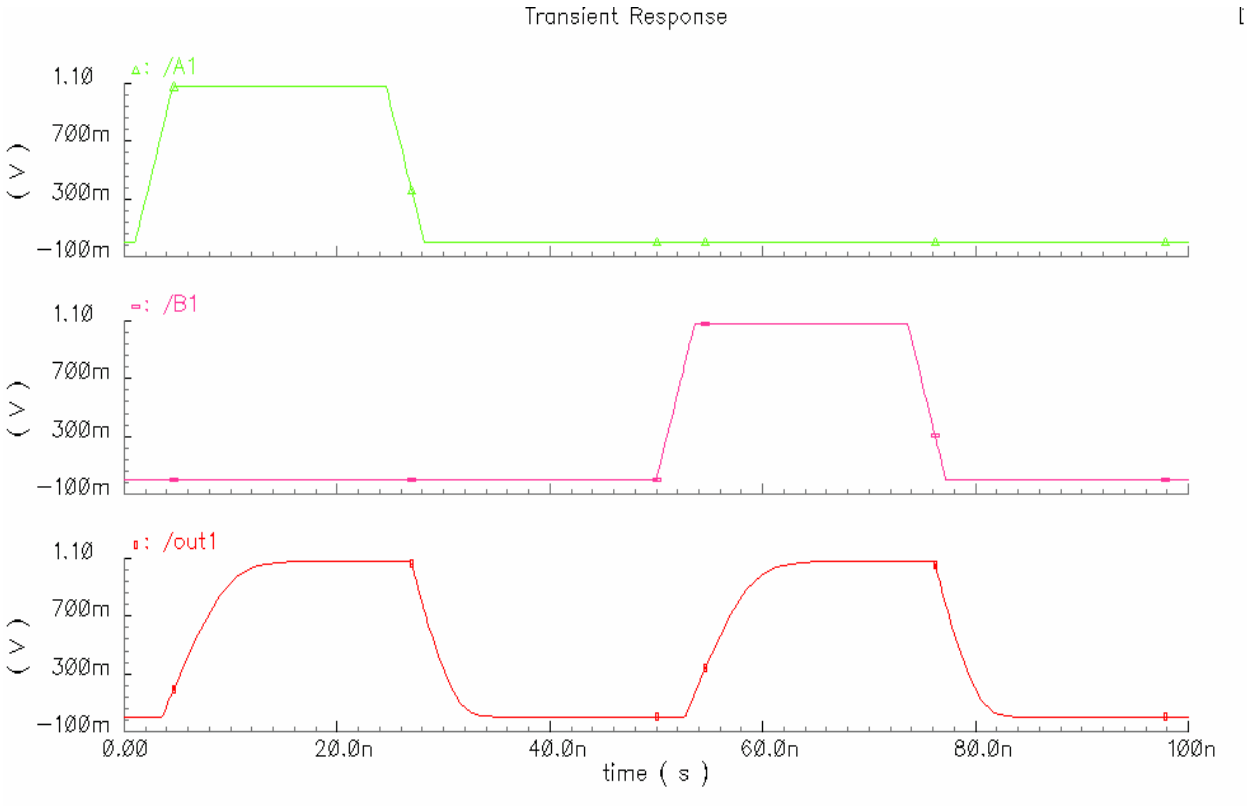


Figure 5.7 Waveform for OR2

5.3.1.1 SPEED (50%Input to 50% Output)

Table 5.13 Delay 50% Input to 50% Output for OR2 at SS, 0.96V, 125^{o}C

Delays	OLD	NEW	%change
A(f) to Y(f)	2.39n	2.59n	8.36
B(f) to Y(f)	2.54n	2.75n	8.26
A(r) to Y(r)	3.67n	3.93n	7.08
B(r) to Y(r)	3.76n	4.04n	7.44

5.3.1.2 SPEED (50%Input to 90% Output)

Table 5.14 Delay 50% Input to 90% Output for OR2 at SS, 0.96V, 125^{o}C

Delays	OLD	NEW	%change
A(f) to Y(f)	0.91n	0.93n	2.19
B(f) to Y(f)	1.07n	1.09n	1.86
A(r) to Y(r)	7.51n	7.83n	4.26
B(r) to Y(r)	7.22n	7.92n	9.69

5.3.1.3 SLEW RATE (10% Input to 90% Output)

Table 5.15 Delay 10% Output to 90% Output for OR2 at SS, 0.96V, 125^{o}C

Output(Y)	OLD	NEW	Difference	%Change
Rise	5.81n	6.44	0.63	10.84
Fall	3.73n	4.13n	0.4	10.72

5.3.2 LEAKAGE CURRENT

Table 5.16 Leakage Current for OR2 at FF, 1.44V, 125C

Inputs (A B)	OLD (nAmp.)	NEW (nAmp.)		X_Change	
		Without Bias	With Bias	Without Bias	With Bias
0 0	4.45	4.11	0.58	1.08	7.67
0 1	3.33	3.23	0.44	1.03	7.56
1 0	4.13	4.03	0.56	1.02	7.37
1 1	1.52	1.42	0.24	1.07	6.33

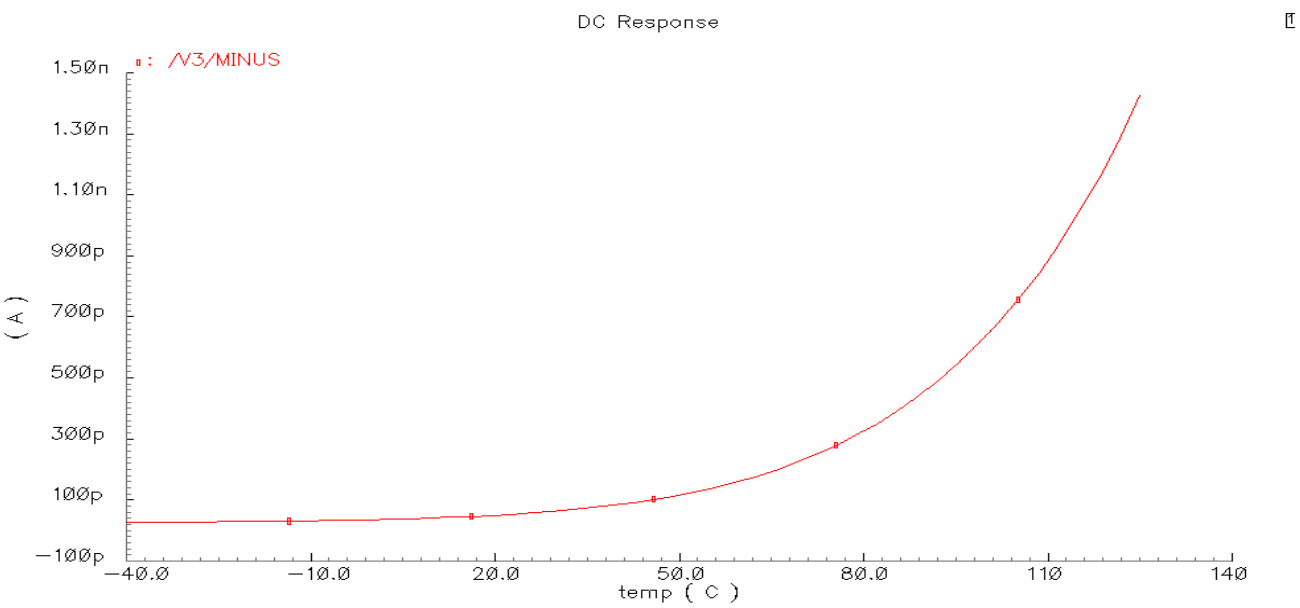


Figure 5.8 Leakage v/s Temperature for OR2

5.3.3 DYNAMIC POWER (Maximum Load, Maximum Slope) Unit- uW/MHz

Table 5.17 Dynamic power for OR2 at FF, 1.44V, -40C

Inputs	OLD	NEW	%Change
A(r)_B(r)_Y(r)	0.750	0.749	-0.1333
A(f)_B(f)_Y(f)	0.750	0.749	-0.1333

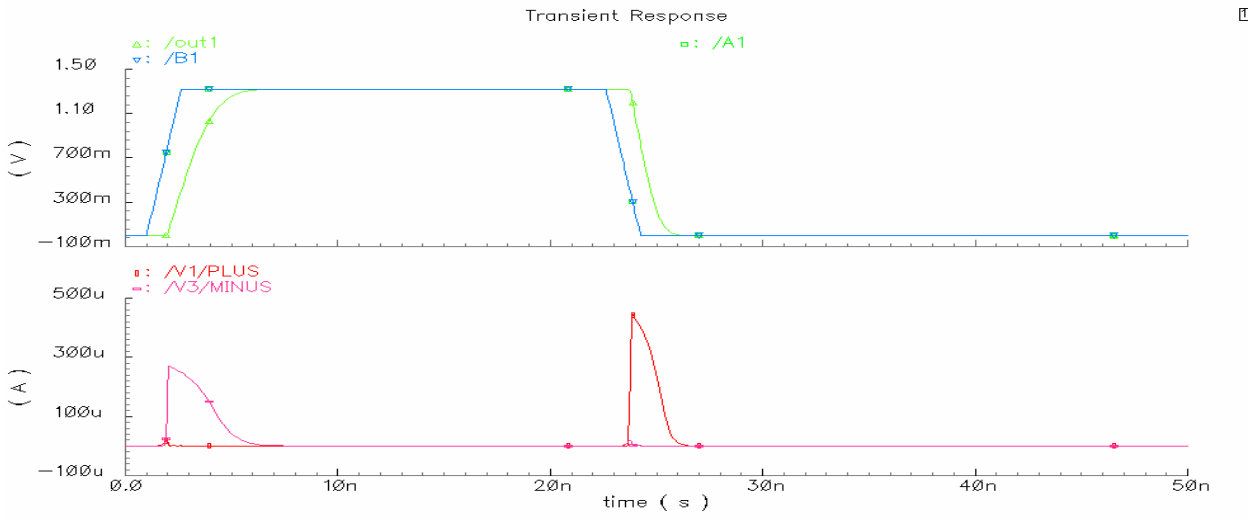


Figure 5.9 Dynamic Current for OR2 at FF, 1.44V, -40C

5.3.4 DYNAMIC CURRENT (Maximum Load, Maximum Slope) Unit- uA

Table 5.18 Dynamic current for OAI22 at FF, 1.44V, -40C

Inputs	OLD	NEW	%Change
A(r)_B(r)_Y(r)	11.37	11.36	-0.087
A(f)_B(f)_Y(f)	11.37	11.36	-0.087

5.4 NOR2

5.4.1 SPEED

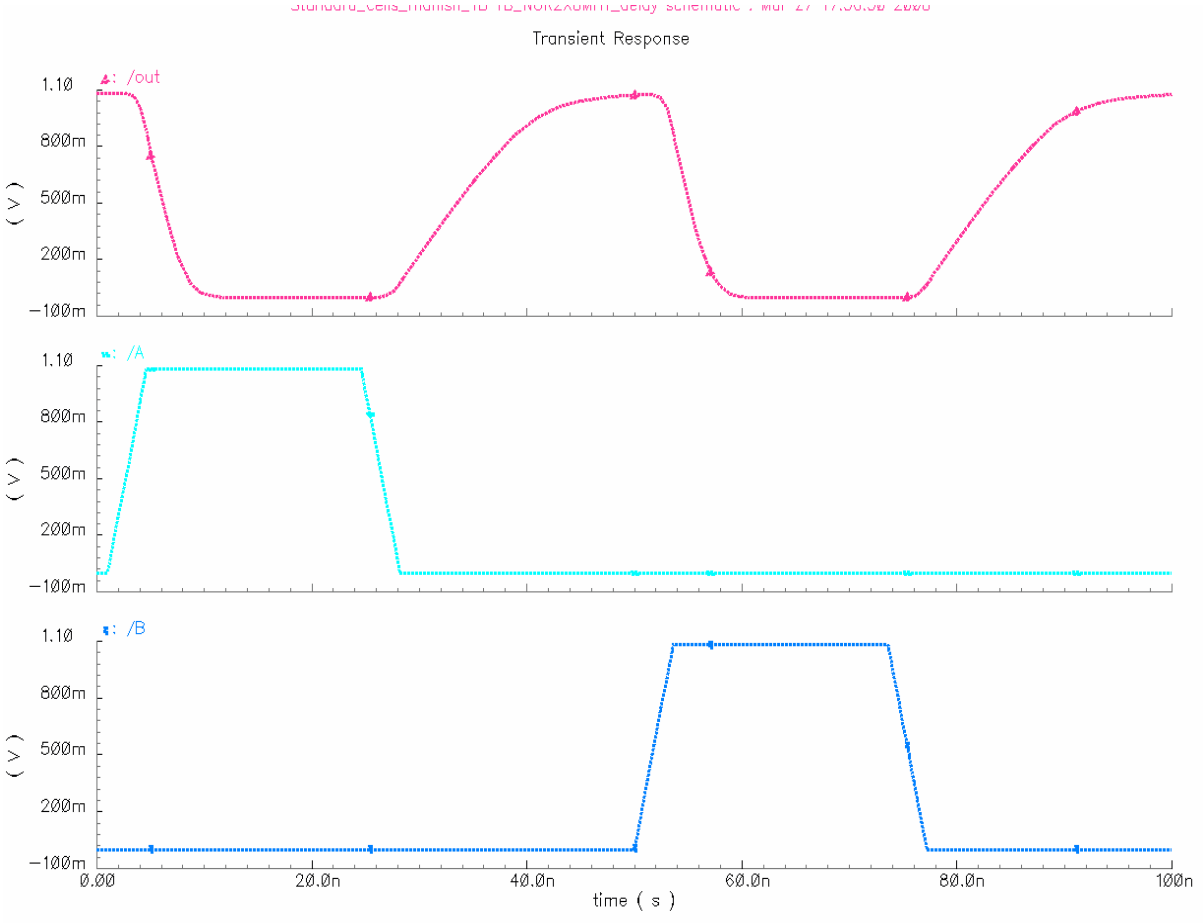


Figure 5.10 Waveform for NOR2

5.4.1.1 SPEED (50%Input to 50% Output)

Table 5.19 Delay 50% Input to 50% Output for NOR2 at SS, 0.96V, 125^{o}C

Delays	OLD	NEW	%change
A(r) to Y(f)	2.941	3.137	6.66
B(r) to Y(f)	2.948	3.121	5.86
A(f) to Y(r)	7.105	7.612	**7.13**
B(f) to Y(r)	7.092	7.685	8.36

5.4.1.2 SPEED (50%Input to 90% Output)

Table 5.20 Delay 50% Input to 90% Output for NOR2 at SS, 0.96V, 125^{o}C

Delays	OLD	NEW	%change
A(r) to Y(f)	1.35	1.399	3.62
B(r) to Y(f)	1.343	1.381	2.82
A(f) to Y(r)	13.96	15.2	8.88
B(f) to Y(r)	14.08	15.28	8.52

5.4.1.3 SLEW RATE (10% Input to 90% Output)

Table 5.21 Delay 10% Output to 90% Output for NOR2 at SS, 0.96V, 125^{o}C

OUTPUT(Y)	OLD	NEW	%Change
Rise	11.9	13.03	9.49
Fall	3.84	4.231	10.18

5.4.2 LEAKAGE CURRENT

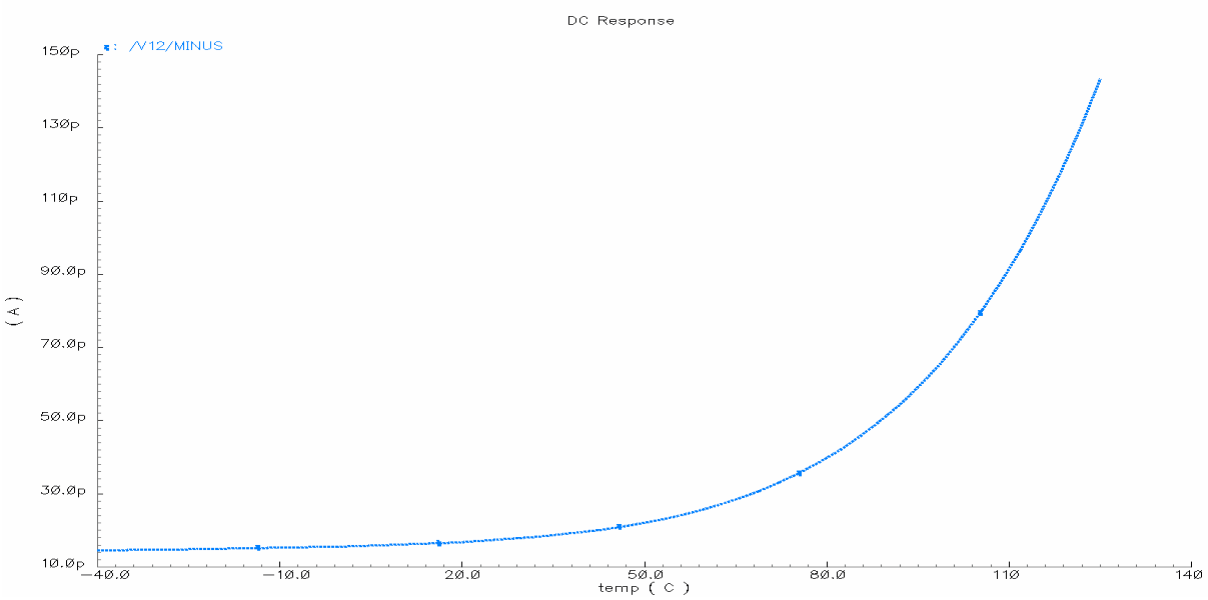


Figure 5.11 Leakage v/s Temperature for NOR2

Table 5.22 Leakage Current for NOR2 at FF, 1.44V, 125C

Input (A B)	OLD	NEW		X_Change	
		Without Bias	With Bias	Without Bias	With Bias
00	**3.472**	**3.22**	**0.660**	**1.07x**	**5.26x**
01	**3.81**	**3.459**	**0.353**	**1.10x**	**10.79x**
10	**5.273**	**4.761**	**0.543**	**1.10x**	**9.71x**
11	**0.624**	**0.572**	**0.040**	**1.09x**	**15.6x**

5.4.3 DYNAMIC POWER (Maximum Load, Maximum Slope) Unit- uW/MHz

Table 5.23 Dynamic power for NOR2 at FF, 1.44V, -40C

Inputs	OLD	NEW	%Change
A(f)_B(f)_y(r)	1.1167	1.11619	0.04
A(r)_B(r)_y(f)	1.1167	1.11619	0.04

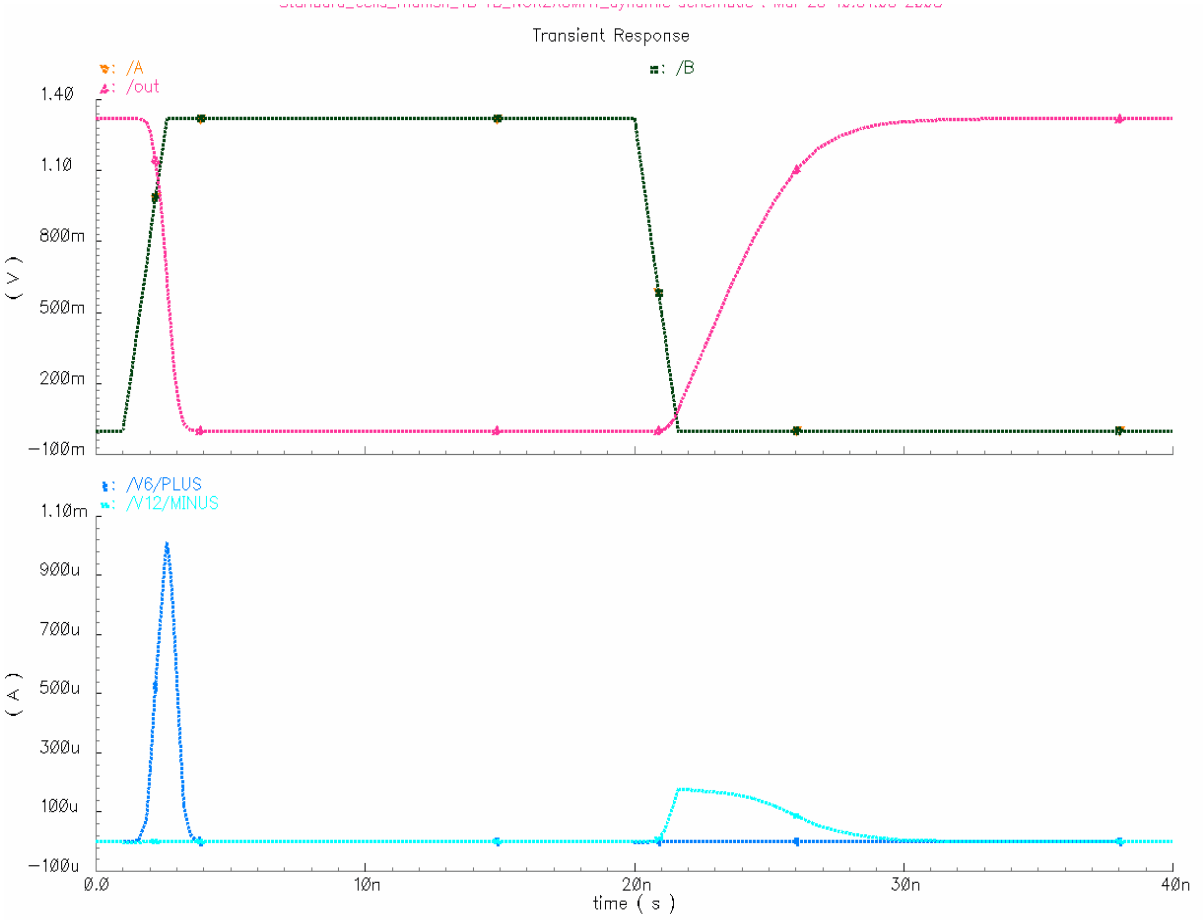


Figure 5.12 Dynamic Current for NOR2 at FF, 1.44V, -40C

5.4.4 DYNAMIC CURRENT (Maximum Load, Maximum Slope) Unit- uA

Table 5.24 Dynamic current for NOR2 at FF, 1.44V, -40C

Inputs	OLD	NEW	X_Change
A(f)_B(f)_y(r)	21.15	21.14	1.00x
A(r)_B(r)_y(f)	21.15	21.14	1.00x

5.5 XNOR3

5.5.1 SPEED

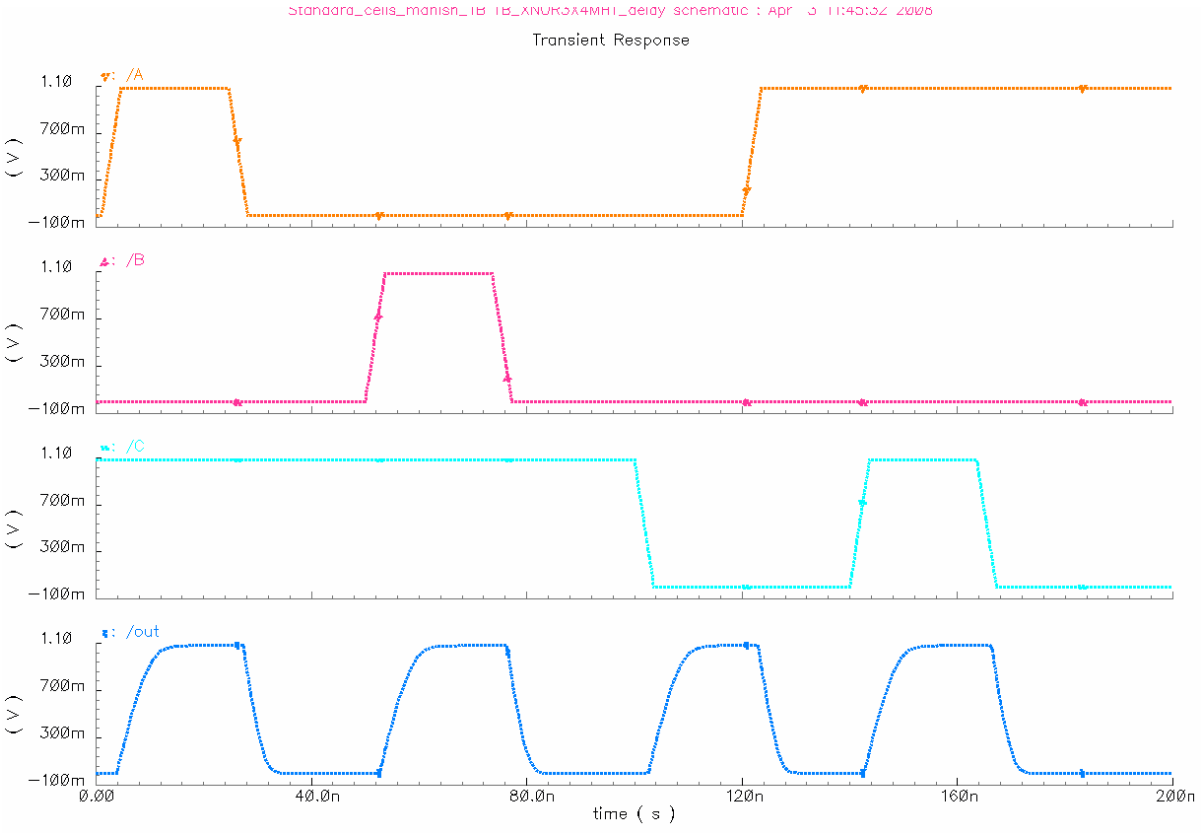


Figure 5.13 Waveform for XNOR3

5.5.1.2 SPEED (50%Input to 90% Output)

Table 5.26 Delay 50% Input to 90% Output for XNOR3 at SS, 0.96V, 125^{o}C

Delays	OLD	NEW	%change
A(f)_Y(f)	1.28	1.304	1.87
B(f)_Y(f)	1.254	1.25	-0.31
C(f)_Y(f)	1.238	1.277	**3.15**
A(r)_Y(r)	7.244	7.933	9.51
B(r)_Y(r)	7.133	7.71	8.08
C(r)_Y(r)	7.088	7.632	7.67

5.5.1.3 SLEW RATE (10% Input to 90% Output)

Table 5.27 Delay 10% Output to 90% Output for XNOR3 at SS, 0.96V, 125^{o}C

OUTPUT(Y)	OLD	NEW	%Change
Rise	5.702	6.332	11.04
Fall	3.598	3.926	9.11

5.5.2 LEAKAGE CURRENT

Table 5.28 Leakage Current for XNOR3 at FF, 1.44V, 125C

Inputs (A B C)	OLD	NEW		X_Change	
		Without Bias	With Bias	Without Bias	With Bias
000	10.36	10.09	1.688	1.02	6.13
001	13.17	12.8	1.85	1.02	7.11
010	15.25	14.18	1.912	1.07	7.97
011	13.4	12.76	1.8	1.05	7.44
100	14.82	13.34	1.887	1.11	7.85
101	12.97	11.92	1.775	1.08	7.30
110	10.9	10.21	1.684	1.06	6.47
111	13.7	12.92	1.846	1.06	7.42

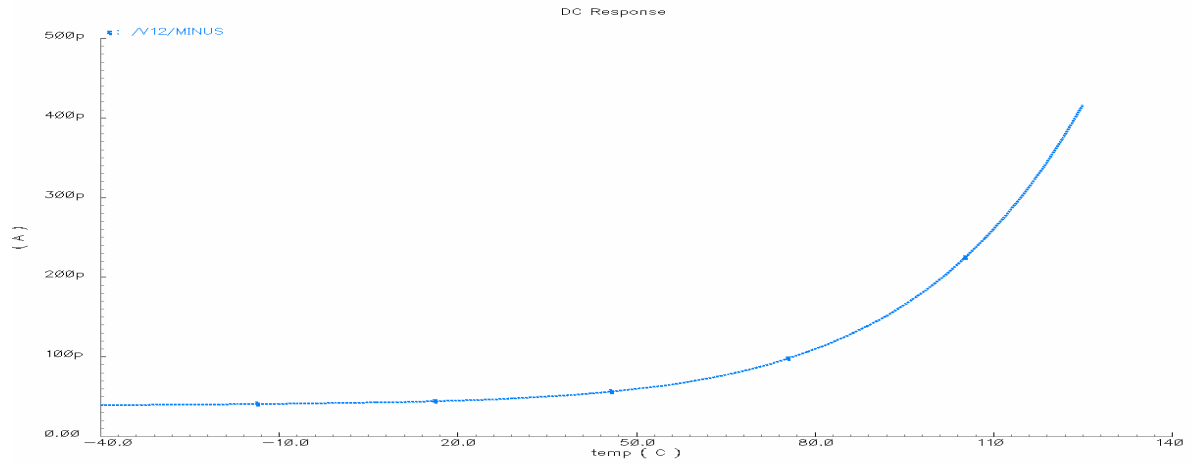


Figure 5.14 Leakage v/s Temperature for XNOR3

5.5.3 DYNAMIC POWER (Maximum Load, Maximum Slope) Unit- uW/MHz

Table 5.29 Dynamic power for XNOR3 at FF, 1.44V, -40C

Inputs	OLD	NEW	%Change
A(f)_B(f)_C(f)_y(f)	0.7687	0.7661	0.0033
A(r)_B(r)_C(r)_y(r)	0.7687	0.7661	0.0033

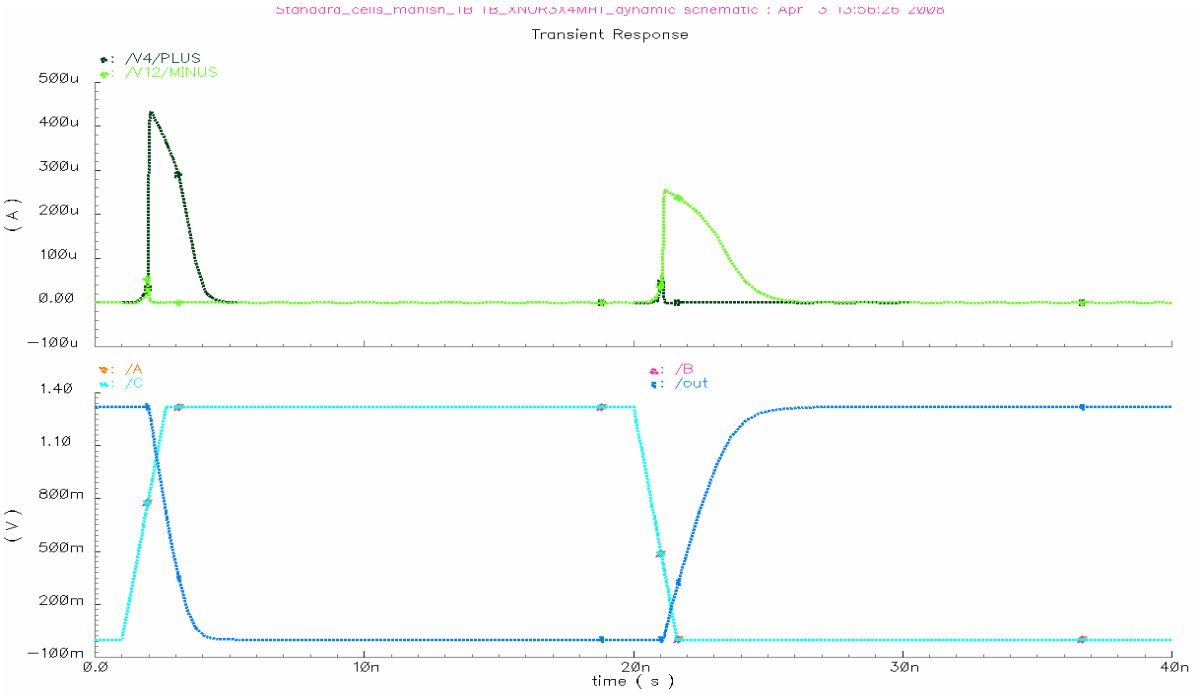


Figure 5.15 Dynamic Current for XNOR3 at FF, 1.44V, -40C

5.5.4 DYNAMIC CURRENT (Maximum Load, Maximum Slope) Unit- uA

Table 5.30 Dynamic current for XNOR3 at FF, 1.44V, -40C

Inputs	OLD	NEW	X_Change
A(f)_B(f)_C(f)_y(f)	14.56	14.51	1.00x
A(r)_B(r)_C(r)_y(r)	14.56	14.51	1.00x

5.6 MX2

5.6.1 SPEED

5.6.1.1 SPEED (50% Input to 50% Output)

Table 5.31 Delay 50% Input to 50% Output for MX2 at SS, 0.96V, 125^{o}C

Delays	OLD	NEW	%change
S0(f) to Y(f)	2.42	2.59	7.02
A(f) to Y(f)	2.60	2.82	8.46
B(f) to Y(f)	2.60	2.83	8.84
S0(r) to Y(r)	3.52	3.81	8.23
A(r) to Y(r)	3.69	4.03	9.21
B(r) to Y(r)	3.68	4.04	9.78

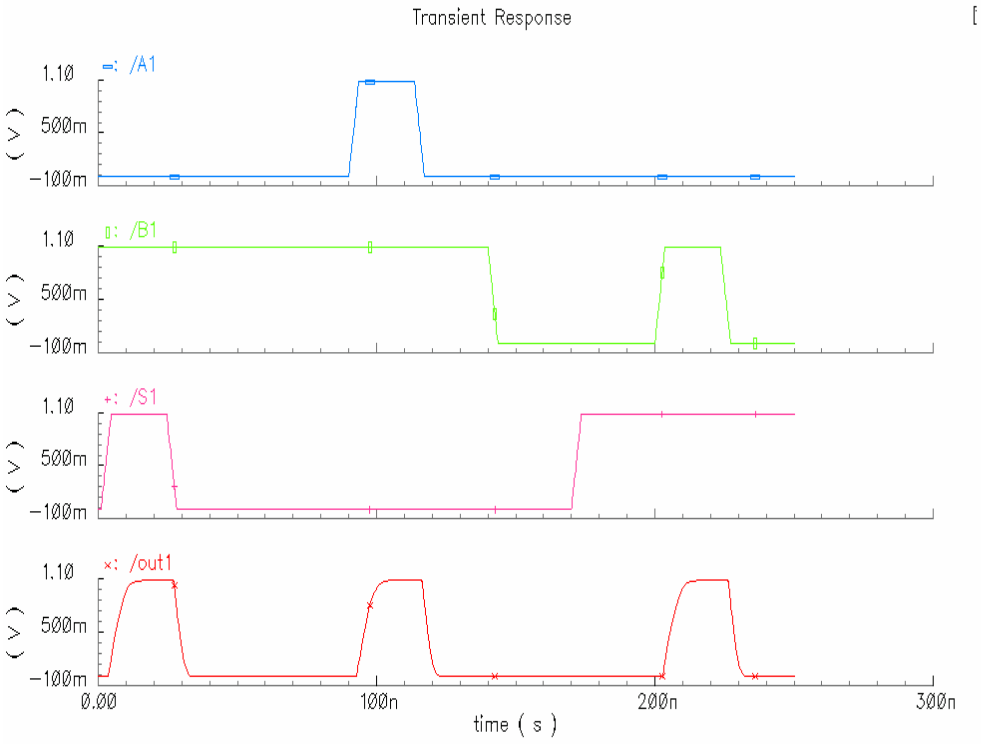


Figure 5.16 Waveform for MX2

5.6.1.2 SPEED (50%Input to 90% Output)

Table 5.32 Delay 50% Input to 90% Output for MX2 at SS, 0.96V, 125^{o}C

Delays	OLD	NEW	%change
S0(f) to Y(f)	1.05	1.08	2.66
A(f) to Y(f)	1.24	1.32	6.45
B(f) to Y(f)	1.25	1.33	6.4
S0(r) to Y(r)	6.87	7.58	10.33
A(r) to Y(r)	7.09	7.79	9.87
B(r) to Y(r)	7.03	7.79	10.81

5.6.1.3 SLEW RATE (10% Input to 90% Output)

Table 5.33 Delay 10% Output to 90% Output for MX2 at SS, 0.96V, 125^{o}C

Output(Y)	OLD	NEW	%Change
Rise	5.59	6.16	10.05
Fall	3.42	3.79	10.81

5.6.2 LEAKAGE CURRENT

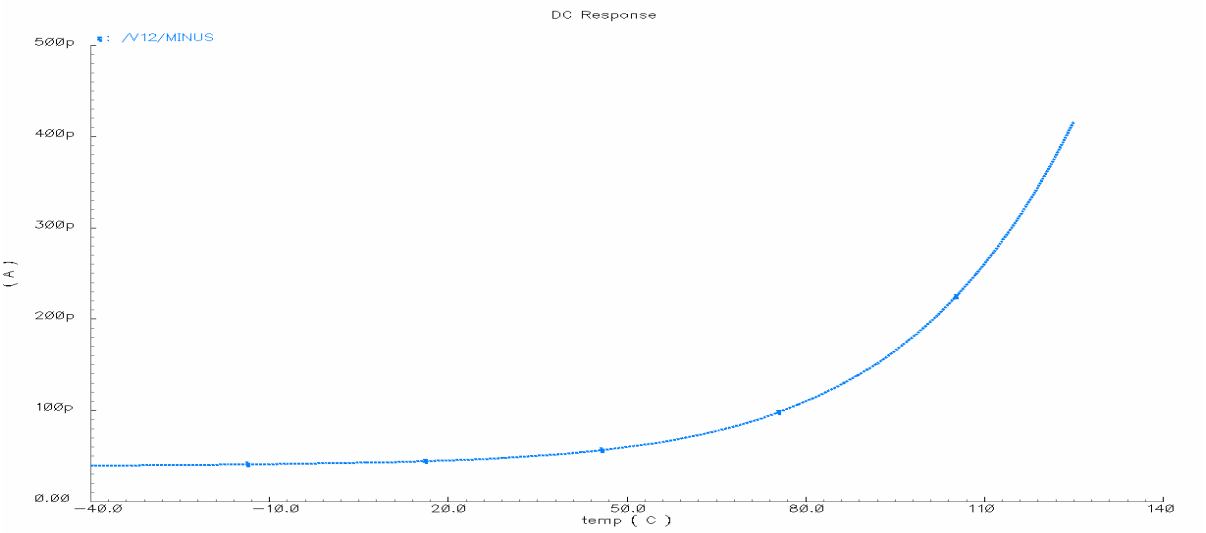


Figure 5.17 Leakage v/s Temperature for MX2

Table 5.34 Leakage Current for MX2 at FF, 1.44V, 125C

Inputs (A B S0)	OLD (nAmp.)	NEW (nAmp.)		X_Change	
		Without Bias	With Bias	Without Bias	With Bias
0 0 0	4.55	4.08	0.65	1.11	7.0
0 0 1	5.15	4.69	0.66	1.09	7.80
0 1 0	8.02	7.38	0.99	1.08	8.10
0 1 1	7.05	6.62	0.94	1.06	7.5
1 0 0	6.46	6.03	0.93	1.07	6.94
1 0 1	8.62	7.98	1.00	1.08	8.62
1 1 0	5.28	4.68	0.70	1.12	7.54
1 1 1	5.87	5.28	0.70	1.11	8.38

5.6.3 DYNAMIC POWER (Maximum Load, Maximum Slope) Unit- uW/MHz

Table 5.35 Dynamic power for MX2 at FF, 1.44V, -40C

Inputs	OLD	NEW	%Change
A(r)_B(r)_S(r)_Y(r)	0.571	0.570	-0.175
A(f)_B(f)_S(f)_Y(f)	0.571	0.570	-0.175

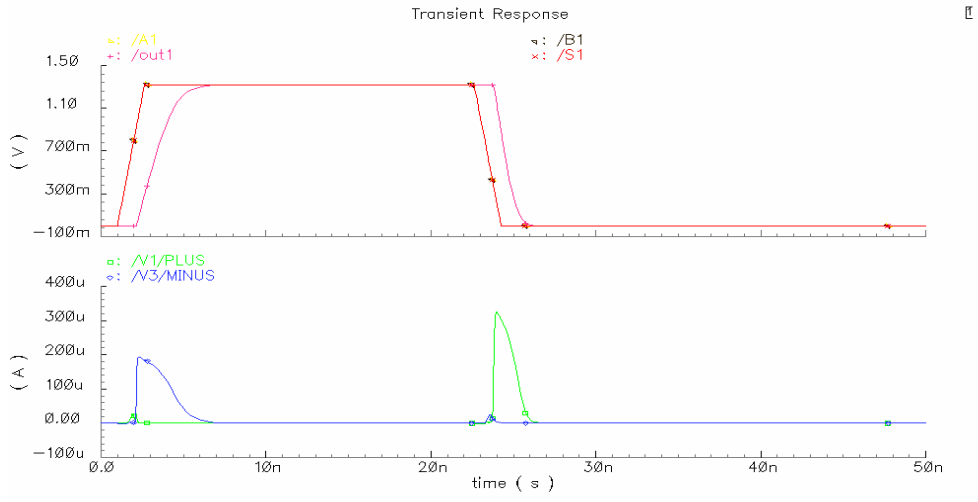


Figure 5.18 Dynamic Current for MX2 at FF, 1.44V, -40C

5.6.4 DYNAMIC CURRENT (Maximum Load, Maximum Slope) Unit- uA

Table 5.36 Dynamic leakage for MX2 at FF, 1.44V, -40C

Inputs	OLD	NEW	%Change
A(r)_B(r)_S(r)_Y(r)	8.665	8.645	-0.23
A(f)_B(f)_S(f)_Y(f)	8.666	8.646	-0.23

5.7 TLAT

Table 5.37 Slope Value for TLAT

Clk Slope(ns)	Signal Slope(ns)
0.08	1.33
1.32	2.77

5.7.1 SETUP TIME & HOLD TIME

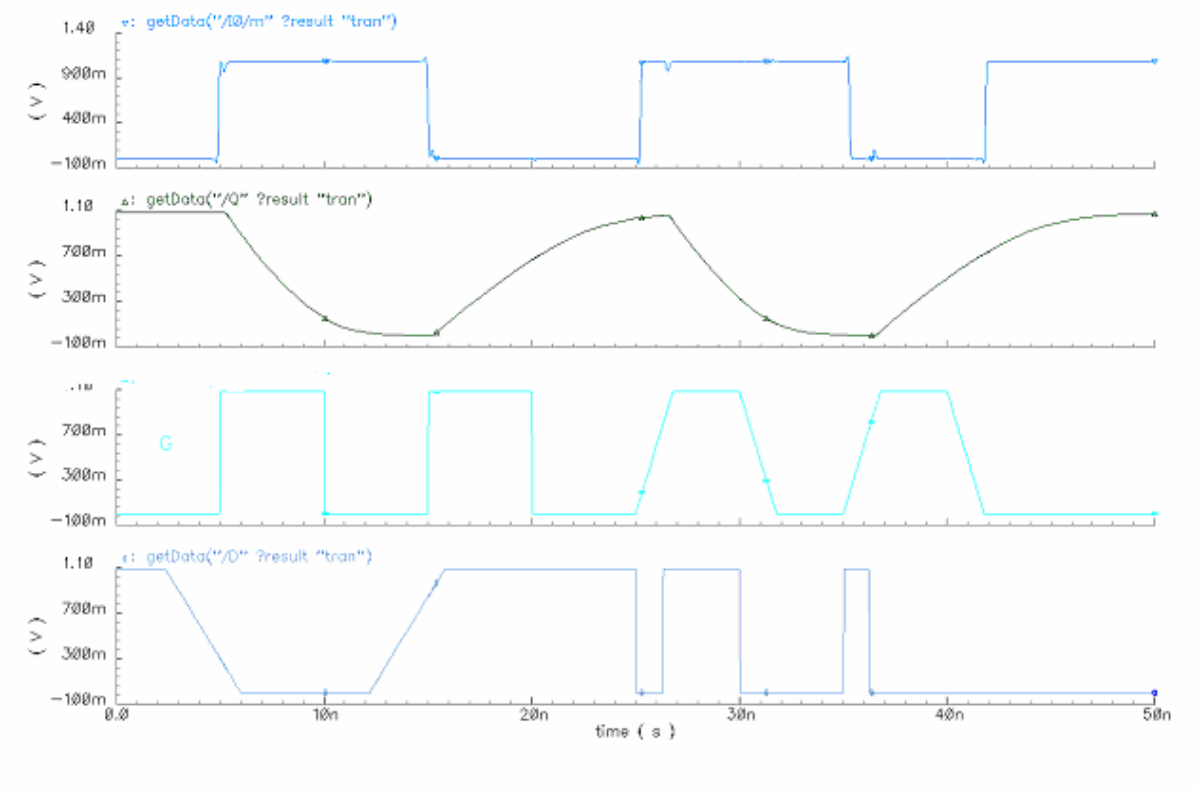


Figure 5.19 Waveform for Setup and Hold Time of TLAT

5.7.1.1 SETUP TIME

Table 5.38 Setup Time for TLAT at SS, 0.96V, 125°C

Setup Time	Old(ns)	New(ns)	% Change
G(r) to D(r)	0.2617	0.2	-23
G(r) to D(f)	0.1	0.15	50

5.7.1.2 HOLD TIME

Table 5.39 Hold Time for TLAT at SS, 0.96V, 125°C

Hold Time	Old(ns)	New(ns)	% Change
G(r) to D(r)	0.02	0.03	50
G(r) to D(f)	0.11	0.12	8.1

5.7.2 CLK TO Q DELAY (50%Input to 50% Output)

Table 5.40 Delay 50% Input to 50% Output for TLAT at SS, 0.96V, 125°C

G to Q delay	Old (ns)	New (ns)	% Change
G(r) to Q(r)	3.145	3.18	1.1
G(r) to Q(f)	2.087	2.119	1.5

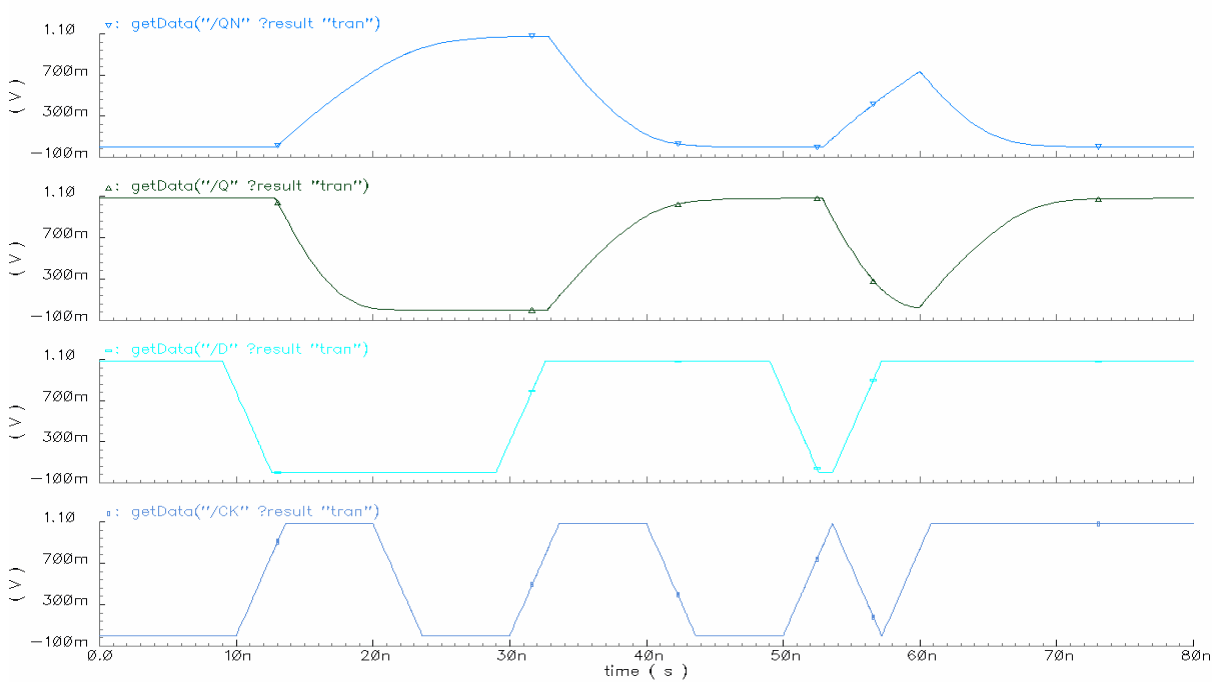


Figure 5.20 Waveform for TLAT

5.7.3 LEAKAGE CURRENT

Table 5.41 Leakage Current for TLAT at FF, 1.44V, 125C

D G	Old(nA)	New(nA)	X Change
0 0	5.637	0.704	8
0 1	10.10	1.32	7.6
10	28.12	4.68	6
1 1	6.34	0.792	8

5.7.4 DYNAMIC CURRENT (Maximum Load, Maximum Slope) Unit- uW/MHz

Table 5.42 Dynamic current for TLAT at FF, 1.44V, -40C

Input	Old	New	X Change
G= L-H D= L-H	11.22	10.91	1.02
G= H-L D= H-L	14.13	12.31	1.147

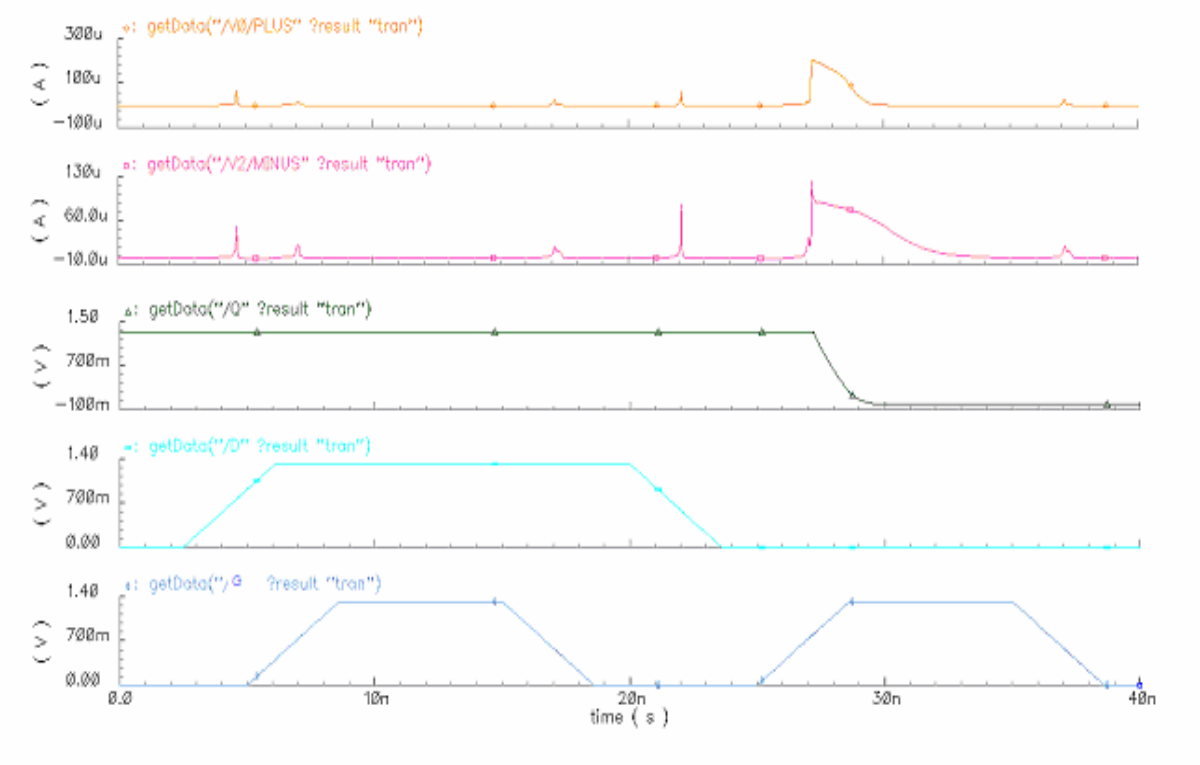


Figure 5.21 Dynamic Current for TLAT at FF, 1.44V, -40C

5.8 DFFHQ

Table 5.43 Slope Value for DFFHQ

Clk Slope(ns)	Signal Slope(ns)
0.08	1.33
1.32	2.77

5.8.1 SETUP TIME & HOLD TIME

5.8.1.1 SETUP TIME

Table 5.44 Setup Time for DFFHQ at SS, 0.96V, 125^{o}C

Setup Time	Old(ns)	New (ns)	% Change
CLK(r) to D(r)	1.21	1.3	6.92
CLK(r) to D(f)	0.456	0.755	39.60

5.8.1.2 HOLD TIME

Table 5.45 Hold Time for DFFHQ at SS, 0.96V, 125^{o}C

Hold Time	Old (ns)	New (ns)	% Change
CLK(r) to D(r)	0.035	0.04	12.5
CLK(r) to D(f)	0.065	0.09	27.77

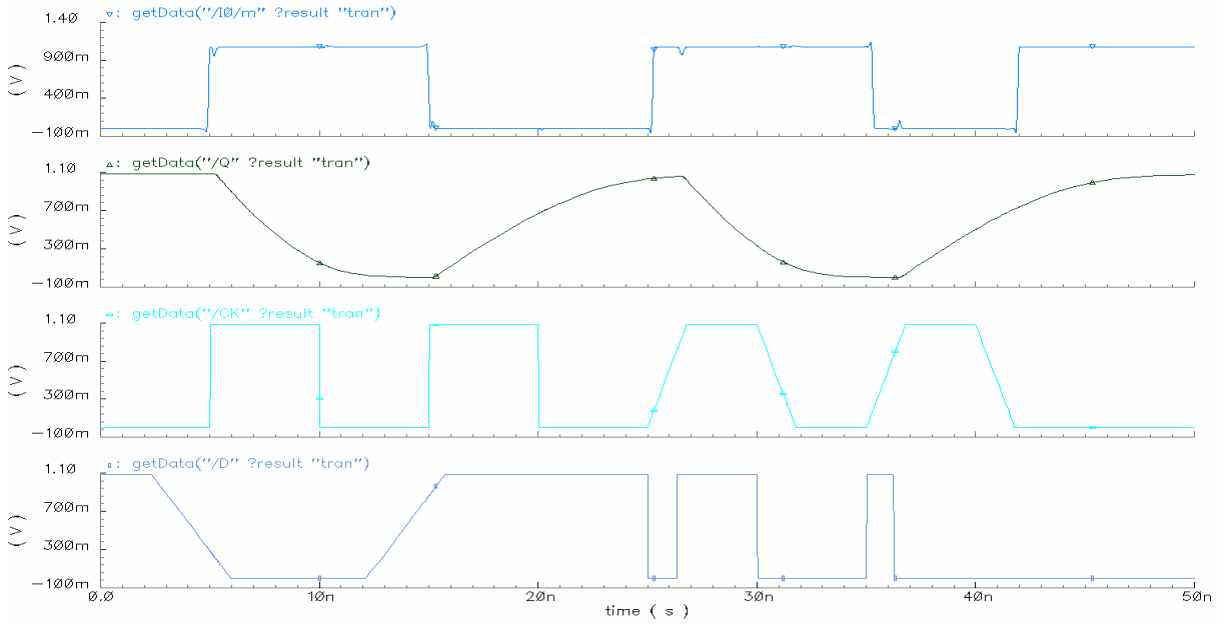


Figure 5.22 Waveform for Setup and Hold Time of DFFHQ

5.8.2 CLK TO Q DELAY (50%Input to 50% Output)

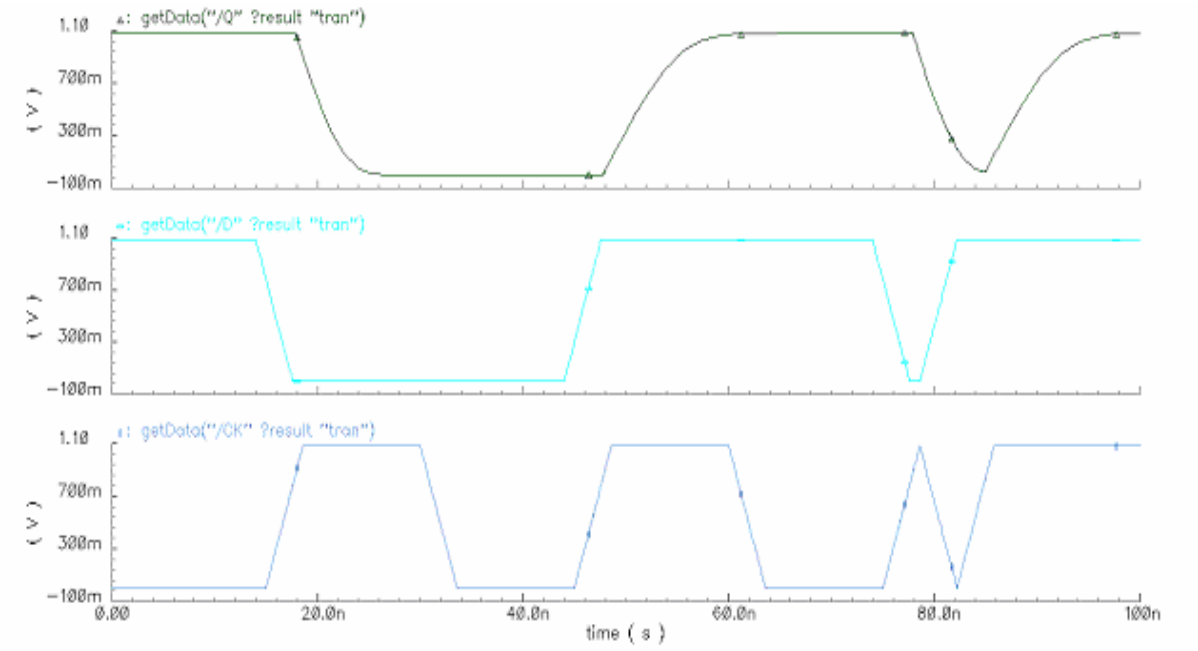


Figure 5.23 Waveform for DFFHQ

Table 5.46 Delay 50% Input to 50% Output for DFFHQ at SS, 0.96V, 125^{o}C

CK to Q delay	Old (ns)	New (ns)	% Change
CLK(r) to Q(r)	2.145	2.18	1.60
CLK(r) to Q(f)	1.087	1.119	2.85

5.8.3 LEAKAGE CURRENT

Table 5.47 Leakage Current for DFFHQ at FF, 1.44V, 125C

D CK	Old(nA)	New(nA)	X Change
0 0	4.637	0.579	8
0 1	9.10	1.3	7
1 0	6.57	0.938	7
1 1	7.87	0.874	9

5.8.4 DYNAMIC CURRENT (Maximum Load, Maximum Slope) Unit- uA

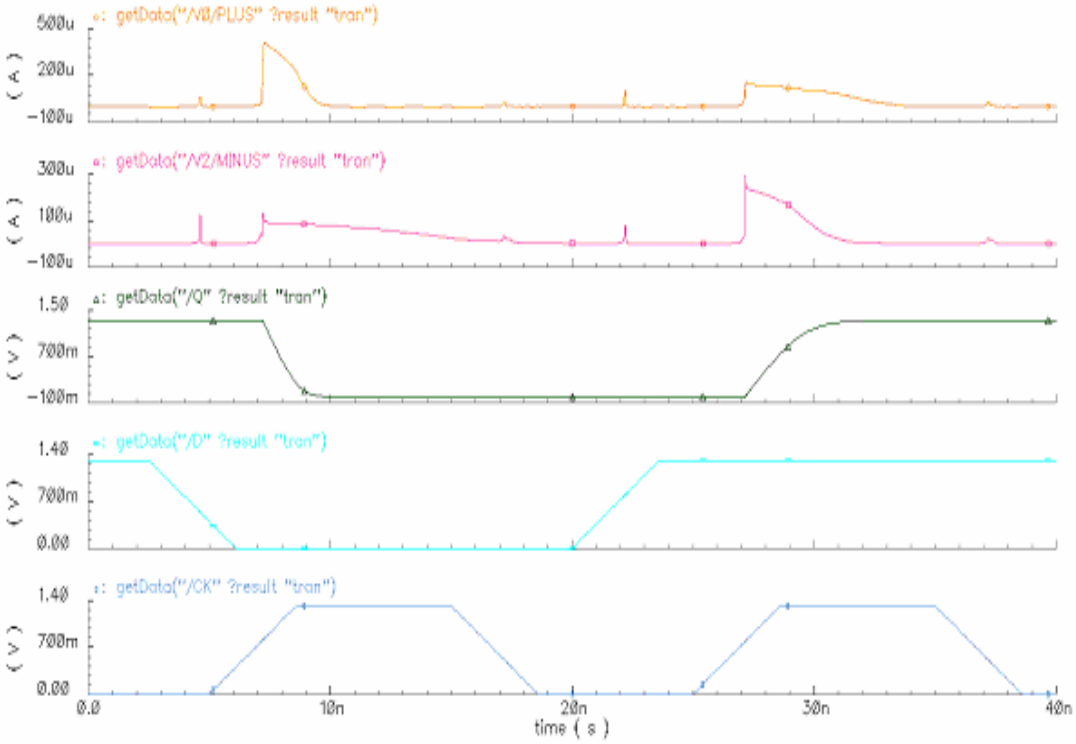


Figure 5.24 Dynamic Current for DFFHQ at FF, 1.44V, -40C

Table 5.48 Dynamic current for DFFHQ at FF, 1.44V, -40C

Input	Old	New	X Change
CK= L-H D= L-H	31.22	30.60	1.02
CK= H-L D= H-L	24.13	21.16	1.14

5.9 SDFFHQ

Table 5.49 Slope Value for SDFFHQ

Clk Slope(ns)	Signal Slope(ns)
0.08	1.33
1.32	2.77

5.9.1 SETUP TIME & HOLD TIME

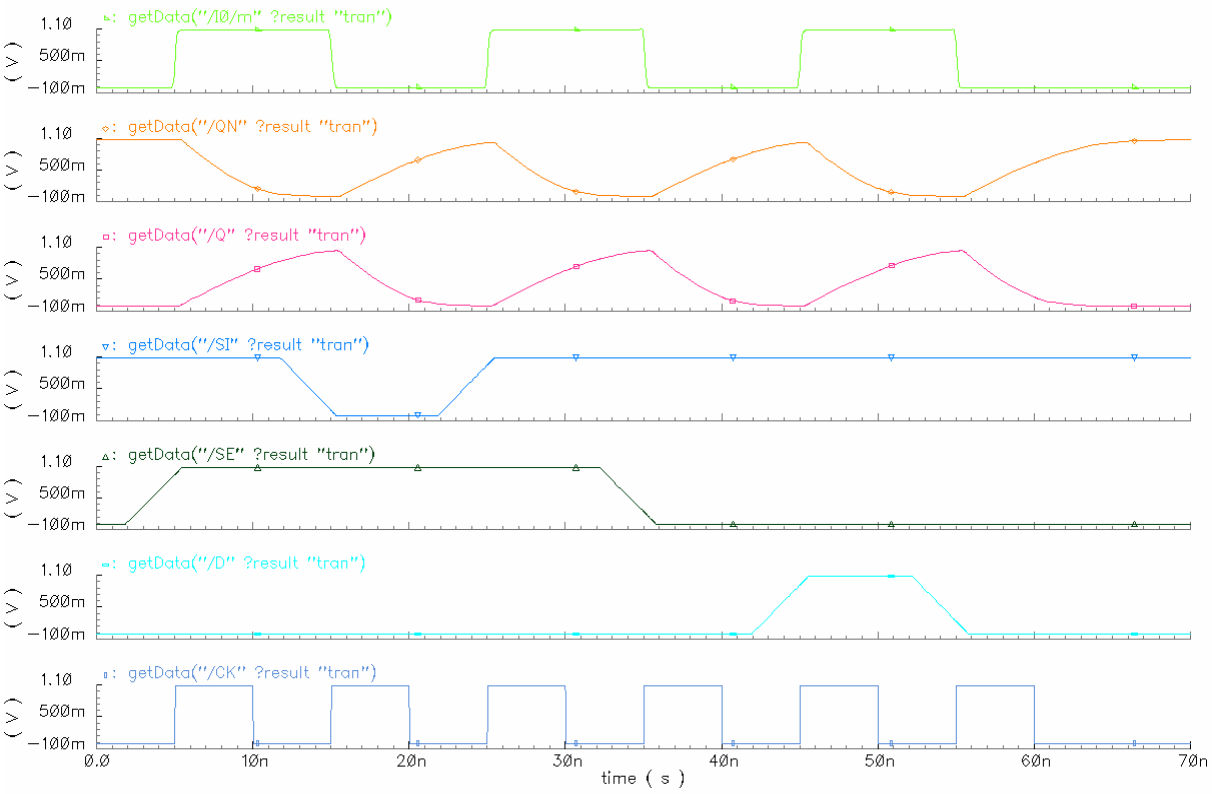


Figure 5.25 Waveform for Setup and Hold Time of SDFFHQ

5.9.1.1 SETUP TIME

Table 5.50 Setup Time for SDFFHQ at SS, 0.96V, 125^{o}C

Setup Time	Old (ns)	New (ns)	% Change
CLK(r) to D(r)	0.21	0.261	19.54
CLK(r) to D(f)	0.09	0.11	18.18

5.9.1.2 HOLD TIME

Table 5.51 Hold Time for SDFFHQ at SS, 0.96V, 125^{o}C

Hold Time	Old (ns)	New(ns)	% Change
CLK(r) to D(r)	0.005	0.01	50
CLK(r) to D(f)	0.01	0.03	66.67

5.9.2 CLK TO Q DELAY (50%Input to 50% Output)

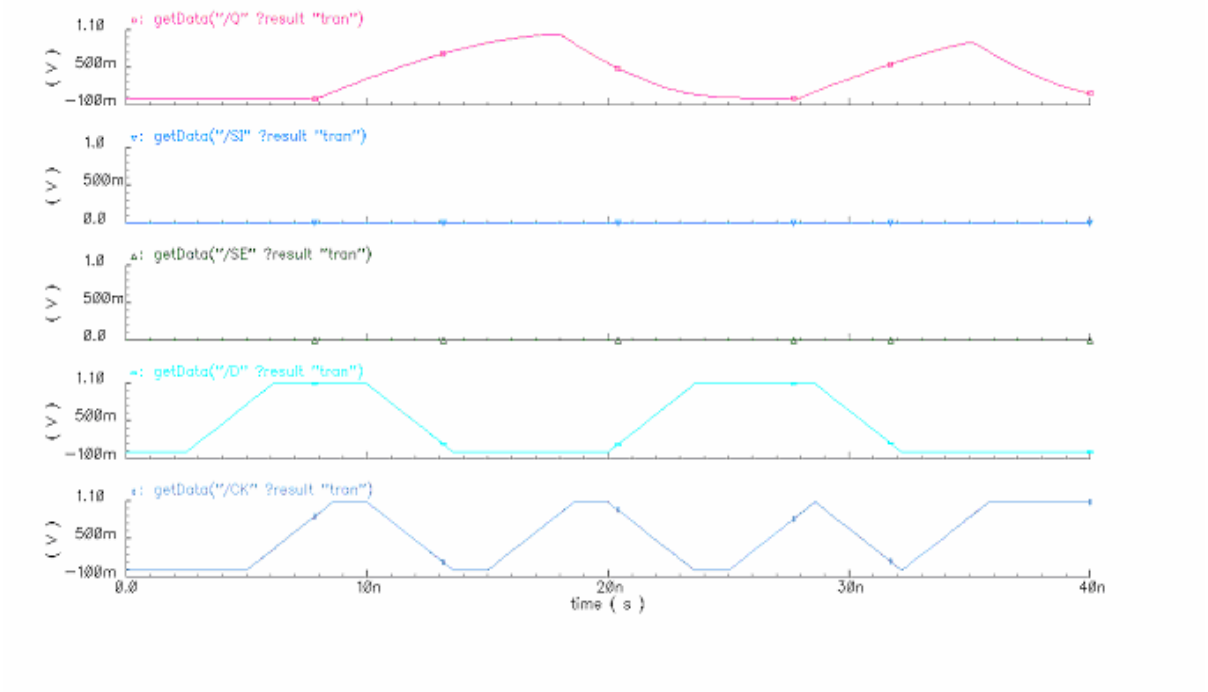


Figure 5.26 Waveform for SDFFHQ

Table 5.52 Delay 50% Input to 50% Output for SDFFHQ at SS, 0.96V, 125^{o}C

CK to Q delay	Old (ns)	New (ns)	% Change
CLK(r) to Q(r)	3.145	4.18	24.76
CLK(r) to Q(f)	2.04	2.91	29.89

Table 5.53 Delay 50% Input to 50% Output for SDFFHQ at SS, 0.96V, 125^{o}C

SE to Q delay	Old (ns)	New (ns)	% Change
SE(r) to Q(r)	2.32	4.14	43.96
SE(r) to Q(f)	1.60	2.21	27.60

Table 5.54 Delay 50% Input to 50% Output for SDFFHQ at SS, 0.96V, 125^{o}C

SI to Q delay	Old (ns)	New(ns)	% Change
SI(r) to Q(r)	1.32	2.92	54.79
SI(r) to Q(f)	1.20	1.9	36.84

5.9.3 LEAKAGE CURRENT

When CK =0

Table 5.55 Leakage Current for SDFFHQ at FF, 1.44V, 125C

D SE SI	Old (nA)	New(nA)	X Change
0 0 0	7.12	0.89	8
0 0 1	15.87	2.27	7
0 1 0	28.12	4.01	7
0 1 1	16.34	2.04	8
1 0 0	18.21	2.02	9
1 0 1	31.24	5.20	6
1 1 0	19.32	2.41	8
1 1 1	17.54	2.19	8

5.9.4 DYNAMIC CURRENT (Maximum Load, Maximum Slope) Unit- uW/MHz

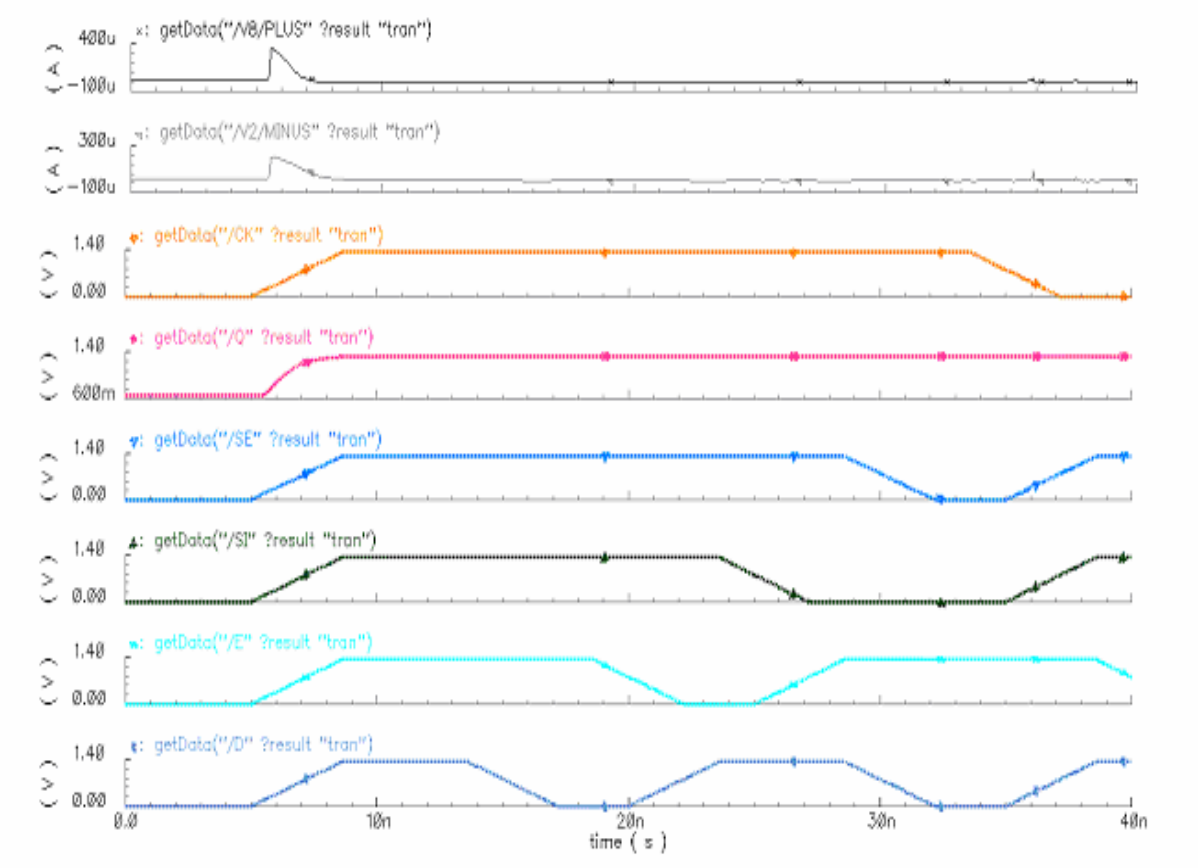


Figure 5.27 Dynamic Current for SDFFHQ at FF, 1.44V, -40C

Table 5.56 Dynamic current for TLATSR at FF, 1.44V, -40C

Input	Old	New	X Change
CK= L-H D = L-H SE = L-H SI = L-H	23.43	20.91	1.12
CK= H-L D= H-L SE = H-L SI= H-L	18.56	15.67	1.18

5.10 SDFFNH

Table 5.57 Slope Value for SDFFNH

Clk Slope(ns)	Signal Slope(ns)
0.08	1.33
1.32	2.77

5.10.1 SETUP TIME & HOLD TIME

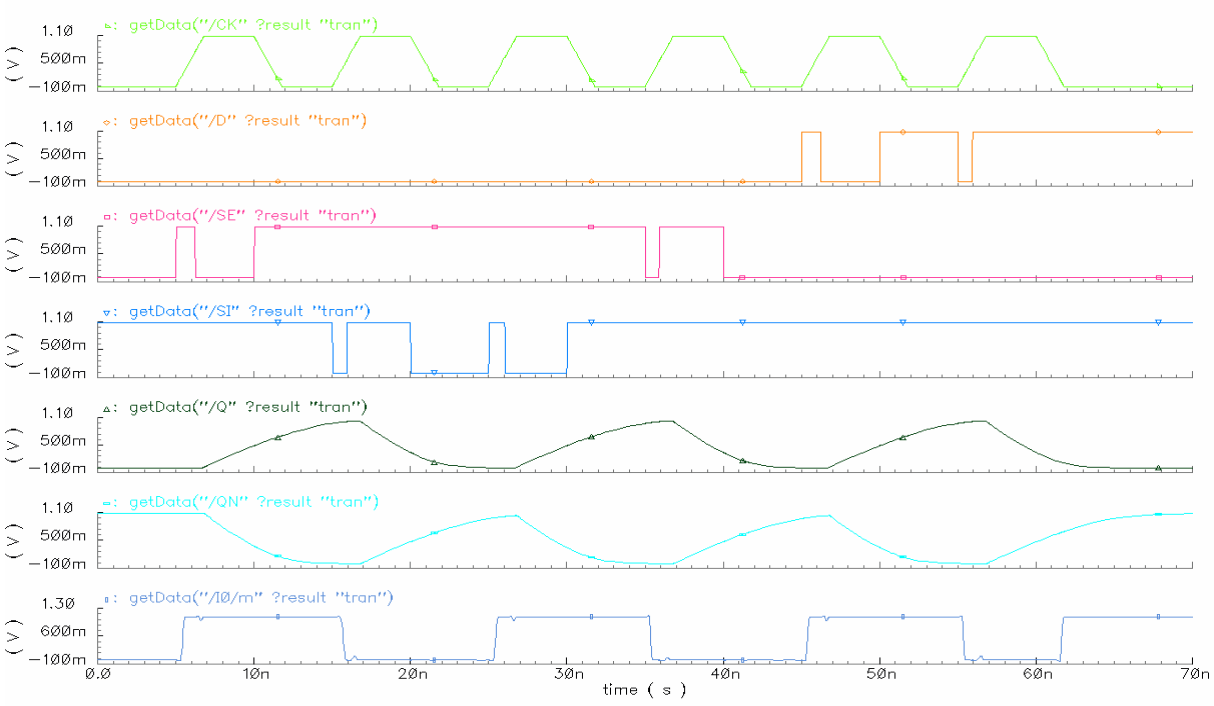


Figure 5.28 Waveform for Setup and Hold Time of SDFFNH

5.10.1.1 SETUP TIME

Table 5.58 Setup Time for SDFFNH at SS, 0.96V, 125°C

Setup Time	Old (ns)	New (ns)	% Change
CLK(r) to D(r)	0.12	0.145	17.24
CLK(r) to D(f)	0.03	0.09	66.67

5.10.1.2 HOLD TIME

Table 5.59 Hold Time for SDFFNH at SS, 0.96V, 125°C

Hold Time	Old(ns)	New(ns)	% Change
CLK(r) to D(r)	0.015	0.02	25
CLK(r) to D(f)	0.09	0.11	18.18

5.10.2 CLK TO Q DELAY (50%Input to 50% Output)

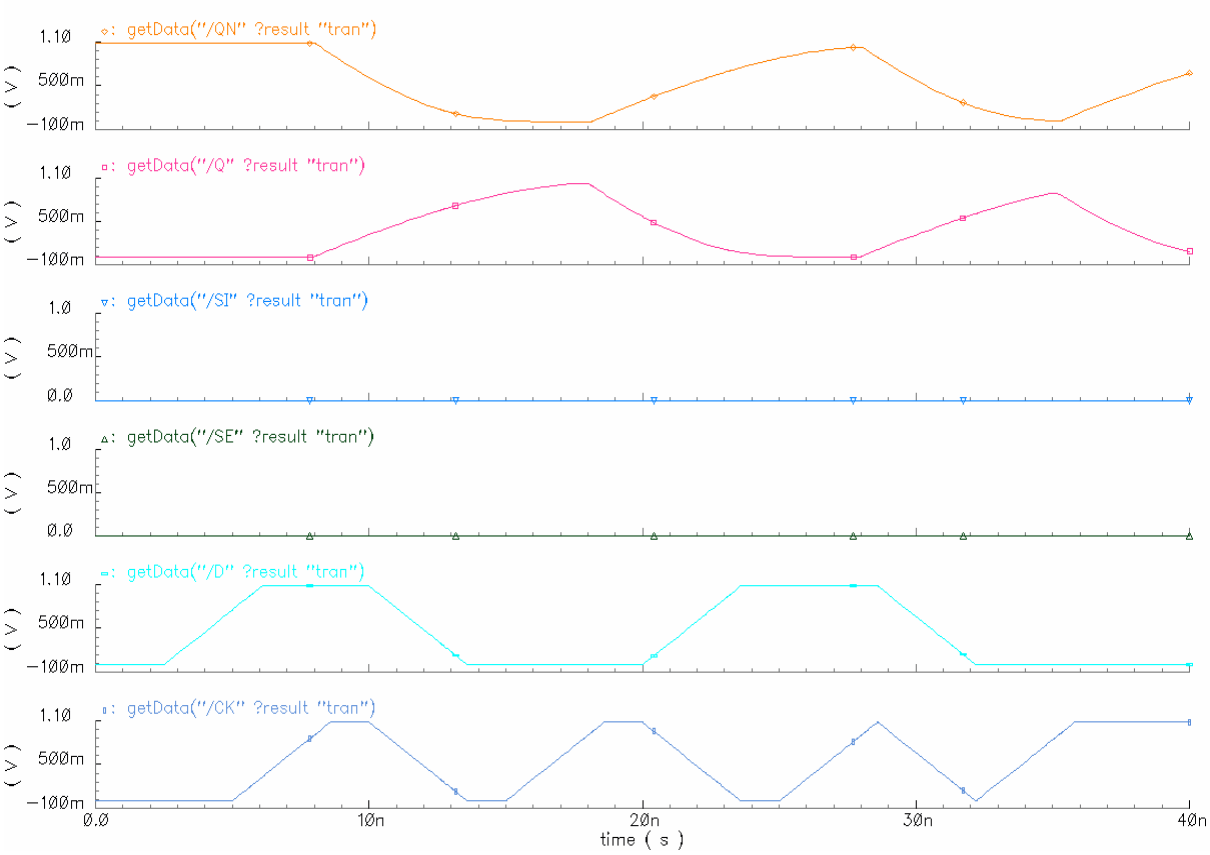


Figure 5.29 Waveform for SDFFNH

Table 5.60 Delay 50% Input to 50% Output for SDFFNH at SS, 0.96V, 125^{o}C

CK to Q delay	Old(ns)	New(ns)	% Change
CLK(r) to Q(r)	3.145	3.18	1.1
CLK(r) to Q(f)	1.81	1.92	5.72

Table 5.61 Delay 50% Input to 50% Output for SDFFNH at SS, 0.96V, 125^{o}C

SEto Q delay	Old(ns)	New(ns)	% Change
SE(r) to Q(r)	1.92	2.32	20.88
SE(r) to Q(f)	1.7	1.87	-10

Table 5.62 Delay 50% Input to 50% Output for SDFFNH at SS, 0.96V, 125^{o}C

SI to Q delay	Old(ns)	New(ns)	% Change
SI(r) to Q(r)	1.92	2.32	20.88
SI(r) to Q(f)	1.7	1.86	-9.41

5.10.3 LEAKAGE CURRENT

When CK =0

Table 5.63 Leakage Current for SDFFNH at FF, 1.44V, 125C

D SE SI	Old(nA)	New(nA)	X Change
000	5.637	0.704	8
001	10.10	1.32	7.6
010	28.12	4.68	6
011	6.34	0.792	8
100	19.21	1.921	10
101	31.24	5.20	6
110	19.32	2.41	8
111	17.54	2.19	8

5.10.4 DYNAMIC CURRENT (Maximum Load, Maximum Slope) Unit- uW/MHz

Table 5.64 Dynamic current for SDFFNH at FF, 1.44V, -40C

Input	Old	New	X Change
CKN= L-H D= L-H SE = L-H SI= L-H	21.22	20.91	1.01
CKN= H-L D= H-L SE = H-L SI= H-L	24.13	22.31	1.08

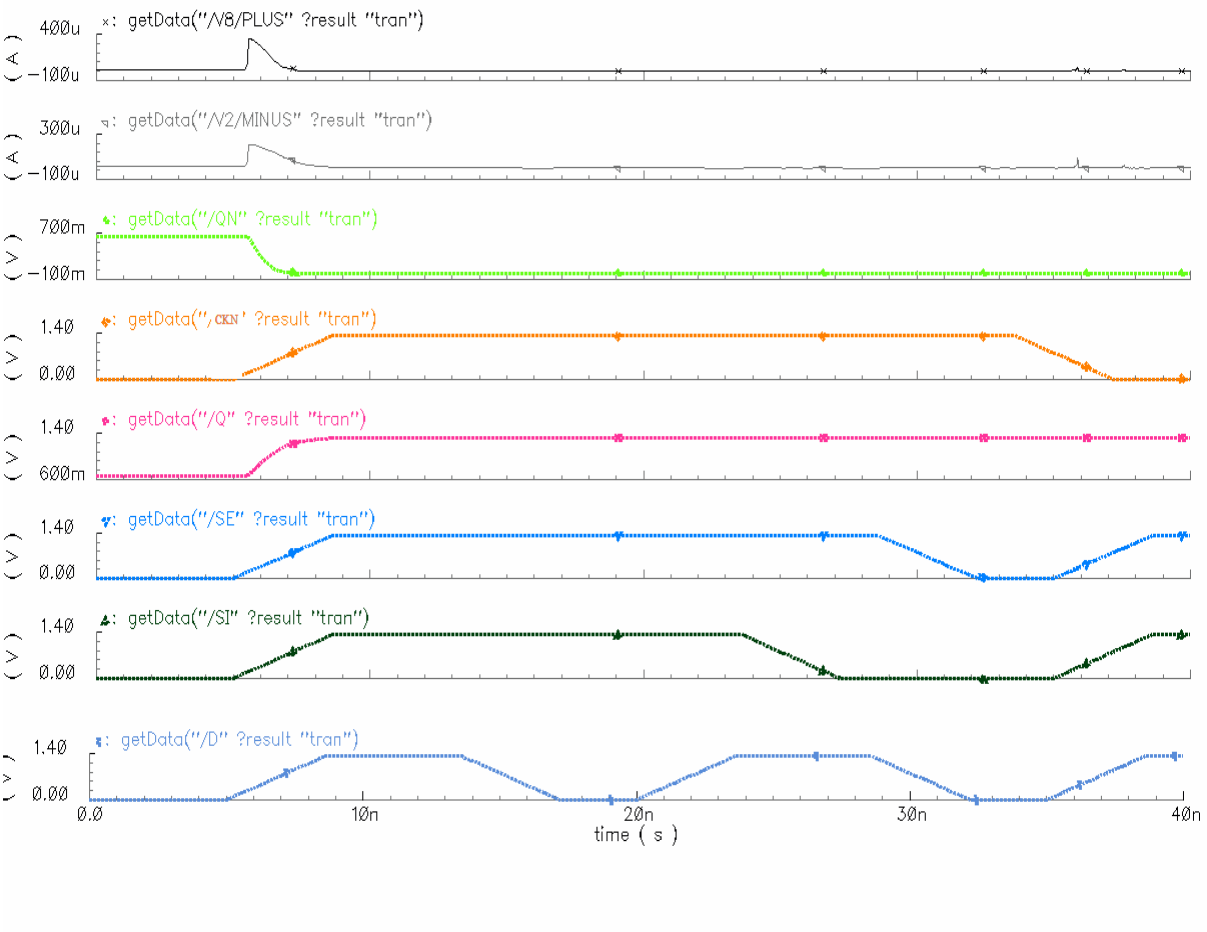


Figure 5.30 Dynamic Current for SDFFNH at FF, 1.44V, -40C

CHAPTER 6
CONCLUSION AND FUTURE WORK

6.1 Conclusion

As the purpose first states, the possibility of making a standard cell library from which other constructions could be made, has been examined. A few basic cells, has been created. Each individual cell was run through simulator Spectre (cadence) and calculating delay (50%-50%), slew delay and leakage current for the cell library. Those were the steps carried out in order to make an ultra low power standard cell library. Results show that the library provides a factor of 8-10 in leakage reduction over its predecessor library. In some cases, much greater leakage power reduction can be achieved. In addition to the power reduction, library implementations have not significant increase in delay 10-15%. Lastly, the versatility of the library has been expanded beyond the original library's scope with the addition of several new library cells. This generates more compact and efficient layout as some cells in the new library replace combinations of several sub-cells in the old library.

6.2 Future Work

The library has been under development; so far only 280 components have been developed out of 632. In this thesis work, have completed OAI, MUX, TLATCH, DFFH, DFFHQ, SDFFH, SDFFHQ logic cells. The culmination of this work will be to release the library through the RF silicon. The library has been used in the design of seven chips, with several more in the final design stage. The heavy usage has helped detect many bugs found in the library. At present, almost all of the library cells have been used by one or more chip designs, verifying correct operation.

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