DESIGN OF LOW POWER CMOS CELL STRUCTURES BASED ON GATE DIFFUSION INPUT TECHNIQUE

Thesis submitted towards the partial fulfillment of the requirements for the award of the degree of

Master of Technology (VLSI Design & CAD)

Submitted by

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JULY – 2010

CERTIFICATE

I hereby certify that the work which is being presented in the thesis entitled, **"DESIGN OF LOW POWER CMOS CELL STRUCTURE BASED ON GATE DIFFUSION INPUT TECHNIQUE"** in partial fulfillment of the requirement for the award of degree of M.Tech (VLSI Design & CAD) at Electronic and Communication Department of Thapar University, Patiala, is an authentic record of my own carried out under the supervision of Mr. Sanjay Kumar, Assistant Professor, ECED.

The matter embodied in this thesis has not been submitted in any other University/Institute for the award of any degree.

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ACKNOWLEDGEMENTS

Far and away the best prize that life has to offer is the chance to work hard at work worth doing. Every journey ends with a desired or non desired designation but the moral is that we should not forget to give a heartfelt thank to all those who were thinking for us when we were not thinking , lifted us when we fall down, guide us, help us and show the way for our designation. It is pleasant aspect that I have now the opportunity to express my gratitude for all of them.

In my child hood I read some beautiful lines that a teacher is like a candle which burns for give you light but when it does not burn it means it teach you how to find a way in the darkness. So first I would like to thank *Mr. Sanjay Kumar*, Assistant Professor, my thesis advisor and mentor at Thapar University, under whose inspiration, encouragement and guidance I have successfully completed this thesis work. He let me work on my thesis in complete freedom while strongly supporting my academic endeavors, no matter where they took me. I would like to thank him for introducing me to the problem and providing invaluable advice throughout the course of the work. I truly admire his perseverance, depth of knowledge and his confidence I am extremely thankful to god that he gave me opportunity to work with a such kind of person. I will be always thankful to you Sanjay sir in my whole life and in future I will be whatever and wherever, will respect you as my best and I wish to god for always fulfill your's dreams.

Next, I wish to express my gratitude to Professor *(Dr.) A. K. Chatterjee*, Head, Department of Electronics and Communication Engineering and *Mrs. Alpana Agarwal*, P. G. Coordinator, for their excellent guidance and encouragement right from the beginning of this course. I am especially indebted to them for critical reviewing of my compilation to bring it in the submitted presentable form. I am also grateful for their trust in the choices I made to complete this thesis work.

Next, I'd like to thank *B. K. Hemant (Anna)* sir and *Mohd. Illiyas* sir, for their help, suggestions, and especially for the night lab. Now I will not miss the chance to give thanks to my classmates and college mates Vijay, Vishal, Vaibhav, Charan, Pankaj, Amit, Anand, Shirish and Sachin and all of them whose name I am missing. Thanks guys for their support and such a lifetime memorable moment in thapar.

Other things may change us, but we start and end with the family and I am glad to god that I am part of this family. I would like to thank my entire Family for standing by me through all the joys and sorrows that life had to offer. My heartfelt thanks and life-long gratitude go to my Loving Father and Dearest Mother for all the love and affection that they have showered upon me. You both are the Best and Most Loving Parents that anyone can hope to have in this entire universe. If not for your constant support, encouragement and sacrifices I would never have made it to this stage in life. I love you so much. I would also like to express love to my younger brother Bhanu.

I would like to thank all of them, whose names remain unmentioned but who have never retraced back from helping me whenever the need arose.

And finally how can it is possible I will forget you my friend, my believe, my God. My acknowledgements would not be complete without expressing my gratitude towards Almighty God. I feel very fortunate to come to know Him during all these years of my life and have continually been blessed by His endless love ever since. He is the true shepherd of my life.

ABSTRACT

From the day when first transistor was invented (in 1947), low area, low power, and high speed these are primary issue for a researcher in the transistor based technology. In present scenario the minimization of power consumption have emerged as a key design constraint over the last few years due to increasing demand of complex mobile system in the very large scale integrated circuit design. The battery operated devices which commonly used in present time, also require more portability, high power output with fast timining and cost in budget.

As there are many flexible design topologies like complementary CMOS, pass-transistor logic, transmission gate based technology and so on, but we have no any design technique which provide required flexibility in low power design. So an approach is presented for minimizing power consumption for low power CMOS cell structure.

GATE DIFFUSION INPUT (GDI) technique is a believable step up in the world of low power VLSI design. The primary concern in this thesis work is the reduction of power dissipation using the Gate diffusion input technique with the design of CMOS cell structure and compare with CMOS based cell structure cell design. All these circuits were designed in IC station Cadence IC5141 using standard TSMC 0.18 µm technology.

All the circuit simulations in this thesis have been done in a systematic process. From the schematic design of the structures to post-layout simulations using IC station Cadence IC5141. For the simulation, DRC, LVS, and POST-LAYOUT Assura is used which is a design verification suite of tools within the Virtuoso custom design platform. And then finally the powers have been taken for the various time period for both the design methods.

TABLE OF CONTENTS

LIST OF FIGURES

LIST OF TABLES

LIST OF SYMBOLS

α	Switching Activity [dimensionless]
C_L	Load Capacitance [Farads]
C_{ox}	Oxide Capacitance [Farads/ μm^2]
E	Energy [Jouls]
$E_{dynamic}$	Dynamic Energy [Jouls]
E_{static}	Static Energy [Jouls]
f	Frequency of Operation [Hz]
L_{DP}	Depth of Critical Path [dimensionless]
I_{static}	Static Current [Amperes]
I_D	Drain Current [Amperes]
I_{on-sub}	Subthreshold Current [Amperes]
I_0	Drain Current for V_{gs}= V_{th} [Amperes]
P	Power [Watts]
μ_{eff}	Effective Mobility of majority carriers [Cm^2/V Sec]
n	Subthreshold Slope Factor [dimensionless]
$\frac{W}{L}$	Aspect Ratio [μm/ μm]
t_d	Propagation Delay of an Inverter [Seconds]
T_D	Total Delay of a circuit [Seconds]
V_{dd}	Supply Voltage [Volts]
V_{th}	Threshold Voltage of MOSFET [Volts]
V_T	Thermal Voltage [Volts]
V_s	Voltage Swing [Volts]

CHAPTER 1 INTRODUCTION

1.1 A HISTORICAL PERSPECTIVE

There is a revolutionary boom in the present scenario of digital electronics system. Early digital electronics systems were based on magnetically controlled switches (or relays). They were mainly used in the implementation of very simple logic networks. Examples of such are train safety systems, where they are still being used at present. Up until the 1950s electronic active device technology was dominated by the vacuum tube. All changed with the invention of the transistor at Bell Telephone Laboratories in 1947, followed by the introduction of the bipolar transistor by Schockley in 1949. It took till 1956 before this led to the first bipolar digital logic gate, introduced by Harris, and even more time before this translated into a set of integrated-circuit commercial logic gates, called the Fairchild Micrologic family. The first truly successful IC logic family, TTL (Transistor-Transistor Logic) was pioneered in 1962 [1].

The basic principle behind the MOSFET transistor (originally called IGFET) was proposed in a patent by J. Lilienfeld (Canada) as early as 1925, and, independently, by O.Heil in England in 1935. MOS digital integrated circuits started to take off in full in the early 1970s. Remarkably, the first MOS logic

gates introduced were of the CMOS variety, and this trend continued till the late 1960s. The first practical MOS integrated circuits were implemented in PMOS-only logic and were used in applications such as calculators. The second age of the digital integrated circuit revolution was inaugurated with the introduction of the first microprocessors by Intel in 1972 (the 4004) and 1974 (the 8080). These processors were implemented in NMOS-only logic, which has the advantage of higher speed over the PMOS logic. Simultaneously, MOS technology enabled the realization of the first high density semiconductor memories [1].

In the late 1970s, NMOS-only logic started to suffer from the same plague that made high-density bipolar logic unattractive or infeasible: power consumption [1]. This is where we still are today. Interestingly enough, power consumption concerns are rapidly becoming dominant in CMOS design. CMOS technology also playing a vital role in present revolution in information technology.

1.2 MOTIVATION

IC technology has evolved in the 1960s when Gordon Moore, then with Fair-child Corporation and later cofounder of Intel, predicted that the number of transistors that can be integrated on a single die would grow exponentially with time (this prediction, later called *Moore's law*) from the integration of a few transistors (referred to as Small Scale Integration (SSI) the integration of millions of transistors in Very Large scale Integration (VLSI) chips currently in use[1]. Early ICs were simple and only had a couple of gates or a flip-flop. Some ICs were simply a single transistor, along with a resistor network, performing a logic function. In a period of four decades there have been four generations of ICs with the number of transistors on a single chip growing from a few to over million.

There have been four generation of ICs: SSI (Small Scale Integration), MSI (Medium Scale Integration), LSI (Large Scale Integration), and VLSI (Very Large Scale Integration). Now we are beginning to see the emergence of the fifth generation, ULSI (Ultra Large Scale Integration) which is characterized by complexities in excess of 20 million devices on a single IC chip [3].

The increasing demand of complex mobile systems, which has been observed during the last years in the worldwide market, led the designers to take into account a new objective in the design of complex digital circuits: the minimization of power consumption. The high diffusion of systems like laptop and palmtop computers, cellular phones, wireless modems and portable multimedia applications is one of the most important reasons that fuel the need for a low-power design. The need for minimization of power dissipation of a system is also enforced by some thermal considerations; a big portion of the energy requested by a device from the power supply is converted into heat. In this way heat dissipation system and cooling mechanisms become indispensable for the correct and safe operation of the device and also for its reliability.

1.3 THESIS ORGANIZATION

The primary goal of this thesis is to demonstrate a circuit level design approach, for use in designs which demand extreme low power dissipation.
This thesis is organized as follows:

CHAPTER 1: INTRODUCTION. This chapter briefly explains the historical perspective in the area of VLSI. This chapter also provides the motivation of new trend in low power design in the today's era of scaling down of technologies and nanotechnology. Finally, this thesis chapter explains organization of the thesis.

CHAPTER 2: FACTORS AND SOURCES OF POWER DISSPATION FOR VLSI DESIGN. This chapter briefly introduces the different sources and factors of power dissipation that occur in CMOS digital circuits.

CHAPTER 3: CMOS TOPOLOGIES. This chapter describes in brief the different CMOS topologies which are widely used in VLSI design and also describe their characteristics. This chapter also describes the complementary CMOS and its basic structure designing.

CHAPTER 4: DESIGN METHODOLOGY OF GATE DIFFUSION INPUT TECHNIQUE. This chapter introduces gate diffusion input technique, its design methodology and its characteristics. Also include the analysis of GDI cell and swing restore buffering process.

CHAPTER 5: DESIGN AND ANALYSIS OF LOW POWER CMOS CELL STRUCTURE. This chapter will describe the circuit designing and their simulation for CMOS based design as well as GDI technique based design. This chapter also includes the comparison of power dissipation in CMOS based design and GDI technique based design.

CHAPTER 6: LAYOUT DESIGN AND POST LAYOUT SIMULATION. This chapter discusses the designs of different layouts for all the proposed structures, which are designed in CADENCE IC Station TSMC 0.18 micron Technology and the Layout versus Schematic (LVS) program was executed to perform a comparison of the schematic to the physical layout.

CHAPTER 7: CONCLUSION AND FUTURE ASPECT. This chapter summarizes the major accomplishments of this thesis and presents the scope for future and further research.

CHAPTER 2

FACTORS AND SOURCES OF POWER DISSIPATION FOR VLSI DESIGN

A dichotomy exists in the design of VLSI systems: they must be simultaneously low power and high performance. This dichotomy largely arises from the use of these systems in battery-operated portable (wearable) platforms. The power consumption of a design determines how much energy is consumed per operation and much heat the circuit dissipates. These factors influence a great number of critical design decisions, such as the power-supply capacity, the battery lifetime, supply-line sizing, packaging and cooling requirements.

2.1 POWER DISSIPATION

Power dissipation is an important property of a design that affects feasibility, cost, and reliability. In the world of high-performance computing, power consumption limits, dictated by the chip package and the heat removal system, determine the number of circuits that can be integrated onto a single chip, and how fast they are allowed to switch. With the increasing popularity of mobile and distributed computation, energy limitations put a firm restriction on the number of computations that can be performed given a minimum time between battery recharges.

The power dissipation can further be decomposed into:

- Static power dissipation.
- Dynamic power dissipation.

2.1.1 STATIC POWER DISSIPATION

The static or steady state power dissipation of a circuit is expressed by the following relation [4]

$$P_{stat} = I_{stat} V_{dd} \quad (2.1)$$

where, I_{stat} is the current that flows through the circuit when there is no switching activity. Ideally, CMOS circuits dissipate no static (DC) power since in the steady state there is no direct path from V_{dd} to ground as PMOS and NMOS transistors are never on simultaneously. Of course, this scenario can never be realized in practice since in reality the MOS transistor is not a perfect switch. Thus, there will always be leakage currents and substrate injection currents, which will give to a static component of CMOS power dissipation. For a sub-micron NMOS device W/L = 10/ 0.5, the substrate injection current is of the order of 1- 100 μA for a V_{dd} of 5 V [5].

Another form of static power dissipation occurs for the so-called Ratioed logic. Pseudo-NMOS is an example of a Ratioed CMOS logic family. In this, the PMOS pull-up is always on and acts as a load device for the NMOS pull-down network. Therefore, when the gate output is in low-state, there is a direct path from V_{dd} to ground and the static currents flow. In this state, the exact value of the output voltage depends on the ratio of the strength of PMOS and NMOS networks hence the name. The static power consumed by these logic families can be considerable.

For this reason, logic families such as this, which experience static power consumption, should be avoided for low-power design. With that in mind, the static component of power consumption in low-power CMOS circuits should be negligible and the focus shifts primarily to dynamic power consumption.

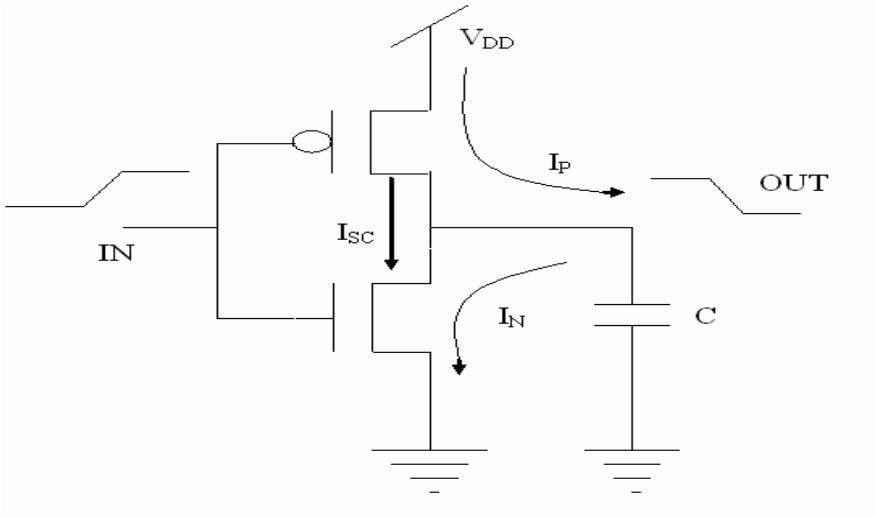

Figure. 2.1. CMOS Inverter for Power Analysis.

2.1.2 DYNAMIC POWER DISSIPATION

The dynamic component of power dissipation arises from the transient switching behavior of the CMOS device. At some point during the switching transient, both the NMOS and PMOS devices will be turned on. This occurs for gate voltages between V_{tn} and V_{dd} - V_{tp} . During this time, a short-circuit exists between V_{dd} and ground and the currents are allowed to flow. A detailed analysis of this phenomenon by Veendrick reveals that with careful design of the transition edges, this component can be kept below 10-15% of the total power [5]; this can be achieved by keeping the rise and fall times of all the signals throughout the design within a fixed range (preferably equal). Thus, although short circuit dissipation cannot always be completely ignored, it is certainly not the dominant component of power dissipation in well-designed CMOS circuits.

Instead, dynamic dissipation due to capacitance charging consumes most of the power. This component of dynamic power dissipation is the result of charging and discharging of the parasitic capacitances in the circuit.

The situation is modeled in Figure 2.1, where the parasitic capacitances are lumped at the output in the capacitor *C*. Consider the behavior of the circuit over one full cycle of operation with the input voltage going from V_{dd} to ground and back to V_{dd} again. As the input switches from high to low, the NMOS pull-down network is cut-off and PMOS pull-up network is activated charging load capacitance *C* up to V_{dd}. This charging process draws energy equal to CV_{dd}^{2} from the power supply. Half of this is dissipated immediately in the PMOS transistors, while the other half is stored on the load capacitance. Then, when the input returns to V_{dd}, the process is reversed and the capacitance is discharged, its energy being in the NMOS network. In summary, every time a capacitive node switches from ground to V_{dd} (and back to ground), energy of CV^2 is consumed.

This leads to the conclusion that CMOS power consumption depends on the *switching activity* of the signals involved. We can define *activity*, α as the expected number of zero to one transition per data cycle. If this is coupled with the average data rate, *f*, which may be the clock frequency in a synchronous system, then the effective frequency of nodal charging is given the product of the activity and the data rate: αf. This leads to the following formulation for the average CMOS power consumption:

$$P_{dyn} = \alpha C V_{DD}^{2} f \tag{2.2}$$

This classical result illustrates that the dynamic power is proportional to the switching activity, capacitive loading and the square of the supply voltage. In CMOS circuits, this component of power dissipation is by far the most important accounting for at least 90% of the total power dissipation [5].

2.2 SOURCES OF POWER DISSIPATION

CMOS is, by far, the most common technology used for manufacturing digital ICs. There are three sources of power dissipation in a CMOS circuit.

$$P_{total} = P_{swithing} + P_{short\text{-}circuit} + P_{leakage} \quad (2.3)$$

The first due to signal transition. As the "nodes" in a digital CMOS circuit transition back and forth between the two logic levels, the capacitances associated with the nodes get charged and discharged. Current flows through the channel of the transistor and the electricity energy then gets converted in to heat and dissipated away. This portion of power dissipation is proportional to the supply voltage, the dissipation due to transition various overall as the square of the supply voltage.

The second source of power dissipation is comes from short circuit currents, which flow directly from the supply to the ground terminal when the n sub network and p sub network of a CMOS gate conduct simultaneously. With inputs to the gate stable at either logic level, only one of the two sub network conduct and no short circuit current flow. However, when the outputs of a gate switch in response to change in input both sub network conduct simultaneously for a brief interval. The duration of the interval depends on the input and the output transition times and so does the short circuit dissipation.

Both of the above sources of power dissipation in CMOS circuits are related to transition at gate outputs and are therefore collectively referred to as dynamic dissipation. In contrast, the third and the last source of dissipation is due to the leakage currents, which flow when the input to and, therefore, the output of a gate are not changing and is called static dissipation. One of the reasons CMOS circuit are in widespread use is that the only static dissipation in standard CMOS circuit is due to leakage currents and is usually small in magnitude. But as the supply

voltage is being scaled down to reduce dynamic power, transistor with low threshold voltage, the greater the standby leakage current [6].

2.3 SWITCHING POWER DISSIPATION

This component represents the power dissipated during a switching event, i.e., when the output node voltage of a CMOS logic gate makes a power consuming transition. In digital CMOS circuits, dynamic power is dissipated when energy is drawn from the power supply to charge up the output node capacitance. During the charge-up phase, the output node voltage typically makes a full transition from 0 to V_{dd}, and the energy used for the transition is relatively independent of the function performed by the circuit.

To illustrate the dynamic power dissipation during switching, consider the circuit example given in Figure 2.2. Here, a two-input NOR gate drives two NAND gates, through interconnection lines. The total capacitive load at the output of the NOR gate consists of

- The output capacitance of the gate itself,
- The total interconnect capacitance, and
- The input capacitances of the driven gates.

The output capacitance of the gate consists mainly of the junction parasitic capacitances, which are due to the drain diffusion regions of the MOS transistors in the circuit. The important aspect to emphasize here is that the amount of capacitance is approximately a linear function of the junction area. Consequently, the size of the total drain diffusion area dictates the amount of parasitic capacitance.

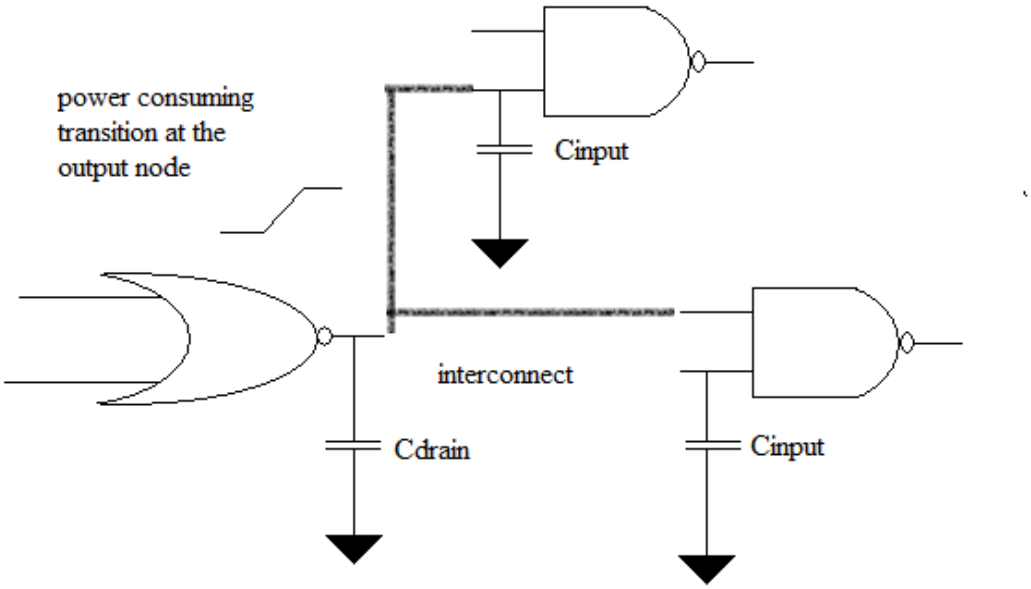

Figure 2.2: A NOR gate driving two NAND gates through interconnection Lines [2].

The interconnect lines between the gates contribute to the second component of the total capacitance. Note that especially in sub-micron technologies, the interconnect capacitance can become the dominant component, compared to the transistor-related capacitances. Finally, the input capacitances are mainly due to gate oxide capacitances of the transistors connected to the input terminal. Again, the amount of the gate oxide capacitance is determined primarily by the gate area of each transistor.

Any CMOS logic gate making an output voltage transition can thus be represented by its NMOS network, PMOS network, and the total load capacitance connected to its output node, as seen in Figure 2.3. The average power dissipation of the CMOS logic gate, driven by a periodic input voltage waveform with ideally zero rise- and fall-times, can be calculated from the energy required to charge up the output node to V_{dd} and charge down the total output load capacitance to ground level.

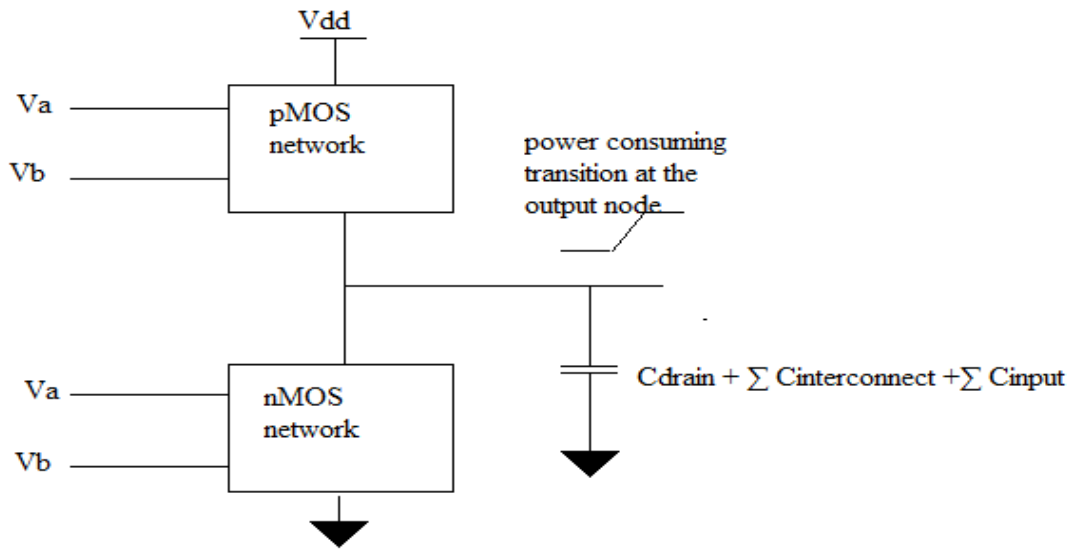

Figure 2.3: Representation of a CMOS logic gate for switching power Calculation [2].

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$$P_{avg} = \frac{1}{T}\left[\int_0^{T/2} V_{out}\left(-C_{load}\frac{dV_{out}}{dt}\right)dt + \int_{T/2}^{T}(V_{DD}-V_{out})\left(C_{load}\frac{dV_{out}}{dt}\right)dt\right] \quad (2.4)$$

Evaluating this integral yields the well-known expression for the average dynamic (switching) power consumption in CMOS logic circuits.

$$P_{avg} = \frac{1}{T} C_{load} V_{dd}^{2} \tag{2.5}$$

or $$P_{avg} = C_{load}.V_{dd}^{2}.\text{f} \tag{2.6}$$

Note that the average switching power dissipation of a CMOS gate is essentially independent of all transistor characteristics and transistor sizes. Hence, given an input pattern, the switching delay times have no relevance to the amount of power consumption during the switching events as long as the output voltage swing is between 0 and V_{dd}.

Equation (2.6) shows that the average dynamic power dissipation is proportional to the square of the power supply voltage; hence, any reduction of V_{dd} will significantly reduce the power consumption. Another way to limit the dynamic power dissipation of a CMOS logic gate is to reduce the amount of switched capacitance at the output. This issue will be discussed in more detail later. First, let us briefly examine the effect of reducing the power supply voltage V_{dd} upon switching power consumption and dynamic performance of the gate.

The analysis of switching power dissipation presented above is based on the assumption that the output node of a CMOS gate undergoes one power-consuming transition (0-to-V_{dd} transition) in each clock cycle. This assumption, however, is not always correct; the node transition rate can be smaller than the clock rate, depending on the circuit topology, logic style and the input signal statistics. To better represent this behavior, we will introduce a T (node transition factor), which is the effective number of power-consuming voltage transitions experienced per clock cycle. Then, the average switching power consumption becomes:

$$P_{avg} = \alpha_T.C_{load}.V_{dd}^{2}.f_{CLK} \tag{2.7}$$

In the most general case, the internal node voltage transitions can also be partial transitions, i.e., the node voltage swing may be only *Vi* which is smaller than the full voltage swing of V_{dd}. Taking this possibility into account, the generalized expression for the average switching power dissipation can be written as

$$P_{avg} = \left(\sum_{i=1}^{\#\ of\ nodes} \alpha_{Ti} \,.\, C_i . V_i\right).V_{dd}.f_{CLK} \tag{2.8}$$

Where *Ci* represents the parasitic capacitance associated with each node and α_{Ti} represents the corresponding node transition factor associated with that node[2].

2.4 SHORT-CIRCUIT POWER DISSIPATION

The switching power dissipation examined above is purely due to the energy required to charge up the parasitic capacitances in the circuit, and the switching power is independent of the rise and fall times of the input signals. Yet, if a CMOS inverter (or a logic gate) is driven with input voltage waveforms with finite rise and fall times, both the NMOS and the PMOS transistors in the circuit may conduct simultaneously for a short amount of time during switching, forming a direct current path between the power supply and the ground.

The current component which passes through both the nMOS and the pMOS devices during switching does not contribute to the charging of the capacitances in the circuit, and hence, it is called the short-circuit current component. This component is especially prevalent if the output load capacitance is small, and/or if the input signals rise and fall times are large. Note that the magnitude of the short-circuit current component will be approximately the same during both the rising-input transition and the falling-input transition, assuming that the inverter is symmetrical and the input rise and fall times are identical.

The pMOS transistor also conducts the current which is needed to charge up the small output load capacitance, but only during the falling-input transition (the output capacitance is discharged through the nMOS device during the rising-input transition). This current component responsible for the switching power dissipation of the circuit (current component to charge up the load capacitance).

For a simple analysis consider a symmetric CMOS inverter with $k = k_n = kp$ and $V_T = V_{T,n} = |V_{T,p}|$, and with a very small capacitive load. If the inverter is driven with an input voltage waveform with equal rise and fall times ($t = t_{rise} = t_{fall}$), it can be derived that the time-averaged short circuit current drawn from the power supply is

$$I_{avg}(short-circuit) = \frac{1}{12}\frac{k.t.f_{CLK}}{V_{dd}}(V_{dd}-2V_T)^3 \tag{2.9}$$

Hence, the short-circuit power dissipation becomes

$$P_{avg}(short-circuit) = \frac{1}{12}.k.t.f_{CLK}.(V_{dd}-2V_T)^3 \tag{2.10}$$

Note that the short-circuit power dissipation is linearly proportional to the input signal rise and fall times, and also to the transconductance of the transistors. Hence, reducing the input transition times will obviously decrease the short-circuit current component.

The discussion concerning the magnitude of the short-circuit current may suggest that the short-circuit power dissipation can be reduced by making the output voltage transition times larger and/or by making the input voltage transition times smaller. Yet this goal should be balanced carefully against other performance goals such as propagation delay [2].

2.5 LEAKAGE POWER DISSIPATION

The NMOS and PMOS transistors used in a CMOS logic gate generally have nonzero reverse leakage and subthreshold currents. In a CMOS VLSI chip containing a very large number of transistors, these currents can contribute to the overall power dissipation even when the transistors are not undergoing any switching event.

The magnitude of the leakage currents is determined mainly by the processing parameters. Of the two main leakage current components found in a MOSFET, the reverse diode leakage occurs when the *pn*-junction between the drain and the bulk of the transistor is reversely biased. The reverse-biased drain junction then conducts a reverse saturation current which is eventually drawn from the power supply. Consider a CMOS inverter with a high input voltage, where the NMOS transistor is turned on and the output node voltage is discharged.

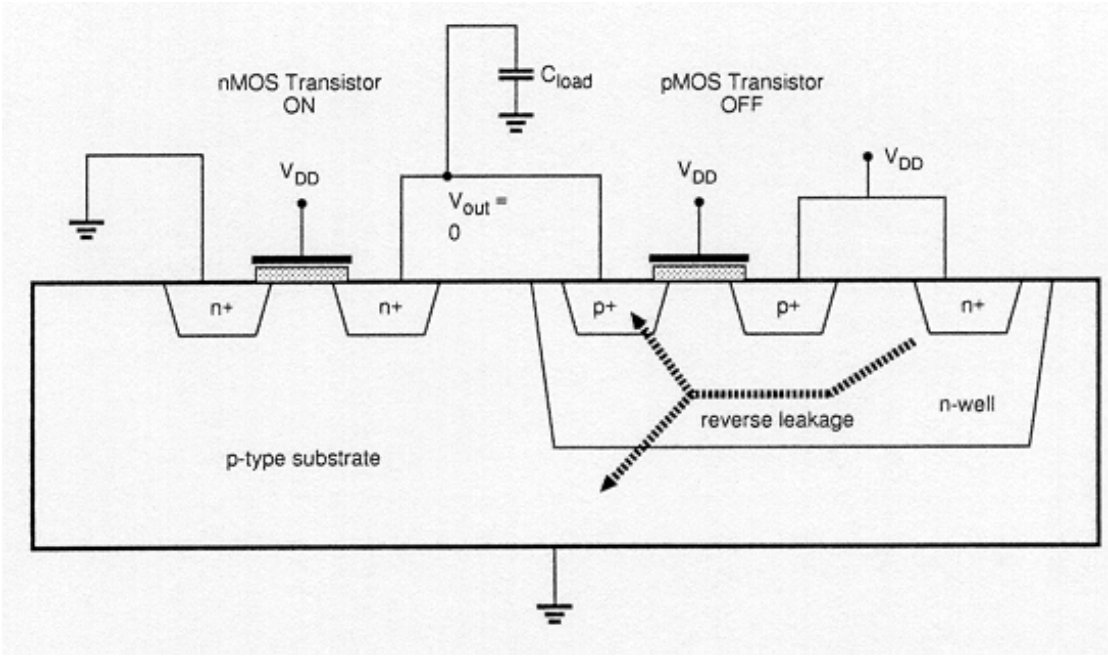

Figure 2.4: Reverse leakage current paths in a CMOS inverter with high Input voltage [2].

Although the PMOS transistor is turned off, there will be a reverse potential difference of V_{dd} between its drain and the n-well, causing a diode leakage through the drain junction. The n-well region of the PMOS transistor is also reverse-biased with V_{dd}, with respect to the p-type substrate. Therefore, another significant leakage current component exists due to the n-well junction (Figure 2.4).

A similar situation can be observed when the input voltage is equal to zero, and the output voltage is charged up to V_{dd} through the PMOS transistor. Then, the reverse potential difference between the NMOS drain region and the p-type substrate causes a reverse leakage current which is also drawn from the power supply (through the pMOS transistor).

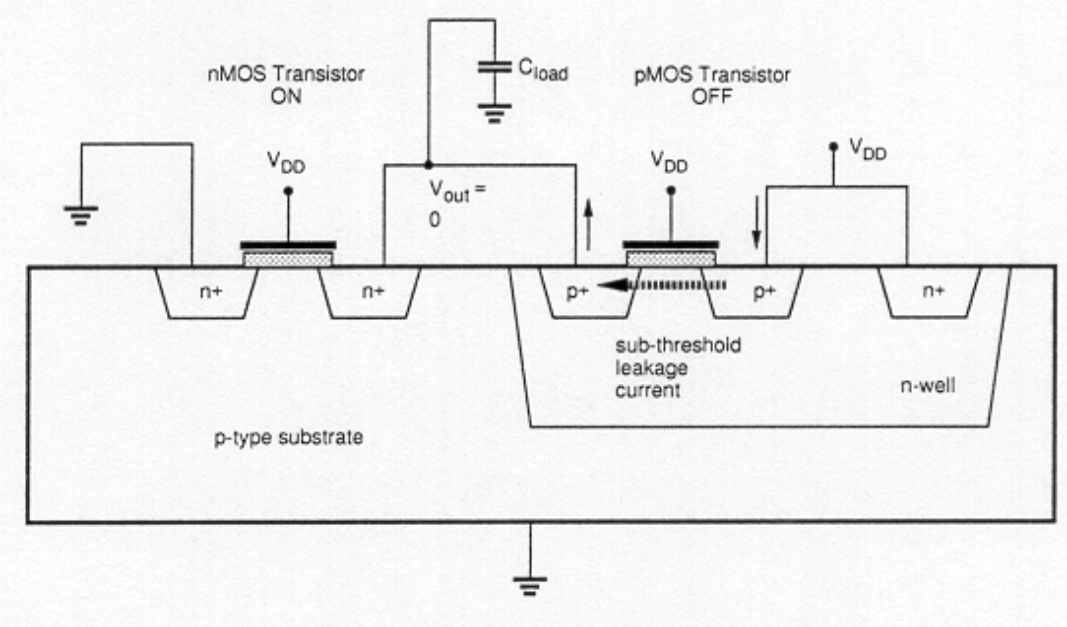

Figure 2.5: Subthreshold leakage current path in a CMOS inverter with high Input voltage [2].

Another component of leakage currents which occur in CMOS circuits is the subthreshold current, which is due to carrier diffusion between the source and the drain region of the transistor in weak inversion. A MOS transistor in the subthreshold operating region behaves similar to a bipolar device and the subthreshold current exhibits an exponential dependence on the gate voltage. The

amount of the subthreshold current may become significant when the gate-to-source voltage is smaller than, but very close to the threshold voltage of the device. In this case, the power dissipation due to subthreshold leakage can become comparable in magnitude to the switching power dissipation of the circuit. The subthreshold leakage current is illustrated in Figure 2.5 [2].

In addition to the three major sources of power consumption in CMOS digital integrated circuits discussed here, some chips may also contain components or circuits which actually consume static power. One example is the pseudo-NMOS logic circuits which utilize a PMOS transistor as the pull-up device. The presence of such circuit blocks should also be taken into account when estimating the overall power dissipation of a complex system.

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CHAPTER 3 CMOS TOPOLOGIES

In this chapter we will analyze complementary CMOS logic style, Pass transistor logic style and Transmission gate and also try to find the drawbacks of these topologies.

3.1 COMPLEMENTARY CMOS LOGIC STYLE

A static CMOS gate is a combination of two networks, called the pull-up network (PUN) and the pull-down network (PDN) as shown as Figure.3.1. The figure shows a generic N input logic gate where all inputs are distributed to both the pull-up and pull-down networks. The function of the PUN is to provide a connection between the output and V_{DD} anytime the output of the logic gate is meant to be 1 (based on the inputs). Similarly, the function of the PDN is to connect the output to VSS when the output of the logic gate is meant to be 0. The PUN and PDN networks are constructed in a mutually exclusive fashion such that one and only one of the networks are conducting in steady state. In this way, once the transients have settled, a path always exists between V_{dd} and the output F, realizing a high output (“one”), or, alternatively, between V_{SS} and F for a low output (“zero”). This is equivalent to stating that the output node is always a low-impedance node in steady state [1].

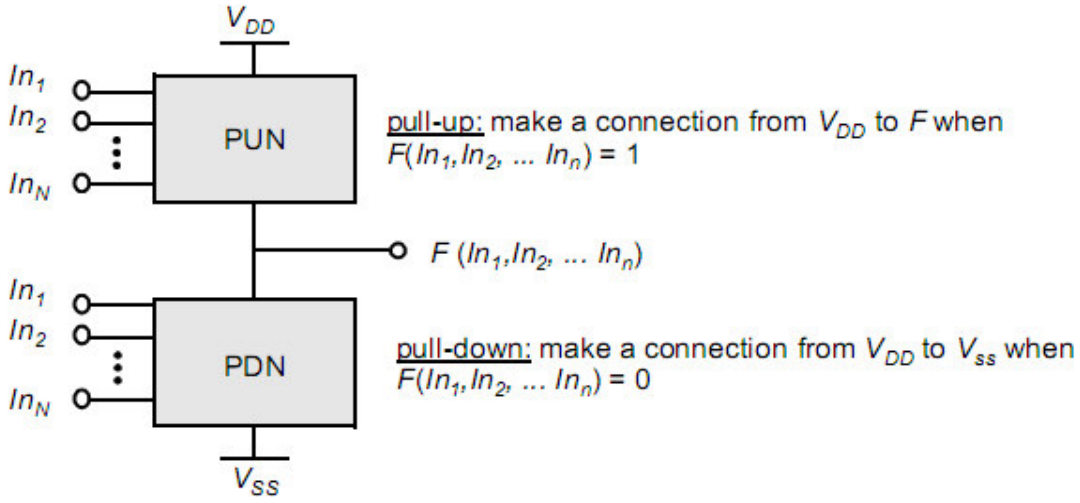


Figure.3.1 Complementary logic gate as a combination of a PUN (pull-upnetwork) and a PDN (pull-down network) [1].

3.1.1 SYNTHESIS OF COMPLEX CMOS GATE

Using complementary CMOS logic, consider the synthesis of a complex CMOS gate whose function is $F = \overline{D + A(B + C)}$. The first step in the synthesis of the logic gate is to derive the pull-down network. By using the fact that NMOS device in series implements the AND function and parallel device implements the OR function. The next step is to use duality to derive the PUN in a hierarchical fashion. The PDN network is broken into smaller networks (i.e., subset of the PDN) called sub-nets that simplify the derivation of the PUN. The sub-nets (SN) for the pull-down network are identified at the top level; SN1 and SN2 are in parallel so in the dual network, they will be in series. Since SN1 consists of a single transistor, it maps directly to the pull-up network.

On the other hand, we need to recursively apply the duality rules to SN2. Inside SN2, we have SN3 and SN4 in series so in the PUN they will appear in parallel. Finally, inside SN3, the devices are in parallel so they appear in series in the PUN. The complete gate is shown in Figure3.2.There is for every possible input combination, there always exists a path to either V_{dd} or *GND*.

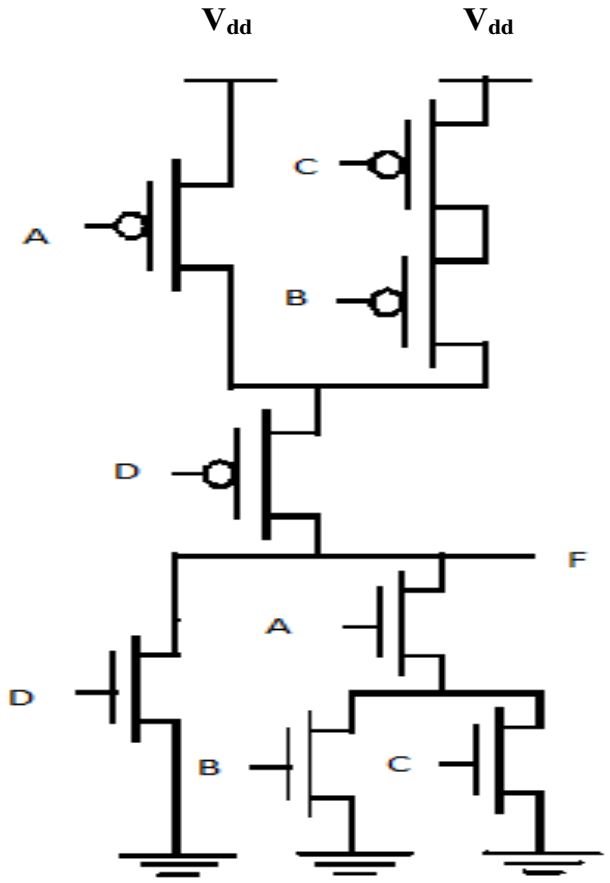


Figure.3.2 Complete Gate of F = $\overline{D + A(B + C)}$

3.2 PASS TRANSISTOR LOGIC STYLE

A popular and widely used alternative to complementary CMOS is pass transistor logic, which attempts to reduce the number of transistor required to implement logic by allowing the primary inputs to drive gate terminal as well as source drain terminal. This is contrast to logic family which only allows primary inputs to drive the gate terminal of MOSFET.

Figure. 3.3 shows an implementation of the AND gate function that way, using only nMOS transistor. In this gate, if the B input is high, the top transistor is turned on and copies the input A to the output F. When B is low, the bottom pass transistor is turned on and passes a 0. The switch driven by $\bar{B}$ seems to be redundant at first glance. It presence to ensure that gate is static. A low impedance path must exist to the supply rails under all circumstances (in this particular case, when B is low).

The promise of this approach is that fewer transistors are required to implement a given function. For example, the implementation of the AND requires 4 transistors (including the inverter required to invert B), while a complementary CMOS implementation would require 6 transistors. The reduced number of devices has the additional advantage of lower capacitance.

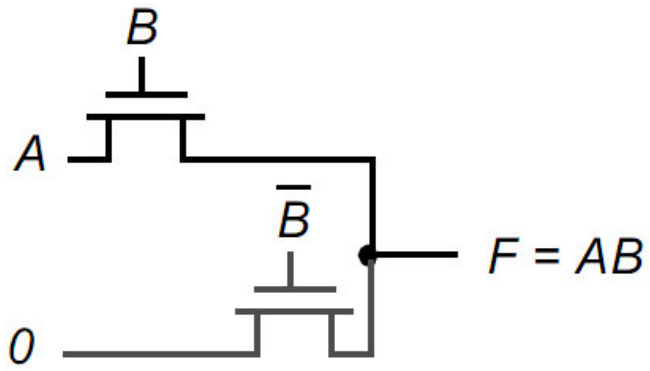


Figure.3.3 Pass-transistor implementation of an AND gate [1].

Unfortunately, an NMOS device is effective at passing a 0 but is poor at pulling a node to V_{dd}. When the pass transistor pulls a node high, the output only charges up to $V_{dd} - V_{tn}$. In fact, the situation is worsened by the fact that the devices experience body effect, as there exists a significant source-to-body voltage when pulling high. Consider the case when the pass transistor is charging up a node with the gate and drain terminals set at V_{dd}. Let the source of the NMOS pass transistor be labeled x. Node x will charge up to $V_{dd} - V_{tn}(V_x)$.

$$V_x = V_{dd} - \left(V_{tn0} + \Upsilon \left(\sqrt{|2\emptyset_f| + V_x} \right) - \sqrt{|2\emptyset_f|} \right) \qquad (3.1)$$

3.2.1 VOLTAGE SWING FOR PASS TRANSISTOR CIRCUIT

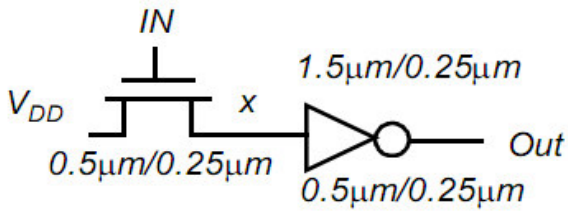


Figure.3.4 a. Transient response of charging up a node using an N device [1].

Extra transistors can be added to provide a path to *GND*, but for this discussion, the simplified circuit is sufficient. Notice that the output charges up quickly initially, but has slow tail. This is attributed to the fact that the drive (gate to source voltage) reduces significantly as the output approaches V_{dd} - V_{tn} and the current available to charge up node x reduces drastically. Hand calculation results in an output voltage of 1.8 V, which comes close to the simulated value.

The basic difference of pass-transistor logic compared to the CMOS logic style is that the source side of the logic transistor networks is connect to some input signal instead of the power lines. The advantage is that one pass-transistor network (either NMOS or PMOS) is sufficient to perform the logic operation, which result in a smaller number of transistors and smaller input loads, especially when NMOS networks are used. However, the threshold voltage drop through the NMOS transistors while passing a logic "1" makes swing (or level) restoration at the gate output necessary in order to avoid static current at the subsequent output inverters or logic gates . Adjusting the threshold voltages as a solution at the process technology level is usually not feasible for other reasons [1].

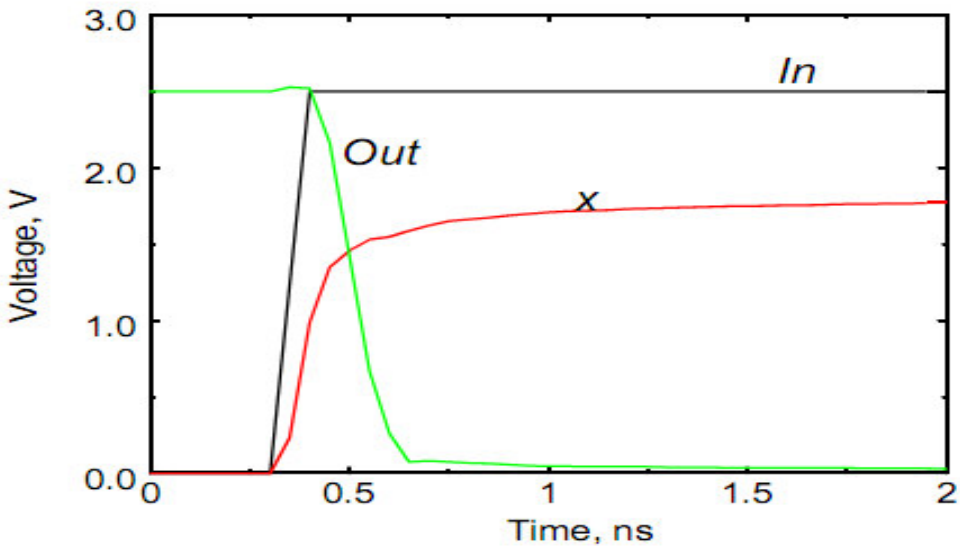


Figure.3.4.b Transient response of charging up a node using an N device[1].

In order to decouple gate inputs and outputs and to provide acceptable output driving capabilities, inverters are usually attached to the gate outputs. Because the MOS networks are connected to variable gate inputs rather than constant power lines, only one signal path through each network must be active at a time in order to avoid short between inputs. Therefore, each pass transistor network must realize a multiplexer structure, which limits the number of logic functions that can be implemented efficiently. Because these pass-transistor multiplexer structures require complementary control signals, dual rail logic is usually use in order to provide all signals in complementary form. As a consequence, two MOS networks area gain required in addition to the swing restoration and output buffering circuitry, which all in all annihilates the advantage of low transistor count and small input loads of pass transistor logic.

Also, the required double inter-cell wiring increases wiring complexity and capacitance by a considerable amount. A small advantage of dual-rail logic is that inverted signals are for free. Layout of pass transistor cells is not as straight forward and efficient due to rather irregular transistor arrangements and high wiring requirements. Finally, pass transistor logic with swing restoration circuitry is sensitive to voltage scaling and transistor sizing with respect to circuit robustness (reduced noise margins), efficient or reliable operation of logic gates

is not necessarily guaranteed at low voltages or small transistor sizes. In other words, transistor sizing is crucial for correct gate operation and therefore more difficult (ratioed logic) [1]. Short circuit current are rather large due to competing signal in the swing restoration circuitry.

3.3 DIFFERENT PASS TRANSISTOR LOGIC STYLES

Many different pass transistor logic styles have been proposed recently. The most important ones are now briefly summarized.

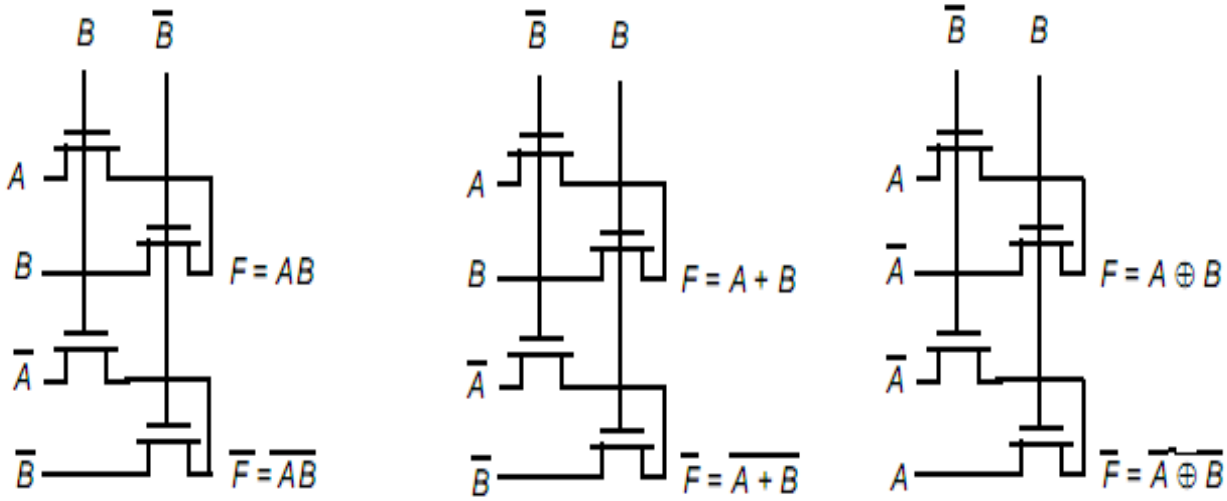
3.3.1 COMPLEMENTARY PASS-TRANSISTOR LOGIC (CPL)

For high performance design, a differential pass-transistor logic family, called CPL or DPL, is commonly used. The basic idea (similar to DCVSL) is to accept true and complementary inputs and produce true and complementary outputs. A number of CPL gates (AND/NAND, OR/NOR, and XOR/NXOR) are shown in Fig.3.5 these gates possess a number of interesting properties.

- CPL belongs to the class of static gates, because the since the circuits are differential, complementary data inputs and outputs are always available. Although generating the differential signals requires extra circuitry, the differential style has the advantage that some complex gates such as XORs and adders can be realized efficiently with a small number of transistors. Furthermore, the availability of both polarities of every signal eliminates the need for extra inverters, as is often the case in static CMOS or pseudo-nMOS.

- Output defining nodes are always connected to either V_{dd} or GND through a low resistance path. This is advantageous for the noise resilience.

- The design is very modular. In effect, all gates use exactly the same topology. Only the inputs are permutated.



And/ Nand OR/NOR Xor/Nxor

Figure.3.5 Complementary pass transistor logic [1]

More complex gates can be built by cascading the standard pass-transistor modules. A CPL gate consists of two nMOS logic networks (one for each signal rail), two small pull-up pMOS transistors for swing restoration, and two output inverters for the complementary output signals. Two input multiplexer which represents the basic and minimal CPL gate structure (ten transistors).

All two-input functions (e.g. AND, OR, XOR,) can be implemented by this basic gate structure, which is relatively expensive for simple monotonic gates such as NAND and NOR. The advantages of the CPL style are the small input loads the efficient XOR and multiplexer gate implementations, the good output driving capability due to the output inverters and the fast differential stage due to the cross coupled pMOS pull-up transistors. This differential stage, on the other hand, leads to considerably larger short-circuit currents. Other disadvantages of CPL are the substantial number of nodes and high wiring overhead due to the dual-rail signals and the inefficient realization of simple gates (i.e., high transistor count, two signal inversion levels) [1].

3.3.2 SWING RESTORED PASS-TRANSISTOR LOGIC (SRPL)

The SRPL style is derived from CPL. Here, the output inverters are cross-coupled to a latch structure which performs swing restoration and output buffering at the same time. Note that the pull-up PMOS transistors are not required anymore and that the output nodes of the NMOS network are also the gate outputs. Because the inverters have to drive the outputs and must also be overridden by the NMOS network, transistor sizing becomes very difficult and results in poor output driving capability, slow switching, and large short-circuit currents. This becomes even worse when cascading SRPL gates. The resulting series of NMOS networks with competing inverters in between leads to very slow switching and

Unreliable operation. SRPL gates are highly sensitive to transistor sizing and show acceptable performance only in very special circuit arrangements (e.g., no gates in series, small output loads)[12].

3.3.3 DOUBLE PASS-TRANSISTOR LOGIC (DPL)

In the DPL style both NMOS and PMOS logic networks are used in parallel. This provides full swing on the output signals (i.e; no level restoration circuitry is needed), and circuit robustness is therefore high. However, the number of transistor especially large PMOS transistors and the number of nodes is quite high, leading to substantial capacitive loads. The combination of large PMOS transistors and inefficient dual-rail logic makes DPL not competitive compared to other pass-transistor logic styles and to complementary CMOS. Note that DPL can be regarded as dual-rail pass-gate logic[12].

3.3.4 SINGLE-RAIL PASS-TRANSISTOR LOGIC (LEAP)

Single-rail pass-transistor logic is proposed in the LEAP logic design scheme [8]. As opposed to the dual-rail logic styles, only single inter-cell wiring and single NMOS networks are required, while the required complementary input signals are generated locally by inverters. Swing restoration is realized by a fed back pull-up PMOS transistor which, however, is slower than the cross-coupled NMOS transistors of CPL working in differential mode. Note also that this swing restoration structure only works for, because the threshold voltage drop through the NMOS network for a logic "1" prevents the NMOS of the inverter and with that the pull-up PMOS from turning on. Therefore, robustness at low voltages is only guaranteed if the threshold voltages are appropriately small. On the other hand, ease-of-use of logic gates and compatibility with conventional cell-based design is partly provided in this logic style. The fact that conventional logic networks can be mapped more efficiently onto simple logic gates than on multiplexers is dealt in the LEAP system with a new synthesis approach which exploits the full functionality of multiplexer structures [12].

3.3.5 OTHER PASS-TRANSISTOR LOGIC STYLES

Some other pass-transistor logic styles have been proposed. The differential pass-transistor logic (DPTL) in [13] is a generalized dual-rail pass-transistor logic structure. It consists of the nMOS pass-transistor networks and a buffer circuit for level restoration, which can be a clocked pre charging buffer (dynamic) or a static buffer (e.g., as in CPL). In the energy economized pass -transistor logic (EEPL), the sources of the pMOS pull-up transistors of a CPL gate are connected to the complementary output signal instead of V_{dd}. The reputed advantage of shorter delay and smaller power dissipation compared to CPL, however, could

not be confirmed in this work. The push-pull pass-transistor logic (PPL) can be regarded as a CPL gate without output inverters and with complementary transistors on one signal rail [i.e., pMOS pass-transistors followed by an nMOS pull-down transistor[12].

Table 3.1 Difference between different logic styles [12]

Logic Style	# MOS networks	Output driving	I/O decouples.	Swing restores.	# rails	Robustness
CMOS	n + p	Medium	Yes	No	single	high
CPL	2n	Good	Yes	Yes	Dual	Medium
SRPL	2n	Poor	No	Yes	Dual	Low
DPL	2n + 2p	Good	Yes	No	Dual	High
LEAP	N	Good	Yes	Yes	Single	medium
EEPL	2n	Good	Yes	Yes	Dual	Medium
PPL	n + p	poor	No	Yes	Dual	low

3.4 TRANSMISSION GATE

3.4.1 BASIC CONCEPT

The structure of a CMOS transmission gate is shown in Figure 3.6. It consists of an nFET Mn in parallel with a pFET Mp such that the gates are controlled by the complementary voltages [2].

- V_g applied to the nFET, and
- $V_{dd} - V_g$ applied to the pFET.

The TG is designed to act as a voltage-controlled switch. When is high, both Mn and Mp are biased into conduction and the switch is closed; this gives an electrical conduction path between the left and right sides. If is low, then both

MOSFETs are in cutoff and the switch is open; in this case, there is no direct relationship between the voltages and the philosophy for using a parallel combination of an nFET and a pFET is straightforward to understand. An nFET cannot pass a strong logic 1 voltage, while a pFET cannot pass strong logic 0 voltages.

By paralleling the two devices, the full voltage range from 0v to can be transmitted. Setting gives the ideal situation where will reach the same value of transmission gate logic symbol. It is created using a pair of oppositely directly arrowheads to stress the fact that the device is bidirectional. From the circuit viewpoint, this means that current flow can be established in either direction. Conduction from one side to the other is controlled by the complementary switching signals X and $\overline{X}$ that are applied to the gates of the nFET and pFET.

Respectively; in the symbol, the bubble indicates the gate of the pFET. By definition, the TG acts as a closed switch when X=1, while it acts as an open switch when X=0.

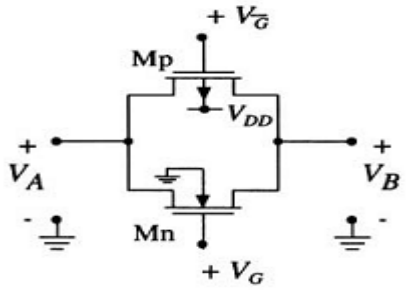


Figure.3.6 Transmission Gate [7]

Which gives the condition X = 1 (on the left side of the colon) needed to obtain the bit transfer action (on the right side of the colon). An alternate logic expression that is more useful for describing and analyzing TG-based logic networks is given by

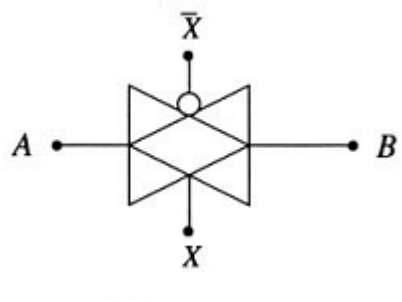
$$B = A X \tag{3.2}$$

Which is valid if X=l. Note that since we have referenced the switch control variable X to the nFET gate. Logically, the two are interchangeable, but the

electrical characteristics are distinct. There are two areas of interest when studying TG-based CMOS networks. First, it is important to understand the circuit aspects of the parallel nFET pFET pair, since this establishes the DC, transient, and layout characteristics of the switch. The second aspect deals with the use of TGs in constructing various logic gates and networks[7].

3.4.2 TG AS A TRI-STATE CONTROLLER

Before progressing deeper into the analysis, it is useful to examine the transmission gate in the context of static logic circuits. Figure. 3.6 shows a tri-state static inverter circuit that is controlled by



(a) TG Symbol

X	A	B
1	0	0
1	1	1
0	0	?
0	1	?

(b) TG Operation

Figure. 3.7 Transmission gate symbol and operation [7]

Variable X. This circuit operates as an inverter when X=1, but produces the Hi-Z state when X=0.The operational modes of the circuit are summarized in Figure.3.6. When X=1 as in (a), both of the central FETs MnX and MpX are active, and the output voltage is set by the value of In thiscase, the circuit is an inverter with additional parasitic due to MnX and MpX as shown in Figure.3.8(b).

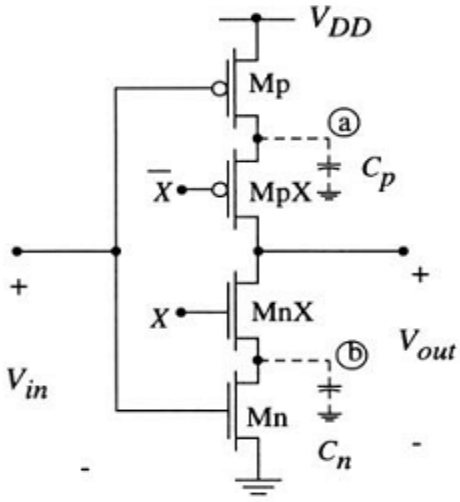
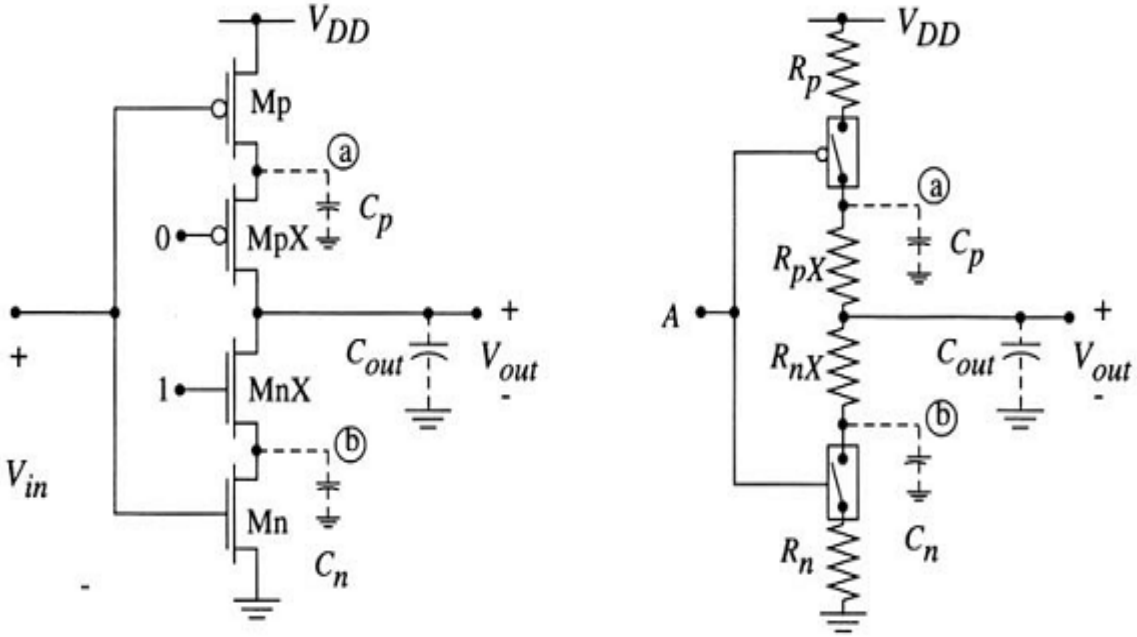
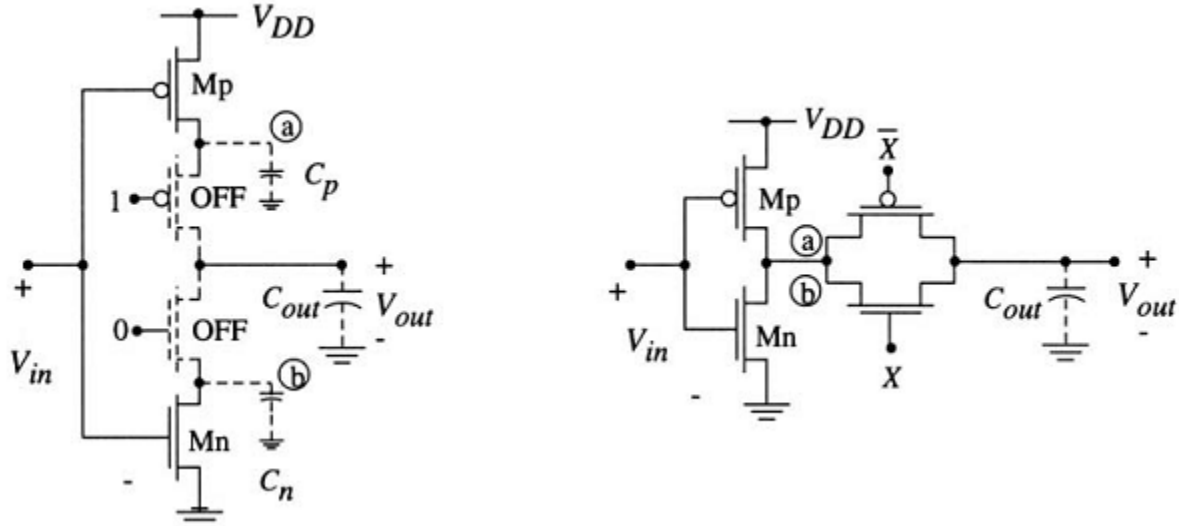


Figure.3.8 Tri State output circuit [7]



(a) Normal operation **(b) RC equivalent**

Figure.3.9 High speed state and TG equivalent [7]



(a) Isolated output node **(b) Relationship to TG output**

Figure.3.10 High impedance state and TG analogy [7]

If, on the other hand, if X=0 then both MnX and MpX are in cutoff, isolating the output node. This is shown in Figure.3.9 (a). The relationship to the TG circuit is shown in Figure3.9 (b), where we have deformed the circuit and connected nodes a and b together to yield an inverter with its output directed through a transmission gate. The TG may thus be used as a switch to control the data flow through a static logic network. However, it is possible to use the transmission gate as a general logic-controlled switch to synthesize complex logic functions.

Modern high-density, high-performance chip designs, however, are severely limited by interconnect. This constraint has led designers to question the need for using the nFET/pFET pair required in the TG. The FET itself is not a problem because of its small size. The wiring, on the other hand, can be significant, especially when TGs are distributed throughout a complex system layout. Owing to this consideration, many modern designs tend to shy away from using TGs, opting instead for single nFETs in their place. In principle, any TG-based network can be converted to using nFETs only so long as we modify the electrical characteristics where needed [7].

CHAPTER 4

DESIGN METHODOLOGY OF GATE DIFFUSION INPUT TECHNIQUE

4.1 BASIC GATE DIFFUSION INPUT (GDI) FUNCTION

The GATE DIFFUSION INPUT (GDI) method is based on the use of a simple cell. At first glance, the basic cell reminds one of the standard CMOS inverter, but there are some important differences.

- The GDI cell three inputs: G (Common gate input of NMOS and PMOS), P (input to the source/drain of PMOS), and N (input to the source/drain of PMOS).
- Bulks of both NMOS and PMOS are connected to N or P (respectively), so it can be arbitrarily biased at contrast with a CMOS inverter.

It must be remarked that not all of the functions are possible in standard p-well CMOS process but can be successfully implemented in twin-well CMOS or silicon on insulator (SOI) technologies [11] [17].

Table 4.1 shows how a simple change of the input configuration of the simple GDI cell corresponds to very different boolean functions. Most of these functions are complex (6–12 transistors) in CMOS, as well as in standard PTL

implementations, but very simple (only two transistors per function) in the GDI design method. Most of the designed circuits were based on the F1 and F2 functions.

The reasons for this are as follows.

- Both F1 and F2 are complete logic families (allows realization of any possible two-input logic function) [11].
- F1 is the only GDI function that can be realized in a standard p-well CMOS process, because the bulk of any NMOS is constantly and equally biased [11].

When N input is driven at high logic level and P input is at low logic level, the diodes between NMOS and PMOS bulks to Out are directly polarized and there is a short between N and P, resulting in static power dissipation and $V_{out} \sim 0.5V_{dd}$.

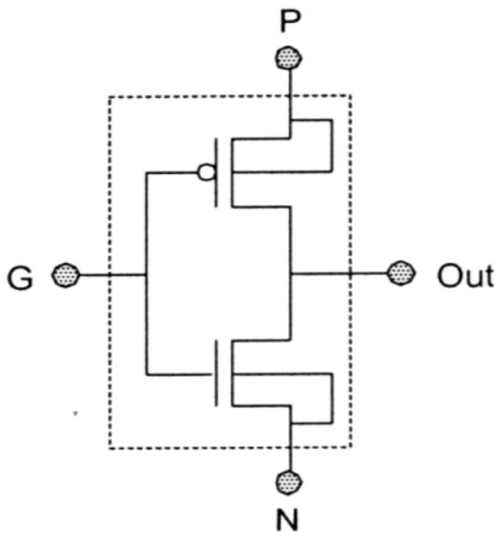


Figure. 4.1 GDI basic cell [11]

This cause a drawback for OR, AND, and MUX implementations in regular CMOS with configuration. The effect can be reduced if the design is performed in floating-bulk SOI technologies, where a full GDI library can be implemented. In that case, floating-bulk effects have to be considered [11].

As can be seen, the GDI cell structure is different from the existing PTL techniques, and has some important features, which allow improvements in design complexity level, transistor count, and power dissipation. Understanding of GDI cell properties demands a deeper operational analysis of the basic cell in different cases and configurations.

Table 4.1 various logic functions [11].

N	P	G	OUT	FUNCTION
'0'	B	A	$\bar{A}B$	F1
B	'1'	A	$\bar{A} + B$	F2
'1'	B	A	A + B	OR
B	'0'	A	AB	AND
C	B	A	$\bar{A}B + AC$	MUX
'0'	'1'	A	$\bar{A}$	NOT

4.2 ANALYSIS OF GDI CIRCUITS

In this section, we analyze GDI circuits. First we explain their operation and analyze their transient behavior. Then we consider wing restoration issues and switching characteristics.

- Operational Analysis of GDI Cell One of the common problems of PTL design methods is the low swing of output signals because Of the threshold drop across the single-channel pass transistors. In existing PTL techniques, additional buffering circuitry issued to overcome this problem.
- To understand the effects of the low swing problem in a GDI cell, let us take following analysis, based on the example of F1 function, and can be easily extended to use in other GDI functions. Table II presents a full set of logic states and related functionality modes of F1.

As can be seen from Table 4.2, the only state where low swing occurs in the output value is A = 0, B = 0. In this case, the voltage level of F1 is V_{tp} (instead of the expected 0 V) because of the poor high-to-low transition characteristics of the PMOS pass transistor [4]. It is obvious that the only case (among all the possible transitions) where the effect occurs is the transition from A = 0, B = V_{dd} to A = 0, B = 0 [17].

The fact that demands special emphasis is that in about 50% of the cases (for B =1) the GDI cell operates as a regular CMOS inverter, which is widely used as a digital buffer for logic-level restoration.

Table 4.2 Functionality of F1 function [11]

A	B	Functionality	F1
0	0	pMOS trans Gate	V_{tp}
0	1	CMOS Inverter	1
1	0	nMOS trans gate	0
1	1	CMOS inverter	0

When V_{dd} without a swing drop from the previous stages, a GDI cell functions as an inverter buffer and recovers the voltage swing. Although this feature allows a self-swing restoration in certain cases. But it is applicable only in certain cases which can be a drawback.

4.3 TRANSIENT ANALYSIS

The exact transient analysis for a basic GDI cell, in most cases, is similar to a standard CMOS inverter. This classic analysis is based on the Shockley model, where the drain current I_d is expressed as follows:

$$I_d = k \{ (\mathrm{Vgs} - \mathrm{Vth}) \mathrm{V_{ds}} - 0.5\mathrm{V^2_{ds}} \} \quad (4.1)$$

Where K is drivability factor, V_{th} is threshold voltage, W is channel width, and L is channel length.

In contrast with CMOS inverter analysis, where V_{gs} was taken as an input voltage, in most of GDI circuits V_{gs} must be considered as a variable of input voltage in the Shockley model.

The case of most interest is when a step signal is supplied to diffusion of NMOS transistor and causes a swing drop in output. During this response, the NMOS transistor passes from saturation to sub threshold region. In assuming the fast transition in the input, the linear region can be neglected in our analysis. Analytical expressions that describe the transient response can be derived from (4.1), while considering capacitive load in the output [11].

The capacitive current is-

$$Ic = C\frac{dVs}{dt} = I_d \tag{4.2}$$

Where C is the output capacitance, V_{gs} is the voltage across the capacitance C_L, I_c is the current charging the capacitor, and I_d is the drain current through the N-channel device. The expression for V_s as a function of time is derived as follows:

In saturation region:

$$C\frac{dVs}{dt} = 0.5\ k\ (Vgs\ -\ \mathrm{Vt})\ 2 = 0.5\ \mathrm{k}\ (\mathrm{V}_{dd} - \mathrm{V}_t - \mathrm{V}_S)^2 \tag{4.3}$$

Where, in the case of GDI cells linked through diffusion inputs, the capacitance C includes both diffusion and well capacitances of the driven cell.

The integral form of (4.3) is

$$\int \frac{\mathrm{dVs}}{0.5\mathrm{k}(\mathrm{V}_{dd}-\mathrm{Vt}-\mathrm{Vs})^2} = \int \frac{\mathrm{dt}}{\mathrm{C}} \tag{4.4}$$

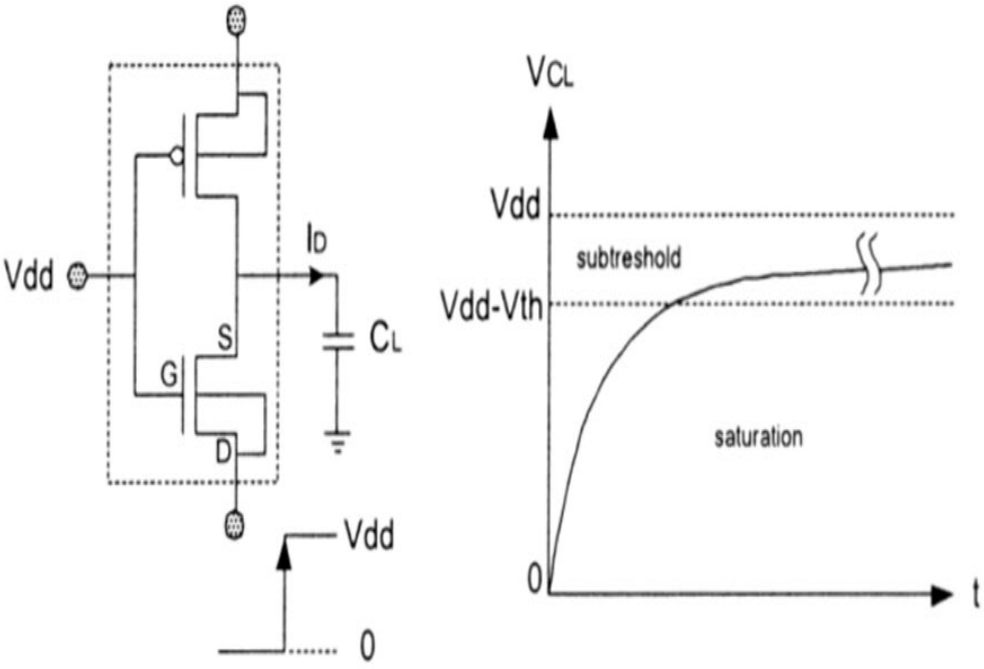


Figure.4.2 Transient response of GDI cell [11]

The same expression can be written as

$$\int \frac{dV_s}{aVs^2+bVs+c} = \int dt \tag{4.5}$$

Where $a = \frac{0.5k}{C}$, $b = \frac{-k\,(V_{dd}-V_t)}{C}$, $c = \frac{0.5k\,(V_{dd}-V_t)^2}{C}$ (4.6)

Where a, b, and c are constants of the process or the given circuit. The final expression of transient response in the saturation region is

$$t + k_1 = \frac{1}{\sqrt{b^2-4ac}} \ln\left(\frac{2aV_s+b-\sqrt{b^2-4ac}}{2aV_s+b+\sqrt{b^2-4ac}}\right) \tag{4.7}$$

Where t is time in the saturation region and k_1 is a constant of integration and is calculated for initial conditions (t =0, V_s = 0). The solution of (4.7) is done numerically for specific values of (a, b, c).

After entering the sub threshold region, V_s continues rising while the output capacitance is charged by I_d according to (4.1).

In sub threshold region:-

$$C\frac{dV_s}{dt} = I_{D0}\left(\frac{W}{L}\right)e^{\left(\frac{qV_{gs}}{KT}\right)} \tag{4.8}$$

$$= I_{D0}\left(\frac{W}{L}\right)\frac{e^{\left(\frac{qV_{dd}}{kT}\right)}}{e^{\left(\frac{qV_{gs}}{KT}\right)}} \tag{4.9}$$

$$\int dV_s e^{\left(\frac{qV_{gs}}{KT}\right)} \cdot A = \int dt \tag{4.10}$$

Where T is temperature in K, k is Boltzmann's constant, q is charge of an electron, and A is a constant.

$$A = \frac{C}{I_{D0}\left(\frac{W}{L}\right)e^{\left(\frac{qV_{dd}}{KT}\right)}} \tag{4.11}$$

The expression for response in the sub threshold region is-

$$t + k_1 = \frac{e^{\left(\frac{qV_{gs}}{KT}\right)}}{q/kt} \cdot A \tag{4.12}$$

$$k_2 = \frac{e^{\frac{q(V_{dd}-V_t)}{kT}}}{q/kt} \cdot A \tag{4.13}$$

Where k_2 is constant of integration defined by the initial conditions, A is from (4.10), and V_t is the threshold voltage.

It must be noted that the analysis of propagation delay of a basic GDI cell given by (4.2)–(4.7) can be refined by taking into account the effect of the diode

between the NMOS source and body. This diode is forward biased during the transient. By conducting an additional current, it contributes to charging the output capacitance C_L. This current contribution can be calculated to be

$$I_{BS} = I_0 \left(e^{(q[V_{dd}-V_s]/nkT)} - 1\right) \quad (4.14)$$

Where I_{BS} the diode is current, I_0 is the reverse current, and n is a factor between one and two. This current should be added in (4.2) to derive an improved propagation delay, resulting in a faster transient operation of GDI cell [17] [11].

4.4 ANALYSIS OF SWING-RESTORING BUFFERS

An important concern in PTL circuit design is the problem of swing degradation. This section presents a methodology for swing restoration in GDI circuits under constraints of area (power) and circuit frequency (delay).

The simplest method of swing restoration is to add a buffer stage after every GDI cell. This will certainly prevent the voltage drop, but the payment will be in additional area, delay, and power dissipation, which makes this method highly inefficient Note that our approach to swing restoration is rather simple; various buffering techniques are presented in the literature. Given a clocked logic circuit with known T_{cycle} and T_{setup}, buffering of cascaded GDI cells will be optimal if the following conditions are preserved [11] [17].

4.4.1 SUCCESSIVE SWING RESTORATION

While cascading GDI cells, each cell contributes a voltage drop in the output that is equal toV_{drop}. Assuming $0.3V_{dd}$ as a maximal allowed voltage drop of the whole cascade, the number of linked GDI cells between two buffers is limited by

$$N_1 = \frac{0.3V_{dd}}{V_{drop}} \tag{4.15}$$

As shown above, after exiting the saturation area, the value of V_{drop} is equal to V_{th} and decreasing with time as follows, using (4.9):

$$V_{drop} = V_{dd} - V_t = V_{dd} - \frac{\ln\left(\frac{(t+k_2)\frac{q}{kT}}{A}\right)}{q/kT} \tag{4.16}$$

Equation (4.16) applies for sub threshold region only, namely, for $V_S < V_{dd.}$

According to (4.16), remaining in the sub threshold region for t_2 will assure a significant decrease of V_{drop} and as a result, increasing in the number of linked cells N_1.This allows achieving Successive swing restoration while using a lower number of buffers.

If interconnection effects are essential, a signal potential loss over long interconnects has to be treated. In this case, will be extended with respect to IR drop.

Suppose that the V_{dd} voltage has to be applied to the drain input of the NMOS through a long wire. For given W and L dimensions, the resistance of the interconnect is defined by

$$R = \boldsymbol{\rho}_{square}\frac{L_{wire}}{W_{wire}} \tag{4.17}$$

Where $\boldsymbol{\rho}_{square}$ is a metal sheet resistance per square.

The current following through the wire I_{wire} and causing the voltage drop is given by-

$$I_{wire} = \frac{V_{dd} - V_{drain}}{R} \tag{4.18}$$

V_{drain} can be determined by equalization between the wire and nMOS transistor's current as follows-

$$\frac{V_{dd} - V_{drain}}{R} = I_d \tag{4.19}$$

Where I_d is found from (4.1) according to the operation region of the transistor Equations (4.19) can be solved numerically, and its contribution to the final V_{drop} expression is represented by-

$$V'_{drop} = V_{drop} + (V_{dd} - V_{drain}) \tag{4.20}$$

With V_{drop} from (4.16). The operation in the subthreshold region causes increase of delay. Therefore, this method can be efficiently used mostly in low-frequency design.

Scaling, namely, V_{dd} reduction and threshold non scalability, influences the number of required buffers in GDI design equation (4.15). As a result, when operation with the lower supply voltages is performed, while the same technology and V_T remain, insertion of additional buffers has to be considered. The direct impact of this is on the area and number of gates.

Finally, several points have to be emphasized concerning the buffer insertion topology in GDI.

- Buffer insertion has to be considered only in the case of linking GDI cells through diffusion inputs. No buffers are needed before gate inputs of GDI cells.
- Due to this feature, the "mixed path" topology can be used as an efficient method for buffer insertion. It allows one to reduce the number of buffers by intermittently involving diffusion and gate input in a given signal path.
- The designer should check the tradeoff between buffer insertion and delay, area, and power consumption to achieve an efficient swing restoration.

4.5 IMPACTS OF PROCESS VARIATION ON SWING RESTORATION

In every VLSI process, there is variation in parameters like threshold tracking, variations, etc. The process dependence of V_{th} and I_{D0} influence the value of and the swing restoration in GDI. This effect can be best described by defining a sensitivity of to the mentioned parameter variations as follows:

Current sensitivity of

$$V_{drop} = \frac{\partial V'drop}{\partial I_{do}} \tag{4.21}$$

$$V_{drop} = \frac{\partial V'drop}{\partial V_T} \tag{4.22}$$

4.6 SWITCHING CHARACTERISTICS: GDI V/s CMOS

Due to the complexity of the logic function that can be implemented in a GDI cell by using only two transistors; it is important to perform a comparison of its witching characteristic with CMOS.

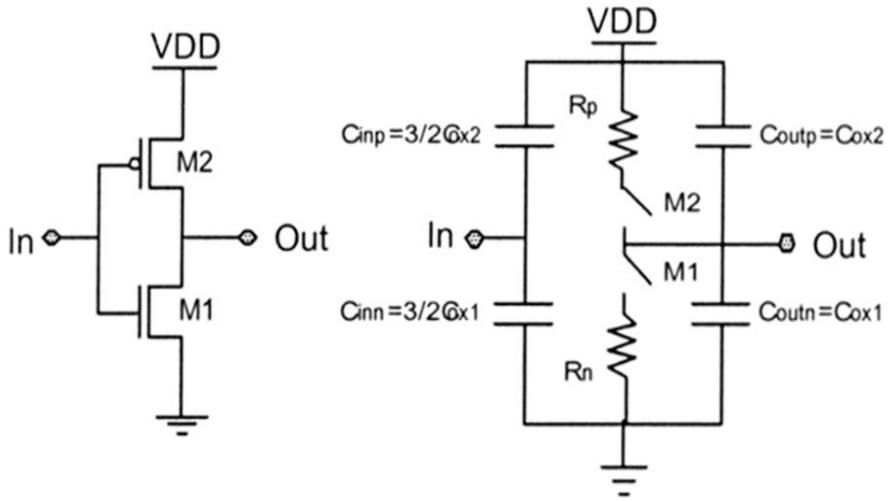


Figure.4.3 the CMOS inverter and its digital model [11]

Gate, whose logic function is of the same order of complexity. This comparison can be used as a base for delay estimation in early stages of circuit design, if GDI or CMOS design techniques are considered.

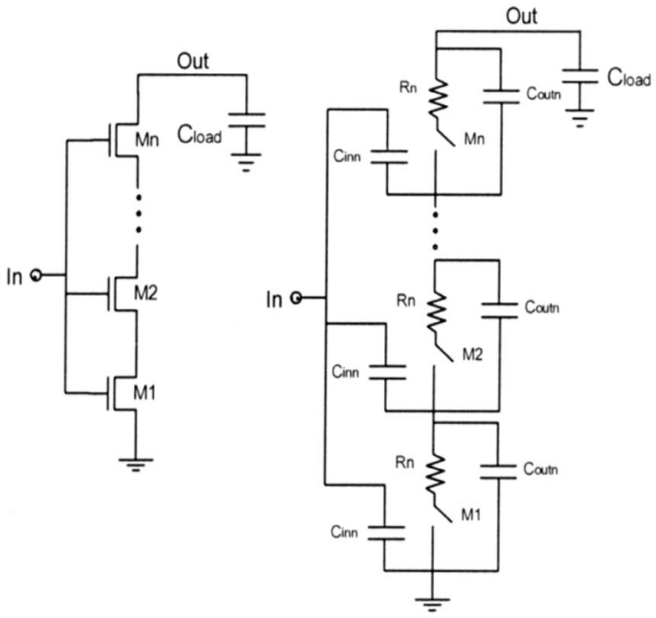


Figure.4.4 Series connection of MOSFETs and its digital model [11]

While a GDI cell's characteristics are close to a standard inverter, the gate with equivalent functional complexity in CMOS will be NAND. The switching behavior of the inverter can be generalized by examining the parasitic capacitances and resistances associated with the inverter. Consider the inverter shown in Figure.4.2 with its equivalent digital model.

The propagation delay for an inverter driving a capacitive load is

$$t_{phl} = R_n \ C_{tot} = R_n \ (C_{out} + C_{load}) \qquad (4.23)$$

Where C_{tot} is the total capacitance on the output of the inverter, that is, the sum of the output capacitance of the inverter, any capacitance of interconnecting lines, and the input capacitance of the gate(s).

A NAND gate with a series connection of identical n-channel MOSFETs is shown in Figure 4.3. We can estimate the intrinsic switching time of series-

connected MOSFETs with an external load capacitance by [6]

$$t_{PHL} = N.R_n\left(\frac{C_{load}}{N} + C_{load}\right) + 0.35.R_n.C_{inn}(N-1)^2 \quad (4.24)$$

The first term in this equation represents the intrinsic switching time of the series connection of n MOSFETs, while the second term represents RC delay caused by R_n chargingC_{inn}.

For C_{inn} equal to 3/2C_{ox} and assuming two serial n-MOS transistors, the propagation delay in NAND gate

$$t_{phl} = 1.52\ R_n C_{out} + 2\ R_n C_{load} \quad (4.25)$$

Therefore, the delay of a NAND gate compared to a GDI gate is approximated by

$$1.52 \leq \frac{t_{PHL(CMOS)}}{t_{PHL(GDI)}} \leq 2 \quad (4.26)$$

Where the high bound is for high C_{load} and the low bound is for low C_{load}.

4.7 FAN-IN AND FAN-OUT BOUNDS IN GDI

4.7.1 FAN-OUT

The logic effort is directly related to the fan-out when the effort delay of a logic structure is analyzed. The effort delay of the logic gate is the product of these two factors.

$$F = g.h \quad (4.27)$$

Where f is the effort delay, g is the logic effort, and h represents a fan-out of the

gate. For a desired delay, reducing the logic effort results in an improved fan-out by the same ratio.

The values of logic effort for inputs of various static CMOS gates normalized comparatively to the logic effort of inverter. While a GDI cell's logic effort is close to a standard inverter, the equivalent logic functions in CMOS will be NAND, NOR, or MUX, depending on GDI input configuration. If the diffusion input is considered, an additional factor has to be applied to represent the capacitance ratio between the gate and diffusion inputs: the given above factors have to be multiplied by C_{gate} / C_{diff} .Both parameters are defined by the design technology.

4.7.2 FAN-IN

*A*n (n + 2) input GDI cell can be implemented by extension of any n-input CMOS structure. While the stack of serial MOSFET devices and fan-in in CMOS gates are limited by body-effect considerations, the addition of diffusion inputs in GDI for the same structure results in an improved fan-in, defined by

$$\text{Fan-in}_{GDI} = \text{Fan-in}_{CMOS} + 2 \tag{4.28}$$

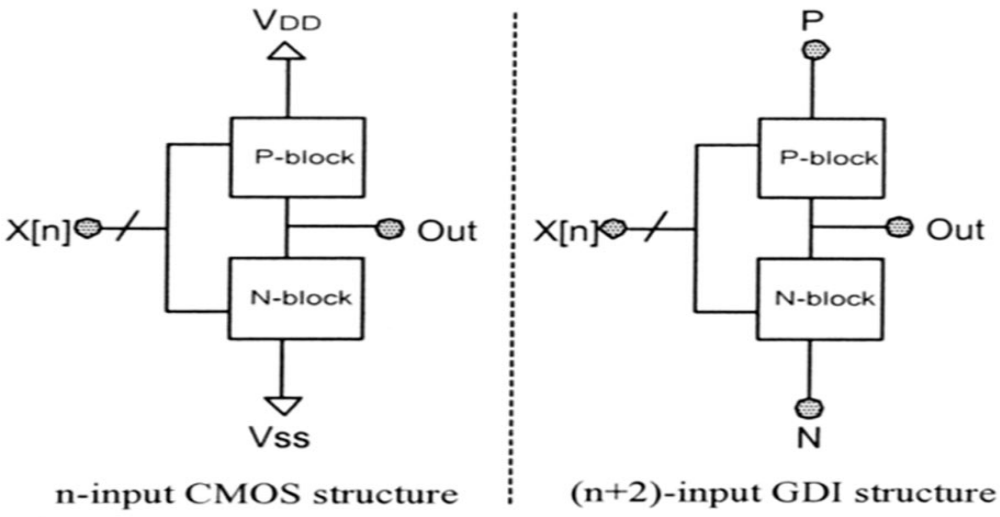


Figure4.5 General GDI cell implement [11].

The examples of GDI functions given in Table 4.1 refer only to extension of a single-input CMOS inverter structure to a triple- input GDI cell in order to achieve implementation of complicated logic functions with a minimal number of transistors. Actually, this approach can be defined in more general form.

Extension of any n-input CMOS structure to an (n + 2) input GDI cell can be done by introducing an input P instead of supply voltage V_{dd} in the PMOS block of a CMOS structure and an input N instead of V_{ss} in the nMOS block.

This extended implementation can be represented by the following logic expression:

$$Out = \overline{F}\ (x_1 \dots \dots . x_n)P + F(x_1 \dots \dots . x_n)N \tag{4.29}$$

Where $F(x_1 \dots \dots . x_n)$ is a logic function of an nMOS block (not of the whole original n-input CMOS structure).

Due to their special properties, GDI cells can be successfully used for low-power design of combinational circuit where transitions of logic values are prevented from propagating through the circuit if the final result does not change as a result of those transitions [11] [17].

CHAPTER 5 DESIGN AND ANALYSIS OF LOW POWER CMOS CELL STRUCTURES

All the design structures based on CMOS Logic and Gate Diffusion Input are designed and simulated using standard TSMC 0.18 µm CMOS technology and 3.3 V voltage supply at an operating temperature of 27º C. Cadences Corporation based tool known as IC station Cadence IC5141 have been used for all the design and analysis. The basic cells, for example, Inverter, Two-Input AND Gate, Two-Input OR Gate, Two-Input Exclusive-OR Gate, Half Adder, One-Bit Full Adder are designed and analyzed with appropriate sizing.

5.1 DESIGN AND SIMULATION FOR A CMOS INVERTER

The first basic cell which the VLSI designers implements and analyze is the basic CMOS Inverter. Here also this thesis work starts with the designing of the basic CMOS Inverter of minimum transistor size. The standard TSMC 0.18 μm CMOS technologies have been used and a load capacitance of 5 fF is used. The transient analysis is done by use of the ASSURA (Virtuoso) Simulator of Cadence Corporation. The basic structure of a CMOS Inverter is shown in Figure 5.1.

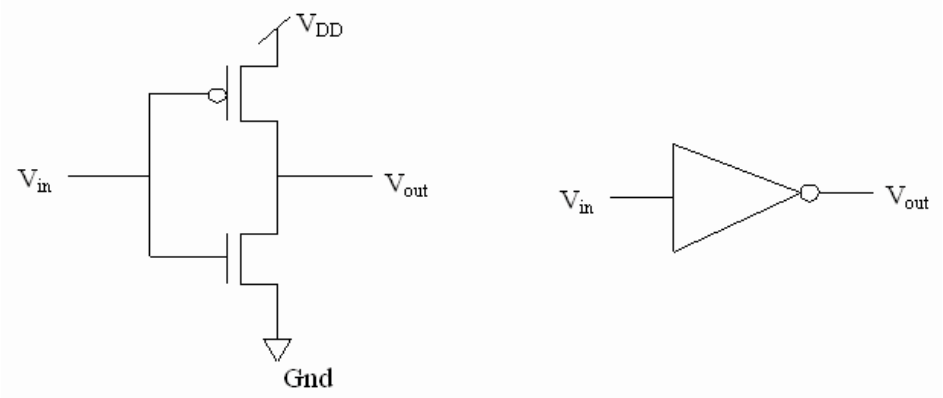
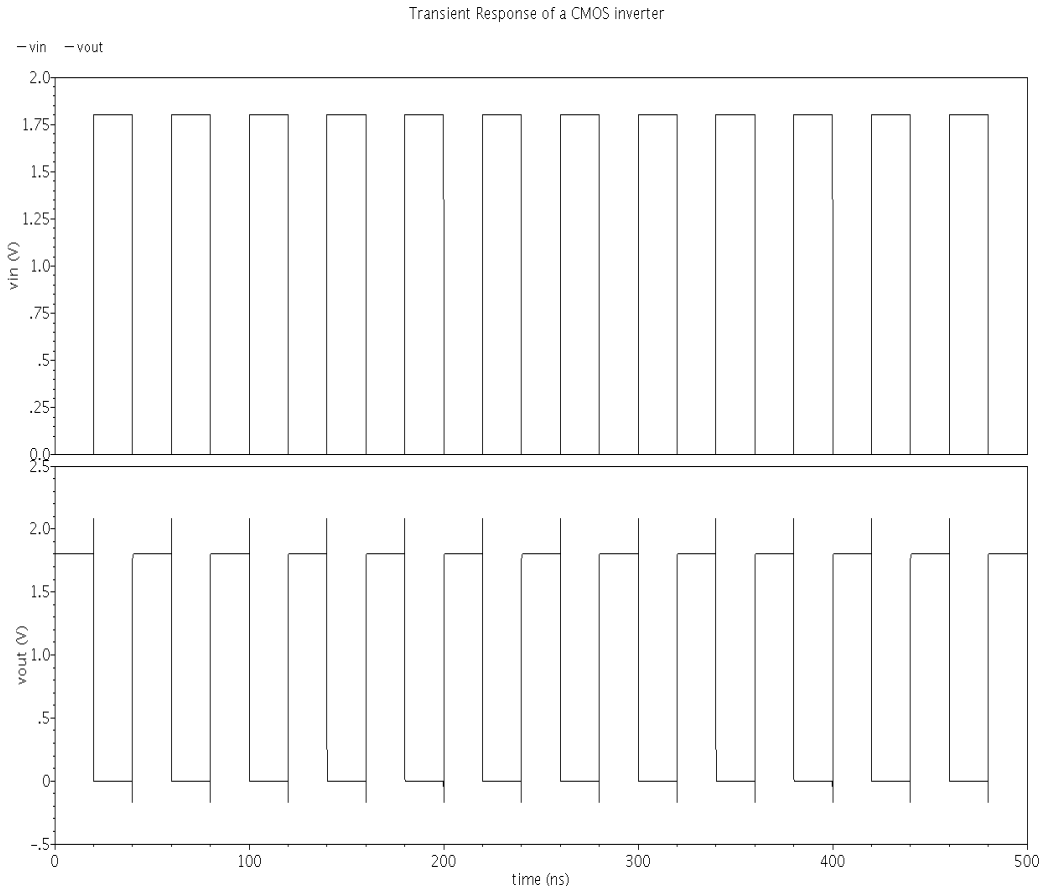


Figure 5.1. The Basic Structure of CMOS Inverter.

The transient simulation results are as shown in the Figure 5.2 below.



(a)

(b)

Figure 5.2. Simulation Results of CMOS Inverter.

(a) Input Signal,

(b) Voltage Waveform of Output Signal.

5.2 DESIGN AND SIMULATION FOR A TWO-INPUT CMOS AND GATE

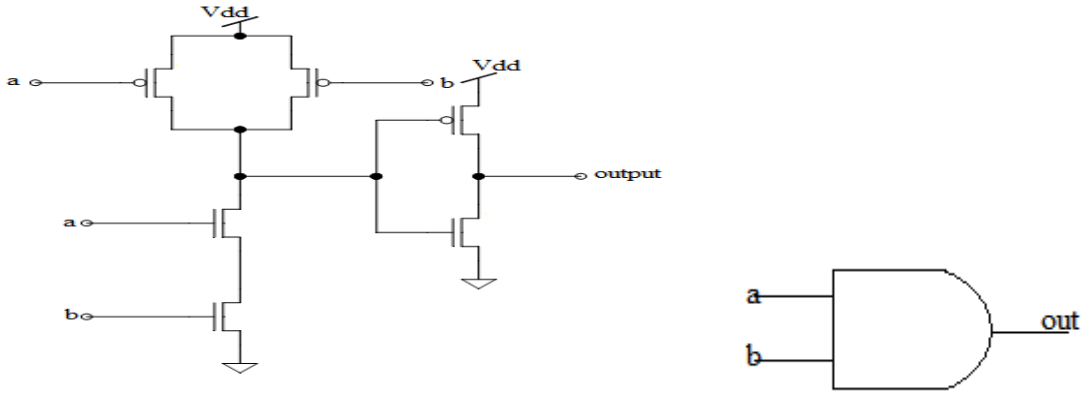
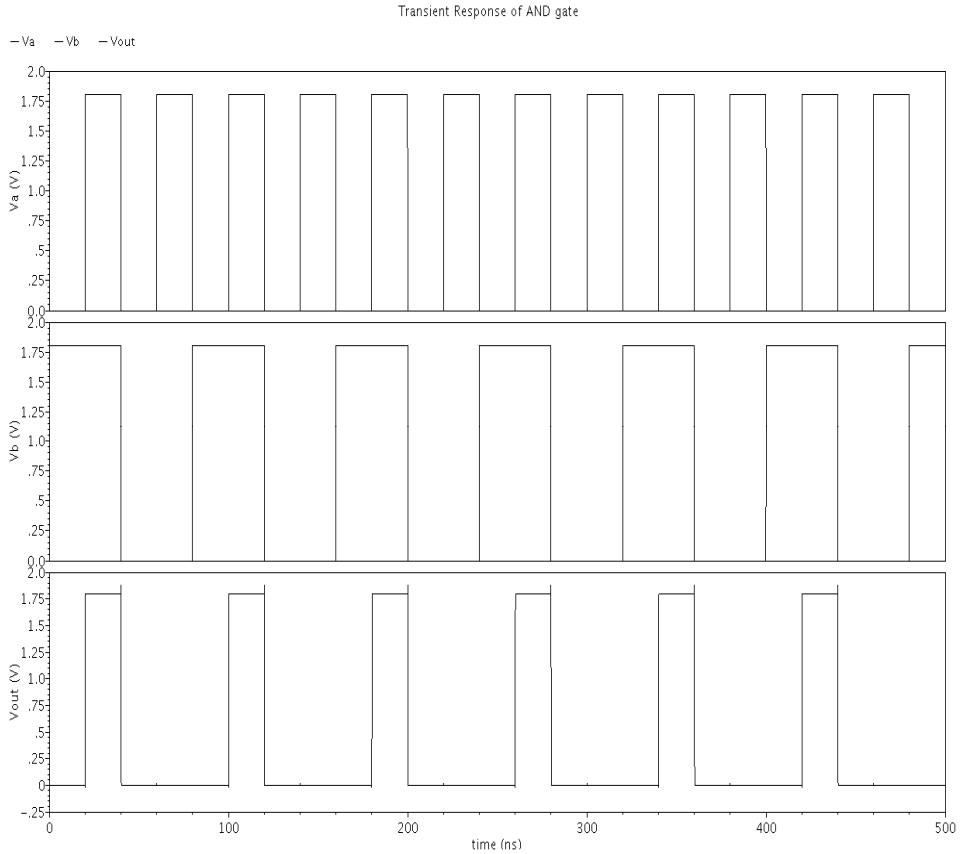


Figure 5.3 The Basic Structure of a Two-Input CMOS AND Gate



(a)

(b)

(c)

Figure 5.4 Simulation Results of Two-Input CMOS AND Gate

(a) Input Signal (VA), (b) Input Signal (VB),
(c) Voltage Waveform of Output Signal.

5.3 DESIGN AND SIMULATION FOR A TWO-INPUT CMOS OR GATE

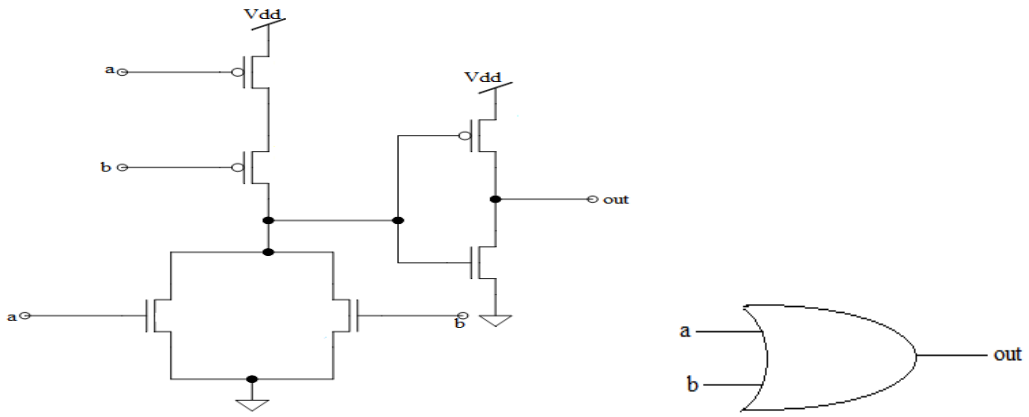
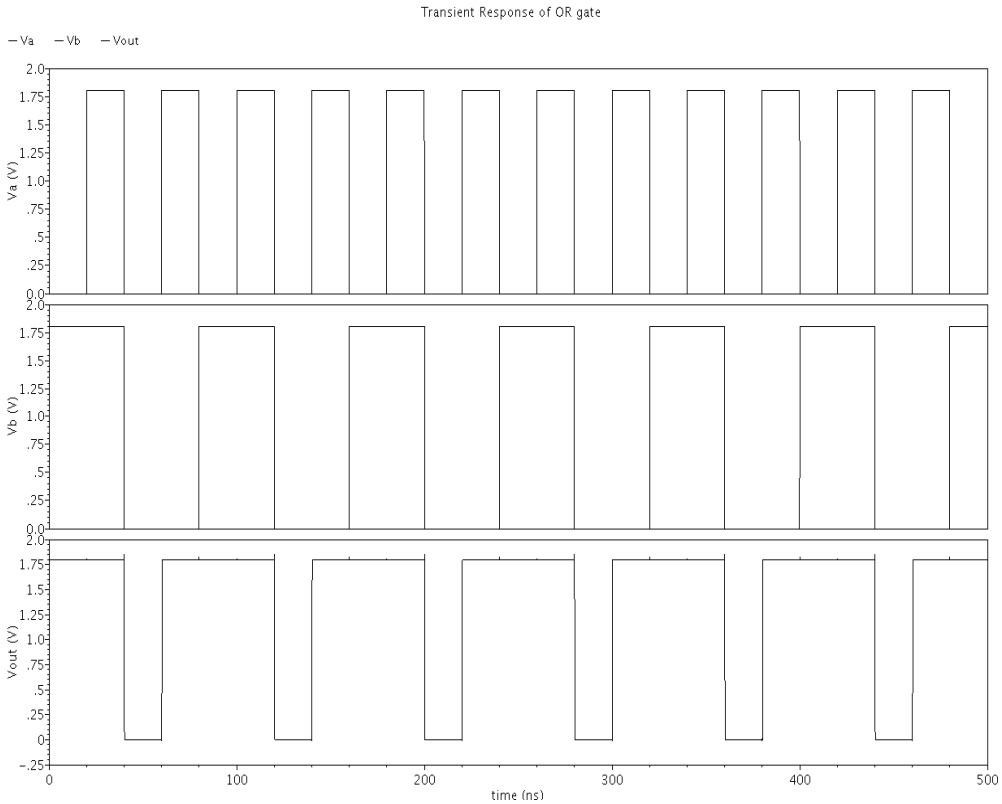


Figure 5.5 The Basic Structure of a Two-Input CMOS OR Gate



(a)

(b)

(c)

. Figure 5.6 Simulation Results of Two-Input CMOS OR Gate
(a) Input Signal (VA), (b) Input Signal (VB),
(c) Voltage Waveform of Output Signal.

5.4 DESIGN AND SIMULATION FOR A TWO-INPUT CMOS XOR GATE

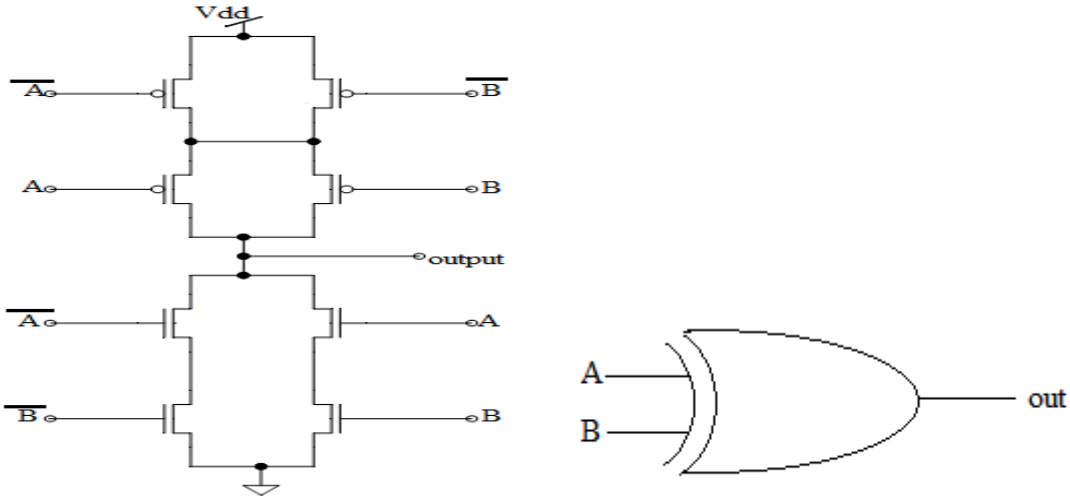
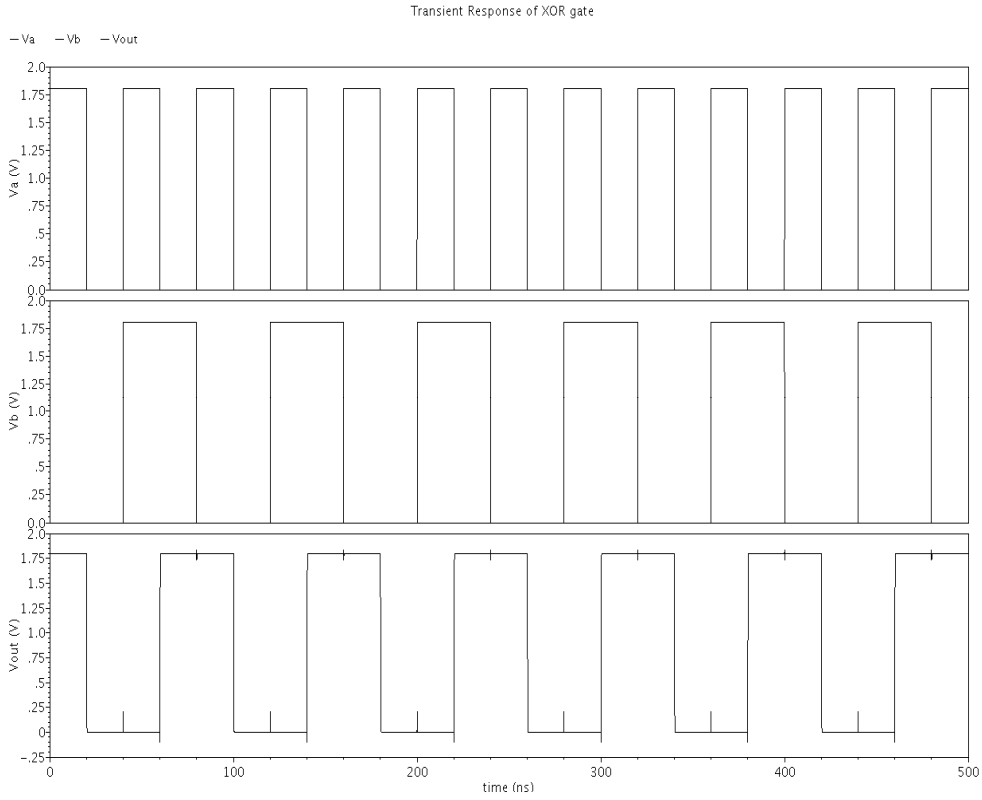


Figure 5.7 The Basic Structure of a Two-Input CMOS XOR Gate



(a)

(b)

(c)

Figure 5.8 Simulation Results of Two-Input CMOS XOR Gate
(a) Input Signal (VA), (b) Input Signal (VB),
(c) Voltage Waveform of Output Signal.

5.5 DESIGN AND SIMULATION FOR A CMOS HALF ADDER

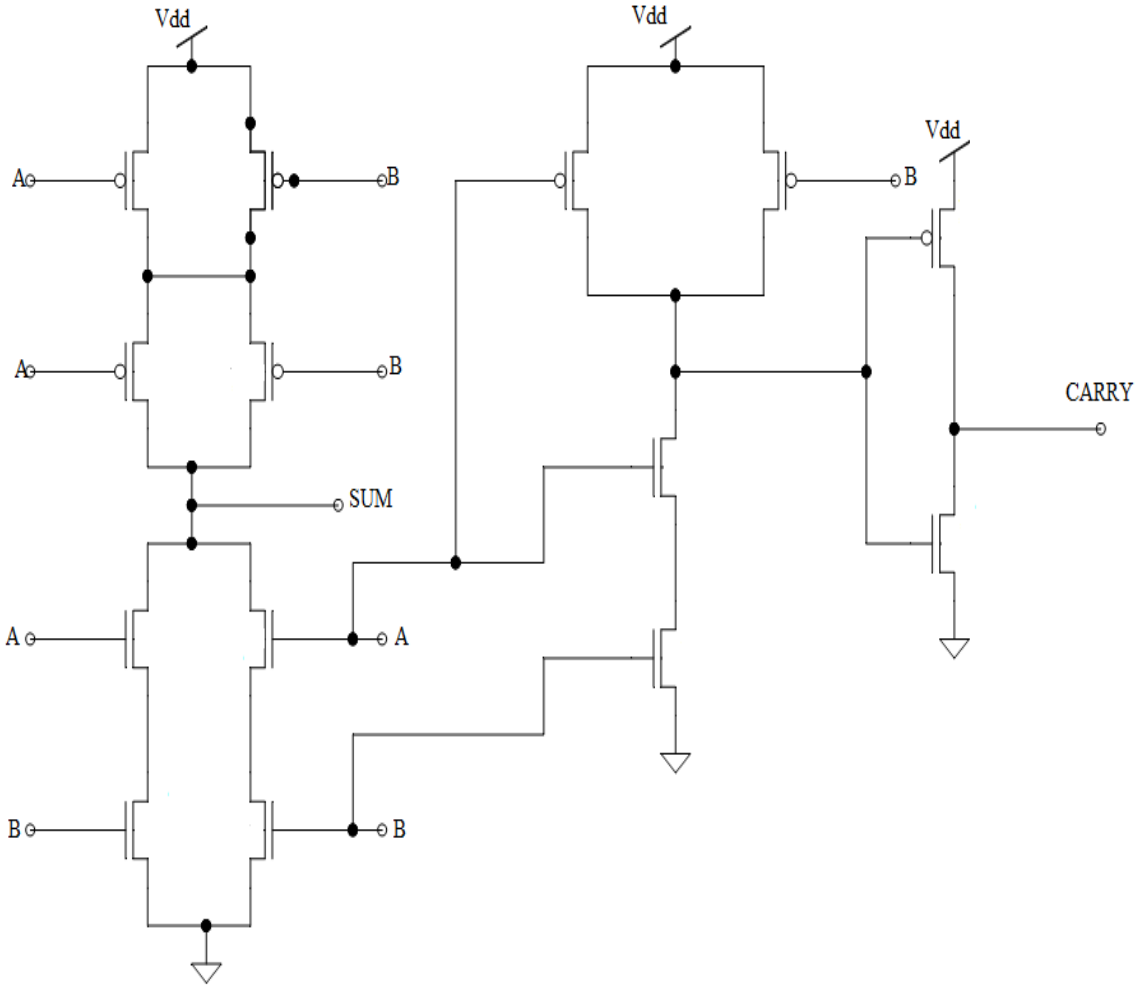


Figure 5.9 The Basic Structure of a CMOS HALF Adder.

The transient simulation results of CMOS based HALF adder are as shown in the Figure 5.10 below.

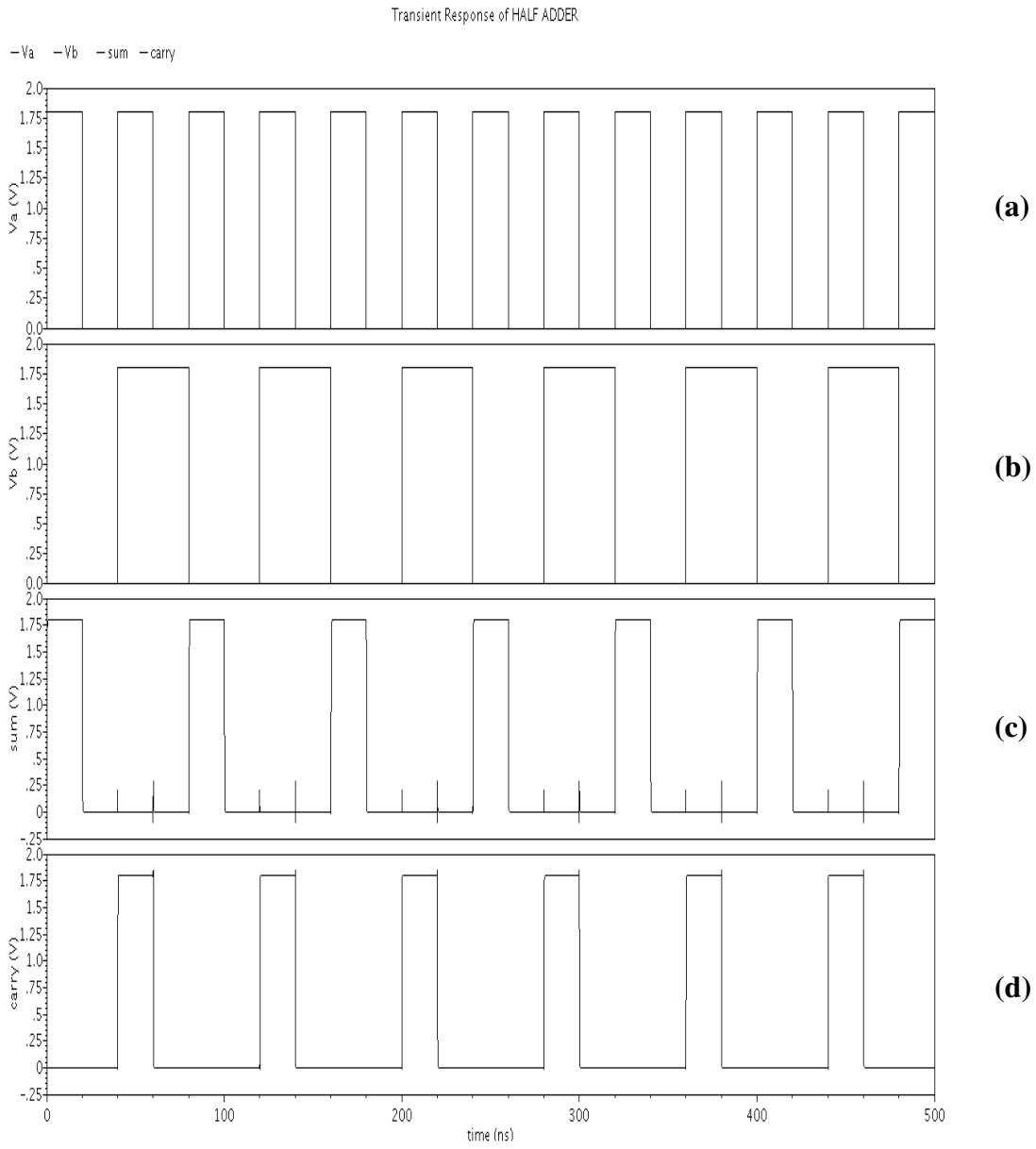


Figure 5.10 Simulation Results of CMOS based HALF adder
(a) Input Signal (VA), (b) Input Signal (VB)
(c) Output Waveform of sum, (d) Output Waveform of carry

5.6 DESIGN AND SIMULATION FOR ONE-BIT CMOS FULL ADDER

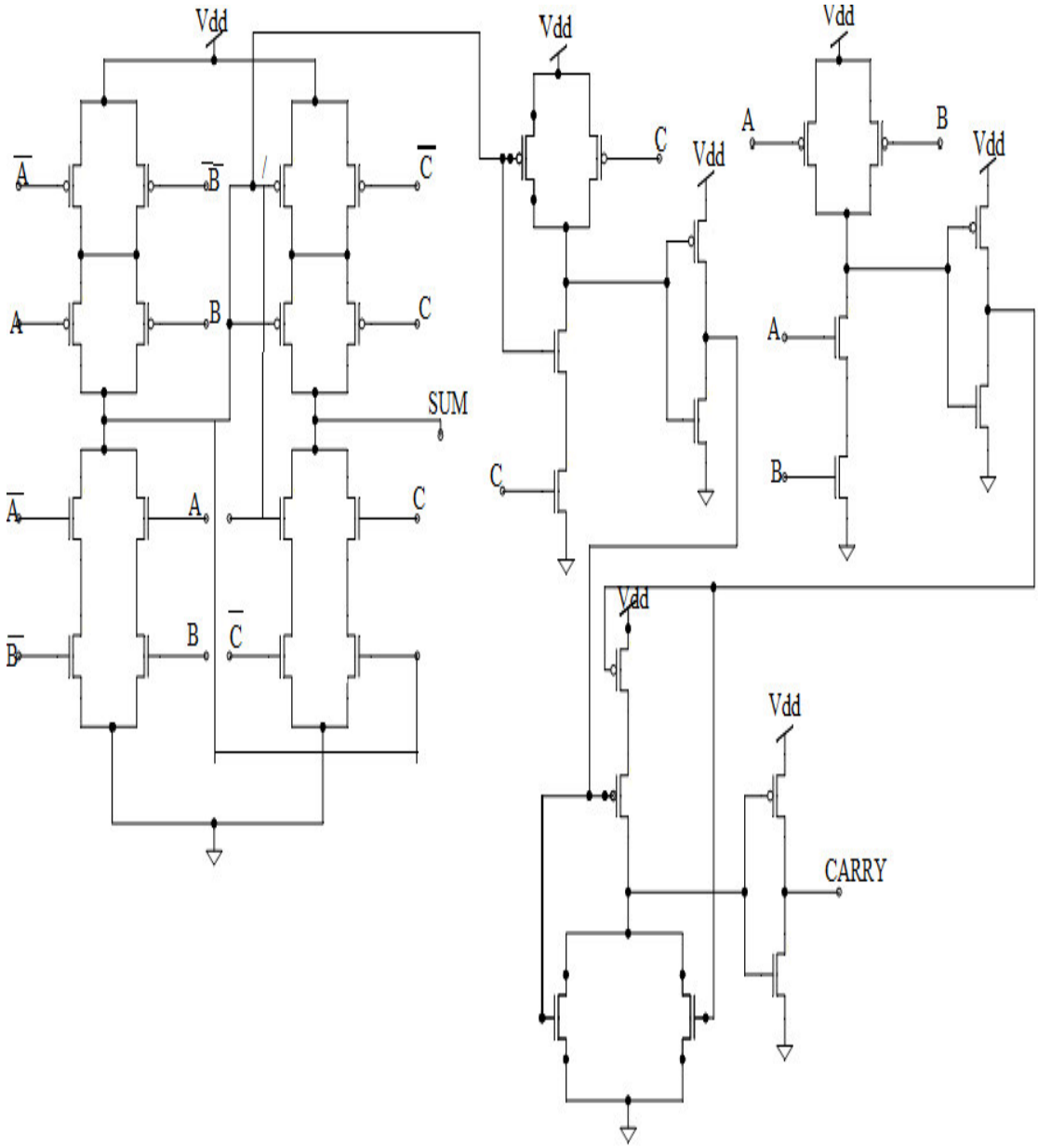


Figure 5.11 The Basic Structure of a ONE-BIT CMOS FULL Adder.

The transient simulation results of CMOS based FULL adder are as shown in the Figure 5.12 below.

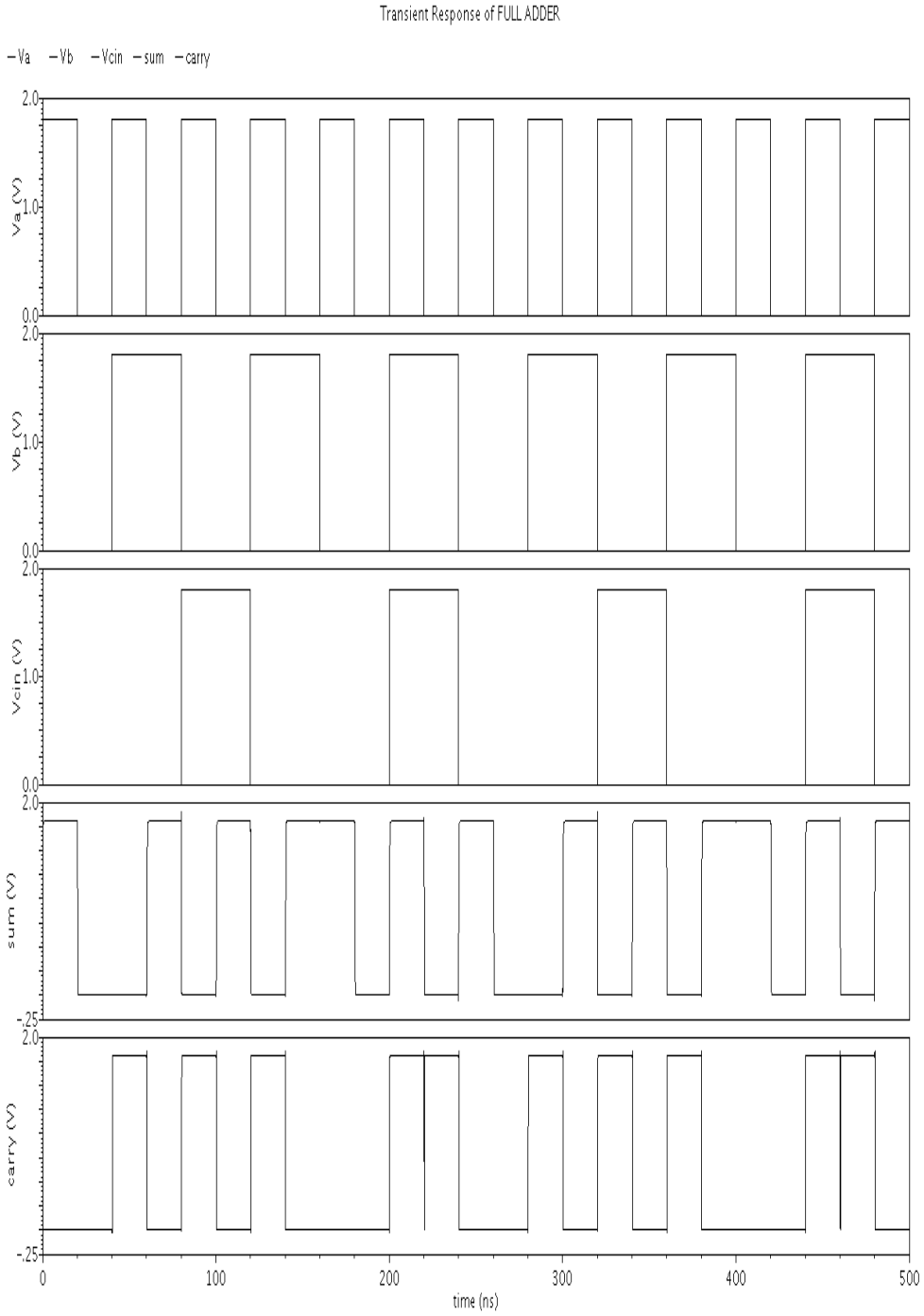


Figure 5.12 Simulation Results of one-bit CMOS Full adder.

(a) Input Signal (VA), (b) Input Signal (VB), (c) Input Signal (Vcin)

(d) Output Waveform of sum, (e) Output Waveform of carry

5.7 DESIGN AND SIMULATION FOR A TWO-INPUT AND GATE BASED ON GDI TECHNIQUE

A two-input AND gate based on GDI technique is shown in Figure 5.13 and simulated waveforms are as shown in Figure 5.14, respectively.

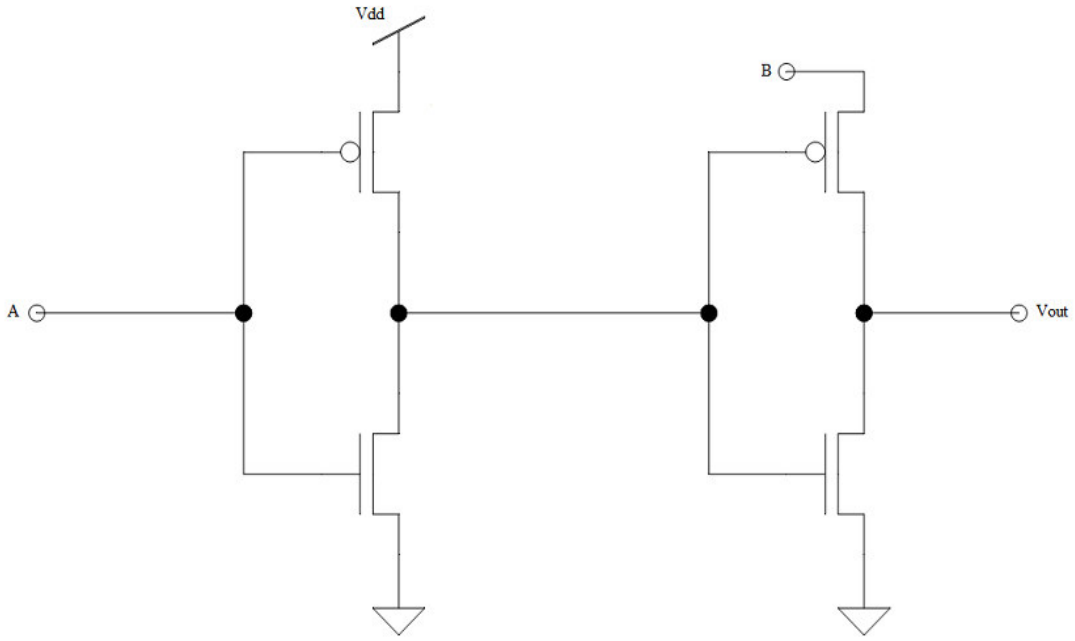


Figure 5.13. The Basic Structure of a Two-Input AND gate based on GDI technique.

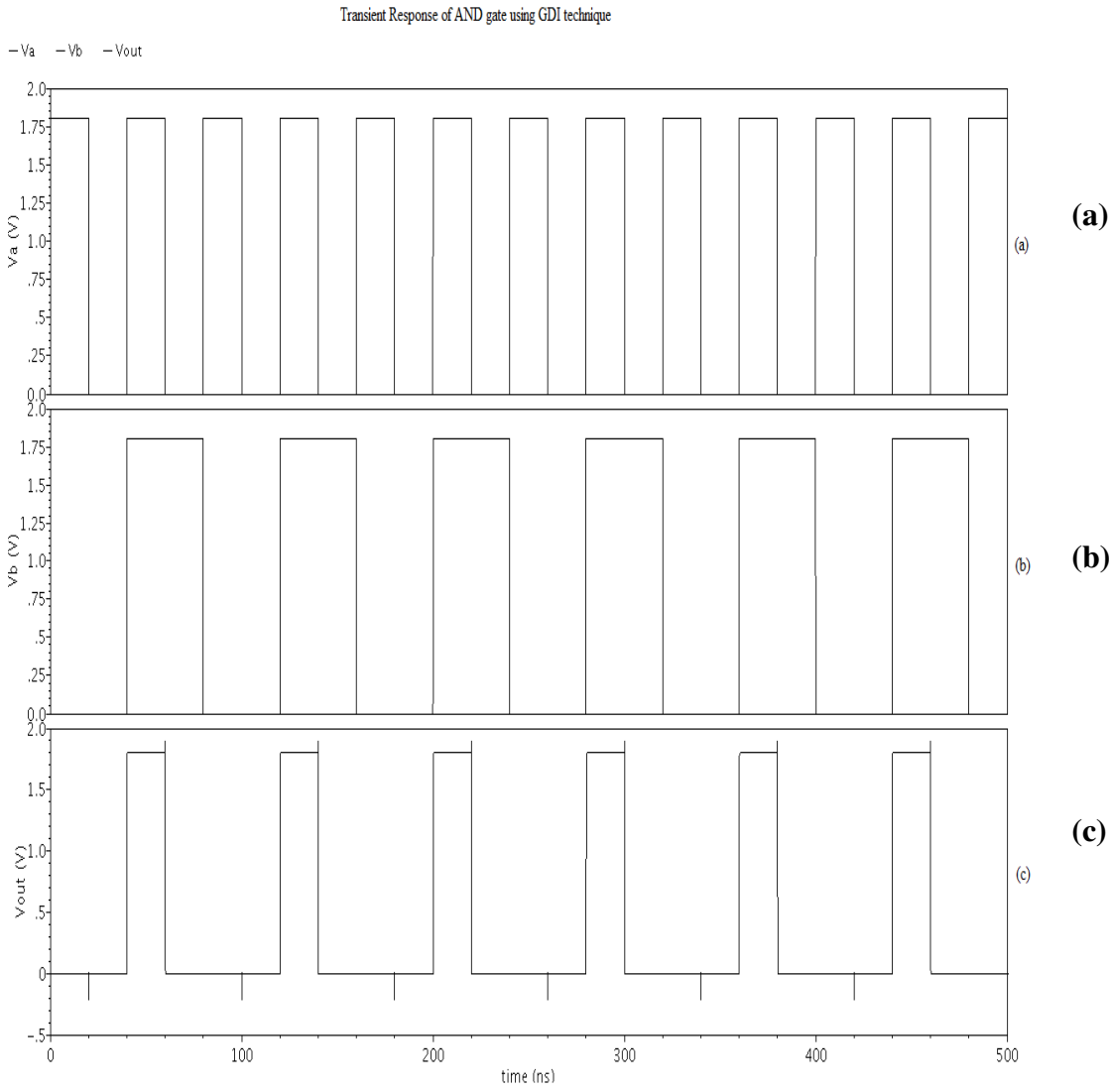


Figure 5.14.Simulation Results of a Two- Input AND gate based on GDI technique
(a) Input Signal (VA), (b) Input Signal (VB),
(c) Voltage Waveform of Output Signal.

5.8 DESIGN AND SIMULATION FOR A TWO-INPUT OR GATE BASED ON GDI TECHNIQUE

A two-input OR gate based on GDI technique is shown in Figure 5.15 and simulated waveforms are as shown in Figure 5.16, respectively.

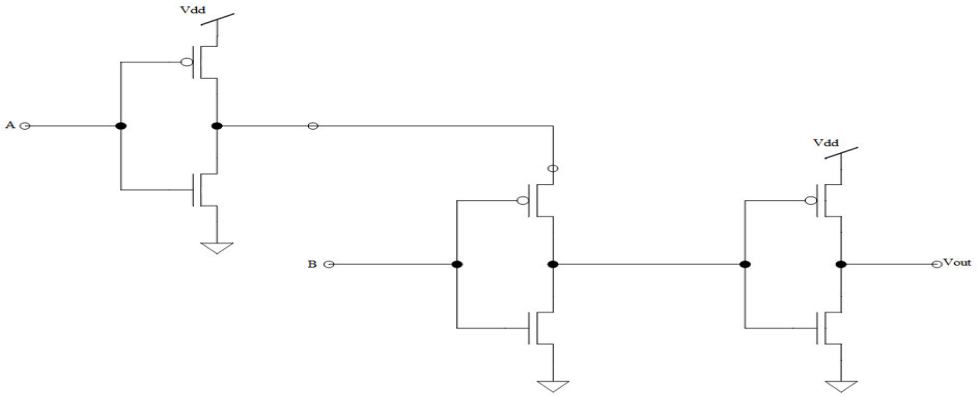
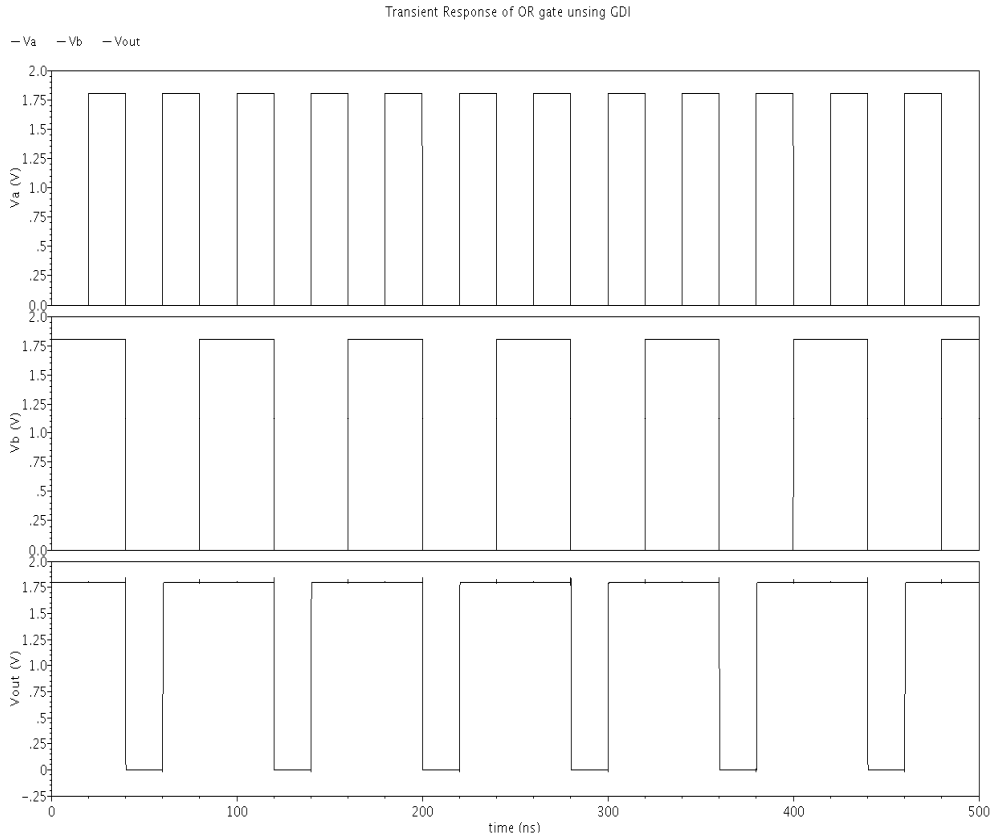


Figure 5.15. The Basic Structure of a Two-Input OR gate based on GDI technique.



(a)

(b)

(c)

Figure 5.16. Simulation Results of a Two- Input OR gate based on GDI technique
(a) Input Signal (VA), (b) Input Signal (VB),
(c) Voltage Waveform of Output Signal.

5.9 DESIGN AND SIMULATION FOR A TWO-INPUT XOR GATE BASED ON GDI TECHNIQUE

A two-input OR gate based on GDI technique is shown in Figure 5.17 and simulated waveforms are as shown in Figure 5.18, respectively.

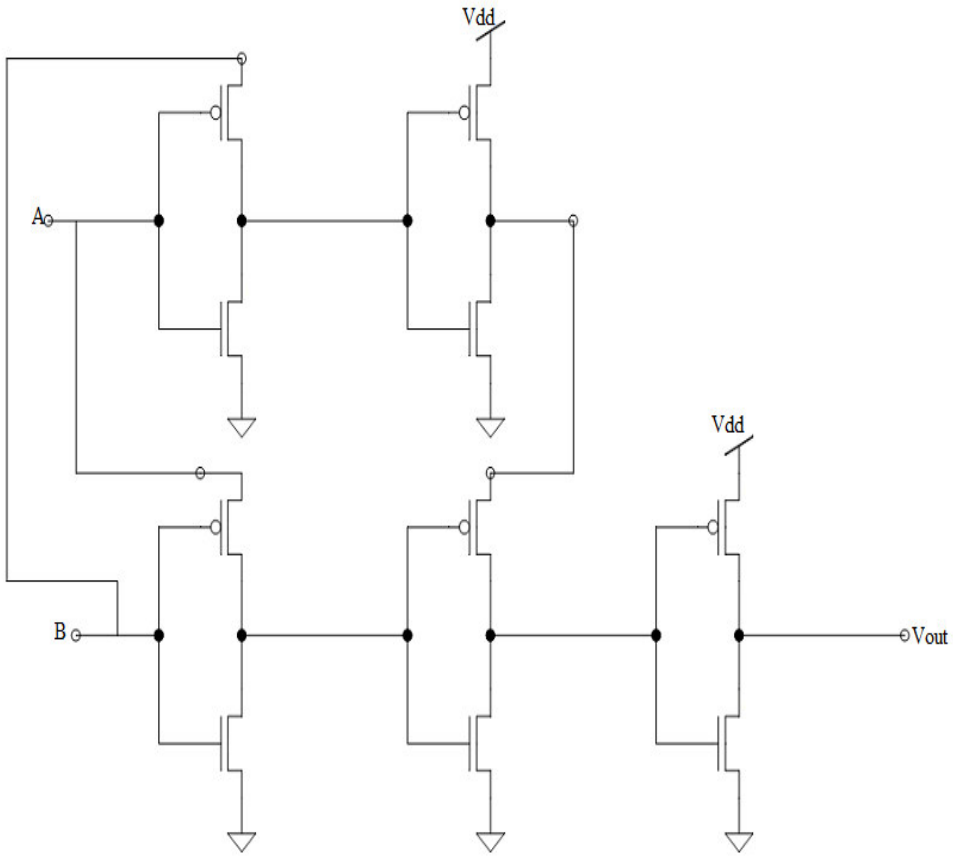


Figure 5.17. The Basic Structure of a Two-Input XOR gate based on GDI technique.

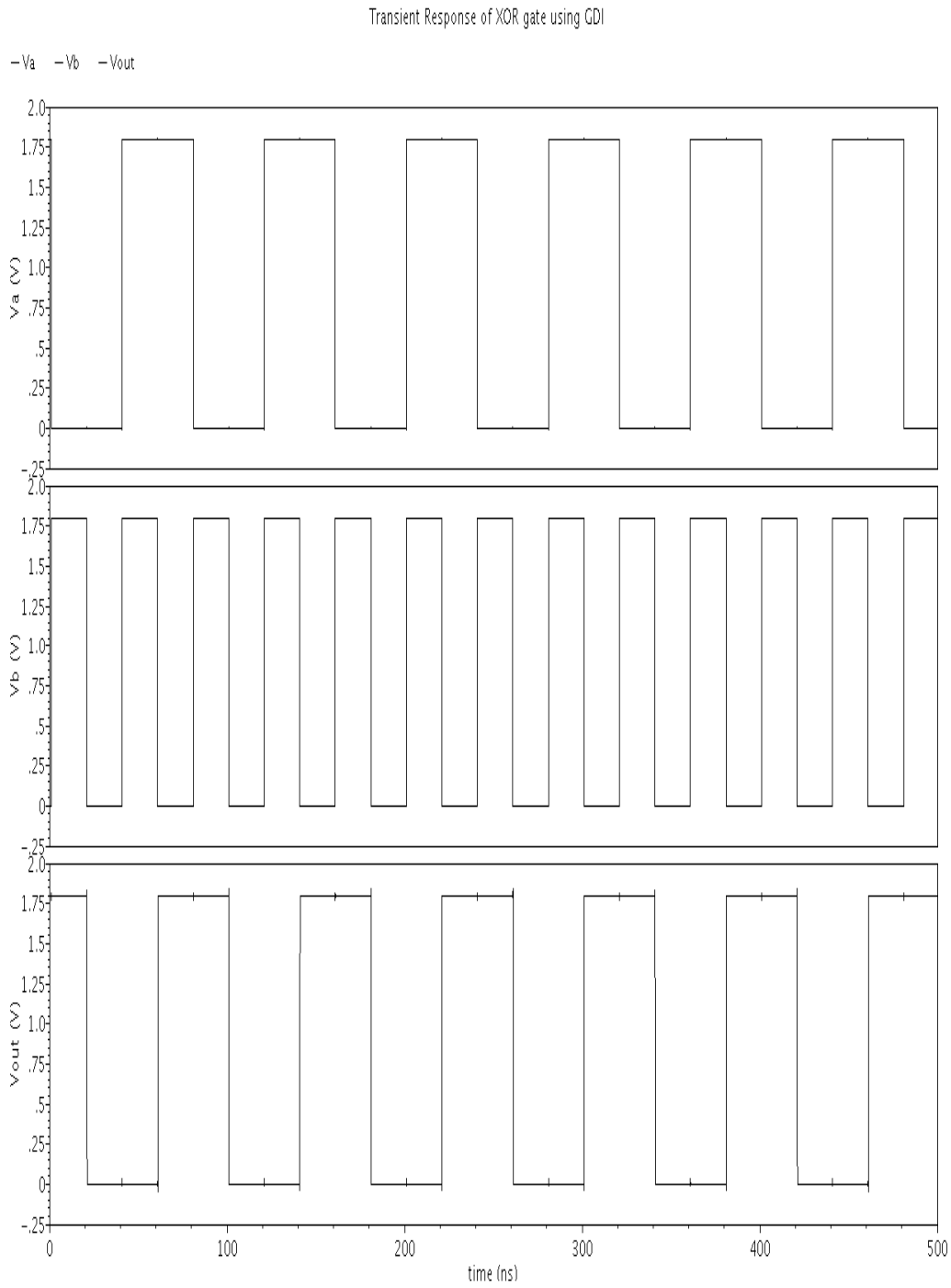


Figure 5.18. Simulation Results of a Two- Input XOR gate based on GDI technique
(a) Input Signal (VA), (b) Input Signal (VB),
(c) Voltage Waveform of Output Signal.

5.10 DESIGN AND SIMULATION FOR A HALF ADDER BASED ON GDI TECHNIQUE

A HALF ADDER based on GDI technique is shown in Figure 5.19 and simulated waveforms are as shown in Figure 5.20, respectively.

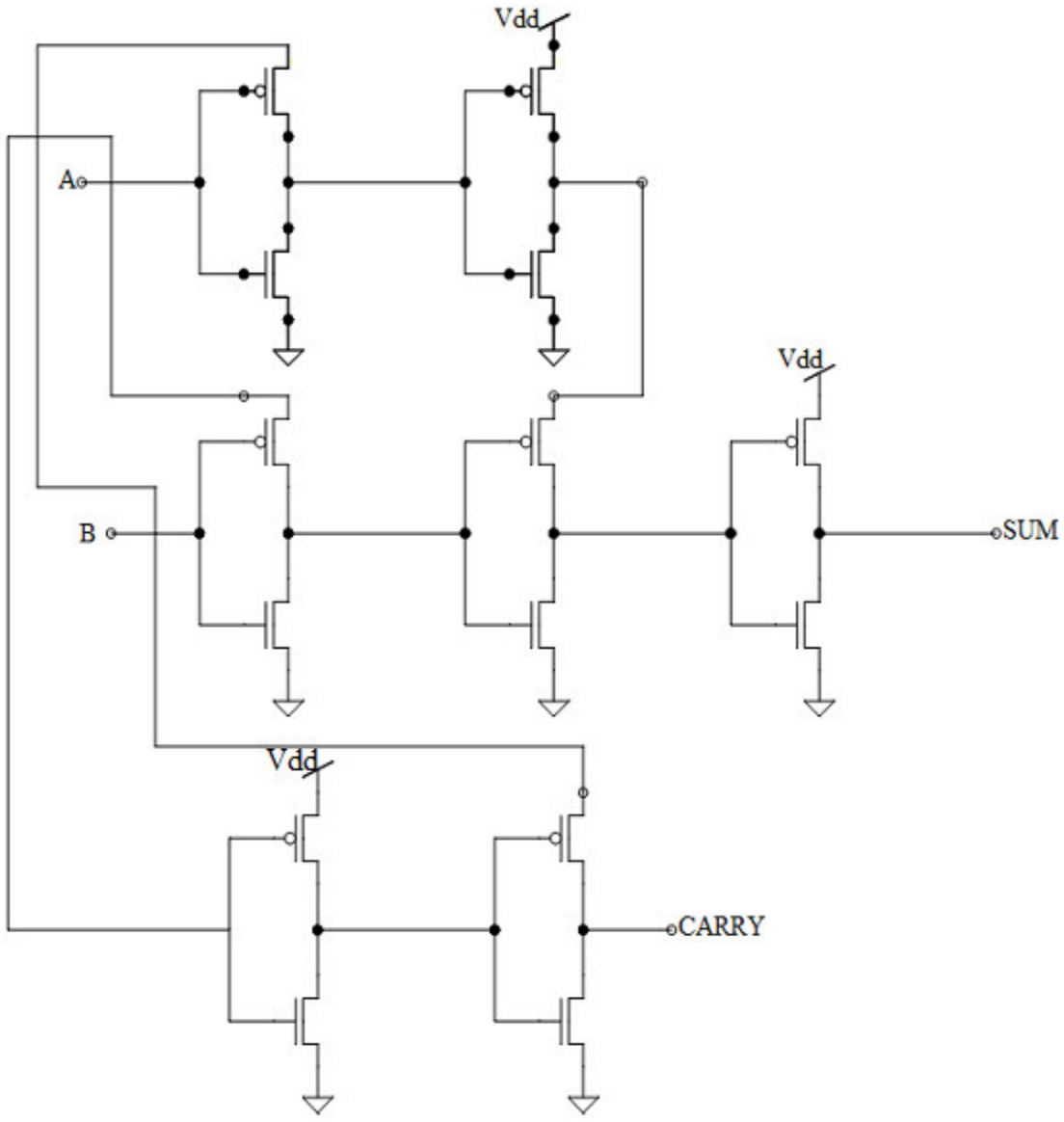
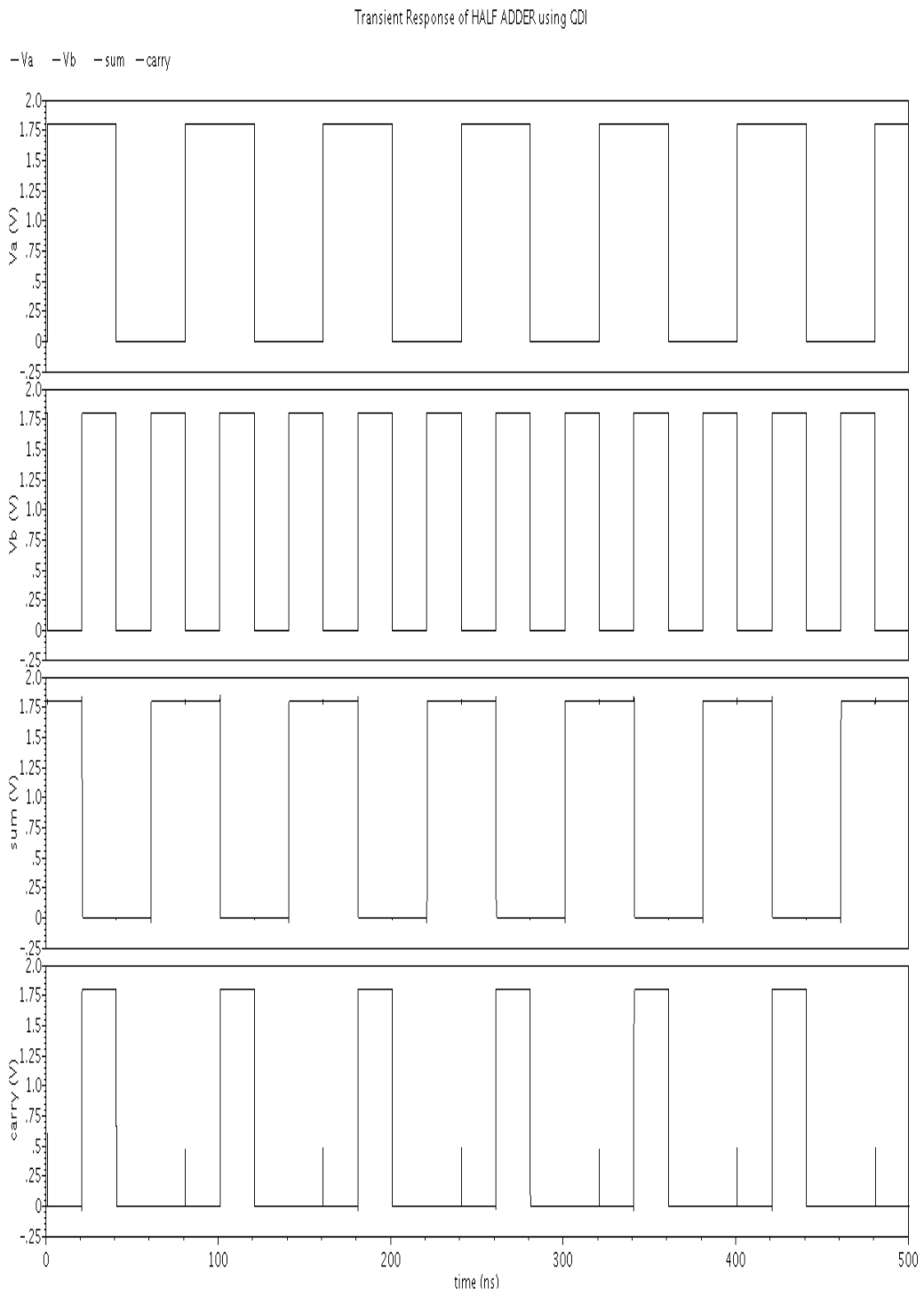


Figure 5.19. The Basic Structure of a HALF ADDER based on GDI technique.



(a)

(b)

(c)

(d)

Figure 5.20. Simulation Results of a HALF ADDER based on GDI technique.
(a) Input Signal (VA), (b) Input Signal (VB)
(c) Output Waveform of sum, (d) Output Waveform of carry

5.11 DESIGN AND SIMULATION FOR ONE-BIT FULL ADDER BASED ON GDI TECHNIQUE

A FULL ADDER based on GDI technique is shown in Figure 5.21 and simulated waveforms are as shown in Figure 5.22, respectively.

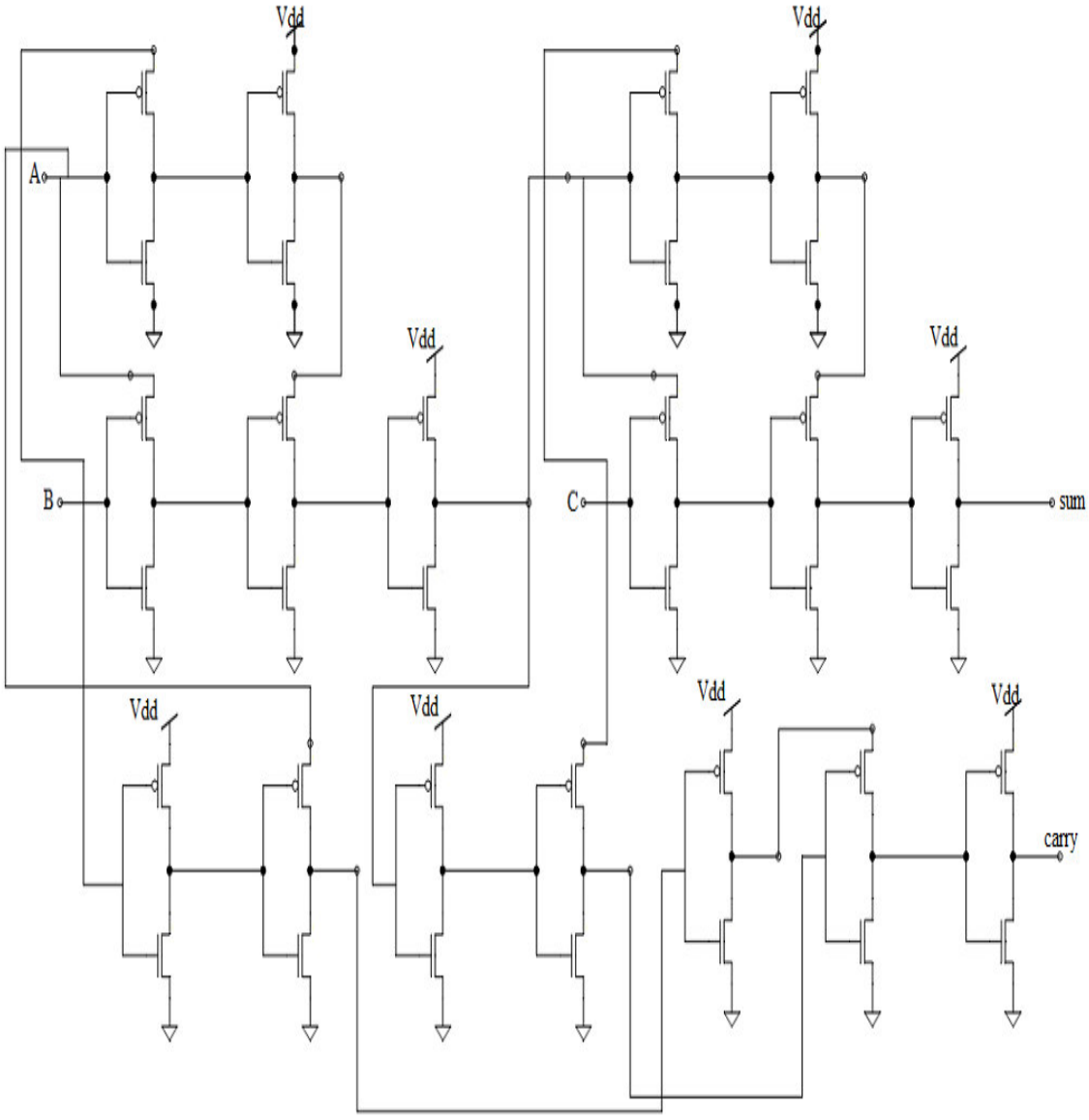


Figure 5.21. The Basic Structure of a FULL ADDER based on GDI technique.

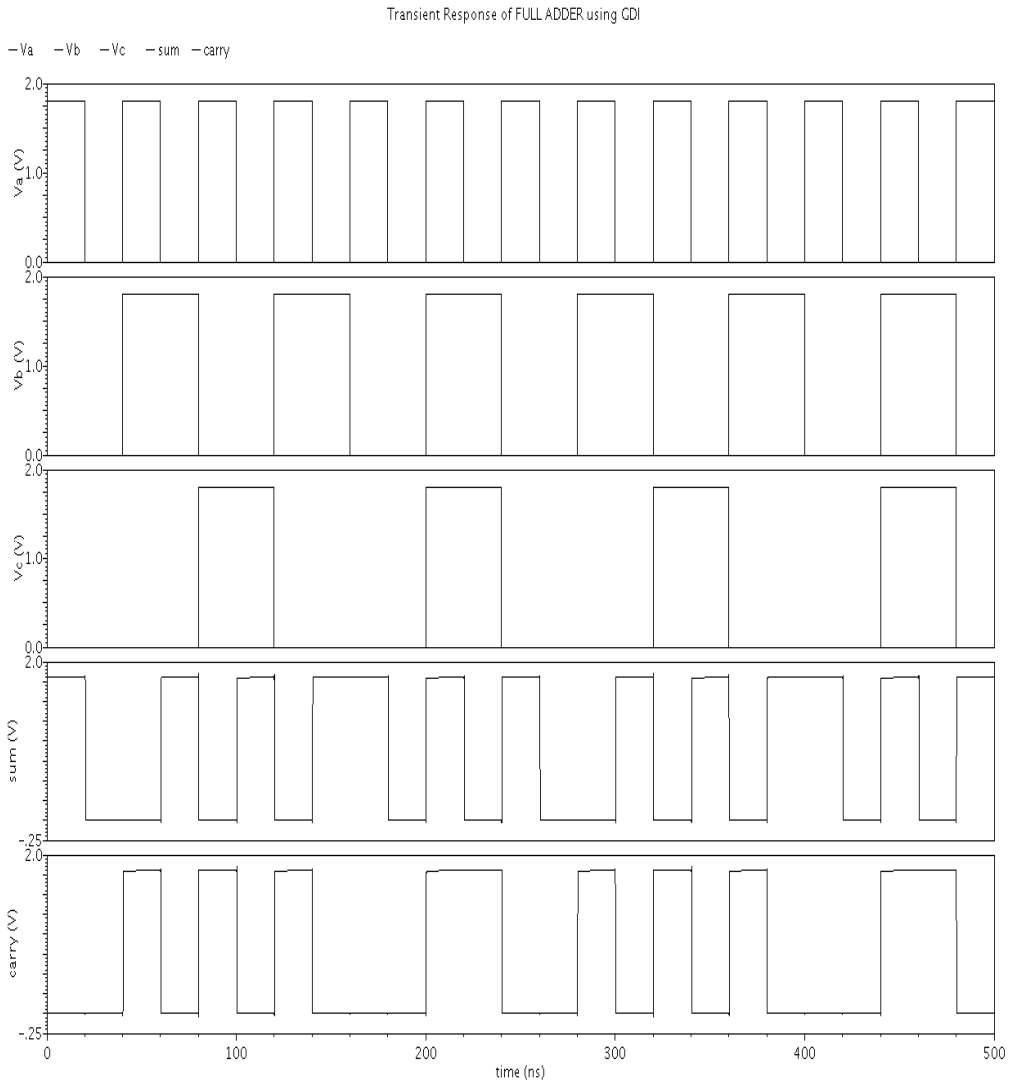


Figure 5.22. Simulation Results of a FULL ADDER based on GDI technique.
(a) Input Signal (VA), (b) Input Signal (VB), (c) Input Signal (Vcin)
(d) Output Waveform of sum, (e) Output Waveform of carry

5.12 POWER DISSIPATION ANALYSIS

5.12.1 VARIATION OF POWER DISSIPATION WITH FREQUENCY

This section deals with the comparison of the full complementary CMOS logic style with the GDI based logic style in terms of the average dynamic power dissipation, expressed in micro-Watts.

TABLE 5.1
AVERAGE DYNAMIC POWER DISSIPATED OF TWO-INPUT AND GATE BASED ON CMOS AND GDI TECHNIQUE FOR DIFFERENT POWER CLOCK FREQUENCIES

Frequency(MHz)	CMOS (µw)	GDI Technique(µw)
10	0.014	0.0037
20	0.023	0.0076
25	0.031	0.0095
40	0.042	0.0152
50	0.051	0.019
100	0.120	0.038

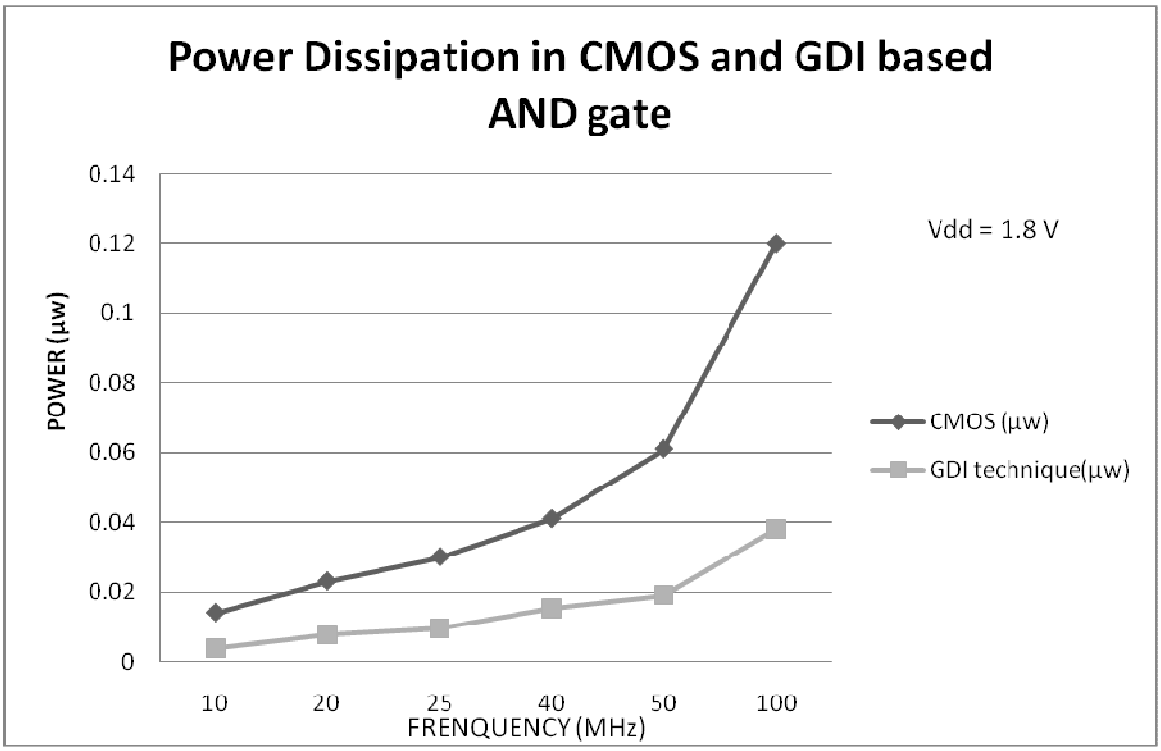


Figure 5.23. Power Dissipation Results for an AND gate.

TABLE 5.2
AVERAGE DYNAMIC POWER DISSIPATED OF TWO-INPUT OR GATE BASED ON CMOS AND GDI TECHNIQUE FOR DIFFERENT POWER CLOCK FREQUENCIES

Frequency(MHz)	CMOS (µw)	GDI Technique(µw)
10	0.259	0.192
20	0.518	0.363
25	0.71	0.479
40	1.03	0.724
50	1.48	0.952
100	2.93	1.89

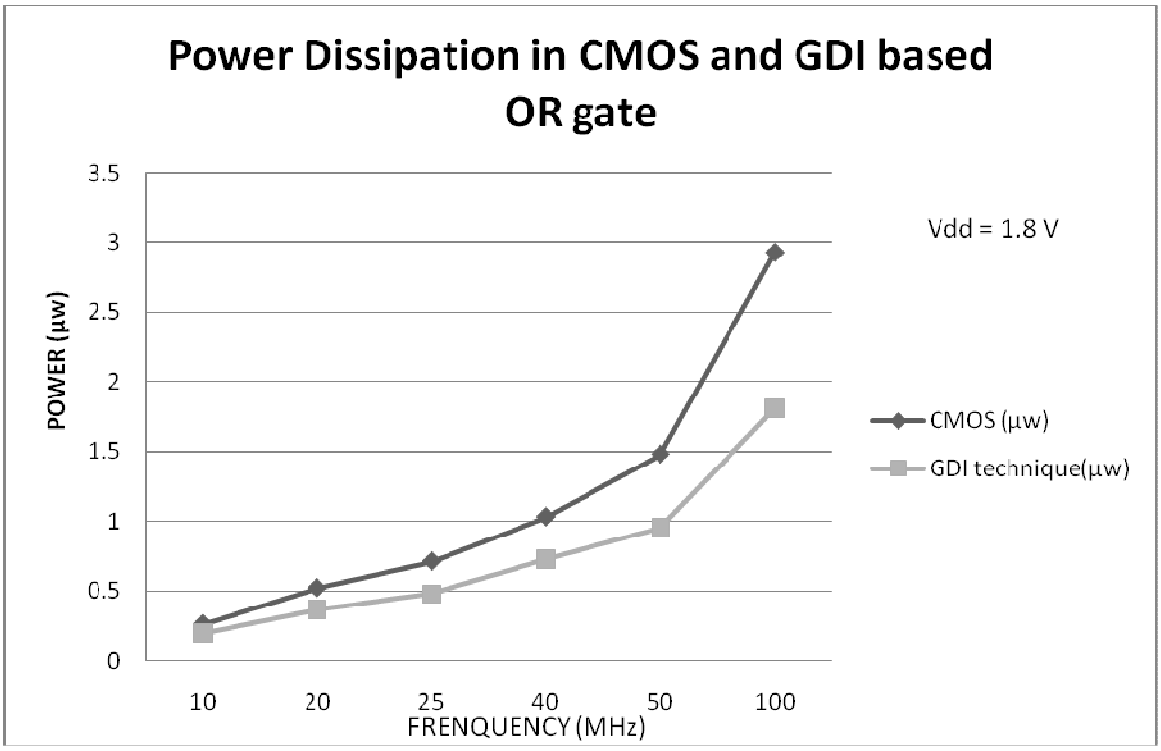


Figure 5.24. Power Dissipation Results for an OR gate.

TABLE 5.3
AVERAGE DYNAMIC POWER DISSIPATED OF TWO-INPUT XOR GATE BASED ON CMOS AND GDI TECHNIQUE FOR DIFFERENT POWER CLOCK FREQUENCIES

Frequency(MHz)	CMOS (µw)	GDI Technique(µw)
10	0.349	0.232
20	0.618	0.453
25	0.891	0.581
40	1.28	0.926
50	1.79	1.16
100	3.66	2.32

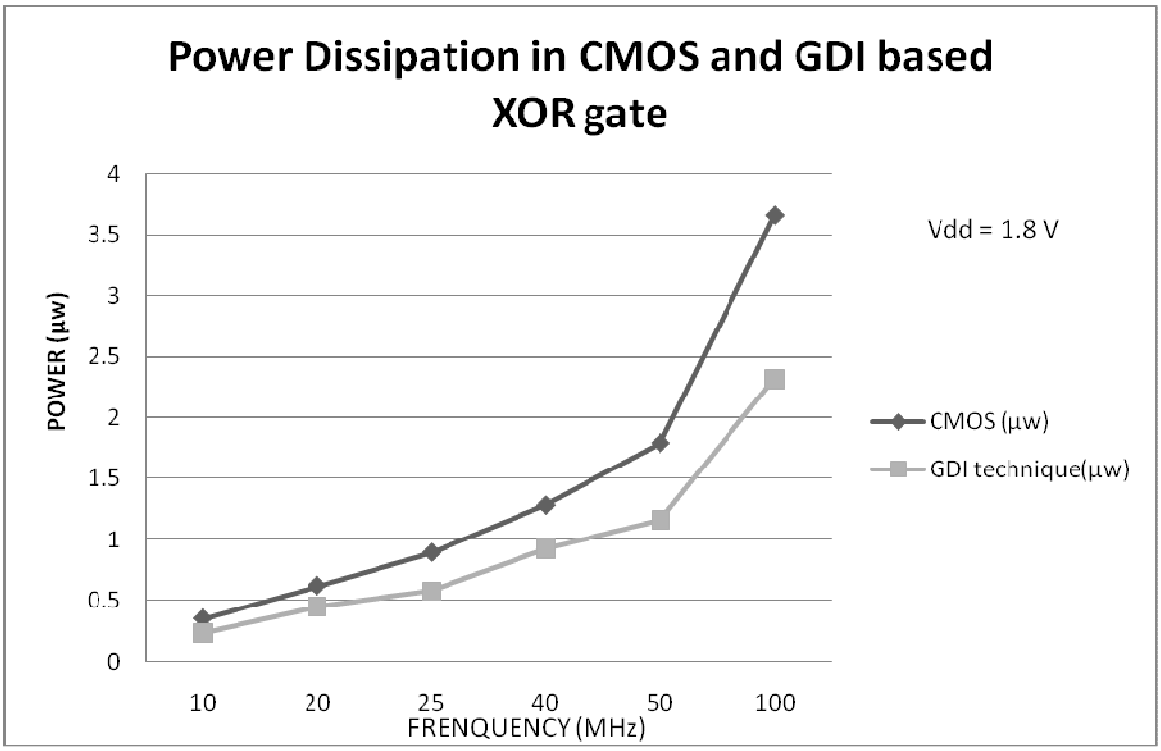


Figure 5.25. Power Dissipation Results for a XOR gate.

TABLE 5.4

AVERAGE DYNAMIC POWER DISSIPATED OF HALF ADDER BASED ON CMOS AND GDI TECHNIQUE FOR DIFFERENT POWER CLOCK FREQUENCIES

Frequency(MHz)	CMOS (µw)	GDI Technique(µw)
10	1.10	0.437
20	2.01	0.874
25	2.72	1.06
40	4.03	1.75
50	5.54	2.18
100	11.07	4.37

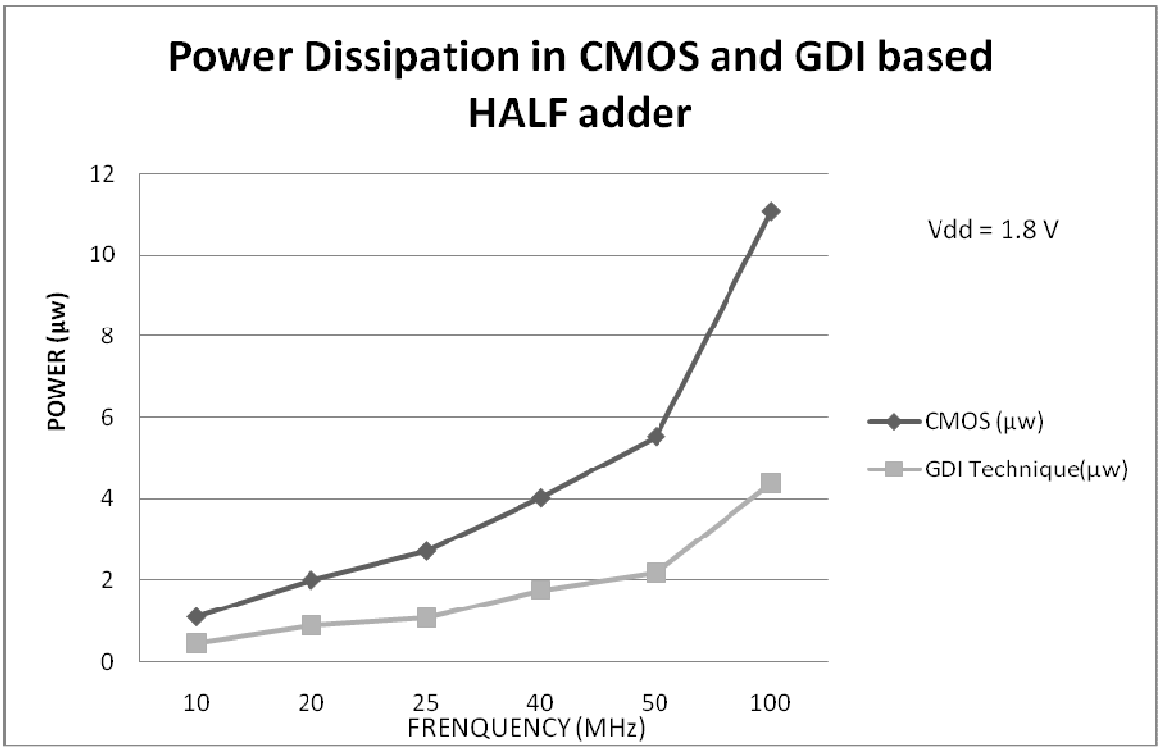


Figure 5.26. Power Dissipation Results for a HALF adder.

TABLE 5.5
AVERAGE DYNAMIC POWER DISSIPATED OF FULL ADDER BASED ON CMOS AND GDI TECHNIQUE FOR DIFFERENT POWER CLOCK FREQUENCIES

Frequency(MHz)	CMOS (µw)	GDI Technique(µw)
10	2.39	1.37
20	4.77	2.71
25	6.75	3.38
40	9.84	5.36
50	13.23	6.68
100	26.8	13.21

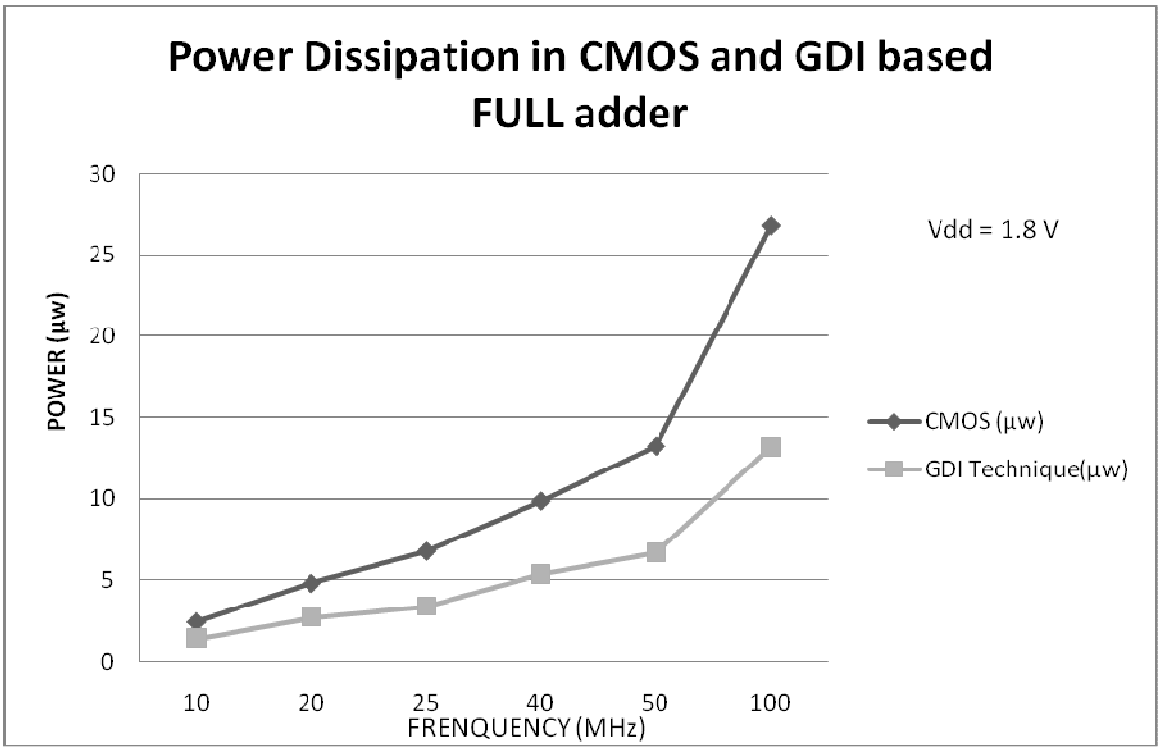


Figure 5.27. Power Dissipation Results for a FULL adder.

CHAPTER 6 LAYOUT DESIGN AND POST-LAYOUT SIMULATION

6.1 INTRODUCTION TO LAYOUT DESIGN

The process of creating an accurate physical representation of an engineering drawing (netlist or schematic) that conforms to constraints imposed by the manufacturing process, the design flow, and the performance requirements shown to be feasible by simulation [23].

6.1.1 NUMEROUS IMPLICATIONS BURIED IN THE LAYOUT DESIGN

A process: First and foremost, layout design is a process with many steps that should be followed in a logical order for optimal results. For example, the "process" of layout design may include setting up a database or suite of tools with the appropriate layers; defining the floorplan of each cell or chip; and/or running verification checks in the proper order [23].

Creation: "Design" and "creation" are usually synonymous, and layout design is no exception. Implementing one schematic in two different technologies usually results in layouts that look quite different, thus demonstrating the creative nature of the trade. In the same way, a schematic that will be used in two different regions of the chip may result in two different architectures, adapted to their geographical location [23].

Accuracy: Although layout design is a creative process, we must not forget that the first requirement of the final layout must be that it is equivalent on a transistor-by-transistor basis to the engineering drawing. Redesigning the configuration of transistors to "improve" the circuit is not the role of the layout designer unless you plan to take over (or already have taken over) the circuit design task as well [23].

Physical representation: CMOS ICs are made using an extremely complicated process that in the end results in tiny transistors and wires being constructed and connected on a silicon substrate. Layout design is the art of drawing these transisters and wires as they look like in silicon; thus, the layout can be thought of as the physical representation of the circuit [23].

Engineering drawing: This may sound a bit old-fashioned, but it is accurate. Transistor-level or gate-level schematics have historically been the primary "drawing" and in many companies they remain so. Fancier methodologies these days result in some layout designers receiving a large text-based file called a "netlist." However, in order for humans to understand a netlist, it is usually accompanied by a block-level schematic or drawing [23].

Conform: By conforming, we mean "meeting the requirements of" and not necessarily "the smallest or best design possible." There are many trade-offs to be made in the process of design: reliability, manufacturability, flexibility, and (perhaps most importantly) time to market, to name a few. Of course, there are minimum requirements that have to be met, but to achieve the optimal design at the expense of the project schedule is not practical in today's marketplace [23].

6.1.2 CONSTRAINTS IMPOSED IN THE LAYOUT DESIGN

Constraints imposed by the manufacturing process: These constraints include layout design rules such as the smallest width a metal track can be, but also many other manufacturability or reliability guidelines that will improve the overall quality of the layout. For example, in the case of a metal track, a wider line may improve the manufacturability of the design and thus should be used where space permits.

Constraints imposed by the design flow: These constraints include guidelines established to enable all other tools that are to be used in the design flow to be able to efficiently use the completed layout. For example, some routers like to have connections to cells on a regular pitch, while others do not care. Another example is the methodology to add text to layout so that the text can be used later for identification purposes.

Constraints imposed by the performance requirements shown to be feasible by simulation: An engineer completing a circuit design without detailed knowledge of how the circuit will be implemented in layout is required to make some assumptions. For example, the engineer designing the circuit will not know the exact area of the block without implementing the circuit in layout and so must make an educated estimate based on the information available. The total area figure may be important to know so that the maximum line length within the block is also known. This normally cannot be avoided, and the trick is to try to communicate these assumptions and thus constrain the layout accordingly. In our example the total area estimate used by the circuit designer should also be used by the layout designer as a target area, and differences from this estimate on the low or high side should be fed back to the circuit designer for resimulation [23].

6.2 DESIGN RULES AND LAYOUT

The object of a set of design rules is to allow a ready translation of circuit design concept, usually in stick diagram or symbolic form, into actual geometry in silicon. The design rules are the effective interface between the circuit/system designer and the fabrication engineer. Clearly, both sides of the interface have a vested interest in making their own particular tasks as easy as possible and design rules usually attempt to provide a workable and reliable compromise that is friendly to both sides.

Circuit designers in general want tighter, smaller layout for improved performance and decreased silicon area. On the other hand, the process wants design rules that result in a controllable and reproducible process. Generally we find that there has to be a compromise for a competitive circuit to be produced at a reasonable cost.

One of the important facts associated with design rules is the achievable definition of the process line. Definition is determined by process line equipment and process design. For example, it is found that if a 10:1wafer stepper is used instead of a 1:1 projection mask aligner; the level-to-level registration will be closer. Design rules can be affected by the maturity of the process line

The simple ‘ lambda based’ design rules set out first in this text are based on the invaluable work of Mead and Conway and have been widely used particularly in the educational context and in the design of multiproject chips. The design rules are based on a single parameter λ which leads to a simple set of rules for the designer, and wide acceptance of the rules by a large cross-section of the fabrication houses and silicon brokers and allows for scaling of the design to a limited extent. The simplicity of lambda based rules also provide a simple introduction to design rules and to mask layout design in general and helps to set the scene for the ‘micro’ based rule sets which follow [10].

6.2.1 DESIGN RULES CHECKER (DRC)

After complete design of a layout of its schematic it is needed to check the design rule. Assura DRC is part of the Virtuoso custom design platform that enables design to check, identify, and correct design rule errors and achieve design sign off before tapeout. Using hierarchical processing techniques, Assura DRC can effciently handle designs with high complexity and many levels of layout hierarchy [25].

DRC software usually takes as input a layout in the GDSII standard format and a list of rules specific to the semiconductor process chosen for fabrication. From these it produces a report of design rule violations that the designer may or may not choose to correct.

6.2.1 LAYOUT VERSUS SCHEMATIC (LVS)

LVS is followed just after the DRC process and after the LVS, RCX is followed for the post-layout. The Layout Versus Schematic (LVS) is the essential type of electronic design automation (EDA) verification software that determines whether a particular integrated circuit layout corresponds to the original schematic of circuit diagram of the design.

A successful design rule check (DRC) ensures that the layout conforms to the rules designed / required for faultless fabrication. However, it does not guarantee if it really represents the circuit you desire to fabricate. This is where an LVS check is used. LVS checking software recognizes the drawn shapes of the layout that represent the electrical components of the circuit, as well as the connections between them. The software then compares them with the schematic or circuit diagram.

6.3 PHYSICAL LAYOUT DESIGN OF DIFFERENT CMOS AND GDI BASED CELL STRUCTURES

The physical layout design of different cells based on fully-complementary CMOS logic and gate diffusion input technique based has been done in standard TSMC 0.18 μm CMOS technology. For the project work, IC station Cadence IC5141 was used for the design of different physical layout cell structures and an ASSURA Simulator was used for all the validation of the physical layout designs.

6.3.1 LAYOUT CELL DESIGN OF A CMOS INVERTER

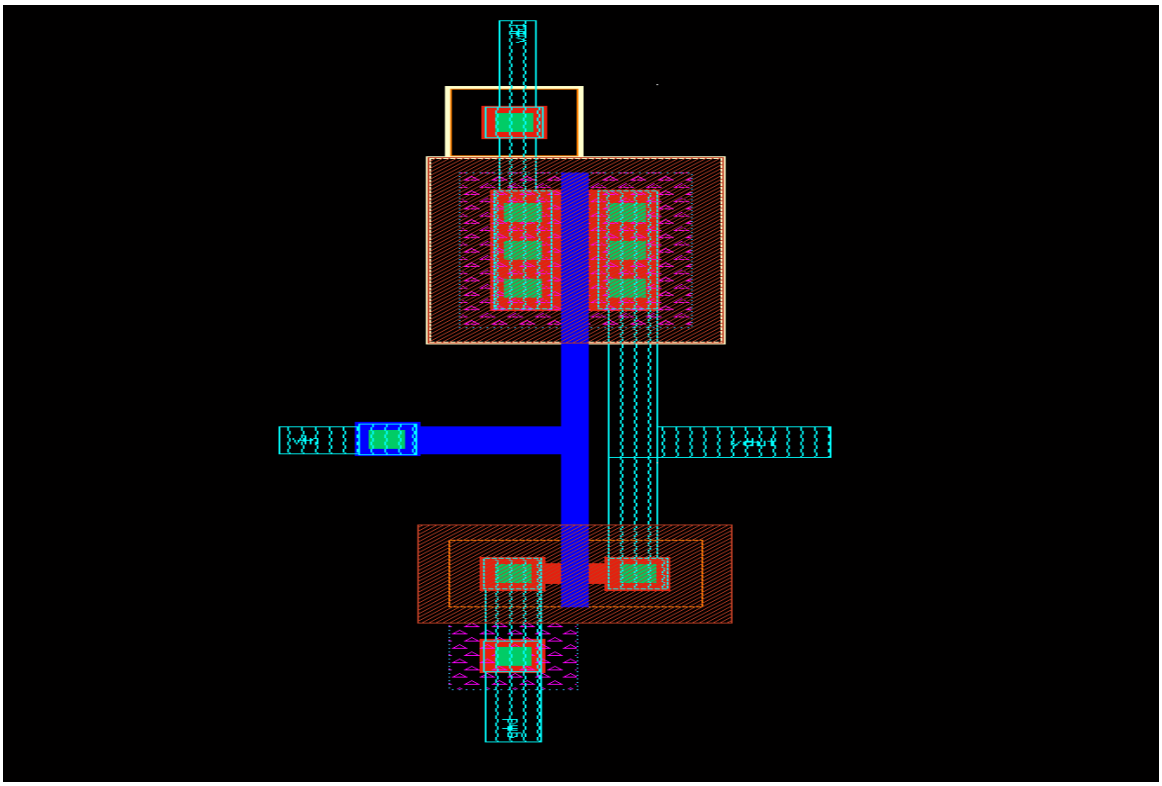


Figure 6.1. Layout of CMOS Inverter.

6.3.2 LAYOUT CELL DESIGN OF A TWO-INPUT CMOS AND GATE

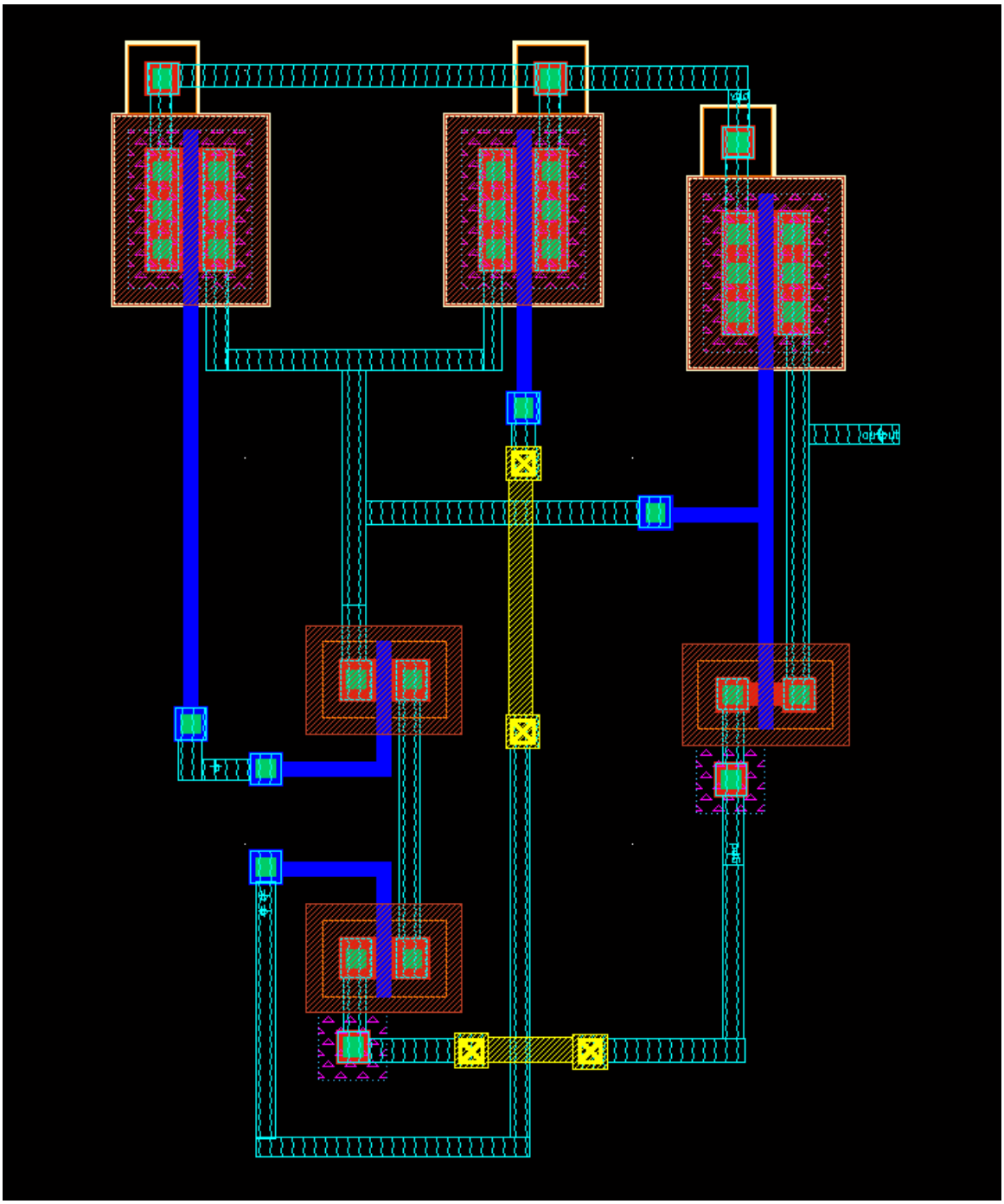


Figure 6.2. Layout of Two- Input CMOS AND Gate.

6.3.3 LAYOUT CELL DESIGN OF A TWO-INPUT CMOS OR GATE

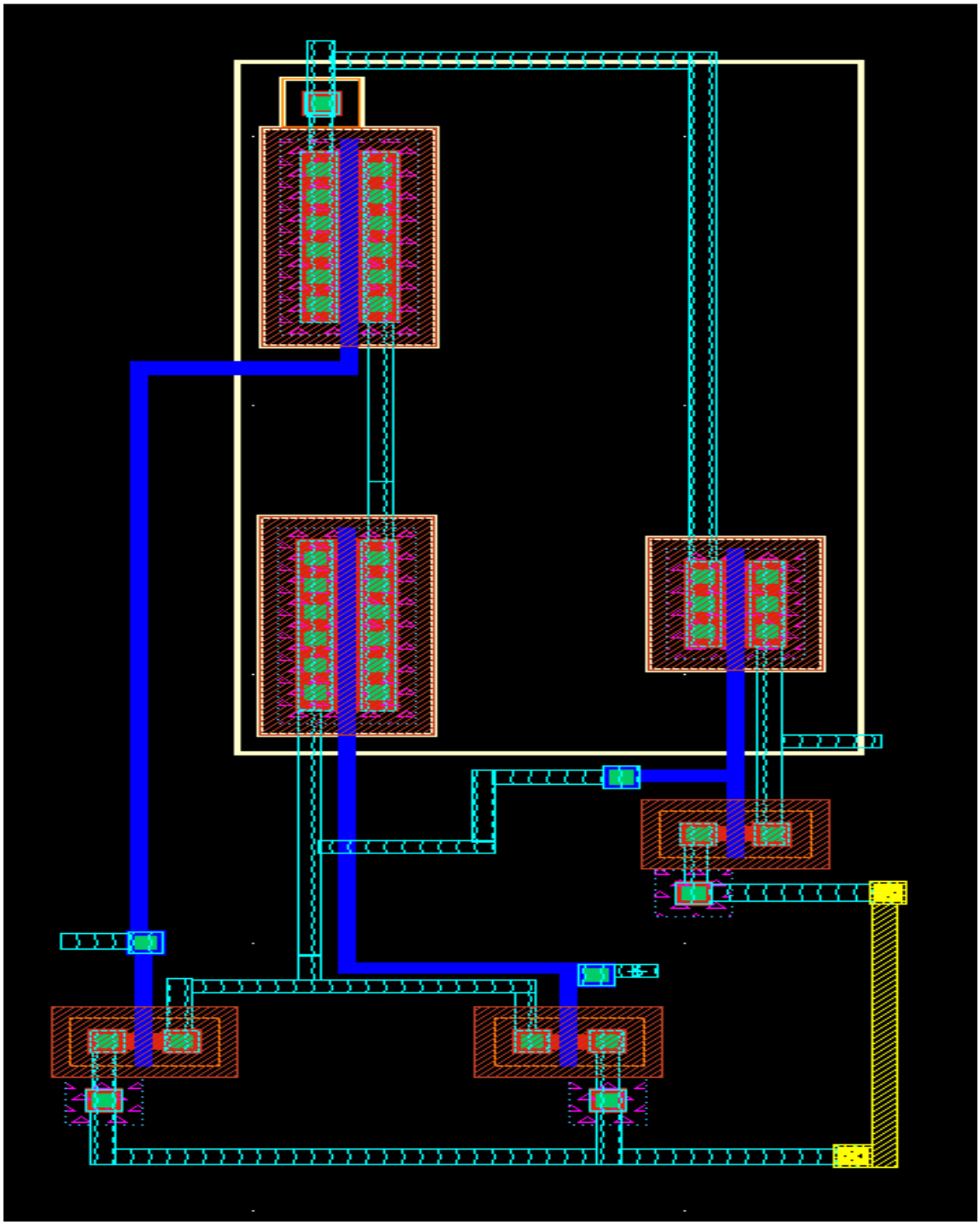


Figure 6.3. Layout of Two- Input CMOS OR Gate.

6.3.4 LAYOUT CELL DESIGN OF A TWO-INPUT CMOS XOR GATE

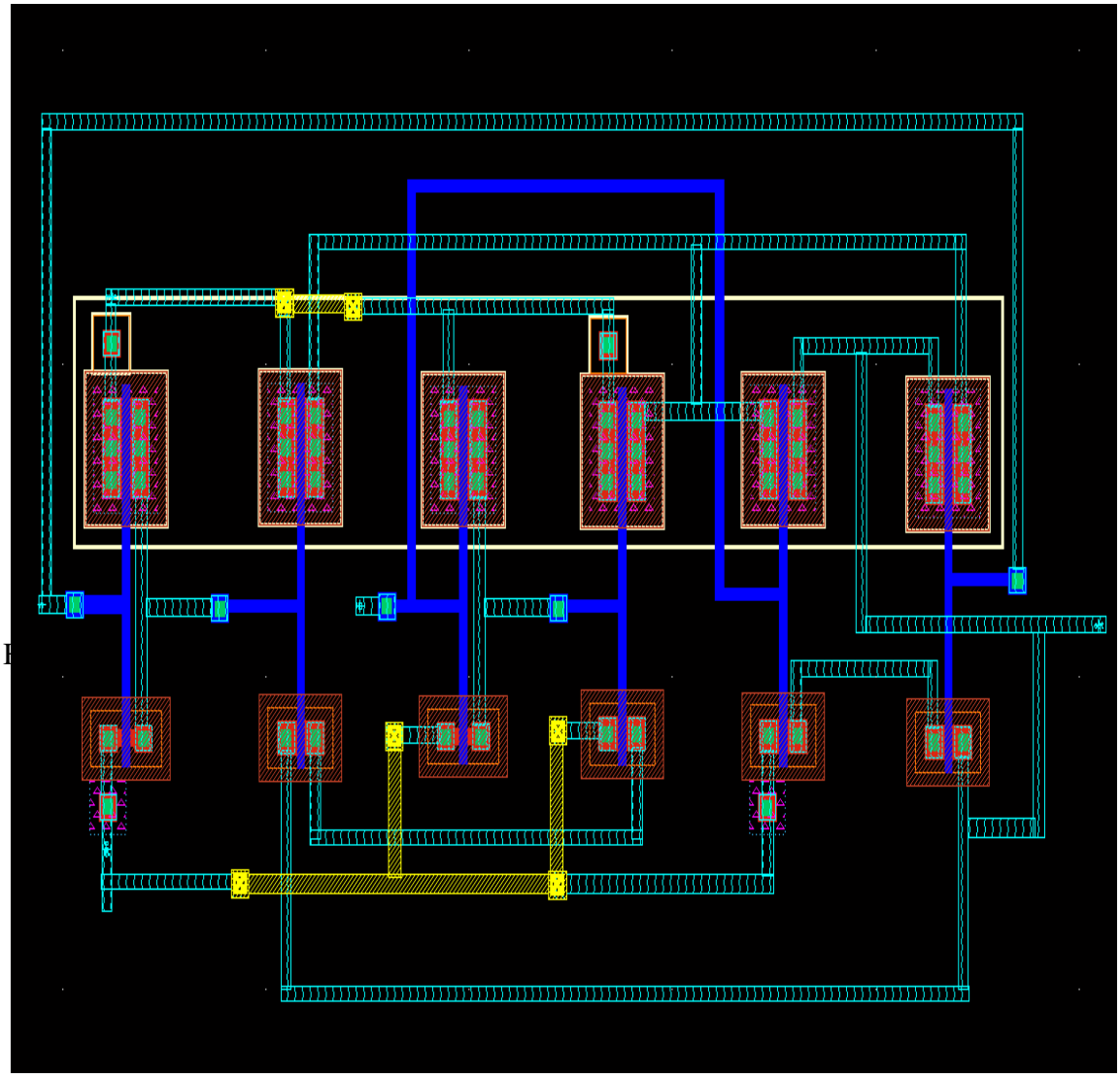


Figure 6.4. Layout of Two- Input CMOS XOR Gate.

6.3.5 LAYOUT CELL DESIGN OF A TWO-INPUT HALF ADDER.

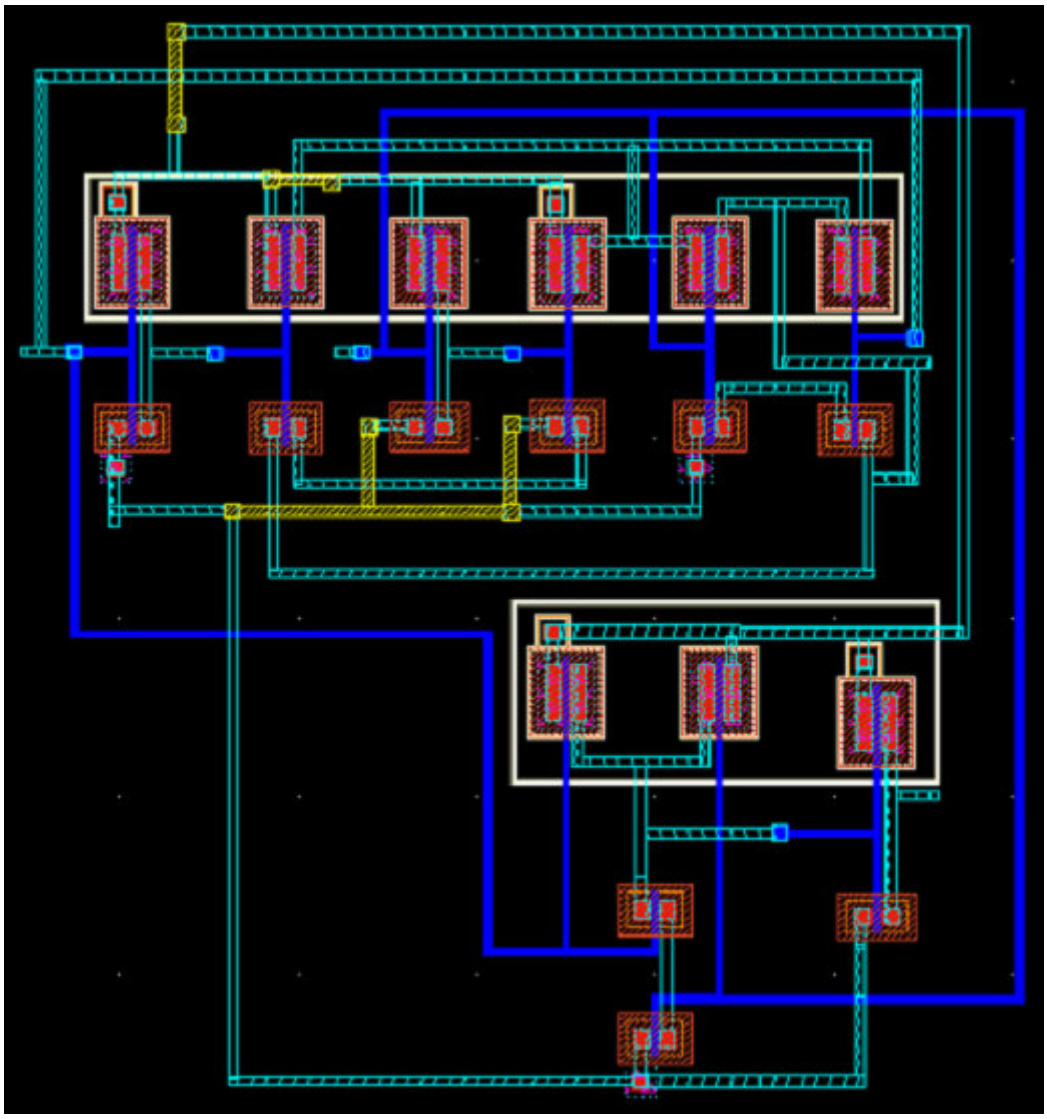


Figure 6.5. Layout of Two - Input CMOS HALF adder.

6.3.6 LAYOUT CELL DESIGN FOR A ONE-BIT CMOS FULL ADDER

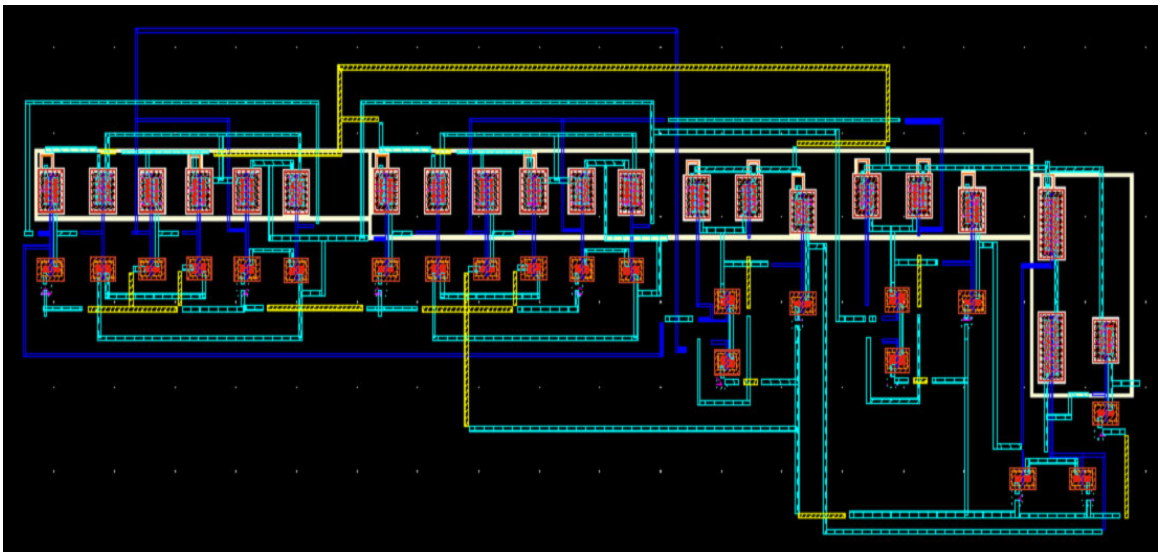


Figure 6.6. Layout of Two-Input CMOS HALF adder.

6.3.7 LAYOUT DESIGN OF A TWO-INPUT AND GATE USING GDI TECHNIQUE

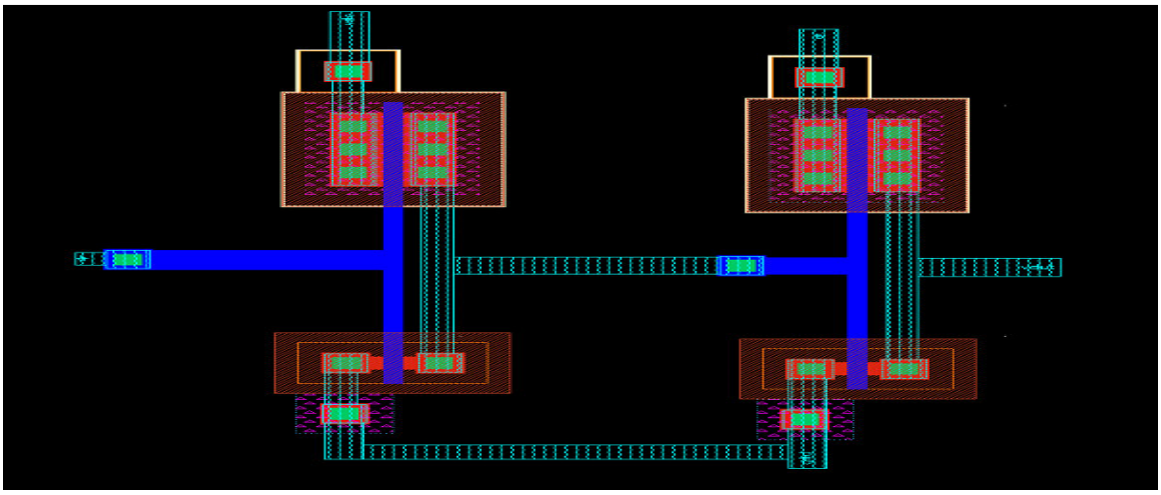


Figure 6.7. Layout of Two - Input AND gate using GDI technique

6.3.8 LAYOUT DESIGN OF A TWO-INPUT OR GATE USING GDI TECHNIQUE

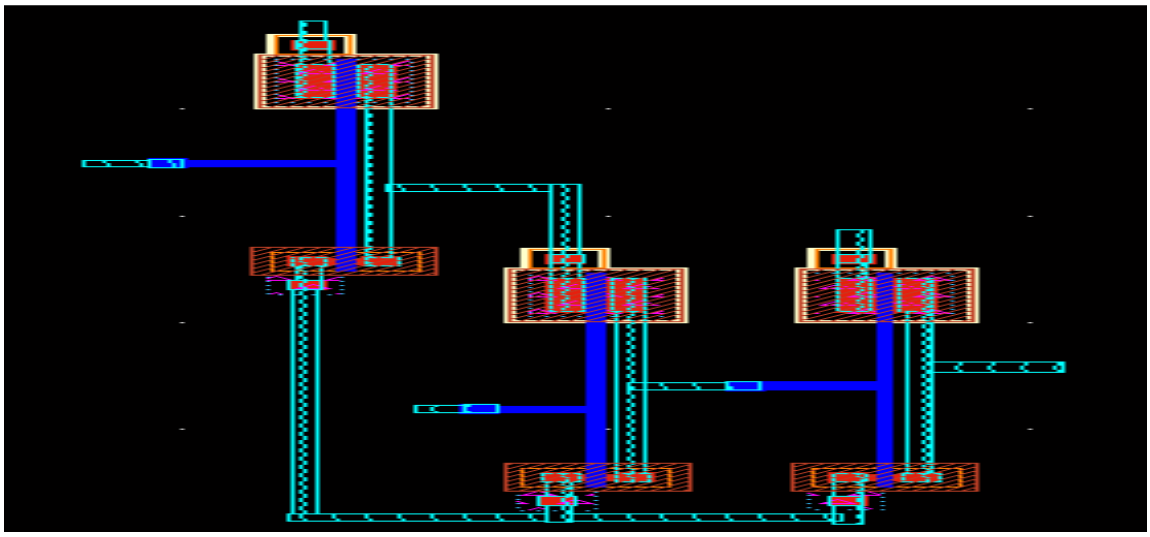


Figure 6.8. Layout of Two - Input OR gate using GDI technique

6.3.9 LAYOUT DESIGN OF A TWO-INPUT XOR GATE USING GDI TECHNIQUE

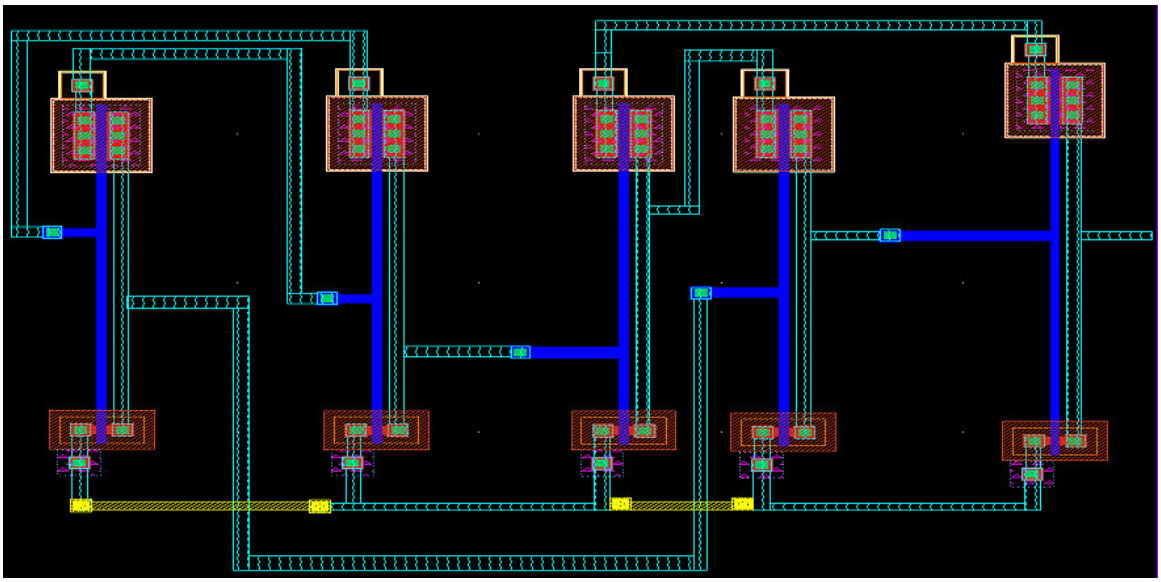


Figure 6.9. Layout of Two - Input XOR gate using GDI technique

6.3.10 LAYOUT DESIGN OF A TWO-INPUT HALF ADDER USING GDI TECHNIQUE

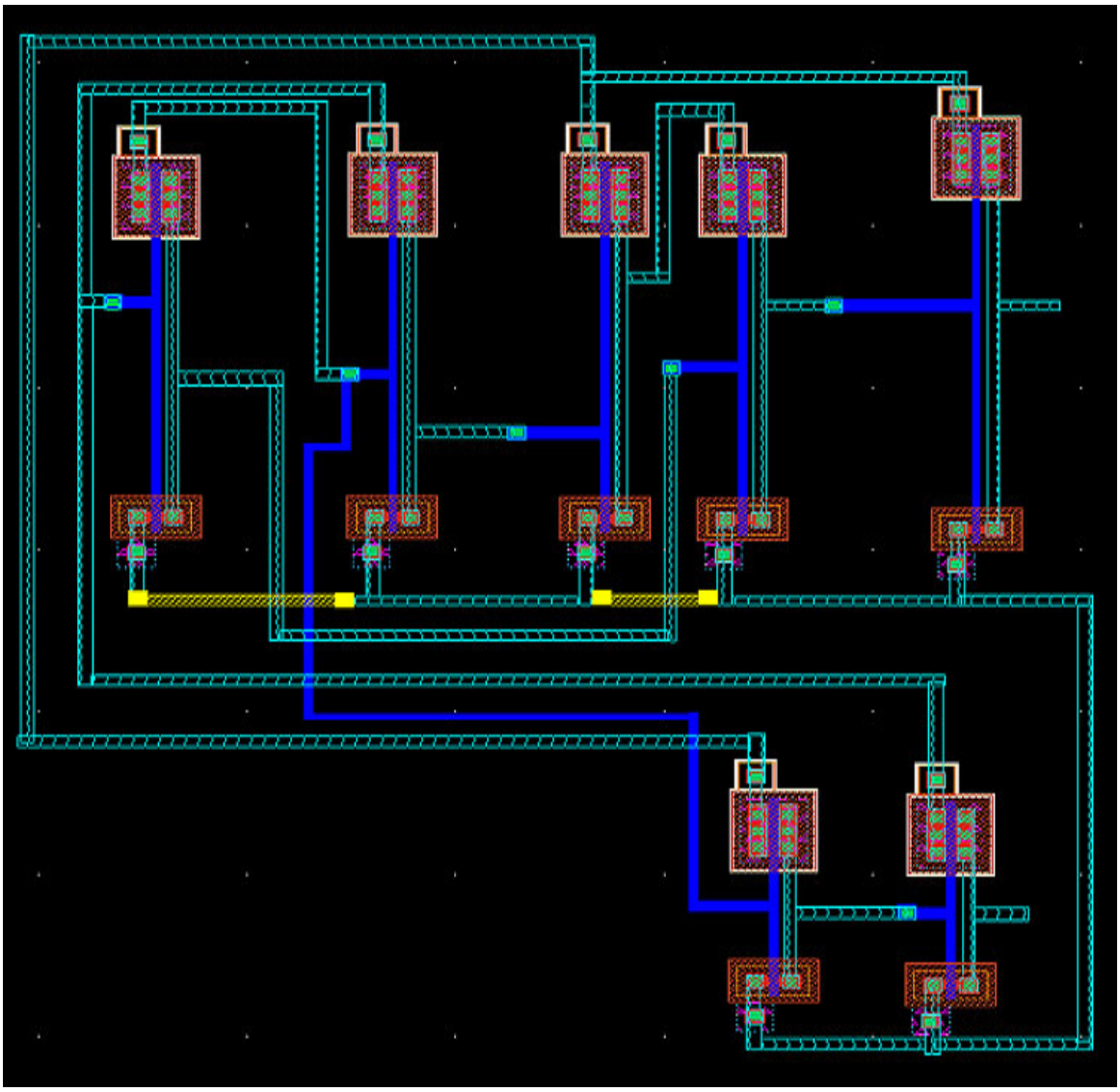


Figure 6.10. Layout of Two - Input HALF adder using GDI technique

6.3.11 LAYOUT DESIGN OF A FULL ADDER USING GDI TECHNIQUE

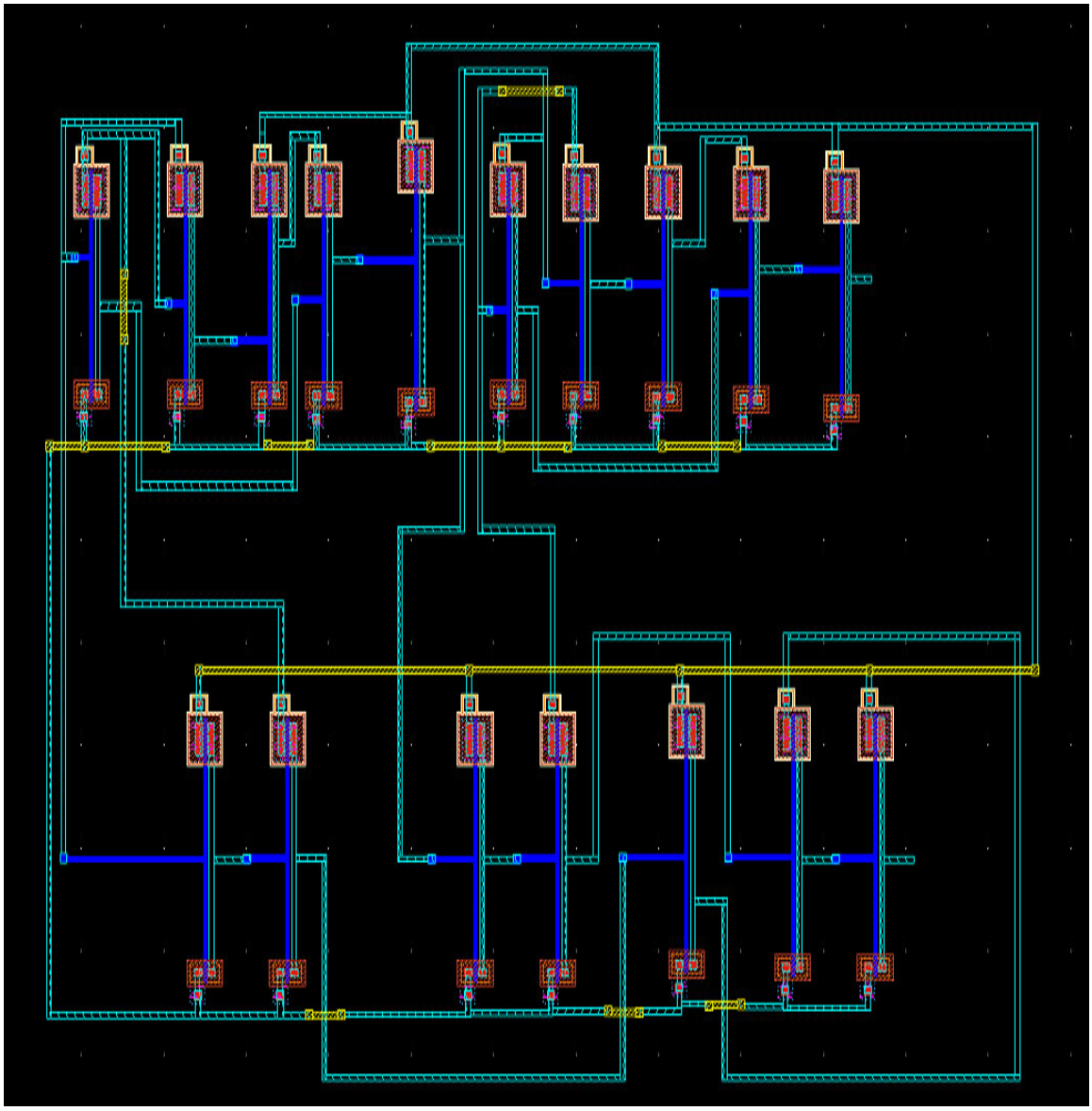


Figure 6.11. Layout of FULL adder using GDI technique

6.4 POST-LAYOUT SIMULATIONS

After the successful run of DRC and then after LVS, post–layout is another step-up. Post-Layout simulations have been done on extracted netlist. For the, post–layout simulation Assura Parasitic Extraction (RCX) is used.

6.4.1 PARASITIC EXTRACTION (RCX)

Parasitic Extraction (RCX) provides high-speed, full-chip parasitic extraction with silicon accuracy on design layouts. Parasitic Extraction (RCX) is a comprehensive full-chip, 3D device-level parasitic extraction solution with the accuracy and flexibility needed for the most advanced layout designs. Built on a foundation of patented algorithms and proprietary extraction technologies, Parasitic Extraction (RCX) brings the physics of interconnect parasitic into the custom design platform for designing, characterizing, and optimizing chip layouts within a single design environment [24].

Parasitic Extraction (RCX) provides silicon-accurate resistance (R) and capacitance (C) extraction for all process technologies. It models physical effects found in advanced process technologies to ensure that extracted parasitics match those on silicon. Parasitic Extraction (RCX) also provides hierarchical extraction capabilities with exceptional capacity and performance, making it possible for designers to perform full-chip simulation and analysis with parasitics on designs with multiple levels of hierarchy [24].

Parasitic Extraction (RCX) supplies the critical parasitic information for optimizing chip performance and yield.

6.4.2 POST - LAYOUT SIMULATION RESULTS FOR A CMOS INVERTER

Figure 6.12 below shows the post-layout result of the transient analysis for a minimum-sized CMOS Inverter.

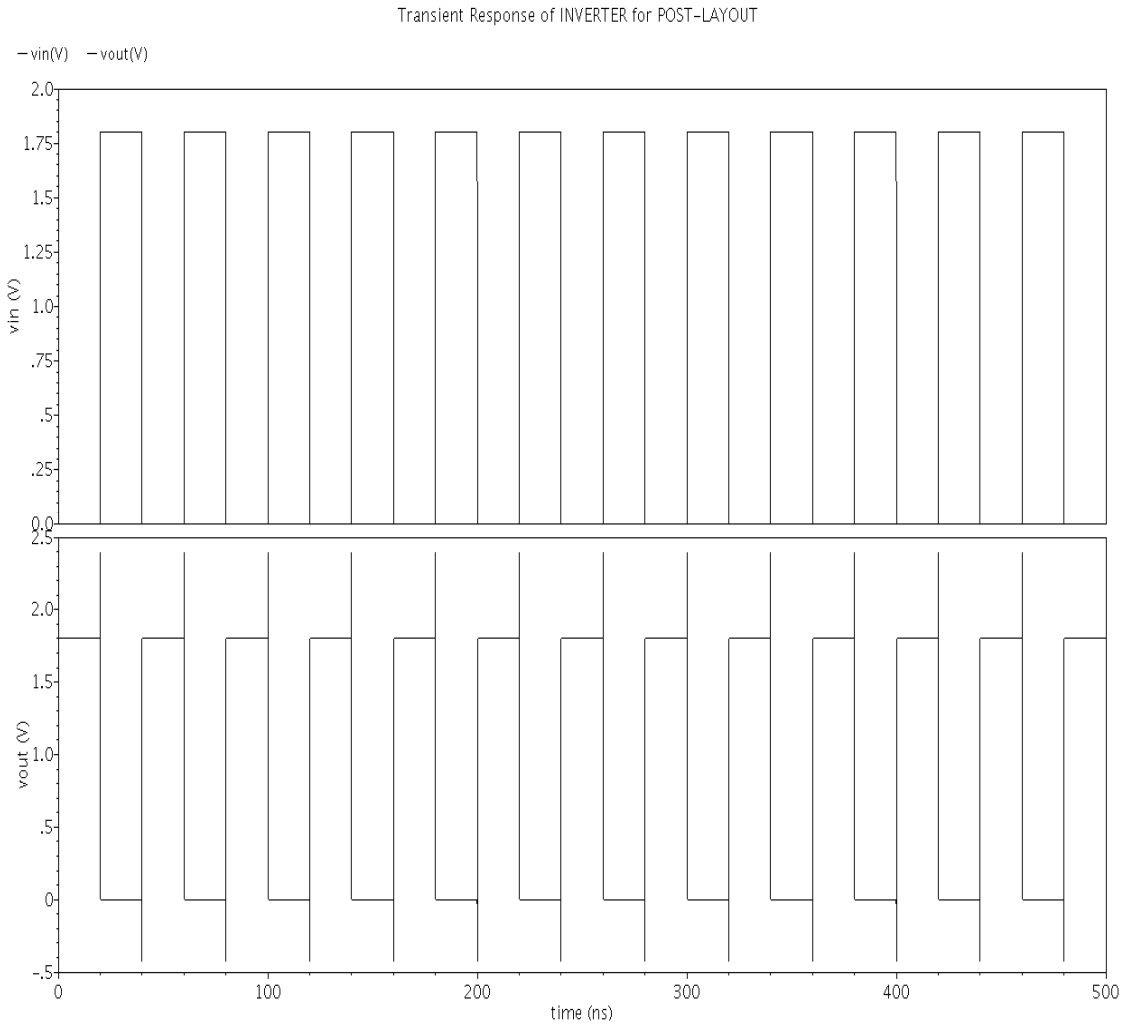


Figure 6.12. Post -Layout Simulation–Transient Analysis for CMOS Inverter.

6.4.3 POST - LAYOUT SIMULATION RESULTS FOR A TWO INPUT CMOS AND GATE

Figure 6.13 below shows the post-layout result of the transient analysis for a two-input AND gate.

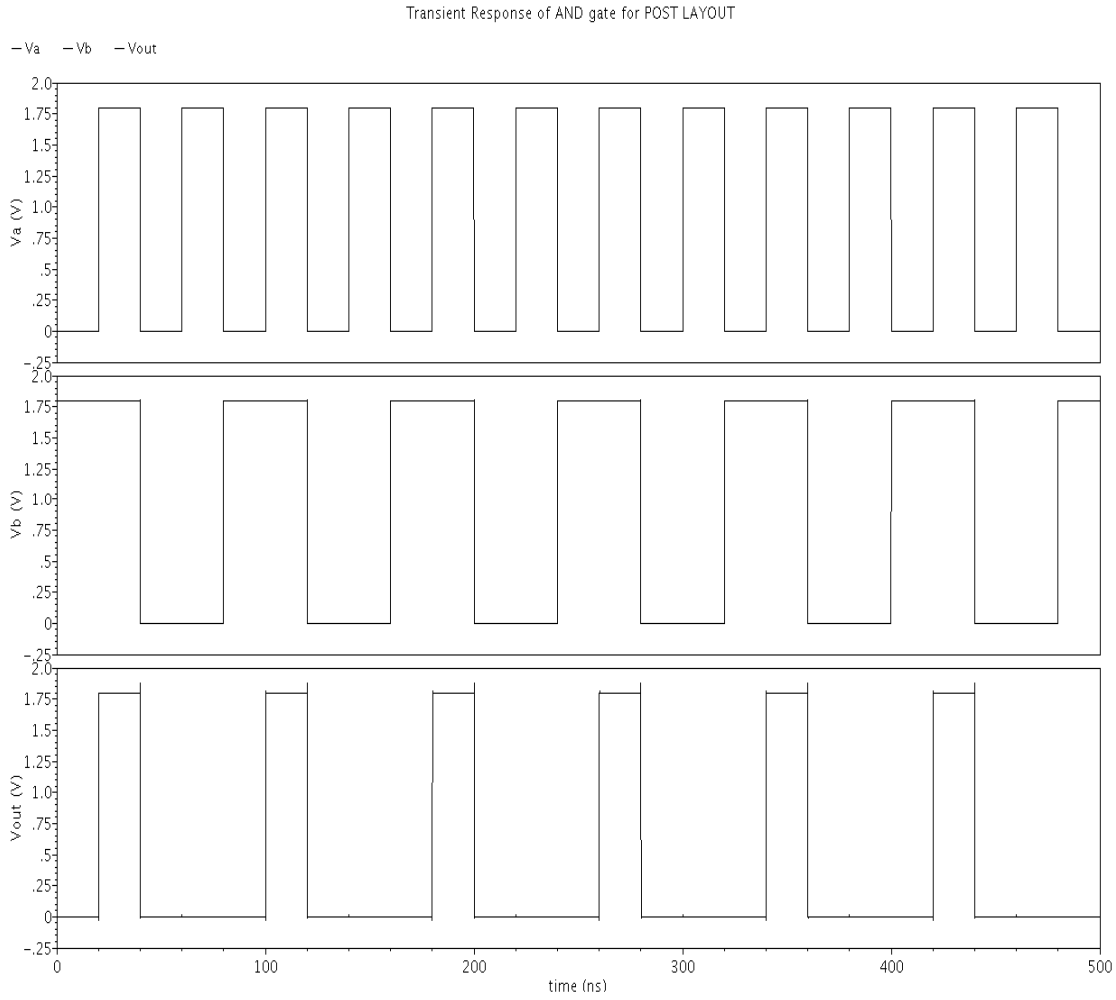


Figure 6.13. Post - Layout Simulation – Transient Analysis for a Two-Input CMOS AND Gate.

6.4.4 POST - LAYOUT SIMULATION RESULTS FOR A TWO-INPUT CMOS OR GATE

Figure 6.14 below shows the post-layout result of the transient analysis for a two-input OR gate.

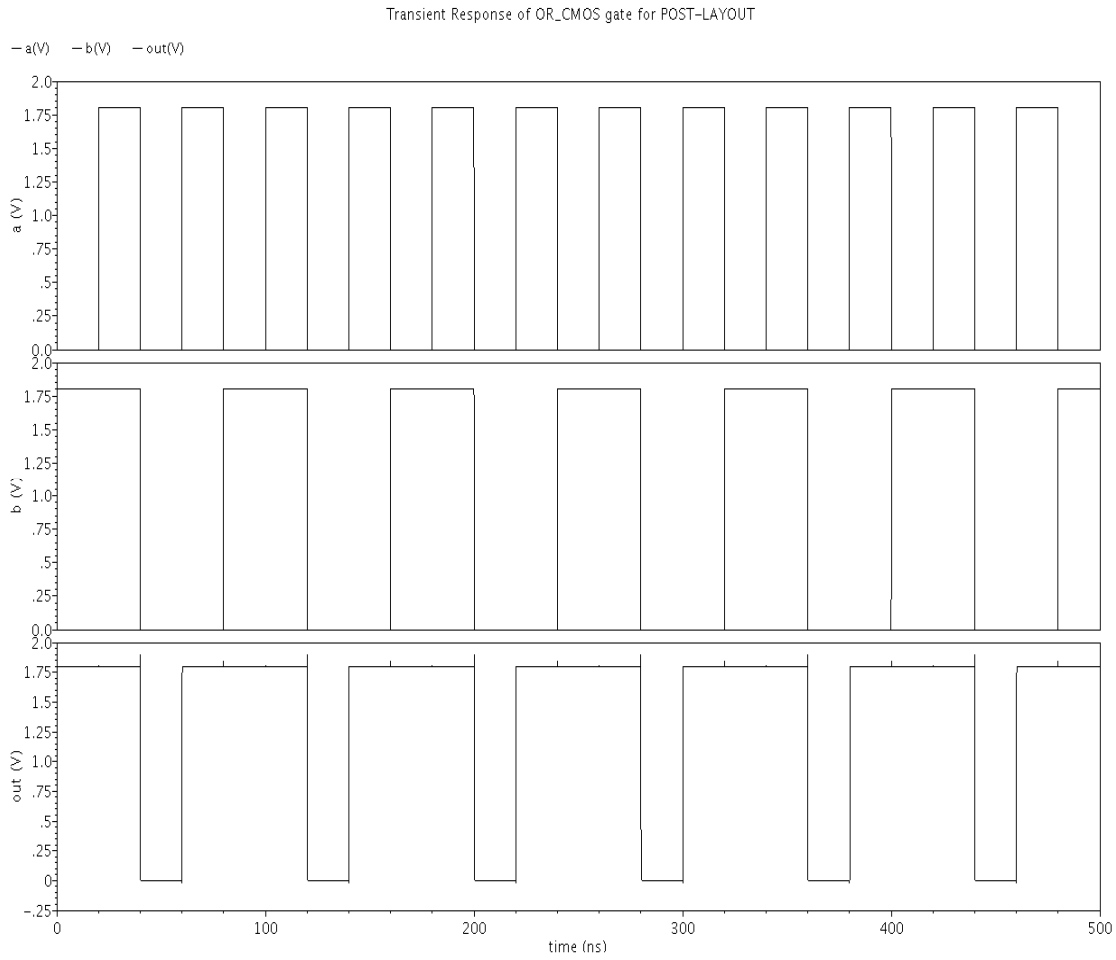


Figure 6.14. Post - Layout Simulation–Transient Analysis for Two-Input CMOS OR Gate.

6.4.5 POST - LAYOUT SIMULATION RESULTS FOR CMOS HALF ADDER

Figure 6.15 below shows the post-layout result of the transient analysis for a CMOS HALF ADDER.

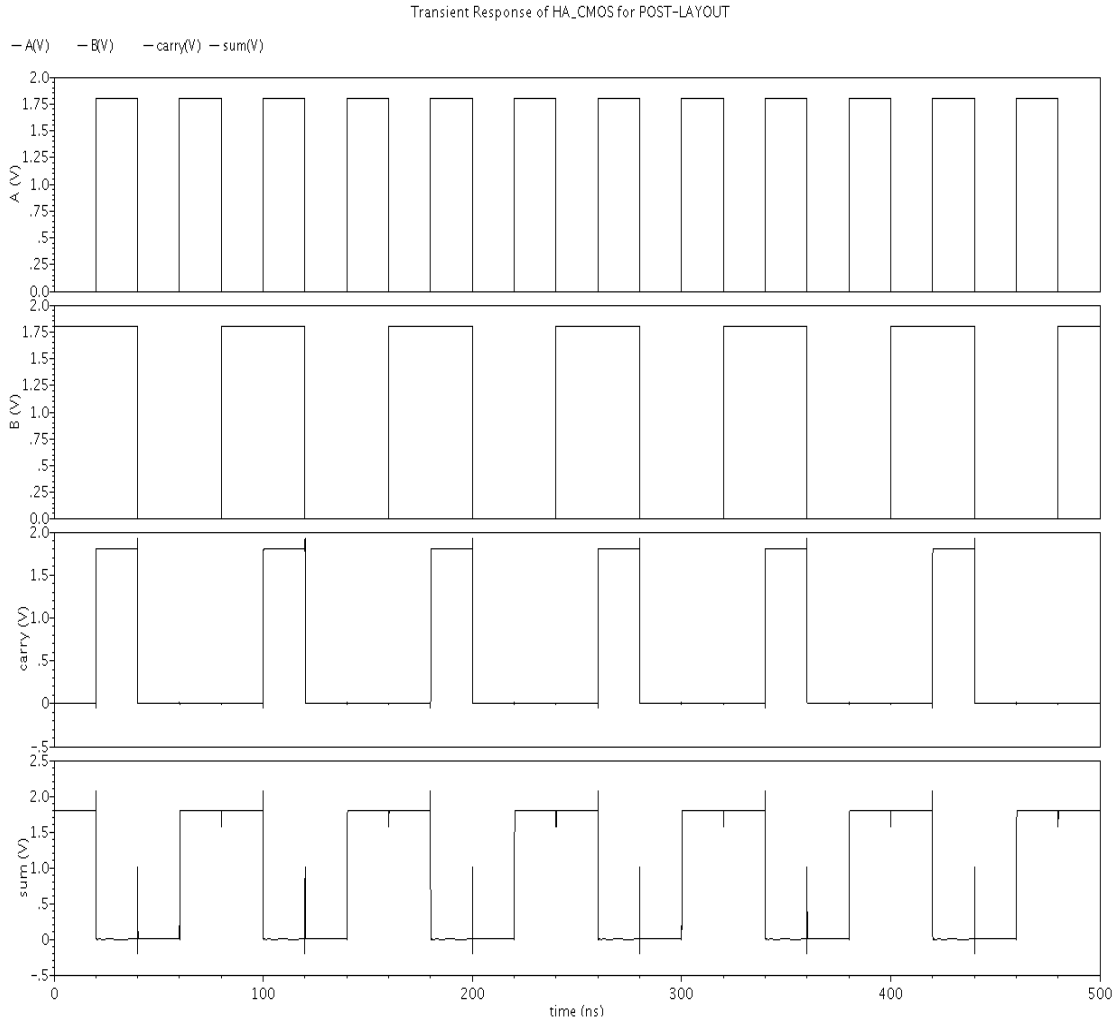


Figure 6.15. Post - Layout Simulation – Transient Analysis for CMOS HALF ADDER.

6.4.6 POST - LAYOUT SIMULATION RESULTS FOR ONE-BIT CMOS FULL ADDER

Figure 6.16 below shows the post-layout result of the transient analysis for a CMOS FULL ADDER.

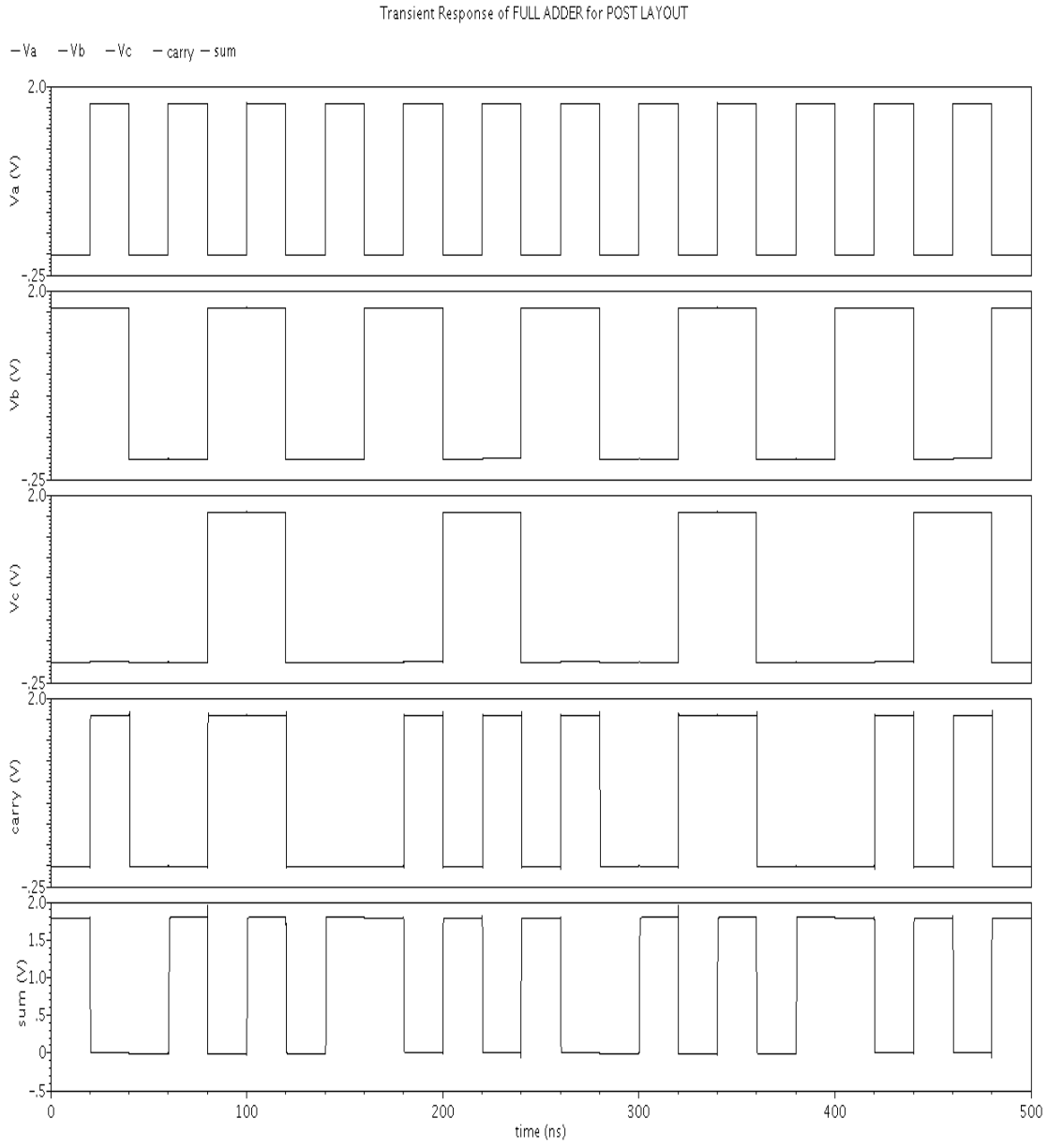


Figure 6.16. Post - Layout Simulation – Transient Analysis for CMOS FULL ADDER.

6.4.7 POST - LAYOUT SIMULATION RESULTS FOR OR GATE USING GDI TECHNIQUE

Figure 6.17 below shows the post-layout result of the transient analysis for a OR GATE using GDI technique.

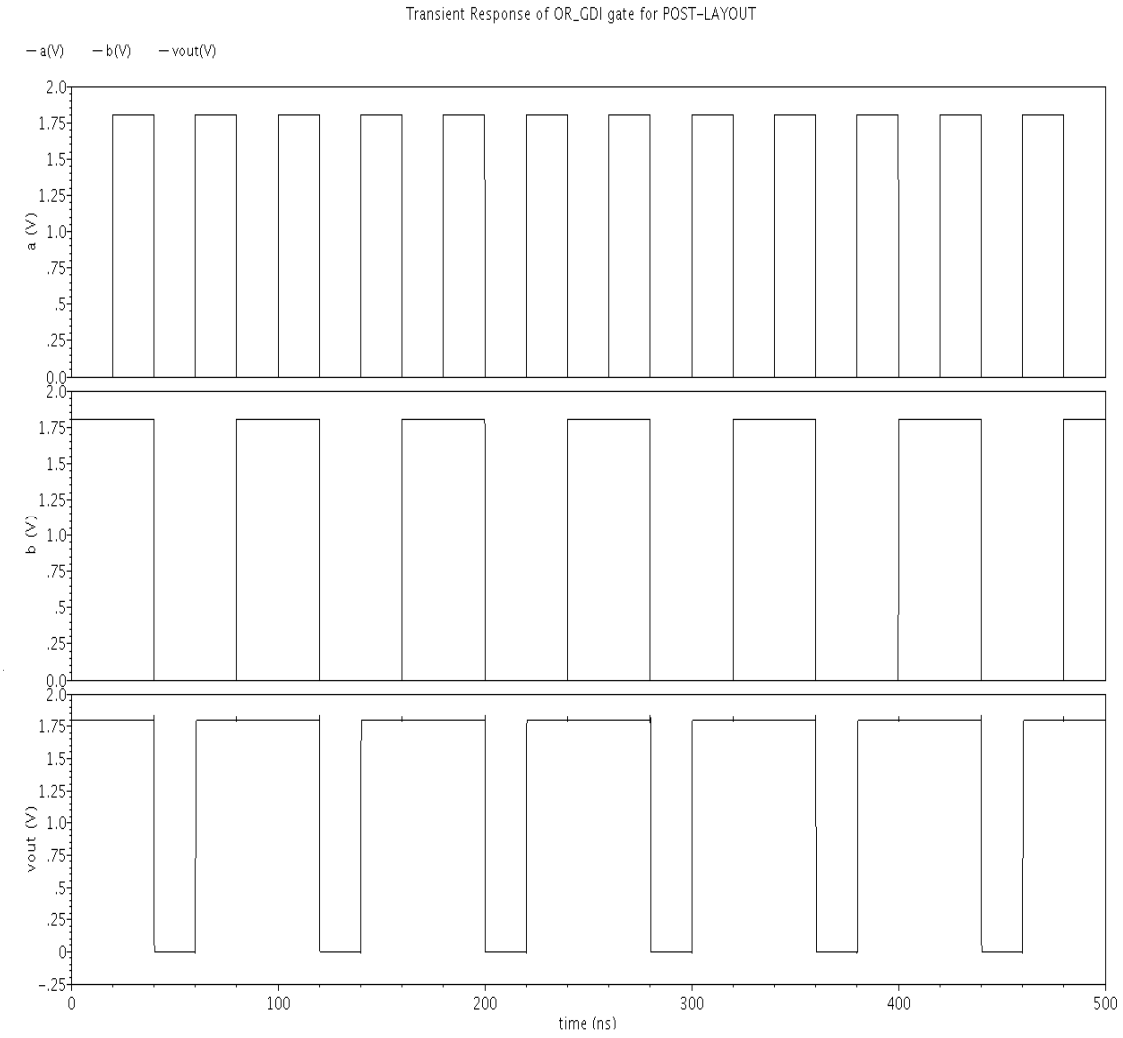


Figure 6.17. Post-Layout Simulation–Transient Analysis for OR GATE using GDI technique.

6.4.8 POST - LAYOUT SIMULATION RESULTS FOR XOR GATE USING GDI TECHNIQUE

Figure 6.18 below shows the post-layout result of the transient analysis for a XOR GATE using GDI technique.

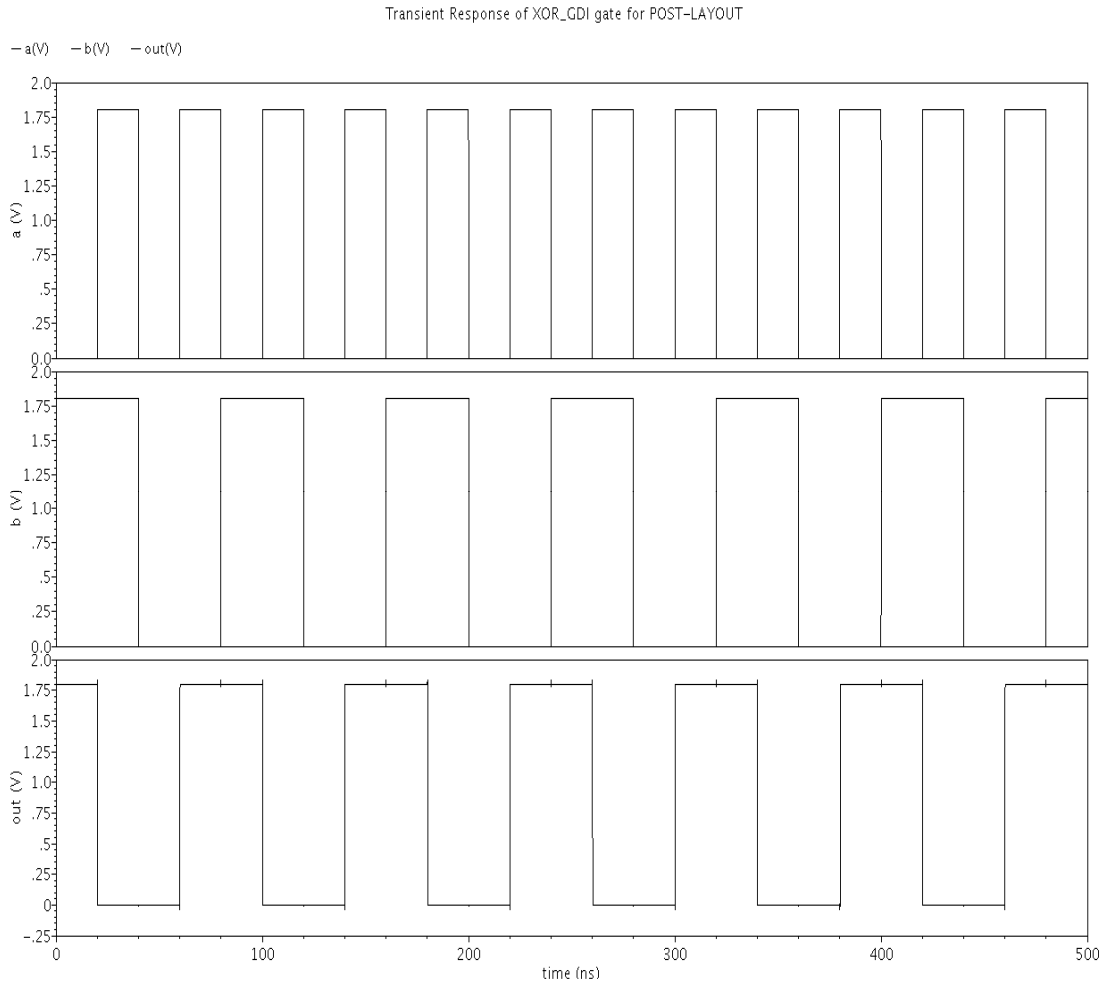


Figure 6.18. Post - Layout Simulation – Transient Analysis for XOR GATE using GDI technique.

6.4.9 POST - LAYOUT SIMULATION RESULTS FOR HALF ADDER USING GDI TECHNIQUE

Figure 6.19 below shows the post-layout result of the transient analysis for a HALF ADDER using GDI technique.

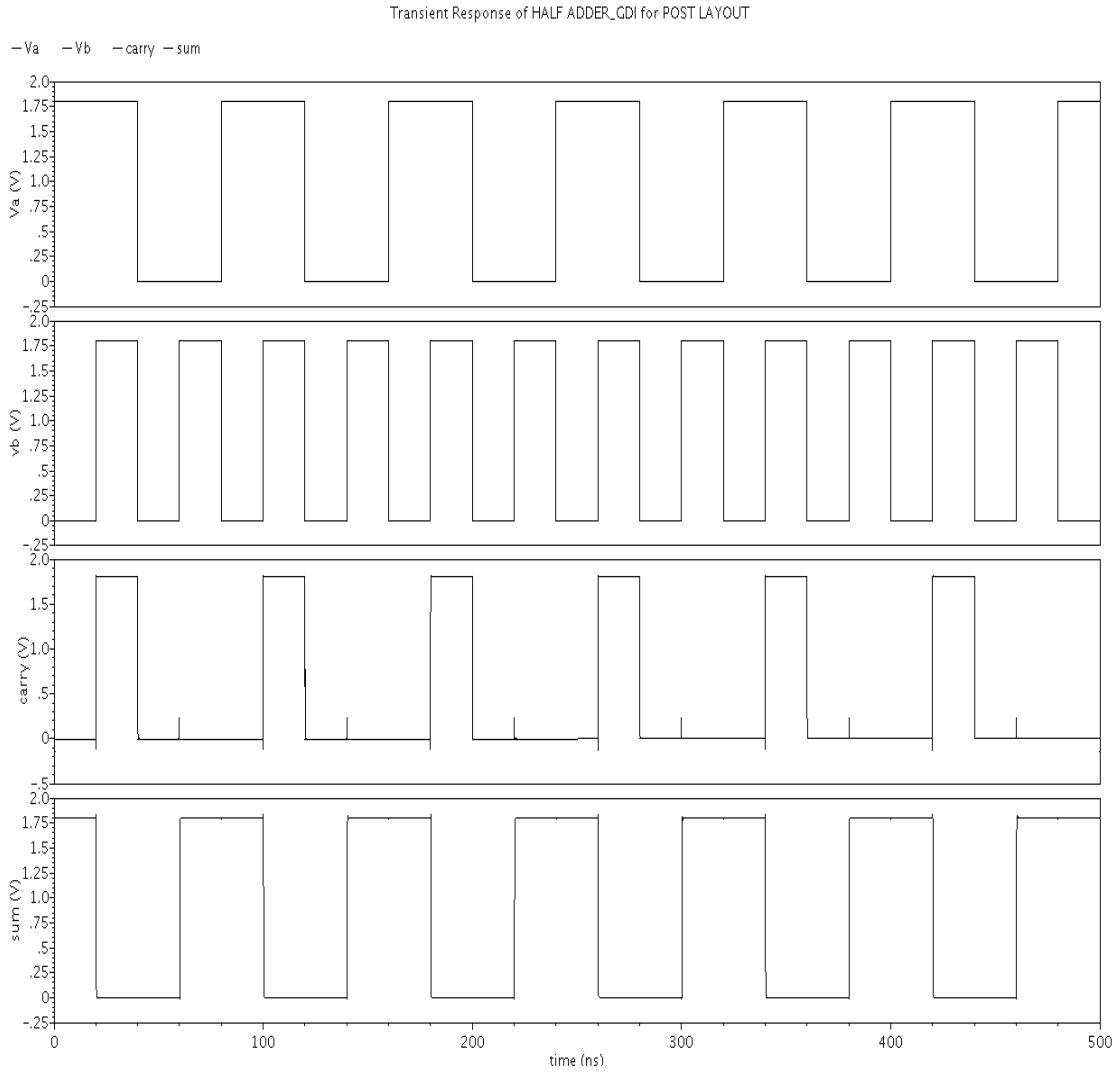


Figure 6.19. Post - Layout Simulation – Transient Analysis for HALF ADDER using GDI technique.

6.4.10 POST - LAYOUT SIMULATION RESULTS FOR FULL ADDER USING GDI TECHNIQUE

Figure 6.20 below shows the post-layout result of the transient analysis for a FULL ADDER using GDI technique.

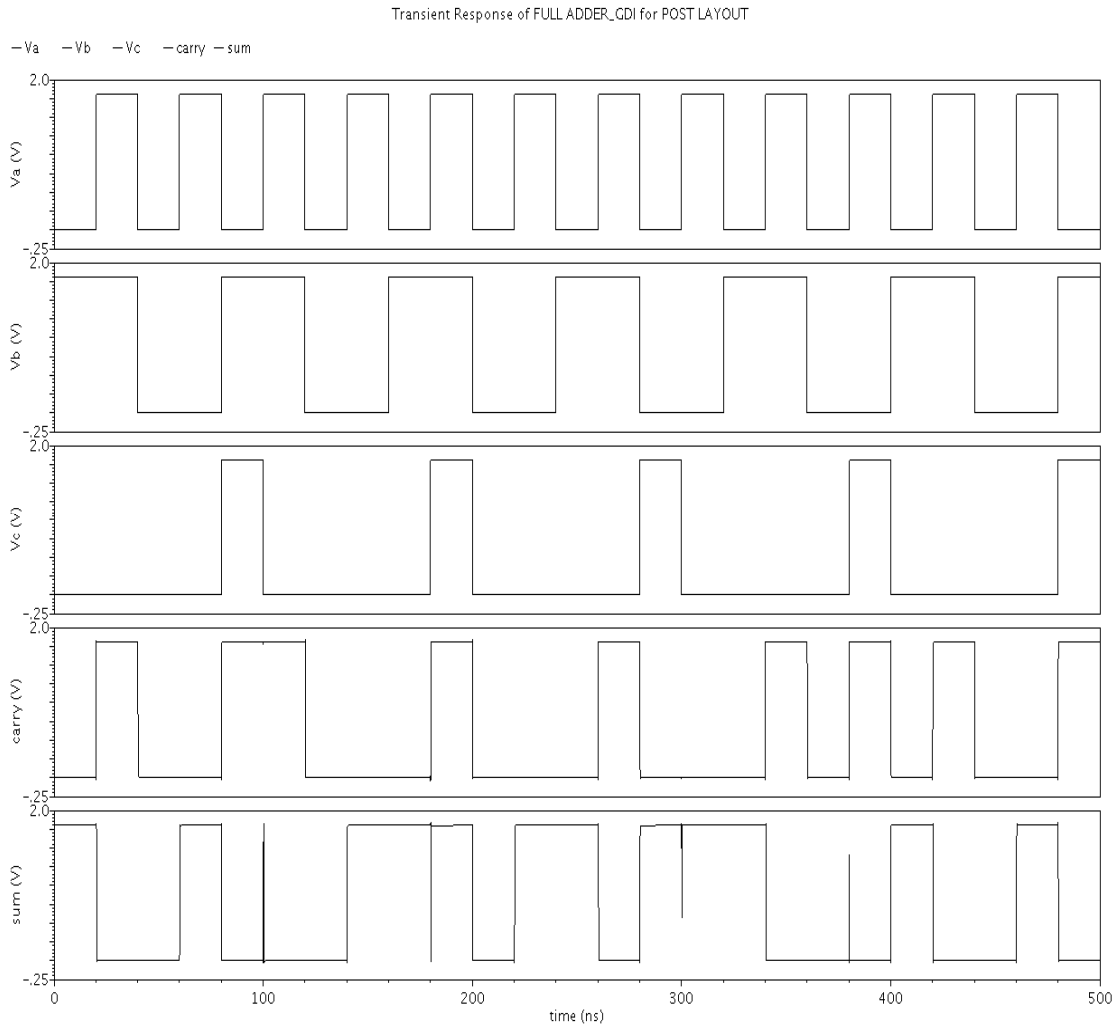


Figure 6.20. Post - Layout Simulation – Transient Analysis for FULL ADDER using GDI technique.

CHAPTER 7 CONCLUSIONS AND FUTURE SCOPE OF WORK

7.1 CONCLUSIONS

The primary goal of this thesis work is not only to provide an efficient result in low power VLSI design but also shows a successful try in terms of reduction of power dissipation . The basic low power CMOS cell structures as like a two-input AND gate, a two-input OR gate, a two-input XOR gate etc are designed using complementary CMOS logic style and an another effective approach Gate Diffusion Input technique.

The entire CMOS cell structures which are designed in this thesis work are designed in Cadence IC Design Architect using standard TSMC 0.18 μm Technology. Because of the main concern is power dissipation so after the schematic design and the simulation, different value of power dissipation at different value frequencies has been taken for both the logic style and compared with each other. All the circuits operate at a supply voltage of 1.8 V and load capacitance is varied according to the circuit design.

With gate diffusion input technique, the circuit energies are conserved rather than dissipated as heat. Besides the power reduction GDI technique also provide reduction in size as an example where in AND gate using the complementary CMOS logic style 6 transistor are used whereas using the GDI technique only 4

transistor are used. Depending on the application and the system requirements, this approach can be used to reduce the power dissipation of the digital systems. With the help of GDI technique, the power savings of up to 40 % to 60 % can be reached.

7.2 FUTURE SCOPE OF WORK

- Hence GDI technique can be used to design low power circuits such as digital wrist watches, radio frequency identification (RFID), sensor nodes, Laptops, pacemakers and battery operated devices such as, cellular phones etc.

- This thesis work is based on combinational circuit design so there is a highly fill place for the sequential circuit design for providing a better design. In low power VLSI design GDI technique has very good scope for future.

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APPENDIX A

SPICE BSIM3v3 VERSION 3.2 MOS MODEL PARAMETERS

The typical parameters are listed below:

DIODES & NMOSFET SPICE PARAMETERS

model bsim_diode_area diode
cj0=0.00103*(1+dcj_n_18_rf) vj=0.813 m=0.443
is=1e-06 n=1

model bsim_diode_perim diode
cj0=1.34e-10*(1+dcjsw_n_18_rf) vj=0.88 m=0.33
is=7e-11 n=1

model bsim_diode_swg diode
cj0=5e-10 *(1+ dcjgate_n_18_rf) vj=0.88 m=0.33
is=7e-11 n=1

model bsim_mos_transistor_mos bsim3v3 type=n

version=3.2	binunit=1	mobmod=1
capmod=2	nqsmod=0	noimod=2
tox=4.2e-09 + dtox_n_18_rf	toxm=4.2e-09	xj=1.6e-07
nch=3.745e+17	rsh=8	ngate=1e+23
vth0=0.3075 + dvth0_n_18_rf	k1=0.4578	k2=-0.02638
k3=-10.88	k3b=0.2379	w0=-8.813e-08
nlx=4.279e-07	dvt0=0.4042	dvt1=0.3237
dvt2=-0.8602	dvt0w=0.383	dvt1w=6e+05
dvt2w=-0.025	lint=1.587e-08	wint=1.022e-08
dwg=-3.396e-09	dwb=1.346e-09	u0=332.1 du0_n_18_rf
ua=-1.17e-09	ub=2.407e-18	uc=4.355e-11
vsat=8.1e+04	a0=1.93	ags=0.5072
b0=1.486e-06	b1=9.064e-06	keta=0.01752
a1=0	a2=1	voff=-0.1208
nfactor=1.038	cit=-0.001511	cdsc=0.002175
cdscd=0	cdscb=0.0008241	eta0=0.005504
etab=-0.001459	dsub=0.001592	pclm=0.741
pdiblc1=0.005061	pdiblc2=0.006001	pdiblcb=0
drout=0.001592	pscbe1=4.866e+08	pscbe2=3e-08
pvag=-0.2958	rdsw=9.905	prwg=1.1

prwb=0 wr=p_wr alpha0=0
alpha1=0 beta0=30 xpart=1
cgso=1.55e-10 *(1+dcgso_n_18_rf) cgdo=1.55e-10 *(1+dcgdo_n_18_rf)
cgbo=0
cgsl=3e-11*(1+dcgsl_n_18_rf) cgdl=3e-11 *(1+dcgdl_n_18_rf)
ckappa=0.6
cf=2.33e-11 *(1+dcf_n_18_rf) clc=1e-07 cle=0.6
dlc=4e-08 dwc=0 vfbcv=-1
noff=1 voffcv=0 acde=1
moin=15 noia=1.31826e+19
noib=1.44544e+05
noic=-1.24516e-12 em=4.1e+07 af=1
ef=0.92 kf=0 lmin=1.8e-07
lmax=1.805e-07 wmin=5e-06 wmax=1.05e-
04
xl=-1.05e-08 + dxl_n_18_rf xw=0 + dxw_n_18_rf js=1e-06
jsw=7e-11 cj=0.00103 *(1+dcj_n_18_rf) mj=0.443
pb=0.813 cjsw=1.34e-10 *(1+dcjsw_n_18_rf) mjsw=0.33
tnom=25 ute=-1.286 kt1=-0.2255
kt1l=-4.175e-09 kt2=-0.02527 ua1=2.153e-09
ub1=-2.673e-18 uc1=-3.832e-11 at=1.449e+04
prt=-46.18 xti=3 wl=0
wln=1 ww=7.262e-16 wwn=1
wwl=0 ll=-1.062e-15 lln=1
lw=2.996e-15 lwn=1 lwl=0
llc=-6.64e-15 lwc=0 lwlc=0
wlc=0 wwc=0 wwlc=0
lvth0=-0.0001 + dlvth0_n_18_rf wvth0=0.06027 + dwvth0_n_18_rf pvth0=0
dpvth0_n_18_rf
lnlx=-2.854e-08 wnlx=0 pnlx=0
lnfactor=0.032 wua=-1.88e-11 wu0=0.54
pub=3.8e-20 pw0=1.3e-09 lua=1.5e-11
lub=9.76e-20 wrdsw=0 weta0=0
wetab=0 leta0=0.001574 letab=0
peta0=0 petab=0 wpclm=0
wvoff=-0.0004078 lvoff=-0.004208 pvoff=-
0.0003788
wa0=-0.04731 la0=-0.4667 pa0=-0.02649
wags=0.004242 lags=0.3028 pags=0
wketa=0 lketa=-0.01942 pketa=0
wute=0.06373 lute=0 pute=0
wvsat=5066 lvsat=0 pvsat=0
dpvsat_n_18_rf
lpdiblc2=-0.004752 wat=7067 wprt=0
ldif=8e-08 hdif=2.6e-07 n=1
pbsw=0.88 cjswg=5e-10 *(1+dcjgate_n_18_rf) ctp=0.000914
ptp=0.000924 cta=0.000919 pta=0.00158
elm=5 tlevc=1

DIODES & PMOSFET SPICE PARAMETERS

model bsim_diode_area diode
cj0=0.00114 *(1+ dcj_p_18_rf) vj=0.762 m=0.395
is=3e-06 n=1

model bsim_diode_perim diode
cj0=1.74e-10 *(1+ dcjsw_p_18_rf) vj=0.665 m=0.324
is=4.12e-11 n=1

model bsim_diode_swg diode
cj0=4.2e-10 *(1+ dcjgate_p_18_rf) vj=0.665 m=0.324
is=4.12e-11 n=1

Model bsim_mos_transistor_mos bsim3v3 type=p

mobmod=3 version=3.2 capmod=2
binunit=1 nqsmod=0 noimod=2
tox=4.2e-09 + dtox_p_18_rf toxm=4.2e-09 xj=1e-07
nch=6.131e+17 ngate=1e+23 vth0=-0.4325
dvth0_p_18_rf
k1=0.5704 k2=0.006973 k3=-2.833
k3b=1.326 w0=-1.943e-07 nlx=2.56e-07
dvt0=0.4885 dvt1=0.09578 dvt2=0.1287
dvt0w=-0.1261 dvt1w=2.479e+04 dvt2w=0.6915
lint=-1.041e-08 wint=-1.525e-07 dwg=-1.151e-
07
dwb=-1.039e-07 u0=90+du0_p_18_rf ua=1.49e-09
ub=4.646e-19 uc=-0.09587 vsat=4.75e+04
a0=1.35 ags=0.3818 b0=-3.088e-07
b1=0 keta=0.01044 a1=0
a2=1 voff=-0.1073 nfactor=0.984
cit=-0.001067 cdsc=0.0007578 cdscd=0
cdscb=0.0001 eta0=1.071 etab=-0.9291
dsub=1.919 pclm=0.553 pdiblc1=0.007
pdiblc2=0.008005 pdiblcb=0 drout=0.157
pscbe1=4.866e+08 pscbe2=2.8e-07 pvag=-0.888
rdsw=202.1 prwg=1.2 prwb=0
wr=p_wr alpha0=0 alpha1=0
beta0=30
11*(1+dcgdl_p_18_rf)
ckappa=0.6 clc=1e-07 cle=0.6
dwc=2.3e-07 vfbcv=-1 noff=1
voffcv=0 acde=1 moin=15
noia=3.57456993317604e+18 noib=2.5e+03 noic=2.6126e-
11
em=4.1e+07 af=1 ef=1.1388
kf=0 lmin=1.8e-07 lmax=1.805e-
07

wmin=5e-06 wmax=1.05e-04 xl=-2e-09
dxl_p_18_rf
xw=0 + dxw_p_18_rf js=3e-06 jsw=4.12e-11
cj=0.00114*(1+dcj_p_18_rf) mj=0.395 pb=0.762
cjsw=1.74e-10 *(1+dcjsw_p_18_rf) mjsw=0.324 tnom=25
ute=-0.4484 kt1=-0.2194 kt1l=-8.204e-
09
kt2=-0.009487 ua1=4.571e-09 ub1=-6.026e-
18
uc1=-0.0985 at=1.203e+04 prt=0
xti=3 ww=1.236e-14 lw=-2.873e-16
ll=6.635e-15 wl=0 wln=1
wwn=1 wwl=0 lln=1
lwn=1 lwl=0 llc=-1.31e-14
lwc=0 lwlc=0 wlc=0
wwc=0 wwlc=0 lvth0=0.0057
dlvth0_p_18_rf
wvth0=-0.0148 + dwvth0_p_18_rf lu0=-3 lnfactor=0.03
pvth0=0.0031+ dpvth0_p_18_rf lnlx=-1.584e-08 wrdsw=10.07
weta0=0 wetab=0 wpclm=0
wua=2.7e-09 lua=-2.37e-10 pua=5.855e-11
wub=0 lub=0 pub=0
wuc=0 luc=0 puc=0
wvoff=-0.009816 lvoff=-0.0009871 pvoff=-9.833e-
05
wa0=-0.04807 la0=-0.281 pa0=0.08661
wags=-0.04177 lags=0.04454 pags=-0.04076
wketa=0 lketa=-0.012 pketa=0
wute=-0.2682 lute=0 pute=0
wvsat=-1.42e+04 lvsat=0 pvsat=-350
dpvsat_p_18_rf
lpdiblc2=0.003012 wat=-6405 wprt=216.6
n=1 pbsw=0.665 cta=0.001
ctp=0.000753 pta=0.00155 ptp=0.00124
ldif=8e-08 rsh=8 rd=0
rsc=0 rdc=0 hdif=2.6e-07
rs=0

The variations in the values of the parameters for different corners are given below:

NOTE: In **CADENCE** following notations are used for corners:

tt : typical NMOS and typical PMOS

ff : fast NMOS and fast PMOS

ss : slow NMOS and slow PMOS

fnsp : fast NMOS and slow PMOS

snfp : slow NMOS and fast PMOS

SECTION tt

dcd_n_18_rf=0
dcgs_n_18_rf=0
drgate_n_18_rf=0
dtox_n_18_rf=0.0000e+00
dxl_n_18_rf=0.0000e+00
dxw_n_18_rf=0.0000e+00
dvth0_n_18_rf=0.0000e+00
du0_n_18_rf=0.0000e+00
dlvth0_n_18_rf=0.0000e+00
dwvth0_n_18_rf=0.0000e+00
dwu0_n_18_rf=0.0000e+00
dpvth0_n_18_rf=0.0000e+00
dpvsat_n_18_rf=0.0000e+00
dcf_n_18_rf=0.0000e+00
dcgdo_n_18_rf=0.0000e+00
dcgdl_n_18_rf=0.0000e+00
dcgso_n_18_rf=0.0000e+00
dcgsl_n_18_rf=0.0000e+00
dcj_n_18_rf=0.0000e+00
dcjsw_n_18_rf=0.0000e+00
dcjgate_n_18_rf=0.0000e+00
dcd_p_18_rf=0
dcgs_p_18_rf=0
drgate_p_18_rf=0
dcgdl_p_18_rf=0.0000e+00
dcgsl_p_18_rf=0.0000e+00
dcf_p_18_rf=0.0000e+00
dtox_p_18_rf=0.0000e+00
du0_p_18_rf=0.0000e+00
dxl_p_18_rf=0.0000e+00
dxw_p_18_rf=0.0000e+00
dvth0_p_18_rf=0.0000e+00
dlvth0_p_18_rf=0.0000e+00
dwvth0_p_18_rf=0.0000e+00
dpvth0_p_18_rf=0.0000e+00
dpvsat_p_18_rf=0.0000e+00
dcgdo_p_18_rf=0.0000e+00
dcgso_p_18_rf=0.0000e+00
dcj_p_18_rf=0.0000e+00
dcjsw_p_18_rf=0.0000e+00
dcjgate_p_18_rf=0.0000e+00

SECTION ss

dcd_n_18_rf=0.1
dcgs_n_18_rf=0.15
drgate_n_18_rf=0.35
dtox_n_18_rf=1.0000e-10
dxl_n_18_rf=2.2000e-08
dxw_n_18_rf=-2.0000e-08
dvth0_n_18_rf=1.4500e-02
du0_n_18_rf=-1.0000e+01
dlvth0_n_18_rf=1.4000e-03
dwvth0_n_18_rf=1.1000e-02
dwu0_n_18_rf=-4.5000e+00
dpvth0_n_18_rf=-1.0000e-03
dpvsat_n_18_rf=1.4000e+02
dcgdo_n_18_rf=-0.1
dcgso_n_18_rf=-0.1
dcgdl_n_18_rf=-0.1
dcgsl_n_18_rf=-0.1
dcf_n_18_rf=0.15
dcj_n_18_rf=0.1
dcjsw_n_18_rf=0.1
dcjgate_n_18_rf=0.1
dcd_p_18_rf=0.1
dcgs_p_18_rf=0.15
drgate_p_18_rf=0.35
dcgdl_p_18_rf=-0.1
dcgsl_p_18_rf=-0.1
dcf_p_18_rf=0.15
dtox_p_18_rf=1.0000e-10
du0_p_18_rf=-0.0e+00
dxl_p_18_rf=1.0000e-08
dxw_p_18_rf=-2.0000e-08
dvth0_p_18_rf=-1.4000e-02
dlvth0_p_18_rf=0.0000e-00
dwvth0_p_18_rf=-1.0000e-02
dpvth0_p_18_rf=3.0000e-04
dpvsat_p_18_rf=4.6000e+01
dcgdo_p_18_rf=-0.1
dcgso_p_18_rf=-0.1
dcj_p_18_rf=0.1
dcjsw_p_18_rf=0.1
dcjgate_p_18_rf=0.1

SECTION ff

dcd_n_18_rf=-0.1
dcgs_n_18_rf=-0.15
drgate_n_18_rf=-0.35
dtox_n_18_rf=-1.0000e-10
dxl_n_18_rf=-1.3600e-08
dxw_n_18_rf=2.0000e-08
dvth0_n_18_rf=-1.4500e-02
du0_n_18_rf=1.0000e+01
dlvth0_n_18_rf=-7.0000e-04
dwvth0_n_18_rf=-1.0100e-02
dwu0_n_18_rf=2.0000e+00
dpvth0_n_18_rf=6.5000e-04
dpvsat_n_18_rf=-8.0000e+01
dcgdo_n_18_rf=0.1
dcgso_n_18_rf=0.1
dcgdl_n_18_rf=0.1
dcgsl_n_18_rf=0.1
dcf_n_18_rf=-0.15
dcj_n_18_rf=-0.1
dcjsw_n_18_rf=-0.1
dcjgate_n_18_rf=-0.1
dcd_p_18_rf=-0.1
dcgs_p_18_rf=-0.15
drgate_p_18_rf=-0.35
dcgdl_p_18_rf=0.1
dcgsl_p_18_rf=0.1
dcf_p_18_rf=-0.15
dtox_p_18_rf=-1.0000e-10
du0_p_18_rf=0
dxl_p_18_rf=-8.0000e-09
dxw_p_18_rf=1.5000e-08
dvth0_p_18_rf=1.8000e-02
dlvth0_p_18_rf=-1.0000e-03
dwvth0_p_18_rf=8.5000e-03
dpvth0_p_18_rf=1.0000e-05
dpvsat_p_18_rf=-2.1000e+01
dcgdo_p_18_rf=0.1
dcgso_p_18_rf=0.1
dcj_p_18_rf=-0.1
dcjsw_p_18_rf=-0.1
dcjgate_p_18_rf=-0.1

SECTION snfp

dcd_n_18_rf=0.05
dcgs_n_18_rf=0.075
drgate_n_18_rf=0.175
dtox_n_18_rf=0.0000e+00
dxl_n_18_rf=1.1000e-08
dxw_n_18_rf=-1.0000e-08
dvth0_n_18_rf=1.3000e-02
du0_n_18_rf=-5.0000e+00
dlvth0_n_18_rf=1.1000e-03
dwvth0_n_18_rf=4.7000e-03
dwu0_n_18_rf=-2.0000e+00
dpvth0_n_18_rf=-5.5000e-04
dpvsat_n_18_rf=6.0000e+01
dcgdo_n_18_rf=0.0000e+00
dcgso_n_18_rf=0.0000e+00
dcgdl_n_18_rf=0.0000e+00
dcgsl_n_18_rf=0.0000e+00
dcf_n_18_rf=0.075
dcj_n_18_rf=0.05
dcjsw_n_18_rf=0.05
dcjgate_n_18_rf=0.05
dcd_p_18_rf=-0.05
dcgs_p_18_rf=-0.075
drgate_p_18_rf=-0.175
dcgdl_p_18_rf=0
dcgsl_p_18_rf=0
dcf_p_18_rf=-0.075
dtox_p_18_rf=0.0000e+00
du0_p_18_rf=0
dxl_p_18_rf=-4.0000e-09
dxw_p_18_rf=1.0000e-08
dvth0_p_18_rf=1.7000e-02
dlvth0_p_18_rf=-3.0000e-04
dwvth0_p_18_rf=3.5000e-03
dpvth0_p_18_rf=9.0000e-05
dpvsat_p_18_rf=-3.0000e+01
dcgdo_p_18_rf=0.0000e+00
dcgso_p_18_rf=0.0000e+00
dcj_p_18_rf=-0.05
dcjsw_p_18_rf=-0.05
dcjgate_p_18_rf=-0.05

SECTION fnsp

dcd_n_18_rf=-0.05
dcgs_n_18_rf=-0.075
drgate_n_18_rf=-0.175
dtox_n_18_rf=0.0000e+00
dxl_n_18_rf=-9.5000e-09
dxw_n_18_rf=1.0000e-08
du0_n_18_rf=6.0000e+00
dvth0_n_18_rf=-1.2300e-02
dlvth0_n_18_rf=-7.0000e-04
dwvth0_n_18_rf=-4.6000e-03
dwu0_n_18_rf=1.7000e+00
dpvth0_n_18_rf=4.1000e-04
dpvsat_n_18_rf=-7.0000e+01
dcgdo_n_18_rf=0.0000e+00
dcgso_n_18_rf=0.0000e+00
dcgdl_n_18_rf=0.0000e+00
dcgsl_n_18_rf=0.0000e+00
dcf_n_18_rf=-0.075
dcj_n_18_rf=-0.05
dcjsw_n_18_rf=-0.05
dcjgate_n_18_rf=-0.05
dcd_p_18_rf=0.05
dcgs_p_18_rf=0.075
drgate_p_18_rf=0.175
dcgdl_p_18_rf=0
dcgsl_p_18_rf=0
dcf_p_18_rf=0.075
dtox_p_18_rf=0.0000e+00
dxl_p_18_rf=4.5000e-09
dxw_p_18_rf=-1.0000e-08
dvth0_p_18_rf=-1.3000e-02
du0_p_18_rf=0
dlvth0_p_18_rf=-3.0000e-04
dwvth0_p_18_rf=-5.0000e-03
dpvth0_p_18_rf=1.3000e-04
dpvsat_p_18_rf=3.4000e+01
dcgdo_p_18_rf=0.0000e+00
dcgso_p_18_rf=0.0000e+00
dcj_p_18_rf=0.05
dcjsw_p_18_rf=0.05
dcjgate_p_18_rf=0.05