

**DESIGN AND ANALYSIS OF ALL OPTICAL LOGIC GATES
BASED ON 2-D PHOTONIC CRYSTALS**

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Submitted by

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CERTIFICATE AND DECLARATION

I, Deeksha Rani, hereby declare that the work which is being presented in the dissertation entitled, “ **DESIGN AND ANALYSIS OF ALL OPTICAL LOGIC GATES BASED ON 2-D PHOTONIC CRYSTALS**” in partial fulfillment of the requirement for the award of degree of M.E in Electronics and Communication submitted in Electronics and Communication Engineering Department of Thapar University, Patiala is an authentic record of my own work carried out under the supervision of **Dr. R. S. Kaler**, Senior Professor, ECED.


The matter presented in this dissertation has not been submitted in any other University/Institute for the award of degree.

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ABSTRACT

Photonic crystal is artificially designed optical material in which dielectric constant changed periodically. Due to their unique properties, the photonic crystal based logic gates have numerous advantages over the conventional logic gates such as compactness, simple structure, high speed and high confinement. The size of optical logic gate based on photonic crystal is in the order of wavelength. The photons are not affected by the external disturbance; it results in low transmission losses. There are some wavelengths which do not propagate through the structure and form the photonic band gap. By engineering the photonic band gap, the flow of light can be controlled. These logic structures are key component of optical network and optical communication system. Because of various advantages, it is favorable for use of future optical signal processors and optical computers.

The objective of this dissertation is to analyze the performance of 2-D photonic crystal based all optical logic gates and for this purpose Opti-FDTD software is used which allows the design of various configurations of photonic crystal structures.

Firstly, a simple design of optical logic OR gate is presented for the application of switching as it has high extinction ratio. This structure is compact as well as suitable to design other optical circuits. Secondly, all optical logic NOR gate is designed based on two cross waveguides structures. These cross waveguide structures are optical NOT and OR gate. The parameter of structure (NOT and OR gate) is optimized by iterative process. These optimized structures have high contrast ratio. Thirdly, a simultaneous implementation of NOT and AND gate to design optical NAND logic gate without using any external device. These structures are compact in size and have high contrast ratio compared to the earlier reported work. For practical applications, analyze the fabrication error tolerance of NAND gate. These structures are simple to fabricate; so it is favorable for use of future optical communication system and signal processor.

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LIST OF ACRONYMS

1D	One-Dimensional
2D	Two-Dimensional
3D	Three-Dimensional
AOLG	All Optical Logic Gates
ASK	Amplitude Shift Keying
BDM	Broadband Defect Mode
BPSK	Binary Phase Shift keying
DC	Directional Coupler
EM	Electromagnetic Waves
FDTD	Finite Difference Time Domain
GVD	Group Velocity Dispersion
IRS	Intrapulse Raman Scattering
KHz	Kilohertz
MMI	Multi-Mode Interference
NLDC	Non-Linear Directional Coupler
OLNG	Optical Logic Not Gate
PAM	Pulse Amplitude Modulation
PBG	Photonic Band Gap
PCFs	Photonic Crystal Fibers
PCRR	Photonic Crystal Ring Resonators

PhC	Photonic Crystal
PIC	Photonic Integrated Circuits
PWE	Plane Wave Expansion
Si	Silicon
SOA	Semiconductor Optical Amplifiers
SPM	Self-Phase Modulation
TE	Transverse Electric
THz	Terahertz
TIR	Total Internal Reflection
TM	Transverse Magnetic
VCSEL	Vertical Cavity Surface Emitting Lasers
XPM	Cross-Phase Modulation

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CHAPTER 1

INTRODUCTION

The semiconductor has played an important role in our daily life and changed the world beyond anything. However, the research for the miniaturization and high speed of integrated circuit has occurred in every part of the world. This miniaturization of circuit results in increased resistance and high power losses. In order to achieve high speed of computing and compact circuits, the researchers have turned towards photon instead of electrons. Light has a number of advantages over electrons. The bandwidth of optic system is in the order of THz but in the electronic system the bandwidth is only KHz [1, 2]. Since the information carriers are photons they do not interact by environmental disturbance. Although performance of electronic system is improved day by day but a new optical material known as photonic crystal [3] is introduced.

The requirement of material that controls the flow of photon is the main idea behind the design of PhCs. The traditional mechanism used for the manipulation of flow of photon is total internal reflection. But the photonic crystals provide a totally different mechanism for the control of light. The photonic band gap (due to periodically varying dielectric constant) controls the flow of light. There are various advantages such as compactness, confinement, and low power consumption. These advantages make it suitable for PIC [4]. There are number of applications by engineering the photonic band gap such as optical filter, resonator, logic gates etc.

1.1 PHOTONIC CRYSTALS

Photonic crystal is a new category of optical material in which dielectric constant changes periodically. The space in which dielectric constant placed in particular pattern is known as crystal lattice and the distance between two dielectric crystals is lattice constant. The light propagates inside the crystal then refraction and reflection occurs at each interface of the dielectric material. It causes interference due to which some wavelengths close to periodicity of dielectric constant do not propagate through the photonic crystal. These forbidden wavelengths form the band gap which is similar to electronic band gap [5]. The study of photonic crystals is analogous to the semiconductor in solid state physics. This

photonic band gap (PBG) controls the flow of photon or light. This enables to change the flow of photons by engineering the crystals for particular application.

There are number of difference between photonic crystal and lattice of ions (crystals). In photonic crystal, particles which scattered are photon whereas in semiconductor electrons scattered through the lattice as shown in Fig. 1.1. The former based on Maxwell's equation while the latter based on Schrodinger's equation. Semiconductor crystal forbidden the certain energy but photonic crystal forbidden certain range of frequency. This forbidden range of frequency does not propagate through the lattice. The photonic crystals are artificially fabricated material for particular PBG in contrast to the naturally occurring semiconductor material. The main problem in fabrication is the size of lattice constant must be around half the wavelength of EM waves.

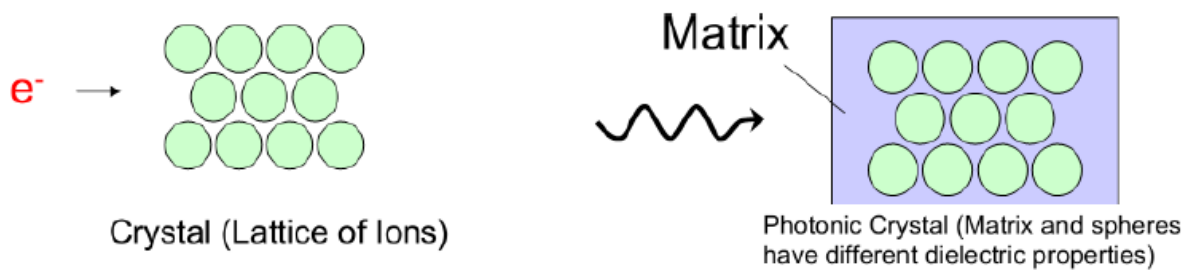


Fig. 1.1 Analogy of ionic lattice in semiconductor and photonic crystal lattice [2].

The properties of PhC can be changed through the process of doping in which dielectric rods are added or removed in the certain region. This addition or removal of dielectric material is known as defect (Point defect or Line defect). This defect causes localization of electromagnetic waves (EM) in the PBG [6]. The periodicity of photonic crystal is broken by introducing the defect which leads to the number of applications.

1.2 HISTORICAL PERSPECTIVE OF PHOTONIC CRYSTALS

In 1887, Lord Rayleigh studied the 1-D photonic crystals consist of multi-layer dielectric stacks [7]. This study showed the photonic band gap which also know as stop band. Vladimir P. Bykov investigated the effect of band gap on the spontaneous emission within the structure [8]. He also gave theoretical concept for 2-D and 3-D PhC structures [9]. In 1979, Ohtaka developed a formal for the calculation of band gap of 3-D PhC structures [10].

In 1987, the two milestone papers were published by Yablonovitch and John. The main idea of Yablonovitch's paper was to control the spontaneous emission by engineering the density of states [11]. The idea of John's paper was to control the flow of light by using photonic crystal [6]. It is difficult to design the structure in optical scale. It results most of work that were theoretically studied. In 1991, Yablonovitch presented the first 3-D band gap in the microwave regime [12].

Thomas Krauss demonstrated the 2D photonic crystal at the optical wavelength in 1996 [13]. There are number of research work occurred around the world to improve the optical processing as well as to use the PhC slab. In 1998, Philip Russell developed first commercial used photonic crystal fiber [14]. The study of 2-D photonic crystal is fast as compared to 3-D, due to difficulty level of construction. There is study of naturally occurring PhC based structure for better understanding [15]. Table 1.1 shows the progress of photonic crystal in brief.

1887	Study of 1-D PhC which show the stop band [7].
1987	Two milestone paper was published based on 2-D photonic crystal [6,11]
1991	Yablonovitch verified the existence for 3-D PhC in the micrometer range [12].
1996	Present the 2-D PhC at the optical wavelength [13]
1998	Development of first commercial optical fiber based on photonic crystal [14]

Table 1.1 Historical progress of photonic crystal.

1.3 NUMERICAL ANALYSIS

All the electromagnetic waves including the propagation of light in any dielectric medium is governed by four differential Maxwell Equations [3]. The equations in SI unit are given below:

$$\nabla \times H - \frac{\partial D}{\partial t} = J$$

$$\nabla \times E + \frac{\partial B}{\partial t} = 0$$

$$\nabla \cdot B = 0$$

$$\nabla \cdot D = \rho \quad (1.1)$$

where H and E are the magnetic and electric fields respectively, B and D are the magnetic induction field and electric displacement, respectively and J and ρ are the free current and free charge densities, respectively.

For the linear, macroscopic, isotropic, dispersive and transparent materials, the magnetic induction field and electric displacement is related to magnetic and electric field respectively through the following equations

$$\begin{aligned} B &= \mu H = \mu_0 \mu_r H \\ D &= \varepsilon E = \varepsilon_0 \varepsilon_r E \end{aligned} \quad (1.2)$$

where μ and ε are the permeability and permittivity of the material respectively. μ_0 is $4\pi \times 10^{-7}$ Henry/m and ε_0 is 8.854×10^{-12} Farad/m in the vacuum permeability and permittivity respectively.

We now assumed that there is no free charge or current in the structure so $\rho=0$ and $J=0$. With all the above assumptions and relations, the Maxwell equations (1.1) become

$$\begin{aligned} \nabla \times H - \frac{\partial D}{\partial t} &= 0 \\ \nabla \cdot D &= 0 \end{aligned} \quad (1.3)$$

So,

$$\begin{aligned} \nabla \times H &= \varepsilon_0 \varepsilon_r \frac{\partial E}{\partial t} \\ \nabla \times E &= -\mu_0 \frac{\partial H}{\partial t} \\ \nabla \cdot H &= 0 \\ \nabla \cdot E &= 0 \end{aligned} \quad (1.4)$$

The electric and magnetic field are the function of space and time. The Maxwell equations are linear so the dependence of time can be separated from the dependence of spatial by expanding E and H fields into a set of harmonic modes. Now harmonic mode can be written as a mode profile times a complex exponential:

$$\begin{aligned} H(r, t) &= H(r) e^{-i\omega t} \\ E(r, t) &= E(r) e^{-i\omega t} \end{aligned} \quad (1.5)$$

By substituting above equations into equations (1.4), the mode profiles for any frequency can be governed by the equations given below:

$$\begin{aligned}\nabla \cdot H(r) &= 0 \\ \nabla \cdot E(r) &= 0\end{aligned}\tag{1.6}$$

The two curl equations are

$$\begin{aligned}\nabla \times H(r) &= -i\omega\epsilon_0\epsilon_r E(r) \\ \nabla \times E(r) &= i\omega\mu_0 H(r)\end{aligned}\tag{1.7}$$

To decouple the above equations, divide the magnetic field equation of 1.7 by ϵ_r and then take the curl.

$$\nabla \times \left(\frac{1}{\epsilon_r} \nabla \times H(r) \right) = -i\omega\epsilon_0 (\nabla \times E(r))\tag{1.8}$$

Substitute the value of $E(r)$ from the equation 1.7 in the above and also used the relation of speed of light and constants ϵ_0 and μ_0 as $c = 1/\sqrt{\epsilon_0\mu_0}$. The resultant equation is known as master equation which is given below:

$$\nabla \times \left(\frac{1}{\epsilon_r} \nabla \times H(r) \right) = \left(\frac{\omega}{c} \right)^2 H(r)\tag{1.9}$$

E can be found from the equation (1.7) and (1.9). It also satisfies the transversality requirement due to divergence curl is always zero. Equation (1.9) is also known as eigenvalue problem. Here eigenvectors is magnetic field $H(r)$; Eigen values are $(\omega/c)^2$ which have real and orthogonal values and Eigen operator is the Hermitian $(\nabla \times \frac{1}{\epsilon} \nabla \times)$ operator. This operator is linear operator.

1.4 TYPE OF PHOTONIC CRYSTALS

On the basis of geometry, Photonic crystal can be categorized into three ways: One-Dimensional (1D), Two-Dimensional (2D) and Three-Dimensional (3D) PhC [3, 16]. In 1D photonic crystal structure, the dielectric material changes only in one direction. The photonic band gap exists only in that direction. The propagation of electromagnetic wave is affected along that lattice direction where dielectric constant is changed. This is

simplest as well as easiest to fabricate the structure. This is not the new arrangement. This is being used as mirror in vertical cavity surface emitting lasers (VCSELs) from the time when PhC are not known [17]. It also known as distributed Bragg mirror. The different types of photonic crystals are illustrated in Fig. 1.2.

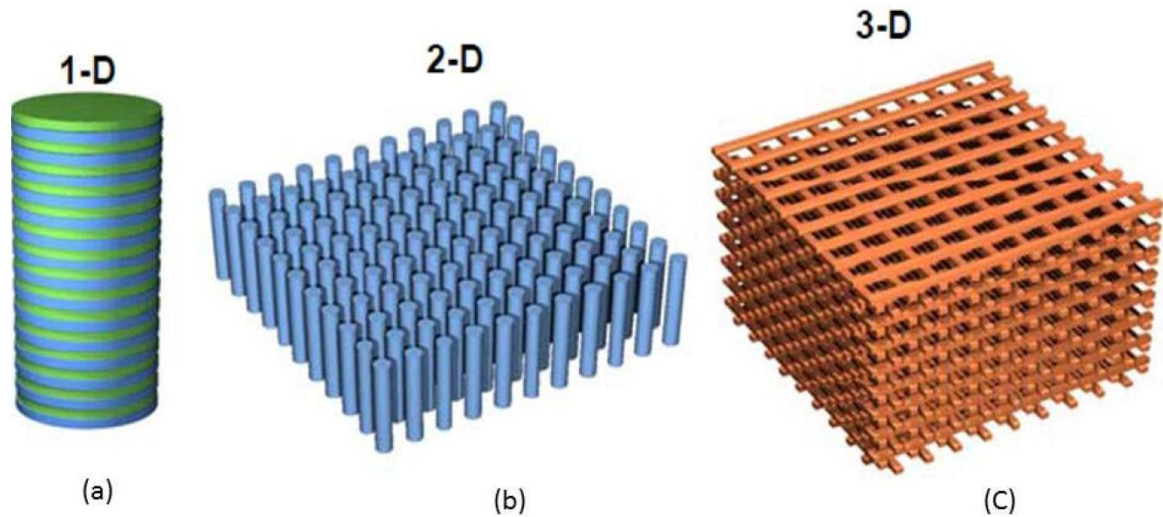


Fig. 1.2 Schematic illustration of PhC (a) one-dimensional (b) two-dimensional (c) three-dimensional [18]

In 2D photonic crystal, dielectric constant is periodically changed along two directions but is uniform in third direction. It is formed by placing periodically dielectric rods in the air or by air rods in the dielectric substrate. The PBG exist in the plane of periodicity and light do not propagate in this plane [13]. For the propagation of light in this plane, the harmonic modes can be divided into two independent polarizations (TE and TM mode). Each polarization has its own different band structures. It is possible that the PBG may exist for one of polarization but not for other. By introducing the defects, light can be localized in the band gap and crystals' face can support the surface states.

In 3D photonic crystal, dielectric constant is changed periodically in all the direction. Therefore there is no axis along which light can propagate in the structure [12]. It results in complete band gap. It is difficult to localize the EM waves at the point defects and propagate through the linear defect. In 1D and 2D can localize light at the point or line defect but in 3D there is extra capability to localize the light in all directions.

The two dimensional PhCs have attracted the researchers and scientists because it is easy to fabricate and analyze. In this thesis work, two dimensional photonic crystals with square lattice are considered.

1.5 TYPE OF DEFECTS

There are two types of defects: Point defects and Line defects. Disturbing a single lattice site causes a defect along a line in the z direction. This defect has broken the symmetry of periodic dielectric constant. It causes localization of light or set of closely mode to a point in the plane of propagation [6, 11]. These modes have frequency within the band gap. This disturbance is known as point defect or cavity. In the simple words, cavity is surrounded by reflecting walls that don't allowed escaping of light thus leads to mode. There are number of ways like replace the single column with another shape, size or dielectric constant than the original or remove a column from the crystal as shown in Fig. 1.3

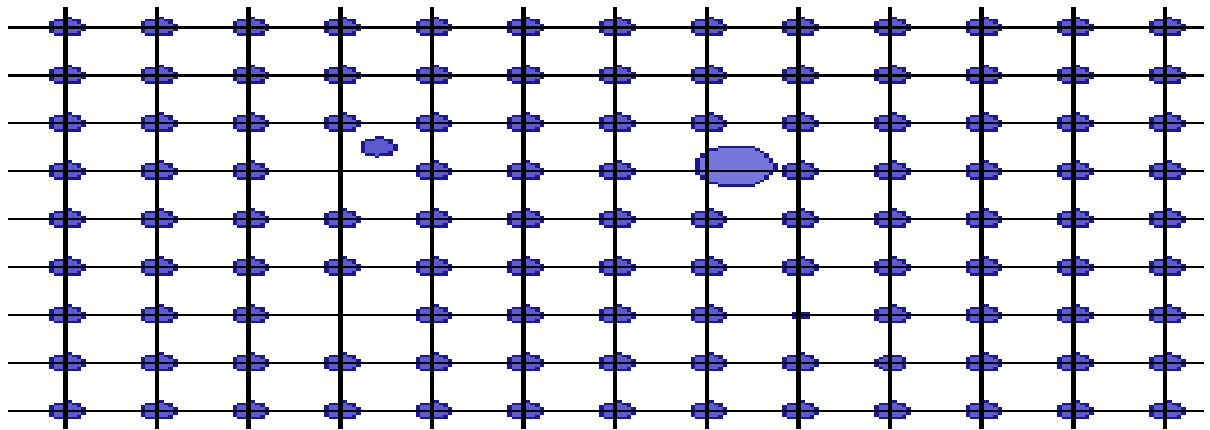


Fig. 1.3 Different ways of introducing point defects in the structure (designed in OptiFDTD software)

A monopole state is obtained that pushed up from the dielectric band by missing a rod and that pulls down a pair of doubly degenerate dipole modes from the air band by increasing the radius. A monopole has a single lobe whereas dipole has two lobes in the electric field. The point defects in PhCs are used to trap the light.

Another defect is the linear defects. It is used to guide the light from one position to another [3]. The main idea is to form a waveguide from the photonic crystal by changing a linear series of crystal as shown in Fig. 1.4. Light with the frequency in the photonic band gap that propagates in the waveguide is confined to the defect and can be directed along the defect [19]. The structure with the linear defect still has one direction in which discrete translational symmetry is conserved within the plane. The mechanism of guiding light is index guiding i.e. TIR (total internal reflection) in the conventional dielectric

waveguides but this mechanism confine the line only in the region of higher- ϵ . In this case the mechanism of guidance is photonic band gap which is independent of the material's properties that filled in the core. This property is important for the number of applications in which reduction of interaction between the dielectric material and light is required.

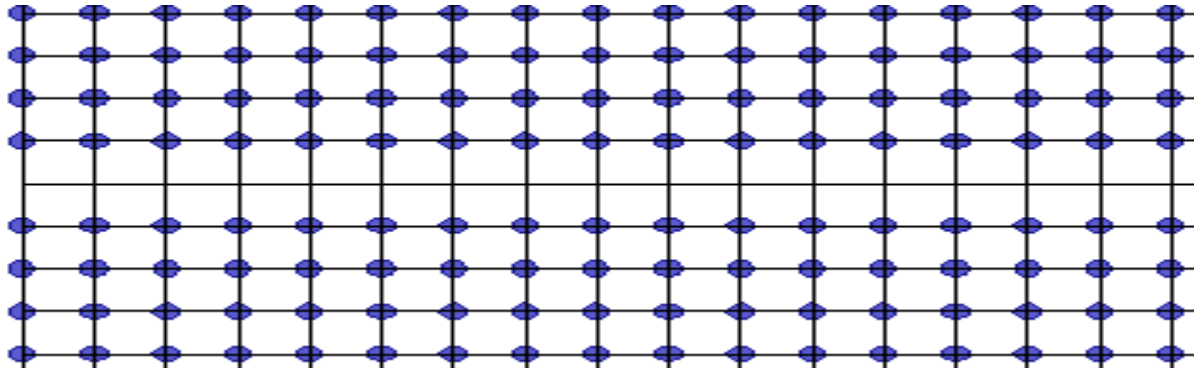


Fig. 1.4 Linear defect in crystal structure by removing the photonic crystal (designed in OptiFDTD)

The difference between the point defects and linear defects is not only that were discussed earlier. A mode is localized only when its frequency within PBG for a point defect. A mode is not only function of frequency but also its wave vector for the linear defect. There is a need to define the combination of wave vector and frequency for the guided mode.

There are number of ways in which linear defect can be introduced in the PhCs. So there is corresponding number of guided modes. The only condition is to maintain the discrete translational symmetry in one direction. This can be achieved by removing every n th rod or every rod along a single rod. This results in a single mode waveguide which has only one guided mode at the given frequency. Second way is by removing every rod along multiple rows of rods which results in a multi mode waveguide. This is undesirable for the application of information transmission because signal travels with the multiple velocities which results in modal dispersion.

1.6 ADVANTAGES OF PHOTONIC CRYSTALS

There are many advantages over the conventional optical devices. Its main advantage is to control optical properties and confinement of light by engineering the design of structure [3]. Some of advantages are shown below:

1. Photonic crystals reflect light of particular wavelength range which results in one mode of cavities unlike the metal cavities. The metal reflects all wavelength which results in infinite mode.
2. It can withstand with high electric fields
3. The size of photonic crystal devices are in the order of wavelength of light. Therefore, the devices are compact in size.
4. It processes the data at high speed as the travelling speed in structure is speed of light.
5. These devices are immune to short circuits as well as noise as the information carriers are photons unlike electrons in metallic wires.
6. Power consumption is low due to linear property of photonic crystal.
7. It confines the light highly in the structure due to large difference present for effective index.
8. It controls the spontaneous emission in the lattice.

1.7 DISADVANTAGES OF PHOTONIC CRYSTALS

On the other hand, photonic crystal offers few disadvantages. The main disadvantage is complexity to design on the 3-D scale [14]. There are several experiment occurred to yield efficient results. The other disadvantage of photonic crystal is the designing cost. It is more expensive than the conventional devices.

Due to various advantages, photonic crystal based devices are developed rapidly to meet the growing demand of high speed and capacity.

1.8 PROBLEM FORMULATION

In all the research works done so far, the optimized all optical logic gates is not designed for photonic integrated circuits. There are still many drawbacks such as low contrast ratio, higher losses, non-scalability and low fabrication error tolerances.

1. The contrast ratio of AOLGs should be improved to optimize the performance of optical logic gates.
2. The various reflections losses in the AOLG should be reduced for efficient cascading of two optical gates.
3. The fabrication error tolerance must be improved for the physical implementation of miniature sized circuits.

1.9 OBJECTIVE OF DISSERTATION

1. To improve extinction ratio or contrast ratio by optimizing the power of output port for logic 1 and logic 0. The contrast ratio is defined as the ratio of output power of logic high to logic low.
2. To design optical logic gates (NOR and NAND) by using compatible basic optical gates. The basic logic gates are NOT, OR, and AND.
3. To determine the range of fabrication error tolerance as well as to analyze the performance of optical NAND gate with different fabricated error tolerance for practical application.

1.10 ORGANIZATION OF DISSERTATION

Chapter 2 includes the literature survey regarding the topic of the dissertation. In order to begin with the dissertation, the first step is to study the papers related that have been previously published by researchers. Literature review helps to perform this work easily.

Chapter 3 presents the design of optical OR gate based on 2D photonic crystal of silicon (Si) rods in silica (SiO₂) substrate. The structure consists of quasi line waveguides and square cavity. The functionality of layout is numerically verified by the FDTD simulations.

Chapter 4 presents the design of all optical logic NOR gate based on two different cross waveguide structures. These two different cross structures are optical logic NOT and OR gate. These structures consist of 2-D photonic crystal of silicon rods in air. The optimized structures (NOT and OR gate) are combined without using any external devices such as amplifier, resonator etc. The contrast ratio of presented structure is high as compared to earlier reported work.

Chapter 5 presents the simultaneous implementation of NOT and AND gate to design optical NAND logic gate based on 2D square lattice photonic crystal. These structures are compact in size and have high contrast ratio compared to the earlier reported work. For practical applications, analyze the fabrication error tolerance of NAND gate. These structures are simple to fabricate; so it is favorable for use of future optical communication system and signal processor.

Chapter 6 includes the Conclusion, Recommendation and Future Prospect of the work.

CHAPTER 2

LITERATURE SURVEY

Optical logic gate based on photonic crystal has gained much interest in recent years as depicted in this chapter. Nowadays, many researchers started to pay more attention to design photonic crystal optical logic gates as it is one of important optical media to form optical processors, data handler and optical communication system.

As exhibited in this chapter, optical logic gates are generally divided into three categories based on the designing and fabrication such as resonators, interference waveguide, and self-collimation. Some authors designed the logic gate based on the resonators. These resonators can be linear or nonlinear. Some of the authors studied optical gate based on the interference waveguides. These structures are simple and easy to understand the principle. Some of the author investigated the self-collimation phenomenon for the designing of logic gate. They also studied their advantages and disadvantages of each method.

The literature survey of all optical logic gate based on Photonic Crystals by various researchers in past years is shown below:

Chunrong Tang et al. [20]

In this paper, authors designed various all optical logical gates on a 2-D Photonic crystal. These design of logic gate based on multimode interference (MMI). It has two input port structure. The phase shift of $3\pi/2$ is introduced by different length of input waveguides. By introducing the phase shift, these logic gates are directly used for BPSK signals. The various logic gates which realized are OR, NAND, XNOR and XOR. The structures are analyzed and simulated using FDTD and PWE method. Two types of logic gates (XNOR/XOR) are designed: without bend and with bend. The contrast ratio for logic OR and NAND gates is 13dB, for XNOR is 17dB and for XOR is 21dB in the C-Band (1530–1565nm). Since non linear material is not used so power consumption is less and the size of component is small. Hence the layout of logic gate has the potential to constitute PICs that will be utilized in all-optical signal processing, all-optical networks and photonic computing.

Junjie Bao et al. [21]

In this paper, author investigated a new approach for the design of all optical logic gates based on 2-D photonic crystals in square lattice of Si rods in silica. It consists of two photonic crystal ring resonators (PCRRs) and cross shaped waveguide without using any optical amplifiers and non linear materials. The layout of optical logic gate are simulated and analyzed by PWE and FDTD method. The numerically demonstration of structure shows that these structure acts as logic NOR and NAND gate. The size of logic gate is very small as $6.8\mu\text{m}$ only. The logic level high '1' and low '0' are defined. As this structure composed of linear material, it consumed low power as compared to the structure composed of non linear material. It is estimated that these new structures will make PCRRs have new applications for ultra-compact high density PIC and all-optical logic circuits.

Yi-Pin Yang et al. [22]

The authors demonstrated a layout of all optical logic AND gate based on 2-D photonic crystal in triangular lattice. It has two input port and one output port. It composed of PCRR waveguide sandwiched between two input waveguides. The electric field distribution of the device is analyzed by FDTD method. The optical logic AND gate can function at different wavelength in the communication window of $1.3\mu\text{m}$ and $1.55\mu\text{m}$ due to the total internal reflection (TIR) and the interference in resonator. The definition of logic level high '1' and low '0' is considered to be more than 95% and less than 35% of transmission, respectively. This design finds the applications in multi wavelength optical logic circuits.

Yulan Fu et al. [23]

In this paper, the author theoretically designed five types of all optical logic gates in a 2-D single photonic crystal lattice simultaneously. The five types of optical logic gates are NOT, OR, NAND, XOR and XNOR gates. The structure based on the interference effect of light beam. This ingenious design consists of waveguide. By controlling the optical path difference, the different gates are possible to realize. These gates do not required high power for their logic function. The maximum contrast ratio is 20dB. This offers an effective and a simple approach for the realization of integrated all-optical logic devices.

Raghda M.Younis et al. [24]

The authors presented compact and linear designs of two all optical AND and OR logic gates. These devices consist of Y-shape line defect and ring cavities which are sandwiched between two linear waveguides. The transmission characteristics of the designed optical logic gates are analysed and simulated by FDTD method. The contrast ratio of designed logic AND gate is not less than 6dB. The transmission power for logic OR gate is not less than 0.5. In addition to this, the suggested design of AND and OR logic gates can operate at the bit rates of 0.208 and 0.5 Tb/s, respectively. Moreover, the author calculated the fabrication tolerances of the designed devices found that the radii of rods of the ring cavities need to be controlled with no more than $\pm 3\%$ and $\pm 10\%$ fabrication errors for optical AND and OR gates, respectively. Therefore, these devices can be used for future PIC due to their small size and simplicity.

Ye Liu et al. [25]

In this paper, author demonstrated an ultra compact design of different all optical logic gates theoretically based on 2-D nonlinear photonic crystal slabs. The nonlinear material used for the structure is Ag-polymer film with the low refractive index. The order of nonlinearity is third. The PhC cavities with a high Q factor of about 2000 is designed on the 2D square lattice Ag-polymer slab. The resonant frequency of the line defect cavity depends upon the cavity length. The authors find that various all optical logic gates are possible to design by changing this factor. All optical OR, AND, NOR and NAND gates are demonstrated by combining two line defect cavities with appropriate condition of the power and resonant frequency in 2D photonic crystal slabs. The pump power as low as tens of MW/cm² has been sufficiently large to function the logic gates. The different logic devices are designed on the same photonic crystal structure. Due to the low cost of polymer films and the important nonlinear properties, this structure may be utilized for designing and realizing the components which can find practical applications in optical computing, all-optical integration and all-optical information processing.

P Andalib et al. [26]

The authors designed an ultra compact all optical logic NOR gate based on nonlinear effect of photonic crystals. It has two input ports and one output port. It consist of linear waveguides and PCRRs. The transmission characteristics of the design are analysed and

simulated by FDTD and PWE methods. Si rods with its appropriate properties are used as nonlinear material for the device. Si nano crystal rods are inserted in the ring resonators for nonlinear functioning of device. It localized the light beam because of resonance. The logic function of NOR gate is verified using simulation method. The high speed of logic gate can perform with a bit rate of 138.9 Gbit s⁻¹.

Preeti Rani et al. [27]

The author presented a layout of all optical logic AND gate based on 2D triangular lattice photonic crystal of air holes in Si substrate. It composed of Y-shaped linear waveguide without using any external devices such as optical amplifiers. The device is analyzed and simulated using PWE and FDTD method respectively. The method of finding the operating parameters has been explained. The optimized parameters are determined where high contrast ratio is obtained. The power consumption of optical logic gate is low as it is based on linear material. The contrast ratio of device is ratio of power of logic high to logic low. It is only 6dB for this structure. This layout finds its application in realizing devices and components for optical communication system and networks. This structure is favorable for large scale integration and can be used in on chip photonic integrated circuits.

Yuanliang Zhang et al. [28]

In this paper, the authors demonstrated a device for optical logic gates and switches. It is based on self collimated beams in a 2D photonic crystal. It consists of line defect induced 3dB splitter. The operating principle is shown by theoretical calculation as well as FDTD simulations. Its principle is based on the interference of reflected and transmitted self collimated beams. This is applicable for the frequency range from 0.188 to 0.199(a/λ). The contrast ratio within the frequency range is 17dB and maximum is 21dB. Due to simple in structure and clear operating principle, this structure can be used for future PICs.

Chih Jung Wu et al. [29]

The author presented a design of compact optical logic NOT gate (OLNG) based on the waveguides of PhC without using any optical amplifier and nonlinear materials. The numerically demonstration of the device through FDTD method shows that the layout acts as OLNG. It also presented a way to determine the operating parameters. For the

optimized parameters, the contrast ratio is 24.73dB or 297.07. The operating bit rate of presented OLNG is $2.155Tbit/s$, which is higher than electronic logic gates. The size of the optical logic NOT gate is $7a \times 7a$, where 'a' is the lattice constant since no optical amplifier is required. It can operate at the low power as non linear material is not used. It has wide operating bandwidth. This is favorable for developing multi wavelength parallel-processing optical logic systems and for large-scale optical integration. This simple optical chip equals to tens of thousands of conventional logic chips. It is used for future PIC as well as for developing all optical computers.

Yu-Chi Jiang et al. [30]

The authors realized the five different types of logic functions based on 2D PhC waveguide structures. The five different logic gates are NOT, OR, NOR, XNOR and $\bar{A} + B$. These gates are realized by choosing different reference and input ports. It based on the theory of interference of light beam. These gates are analyzed and simulated by the FDTD method. The logic level high and low is defined as the transmittance ratio larger than 0.5 and less than 0.1 at the output port, respectively. This investigation is carried out without considering phase difference between input beams. By considering the phase differences, the electric field distribution is altered. For this case high transmittance of 0.9 can be obtained. Therefore, the structure is favorable in optical device integration and also in the applications of waveguide in optical communications.

A.G. Coelho et al. [31]

In this paper, the author shown the implementation of non linear directional coupler (NLDC) based in triple core PCF logic gates. It is operating with the two ultra short soliton pulses of 100fs. These pulses are modulated through PAM in logic levels 1 and 0. The logic gates (AND and OR) are obtained using the same PAM-ASK for the input signals. The pulse propagation is modelled by an extended nonlinear Schrodinger equation including the terms associated with the anomalous group-velocity dispersion (GVD) and the third-order dispersion , as well as the nonlinear effects of self-phase modulation (SPM), cross-phase modulation (XPM), self-steepening, and intrapulse Raman scattering (IRS) in a lossless configuration. The logic gates can be realized by considering the phase shift in the input signals. This study opens the area of research for all optical logic gates based on DCs based in triple core PCFs.

Bin Liu et al. [32]

The author studies the realization of nonlinear all optical logic gates based on 1D PhCs with dual defects. To avoid the adverse effect of unstable progress on the layout, the broadband defect mode (BDM) is used. The transmission spectrum and distribution of field is analyzed by transfer matrix method. After analyzing, the method of realizing BDM near the central frequency, strong localization and symmetrically distributed field is developed. BDM with proper parameter can be used to reduce the influence between field distribution and nonlinear refractive index. The designed logic gates NOT, AND and XOR are better than the traditional logic gate based on 1D PC with one defect. It is due to the low threshold, stability control and high contrast. Due to these advantages, design of AOLG in this work is better while applying in all optical signal processing.

J.R.R. Sousa et al. [33]

The author investigated all optical logic gates (AOLG) based in a Michelson Interferometer (MI) of photonic crystal fibers (PCFs). An ultra short pulse of approximately 100fs is transmitted through the structure to determine the potential of the device. The author also studies various parameters to characterize the device's performance such as extinction ratio, transmission, compression factor and cross talk which are function of the nonlinear dephasing added to one of the Bragg gratings of the MI. The high order dispersion effects such as IRS, third order dispersion and self steepening are influenced the propagation of pulse. The three different ways to excite the power (above, equal and below the switching power) are analyzed. So, author able to identify several ranges for the realization of gates (NOT, OR and XOR). Therefore, a Michelson Interferometer device based in PCF seems to be a potential candidate for the development of ultrafast AOLG. The alternative configuration can be explored for more set of logic functions.

Majid Ghadrddan et al. [34]

In this paper, the author designed all optical AND and XOR logic gates based on nonlinear PCRR for implementing simultaneously. PhC consists of 2D square lattice of dielectric rods in air. The structure is analysed and simulated by FDTD and PWE method. The concurrent implemented structure (i.e. half adder) is operating at the wavelength of $1.55\mu\text{m}$ and its lattice constant (a) is $0.5943\mu\text{m}$. The contrast ratio for AND and XOR

gate is 12.78dB and 5.67dB respectively. The operating power of structure is $277\text{mW}/\mu\text{m}^2$ and switching time is low of 0.85 ps. The operating speed and dimension of structure is 746Gb/s and $12 \times 14 \mu\text{m}$ respectively. Due to simple shape and clear operating principle, the designed structure has a potential to be used in PIC.

Jibo Bai et al. [35]

The authors designed all optical NOT and NOR logic gates based on 2D square lattice PhC of silicon. This structure composed of ultra-compact PCRR which is formed by line defect along the ΓM direction instead of the conventional ΓX direction. The behavior of logic gate is analyzed and simulated by interference of beam theoretically and FDTD method simultaneously. Both the input and probe signals are operated at the same wavelength. This structure required non linear material with effective radius of $2.2\mu\text{m}$. This device is suitable for on chip PIC circuits.

Susan Christina Xavier et al. [36]

In this paper, the authors presented an approach to design all optical logic gate based on 2D PhC. This approach based on the self collimation effect in which beam split by line defect and interferes with the other self collimated beams. The interference can be destructive or constructive depends on the phase difference. The structure are analyzed by FDTD method to verify the functioning of design as logic gate AND, NAND, NOR and XNOR. The dimension of structure is $10 \mu\text{m} \times 10 \mu\text{m}$ only which results in high speed of operation. The contrast ratio of logic high to low is 6dB.

Junzhen Jiang et al. [37]

The authors devised a new approach for the design of AOLG based on 2D single hexagonal lattice PCRR of Si rods in air. The layout of logic gates is optimized by the theory of single interference and perturbation. It is numerically analyzed by FDTD method. Numerical results show the function of logic gates NOT and NOR with the single PCRR. The logic level high and low are defined as greater than 86% and less than 8%, respectively. It is better than earlier reported work.

Hamed Alipour-Banaei et al. [38]

The author demonstrated the design of optical NOR and NAND gates based on combination of non linear effect with PCRR. Its behavior of structure is controlled by

power intensity. The minimum power required for operation is $2\text{KW}/\mu\text{m}^2$. The author used two PCRR so that resonant wavelength is $1.55\mu\text{m}$. Generally it has two input ports and one bias. For analyses and simulation PWE and FDTD method is used.

CHAPTER 3

DESIGN OF OPTICAL LOGIC OR GATE BASED ON 2D PC WAVEGUIDE STRUCTURE

A new design of all optical logic gates based on 2D photonic crystal of silicon rods in silica is presented. This structure efficiently acts as a logic switch and behaves as an OR gate. The continuous input applied to this structure is partially reflected and the rest of it is transmitted through circular cavity formed by point and line defects. The output is thus obtained. The structure has been simulated and analyzed by finite difference time domain (FDTD) and Plane Wave Expansion (PWE). The size of logic gate is only about $20\mu\text{m} \times 20\mu\text{m}$ and it operates at fundamental third optical window. Therefore, it can be used for photonic integrated circuits. The obtained contrast ratio is 10dB and this design can be used for other logic functions also.

3.1 INTRODUCTION

All optical logical gates play important role in optical communication system since they are the basic elements for optical signal processing. It is a solution of all the limitations in electronic communication system. It meets the growing demands of terahertz signal processor that is the main bottleneck of electronics [39, 40]. There are a number of methods to design all optical gates such as semiconductor optical amplifier (SOA) [41], optical waveguide interferometer [42], fibre grating [43, 44] but all have some drawbacks. They cannot be used for physical photonic integrated circuit due to large size and they have high power consumption.

The advantages of photonic crystal based logic gate are high speed, improved throughput, low power consumption and compactness i.e. order of wavelength. It can be used for photonic integrated circuit. Photonic crystal is periodically changed in dielectric constant that controls the flow of photons. There is a photonic band gap (PBG) which represents the range of wavelength that cannot propagate through the photonic crystal [45, 46]. This can be calculated using PWE method [47]. The transmission characteristics of the device are analyzed by using a two-dimensional FDTD numerical method [48]. Due to ease of fabrication and simple design of logic gates, the photonic integrated circuits (PIC) are currently being investigated for various logic gates.

Raghda M. Younis et al. [24] designed all optical logic OR gates. The structure is Y-shaped line defect coupler and ring cavities. The advantage of this structure is that it can operate at terabits. It gives the transmittance power greater than 0.5. Chunrong Tang et al. [20], designed logic gate in two dimensional photonic crystal based on multimode interference. Avoiding external phase shifter is the main advantage of this structure. Therefore, it can be used for BPSK signals. The major flaws are that the contrast ratio is not sufficiently high and the phase shifted input is also not accurate.

It is observed that the transmitted power for logic low can be reduced further as well as contrast ratio can be increased for improving the performance of logic devices. This chapter investigated a new approach based on square cavity and quasi line waveguide for the design of optical logic OR gate in 2D square lattice. Line defect is formed by removing dielectric rods or filling the holes which sometimes are treated as linear waveguide. Point defect is formed by increasing the size of hole or rod, removing the rod or filling the hole [49, 50]. The point defect acts as cavity which has high Q factor. It is the ratio of central frequency to bandwidth and also defines the shape of peak of resonant frequency. Contrast ratio of logic gate is a factor that determines the suitability of the design. In this design the contrast ratio is 10dB which is more than earlier reported work.

This chapter has four sections in which introduction of photonic crystal and its properties have been discussed briefly in section 3.1. Design of logic OR gate has been described in section 3.2. In section 3.3, simulation and results have been discussed and the conclusion has been drawn from these simulations in section 3.4.

3.2 SIMULATION SETUP

A design of optical logic OR gate with the wafer size of $20\mu\text{m} \times 20\mu\text{m}$ in 2D square lattice photonic crystal has been explored. It consists of two linear waveguides and one circular cavity at the intersectional point. The linear waveguides are formed by the removal of dielectric rods. The dielectric rods of refractive index 3.4 are placed in SiO_2 wafer of refractive index 1.34. In this design the number of dielectric rods in X direction is 15 and in Z direction is 18. The distance between two dielectric rods is known as lattice constant and it is represented by “a”. The circular cavity is formed at the intersection of quasi waveguides with four elliptical rods of $0.2\mu\text{m} \times 0.5\mu\text{m}$ and one central rod of radius $0.7\mu\text{m}$. Fig. 3.1 shows the layout of logic OR gate. There are two input planes which are represented by A and B (one is vertical and another is horizontal) and one output plane

which is represented by C. The observation point and observation plane are used. The cavities in middle direct output towards the port C and no signal comes out at the port D. Various structural parameter for the design of optical OR gate is given in Table 3.1

Parameters	Materials/Values
Wafer material	SiO ₂
Dielectric Rods	Si
Size of Wafer	20μm x 20μm
Refractive index of rods	3.4
Radius of rods	0.2a
Lattice constant 'a'	1μm

Table 3.1 Structural Parameters of the Designed OR Gate

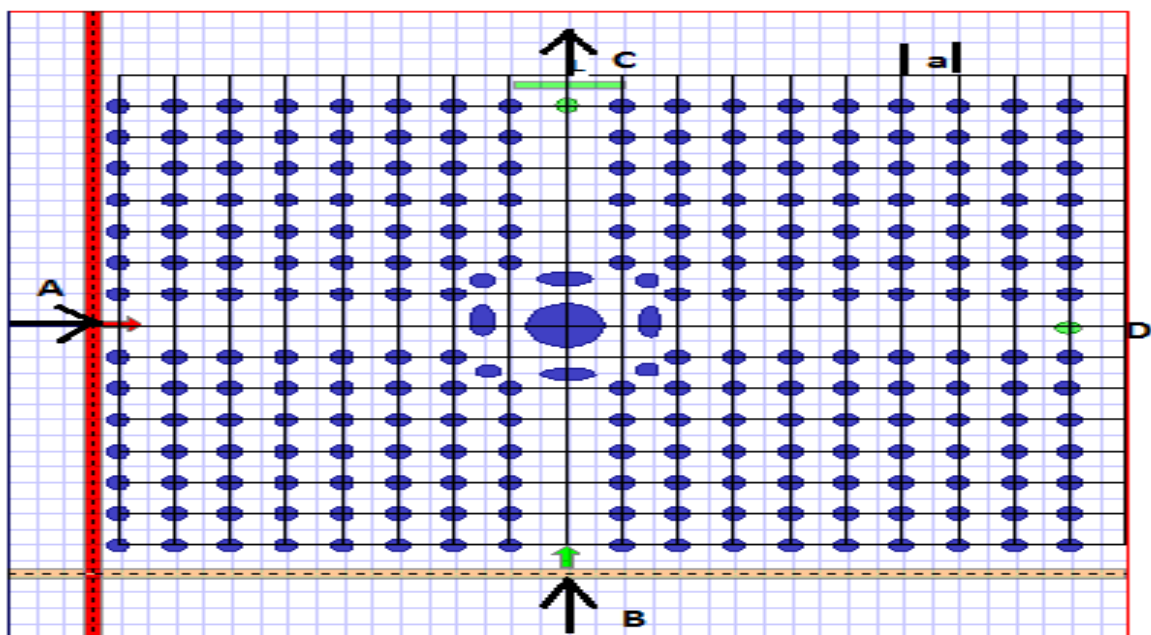


Fig. 3.1 Layout of all optical logic OR gate in OptiFDTD with the input port A and B and output port is C. The distance between two Si rod is 'a'.

Logic OR gate is usually at logic level "0". It changes its state when any one or both the inputs are at logic level "1". It returns to state "0" only when both the inputs are at logic level "0" or low. This logic device is implemented with the help of photonic crystal in 2D square lattice. Fig. 3.2 shows the block diagram of logic OR gate.

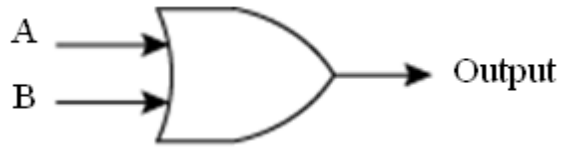


Fig. 3.2 Symbol of logic OR gate

3.3 RESULTS AND DISCUSSIONS

The band diagram shown in Fig. 3.3 gives the forbidden band gap. This band gap is analogous to electronic band gap between conduction and valence band. The range of band gap is $0.316417 \leq (1/\lambda) \leq 0.358938$ and band gap width is 0.0425209. The calculated band gap is for Transverse Magnetic Mode (TM) whose magnetic field is parallel to rod axis. The light in this range of frequency does not propagate through this structure. The frequency of the photonic crystal structure is $\omega/2\pi c=1/\lambda$, where ‘ ω ’ is the angular frequency, ‘ c ’ is the velocity of light in free space and ‘ λ ’ is the free space wavelength.

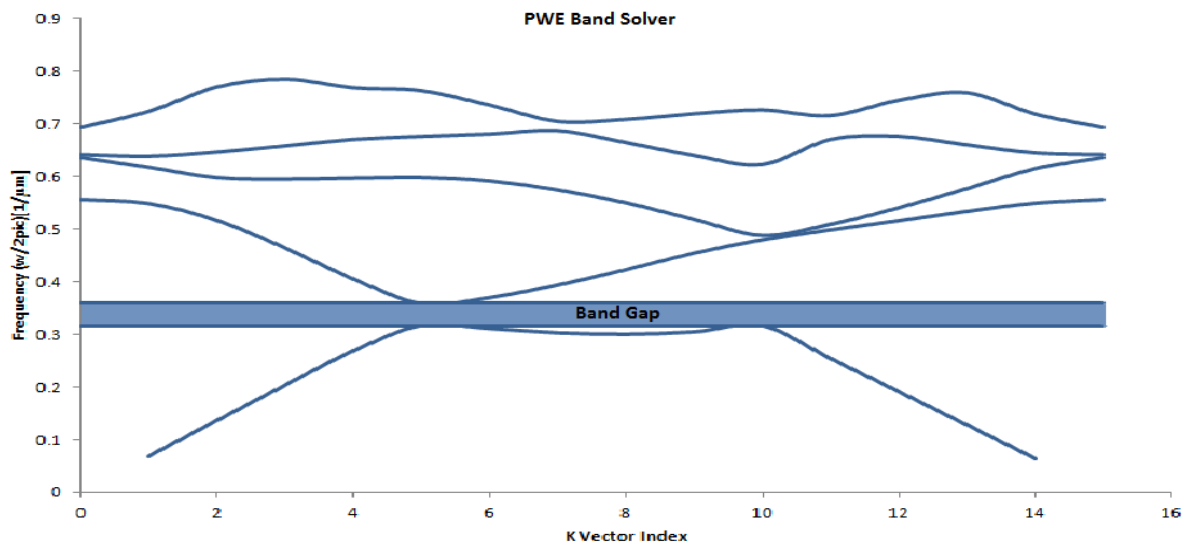


Fig. 3.3 Band Diagram of optical logic OR gate with forbidden band gap of 0.0425209 before introducing point defect and line defect

The band diagram in Fig. 3.4 shows that there is no band gap for propagation in the Y direction due to the introduction of the defects in XZ plane. This shows that there is no forbidden frequency range. Thus, all wavelengths pass through the structure. The defects reduce band gap and also sometimes eliminate it [49, 50]. There is a line defect

introduced in this structure by removing dielectric rods. This line defect acts as waveguide which guides the flow of light.

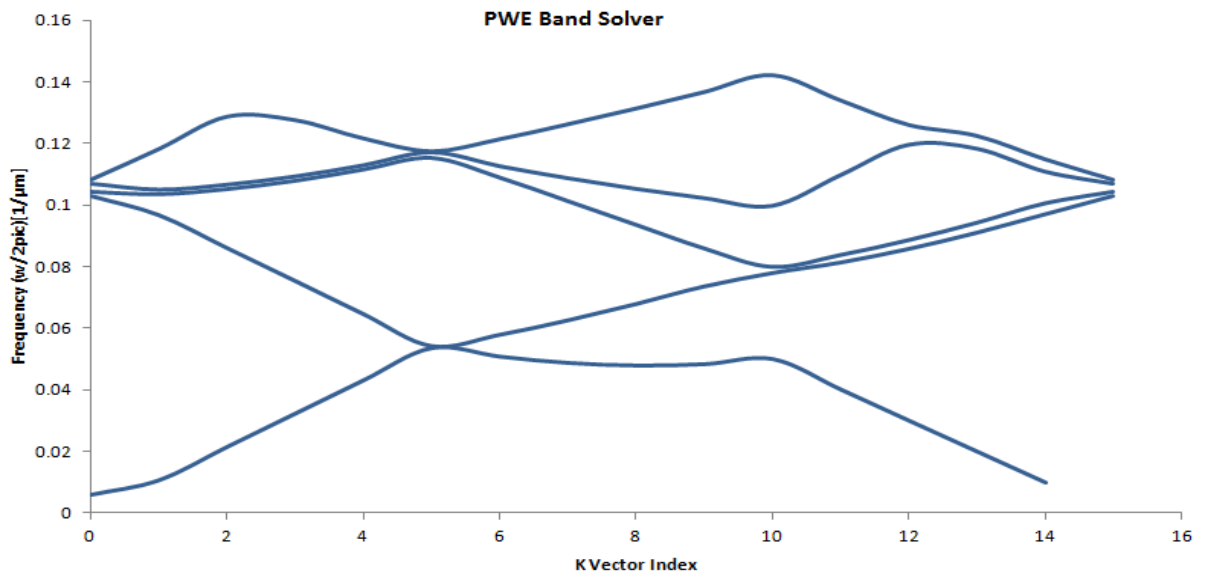


Fig. 3.4 Band Diagram of optical logic OR gate with no band gap after introducing point defect and line defect

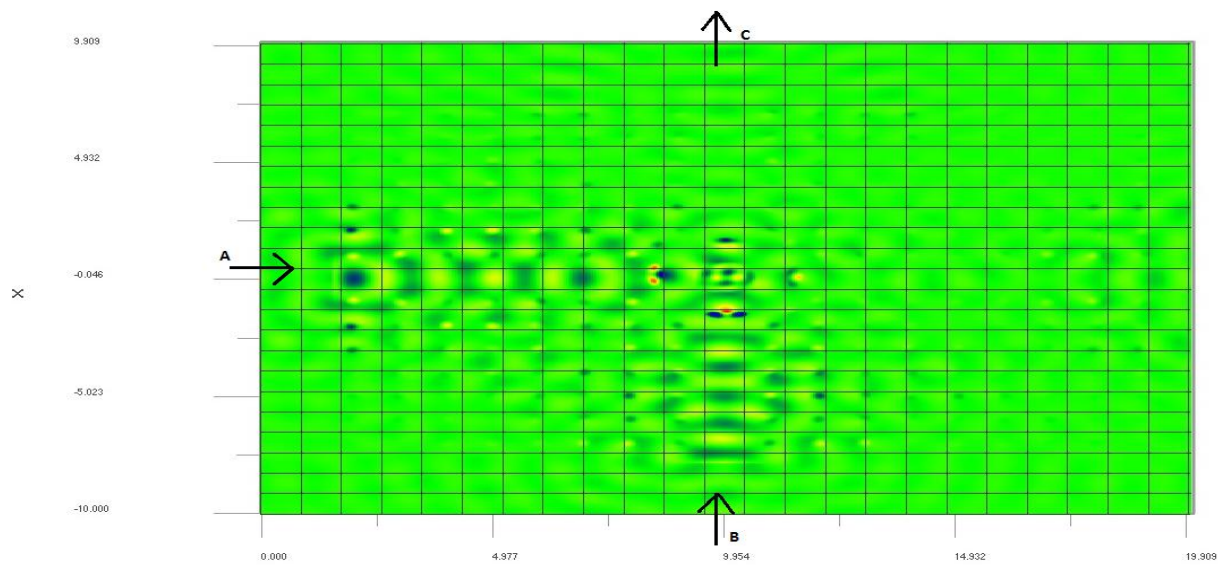
A Two Dimensional 32 bit simulation is carried out using finite difference time domain method with transverse magnetic (TM) mode to obtain the logic function of logic OR gate. The different possible combination of a continuous Gaussian input plane is used for logic gates. The two inputs are directed from vertical input plane at port A and horizontal input plane at port B with wavelength of $1.55\mu\text{m}$. From the simulation results, the output at port C follows the logic OR gate. The table with different combination of input and output is shown below.

Input Port A	Input Port B	Output Port C	Output Power from observation point (W/m)
0	0	0	0.054703
0	1	1	0.376082
1	0	1	0.275885
1	1	1	0.547027

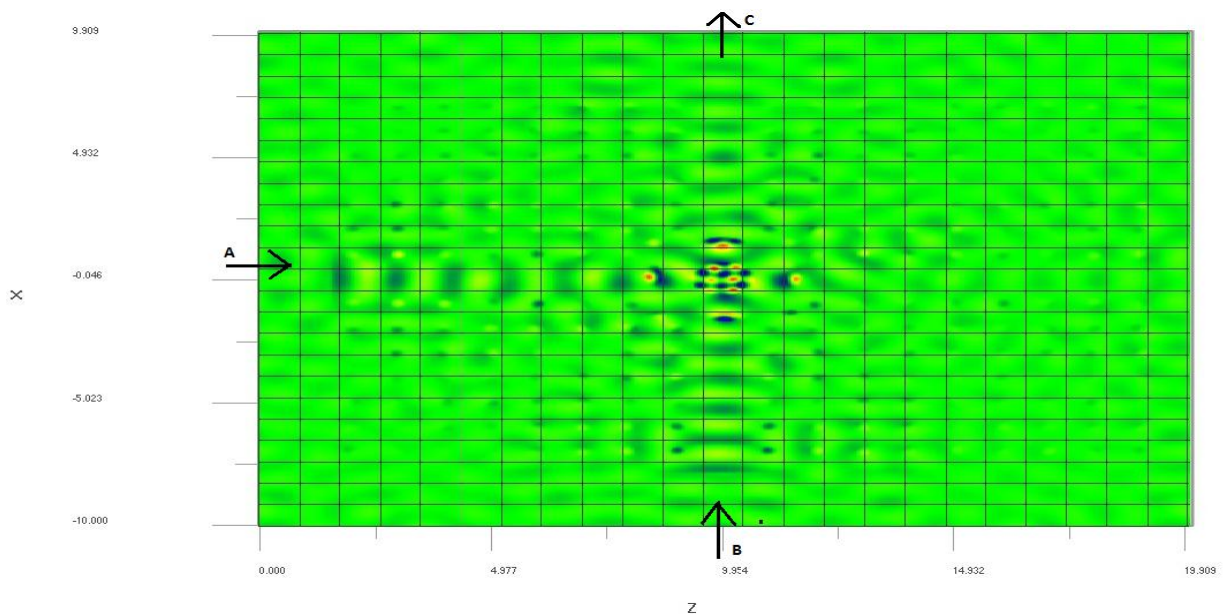
Table 3.2 Truth table of logic OR gate

As shown in Table 3.2, when logic gate is ON the power of output is more than 0.25. When it is OFF, the output transmission power is less than 0.1. The transmission power of ON state is 10 times the transmission power of OFF state. This shows the possibility of implementation of logic switch on integrated circuits.

The distribution of electric field through photonic crystal have been analysed by FDTD. This describes the transmission path of light during different input conditions. When both the inputs are low, then the output is low otherwise the output is high. This is shown in Fig. 3.5.



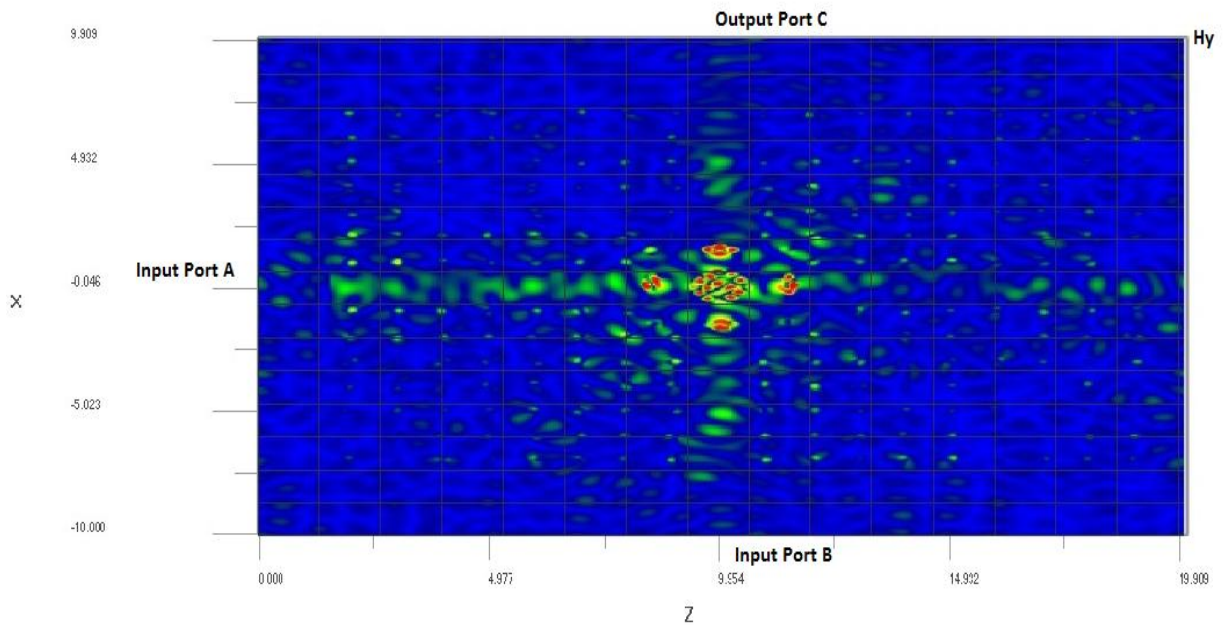
a) When input port $A=0$ and $B=0$ then output port $C=0$



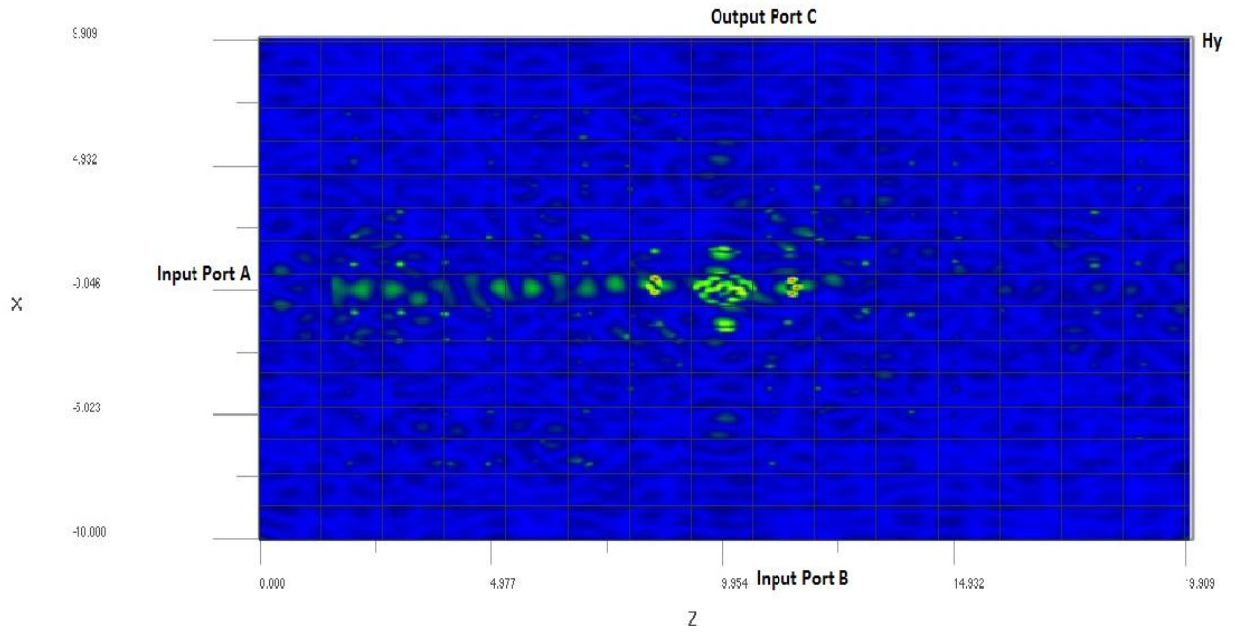
b) When input port $A=1$ and $B=1$ then output port $C=1$

Fig. 3.5 The distribution of electric field with different input conditions. **a)** When both the inputs are low (small amplitude is given) then the output is also low. **b)** When both the input is high then output is also high.

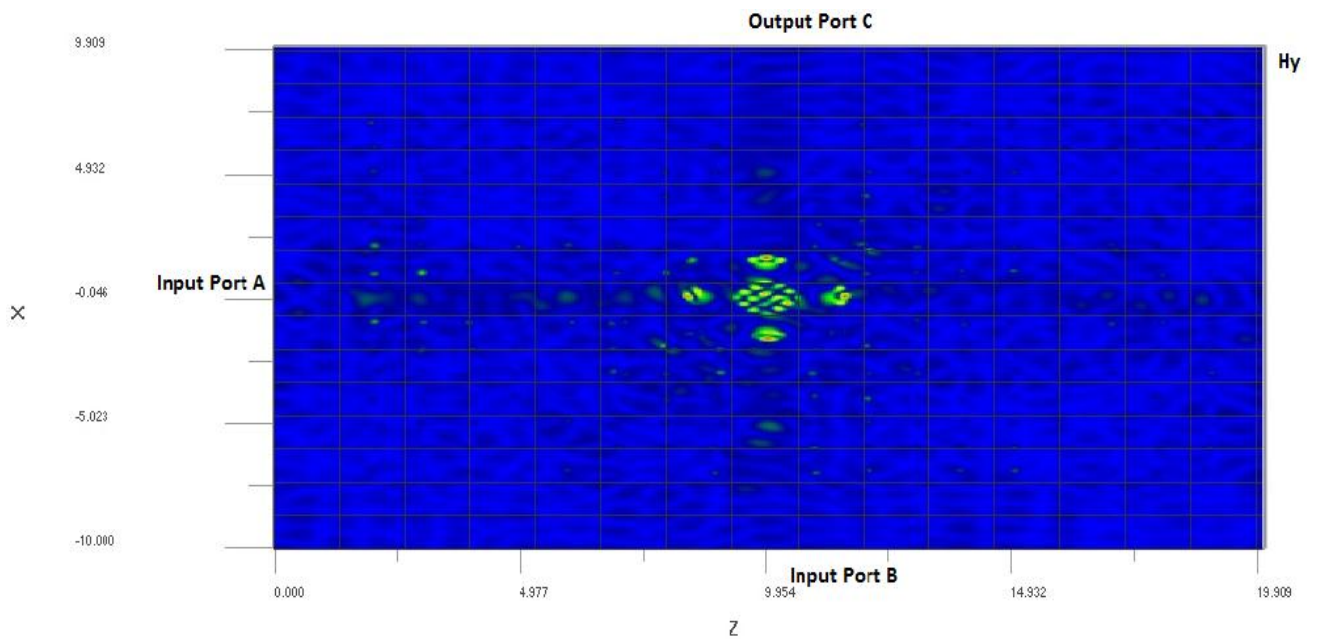
When there is any defect in the structure then it can localize the light mode. In Fig. 3.6 (a), most of light is confined at the centre. Some part of light is has moved out from central trap. It implies that there is logic 0 at the output port. Central part acts as trapper or cavity to confine light. Similarly when one of inputs is high then some part of light gets confined at the centre as shown in Fig. 3.6 (b) and 3.6 (c). So it will show logic high as most of the light is present at the output port.



a) Both input ports A and B are logic low



b) Input Port A is high and B is low



c) Both input Ports A and B are high

Fig. 3.6 Different level of confinement of light at the central part in different conditions. **a)** Both inputs are low so most of the light is confined at the centre. **b)** One of inputs is high so some portion of light is confined at the centre. It will show logic high at output port C. **c)** both the inputs are high so most of light has moved out of cavity.

The graph of Fig.3.7 shows that for low value of power, the bandwidth is large and as the power input is increased, the bandwidth is narrowed down. It also shows the relative power (in W/m) changes with wavelength for all possible combinations. Contrast Ratio (C.R.) is ratio of transmission power at high to low conditions. Power for ON (P-ON) =0.54703 and Power for OFF (P-OFF) = 0.054703 is given in table. The formula for contrast ratio is given below [20]

$$C.R. = 10 \log \left(\frac{\text{Power for ON state}}{\text{Power for OFF state}} \right) \quad (3.1)$$

$$= 10 \log \left(\frac{0.54703}{0.054703} \right)$$

$$= 10\text{dB}$$

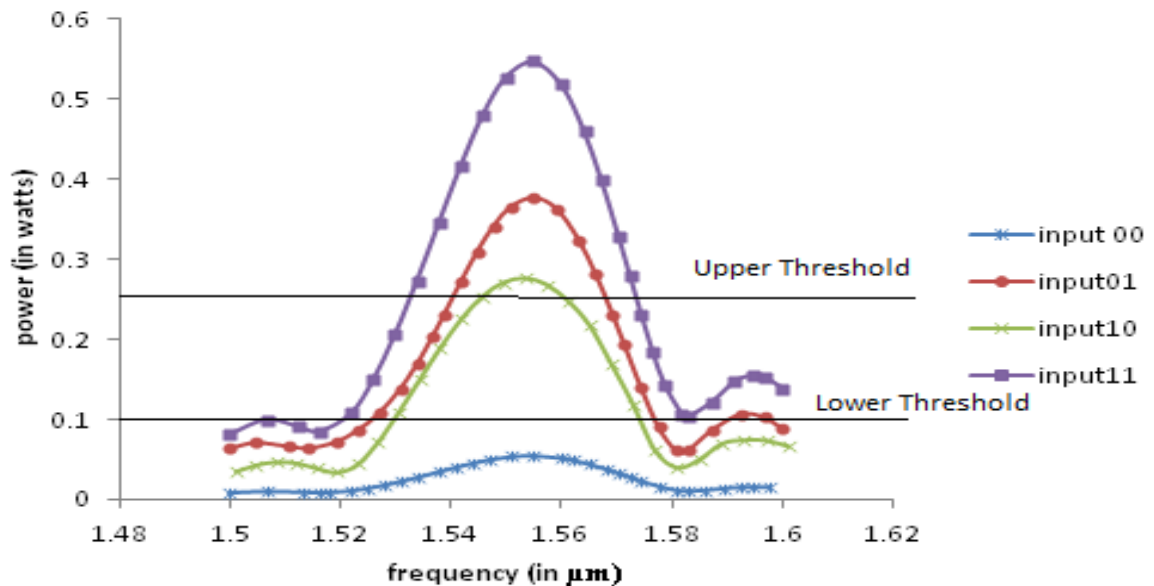


Fig. 3.7 Graph of power (W/m) versus frequency for different input conditions. There are two levels. Value below threshold is logic low and value above upper threshold is logic high.

There are two threshold levels to identify the logic state. The lower threshold implies that any power below this level acts as logic low or 0. Similarly, the power values greater than upper threshold act as logic high or “1”. No state is defined between upper threshold and lower threshold.

3.4 CONCLUSION

We presented a new structure of all optical OR logic gates based on 2D photonic crystal using silicon dielectric rods in silica. This structure efficiently acts as logic switch and behaves as logic OR gate. The structure has been simulated and analyzed by FDTD and PWE. The continuous input applied to this structure is partially reflected and partially transmitted through circular cavity. The circular cavity is formed by point and line defect. Thus, the output is obtained. The main advantages of this structure are the size of logic gate is small (about $20\mu\text{m} \times 20\mu\text{m}$) and it operates at $1.55\mu\text{m}$ which is fundamental third optical window. Therefore, it can be used for photonic integrated circuits. Also, the obtained contrast ratio is 10dB. This structure shows the possibility of designing other logic functions. It can be used for various logic circuits, flip flop, decoders and many other photonic integrated circuits.

ALL OPTICAL NOR GATE BASED ON CROSS STRUCTURES IN 2D PHOTONIC CRYSTALS USING BASIC GATES

An optical NOR gate is presented based on two different cross waveguide structures in 2D photonic crystal. The two different cross waveguide structures are logic NOT and OR gate. The layout of logic NOT and OR gate are simulated and analysed individually using Finite Difference Time Domain method. The structure is optimized by iterative process. The contrast ratio for logic NOT gate is 11.605dB and for OR gate is 22.113dB. The size of NOT and OR structures are $10\mu\text{m} \times 10\mu\text{m}$. With the optimized parameters, both the gates are combined without using any external device to design the NOR gate. The operation of NOR gate is numerically demonstrated using FDTD simulation. The contrast ratio is 15.97dB for NOR gate. Since non linear material is not used, the power consumption is less. This NOR structure has an operating bandwidth of 40nm. Thus, it is favorable for use in optical communication system and optical signal processor.

4.1 INTRODUCTION

In modern communication systems, most of the data is transmitted in the form of digital voice or pictures. Therefore, the demand of high capacity and high processing speed has increased. Electronic devices are still used to fulfil these growing demands. But these devices have limitation of processing speed which is the main bottleneck of electronics [51-53]. Therefore, there is a need of all optical processor and data handler [54]. The optical devices have an advantage of miniature sizes and high speed. All optical logic gates or optical switches are basic elements in optical information processor [21]. There are different ways to design all optical logic gates. They are based on nonlinear effects in waveguides [55], in semiconductors [56] and in optical fibres [57]. But all suffer from certain limitations such as low speed, big size and difficulty to integrate on chip.

Photonic crystals (PhCs) are the best candidates for realization of all optical logic functions. The logic gate based on PhC has unique properties such as compactness, low power consumption, high speed and high confinement [4]. Photonic crystal is an optical material in which the dielectric constant changes periodically. The light propagates inside the structure and reflects at each interface of the dielectric material. It causes interference

due to which some wavelengths do not propagate through the photonic crystal. These forbidden wavelengths form the band gap which is similar to electronic band gap [45, 46]. This photonic band gap controls the flow of photon or light. It can be calculated by Plane wave expansion (PWE) method [47]. Various designs of all optical photonic crystal logic gates based on resonator structure [58], self collimation phenomena [28] and interference waveguide [59] have been presented. But they are based on nonlinear material and require a certain scale of volume which is a limitation for photonic integrated circuits.

Chih Jung Wu et al. [29] designed a compact and low power logic NOT gate based on the waveguide interference without using optical amplifier. The structure have 24.73dB contrast ratio and its bit rate is 2.155 Tbit/s. Bai et al. [35] designed an optical NOT and NOR gate based on the ring resonator and Y branch waveguide without using nonlinear material. The contrast ratio of this structure is 4.47dB. Chunrong Tang et al. [20] designed the logic gate in two dimensional photonic crystal based on the multimode interference without using external phase shifter. Therefore, it can be used for BPSK signals.

In all the above structures, the contrast ratio is not sufficiently high for their efficient operation. It is observed that the main flaw of the structure discussed [29] is high losses as some unwanted light is reflected in the input port. The structure based on the ring resonator [35] is sensitive to phase difference between input and reference signal. Due to which the contrast ratio is low. Thus, it results in the poor performance of this logic gate.

This chapter has investigated a new approach for the design of optical logic NOR gate by combining NOT gate and OR gate. This approach has resulted in low reflection losses at the input ports and therefore high contrast ratio is achieved. The designed structures consist of cross waveguides. These structures are optimized for high transmission efficiency by introducing the point cavities of appropriate radius at the cross intersection point. The contrast ratio of logic gate is a factor that determines the suitability of the design. It is ratio of power of logic “1” to logic “0”. In this design the contrast ratio is 11.605dB for NOT gate and 22.113dB for OR gate which is higher than the earlier reported works.

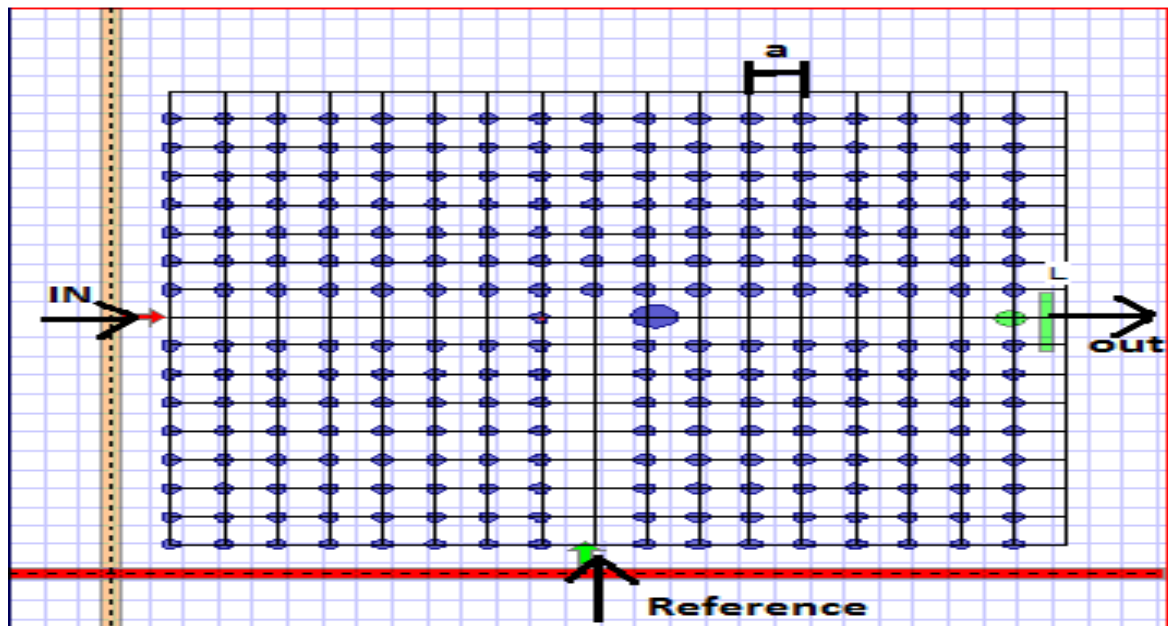
This chapter is organized as follows. The Section 4.2 presents the model and operating principle of the optical NOT and OR gate then the model of NOR gate. In Section 4.3, the simulation method is discussed. In Section 4.4, the basic optical logic gate NOT and OR

gate are investigated and optimized then the model of NOR gate is investigated. Section 4.5 gives a brief conclusion.

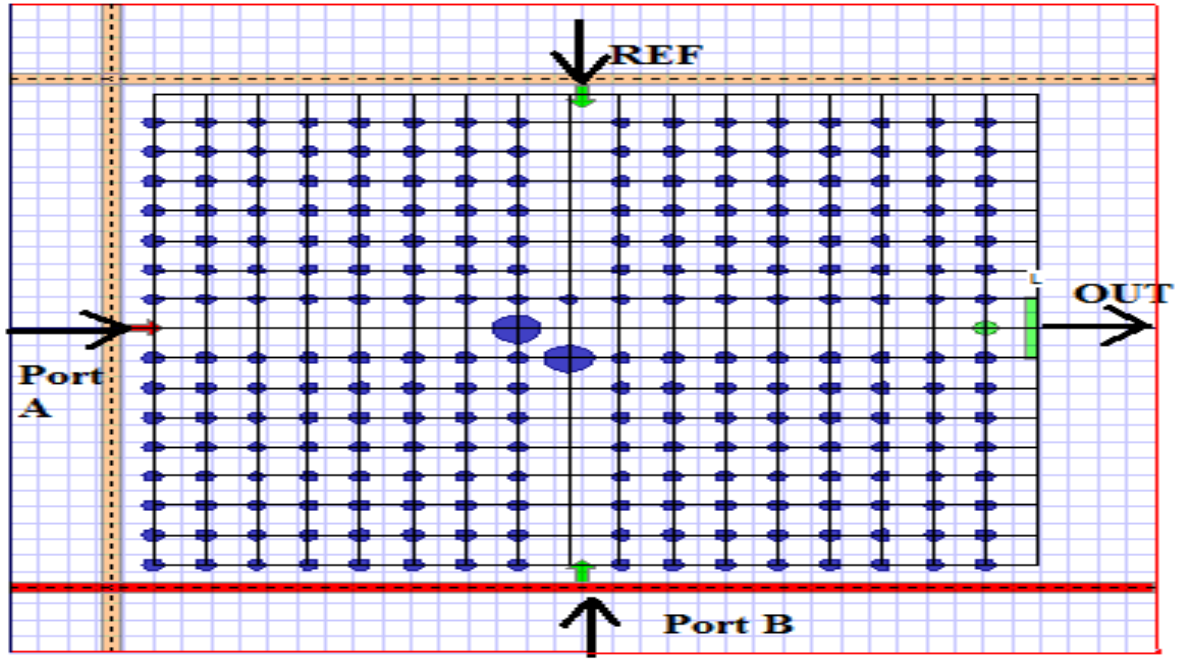
4.2 SIMULATION SETUP

4.2.1 Layout of Basic optical logic “NOT gate” and “OR gate”

The design of optical logic NOT and OR gates on 2D square lattice in XZ plane individually is presented. The wafer size of both the gates is $10\mu\text{m} \times 10\mu\text{m}$. The structure of NOT gate consists of two linear interference waveguides in T shape. But the structure of OR gate consists of two linear waveguides cross at the centre. The linear waveguides are formed by the removal of series of dielectric rods which is known as line defect. The Silicon rods (16×17) of refractive index 3.4 and radius (r) of 0.18 times lattice constant (represented as ‘ a ’) are placed in the air. The distance between two dielectric rods is known as lattice constant. The two reflecting rods are placed around the centre to form horizontal cavity in the NOT gate. In the layout of OR gate, the three reflecting rods are introduced. The radius of reflecting rods is chosen properly so that transmitted power is high at the output port.



(a)



(b)

Fig. 4.1 Schematic Layout of all optical logic gates on 2D square lattice in XZ plane. The arrow pointing inward represent the input signal and reference signal and outward represent the output signal.(a) Logic NOT gate consists of two linear waveguide in T shape and point defect. (b) Logic OR gate consists of two line defect and three point defect.

The layout of logic NOT gate is shown in Fig. 4.1(a). A vertical input plane is used for injecting the input signal which is represented by IN. Another signal is the reference signal which is launched from the horizontal input plane at the port marked as reference in Fig. 4.1(a). Both the signals have same phase and frequency. The observation point and line in the horizontal waveguide at the output port are used as a power detector. The point to be noted is that the NOT gate is a bidirectional gate. The input and output ports of NOT gate can be interchanged. The layout of all optical logic OR gate is demonstrated in Fig. 4.1(b). There are two input ports (marked as ports A and B in Fig. 4.1(b)) for input signals and one port for reference signal (marked as REF in Fig. 4.1(b)). The reference signal is used when no input signal is available at the input port. The silicon rods with different size are introduced as reflecting rods or point defect in the layout. The radius of defected rods (r_i) is large so that more power is transmitted toward the output. The radius of reflected rods (r_r) is optimized by computing the contrast ratio in the section below.

4.2.2 Layout of optical NOR gate using basic logic gates

It is known that the function of logic NOR gate is logical complement of an OR gate. NOR gate is designed by combining OR gate and NOT gate without using any external device like amplifier, coupler etc. It is also designed on 2D square lattice photonic crystal with wafer size of $13\mu\text{m} \times 10\mu\text{m}$. The rest of parameters such as dielectric constant, radius of dielectric rods, position and radii of reflected rods are same as that in the layout of Fig. 4.1.

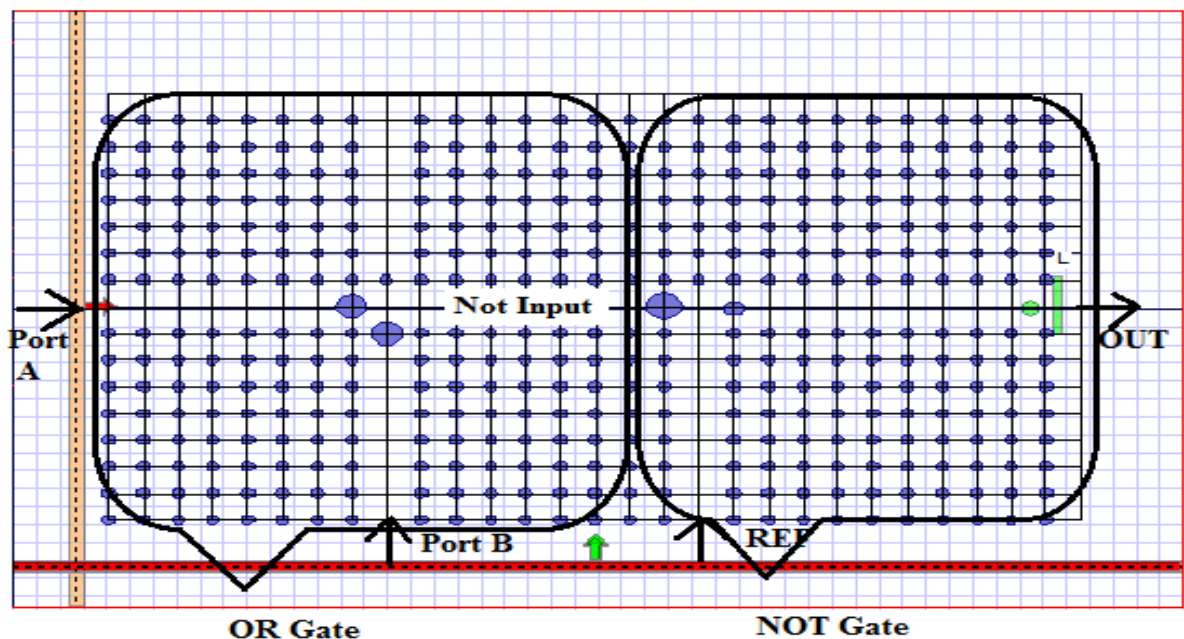


Fig. 4.2 Layout of optical NOR gate using basic optical logic gates on 2D square lattice in XZ plane. It consists of two input port, one reference signal port and one output port.

All optical NOR gate consists of three interference waveguides as shown in Fig. 4.2. One waveguide is common for both the combined optical logic gates. The output of OR gate acts as the input of NOT gate. The NOT gate complements the output of logic OR gate. The output port of NOR gate is same as the output port of NOT gate.

4.3 SIMULATION METHOD

The plane wave expansion method (PWE) is used to find the photonic bandgap. This photonic band gap is used to determine the operating wavelength or frequency. The normalized frequency of the photonic crystal structure is $\omega/2\pi c=1/\lambda$, where ‘ ω ’ is the

angular frequency, ‘c’ is the velocity of light in free space and ‘λ’ is the free space wavelength.

FDTD (Finite difference time domain) method is used to simulate and optimize the function of logic gate shown in Fig. 4.1. and 4.2. by calculating the transmittance power at the output port. In the simulation, structure is surrounded by perfectly matched layer from all the sides. It is used to avoid reflection from all the sides and absorb waves.

The time and space steps size are fundamental constraints in FDTD method. Its size relate to accuracy, stability and dispersion of the FDTD method. The space step size for accuracy should be chosen according to the following rule [60]

$$\Delta x < \frac{\lambda}{10} \quad (4.1)$$

$$\Delta z < \frac{\lambda}{10} \quad (4.2)$$

where Δx and Δz are the space step along X and Z direction. The axis of rod is along y direction. For time step size it should satisfy the following condition [61]

$$\Delta t < \frac{1}{v\sqrt{\Delta x^{-2} + \Delta z^{-2}}} \quad (4.3)$$

where Δt is the time step size and v is the speed of light in the wafer’s medium. The material is assumed to be non magnetic for the simulation. All the simulations are carried out in the TE modes.

4.4 RESULTS AND DISCUSSIONS

Since one needs NOT and OR gates to build all optical NOR gate, the performance of NOR depends on the both gates. So we first analyse and simulate the basic gates individually and then investigate the NOR gate.

4.4.1 NOT and OR gate

The NOT and OR gate are simulated by launching the continuous wave (CW) through the vertical input plane. To guide wave efficiently through the waveguide, the operating wavelength should be chosen from within the band gap or near the centre of gap. The band gap for NOT and OR gate layouts is calculated using plane wave expansion (PWE) method. The optimized diameter of reflecting rods and the lattice constant can be

estimated when operating wavelength is found. The band diagram shown in Fig. 4.3 gives the forbidden band gap. This band gap is analogous to electronic band gap between conduction and valence band.

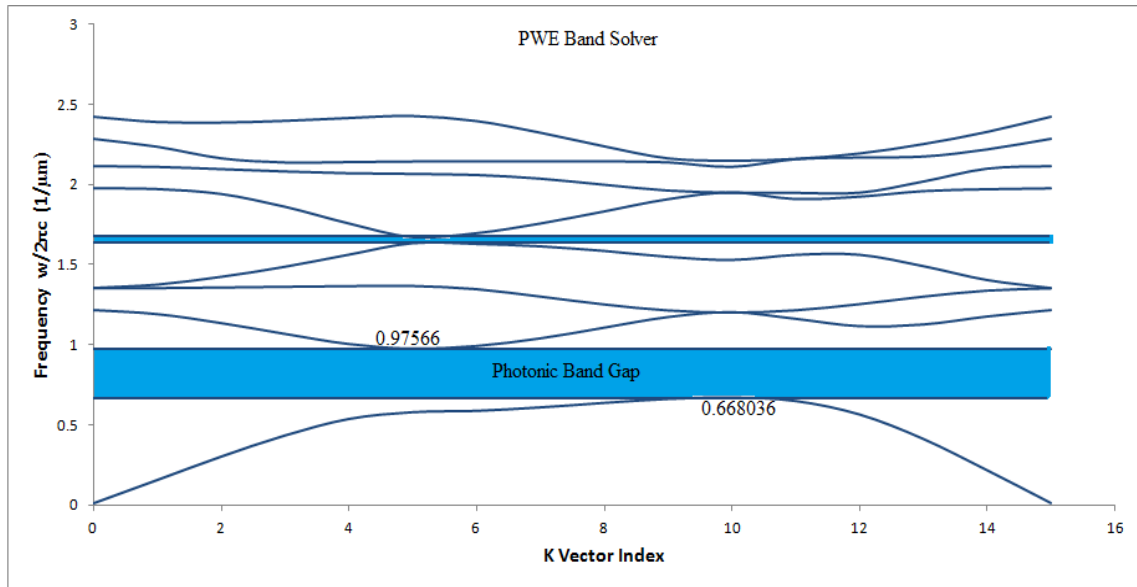


Fig. 4.3 Bandgap of OR and NOT gate using PWE Band Solver. Shaded area is the band gap. The calculated band gap is for Transverse Electric Mode (TE) whose electric field is parallel to rod axis.

There are two band gaps as shown in Fig. 4.3. The first band gap is from $1/\lambda$ (in $1/\mu m$) = 0.668036 to $1/\lambda$ (in $1/\mu m$) = 0.97566 and band gap width is 0.307624. The operating normalized frequency is chosen to be 0.7933 ($1/\mu m$), which corresponds to the wavelength equals to $1.2605\mu m$. The photonic band gap depends on the parameters such as wafer size and dielectric constant. Both of these parameters are same for NOT and OR gates, therefore the band gap is also similar.

Now the operation of logic NOT gate is discussed. The optical NOT gate complement its logic input. To demonstrate the behaviour of optical logic NOT gate, first launch the CW wave through the input port (IN) as logic '1'. The reference signal (REF) always exists of the same power P_a as the input signal. The power at the output port is $0.025P_a$ which acts as logic '0'. For physical understanding of layout of logic NOT gate, the electric field distribution is shown in Fig. 4.4(a).

In the second case, set the input port (IN) as logic level 0 and power of the reference port is set to be P_a . Then, power at the output port of logic NOT gate is $0.765P_a$ which acts as

logic high or '1'. For physical understanding of design of logic NOT gate, the corresponding electric field distribution is presented in Fig. 4.4(b).

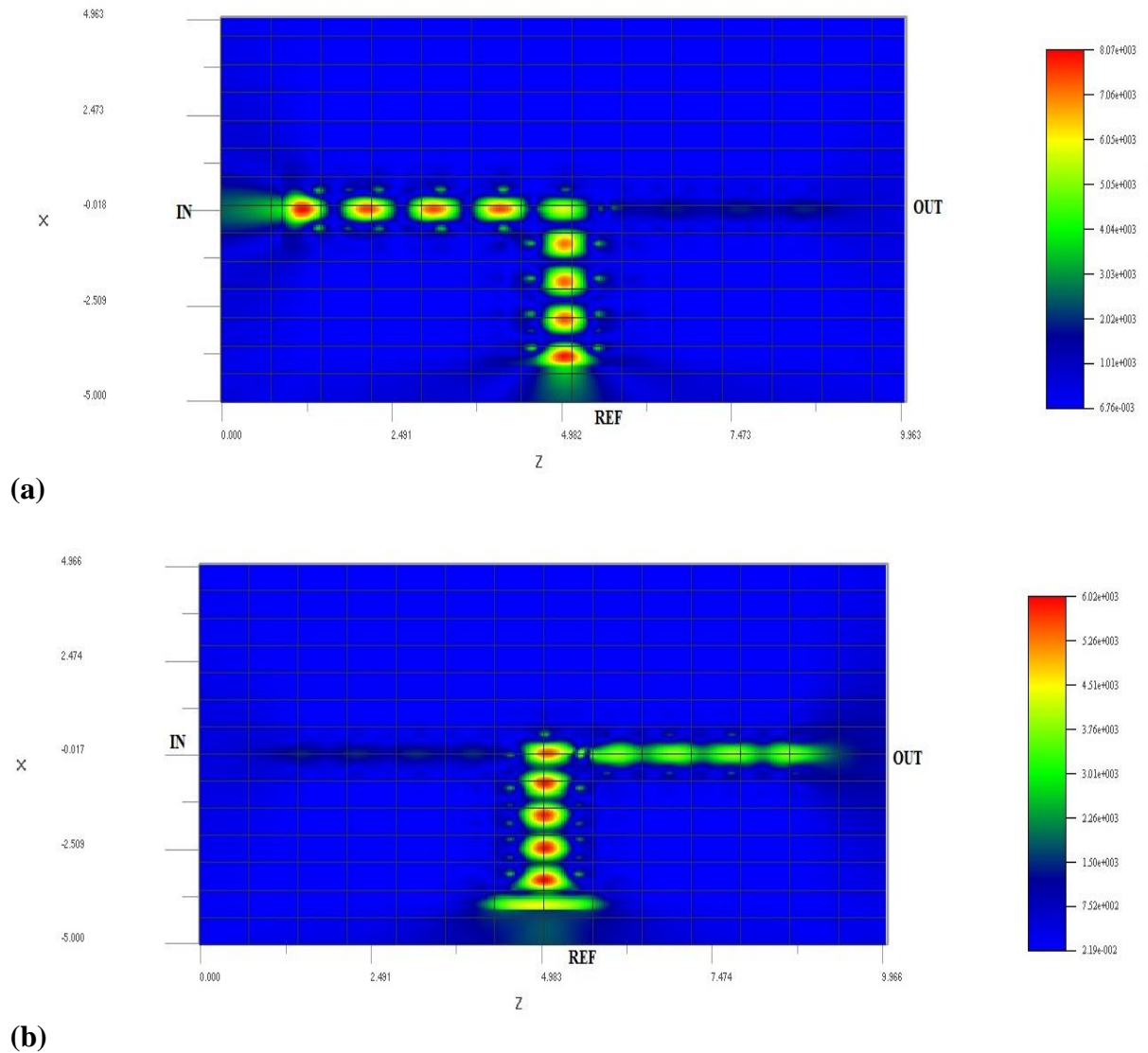


Fig. 4.4 Electric field distribution in the design of logic NOT gate. (a) when input signal is present then there is no output. It means output at logic level '0'. (b) when input signal is absent then there is output. It means output at logic level '1'

Input (IN)	Logical Output	Output Power
0	1	$0.765P_a$
1	0	$0.025P_a$

Table 4.1. Truth Table of Logic NOT gate

Table 4.1 shows that when input is high then output is low and when input is low then output is high. This is the logical function of NOT gate. The maximum output power for logic high is $0.765P_a$ and minimum power for logic low is $0.025P_a$.

The resonance of cavity plays an important role in localizing the field energy and reducing reflection for getting maximum transmission power. It tunnels the input wave towards the output with higher efficiency at the resonant wavelength of cavity. The resonance of cavity depends on the number of parameters. The optimized values of these parameters are obtained through iterative process. The radius of reflected rod (r_i) of logic NOT gate (Fig. 4.1(a)) is optimized by measuring the contrast ratio at different wavelengths as shown in Fig. 4.5.

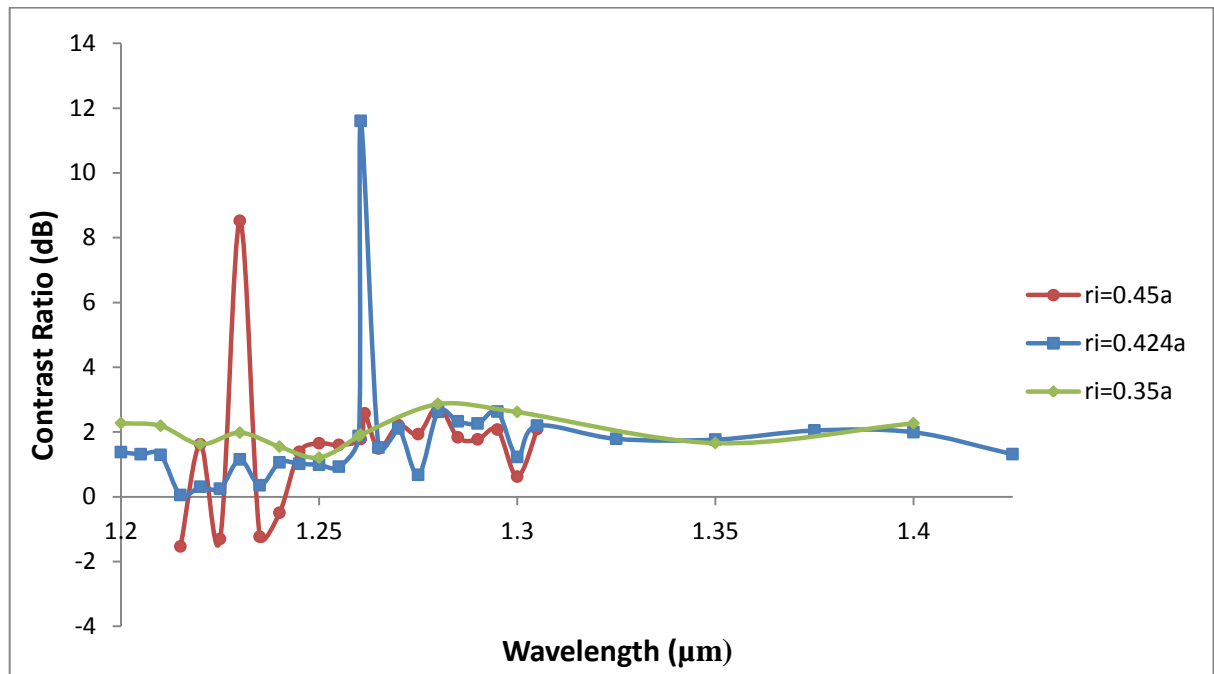
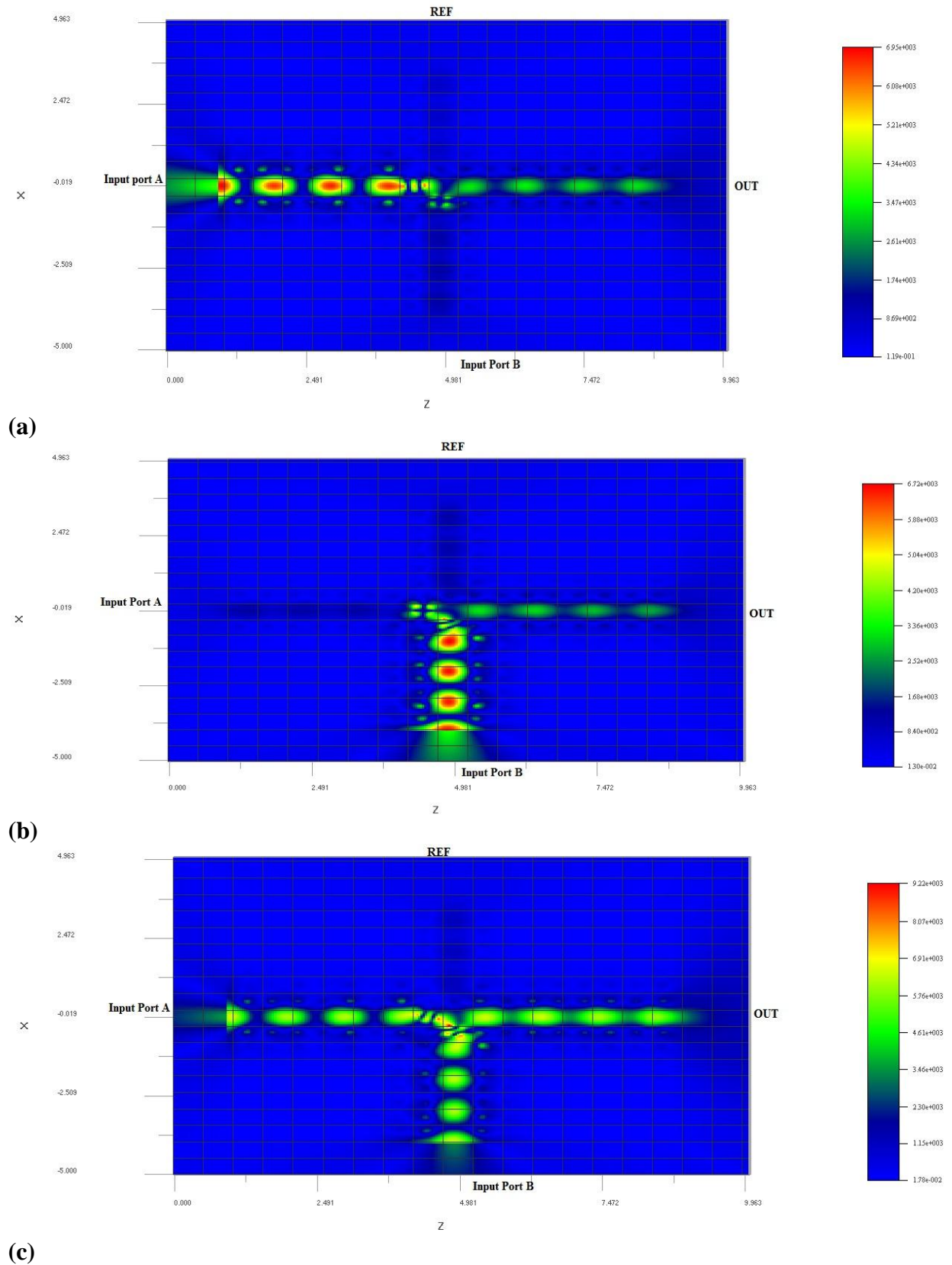


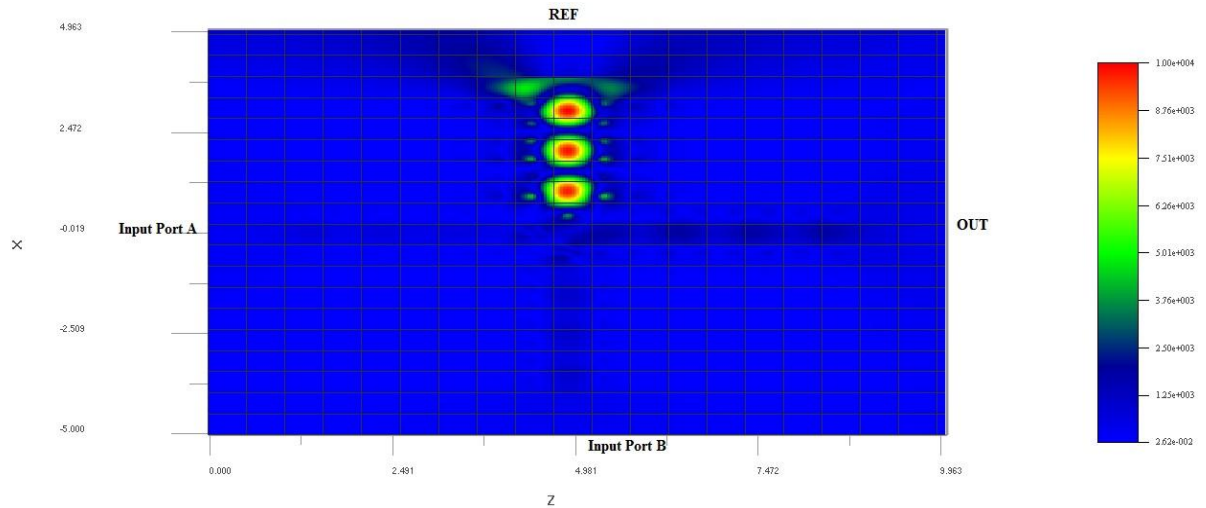
Fig. 4.5 Contrast ratio versus wavelength when the radius of reflected rod is varied.

The contrast ratio obtained with the radius (r_i) equals to $0.35a$ does not give any significant results. Whereas it is comparatively higher for the radius (r_i) equals to $0.45a$ but is still lower than the threshold value of 10dB . So the optimized radius of reflected rod (or defected rod) is $0.424a$ as this radius gives the highest contrast ratio of 11.605dB at the operating wavelength as shown in Fig. 4.5.

Now the design of optical logic OR gate is analysed and simulated. When the input signal is launched through horizontal waveguide (Input port A) or vertical waveguide (Input port B) then tunnelling of wave occurs. The result of which is, we obtain the logic high at the

output port (OUT). The tunnelling of wave occurs due to point defects at the cross centre. For the physical understanding, the corresponding electric field distribution is shown in Fig 4.6(a) and 4.6(b).





(d)

Fig. 4.6 Electric field distribution of optical logic OR gate when (a) input signal is given through the port A (b) input signal is injected through port B (c) both the input signal are launched simultaneously (d) no input signal is injected, only reference signal is exist.

When both the input signals are launched through horizontal waveguide (input port A) and vertical waveguide (input port B) then output power is high as shown in Fig. 4.6(c). Only reference signal is given when there is no input signal. In this condition all the energy is localized in the cavity. No tunnelling of the wave occurs. The result of which is, the output is logic low as shown in Fig. 4.6(d).

Input Port A	Input Port B	Logical Output	Output Power
0	0	0	$0.04P_a$
0	1	1	$0.337P_a$
1	0	1	$0.35P_a$
1	1	1	$0.84P_a$

Table 4.2. Truth table of logic OR gate

The output of optical logic OR gate is high when any one or both of input signals is high as shown in Table 4.2. The output power is computed by the FDTD method. It depends on the radius of reflected rods. The radius can be optimized by computing the contrast ratio at various wavelengths to obtain the maximum output power at the output port. If we increase the radius more than 0.48 times ‘a’ then the layout in Fig. 4.1(b) does not perform as OR gate. Thus, the functionality of logic OR gate is obtained efficiently for radius less than 0.48 times the lattice constant ‘a’.

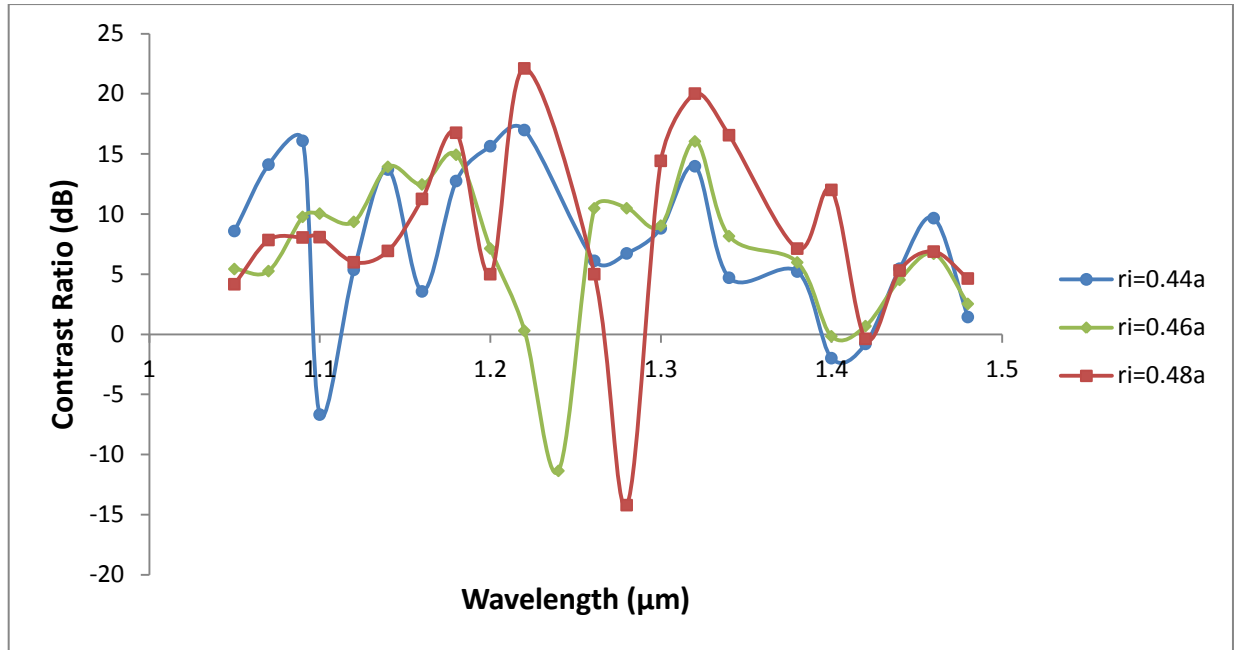


Fig. 4.7 Contrast ratio versus wavelength for different radius of reflected rods.

The contrast ratio with the three different radius is discussed. The optimized radius of reflected rods (or defected rods) is 0.48 times the lattice constant ‘a’ as it gives the highest contrast ratio of 22.113dB at the operating wavelength as shown in Fig.4.7. Once the optimized radius of reflected rods for logic NOT and OR gates are obtained, these gates are used with their respective radius in the design of NOR gate.

4.4.2 NOR gate

The layout of NOR gate is simulated by launching the continuous wave through the vertical input plane. To guide the wave properly through the waveguide, the operating wavelength is chosen from within photonic bandgap or near the centre of bandgap. The band diagram computed using PWE is shown in Fig. 4.8. This structure also has two photonic band gaps. The range of first band gap is from $1/\lambda$ (in $1/\mu m$) = 0.997585 to $1/\lambda$ (in $1/\mu m$) = 0.683049 and band gap width is 0.314536 (in $1/\mu m$). The operating frequency is chosen around the central frequency i.e. 0.7692(in $1/\mu m$) which corresponds to the wavelength equals to $1.3\mu m$. The band gap increases with the size of wafer and dielectric constant.

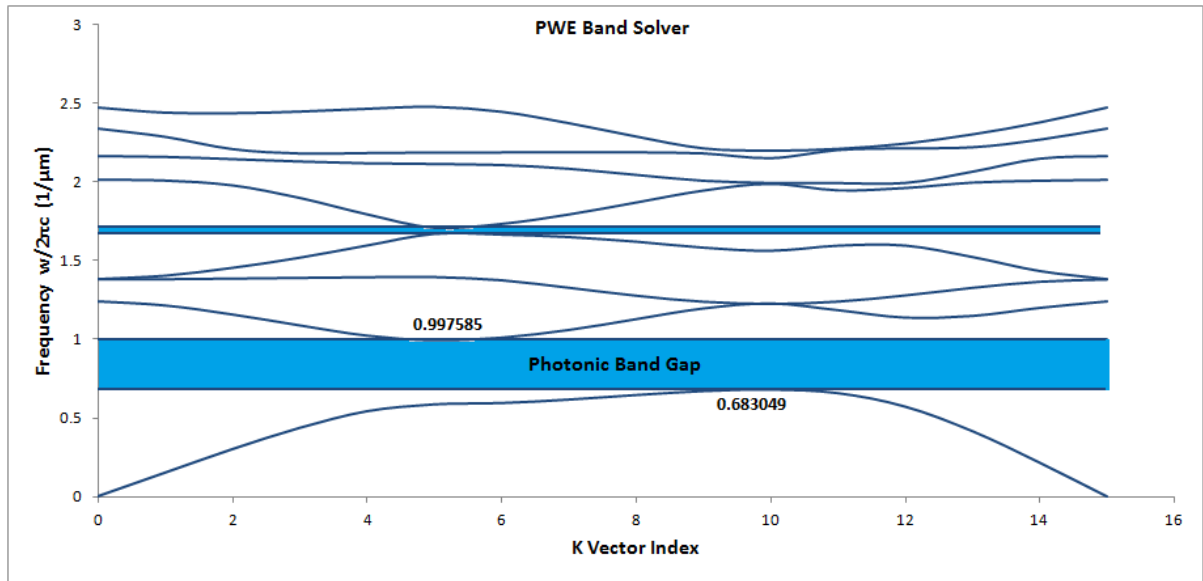
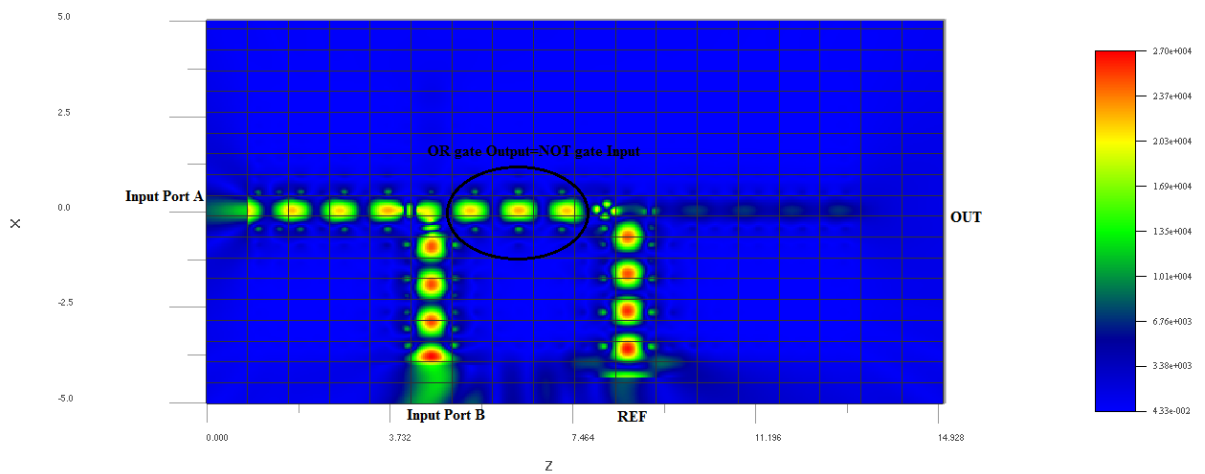
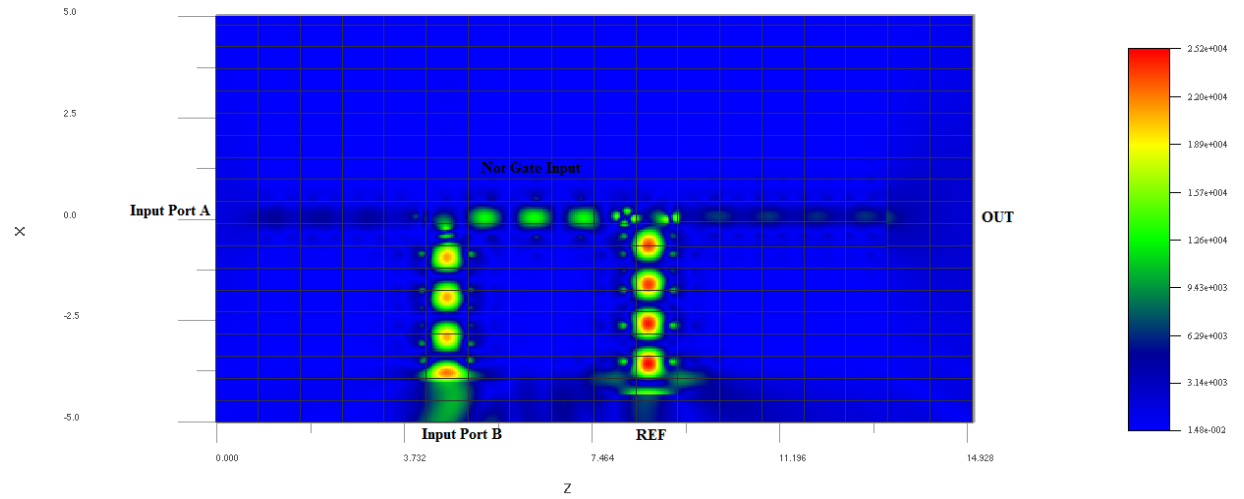


Fig. 4.8 Bandgap of logic NOR gate using PWE Band Solver. Shaded area is the band gap. The calculated band gap is for Transverse Electric Mode (TE) whose electric field is parallel to rod axis.

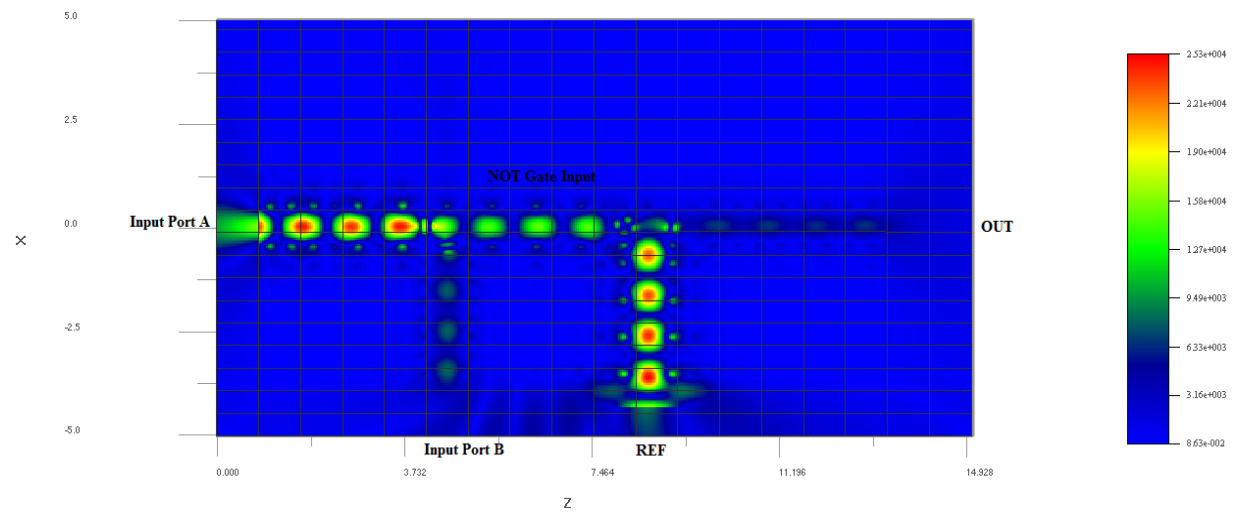
A 2D simulation is carried out to verify the functionality of NOR gate shown in Fig 4.2. First inject the input waves through the input ports A and B. It results in logic low at the output port of NOR gate. This is because the output of logic OR gate is input of NOT gate. The NOT gate complements the output of OR gate. Physically it can be understood through the electric field distribution as shown in Fig. 4.9(a). Also, when one of input signals is launched through the input port then the output is logic low for NOR gate as shown in Fig 4.9(b) and 4.9(c). The reference signal of NOR gate is always logic high.



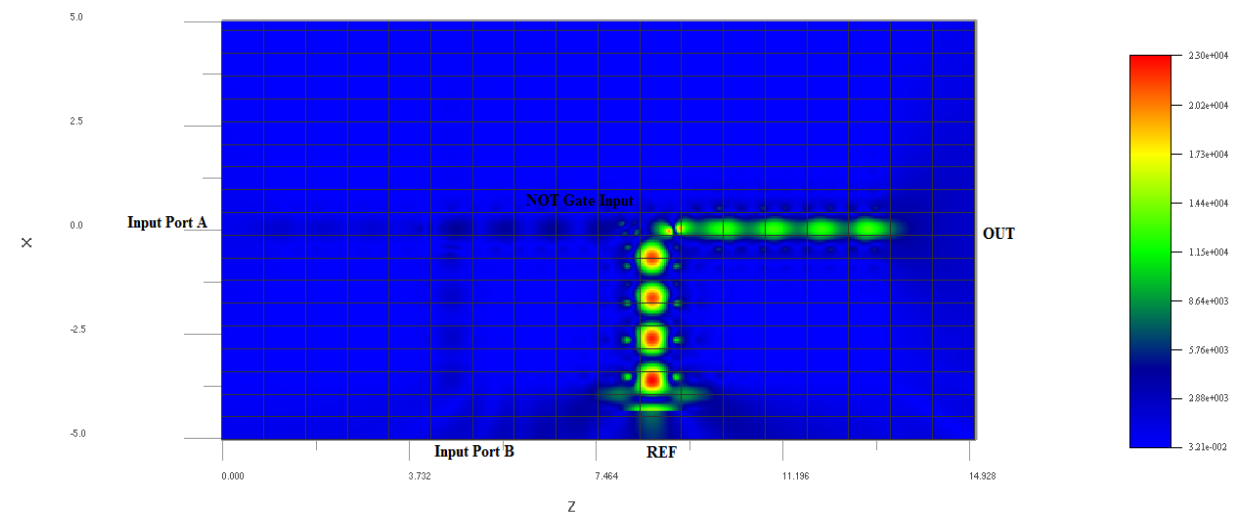
(a)



(b)



(c)



(d)

Fig. 4.9 Electric field distribution of optical logic NOR gate when (a) both the input signal are launched simultaneously (b) input signal is injected through port B (c) input

signal is given through the port A (d) no input signal is injected, only reference signal exist.

The output of logic NOR gate is high when there is no input signal at the input port as shown in Fig. 4.9(d). Only the reference signal exists at the REF port. The output of gate is high due to the tunnelling of wave and is low due to the interference of input signal with the reference signal. The reflection losses are however observed in the input ports. The output power of this gate is computed by FDTD method.

Input Port A	Input Port B	Logical Output	Output Power
0	0	1	$0.8P_a$
0	1	0	$0.013P_a$
1	0	0	$0.081P_a$
1	1	0	$0.014P_a$

Table 4.3 Truth table of optical logic NOR gate

The functionality of NOR gate is verified from the Truth Table 4.3. It shows that the output of NOR gate is high only when there is no input signal. The maximum output power for logic high is $0.8P_a$ and the minimum power for logic low is $0.013P_a$. Now the contrast ratio is obtained at the different wavelengths.

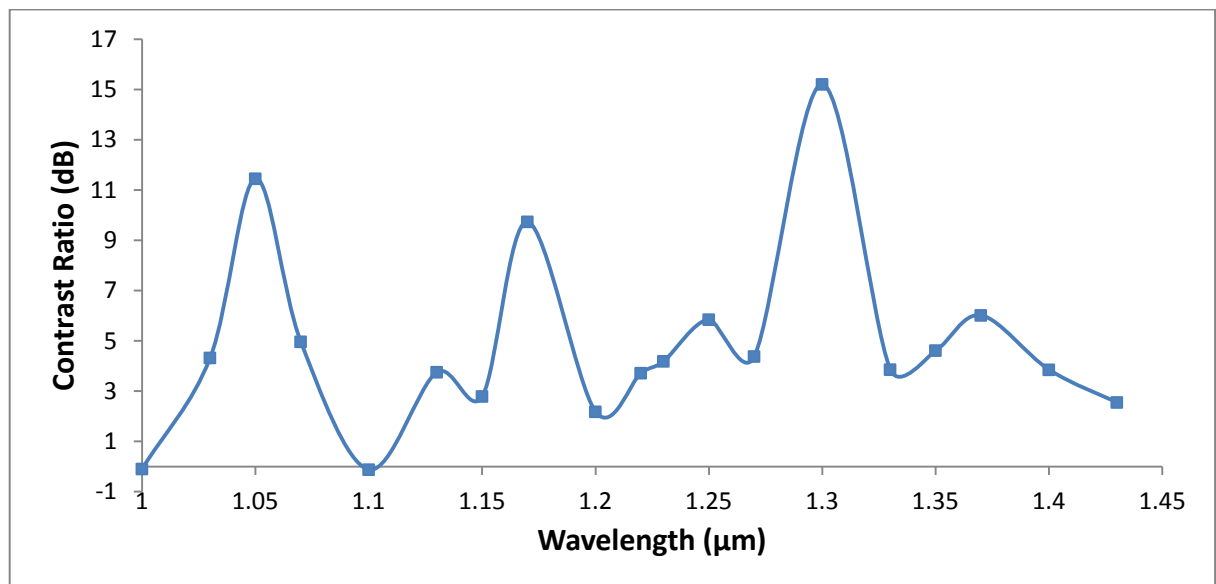


Fig. 4.10 Contrast ratio versus wavelength for optical NOR gate.

The contrast ratio is a factor of suitability check. If contrast ratio is large then the design can be used for integrated circuits. The maximum contrast ratio for NOR gate is 15.197dB as shown in Fig. 4.10. It has wide operating bandwidth i.e. the range of frequencies where contrast ratio is greater than any specified threshold value. We assume the minimum threshold value of contrast ratio as 10dB. Bandwidth of this structure is 0.04 μ m.

4.5 CONCLUSION

An optical logic NOR gate based on two different cross structures is presented. These two different cross structures are NOT and OR gate. The layout of logic NOT and OR gates are optimized individually using simulations. The contrast ratio for logic NOT gate is 11.605dB and for OR gate is 22.113dB. The size of NOT and OR structures are 10 μ m x 10 μ m only. With the optimized parameters, both the gates are combined without using any external device to design the NOR gate. The operation of NOR gate is numerically demonstrated using FDTD simulation. The contrast ratio is 15.97dB for NOR gate. Since non linear material is not used, the power consumption is less. It has an operating wavelength of 40nm. This structure is favorable for large scale integration circuits in the field of logic circuits.

CHAPTER 5

DESIGN AND ANALYSIS OF ALL OPTICAL NAND GATE BASED ON 2D PHOTONIC CRYSTALS

A design for simultaneous implementation of logic NOT and AND gate is presented to form all optical logic NAND gate. This structure is based on 2D photonic crystals. It consists of square lattice of silicon dielectric rods in air. The layout of logic NOT and AND gates are optimized individually using FDTD simulations. The contrast ratio for logic NOT gate is 11.605dB and for AND gate is 7.624dB. The size of NOT and AND structures are 10 μ m x 10 μ m only. With the optimized parameters, both the gates are combined without using any external device to design the NAND gate. The fabrication error tolerance is analyzed for optical logic NAND gate, when radius of all rods is larger than the theoretical parameters from +10% to +30%. The maximum contrast ratio for Δ =+10%, +20%, +30% is 15.04dB, 10.54dB and 12.04dB respectively. The contrast ratio for theoretical designed NAND gate is 22.076dB. Since non linear material is not used, the power consumption is less. This structure is favorable for large scale integration circuits in the field of logic circuits and also useable in future optical communication system and optical signal processor.

5.1 INTRODUCTION

All optical logic gates are the important component of optical signal processor and optical computing system. Because it performs necessary functions at the nodes of optical network such as pattern matching, data encoding and decoding, recognition and different switching functions [21]. There are various methods to realize optical gate such as semiconductor optical amplifier [62], optical waveguide interferometer [55] and fibre grating [63, 64]. But all suffer from certain limitations such as low speed, big size and difficulty to integrate on chip.

Photonic crystal is artificially designed optical material in which dielectric constant varied periodically [11, 65]. Due to their unique properties, the photonic crystal based logic gates have numerous advantages such as compactness, simple structure, high speed and high confinement [28, 58, 66]. There are some wavelengths which do not propagate through the photonic crystal. These wavelengths form the photonic band gap [45, 46]. By engineering this gap, flow of light can be controlled. This gap can be calculated by PWE

method [47]. There are a number of design of all optical photonic crystal logic gate have been presented. These design based on ring resonator [58] and self collimation phenomena [28]. But they are based on nonlinear material and require a certain scale of volume which is a limitation for photonic integrated circuits.

Andalib et al. [58] designed logic AND gate based on two nonlinear photonic crystal ring resonator. Its bit rate is 120Gbits/sec and contrast ratio is -6.93 dB only. The main advantage of this structure is that it is not sensitive to the deviation of input power. Susan Christina Xavier et al. [36] presented a design of optical AND and NAND gate. It is based on self collimated phenomena. The same structure behaves as AND, NAND and other optical logic gate by changing the input signal and reference signal level. Preeti Rani et al. [27] designed a logic AND gate based on 2D photonic crystal. The layout consists of Y shaped waveguide without using nonlinear material. Its contrast ratio is 6.017 dB at the normalized wavelength.

In all the above structures, the contrast ratio is not sufficiently high for their efficient operation. It is observed that the main flaw of the structure discussed in [58] is that it required high input power due to non linear material. The structure [36] is sensitive to phase difference between input and reference signal. Due to which the contrast ratio is low. Thus, it results in the poor performance of this logic gate.

In this chapter, a new approach for the design of optical logic NAND gate have investigated by simultaneous implementation of NOT gate and AND gate. This approach has resulted in low reflection losses at the input ports and therefore high contrast ratio is achieved. The designed structures consist of cross waveguides. It based on 2D photonic crystal of silicon in air substrate. These structures are optimized for high contrast ratio by introducing the point cavities of appropriate radius at the cross intersection point. The contrast ratio of logic gate is a factor that determines the suitability of the design. In this design the contrast ratio is 11.605dB for NOT gate and 7.624dB for AND gate which is higher than the earlier reported works [58]. The designed structure of NAND gate performed well when the radius of all rods is fabricated with error tolerance of +10% to +30% from designed parameters.

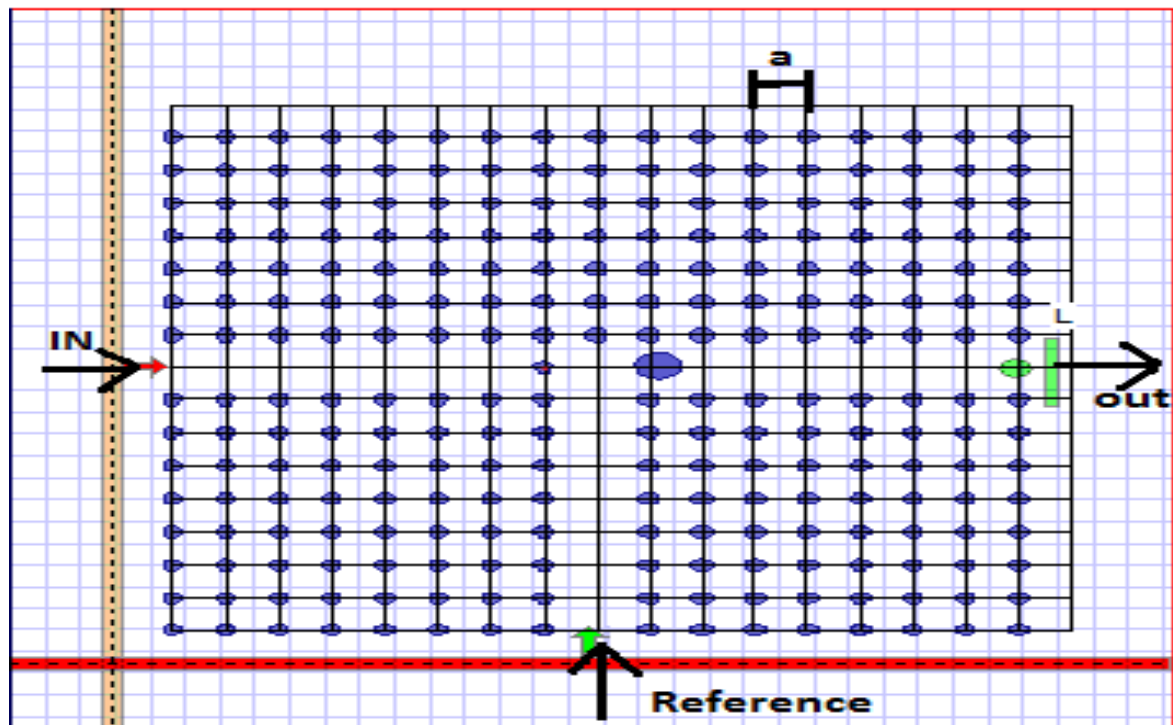
This chapter is organized as follows. In Section 5.2, first present the model and operating principle of the optical NOT and AND gate then the model of NAND gate. In Section 5.3,

the basic optical logic gate NOT and AND gate are investigated and optimized then the model of NAND gate is investigated. In Section 5.4, a brief conclusion is given.

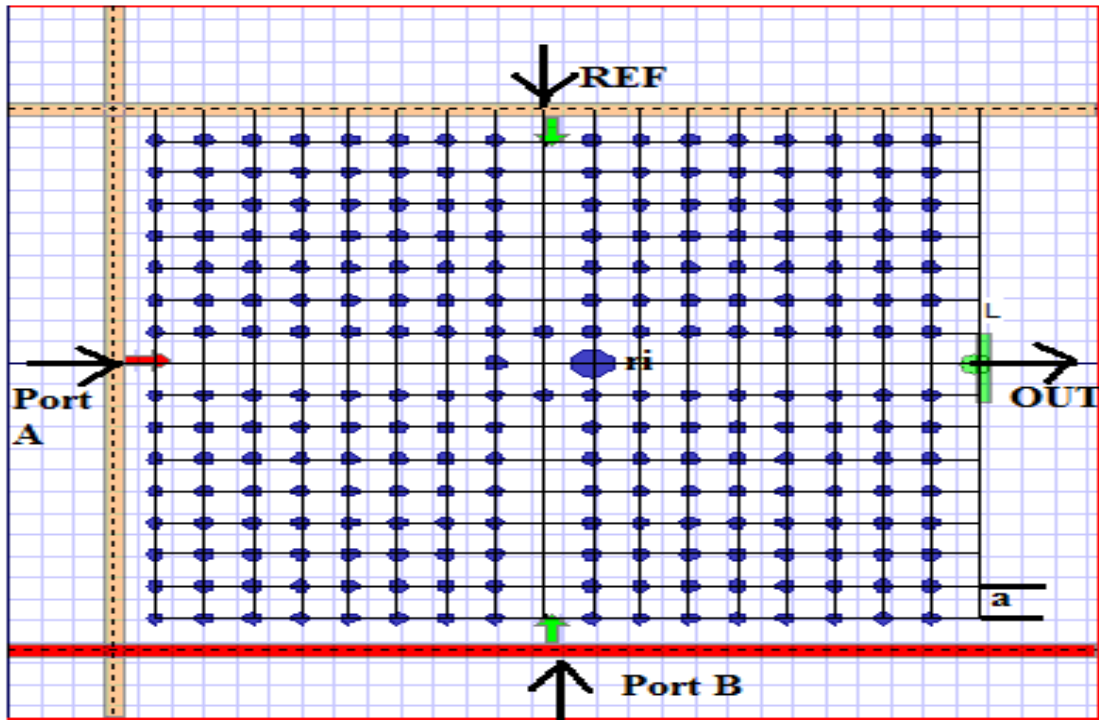
5.2 SIMULATION SETUP

5.2.1 Layout of Basic optical logic “NOT gate” and “AND gate”

The design of optical logic NOT and AND gates on 2D square lattice in XZ plane individually is presented. The wafer size of both the gates is $10\mu\text{m} \times 10\mu\text{m}$. The structure of NOT gate consists of two linear interference waveguides in T shape. But the structure of AND gate consists of two linear waveguides cross at the centre. The linear waveguides are formed by the removal of series of dielectric rods which is known as line defect. The Silicon rods (16×17) of refractive index 3.4 and radius (r) of 0.18 times lattice constant (represented as ‘ a ’) are placed in the air. The distance between two dielectric rods is known as lattice constant. The two reflecting rods are placed around the centre to form horizontal cavity in the NOT gate. In the layout of AND gate, the four reflecting rods are introduced. The radius of reflecting rods are chosen properly so that transmitted power is high at the output port.



(a)



(b)

Fig. 5.1 Schematic Layout of all optical logic gates on 2D square lattice in XZ plane. The arrow pointing inward represent the input signal and reference signal and outward represent the output signal.(a) Logic NOT gate consists of two linear waveguide in T shape and point defect. (b) Logic AND gate consists of two line defect and four point defect.

The layout of logic NOT gate is shown in Fig. 5.1(a). A vertical input plane is used for injecting the input signal which is represented by IN. Another signal is the reference signal which is launched from the horizontal input plane at the port marked as reference in Fig. 5.1(a). Both the signals have same phase and frequency. The observation point and line in the horizontal waveguide at the output port are used as a power detector. The point to be noted is that the NOT gate is a bidirectional gate. The input and output ports of NOT gate can be interchanged. The layout of all optical logic AND gate is demonstrated in Fig. 5.1(b). There are two input ports (marked as ports A and B in Fig. 5.1(b)) for input signals and one port for reference signal (marked as REF in Fig. 5.1(b)). The reference signal is always used. The silicon rods with different size are introduced as reflecting rods or point defect in the layout. The radius of defected rods (r_i) is large so that more power is

transmitted toward the output. The radius of reflected rods (r_i) is optimized by computing the contrast ratio in the section below.

5.2.2 Layout of optical NAND gate using basic logic gates

It is known that the function of logic NAND gate is logical complement of an AND gate. NAND gate is designed by combining AND gate and NOT gate without using any external device like amplifier, coupler etc. It is also designed on 2D square lattice photonic crystal with wafer size of $13\mu\text{m} \times 10\mu\text{m}$. The rest of parameters such as dielectric constant, radius of dielectric rods, position and radii of reflected rods are same as that in the layout of Fig. 5.1.

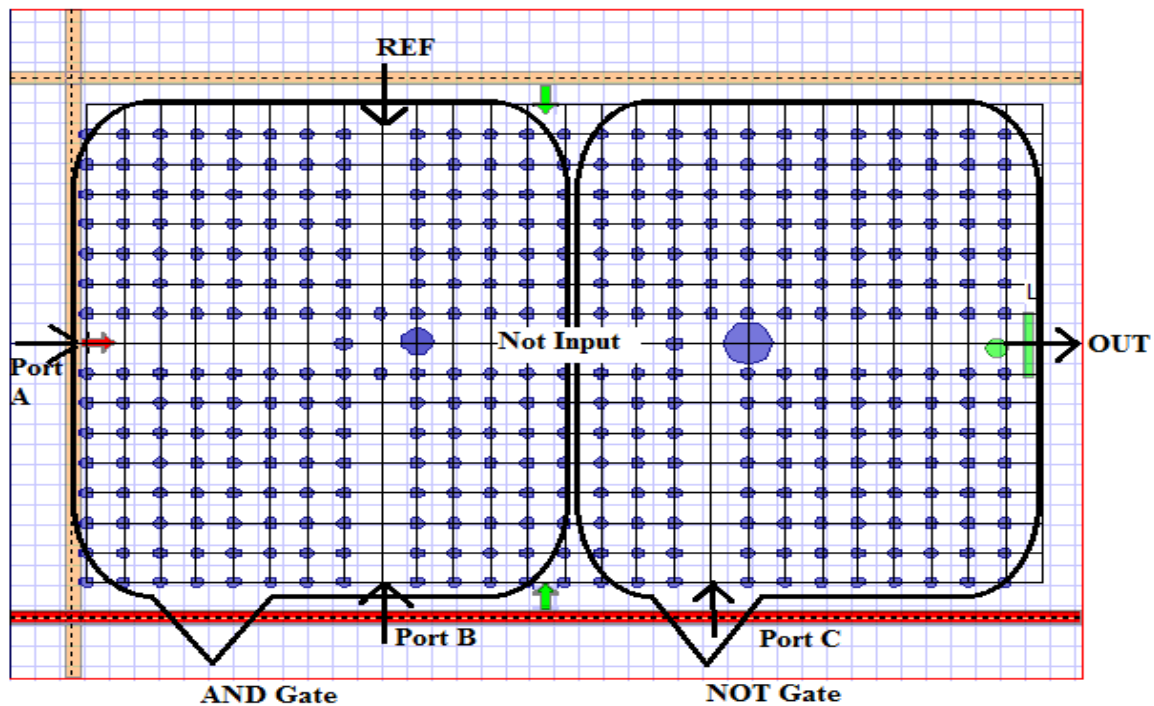


Fig. 5.2 Layout of optical NAND gate using basic optical logic gates on 2D square lattice in XZ plane. It consists of three input port, one reference signal port and one output port.

All optical NAND gate consists of three interference waveguides as shown in Fig. 5.2. One waveguide is common for both the combined optical logic gates. The output of AND gate acts as the input of NOT gate. The NOT gate complements the output of logic AND gate. The output port of NAND gate is same as the output port of NOT gate.

5.3 RESULTS AND DISCUSSIONS

Since one needs NOT and AND gates to build all optical NAND gate, the performance of NAND depends on the both gates. So we first analyse and simulate the basic gates individually and then investigate the NAND gate.

5.3.1 NOT and AND gate

The NOT and AND gate are simulated by launching the continuous wave (CW) through the vertical input plane. To guide wave efficiently through the waveguide, the operating wavelength should be chosen from within the band gap or near the centre of gap. The band gap for NOT and AND gate layouts is calculated using plane wave expansion (PWE) method. The band diagram of structures is shown in Fig. 5.3 give the forbidden band gap. This band gap is analogous to electronic band gap between conduction and valence band.

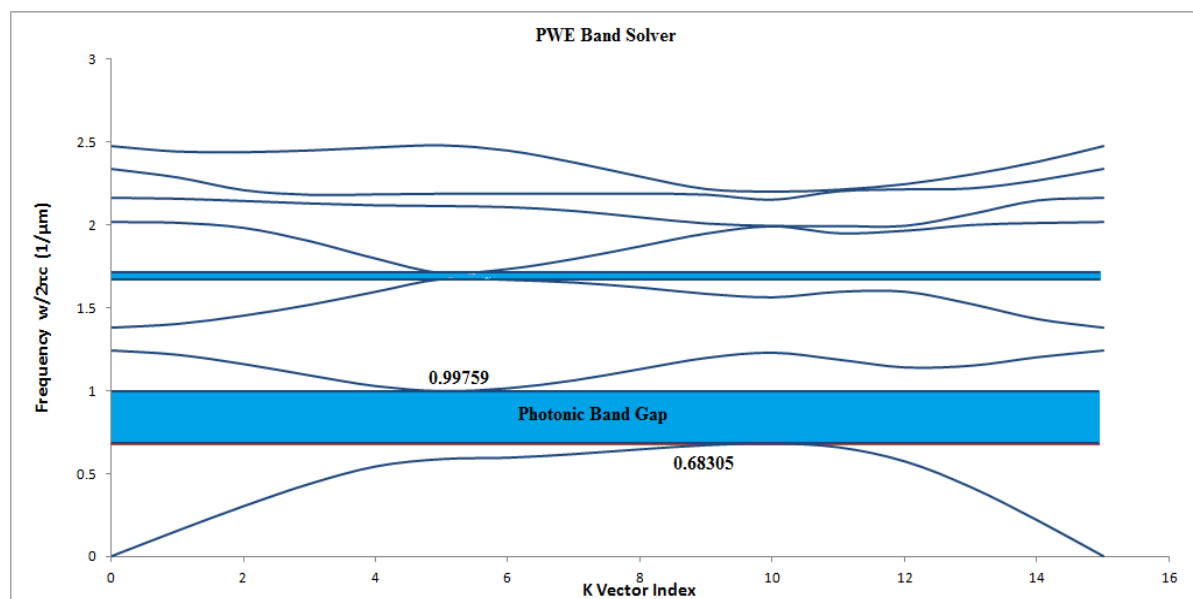


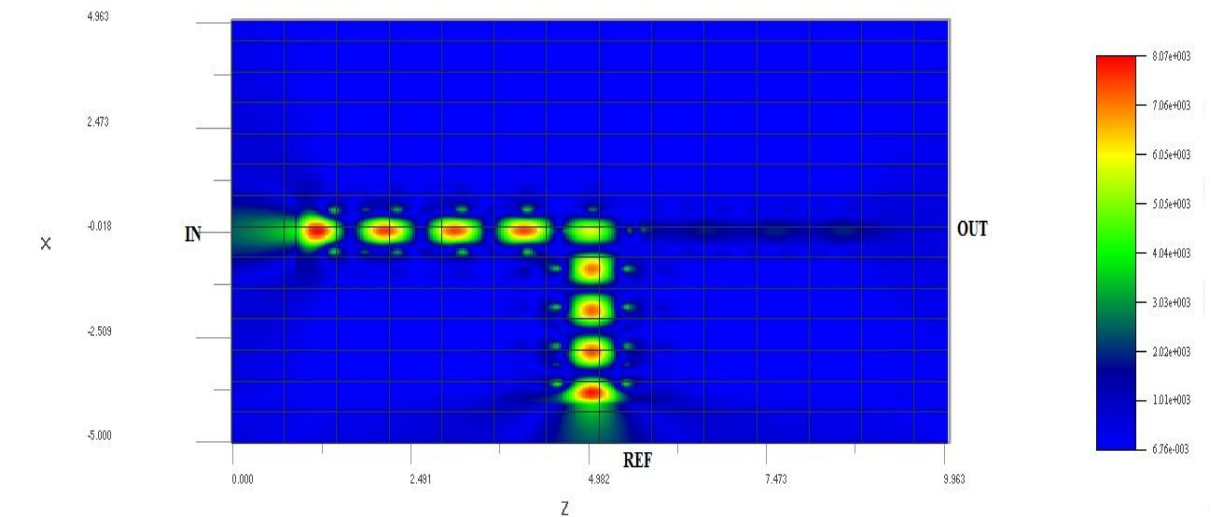
Fig. 5.3 Bandgap of AND and NOT gate using PWE Band Solver. Shaded area is the band gap. The calculated band gap is for Transverse Electric Mode (TE) whose electric field is parallel to rod axis.

There are two band gaps as shown in Fig. 5.3. The first band gap is from $1/\lambda$ (in $1/\mu m$) = 0.68305 to $1/\lambda$ (in $1/\mu m$) = 0.99759 and band gap width is 0.31451. The operating normalized frequency is chosen to be 0.78125 ($1/\mu m$), which corresponds to the wavelength equals to $1.28\mu m$. The photonic band gap depends on the parameters such as

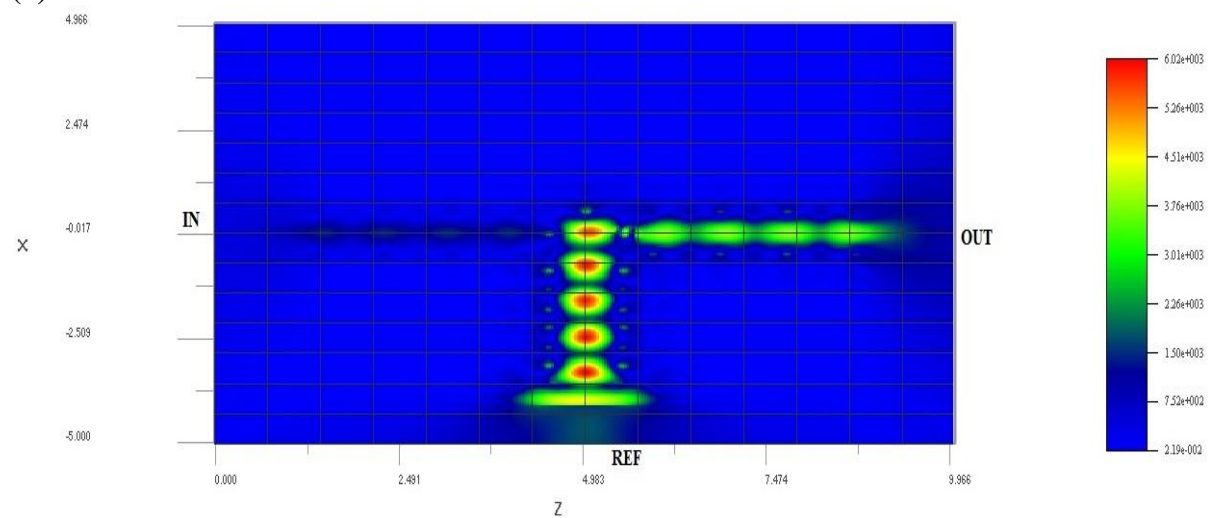
lattice constant and dielectric constant. Both of these parameters are same for NOT and AND gates, therefore the band gap is also similar.

Now the operation of logic NOT gate is discussed. The optical NOT gate complement its logic input. To demonstrate the behaviour of optical logic NOT gate, first launch the CW wave through the input port (IN) as logic '1'. The reference signal (REF) always exists of the same power P_a as the input signal where P_a can be any value. The power at the output port is $0.025P_a$ which acts as logic '0'. For physical understanding of layout of logic NOT gate, the electric field distribution is shown in Fig. 5.4(a).

In the second case, set the input port (IN) as logic level 0 and power of the reference port is set to be P_a . Then, power at the output port of logic NOT gate is $0.765P_a$ which acts as logic high or '1'. For physical understanding of design of logic NOT gate, the corresponding electric field distribution is presented in Fig. 5.4(b).



(a)



(b)

Fig. 5.4 Electric field distribution in the design of logic NOT gate. **(a)** when input signal is present then there is no output. It means output at logic level ‘0’. **(b)** when input signal is absent then there is output. It means output at logic level ‘1’

Input (IN)	Logical Output	Output Power
0	1	$0.765P_a$
1	0	$0.025P_a$

Table 5.1 Truth Table of Logic NOT gate

Table 5.1 shows that when input is high then output is low and when input is low then output is high. This is the logical function of NOT gate. The maximum output power for logic high is $0.765P_a$ and minimum power for logic low is $0.025P_a$.

The resonance of cavity plays an important role in localizing the field energy and reducing reflection for getting maximum transmission power. It tunnels the input wave towards the output with higher efficiency at the resonant wavelength of cavity. The resonance of cavity depends on the number of parameters. The optimized values of these parameters are obtained through iterative process. One of the parameter is radius of reflected rod. The radius of reflected rod (r_i) of logic NOT gate (Fig. 5.1(a)) is optimized based on the higher contrast ratio. The contrast ratio (CR) is defined as [20]

$$CR = 10 \log_{10} \frac{P_1}{P_0} \quad (5.1)$$

where P_1 and P_0 are the optical output power of logic high (‘1’) and logic low (‘0’) respectively. In Fig. 5.5, the contrast ratio is measured at the different wavelength with various radius of reflected rod.

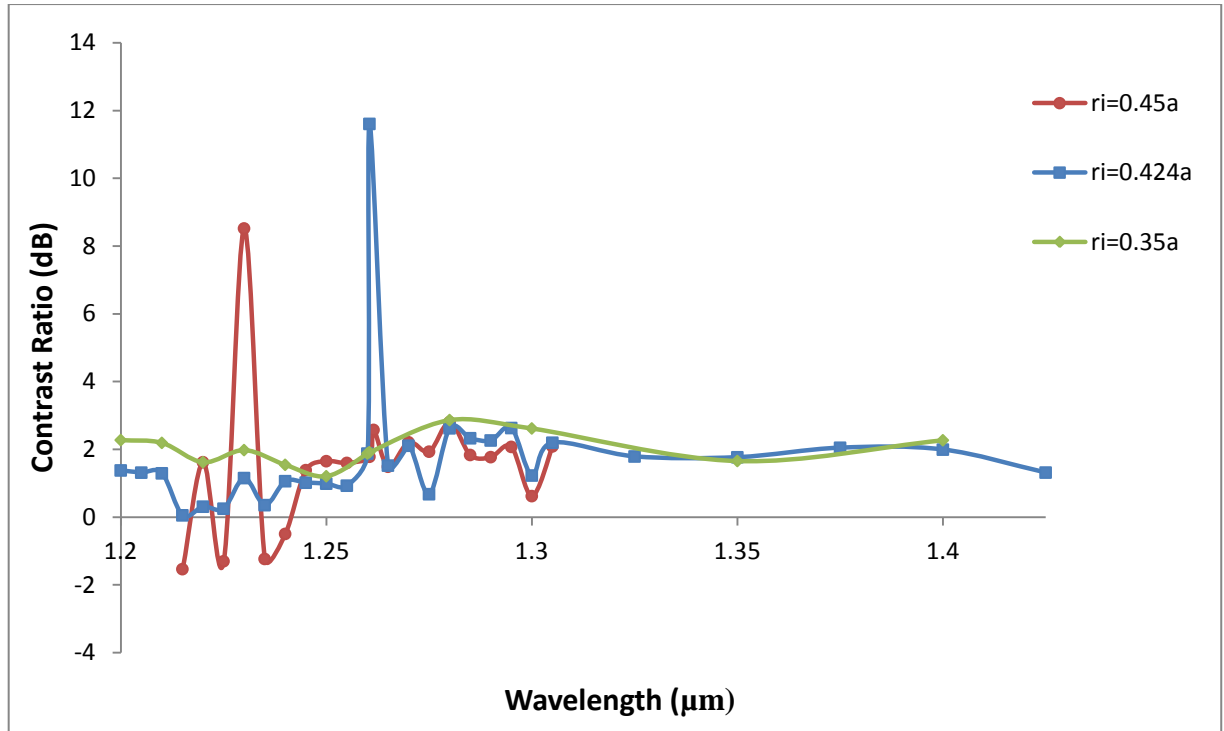
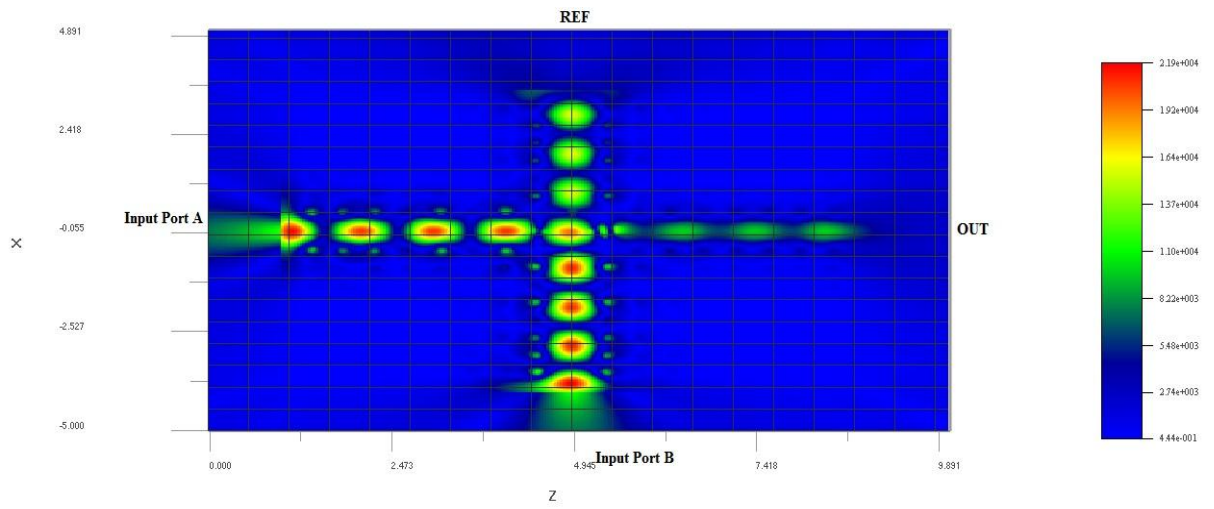


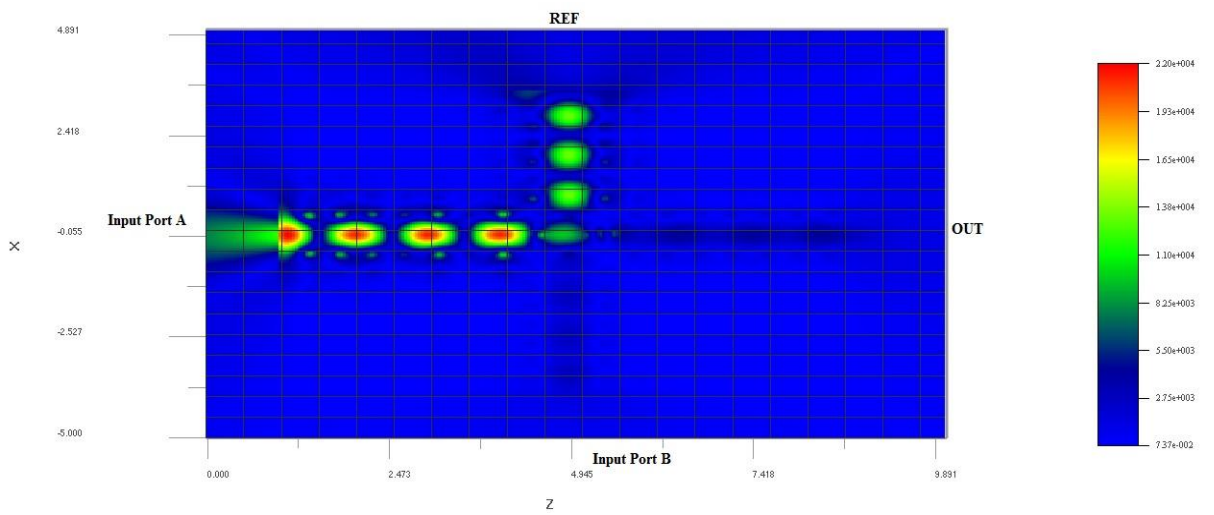
Fig. 5.5 Contrast ratio versus wavelength when the radius of reflected rod is varied.

The contrast ratio obtained with the radius (r_i) equals to $0.35a$ does not give any significant results. Whereas it is comparatively higher for the radius (r_i) equals to $0.45a$ but is still lower than the threshold value of 10dB . So the optimized radius of reflected rod (or defected rod) is $0.424a$ as this radius gives the highest contrast ratio of 11.605dB at the operating wavelength as shown in Fig. 5.5.

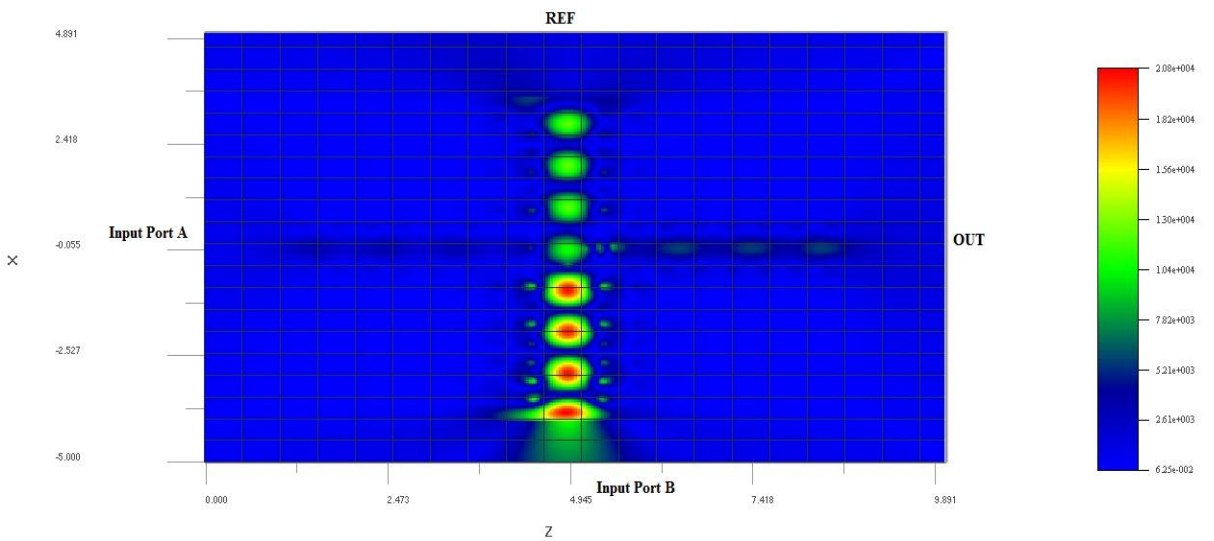
Now the design of optical logic AND gate is analysed and simulated. When the input signal is launched through both the horizontal waveguide (Input port A) and vertical waveguide (Input port B) then tunnelling of wave occurs. The result of which is, we obtain the logic high at the output port (OUT). The tunnelling of wave occurs due to point defects at the cross centre. For the physical understanding, the corresponding electric field distribution is shown in Fig. 5.6(a).



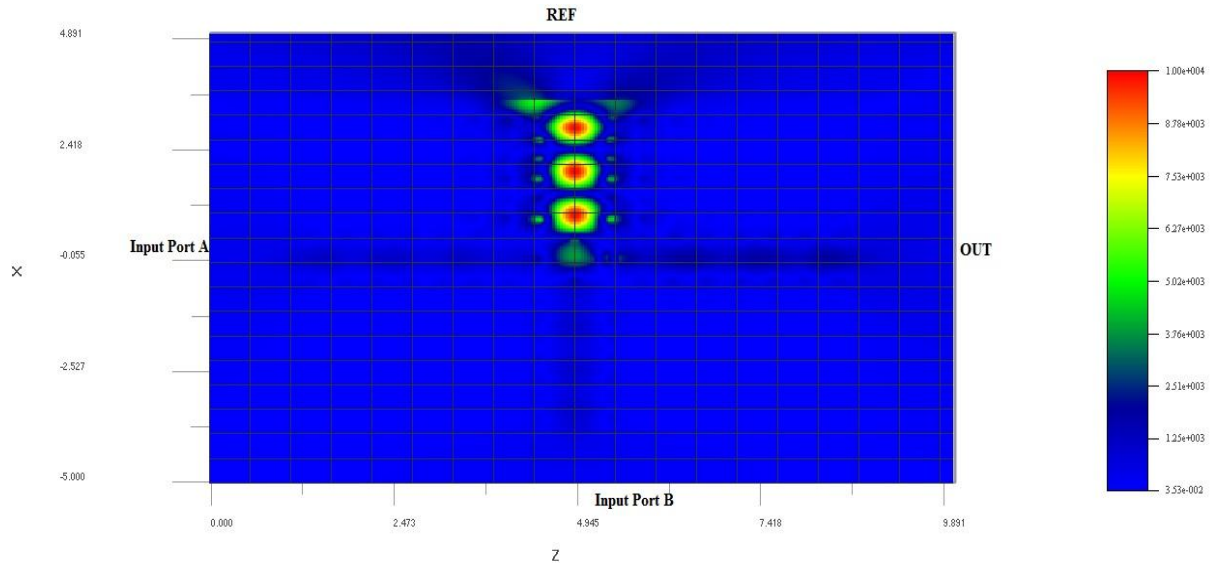
(a)



(b)



(c)



(d)

Fig. 5.6 Electric field distribution of optical logic AND gate when (a) input signal is given through both the port A and the port B (b) input signal is injected through the port A (c) the input signal are launched through the port B (d) no input signal is injected, only reference signal is exist.

When one of the input signals are launched through horizontal waveguide (input port A) or vertical waveguide (input port B) then output power is low as shown in Fig. 5.6(b) and 5.6(c). Only the reference signal is given when there is no input signal. In this condition all the energy is localized in the cavity. No tunnelling of the wave occurs. The result of which is, the output is logic low as shown in Fig. 5.6(d).

Input Port A	Input Port B	Logical Output	Output Power
0	0	0	$0.074P_a$
0	1	0	$0.088P_a$
1	0	0	$0.034P_a$
1	1	1	$0.513P_a$

Table 5.2. Truth table of logic AND gate

The output of optical logic AND gate is high when both of input signals is high as shown in Table 5.2. The output power is computed by the FDTD method. It depends on the radius of reflected rods. The radius can be optimized by computing the contrast ratio at various wavelengths to obtain the maximum contrast ratio at the output port. If we increase the radius greater than 0.6 times 'a' then the layout in Fig. 5.1(b) does not

perform as AND gate. Thus, the functionality of logic AND gate is obtained efficiently for radius less than 0.6 times the lattice constant ‘a’ and greater than 0.45 times ‘a’.

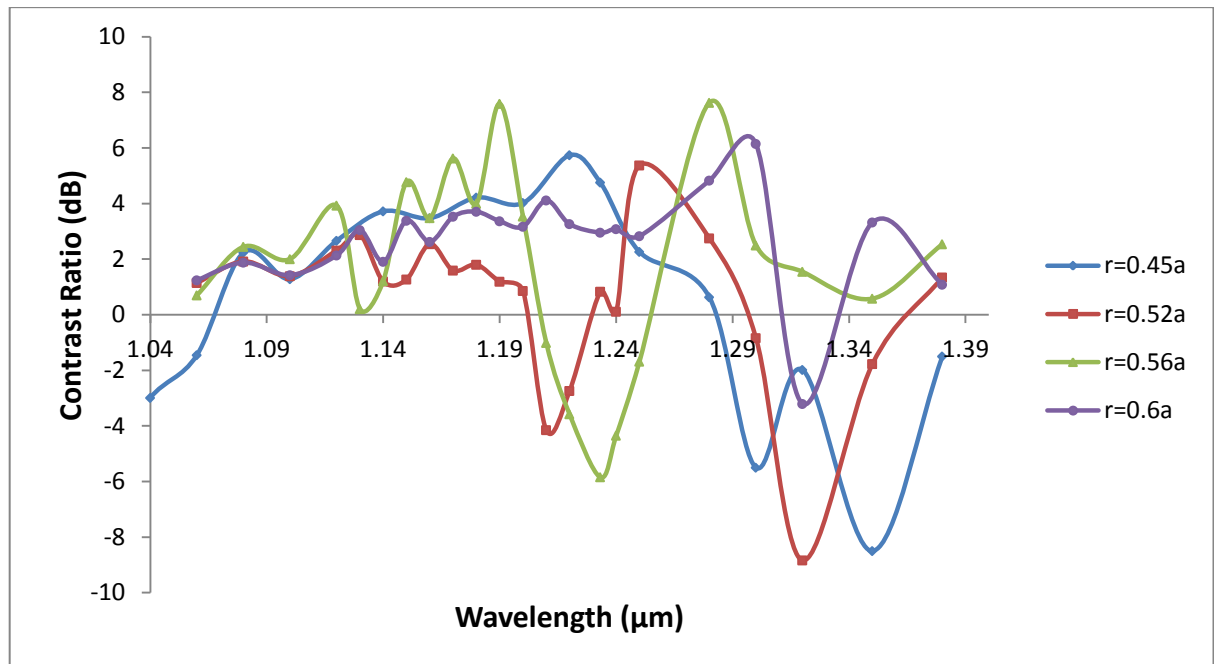


Fig. 5.7 Contrast ratio versus wavelength for different radius of reflected rods.

The contrast ratio with the four different radius is discussed. The optimized radius of reflected rods (or defected rods) is 0.56 times the lattice constant ‘a’ as it gives the highest contrast ratio of 7.624dB at the operating wavelength as shown in Fig. 5.7. Once the optimized radius of reflected rods for logic NOT and AND gates are obtained, these gates are used with their respective radius in the design of NAND gate.

5.3.2 NAND gate

The layout of NAND gate is simulated by launching the continuous wave through the vertical input plane. To guide the wave properly through the waveguide, the operating wavelength is chosen from within photonic bandgap or near the centre of bandgap. The band diagram computed using PWE is shown in Fig. 5.8. This structure also has two photonic band gaps. The range of first band gap is from $1/\lambda$ (in $1/\mu\text{m}$) = 0.73594056 to $1/\lambda$ (in $1/\mu\text{m}$) = 1.04870228 and band gap width is 0.312762 (in $1/\mu\text{m}$). The operating frequency is chosen around the central frequency i.e. 0.8403361 (in $1/\mu\text{m}$) which corresponds to the wavelength equals to 1.19μm.

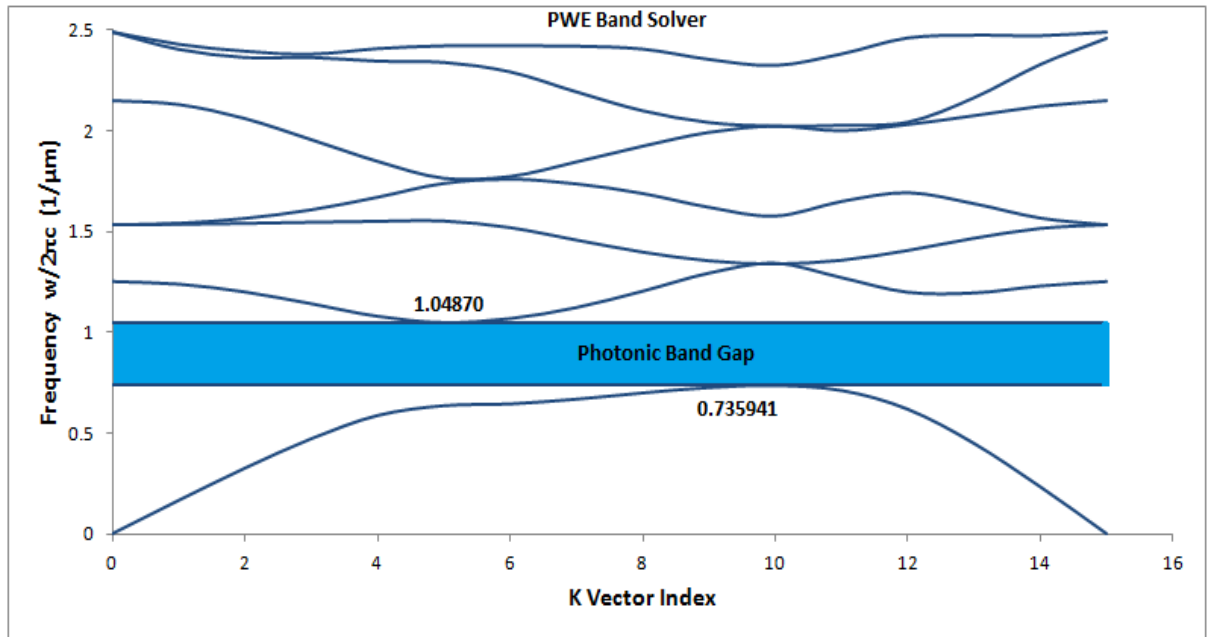
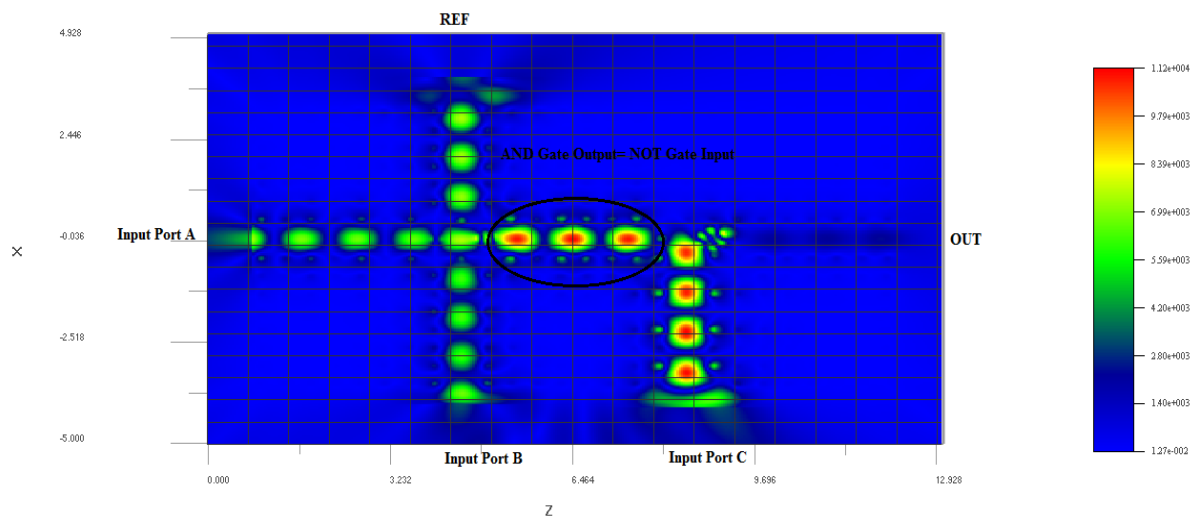
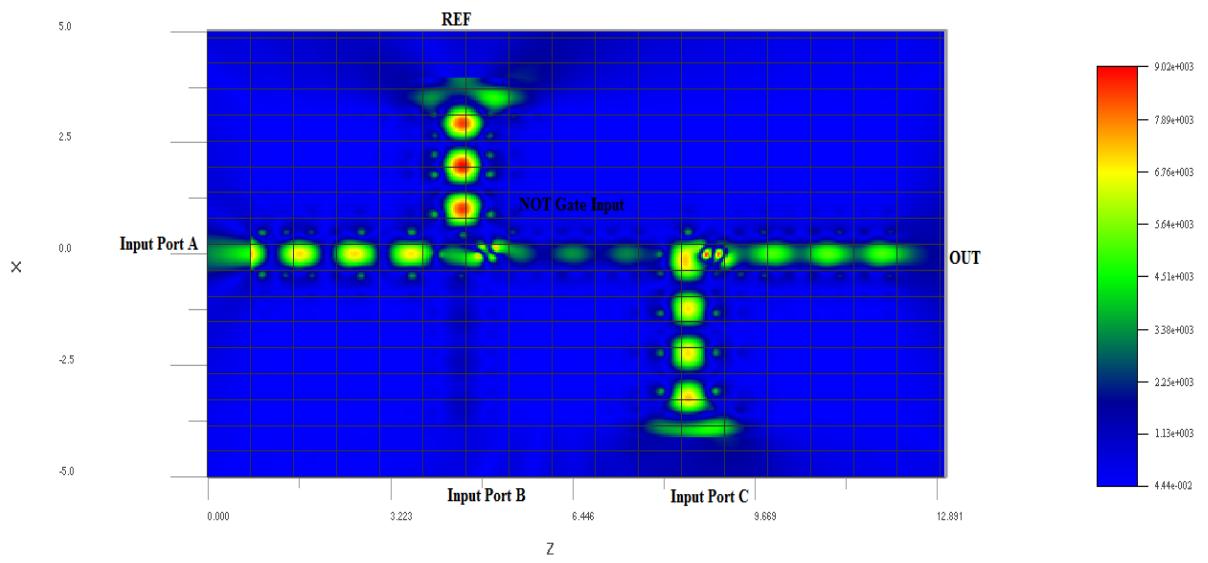


Fig. 5.8 Bandgap of logic NAND gate using PWE Band Solver. Shaded area is the band gap. The calculated band gap is for Transverse Electric Mode (TE) whose electric field is parallel to rod axis.

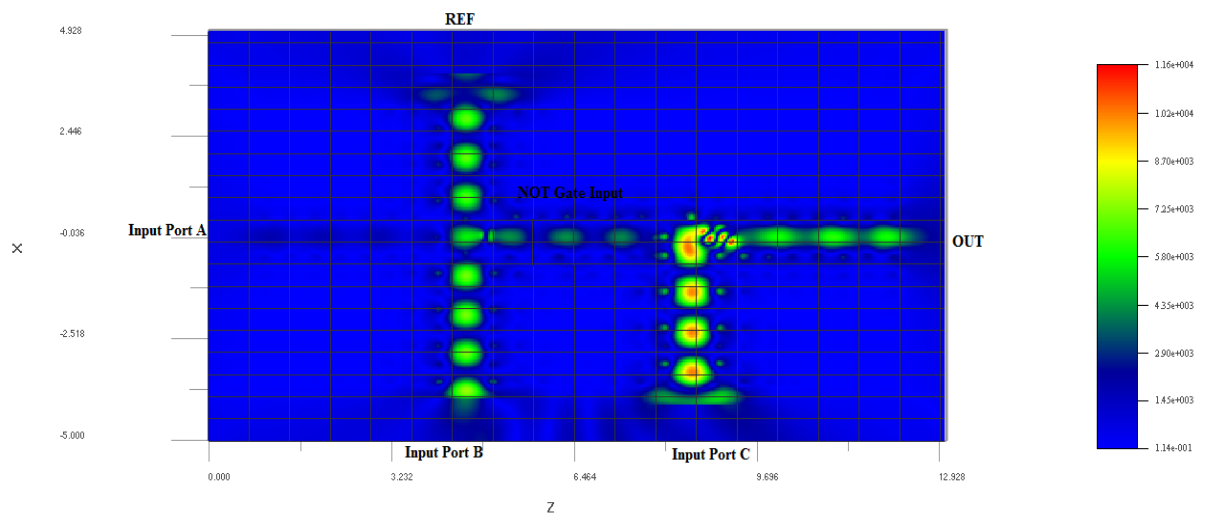
A 2D simulation is carried out to verify the functionality of NAND gate shown in Fig. 5.2. First inject the input waves through the input ports A and B. It results in logic low at the output port of NAND gate. This is because the output of logic AND gate is input of NOT gate. The NOT gate complements the output of AND gate. Physically it can be understood through the electric field distribution as shown in Fig. 5.9(a). Also, when one of input signals is launched through the input port then the output is logic high for NAND gate as shown in Fig. 5.9(b) and 5.9(c). The reference signal and input signal through the port C of NAND gate is always logic high.



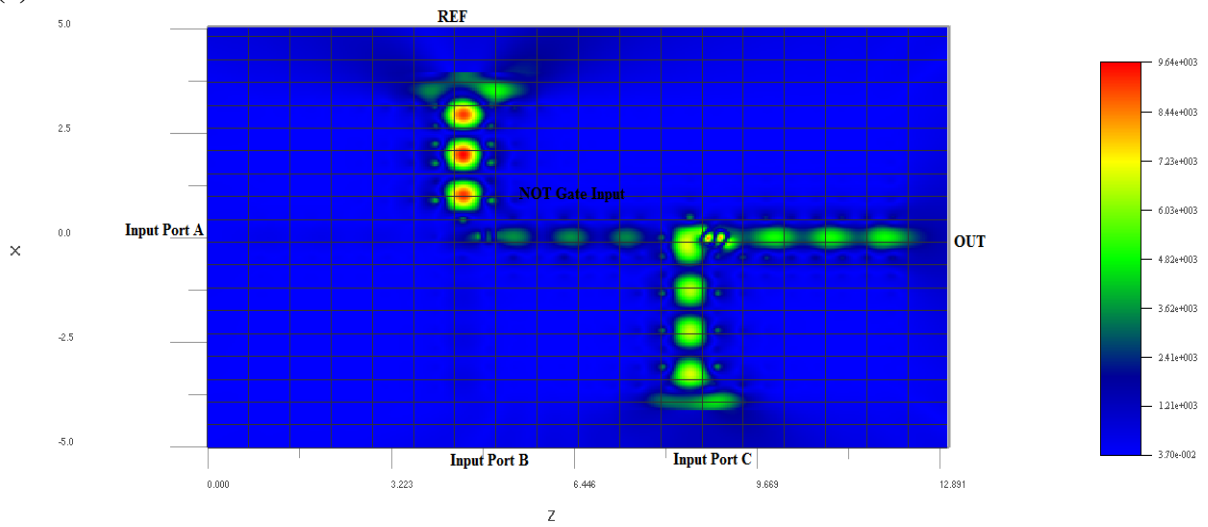
(a)



(b)



(c)



(d)

Fig. 5.9 Electric field distribution of optical logic NAND gate when (a) both the input signal are launched simultaneously (b) input signal is injected through port A (c) input signal is given through the port B (d) no input signal is injected, only reference signal is exist.

The output of logic NAND gate is high when there is no input signal at the input port (A and B) as shown in Fig 5.9(d). Only the reference signal and input signal exists at the REF port and port C respectively. The output of gate is high due to the tunnelling of wave and is low due to the interference of input signal with the reference signal. The reflection losses are however observed in the input ports. The output power of this gate is computed by FDTD method.

Input Port A	Input Port B	Logical Output	Output Power
0	0	1	$0.673P_a$
0	1	1	$0.541P_a$
1	0	1	$0.7P_a$
1	1	0	$0.004P_a$

Table 5.3 Truth table of optical logic NAND gate

The functionality of NAND gate is verified from the truth Table 5.3. It shows that the output of NAND gate is low only when both the input signals is high. The maximum output power for logic high is $0.7P_a$ and the minimum power for logic low is $0.004P_a$. Now the fabrication error tolerance of the logic NAND model (shown in Fig. 5.2) is presented for the practical applications. The radius of all the rods in the model with $\Delta\%$ error from theoretical designed parameters is assumed. The fabrication tolerance Δ can be express as follows [67]:

$$R_{error} = R_{theory} \times 1 + \Delta \quad (5.2)$$

where R_{error} is radius of each rod that has error, R_{theory} is theoretical radius of each rod and Δ is the error tolerance. The contrast ratio is calculated at the different wavelengths with different fabrication error tolerance.

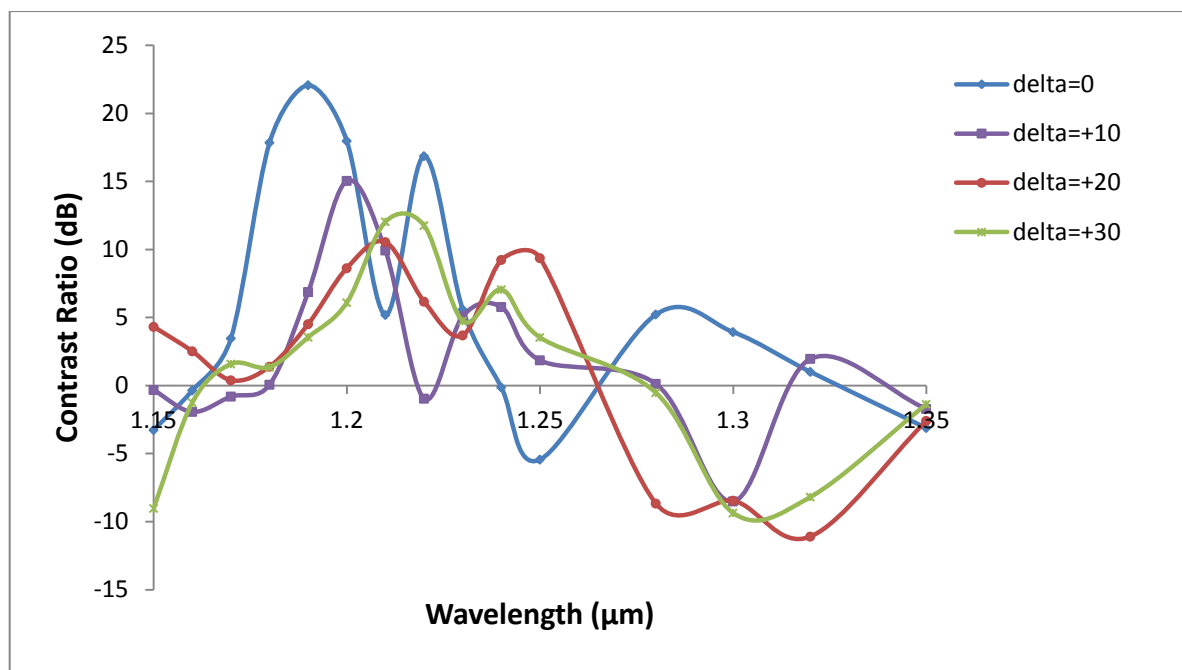


Fig. 5.10 Contrast ratio versus wavelength with different delta for optical NAND gate.

The maximum contrast ratio for $\Delta=+10\%$, $+20\%$, $+30\%$ is 15.04dB, 10.54dB and 12.04dB respectively as shown in Fig. 5.10. The fabrication error tolerance of this model exhibits better performance. The contrast ratio of the theoretical layout is 22.076dB. The radius of all rods in the layout of NAND gate can be controlled within $+10\%$ to $+30\%$ fabrication error with efficiently performance.

5.4 CONCLUSION

A design for simultaneous implementation of logic NOT and AND gate is presented to form all optical logic NAND gate. This structure is based on 2D photonic crystals. It consists of square lattice of silicon dielectric rods in air. The layout of logic NOT and AND gates are optimized individually using FDTD simulations. The contrast ratio for logic NOT gate is 11.605dB and for AND gate is 7.624dB. The size of NOT and AND structures are $10\mu\text{m} \times 10\mu\text{m}$ only. The chapter also analyzes the fabrication error tolerance for optical logic NAND gate, when radius of all rods is larger than the theoretical parameters from $+10\%$ to $+30\%$. The maximum contrast ratio for $\Delta=+10\%$, $+20\%$, $+30\%$ is 15.04dB, 10.54dB and 12.04dB respectively. The contrast ratio for theoretical designed NAND gate is 22.076dB. Since non linear material is not used, the power consumption is less so favorable for large scale integration circuits in the field of future optical communication system and optical signal processor.

CONCLUSION, RECOMMENDATION AND FUTURE SCOPE

6.1 CONCLUSION AND RECOMMENDATION

This chapter provides the summary of the research work done in this dissertation. First the conclusions have been made from this study and then the scope for the future research is discussed. The main results obtained in this thesis are concluded and summarized below:

1. A design of all optical OR logic gates based on 2D photonic crystal using silicon dielectric rods in silica is discussed. This structure efficiently acts as logic switch and behaves as logic OR gate. The structure has been simulated and analyzed by FDTD and PWE. The main advantages of this structure are the size of logic gate is small (about $20\mu\text{m} \times 20\mu\text{m}$) and it operates at $1.55\mu\text{m}$ which is fundamental third optical window. Therefore, it can be used for PIC. Also, the obtained contrast ratio is 10dB. This structure shows the possibility of designing other logic functions.
2. An optical logic NOR gate based on two different cross structures is presented. These two different cross structures are NOT and OR gate. The layout of logic NOT and OR gates are optimized individually using simulations. The contrast ratio for logic NOT gate is 11.605dB and for OR gate is 22.113dB. The size of NOT and OR structures are $10\mu\text{m} \times 10\mu\text{m}$ only. With the optimized parameters, both the gates are combined without using any external device to design the NOR gate. The operation of NOR gate is numerically demonstrated using FDTD simulation. The contrast ratio is 15.97dB for NOR gate. Since non linear material is not used, the power consumption is less. It has an operating wavelength of 40nm. This structure is favorable for large scale integration circuits in the field of logic circuits.
3. A design for simultaneous implementation of logic NOT and AND gate is presented to form all optical logic NAND gate. This structure is based on 2D photonic crystals of silicon dielectric rods in air. The layout of logic NOT and AND gates are optimized individually using FDTD simulations. The contrast ratio for logic NOT gate is 11.605dB and for AND gate is 7.624dB. The size of NOT and AND structures are $10\mu\text{m} \times 10\mu\text{m}$ only. With the optimized parameters, both

the gates are combined without using any external device to design the NAND gate. We also analyze the fabrication error tolerance for optical logic NAND gate, when radius of all rods is larger than the theoretical parameters from +10% to +30%. The maximum contrast ratio for $\Delta=+10\%$, +20%, +30% is 15.04dB, 10.54dB and 12.04dB respectively. The contrast ratio for theoretical designed NAND gate is 22.076dB. Since non linear material is not used, the power consumption is less.

6.2 FUTURE SCOPE:

During the course of this dissertation, several avenues for continuation of this study became evident. The topics which were considered worthwhile are summarized below:

1. These layouts of logic gate can be used to design complex logic circuits, future optical networks and communication system because these designs have high extinction ratio, compatible, compact size and low power consumption.
2. In this dissertation the phase difference between the input signals have not been taken into account. Simulation studies can be done for same architectures while taking into account the phase difference.
3. We have operating bandwidth around 40nm in this dissertation. This can be further reduced for improving the selectivity.

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LIST OF PUBLICATIONS:

- [1] Deeksha Rani, R. S. Kaler, “Reconfigurable design of logic OR gates based on a 2D PC waveguide structure” Communicated to Optik- International journal for light and electron.
- [2] Deeksha Rani, R. S. Kaler, Balveer Painam “All Optical NOR gate based on cross structures in 2D photonic crystal using logic NOT and OR gate” Communicated to Optik- International journal for light and electron.
- [3] Deeksha Rani, R. S. Kaler, “Design and analysis of all optical NAND gate based on 2D photonic crystal” Communicated to Fiber and Integrated Optics.