DESIGN OF PARTIALLY DEPLETED SOI MOSFET FOR LOW POWER APPLICATION

Thesis submitted in partial fulfillment of the requirements
for the award of degree of

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in
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June, 2011

CERTIFICATE

I hereby certify that the work which is being presented in this thesis entitled **"Design of Partially Depleted SOI MOSFET for Low Power Application"**, is an authentic record of my own work carried out as the requirements for the award of degree of Master of Technology in VLSI Design & CAD at Thapar University, Patiala under the guidance of **Mr. Arun Kumar Chatterjee**, Assistant Professor, Electronics and Communication Engineering Department, Thapar University.

The matter presented in this thesis has not been submitted in any other University/Institute for the award of any degree.

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(Shiva Agrawal)

ABSTRACT

Performance, area and power consumption is a critical concern in today's VLSI system design. Therefore, Silicon-on-insulator wafers are used in semiconductor device applications. Silicon-on-insulator is used for a variety of applications in power switching device, semiconductor memories, high-speed bipolar circuits and micro-electro-mechanical system etc.

In this thesis work, 90nm bulk-Si MOSFET, partially depleted SOI MOSFET with lightly doped drain implantation and partially depleted SOI MOSFET with lightly doped drain and halo implantation has been simulated using Atlas and Athena module of Silvaco tool. SOI technology is well discussed in terms of its structure, advantages, characteristics, short channel effects and fabrication techniques etc.

At 90nm, electrical characteristics of bulk-Si MOSFET, partially depleted SOI MOSFET with lightly doped drain implantation and partially depleted SOI MOSFET with lightly doped drain and halo implantation has been found out. Effect of different parameters such as gate oxide thickness, channel doping and halo implantation on threshold voltage and off current of partially depleted SOI MOSFET has been studied.

Further, a capacitorless 1T DRAM cell has been designed using 90nm partially depleted SOI MOSFET with lightly doped drain implantation. Also, working of capacitorless 1T DRAM using partially depleted SOI MOSFET as access transistor has been shown.

Leakage current in partially depleted SOI with lightly doped drain implantation has been reduced by using process technique, called halo implantation. The leakage current in partially depleted SOI MOSFET with lightly doped drain and halo implantation has been reduced by about 90% as compared to partially depleted SOI MOSFET with lightly doped drain implantation.

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LIST OF SYMBOLS

I_D	Drain current	A
V_{gs}	Gate-source voltage	V
V_{ds}	Drain-source voltage	V
Q	Magnitude of electronic Charge	C
$\emptyset_B$	Barrier potential	eV
K	Boltzmann's constant	J/K
T	Absolute temperature	K
t_d	Time delay	s
t_{rd}	Rise time of drain pulse	s
t_{rG}	Rise time of gate pulse	s
V_{DD}	Supply voltage	V
I_{GIDL}	GIDL current	A
E_s	Electric field in the gate-drain overlap region	V/cm
m^*	Electron effective mass	g
E_g	Energy gap of semiconductor	eV
$\hbar$	Planck constant	Js
Q_B	Effective depletion region charge	C
Q_{B0}	Depletion region charge	C
d_{bs}	Depletion region width of the source	µm
d_{bd}	Depletion region width of the drain	µm
L	Effective channel length	µm
ε_s	Permittivity of silicon	F/cm
N_A	Acceptor concentration	cm^{-3}
V_{db}	Drain-body voltage	V
V_{sb}	Source-body voltage	V
ϕ_0	Surface potential of two terminal MOSFET structure in strong inversion	V
V_{th}	Effective threshold voltage	V
V_{FB}	Flat band voltage	V
ΔV_{TL}	Change in threshold voltage due to short channel effect	V
t_{ox}	Oxide thickness	Å
ε_{ox}	Permittivity of SiO_2	F/cm

I_{off}	Off current	nA

LIST OF ABBREVIATIONS

RAM	Random Access Memory
DRAM	Dynamic Random Access Memory
SRAM	Static Random Access Memory
SOI	Silicon-on-Insulator
MOSFET	Metal Oxide Semiconductor Field Effect Transistor
PD	Partially Depleted
LDD	Lightly Doped Drain
FBC	Floating Body Cell
ZRAM	Zero Capacitor Random Access Memory
GIDL	Gate Induced Drain Leakage
BOX	Buried Oxide
TFT	Thin-Film Transistors
FD	Fully Depleted
LSI	Large Scale Integration
DIBL	Drain Induced Barrier Lowering
GP	Ground Plane
DIVSB	Drain Induced Virtual Substrate Biasing
SOS	Silicon-on-Sapphire
SIMOX	Separation by Implantation of Oxygen
PACE	Plasma-Assisted Chemical Etching
ELTRAN	Epitaxial Layer Transfer

CHAPTER

1 INTRODUCTION

Semiconductor memories are the most vital microelectronic component of digital logic system design, such as computers and microprocessor-based applications etc. Therefore, advancement in the fabrication of semiconductor memories includes process enhancement and technology development through the scaling for higher densities and faster speeds.

Semiconductor memory is classified according to the type of data storage and data access. Read/write memory allows the modification of data bits stored in the memory array, as well as their reading on demand, called Random Access Memory (RAM). The data stored in RAM is volatile i.e., the stored data is lost when the power supply voltage is turned off. RAM is classified into two main categories. Dynamic Random Access memory (DRAM) and Static Random Access memory (SRAM) [1].

In DRAM charge is stored on a capacitor to represent data values of a logic "low" or logic "high". These are called DRAMs rather than SRAMs because the stored charge leaks away even with the power continuously applied. Therefore, the cells must be read and refreshed at periodic intervals. Despite this, the DRAMs have advantages of cost per bit and high density that have made them the most widely used semiconductor memories in commercial applications [2].

As, the DRAM cell has been scaled down in size for technology developments, the minimum amount of stored charge needed to maintain reliable memory operation. Therefore, for scaling to higher densities, it is necessary that the cell's storage capacity will be increased. Although the planar storage capacitors is used in most 1-Mb designs, stacked and trench capacitors is developed for the 4Mb to 64Mb designs to achieve the DRAM cells with larger capacitance values without increasing the area these cells occupy on the chip surface [2]. As further, scaling of three dimensional cells (trench cell and stack cell) is not possible and data retention time is the most important characteristic of DRAM. These days the focus is on increase the data

retention time, reduced junction leakage current for realizing long retention time. It is found that new technology devices like capacitorless SOI (Silicon-on-Insulator) DRAM cell (1T DRAM) can overcome the problem of scaling and reduced junction leakage current.

1.1 Need to Minimize Leakage

To achieve high density, better performance and low power consumption, Complementary Metal Oxide Semiconductor devices have been scaled for more than 30 years. Due to scaling supply voltage has been scaled down in order to keep the power consumption under control but at the same time, the threshold voltage scaling results in the increase of the subthreshold leakage current. Now the leakage current is become an important fraction of the total power dissipation of integrated circuit. Therefore, there is need to reduce the leakage current.

In DRAM retention time must be longer. The retention time is the time from when the capacitor stores the data until it is read out. The retention time specifications have become more demanding for each successive DRAM generation. Battery-operated equipments such as laptops, cellular phones, Personal digital assistants, digital wristwatches, pacemakers and cellular phones etc require longer retention time to reduce power consumption. Retention time is dependent on the weakest cell, which loses the stored data due to leakage currents before it can be refreshed. Due to scaling, the electric field in memory cells become stronger, this increases leakage current and causing poor retention characteristic [3]. Therefore, to reduce leakage current various solutions has been proposed.

1.2 Why SOI

To integrate more and more transistor into a single Integrated Circuit, the concept of “More Moore” is applied to the scaling of horizontal and vertical physical feature size of CMOS transistors. In 1965, Gordon E. Moore predicts that the number of transistors is approximately doubled every two years without correspondingly increases the cost of the chips. The scaling of CMOS transistors is limited to 22nm because of physics boundaries. Furthermore, the concern is not only about the inability of the devices itself to continue operate steadily but also the constraints from

the economic and technology point of view [4]. There are some points, which clear why SOI is preferred over CMOS.

(1) Physical challenges- These are due to the increment of tunneling and leakage currents as the devices are becoming smaller, this impacts the performance and functionality of CMOS devices.

(2) Material challenges- These basically come from the inability of the dielectric and wiring materials to provide reliable insulation and conduction, respectively with continued scaling.

(3) Power-thermal challenges- As the number of transistors integrated per unit-area increases and this requires larger power consumption and higher thermal dissipation.

(4) Technological challenges- CMOS transistors are basically patterned on wafer by means of lithography and masks. Therefore, lithography-based techniques have to improve to provide the resolution below the wavelength of the light to manufacture to CMOS devices.

(5) Economical challenges- These are due to the rising in cost of production, fab, and testing that may reach a point where it will be not affordable from economic point of view.

There are also other problems in bulk-Si such as- carrier mobility is decreasing due to impurity scattering, the gate tunnelling current is increasing as the gate insulator becomes thinner, and the pn junction leakage is increasing as the junction becomes shallower. To resolve this problem a new technology called SOI has been proposed.

SOI technology has many unique characteristics such as low capacitance, high speed operation; they also include good radiation hardness, ability to withstand high temperatures, and ability to handle high voltages. Due to many advantages of SOI a 1T DRAM cell is realized by SOI MOSFET (Metal Oxide Semiconductor Field Effect Transistor) [5].

1.3 Objective

The objective of this thesis work is to simulate the bulk-Si MOSFET, PD (Partially Depleted) SOI MOSFET with LDD (Lightly Doped Drain) implantation and PD SOI MOSFET with LDD and halo implantation both. The main aim of this thesis work is

to reduce leakage current to 10pA in PD SOI MOSFET. The proposed physical parameters to achieve this aim are given in Table 1.1.

Table 1.1
Proposed physical parameters for the design
of 90nm PD SOI nMOSFET

Physical parameters	Value
Technology node	90nm
Minimum supply voltage	0.9-1.2V
Gate length	90nm
Thickness of Si layer	100nm
Thickness of BOX	400nm
Gate oxide thickness	3nm
Threshold voltage	0.25V

1.4 Report Organization

This thesis report contains five chapters.

The second chapter encloses the literature review which discusses the DRAM cells, SOI structure, advantages, disadvantages and other relevant topics that describes the SOI technology.

The third Chapter encloses the steps of fabrication process for bulk-Si MOSFET, PD SOI MOSFET with LDD implantation and PD SOI MOSFET with LDD and halo implantation using Athena module of Silvaco tool.

In fourth chapter results are discussed. By Plotting graphs of I_D (drain current) vs. V_{gs} (gate voltage), log I_D vs. V_{gs} and I_D vs. V_{dS} (drain voltage), electrical behaviour of bulk-Si MOSFET, PD SOI MOSFET with LDD implantation, PD SOI MOSFET with LDD and halo implantation is discussed. In PD SOI MOSFET, the effect of different parameters such as gate oxide thickness, channel doping and halo implantation on threshold voltage and off current is discussed.

The fifth chapter summarizes all the work of this thesis and presents the scope for the future related to this thesis work.

CHAPTER

2 LITERATURE REVIEW

2.1 Introduction to DRAM Cells

Memory cell size has been reduced to be one-third for each DRAM generation in volume production to absorb die size increase and it is well described by Figure 2.1, Figure 2.2 [6]. Figure 2.3 Shows development of DRAM cell design from four-transistor (4T) cell to one-transistor (1T) cell. One-transistor (1T) and one capacitor cell is the simplest cell [1]. Capacitor is used to store binary information, 1 (high voltage) or 0 (low voltage) and a transistor to access the capacitor. Binary data (voltage) stored in the capacitor cell is degraded mostly due to a junction leakage current at the storage node. Therefore, the cell data must be read and rewritten periodically (refresh operation) even when memory arrays are not accessed.

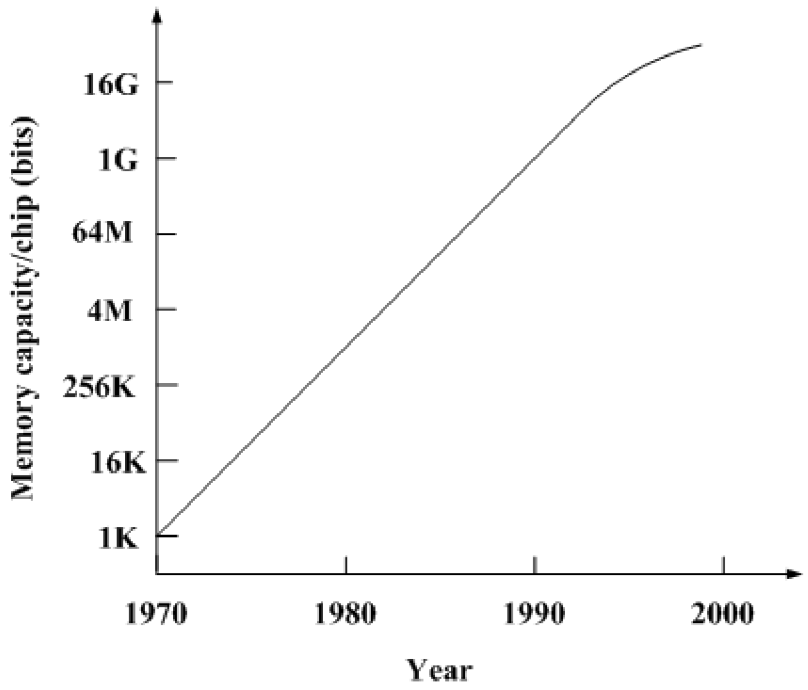


Figure 2.1: Trends in the memory capacity of DRAMs [6]

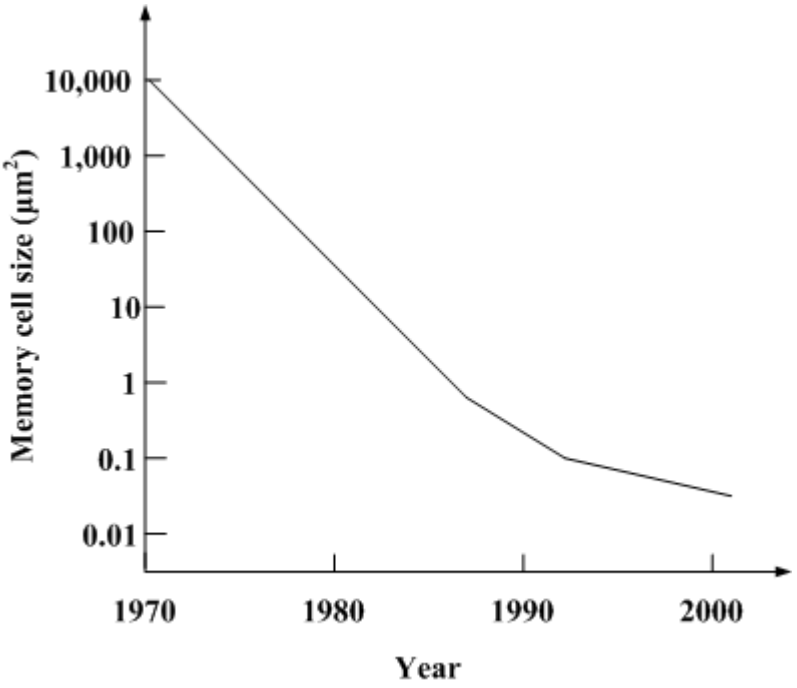


Figure 2.2: Trends in the memory cell size of DRAMs [6]

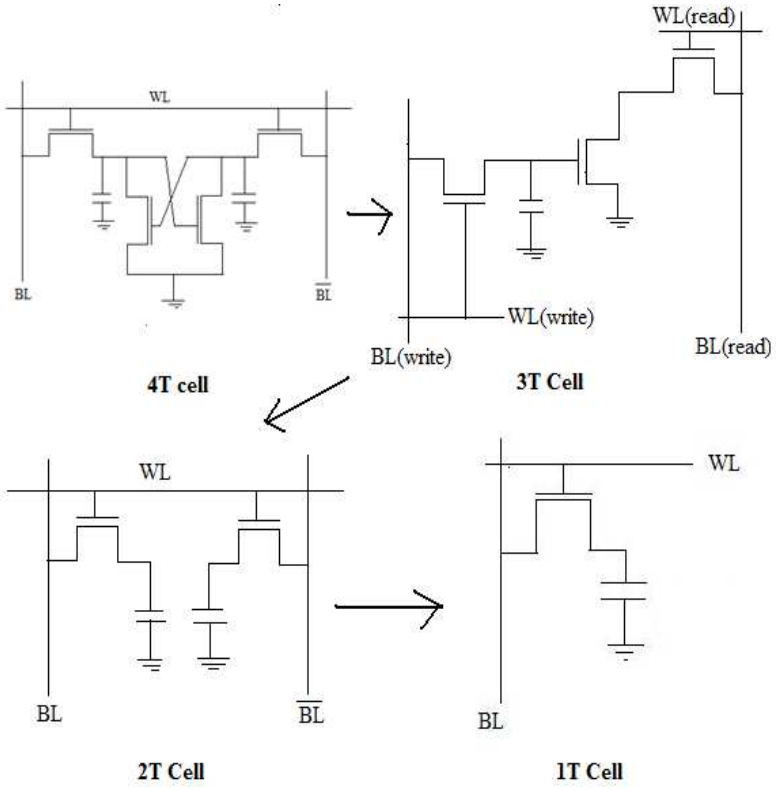


Figure 2.3: Various configuration of DRAM cell [1]

1T DRAM cell consists of a storage capacitor and a MOSFET transistor use as a transfer device that acts as a switch as shown in Figure 2.4. Word lines controls the gate of transfer MOSFET transistor and the bit lines are connected to sense amplifiers. If the capacitor is charge it indicates a logical “1” and if it is discharge it indicates a logical “0”.

When word line goes high MOSFET transistor turns “on” and acts as pass transistor, now capacitor is connected to bit line and the information stored in the capacitor in the form of voltage appears on the bit line. Difference of voltage on the bit line is sensed by sense amplifier. DRAM Cells are arranged in the form of arrays in which rows (word lines) and columns (bit lines) are orthogonal to each other.

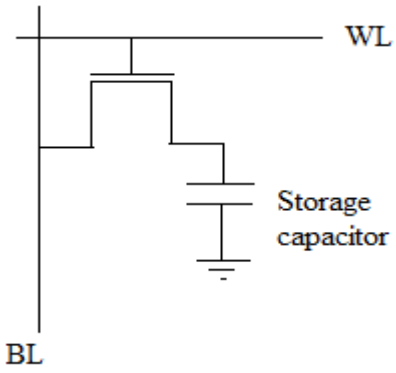


Figure 2.4: One transistor DRAM cell [1]

During the past 15 years, DRAM cell size has decreased from 34μm^2 for 1MB to 0.25μm^2 for 1GB. This rapid evolution is described in two stages: the era of the planar cell capacitor from 16KB to 1MB and the era of three dimensional cells (trench cell and stack cell) from 4MB to 1GB [2].

2.2 Advanced DRAM Cells

1. Floating Body Cell (FBC) for 1T DRAM

For the formation of 1T DRAM cell, floating body cell consist of a Partially Depleted (PD) SOI nMOSFET as shown in Figure 2.5. For write operation, the source of the PD SOI nMOSFET is biased to 0 V, the drain is connected to a bit line and the gate is connected to a word line. To write data “1” the nMOSFET is operated in saturation

region leading to impact ionization. To write data “0”, the p-n junction between the body and the drain is forward-biased. To read the data, the nMOSFET is operated in a linear ohmic region. The difference in drain current of write “1” and write “0” can be read and sensed [7].

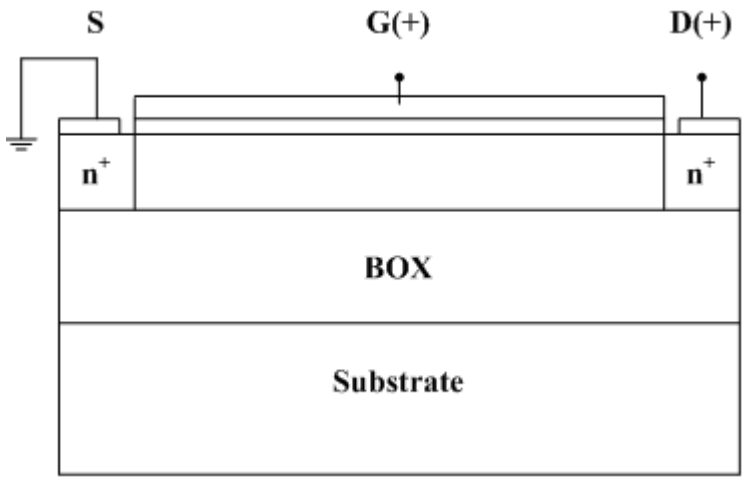


Figure 2.5: PD SOI nMOSFET [7]

2. Zero Capacitor RAM (Z-RAM)

The memories base on floating body principle use MOSFET transistor to pass current and create charge in the body using impact ionization. The amount of charge create with this technique is insufficient to create a robust and manufacturable memory device. A superior approach is used called Z-RAM. Intrinsic bipolar transistor in the PD SOI MOSFET is used to create charge as shown in Figure 2.6. If SOI nMOSFET is used as a memory device, source, body, drain acts as emitter, base and collector respectively, to form npn bipolar transistor. The body of the SOI nMOSFET is the base of the bipolar transistor and acts as a storage node. To write “1” intrinsic bipolar transistor is “on” causing current to flow throughout the transistor body. In this mechanism charge collects at the interface due to the slight bias at the gate. The impact-ionization effect creates an excess of majority carriers in the floating body which is more efficient in this bipolar bit-cell structure. This effect charges the body quickly and therefore results in fast write operations. For read operation, sense amplifier senses the bipolar current through the transistor [8].

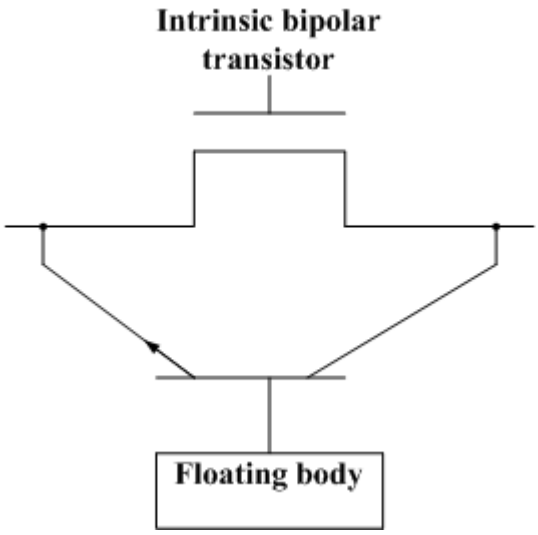


Figure 2.6: Intrinsic bipolar transistor in PD SOI nMOSFET [8]

3. Capacitorless 1T DRAM using Gate Induced Drain Leakage (GIDL) Current

All of the IT-DRAM cells discussed, use impact ionization current for write operation. For fast writing operation in memory cell impact ionization current will be high. But high impact ionization current degrades device reliability because of simultaneous hot-carrier injection into the gate dielectric. A new design of 1T DRAM is proposed that uses GIDL current for write operation as shown in Figure 2.7. To write "1" negative voltage is applied on gate terminal and positive voltage to drain terminal. At the same time, due to band-to-band tunnelling electrons flow to the drain and the generated holes to the floating body and accumulates there. The source current increases because of accumulated holes in the body and the resultant threshold voltage change. To write "0" pn junction consisting of the body and drain is forward bias by applying positive voltage at gate and negative voltage at drain. Source current decreases because of lack of holes in floating body. The difference in write "1" and write "0" current is sensed and read as shown in Figure 2.7(c) [9].

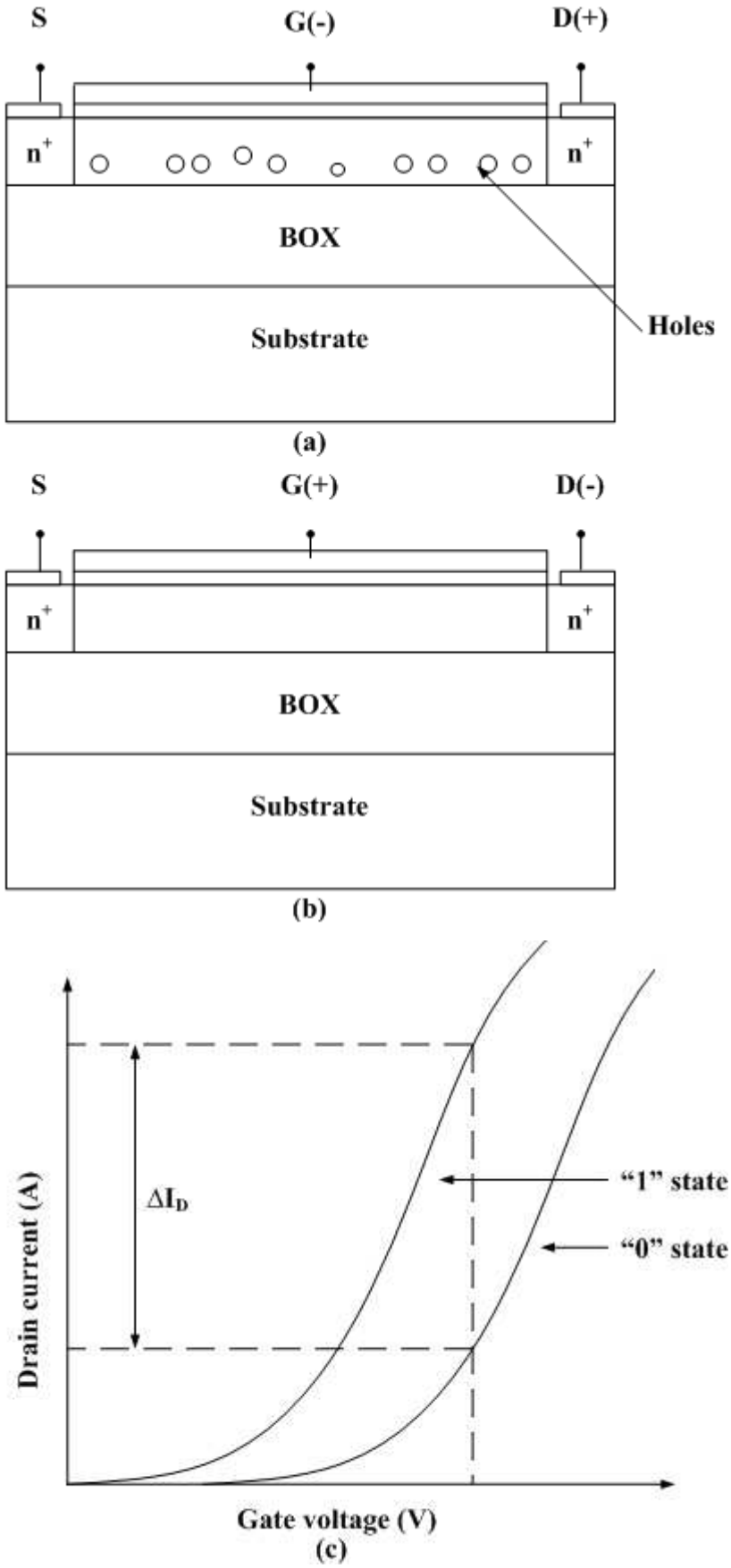


Figure 2.7: 1T DRAM cell **(a) Write "1" operation (b) Write "0" operation** (c) **Drain current difference between write "1" and write "0"** [9]

2.3 SOI Structure

SOI structure is different from bulk-Si MOSFET structure. SOI Structure has the layer of silicon dioxide just below the surface, which is called the Buried Oxide (BOX) and is made by the oxidation of Si or oxygen implantation into Si. If the thin Si film on the BOX is of single crystal, then the MOSFET made in it are called SOI devices; but if it is polycrystalline, then they are called Thin-Film Transistors (TFT). This film above the BOX is called the top Si layer, the SOI layer, or Si film. The Si substrate beneath the BOX is called Si substrate or supporting substrate, handle wafer, or base wafer. The terms "Si body" and "SOI body" refer to the part of the SOI layer that constitutes the body of a MOSFET [5]. The structure of bulk-Si and SOI substrates is shown in Figure 2.8.

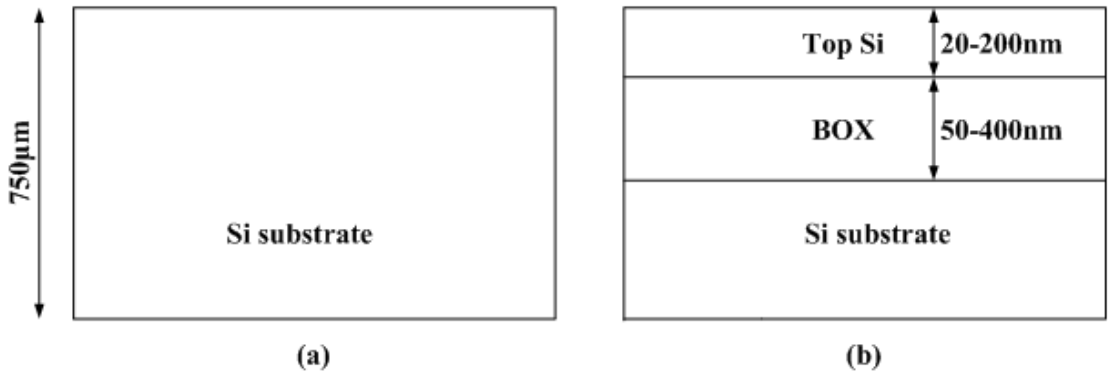


Figure 2.8: Structure of (a) Bulk- Si substrate (b) SOI substrate [5]

2.4 Types of SOI

On the basis of thickness of the SOI layer there are two types of SOI devices-

(1) Fully Depleted SOI (FD SOI)

(2) Partially Depleted SOI (PD SOI)

The thickness of the SOI layer for an FD SOI MOSFET is usually set to about one-third the effective channel length in order to avoid a punch-through current. So, the SOI layer is much thinner in FD SOI than in PD SOI devices.

1. Fully Depleted SOI

In an nMOSFET transistor, when a positive gate voltage is applied it depletes P-type carriers in body and induces an n-type inversion channel on the surface of the body. If

the insulated layer of silicon is made very thin, full layer gets depleted. A technology based on this principle is called a "fully depleted" SOI technology [10]. Fully depleted SOI structure is shown in Figure 2.9.

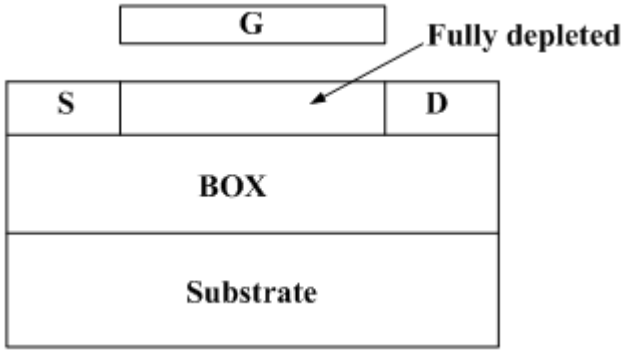


Figure 2.9: Fully-depleted SOI [5]

2. Partially Depleted SOI

If the insulated layer of silicon is made thicker, then the inversion region does not extend the full depth of the body. A technology based on this principle is called a "partially depleted" SOI technology [10]. Partially depleted SOI structure is shown in Figure 2.10.

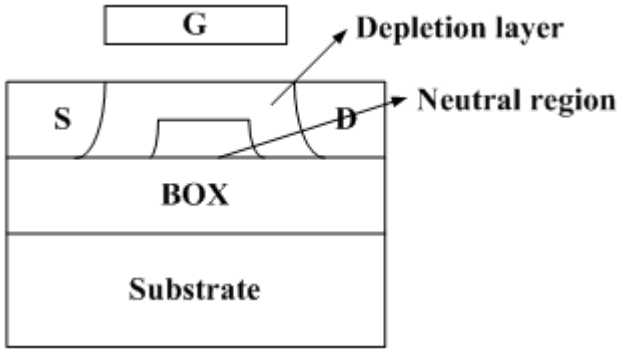


Figure 2.10: Partially depleted SOI [5]

2.5 Advantages of SOI

SOI MOSFET has many advantages over bulk-Si MOSFET. These are as-

1. Negligible Drain-to-Substrate Capacitance

In SOI devices, the capacitance between the drain (source) and the substrate is negligibly small because of the dielectric constant of SiO_2, which is lower than that of

Si and the thickness of the BOX. This improves the switching speed of CMOS devices [5]. Schematic diagram of the capacitances in bulk-Si and SOI is shown in Figure 2.11.

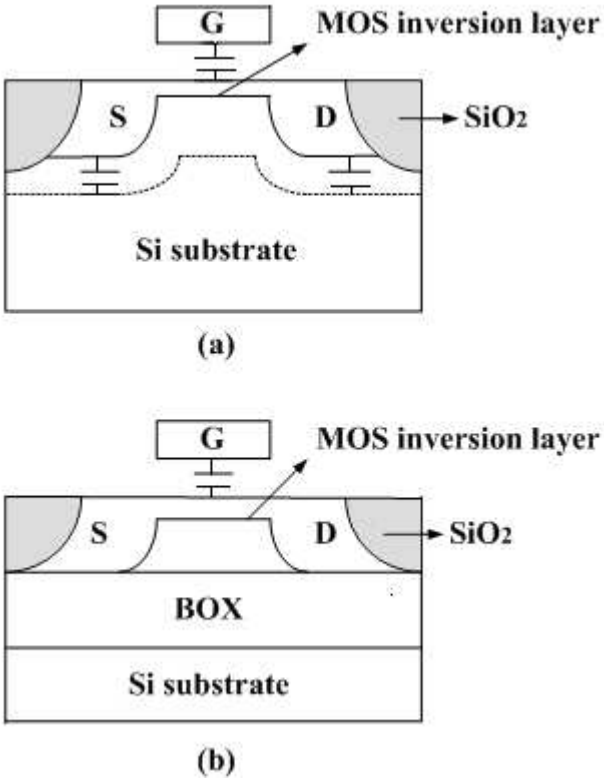


Figure 2.11: Capacitances of (a) bulk-Si MOSFET
(b) SOI MOSFET [5]

2. Positive Body Bias Improves Speed of Stacked Gates

The independent body bias of SOI MOSFET makes them faster in a stacked gate structure. In the stacked gates made with bulk-Si MOSFET in Figure 2.12, the negative body bias of the circled transistor is generated by the current flowing to the ground. This increases the threshold voltage and lowers the operating speed. In contrast, the body bias of stacked SOI MOSFET is positive because it takes a value between the source and drain biases. This yields a lower threshold voltage for stacked transistors, thereby enhancing the operating speed [5].

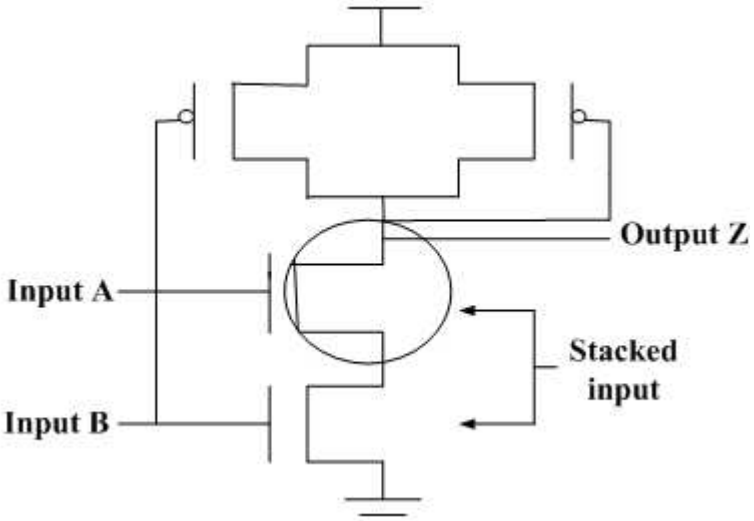


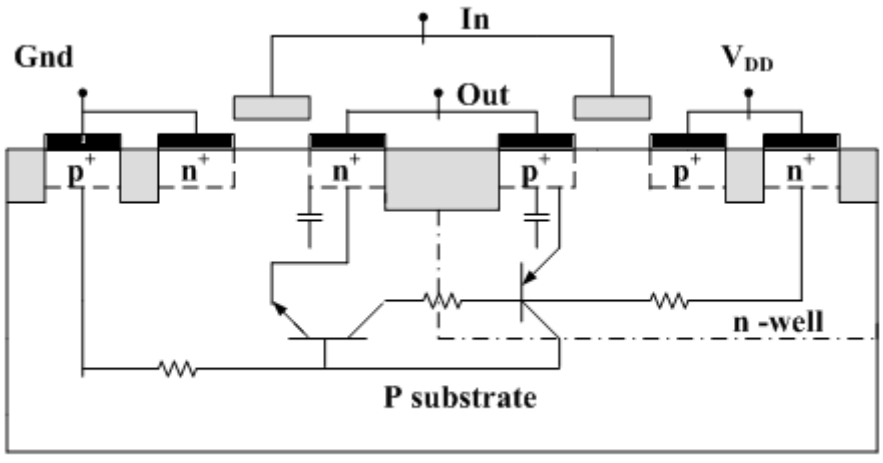
Figure 2.12: Stacked gates using bulk-Si MOSFET [5]

3. No Latch-Up

Latch-up occurs when the parasitic p-n-p-n (or n-p-n-p) thyristor in a CMOS structure turns on, which limits the maximum operating voltage. Figure 2.13 shows that, unlike a bulk-Si device, there is no parasitic thyristor in an SOI device [5].

4. Ideal Device Isolation and Smaller Layout Area

SOI devices are laterally isolated from each other by an insulator film and vertically isolated from the substrate by the BOX, which makes the isolation ideal. As a result, devices can be packed closer together than bulk ones. In addition, the n^+ and p^+ diffusion regions at the output of a CMOS inverter can be connected directly to each other, as shown in Figure 2.13, which makes the area of a device smaller than that of a bulk one [5].



(a)

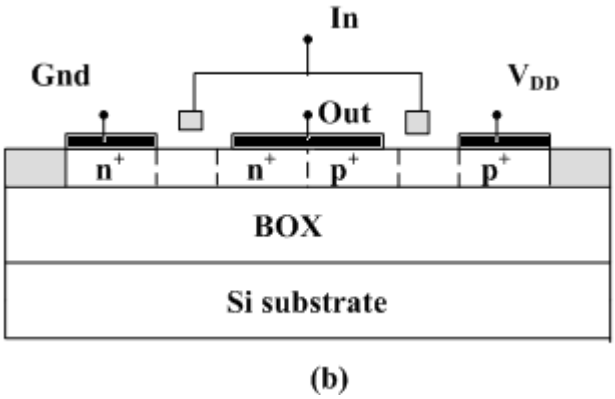


Figure 2.13: (a) Bulk-Si CMOS (b) SOI CMOS [5]

5. Good Soft-Error Immunity

SOI devices exhibit excellent radiation hardness to alpha particles, neutrons and other particles. Alpha particles are generated by trace amounts of radioactive elements in IC materials. They have energy of approximately 5MeV, which enables them to penetrate Si to a depth of about 25μm. Along the trajectory, they generate electron-hole pairs which results in negative and positive charges of around 10fC in every micron. This is sufficient to destroy the memory charge of a DRAM cell or upset the memory state of an SRAM neutrons generated by secondary cosmic rays also induce soft errors [5].

6. Small pn Junction Leakage

The leakage current of a pn junction is smaller in an SOI structure because the impurities in the n^+ and p^+ regions diffuse deeply into the thin Si film, leaving a pn junction only at the sidewall of the diffused area. A low pn junction leakage current is generally beneficial in every type of application but it is important in applications requiring a low stand-by power such as mobile phones and personal digital assistants, because it prolongs battery life [5].

2.6 Basic Characteristics of SOI MOSFET

1. Kink Effect

PD SOI devices exhibit a “kink” effect which is a sharp rise in drain current as the drain voltage increases at a fixed gate voltage. The drain current-voltage characteristics of FD SOI and PD SOI nMOSFET are shown in Figure 2.14.

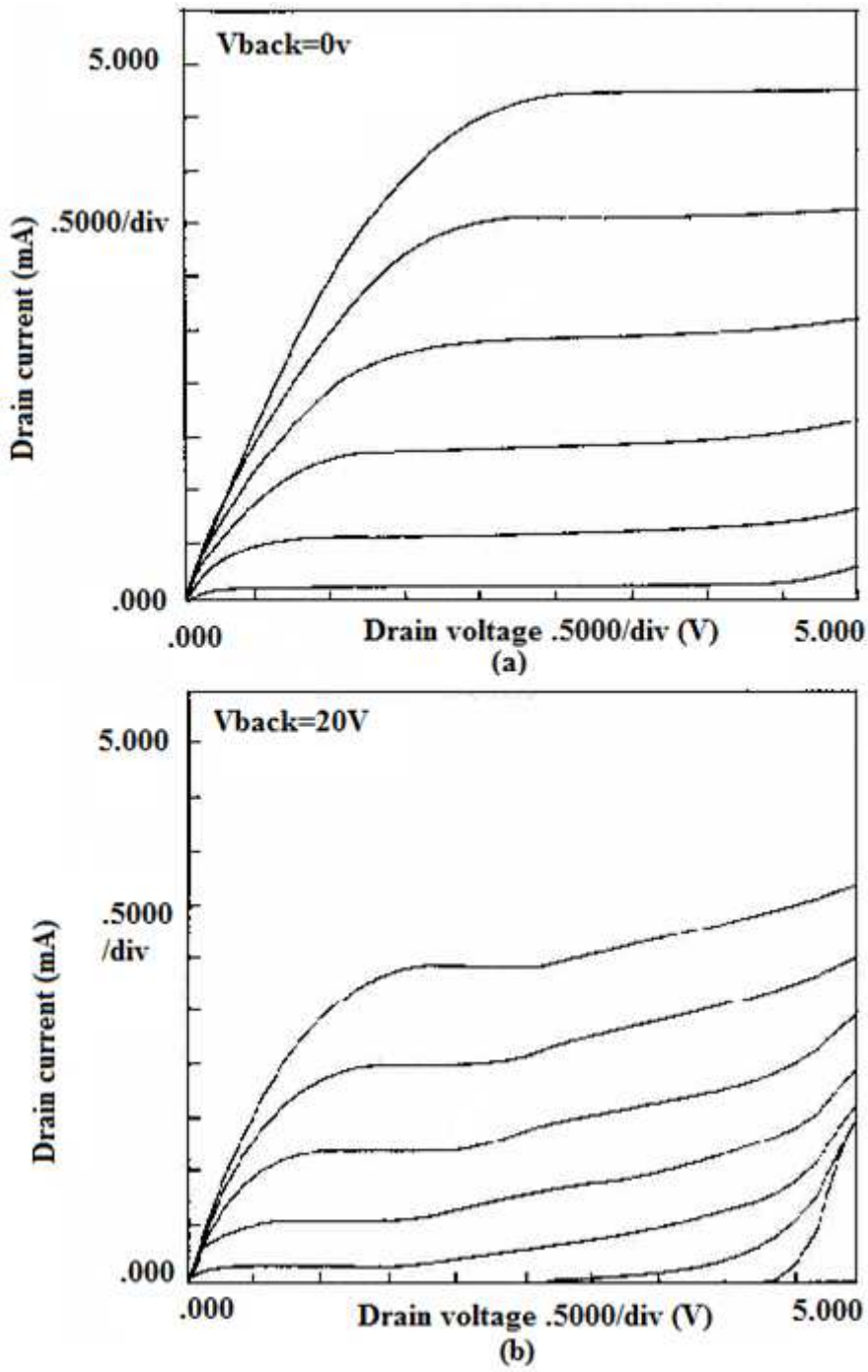


Figure 2.14: Drain current-voltage characteristics of
(a) FD SOI nMOSFET (b) PD SOI nMOSFET [5]

The kink effect denotes an abrupt increase in the saturation current of the partially depleted SOI MOSFET working in strong inversion. In the saturation region, the channel carriers generate pairs (electron/hole) through impact ionization at the drain due to high electric field. The minority carriers are collected by the drain, whereas the majority carriers cross the source and give rise to the gradual charge stored in the substrate. Concomitant increase in substrate potential induces a lowering of threshold

voltage and source potential barrier. Due to this reason much of the minority carriers will be able to diffuse source towards the channel. This is positive feedback. A sudden increase in the drain current is called the kink effect. The Kink is the most important effect in the SOI MOSFET [11].

FD SOI devices do not exhibit kink effect. In an FD SOI device, the potential barrier to holes at the source end is small, even deep within the body region, because the body region is depleted all the way down to the bottom. As a result, there is little accumulation of holes in this region, so a kink cannot appear [5].

2. Steep Subthreshold Slope in FD SOI MOSFET

Steep subthreshold characteristics are an important feature of FD SOI MOSFET. Figure 2.15 shows typical subthreshold characteristics of FD SOI and bulk-Si MOSFET (and PD SOI MOSFET). FD SOI devices have steeper subthreshold characteristics than bulk or PD SOI devices, with subthreshold swing being close to the limiting value. FD SOI devices have steeper subthreshold slope because, for a given change in gate voltage, the channel surface potential changes more in an FD SOI device than in bulk or PD SOI devices.

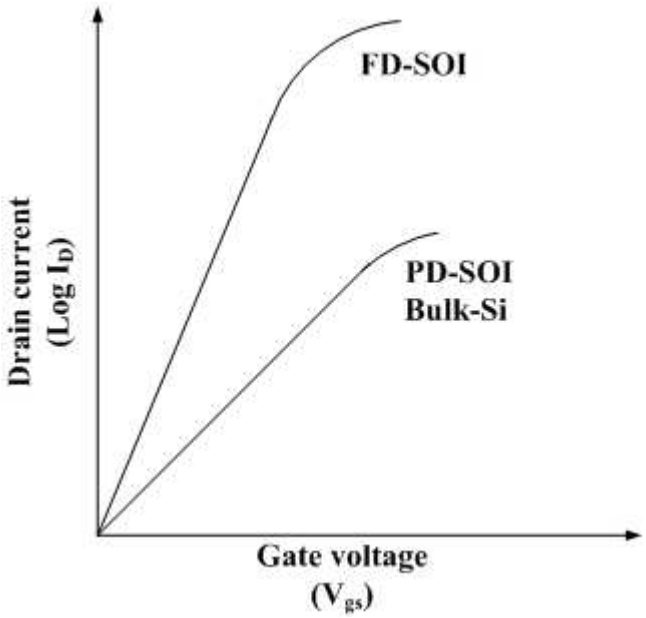


Figure 2.15: Subthreshold characteristics of FD SOI, PD SOI and bulk-Si MOSFET [5]

The subthreshold swing of an FD SOI device is close to 60mV/dec at room temperature, which is the limiting value for MOSFET. The subthreshold characteristics are the drain current vs. gate voltage (I_D vs.V_{gs}) characteristics at gate voltages below the threshold voltage. In this region, the drain current increases exponentially with gate voltage because it is proportional to the number of carriers with enough thermal energy to cross the potential barrier between the source and channel, as shown in the equation 2.1 [5].

$$I_D = \beta \exp\left(\frac{-q\emptyset_B}{KT}\right) \quad \text{..... (2.1)}$$

where β is constant of proportionality and $\emptyset_B$ is the barrier potential.

3. Dynamic Floating-Body Effects

Since an SOI device is fully isolated, the body potential is not fixed and changes for a variety of reasons. The effects brought about by these changes are collectively referred to as floating body effects. The main causes of changes in body potential are impact ionization and majority carrier redistribution in the body region, which occur as the gate and drain voltages, switch between high and low levels.

(a) Effect of Impact Ionization

For the nMOSFET in Figure 2.16, some of the holes generated by impact ionization in the high-electric-field region near the drain accumulate in the body region and raise the body potential to a positive value.

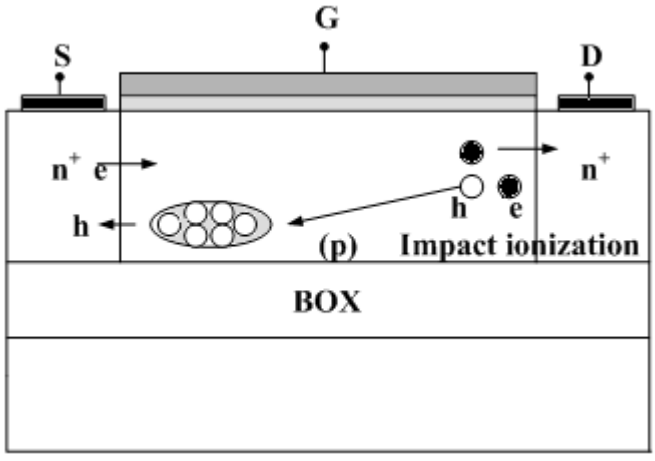


Figure 2.16: Floating body effects due to impact ionization [5]

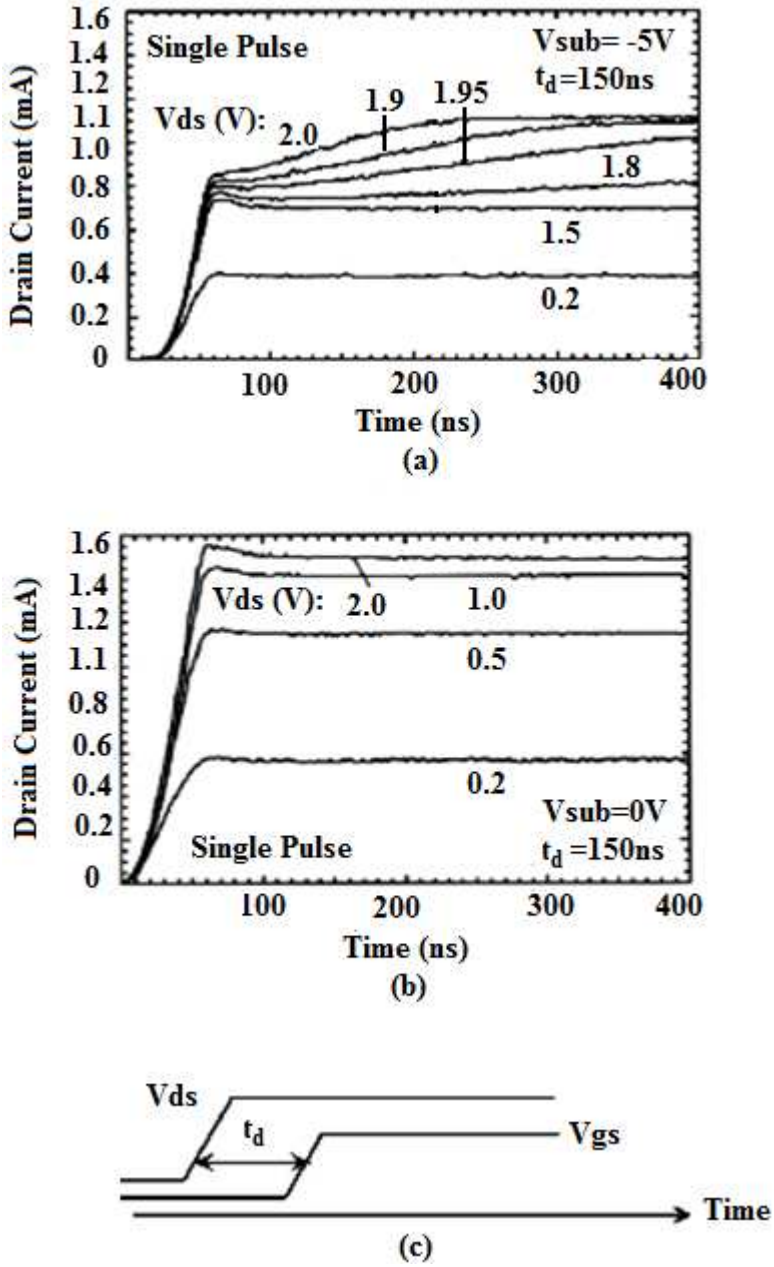


Figure 2.17: Impact ionization in (a) PD SOI MOSFET (b) FD SOI MOSFET (c) Input gate and drain pulse [5]

Figure 2.17(a) and (b) shows drain current waveforms for PD SOI and FD SOI devices, respectively, when a single pulse is applied to the drain, followed by a single pulse to the gate after a time delay of t_d as explained in Figure 2.17(c), with the height of the drain pulse as a parameter. The height of the drain pulse is varied from 0.2V to 2V. The drain pulse had a rise time (t_{rd}) of 100 ns; and the gate pulse has a height of 1V and a rise time (t_{rG}) of 50 ns. As shown in Figure 2.17(a), the drain current of the PD SOI device exhibits transient characteristics immediately after the rising edge of the gate pulse when the drain voltage is 1.5V or more and the drain current saturates

in a shorter time as the drain voltage increases. At drain voltages of 1.5V and above, impact ionization generates a significant number of holes and the number becomes larger at higher drain voltages. Accordingly, as the drain voltage increases, the holes pile up faster in the body region and the threshold voltage drops at a faster rate, causing the increase in drain current to take place sooner. In this way, differences in the number of holes generated during the operation of a PD SOI device give rise to differences in the rate at which holes accumulate in the body region, which appear as differences in the transient characteristics.

On the other hand, no such transient characteristics are observed in FD SOI devices, as shown in Figure 2.17(b). Thus, at voltages for which impact ionization occurs, a PD SOI MOSFET exhibits complex behaviour that depends on the pulse conditions, while an FD SOI MOSFET tends to be stable. This difference arises because the entire body region of an FD SOI device is depleted, which makes the potential barrier to holes between the source and body region smaller than in a PD SOI device, thereby allowing fewer holes to accumulate in the body region [5].

(b) Effects of Majority Carrier Redistribution

Figure 2.18 illustrates phenomena of majority carrier redistribution in a PD SOI nMOSFET. When the gate voltage changes from the low to the high level, the channel depletion layer grows wider, driving away the holes (majority carriers) that it encounters along the way. The holes accumulate at the bottom of the body region and raise the body potential to a positive value. Since the source junction is forward-biased, the holes then flow out towards the source. Next, when the gate returns to the low level, holes are needed to make the channel depletion layer narrower so that a neutral region can form. But since the holes have already flowed out, there is a shortage, which creates negative body potential that causes holes to be supplied from the source as a reverse biased junction current. In this way, the body potential varies due to the shortage of holes in the body region arising from the outflow and supply of holes at the source junction and the expulsion and restoration of holes due to the growth and contraction of the channel depletion layer.

In addition, since similar phenomena are associated with the growth and contraction of the drain depletion layer as the drain changes between high and low levels, the body potential of devices operating in an LSI (Large Scale Integration) exhibits

complex behaviour. The phenomena associated with majority carrier redistribution cause problems only in PD SOI MOSFET, while in principle, they do not occur in FD SOI devices because the entire body region is always depleted [5].

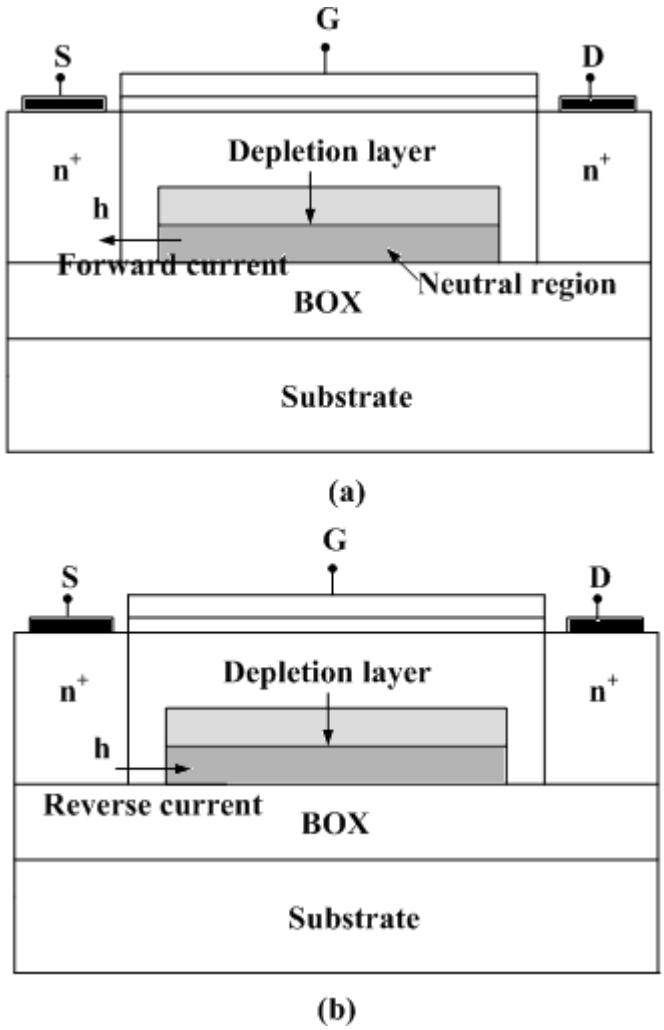


Figure 2.18: Majority carrier redistribution in PD SOI MOSFET [5]

4. Parasitic Bipolar Effects in FD SOI MOSFET

A major part of the appeal of FD SOI MOSFET is that they suppress the kink in the drain current-voltage characteristics without using a body terminal. But although a kink does not appear, the devices are still susceptible to a kind of floating-body effect known as parasitic bipolar effects. These effects occur when the source, body, and drain of MOSFET act as the emitter, base, and collector of parasitic transistors in which the base current consists of majority carriers produced by impact ionization. Since the body region is more depleted in FD SOI than in PD SOI devices, the

injection efficiency of the emitter of the parasitic bipolar transistors is higher, which makes these effects more likely to occur. When they occur, they have a number of consequences, such as a reduction in the breakdown voltage between the source and drain, abnormally steep subthreshold characteristics beyond the theoretical limit, a larger off current and a smaller threshold voltage [5].

Suppressing parasitic bipolar effects in FD SOI devices entails:
(1) Suppressing the generation of majority carriers by impact ionization
(2) Reducing the injection efficiency of the emitter of parasitic bipolar transistors
(3) Lowering the transport efficiency with which minority carriers injected into the base are conveyed to the collector [5].

5. Self-Heating Effects

The thermal conductivity of the silicon oxide film typically used for the buried insulator is 1.4 W/m/K, which is two orders of magnitude smaller than that of Si (140 W/m/K). As a result, the Joule heat generated by the drain current cannot easily escape through the BOX and the substrate. This gives rise to self-heating, which raises the channel temperature.

A large amount of Joule heat is generated in the saturation region, where the drain voltage and current are both large and the resulting increase in temperature reduces the drain current by lowering the carrier mobility, and may lead to the appearance of a differential negative resistance in the drain current-voltage characteristics. Accordingly, different drain current-voltage characteristics may be obtained when measuring the steady-state drain current with a DC supply and when measuring the drain current with a pulse supply, which causes less heating and is thus less likely to induce self-heating, even under the same drain and gate bias conditions [5].

2.7 Short Channel Effects in SOI MOSFET

Short channel effects also occur in SOI devices as the technology starts to shrink. Short channel effects in SOI MOSFET are discussed below.

1. Gate Induced Drain Leakage (GIDL) Current

When the zero or negative voltage is applied at gate terminal and positive voltage is applied at drain terminal as shown in Figure 2.19(a), a depletion region is formed

underneath the gate near drain-side overlap region. Due to biasing of gate holes are accumulated at the surface, this forms the depletion layer narrower at the surface. When the gate is more negative bias (i.e., gate terminal is at zero or negative and drain terminal is at V_{DD}), the n^+ drain region under the gate is depleted and inverted as shown in Figure 2.19(b). This causes in field crowding which results in increase of high field effects such as avalanche multiplication and band-to-band tunnelling. As a result of all these effects, minority carriers are emitted in the drain region underneath the gate. Since the substrate is at lower potential for minority carriers, the minority carriers that have been accumulated or formed at the drain depletion region underneath the gate are swept laterally to the body, completing a path for GIDL current [12].

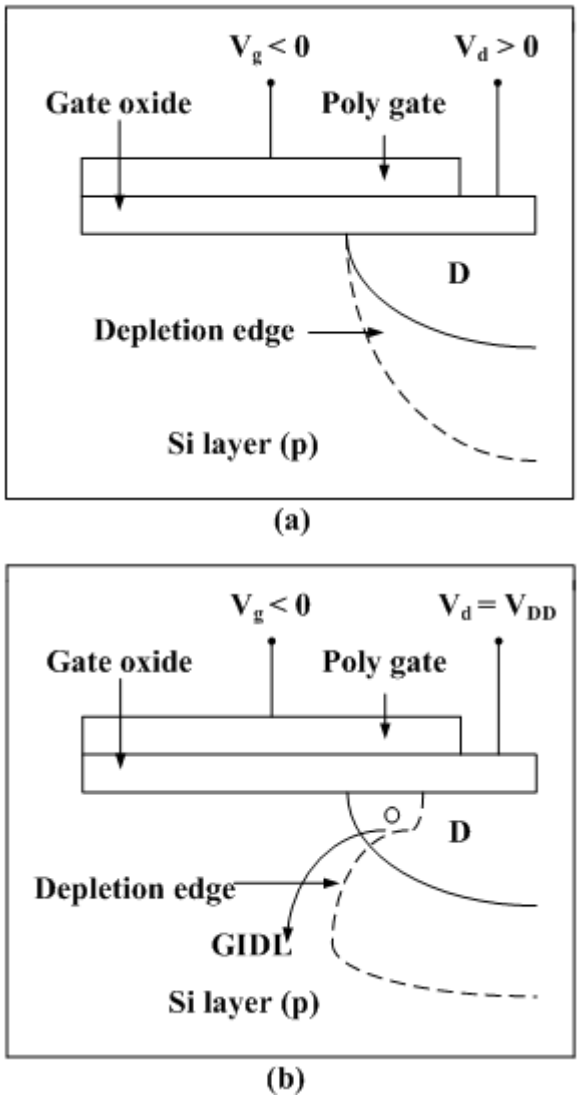


Figure 2.19: GIDL current phenomenon (a) When gate bias is low negative (b) When gate bias is high negative [12]

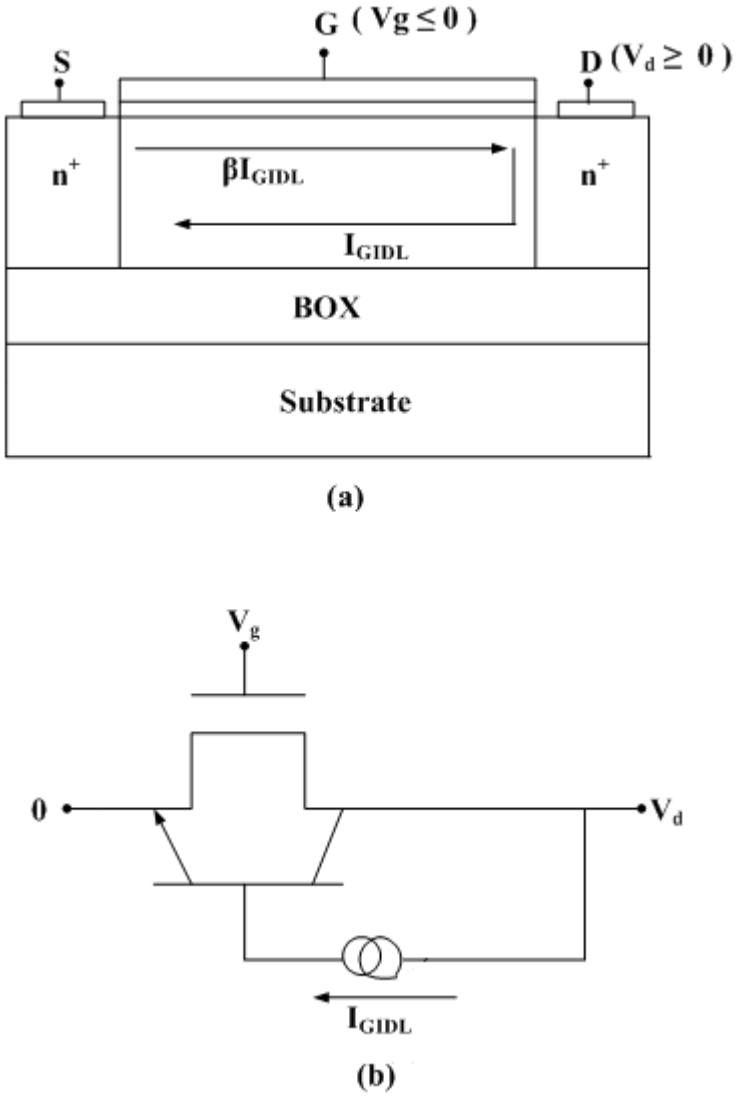


Figure 2.20: (a) GIDL current in SOI nMOSFET
(b) Equivalent lumped circuit [13]

Holes accumulated in the channel turns on the parasitic bipolar transistor which is formed in the channel. In this case source-channel junction form emitter-base junction where as drain behaves like collector as shown in Figure 2.20. When the parasitic bipolar transistor turns "on", the source-channel junction becomes forward biased and electrons starts to flow from source to channel and electrons are collected by the drain and cause the amplification of GIDL current (βI_{GIDL}). Equation 2.2 shows the GIDL current [14].

$$I_{GIDL} = AE_s e\left(\frac{B}{E_s}\right) \quad \text{..... (2.2)}$$

where-

$$A = \frac{q^2(0.2m^*)^{1/2}}{1.8\pi\hbar^2\left(E_g\right)^{3/2}}$$

$$B = \frac{\pi(0.2m^*)^{1/2}E_g{}^{3/2}2\pi}{2\sqrt{2}q\hbar} = 21.3MV/cm$$

I_{GIDL}= GIDL current

E_s= Electric field in the gate-drain overlap region

q = Magnitude of electric charge

m^*= Effective mass of electron

E_g= Energy gap of semiconductor

$\hbar$= Planck constant

According to equation 2.2 in order to limit GIDL, the electric field in the gate-drain overlap region must be limited. GIDL current is reduced by increasing oxide thickness only in the critical region where GIDL occurs.

2. Drain Induced Barrier Lowering (DIBL)

In long-channel devices, the threshold voltage is independent of the channel length and the voltage applied on the drain terminal. While in short-channel devices, the threshold voltage and subthreshold current vary with the voltage applied on the drain terminal.

When drain voltage (V_{ds}) is increased, the depletion width around the drain will widen. As the depletion region of the drain starts to widen, this effect will starts to decrease $|Q_B|$ thus further decreases V_{th}. Thus short-channel devices, V_{th} decrease as V_{ds} increases [15]. The effective charge Q_B is calculated in equation 2.3.

$$\frac{Q_B}{Q_{B0}} = 1 - \beta_1 \frac{1}{L}\frac{d_{bs}+d_{bd}}{2} \quad \text{..... (2.3)}$$

where-

Q_B = Effective depletion region charge

Q_{B0} = Depletion region charge

d_{bs} = Depletion region width of the source

d_{bd} = Depletion region width of the drain

CHAPTER

3 DESIGN OF PD SOI MOSFETs

3.1 Design of 90nm Bulk-Si MOSFET

A 90nm bulk-Si nMOSFET is simulated on Athena. The steps to design 90nm bulk-Si nMOSFET are described here. The physical parameters for the 90nm nMOSFET are defined in the Table 3.1.

Table 3.1
Physical parameters for the design of
90nm bulk-Si nMOSFET

Physical parameters	Value
Technology node	90nm
Minimum supply voltage	0.9-1.2V
Gate length	90nm
Substrate doping	Boron dose $=1\times10^{13}cm^{-3}$
Gate oxide thickness	2.8nm
V_t adjust implant	Boron dose $=9.5\times10^{10}$ cm^{-3}
Polysilicon deposit	200nm
LDD Implant	Phosphorus dose $=10\times10^{11}$ cm^{-3}
Source/drain doping	Arsenic dose $=40\times10^{15}$ cm^{-3}

(1) Substrate doping-

The first step in the design of nMOSFET in Athena is the specification of initial rectangular grid, and then the silicon substrate is doped with boron concentration of $10^{13}cm^{-3}$ as shown in Figure 3.1. Silicon doping is adjusted by dose, energy parameters.

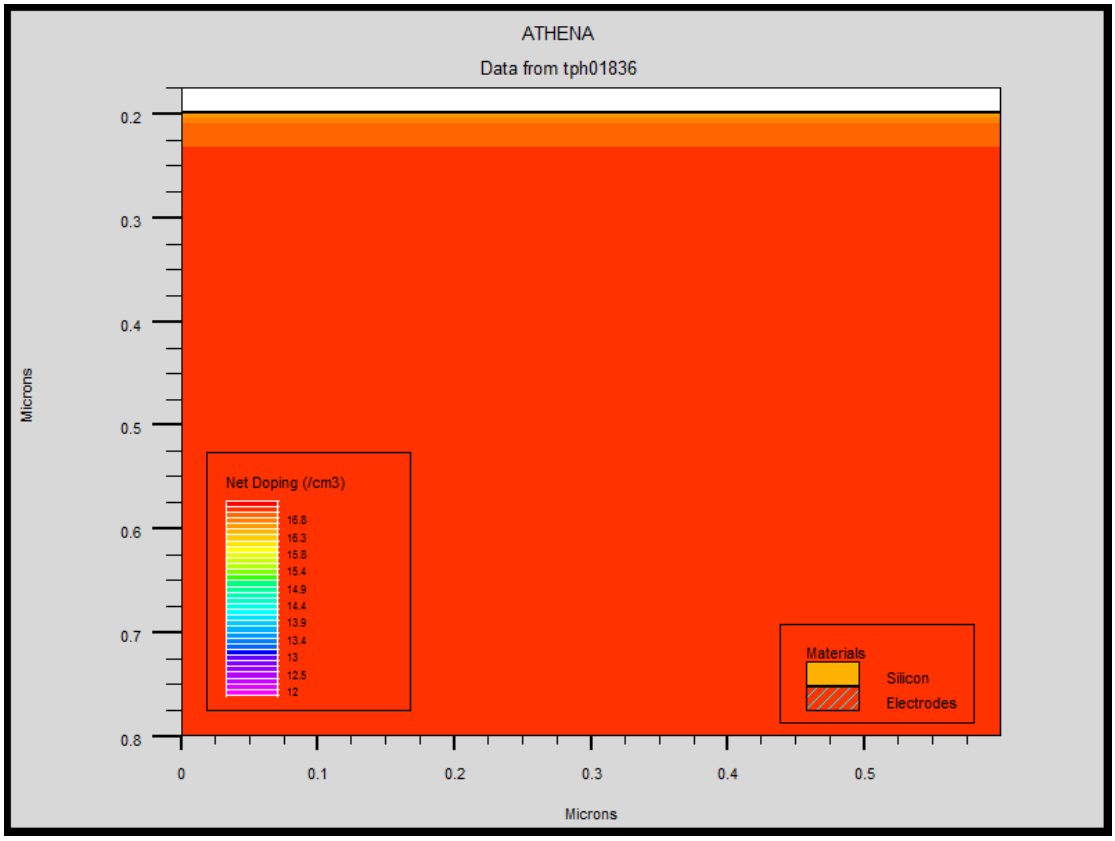


Figure 3.1: Doping in silicon substrate

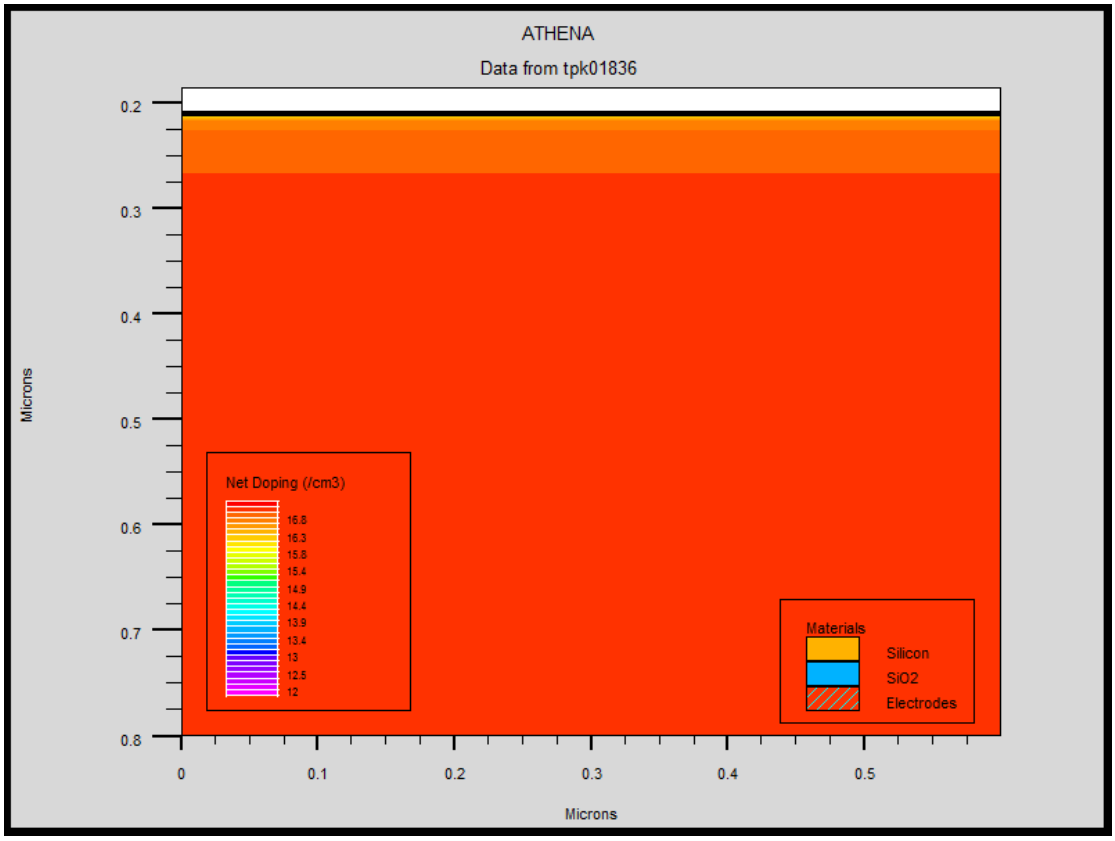


Figure 3.2: Gate oxidation

(2) Gate oxidation-

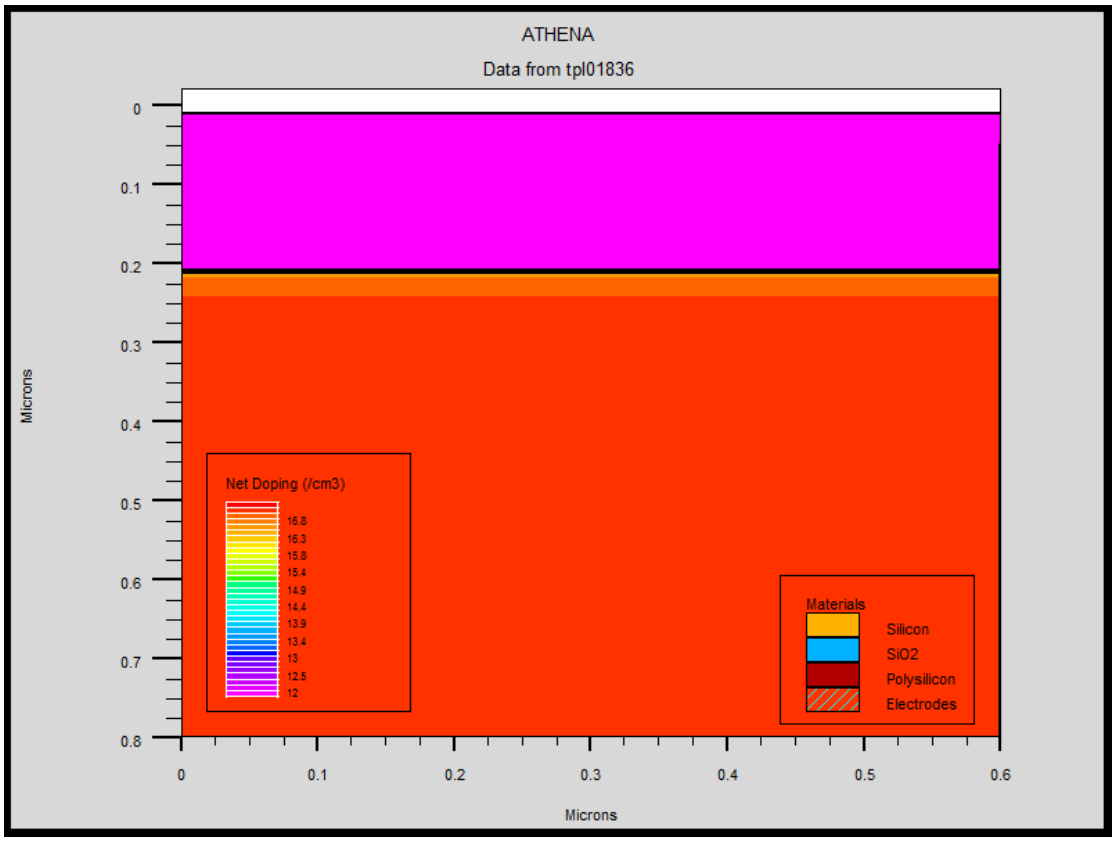
After the formation of silicon substrate, SiO_2 layer is formed over Si substrate. Thickness of gate oxide layer is defined by parameters time, pressure, and temperature. Figure 3.2 shows the formation of gate oxide layer over Si substrate.

(3) V_t adjust implant and polysilicon gate formation-

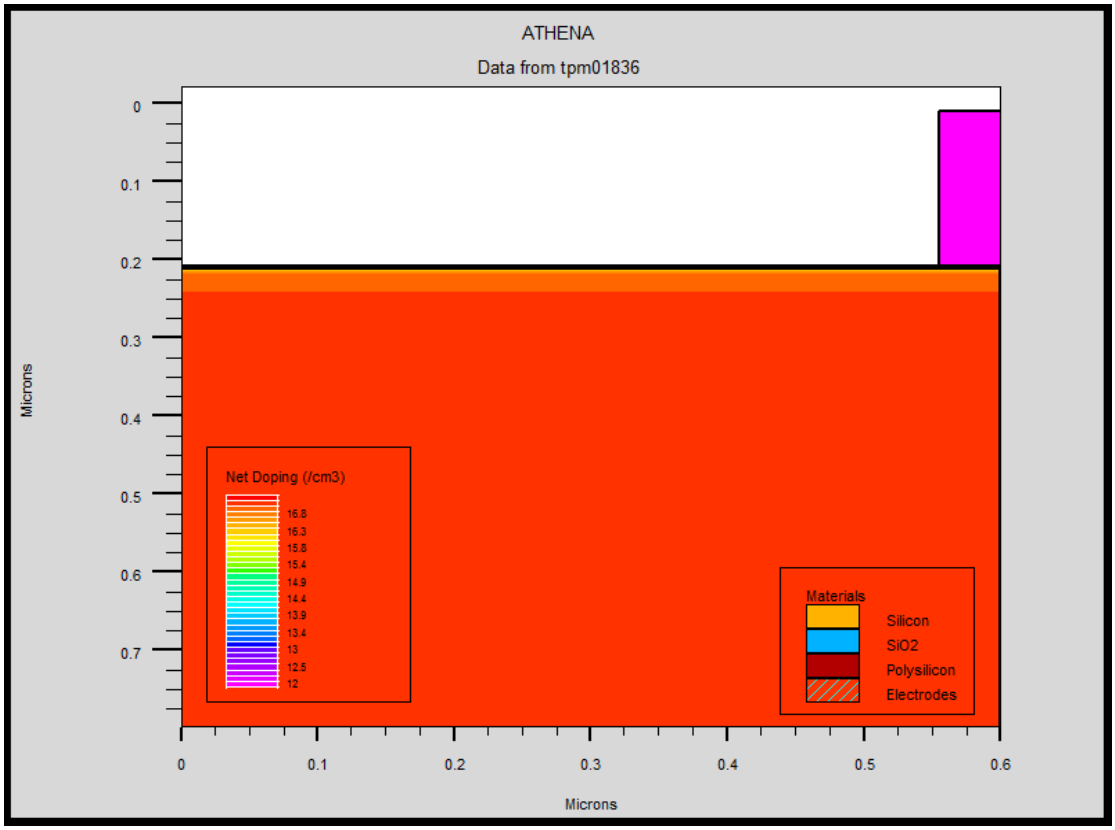
Threshold voltage is adjusted by implanting the required dose of boron at proper energy. Gate formation is done after the gate oxide layer formation. The layer is then etched until half the desired gate length left as shown in Figure 3.3.

(4) Polysilicon oxidation-

Design of polysilicon oxidation is shown in Figure 3.4.



(a)



(b)

Figure 3.3: Gate formation with (a) Polysilicon deposition (b) Deposited polysilicon etched

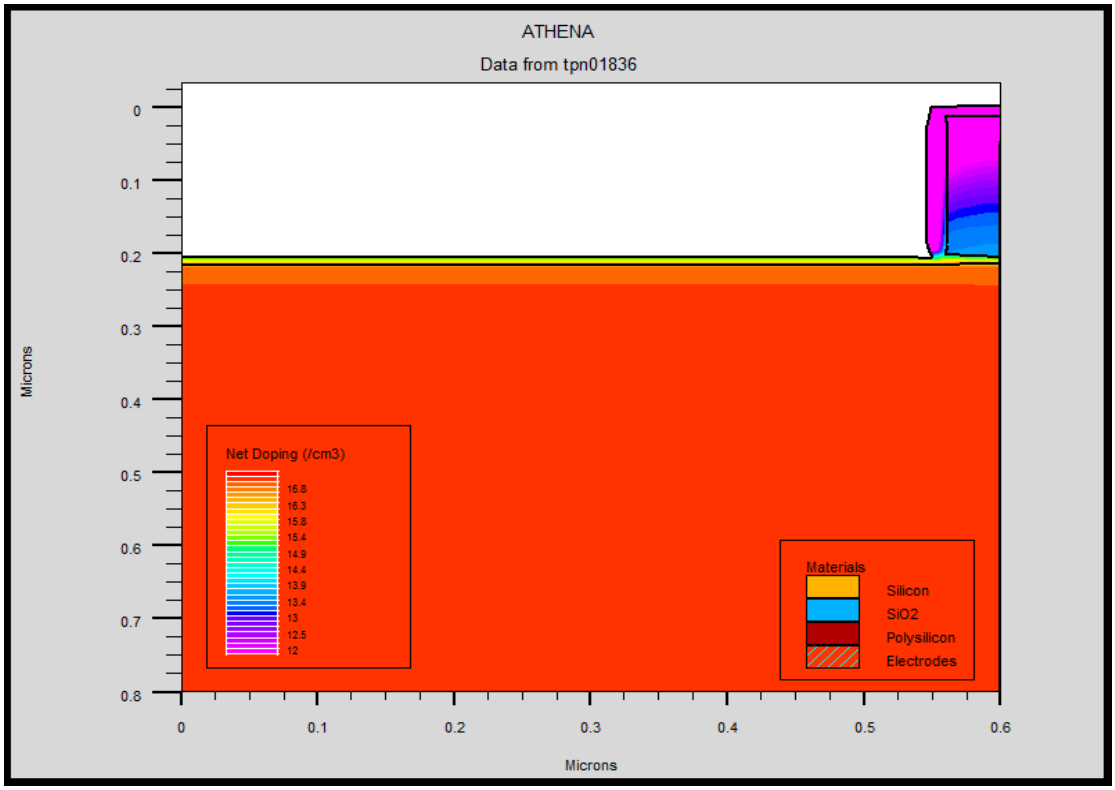


Figure 3.4: Polysilicon oxidation

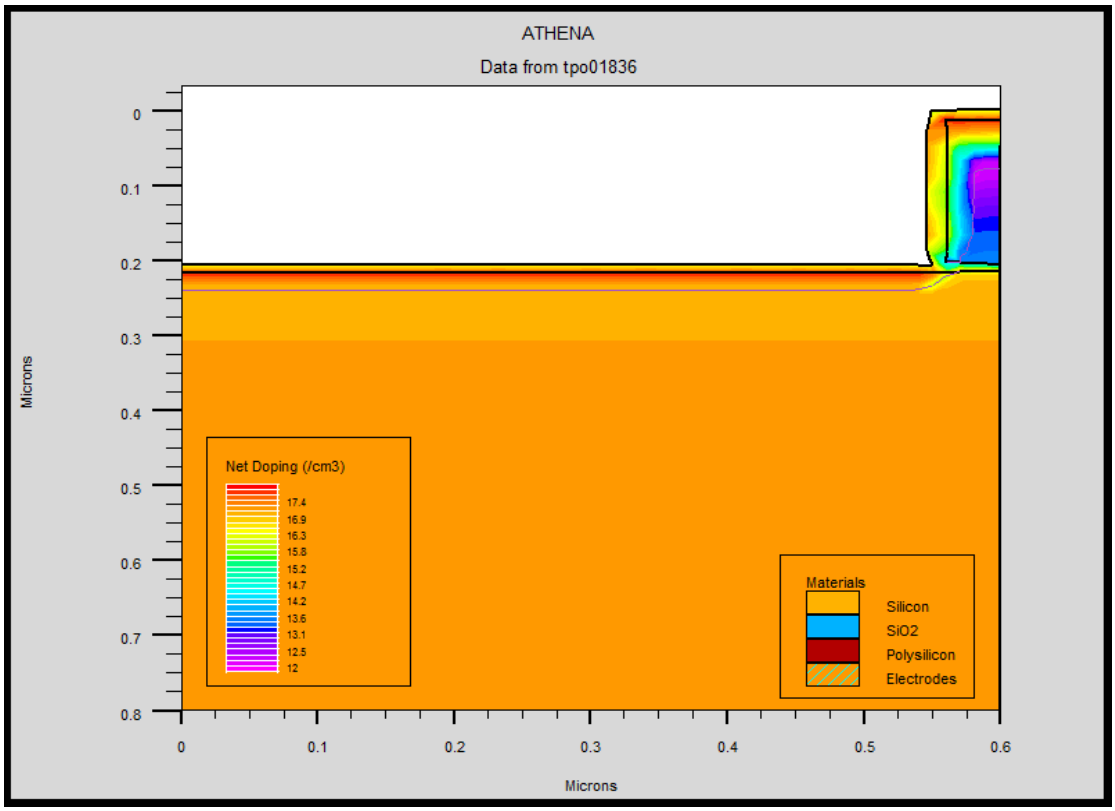
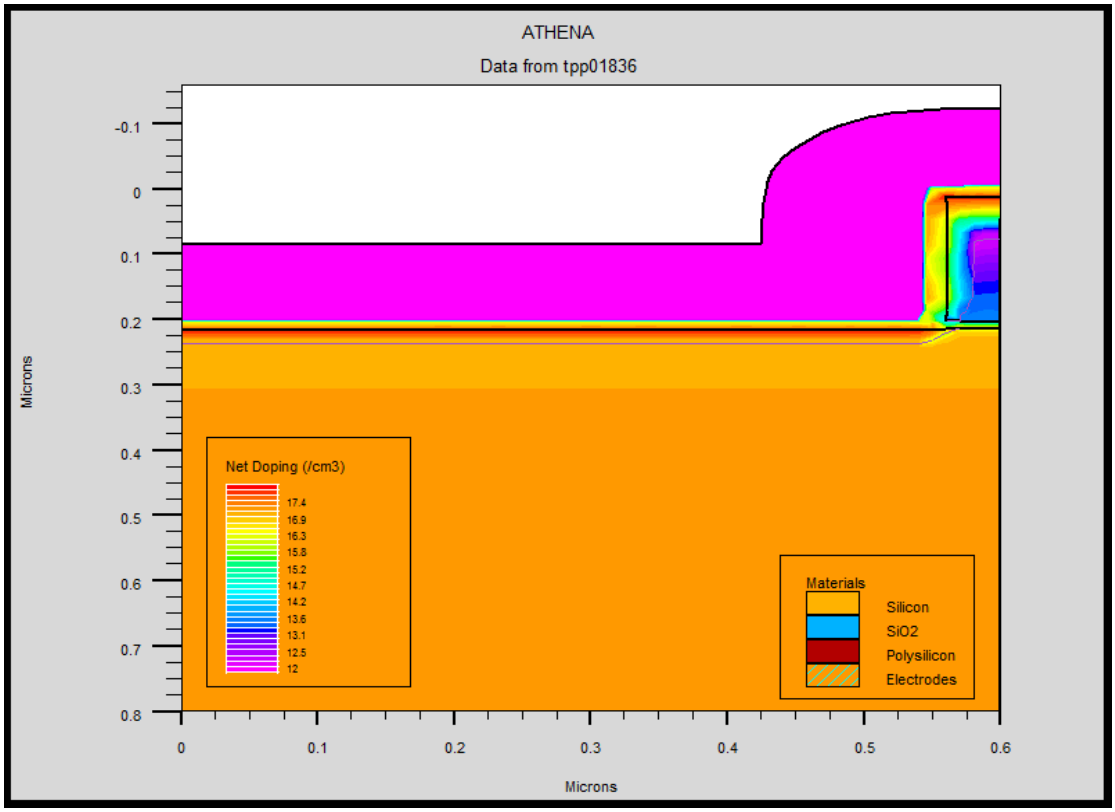
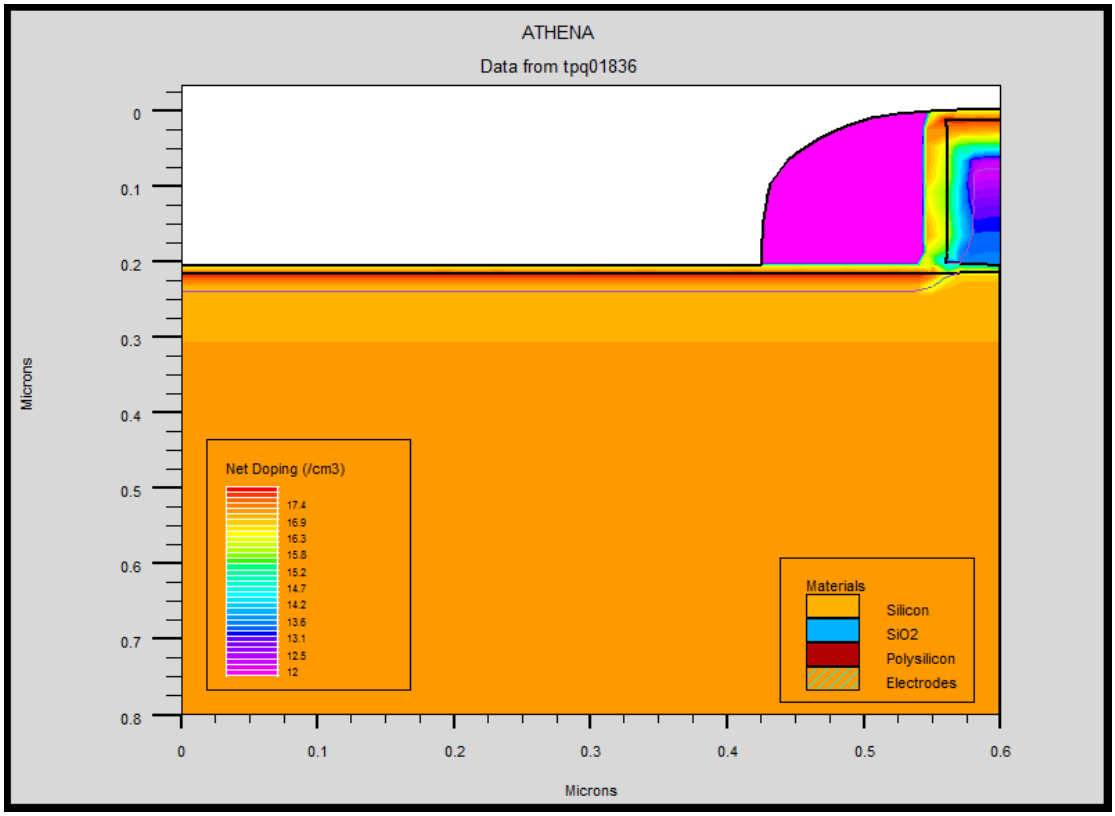


Figure 3.5: Lightly doped drain implant



(a)



(b)

Figure 3.6: Formation of oxide spacer (a) Oxide deposition (b) Oxide is etched at proper thickness and distance

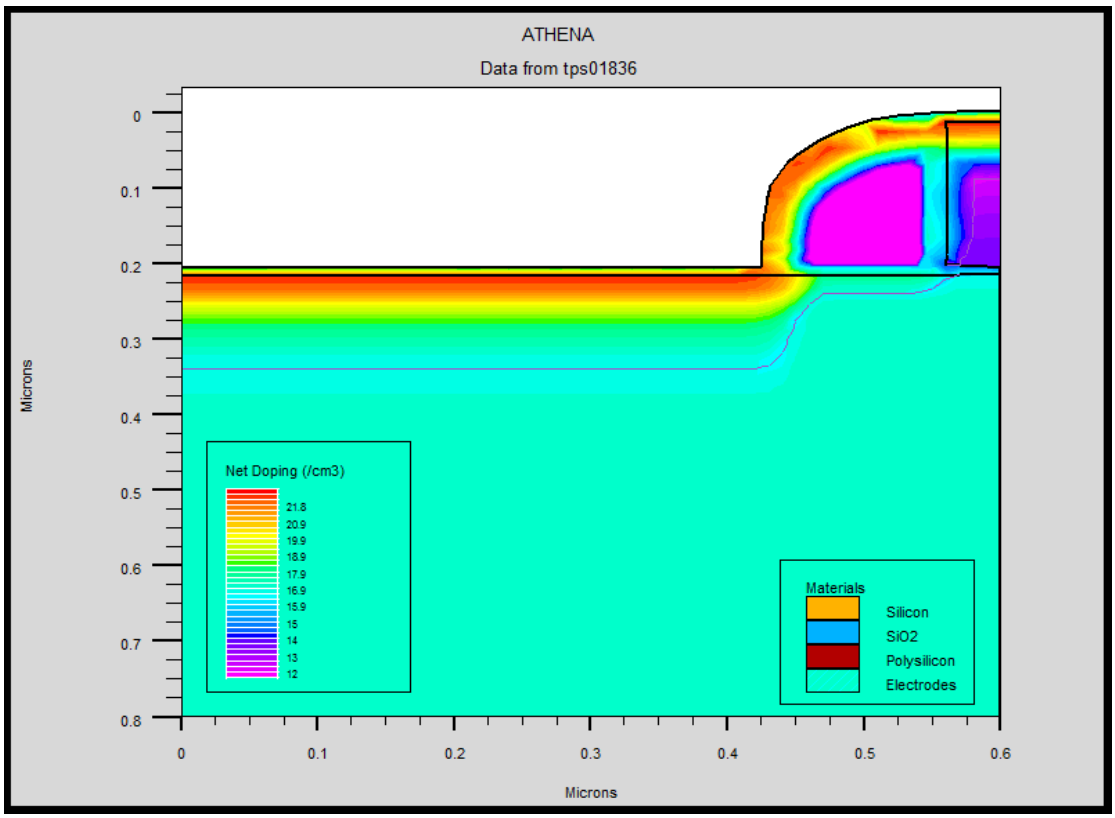


Figure 3.7: Source/drain implantation

(5) Lightly doped drain (LDD) implant-

LDD is formed after the polysilicon oxidation. For the formation of LDD, a suitable dose of phosphorus is implant and it is shown in Figure 3.5. Lightly doped drain reduces the electric field at the oxide semiconductor interface, due to this leakage is reduced.

(6) Formation of oxide spacer-

For the formation of oxide spacer, 0.12µm oxide is deposited, as shown in Figure 3.6. After the formation of Oxide spacer, Oxide spacer is etched at proper thickness for the formation of source and drain.

(7) Source/drain implantation-

For the formation of source and drain, arsenic is doped at proper energy and it is shown in Figure 3.7.

(8) Window for contact-

For the formation of window for contact, oxide is left etched from 0.2µm on the x-axis, as shown in Figure 3.8.

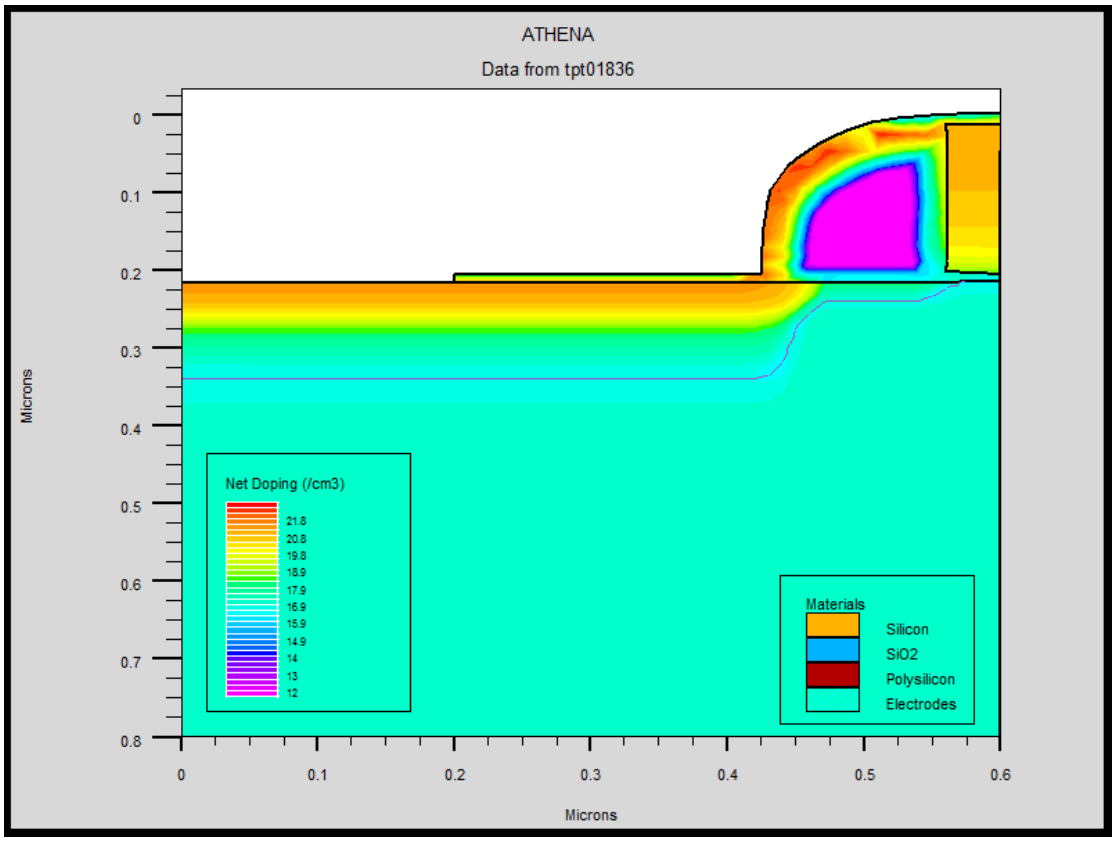
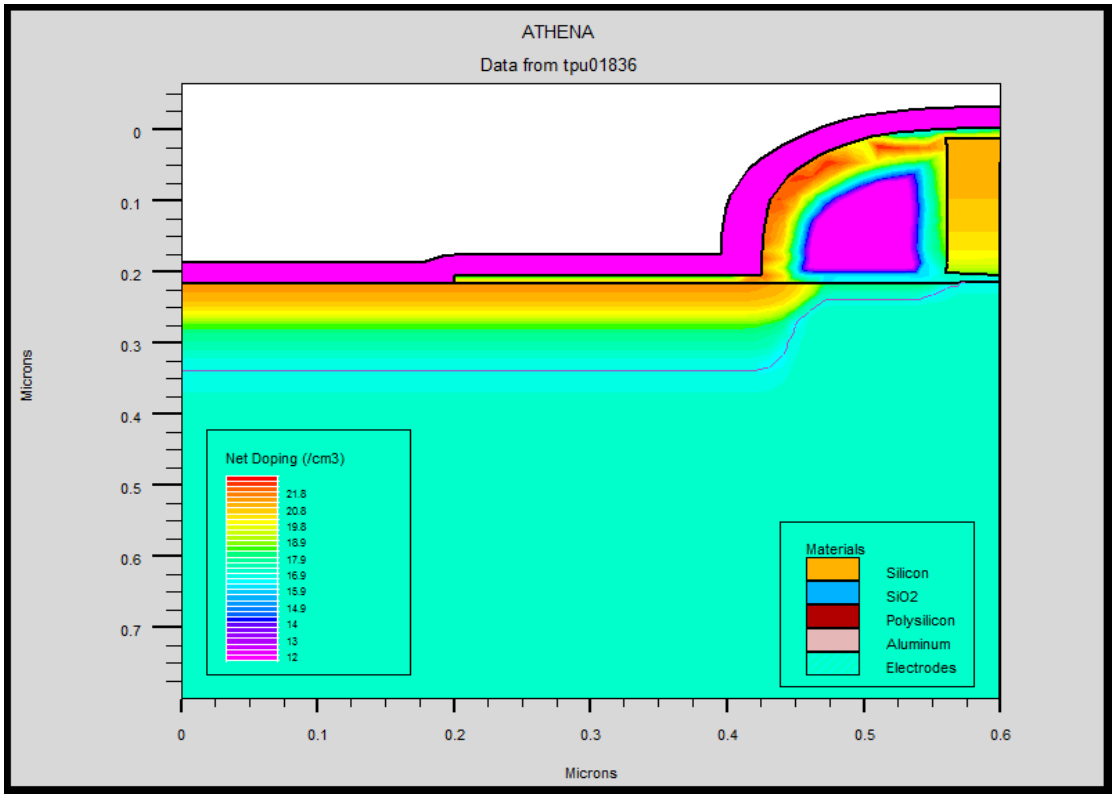
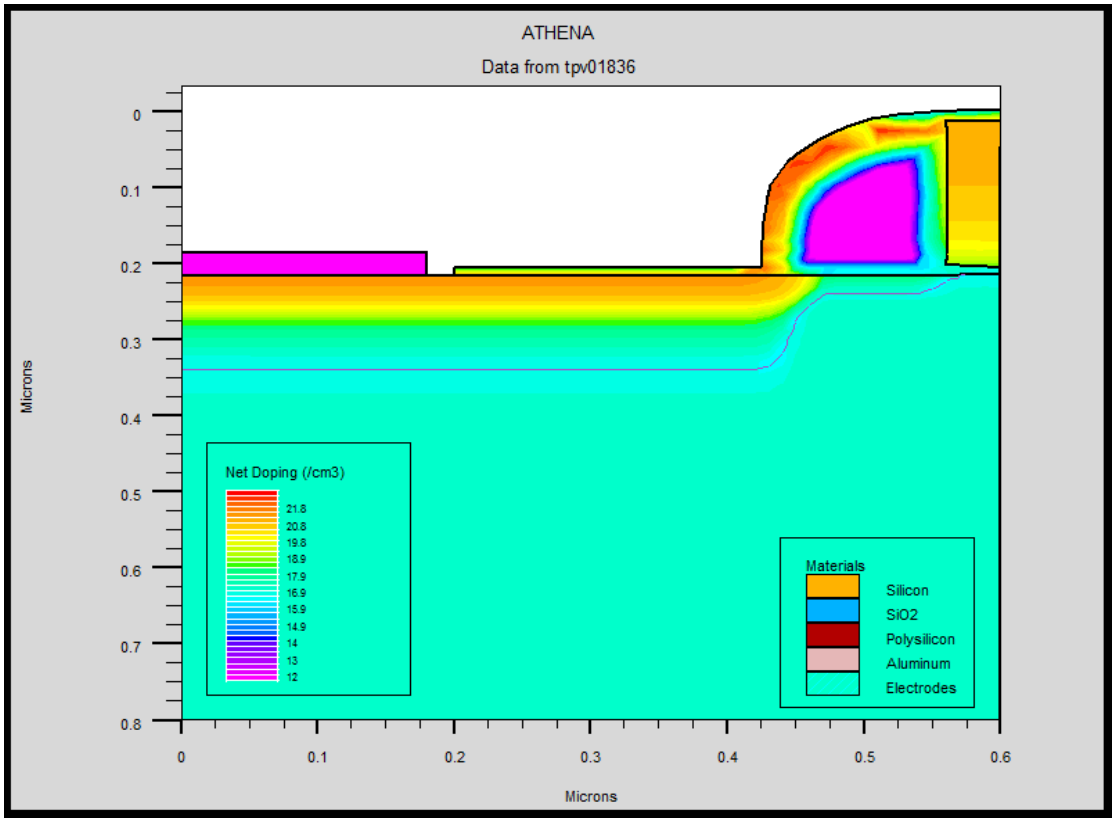


Figure 3.8: Window for contact



(a)



(b)

Figure 3.9: Metallisation by (a) Aluminium deposited and followed by (b) Aluminium etched

(9) Metallisation-

For the metallisation of nMOSFET aluminium is deposited and etched after 0.18µm at x-axis as shown in Figure 3.9.

(10) Reflecting the structure in the "Y" plane and defining the electrodes-

Now, the half structure is mirrored to obtain the complete structure of nMOSFET. All four terminals- gate, source, drain and substrate are defined as shown in Figure 3.10.

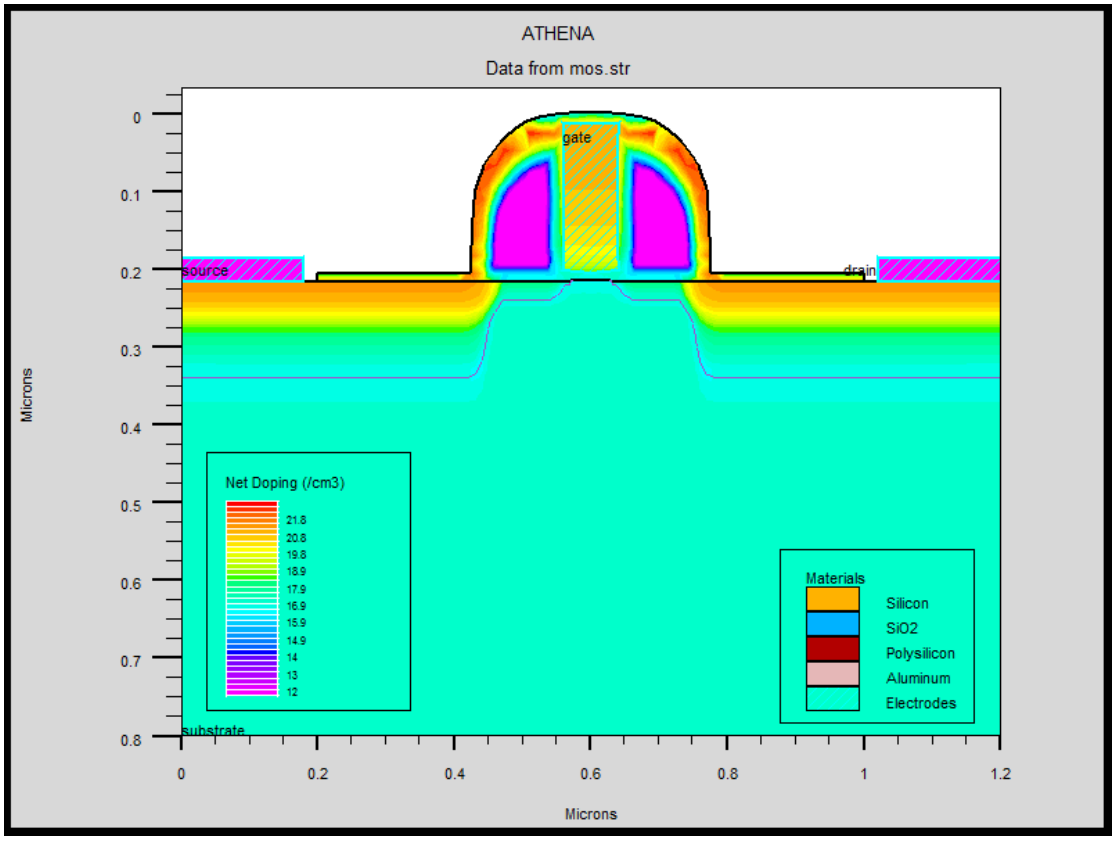


Figure 3.10: Final structure obtained by mirroring the structure and the defining the electrodes

3.2 Design of 90nm PD SOI MOSFET

3.2.1 Design of 90nm PD SOI MOSFET with LDD Implantation

A 90nm PD SOI nMOSFET with LDD implantation is simulated on Athena. The steps to design PD SOI nMOSFET with LDD implantation are described here. The physical parameters for the PD SOI nMOSFET are defined in the Table 3.2.

Table 3.2
Physical parameters for the design of
90nm PD SOI nMOSFET

Physical parameters	Value
Technology node	90nm
Minimum supply voltage	0.9-1.2V
Gate length	90nm
Thickness of Si layer	100nm
Thickness of BOX	400nm
Doping in Si layer	Boron dose $=25\times10^{13}$ cm^{-3}
Gate oxide thickness	3nm
V_t adjust implant	Boron dose $=1\times10^{10}$ cm^{-3}
Polysilicon deposit	100nm
LDD Implant	Phosphorus dose $=1.4\times10^{12}$ cm^{-3}
Halo doping	Boron dose $=10\times10^{12}$ cm^{-3}
Source/drain doping	Arsenic dose $=15\times10^{15}$ cm^{-3}

(1) Defining initial rectangular grid, BOX and Si layer-

Defining the Mesh for the SOI nMOSFET is an important step for device simulation. The grid specified in mesh definition will affect the accuracy and time used in the process simulation. For the ease of the geometry definition of etching, half of the structure first been simulated. The half structure will then be mirrored after all the processes had been carried out to obtain the completed structure. So, grids define in this initial stage is for half of the structure, the gate and channel part would be on the right. Therefore, the right side of the x axes will have finer grid defined compared to that of the left side. After defining the Mesh Definition, the region of BOX and Si layer is defined at x-axis and y-axis.

(2) Defining the initial substrate, BOX and Si layer-

The LINE statements specified in the Mesh Definition set only the rectangular base for the Athena simulation structure. The next step is the initialization of the substrate region, BOX and Si layer by doping concentration, substrate orientation, and some additional parameters and this is shown in Figure 3.11.

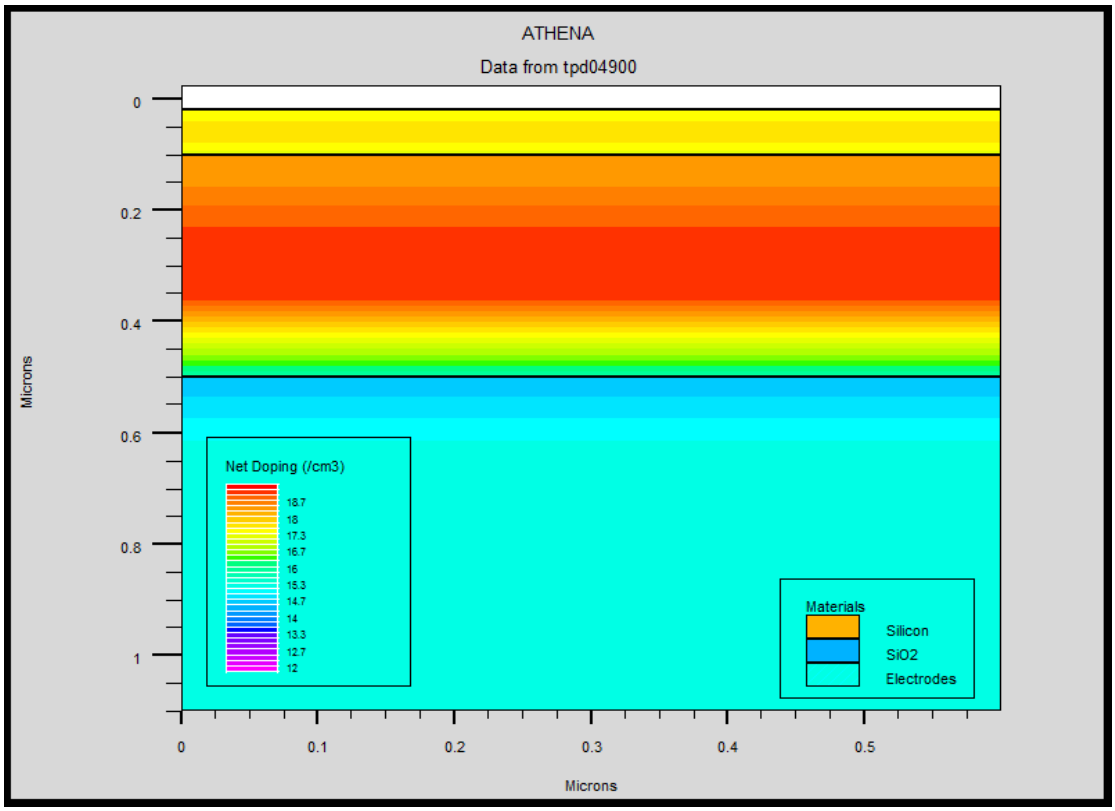


Figure 3.11: BOX and SOI layer

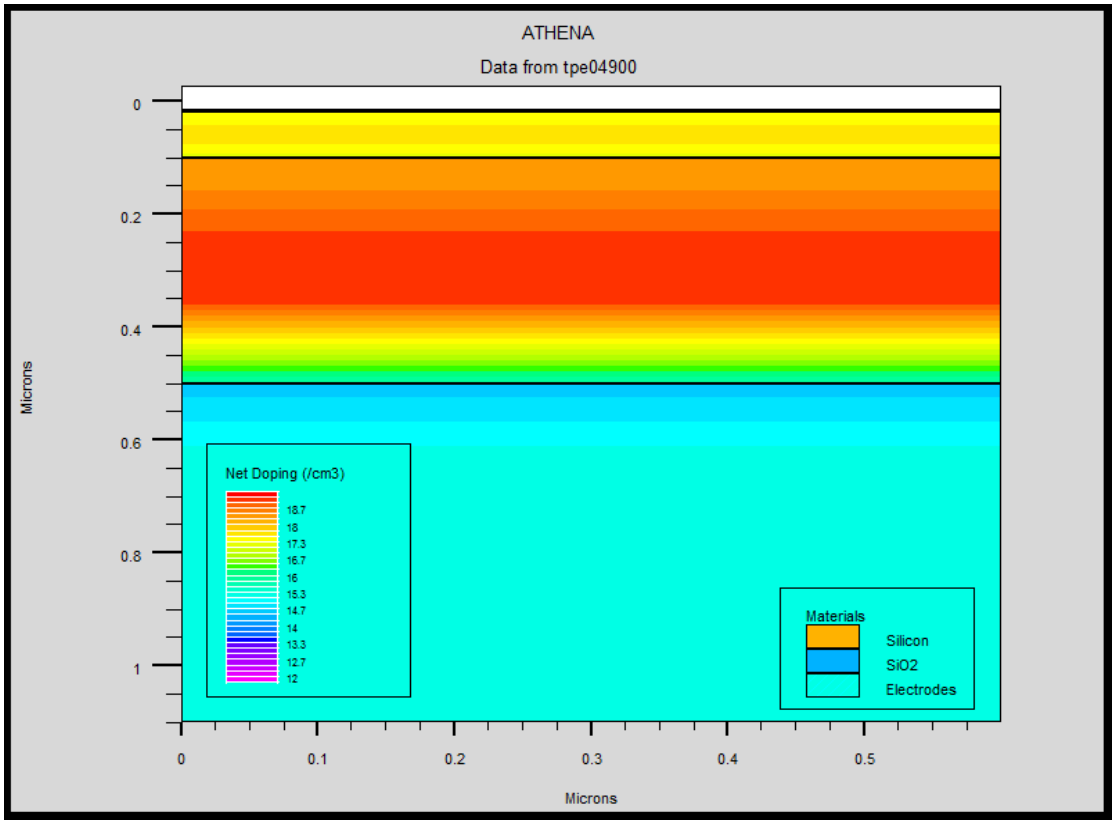


Figure 3.12: Gate oxidation

(3) Gate oxidation-

Figure 3.12 shows formation of gate oxide layer. Diffusion with oxygen is used to create the gate oxide layer. To obtain the desired gate oxide thickness, we can first simulate the diffusion process and extract the gate oxide thickness formed. From the extracted value, the optimizer tool will be used to determine the time and temperature to obtain desired thickness.

(4) V_t adjust implant and polysilicon gate formation-

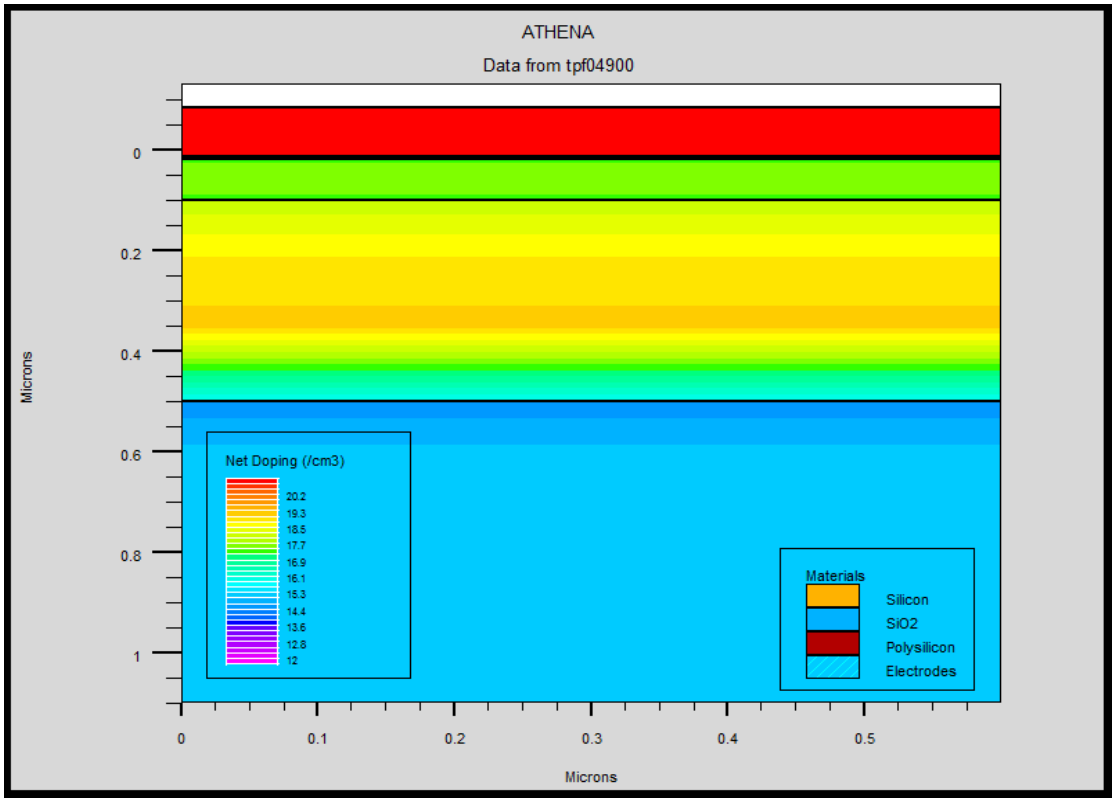
In SOI nMOSFET threshold voltage is adjusted by implanting the required dose of boron at proper energy. Gate formation is done after the gate oxide layer formation. The layer is then etched until half the desired gate length left as shown in Figure 3.13.

(5) Polysilicon oxidation-

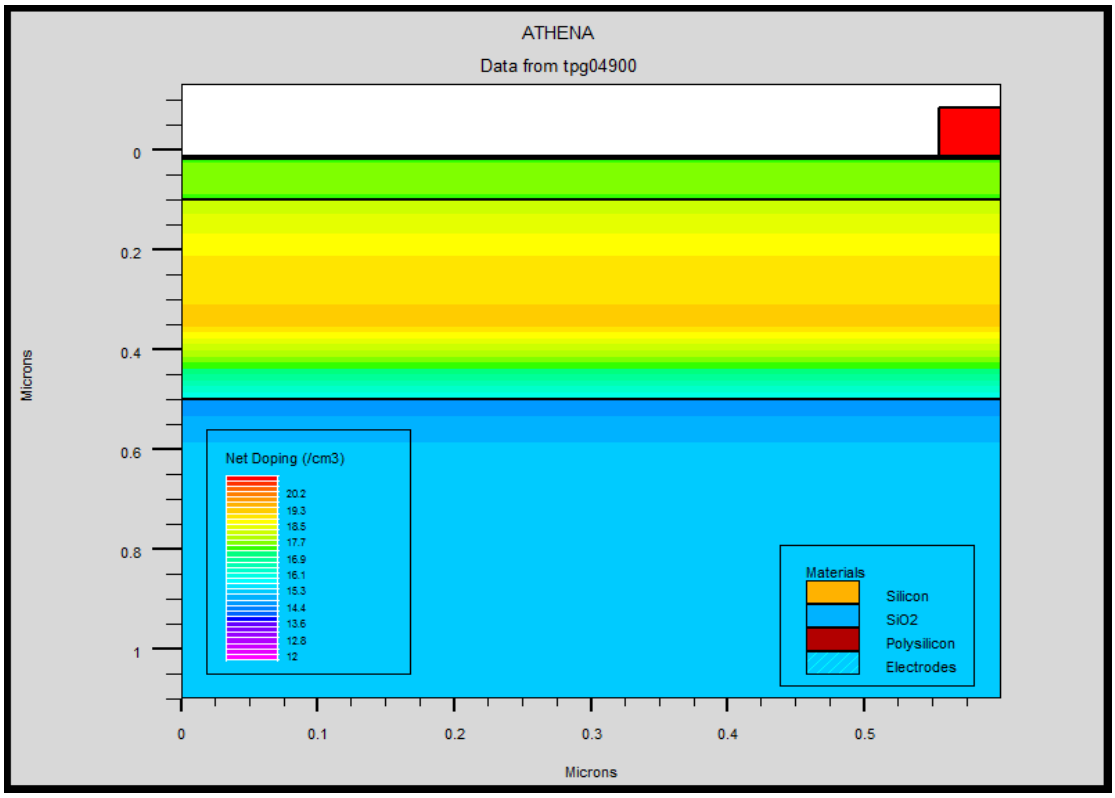
Design of polysilicon oxidation is shown in Figure 3.14.

(6) Lightly doped drain (LDD) implant-

Lightly doped drain reduces the electric field at the oxide semiconductor interface. The Light doped drain reduces the GIDL and hot electron effects. For the formation of LDD, a suitable dose of phosphorus is implant and it is shown in Figure 3.15.



(a)



(b)

Figure 3.13: Gate formation (a) Polysilicon deposition
(b) Deposited polysilicon etched

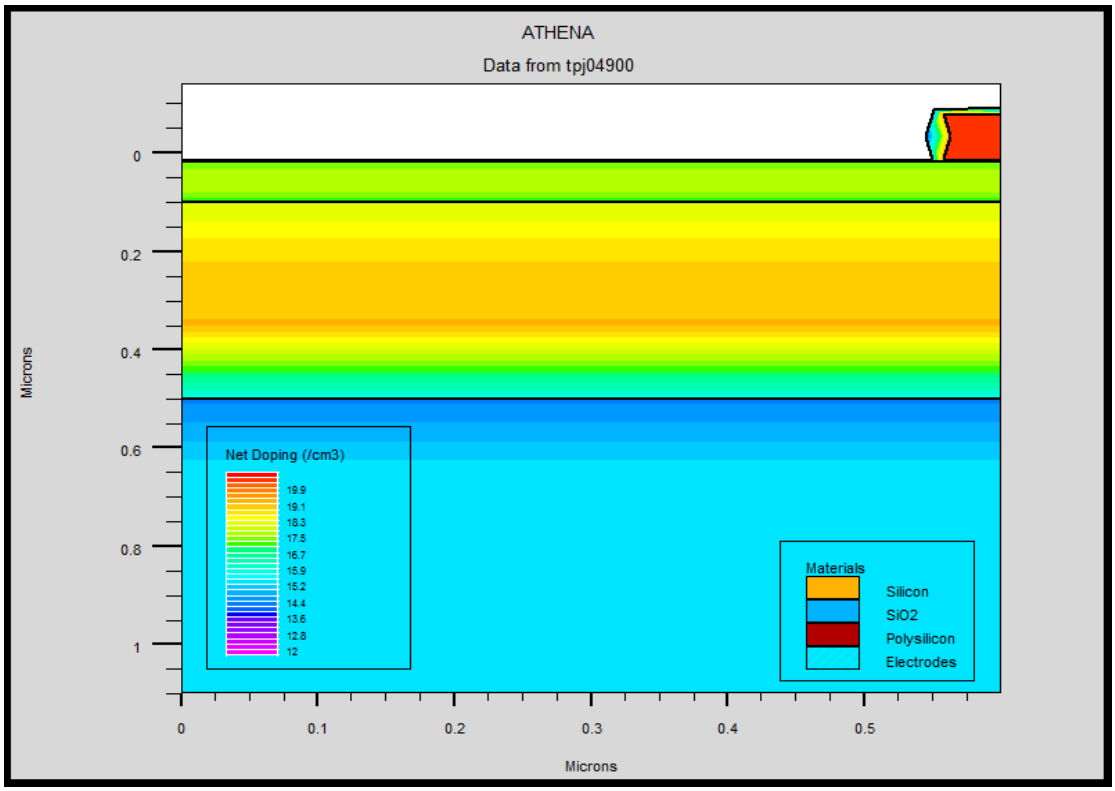


Figure 3.14: Polysilicon oxidation

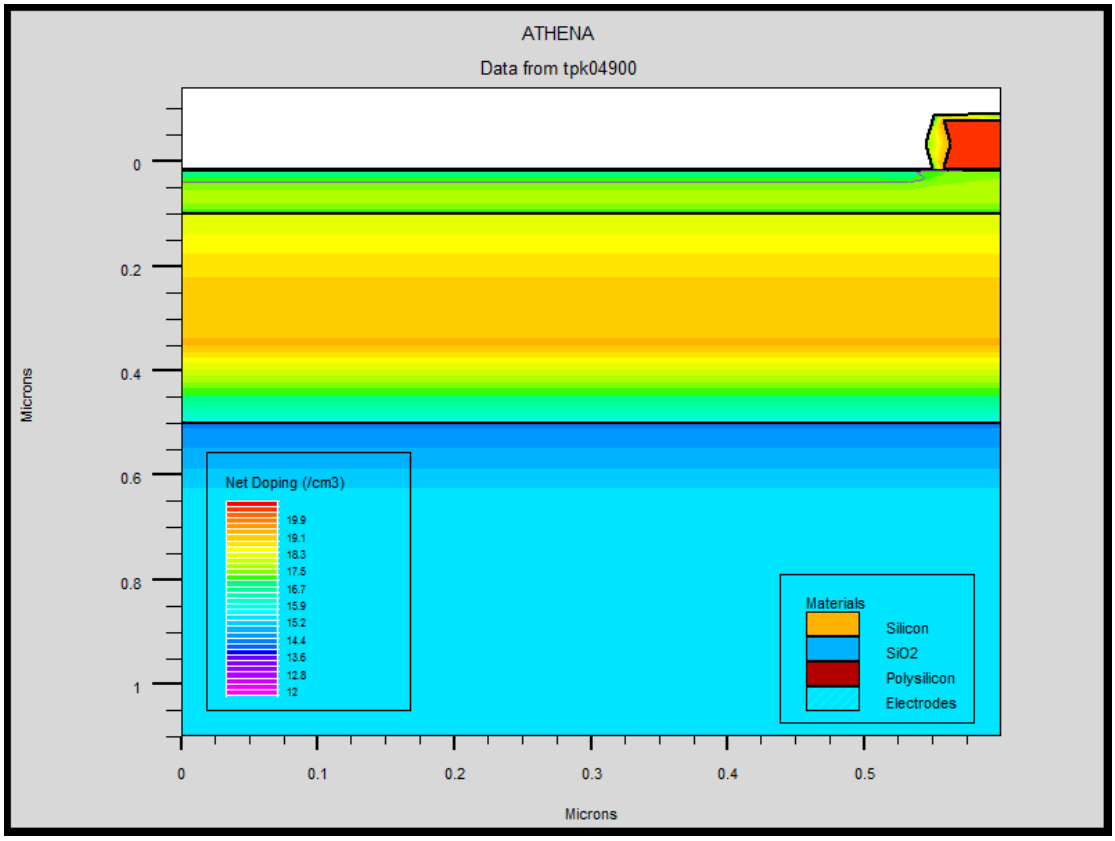


Figure 3.15: Lightly doped drain implant

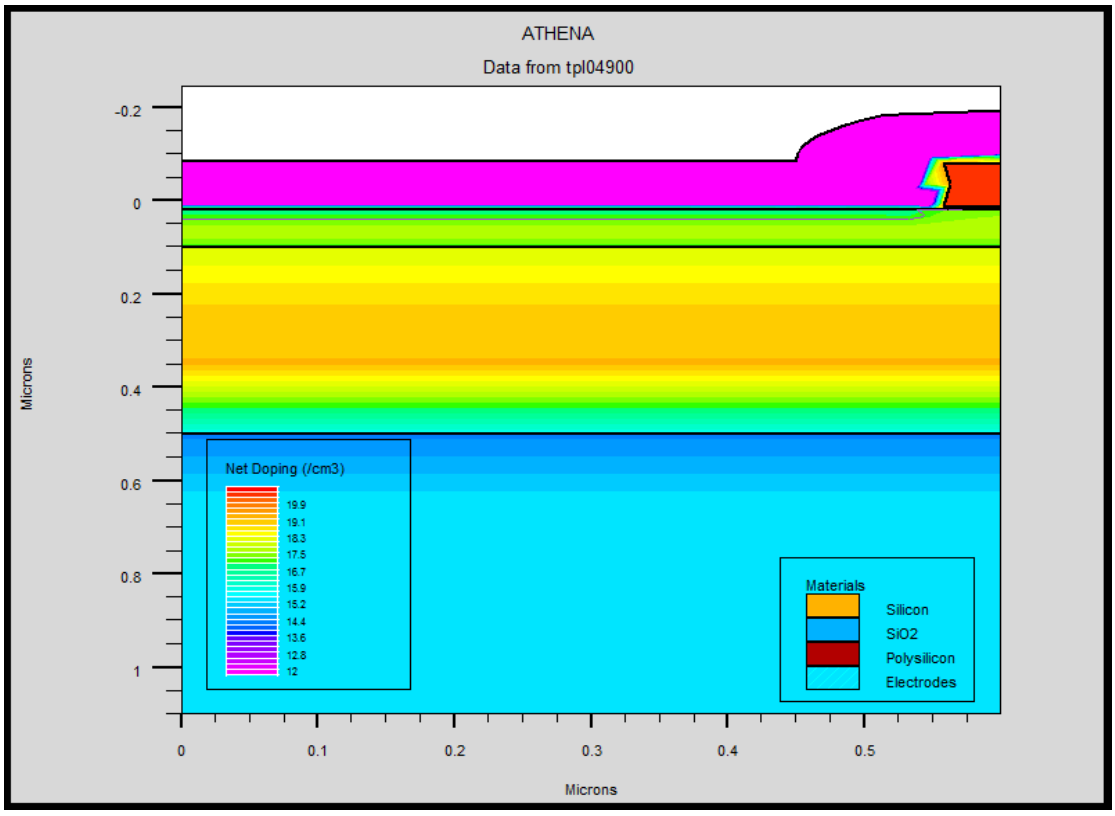


Figure 3.16: Oxide spacer

(7) Formation of oxide spacer-

For the formation of oxide spacer, 0.1μm oxide is deposited, as shown in Figure 3.16.

(8) Source/drain implantation-

Arsenic is doped to form the source/drain junction in the Si layer and it is shown in Figure 3.17.

(9) Window for contact-

For the formation of window for contact, oxide is left etched from 0.45μm on the x-axis, as shown in Figure 3.18.

(10) Metallisation-

Gate oxide layer is etched to open a contact window for the metal, after that aluminium is deposited and etched as shown in Figure 3.19.

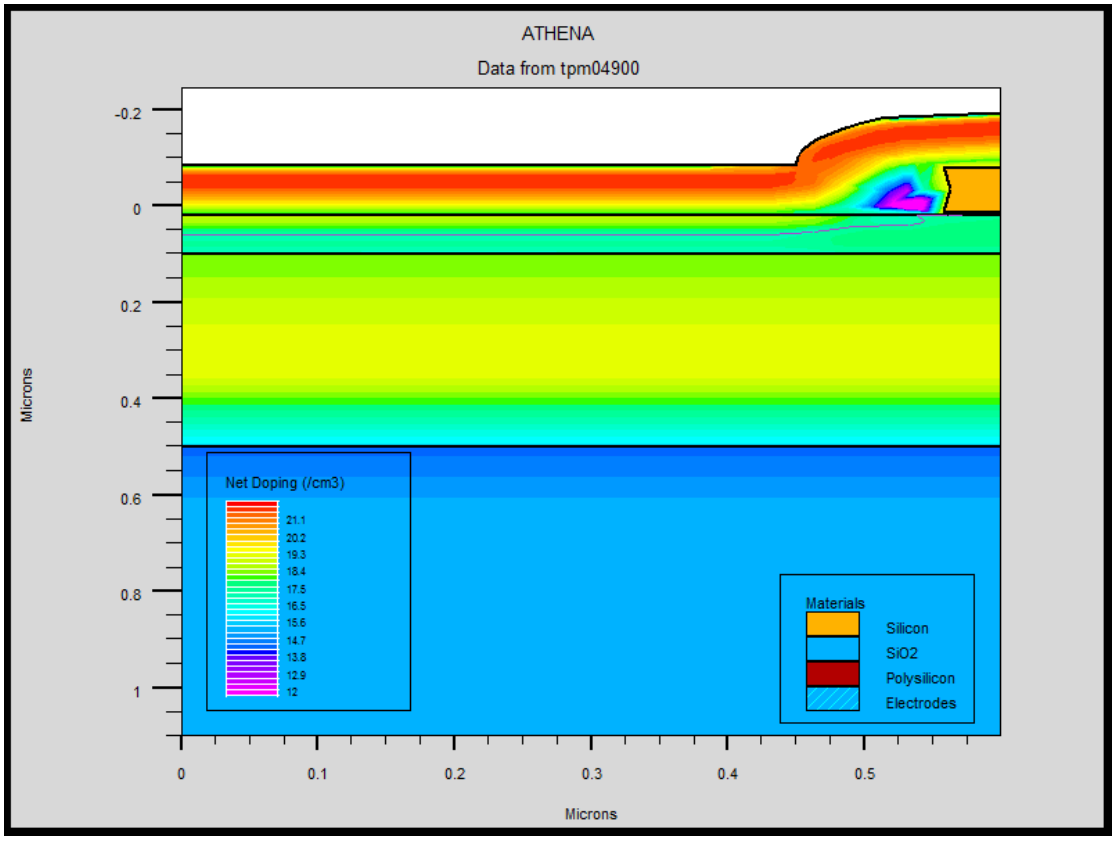


Figure 3.17: Source/drain Implantation

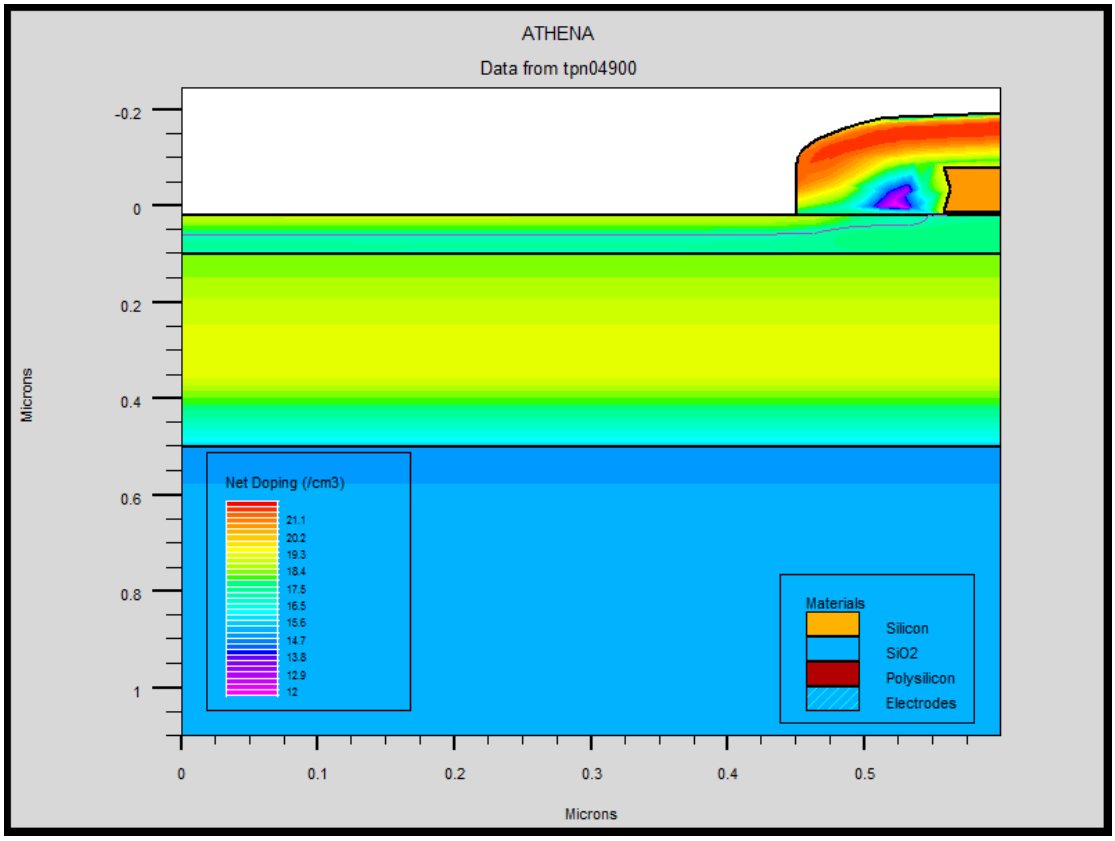
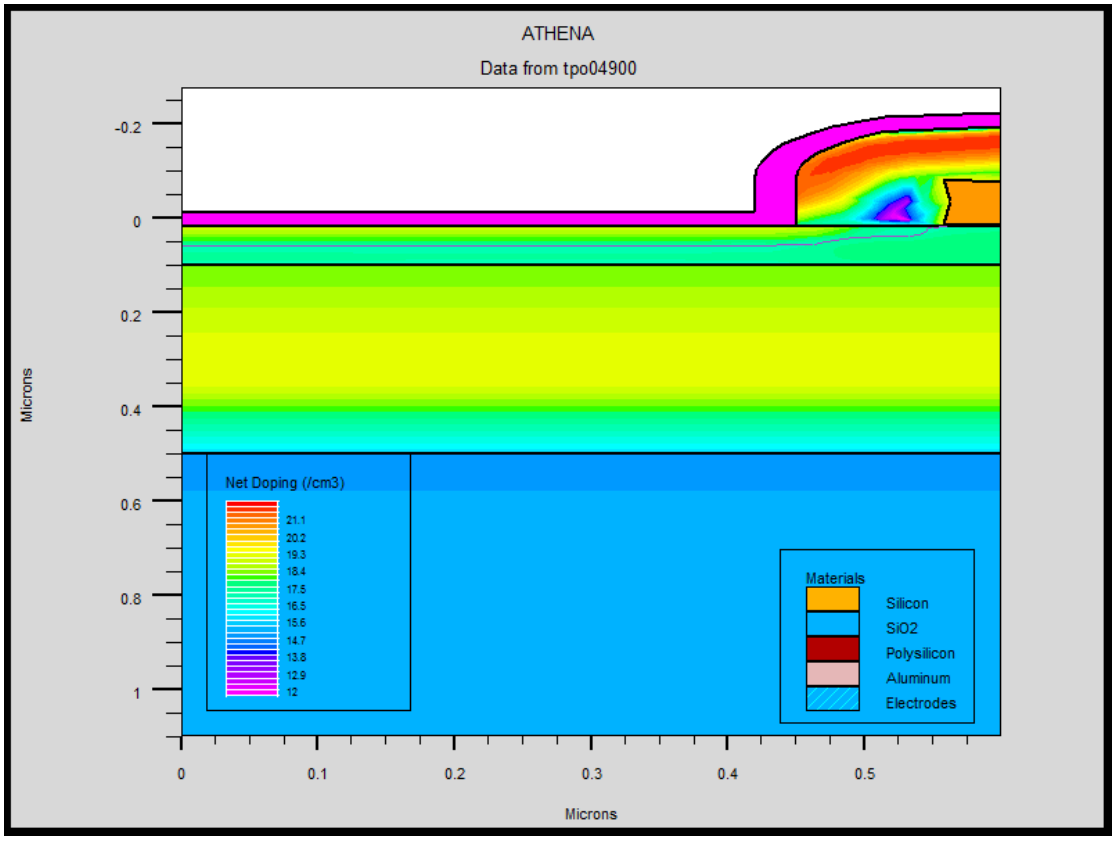
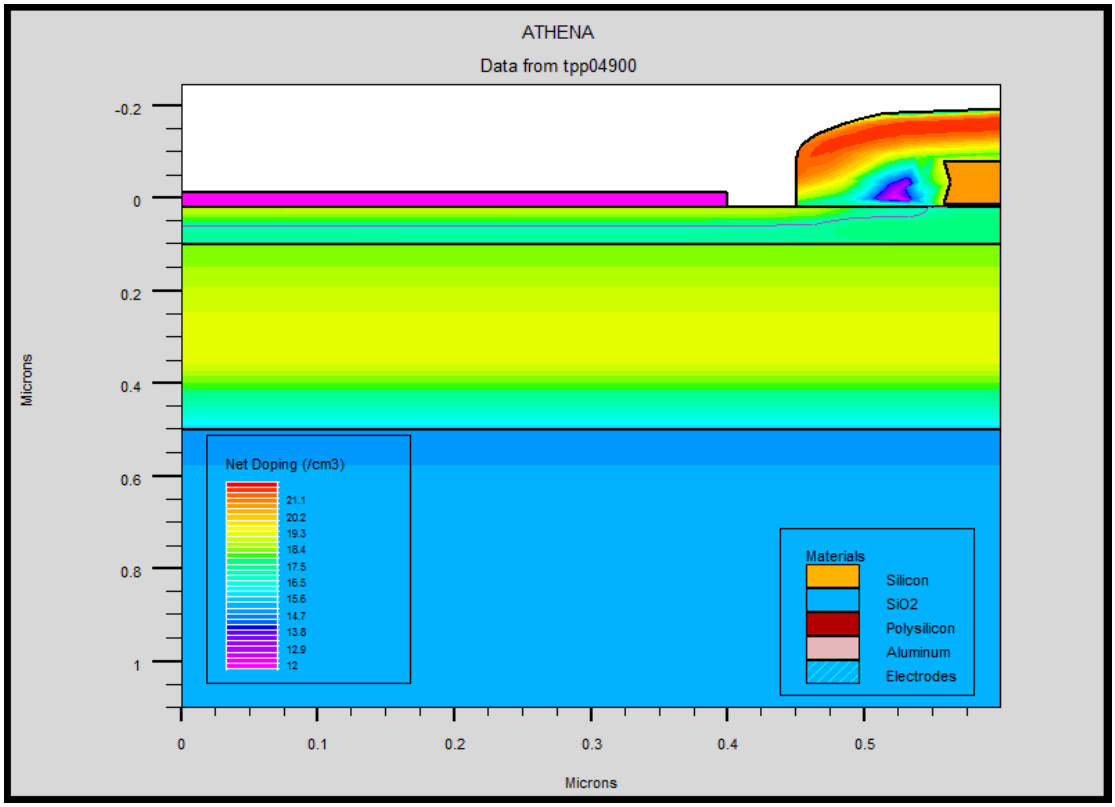


Figure 3.18: Window for contact



(a)



(b)

Figure 3.19: Metallisation by (a) Aluminium deposited and followed by (b) Aluminium etched

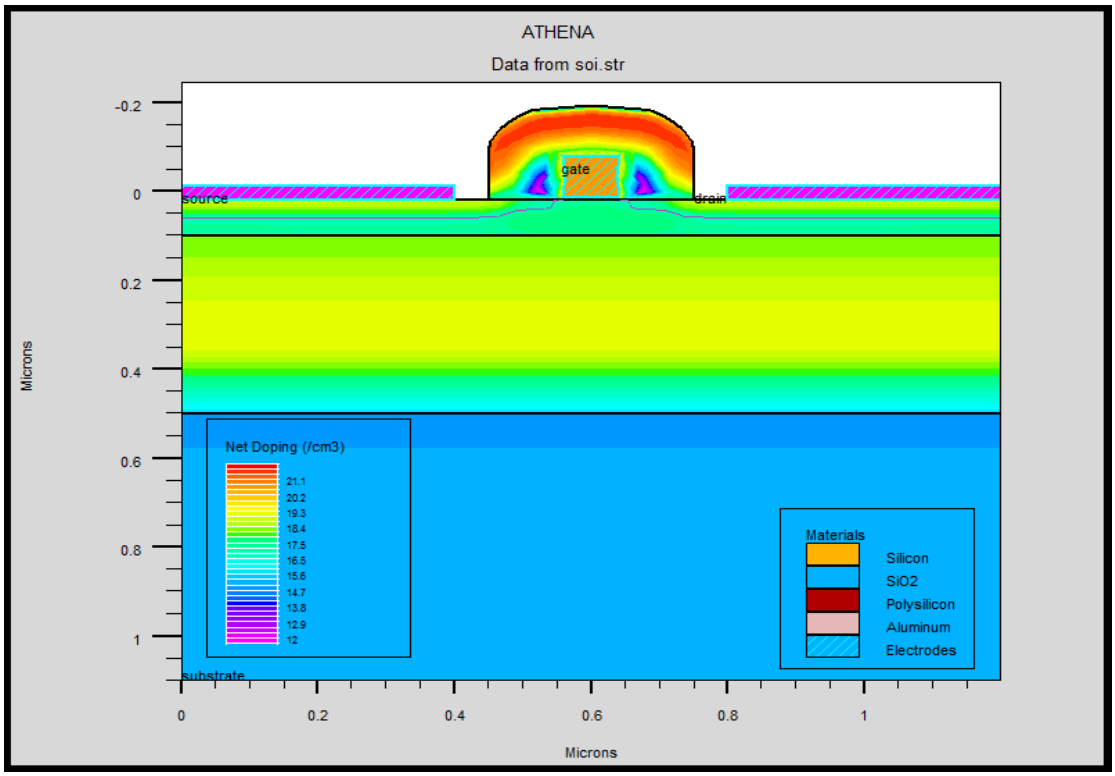


Figure 3.20: Final structure of PD SOI MOSFET with LDD implantation

(11) **Reflecting the structure in the "Y" plane and defining the electrodes-**

Now, the half structure is mirrored to obtain the complete structure of PD SOI MOSFET. All four terminals- gate, source, drain and substrate are defined as shown in Figure 3.20.

3.2.2 Design of 90nm PD SOI MOSFET with LDD and Halo Implantation

For the reduction of leakage current in PD SOI nMOSFET halo doping is done. Design steps for PD SOI structure with LDD and halo implant is same as that of PD SOI structure with LDD implant, only one extra step is added after LDD implant step. For the formation of halo implant, suitable amount of boron dose is implanted at angle 60^0. The complete structure of PD SOI MOSFET with LDD and halo implant is shown in Figure 3.21.

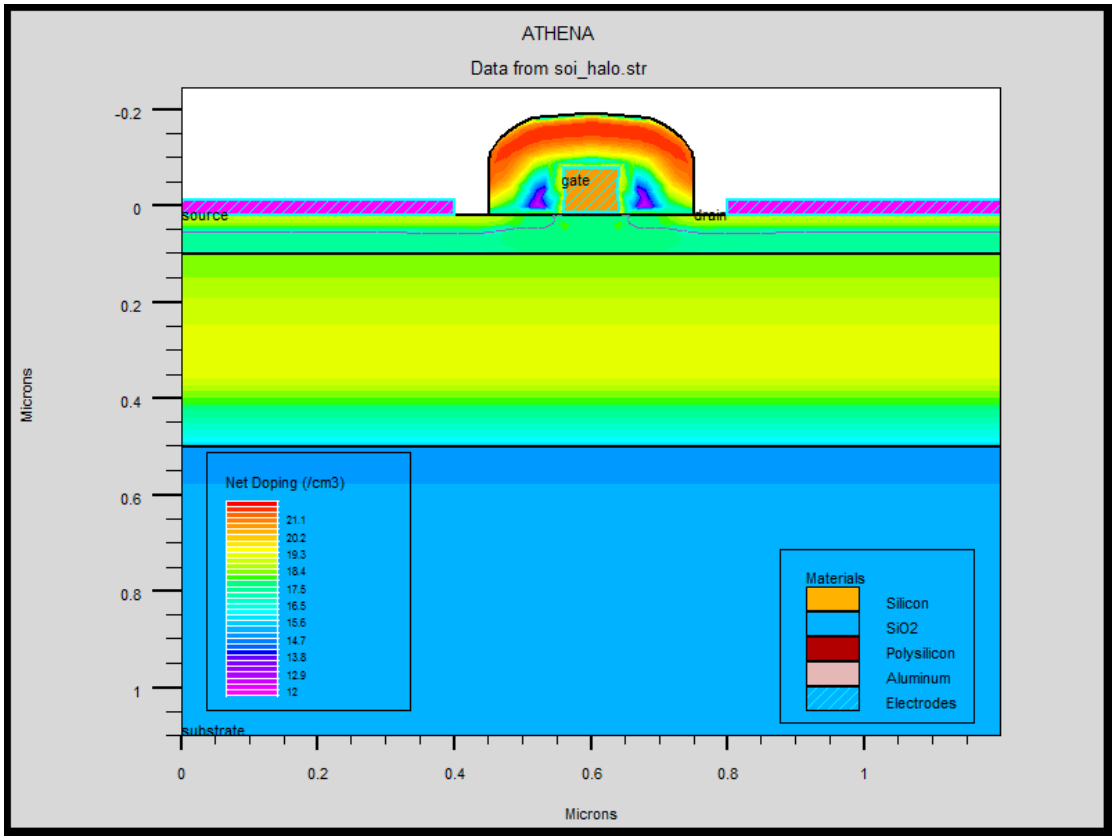


Figure 3.21: PD SOI MOSFET with LDD and halo implant

CHAPTER

4 RESULTS AND DISCUSSIONS

4.1 Electrical Characteristics of 90nm Bulk-Si nMOSFET

Different electrical characteristics such as I_D versus V_{gs}, log I_D versus V_{gs}, I_D versus V_{ds} curves are observed at Athena.

4.1.1 Drain Current versus Gate Voltage (I_D vs. V_{gs})

Figure 4.1 shows the curves between drain current and gate voltage of nMOSFET at different drain voltages (0.9, 1.0, 1.1 and 1.2).

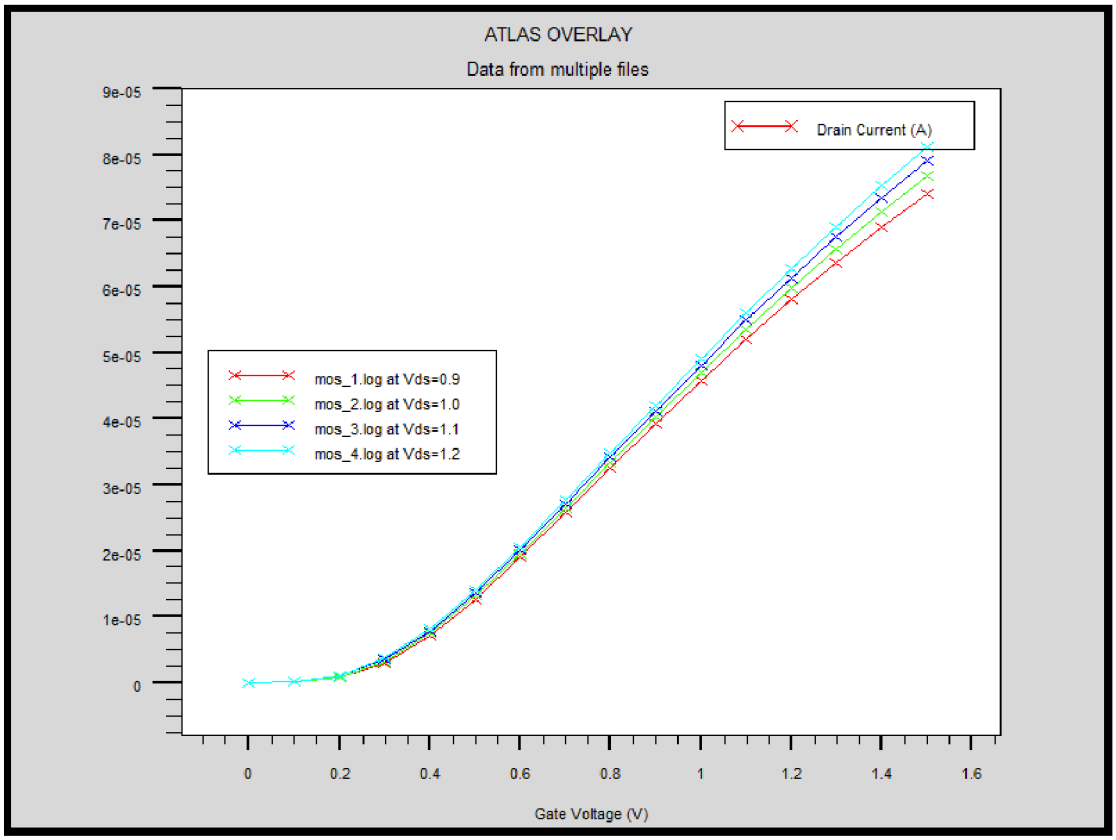


Figure 4.1: I_D versus V_{gs} curves of 90nm bulk-Si nMOSFET at different drain voltages

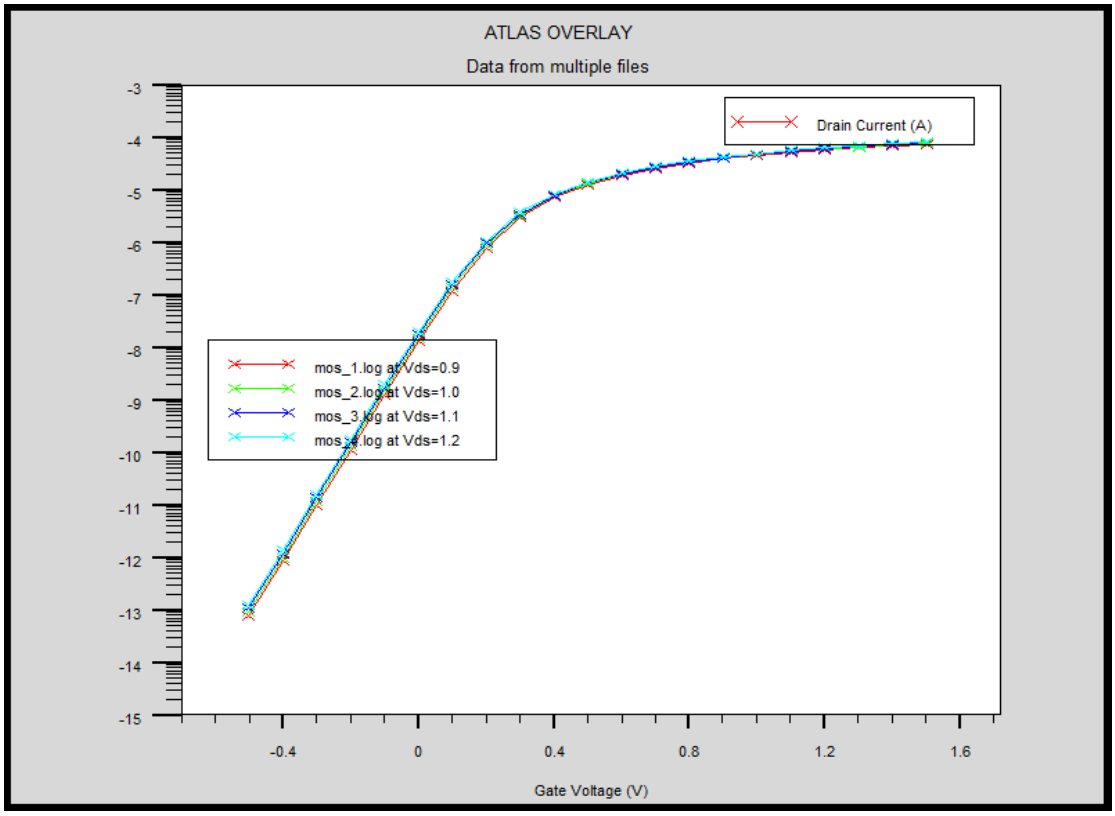


Figure 4.2: Log I_D versus V_{gs} curves of 90nm bulk-Si nMOSFET at different drain voltages

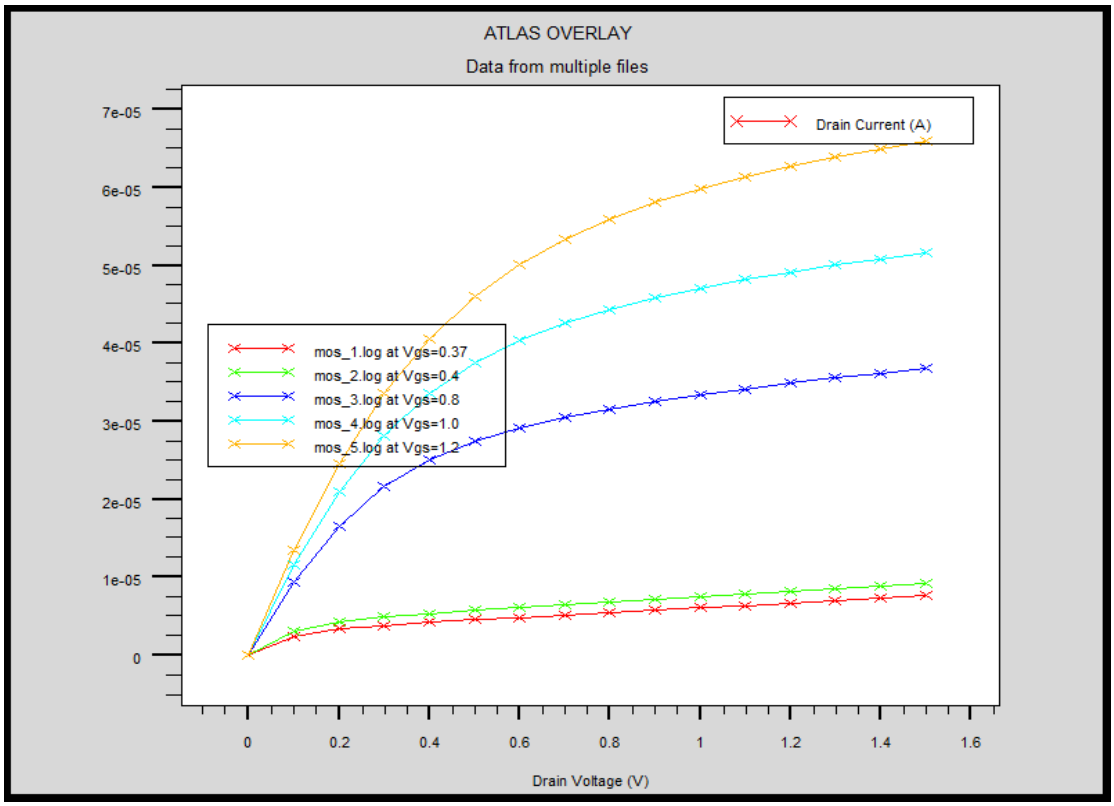


Figure 4.3: I_D versus V_{ds} curves of 90nm bulk-Si nMOSFET at different gate voltages

4.1.2 Subthreshold Characteristics (log I_D vs. V_{gs})

Figure 4.2 shows the curves between log I_D vs. V_{gs} of bulk-Si nMOSFET at different drain voltages (0.9, 1.0, 1.1 and 1.2).

4.1.3 Drain Current versus Drain Voltage (I_D vs. V_{ds})

Figure 4.3 shows the curves between drain current and drain voltage of bulk-Si nMOSFET at different gate voltages (0.37, 0.4, 0.8, 1.0, and 1.2).

4.2 Effect of Physical Parameters on 90nm PD SOI nMOSFET

Effect of physical parameters such as gate oxide thickness, channel doping, and halo implantation on threshold voltage (V_{th}) and off current (I_{off}) are observed on Athena.

4.2.1 Effect of Gate Oxide Thickness on Threshold Voltage

Figure 4.4 shows the effect of gate oxide thickness on threshold voltage. From Figure 4.4 it is clear, as the gate oxide thickness increases, threshold voltage also increases. The gate oxide thickness is a reverse proportion to the gate capacitance. As the gate oxide thickness increases, gate oxide capacitance decreases, which means that the gate less control to the channel. In order to invert the channel, the threshold voltage will increase. Gate oxide thickness is modified by oxidation time, pressure and temperature.

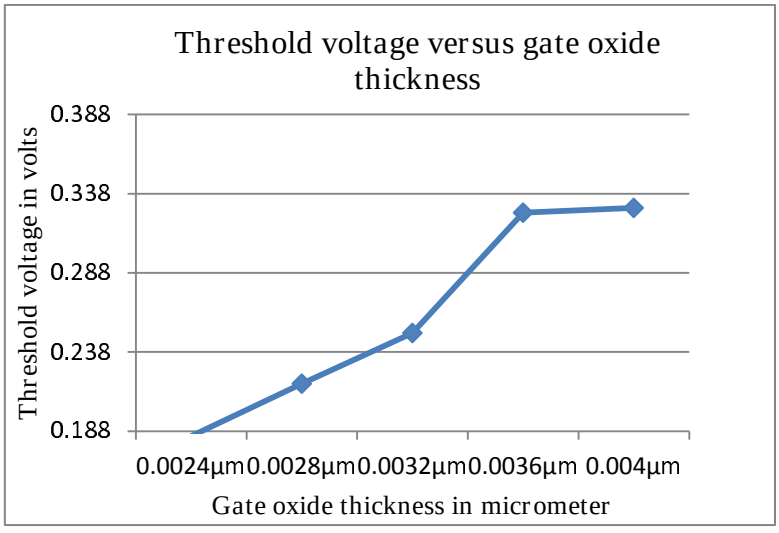


Figure 4.4: Threshold voltage at different gate oxide thickness

4.2.2 Effect of Gate Oxide Thickness on Off current

As the gate oxide thickness increases off current decreases. On increasing the gate oxide thickness electric field decreases, therefore I_{off} decreases as shown in Figure 4.5.

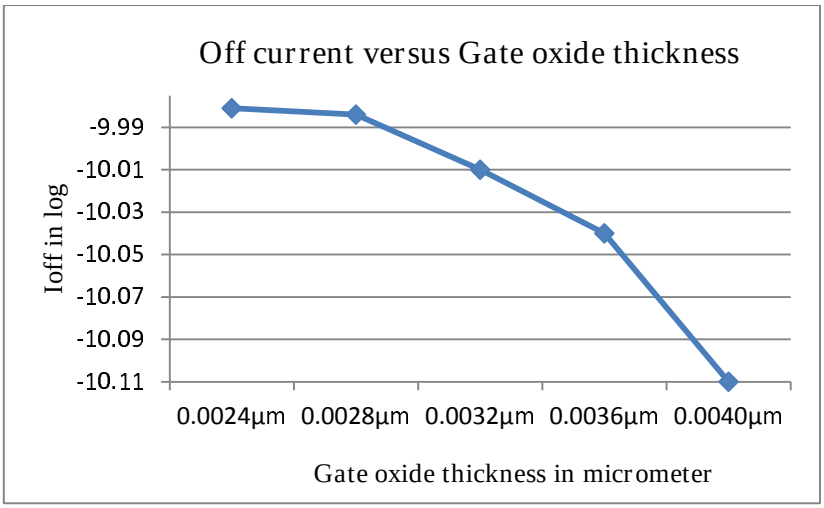


Figure 4.5: Variation of off current with gate oxide thickness

4.2.3 Effect of Channel Doping on Threshold Voltage

From Figure 4.6 it is clear, as channel doping increases threshold voltage also increases. When the channel doping increases, Fermi potential and channel depletion charge also increases, it requires more effort to deplete the whole channel. That causes the increase of threshold voltage with channel doping implantation. Channel doping implantation is changed by changing dose and energy parameters.

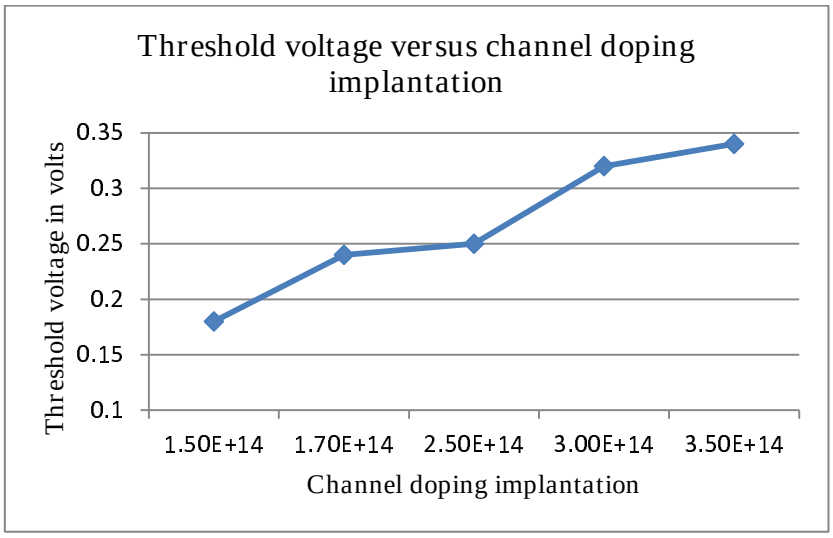


Figure 4.6: Variation of threshold voltage with Channel doping implantation

4.2.4 Effect of Channel Doping on Off current

From Figure 4.7, it is clear, as channel doping implantation increases, I_{off} starts to decreases. Channel doping implantation is changed by changing dose and energy parameters.

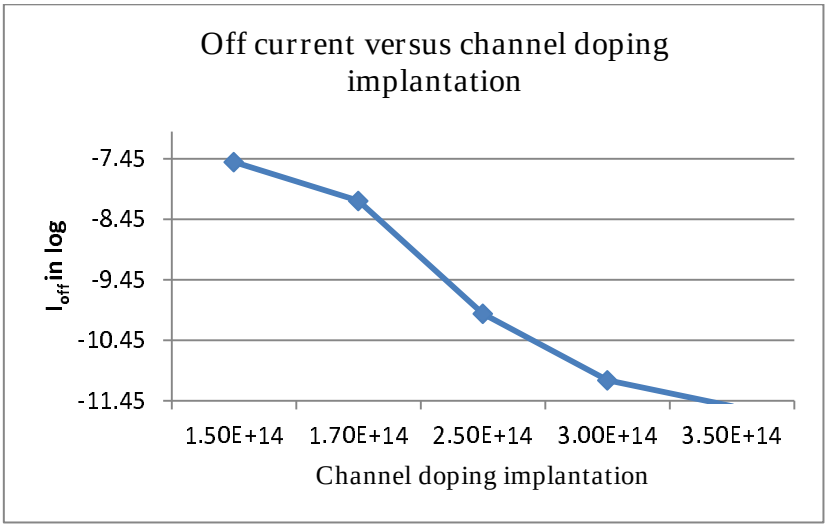


Figure 4.7: Variation of off current with channel doping implantation

4.2.5 Effect of Halo Implantation on Threshold Voltage

Figure 4.8 shows, as the halo implantation increases, threshold voltage also increases. To control the dependence of threshold voltage on channel length, halo doping is introduced. Halo doping is changed by changing dose, energy and tilt parameters.

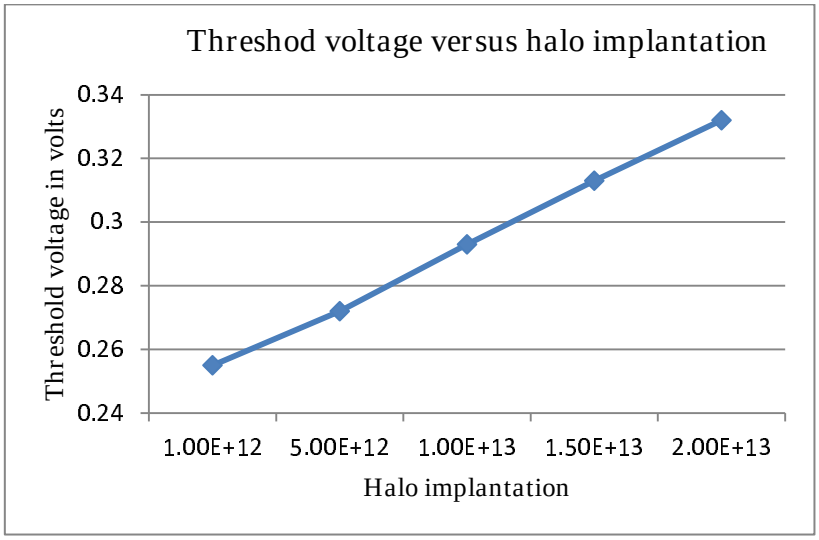


Figure 4.8: Variation of threshold voltage with halo implantation

4.2.6 Effect of Halo Implantation on Off current

Figure 4.9 shows, as the halo implantation increases, I_{off} starts to decrease. Halo doping reduces the charge sharing effects from the source and drain fields, this reduces the width of the depletion region in the drain-substrate and substrate regions. Thus I_{off} reduces.

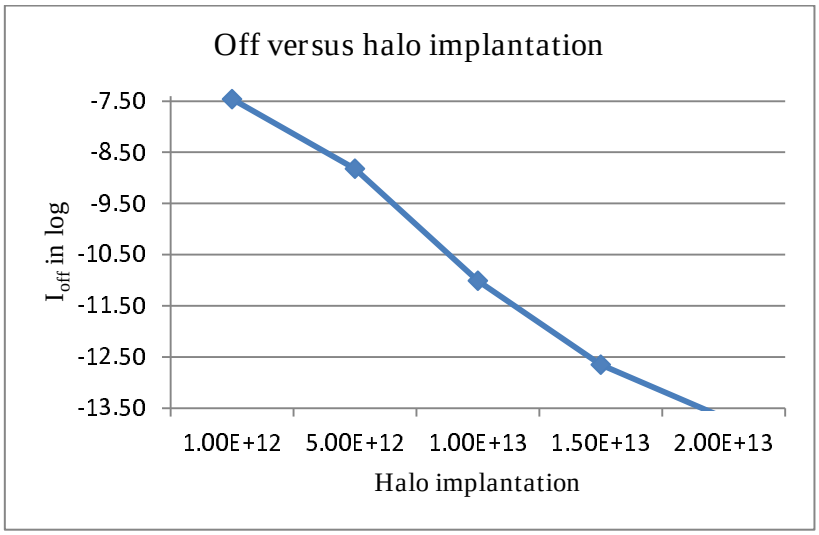


Figure 4.9: Variation of off current with halo implantation

4.3 Electrical Characteristics of 90nm PD SOI nMOSFET with LDD Implantation

4.3.1 Drain Current versus Gate Voltage (I_D vs. V_{gs})

Figure 4.10 shows the curves between drain current and gate voltage of PD SOI with LDD implantation at different drain voltages (0.9, 1.0, 1.1 and 1.2).

4.3.2 Subthreshold Characteristics (log I_D vs. V_{gs})

Figure 4.11 shows the curves between subthreshold and gate voltage of PD SOI with LDD implantation at different drain voltages (0.9, 1.0, 1.1 and 1.2).

4.3.3 Drain Current versus Drain Voltage (I_D vs. V_{ds})

Figure 4.12 shows the curves between drain current and drain voltage of PD SOI with LDD implantation at different gate voltages (0.27, 0.4, 0.8, 1.0, and 1.2).

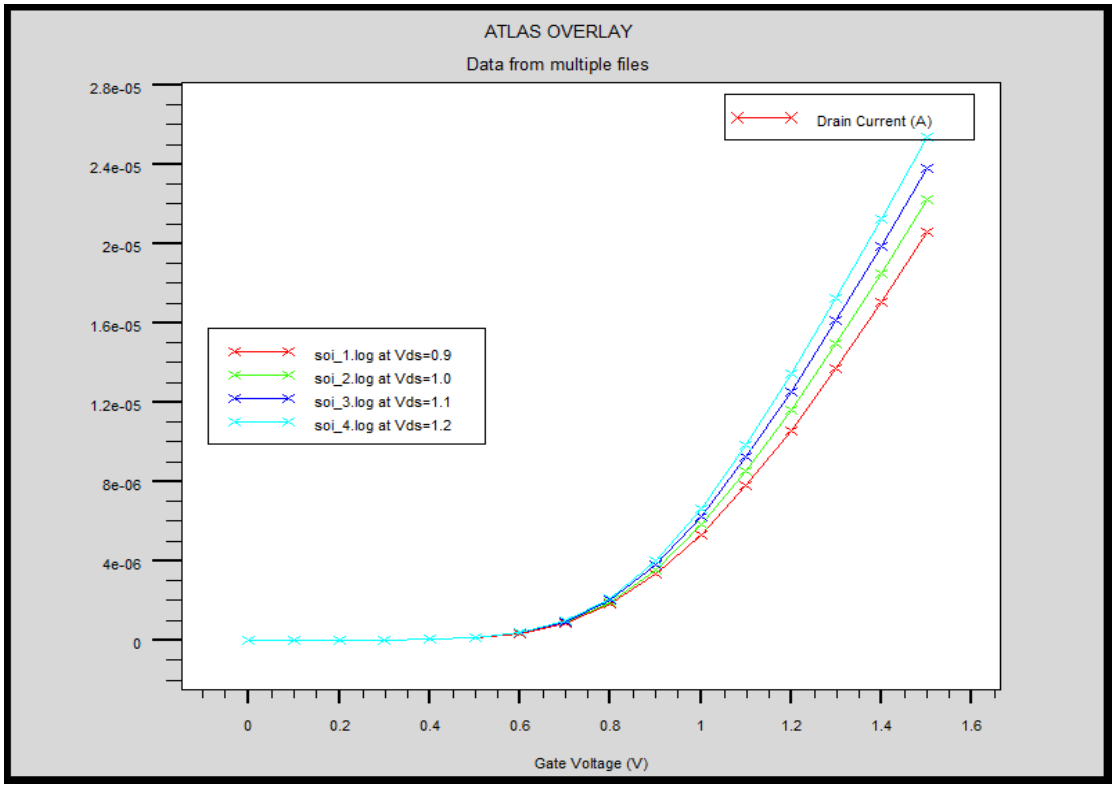


Figure 4.10: I_D versus V_{gs} curves of 90nm PD SOI nMOSFET with LDD implantation at different drain voltages

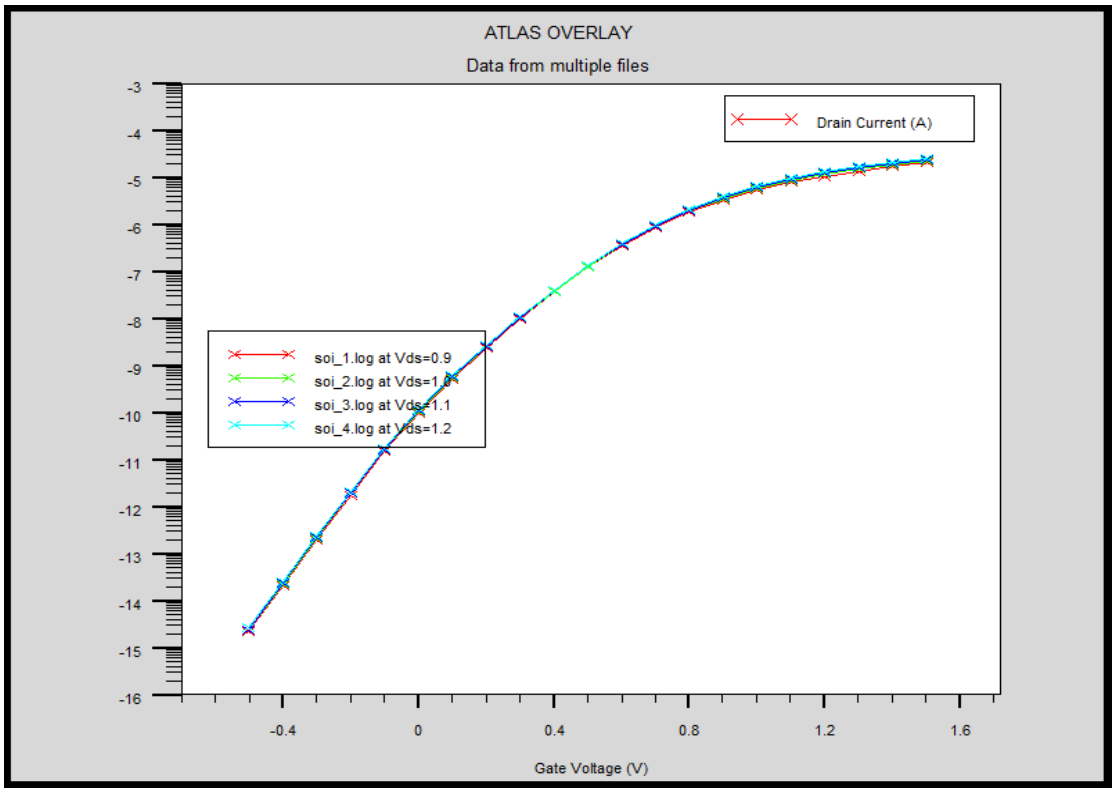


Figure 4.11: Log I_D versus V_{gs} curves of 90nm PD SOI nMOSFET with LDD implantation at different drain voltages

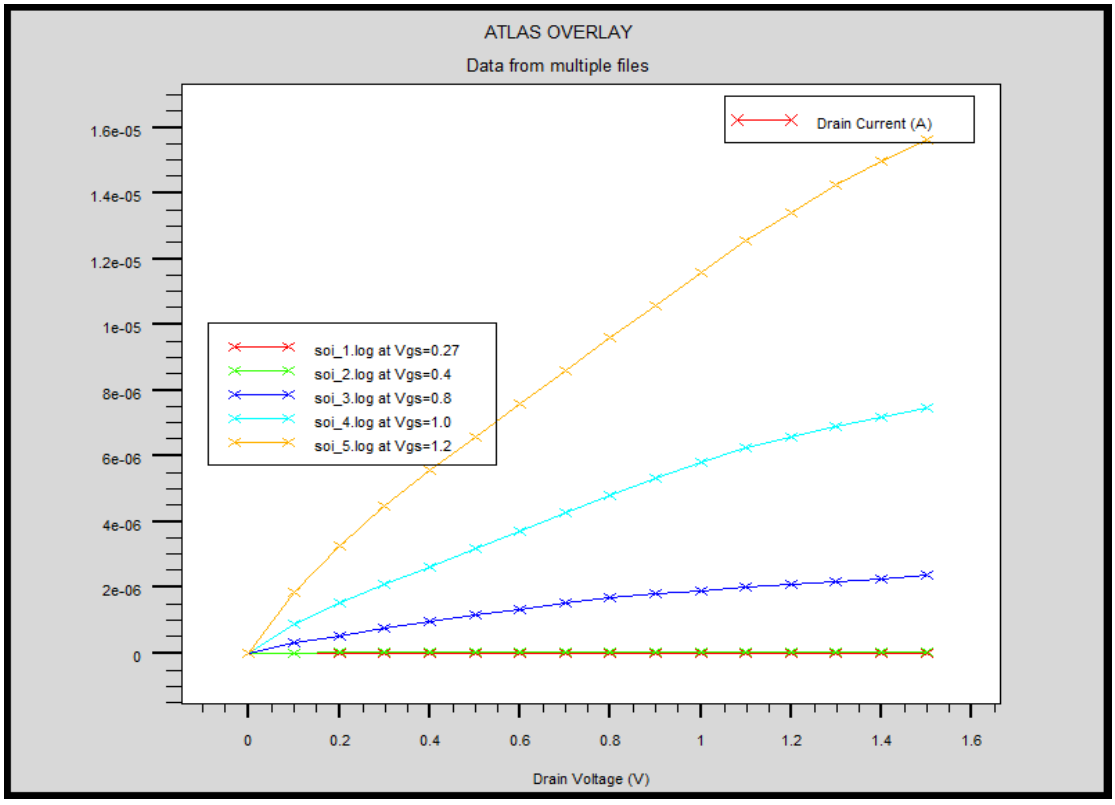


Figure 4.12: I_D versus V_{ds} curves of 90nm PD SOI nMOSFET with LDD Implantation at different gate voltages

4.4 Electrical Characteristics of 90nm PD SOI nMOSFET with LDD and Halo Implantation

4.4.1 Drain Current versus Gate Voltage (I_D vs. V_{gs})

Figure 4.13 shows the curves of I_D vs. V_{gs} for PD SOI nMOSFET with LDD and halo implantation at different drain voltages (0.9, 1.0, 1.1, and 1.2).

4.4.2 Subthreshold Characteristics (log I_D vs. V_{gs})

Figure 4.14 shows the curves of log I_D vs. V_{gs} for PD SOI nMOSFET with LDD and halo implantation at different drain voltages (0.9, 1.0, 1.1 and 1.2).

4.4.3 Drain Current versus Drain Voltage (I_D vs. V_{ds})

Figure 4.15 shows the curves of I_D vs. V_{ds} for PD SOI nMOSFET with LDD and halo implantation at different gate voltages (0.27, 0.4, 0.8, 1.0, and 1.2).

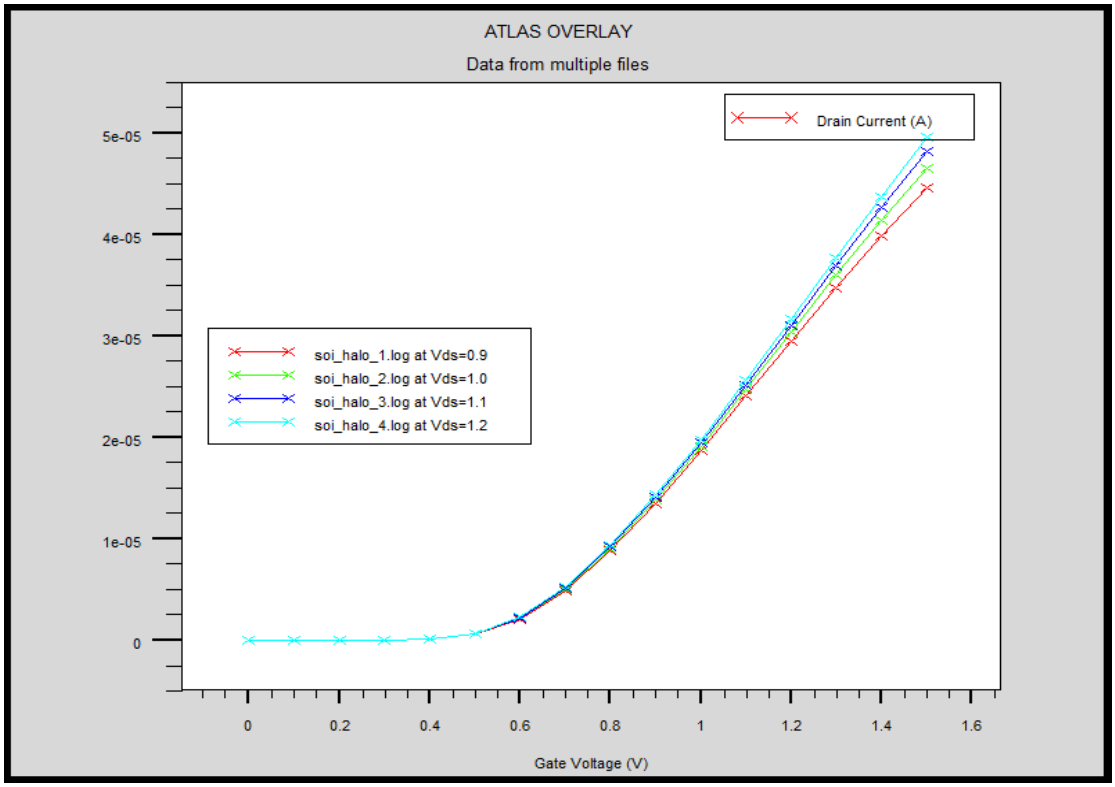


Figure 4.13: I_D versus V_{gs} curves of 90nm PD SOI nMOSFET with LDD and halo Implantation at different drain voltages

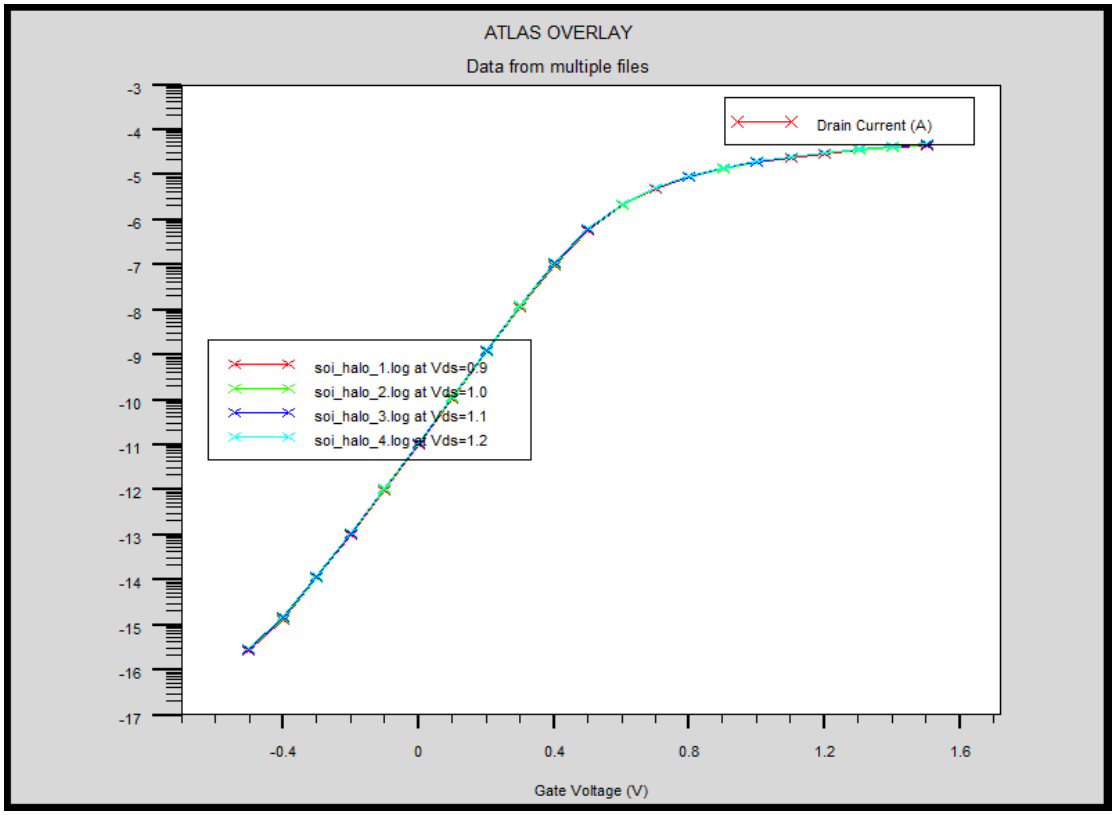


Figure 4.14: Log I_D versus V_{gs} curves of 90nm PD SOI nMOSFET with LDD and halo Implantation at different drain voltages

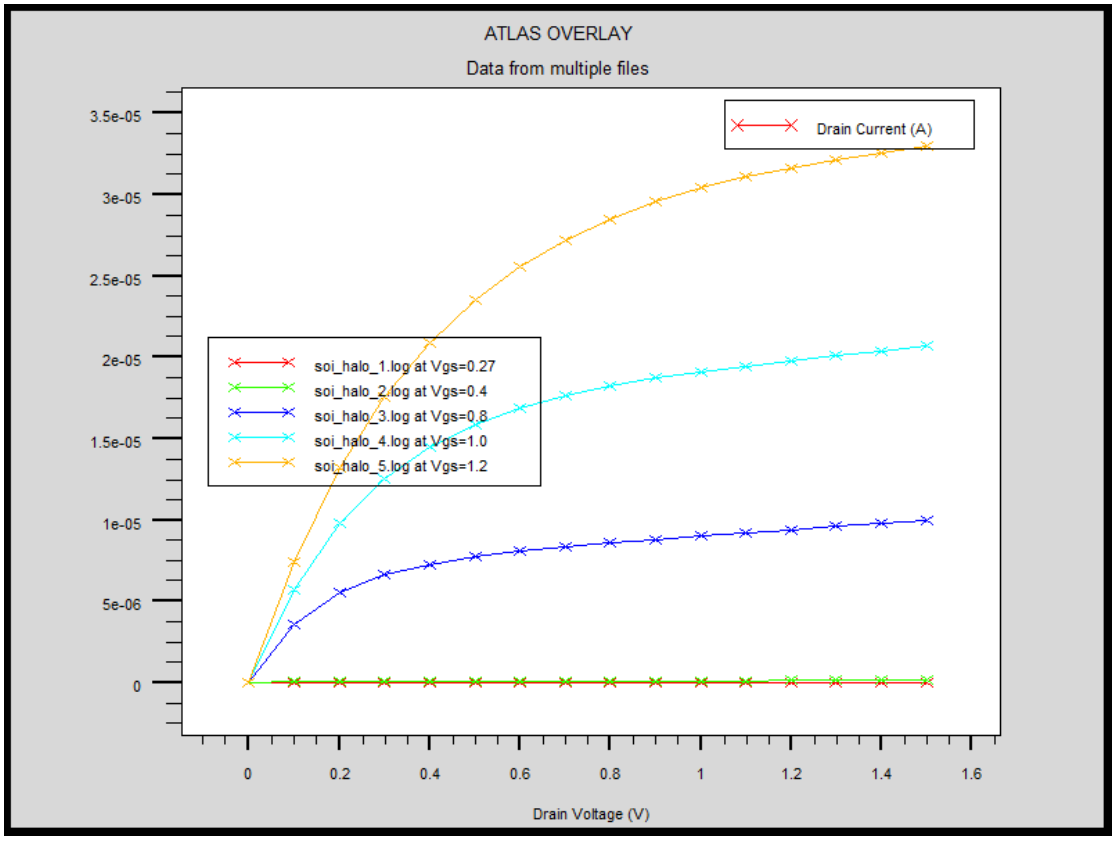


Figure 4.15: I_D versus V_{ds} curves of 90nm PD SOI nMOSFET with LDD and halo Implantation at different gate voltages

4.5 Comparison of Results

PD SOI nMOSFET with LDD implantation has less leakage than 90nm bulk-Si nMOSFET. For further reduction of leakage current in PD SOI nMOSFET halo implantation is done. Due to halo implantation leakage current is reduced. From the results of above plots, the leakage current in different types of MOSFET are compared in Table 4.1.

Table 4.1
Comparison of leakage current in bulk-Si, PD SOI with LDD implantation and PD SOI with LDD and halo implantation

Type of nMOSFET	Bulk-Si	PD SOI with LDD implantation	PD SOI with LDD and halo implantation
Technology node (nm)	90	90	90
Threshold voltage (V)	0.35	0.25	0.29
Off current (nA)	100	0.1	0.01
Saturation current **(µA)**	45.82	5.33	18.70

4.6 Drain Current in Write and Read Operation for SOI DRAM

Figure 4.16 shows the I_D versus V_{gs} characteristics of PD SOI DRAM. For write "1" operation PD SOI nMOSFET is operated in saturation region. For write "0" operation, the pn junction between the body and the drain is forward biased. To read the data nMOSFET is operated in linear region. Bias conditions of PD SOI nMOSFET for memory operation are shown in Table 4.2.

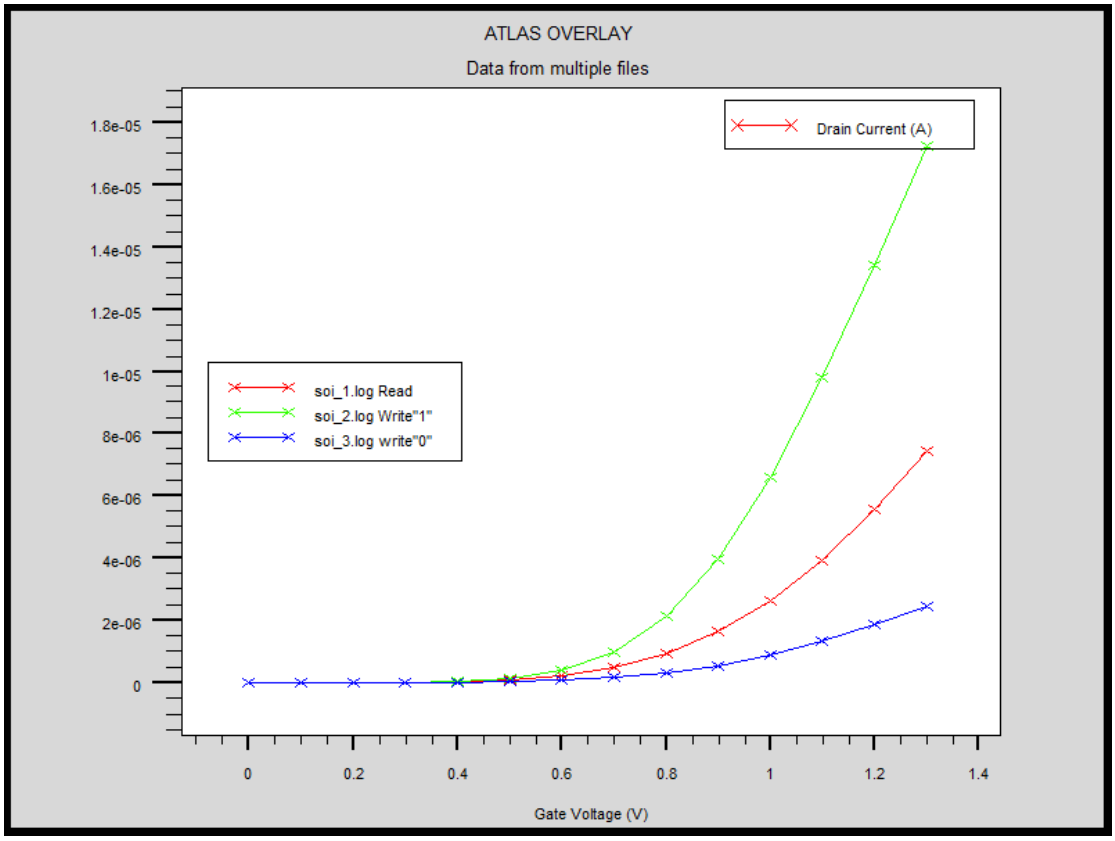


Figure 4.16: Drain current in read, w**rite "1"** and w**rite "0"** operation

Table 4.2
Typical Bias condition for memory operation

	Write "1"	**Write "0"**	Read
Gate voltage (V)	0.28	0.28	0.28
Drain voltage (V)	1.2	0.1	0.4
Source voltage (V)	0	0	0

By verifying the change in drain current during memory operation, we can examine the data state is “0” or “1”. The difference in drain current between state “1” and state “0” is 5.71μA, which is enough to distinguish the state “1” and state “0” in a sense amplifier. The drain current in linear region is reference current (2.6μA). If the drain current (6.5μA) is larger than reference current (2.6μA) than the state “1” is read. To read “0” the drain current (0.87μA) is smaller than reference current (2.6μA).

CHAPTER

5 CONCLUSION AND FUTURE WORK

5.1 Conclusion

A 90nm nMOSFET, PD SOI nMOSFET with LDD implantation and PD SOI nMOSFET with LDD and halo implantation is modelled and simulated using Athena and Atlas module of Silvaco. The effect of different parameters (gate oxide thickness, channel doping and halo implantation) on threshold voltage and leakage current is observed. It is found that on increasing gate oxide thickness, channel doping and halo implantation threshold voltage increases and off current reduces. I_D vs. V_{gs}, log I_D vs. V_{ds} and I_D vs. V_{ds} graphs of bulk nMOSFET and PD SOI nMOSFET with LDD implantation are simulated on Atlas and it is found that PD SOI nMOSFET has less threshold voltage and low leakage current as compared to nMOSFET. For further reduction of leakage current in PD SOI nMOSFET with LDD implantation, a process technique halo implantation is done. It is found that the leakage current is reduced to 90% as compared to PD SOI with LDD implantation. Thus the leakage reduction in PD SOI nMOSFET reduces the power consumption and increases the retention time of DRAM cell.

5.2 Future Scope

As demand for higher density, efficiency and performance of DRAM is continuously increasing, research on other alternatives to conventional device and process is accelerating. For this purpose, this thesis work can be further extended. This section encloses the recommendations for future work. The future scope of work can be divided into two main directions.

First direction is to continue with the SOI structure used in this thesis work. There will be few techniques which will reduce leakage current and improve DRAM performance, which are not discussed in this thesis. To reduce leakage current extra layer of high-k dielectric material and dielectric pocket can be used.

The second direction is to model or simulate a new device structure built on the SOI substrate. This include-

(1) Multi gate SOI MOSFET

(2) FinFET

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APPENDIX

In this Appendix brief introduction of Silvaco tool is given. Silvaco tool is used to design and to predict the performance of semiconductor devices via physics-based simulation.

Simulators

- ATHENA provides the two dimensional simulation of semiconductor processing.
- ATLAS provides general capabilities for physically based two and three-dimensional simulation of semiconductor devices.
- MERCURY is physics based simulator for Field Effect Transistors. It calculates the DC, RF, and noise performance of MESFETs and HEMTs.
- MOCASIM is an advanced three-valley MONTE CARLO simulator designed to generate the transport parameters used in Silvaco's physical device simulators.
- SSUPREM3 is a universal 1-D process simulator with simple device simulation extensions.

Support Tools

- DeckBuild provides an integrated run-time enviroment for Silvaco simulators and tools.
- Optimizer provides interactive capability to optimize various process and device characteristics as well as calibrate model parameters.
- DevEdit provides a GUI-based and command-line structure and mesh editor.
- TonyPlot provides interactive visualization for one and two dimensional devices and Characteristics.
- TonyPlot3D provides interactive visualization for three-dimensional devices.
- Virtual Wafer Fab (VWF) provides an automated wafer manufacturing enviroment for TCAD simulations.

Athena

Athena is a two-dimensional process simulation framework is a comprehensive software tool for modelling semiconductor fabrication processes. Athena provides facilities to perform efficient simulation analysis that substitutes for costly real world experimentation. Athena combines high temperature process modelling such as impurity diffusion and oxidation, topography simulation, and lithography simulation in a single, easy to use framework.

ATLAS

The Atlas Device Simulation Framework enables to device technology engineers to predict the electrical, optical, and thermal behaviour of semiconductor devices via simulation. Atlas provides a physics-based, easy to use, modular, and extensible platform to analyze DC, AC, and time-domain responses for all semiconductor-based technologies in two and three dimensions.

- Accurately characterizes devices for electrical, optical, and thermal performance without costly split-lot experiments.
- Solves yield and process variation problems for optimal combinations of speed, power density, breakdown, leakage, luminosity, and reliablility.
- Easy to use and powerful input syntax.
- Full integration with the Athena process simulation software, DevEdit structure editor and comprehensive visualization package.