DESIGN OF LOW-VOLTAGE HIGH-GAIN CURRENT-MODE OPERATIONAL AMPLIFIER

Thesis Submitted in partial fulfillment of the requirements
for the degree of

Master of Technology (VLSI Design & CAD)

Submitted by
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CERTIFICATE

I hereby declare that the work which is being presented in the thesis entitled "**DESIGN OF LOW-VOLTAGE HIGH-GAIN CURRENT-MODE OPERATIONAL AMPLIFIER**" in the partial fulfillment of the requirements for the award of degree of **Master of Technology in VLSI Design & CAD at Thapar University, Patiala** is an authentic record of my own work carried under the supervision of **Mr. Mohd. Iliyas,** Project Faculty, Department of Electronics & Communication Engineering and refers other researcher's work which are duly listed in the reference section.

The matter embodied in this thesis has not been submitted for the award of any other degree of this or any other university.

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This is to certify that the above statement made by the candidate is correct and true to the best of my knowledge.

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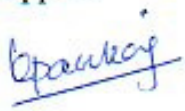


Pankaj Kumar

To my parents, for their never-ending support and the sense of security they have given when I wanted it most; my brothers for encouraging me and convincing me to believe in myself and for always believing in me even when I did not; little kids Monalisa and Aditya who will always be dear to me. They have waited so long for this moment to come true; I am glad that their waiting has finally been rewarded.

ABSTRACT

In this thesis a high-gain current-mode operational amplifier has been designed which is current-mode counterpart of traditional voltage-mode operational amplifier. It has been implemented using a transimpedance input stage followed by a transconductance output stage. Negative feedback around the high-gain current operational amplifier (COA) produces an accurate closed-loop current gain insensitive to process, supply and temperature variations. An analysis of the COA is presented along with possible applications. The design has been implemented on UMC 0.18 μm CMOS n-well process. The current operational amplifier exhibits an open-loop differential gain of 65.38 dB with the unity gain frequency of 353.60 MHz and a settling time of 5.90 ns.

The applications of the COA include the implementation of instrumentation amplifier, current comparator with hysteresis, gyrator, and differential switched-current filter.

TABLE OF CONTENTS

LIST OF FIGURES

LIST OF TABLES

LIST OF SYMBOLS

V_{DD}	Supply Voltage
C_{gs}	Gate to Source Capacitance
C_{gd}	Gate to Drain Capacitance
C_{db}	Drain to Substrate capacitance
g_{mi}	Transconductance of MOSFET
r_{oi}	Output Resistance
g_{oi}	Output Conductance
i_o	Output Current
i_{in}	Input Current
v_o	Output Voltage
v_{in}	Input Voltage
z_o	Output Impedance
z_{in}	Input Impedance
ω_p	Pole Frequency
ω_{in}	Input Pole Frequency
ω_o	Output Pole Frequency
R_s	Source Resistance
C_{in}	Input Capacitance
J_i	Strength of Current Source
$S_{V_{DD}}^{i_o}$	Supply Voltage Sensitivity

W	Width of MOSFET
L	Length of MOSFET
s	Complex Frequency

NOMENCLATURE

VOA	Voltage operational amplifier
COA	Current operational amplifier
CMRR	Common mode rejection ratio
PSRR	Power supply rejection ratio
TT or tt	Typical NMOS Typical PMOS
FF or ff	Fast NMOS and fast PMOS
SS or ss	Slow NMOS and slow PMOS
SF or snfp	Slow NMOS and fast PMOS
FS or fnsp	Fast NMOS and slow PMOS

CHAPTER

1

INTRODUCTION

Since the introduction of Integrated Circuits, the operational amplifier has served as the basic building block in analog circuit design. Voltage-mode operational amplifier circuits have limited bandwidth at high closed-loop gains due to the constant gain-bandwidth product. Furthermore, the limited slew rate of the operational amplifier affects the large-signal, high frequency operation. For wide bandwidth, low-power consumption and low-voltage operation are needed simultaneously and the Voltage-Mode Operational amplifier easily becomes too complex. Therefore, there is a growing need for new, low-voltage analog circuit techniques.

1.1 MOTIVATION FOR CURRENT-MODE CIRCUIT DESIGN

One procedure for finding alternative, preferably simpler, circuit realizations is to use current signals rather than voltage signals for signal processing [1, 2]. MOS transistors in particular are more suitable for processing currents rather than voltages because the output signal is current both in common-source and common-gate amplifier configurations and common-drain amplifier configuration is almost useless at low supply voltages because of the bulk-effect present in typical CMOS processes. Moreover, MOS current mirrors are more accurate and less sensitive to process variation than bipolar current mirrors because with the latter the base currents limit the accuracy. Therefore, at the very least, MOS transistor circuits should be simplified by using current signals in preference to voltage signals. For this reason, integrated current-mode system realizations are closer to the transistor level than the conventional voltage-mode realizations [2].

When signals are widely distributed as voltages, the parasitic capacitances are charged and discharged with the full voltage swing, which limits the speed and increases the power consumption of voltage-mode circuits. Current-mode circuits cannot avoid

nodes with high voltage swing either but these are usually local nodes with less parasitic capacitances [3]. Therefore, it is possible to reach higher speed and lower dynamic power consumption with current-mode circuit Techniques.

When the signal is conveyed as a current, the voltages in MOS transistor circuits are proportional to the square root of the signal, if saturation region operation is assumed for the devices. Similarly, in bipolar transistor circuits the voltages are proportional to the logarithm of the signal. Therefore, a compression of voltage signal swing and a reduction of supply voltage are possible. This feature is utilized for example in log domain filters, switched current filters, and in non-linear current-mode circuits in general [3]. Unfortunately, as a consequence of the device mismatches this non-linear operation may generate an excessive amount of distortion for applications with high linearity requirements. Thus, in certain current-mode circuits, linearization techniques are utilized to reduce the nonlinearity of the transistor transconductance, in which case the voltage signal swing is not reduced. However, new solutions invariably entail new problems. The compression of the voltage signal swing, for example, increases sensitivity to mismatches. Similarly, a large amount of current-mode circuits require advanced complementary bipolar integration processes utilizing vertical npn- and pnp- transistors with a high unity gain frequency, circuits which need excessively high supply voltages in order to be useful in most battery operated applications. Furthermore, some current-mode techniques such as the current feedback are very old and are used as enhanced voltage-mode signal processing building blocks rather than as true current-mode signal processing building blocks. At radio frequencies, current-mode circuit techniques are limited to on chip signal processing in integrated circuits as off chip impedance levels are fixed, typically $50\,\Omega$. However, the aggressive scaling of integration technologies ensures that current-mode circuit techniques will remain useful in the future [3].

1.2 DESIGN SPECIFICATIONS

In this work, a CMOS current operational amplifier (COA) with fully differential input and differential output has been designed and implemented from a differential current mirror input transimpedance stage followed by a differential output transconductance gain stage. This configuration is the current-mode counterpart of the traditional voltage

operational amplifier (VOA). The required specifications are given in the following table.

Table 1.1 Specifications for the design

Power supply	± 1.5 V
Open-loop gain	> 60 dB
3 dB frequency	> 450 kHz
Unity gain frequency	> 300 MHz
Compensation capacitance	≤5 pF
Phase margin	$> 55^0$
CMRR	> 40 dB
PSRR, vdd(0)	> 50 dBΩ
PSRR, vss(0)	> 50 dBΩ
1% settling time	< 15 ns
Slew rate	≥25 μA/ns

1.3 APPLICATIONS

The current-mode operational amplifier has been designed to measure beam current of MC50 cyclotron in closed-loop configuration. MC50 cyclotron is a variable energy isochronous cyclotron for the acceleration (up to 50 MeV) of light particles, which can be used in the fields of nuclear medicine, physics, biology and engineering. It has been used for neutron irradiation, radioisotope production, cyclotron application research, and preventive maintenance. Operation of MC50 cyclotron is very important because it has produced many radioisotopes for medical uses and developed new nuclear isotopes. In the result, MC50 has contributed to the neutron radiography, development of cyclotron application researches and the nuclear science researches. It has a limited capability in proton beam currents (maximum current 60 μA) for the mass production.

The applications of the COA also include the implementation of instrumentation amplifier, current comparator with hysteresis, gyrator, and differential switched-current filter.

1.4 ORGANIZATION OF THESIS WORK

The thesis is organized as follows:

CHAPTER 1: INTRODUCTION. This chapter gives an idea of need for current-mode circuits, the specifications of the design and its applications.

CHAPTER 2: LITERATURE SURVEY. The topic covers the comparative study of current-mode and voltage-mode circuits with respect to input and output impedance, slew rate, power supply rejection ratio, bandwidth, propagation delay and electrostatic discharge etc. It also covers various current-mode circuit design techniques.

CHAPTER 3: DESIGN AND ANALYSIS OF CURRENT-MODE OPERATIONAL AMPLIFIER. It covers the mathematical analysis of the circuit and its design considerations. The aspect ratios of the transistors of the design and its layout are also given in the chapter.

CHAPTER 4: SIMULATIONS AND RESULTS. A comparison between pre-layout and post-layout results have been discussed. The effect of temperature on different parameters has also been discussed. Comparison has been done at all process corners of simulations.

CHAPTER 5: CONCLUSIONS AND FUTURE SCOPE OF THE WORK. A brief conclusion and possible improvements have been discussed in this chapter.

CHAPTER 2 LITERATURE SURVEY

The information processed by lumped electric networks can be represented by either the nodal voltages or branch currents of the networks. The former are referred to as voltage-mode circuits whereas the latter are known as current-mode circuits. Together, they provide a complete characterization of the behavior of the networks. Voltage-mode circuits have received a much broader attention and found a much wider range of applications as compared with their current-mode counterparts despite the fact that the concept of ideal current-mode circuits, similar to that of ideal voltage-mode circuits, emerged approximately 40 years ago [4,5]. This is reflected by a handful monographs on current-mode circuits but countless texts on voltage-mode circuits. The reasons for such popularity that voltage-mode circuits have been enjoying can be summarized as follows:

(i) The nodal voltage of electric networks can be measured conveniently using voltmeters without modifying the topology and affecting the operation of the networks. On the contrary, the measurement of the branch current of the networks is less convenient and often requires a change of the configuration of the networks or additional circuitry.

(ii) The infinite impedance looking into the gate of MOS transistors makes these devices an ideal choice for the realization of voltage-mode circuits, especially in cascade configurations, such as multi-stage voltage amplifiers.

(iii) The ease to obtain a high voltage gain of voltage-mode circuits using techniques such as cascodes and regulated cascodes.

(iv) High supply voltages available in the past such that low-voltage design was not of a critical concern.

(v) Switching noise was not a critical issue with the presence of a high supply voltage.

(vi) Low speed requirements permit the charge and discharge of nodal capacitors over a long period of time.

The aggressive reduction in the supply voltage and the moderate reduction in the device threshold voltage of CMOS technology have greatly affected the performance of CMOS voltage-mode circuits, typically reflected by a reduced dynamic range, an

increased propagation delay, and reduced low noise margins. The impact of supply voltage reduction on the performance of current-mode circuits, however, is less severe as compared with that of voltage-mode circuits. This is because the design emphasis of current-mode circuits is on branch currents rather than nodal voltages. The usefulness of CMOS current-mode circuits in combating the difficulties arising from the reduction of the supply voltage and the increase in the operation speed has received an increasing attention both from industry and academia recently. The different design focuses of voltage-mode and current-mode circuits, arising from the intrinsic characteristics of nodal voltages and branch currents, result in distinct design principles.

This chapter provides a brief comparison of the characteristics of voltage-mode and current-mode circuits based on input and output impedance, bandwidth, slew rate, propagation delay, supply voltage sensitivity, electrostatic discharge etc. Various current-mode circuit design techniques have also been discussed.

2.1 IDEAL CURRENT-MODE CIRCUITS

An ideal voltage-mode circuit possesses infinite input impedance, zero output impedance, and a constant voltage gain. It can be best represented by an ideal operational amplifier [6]. The infinite input impedance and a zero output impedance of operational amplifiers not only enable a convenient cascade of operational amplifiers without a loading effect, they also ensure that the characteristics of these circuits are determined by the external elements only and are independent of the characteristics of the operational amplifiers.

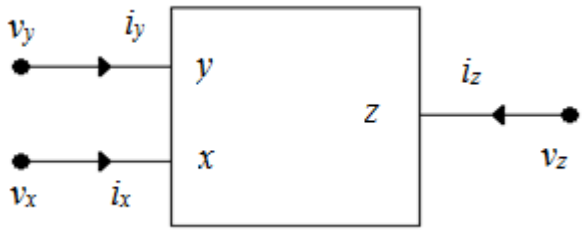


Figure 2.1 Current conveyors.

$$\begin{bmatrix} i_y \\ v_x \\ i_z \end{bmatrix} = \begin{bmatrix} 0 & 1 & 0 \\ 1 & 0 & 0 \\ 0 & \pm 1 & 0 \end{bmatrix} \begin{bmatrix} v_y \\ i_x \\ v_z \end{bmatrix}$$

Figure 2.2 CCI± Current conveyers.

$$\begin{bmatrix} i_y \\ v_x \\ i_z \end{bmatrix} = \begin{bmatrix} 0 & 0 & 0 \\ 1 & 0 & 0 \\ 0 & \pm 1 & 0 \end{bmatrix} \begin{bmatrix} v_y \\ i_x \\ v_z \end{bmatrix}$$

Figure 2.3 CCII± Current conveyers.

Unlike ideal voltage-mode circuits, an ideal current-mode circuit has the characteristics of zero input impedance, infinite output impedance, and a constant current gain. Because current amplification will result in a high level of static power consumption, the current gain of ideal current-mode circuits is set to unity historically. The first ideal current-mode circuits are the first generation current conveyors, denoted by CCI±, where the polarities specify whether the direction of the output current is the same as that of the current flowing into node *x* or not [5]. As shown in Figure 2.1, the current conveyor has three terminals: the current input terminal *x*, the control terminal *y* and the output terminal *z,* and is characterized by the equations given in Figure 2.2. The node *y* is the control node who's current and voltage are identical to those of the input node *x.* The impedance looking into nodes *x* and *y* is zero ideally. Node *z* is the output node with infinite output impedance. The application of CCI± becomes difficult because both nodes *x* and *y* have zero input impedance ideally in order to sink currents. The control node y needs to take a control current rather than a control voltage, which is usually difficult to obtain in practical designs. To alleviate this problem, the second generation current conveyors, denoted by CCII±, where the control node *y* is changed from a current control node to a voltage control node, were proposed [5]. The behavior of CCII± is characterized by the equation given in Figure 2.3. The voltage control node *y* has infinite input impedance ideally. The current control node *x*, on the other hand, has zero input impedance ideally, enabling a current to flow into the node without any resistance. Because the output of the conveyer is a current, the load of the conveyer must be of a low impedance, $v_z = 0$ holds ideally.

Similar to operational amplifiers that have numerous practical implementations, current conveyors can also be realized in a number of ways and new CCII± with an emphasis on speed, power consumption, and low supply voltage are emerging [2]. In addition, the applications of CCII± bear a strong resemblance to those of operational amplifiers where the characteristics of systems employing CCII± are determined by the passive elements external to CCII± only. CCII± have found a broad spectrum of applications such as active filters, impedance conversion, oscillators, and instrumentation amplifiers, to name a few.

2.2 CHARACTERISTICS OF CURRENT-MODE CIRCUITS

In this section, comparison between voltage-mode and current-mode circuit with respect to input/output impedance, bandwidth, slew rate, propagation delay, power supply sensitivity etc. have been discussed.

2.2.1 INPUT AND OUTPUT IMPEDANCES

It was pointed out earlier that a voltage-mode circuit is featured by large input impedance and low output impedance. On the contrary, a current-mode circuit possesses low input impedance and high output impedance. The loading effect arising from the finite output impedance of current-mode circuits or equivalently the non-zero input impedance can be studied using Figure 2.4 where the input source is represented by its Norton equivalent. The load current is given by

$$i_{o2} = \frac{1}{1+\frac{z_{in}}{z_o}} i_o \approx \left(1-\frac{z_{in}}{z_o}\right) i_o , \tag{2.1}$$

where z_o and z_{in} are the output impedance of the driving stage and the input impedance of the driven stage, respectively. Note that $z_{in} << z_o$ was assumed in simplifying (2.1). To minimize the loading effect, $z_{in} << z_o$ is required for current-mode circuits. Similarly, when the input is represented by its Thevenin equivalent, the loading effect of voltage mode circuits can be studied using Figure 2.4 with the load voltage

$$v_{o2} = \frac{1}{1+\frac{z_o}{z_{in}}} \approx (1-\frac{z_o}{z_{in}}) v_o \ . \tag{2.2}$$

To minimize the loading effect, $z_{in} >> z_o$ is required for voltage-mode circuits [6].

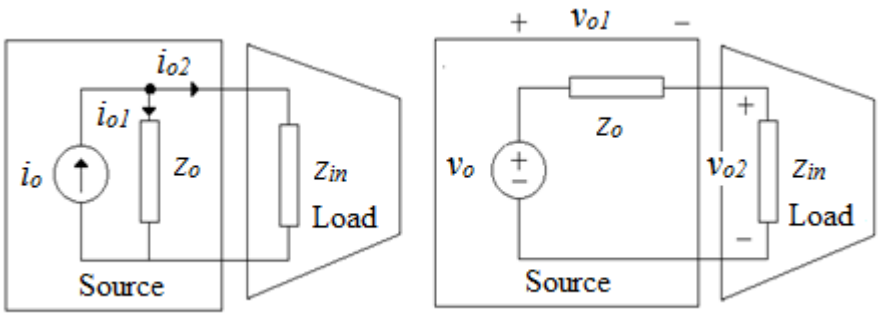
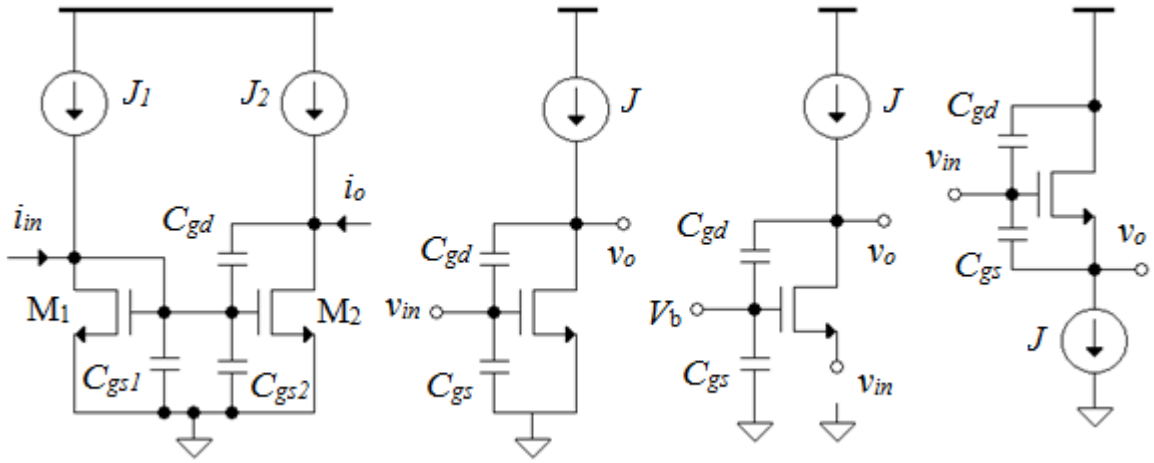


Figure 2.4 Loading effect in current-mode circuits and voltage-mode circuits.

2.2.2 BANDWIDTH

The bandwidth of voltage-mode and current-mode circuits can be best compared using the building blocks of voltage/current mode circuits shown in Figure 2.5.



(a) (b) (c) (d)

Figure 2.5 Bandwidth comparison of voltage-mode and current-mode circuits, (a) Basic current mirror, (b) Common-source amplifier, (c) Common-gate amplifier, (d) Source follower.

Because a well designed current-mode circuit has large output impedance and small input impedance, the load impedance $z_L \approx 0$ holds. As a result, M_2 of the basic current mirror is not subject to Miller effect. The only pole of the basic current mirror is at the gate of $M_{1\sim2}$ with the pole frequency given by

$$\omega_p \approx \frac{g_{m1}}{C_{gs1} + C_{gs2} + C_{gd2}} \quad . \tag{2.3}$$

Due to the existence of the floating gate-drain capacitor C_{gd}, the common-source configuration is subject to Miller effect with Miller capacitances $C_{m1} = C_{gd}(1 + g_m r_o)$ at the gate and $C_{m2} = C_{gd}(1 + \frac{1}{g_m r_o})$ at the drain, where r_o and g_m are the output impedance and transconductance of the transistor, respectively. The pole at the input called Miller pole, is given by

$$\omega_{in} = \frac{1}{R_s(C_{gs} + C_{gd}(1 + g_m r_o))}, \tag{2.4}$$

where R_s is the resistance of the source. The output pole is estimated from

$$\omega_o \approx \frac{1}{r_o(C_{gd} + C_{in})}, \tag{2.5}$$

where C_{in} is the input capacitance of the load stage. The common-gate configuration is not subject to Miller effect due to the absence of floating capacitors. The pole at the input is given by

$$\omega_{in} \approx \frac{1}{R_s C_{gs}} \quad , \tag{2.6}$$

and the pole at the output is computed from

$$\omega_o \approx \frac{1}{r_o(C_{gd} + C_{in})} \quad . \tag{2.7}$$

The source follower is also free of Miller effect simply because its small signal voltage gain is approximately unity. The Miller capacitances at the gate and source are given by $C_{m1} \approx C_{m2} \approx 0$. The pole at the input is given by

$$\omega_{in} \approx \frac{1}{R_s C_{gd}} \quad , \tag{2.8}$$

and the dominant pole at the output is given by

$$\omega_o \approx \frac{1}{r_o C_{in}}. \tag{2.9}$$

For practical applications, C_{in} and r_o are often large; the dominant pole of the common-source, common-gate, and source follower amplifiers is usually at the output node. The pole frequency of the basic current mirror is therefore smaller as compared with the pole frequency of the basic voltage-mode amplifiers [6].

2.2.3 SLEW RATE

The slew rate of voltage-mode and current-mode circuits is compared using the common-source configuration and the basic current mirror shown in Figure 2.6. When a square waveform current is applied to the basic current mirror, because M_1 is in the saturation, i_{DS1} is independent of v_{DS1} when the channel length modulation is neglected. The rate of the change of the output current depends upon how fast $C_{gs1\sim2} = C_{gs1} + C_{gs2}$ is charged or equivalently how fast the gate voltage of $M_{1\sim2}$ rises. Because

$$C_{gs1\sim2}\frac{dv_{GS1\sim2}}{dt} + \frac{1}{2}\mu_n C_{ox}\frac{W}{L}(v_{GS1} - V_T)^2 = J_1 + i_{in}, \tag{2.10}$$

$v_{GS1\sim2}$ increases with i_{in}. For fixed biasing currents, the larger the amplitude of the input, the higher the slew rate of the output current.

For voltage mode circuits, the slew rate is usually determined by the output stage because of the large width of the transistors in the output stage and the large capacitance of the load. Consider the common-source amplifier, when a sufficiently low voltage V_{min} is applied to the input, the transistor switches off and C_o is charged by J only, we have

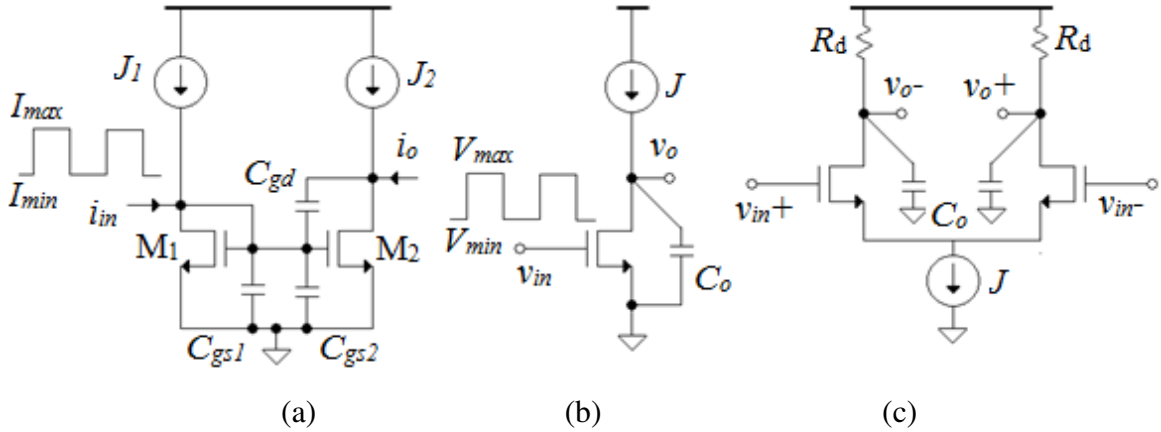
$$\left[\frac{dv_o}{dt}\right]_{rise,\max} = \frac{J}{C_o}. \tag{2.11}$$

When $V_{in} = V_{max}$, C_o is discharged via the transistor with the slew rate

$$\left[\frac{dv_o}{dt}\right]_{fall,\max} = \frac{1}{R_{on}C_o}, \tag{2.12}$$

where R_{on} is the channel resistance of the transistor in the triode region. The preceding results reveal that the slew rate of common-source amplifier is set by the biasing current,

the width of the transistor, and the output capacitance. It is independent of the amplitude of the input voltage. A similar conclusion can be drawn for the voltage mode differential pair configuration [6].



(a) (b) (c)

Figure 2.6 Slew rate comparisons of voltage-mode and current-mode circuits, (a) Basic current mirror, (b) Common-source amplifier, (c) Basic differential pair.

2.2.4 PROPAGATION DELAY

For digital circuits, the average propagation delay is a widely used figure-of-merit depicting the transient behavior of the circuits. It is directly related to the swing of the signal [6]. Neglecting both the resistance and inductance, the average rising (falling) time of the voltage of a node, denoted by Δt, is determined from

$$C_n(\Delta v_n) = \int_0^{\Delta t} i(t)dt = I_{avg}\Delta t\,, \tag{2.13}$$

where I_{avg} is the average current charging/discharging the node, C_n is the capacitance of the node, $i(t)$ is the net current flowing into/out the node, and Δv_n is the voltage swing of the node. Eq. (2.13) reveals that a small propagation delay can be achieved by either minimizing the swing of the voltage of the node or maximizing the current charging and discharging the capacitance of the node. For voltage mode circuits, Δv_n is constrained by the signal to noise ratio requirements and must be kept sufficiently large, resulting in a slow transient response.

Unlike voltage-mode circuits, the information carriers of current-mode circuits are branch currents. The variation of nodal voltages can be kept small as long as the current of the branches associated with the nodes is large. Consider Figure 2.7, from

$$\Delta v_n = z_n \left(\sum_{b_1=1}^{B_1} \Delta i_{in,b1} - \sum_{b_2=1}^{B_2} \Delta i_{o,b2} \right), \tag{2.14}$$

where z_n is the impedance of the node, B_1 and B_2 are the number of input and output branches connected to the node, respectively, we conclude that for a given Δv_n, a large current variation can be obtained as long as z_n is kept small. The small nodal voltage variation of current-mode circuits lowers the amount of time needed to charge/discharge C_n, resulting in a faster transient response. This is one of the key advantages of current-mode circuits [6].

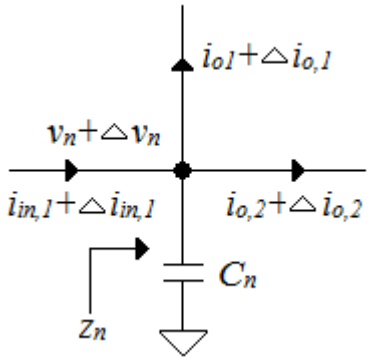


Figure 2.7 Variation of nodal voltages and branch currents of current-mode circuits.

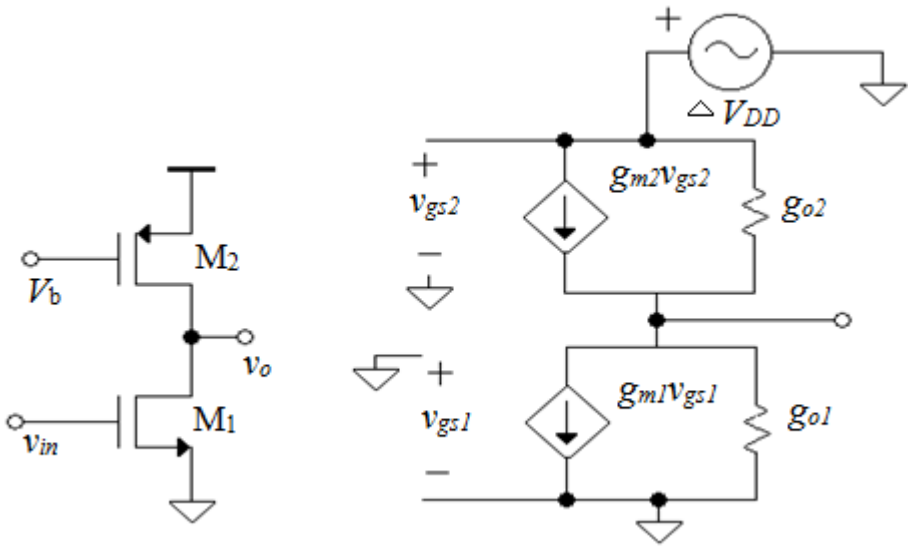
2.2.5 SUPPLY VOLTAGE SENSITIVITY

The effect of V_{DD} and ground fluctuations on the output voltage (current) of CMOS circuits is of a critical concern in mixed-mode circuits because both analog and digital circuits often share the same supply voltage and ground. Supply voltage sensitivity, defined as

$$S_{v_{DD}}^{v_o} = \frac{\partial v_o}{\partial V_{DD}}, \tag{2.15}$$

is a measure of the effect of the variation of the supply voltage on the response of the circuits. Assume the supply voltage is changed from V_{DD} to $V_{DD} + \Delta V_{DD}$, where ΔV_{DD} is a

random variable with zero mean. For practical circuits, $\Delta V_{DD} << V_{DD}$ holds and the small-signal analysis approach can be employed to analyze the effect of ΔV_{DD} on the response of the circuits. Consider the common-source amplifier shown in Figure 2.8(a). M_2 is biased in the saturation and



(a) (b)

Figure 2.8 Supply voltage sensitivity analysis of voltage-mode circuits, (a) Common-source amplifier, (b) Small-signal equivalent circuit.

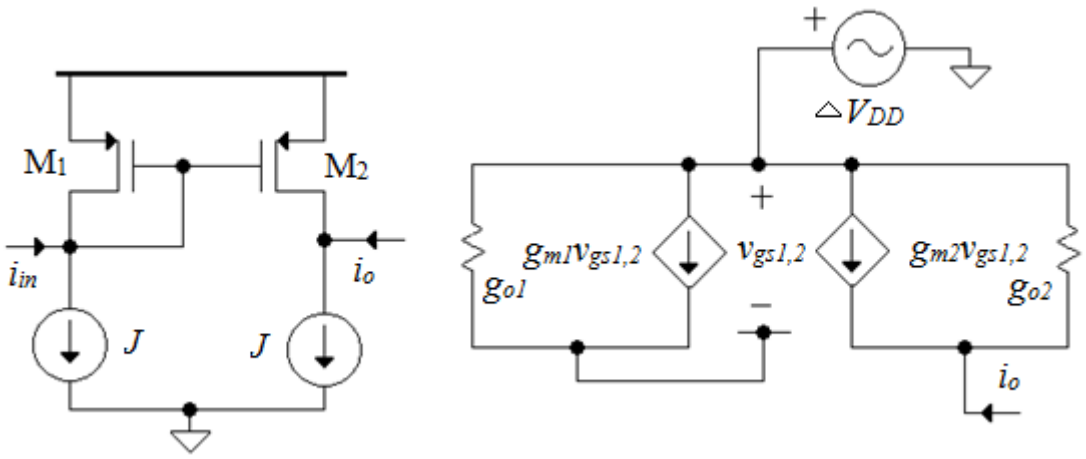
behaves as a current source. The small-signal equivalent circuit of the amplifier for supply voltage sensitivity analysis with junction capacitances neglected is shown in Figure 2.8(b). At low frequencies where C_{gs} and C_{gd} are neglected, we have

$$S_{V_{DD}}^{v_o} \approx \frac{g_{m2}}{g_{o1}+g_{o2}} = (r_{o1} \| r_{o2}) g_{m2} . \tag{2.16}$$

The above result shows that ΔV_{DD} is directly amplified with a large voltage gain. It is worth noting that Figure 2.8(a) is the common-gate amplifier with v_{in} the biasing voltage of M_1, which behaves as a current source, and ΔV_{DD} the input of the common-gate configured M_2. Now let us consider the circuit shown in Figure 2.9. The load is a current mirror with the source current provided by an ideal current source J. Using a small-signal analysis, it can be shown that

$$S_{V_{DD}}^{i_o} = g_{o2} . \tag{2.17}$$

As compared with (2.16), because $g_o << g_m$ the current-mode circuit is less sensitive to the fluctuation of the supply voltage. Also seen is that the effect of ΔV_{DD} on v_o is mainly due to the finite output impedance r_{o2} of the load current mirror [6].

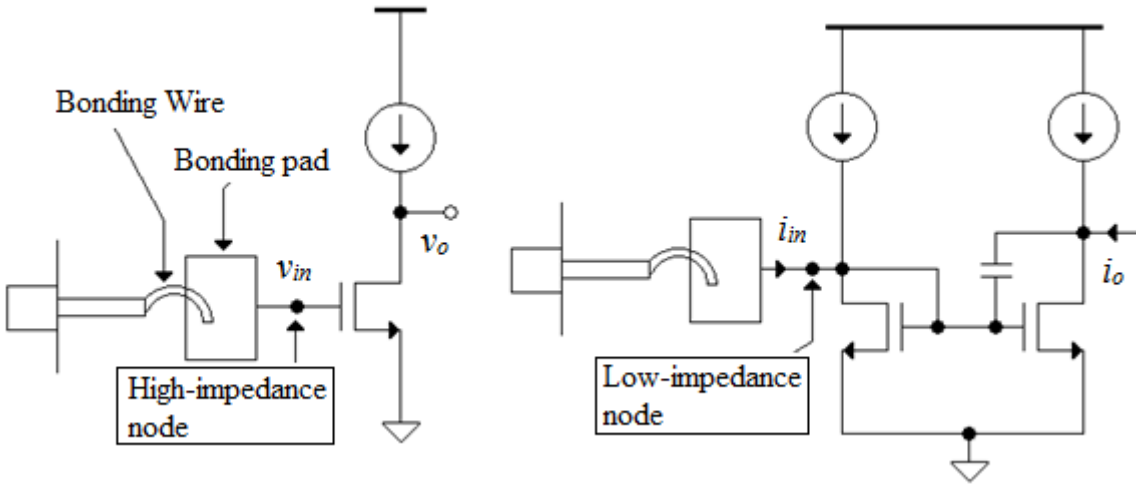


(a) (b)

Figure 2.9 Supply voltage sensitivity analysis of current-mode circuits, (a) Current mirror amplifier, (b) Small-signal equivalent circuit.

2.2.6 ELECTROSTATIC DISCHARGE

A large number of ESD (electrostatic discharge) induced damages of MOSFETs is due to the breakdown of the gate oxide insulator, especially when the thickness of the gate oxide t_{ox} is scaled down aggressively in deep sub-micron CMOS technologies.



(a) (b)

Figure 2.10 ESD sensitivity, (a) Voltage-mode circuits, (b) Current-mode circuits.

Voltage-mode circuits are particularly vulnerable to ESD strikes as the input node of these circuits is usually the gate of MOSFETS, a high impedance node [6]. No low impedance paths from the input pads to the ground exist to discharge electrostatic charge accumulated at the pads, as shown in Figure 2.10(a). On the contrary, the low impedance characteristics of the input pads of current-mode circuits prevent the accumulation of static charge at the pads, as shown in Figure 2.10(b).

2.3 DESIGN TECHNIQUES FOR CURRENT-MODE CIRCUITS

The rapid down scale of the feature size of MOS devices, the aggressive reduction in the supply voltage, and the moderate reduction in the threshold voltage of modern CMOS technologies have greatly affected the performance of CMOS current-mode circuits, reflected by a small dynamic range, a reduced effective gate source voltage, a low device output impedance, and an increased level of device mismatches. This section examines the design techniques that improve the performance of low-voltage CMOS current-mode circuits.

2.3.1 BASIC CURRENT AMPLIFIERS

The schematic of basic CMOS current amplifiers is shown in Figure 2.11(a). Because a well-designed current-mode circuit possesses small input impedance and large output impedance, it is reasonable to assume that the load impedance is sufficiently small. As a result, M_2 is not subject to Miller effect. Under a perfect matching condition and neglecting the channel length modulation, the current transfer function is given by

$$\frac{I_o(s)}{I_{in}(s)}\frac{A}{\frac{s}{\omega_b}+1}, \tag{2.18}$$

where $A=\frac{g_{m2}}{g_{m1}}$ and

$$\omega_b \approx \frac{g_{m1}}{C_{gs1}+C_{gs2}+C_{gd2}}. \tag{2.19}$$

The input impedance of the basic current amplifier is given by

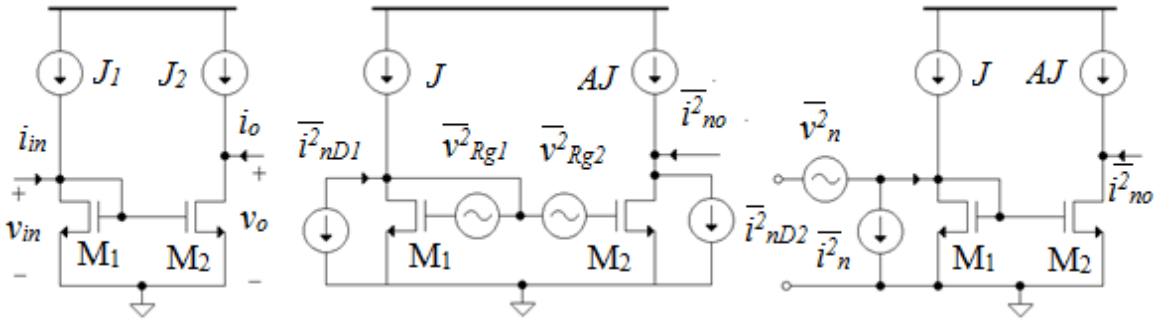
$$z_{in}(s) = \frac{1}{g_{m1}}\left(\frac{1}{\frac{s}{\omega_b}+1}\right). \tag{2.20}$$

The input impedance can be lowered by either increasing the width of M_1 or increasing the biasing current. The former lowers the bandwidth whereas the latter increases the static power consumption.

The output impedance is given by $z_o \approx r_{o2}$ approximately. The output impedance of MOSFETs in deep sub-micron CMOS technologies is small. The finite output impedance of MOSFETs gives rise to a change of the output current I_o when the output voltage v_o varies. Because $i_o = g_{m2}v_{gs} + g_{o2}v_o$ and $i_{in} = (g_{m1} + g_{o1})v_{gs}$, we have

$$\begin{aligned} i_o &= \frac{A}{1+\frac{g_{o1}}{g_{m1}}} i_{in} + g_{o2}v_o \\ &\approx A(1-\frac{g_{o1}}{g_{m1}})i_{in} + g_{o2}v_o \\ &\approx Ai_{in} + g_{o2}v_o. \end{aligned} \tag{2.21}$$

The second term on the right hand side of (2.21) is the output error current.



(a) (b) (c)

Figure 2.11 (a) Basic current amplifier, (b) Noise source in basic current amplifier, (c) input-referred noise voltage and noise current generators of basic current amplifier.

The noise equivalent circuit of the basic current amplifier is shown in Figure 2.11(b, c). The equivalent channel noise of M_1 and M_2 denoted by $\overline{i_{n1}^2}$ and $\overline{i_{n2}^2}$ respectively, consists of (i) the thermal noise of the channel and (ii) the thermal noise of the gate resistance that

is referred to the channel. Because circuits of our interests operate at high frequencies, the flicker noise of MOS transistors, which has a typical corner frequency of a few MHz, is neglected. As a result,

$$\overline{i_{n1,2}^2} = 4kT(\gamma + R_{g1,2}g_{m1,2})g_{m1,2}\Delta f \quad , \tag{2.22}$$

where R_g is the gate series resistance, $\gamma \approx 2.5$ for deep sub-micron devices, T is the temperature in Kelvin, and k is Boltzmann constant. For a typical $0.18\,\mu m$ CMOS technology, the sheet resistance of silicided polysilicon (gate) is approximately 8Ω. If the dimension of the gate of a NMOS transistor *is* W = 100 µm and L = 0.18 µm with one-finger layout, then *Rg* ≈ *4.44* kΩ. Assume g_m = 5 mA/V, we have $R_g g_m$ = 22.2. Clearly in this case the noise of the NMOS transistor is dominated by the thermal noise of the gate series resistance. To reduce the thermal noise of the gate series resistance, the multi-finger layout approach becomes mandatory [6, 7]. Consider that 4 fingers are used for the transistor, we have W = 25 µm for each finger. Because these fingers are connected in parallel, $R_g \approx 1.11$ kΩ and $R_g g_m \approx 5.5$ which is comparable to the value of γ. Using conventional approaches for noise analysis, we can show that the power of the input-referred noise voltage and current generators respectively, are given by

$$\overline{v_n^2} = \frac{1}{g_{m1}^2}\left(\frac{\overline{i_{n2}^2}}{A^2}\right)$$

$$\overline{i_n^2} = \overline{i_{n1}^2} + \frac{\overline{i_{n2}^2}}{A^2}. \tag{2.23}$$

where $\overline{v_n^2}$ and $\overline{i_n^2}$ are the mean square values of input referred voltage and current.

2.3.2 OUTPUT IMPEDANCE BOOSTING TECHNIQUES

Different techniques for improving output impedance have been discussed in this section. These techniques include Basic cascode, Self-biased cascode, Wilson Current Mirror and improved Wilson Current Mirror.

2.3.2.1 BASIC CASCODES

It was pointed out in the preceding section that the output error current of the basic current amplifiers can be minimized by maximizing the output impedance. Cascode configuration shown in Figure 2.12(a) employs a negative voltage-current feedback to sustain the output current in the presence of a varying output voltage. The output impedance of the cascode current amplifier can be obtained from its small signal equivalent circuit $z_o \approx (g_{m3} r_{o3}) r_{o2}$.

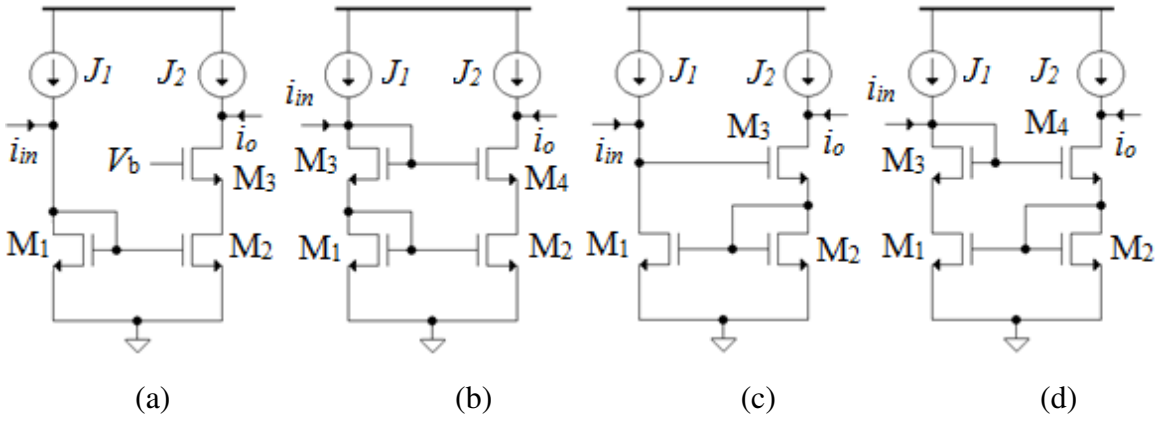


Figure 2.12 (a) Cascode current amplifier with an external biasing voltage V_b, (b) Self-biased cascode current amplifier, (c) Wilson current amplifier, (d) Improved Wilson Current amplifier.

Let us examine the reduction in the output error current from the cascode. Writing KCL at the drain of M_2 yields

$$v_2 = \frac{g_{o3} v_o - g_{m2} v_{in}}{g_{o2} + g_{o3} + g_{m3}} \quad . \tag{2.24}$$

Further $i_{in} = (g_{m1} + g_{o1}) v_{in}, i_o = -g_{m3} v_2 + g_{o3}(v_o - v_2)$,

And assume $g_m >> g_o$, we have

$$i_o \approx A i_{in} + (\frac{g_{o2}}{g_{m3} r_{o3}}) v_o \quad . \tag{2.25}$$

A comparison of (2.21) and (2.25) reveals that the output current error of the cascode current amplifier is $g_{m3} r_{03}$ times lower than that of the basic current amplifier [6]. The

cascode current amplifiers also possess large bandwidth. This is because M_2 are nearly free of Miller effect. The Miller capacitances of M_2 are given by $C_{m1} = C_{gd2}(1 + \frac{g_{m3}}{g_{m2}})$ at the gate and $C_{m2} = C_{gd}(1 + \frac{g_{m2}}{g_{m3}})$ at the drain. M_3 is common-gate configured and is not subject to Miller effect. From the current transfer function

$$\frac{I_o(s)}{I_{in}(s)} = \frac{g_{m2}}{g_{m1}} \frac{1}{s^2(\frac{C_{gs12}C_{gs3}}{g_{m1}g_{m3}}) + s(\frac{C_{gs12}}{g_{m1}} + \frac{C_{gs3}}{g_{m3}}) + 1} \quad , \tag{2.26}$$

we obtain the poles of the system

$$p_{1,2} = \frac{g_{m1}g_{m3}}{2g_{gs12}C_{gs3}} \left\{ -\left(\frac{C_{gs12}}{g_{m1}} + \frac{C_{gs3}}{g_{m3}} \right) + \left(\frac{C_{gs12}}{g_{m1}} - \frac{C_{gs3}}{g_{m3}} \right) \right\}$$

$$= \begin{cases} -\frac{g_{m1}}{C_{gs12}} \\ -\frac{g_{m3}}{C_{gs3}}. \end{cases} \tag{2.27}$$

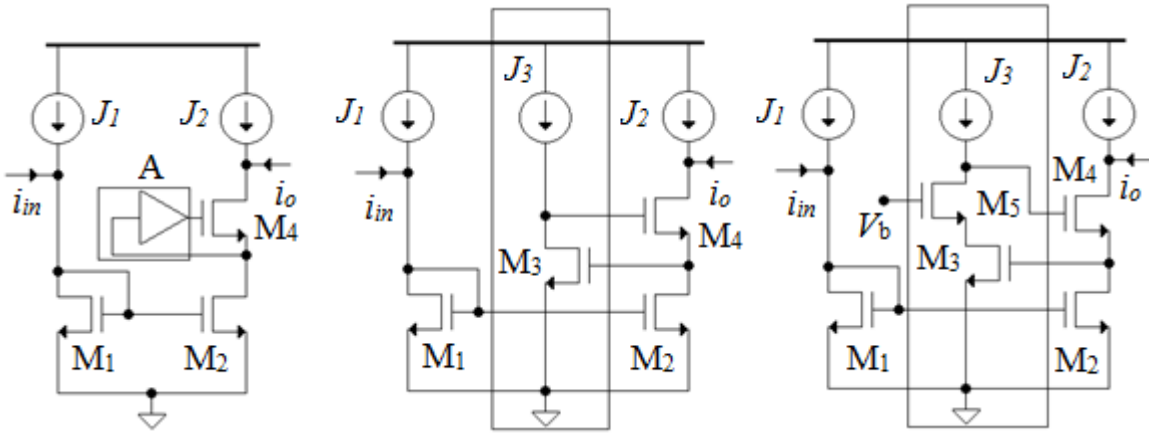
The bandwidth of the cascode current amplifier is the same as that of the basic current amplifier. The biasing voltage can be obtained from the cascode itself, as shown in Figure 2.12(b). The minimum supply voltage of the self-biased cascode current amplifier of Figure 2.12(b) is $2V_T + V_{sat}$ increased from $V_T + V_{sat}$ of the externally biased cascode current amplifier of Figure 2.12(a). Wilson current amplifier shown in Figure 2.12(c) is another variation of cascode current amplifiers. The input impedance at low frequencies is given by $z_{in} = \frac{1}{g_{m1}} + \frac{g_{m2}}{g_{m1}g_{m3}}$. The output impedance of Wilson current amplifier is given by $z_o \approx (\frac{g_{m1}g_{m3}}{g_{m2}}) r_{o3}r_{o1}$, the same output impedance as that of the basic cascode current amplifier. The current gain of Wilson current amplifier is given by

$$\frac{I_o(s)}{I_{in}(s)} = \frac{g_{m2}g_{m3}}{C_{gs12}C_{gs3}} \frac{s\frac{C_{gs12}}{g_{m2}} + 1}{s^2 + s(\frac{g_{m1} + g_{m3}}{C_{gs12}}) + \frac{g_{m1}g_{m3}}{C_{gs12}C_{gs3}}}. \tag{2.28}$$

The current gain in the dc steady state is the same as that of the basic cascode current amplifier. The zero is located at frequency $z = \frac{g_{m2}}{C_{gs12}}$ and the complex conjugate poles are given by $p_{1,2} = \frac{g_{m1}}{C_{gs12}}(-1+j)$ when $M_{1\sim3}$ are identical, resulting in $g_{m1} \sim g_{m3}$, $C_{gs12} = (C_{gs1} + C_{gs2}) \approx 2C_{gs3}$. Its bandwidth is the same as that of the basic current amplifier. Difficulties exist in obtaining an appropriate dc operating point of Wilson current amplifier because of the constraint $V_{DS1} > 2V_T$. This difficulty can be removed by adding another transistor in the input branch, as shown in Figure 2.12(d) [6]. Both the input and output impedances of the improved Wilson current amplifier can be obtained following a similar approach as that for Wilson current amplifier and the results are given by $z_{in} = \frac{1}{g_{m1}} + \frac{g_{m2}}{g_{m1}g_{m4}}$ and $z_o = (g_{m1}r_{o1})r_{o4}$.

2.3.2.2 REGULATED AND MULTI-REGULATED CASCODES

To further increase the output impedance, a negative voltage-voltage feedback amplifier can be employed, as shown in Figure 2.13(a). The amplifier stabilizes the output current I_o when V_o varies. The circuit can be implemented in various ways. Figure 2.13(b) is an implementation using a common-source amplifier.



(a) (b) (c)

Figure 2.13 (a, b) Regulated cascode current amplifiers, (c) Multi-regulated cascade current amplifiers.

The output impedance of the regulated cascode current amplifier of Figure 2.13(a) can be derived from its small signal equivalent circuit

$$r_o = \frac{v_2}{i_T} = r_{o2}r_{o4}\left[\frac{1}{r_{o2}} + \frac{1}{r_{o4}} + r_{o3}g_{m3}g_{m4} + g_{m3}\right]$$
$$\approx A(g_{m4}r_{o4})r_{o2}, \qquad (2.29)$$

where $A = g_{m3}r_{o3}$ the voltage gain of the auxiliary amplifier.

The output impedance can be further increased by boosting the voltage gain of the auxiliary amplifier. One approach is shown in Figure 2.13(c) where the feedback network itself is now a cascode amplifier. Replacing the term associated with the common source auxiliary amplifier in (2.29) with the gain of the cascode amplifier given by $A_v = -(g_{m3}r_{o3})(g_{m5}r_{o5})$, we obtain the output impedance of the multi-regulated cascode current amplifier

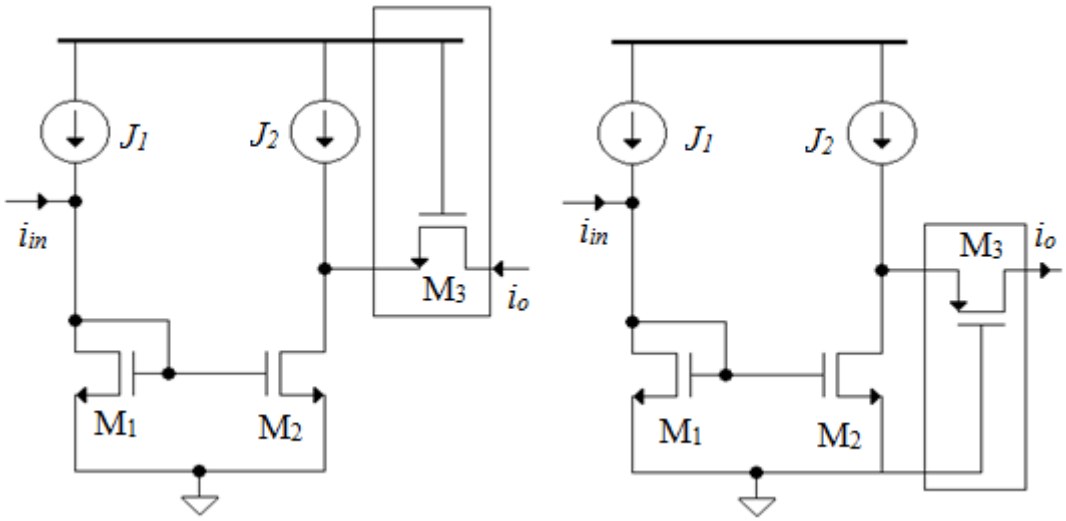
$$r_o = [(g_{m3}r_{o3})(g_{m5}r_{o5})](g_{m4}r_{o4})r_{o2}. \qquad (2.30)$$

It should be noted that the minimum supply voltage of the regulated and multi-regulated cascode current amplifiers is given by $2V_T+V_{sat}$, whereas that of the basic cascode current amplifiers is only $V_T + V_{sat}$ [6].

2.3.2.3 PSEUDO-CASCODES

Regulated and multi-regulated cascodes increase the output impedance, however, at the cost of a higher supply voltage. This is because in order to have large output impedance, the biasing current source J_2 in the output branch of the regulated and multi-regulated cascode current amplifiers must also be cascode configured. To keep the supply voltage low and at the same time to ensure large output impedance, the pseudo-cascode technique shown in Figure 2.14 is used.

Note that in this case, J_2 need not to be implemented in cascode. The minimum supply voltage of the output branch is only $V_T + V_{sat}$. It can be shown that the output impedance of the pseudo-cascode current amplifiers is given by $z_o \approx (g_{m3}r_{o3})r_{o2}$. The added common gate stage has no negative effect on the bandwidth. Pseudo-cascodes are self-biased, making them attractive for low-power applications [6].



(a) (b)

Figure 2.14 Pseudo-cascode current amplifiers.

2.3.2.4 LOW-VOLTAGE CASCODES

Because V_T is usually much larger than V_{sat}, the cascode current amplifier of Figure 2.12(b) can be modified to Figure 2.15(a) to lower the supply voltage requirement while preserving the properties of the cascode current amplifiers. The minimum supply voltage of the low-voltage cascade current amplifier is given by $V_{DD,min} = V_T + V_{sat}$. The input impedance at low frequencies is given by $1/g_{m1}$, which is the same as that of the basic current amplifier. The output branch is the same as the basic cascode current amplifier with $z_o \approx (g_{m4}r_{o4})r_{o2}$. To derive the current gain and bandwidth, writing KCL at the gate and drain of M_1, the drain of M_2, and noting that

$$I_{in} = sC_{gs12}V_2 + g_{m3}(0 - V_1)$$

and

$$I_o = g_{m4}(0 - V_3)$$

we arrive at

$$\frac{I_o(s)}{I_{in}(s)} = \frac{g_{m2}}{g_{m1}} \frac{s\frac{C_{gs3}}{g_{m3}} + 1}{s^2\frac{C_{gs3}C_{gs12}}{g_{m1}g_{m3}} + s\frac{C_{gs12}}{g_{m1}} + 1} \tag{2.31}$$

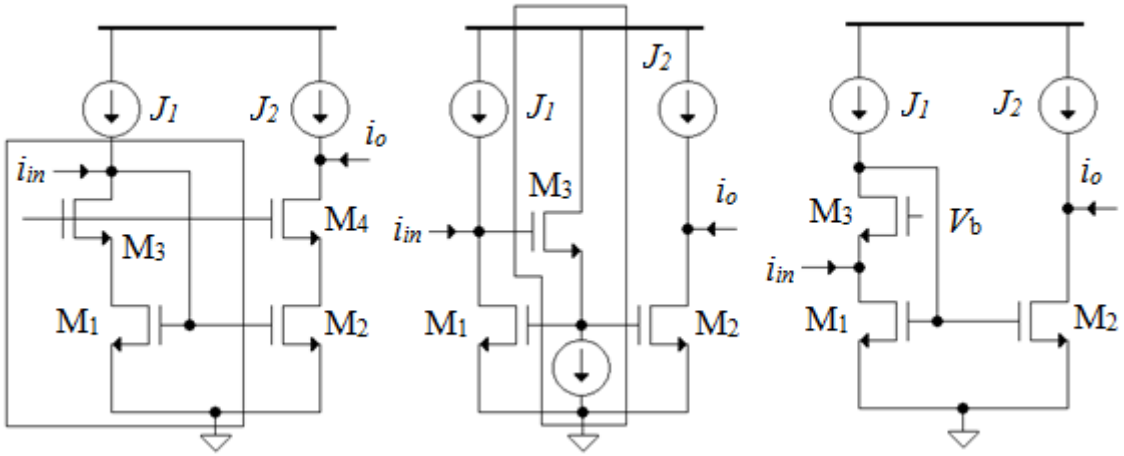
The two poles are at

$$p_{1,2} = \frac{g_{m3}}{2C_{gs3}}[-1 \pm \sqrt{1 - 4(\frac{g_{m1}}{g_{m3}})(\frac{C_{gs3}}{C_{gs12}})}] \tag{2.32}$$

If all transistors are of the same size, we arrive at $C_{gs12} \approx 2C_{gs3}$ and $g_{m1} \approx g_{m3}$. As a result, the poles become

$$p_{1,2} = \frac{g_{m1}}{C_{gs12}}(-1 \pm j)$$

It is evident that the low-voltage cascode current amplifier has the same bandwidth as that of the basic cascode current amplifier.



(a) (b) (c)

Figure 2.15 (a) Low-voltage cascode current amplifier, (b) Low input capacitance current amplifier, (c) Low input-impedance current amplifier.

2.3.3 INPUT-IMPEDANCE REDUCTION TECHNIQUES

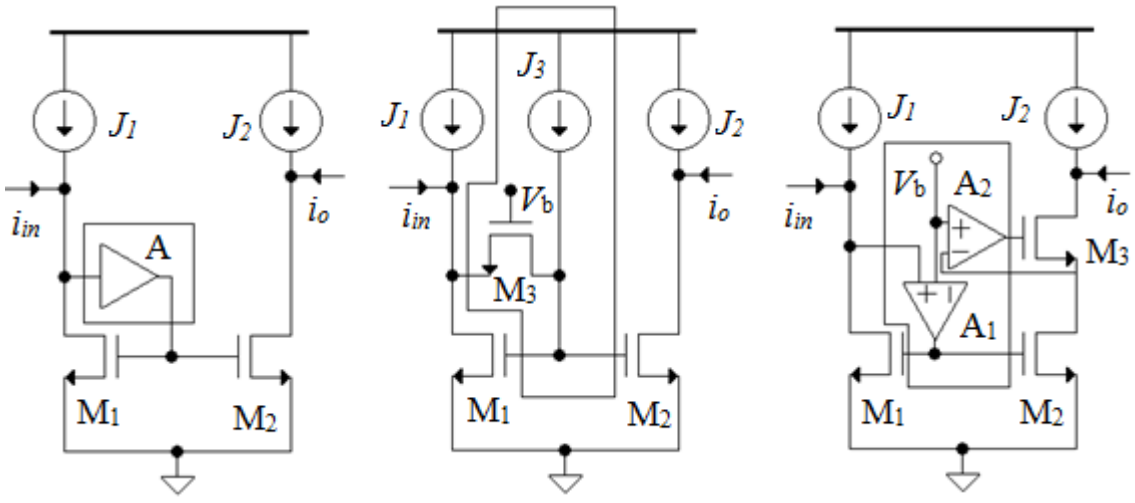
Equally important as large output-impedance for current-mode circuits is small input-impedance. This is because low input-impedance reduces the loading induced current error. Also, in applications such as data links over wire channels, a low input-impedance of the receivers is critical to increase the pole frequency at the input as the channels often have a large capacitance. This section investigates the techniques that reduce the input-impedance of current-mode circuits.

2.3.3.1 INPUT-CAPACITANCE REDUCTION

The capacitance seen from the input of the basic current amplifier is approximately $C_{in} \approx C_{gs1} + C_{gs2}$. To lower the input-capacitance, a source-follower can be employed at the input to isolate the gate capacitance $C_{gs1}+C_{gs2}$ from the input node, as shown in Figure 2.15(b). Because the Miller capacitances of M3 are approximately zero, $C_{in} \approx 0$ holds. The input-impedance at low frequencies is given by $z_{in} \approx \frac{1}{g_{m1}}$. The current gain at low frequencies is given by $\frac{i_o}{i_{in}} = \frac{g_{m2}}{g_{m1}}$, the same as that of the basic current amplifier [6].

2.3.3.2 ACTIVE FEEDBACK

The use of input active feedback to lower the input-impedance is shown in Figure 2.16. It is trivial to show that the input impedance of Figure 2.16(a) at low frequencies is given by $z_{in} = \frac{1}{Ag_{m1}}$ where A is the voltage gain of the auxiliary amplifier.



(a) (b) (c)

Figure 2.16 (a, b) Current amplifiers with input active feedback, (c) Current amplifiers with input active feedback and regulated cascode output.

The auxiliary amplifier can be implemented in various ways provided that these implementations offer large bandwidth. In Figure 2.16(b), a common-gate configuration

is employed to take the advantage of their immunity from Miller effect. Note that due to the close interaction with the feedback network, the input-impedance of the current amplifier of Figure 2.16(b) increases rapidly at high frequencies when the effect of C_{gs}, C_{gd} and parasitic junction capacitances are accounted for.

Both the active input feedback and regulated cascode can be employed simultaneously to lower the input-impedance and boost the output-impedance, as shown in Figure 2.16(c). It is readily to verify that the input-impedance and output-impedance of the active input regulated cascode current amplifier are given by $z_{in} \approx \frac{1}{A_1 g_{m1}}$ and $z_o = A(g_{m3} r_{o3}) r_{o2}$.

The current amplifier shown in Figure 2.15(c) is another approach to implement the active feedback at the input. M_3 introduces a negative feedback to stabilize the input voltage, lowering the input-impedance. The input-impedance is given by $z_{in} = \frac{1}{(g_{m3} r_{o3}) g_{m1}}$. Note that the minimum supply voltage requirement of the current amplifier is V_T + *Vsat* the same as that of the basic current amplifier.

2.3.3.3 BOOTSTRAPPING

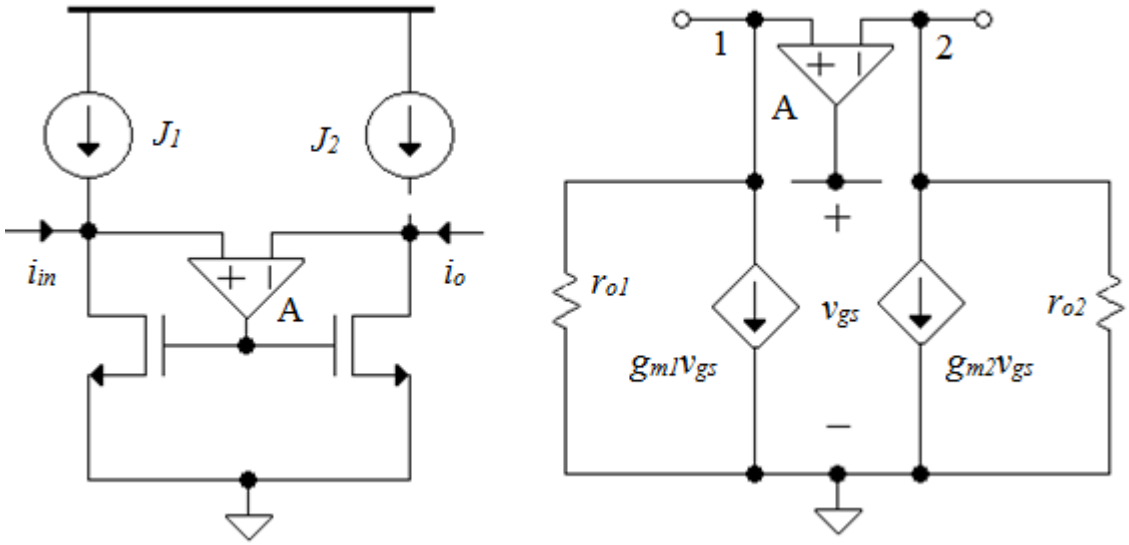
Basic cascode and regulated-cascode current amplifiers are not particularly attractive for low-voltage design because in order to have large output-impedance, the biasing current source J_2 in the output branch must also be cascode configured. To achieve a low input-impedance, a large output-impedance, and at the same time to keep the supply voltage low, bootstrapped current amplifiers are used. The basic configuration of bootstrapped current amplifiers is shown in Figure 2.17(a). The auxiliary amplifier is employed to enable the input and output voltages to track each other. In addition, it lowers the input-impedance and boosts the output-impedance. The small-signal equivalent circuit of the bootstrapped current amplifier at low frequencies is shown in Figure 2.17(b). The output-impedance is obtained

$$z_o = \frac{v_2}{i_T} = \frac{g_{o1} + A g_{m1}}{g_{o1} g_{o2} + A(g_{m1} g_{o2} - g_{m2} g_{o1})} \tag{2.33}$$

Assuming M_1 and M_2 are identical and $v_{DS1} = v_{DS2}$. This leads to $g_{m1}g_{o2} = g_{m2}g_{o1}$. Further because $g_{m1} >> g_{o1}$, (2.33) is simplified to

$$z_o \approx A(g_{m1}r_{o1})r_{o2} \tag{2.34}$$

Eq. (2.34) shows that the output-impedance of the bootstrapped current amplifier is comparable to that of the regulated cascode current amplifier. It should be noted that J_2 must also be bootstrap configured in order to have large output-impedance. The input-impedance can be obtained in a similar manner and is given by $z_{in} \approx \frac{1}{Ag_{m1}}$.



(a) (b)

Figure 2.17 (a) Bootstrapped current amplifiers, (b) Small-signal equivalent circuit.

2.3.4 MISMATCH COMPENSATION TECHNIQUES

The basic current amplifiers suffer from device mismatches, mainly W/L-mismatch, V_T-mismatch, v_{DS}-mismatch, and v_{GS}-mismatches. W/L-mismatch is due to the variation of fabrication processes. The dimension mismatch of transistors with multi-finger configuration differs from that of transistors with single-finger configuration, as shown in Figure 2.18. In a 2-finger configuration case, $\Delta W = 2(\Delta W_1 + \Delta W_2)$ whereas in the one-finger configuration $\Delta W = (\Delta W_1 + \Delta W_2)$. For amplifiers with a current gain of A, we have

$$\left(\frac{W}{L}\right)_2 = A\left[\frac{W}{L} + \Delta\left(\frac{W}{L}\right)\right]. \tag{2.35}$$

Because $i_{D2} = \dfrac{\left(\dfrac{W}{L}\right)_2}{\left(\dfrac{W}{L}\right)_1}\left(\dfrac{v_{gs2} - V_{T2}}{v_{gs1} - V_{T1}}\right)^2\left(\dfrac{1+\lambda v_{DS2}}{1+\lambda v_{DS1}}\right) i_{D1}$ (2.36)

We arrive at

$$i_{D2} = (1+\delta_{W/L}) i_{D1} \tag{2.37}$$

where $\delta_{W/L} = \dfrac{\Delta(W/L)}{W/L}$ .The second term in (2.37) is the output offset current due to W/L-mismatch. The v_{GS}-mismatch is mainly due to unbalanced interconnects connecting the gate and source of the input and output transistors. Let $v_{GS1} = v_{GS}, v_{GS2} = v_{GS} + \Delta v_{GS}$. Neglecting the second-order term in (2.36), we arrive at

$$i_{D2} = (1+\delta_{vGS}) i_{D1}, \tag{2.38}$$

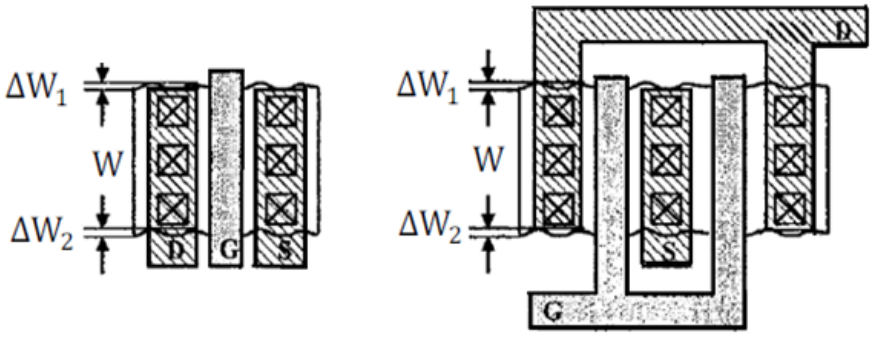
where $\delta v_{GS} \approx \dfrac{2\Delta v_{GS}}{v_{GS} - V_T}$. Note that since the effective gate voltage $v_{GS} - V_T$ is usually small, δ_{vGS} contributes significantly to the overall output offset current. V_T-mismatch is process induced and can be analyzed in a similar way as v_{GS}-mismatch.

$$i_{D2} = (1+\delta_{V_T}) i_{D1}, \tag{2.39}$$

where $\delta V_T \approx \dfrac{2\Delta V_T}{v_{GS} - V_T}$. For the same reason as that for v_{GS}-mismatch, V_T-mismatch is critical. In a similar manner as that of v_{GS}-mismatch, one can analyze the effect of v_{DS}-mismatch

$$i_{D2} = (1+\delta_{vDS}) i_{D1}, \tag{2.40}$$

where $\delta V_{vDS} \approx \dfrac{\lambda \Delta v_{DS}}{1+\lambda v_{DS}}$.



(a) (b)

Figure 2.18 Dimension mismatches of multi-finger transistors, (a) One finger layout (b) two finger layout [6].

For practical circuits, since $v_{gs} << V_{GS}, v_{ds} << V_{DS}$, we have $\Delta v_{GS} << \Delta V_{GS}$ and $\Delta v_{DS} << \Delta V_{DS}$, subsequently $\Delta v_{GS} \approx \Delta V_{GS}$ and $\Delta v_{DS} \approx \Delta V_{DS}$. This leads to $\delta_{vGS} \approx \frac{2\Delta V_{GS}}{V_{GS} - V_T}$, $\delta V_T \approx \frac{2\Delta V_T}{V_{GS} - V_T}$, $\delta V_{vDS} \approx \frac{\lambda \Delta V_{DS}}{1 + \lambda V_{DS}}$. Because $i_{D1} = i_{in} + J$ the output current of the current amplifier with mismatches considered is given by

$$\begin{aligned} i_o &= A(1+\delta)(i_{in} + J) \\ &= A(i_{in} + J) + \delta A(i_{in} + J), \end{aligned} \tag{2.41}$$

where the mismatch coefficient δ in the worst case is obtained from

$$\delta = \left|\delta_{W/L}\right| + \left|\delta_{V_{GS}}\right| + \left|\delta_{V_T}\right| + \left|\delta_{V_{DS}}\right|. \tag{2.42}$$

The second term on the right hand side of (2.41) is the mismatch induced output offset current and is denoted by i_{os}. It consists of two components: the signal dependent component $i_{os1} = \delta A i_{in}$ and the bias dependent component $i_{os2} = \delta A J$. i_{os2} can be removed by employing a two phase clock that samples and holds the offset current in one clock phase and substrates the held offset current from the output current of the current amplifiers in the following clock phase.

Because i_{os2} is time-invariant, it can also be compensated effectively using the balancing network shown in Figure 2.19. To simplify analysis, we assume that all NMOS

current mirrors have the same mismatch coefficient δ_n and all PMOS current mirrors have the same mismatch coefficient δ_p. Making use of (2.41)

$$i_{D2} = A_1(i_{in} + J) + \delta_n A_1(i_{in} + J), \tag{2.43}$$

and

$$\begin{aligned} i_{D4} &= A_2[A_1(i_{in} + J)\delta_n A_1(i_{in} + J)] + \delta_p A_2[A_1(i_{in} + J) + \delta_n A_1(i_{in} + J)] \\ &\approx A_1A_2i_{in} + A_1A_2J + A_1A_2\delta_n i_{in} + A_1A_2\delta_n J + A_1A_2\delta_p i_{in} + A_1A_2\delta_p J, \end{aligned} \tag{2.44}$$

where 2nd-order terms were neglected. In a similar manner it can be shown that

$$i_{D5} \approx A_1A_2J + A_1A_2\delta_p J + A_1A_2\delta_n J. \tag{2.45}$$

The subtraction of (2.45) from (2.44) yields

$$i_o = A_1A_2i_{in} + A_1A_2(\delta_n + \delta_p)i_{in}. \tag{2.46}$$

It is seen from (2.46) that the output offset current is reduced from $A_1A_2(\delta_n + \delta_p)J + A_1A_2(\delta_n + \delta_p)i_{in}$ without the balancing network to $A_1A_2(\delta_n + \delta_p)i_{in}$ with it. Figure 2.20 and 2.21 compare the simulation results of the output current with and without the balancing network. It should be noted that the balancing network approach consumes additional power and silicon area.

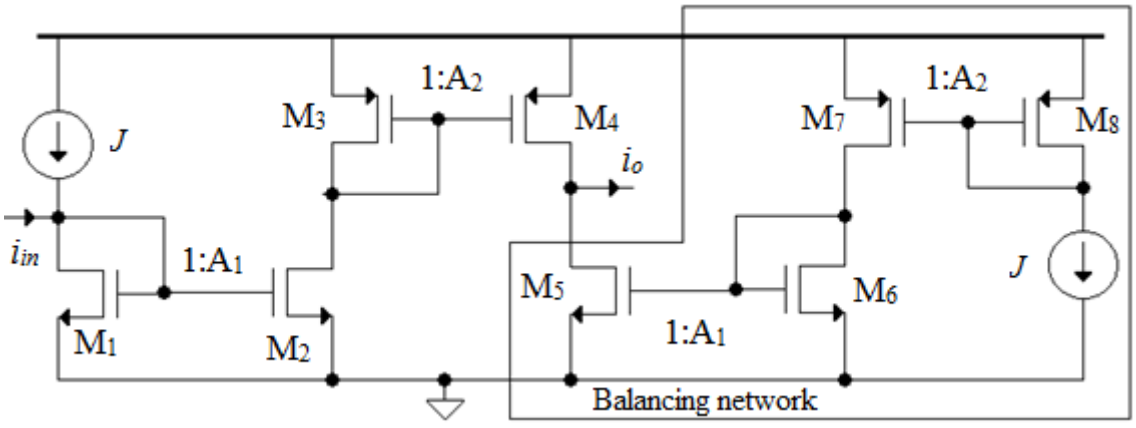


Figure 2.19 Balancing network for mismatch compensation of current amplifiers.

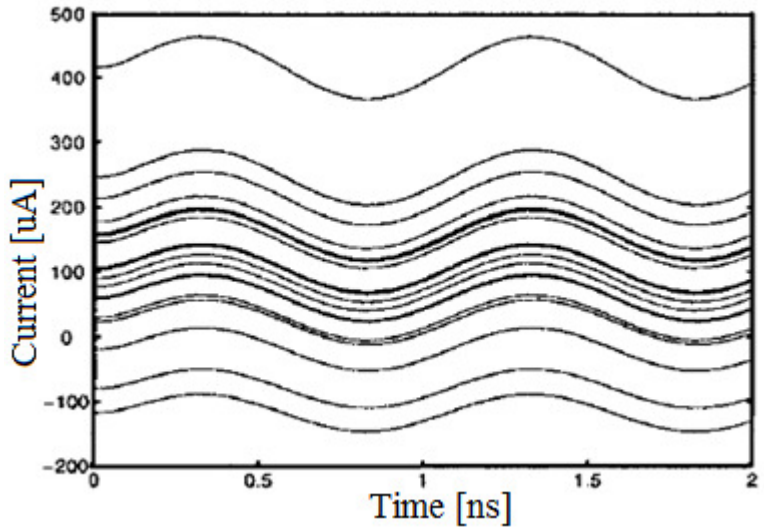


Figure 2.20 Simulated output current without the balancing network [6].

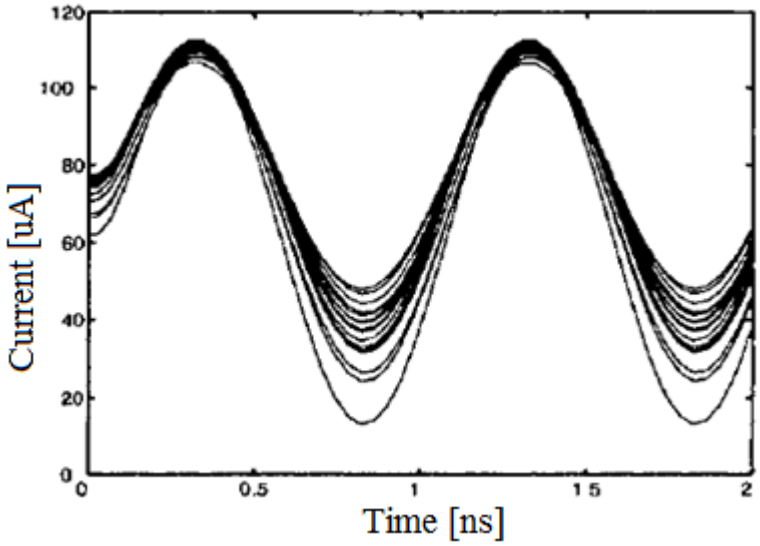


Figure 2.21 Simulated output current with the balancing network [6].

2.3.5 POWER REDUCTION TECHNIQUES

One of the drawbacks of current mirror amplifiers is their high static power consumption, arising mainly from the large biasing current of the output branch. Consider the two-stage current amplifier shown in Figure 2.22 with J_c = 0. The output current is given by $i_o = A_1 A_2 i_{in}$ and the biasing current of the output branch is given by $j_2 = A_1 A_2 J_1$. Since the purpose of the second stage is to amplify i_{d2}, not I_{D2}, this suggests that I_{D3} should be kept small. To achieve this, the dc current source $J_c = A_c J_1$, as shown in Figure 2.22, is added.

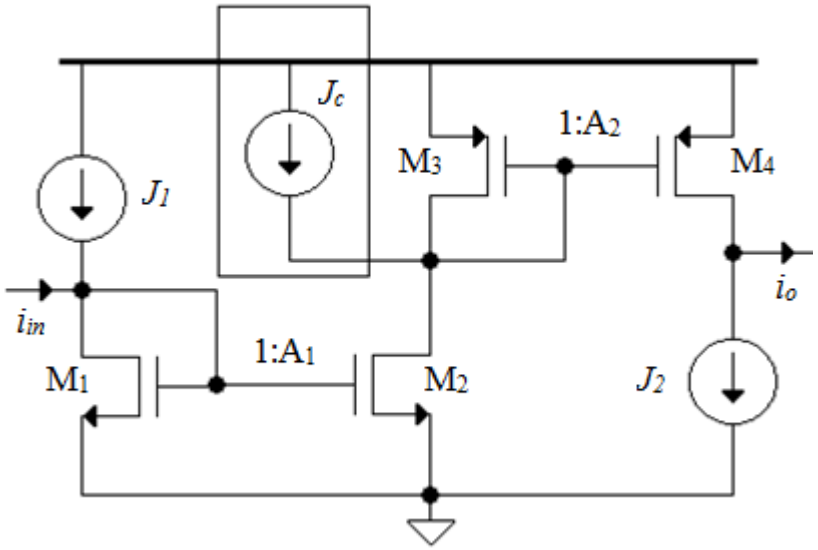


Figure 2.22 Current-branching.

The channel current of M_2 is given by $i_{D2} = A_1(i_{in} + J_1)$ and that of M_3 is given by $i_{D3} = A_1 i_{in} + (A_1 - A_C)J_1$. If we impose A_1 - A_c = 1 and $J_2 = A_2 J_1$, the output current is given by $i_o = A_1 A_2 i_{in}$. In addition to the power consumption reduction, the chip area is also reduced due to smaller M_3 and M_4. This is echoed with an increase in the bandwidth, as is evident in Figure 2.23.

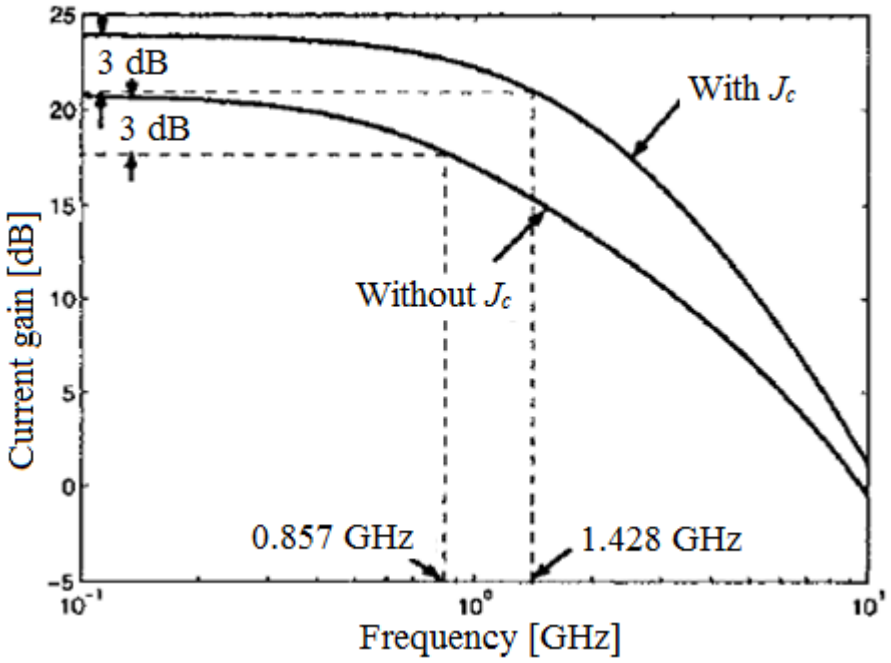


Figure 2.23 Simulated bandwidth of amplifier with current-branching [6].

2.3.6 BANDWIDTH ENHANCEMENT TECHNIQUES

Resistor series peaking, inductor series peaking, and current feedback are three effective means to improve the bandwidth of current-mode circuits. This section examines these techniques.

2.3.6.1 RESISTOR SERIES PEAKING

A resistor can be added between the gates of the input and output transistors of the basic current amplifier, as shown in Figure 2.24, to introduce a zero to the system. The current transfer function is given by

$$H(s)=\left(\frac{g_{m2}}{g_{m1}}\right)\frac{sRC_{gs1}+1}{s^2\dfrac{RC_{gs1}C_{gs2}}{g_{m1}}+s\dfrac{C_{gs2}+C_{gs2}}{g_{m1}}+1}. \tag{2.47}$$

The two poles are at

$$p_{1,2}=\frac{C_{gs1}+C_{GS2}}{2RC_{gs1}C_{gs2}}\left[-1\pm\sqrt{(1-\frac{4RC_{gs1}C_{gs2}g_{m1}}{(C_{gs1}+C_{gs2})^2})}\right], \tag{2.48}$$

and the zero is at $z=-\dfrac{1}{RC_{gs1}}$. Depending upon the value of the peaking resistor R, the locations of both the zero and poles of the system differ and the amplifier exhibits distinct characteristics.

(1) **Distinct real poles** – When $R=\dfrac{1}{g_{m1}}$, the amplifier has two distinct negative real poles located at $p_1=-\dfrac{g_{m1}}{C_{gs2}}$ and $p_2=-\dfrac{g_{m1}}{C_{gs2}}$. The pole p_2 is identical to the zero given by $z=-\dfrac{g_{m1}}{C_{gs1}}$ and cancels out the zero. As a result, the transfer function is simplified to

$$H(s)=\left(\frac{g_{m2}}{g_{m1}}\right)\frac{1}{s\dfrac{C_{gs2}}{g_{m1}}+1}. \tag{2.49}$$

As compared with the bandwidth of the basic current amplifier, the resistor series peaking with two distinct real poles boosts the bandwidth to $\omega = \frac{g_{m1}}{C_{gs2}}$. Note that if $C_{gs2} >> C_{gs1}$, the bandwidth improvement from resistive series peaking with two distinct real poles is rather small.

(2) **Identical real poles** - When $R = \frac{1}{4g_{m1}} \frac{(C_{gs1} + C_{gs2})^2}{C_{gs1}C_{gs2}} \approx \frac{1}{4g_{m1}} \frac{C_{gs2}}{C_{gs1}}$, the circuit has two identical negative real poles $p_{1,2} = -\frac{2g_{m1}}{C_{gs1} + C_{gs2}}$. The bandwidth becomes $\omega_b = 2\sqrt{\sqrt{2} - 1} \frac{g_{m1}}{C_{gs2}}$.

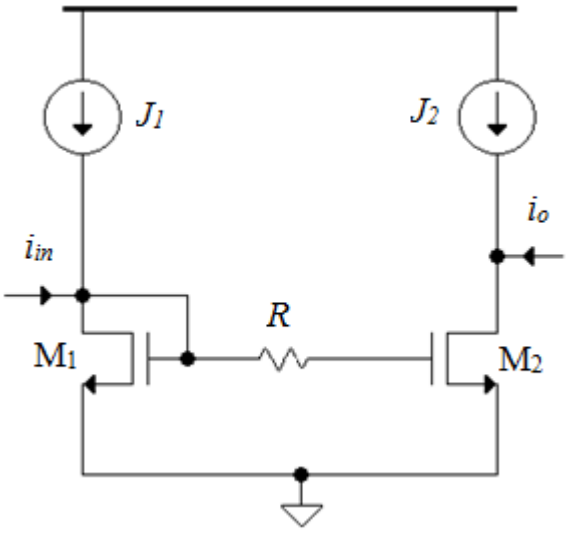


Figure 2.24 Basic current amplifiers with resistor series peaking.

(3) **Complex conjugate poles** - A further increase of R will lead to a pair of complex conjugate poles. An overshoot in the frequency-domain response and ringing in the time-domain response exist. A critical point is when $R = \frac{1}{2g_{m1}} \frac{C_{gs2}}{C_{gs1}}$ amplifier has two complex conjugate poles that are separated by $\frac{\pi}{2}$ and has a maximally flat response, called Butterworth response, with the bandwidth given by $\omega_b = \sqrt{2} \frac{g_{m1}}{C_{gs2}}$. In this case, the time-domain response of the amplifier to a unit step input has an overshoot of 4.32%

approximately. Figure 2.25 shows the dependence of the bandwidth of the current amplifier with the resistor series peaking on the resistance of the peaking resistor.

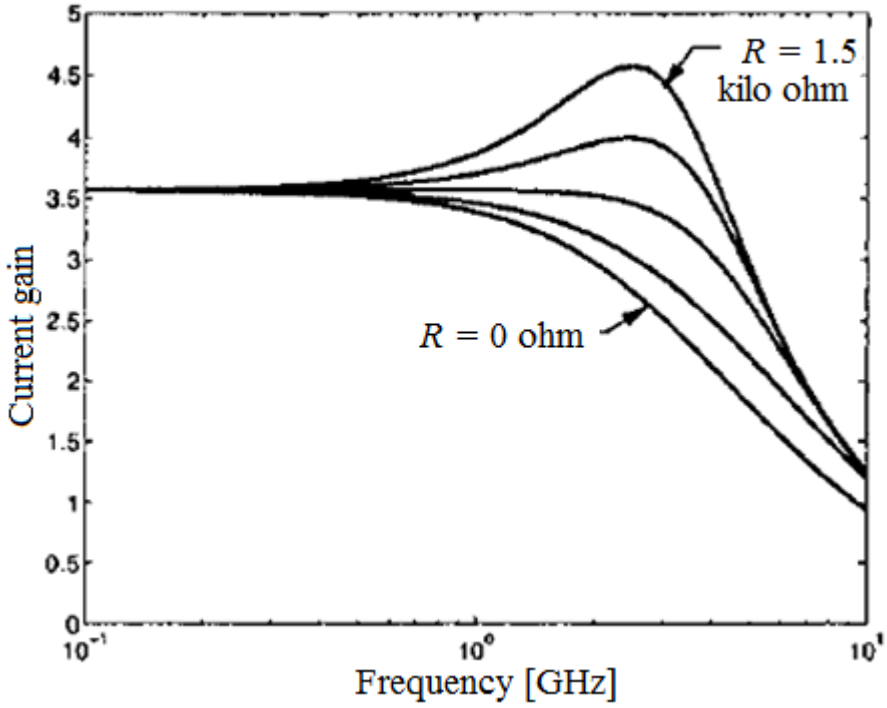


Figure 2.25 Simulated frequency response of current amplifier with resistor series peaking [6].

2.3.6.2 INDUCTOR SERIES PEAKING

The thermal noise of the series peaking resistor increases the total noise of the amplifier. For low-noise applications, such as the front end of GB/s transceivers and optical pre-amplifiers, noiseless elements, such as inductors, are preferred over noisy resistors for bandwidth enhancement. It has been seen that inductor shunt peaking can increase the bandwidth of voltage-mode circuits by as much as 70% [6]. Inductor shunt peaking technique, however, is not particularly applicable to current-mode circuits due to the existence of biasing current sources between the devices forming the dominant poles and the supply voltage. The fact that the dominant pole of the basic current amplifier is located at the gates of M_1 and M_2 suggests that an inductor can be placed between the gates of M_1 and M_2, as shown in Figure 2.26, to boost bandwidth. By assuming $C_{gs2} >> C_{gs1}$ we obtain the current transfer function

$$\frac{I_o(s)}{I_{in}(s)} = (\frac{g_{m2}}{g_{m1}}) \frac{1}{s^2 LC_{gs2} + s\frac{C_{gs2}}{C_{gm1}} + 1}. \tag{2.50}$$

The two poles are located at

$$p_{1,2} = \frac{1}{2Lg_{m1}}(-1 \pm \sqrt{1 - \frac{4Lg_{m1}^2}{C_{gs2}}}) \ . \tag{2.51}$$

Under the condition $L = -\frac{C_{gs2}}{4g_{m1}^2}$, the amplifier has two identical real poles $p_{1,2} = -\frac{2g_{m1}}{C_{gs2}}$. Its time response is critically damped with no ringing. The bandwidth in this case is given by $\omega_b = 2\sqrt{\sqrt{2}-1}\left(\frac{g_{m1}}{C_{gs2}}\right)$. When L is increased to $L = \frac{C_{gs2}}{2g_{m1}^2}$, the amplifier has two complex conjugate poles that are separated by $\frac{\pi}{2}$. In this case, the response of the amplifier has a maximally flat (Butterworth) pass band with the bandwidth given by $\omega_b = \sqrt{2}(\frac{g_{m1}}{C_{gs2}})$. Figure 2.27 shows the frequency response of the current amplifier with inductor series peaking. The attenuation rate of the response in the stop band, which is approximately -40 dB/decade, is higher as compared with that of the amplifier with resistive series peaking. This is because the former increases the bandwidth by adding a pole whereas the latter enhances the bandwidth by introducing a zero. The peaking inductor does not affect the dc characteristics of the amplifier, a similar property as that of the resistor series peaking.

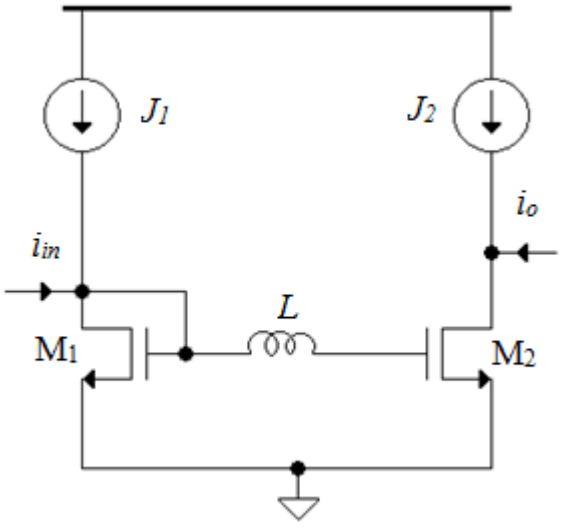


Figure 2.26 Current amplifier with Inductor series peaking.

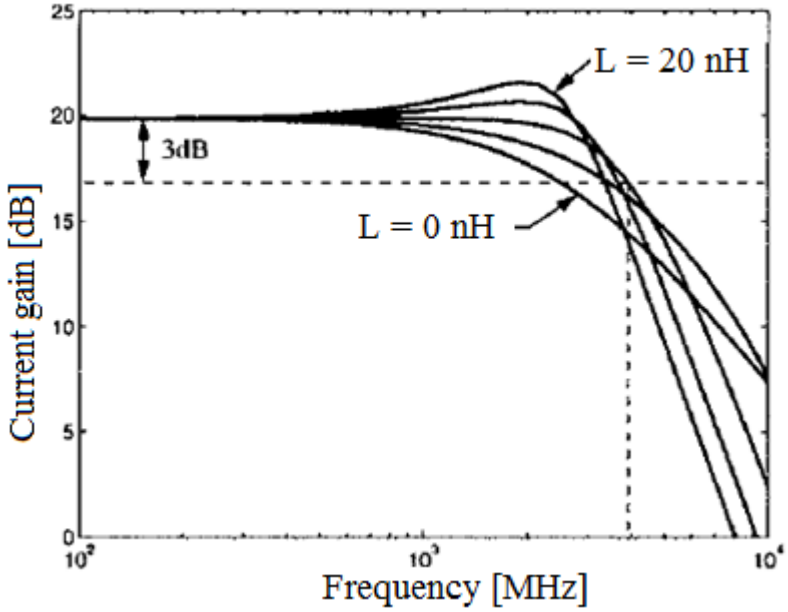


Figure 2.27 Simulated frequency response of current amplifier with inductor series peaking [6].

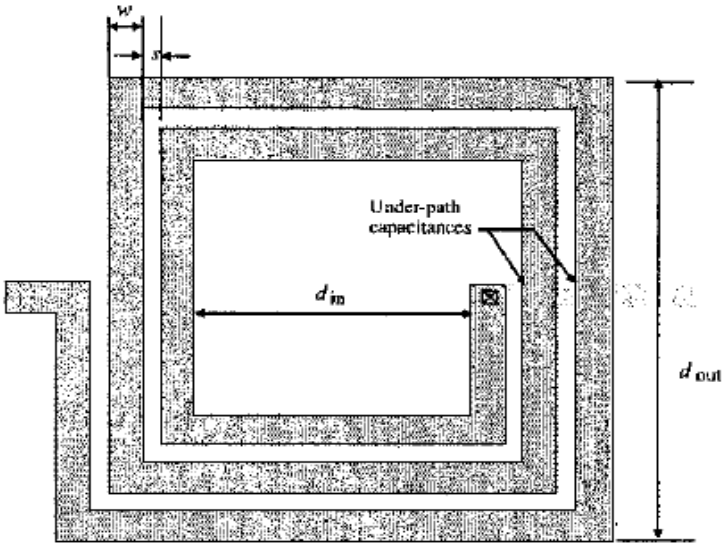


Figure 2.28 Typical layout of square shaped spiral inductors [6].

On-chip inductors are usually implemented in either planar or stacked spiral configurations, as shown in Figure 2.28. Spiral inductors have the characteristics of a low quality factor, a low inductance, and extremely area consuming. The ohmic loss of spiral inductors, mainly due to the skin-effect induced loss at high frequencies, is usually depicted using a series resistor R_s. Its capacitive loss, arising from the large capacitance between the spirals and the substrate, is represented by two shunt capacitors C_{ox} *at* the

terminals of the inductor. The capacitive coupling between the upper and lower spirals at the under paths and fringe capacitance between neighboring spirals is characterized by C_s, as shown in the simple lumped model of on-chip spiral inductors in Figure 2.29.

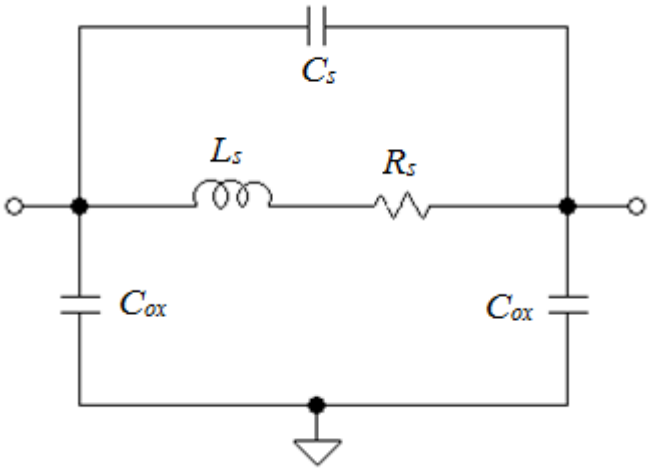


Figure 2.29 Simple lumped model of on chip spiral inductors.

The series resistance of the inductor behaves as a series peaking resistor and improves the bandwidth, as shown in Figure 2.30. The spiral substrate shunt capacitance, however, is directly added to the total capacitance of the gates of $M_{1\sim2}$ of the current amplifier, lowering the bandwidth, as evident in Figure 2.31.

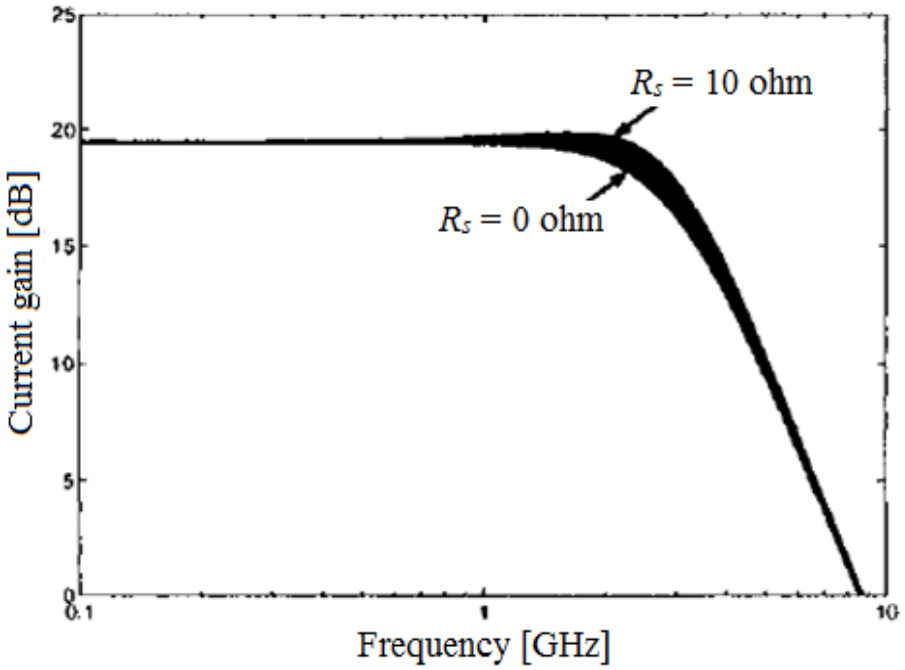


Figure 2.30 Simulated effect of the series resistance of series peaking inductors on the frequency response of the current amplifier [6].

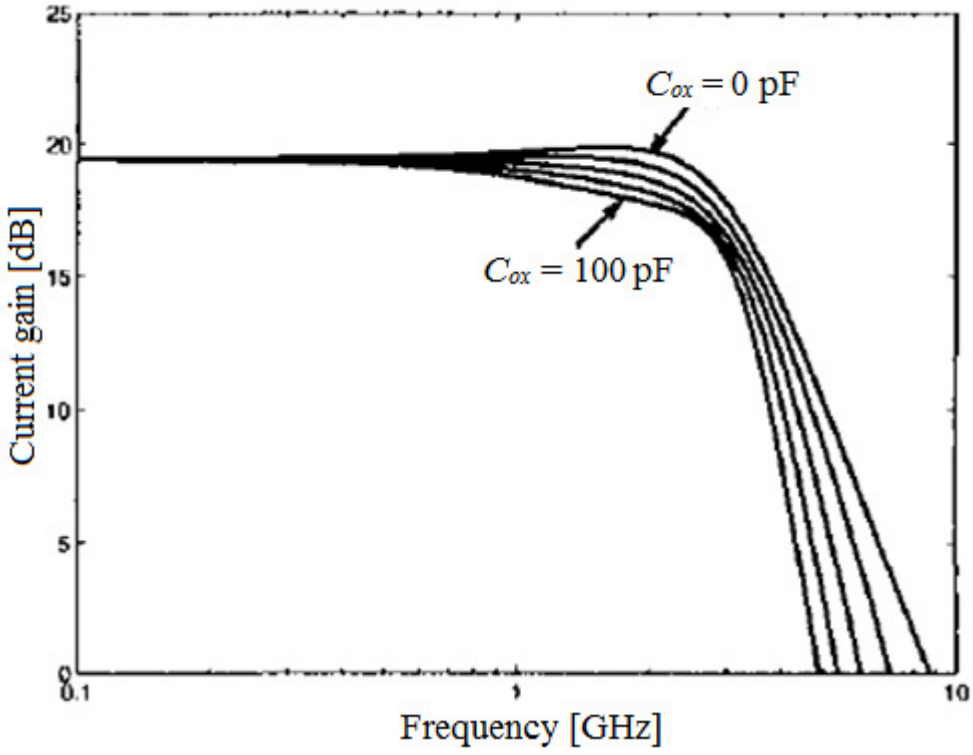


Figure 2.31 Simulated effect of the parasitic capacitance of series peaking inductors on the frequency response of the current amplifier [6].

2.3.6.3 CURRENT FEEDBACK

It is well known that negative current-current feedback increases the output impedance and lowers the input impedance. To sense the output current without affecting both the dc biasing condition and the supply voltage, the current feedback mechanism shown in Figure 2.32 can be used. The transfer function of the amplifier is given by

$$H(s) \approx \left(\frac{g_{m2}}{g_{m1}}\right) \frac{\dfrac{1}{LC_{gs2}}}{s^2 + s\dfrac{1}{g_{m1}L} + \dfrac{g_{m1} + g_{mf}}{g_{m1}LC_{gs2}}}. \tag{2.52}$$

with two poles at

$$p_{1,2} = \frac{1}{2g_{m1}L}\left[-1 \pm \sqrt{1 - \frac{4(g_{m1} + g_{mf})g_{m1}L}{C_{gs2}}}\right]. \tag{2.53}$$

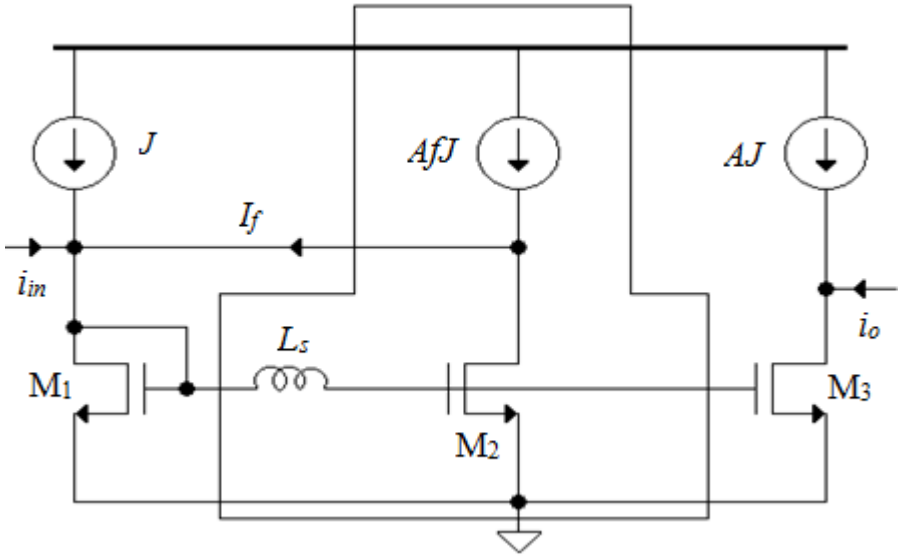


Figure 2.32 Current amplifier with both current-current feedback and inductor series peaking.

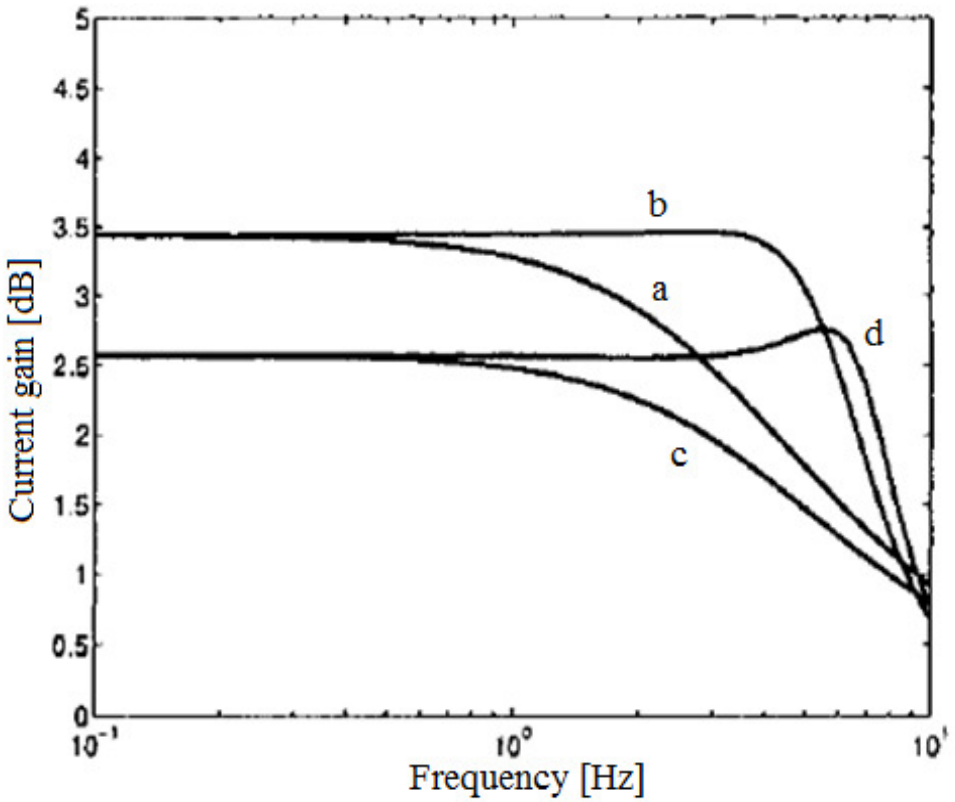


Figure 2.33 Simulated frequency response of current amplifiers with both current-current feedback and inductor series peaking, (a) Basic current amplifier, (b) Inductor series peaking only, (c) Current-current feedback, (d) Inductor series peaking and current-current feedback [6].

Complex conjugate poles that are $\frac{\pi}{2}$ apart occurs when $L=\frac{C_{gs2}}{2g_{m1}^2(1+Af)}$ where $A=\frac{(W/L)_2}{(W/L)_1}$ and $f=\frac{(W/L)_f}{(W/L)_2}$. In this case, the amplifier has a maximally flat response with the bandwidth $\omega_b=\sqrt{2}(1+Af)\frac{g_{m1}}{C_{gs2}}$. The value of the series peaking inductor that gives a maximally flat response is reduced from $L=\frac{C_{gs2}}{2g_{m1}^2}$ without the current-current feed back to $L=\frac{C_{gs2}}{2g_{m1}^2}\frac{1}{(1+\lambda f)}$ with the current-current feedback. A smaller inductor, subsequently, a smaller chip area and less parasitic effects, is needed when current-current feedback is employed. Figure 2.33 shows the frequency response of the current amplifier with both inductor series peaking and current-current feedback.

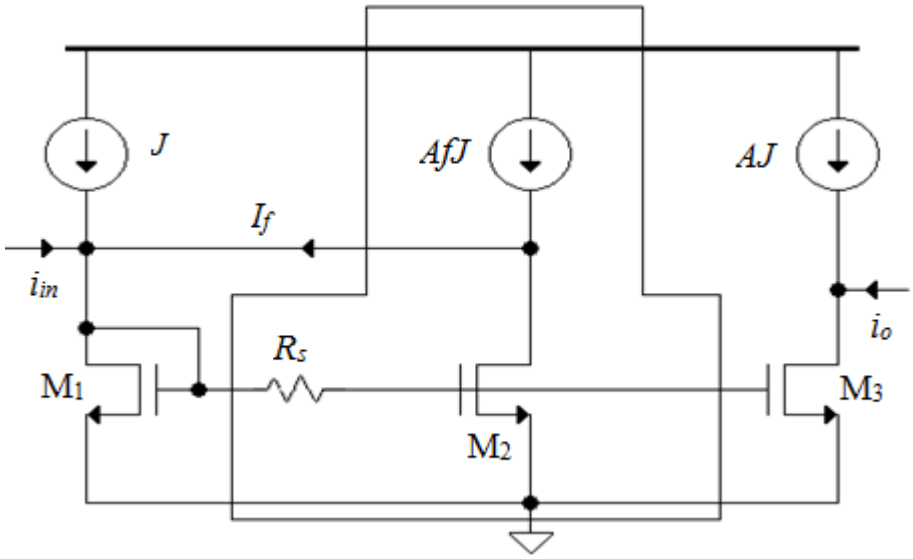


Figure 2.34 Current amplifier with both current-current feedback and resistor series peaking.

In a similar manner, it can be show that the amplifier with both resistor series peaking and current-current feedback, as shown in Figure 2.34, has the current transfer function

$$H(s)=\left(\frac{g_{m2}}{g_{m1}+g_{mf}}\right)\frac{sRC_{gs1}+1}{s^2\frac{RC_{gs1}(C_{gs2}+C_{gs,f})}{g_{m1}+g_{mf}}+s\frac{C_{gs1}+C_{gs2}+C_{gs,f}+RC_{gs1}g_{mf}}{g_{m1}+g_{mf}}+1} \quad . (2.54)$$

Assuming $Rg_{mf} << 1$ and $C_{gs,f} << C_{gs1}$, we have two poles

$$p_{1,2} \approx \frac{C_{gs1}+C_{gs2}}{2RC_{gs1}C_{gs2}}\left[-1 \pm \sqrt{1-\frac{4RC_{gs1}C_{gs2}g_{m1}(1+Af)}{(C_{gs1}+C_{gs2})^2}}\right]. \quad (2.55)$$

When $R=\frac{1}{2g_{m1}}\frac{C_{gs2}}{C_{gs1}}\frac{1}{1+Af}$, the amplifier has a maximum plat response with its bandwidth $\omega_b\sqrt{2}(1+Af)\frac{g_{m1}}{C_{gs2}}$. Also, the resistance value is reduced from $R=\frac{1}{2g_{m1}}\frac{C_{gs2}}{C_{gs1}}$ without the current-current feedback to $R=\frac{1}{2g_{m1}}\frac{C_{gs2}}{C_{gs1}}\frac{1}{1+Af}$ with the current-current feedback. Figure 2.35 shows the current gain of the amplifiers with the resistor series peaking and current-current feedback.

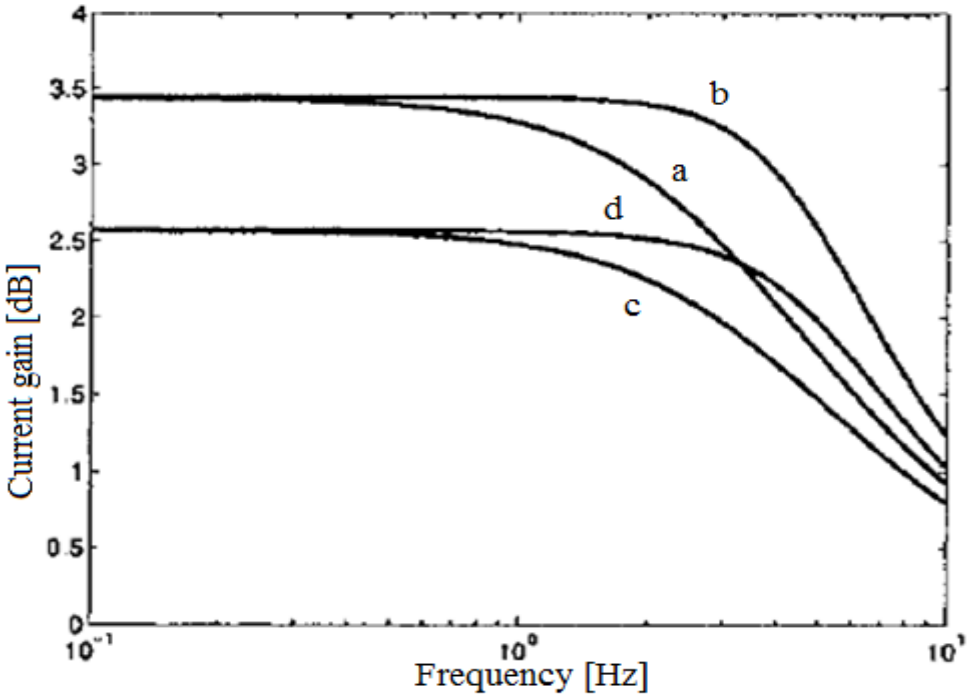


Figure 2.35 Simulated frequency response of current amplifiers with both current-current feedback and resistor series peaking, (a) Basic current amplifier, (b) Resistor series peaking, (c) Current-current feedback, (d) Resistor series peaking and current-current feedback [6].

2.3.7 DYNAMIC RANGE IMPROVEMENT TECHNIQUES

The application of class-A current amplifiers is limited by the small current swing because a large current swing would require the quiescent point to be far away from the pinch-off, resulting in a large drain-source voltage.

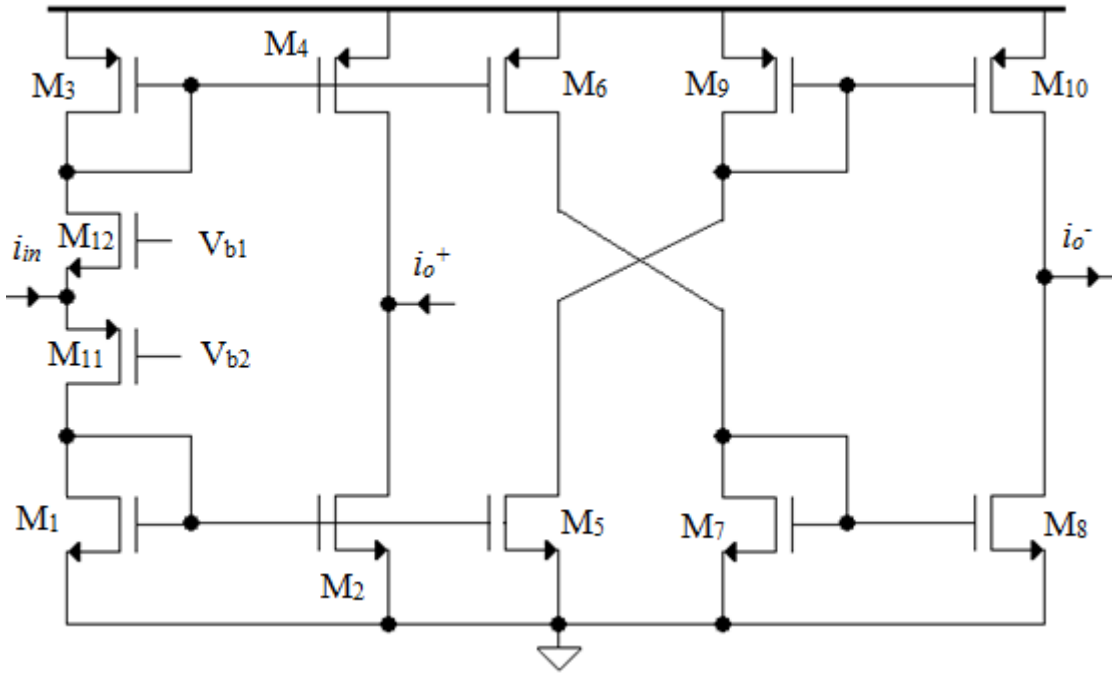


Figure 2.36 Basic class AB current amplifiers.

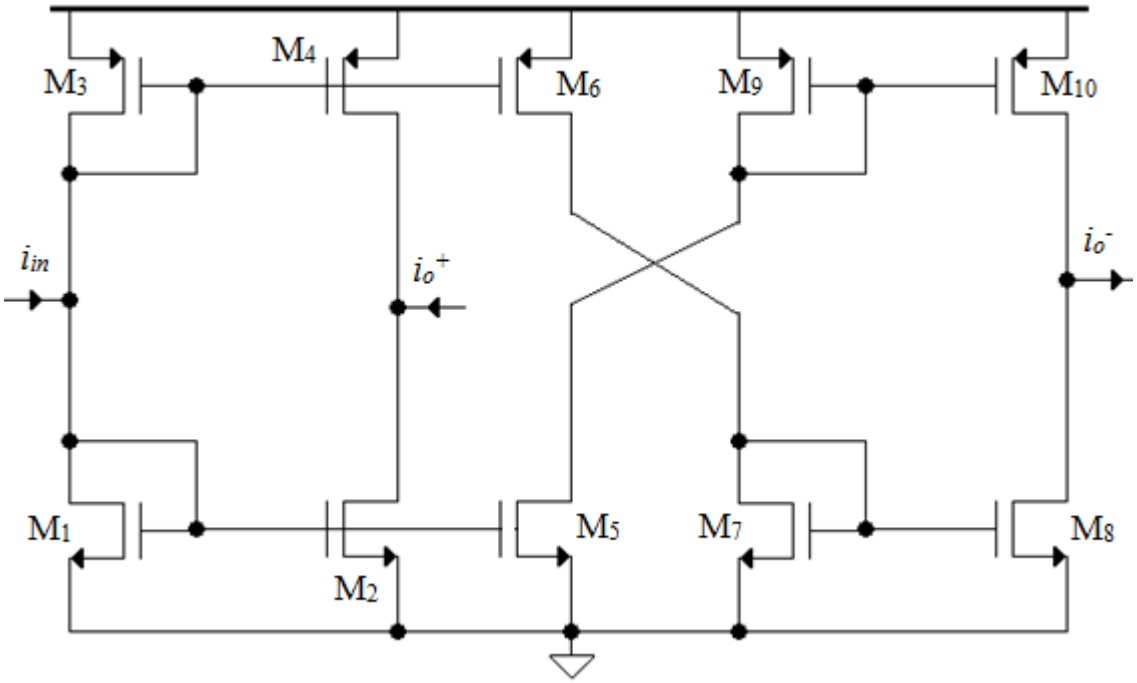


Figure 2.37 Low-voltage class AB current amplifiers.

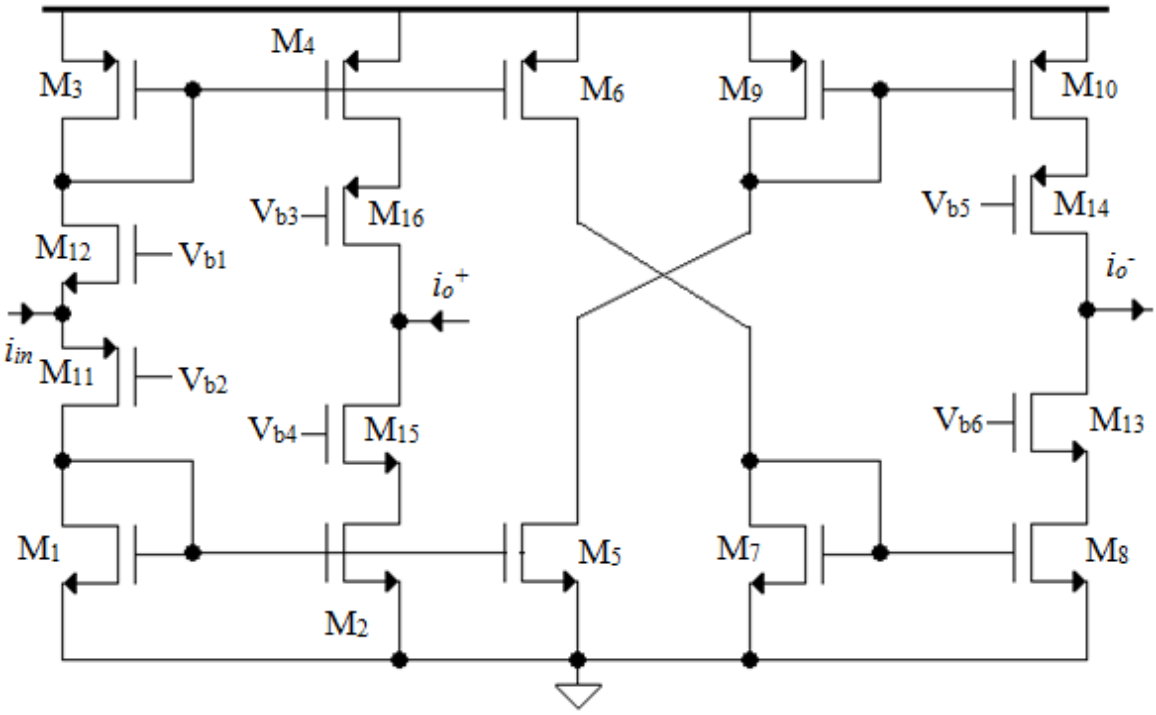


Figure 2.38 Cascode class AB current amplifiers.

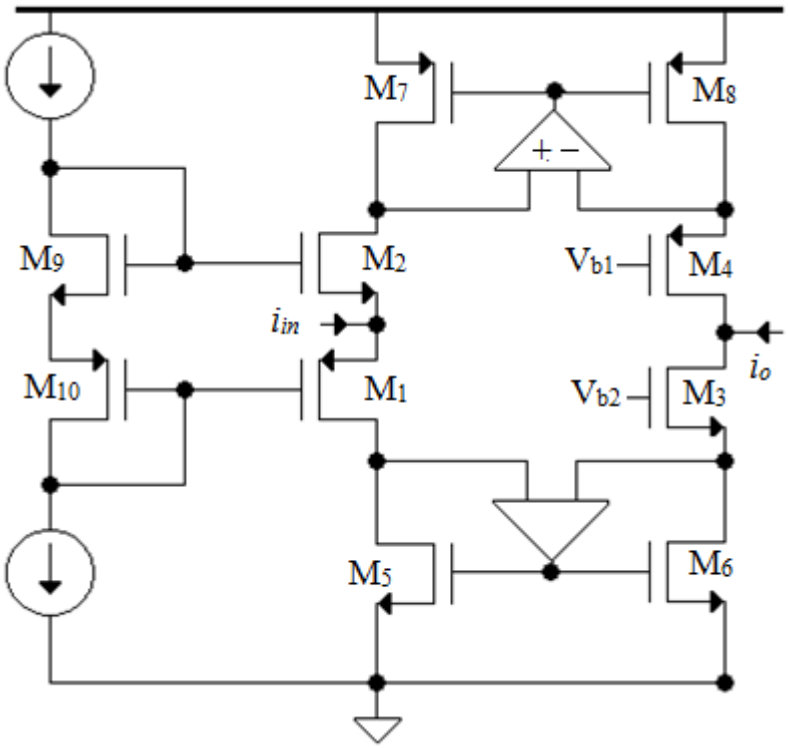


Figure 2.39 Bootstrapped Class AB current amplifiers.

To accommodate high-current applications, class AB configurations that employ a pair of NMOS and PMOS current mirrors activated separately are effective, as shown in Figure 2.36, 2.37, 2.38 and 2.39. Transistors $M_{11\sim12}$ provide a low input impedance. When a

large positive input current is applied at the input (the current flows into the channel), the voltage of the input node arises sufficiently high such that the PMOS current mirror is disabled. The input current is sensed by the NMOS current mirror. Similarly, when a large negative current is applied to the input (the current flows away from the channel), the low voltage at the input node forces M_{11} enter the cut-off mode and the current flowing out of the input node is sourced by the PMOS current mirror. It should, however, be noted that when the amplitude of the input current is small, both the NMOS and PMOS current mirrors are activated, giving rise to static power consumption. The dc operating point of the class AB current amplifier is set to such that $V_{in} = V_{DD}/2$ and the minimum supply voltage is given by $V_{DD,\min} = 2V_T + 2V_{sat}$. The low-voltage class AB current amplifier shown in Figure 2.37 lowers the minimum supply voltage to $2V_T$. The main drawback of this current amplifier is that the quiescent currents are strongly influenced by both the threshold and supply voltages. To minimize the effect of a finite output impedance of the preceding class AB current amplifier, cascode configuration can be employed at both the output stages, as shown in Figure 2.38. The output impedance at low frequencies is given by $r_o = (g_{m13}r_{o13})r_{o8} \| (g_{m14}r_{o14})r_{o10}$. The bootstrapped cascode class AB current amplifier is shown in Figure 2.39. The bootstrapped configuration boosts the output impedance to $r_o = A(g_{m3}r_{o3})r_{o6} \| A(g_{m1}r_{o4})r_{o8}$. The added auxiliary differential amplifiers also minimize the output error current of current mirrors $M_{5\sim6}$ and $M_{7\sim8}$ due to v_{DS}-mismatch.

CHAPTER 3

DESIGN AND ANALYSIS OF CURRENT-MODE OPERATIONAL AMPLIFIER

In this work, a CMOS current operational amplifier (COA) with fully differential input and differential output has been analyzed and implemented from a differential current mirror input transimpedance stage followed by a differential output transconductance gain stage. This configuration is the current-mode counterpart of the traditional voltage operational amplifier (VOA). The simulation results of the COA are based upon the UMC 0.18 μm CMOS process with 1.5 V supply voltage. The design exhibits an open-loop differential gain of 65.38 dB with the gain-bandwidth product 353.60 MHz and a settling time of 5.90 ns. The design and optimization guidelines of the COA have been discussed and analyzed so that they can also be applied to the design of high performance COA.

3.1 INTRODUCTION

In order to achieve high performance analog circuits in CMOS technology, the past few years have seen a great shift in analog circuit design towards representing signals with current instead of voltage. Current-mode signal processing is receiving considerable attention due to its potential of two conceptual advantages over the classical voltage-mode approach: higher frequency capabilities and higher dynamic range. Such current-mode circuits are no longer directly restricted by the supply voltage but associated with the impedance level chosen by the designer [8].

The design and operation principle of the current operational amplifier can be derived from that of the voltage operational amplifier by applying the theory of adjoint networks to obtain the same transfer function. Following this approach, the interreciprocal network can then be used to transform almost all voltage-mode continuous time active circuits to their current-mode equivalent networks, along with the fully differential circuit structures used in high frequency analog signal processing, like switched filters which have a higher rejection capability on block-feed through noises and power supply variations.

In 1968, Sedra and Smith introduced a current conveyor which they implemented using a voltage operational amplifier, complementary MOSFETs, and current mirrors. Applying the theory of adjoint networks, the current operational amplifier (COA) replaces the VOA with a floating current controlled current source when converting from a voltage-mode circuit configuration to a current-mode configuration [8].

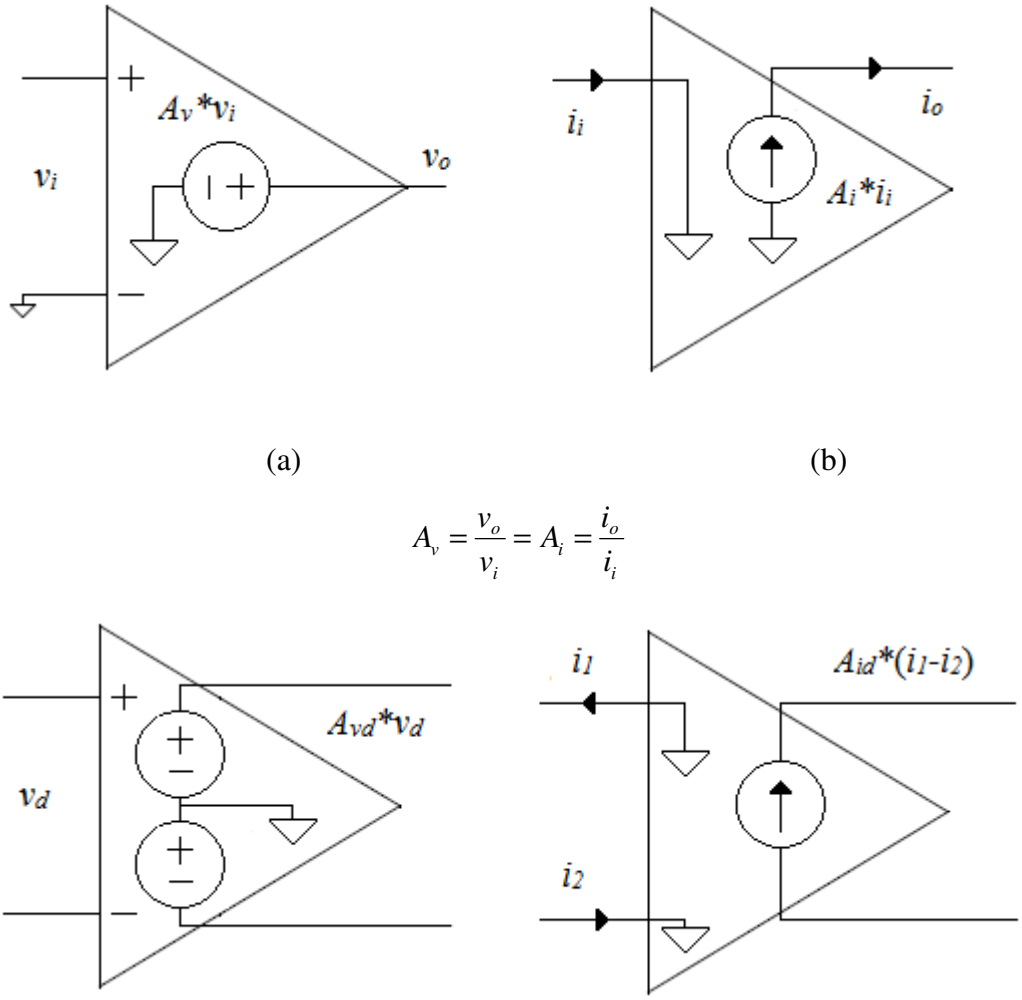


Figure 3.1 Interreciprocal network of VOA to COA.

The equivalent circuit of a voltage operational amplifier is shown in Figure 3.1(*a*). According to the adjoint network theory, the voltage controlled voltage source is replaced by a current controlled current source and the input/output terminals are interchanged.

The resulting equivalent block is a current operational amplifier and is shown in Figure 3.1(b). A fully differential VOA, shown in Figure 3.1(c), is transformed to the fully differential COA as shown in Figure 3.1(d). Due to a differential-input current-controlled floating current source, the COA exhibits ideally infinite differential current gain, output impedance, zero common mode current gain and differential input impedance. Thus, the COA performs the current-mode counterpart of the conventional VOA. The transconductance stage is realized in many different ways, i.e. a differential output current conveyor using multiple output current mirrors.

In this work, a CMOS differential-input, differential-output current operational amplifier for an equally useful general signal processing element is proposed and analyzed. It is configured from an input transimpedance stage followed by a transconductance output stage. Section 3.2 shows the circuit configuration and the performance analysis of the proposed COA. Section 3.3 presents the closed-loop operation of the proposed COA. Design considerations of COA have been discussed in section 3.4. Aspect ratio of the transistors and the layout of the design have been given in section 3.5 and 3.6 respectively.

3.2 CURRENT-MODE OPERATIONAL AMPLIFIER (COA)

The aim is to design a current operational amplifier with a differential input and a differential output, where the two output terminals are high impedance nodes with a current source/sink capability. This is a versatile amplification scheme with floating input and output terminals, which provides maximum freedom to the designer to compose practically any kind of application. Various current-mode building blocks have been proposed for active networks and analog computational applications. The applications of the COA include the implementation of instrumentation amplifier, current comparator with hysteresis, gyrator, and differential switched-current filter [8]. In this work, the current operational amplifier is implemented using a transimpedance input stage followed by a transconductance output stage. The circuit schematic of the COA is shown in Figure 3.2. An output stage providing the complementary output is the differential floating

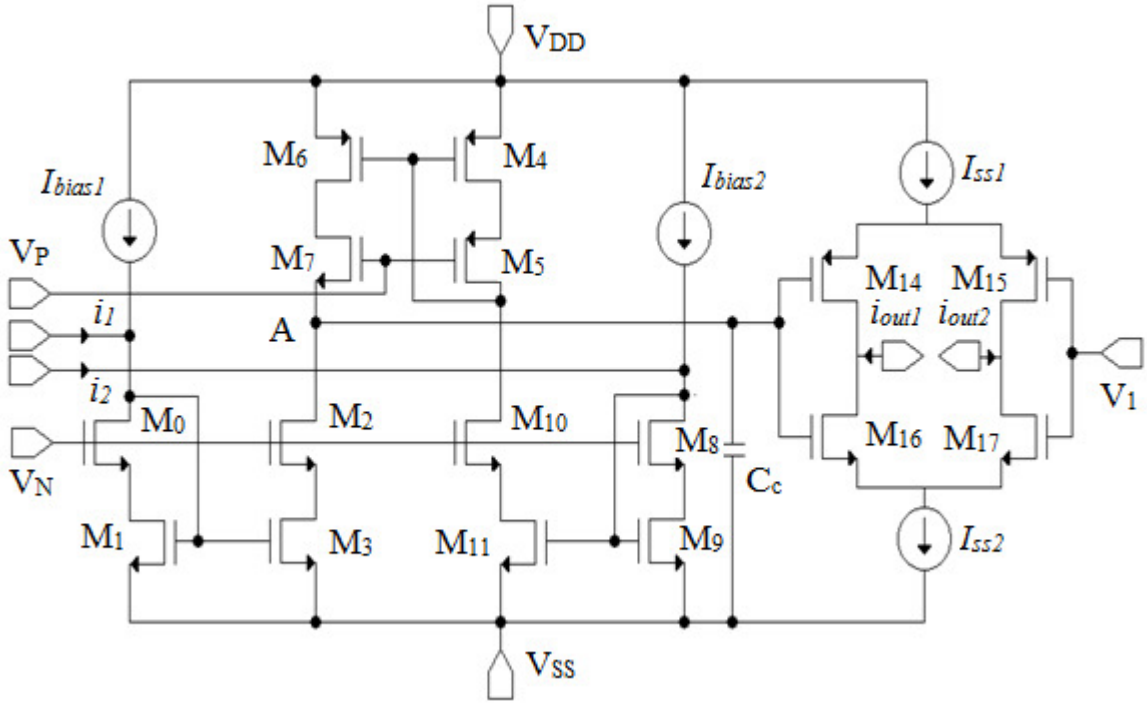


Figure 3.2 Transistor diagram of Current Operational Amplifier.

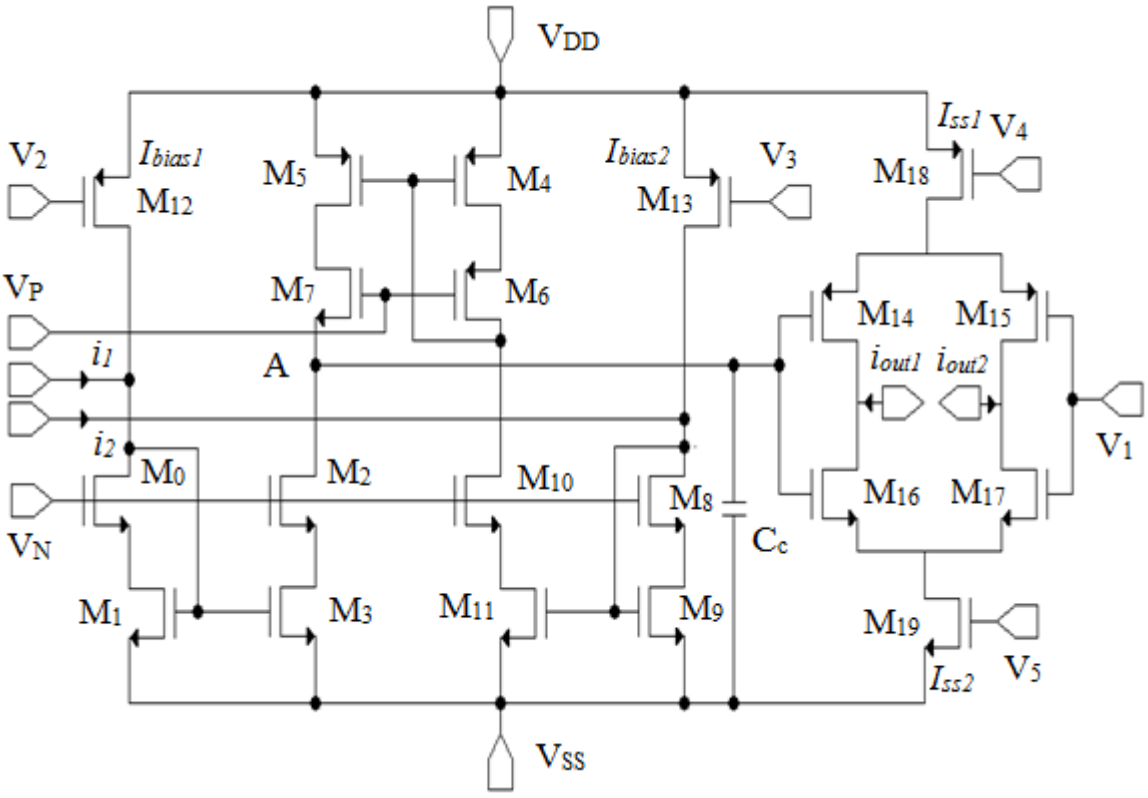


Figure 3.3 Detailed transistor diagram of Current Operational Amplifier.

current source (FCS) described by Arbel and Goldminz. Essentially, this stage is just two matched CMOS inverters biased by a constant supply current and operated as an analog transconductance stage .

3.2.1 OPEN-LOOP GAIN, COMMON MODE REJECTION RATIO (CMRR), INPUT OFFSET CURRENT

Extending the large signal analysis for the current operational amplifier in Figure 3.2, calculating the relation of the input node currents, i_1 and i_2 to the output node (A) current in the transimpedance stage, and the input node (A) current to the output node currents, i_{out1} and i_{out2}, in the transconductance stage (ignoring the I_{SS1} and I_{SS2} bias current effect in Eq. (3.1), we find

$$i_{out1} = -i_{out2} = [(I_{bias1} + i_1)\lambda_1 - (I_{bias2} + i_2)\lambda_2\lambda_3]R_A\left(\frac{g_{m14} + g_{m16}}{2}\right)$$

$$= [(\lambda_1 I_{bias1} - \lambda_2\lambda_3 I_{bias2}) - \left(\frac{\lambda_1 + \lambda_2\lambda_3}{2}\right)(i_1 - i_2) + (\lambda_1 - \lambda_2\lambda_3)(\frac{i_1 + i_2}{2})]R_A\left(\frac{g_{m14} + g_{m16}}{2}\right)$$

=offset + differential gain + common mode gain, (3.1)

where $I_{bias1,}\ I_{bias2}$ are bias currents.

λ_1 = current mirror ratio function of $M_{0,1}$ to $M_{2,3}$

λ_2 = current mirror ratio function of $M_{4,5}$ to $M_{6,7}$

λ_3 = current mirror ratio function of $M_{8,9}$ to $M_{10,11}$

$$R_A = \left(\frac{1}{g_{ds3}}\frac{g_{m2}}{g_{ds2}}\right)\left(\frac{1}{g_{ds6}}\frac{g_{m7}}{g_{ds7}}\right), \quad (3.2)$$

so I_{off} equivalent input offset current

$$I_{off} = (\lambda_1 I_{bias1} - \lambda_2\lambda_3 I_{bias2}), \quad (3.3)$$

ignoring I_{SS1} and I_{SS2}.

A_{dm} differential mode current gain is $A_{dm} = \left(\frac{i_{out1}}{i_d}\right)$

$$= \left(\frac{\lambda_1 + \lambda_2\lambda_3}{2} \right) R_A \left(\frac{g_{m14} + g_{m16}}{2} \right). \tag{3.4}$$

i_d differential mode current input

$$i_d = (i_1 - i_2). \tag{3.5}$$

i_c common mode current input

$$i_c = \left(\frac{i_1 + i_2}{2} \right). \tag{3.6}$$

A_{cm1} common mode current gain of stage 1

$$A_{cm1} = \left(\frac{V_A}{\frac{i_1 + i_2}{2}} \right) = (\lambda_1 - \lambda_2\lambda_3) R_A. \tag{3.7}$$

A_{cm2} common mode current gain of stage 2

$$A_{cm2} = \left(\frac{\frac{|i_{out1}| + |i_{out2}|}{2}}{V_A} \right) = \left(\frac{1}{4} \frac{1}{R_{SS1} \| R_{SS2}} \right), \tag{3.8}$$

where R_{SS1}, R_{SS2} are output resistances of the current sources I_{SS1} and I_{SS2}, respectively.

A_{CM} total common mode current gain [8]

$$A_{CM} = A_{cm1} \times A_{cm2} = \left(\frac{|i_{out1}| + |i_{out2}|}{i_1 + i_2} \right)$$

$$= \frac{1}{4} (\lambda_1 - \lambda_2\lambda_3) \left(\frac{R_A}{R_{SS1} \| R_{SS2}} \right). \tag{3.9}$$

We also find the common mode rejection ratio (defined as the differential gain divided by common gain) given by

$$CMRR = \frac{(\lambda_1 + \lambda_2\lambda_3)}{(\lambda_1 - \lambda_2\lambda_3)} (g_{m14} + g_{m16})(R_{SS1} \| R_{SS2}) \ . \tag{3.10}$$

It is seen that an arbitrarily high CMRR can be achieved through the use of a current source. The impedance R_A is increased by employing a high swing cascode current mirror. So, the current gain is therefore increased by trading of power dissipation and chip area [9].

3.2.2 FREQUENCY RESPONSE, GAIN-BANDWIDTH AND STABILITY

The configuration shown in Figure 3.2 has one high impedance node A in the signal path. It creates a dominant pole in the frequency response given by

$$f_{pd} = \frac{1}{2\pi}\frac{1}{R_A C_A}, \tag{3.11}$$

$$C_A = C_{gd2} + C_{gd7} + C_{gd14} + C_{gd16} + \frac{C_{gs14}}{2} + \frac{C_{gs16}}{2}, \tag{3.12}$$

where C_A is the total parasite capacitance of node A, and is dominated by the gate source capacitances C_{gs14} and C_{gs16} of the transconductance stage. The first non-dominant pole is typically caused by the current mirror stage which contributes at angular frequencies of the order of $g_m / 2C_{gs.}$ In addition, the parasite capacitances (C_{bd}) influence the dominant and the non-dominant poles that can be reduced by using an optimized transistor layout style, e.g. multi-finger structure for the gate. The gain-bandwidth product is

$$GBW = \frac{1}{2\pi C_A}\left(\frac{\lambda_1 + \lambda_2\lambda_3}{2}\right)(g_{m14} + g_{m16}). \tag{3.13}$$

In a voltage operational amplifier, the compensation capacitance separates the dominant and non-dominant poles to provide the desired unity gain phase margin, while in the current operational amplifier, additional capacitance could be added at node A [8].

3.2.3 INPUT AND OUTPUT IMPEDANCE

The input impedance is $$R_{in} = \frac{1}{g_{m1} + g_{m9}}. \tag{3.14}$$

The output impedance of the COA is the conductance of the transconductance stage. It can be increased using the regulated cascode scheme [8]. It is given by

$$R_{out} = \left[(g_{ds14})^{-1} \| (g_{ds16})\right] + \left[(g_{ds15})^{-1} \| (g_{ds17})^{-1}\right]. \quad (3.15)$$

3.2.4 INPUT COMMON MODE RANGE (ICMR)

For bias current, $I_{\text{bias1}} = I_{\text{bias2}} = I$, the equal positive and negative common mode ranges requires that (3.16) must be fulfilled [9].

$$I = \frac{1}{4}\left[\frac{V_{DD} - |V_{Tp}|}{[K_n (W/L)_n]^{-1/2} + [K_p (W/L)_p]^{-1/2}}\right]^2. \quad (3.16)$$

3.2.5 POWER SUPPLY REJECTION RATIO (PSRR)

The power supply rejection ratio is

$$PSSR, vdd \cong \left[-(g_{nodei1} + sC_{nodei1}) + (g_{nodei2} + sC_{nodei2}) + \left(\frac{g_{ds7}}{g_{m7}} g_{ds6} + sC_{gd7}\right) - \left(\frac{g_{ds10}}{g_{m10}} g_{ds11} + sC_{gd10}\right)\right]^{-1}$$

(3.17)

The PSRR,*vss* can be derived in the same manner. It is clear that the power supply rejection ratio for the COA has the dimension of a resistor [8].

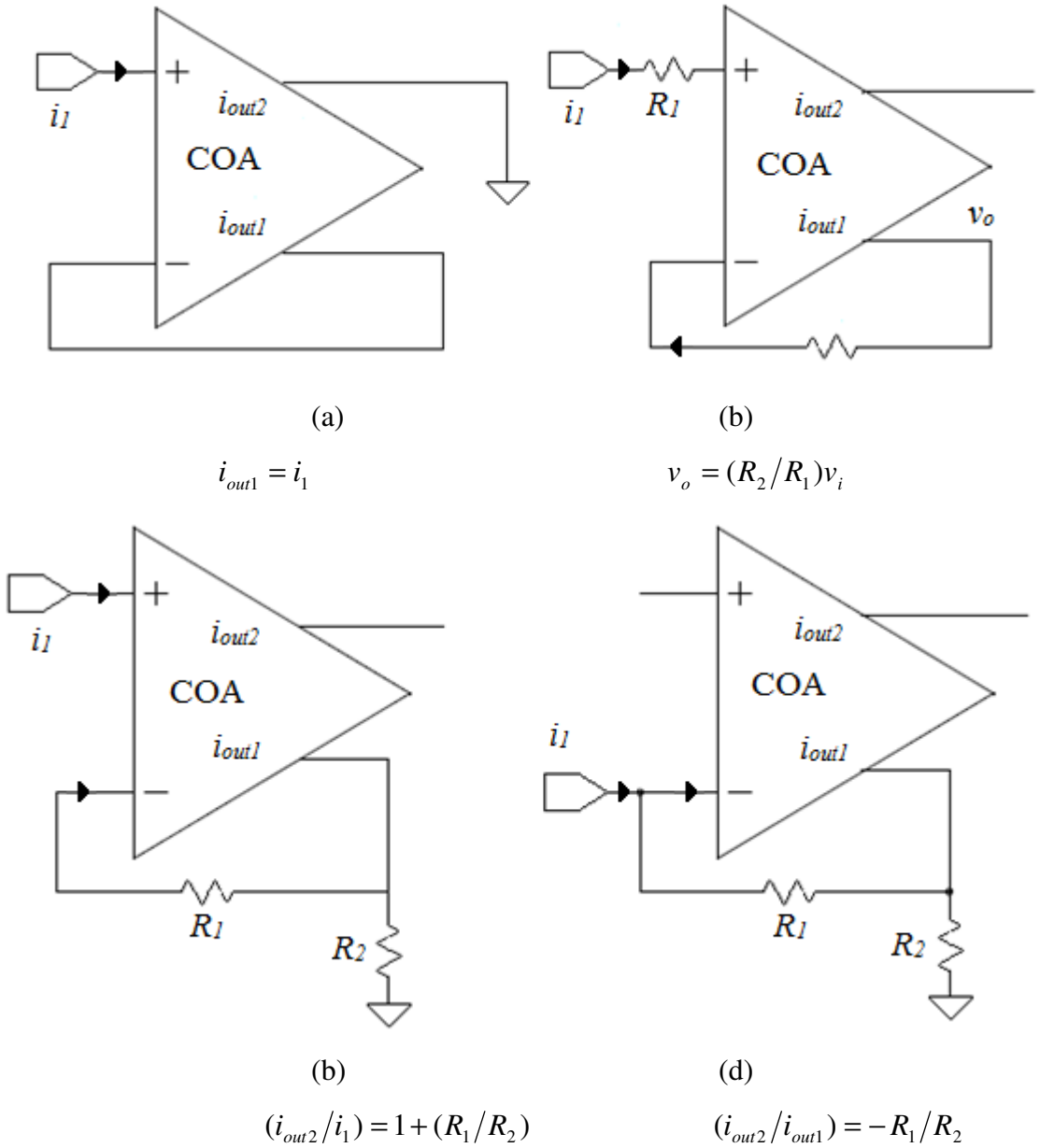
3.2.6 NOISE PERFORMANCE

The RMS value of the equivalent input noise current of the COA is

$$I_{ni}^2 = g_{mn}^2 \left(\sum_{x=0,1,2,3,8,9,10,11} V_{nx}^2\right) + g_{mp}^2 \left(\sum_{y=4,5,6,7} V_{ny}^2\right) + \left[\frac{2g_{m14}}{R_A (g_{m14} + g_{m16})}\right]^2 (V_{n14}^2 + V_{n15}^2) \quad (3.18)$$

3.3 CLOSED-LOOP CURRENT OPERATIONAL AMPLIFIER

Invoking duality, Figure 3.4 shows examples to investigate the closed-loop operation of the current operational amplifier. As shown in Figure 3.4, the closed-loop gain depends on the resistor ratio and not the open-loop gain characteristics. Negative feedback around the COA produces an accurate closed-loop current gain insensitive to temperature, power supply and process variations.



(a) $i_{out1} = i_1$

(b) $v_o = (R_2/R_1)v_i$

(b) $(i_{out2}/i_1) = 1 + (R_1/R_2)$

(d) $(i_{out2}/i_{out1}) = -R_1/R_2$

Figure 3.4 Basic feedback controlled current amplifiers in (a) unity current gain, (b) voltage gain, (c) non-inverting, (d) inverting configurations.

Thus, it has a constant gain-bandwidth independent of the open-loop current gain in a closed-loop configuration. Consequently, this circuit configuration is suitable for high frequency applications. An open-loop COA can be used as a current comparator in which the resolution is determined by the bias current and the open-loop current gain [8,11].

3.4 CURRENT OPERATIONAL AMPLIFIER DESIGN CONSIDERATIONS

In order to tailor the current operation amplifier to a particular application, a trade-off exists between circuit performances, the gain, the bandwidth, the noise, etc. These conditions often conflict with one another, and are also very sensitive to process variations. The procedures outlined in this section give an indication of how to design the COA efficiently to satisfy these performance requirements.

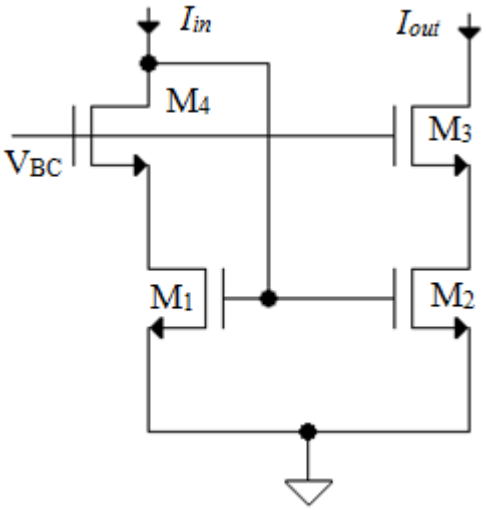


Figure 3.5 Low-Voltage Current Mirror.

The low voltage cascode current mirror is shown in Figure 3.5. We assume that the mirror transistors M_1 and M_2 have identical aspect ratio, i.e. $A_M = W_1/L_1 = W_2/L_2$ where W_1, W_2, L_1, and L_2 are the transistor channel widths and lengths for transistors M_1 and M_2, respectively. Similarly, M_3 and M_4 are assumed to have the same aspect ratio, $A_C = W_3/L_3 = W_3/L_4$. The aspect ratio A_M may be different from the aspect ratio A_C. In the analysis of the dynamic range we use the standard Shichman-Hodges transistor model for the transistor in the saturation region and we neglect the bulk-effect [10].

With the input current I_{in} we find the gate-source voltages:

$$V_{gs1} = V_T + \sqrt{\frac{2I_{in}}{KA_M}} \tag{3.19}$$

$$V_{gs3} = V_T + \sqrt{\frac{2I_{in}}{KA_C}} \tag{3.20}$$

$$V_{ds1} = V_{BC} - V_{gs3} = V_{BC} - V_T - \sqrt{\frac{2I_{in}}{KA_C}} \tag{3.21}$$

$$V_{ds3} = V_{gs1} - V_{BC} + \sqrt{\frac{2I_{in}}{KA_C}}\left(\frac{1}{\sqrt{A_M}} + \frac{1}{\sqrt{A_C}}\right) \tag{3.22}$$

where V_T is the transistor threshold voltage, V_{BC} is the cascode transistor gate voltage, and K is the transistor transconductance parameter.

Requiring $V_{gs} - V_T \le V_{ds}$ for both M_1 and M_3 results in:

$$\sqrt{\frac{2I_{in}}{K}}\left(\frac{1}{\sqrt{A_M}} + \frac{1}{\sqrt{A_C}}\right) + V_T \le V_{BC} \tag{3.23}$$

$$V_{BC} \le 2V_T + \sqrt{\frac{2I_{in}}{KA_M}} \tag{3.24}$$

Eq. (3.23) ensures saturation of M_1 and determines the maximum value of I_{in}, for a given value of the cascode bias voltage $\boldsymbol{V_{BC}}$. We find

$$I_{in,\max} = \frac{K}{2} A_M (V_{BC} - V_T)^2 \left(\frac{\sqrt{A_C / A_M}}{1 + \sqrt{A_C / A_M}} \right)^2 \tag{3.25}$$

Eq. (3.24) ensures saturation of M_3 and determines the minimum value of I_{in} . We find

$$I_{in,\min} = \frac{K}{2} (V_{BC} - 2V_T)^2 A_M \tag{3.26}$$

In a practical design procedure (3.26) can be used to determine the maximum value of the bias voltage which will ensure saturation of M_3, even at the minimum value of input current, and (3.25) can then be used to determine values of A_C and A_M which will ensure saturation of M_1, even at the maximum value of input current.

In the important special case of $I_{in,min} = 0$ we find from (3.26) $V_{BC} \leq 2V_T$. From (3.25) we then find the following design constraint on A_C and A_M:

$$A_M \left(\frac{\sqrt{A_C / A_M}}{1 + \sqrt{A_C / A_M}} \right)^2 \geq \frac{2I_{in,\max}}{V_T^2 K} \tag{3.27}$$

Assuming as a typical case $W_1 = W_3$ and $L_1 = L_3$, i.e. identical aspect ratios for the mirror transistors and the cascode transistors, we find

$$A_M = A_C = \frac{W}{L} \geq \frac{8I_{in,\max}}{V_T^2 K} \tag{3.28}$$

In this case the effective gate-source voltage of the mirror transistors M_1 and M_2 is

$$V_{gs1} - V_T = \sqrt{\frac{2I_{in}}{KA_M}} = \frac{V_T}{2} \sqrt{\frac{I_{in}}{I_{in,\max}}} \tag{3.29}$$

Obviously, in this case the minimum output voltage of the current mirror is

$$V_{out,\min} = V_{BC} - V_T = V_T \tag{3.30}$$

3.5 ASPECT RATIOS OF THE TRANSISTORS IN THE DESIGN

Based on the procedure discussed in section 3.4 the aspect ratios of the transistors in Figure 3.2 are calculated as follows:

Table 3.1 Aspect ratios of Transistors used in the design.

Device	Width/Length in (μm/μm)	Device	Width/Length in (μm/μm)
M_0	35/0.5	M_{10}	35/0.5
M_1	35/0.5	M_{11}	35/0.5
M_2	35/0.5	M_{12}	25/0.5
M_3	35/0.5	M_{13}	25/0.5
M_4	25/0.5	M_{14}	166/0.5

Device	Width/Length in (μm/μm)	Device	Width/Length in (μm/μm)
M_5	25/0.5	M_{15}	166/0.5
M_6	25/0.5	M_{16}	45/0.5
M_7	25/0.5	M_{17}	45/0.5
M_8	35/0.5	M_{18}	520.98/0.5
M_9	35/0.5	M_{19}	83.75/0.5

3.6 PHYSICAL LAYOUT DESIGN OF CURRENT OPERATIONAL AMPLIFIER

The physical layout design of Current operational amplifier has been done in standard UMC 0.18 μm CMOS process technology. The VIRTUOSO layout editor tool by CADENCE was used for the design of physical layout structure. The layout is shown in the Figure 3.6. To verify that the layout fulfills all electrical and geometric rules a Design Rule Check (DRC) program is used. ASSURA tool was used for DRC checks. This tool marks any error in the design and can also extracts (i.e. convert to a netlist) the layout so that it can be simulated. The extracted layout view is shown in the Figure 3.7.

Basic Design Rules are summarized below:

Metal 1 to metal 1 spacing	0.24 um
Minimum contact size	0.24 um*0.24 um
Poly to poly spacing	0.24 um
Poly to metal spacing	0.28/0.00 um
Contact overlap to p+ diffusion	0.1 um
Metal 1 width	0.24 um
Poly extension beyond active	0.22 um
Minimum contact spacing	0.26 um
N well overlap p+ diffusion	0.43 um
Diffusion contact to poly spacing	0.15 um
Minimum p+ implant overlap p+ diffusion	0.22 um
Poly width	0.18 um
Minimum poly extension on to field region	0.22 um
Minimum poly gate to field edge spacing	0.28 um

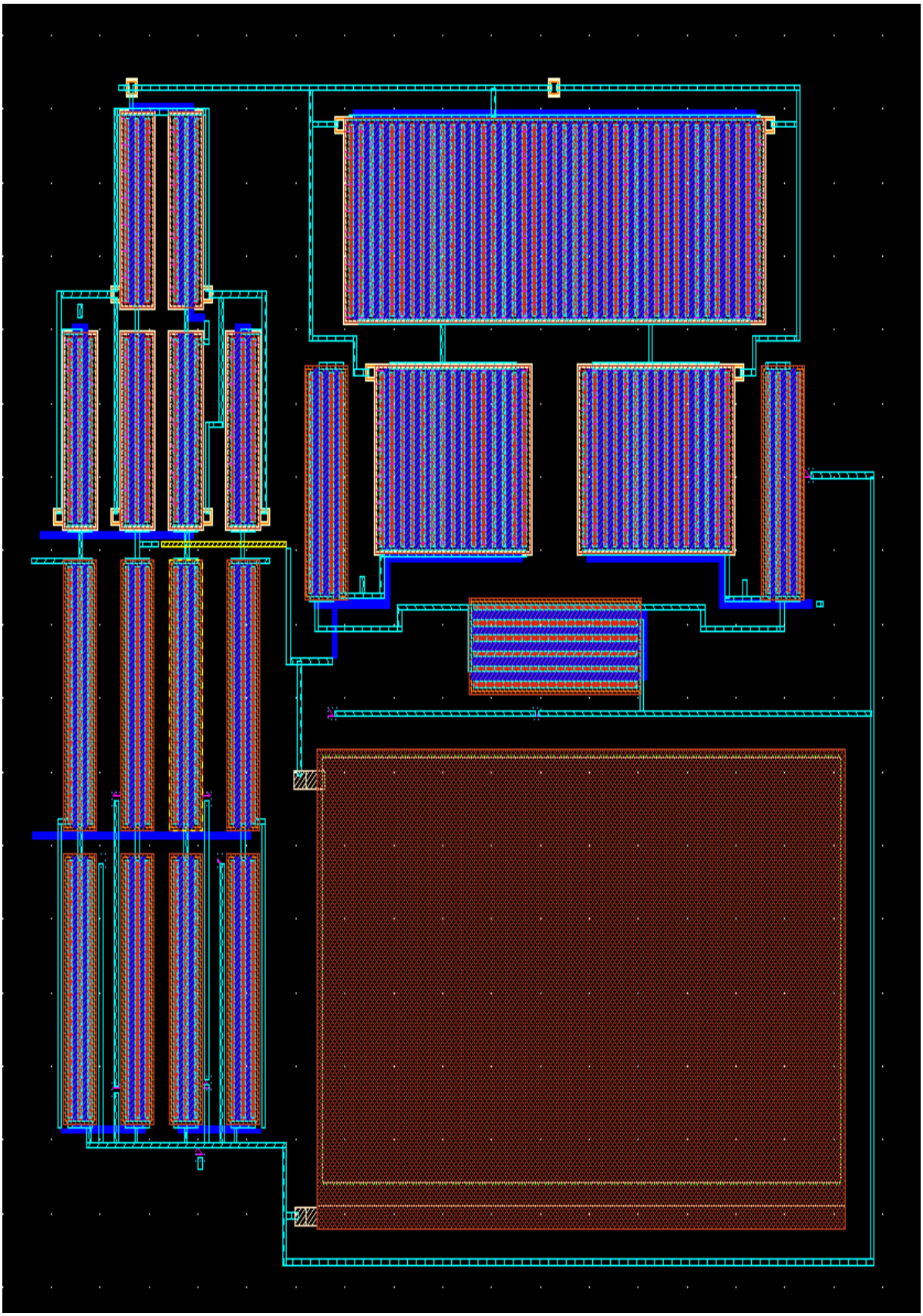


Figure 3.6 Layout of Current Operational Amplifier.

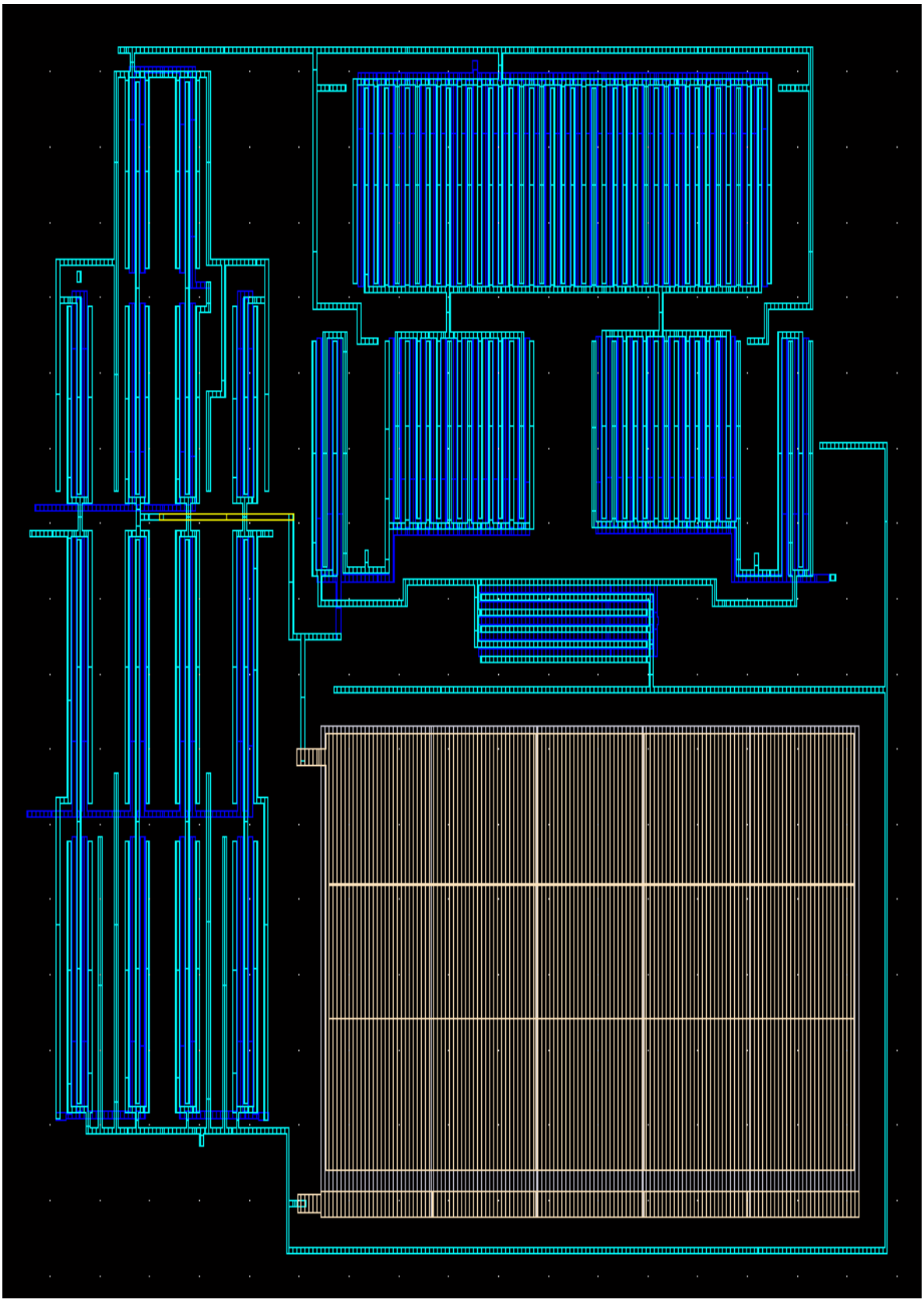


Figure 3.7 Extracted View of the Layout.

Poly contact to diffusion edge spacing	0.18 um
Minimum poly overlap contact	0.1 um
Minimum metal area	0.1764 um*um
Gate poly spacing over diffusion	0.34 um
Minimum metal2 width	0.28 um
Metal1 and metal2 overlap over via	0.08 um
Minimum equal potential N-well spacing	0 um or >=0.9 um
Minimum non equal potential 1.8 V N well spacing	1.5um

CHAPTER 4 SIMULATIONS AND RESULTS

In this chapter, schematic of the fully differential current-mode operational amplifier and extracted view (netlist) of its layout have been tested for various parameters of current operational amplifier. The simulations with schematic and extracted view of layout are also called the pre-layout and post-layout simulations respectively. VIRTUOSO schematic composer and layout editor tools were used for capturing schematic and layout drawing respectively. The circuit was simulated using SPECTRE tool by CADENCE. The circuit design is based upon the parameters of the UMC 0.18 μm CMOS process technology. The technology uses the SPICE BSIM3v3 Version 3.2 model parameters.

4.1 TEST RESULTS

In this section, simulation results with schematic and extracted view of layout have been discussed. Finally with post-layout simulation at typical corner the design provides a gain of 65.38 dB with a common mode rejection ratio of 73.59 dB. The 3 dB frequency and unity gain frequency are 220.20 kHz and 353.60 MHz respectively. Slew rate was obtained to be 37.17 μA/ns. Phase margin was found to be 53.60^0 making design relatively stable. The power dissipation was equal to 5.72 mW. The values of load resistance and compensating capacitance are given in the table below.

Table 4.1 Load resistance and compensating capacitance

	Pre-layout	Post-layout
Load Resistance, $R_L(\Omega)$	2	2
Compensating Capacitance, C_c(pF)	3	1.5493

The value of capacitance in the Table 4.1 are different for the two simulations because the circuit layout has been optimized for reasonable phase margin.

4.1.1 CURRENT-GAIN, 3-dB FREQUENCY, UNITY GAIN FREQUENCY AND PHASE MARGINE

The differential gain, 3-dB frequency, unity gain frequency and phase margin are obtained from gain and phase plot. The circuit is shown in the Figure 4.1. The circuit is in open-loop configuration and AC current signal is applied at the input. The pre-layout and post-layout gain and Phase plots at typical corner are shown in the Figure 4.2 and 4.3 respectively.

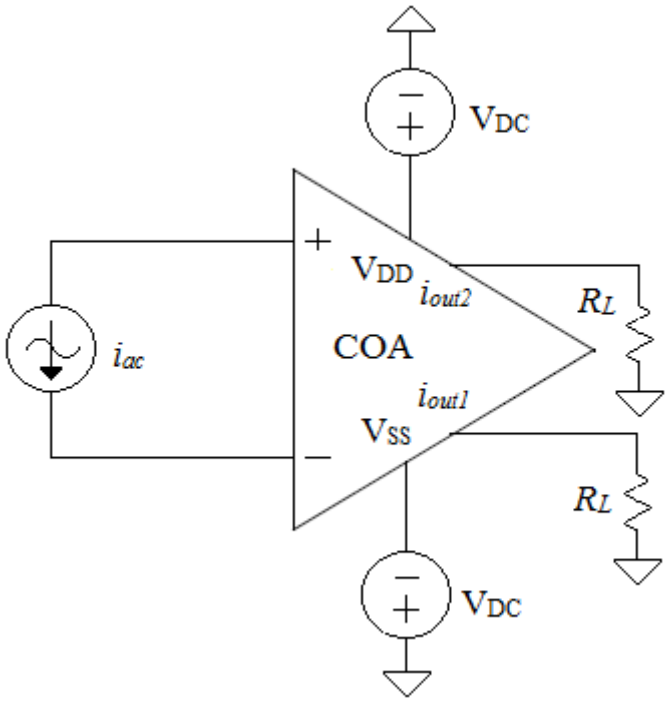


Figure 4.1 Schematic for the frequency response of the open-loop current operational amplifier.

The AC results at different corners of simulations are given below:

Table 4.2 Pre-layout AC results at different process corners of simulations.

Specifications	Process Corners				
	tt	ff	ss	snfp	fnsp
Differential Gain (dB)	64.50	61.52	66.54	61.67	66.85
3 dB Frequency (kHz)	216.1	376.4	133.3	312.6	161.6
Unity Gain Frequency (MHz)	343.6	412.1	275.2	354.2	330.6
Phase Margin(degree)	55.90	54.60	60.56	56.44	57.24

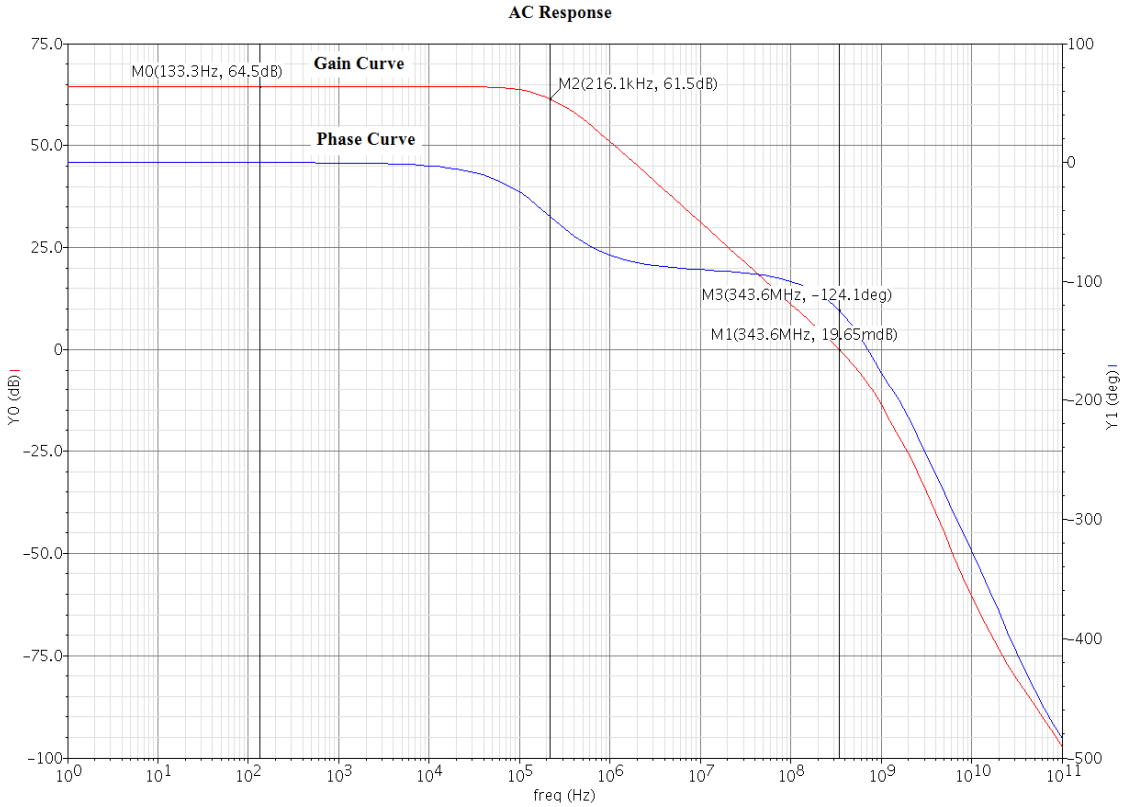


Figure 4.2 Pre-layout frequency response of the current operational amplifier at typical corner .

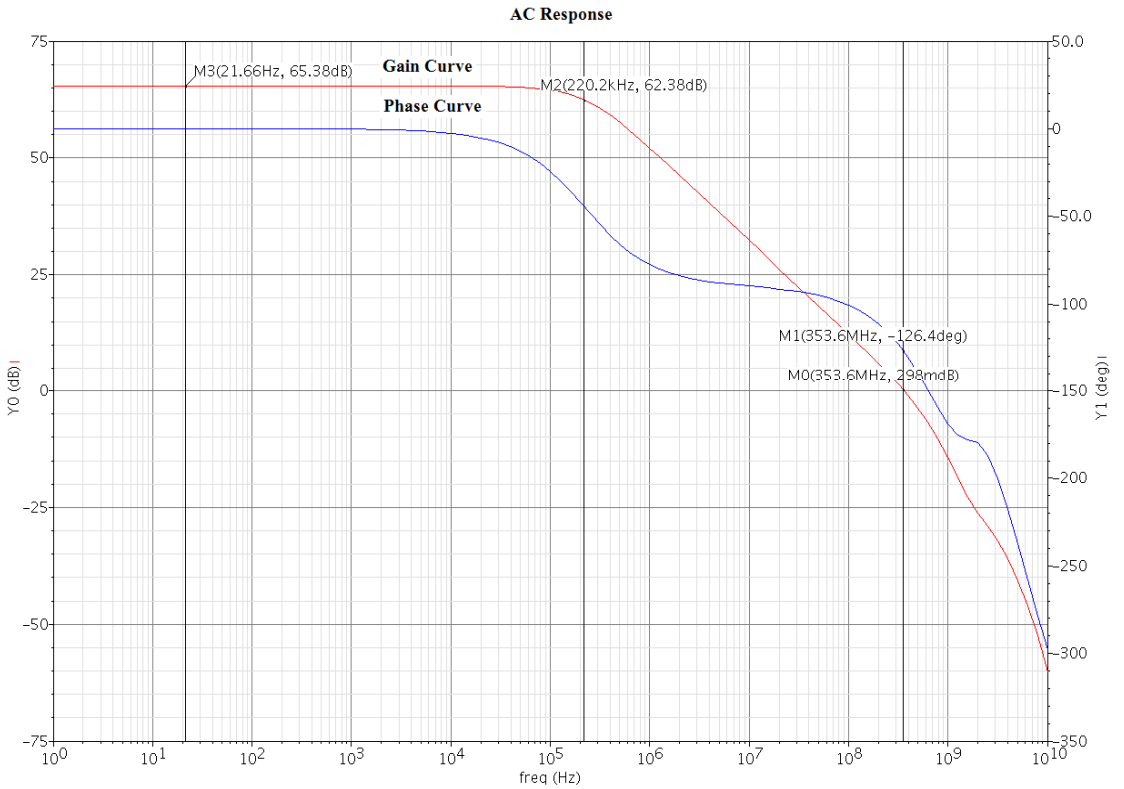


Figure 4.3 Post-layout frequency response of the current operational amplifier at typical corner.

Table 4.3 Post-layout AC results at different process corners of simulations

Specifications	Process Corners				
	tt	ff	ss	snfp	fnsp
Differential Gain (dB)	65.38	63.57	66.46	61.75	68.02
3 dB Frequency (kHz)	220.2	342.2	152.83	338.68	161.6
Unity Gain Frequency (MHz)	353.6	445.81	288.42	361.21	353.97
Phase Margin(degree)	53.60	50.40	56.43	51.99	53.89

The effect of temperature on these parameters is given below in the following table.

Table 4.4 Post-layout AC results at different temperatures at typical corner

Specifications	Temperature		
	-20^0	27^0	80^0
Differential Gain (dB)	66.79	65.38	61.29
3 dB Frequency (kHz)	168.1	220.2	342.45
Unity Gain Frequency (MHz)	329.6	353.6	338.2
Phase Margin(degree)	58.90	53.60	50.78

The result shows that the design has a very high gain and there is very less effect of temperature variation on its gain. The high gain can be used to obtain an accurate gain in closed-loop operation.

4.1.2 TRANSIENT RESULTS

The circuit for transient analysis is shown in Figure 4.4 and 4.5. Since the gain of the amplifier is very high hence the open-loop configuration can be used as a current comparator in which the resolution is determined by the biasing current and the open-loop current gain. Hence transient simulations in open-loop and unity gain configuration both are shown below in Figure 4.6, 4.7, 4.8, and 4.9.

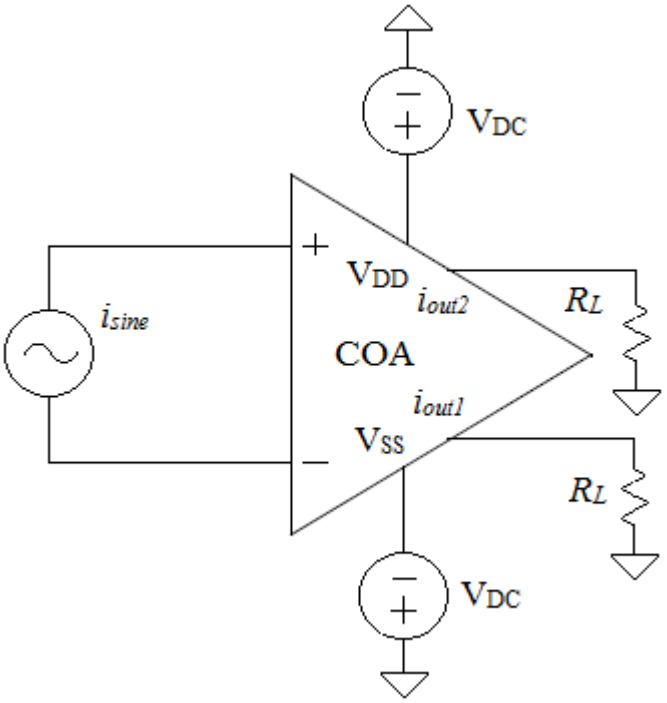


Figure 4.4 Schematic for transient analysis of the open-loop current operational amplifier.

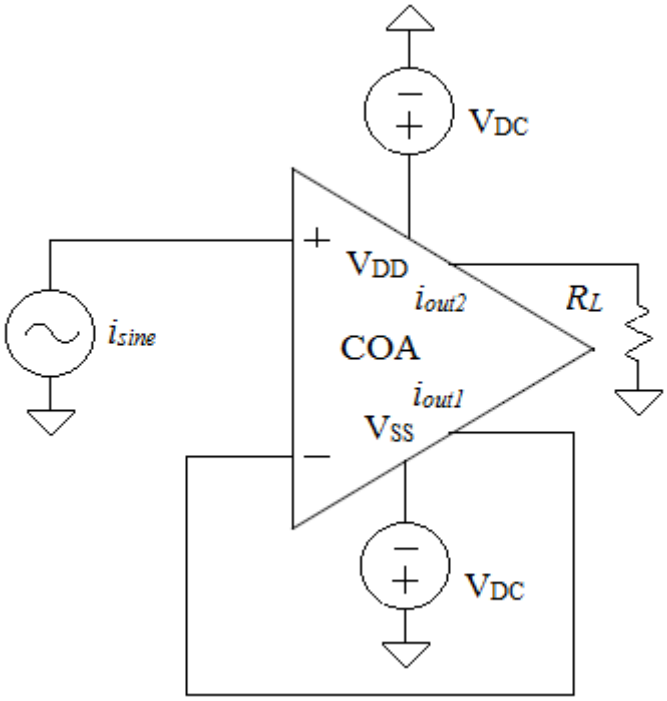


Figure 4.5 Schematic for transient analysis of current operational amplifier configured as unity gain buffer.

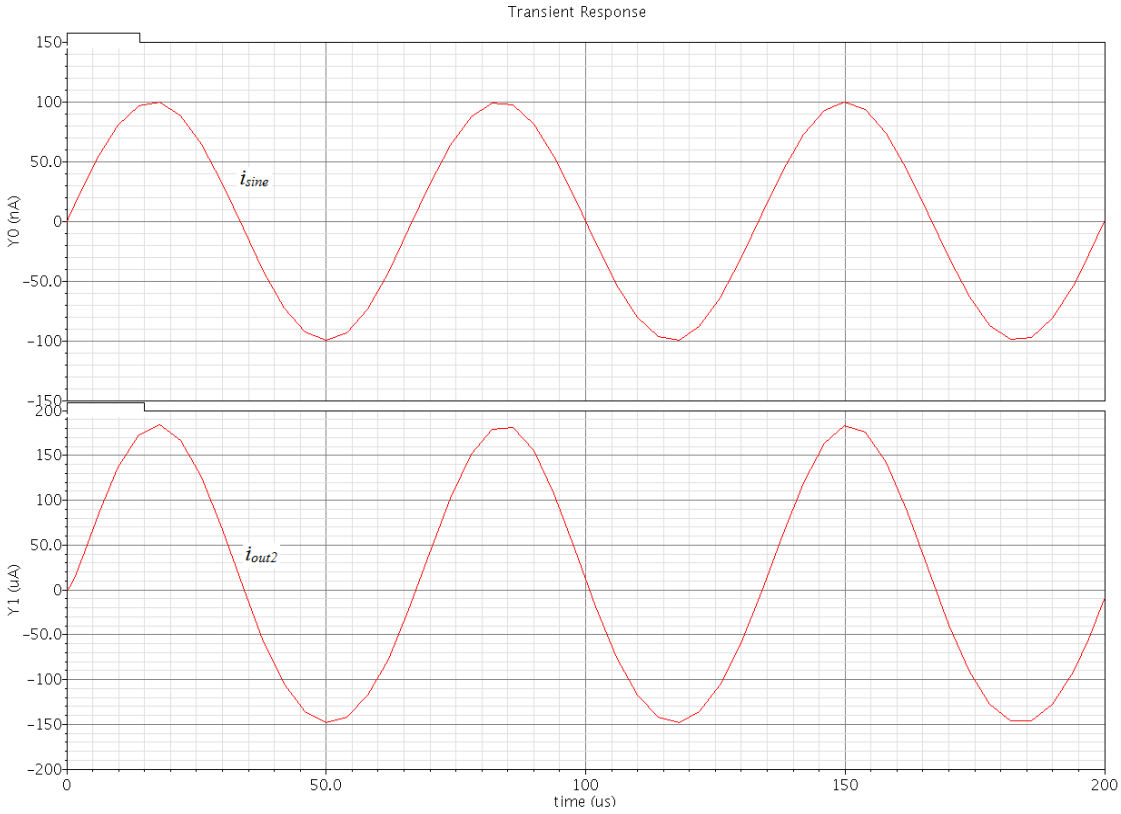


Figure 4.6 Pre-layout transient response of current operational amplifier in open loop configuration at typical corner.

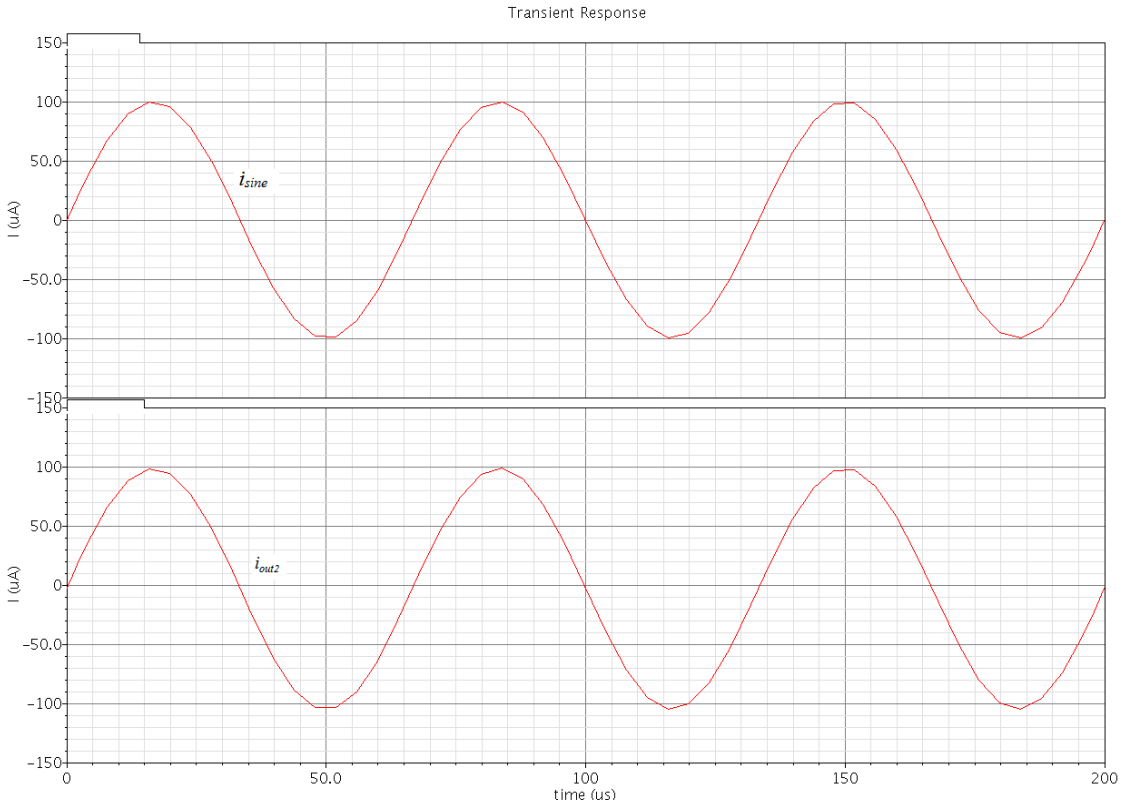


Figure 4.7 Pre-layout transient response of current operational amplifier in unity gain configuration at typical corner.

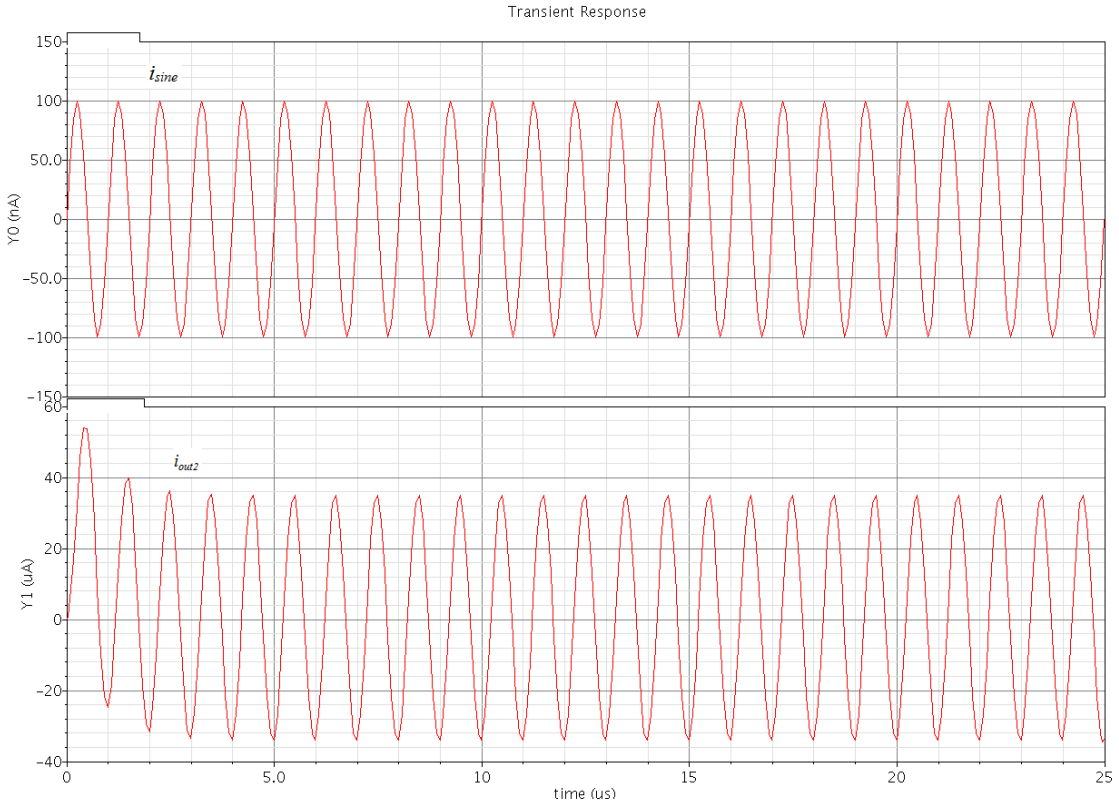


Figure 4.8 Post-layout transient response of current operational amplifier in open-loop configuration at typical corner.

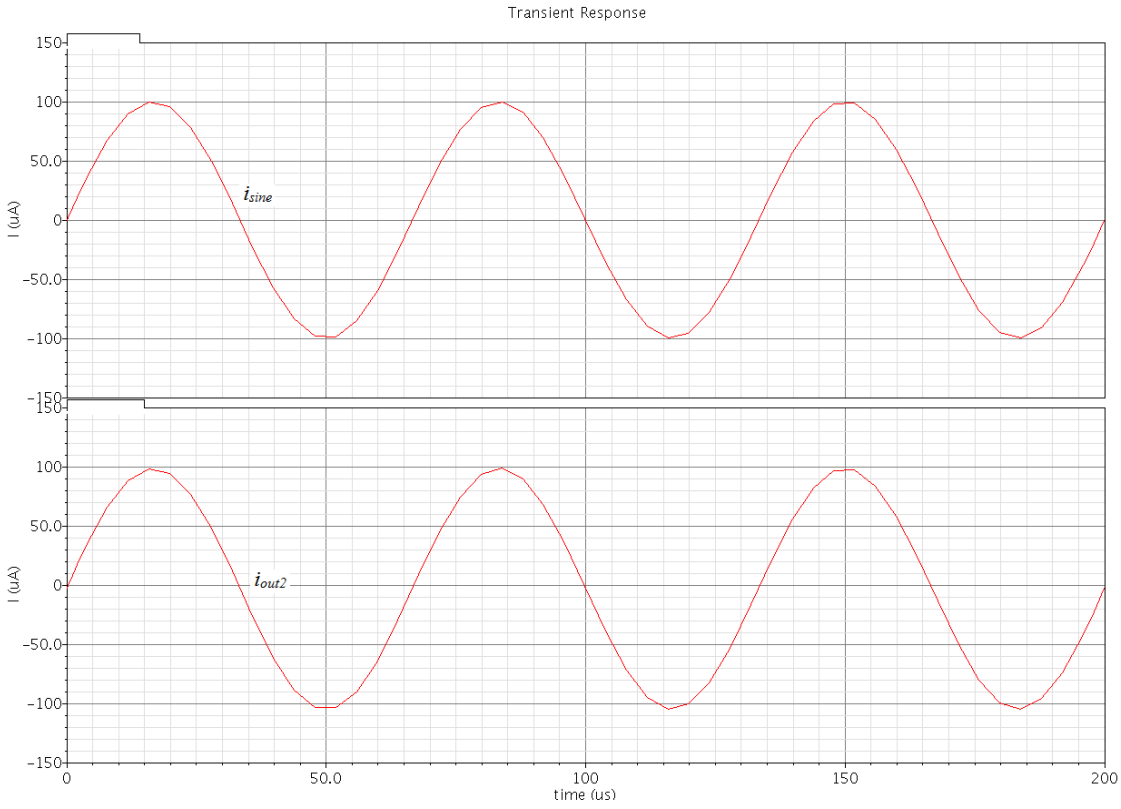


Figure 4.9 Post-layout transient response of current operational amplifier in unity gain configuration at typical corner.

4.1.3 COMMON MODE REJECTION RATIO

The schematic for common mode gain is given in Figure 4.10. When common mode gain (dB) is subtracted from the differential gain (dB) we obtain the common mode rejection ratio. The CMRR curve is shown in the Figure 4.11.

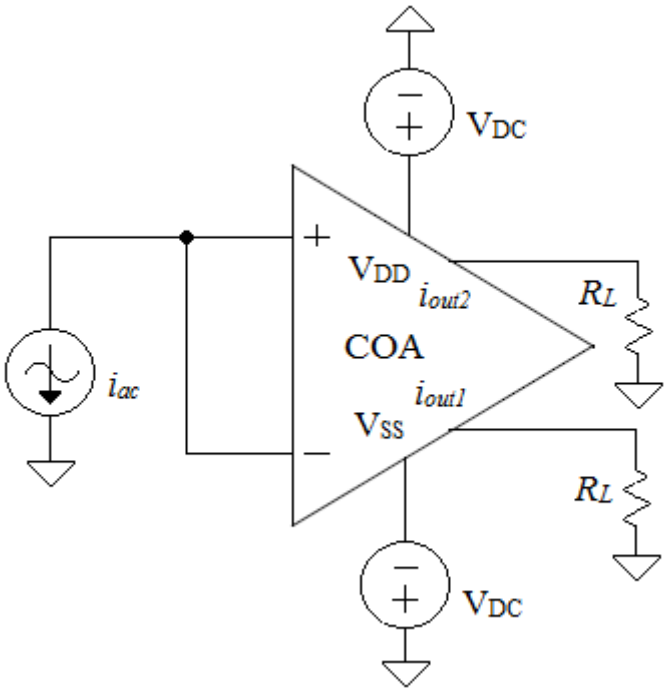


Figure 4.10 Schematic for measuring common mode gain.

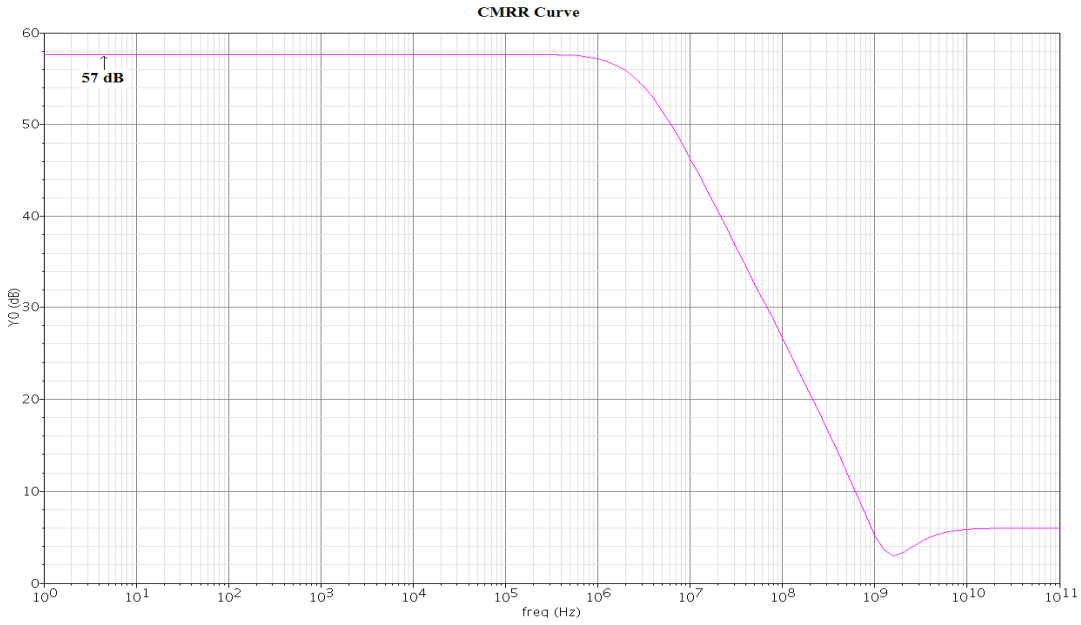


Figure 4.11 Pre-layout CMRR curve at typical corner.

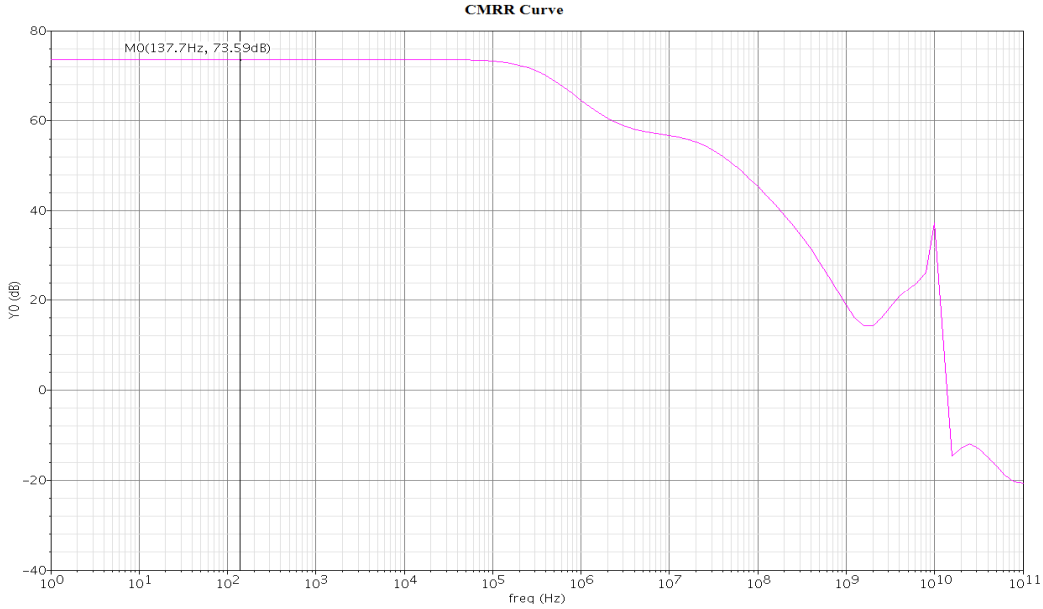


Figure 4.12 Post-layout CMRR curve at typical corner.

The values of CMRR at different process corners of simulations are given in the table below

Table 4.5 Pre-layout CMRR values at different process corners of simulation

Specifications	Process Corners				
	tt	ff	ss	snfp	fnsp
CMRR (dB)	57.0	53.01	61.07	54.79	59.86

Table 4.6 Post-layout CMRR values at different process corners of simulation

Specifications	Process Corners				
	tt	ff	ss	snfp	fnsp
CMRR (dB)	73.5	73.8	103.2	76.6	94.5

The effect of temperature variation on CMRR is given below

Table 4.7 Post-layout CMRR values at different temperatures at typical corner

Specification	Temperature		
	-20^0	27^0	80^0
CMRR (dB)	117.3	73.5	64.9

The result shows that the design has very high common mode rejection ratio in post-layout simulation as compared to pre-layout simulation.

4.1.4 POWER SUPPLY REJECTION RATIO

The schematic for PSRR,vdd(0), and PSRR,vss(0) are shown in Figure 4.13(a) and 4.13(b) respectively. The responses are shown in Figure 4.14, 4.15, 4.16, and 4.17.

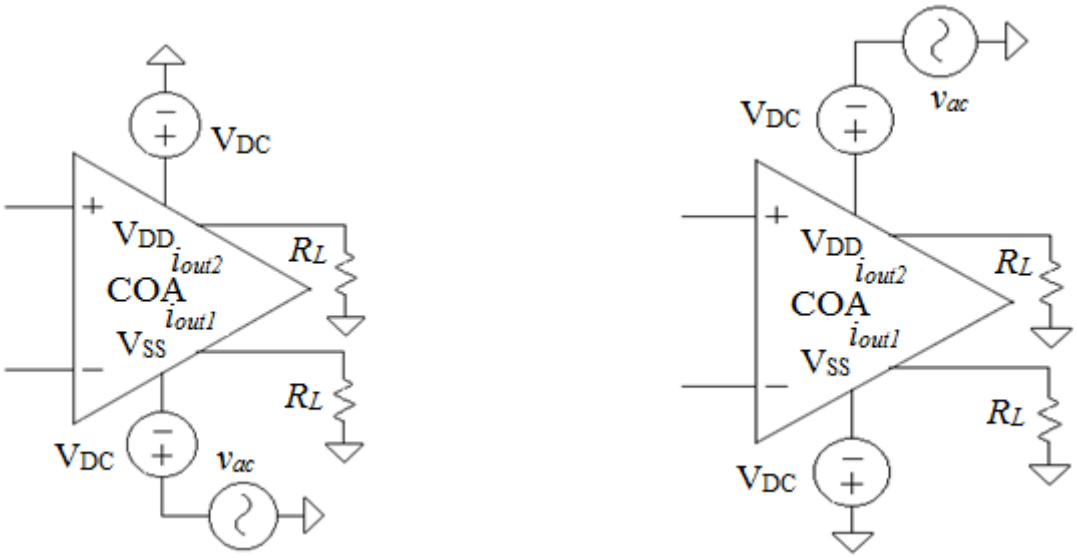


Figure 4.13 Schematic for measuring (a) PSRR,vdd (0) and (b) PSRR,vss (0).

The values of PSRR at different process corners of simulations are given in the table below:

Table 4.8 Pre-layout PSRR values at different process corners of simulation

Specifications	Process corners				
	tt	ff	ss	snfp	fnsp
PSRR, vdd(0) (dBΩ)	113.39	107.17	116.85	110.67	113.85
PSRR, vss(0) (dBΩ)	114.02	108.46	116.95	109.52	116.23

Table 4.9 Post-layout PSRR values at different process corners of simulation

Specification	Process corners				
	tt	ff	ss	snfp	fnsp
PSRR,vdd(0) (dBΩ)	109.19	104.93	110.85	106.42	109.58
PSRR,vss(0) (dBΩ)	108.02	102.94	111.17	104.21	109.82

The effect of temperature on PSRR is given in the following table.

Table 4.10 Post-layout PSRR values at different temperatures

Specifications	Temperature		
	-20^0	27^0	80^0
PSRR, vdd(0) (dBΩ)	107.56	109.19	108.80
PSRR, vss(0) (dBΩ)	111.01	108.02	105.91

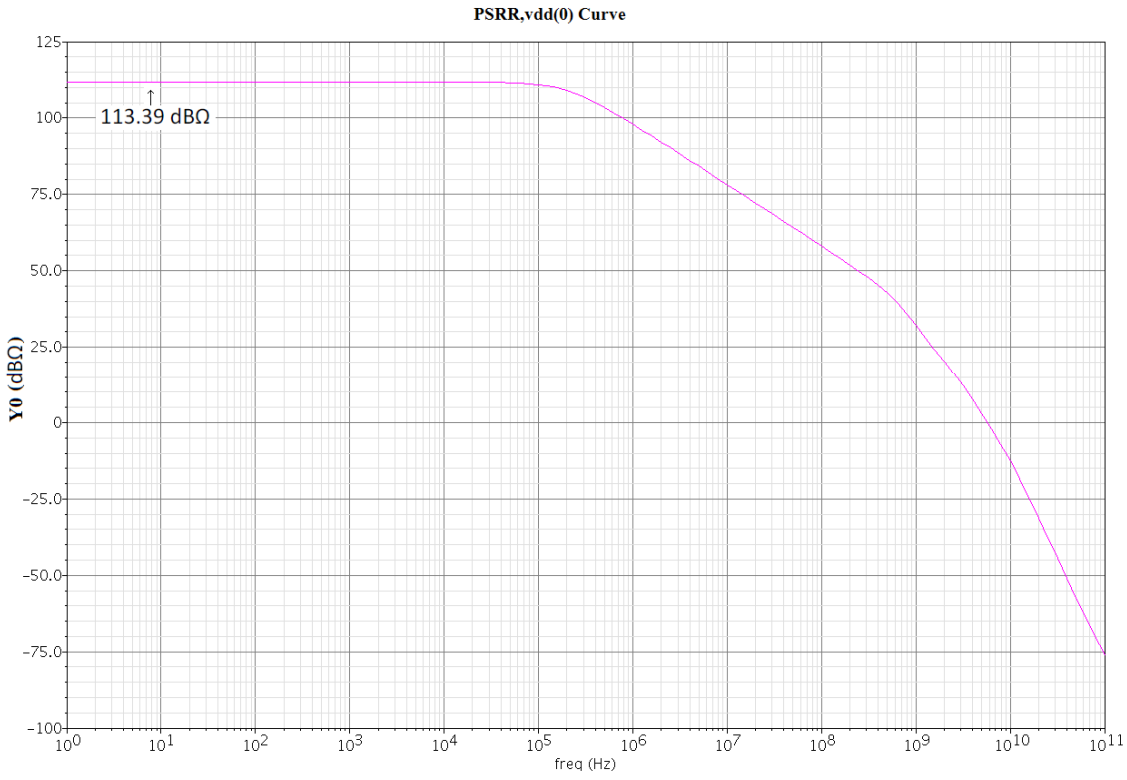


Figure 4.14 Pre-layout PSRR, *v*dd (0) curve at typical corner.

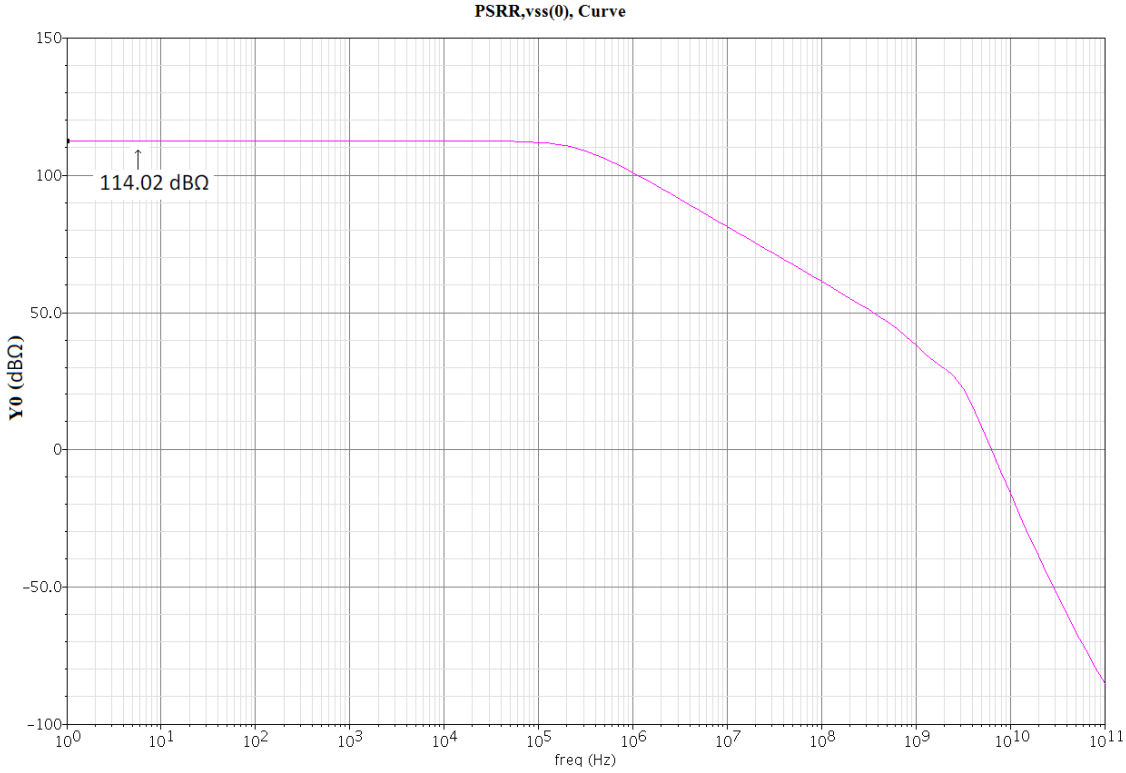


Figure 4.15 Pre-layout PSRR,*v*ss (0) curve at typical corner.

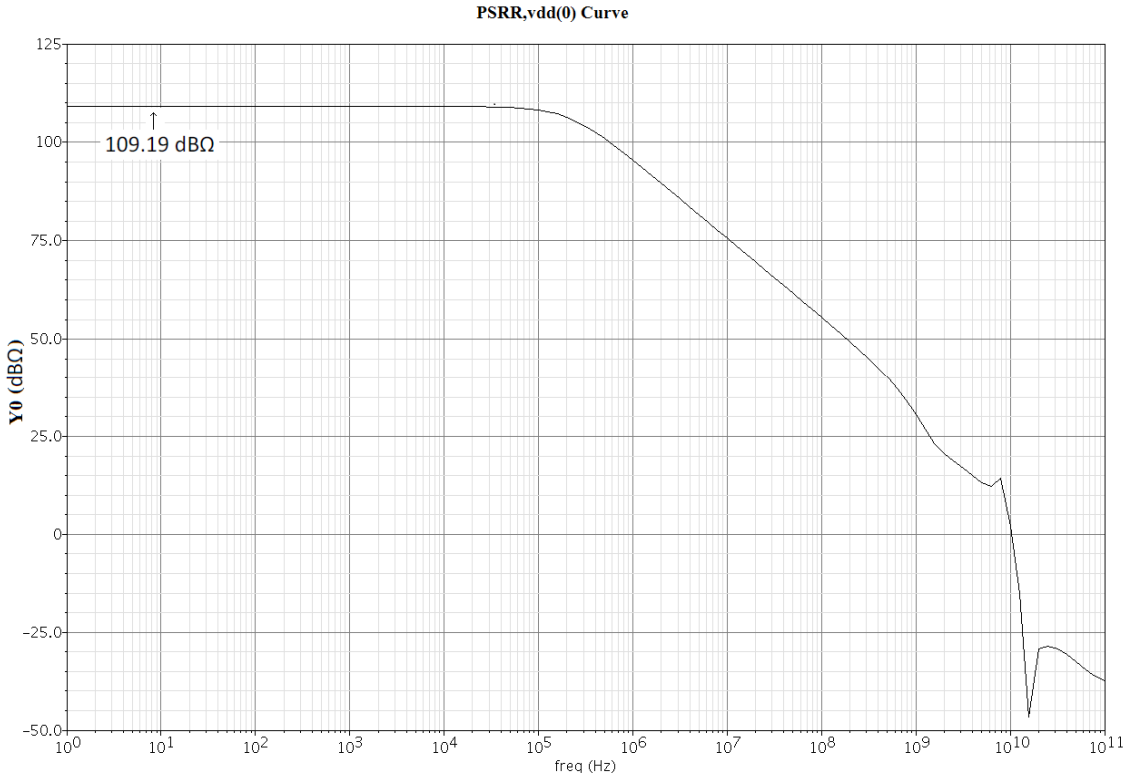


Figure 4.16 Post-layout PSRR,*v*dd (0) curve at typical corner.

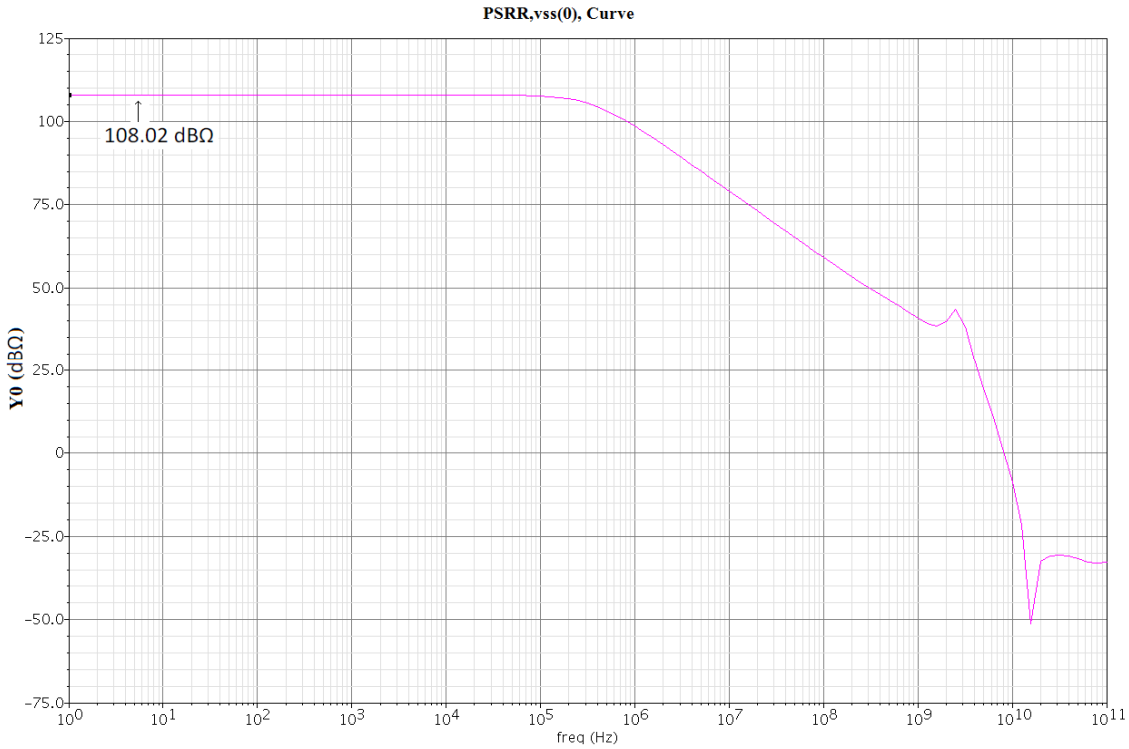


Figure 4.17 Post-layout PSRR,*v*ss (0) curve at typical corner.

High PSRR ensures that the design is capable to reject power supply noises easily [7,12].

4.1.5 SLEW RATE AND 1% SETTLING TIME

The unity gain buffer shown in the Figure 4.18 is used to measure slew rate and settling time. The response is shown in the Figure 4.19 and 4.20.

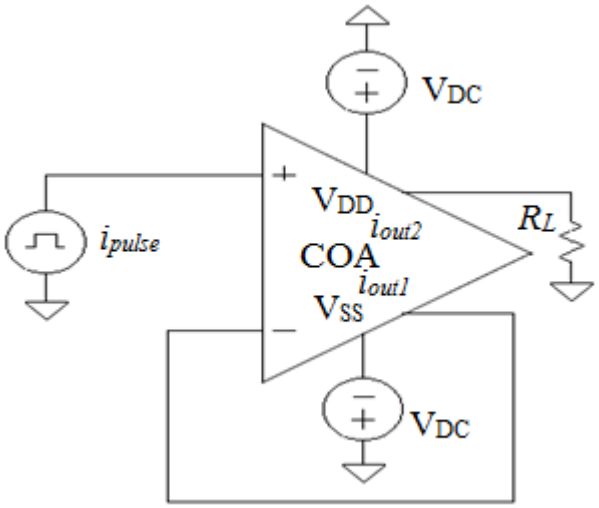


Figure 4.18 Schematic for measuring slew rate and settling time.

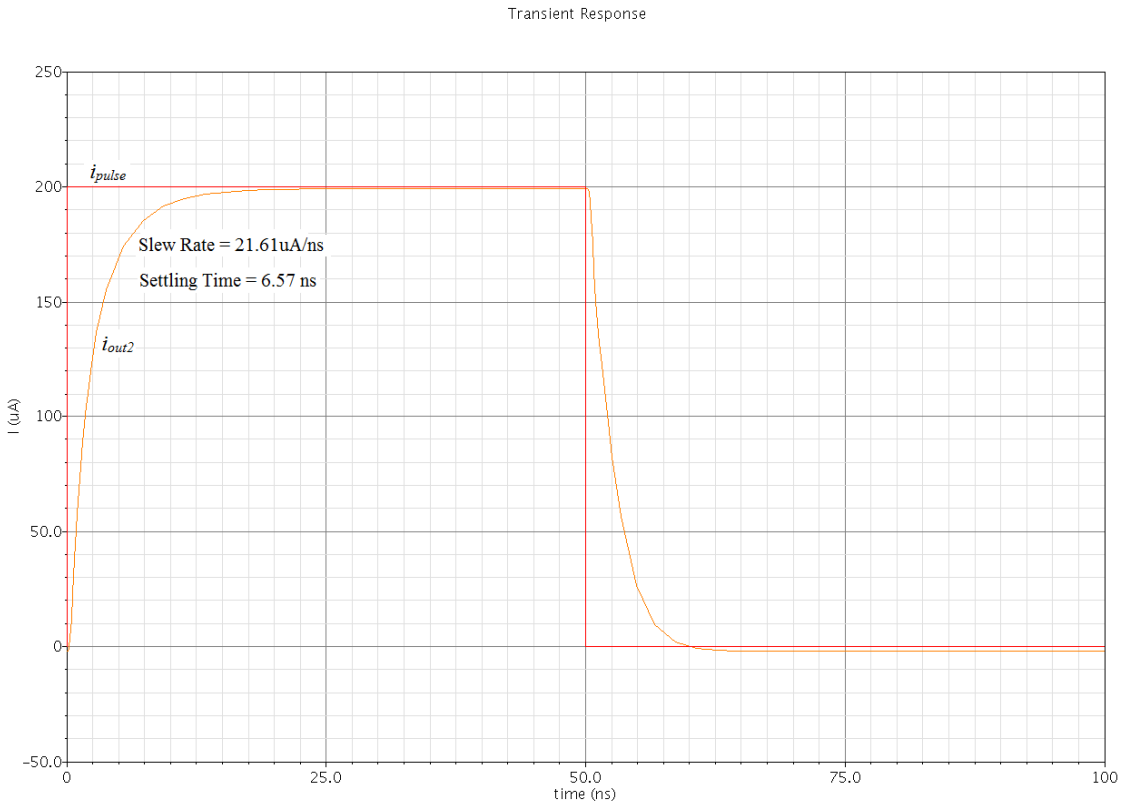


Figure 4.19 Pre-layout slew rate and settling time at typical corner.

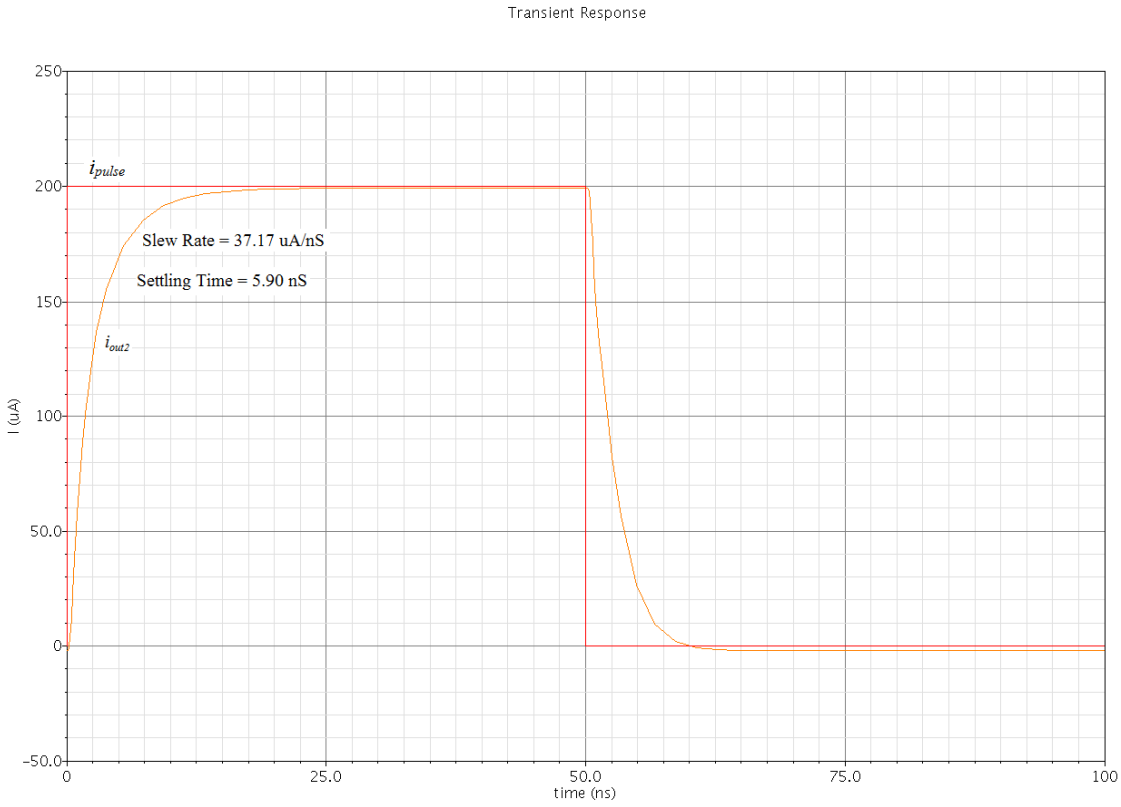


Figure 4.20 Post-layout slew rate and settling time at typical corner.

The values of slew rate and settling time at different process corners of simulations are given in the table below:

Table 4.11 Pre-layout slew rate and settling time at different process corners of simulations

Specifications	Process corners				
	tt	ff	ss	snfp	fnsp
1% Settling Time (ns)	6.57	6.46	7.23	6.89	6.47
Slew Rate (μA/ns)	21.61	22.94	20.95	20.56	22.38

Table 4.12 Post-layout slew rate and settling time at different process corners of simulations

Specification	Process corners				
	tt	ff	ss	snfp	fnsp
1% Settling Time (ns)	5.90	5.56	10.60	6.90	7.92
Slew Rate (μA/ns)	37.17	81.43	40.14	74.64	40.7

The effect of temperature on slew rate and settling time is given in the following table.

Table 4.13 Post-layout slew rate and settling time at different temperatures at typical corner

Specifications	Temperature		
	-20^0	27^0	80^0
1% Settling Time (ns)	5.31	5.90	6.31
Slew Rate (μA/ns)	33.70	37.17	40.47

The result shows that there is improvement in slew rate and settling time as compared to pre-layout values.

4.2. SUMMARY OF RESULTS

The summery of the results have been given below in the tables.

Table 4.14 Pre-layout simulation results at different corners

Specifications	tt	ff	ss	snfp	fnsp
DC Gain (dB)	64.50	61.52	66.54	61.67	66.85
3 dB Frequency (kHz)	216.1	376.4	133.3	312.6	161.6
Unity Gain Frequency (MHz)	343.6	412.1	275.2	354.2	330.6
Compensation Capacitance (pF)	3	3	3	3	3
Phase Margin(degree)	57.43	54.60	60.56	56.44	57.24
CMRR (dB)	57.0	53.01	61.07	54.79	59.86
PSRR, vdd(0) (dBΩ)	113.39	107.17	116.85	110.67	113.85
PSRR, vss(0) (dBΩ)	114.02	108.46	116.95	109.52	116.23
1% Settling Time (ns)	6.57	6.46	7.23	6.89	6.47
Slew Rate (μA/ns)	21.61	22.94	20.95	20.56	22.38
Power Dissipation (mW)	5.70	7.51	4.26	6.12	5.40

Table 4.15 Post-layout simulation results at different corners

Specification	tt	ff	ss	snfp	fnsp
DC Gain (dB)	65.38	63.57	66.46	61.75	68.02
3 dB Frequency (kHz)	220.2	342.2	152.83	338.68	161.6
Unity Gain Frequency (MHz)	353.6	445.81	288.42	361.21	353.97
Compensation Capacitance (pF)	1.5493	1.5493	1.5493	1.5493	1.5493
Phase Margin(degree)	53.60	50.40	56.43	51.99	53.89
CMRR (dB)	73.59	73.83	103.24	76.64	94.51
PSRR,vdd(0) (dBΩ)	109.19	104.93	110.85	106.42	109.58
PSRR,vss(0) (dBΩ)	108.08	102.94	111.17	104.21	109.82
1% Settling Time (ns)	5.90	5.56	10.60	6.90	7.92
Slew Rate (μA/ns)	37.17	81.43	40.14	74.64	40.7
Power Dissipation (mW)	5.72	7.47	4.32	6.16	5.40

Table 4.16 Post-layout simulation results at typical corner: Effect of temperature variation

Specifications	Temperature		
	-20^0	27^0	80^0
DC Gain (dB)	66.79	65.38	61.29
3 dB Frequency (KHz)	168.1	220.2	342.45
Unity Gain Frequency (MHz)	329.6	353.6	338.2
Compensation Capacitance (pF)	1.5493	1.5493	1.5493
Phase Margin(degree)	58.90	53.60	50.78
CMRR (dB)	117.33	73.59	64.97
PSRR, vdd(0) (dBΩ)	107.56	109.19	108.80
PSRR, vss(0) (dBΩ)	111.01	108.02	105.91
1% Settling Time (nS)	5.31	5.90	6.31
Slew Rate (μA/nS)	33.70	37.17	40.47
Power Dissipation (mW)	5.10	5.72	6.38

CHAPTER

5 CONCLUSIONS AND FUTURE SCOPE OF THE WORK

5.1 CONCLUSIONS

In this thesis, a high-gain current-mode operational amplifier with differential input and differential output was designed and analyzed. The design provides a gain of 65.38 dB with a common mode rejection ratio of 73.59 dB. The high open-loop current gain ensures that accurate closed-loop current gain values insensitive to process, supply and temperature can be obtained by employing negative feedback around the current operational amplifier. Slew rate and settling time are 37.17 μA/ns and 5.90 ns respectively. High value of slew rate and low value of settling time show that the speed of the amplifier is quite good at nominal process. Phase margin is equal to 53.60^0. The 3 dB frequency and unity gain frequency are 220.20 kHz and 353.60 MHz respectively and hence the design can be used for a wide range of frequency. The power supply rejection ratios PSRR,*vdd*(0) and PSRR,*vss*(0) are 109.19 dB Ω and 108.02 dB Ω respectively indicating that the design is capable to reject power supply noises easily. The main feature of the design is its very high gain at the cost of reduced 3 dB frequency.

5.2 FUTURE SCOPE OF THE WORK

This section summarizes few potential future directions to further improve the work.

(a) INPUT OFFSET BIAS CURRENT IMPROVEMENT: The input offset bias current errors and the common mode rejection ratio are strongly dependent on the matching accuracy of the current mirrors. This random offset can be minimized by matching the current mirrors by careful layout techniques like common centroid and unit cell layout techniques.

(b) STATIC POWER DISSIPATION IMPROVEMENT: One of the drawbacks of current-mirror amplifiers is their high static power consumption, arising mainly from the large biasing current of the output branch. This can be minimized by using the method of current branching as discussed in section 2.3.5.

(c) BANDWIDTH IMPROVEMENT: The design has a bandwidth greater than 200 kHz. The bandwidth can be further improved using the bandwidth enhancement techniques as discussed in section 2.3.6. These techniques are resistor series peaking, inductor series peaking and current feedback. One may also use their combinations too.

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APPENDIX A

SPICE BSIM3v3 VERSION 3.2 MOS MODEL PARAMETERS

The typical parameters are listed below:

DIODES & NMOSFET SPICE PARAMETERS

```
model bsim_diode_area diode
cj0=0.00103*(1+dcj_n_18_rf )        vj=0.813        m=0.443
is=1e-06                            n=1

model bsim_diode_perim diode
cj0=1.34e-10*(1+dcjsw_n_18_rf )     vj=0.88         m=0.33
is=7e-11                            n=1

model bsim_diode_swg diode
cj0=5e-10 *(1+ dcjgate_n_18_rf)     vj=0.88         m=0.33
is=7e-11            n=1

model bsim_mos_transistor_mos bsim3v3 type=n
version=3.2                         binunit=1       mobmod=1
capmod=2                            nqsmod=0        noimod=2
tox=4.2e-09 + dtox_n_18_rf          toxm=4.2e-09    xj=1.6e-07
nch=3.745e+17                       rsh=8           ngate=1e+23
vth0=0.3075 + dvth0_n_18_rf         k1=0.4578       k2=-0.02638
k3=-10.88                           k3b=0.2379      w0=-8.813e-
08
nlx=4.279e-07                       dvt0=0.4042     dvt1=0.3237
dvt2=-0.8602                        dvt0w=0.383     dvt1w=6e+05
dvt2w=-0.025                        lint=1.587e-08  wint=1.022e-
08
dwg=-3.396e-09                      dwb=1.346e-09   u0=332.1
du0_n_18_rf
ua=-1.17e-09                        ub=2.407e-18    uc=4.355e-11
vsat=8.1e+04                        a0=1.93         ags=0.5072
b0=1.486e-06                        b1=9.064e-06    keta=0.01752
a1=0                                a2=1            voff=-0.1208
nfactor=1.038                       cit=-0.001511   cdsc=0.002175
cdscd=0                             cdscb=0.0008241 eta0=0.005504
etab=-0.001459                      dsub=0.001592   pclm=0.741
pdiblc1=0.005061                    pdiblc2=0.006001 pdiblcb=0
drout=0.001592                      pscbe1=4.866e+08 pscbe2=3e-08
pvag=-0.2958                        rdsw=9.905      prwg=1.1
prwb=0                              wr=p_wr         alpha0=0
```

alpha1=0 beta0=30 xpart=1
cgso=1.55e-10 *(1+dcgso_n_18_rf) cgdo=1.55e-10 *(1+dcgdo_n_18_rf)
cgbo=0
cgsl=3e-11*(1+dcgsl_n_18_rf) cgdl=3e-11 *(1+dcgdl_n_18_rf)
ckappa=0.6
cf=2.33e-11 *(1+dcf_n_18_rf) clc=1e-07 cle=0.6
dlc=4e-08 dwc=0 vfbcv=-1
noff=1 voffcv=0 acde=1
moin=15 noia=1.31826e+19
noib=1.44544e+05
noic=-1.24516e-12 em=4.1e+07 af=1
ef=0.92 kf=0 lmin=1.8e-07
lmax=1.805e-07 wmin=5e-06 wmax=1.05e-04
xl=-1.05e-08 + dxl_n_18_rf xw=0 + dxw_n_18_rf js=1e-06
jsw=7e-11 cj=0.00103 *(1+dcj_n_18_rf) mj=0.443
pb=0.813 cjsw=1.34e-10 *(1+dcjsw_n_18_rf) mjsw=0.33
tnom=25 ute=-1.286 kt1=-0.2255
kt1l=-4.175e-09 kt2=-0.02527 ua1=2.153e-09
ub1=-2.673e-18 uc1=-3.832e-11 at=1.449e+04
prt=-46.18 xti=3 wl=0
wln=1 ww=7.262e-16 wwn=1
wwl=0 ll=-1.062e-15 lln=1
lw=2.996e-15 lwn=1 lwl=0
llc=-6.64e-15 lwc=0 lwlc=0
wlc=0 wwc=0 wwlc=0
lvth0=-0.0001 + dlvth0_n_18_rf wvth0=0.06027 + dwvth0_n_18_rf pvth0=0
dpvth0_n_18_rf
lnlx=-2.854e-08 wnlx=0 pnlx=0
lnfactor=0.032 wua=-1.88e-11 wu0=0.54
pub=3.8e-20 pw0=1.3e-09 lua=1.5e-11
lub=9.76e-20 wrdsw=0 weta0=0
wetab=0 leta0=0.001574 letab=0
peta0=0 petab=0 wpclm=0
wvoff=-0.0004078 lvoff=-0.004208 pvoff=-0.0003788
wa0=-0.04731 la0=-0.4667 pa0=-0.02649
wags=0.004242 lags=0.3028 pags=0
wketa=0 lketa=-0.01942 pketa=0
wute=0.06373 lute=0 pute=0
wvsat=5066 lvsat=0 pvsat=0
dpvsat_n_18_rf
lpdiblc2=-0.004752 wat=7067 wprt=0
ldif=8e-08 hdif=2.6e-07 n=1
pbsw=0.88 cjswg=5e-10 *(1+dcjgate_n_18_rf) ctp=0.000914
ptp=0.000924 cta=0.000919 pta=0.00158
elm=5 tlevc=1

DIODES & PMOSFET SPICE PARAMETERS

```
model bsim_diode_area diode
cj0=0.00114 *(1+ dcj_p_18_rf)          vj=0.762          m=0.395
is=3e-06                               n=1

model bsim_diode_perim diode
cj0=1.74e-10 *(1+ dcjsw_p_18_rf)       vj=0.665          m=0.324
is=4.12e-11                    n=1

model bsim_diode_swg diode
cj0=4.2e-10 *(1+ dcjgate_p_18_rf)      vj=0.665          m=0.324
is=4.12e-11                    n=1

model bsim_mos_transistor_mos bsim3v3 type=p
mobmod=3                               version=3.2       capmod=2
binunit=1                              nqsmod=0          noimod=2
tox=4.2e-09 + dtox_p_18_rf             toxm=4.2e-09      xj=1e-07
nch=6.131e+17                          ngate=1e+23       vth0=-0.4325
dvth0_p_18_rf
k1=0.5704                              k2=0.006973       k3=-2.833
k3b=1.326                              w0=-1.943e-07     nlx=2.56e-07
dvt0=0.4885                            dvt1=0.09578      dvt2=0.1287
dvt0w=-0.1261                          dvt1w=2.479e+04   dvt2w=0.6915
lint=-1.041e-08                        wint=-1.525e-07   dwg=-1.151e-
07
dwb=-1.039e-07                         u0=90+du0_p_18_rf ua=1.49e-09
ub=4.646e-19                           uc=-0.09587       vsat=4.75e+04
a0=1.35                                ags=0.3818        b0=-3.088e-07
b1=0                                   keta=0.01044      a1=0
a2=1                                   voff=-0.1073      nfactor=0.984
cit=-0.001067                          cdsc=0.0007578    cdscd=0
cdscb=0.0001                           eta0=1.071        etab=-0.9291
dsub=1.919                             pclm=0.553        pdiblc1=0.007
pdiblc2=0.008005                       pdiblcb=0         drout=0.157
pscbe1=4.866e+08                       pscbe2=2.8e-07    pvag=-0.888
rdsw=202.1                             prwg=1.2          prwb=0
wr=p_wr                                alpha0=0          alpha1=0
beta0=30          cgdo=1.254e-10 *(1+dcgdo_p_18_rf )     cgbo=0
cgso=1.254e-10 *(1+dcgso_p_18_rf )     xpart=0     cf=1.533e-
10*(1+dcf_p_18_rf )
dlc=7.01e-08          cgsl=2e-11*(1+dcgsl_p_18_rf )      cgdl=2e-
11*(1+dcgdl_p_18_rf )
ckappa=0.6                             clc=1e-07         cle=0.6
dwc=2.3e-07                            vfbcv=-1          noff=1
voffcv=0                               acde=1            moin=15
noia=3.57456993317604e+18              noib=2.5e+03      noic=2.6126e-
11
em=4.1e+07                             af=1              ef=1.1388
```

kf=0 lmin=1.8e-07 lmax=1.805e-07
wmin=5e-06 wmax=1.05e-04 xl=-2e-09 dxl_p_18_rf
xw=0 + dxw_p_18_rf js=3e-06 jsw=4.12e-11
cj=0.00114*(1+dcj_p_18_rf) mj=0.395 pb=0.762
cjsw=1.74e-10 *(1+dcjsw_p_18_rf) mjsw=0.324 tnom=25
ute=-0.4484 kt1=-0.2194 kt1l=-8.204e-09
kt2=-0.009487 ua1=4.571e-09 ub1=-6.026e-18
uc1=-0.0985 at=1.203e+04 prt=0
xti=3 ww=1.236e-14 lw=-2.873e-16
ll=6.635e-15 wl=0 wln=1
wwn=1 wwl=0 lln=1
lwn=1 lwl=0 llc=-1.31e-14
lwc=0 lwlc=0 wlc=0
wwc=0 wwlc=0 lvth0=0.0057 dlvth0_p_18_rf
wvth0=-0.0148 + dwvth0_p_18_rf lu0=-3 lnfactor=0.03
pvth0=0.0031+ dpvth0_p_18_rf lnlx=-1.584e-08 wrdsw=10.07
weta0=0 wetab=0 wpclm=0
wua=2.7e-09 lua=-2.37e-10 pua=5.855e-11
wub=0 lub=0 pub=0
wuc=0 luc=0 puc=0
wvoff=-0.009816 lvoff=-0.0009871 pvoff=-9.833e-05
wa0=-0.04807 la0=-0.281 pa0=0.08661
wags=-0.04177 lags=0.04454 pags=-0.04076
wketa=0 lketa=-0.012 pketa=0
wute=-0.2682 lute=0 pute=0
wvsat=-1.42e+04 lvsat=0 pvsat=-350 dpvsat_p_18_rf
lpdiblc2=0.003012 wat=-6405 wprt=216.6
n=1 pbsw=0.665 cta=0.001
ctp=0.000753 pta=0.00155 ptp=0.00124
ldif=8e-08 rsh=8 rd=0
rsc=0 rdc=0 hdif=2.6e-07
rs=0

The variations in the values of the parameters for different corners are given below:

NOTE: In **CADENCE** following notations are used for corners:

tt	: typical NMOS and typical PMOS
ff	: fast NMOS and fast PMOS
ss	: slow NMOS and slow PMOS
fnsp	: fast NMOS and slow PMOS
snfp	: slow NMOS and fast PMOS

SECTION tt

dcd_n_18_rf=0
dcgs_n_18_rf=0
drgate_n_18_rf=0
dtox_n_18_rf=0.0000e+00
dxl_n_18_rf=0.0000e+00
dxw_n_18_rf=0.0000e+00
dvth0_n_18_rf=0.0000e+00
du0_n_18_rf=0.0000e+00
dlvth0_n_18_rf=0.0000e+00
dwvth0_n_18_rf=0.0000e+00
dwu0_n_18_rf=0.0000e+00
dpvth0_n_18_rf=0.0000e+00
dpvsat_n_18_rf=0.0000e+00
dcf_n_18_rf=0.0000e+00
dcgdo_n_18_rf=0.0000e+00
dcgdl_n_18_rf=0.0000e+00
dcgso_n_18_rf=0.0000e+00
dcgsl_n_18_rf=0.0000e+00
dcj_n_18_rf=0.0000e+00
dcjsw_n_18_rf=0.0000e+00
dcjgate_n_18_rf=0.0000e+00
dcd_p_18_rf=0
dcgs_p_18_rf=0
drgate_p_18_rf=0
dcgdl_p_18_rf=0.0000e+00
dcgsl_p_18_rf=0.0000e+00
dcf_p_18_rf=0.0000e+00
dtox_p_18_rf=0.0000e+00
du0_p_18_rf=0.0000e+00
dxl_p_18_rf=0.0000e+00
dxw_p_18_rf=0.0000e+00
dvth0_p_18_rf=0.0000e+00
dlvth0_p_18_rf=0.0000e+00
dwvth0_p_18_rf=0.0000e+00
dpvth0_p_18_rf=0.0000e+00
dpvsat_p_18_rf=0.0000e+00
dcgdo_p_18_rf=0.0000e+00
dcgso_p_18_rf=0.0000e+00
dcj_p_18_rf=0.0000e+00
dcjsw_p_18_rf=0.0000e+00
dcjgate_p_18_rf=0.0000e+00

SECTION ss

dcd_n_18_rf=0.1
dcgs_n_18_rf=0.15
drgate_n_18_rf=0.35
dtox_n_18_rf=1.0000e-10
dxl_n_18_rf=2.2000e-08
dxw_n_18_rf=-2.0000e-08
dvth0_n_18_rf=1.4500e-02
du0_n_18_rf=-1.0000e+01
dlvth0_n_18_rf=1.4000e-03
dwvth0_n_18_rf=1.1000e-02
dwu0_n_18_rf=-4.5000e+00
dpvth0_n_18_rf=-1.0000e-03
dpvsat_n_18_rf=1.4000e+02
dcgdo_n_18_rf=-0.1
dcgso_n_18_rf=-0.1
dcgdl_n_18_rf=-0.1
dcgsl_n_18_rf=-0.1
dcf_n_18_rf=0.15
dcj_n_18_rf=0.1
dcjsw_n_18_rf=0.1
dcjgate_n_18_rf=0.1
dcd_p_18_rf=0.1
dcgs_p_18_rf=0.15
drgate_p_18_rf=0.35
dcgdl_p_18_rf=-0.1
dcgsl_p_18_rf=-0.1
dcf_p_18_rf=0.15
dtox_p_18_rf=1.0000e-10
du0_p_18_rf=-0.0e+00
dxl_p_18_rf=1.0000e-08
dxw_p_18_rf=-2.0000e-08
dvth0_p_18_rf=-1.4000e-02
dlvth0_p_18_rf=0.0000e-00
dwvth0_p_18_rf=-1.0000e-02
dpvth0_p_18_rf=3.0000e-04
dpvsat_p_18_rf=4.6000e+01
dcgdo_p_18_rf=-0.1
dcgso_p_18_rf=-0.1
dcj_p_18_rf=0.1
dcjsw_p_18_rf=0.1
dcjgate_p_18_rf=0.1

SECTION ff

dcd_n_18_rf=-0.1
dcgs_n_18_rf=-0.15
drgate_n_18_rf=-0.35
dtox_n_18_rf=-1.0000e-10
dxl_n_18_rf=-1.3600e-08
dxw_n_18_rf=2.0000e-08
dvth0_n_18_rf=-1.4500e-02
du0_n_18_rf=1.0000e+01
dlvth0_n_18_rf=-7.0000e-04
dwvth0_n_18_rf=-1.0100e-02
dwu0_n_18_rf=2.0000e+00
dpvth0_n_18_rf=6.5000e-04
dpvsat_n_18_rf=-8.0000e+01
dcgdo_n_18_rf=0.1
dcgso_n_18_rf=0.1
dcgdl_n_18_rf=0.1
dcgsl_n_18_rf=0.1
dcf_n_18_rf=-0.15
dcj_n_18_rf=-0.1
dcjsw_n_18_rf=-0.1
dcjgate_n_18_rf=-0.1
dcd_p_18_rf=-0.1
dcgs_p_18_rf=-0.15
drgate_p_18_rf=-0.35
dcgdl_p_18_rf=0.1
dcgsl_p_18_rf=0.1
dcf_p_18_rf=-0.15
dtox_p_18_rf=-1.0000e-10
du0_p_18_rf=0
dxl_p_18_rf=-8.0000e-09
dxw_p_18_rf=1.5000e-08
dvth0_p_18_rf=1.8000e-02
dlvth0_p_18_rf=-1.0000e-03
dwvth0_p_18_rf=8.5000e-03
dpvth0_p_18_rf=1.0000e-05
dpvsat_p_18_rf=-2.1000e+01
dcgdo_p_18_rf=0.1
dcgso_p_18_rf=0.1
dcj_p_18_rf=-0.1
dcjsw_p_18_rf=-0.1
dcjgate_p_18_rf=-0.1

SECTION snfp

dcd_n_18_rf=0.05
dcgs_n_18_rf=0.075
drgate_n_18_rf=0.175
dtox_n_18_rf=0.0000e+00
dxl_n_18_rf=1.1000e-08
dxw_n_18_rf=-1.0000e-08
dvth0_n_18_rf=1.3000e-02
du0_n_18_rf=-5.0000e+00
dlvth0_n_18_rf=1.1000e-03
dwvth0_n_18_rf=4.7000e-03
dwu0_n_18_rf=-2.0000e+00
dpvth0_n_18_rf=-5.5000e-04
dpvsat_n_18_rf=6.0000e+01
dcgdo_n_18_rf=0.0000e+00
dcgso_n_18_rf=0.0000e+00
dcgdl_n_18_rf=0.0000e+00
dcgsl_n_18_rf=0.0000e+00
dcf_n_18_rf=0.075
dcj_n_18_rf=0.05
dcjsw_n_18_rf=0.05
dcjgate_n_18_rf=0.05
dcd_p_18_rf=-0.05
dcgs_p_18_rf=-0.075
drgate_p_18_rf=-0.175
dcgdl_p_18_rf=0
dcgsl_p_18_rf=0
dcf_p_18_rf=-0.075
dtox_p_18_rf=0.0000e+00
du0_p_18_rf=0
dxl_p_18_rf=-4.0000e-09
dxw_p_18_rf=1.0000e-08
dvth0_p_18_rf=1.7000e-02
dlvth0_p_18_rf=-3.0000e-04
dwvth0_p_18_rf=3.5000e-03
dpvth0_p_18_rf=9.0000e-05
dpvsat_p_18_rf=-3.0000e+01
dcgdo_p_18_rf=0.0000e+00
dcgso_p_18_rf=0.0000e+00
dcj_p_18_rf=-0.05
dcjsw_p_18_rf=-0.05
dcjgate_p_18_rf=-0.05

SECTION fnsp

dcd_n_18_rf=-0.05
dcgs_n_18_rf=-0.075
drgate_n_18_rf=-0.175
dtox_n_18_rf=0.0000e+00
dxl_n_18_rf=-9.5000e-09
dxw_n_18_rf=1.0000e-08
du0_n_18_rf=6.0000e+00
dvth0_n_18_rf=-1.2300e-02
dlvth0_n_18_rf=-7.0000e-04
dwvth0_n_18_rf=-4.6000e-03
dwu0_n_18_rf=1.7000e+00
dpvth0_n_18_rf=4.1000e-04
dpvsat_n_18_rf=-7.0000e+01
dcgdo_n_18_rf=0.0000e+00
dcgso_n_18_rf=0.0000e+00
dcgdl_n_18_rf=0.0000e+00
dcgsl_n_18_rf=0.0000e+00
dcf_n_18_rf=-0.075
dcj_n_18_rf=-0.05
dcjsw_n_18_rf=-0.05
dcjgate_n_18_rf=-0.05
dcd_p_18_rf=0.05
dcgs_p_18_rf=0.075
drgate_p_18_rf=0.175
dcgdl_p_18_rf=0
dcgsl_p_18_rf=0
dcf_p_18_rf=0.075
dtox_p_18_rf=0.0000e+00
dxl_p_18_rf=4.5000e-09
dxw_p_18_rf=-1.0000e-08
dvth0_p_18_rf=-1.3000e-02
du0_p_18_rf=0
dlvth0_p_18_rf=-3.0000e-04
dwvth0_p_18_rf=-5.0000e-03
dpvth0_p_18_rf=1.3000e-04
dpvsat_p_18_rf=3.4000e+01
dcgdo_p_18_rf=0.0000e+00
dcgso_p_18_rf=0.0000e+00
dcj_p_18_rf=0.05
dcjsw_p_18_rf=0.05
dcjgate_p_18_rf=0.05