DESIGN OF LOW POWER, WIDE LINEARITY RANGE DIFFERENTIAL RING VCO WITH POWER DOWN TECHNIQUE

A Thesis Submitted in Partial Fulfillment of the Requirements for the Award of the Degree of

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In VLSI Design

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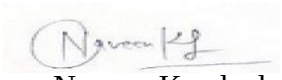
JULY, 2019

DECLARATION

I, **Naveen Kandpal** hereby declare that the work presented in this thesis entitled "**Design of low power, wide linearity range differential ring VCO with power down technique**" in partial fulfillment of the requirement for the award of degree of **Master of Technology (VLSI Design)** submitted at **ECED ,** Thapar Institute of Engineering & Technology (Deemed to be University), Patiala is an authentic record of work carried out under supervision of **Dr. Anil Singh (Assistant Professor, ECED, Thapar institute of Engineering and Technology)** from **2017 to 2019**. The matter presented in this has not been submitted either in part or full to any other university or institute for the award of any other degree.

Date: 08/08/2019



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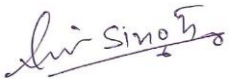

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ABSTRACT

Many electronic circuits and systems such as microprocessors and cognitive radios use a PLL to generate the accurate clock. VCOs are the critical blocks in Phased Locked Loops (PLLs) and various VCO based ADCs as it impact the performance and consumes the most of their power budget. In the field of circuit and system designing, a suitable clock generation circuit plays an important role. For this purpose, VCOs are basic blocks as they consume most of the power consumed by the system itself. Hence the low power and low area VCOs has been always in demand for the researchers. To get the reliable performance of a ADC/PLL, VCO should be robust across the Corners. And in a VCO, achieving the wide tuning range is key concern according to different applications.

This research work explains the low power and wide tuning range differential VCO with an in built power down technique in it. The new architecture is proposed in this work consists of voltage to current converter and NAND based ring oscillators. Also, a PVT compensation circuit is added to achieve better linearity across the different PVT corners. The proposed circuits mentioned above are simulated in Cadence Virtuoso Analog Design Environment in SCL 180 nm CMOS technology with a supply voltage of 1.8V. It has a linearity range from 0.9 V to 1.8 V and tuning range from 40 MHz to 650 MHz .The measured power consumption for this work is 50.4 nw/208.8 μW when power down switch is ON/OFF. The measured phase noise of this architecture is -130.1dBc/Hz at 1MHz offset frequency.

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CHAPTER 1
INTRODUCTION

1.1 BACKGROUND

Many electronic circuits and systems use a clock generator circuit such as microprocessors, cognitive radio, VCOs are critical blocks in Phased Locked Loops (PLLs) and VCO based ADCs as it consumes the most of their power budget [1]. The tuning range linearity of VCO is also important according to various fields such as biomedical applications, Cognitive radio and IoT applications. Ring oscillators require less area and provide wide tuning range than LC based oscillators. As there is a need of thick metal layers in back end flow when working with inductor, LC oscillators consume more area. A ring oscillator is also used to give multiple phases at different node outputs and a wide tuning frequency range. Ring oscillators are more compatible with standard digital CMOS processes as compared to other kind of oscillators. VCO plays an important role in analog and mixed signal designs as it is a fundamental block of PLL and VCO based ADCs in a System on Chip (SoC) as well. For large digital designs such as microprocessors, clock is generated by using a PLL. Once the system is in operation for long duration, the ambient or chip temperature may change and this may result in VCO frequency drift which can even cause the PLL to be out of lock. And hence changes in process, voltage, and temperature (PVT) affect the frequency of operation of VCO and PLL. Tuning range, VCO linearity, PVT compensation, and power consumption of VCO have been important topics for researchers [1]. Some other works suggested that the coarse tuning only happens at the start-up of the oscillation to compensate the process variations [2]. While working with phase locked loop, there is a disadvantage of small tuning range of VCO when temperature of chip gradually increases. PLL has a problem of going out of lock with small tuning range. Therefore, it is important to have wide tuning range in VCO. To solve this problem, several compensation techniques have been reported to minimize the effect of temperature on VCO frequency. Local positive feedback in the inverter delay element of VCO leads to a ring oscillator having two stages to oscillate and generate quadrature clocks, which is then used in clock data recovery circuits. For the frequency synthesis or modulation application, VCO can be used in transceiver chain as well [3]. In case of FSK, VCO are useful as they show good performance as far as low drift with temperature and low cost is concerned [4]. A design with supply and temperature insensitivity is required for the switching of oscillation frequency while dealing with switched mode regulators to removing the sub harmonics in spectrum of frequency. Hence the power consumption will be less [5]. But it has not tackled the problem of process variation minimization.

With a rapid growth of mobile application, spectrum allocation is key concern in data communication. To solve the problem of congestion, network traffic, boost speed, spectrum management, spectrum sensing, transmitter detection cognitive radio devices play important role [6]. Also, the range of frequency produced by VCO can be used for cognitive radio. As compared to LC based oscillator, ring

oscillator based VCOs are preferred due to better tuning range and low power consumption. However, power consumption remains a key concern while designing a VCO and researchers have explored the various techniques to minimize the power dissipation. One of the basic oscillator topologies is the LC oscillator. Although this topology dominates ring oscillators in terms of phase noise [7], it is analog in nature and requires area consuming passive elements. The other architecture is ring oscillator.

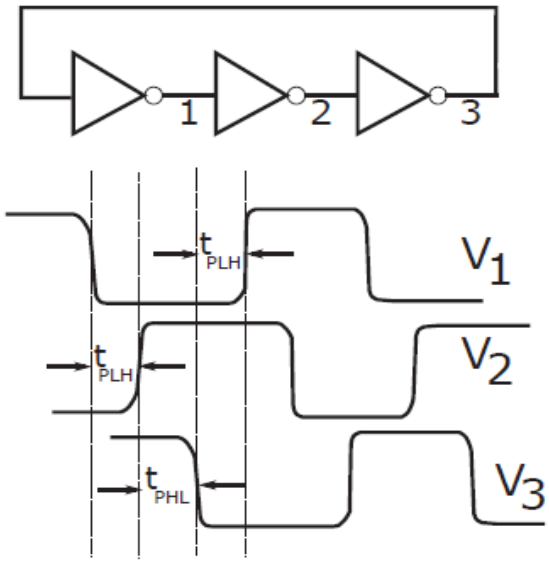

Figure1. 1 Output of three-stage Ring oscillator [7]

The simplest ring oscillator can be formed by an odd number of inverters connected in a closed loop with positive feedback as shown in Figure 1.1 [7]. The delay time is shown between the 50% points of the input and output are labeled tPLH (propagation time from low to high) and tPHL(propagation time from high to low) depending on whether the output logic level is changing from high to low or from low to high. The number of stages n in a ring oscillator is determined by various parameters, including speed requirement of circuit, power consumption, and noise insensitivity, frequency of operation. There must be an odd number of inversions in the loop so that the circuit does not latch up. The waveform of different outputs for the ring oscillator is shown here in Figure 1.1. The performance of high speed digital systems is also directly affected by the phase noise of oscillator. The role of clock signals comes into the picture when accuracy of signal is to be achieved by maximum number of iteration, maximum clock rate [8]. As similar to all other kind of analog circuits, the oscillator is also impacted by noise [9]. This is caused due to phase shifting and interference due to supply sources. These noise sources badly impact the performance of the VCO. The effect of amplitude limitation mechanisms in practical

oscillators is neglected. And the dominant noise is the phase noise, which must be minimized for better performance [9]

1.1.1 DIFFERENTIAL RING OSCILLATOR

In simple ring oscillators odd number of inverters is used. In case of differential ring oscillator even number of inverters are utilized as shown in Figure 1.2. Differential structures are used to give better performances as far as rejection of supply and substrate noise is concerned.

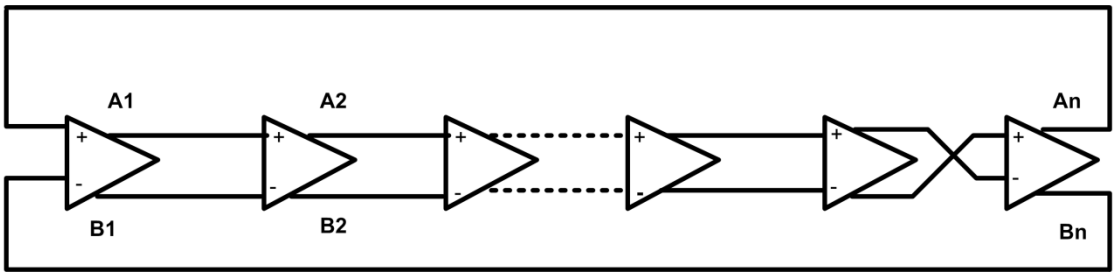

Figure 1.2 N stage differential ring oscillator

The value of time period of any ring oscillator is determined by the product of the total number of stages used and the delay of individual inverter. The optimization of the delay can be done either by adjusting the capacitance or the current.

1.1.2 INTRODUCTION TO VOLTAGE CONTROOLED OSCILLATOR

This is a block used in various analog or mixed signal designs that converts input voltage to output frequency. The basic idea of VCO can be represented as shown in Figure 1.2. And the ideal relationship between output and input is drawn graphically in Figure 1.3. After applying the control voltage, the frequency of oscillation either increases or decreases.

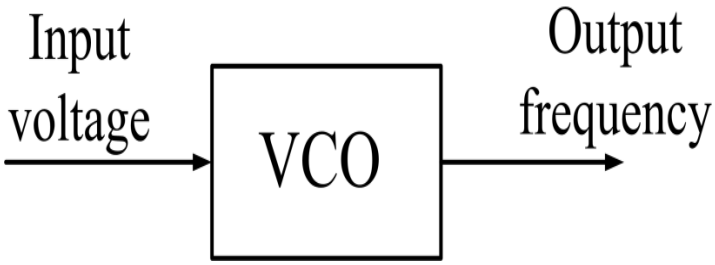

Figure 1. 3 Basic block diagram of voltage controlled oscillator

The gain of the VCO is expressed as $K_{VCO} = \frac{f_2 - f_1}{V_2 - V_1}$ where voltage controls the output frequency. This gain is also called the sensitivity of the VCO. Some useful parameters of VCO can be written as follows.

1.) Center frequency
2.) Tuning range
3.) Linearity range
4.) Power dissipation
5.) Noise immunity

The detailed explanation of all above parameters is discussed in this chapter. Wherever the concept of wireless transmission, reception of audio/video signals comes into the picture, need of oscillating electronic signals becomes necessary. This need is implemented by VCO in electronic devices. So the applications of oscillating circuits are very wide in nature.

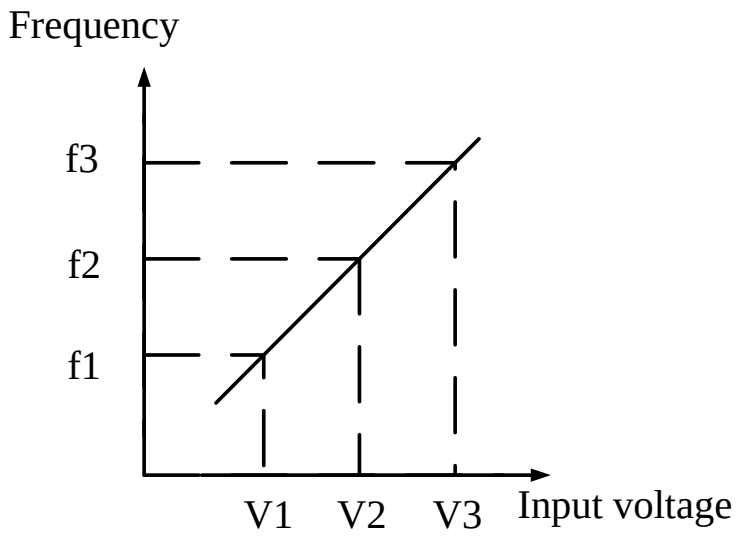

Figure 1. 4 Input output relationship of VCO

- **Centre frequency**

  The mid value shown in Figure 1.3 is considered as center frequency. The value of it totally depends on the application used. These days VCOs used can achieve center frequency upto 10GHz [10].

- **Tuning range**

  For any application, there is a desired range of frequency is needed. That range of frequencies which shows the variation of center frequency is called tuning range. In the Figure 1.3 it is shown as the range between f3 and f1.

- **Linearity range**

  When the VCO is used for phase locked loop, the range for which the output input relation is linear is key concern. And the changes occur in gain of VCO should be minimized. Real

oscillators have very high gain the middle range of curve and lower gain at other corners of the curve. The difference between linearity and non-linearity of the curve of VCO can be shown in figure 1.4.

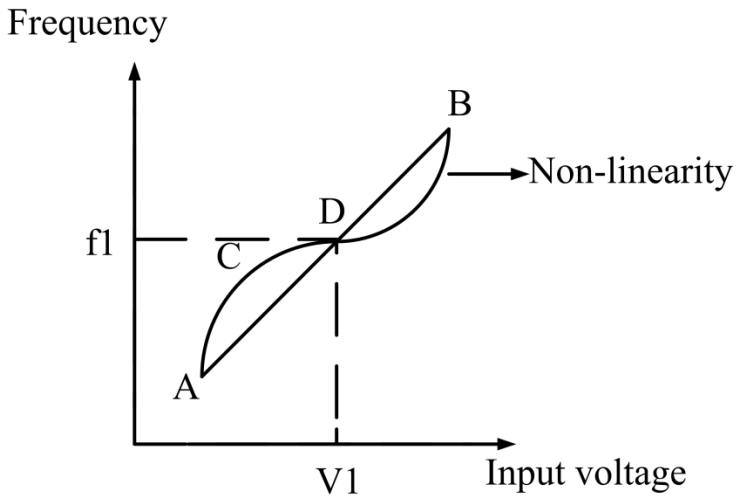

Figure 1. 5 Nonlinearity of VCO

- **Power dissipation**

  When a system has millions of transistors, it is very important to minimize the power dissipation. Oscillators also consume huge power. When VCOs are used in PLL or ADC, it is highly desirable to achieve a low power VCO to make it sure that ADCs are giving better performance in terms of power consumption. So to control power issue, lot of research have been done .This report also focuses on the power down technique.

- **Noise immunity**

  Voltage controlled oscillator are very sensitive to noise caused by supply if oscillators are not differential in nature. It is not that easy to make an oscillator noise free. Noise may worsen the output phase as well.

1.1.3MATHEMATICAL MODELLING OF VCO

When the representation of VCO output with respect to the time comes into the picture, the mathematical modeling is necessary to describe its performance of oscillator. It is the generalized fact that frequency will be higher if the phase is more. Graphical representation of it is shown in figure 1.5 as frequency is defined as $\omega = \frac{d\Phi}{dt}$. After explaining the relation between phase and frequency one can easily write the equation of VCO in terms of frequency. The equation 1 shows the VCO characteristics

$$\omega_{out} = \omega_0 + K_{VCO}V_{control} \quad (1)$$

Where input voltage to VCO is control voltage and K_{VCO} is the gain of VCO

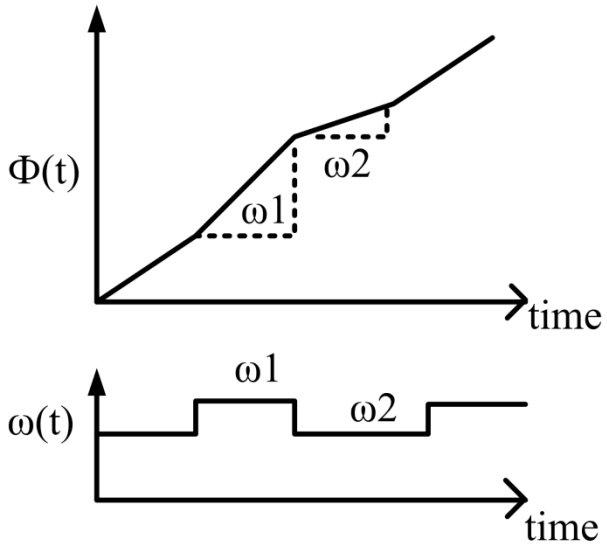

Figure 1.6 Relation between phase and frequency

And if there is variation in the input voltage of VCO, it may lead to produce harmonic components at the output that are not desirable when VCO works in non-linear region.

1.1.4 CONVENTIOANAL CURRENT STARVED RING VCO

The theory and the working of current starved ring oscillator is somewhere similar to the normal ring oscillator with the current source. There is odd number of stages present in current starved architecture shown below in figure 1.6. And the delay of individual stage is responsible to produce frequency of oscillation either in increasing or decreasing order. So the delay and hence the frequency is completely controlled by the voltage applied at the gate terminal that causes to make changes in current flowing in transistor M0 shown in figure 1.6. The working of this circuit can be explained by the relation between control voltage and current available. The delay can be controlled by the current using the charging and discharging process of load which is capacitive in nature. This current mirror is designed in such a way that it would be able to increase or decrease the resistance of pull up/pull down transistors. Higher the control voltage, the available current will be higher so smaller the resistance. M10, M11, M12, M13 are used as current sources while M1, M2, M3 are used as current sink. Inverters are said to be current starved as current is limited by current sources. Current flowing through M13 and M0 are same.

The problem with this kind of architecture is its periodic time. As voltage swing is not good enough to produce oscillation in shorter period of time. Current flowing through M13 and M0 are same.

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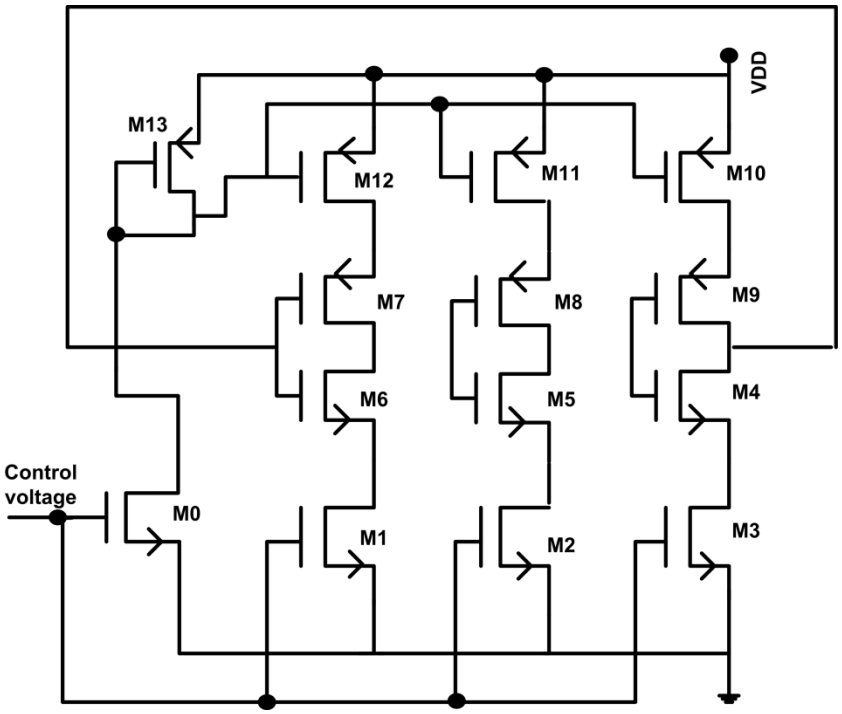

Figure1.7 Conventional current starved Ring VCO

To get the oscillations, odd number of inverters is used to make chain of inverters through M4 to M9 in figure 1.6. The tuning of control voltage is done by using a current mirror. This current mirror is designed in such a way that it would be able to increase or decrease the resistance of pull up/pull down transistors. Higher the control voltage, the available current will be higher so smaller the resistance. M10, M11, M12, M13 are used as current sources while M1, M2, M3 are used as current sink. Inverters are said to be current starved as current is limited by current sources. Current flowing through M13 and M0 are same.

The problem with this kind of architecture is its periodic time. As voltage swing is not good enough to produce oscillation in shorter period of time. Also it suffers from low linearity range, high noise etc. Instead of M0 a current source can also be used to have a much better control over current [11].

A very popular delay cell is shown in figure 1.7, which is called as Park and Kim delay cell [12]. This architecture is widely used due to its capability of having more immunity to noise and good CMRR as compared to that of single ended structures. When we use current source transistors to have tail current, it minimizes the output swing and tuning range of linearity. Hence this is replaced here in Park and Kim cell.

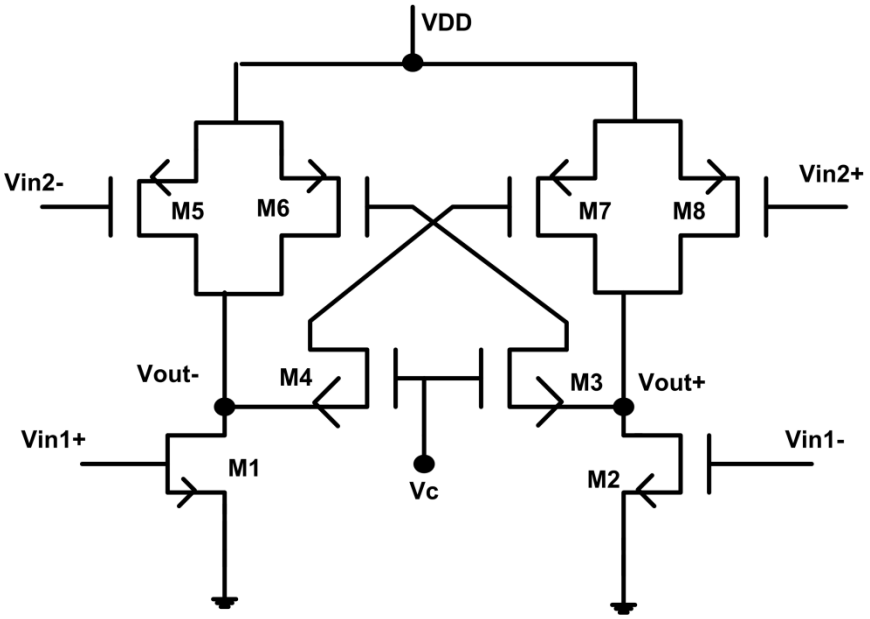

Figure1.8 Differential Park and Kim delay cell [12]

So to reduce power supply noise and common mode rejection ratio, this basic delay cell is widely used in Ring VCOs.

The problem with this Park-Kim VCO is the frequency which is very low. Hence it is not desirable for high frequency application. Whenever we deal with IoT applications, this kind of delay cells are not desired as the range of IoT applications is from 100MHz to 5.8 GHz that cannot produced by the above mentioned Park and Kim cell. There is a contradiction between the value of sizes used in the architecture and time constant. The relation between time constant and sizes of the circuit is difficult. [12] We cannot enhance the value of sizes as it will lead to the larger values of parasitic capacitances. It is hard to achieve the oscillation just by adjusting the sizes of transistor. To get the required range of oscillation frequency, inductor peaking method can be used. But inductors are not used generally due to large area consumed. The cross coupled latch becomes very weak, for high Vc and frequency will be high and vice versa. The concept of cross coupled latch can be modified when it comes to high frequency application. Now the requirement of this is to minimize of the effect of changes in PVT for a given circuit. To understand the effect of these parameters, the threshold effect is drawn here in figure 1.7. The ideal threshold voltage sensor can be used to implement PVT compensated circuit. To sense the threshold variations, PMOS based circuit with very high resistance as shown in figure 1.7 is used.

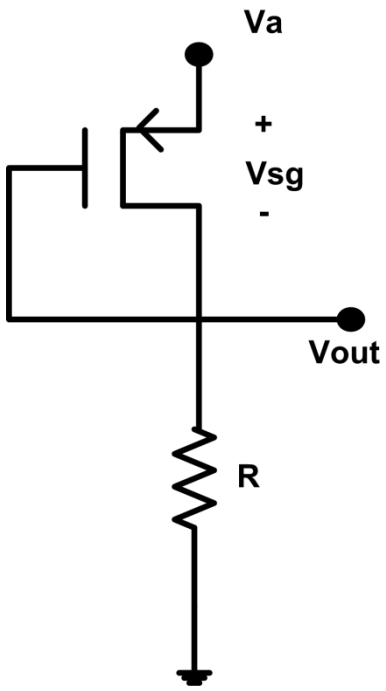

Figure 1.9 Ideal threshold voltage sensor

The current flowing through resistor R is given by V_{out}/R which is equal to the

$$I = K(V_{SG} - |V_T|)^2$$

Whenever process or temperature changes occur in the circuit and system, it changes the performance of the circuit. So compensation technique must be used to minimize the effect of all these variations. Hence by applying the KVL and the relation between R and V_{out} can be written as follows

$$V_{out} = V_a - V_{SG} \quad (2)$$

$$V_{out} = KR(V_{SG} - |V_T|)^2 \quad (3)$$

Now by rearranging the above equation, we get a value of source to gate voltage in terms of threshold voltage output and resistance.

$$V_{SG} = |V_T| + \sqrt{\frac{V_{out}}{RK}} \quad (4)$$

For R >>$1/K$, second term will give a value which is very small and can be neglected.

$$V_{SG} = |V_T|$$

Thus it is clearly shown that the output depends on the supply voltage and threshold voltage. And if the supply voltage is constant then output just senses the threshold voltage. So we can say that by using this kind of circuit we can make it sure that output of the circuit is dependent only on the temperature of it regardless of the value of any other parameter.

$$V_{out} = V_a - |V_T| \quad (5)$$

These kinds of techniques have been to get a circuit which is insensitive to variations of temperature and hence these circuits can be used in best and worst possible environmental conditions. In the above equation V_a is power supply. For a given power supply, the output can be controlled by just the value of threshold value. This approach also used in this work to minimize the temperature variations. And further the circuit used to reduce the voltage and process variations as described in upcoming chapters. To achieve a better linearity in the presence of supply noise, different kinds of PVT invariant methods have been used by the researchers. Some are digital in nature while other use algorithm approaches to minimize it. One of the most widely used algorithms is Least Mean Square method. It can be used using hardware description language. Any analog voltage that is applied to the input of VCO can be affected by some kind of external noise sources. During fabrication, changes in W or L of any given transistor can directly change the mobility and other important physical parameters of device. As far as millions of transistors are concerned it is unavoidable thing for any researcher or designer to neglect this kind of variations. It can be used using hardware description language. So the problem of dependence of output on temperature can be reduced. The problem of variation in supply for any given circuit plays an important role as it directly impacts the performance of the circuit.

1.1.5 DESIGN ISSUES IN VCO

As VCOs are complete analog circuits in nature. The problem of noise and power consumption is of more concern these days. A good wide tuning range and small area are some qualities of ring VCO that makes it superior than other kind of oscillator. As the CMOS technology is reducing, the area and power consumption cannot be compromised. But VCOs described earlier in chapter 1 cannot be used in the applications where high frequency is required such as mobile phone, wireless local area network etc., as they do not give the high frequency range required for these applications. To overcome this problem method of noise suppression can be used [12]. The most widely used method for this purpose is injection locking. A special kind of structure having injection locking concept is used in recent research to obtain rail to rail swing in order to nullify the effect of phase noise and supply. The analysis of a given circuit becomes so tedious when parasitic effects are taken into account. And hence it becomes very difficult to handle circuit while maintaining the best performance.

1.2 LITERATURE SURVEY

1.2.1 DETAILED STUDY OF DIFFERENT ARCHITECTURES OF VCO

In this chapter, the research work that has been done for lower power VCOs, PVT variations, linearity range and power consumption of various architectures of VCO is reported. Various papers have been studied to get an idea about the structures used in basic cell of ring oscillators for VCOs. A brief review based on the study of papers is as follows:

Y.S. Park et al. [1] reported a four stage ring voltage controlled oscillator which is supply insensitive. To enhance the performance of VCO, bias controller circuit and swing controller circuit are used. In this paper, supply sensitivity is reduced by factor of 25 in case of static supply voltage and by factor of 10 in case of dynamic supply voltage. The compensation technique used for increasing the insensitivity is adaptive in nature.

Young-Seok Park et al. [2] implemented a new RVCO to suppress the frequency change due to supply voltage noise and process variation. In this paper voltage regulators are replaced by swing controller and current bias controller, as voltage regulators need large values of capacitances to get the stability in feedback. The oscillation frequency variation is reduced from 63% to 6% between FF and SS corners. The frequency of ring VCO is stabilized by keeping the ratio of bias current and swing voltage constant.

K. R. Lakshmikumar et al. [3] presented a two stage ring oscillator to provide quadrature phase which is widely used in CDR (clock and data recovery) circuits. A biasing technique is used to suppress the variation of process and temperature on the free running frequency of the circuit. The concept of internally generated supply is implemented using constant trans- conductance bias. In this paper 5% variation in the frequency over the range of temperature from -40^0 to 125^0 is reported.

W. Rahajandraibe et al. [4] introduced double frequency control that allows the VCO to keep the constant operation throughout -40^0 to 120^0 temperature. Better frequency insensitivity is obtained by using two methods. One is voltage controlled while other one is current controlled. Temperature compensation is calibrated for frequency synthesizer and FSK modulation in this work. Frequency is reduced from 1300 ppm/°C to 73 ppm/°C with a power consumption of 18 mW.

K.N. Leung [5] reported an approach to power up the ring oscillator by using temperature sloped and magnitude adjustable supply voltage. This work eliminates the need of external low-temperature coefficient capacitors and resistors. In this work a first-order band gap voltage reference and a linear regulator is used. By using resistance ratio, the slope of temperature of reference voltage is adjusted.

After generating positive or negative slope, reference voltage VREF is then scaled by the regulator circuit to achieve supply which is adjustable.

H. M. El Misilmani et al. [6] presented the design and analysis issues of cognitive radio. It also includes the design of amplifiers, antennas, and ring oscillators. In this work, various issues are explained about the front end design of radio frequency cognitive radio. The optimum utilization and sensing, transmission of antennas are key concern in the radio communication these days. Hence CR (cognitive radio) is very useful to steer frequency to any band of interest. To accept any modulation scheme CR plays an important role. This work also reported the noise canceling method in the circuit, and it leads to give more gain. As far as power consumption is concerned, CR receivers give less input return loss. The sensing of a given spectrum in cognitive radio system needs very good linearity to manage signals. And low-noise to detect weak signals in the spectrum simultaneously.

Xuan Zhang et al. [13] presented a low power oscillator with the calibration technique for the compensation of PVT. Calibration circuit is made up of a VCO, a Time to Voltage converter, a comparator, a successive approximation register, a digital-to-analog converter and a state machine. A test controller is used to adjust trimming bits externally by providing calibration of current. A variable resistive divider network plays important role to supply input voltage externally.in this work, the frequency deviation achieved using self-calibration method is around 1.6%. Also, a latch based regenerative comparator is used to save power by ensuring the difference between two inputs of it is used to shut it off. Comparator used in this work makes decision in less than 2 ns.

Sung-Geun Kim et al. [14] introduced a phase locked loop with the help of a feed forward ring VCO which is insensitive to noise of supply. To get a quadrature phase, 4 stages are used in ring VCO. 400-MHz with 0.65-V supply PLL is implemented in 180-nm standard CMOS with the help of supply sensing block. This sensing block generates a voltage whenever a variation is sensed in the supply due to the noise. Also frequency of oscillation is obtained as the function of difference between two body bias voltages of inverters used in the basic cell of ring oscillator. The total power consumption in this work is 242.1 μW.

Mihai A. Margarit et al. [15] presented a VCO for portable wireless communication having the concept of automatic control of amplitude with low noise and low power consumption. The automatic control of amplitude AC is implemented by a rectifier, a LPF, a differential-to-single-ended amplifier. In this work, replica bias circuit is used to find two different voltages over different temperature and process. The measured Phase-noise of this VCO is -106dBc/Hz.

Shuenn-Yuh Lee and Jian-Yu Hsieh [16] proposed a low phase noise VCO by using multiple gated cross coupled negative resistance and bypass capacitor. In this work, the architecture is made in such a way that if the transistors used here are at strong-inversion and sub threshold region, the equal output amplitudes of the 3rd harmonic with different signs in these transistors is obtained and cancelled simultaneously. Also to reduce the higher order non linarites, a bypass capacitor is used. Using 180 nm CMOS technology with 0.9 Volt supply, the power consumption is 2.7 mW and phase noise is -122.3dBc/Hz.

Susan M. Schober and John Choma [17] reported a capacitively coupled ring VCO to get a better ring VCO free from poor jitter and spectral distortion. The advantage of this kind of architecture is that it can be easily extended to multiple phases ring VCO. The phase of this VCO depends on the number of ring stages and rows that are connected by node capacitances. Frequency of oscillation of VCO is inversely proportional to the propagation delay of inverters and capacitances. By simply increasing the number of capacitances, various phase angles can be achieved. This VCO occupies an area of $0.0024mm^2$, and the power consumption is 0.88mW with 1 Volt supply .The phase noise is -124.5dBc/Hz.

In-Chul Hwang et al. [18] introduced a VCO with differential delay cell that is used to adjust its delay through the increasing and decreasing of resistance of a transmission gate. This self-regulatory delay cell has a compensation circuit to make it insensitive from supply noise. Clock generators with large digital circuits need this kind of VCO which is having self-regulation in it. To provide high common mode rejection Source-coupled differential delay cell and inverters are used. To suppress the supply noise, the concept of two feedback loop is presented. One loop compensates the delay variation and second loop regulates the supply by using cross coupled NMOS latch. The internal feedback loop rejects the noise caused by supply.

Guoying Wu et al. [19] described a low voltage ring VCO that is having temperature sensitivity of 34 ppm/°C for the from -40°C to 120°C. To control the frequency, the control voltage is generated by the self-calibration algorithm. This work presented the coarse tuning and temperature compensation with the use of separate control voltages and hence they cover different frequency ranges. The control voltage is generated by a temperature sensor in this architecture. This VCO is designed using 130nm technology and frequency variation difference in between SS and FF is 35%. The variation in voltage for the temperature range from -40°C to 120°C is around 238 mV.

B. Ghafari et al. [20] explained a small-size VCO for the application of Medical Implant Communication Service (MICS) as the frequency range is 352 to 454 MHz which is suitable for MICS band frequency. To get the minimum power consumption, the optimum W/L ratio is selected as 5. To achieve low noise the transistors are biased in such a fashion that they do not conduct continuously.

These transistors can be periodically switched on and off to minimize supply sensitivity. To achieve low power consumption and phase noise, a tail transistor is used to control oscillation frequency, instead of holding latch transistors used in other previous works.

Oh-Yong Jung et al. [21] explained a ring VCO having an additional RC network in the inverter to produce a negative conductance. This method is used to improve the startup time of the oscillation. Architecture is proposed in such a way that it improves current flowing through the drain in the inverter and it produces a waveform, which reduces the RMS value of sensitivity and hence further reduces power consumption. The key concept of achieving oscillation at output of ring oscillator is if poles of transfer function of the oscillator lie in the right half plane. RC network instead of cross coupled transistor plays an important role to minimizing the power dissipation in the circuit. In this work, the phase noise obtained is −94.84 dBc/Hz at 490 MHz oscillation frequency and the power dissipation is 45 μW.

Zied Sakka [22] reported a ring VCO which is temperature and supply insensitive used for impulse radio ultra wide band applications. A temperature correction circuit is proposed in such a way that control voltage depends only on threshold voltage and overdrive voltage. Temperature sensitivity of overdrive voltage as a function of resistor used is employed in this work. And hence the value of temperature coefficient is adjusted to achieve required oscillation of the frequency. In this work, the range of supply voltage and temperature are taken from 1.5V to 2.1V and from 10°C to 70°C.

Ting Wu et al. [23] introduced on chip calibration to make ring VCO supply voltage insensitive. Normally the VCO has positive supply voltage sensitivity for most of its operating frequencies, so the concept of adding a compensation method with negative supply voltage sensitivity can enhance the supply noise insensitivity. Compensation technique in this work is based upon Lee–Kim delay cell. By measuring the polarity of supply and calibration of current, the desired results are obtained. The RMS jitter for this On-chip calibration is 3.95ps at a 1.4GHz frequency for this architecture.

Nadia Gargouri et al. [24] explained a two-stage VCO for the application of impulse-radio ultra-wideband. For the better performance and dimensions of VCO, a graphical approach has been implemented. The range of this VCO is enhanced to 176.6% for the use of ultra wideband range. The measured phase noise for this work is −107.1dBc/Hz. And the power consumption of VCO is 7.41mW by using 1.8V supply. A wide tuning range, low power, and low phase noise is achieved through the proper stabilization method.

M. Shahriar Jahan and Jeremy H. Holleman [25] presented the architecture of an ultra-low-power voltage-controlled oscillator which is used for Medical Implant Communication Service band. The VCO is based on a single ended instead of differential structure of oscillator. The current starved architecture

for controlling of the voltage is implemented. The concept of beta multiplier reference (BMR) which is highly insensitive to noise caused by supply is introduced. It is also digitally controllable to make the VCO usable for the range of 400 MHz to 935MHz. It is also useful for FSK. The power dissipation is around 2 μW with low supply of 1V which is suitable for biomedical applications.

Changzhi Li and Jenshan Lin [26] explained a fully differential ring oscillator having two stages which is used for application for radar sensor and impulse radio as well. In this work, very wide tuning range of 1 to 9 GHz is achieved. To get wider range of tuning a second order of algorithm is used. And hence network of resistors used in this work is programmed through that algorithm. This architecture removes the unnecessary complex structure of resistive network. The current flowing through the basic cell is around 3.7mA and remains same for the entire range of tuning in ring oscillator. As far as power and noise are concerned, this architecture is simpler than other structures.

Tumay Kanar and Gabriel M. Rebeiz [27] introduced a VCO which cancels the harmonic distortion with low power. By simply adding a summer this work is made up for wide band of frequency applications. Wide band signals are generated using built-in self-circuit concept. A differential kind of structure is implemented to cancel the harmonics present in the frequency spectrum.

Wei Li and Kwok-Keung M. Cheng [28] explained a VCO which consists of differential latch and tank circuit to achieve low power results. The concept of insertion of buffers is used in this architecture. And the buffer used is open drain in nature. To tune biasing, adoption of voltage headroom technique is implemented to get the optimum performance. The tuning range is more than 17% for this work. A voltage divider and injection locking further enhances the frequency range of the circuit. The phase noise of this work is -112.6dBc/Hz.

Joo-Myoung Kim et al. [29] reported a ring VCO for low noise. Low noise is achieved by applying the reduction technique at the output terminal of VCO. The analysis the reduction of phase noise, time domain analysis approach is described. The time of conduction is then reduced in a given duration of transition. The basic ring oscillator used here is of four stages, to optimize the effect of noise. Current flowing due to noise is removed by establishing the negative skew technique implemented for deep submicron technology.

Yongsun Lee et al. [30] described spurious and jitter free PLL using a ring VCO. The basic idea of this work is the realignment of the phase. The correction technique is used to suppress the noise by comparing two kind of different structures in this paper. Flicker noise is not analyzed here. And hence noise from the clock used for reference is also not described. In 65nm CMOS technology, this work reported .004mm^2. Power consumed by the entire circuit is 4.12 mW.

Honghui Deng et al. [31] reported six stage ring VCO which is differential in nature. The phase noise of this VCO is analyzed. Using the technology of 350nm with the power supply of 3.3 volt is used with the help of wave shaping technique to get a larger swing at the output. In this work, a comparator is implemented to adjust the DC operating point for the stability point of view. Comparator is designed in such a way that a feedback connection is formed to get better stability. The phase noise of this work is -102dBc/Hz@1MHz.

Bhavana Goyal et al. [32] described a single ended VCO that shows better stability of frequency as compared to differential VCO. By using single gate capacitance higher operating speed is achieved. This work focuses on high frequency analysis. The tail current is not present in this architecture. And hence the higher linear frequency range is achieved. And the area consumed by this circuit is also less than the traditional current starved voltage controlled oscillator.

Jorg Daniels et al. [33] explained a digital calibration technique using look up table to improve the linearity range of voltage to frequency curve of VCO. This work has been designed in 65nm technology. Analog to digital converter is also used here to correct the output of LUT. Two differential VCOs are used in such a manner that they make sixteen basic delay cell kind of structure to get out of phase frequency at the output. The sampling is done in such a way that the range of it is from 50MHz to 400MHz. to sample each pulse at the output, a six bit counter is used with flip flops to maintain the phase at the required cycle of clock. The linearity achieved in this work is for 12 bit.

Maran Ponnambalam and Premanand Chandramani [34] used a biasing and injection circuit to implement a ring VCO that is differential. As far as parasitic capacitances and non- idealities are concerned, output is observed with respect to slew rate. The analysis of phase noise, power consumption and non -linearity is done using injection locking circuit in this work. The starting point of oscillation is .45 volt for control voltage. Differential delay cell used in this work uses the capacitive load of 20fF. The problem of non-linearity is removed by using the parallel architecture of PMOS current sink with the VCO circuit. Multiple frequencies are synthesized using injection locking technique and this is an added advantage. Hence need of PLL in frequency synthesizer is no more necessary in this architecture.

Behzad Saeidi et al. [35] reported a very wide range VCO having an adaption in built technique in it. To find the error between output and input frequency, coarse tuning is used. It is assumed here that the variation in temperature is equal to the range of frequency. Bandwidth achieved in this work is independent of control voltage variation. Variations in temperature are achieved from 350C to 850C. Multi standard trans-receiver method is used to reduce the noise caused by VCO when working for PLL. Uncertainty of resolution is neglected in the analysis of this work. But the tolerance for temperature and supply noise is drastically reduced as compared to other structures. The problem of non-linearity in

frequency with respect to control voltage is improvised to some extent. But the power consumption is not in that range which is suitable for high frequency application. The concept of adaption of temperature is used here to get a wide range of 45MHz to 3.90GHz.

Bai Xi et al. [36] explained a VCO circuit design with the help of comparator, S-R flip Flop and current sources. The load capacitance charging and discharging is compensated using the switch control circuit. When the control voltage exceeds from a certain limit, the comparator changes its state and hence control the output of VCO accordingly. When the increase in control voltage reaches at a certain level, the oscillation at the output becomes stable.

CHAPTER 2
PROPOSED ARCHITECTURE

Power consumption, wide linearity range and low noise are some key concern in any of the circuits used in VLSI industry. Hence the reductions of power and linearity range have been a major topic of interest for the researchers. This chapter focuses on the VCO (Voltage Controlled Oscillator) made up of two five stage fully differential ring oscillators with the power down technique. Figure 2.1 shows the architecture of proposed VCO.

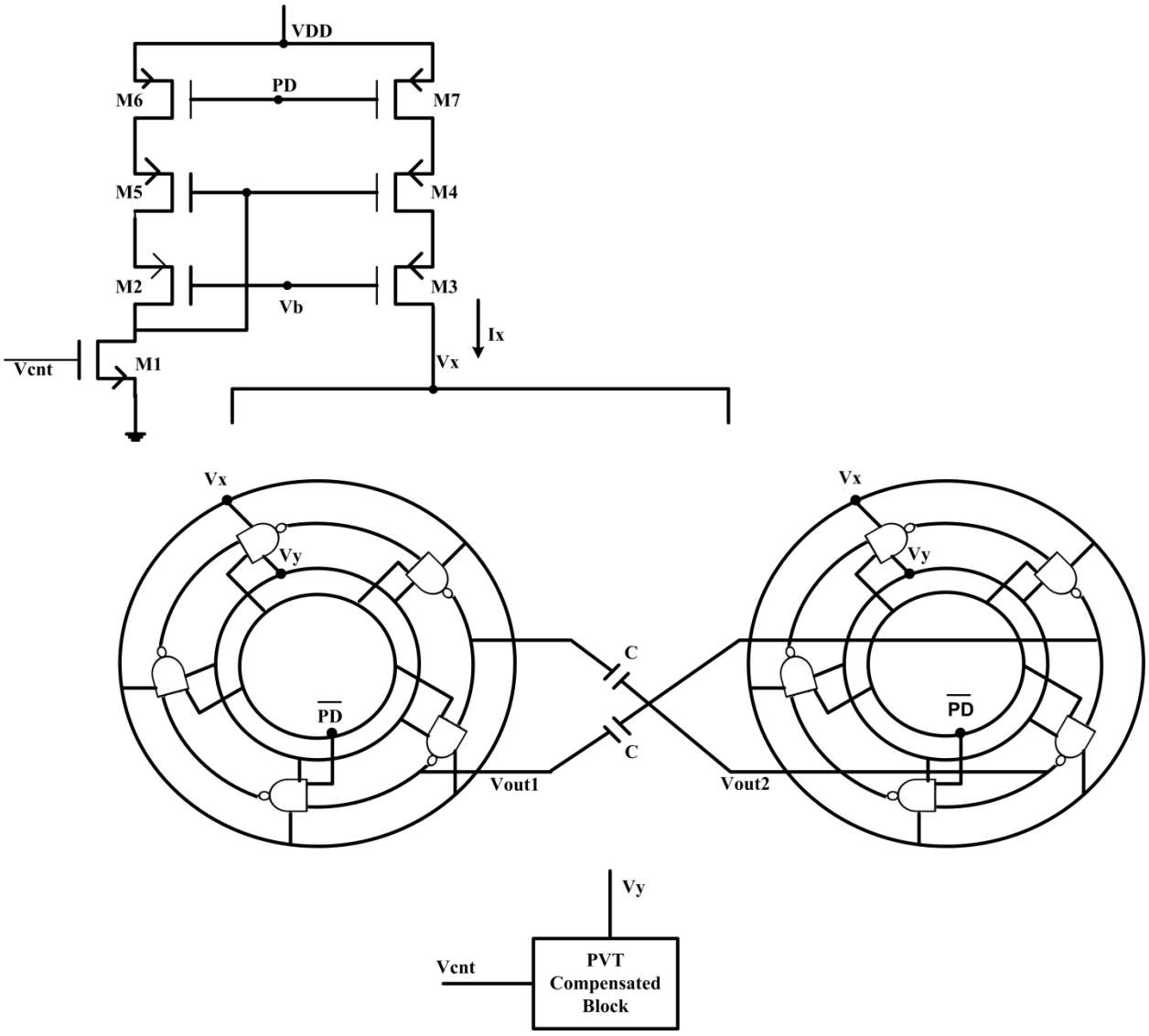

Figure 2.1 Proposed differential VCO architecture

The working of the proposed architecture can be explained with the help of following three different sub-blocks.

1.) Voltage to current converter
2.) NAND based ring oscillator
3.) PVT compensated block

2.1 DESIGN OF VOLTAGE TO CURRENT CONVERTER

As shown in figure 2.1, the V to I converter is made up of seven transistors through M1 to M7. The basic idea of using this circuit is to generate the current which is controlled by the V_{cnt}. This is the key building block as this circuit utilizes the concept of power down technique. A current is generated according to control voltage, which flows through the drain of M1 and M2. Further this current is mirrored through this circuit in PMOS transistor M3. Hence the current Ix is directly proportional to control voltage. And the voltage Vx across this drain terminal of PMOS M3 is further used as supply voltage of the two NAND based ring oscillator. A power down pulse is applied to gate of PMOS transistors M6 and M7. Whenever the PD (power down) pulse goes high, it will turn off the PMOS transistors M6 and M7. And hence the connection of power supply will be lost with the remaining part of proposed circuit. And the NAND based ring oscillator will not give any frequency at the output vout1 or vout2. When power down pulse goes low, the supply of basic NAND based cell is controlled by Vx to achieve constant oscillation. Hence the successful implementation of power down is achieved just by applying pulse to gate of two PMOS M6 and M7 in the proposed architecture.

2.2 NAND BASED RING OSCILLATOR

The voltage Vx generated by the V to I converter described in section 2.1 is then fed to the supply of NAND based ring oscillators. And hence the Ix controls the NAND based circuit and hence this makes the architecture current starved VCO, where current generated by the control voltage produce the output oscillation. The basic structure of NAND based delay cell is shown below in Figure 2.2. Complement of PD works in two modes. When complement of PD is given, it works to stop the frequency of oscillation completely to get the minimized power for that duration. When complement of PD is remain high (at 1.8 volt), it gives proper oscillations and hence the better V to F curve linearity is achieved in this case.

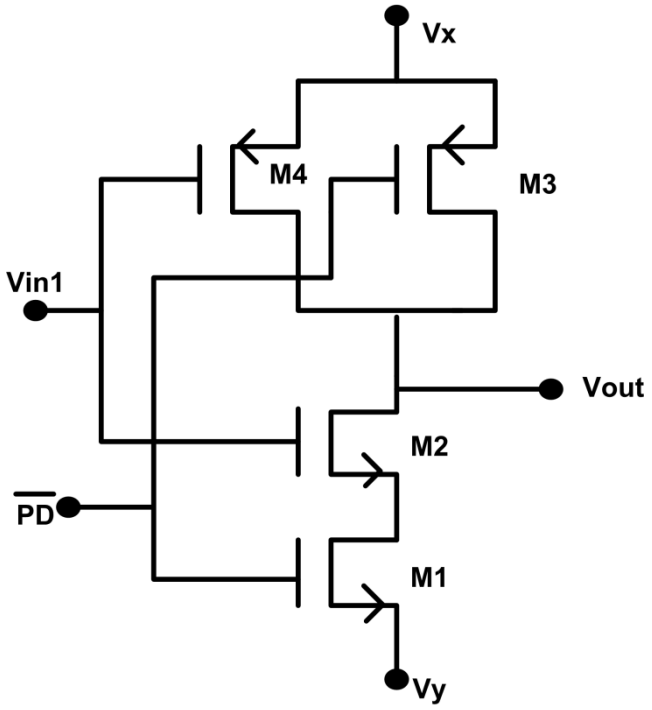

Figure 2.2 Basic NAND base delay cell.

2.3 PVT COMPENSATION OF VCO

When the circuit is in working mode for a long time, the temperature of a circuit changes and hence the mobility of carries will change. And changed mobility directly impacts the performance of VCO. And it causes to change the linearity of frequency range of oscillator. The reduced linearity ranges with the variations in process and temperature is a major concern for the performance of VCO especially when it is used in PLLs and ADCs. A PVT compensation circuit as shown in Figure 2.3 is used to compensate the linearity range. The circuit inside the PVT compensation block is shown in Figure 2.3. An input to the gate of transistor M10 is connected through a process, voltage, temperature resistant circuit where transistor M8 is used as a high resistance. By keeping the gate of M9 at the ground this transistor will remain ON. Size of transistor M8 is more to reduce the VGS of transistors which in turn increases the linearity range across all the PVT corners. Transistor M8 acts as high resistance. Along with resistor R, transistor M8 also gives better temperature insensitivity at Vz and further at Vy node. By increasing the number of transistors in parallel (m in figure 2.3), current is distributed in parallel and hence the linearity range across the large amount of control voltage is achieved. The ground terminal of NAND based inverter ring is connected with the drain of a transistor M10 which is used as a current sink in this architecture. An input to the gate of transistor M10 is connected through a process, voltage, temperature resistant circuit where transistor M8 is used as a high resistance. By keeping the gate of M9 at the ground this transistor will remain ON. NAND gates are used to make ring oscillator. To get the required

range of frequency NAND gates are used instead of simple inverters. The delay of NAND gate is different than that of a CMOS inverter. The Second input of the NAND gate is connected to the complement of power down pulse to stop the oscillations completely when power down pulse goes high.

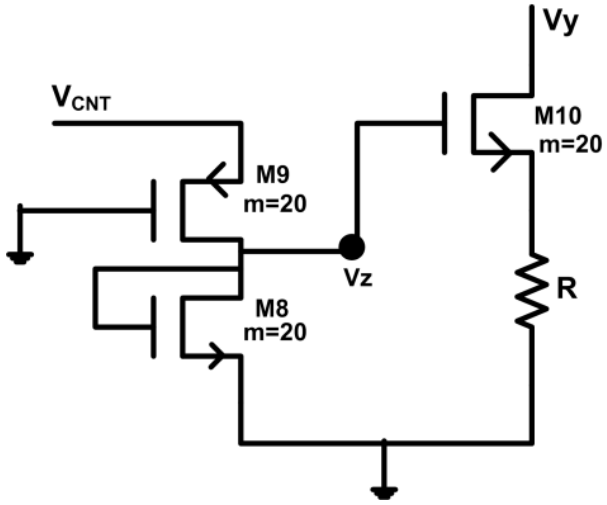

Figure 2. 3 PVT Compensation circuit

The concept of threshold voltage sensor as shown in figure 1.7 as described in chapter 1 is used here to make a circuit which is having better linearity range across the corners. When M8 (shown in figure 2.3) acts as a high value resistance, the voltage at Vz does not vary much with respect the PVT across various corners. The better linearity performance is achieved by increasing the number of Transistors in parallel. And the PVT compensation block gives linear frequency at all (FF, SS, SF, FS, TT) corners, which makes is more suitable for all possible conditions. When manufacturing process of a silicon wafer or a die takes place, the area of the design at the middle of the chip will be not same as it will be at boundaries. The reason of this is the metal layers are not uniform all over the chip after fabrication. When we study about chip fabrication and as we go from one point to another in a die, metal layers sizes is not same.so the process variation comes into the picture gradually.

The variation of process cannot be ignored as we go from higher technology nodes to lower one. From the figure it can be concluded that variation in frequency is very less for low control voltage across the all corners. Whereas it more for the bigger values of control voltage.

CHAPTER 3
PHASE NOISE ANALYSIS OF THE VCO

3.1 PHASE NOISE

This chapter deals with the small signal and mathematical analysis of phase noise of proposed architecture. Noise on the oscillation frequency due to control voltage is an important and unavoidable source for phase noise in the proposed differential ring oscillator. The variations in the frequency of signal are described in terms of phase noise. For a given duration of time frequency stability must be maximized to make sure that oscillator gives sustained oscillation.

If the behavior of any VCO is measured using a spectrum analyzer, one can see random and discrete kind of spikes and spurious having the frequency components. And this is also called the short term stability of VCO. Ideally if there is zero noise in any oscillator, the frequency spectrum of that VCO will be seen as just a single line in spectrum analyzer. But this single line becomes broader as the various noise sources (thermal, flicker, etc.) comes into the picture.

Mathematical analysis of the phase noise can be explained by using the equations established in for white noise and flicker noise separately.

If we consider a large system having local oscillator and number of amplifier, reduction of noise is necessary. As large number of amplifiers used in system can amplify the noise. And hence that leads to the large distortion in the performance of system design.

The expression for SSB phase noise due to white noise in the differential oscillator is given by the following expression [37].

$$\mathrm{L}(f) = 2\frac{KT}{I\ln 2}\left[\gamma\left(\frac{3}{4V_{effd}} + \frac{1}{V_{efft)}}\right) + \frac{1}{V_{op}}\right]\left(\frac{f_0}{f}\right)^2 \qquad (6)$$

Where gmd = 2Ieff \V and I_{eff} is given by I_X in this circuit and replaced in equation 1. The value of overall trans-conductance for the circuit is achieved by using small signal analysis as depicted in Figure 3.1. Transistors M6 and M7 are replaced by the resistance as PMOS works as a resistor in linear region. The total trans-conductance is obtained in terms of individual trans- conductance of PMOS and NMOS used in this V to I converter.

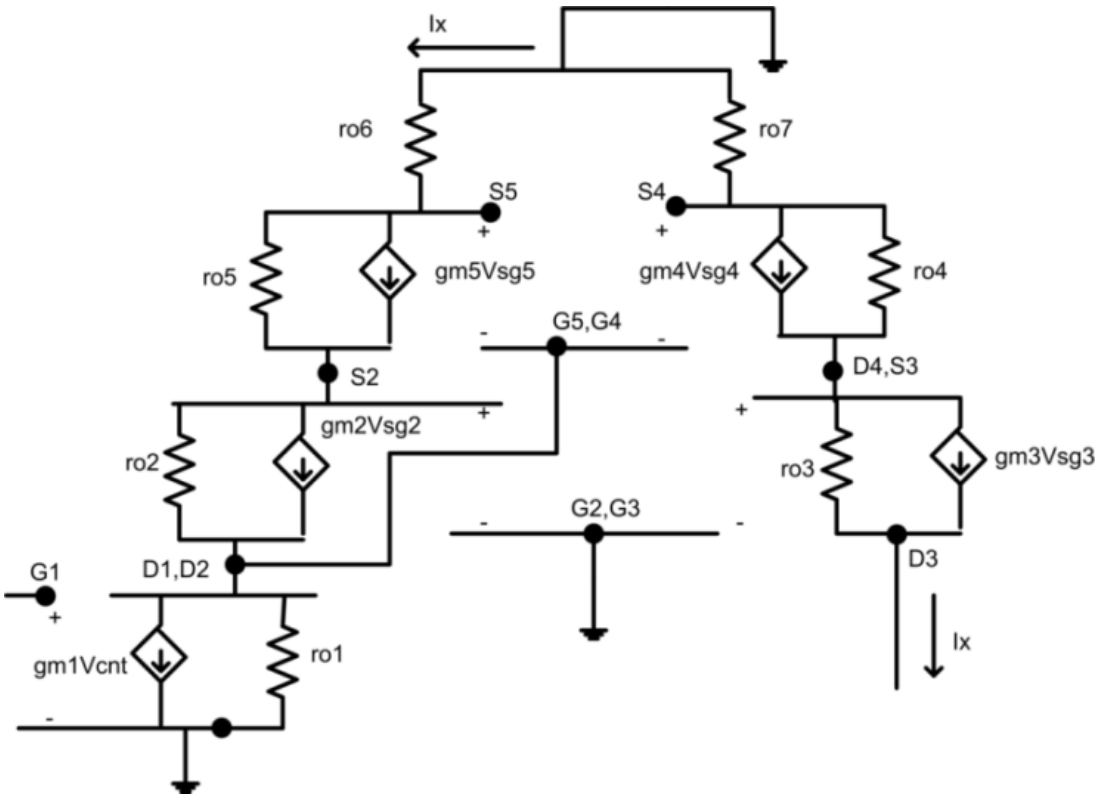

Figure 3.1 Small Signal Analysis

The analysis is started by using KCL and KVL from the upper part of the small signal model shown above in Figure 3.1. Following equations are used to get the final expression for trans- conductance

$$V_{G5} = V_{D1} = r_0(I_X - g_{m1}V_{cnt}) \tag{7}$$

$$V_{D5} = r_{05}\left[g_{m1}g_{m5}V_{cnt} - I_X\left(1 + g_{m5}r_{06} + r_{01} + \frac{r_{06}}{r_{05}}\right)\right] \tag{8}$$

$$I_X = \left(g_{m2} + \frac{1}{r_{02}}\right)V_{D5} - \frac{V_{G5}}{r_{02}} \tag{9}$$

The relation between I_X and V_{cnt} is obtained by putting equation (7) and (8) in equation (9). And value of g_{md} for the proposed power down circuit is expressed in equation (10)

$$\frac{1+\frac{r_{01}}{r_{02}}+\left(g_{m2}+\frac{1}{r_{02}}\right)+r_{05}\left(1+g_{m5}r_{06}+r_{01}+\frac{r_{06}}{r_{05}}\right)}{\frac{r_{01}}{r_{02}}g_{m1}(1+g_{m2}r_{02}+r_{05}g_{m5})} \tag{10}$$

For the analysis of the oscillation frequency of proposed VCO, the charging and discharging time is calculated with the help of simplified basic NAND based cell shown in figure 3.3. Where the second input to the NAND gate is fixed at 1.8 V. Second input of NAND gate is being fixed to get oscillation

for the desired period of time. The calculation is done using the model of CMOS inverter switching characteristics [38]. The fall time and rise time calculation is done as follows.

The fall time for the basic cell is given by $t_f = 2.2(r_{n1} + r_{n2})C_{tot}$ where C_{tot} is total capacitance from the drain of MOSFET M1 to Vy. And rise time is$t_r = 2.2r_{p3}C_{tot}$. By putting all the values in the equation of propagation delay, the expression of time delay for one stage in proposed VCO is

$$t_d = 2.2r_{p3}C_{tot} + 2.2(r_{n1} + r_{n2})C_{tot}$$

So the frequency of oscillation for this 5 stage ring oscillator is achieved by$f_0 = 1/n\,t_d$. And the value of it is given in equation 11 below.

$$f_0 = \frac{1}{11\left[(r_{n1} + r_{n2})r_{p3}\right]C_{tot}} \tag{11}$$

So the frequency of oscillation depends on the resistance of transistors M1, M2, M3 and total capacitance to charge and discharge. Vy act as ground terminal for the circuit. It also works as current sink for the proposed circuit. Vy is the drain voltage for M10, which is used further for the PVT compensated block as well.

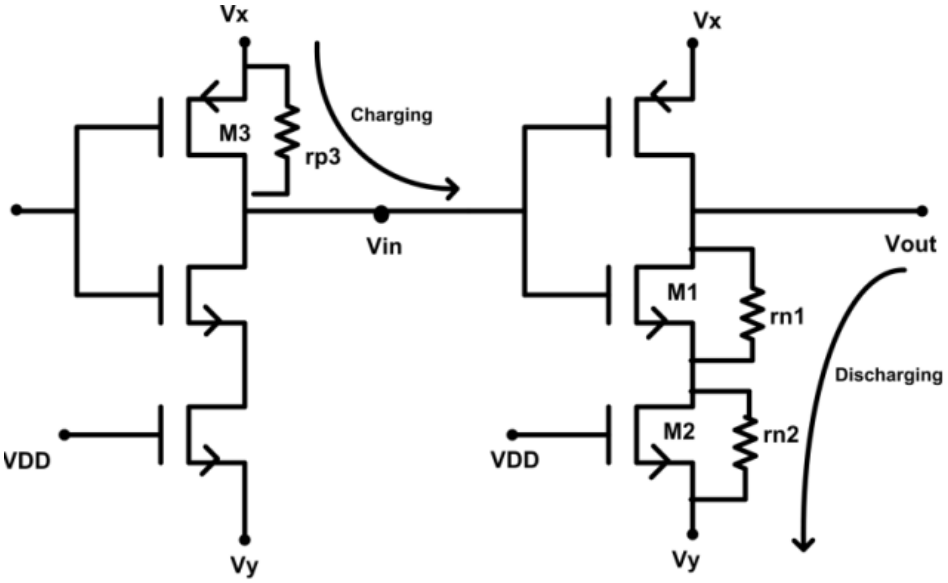

Figure 3.2 Basic cell of NAND based ring VCO

The power per unit bandwidth of an oscillator reduces with the increase of frequency. The second kind of noise is also called 1/f noise (Flicker noise). It follows the characteristics of the curve of 1/f, and also called the spectrum of pink noise. Flicker noise is present in almost every device and it depends on the flow of the current available in the circuit. The expression of flicker noise that modulates the VCO is

given by the following equation. Distortions and perturbations caused by phase and random noise in the voltage controlled oscillator result in a random fluctuation and shift of frequency of the oscillation. Whereas the thermal noise is a proportional to the temperature and resistance of the circuit, flicker noise is a proportional to the characteristics of the circuits. SSB (Single sideband) phase noise is the noise power in a band of 1Hz frequency, which is set at a value of the offset frequency from the carrier. And the unit of this is dBc/Hz.

$$L(f) = A\frac{K_f}{WLC_{oxf}}\left(\frac{1}{{V_{efft}}^2}\right)\frac{{f_0}^2}{f^3} \tag{12}$$

The ratio of current mirror is not (1/A): 1 for the proposed circuit so A is replaced by 1 in the flicker noise equation written above in equation 13. So the equation for this circuit is written below. Finally the flicker noise equation for the proposed architecture shown here describes the dependence of the effective voltage and dimensions of the device effectively.

$$L(f) = \frac{K_f}{WLC_{oxf}}\left(\frac{1}{{V_{efft}}^2}\right)\frac{{f_0}^2}{f^3} \tag{13}$$

And thermal noise is defined for the higher values of frequency. In this work, flicker noise calculations are not observed. At some point the phase noise becomes stable and that is true for thermal noise only. For this work it is simulated that at 1 MHz offset frequency, the phase noise is around -131.6dBC/Hz which is better than other works listed in table 1 as well. It shows that the exponential decay of phase noise whenever we go from low to high range of frequency. This work is observed and simulated in 180nm CMOS process. As CMOS technology goes to lower node, due to millions of transistors and short channel effect, power dissipation cannot be avoided. Hence this power down technique and low noise architecture is also useful for those nodes also. The main points that are better than other works are wide tuning range, low power consumption (when power down switch is activated), low phase noise. Hence it can be concluded that this report shows a better tradeoff between important parameters required for the design of the voltage controlled oscillator which is fully differential in nature as well. In future this work can also be expanded to achieve quadrature or multiphase frequency of oscillation.

TABLE3. 2 COMPARISON OF PROPOSED ARCHITECTURE WITH PREVIOUS WORK

Parameters	Technology	Phase-noise(dBc/Hz)@ offset frequency	Tuning range (MHz)	Free running Frequency (MHz)	Power (μW)	Linearity
Ref. 16	180nm	-122.3 @ 1 MHz	2170 to 2173	-	2700	-
Ref. 19	350nm	-101 @ 600 KHz	.004 to 1000	900	9800	0.6 to 1.4
Ref. 20	130nm	-	-	2000	11700	-
Ref. 21	65nm	-111 @ 1 MHz	352 to 454	400	158	-
Ref. 22	65nm	-94.84 @ 1 MHz	-	490	45	-
Ref. 23	180nm	-85.31 @ 1 MHz	-	4000	4500	-
Ref. 24	180nm	-	-	500	9400	-
Ref. 25	180nm	-89.7 @ 1 MHz	4129 to 6122	-	4475	-
Ref 26	180nm	-107.1@10 MHz	-	-	7410	-
This Work	**180nm**	**-130.1 @1 MHz**	**40 to 650**	**550**	**208 (without PD) .0504 (with PD)**	**0.9 to 1.8**

The above mentioned table shows the comparison of different architectures of VCOs. The power consumption, linearity range, supply voltage and phase noise are compared.

CHAPTER 4

SIMULATION AND EXPERIMENTAL RESULLTS OF PROPOSED ARCHITECTURE

The preceding chapters illustrate the proposed architecture VCO with power down technique. Circuit level description of various blocks has been explained in the previous chapters. In this chapter, the result and simulations of the all blocks are described, which are mentioned above. Also various results of phase noise analysis are done for the proposed design in next sections.

4.1 VOLTAGE TO CURRENT CONVERTER

A linear relation between current and voltage is provided by the V to I converter in this design. As the control voltage increases, the value of current also increases. This is further used in 5 stage differential ring oscillator. The range which is linear is from 0.9 to 1.8 volt as shown in Figure 4.1 below. The relation between control voltage and Ix is also shown in Figure 4.2

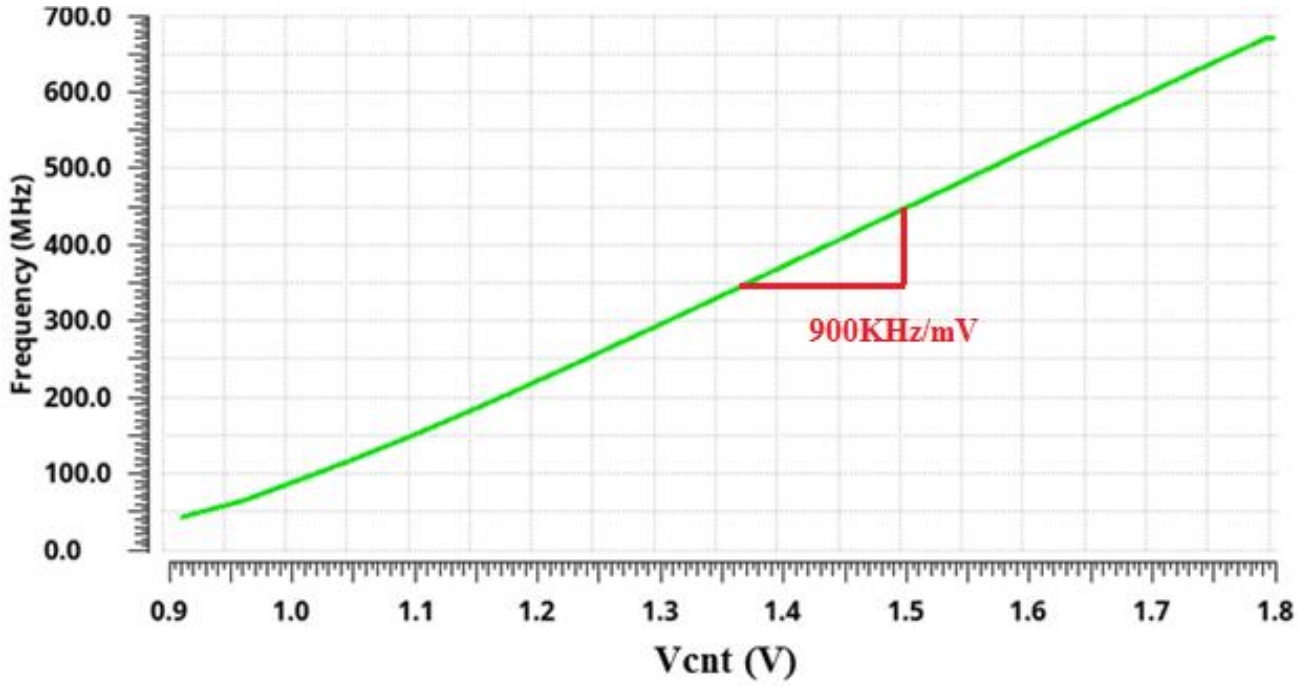

Figure 4. 1 Linear relation between control voltage and output frequency

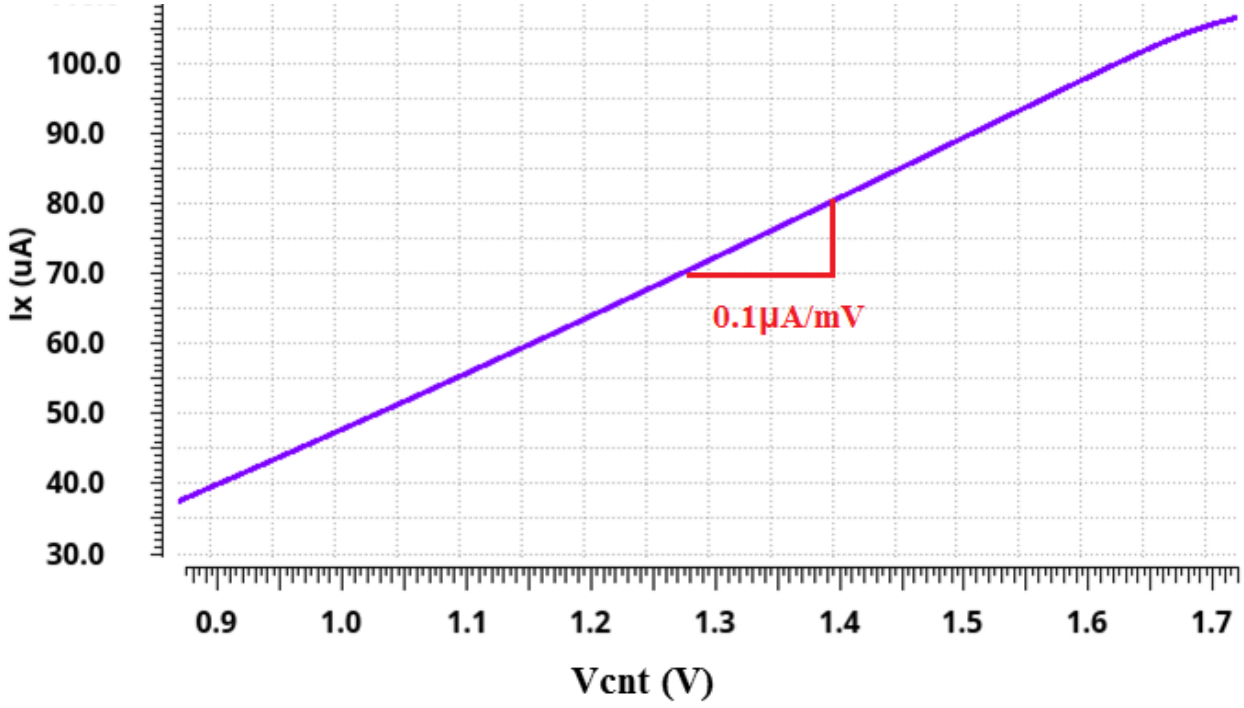

Figure 4. 2 Linear relations between control voltage and Ix

4.2 DIFFERENTIAL OUTPUT FOR PROPSED CIRCUIT

The need of differential structure is generally occur for the minimization of noise caused by different sources. Noise in analog circuits is an unwanted and undesired form of signals that must be removed.

To make a circuit differential in nature a replica of basic cells are used. In this work out of phase output is obtained by using two capacitances in cross coupled way as shown in proposed circuit in chapter 2.

The output phase for the ring VCO is found at every value of θ by using the concept of differentially cross-coupled charge within the ring. Out of all possible values of phases, 180^0 phase shift is used to get differential output Vout1 and Vout2 in this report. Phase between two outputs of the VCO can be any of multiple integer values of θ. But here the discussion is focused on only the value of180^0. Otherwise it could be anything among 0, 30, 60, 90,180, 220,250 etc. The Frequency of oscillation in VCO for $r * s$ ring VCO (where r is a positive integer representing the number of rows and s is number of inverter stages) is given by. [13]

$$f_0 = \frac{1}{2s\tau_{pd} + (2(r-1)R_{eq}C_{eq})}$$

τ_{pd} is propagation delay of one stage. This work consists of s=5 and r=2. Capacitors are used to provide 180 degree of phase shift. To make it quadrature phase VCO, number of capacitors can be increased in the proposed design. Differential outputs for this architecture is shown in Figure 4.4. This VCO architecture is made differential to minimize the effect of noise. And this is clearly shown in the

upcoming section with experimental results and simulations. The same differential output is also simulated for the values of supply voltage of 1.62Volt and 1.98Volt as well. Using the parameter analysis in CADENCE virtuoso, this simulation is done for various temperature and process corners. The temperature range is taken from 0 to 85 whereas the range of supply voltage is put from 1.62 to 1.92 Volt.

These variations are taken to make circuit implementable at different environmental conditions. The frequency for proposed circuit in the presence of capacitances is given by equation written below. Capacitances are used to get out of phase VCO oscillations.

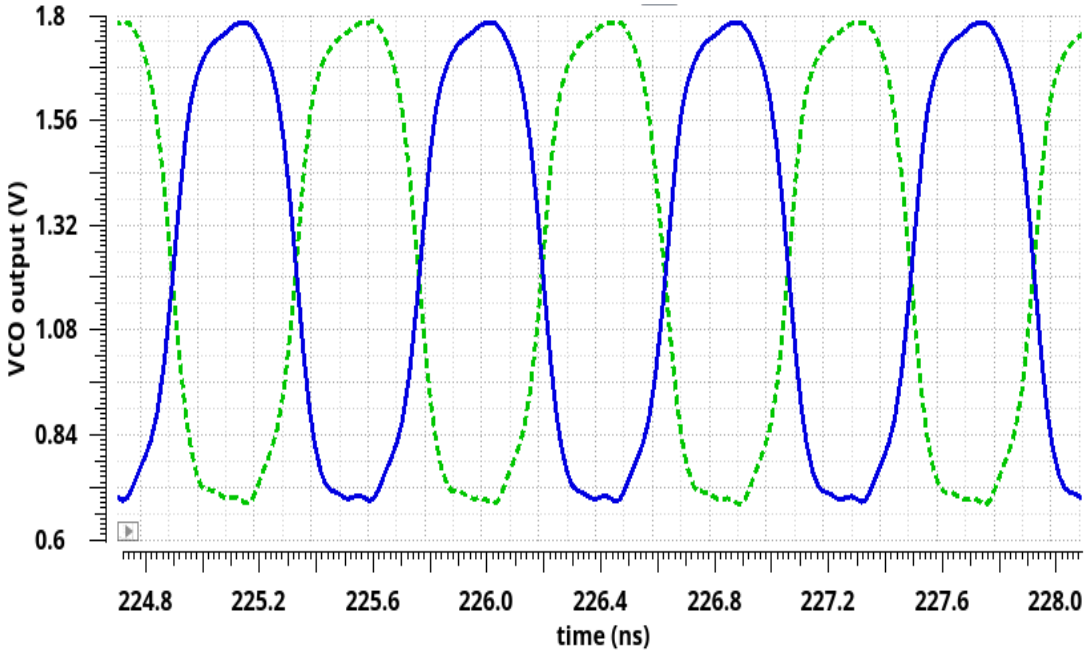

Figure 4. 3 Differential Output of VCO

The frequency for proposed circuit in the presence of capacitances is given by equation 14. Capacitances are used to get out of phase VCO oscillations.

$$f_0 = \frac{1}{10\tau_{pd} + 2R_{eq}C_{eq}} \qquad (14)$$

4.3 VCO OUTPUTS WITH POWER DOWN TECHNIQUE

This section explains the simulation results of VCO output with power down pulse implemented in 180 nm CMOS technology using cadence virtuoso. Figure 4.4 shows the oscillation frequency and average current through supply with the low and high power down pulse. The magnified version of the output of VCO with PD pulse is shown in Figure 4.5. It is clearly shown in this Figure 4.5 that VCO output has

zero frequency when PD pulse has high value. That indicates that power becomes negligible at that duration of time.

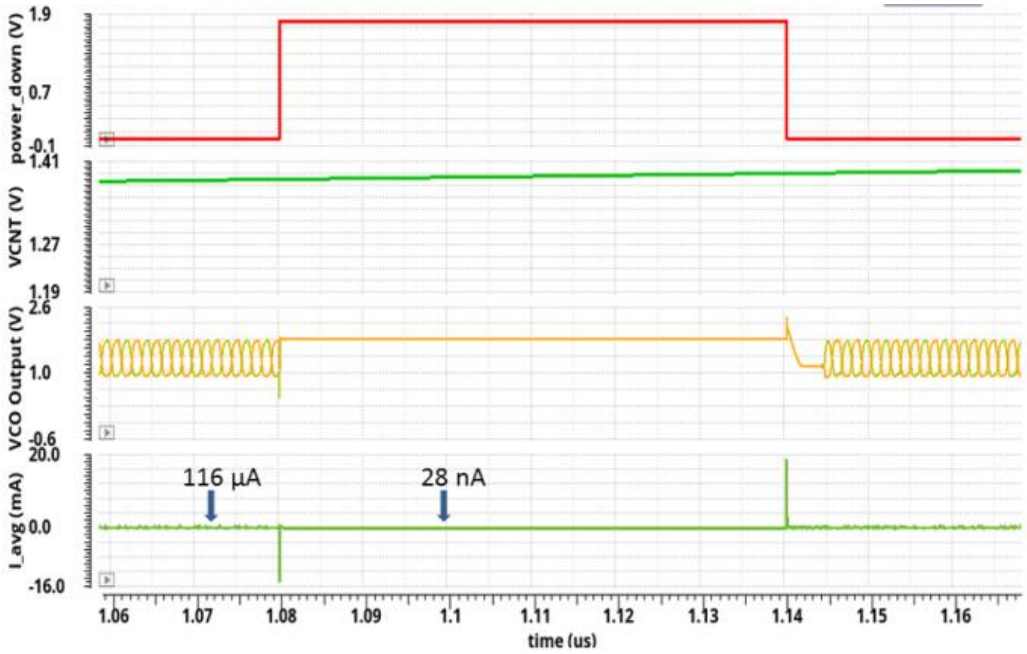

Figure 4.4 VCO output with power down pulse

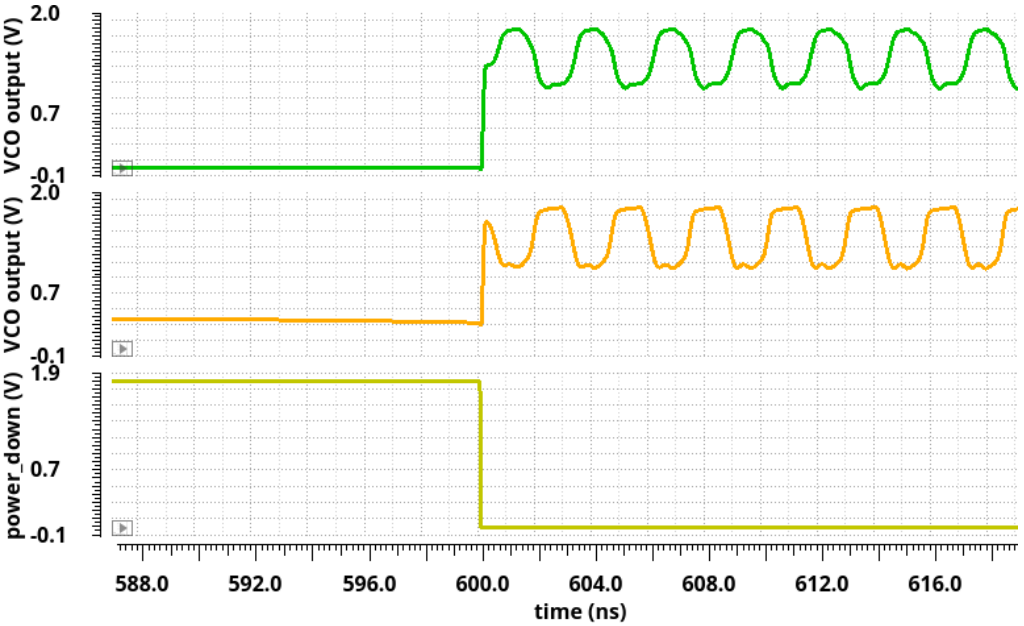

Figure 4.5 VCO output with power down pulse (magnified)

4.4 PVT COMPENSATION BLOCK

This section describes the PVT invariance technique used in this work. The circuit which is implemented for process, voltage and temperature is already explained in preceding chapters. This chapter deals with the output waveforms of the relationship between frequency and control voltage. The improved linearity can easily be achieved with PVT compensation circuit. And it is shown in figure 4.6 and 4.7. Hence the range of frequency achieved is also suitable for cognitive radio application. The range which is obtained by the proposed architecture is from 40 MHz to 650 MHz

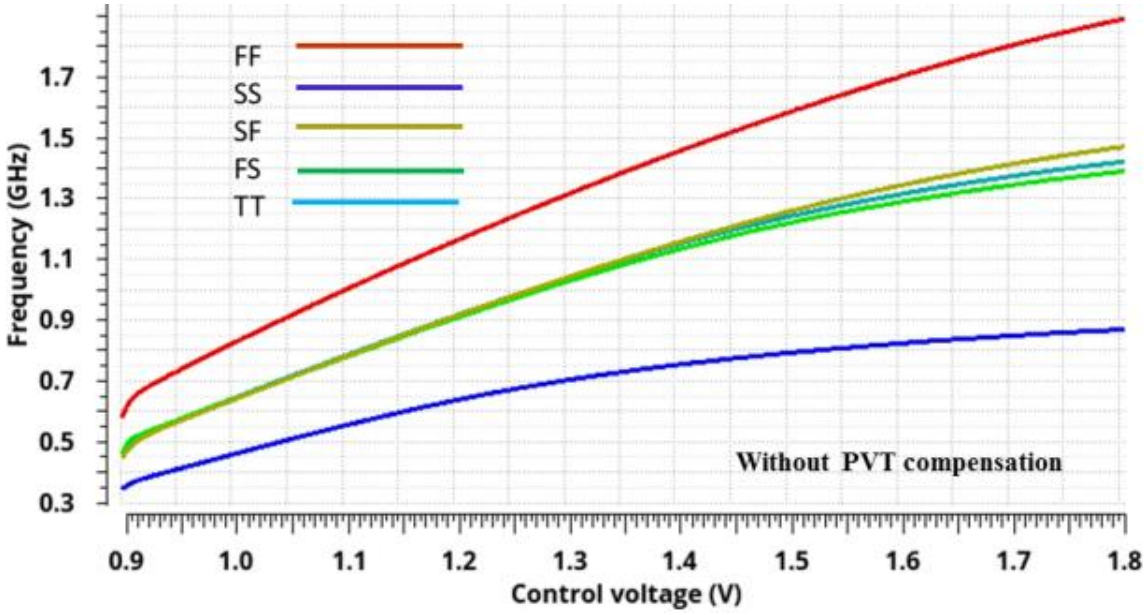

Figure 4. 6 Frequency at different corners (without PVT)

This Figure shows the VCO voltage to frequency curve at different corners. The measured temperature range is 0^0 to 85^0. And supply voltage range is taken from 1.62 V to 1.92 V. PVT corner analysis is very important for any design as circuit design must be working in all the possible environmental conditions. Figure 4.6 shows lower linearity range across all the corners whereas the improved linearity range is shown in figure 4.7. This section describes the PVT invariance technique used in this work. The circuit which is implemented for process, voltage and temperature is already explained in preceding chapters. This chapter deals with the output waveforms of the relationship between frequency and control voltage. From .9 to 1.2 curve of control voltage and frequency is linear but after that value it tends to become nonlinear at different corners. Now to change the slope of those nonlinear curves, concept of PVT compensation is applied in this work. The supply current is directly proportional to control voltage. And when we increase the load by adding transistors in parallel as discussed in chapter 2, the slope will bend towards higher frequency for all corners. And hence we will get better linearity

range. The maximum supply voltage is 1.8 Volt. So the range of control voltage is also limited to the same value. It is also shown in both figures that variation is in close proximity for FS, SF, TT corners for both the cases. But it tends to become worsen at FF and SS corners. When the temperature is high, it directly affects the threshold voltage and hence the drain current of the transistor changes.

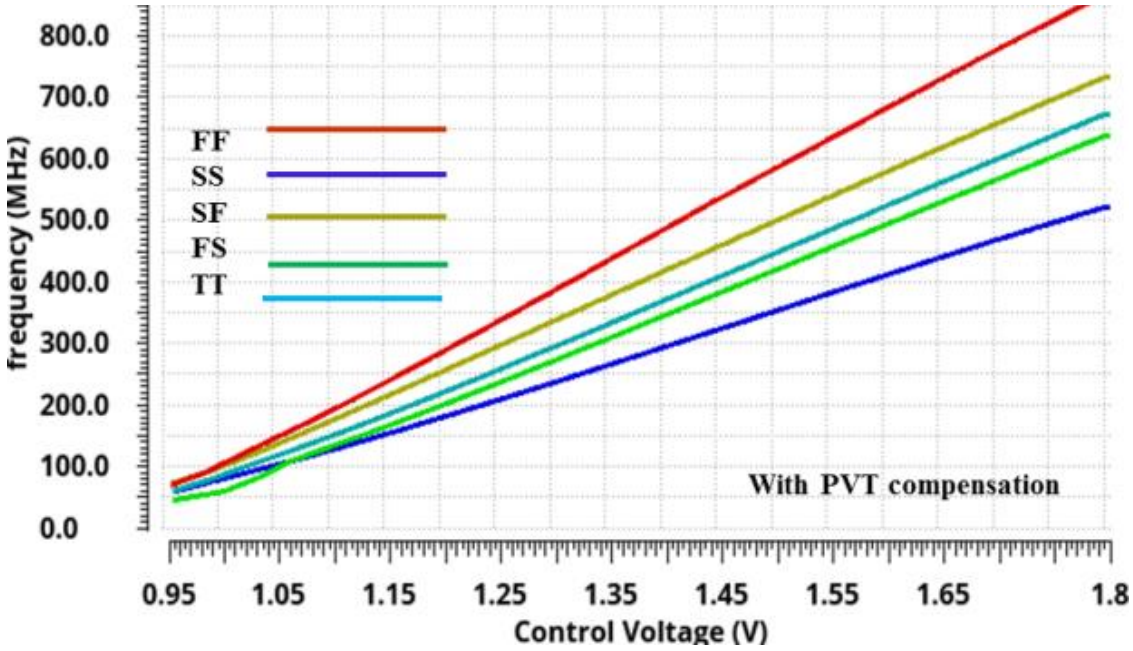

Figure 4.7 Frequency at different corners (with PVT)

The better linearity performance is achieved by increasing the number of transistors in parallel. And the PVT compensation block gives linear frequency at all (FF, SS, SF, FS, TT) corners, which makes is more suitable for all possible conditions. When manufacturing process of a silicon wafer or a die takes place, the area of the design at the middle of the chip will be not same as it will be at boundaries. The reason of this is the metal layers are not uniform all over the chip after fabrication. When we study about chip fabrication and as we go from one point to another in a die, metal layers sizes is not same.so the process variation comes into the picture gradually. The variation of process cannot be ignored as we go from higher technology nodes to lower one.

4.5 PHASE NOISE SIMULATION RESULT

In this section, the results of phase noise of different blocks are explained. The measured phase noise is -130.1dBc/Hz at 1MHz offset frequency. And the noise contributed by V to I converter is -169.71 dBc/Hz. Simulation results for all the basic building blocks of proposed architecture can be compared for the analysis of circuit performance.

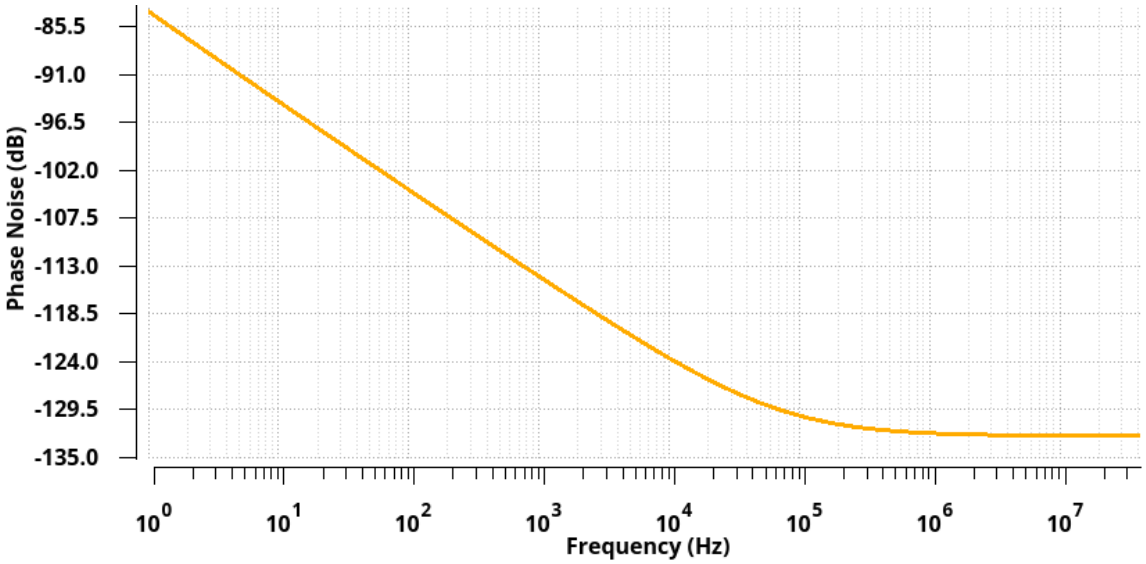

Figure 4.8 Phase noise of proposed Architecture

The noise of PVT compensated block is -145.5 dBc/Hz .and noise for V to I converter is -169.71 dBc/Hz. The contribution of phase noise and circuit noise of different blocks is shown in Figure 4.8 to Figure 4.10. , it can be concluded that there is not much contribution of PVT compensated block in the total noise. This block is also used as current sink in this circuit. It absorbs the current from the remaining part of architecture. Current coming from V to I converter flows into the PVT compensated block.

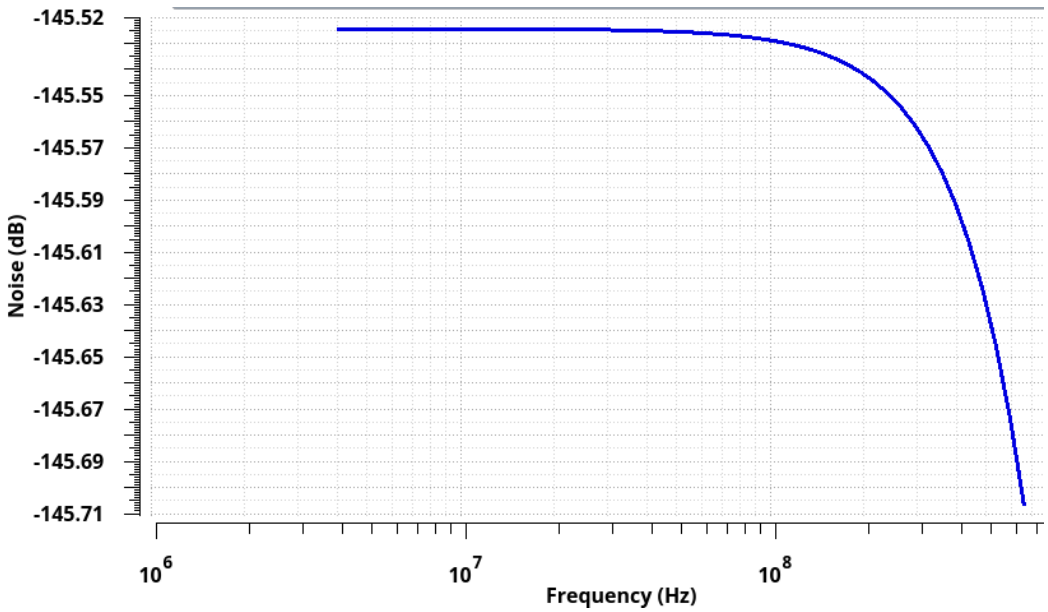

Figure 4.9 Noise of PVT compensated block

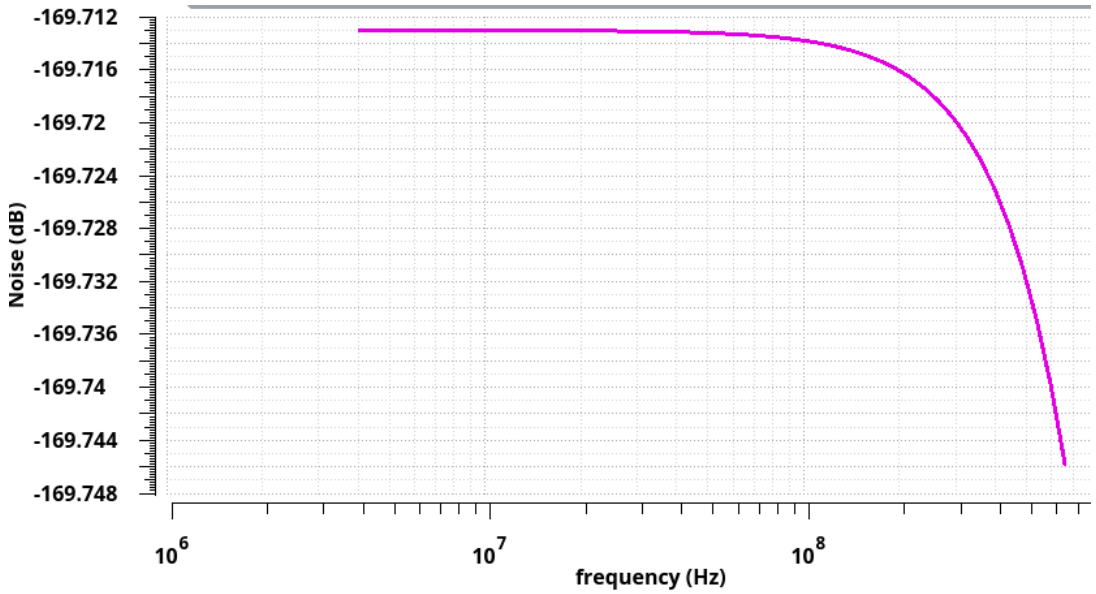

Figure 4.10 Noise of voltage to current converter (with low power down)

General mathematical expressions for the phase and flicker noise are already expressed in previous chapter. Here it is clearly observed that the total measured phase noise is better than other previous work mentioned in the table 1.

CHAPTER 5
CONCLUSION AND FUTURE SCOPE

5.1 CONCLUSION

A five-stage differential ring VCO that uses a power down concept is proposed. The power consumption goes drastically low in Nano watts by using a power down pulse. This architecture also shows better linearity and PVT insensitivity across the different corners by using a PVT compensated block. This circuit shows a wide tuning range from 40 MHz to 650 MHz which is suitable for cognitive radio devices. This range is also linear for 0.9 V to 1.8 V. The Circuit is designed and simulated using SCL 0.18 μm CMOS technology. Simulation results show that proposed differential VCO has low power consumption and a wide linear tuning range. The measured phase noise is -130.1dBc/Hz at 1MHz offset frequency and power dissipation is 208 μW (without power down) and 50.4 nW (with power down) from a 1.8 V supply. Table 1 compares the proposed VCO with recently reported VCOs. The Proposed technique successfully gives the wide tuning range, which is not possible for other architectures mentioned in table 1. The power consumption is also low for this architecture by using power down technique as compared to other structures.

5.2 FUTURE SCOPE

The different parameter of VCO is considered for low power and wide tuning range and characteristic are compared with other architectures of CMOS VCOs to get an idea for future perspective for the design of VCOs. And hence to reduce the variation in PVT, the fully digital calibration technique can be applied. The proposed VCO is designed for the cognitive radio that can also be designed for IoT application in future. By using different algorithms the proposed VCO can be used for low power, low noise PLL and ADCs.

CHAPTER 6

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1. Naveen Kandpal and Anil Singh, "A Low Power and Wide Linearity Range Fully Differential Ring Voltage Controlled Oscillator with Power Down Technique for Cognitive Radio" Journal of Circuits, Systems, and Computers. (Communicated)

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