FERMI ENERGY AND TEMPERATURE DEPENDENT PERFORMANCE ANALYSIS OF MLGNR BASED VLSI INTERCONNECTS

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CERTIFICATE

Certified that the thesis entitled **"FERMI ENERGY AND TEMPERATURE DEPENDENT PERFORMANCE ANALYSIS OF MLGNR BASED VLSI INTERCONNECTS"** being submitted by **Mr. Himanshu Sharma** to the **Department of Electronics and Communication Engineering, Thapar Institute of Engineering & Technology, Patiala** in fulfillment of the requirements for the award of degree of **"Doctor of Philosophy"** is a record of bonafide research work carried out by him. He has worked under my guidance and supervision and fulfilled the requirements for the submission of this thesis which has reached the requisite standard. The matter presented in this thesis does not incorporate any material previously published or written by any other person except where, due references are made in the text.

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Himanshu Sharma

This is to certify that the above statement made by the candidate is correct to the best of my knowledge and belief.

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ABSTRACT

The downscaling of technology nodes leads to increase the number of active devices which are used in very large-scale integration (VLSI) for chip design industry. Longer interconnects are required to interface millions of active devices in an integrated circuit (IC). Parasitic parameters of interconnects increase linearly with an increase in the length of the interconnects. As a result, the performance of the interconnects becomes a primary focus when compared with the performance of active devices in nano-scaled technology nodes. This research discusses the conventional aluminum and copper interconnects and explored the possibilities to replace these interconnects owing to their higher resistivity, electro-migration, surface and grain boundary scatterings. With the advancement of the technology nodes, it is required to increase the current density and decrease the cross-sectional dimensions of an interconnect. Carbon nanomaterials, i.e., graphene nanoribbons (GNRs) and carbon nanotubes (CNTs), demonstrate effective electrical, thermal, and mechanical properties. The GNR and CNT are allotropes of carbons with the potential to function as interconnects in the development of an IC for the VLSI industry. Although the GNR and CNT exhibit similar properties, considering the fabrication process, graphene is more suitable and can be easily controlled when compared with CNT because of its planer nature. Further, considering the number of layers, the GNR could be divided into two types: single layer GNR (SLGNR) and multilayer GNR (MLGNR). The SLGNR shows high resistivity in contrast to the MLGNR; hence, the MLGNR is a suitable material for on-chip high-performance VLSI interconnects.

The performance of MLGNR as an interconnect at global levels in on-chip VLSI IC should be studied to be employed in different applications. This research work presents the impact of Fermi energy and temperature variations on the performance of MLGNR interconnects at a global length. A Fermi energy dependent equivalent circuit model is proposed to calculate the parasitic parameters of the MLGNR interconnect. The impact of Fermi energy on the MLGNR conductivity is analyzed using mathematical equations. An increase in intercalation doping increases the Fermi energy of the MLGNR layers, which increases its conductivity. The impact of the Fermi energy variation on the parasitic parameters of the MLGNR interconnect at three different technology nodes (32nm, 22nm, and 16nm) for variable global lengths (500–2000μm) is analyzed.

The performance of elite ICs is influenced under variable thermal conditions. With the downscaling of the technology nodes, the impact of temperature on interconnects becomes a

major challenge in designing next generation VLSI ICs. Therefore, the impact of temperature on the performance of MLGNR functioning as an interconnect should be analyzed to estimate their actual performance under a thermally variable environment at global levels. A temperature-dependent circuit model of the MLGNR is proposed to evaluate the impedance parameters, which include the various electron–phonon scatterings as a function of temperature. The scattering mechanism in the MLGNR is of two types: electron–electron scattering and electron–phonon scattering. The electron–phonon scattering is crucial when compared with electron–electron scattering with the rise in temperature on the effective mean free path (MFP) of the MLGNR. The phonon scattering is classified into acoustic, optical, and zone boundary scatterings. The temperature-dependent effective MFP of the GNR interconnect is dominated by the acoustic scattering from low to moderate range of temperatures, i.e., from 200 to 300K. Further, at a high temperature range (300–500K), the acoustic, optical, and zone boundary scatterings impact the effective MFP of the GNR.

Based on the temperature dependence, the parasitic parameters are calculated at global lengths for 32nm, 22nm, and 16nm technology nodes. The physical parameters used for the three technology nodes are obtained from the International Technology Roadmap for Semiconductors (ITRS 2013). The impact of temperature on the MFP is considered to evaluate the parasitic parameters of the MLGNR functioning as interconnects using MATLAB computing software. The effective MFP of the GNR reduces, which further dominates its own resistance at high temperatures (300–500K) for three different technology nodes. The resistance of the MLGNR interconnect increases sharply after 300K due to the shrinking of the effective MFP for the three different technology nodes considered for the study at a global length of interconnects. To calculate and analyze the performance of the MLGNR interconnects from the delay, power dissipation, and power delay product (PDP) parameters, the simulation program with integrated circuit emphasis (SPICE) simulation tool is utilized based on Fermi energy and temperature-dependent models. The delay and PDP of the MLGNR increases with an increase in the interconnect length but decreases with a rise in Fermi energy. The Fermi energy-dependent MLGNR results are compared with the copper interconnect in terms of delay and PDP for equal length and technology nodes. Similarly, the delay and PDP increase with a rise in temperature (200–500K) at the global length of interconnects. The temperature-dependent analytical delay model of the MLGNR interconnects is also presented, and the results obtained from the analytical delay model are compared with the simulation results. The simulation and analytical results show that the outcomes of the two models correspond well. The trend of the two models shows that the delay increases with a rise in temperature (200–

500K) for different technology nodes, i.e., 32nm, 22nm, and 16nm. Furthermore, Relative stability of MLGNR is analyzed from 500–2000μm length with respect to switching delay and observed that with increasing interconnect length switching delay increases as a result input signal damp faster which upswings the relative stability of MLGNR for all three various technological nodes. Besides, relative stability is analyzed at length 2000μm and temperature 500K of MLGNR through Nyquist plots and observed that the system will achieve stability faster as we move from 32nm to 16nm technological node due to higher values of parasitic because of the reduction in MFP of electrons.

The combined impact of Fermi energy and temperature on the performance of MLGNR in delay and PDP terms at global levels for three different technology is also presented and analyzed that both delay and PDP increases with rise in temperature (200–500K) but decreases with rise in the level of Fermi energy (0.2eV–0.6eV). A temperature-dependent comparative analysis of the MLGNR with copper and SWCNT interconnects considering delay and PDP as performance parameters is conducted for equal length and technology nodes. Moreover, the results show that the performance of the MLGNR interconnects is much better than those of the SWCNT and copper interconnects considering the impact of Fermi energy and temperature at a global length of interconnects for 32nm, 22nm, and 16nm technology nodes. Therefore, it has been concluded that the MLGNR is an outstanding material for the fabrication of nano-electronic ICs in a thermally variable conditions.

ACRONYMS AND ABBREVIATIONS

Abbreviation	Description
ac-GNRs	Armchair edged Graphene Nanoribbons
CMOS	Complementary Metal Oxide Semiconductor
CNTs	Carbon Nanotubes
Cu	Copper
DIL	Driver Interconnect Load
EMC	Electromagnetic Compatibility
EMI	Electromagnetic Interference
ESC	Equivalent Single Conductor
ICs	Integrated Circuits
ITRS	International Technology Roadmap for Semiconductor
MCC	Multi-conductor Circuit
MFP	Mean Free Path
MLGNR	Multilayer Graphene Nanoribbon
MTL	Multi-conductor Transmission Line
MWCNT	Multi-Walled Carbon Nanotube
PDE	Partial Differential Equation
PDP	Power Delay Product
PTM	Predictive Technology Model
SLGNR	Single Layer Graphene Nanoribbon
SPICE	Simulation Program with Integrated Circuit Emphasis
SPP	Surface Polar Phonons
SWCNT	Single-Walled Carbon Nanotube

VLSI	Very Large Scale Integration
zz-GNRs	Zig-Zag edged Graphene Nanoribbons

GLOSSARY OF SYMBOLS

Symbol	Description
A	Area
C_{bundle}	Total capacitance of an SWCNT bundle
C_e^{bundle}	Electrostatic capacitance of SWCNT shell
C_q^{bundle}	Quantum capacitance of SWCNT shell
C_e	Electrostatic capacitance of MLGNR
C_g	Capacitance of copper interconnect
C_l	Load capacitance
C_m	Coupling capacitance of MLGNR
C_q	Quantum Capacitance of MLGNR
D	Diameter of SWCNT
d	Distance from the ground plane
D_{AC}	Acoustic deformation potential
D_{op}	Optical deformation potential
E_f	Fermi energy
h	Planck's constant
K_B	Boltzmann's constant
l	Length of interconnect
L_{bundle}	Total inductance of an SWCNT bundle
l_{ko}	Kinetic inductance of SWCNT shell

l_{mo}	Magnetic inductance of SWCNT shell
L_{cu}	Inductance of copper interconnect
l_e	Magnetic inductance of MLGNR
l_k	Kinetic inductance of MLGNR
l_m	Coupling inductance of MLGNR
M_q	Peak overshoot voltage
N_{bundle}	Total number of SWCNT tubes in a bundle
$N_{W(bundle)}$	Number of columns in a SWCNT bundle
$N_{H(bundle)}$	Number of rows in a SWCNT bundle
$N_{ch_{GNR}}$	Number of conduction channels of SLGNR
$N_{ch_{MLGNR}}$	Number of conduction channels of MLGNR
N_{op}	Phonon occupation numbers
N_s	2-D electron gas concentration in GNR
n	Number of layers in MLGNR
n_x	Number of cycles
n_o	Number of distributed segments
$R(T)_{bundle}$	Temperature-dependent resistance of the SWCNT bundle
R_c	Contact resistance
R-L-C	Resistance-Inductance-Capacitance
R_o	Resistance of copper at room temperature
R_q	Quantum resistance
r_s	Scattering resistance

s	Complex frequency
T	Temperature in kelvin
T_{q}	Switching delay
t	Thickness of interconnect
v_{f}	Fermi velocity
v_{s}	Speed of acoustic phonons
w	Width of interconnect
x	Center to center distance of the adjoining tubes
ϵ_{r}	Dielectric constant
λ^{AC}	MFP due to acoustic phonon scattering of GNR
λ_{d}	MFP due to defect scattering of MLGNR
λ_{eff}	Effective MFP of interconnect
λ_{r}	MFP due to edge scattering of MLGNR
ρ_{m}	Mass density of graphene
ρ_{0}	Resistivity of copper
δ	Vander Wall's spacing
λ^{OZB}	MFP due to optical and zone boundary scattering of GNR
$\frac{h}{2\pi} w_{\mathrm{op}}$	Optical phonon energy
$\lambda_{\mathrm{abs}}^{\mathrm{op}}$	Scattering due to optical phonon (absorption) of GNR
$\lambda_{\mathrm{emm}}^{\mathrm{op}}$	Scattering due to optical phonon (emission) of GNR
ω_{n}	Angular frequency
ξ	Damping coefficient

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CHAPTER 1

INTRODUCTION

1.1 Preface

Human society and civilization have been strongly transformed into an era of communications and digital computing. Integrated electronic circuits have been developed, measured by the number of transistors and connecting wires on a single chip. The phenomenon growth has been achieved with downscaling or scaling the size of metal oxide semiconductor (MOS) transistors. The rapid shrinking has been detected in the transistors from the previous four decades. The MOS transistor being smaller in size, consume less power and operate faster as a result brought improvement in the efficiency, power consumption and consistency of electronics circuit. With the downscaling of technology nodes the efficiency of gate becomes less pronounced compared to the interconnect performance due to insignificant parasitic effects. The very large scale integration (VLSI) is the methodology used for creating integrated circuits (ICs), where several transistors are integrated into a single chip. The performance of the VLSI circuits can be improved by the interconnects used to connect different devices of electrical circuit [1–2]. The interconnects can be characterized as a bunch of wires that are used to connect the transistors in order to execute the work related to the devices in the VLSI design chip.

The study of on-chip interconnects is a challenging area in the field of VLSI integrated circuits. The reliability for adopting the paramount material as an interconnect, such as copper and aluminum, is challenging [3–5]. Downscaling the dimensions of the interconnects affects the parasitic parameters. The performance of the interconnects in an IC primarily depends on the current carrying capability and its parasitic parameters (capacitance (C), inductance (L), resistance (R)) [3, 6–10]. The continuous scaling of technology nodes introduces several new ideas in VLSI-ICs, which are incorporated to connect millions of active devices in the ICs [11–18]. The structure of an interconnect is shown in Figure 1.1, which is driven by a complementary MOS (CMOS) inverter and connected to a capacitive load. To evaluate the performance, an interconnect has to be replaced by an R-L-C electrical circuit model. The parasitic parameters of the interconnects depend on the cross-sectional dimensions and properties of materials used as the VLSI interconnect [19–22].

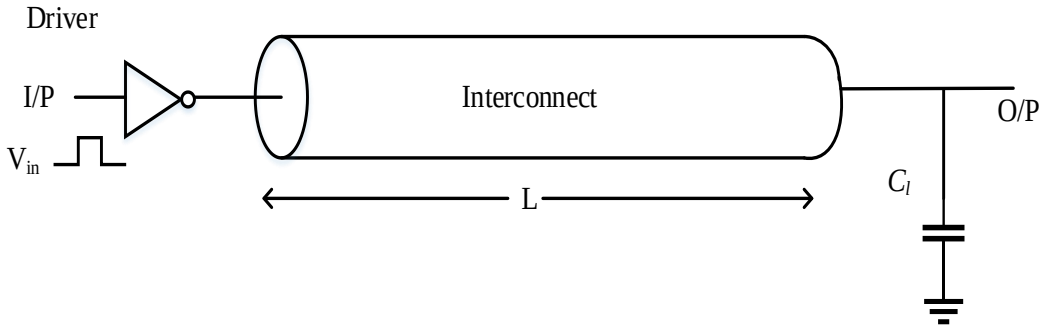


Figure 1.1 Structure of an interconnect

The ICs are fabricated depending on the length as well as cross-sectional dimensions of interconnects, which are classified into three types i.e., global, intermediate, and local interconnects as shown in Figure 1.2.

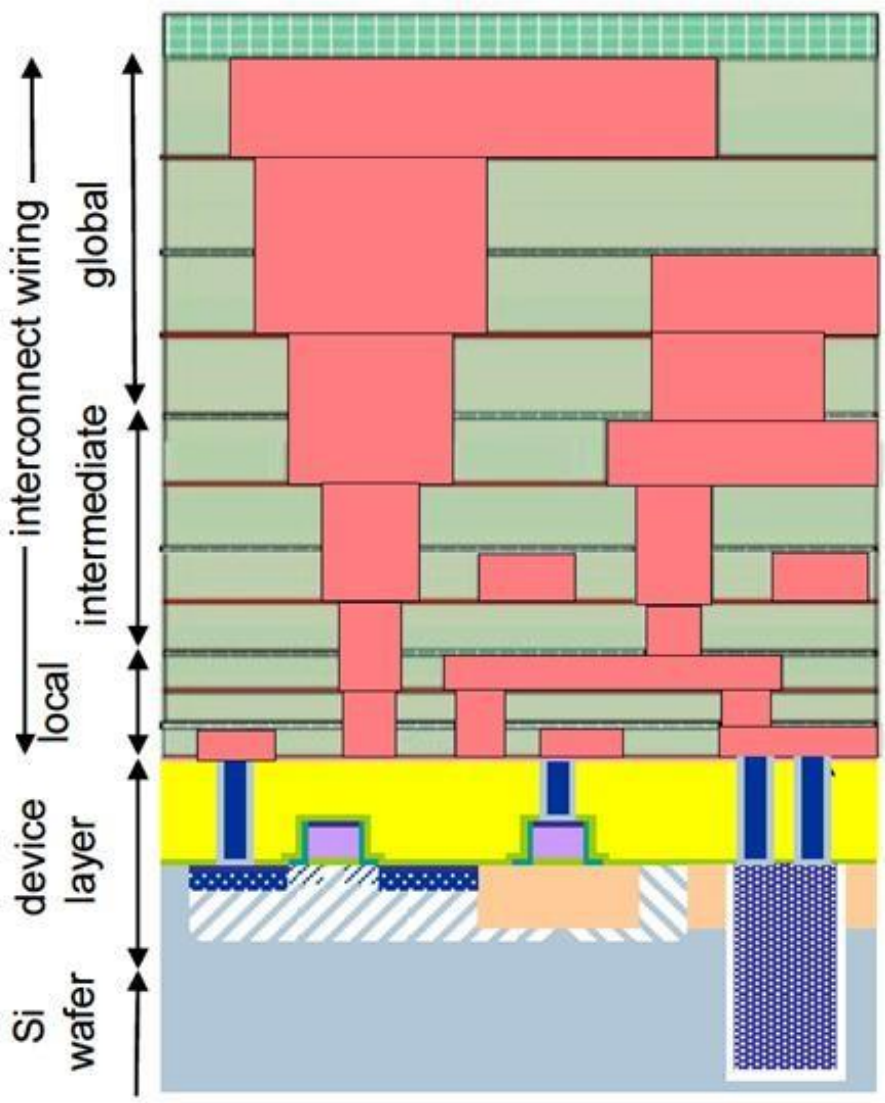


Figure 1.2 Cross-sectional structure of MOS showing interconnect levels [15]

The cross-sectional structure shows several active devices connected through the VLSI interconnect layers [15].

Local interconnects are the first level interconnects. These are obtained at the length ranging in few micrometers to tens of micrometers [15–25]. Such interconnects connect the gate, source, and drain in an MOS technology. Local interconnects have higher resistance in comparison to global interconnects because they are utilized for small length and cross-sectional dimensions.

Intermediate interconnects are advantageous over local interconnects because of its lower resistance. Such interconnects are also termed as semi-global interconnects. They cover both small as well as long length having range between 20μm to 400μm [26–27]. These are used to link devices within a block.

Global interconnects are generally lengthy interconnects having length greater than 500μm. They often cover a large distance between devices [27–28]. The global interconnects are used to distribute power and connect the various functional blocks including ground, and clock [25]. To understand the performance of interconnects, power dissipation and signal delay are the key parameters of global interconnects.

1.2 Significance of Nano-Scale Reign

Efficient packaging of CMOS transistors and the interconnections between them are significant challenges in the manufacturing of VLSI ICs. With the growing demand for packaging, obtaining a high performance is crucial. Scaling process in VLSI circuits minimizes the feature size of the device to a sub-micrometer level depending on the technology parameters while the geometric ratios are maintained. Scaling is categorized in two parts, i.e., device scaling and interconnect scaling. In device scaling, dimensions of the CMOS transistors are reduced as nodes of technology are downscaled. With downscaled dimensions of active devices, interconnects dimensions should be downscaled [15–16]. The scaling of interconnects from the cross-sectional and length aspects is shown in Figures 1.3(a) and (b). The interconnects are weighed as S1, S2, and S3, which represent different scaling factors. To evaluate the performance of the ICs, the scaling effect on the interconnects should be reviewed. The performance of local interconnects does not affected with downscaling as the overall performance depends on the device parameters. The global interconnects have large parasitic parameters, which affect the functioning of the IC.

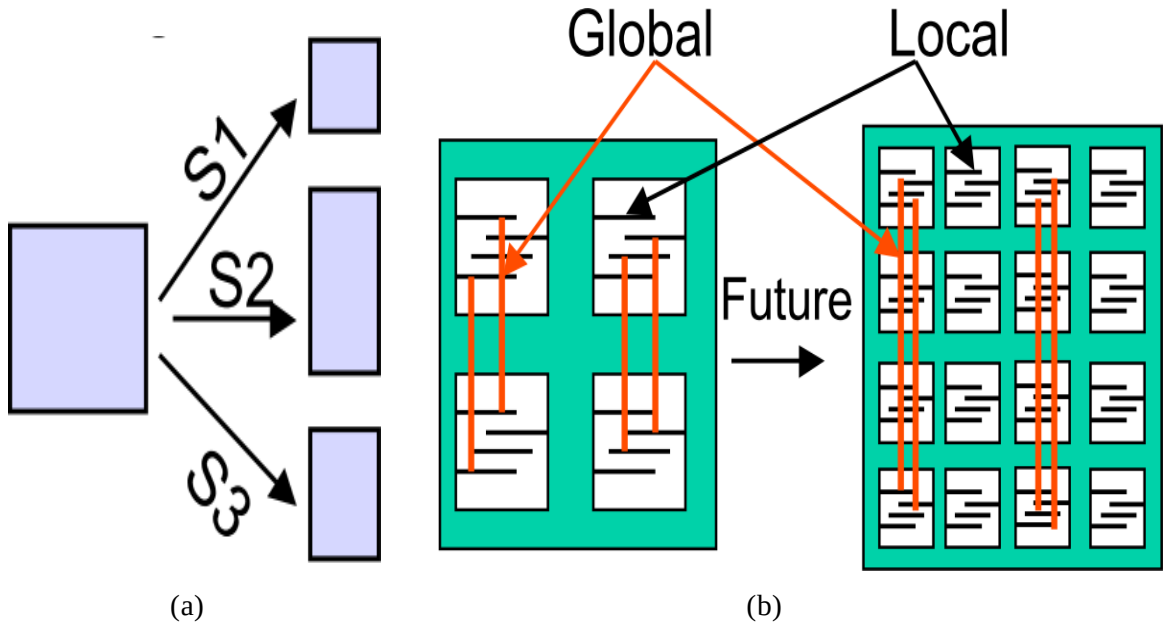


Figure 1.3 (a) Wire cross-section of interconnects (b) IC corresponding to scaling of wire length [15, 16]

In global interconnects, if scaling is performed by a factor 1/S, then the delay time increases by $S^2.S_c^2$, where S_c is the scaling factor of the chip size [3, 4, 29].

1.3 Importance of Repeaters

As discussed in section 1.2, the advancement in VLSI technology led to the miniaturization of chip size. The parasitic parameters of local interconnects are very small than a driver, i.e., transistor parasitic. The parasitic parameters of interconnects raises linearly with increasing interconnect lengths, thus, affecting the performance parameters of interconnects with respect to the power, delay, and PDP (Power Delay Product). Delay in

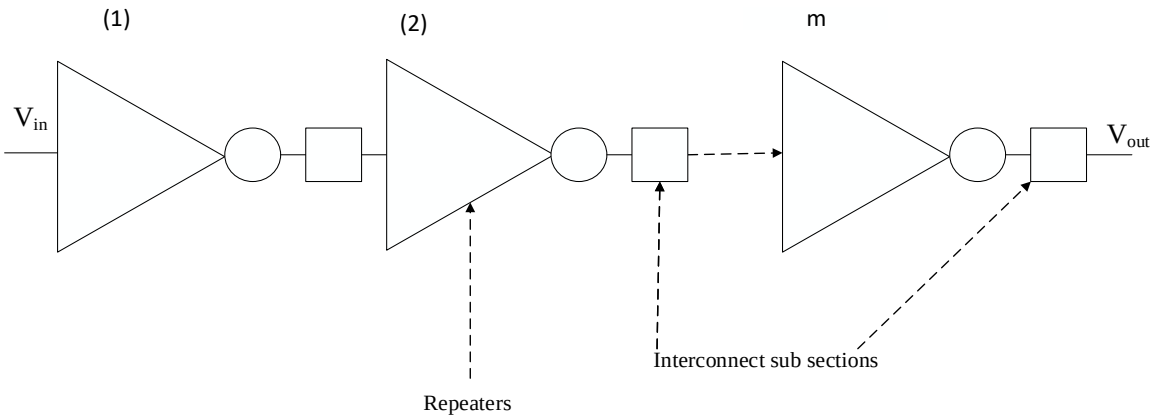


Figure 1.4 Lumped interconnect divided into subsections with optimum number of repeaters (m)

interconnects becomes larger than that of the drivers at global levels. Therefore, repeaters are proposed in between the long interconnects to reduce the delay [3, 30–33]. Figure 1.4 shows an interconnect that is divided into small subsections driven by CMOS inverters called as repeaters [34]. The signal delay is the time constant (RC) of interconnect. The downscaling of technological nodes decreases the conductivity of integrated circuits, which further increases the delay in signals. Thus, to enhance the performance of interconnects at global lengths, optimum number of repeaters with optimum size should be deployed at regular intervals [3, 30–32, 34–43].

1.4 Interconnect Models

The connection between the active devices in an IC through interconnect wires behaves as a transmission line. A circuit model exists for every transmission line, which has parasitic parameters. The actual performance of circuit model is evaluated through its parasitic parameters [44]. The circuit models can be simple or complex but depend on the arrangement of the structure.

1.4.1 Lumped Model

It is an interconnect model that consists of parasitic parameters (resistance, inductance, and capacitance). The different configurations of lumped models are shown in Figure 1.5. Further,

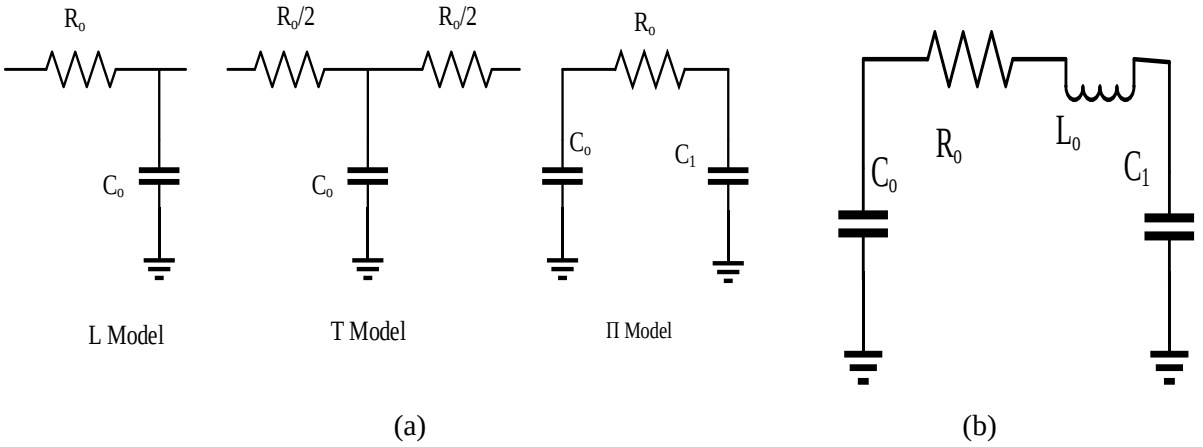


Figure 1.5 (a) Different lumped RC interconnect circuit models (b) RLC lumped model

these modes are categorized into L-shaped, T-shaped, and Π-shaped depending on the probability that they are connected or laid out [45]. In recent studies, RLC circuit models were preferred over RC models because of their better performance. Figure 1.5 (a) shows three different lumped circuit models, i.e., L, T, and Π shaped.

1.4.2 Distributed Model

The distributed model comprised of sub-sections of lumped models, as shown in Figure 1.6

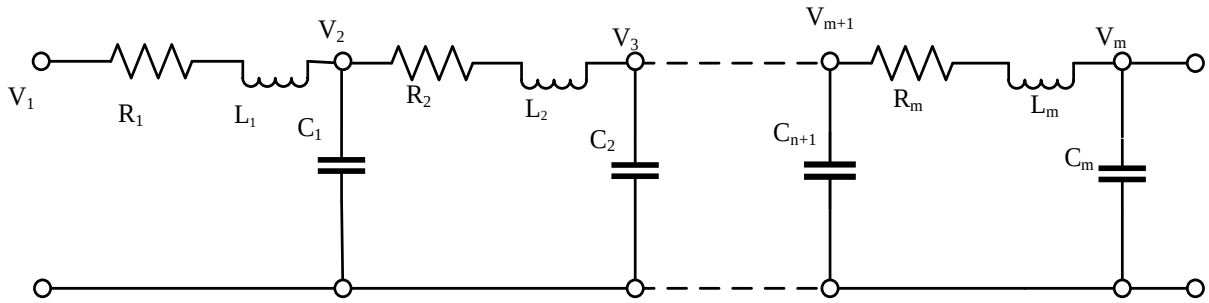


Figure 1.6 Distributed model (RLC with m segments)

Repeaters are inserted to drive subsections of long distributed models. This model increases the driving capacity and reduces the overall delay of longer interconnects. The optimum size with optimum number of repeaters are considered for the simulations at different nodes of technology [46-53].

1.5 Aluminum and Copper as Interconnects

Aluminum material was used in previous studies as an interconnect in silicon ICs because of the following properties:

- Low resistivity
- Good Conductivity
- Ease of deposition
- Dry etching
- Does not contaminate Si
- Excellent adhesion to dielectrics

It also forms good ohmic contact with silicon. Despite the numerous advantages, it has a few disadvantages:

- Electro-migration
- Hillocks (shorts between levels)
- Higher scattering
- Short mean free path

With the downscaling of technological nodes [24, 54], the interconnect current density increases. At high current densities, electro-migration occurs (it is the transport of material performed by the progressive development of the particles in a conduit because of the energy exchange between directing electrons and directing metal molecules). Further, the resistivity of aluminum is 2.7μΩcm, which is very high in comparison with 1.7μΩcm of the copper resistivity. Hence, aluminum as interconnect at micro-scaled technological

nodes cannot produce higher current density owing to its high resistivity and electromigration [6, 18, 55–58].

At such a stage, a better interconnect was required. Therefore, copper was considered as an interconnect owing to its higher conductivity and is further contrary to electro-migration than aluminum [59]. The comparison of various copper properties with similar types of conducting elements as depicted in Table 1.1.

Table 1.1 Properties comparison of various conducting materials [24]

Properties / Materials	**Copper (Cu)**	**Aluminum (Al)**	**Gold (Au)**	**Silver (Ag)**	**Tungsten (W)**
Resistivity (μΩ-cm)	1.7	2.7	2.35	1.6	5.65
Melting Point (K)	1357	933	1264	1062	3387
Corrosion in Air	Poor	Good	Excellent	Poor	Good
Adhesion to SiO_2	Poor	Good	Poor	Poor	Poor

It is concluded from Table 1.1 that copper was appropriate as VLSI interconnect owing to its high melting point and less resistivity among other conducting materials at micro-scaled technological nodes. Although, technologies downscales to less than 45nm, copper resistance along the cross-sectional dimensions increases sharply due to the small MFP (Mean Free Path) of electrons and stuffy effects such as the boundary scattering of the surface and grain, resulting in an increasing electro-migration and decreasing current density issues [18, 46, 60]. The difficulty in increasing resistance of copper as an interconnect is challenging at the global level interconnects. Hence, an alternative and potential fabrication material is required to improve the performance of the VLSI circuits [61–68].

Carbon nanomaterials are emerging as a suitable interconnect material at global lengths as an alternative to copper interconnects [60, 69–71].

1.6 Graphene Nanoribbon as Interconnects

Recently, the nanomaterials made from carbon are proposed as on-chip interconnects in VLSI used for developing ICs for nano-scaled technological nodes [16, 24, 72–73]. Earlier, copper was employed as interconnect for global, intermediate, and local levels. With the development of technological nodes, it becomes essential to rise the current density and reducing the dimensions of cross-sectional area of the interconnects. As discussed, stuffy effects like the boundary scattering of surface and grain in the copper [60, 64, 74] results in increasing electro-migration, & resistivity; and reduces the current-density. Therefore, a suitable interconnect material is required to be used as interconnect to reduce the issues corresponding with copper. Further, the nano-materials made from carbon exhibits a significant effect similar to that of the in VLSI interconnects owing to its thermal, electrical as well as mechanical aspects [60, 75–77]. Nanomaterials like, Carbon Nano Tube (CNT) and Graphene Nano Ribbon (GNR), are resulted to be better alternatives other than using copper, for the nano-scaled nodes of technology. Since last many years, CNTs are tested well and different parameters of modeling has also been presented in the studies [28, 52, 78–82]. "Multi-Wall Carbon Nanotubes" (MWCNTs) and "Single-Wall Carbon Nanotubes" (SWCNTs) are the two sets of CNTs, with well researched electrical capabilities [28, 79]. CNT interconnects depict a smaller delay in signal than that of the copper used in applications of VLSI [52]. In addition to this, the effect of cross-talk and the tedious processes of development are the main issues reported in MWCNTs and SWCNTs [83–84].

Table 1.2 lists the properties of GNRs, MWCNT, SWCNT, and copper corresponding to interconnect applications.

Table 1.2 Comparison of GNR, SWCNT, MWCNT, and Copper [85]

Properties	GNR	SWCNT	MWCNT	Copper
Mean free path(nm) @ room temp.	>1000	1000	$2.5X10^4$	40
Max current density(A/cm^2)	$>10^8$	10^{10}	10^{10}	$\sim10^7$
Thermal conductivity($\times10^3$ W/mK)	3-5	1.75-5.8	3	0.385
Melting point(K)	3800(graphite)			1357

Table 1.2 shows that the GNR and CNTs are better than copper with respect to the MFP, maximum current density, and thermal conductivity. Graphene sheets are also known to be

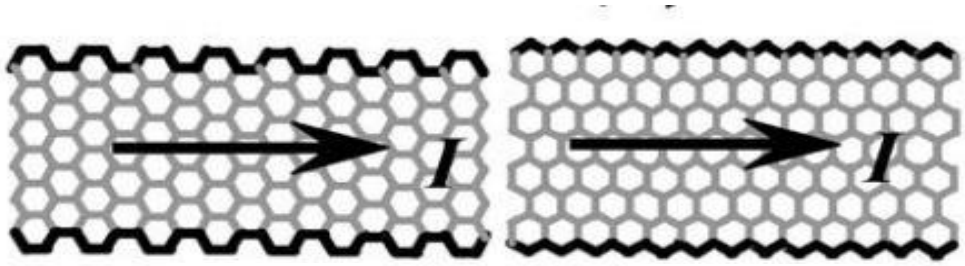
the unfolded type of Carbon Nanotube. The Graphene nanoribbons are acquired by sorting the graphene made from a thin carbon atom sheet and is used for structuring CNTs [60, 85]. It also shows same types of characteristics as that of a CNT, although its process of fabrication is much easier than that of the CNTs [85, 86, 87]. Graphene is considered as an emerging and alternative material for replacing copper in VLSI interconnect [86–92].

1.7 Classification of GNRs

GNRs are classified into various types with respect to its chirality, lattice structures, and conductivity.

1.7.1 Fundamental Physics

As per its chirality, the Graphene Nanoribbons are classified into two types: (1) zz-GNRs (zigzag-edged); (2) ac-GNRs (Armchair-edged). The arm-chaired Graphene Nanoribbon can be semi-conducting or metallic according to (N) number of hexagonal rings present across its width [69],



ac- edge zz- edge

(a) (b)

Figure 1.7 Schematic interpretation of (a) ac-GNR (b) zz-GNR [85]

that is it shows metallic features with $N = 3p - 1$ and semi-conducting with $N = 3p$ or $3p + 1$, where p is an integer showing specular features of the edges of GNR (Figure 1.7(a)). When compared with the arm-chaired, the zig-zag edge GNR are observed to be independent of N and metallic in nature (Figure 1.7(b)).

1.7.2 According to Structure and Conductivity

GNRs can be classified according to the number of layers [93–95]:

(a) Single-layer and

(b) Multi-layer

Single-layer graphene nanoribbons (SLGNRs) consist of a single sheet of graphene. Figure 1.8(a) shows a single layer GNR, which is located at d distance from the level of ground. The SLGNR structure helps to construct MLGNR interconnect.

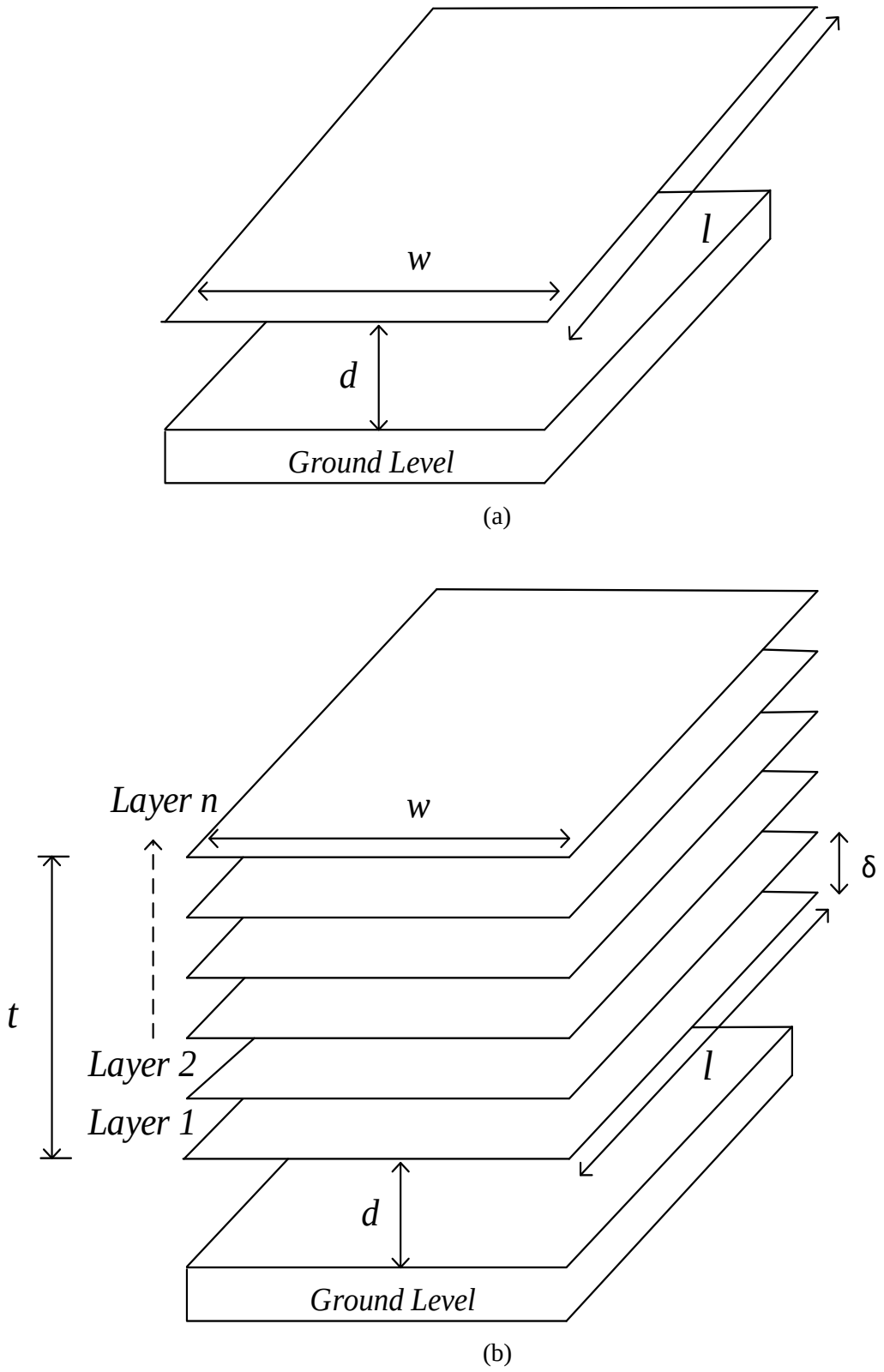


Figure 1.8 Interconnect structures (a) SLGNR and (b) MLGNR

The MLGNR structure is derived by stacking layers of GNR in a parallel combination, as shown in Figure 1.8(b). As per the compact physical circuit model of GNRs as interconnects, MLGNR has lower resistance than the SLGNR [96].

Hence, MLGNR is presented as substitute and appropriate material for this research to show higher performance at global levels in VLSI interconnects.

1.8 Influence of Fermi energy and Temperature on MLGNR

A neutral type MLGNR cannot have better performance than the copper material. Where, its performance can be enhanced by using compounds like the AsF_5 (Arsenic Pentafluoride) as the doping material [85]. Intercalation is the process of doping or mixing metal atoms into the layers of MLGNR. From the intercalation process, conductivity of every layer of MLGNR can be improved by several times. Intercalation helps in increasing E_f (Fermi Energy) by increasing the space among the adjacent layers of GNR, results in the increase in carrier density because of the charge transfer and thereby reduces screening effects and bandgap [85]. Hence, doping with metallic carrier concentration compounds results in higher conductivity of MLGNR, and for understanding the performance of MLGNR (doped) as interconnect, its effect is required to be estimated.

With the downscaling of technological nodes, effect of variable temperatures on interconnect is also major challenge in designing next generation VLSI ICs. In CNT interconnects, the MFP is affected notably because of the temperature variations, that has a direct influence on the impedance parameters [34, 97–103]. Hence, the temperature variations above the room temperature has a direct impact on the functioning of interconnects at nano-scaled nodes of technology. The effect of temperature on the functioning of MLGNR as interconnect is required to be evaluated for analyzing its actual performance under variable thermal conditions. Few researches have analyzed the effects of temperature on power dissipation and delay. Although, the performance of MLGNR was not yet estimated for 32nm, 22nm, and 16nm nodes of technology from power-delay product perspective at global lengths [104–107].

The present study proposes the effect of temperature and Fermi energy variation on impedance parameters of the MLGNR. Further, the proposed Fermi energy and temperature-dependent impedance models are used for evaluating the performance of MLGNR with respect to the power dissipation, signal delay, and PDP at global lengths for 32nm, 22nm, and 16nm nodes of technology using simulation set up through CMOS inverter. To perform the comparative analysis, the influence of temperature on copper and SWCNT is presented for global levels and comparing the results with MLGNR interconnects.

1.9 Motivation

The Moore law for scaling of technological nodes has led to the major advancement in chip design and functionality. With the downscaling of technological nodes, the efficiency of gate becomes insignificant compared to the interconnect performance. The reliability issue

play a major role at nano-scaled technological nodes since future interconnects requires higher current density with compact cross-sectional dimensions. Formerly, copper was employed as interconnect due to high current density and less resistivity but as technology downscales below 45nm its resistance increases due to the reduction of MFP. The scaling of interconnect dimensions effects the delay time as well as power dissipation. The electronics circuit operational speed is affected by the signal delay at the output of wire. The power dissipation is also a key factor in VLSI ICs. In today's world, everyone demands higher power standby and speed in electronic circuits. The motivation for minimizing delay in signal and power dissipation at global lengths for various technological nodes varies according to applications. The overall performance of electronic circuit depends on the product of power dissipation and delay. Both are independent parameters but to estimate actual performance of an interconnect their product must be taken into account for elite integrated circuits. This research work has proposed MLGNR as suitable and alternative material in on-chip interconnects for future technological nodes compared to copper interconnects. It is reported in literature [85] that the neutral MLGNR has no ability to perform superior than copper thereby the concept of intercalation doping has been proposed. The intercalation rises the levels of Fermi energy and improves the conductivity of MLGNR. The performance analysis dependent on Fermi energy of MLGNR in delay and PDP terms has been analyzed from 500–2000μm length for 16nm, 22nm, and 32nm technological nodes. Further, the temperature effect on the performance of interconnects is also a foremost task for fabricating next generation ICs. Therefore, its effect on the functioning of MLGNR is required to be evaluated and analyzed in power, delay and PDP terms at long length for all three technological nodes. Moreover, the combined impact of temperature and Fermi energy on the MLGNR performance is examined. In addition, performance and comparative analysis of MLGNR with copper and SWCNT interconnects is carried out at global length of various technological nodes (16nm, 22nm, and 32nm) and observed that MLGNR performance is superior than copper and SWCNT interconnects from delay and PDP perspectives. Hence, MLGNR becomes an appropriate and alternate material as interconnect for nano-electronic IC fabrication in thermally variable conditions.

1.10 Main Contributions of Research Work

The main contributions of this research work are as follows:

- An analytical model is developed to analyze the effect of temperature and Fermi energy on the performance of MLGNR interconnects.
- The circuit modeling of multi-layer GNR is proposed and intercalation doping impact

on the parasitic parameters of MLGNR is analyzed. Further, influence of intercalation doping on the MLGNR performance is examined with respect to the delay and PDP at 16nm, 22nm, 32nm technological nodes from 500–2000μm interconnect lengths and comparison with copper interconnects is carried with equal length and technological nodes.

- The influence of temperature on the effective MFP that primarily relies on the scattering mechanism of electron-phonon and its impact on the parasitic parameters (resistance, inductance, and capacitance) of multilayer GNR is derived.
- The impedance and performance analysis of MLGNR dependent on temperature are explored at global lengths for three different technological nodes.
- Analytical delay model (temperature dependent) for MLGNR is proposed and its stability analysis is executed from 500–2000μm length for three different technological nodes.
- The impedance models for copper and SWCNT interconnects dependent on temperature are presented.
- Finally, comparison analysis (temperature dependent) of MLGNR with copper and SWCNT interconnects is also presented at global lengths for all three technological nodes.

1.11 Organization of Thesis

The work presented in this thesis through seven chapters and a brief outline of all chapters is as follows:

Chapter 1 introduces the familiarization of VLSI interconnects. It follows with the overview of conventional interconnects, such as aluminum and copper, including their advantages and disadvantages. The necessity of graphene nanoribbons as an interconnect and its fundamental physics are discussed. The effect of Fermi energy and temperature on the performance of MLGNR is discussed to evaluate the delay in propagation, power dissipation, and PDP for global level interconnects. Further, chapter-wise details of the thesis organization are presented.

Chapter 2 presents the comprehensive study of previous work on the issues related to GNR and significance of the present work. It explores the VLSI interconnects, aluminum, and copper interconnects, requirement for GNR as interconnect, advantages of SLGNR and MLGNR as interconnects. The shortcomings in copper interconnect at nano-scaled nodes of technology are highlighted in the literature survey. The requirement for the GNR as interconnect with the

downscaling in technological nodes is presented. It covers the existing results of SWCNT to understand its relevance as alternative interconnects at local levels. Moreover, the literature presented in the study corresponds to MLGNR at global levels. Finally, thermally aware modeling of copper and SWCNT interconnects is presented. The performance of elite ICs is influenced under variable thermal conditions. The ICs execute the tasks differently at different temperature extending in the range 200–500K for diverse areas of application. Studies show that MLGNR can be used as an alternative material but no study reports the temperature effect on the performance of MLGNR as an interconnect. A few reports have introduced the impact of temperature on the mechanism of scattering for copper, MWCNT, and SWCNT as interconnects at local levels (<100 μm). Certain gaps in literature are observed after a critical analysis. Thus, the objectives and methodology of the current work has been formulated. Study reported in the present thesis includes the effect of temperature and Fermi energy level variation on impedance parameters of the MLGNR. Further, evaluates the performance of MLGNR with respect to the power dissipation, propagation delay and PDP for global level interconnects.

Chapter 3 investigates the circuit modeling of multi-layer GNR. The equivalent circuit model of MLGNR with its parasitic parameters is presented. The impact of variation in Fermi-energy on the number of conduction channels is analyzed at 32nm, 22nm, and 16nm nodes of technology. On the basis of an electrical model, the influence of intercalation doping on MLGNR interconnect with respect to delay in signal and PDP as performance parameters at three different nodes of technology is discussed. In addition to this, the comparative analysis with copper interconnect is performed and the results show that the intercalation doped MLGNR have better results for all three nodes of technology at global levels.

Chapter 4 explores the impact of temperature and presents a detailed thermally-aware equivalent circuit transmission model to calculate the effective MFP that primarily relies on the scattering mechanism of electron-phonon and its impact on the parasitic parameters (resistance, inductance, and capacitance) of multilayer GNR. From the mathematical equations, the temperature-dependent effective MFP of SLGNR is calculated for the temperature ranging in 200–500K. Further, impedance and performance analysis of MLGNR (temperature-dependent) with respect to signal delay and PDP at global levels for all three various nodes of technology is presented.

Chapter 5 presents the analytical delay model of MLGNR interconnects dependent on temperature. The outcomes acquired from analytical delay model are compared with the simulation results presented in chapter 4. The simulation and analytical results show that the outcomes of the two models correspond well. The trend of the models shows the increase in

delay with the rising temperature levels (200–500K) for 32nm, 22nm, and 16nm nodes of technology. Relative stability of MLGNR is analyzed from 500–2000μm length with respect to switching delay and observed that with increasing interconnect length switching delay increases as a result input signal damp faster which upswings the relative stability of MLGNR for all three various technological nodes. Moreover, relative stability is also analyzed at length 2000μm and temperature 500K of MLGNR through Nyquist plots and observed that the system will achieve stability faster as we move from 32nm to 16nm technological node due to higher values of parasitic because of the reduction in MFP of electrons.

Chapter 6 presents the combined impact of temperature and Fermi energy on the performance of MLGNR at global interconnects for three different nodes of technology. The impedance models dependent on temperature of copper and SWCNT interconnects are also presented. Further, performance and comparison analysis (temperature-dependent) of MLGNR with copper and SWCNT interconnects is conducted for equal length and technological nodes and the results confer that the MLGNR performance is better in the proposed temperature range (200–500K).

Chapter 7 outlines the main findings and presents the scope for future work.

CHAPTER 2

LITERATURE REVIEW

This chapter assesses various papers that have been reviewed to understand the suitability of graphene nanoribbon as interconnects for VLSI circuits and provides the background information corresponding to the present study. It presents the studies that are based on delay models of VLSI integrated circuits. The study related to copper and SWCNT interconnects corresponding to their thermally aware analytical modeling is presented.

2.1 Introduction

With the scaling of technology nodes, interconnect current density increases. At high current densities electro-migration (it is the transport of material performed by the progressive development of the particles in a conduit because of the energy exchange between directing electrons and directing metal molecules) occurs. As the technology is downscaled, the chip size increases and device dimensions of VLSI IC decreases [18, 19]. The characteristics of interconnect play an important role at deep sub-micron technological nodes. The performance of different interconnects has been reported in the literature in terms of delay. The role of repeaters with variable sizes and numbers are discussed in the literature to minimize the impact of parasitic parameters that affect the delay at global level interconnects [30, 32, 35]. The performance of copper decreases with the downscaling of technological nodes, and the CNTs as an alternative material is reported in literature. The work corresponding to CNT as interconnect has been discussed and various analytical models are presented to analyze the performance from delay perspective. The performance of SWCNT is compared with copper at local lengths for different nodes of technology. It is reported in literature that SWCNT is better than copper material as interconnect in terms of delay, but crosstalk as a major issue has been reported in CNTs. The GNRs exhibit large MFP, lesser resistance, and ease of fabrication, which makes it a suitable material at global levels for different nodes of technologies. To analyze the accurate performance of interconnect, thermal conditions should be considered in nano-scaled technology nodes. The various temperature-dependent analytical models are presented for copper and SWCNT interconnects. Studies reported in literature focused on the performance of graphene nanoribbons, SWCNT, and copper materials as interconnects and impact of temperature on the performance of copper and SWCNT in delay; power dissipation

terms [62, 64, 108, 109, 110].

2.2 Interconnect Delay Models

The transmission analysis of interconnects plays a significance role similar on drivers in ICs. The performance of interconnects relies on the delay as well as power dissipation parameters, hence, different delay models have been presented in the literature with their mathematical expressions.

N. Srivastava *et al.* [2] reported the importance of interconnect wires to drive the transistor. The paper discusses the drawbacks of copper material with downscaling of technological nodes. Signal delay in copper interconnects as technologies downscales below 45nm is presented. The current carrying capability of copper interconnect is discussed and compared with the rising demand of carbon nanomaterials, such as carbon nanotubes.

H. B. Bakoglu *et al.* [4] presented the signal delay as a performance parameter to determine the performance of interconnects. A time delay interconnect model was reported. The RC time delay of interconnect lines increases rapidly as chip size increases and device dimensions decrease. The delay of different materials, such as aluminum, polysilicon, and WSi_2 are compared. The role of cascaded repeaters for long interconnects in reducing the signal delay has been discussed in the paper.

L. W. Schaper *et al.* [6] displayed the impression of emerging MOS technology in comparison with bipolar technologies. The paper highlights the advantages of CMOS technology with respect to its power consumption and thermal stability. The performance of MOS devices are much better than the bipolar. The future challenges in MOS technology are focused.

T. Sakurai *et al.* [7] evaluated the delay and voltage waveforms for RC line. Using boundary conditions, a closed formula for RC line is derived. Equations for the voltage drop and transition time of RC distributed line are derived. The coupling capacitance and crosstalk between the parallel distributed lines is proposed. It is estimated that the error from the proposed capacitance coupling in between two lines is 15% lesser for practical range of parameters. Using the equation, optimum width can be calculated by minimizing RC delay. The trend scaling of technology nodes is discussed and its impact on future trend of RC delay is presented. Expressions are presented to estimate the leakage capacitance and crosstalk between the parallel lines of VLSI circuits.

A. B. Kahng *et al.* [8] gives a new and simple technique for modeling RC and RLC load interconnects. The inductance effect while developing delay analytical model for RC and RLC interconnects is presented. The outcomes of their developed delay analytical model estimated 25% of the SPICE delays, while the variation in Elmore delay is estimated as 50% than the

SPICE calculated delay. They reported that when π model is used, delay accuracy is 3% better for RLC model, which the L model achieves in 100 segments. Hence, π model is frequently used in SPICE simulations than the L model with several segments to achieve the approximation of distributed parasitic line.

A. Deutsch *et al.* [11] reported the performance of silicon nanowires for global, semi-global, and local interconnects based on the analytical model using technology dependent parameters. The paper proposed analytical model to evaluate the capacitive and inductive couplings for semi-global levels. The analytical expressions are presented for evaluating the parasitic. Moreover, transmission performance of interconnects with respect to the delay and crosstalk for global, intermediate, and local level lengths at different technological nodes is calculated.

J. S. Roychowdhury *et al.* [14] investigated a new technique, i.e., time variant of lossy transmission medium for simulations. The impulse analytical form is used for this technique. The objective of the technique is to include the information of line in the mathematical solution of Telegraphic equations. The impulse analytic form overcomes the limitations of the numerical inversion method and applies the existing convolution methods. The numerical convolution has been presented for Trapezoidal and Euler methods to employ the impulse analytical form. Furthermore, the convolution using analytical responses is observed to be better than the accuracy of lumped (RC) procedures.

K. C. Saraswat *et al.* [18] presented the effect of scaling with increase in chip size and decrease in cross-sectional dimensions on the delay of VLSI integrated circuits. Analytical modeling is presented to relate the various parameters of technology node to calculate the signal delay of interconnects. The materials whose signal delay is calculated are poly-Si, WSi_2, W, and Al. It is concluded that with the scaling of dimensions in technology nodes, the delay increases.

K. Banerjee *et al.* [35] addressed the issue of power dissipation during buffer insertion in interconnects. The signal delay is very shallow in optimizing repeater size. Therefore, new methodology has been presented for computing the size of the repeater and inter repeater length of interconnect for minimizing power dissipation. As per this methodology, power optical buffering was computed for different technology nodes. Further, this technique is useful to minimize power dissipation for different technology nodes using power optimal solutions.

Y. Ismail and E. G. Friedman [42] proposed the impact of inductance to evaluate interconnect performance with respect to the propagation delay. As the industry is downscaling the increase in chip size and decrease in dimensions, the effect of inductance on the speed of VLSI circuits is presented. To calculate the propagation delay, a closed form equation is developed for CMOS gate using RLC line. It has been investigated that neglecting the inductance in RLC line

causes the percentage error in signal delay to be 35% more than the on-chip VLSI interconnect. They analyzed that the percentage increase in delay is more than 30% considering repeaters in RC line than that of the RLC models. Therefore, the results revealed that impact of inductance has a major role in computing signal delay with scaling of technology nodes.

F. Shi *et al.* [45] expressed the crosstalk between adjacent interconnects with fast growing scaling of nano-scaled technology nodes. The crosstalk is a major challenge to system performance at global interconnects. The introduction of delay model in the study has proved that its accuracy is better than that of the reported delay models in literature.

M. S. Sarto *et al.* [52] proposed a single conductor equivalent model for SWCNT to estimate the signal delay and wave shape, which was later extended to MWCNT bundle interconnects. The mathematical model is presented to convert an equivalent circuit of MWCNT bundle in a single conductor transmission line. The optimum number of repeaters with optimum repeater size is proposed in the study.

2.3 GNR as Interconnect

The conventional aluminum and copper were used as interconnects at the global, intermediate, and local levels. However, with the decrease in cross-sectional dimensions and increase in technology nodes, studies have reported various disadvantages of these materials. The carbon nanomaterials, such as CNT and GNR, are better alternatives to replace copper as interconnects. The CNTs are tested and various parameters of modeling are reported. CNTs have smaller signal delay than that of the copper interconnect. The crosstalk effect and tedious processes of development are the major issues of the CNTs. Graphene has same kind of properties as the CNTs, but its fabrication is easier, and various studies show the GNR as an outstanding interconnect material.

Xu *et al.* [69] presented the conductance and delay study of graphene nanoribbon interconnect. The simple tight binding and Landauer formula has been used to derive conductance model. The conductance is calculated for various structures of GNR and compared with copper, tungsten, and CNT materials. The impact of variation of Fermi level, edge specularity, and mean free path on the conductance of GNR is examined. The equivalent circuit model of GNR is presented to calculate delay at local and global levels.

A. Maffucci and G. Miano [70] suggested circuits comprising nanowire for future VLSI devices. Propagation of signal in nanoscale wires can be concentrated by consolidating Boltzmann transport hypothesis. The study implements the method to model the propagation of signal in GNR interconnects. They expressed the quantum capacitance and kinetic inductance regarding the quantity of viable channels (conducting) for both zig-zag and

armchair GNRs with varying width.

R. Murali *et al.* [71] presented GNR material as interconnect and its resistivity is contrasted with copper. The normal resistivity reported is approximately three times than that of the copper wire having width (18nm<W<52nm), although the resistivity of best GNR is equal to that of the copper. The conductivity is observed to be affected by electron scattering and edge roughness scattering. Accordingly, the resistivity of GNR with specular edges is three times the minimum limit forced by substrate phonon dispersing. The quality graphene nanoribbons can possibly overcome that of the copper for its use as in chip interconnects.

A. A. Balandin *et al.* [75] investigated the suspended single layer graphene. It has been analyzed that graphene is better than CNT at high operating thermal environment. The thermal conductivity values of graphene are extracted from Raman G peak frequency using excitation laser power and temperature coefficient of G peak frequency. The thermal stability of graphene is suitable for electronic applications and temperature management.

Chuan Xu *et al.* [85] discussed GNR-based interconnect for future VLSI interconnect, and derived the conductance and RLC model of GNR. They used the Landauer formula to estimate the GNR conductance. GNR conductance is further compared with various interconnect materials like copper, CNT, and tungsten. The intercalation doping in GNR and its effects are presented. Similar to other materials, GNR has drawbacks, such as edge scattering phenomenon. The layering of GNR reduces its conductivity due to current leakage, but as they doped MLGNR, its conductivity was marked up by 100 times. This doping is conducted by placing one dopant layer among adjacent graphene layers. As a result, it increases the current density because of an increase in charge carriers and mean free path. GNR strengthens as interconnect is calculated on the basis of delay, which is compared with the copper interconnect.

W. Choi *et al.* [87] presented the detailed study of graphene and its physical properties. It has been reported that the graphene is the future interconnect material owing to its optoelectronic properties. The study aims to prove graphene as an outstanding interconnect material in future research guidelines. It is reported that graphene can be employed as a sensor in electronics and emission processes.

A. Maffucci and G. Miano, [90] presented the transmission line model of graphene nanoribbon to understand its electromagnetic behavior. Using tight binding model, GNR electrodynamics is described using linearized Boltzmann equation. The parasitic parameters (resistance, inductance, and capacitance) are used to describe the transmission line model of GNR. Besides these parameters, two new terms, i.e., kinetic inductance and quantum

capacitance were introduced. They are influenced by the number of conduction channels, which represents the number of sub-bands in neighboring nanoribbons. The Fermi energy causes the electrical conduction in GNR as transmission line. The various properties of GNR are examined and discussed. The influence of contact resistance on the lumped resistance was presented. Further, it has been examined that the impact of kinetic inductance is predominant than that of the magnetic inductance, whereas the electrostatic and quantum capacitance impact are almost equal and negligible in transmission line.

A. Maffucci and G. Miano, [91] presented electrodynamical model of graphene nanoribbon to describe behavior of electrical signal propagation using modified Boltzmann equation. The derived model is operated in conventional conditions to predict the possibility of graphene as interconnect. The conductivity of graphene is studied with reference to 2D and 1D nanomaterials. The various modulation effects of graphene nanoribbons in terms of size, chirality, and width are analyzed. Further, in case of 2D nanoribbons, spatial dispersion has been reported.

A. Naeemi and J. D. Meindl [94] explained the GNR conductance and conductance model considering Fermi energy, chirality, width, and scattering phenomenon. Below 8 nm, GNR resistance is smaller than that of copper. Hence, metallic GNRs can perform better than copper at 8nm at different aspect ratios. GNRs with width greater than 100nm can enlarge the Fermi energy upturn conductance, which is not possible with smaller widths. GNR contact resistance is not considered in this paper because of lack of data.

J. D. Meindl and A. Naeemi [96] presented circuit model for armchair and zig-zag graphene nanoribbons and benchmarked their conductance counter to carbon nanotubes and copper interconnects. They reported that thick GNRs have less resistance with unit aspect ratio than that of copper below 8-nm width. The stacked layers of graphene have less resistivity than the copper material. Further, it is concluded that rough edges increase the resistance of GNRs, thus, certain methods have to be adopted to fabricate nanoribbons with smooth edges to make GNRs highly efficient at nano-scaled technology nodes.

2.4 MLGNR as Interconnect

The multilayer graphene nanoribbons have lower resistance than that of the SWCNT and copper interconnects and larger MFP. Resistance of copper as interconnect increases rapidly below 45nm technology nodes and fabrication of SWCNT is difficult due to its tedious growing processes. The MLGNR is better than copper and SWCNT due to its small resistance, large current carrying capability, and ease of fabrication. Hence, the MLGNR suitable material as

interconnect for next generation VLSI electronic applications. The research is focused on the performance analysis of MLGNR at nano-scaled technology nodes.

S. Rakheja *et al.* [86] explained the significance and challenges faced by interconnects at nano-scaled technology nodes with respect to delay, power dissipation, noise, jitter, and electromigration between adjacent interconnects at local levels as per the "International Technology Roadmap for Semiconductors" (ITRS 2011). The carbon-based 2-D material, i.e., graphene shows tremendous electrical properties, which makes it a suitable material to be implemented as interconnect in electrical and spintronic domains. The analytical models of graphene due to electron transmission mechanism parameters, such as MFP, mobility, and resistivity are explained for 2-D and 1-D for GNRs as a function of edge roughness and Fermi level. The advantages of MLGNR over SLGNR are addressed. They evaluated the current and velocity saturation impact on current density and impurity carrier concentration of graphene phonons and surface polar phonons (SPP) on polar substrates. Moreover, the results presented in the paper revealed that the graphene nanoribbons as interconnects are better than copper material in electrical and spintronic domains.

M. Politou, *et al.* [89] explored the study by discussing the mobility and MFP of GNR while scaling of technology nodes. The stacked layers of graphene show less resistance than single layer of graphene and is considered competitive with current copper as interconnects. The experimental results are very much similar to SPICE simulation. At the end, they highlighted contact resistance to be the key issue in bringing MLGNR as on-chip VLSI interconnect.

S. H. Nasiri, *et al.* [92] presented relative stability of the MLGNR interconnects based on the transmission line theory in collaboration with Nyquist stability charts. It has been analyzed that with increasing either length or width, relative stability of MLGNR increases and system becomes more stable. The rise in the values of parameters of MLGNR the delay increases, which damps the step response of the input and make the system stable.

A. Hazra and S. Basu, [95] presented on-chip VLSI interconnect is the most challenging area at nano-scaled technology nodes. It has been reported that the delay in interconnects becomes more evident to gate delay. The scaling of interconnect dimensions with the increase in technology nodes has significant impact on parasitic parameters and results in increase in resistivity due grain boundary and surface scatterings. The materials like copper (Cu), Al, etc. are severely affected by the scaling of interconnects dimensions. Because of the various electrical properties, graphene becomes suitable material as interconnects. The geometrical structures of armchair and zigzag for single layer and multilayer graphene nanoribbons are presented. The fabrication techniques to implement GNR are discussed. The electrical

parameters of MLGNR are studied with the help of its electrical model. The performance of GNR is calculated from resistance, delay, crosstalk, and relative stability. The performance of GNR was compared with Cu and Al materials. It was concluded that GNR gives better results with respect to all electrical parameters.

W. Y. Yin and W. S. Zhao, [104] reported the equivalent circuit model of MLGNR with its parasitic parameters. The performance with respect to the delay and crosstalk of MLGNR interconnect has been reported for intermediate and global levels at 22nm node. The analytical 50% delay model of MLGNR interconnect is explored. They compared performance of MLGNR with copper interconnect for global level lengths. All interconnect dimensions and simulation parameters used for their calculations and simulation are obtained from ITRS 2010 version.

J. P. Cui, *et al.* [105] presented the propagation of signal characteristics and transient analysis of MLGNR with an ESC model. The analytical modeling of MLGNR is presented using the inductive and capacitive couplings. Based on the transfer function presented in paper, the output waveforms were estimated for 14nm and 22nm nodes of technology, based on the ITRS 2010 version. The effect of Fermi energy on time delay of MLGNR interconnect is calculated. Using PDE (Partial Differential Equations) for differential and common modes of voltage wave-propagation in edge-coupled MLGNR interconnects, their response of output voltage is predicted for different nodes of technology, used in evaluating the signal integrity or EMI and EMC; related issues corresponding to MLGNR built the lines of transmission for the future integrated circuits.

Y. Fang, *et al.* [106] reported the circuit modeling of SLGNR and MLGNR interconnects. The ESC model of graphene nanoribbon is presented with capacitive as well as the inductive couplings among the adjacent layers. Effect of contact resistance on delay in time of the GNR is discussed. The performance analysis with copper interconnect in terms of delay is demonstrated. The authors discussed that MLGNR gives optimal results in comparison to the copper for 14nm & 22nm technological nodes based on ITRS 2010 version.

2.5 Impact of Temperature on SWCNT and Copper Interconnects

The impact of variable thermally aware environment on the performance of high-speed interconnects is presented. Temperature has significant impact on SWCNT and copper. The impact of temperature results in electromigration and scattering mechanism of interconnects, which further hits the interconnect performance from power dissipation and signal delay parameters. As a result, both aspects should be estimated in different thermally active conditions. Only some of existing researches include the effect of temperature in the proposed

interconnects as most studies were limited to local interconnects.

A. Hosseini *et al.* [53] presented thermally active ESC model for single walled carbon nanotube. The temperature-dependent parasitic parameters of SWCNT based on various scattering mechanisms are reported. To estimate the performance of SWCNT, simulation-based platform is demonstrated under variable temperature conditions. The performance parameters, such as delay and power dissipation, of SWCNT is calculated. The results revealed that the delay is reduced by more than 5% for SWCNT than copper interconnect for 27–127 ºC temperature conditions at local level interconnects. Therefore, it is concluded that SWCNT is a reliable and potential material to replace copper for high-performing VLSI ICs of the future.

E. Pop *et al.* [103] presented the thermal & electrical transportation phenomenon in metallic-SWCNT on the insulation substrate, under wide range of bias and temperature conditions. Various temperature-dependent factors are considered while manufacturing.

M. Radosavljevic *et al.* [107] investigated bundles of SWCNT for high-field transport with different contacts. The bundles pass on streams in wealth of 250μA (a present thickness of 109A/cm2) before immersion and breakdown of electrical conduction is commonly through nano tubes on the surface of the bundle, which particularly come through cathodes. They measure the contact resistance by four tests outline, and show that it is enduring as the slant voltage changes. Thus, the electron–phonon diffusing causes current submersion at high field not a contact affect. Electrical breakdown leads to current drops approximately 12μA of metallic nanotubes bundle surface by sequential decimation. Considering a high inclination, the present passing on farthest point of the bundle increases as a result of field-updated coupling among nanotubes in the bundle.

A. Naeemi *et al.* [108] presented the temperature-dependent circuit modeling for single-walled as well as the multi-walled CNTs. The scattering mechanism in SWCNTs and MWCNTs and variation in number of conducting channels due to the impact of temperature is reported. The resistance of the SWCNT and MWCNT increases with increase in temperature at local level interconnects due to the shrinking of MFP.

A. G. Chiarillo *et al.* [109] reported the electrical performance of copper and SWCNT interconnects. The performance of nano-interconnects is affected by size and impact of temperature. It is discussed that the decrease in size and rise in temperature increases the resistance of interconnects, and case studies are presented for 22nm technology nodes.

W. C. Chen *et al.* [110] presented electrothermal description of SWCNT. The impact of variation of temperature on SWCNT is analyzed for low bias and high bias. It is reported that the rise in temperature effects the parasitic parameters, which influences functionality of

SWCNT with respect to the signal delay as performance parameter. Therefore, it is concluded that the impact of temperature should be considered while designing VLSI ICs.

2.6 Research Gaps in Recent Study

From the literature survey, it is presumed that GNR can outperform copper and has the ability to replace copper as an interconnect material. The copper resistance in interconnects increase sharply as the technology nodes scaled down from its mean free path (<45nm).

Recent studies suggested the GNR-based interconnects are an alternative material for the forthcoming IC design because it is much controllable due to its planer nature during implementation. Carbon nanomaterials, such as CNT and GNR, are being studied due to its mechanical, electrical as well as thermal properties. Recently, GNR is studied because it has less resistance than that of the CNT as interconnect. According to geometry, GNR is classified as SLGNR and MLGNR, and MLGNR is preferred because it has less resistance than SLGNR. Further, by intercalation doping in MLGNR makes it more efficient than copper and SWCNT for the local and global level interconnects.

The performance depends on delay in propagation, power dissipation, & PDP. In literature, very little work is reported on Fermi energy that higher Fermi energy can result in larger number of conduction channels in MLGNR and affects its performance. The effect on the performance of MLGNR as an interconnect is not available in the literature. This study proposes to analyze the MLGNR interconnect performance by considering the impact of Fermi energy and temperature variation and comparing the results with those of the copper interconnect.

2.7 Problem Formulation & Objectives

The following are the objectives of the present study:

1. To develop Fermi energy and temperature dependent equivalent impedance model for MLGNR based interconnect.
2. To analyze the impact of Fermi energy on the performance of MLGNR interconnect in terms of delay, power dissipation and power delay product (PDP) on MLGNR interconnects.
3. To analyze the impact of temperature on the performance in terms of delay, power dissipation and PDP on MLGNR interconnects.
4. To analyze the combined effect of Fermi energy and temperature of the performance in terms of delay, power dissipation and PDP of MLGNR interconnects.
5. To compare the results obtained from the above analysis with the similar results obtained from copper and SWCNT interconnects.

2.8 Research Methodology

As the GNR is emerging and can be used as an alternative VLSI interconnect material at deep submicron technological nodes when downscaled from mean free path (<45nm). The proposed methodology will develop the temperature and Fermi energy dependent equivalent impedance model for MLGNR interconnects. The developed model will examine the impact of temperature and Fermi energy on the performance of MLGNR interconnect with respect to propagation delay power dissipation and PDP. Electrical parameters will be calculated using mathematical equations obtained from the equivalent impedance model proposed in the report. MATLAB is used to evaluate the resistance, capacitance, and inductance for temperature and Fermi energy-dependent GNR-based VLSI interconnect. Further, the calculated impedance parameters will be simulated using T-spice tool of simulation for evaluating temperature and Fermi energy-dependent performance of GNR-based interconnect from signal delay and PDP perspectives. Furthermore, the result obtained from the aforementioned objectives will be in comparison with those of copper and SWCNT interconnects for different nodes of technology

CHAPTER 3

FERMI ENERGY-DEPENDENT CIRCUIT MODEL AND PERFORMANCE ANALYSIS OF MLGNR INTERCONNECTS

This chapter explores the intercalation doping impact on the conductivity of "Multi-Layer Graphene Nanoribbon" in on-chip interconnects. The Fermi energy-dependent simulated results of MLGNR for 32nm, 22nm, and 16nm nodes of technology at global level interconnects are presented. Further, a comparative analysis with copper at three technological nodes for long interconnects is also carried out.

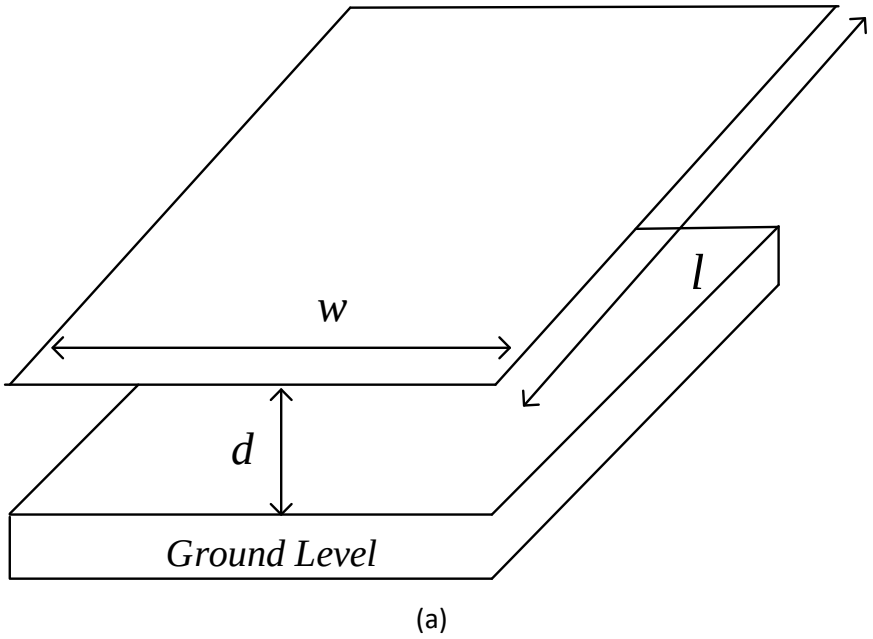
3.1 Introduction

Graphene nanoribbons are especially suited for on-chip interconnects and have obtained outstanding performance. The electrical ESC: "Equivalent Single Conductor" as inspection model of MLGNR is developed to evaluate its various circuit impedance parameters. The effect on the performance of MLGNR at 32nm, 22nm, and 16nm nodes of technology is addressed related to an electrical model. It has been reported in literature [85] that the neutral MLGNR has no ability to perform better compared to copper, and its performance can be enhanced after doping it with compounds, for example arsenic pentafluoride (AsF_5). Intercalation is termed as the mechanism to inject metal atoms among the layers of MLGNR. In addition, intercalation doping is directly proportional to the Fermi energy which rises the conductivity of the layers of MLGNR. The different levels of Fermi energies have major effect on the impedance parameters of MLGNR at three different nodes of technology for global lengths (500–2000μm). The "Simulation Program with Integrated Circuit Emphasis" (SPICE) simulation tool is used for simulating and estimating the performance of MLGNRs in delay as well as PDP (power delay product) terms. For the copper (Cu) interconnects at three different nodes of technology, a comparable and related analysis is undertaken.

3.2 Fermi-Energy-Dependent Model of the MLGNR

Graphene is a thin sheet of graphite where atoms of carbon are occupied in 2D honey comb lattice structures [85]. A thin width sheet of graphene are considered for pattering GNRs (Figure 1.7). The geometrical framework of MLGNR interconnect is derived through stacking

SLGNRs (Figure 3.1(a)) in a parallel combination as depicted in Figure 3.1(b), placed at distance *d* from the level of ground, where MLGNR interconnect thickness is represented by *t*. The distance among the adjacent layers of GNR is called Van Der Waal's Gap and is denoted with δ, having 0.34nm.



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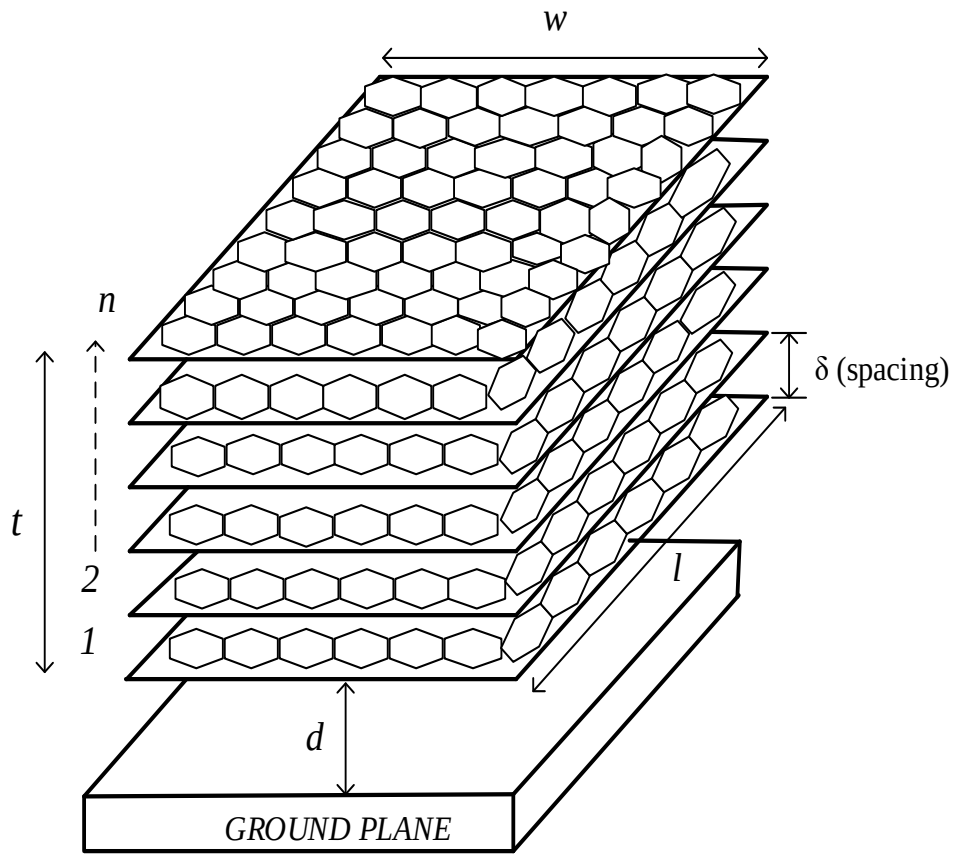


Figure 3.1 (a) SLGNR and (b) MLGNR as interconnect

Initially, the SLGNRs equivalent circuit model was obtained from the impedance parameters such as capacitance, resistance and inductance (Figure 3.2).

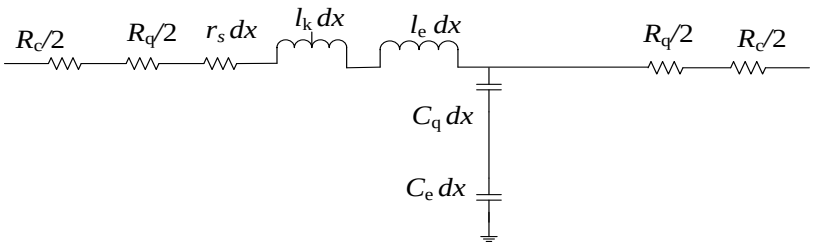


Figure 3.2 Equivalent circuit model of SLGNR

The GNR interconnect resistance is categorized into three different resistive components: r_s, R_q and R_c are defined by scattering, quantum, and contact resistance respectively. Primarily, the R_c occurs owing to the contact of the metal with MLGNR and its value is quite small; in the range of few hundreds of ohms to tens of kilo ohms depends on fabrication procedure [104, 111]. In MLGNR, every layer contributes to total current conduction, therefore its impact is negligible small and excluded for this research. R_q (quantum resistance) is associated with GNR having smaller length compared to electrons' effective mean free path (λ_{eff}), and for such lengths, quantum resistance does not depends upon length. Given following equation can be used to calculate R_q [104]:

$$R_q = \frac{12.9}{N_{ch_{GNR}}} \qquad (k\Omega) \qquad [l < \lambda_{eff}] \tag{3.1}$$

Where length is defined by l, $N_{ch_{GNR}}$ represents the number of conducting channels and is obtained by n_c (conduction) along with n_v (valence) sub-bands as described by Fermi–Dirac distribution function [104]. The following equation gives the Fermi–Dirac distribution function:

$$N_{ch_{GNR}} = \sum_{i=1}^{n_c} \left| 1 + e^{\frac{(E_i - E_f)}{K_B T}} \right|^{-1} + \sum_{i=1}^{n_v} \left| 1 + e^{\frac{(E_i + E_f)}{K_B T}} \right|^{-1} \tag{3.2}$$

Where i, T, are defined by integer and temperature in kelvin respectively. Boltzmann constant is written by K_B having 1.3807×10^{-23} J.K^{-1}. Electron and hole energy is defined byE_i in i^{th} sub-band [96] defined as by equation 3.3:

$$E_i = \frac{h v_f}{2w} |i|, \qquad i \neq 0 \tag{3.3}$$

Where *w* is interconnect width and Planck's constant is denoted by symbol *h* having 6.626×10^{-34} J.s. Fermi velocity is represented by v_f having 8×10^5 m/s. As stated in the previous research [96], the ac-GNRs (semiconducting or metallic) shows smaller resistivity than the zz-GNR. Moreover, the semiconducting ac-GNR has been found to have nearly the similar resistivity as the ac-GNR (metallic). For the evaluation of interconnects potential, the metallic ac-GNR is presented for this research. The number of conduction channels in ac-GNR (metallic) depends on the width and Fermi energy. Therefore, equation 3.2 is deduced to width and Fermi energy dependent as given by equation 3.4 for metallic ac-GNR [104].

$$N_{ch\ GNR} = kE_f = \alpha w E_f, \quad E_f \geq 0.1 \text{ eV} \quad w > 10 \text{ nm} \tag{3.4}$$

Where *k* defines angle factor and α is 1.2 $eV^{-1}nm^{-1}$, E_f is calculated in eV (electron volt). Likewise, $N_{ch\ GNR} = \alpha w E_f - 0.82$ is used to calculate number of conduction channels for zz-GNR.

As discussed in the literature [85], the performance of SLGNR cannot show better results as compared to MLGNR; therefore equivalent circuit model of SLGNR are used in parallel for multi-conductor circuit (MCC) of MLGNR interconnect as presented in Figure 3.3 [34].

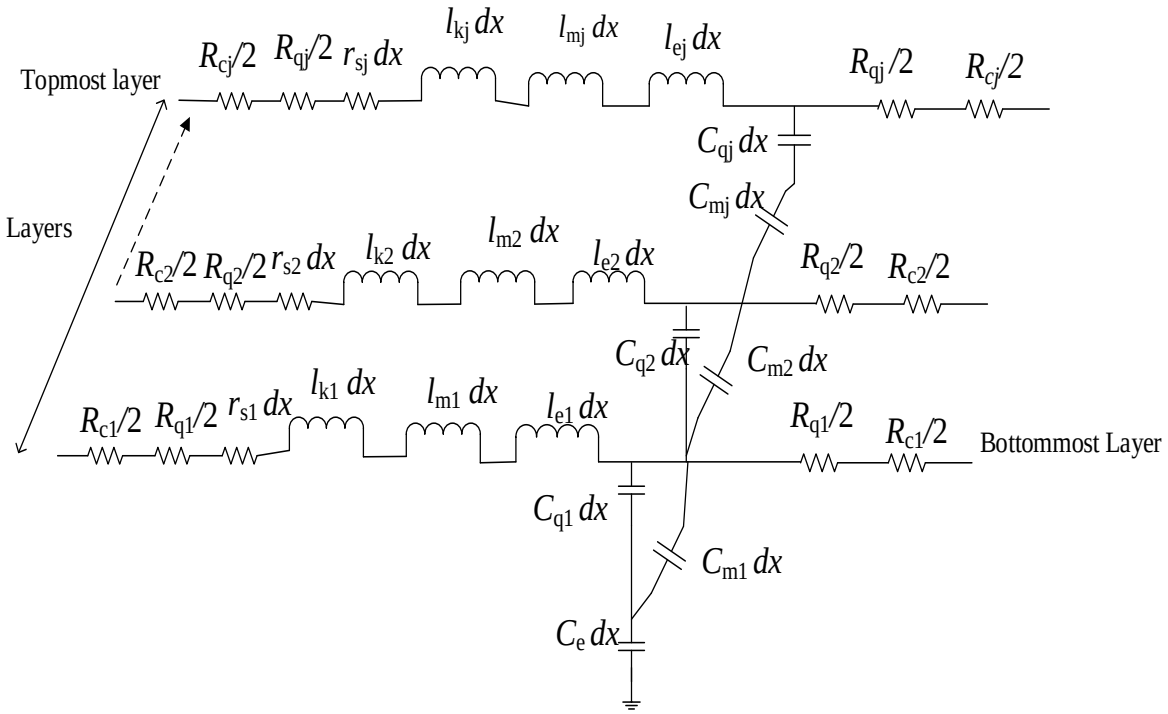
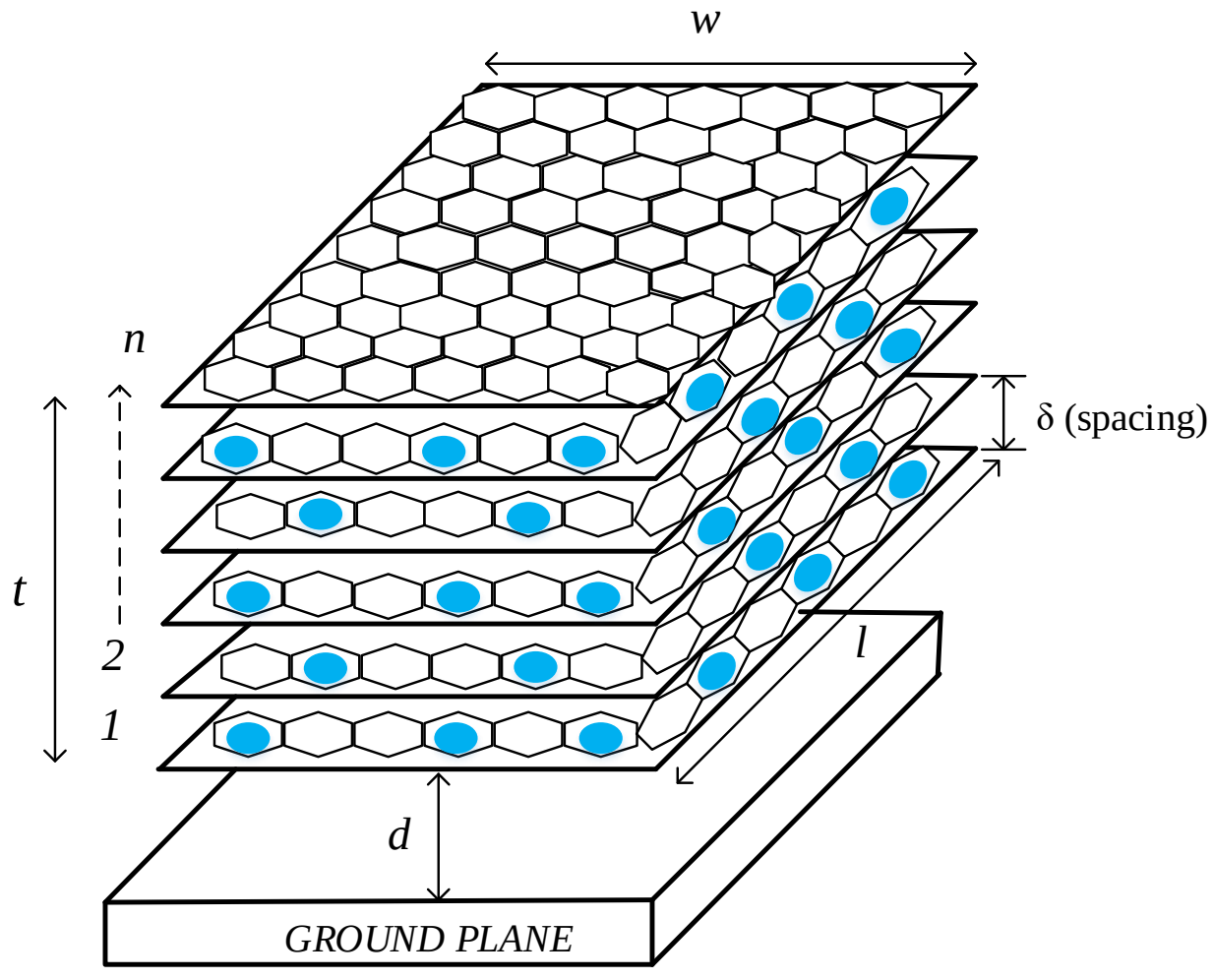


Figure 3.3 Equivalent MCC of MLGNR

In MLGNR bundle the number of conducting layers (*n*) can be estimated by equation 3.5 [111, 112]:

$$n = 1 + \text{Integer}\left[\frac{t}{\delta}\right] \tag{3.5}$$

As per Thompson and Fischer [113], Fermi energy of every layer of MLGNR can be enhanced by diffusing the graphite-intercalated compounds for example AsF_5 among adjacent layers of graphene as depicted in Figure 3.4(a). The modulation of Fermi energy has been achieved by stage 1 intercalation approach [113, 114, 115]. The "stage" of a compound is the number of carbon layers between nearest intercalant layers. Between adjacent graphene layers there is a layer intercalation compounds signifies the identity period of doping layer and Figure 3.4(a) corresponds to stage 1 intercalation. The AsF_5-doped compounds insertion suppresses the interlayer interaction therefore upswings the MFP (mean free path). In MLGNR, the mechanism of enhanced conductivity is because of transferring the charge in graphene layers from intercalated compounds, results in changing the band structure that provides an expanded Fermi field. It is shown in Figure 3.4(b) that doping with either pentavalent (electrons) or trivalent (holes) compounds upswings the Fermi energy.



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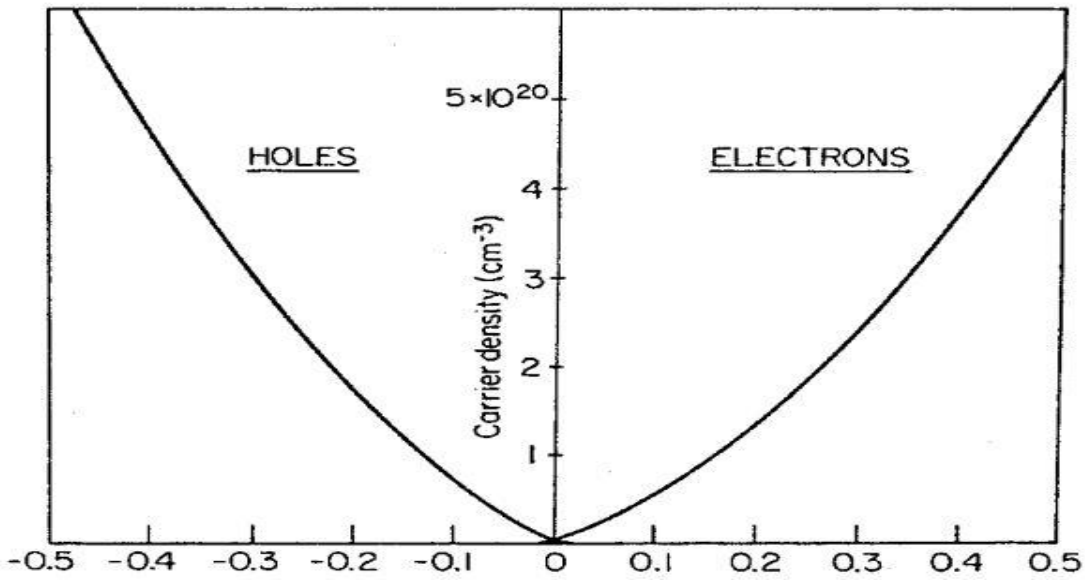


(b)

Figure 3.4 (a) Schematic of stage 1 intercalation doped MLGNR interconnect (b) Fermi level shift with electron and hole carrier concentration doping compounds [114]

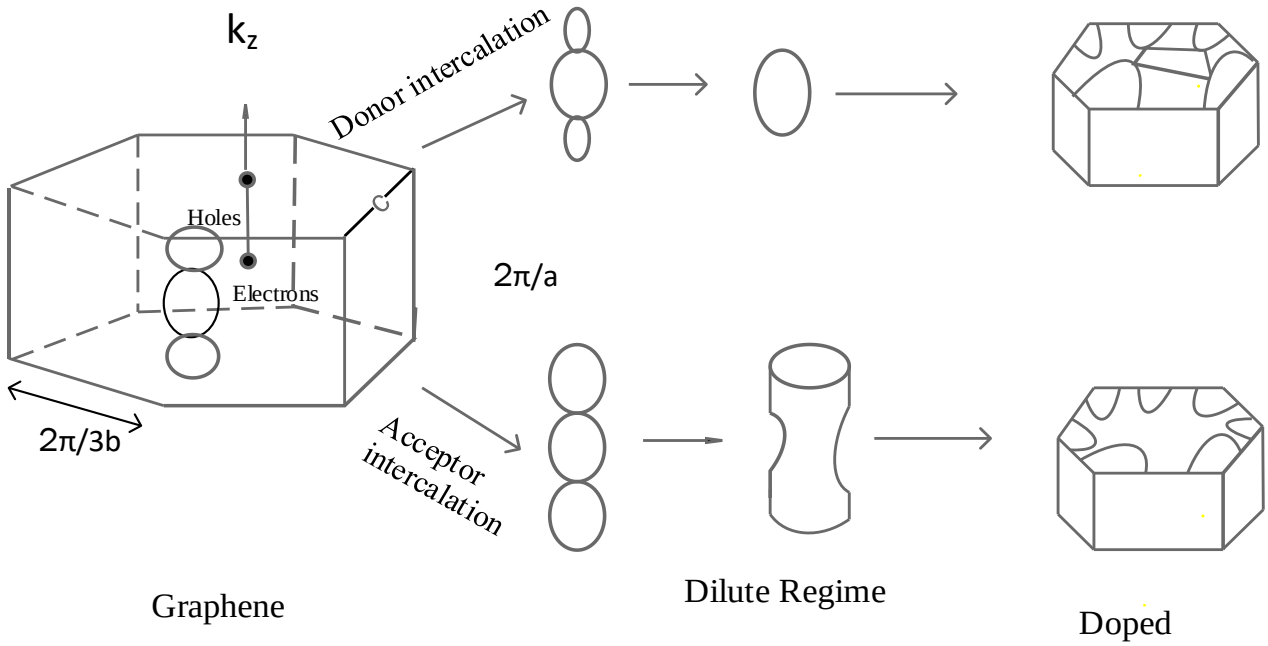
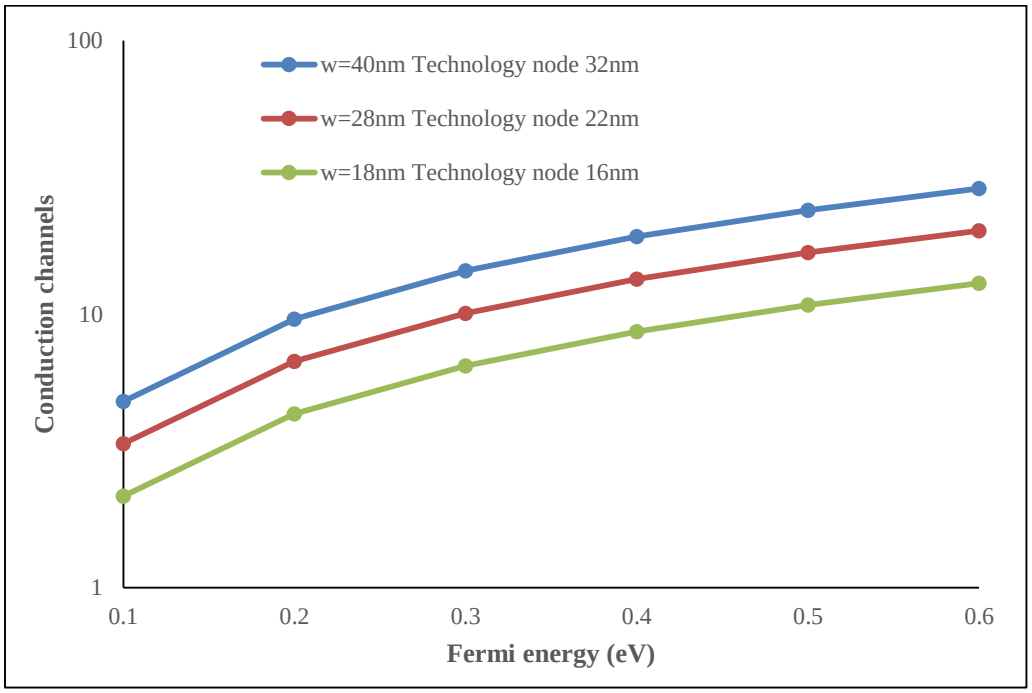


Figure 3.5 Evolution of Fermi surface from pure graphene to doped one by intercalation [113]

Fermi surface called a space that is reciprocal of the space energy constant *E*; and represents the graphene energy band structure which is defined by following equation [94]:

$$E = \pm h v_f \sqrt{k_x^2 + \left(k_y \pm \frac{2\pi}{3b} \right)^2} \quad (3.6)$$

Where k_x and k_y corresponds to the wave vectors in x as well as y directions respectively.



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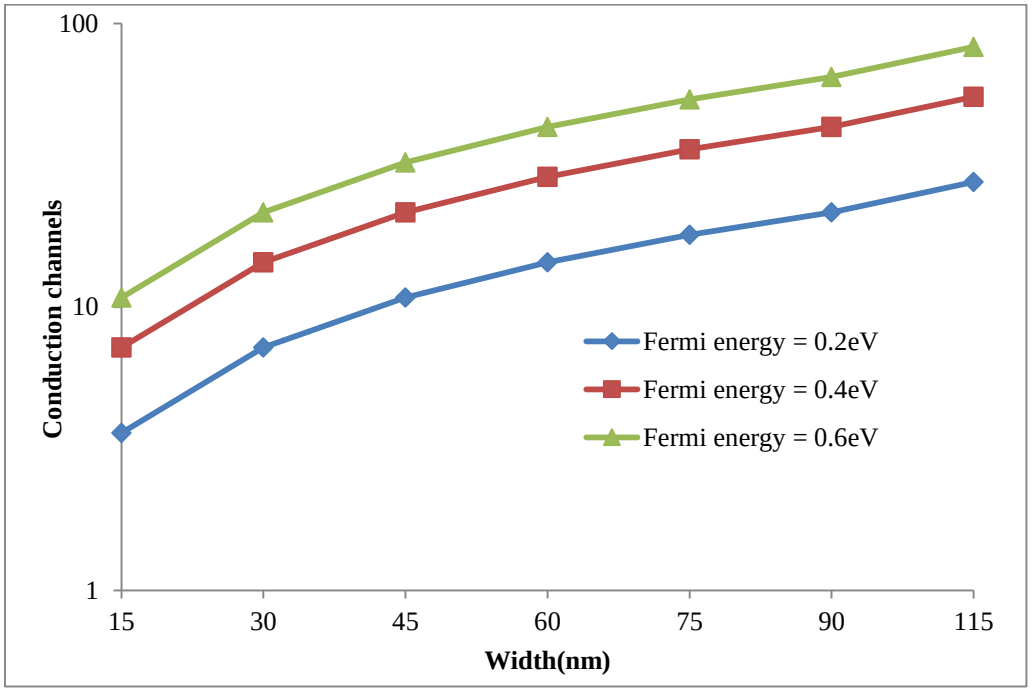
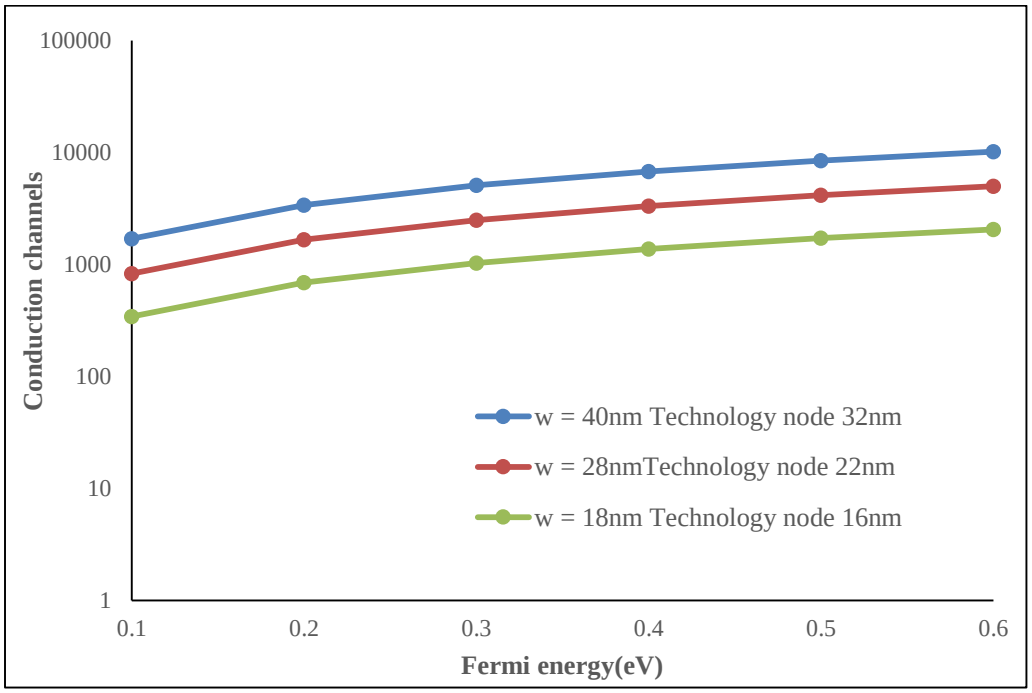


(b)

Figure 3.6 Conduction channels in every layer of ac-MLGNR (metallic) as a function of (a) Fermi energy (b) Interconnect width

Total number of conduction channels in MLGNR can be estimated by following equation:

$$N_{ch_{MLGNR}} = \alpha w E_f \left(\frac{t}{\delta} \right) \tag{3.7}$$



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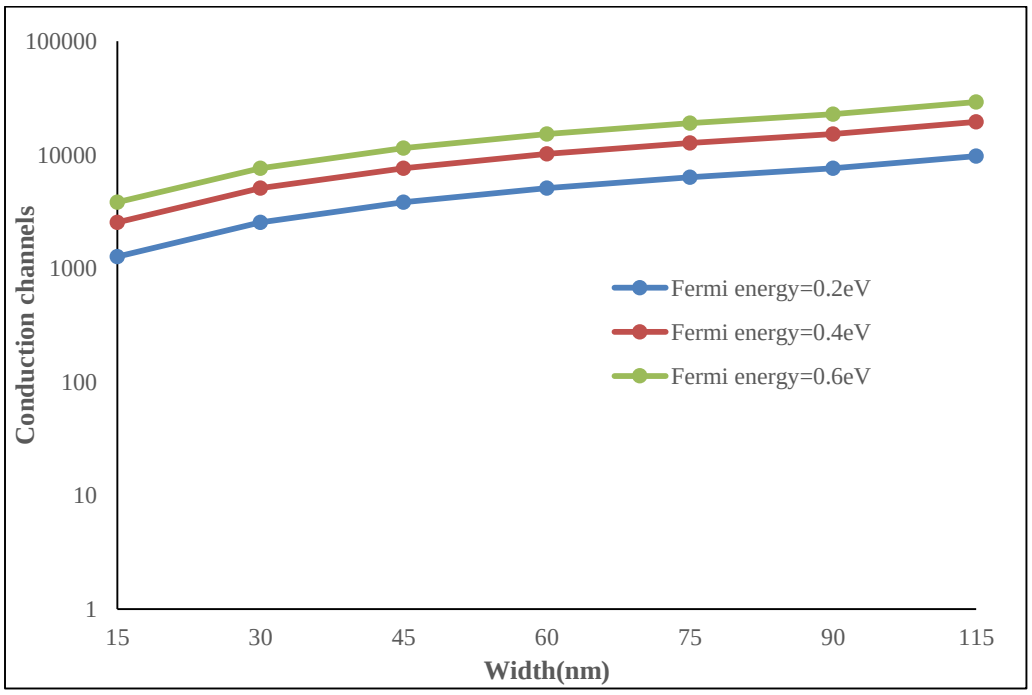


(b)

Figure 3.7 Total number of conduction channels in ac-MLGNR (metallic) as a function of (a) Fermi energy (b) Interconnect width

$\sqrt{3}a_o/2$ is the value of b where a_o is the length of nearest carbon bond having 0.142nm value in GNRs. Electron concentration surface increases because of n-type intercalation (AsF_5) due to electron donor. The opposite holds due to p-type intercalation.

The experimental data for stacking intercalation layers among the graphene layers was published in the literature [114, 115]. Figure 3.5 represents the hypothetical Fermi surface because of the acceptor as well as donor dilution compounds. The Fermi surface is because of the moving in the right direction of Fermi energy from neutral MLGNR. The rise in Fermi energy is due to the intercalation of the donor.

$N_{\mathrm{ch_{GNR}}}$ rises linearly with escalation in Fermi energy that is calculated by equation 3.4 for a metallic ac-GNR at technology-based width. Figure 3.6(a) shows that in the 32nm, 22nm, and 16nm nodes of technology, conducting channels are rising with the increase in Fermi energy while decreasing with shrinking interconnect width. Figure 3.6(b) represents that interconnect width is directly proportional to number of conducting channels and inversely proportional to Fermi energy. It is verified by Figure 3.6 that with rise in Fermi energy conducting channels increases means carrier density rises per cubic centimeter, as shown in Figure 3.4(b).

Figure 3.7(a) shows that in the 32nm, 22nm, and 16nm nodes of technology, conducting channels follows the same trend as presented in Figure 3.6 i.e. increases with rise in Fermi energy. Further, the total number of conducting channels of MLGNR are much higher compared to every layer of multi-layer GNR (Figure 3.6). Therefore, suitable doping among the adjacent GNR layers is important for increasing the MLGNR interconnect conductivity with downscaling of technological nodes.

3.2.1 Scattering Resistance (r_s)

This chapter takes into account low bias since the GNR is self-heated with a higher bias and does not obey ohmic behavior. A new resistance known as the r_s (scattering resistance) is employed if the interconnect length is more as compared to λ_{eff}. The following equation is used to calculate: resistance of GNR due to scattering in p.u.l. (per unit length) [111]:

$$r_s = \frac{12.9}{N_{ch_{\mathrm{GNR}}}\lambda_{eff}} \quad (\mathrm{k\Omega}) \tag{3.8}$$

From the Matthiessen's rule, λ_{eff} for r^{th} sub-band is represented by equation 3.9 [111]:

$$\lambda_{eff,r} = \left(\lambda_d^{-1} + \lambda_r^{-1}\right)^{-1} \tag{3.9}$$

Where λ_d is MFP occurring because of defect and impurity scattering. Berger et al. [116] report MFP, because of defects is approximately 1μm for SLGNR, however reduced to 419nm for

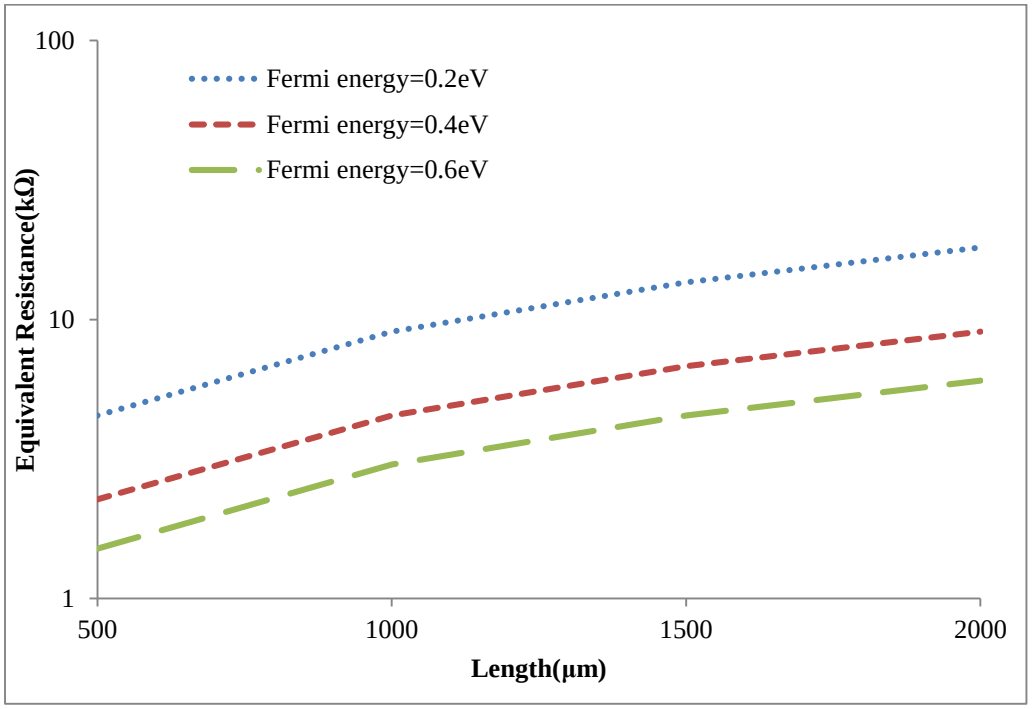
MLGNR due to an inter-sheet electron hopping [104]. λ_r is an MFP because of edge scattering and is determined by the equation given below:

$$\lambda_r = \frac{w}{1-p}\sqrt{\left(\frac{2wE_f}{rhv_f}\right)-1} \tag{3.10}$$

Where p is denoted by specular constant indicating roughness of edge; p ranges between 0 and unity (1). p is equal to unity for total specular edges; p is equal to zero for absolute diffuse edges.

Literature [85, 104] states that the GNR conductance can be increased if the edges are converted from a completely diffused to a smooth one. In order to approximate or be superior to copper interconnect efficiency, value of p is equal to or larger than 0.8. Specular edges are therefore expected to boost the performance of MLGNR than copper at global interconnect lengths. For prolonged MLGNR ($l>\lambda_{eff}$), the total resistance may be calculated using equation 3.11 [104]. In this research, complete specular edges are considered and therefore p is considered as 1.

$$R_{MLGNR} = R_q + r_s = \frac{12.9}{n.N_{ch_{GNR}}}\left(1+\frac{l}{\lambda_d}\right) \tag{3.11}$$



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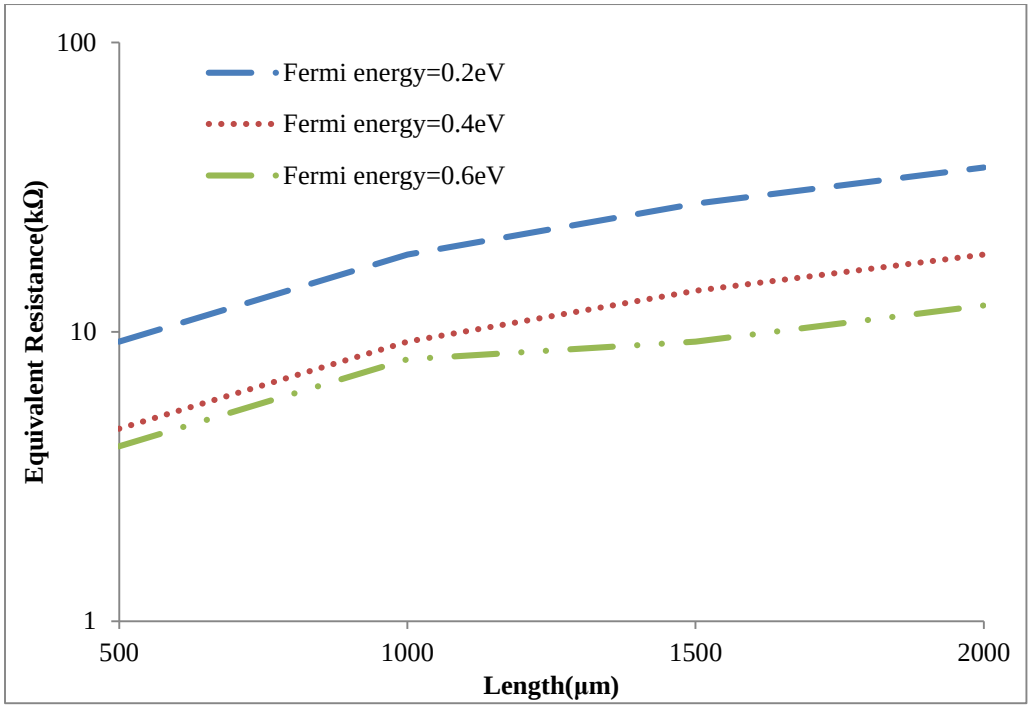

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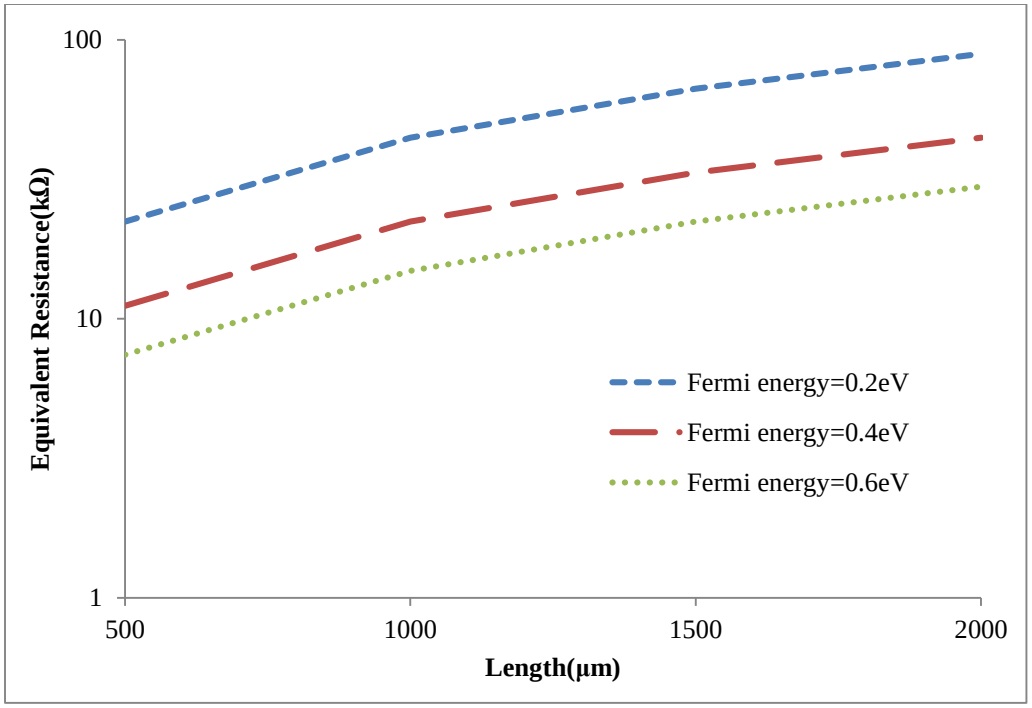


(c)

Figure 3.8 Equivalent resistance (MLGNR) with different levels of Fermi energies at (a) 32nm, (b) 22nm, and (c) 16nm nodes of technology as a function of length

The value of MLGNR equivalent resistance is obtained analytically using the MATLAB computing software for three various technological nodes and is graphically illustrated in

Figure 3.8. The criteria of parameters is derived from ITRS 2013 as shown in Table 3.1 [16]. The number of conducting channels is in reverse interaction with resistance (equation (3.11)). Due to increase of E_f in GNR layers, the MLGNR resistance decreases at different global lengths. Therefore, the performance of MLGNR increases with the reduction in resistance at long lengths.

3.2.2 Equivalent Inductance and Capacitance

Neighboring layers will act as two parallel plate capacitors if GNRs width is greater compared to the spacing among adjacent layers. The couplings among adjacent layers in MLGNR are interlayer coupling capacitance and interlayer coupling inductance. The C_m (interlayer coupling capacitance) and l_m (interlayer coupling inductance) among the adjacent GNR layers are represented in the following equations [85, 111]:

$$l_m = \mu_o \delta / w \tag{3.12}$$

$$C_m = \varepsilon_o w / \delta \tag{3.13}$$

Where μ_o, ε_o are the magnetic permeability having $4\pi\times10^{-7}$ H/m and relative permittivity of free space having 8.85×10^{-12} F/m respectively. The MLGNR comprises of magnetic inductance as well as kinetic inductance. l_k (kinetic inductance) is produced by the kinetic energy, due to the motion of electrons in conducting channels of GNR whereas the l_e (magnetic inductance) is produced by the magnetic field due to different levels of currents varying with time as recommended by the Ampere's as well as Faraday's laws. The l_e and l_k in p.u.l. of the MLGNR were estimated using equations (3.14) and (3.15) [85, 111], respectively, as follows:

$$l_e = \frac{\mu_o d}{w} \tag{3.14}$$

$$l_k = \frac{8}{n\alpha w E_f} \quad (\text{nH/μm}) \tag{3.15}$$

The l_k is always larger than the l_m and has dominating effect on the layers of MLGNR. Hence, l_m can be ignored [104].

The MLGNR comprises of C_q (quantum capacitance) and C_e (electrostatic capacitance). As compared to quantum capacitance, the coupling capacitance per GNR layer is small and therefore can be neglected. The p.u.l. C_e along with C_q are given by equations (3.16) and (3.17) [85, 111] respectively, as follows and β is 2.3nm:

$$C_e = \frac{\varepsilon_o w}{d} \tag{3.16}$$

$$C_{\mathrm{q}} = 0.1.n.N_{\mathrm{ch_{GNR}}}\left[1+\sqrt{1+1/\alpha\beta E_{\mathrm{f}}}\right] \quad (\mathrm{fF/\mu m}) \tag{3.17}$$

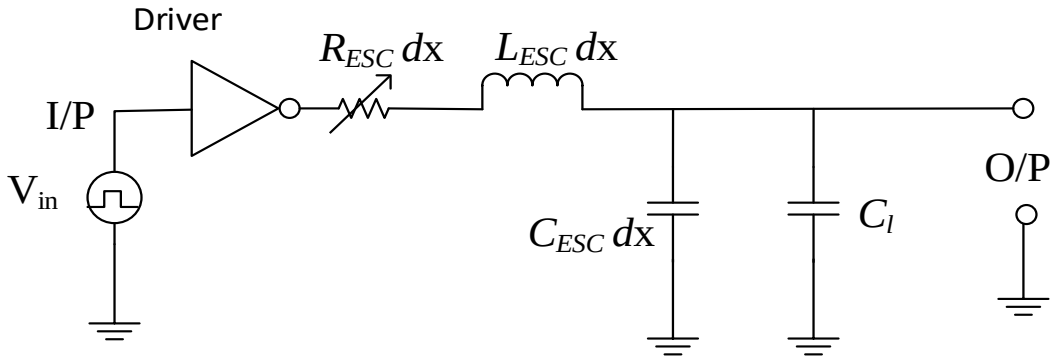


Figure 3.9 Equivalent model of MLGNR interconnect as single conductor using CMOS inverter

MLGNR is modeled as single conductor, dependent on Fermi energy based on the derived parameters as shown in Figure 3.9. The input signal is considered as pulse having same rise as well as fall time [117]. By the following equations the equivalent circuit parameters of single conductor transmission model of MLGNR are provided:

$$R_{\mathrm{ESC}} = R_{\mathrm{MLGNR}} = \frac{12.9}{nN_{\mathrm{ch_{GNR}}}}\left(1+\frac{l}{\lambda_{\mathrm{d}}}\right) \tag{3.18}$$

$$L_{\mathrm{ESC}} = l_{\mathrm{k}} + l_{\mathrm{e}} \tag{3.19}$$

$$C_{\mathrm{ESC}} = (C_{\mathrm{q}}^{-1} + C_{\mathrm{e}}^{-1})^{-1} \tag{3.20}$$

3.2.3 Impedance Model for Copper Interconnect

Copper interconnect is discussed in this particular section. The three copper interconnects are shown in Figure (3.10) are separated from each other with spacing *s*, placed at distance *d* from level of ground, and *t* represents thickness. The parasitic parameters play an essential part in calculating the performance of the copper interconnects. The following equation is given for the copper resistance at room temperature [118]:

$$R_{\mathrm{C}} = \frac{\rho_{\mathrm{o}} l}{w.t} \tag{3.21}$$

Where ρ_{o} defined the copper resistivity. The ρ_{o} value depends on nodes of technology which is shown in Table 3.1.

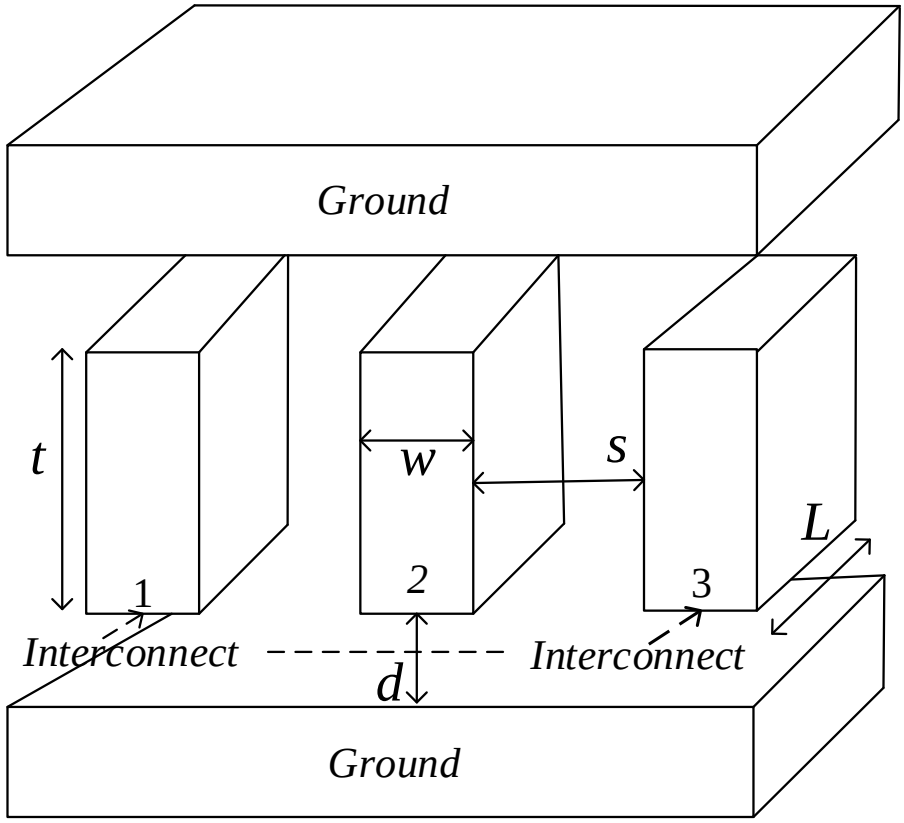


Figure 3.10 Conventional geometry for copper interconnect

The inductance of copper interconnects having rectangular cross-section is determined by the given following equation [34, 118]:

$$L_{\mathrm{C}} = \frac{\mu_{\mathrm{o}} l}{2\pi}\left[\mathrm{In}\left(\frac{2l}{w+t}\right)+\frac{1}{2}+\frac{0.22(w+t)}{l}\right] \tag{3.22}$$

The copper interconnect capacitance is estimated by the fringe flux and area to the underlying plane, represented in equation 3.23 [34, 118]:

$$C_{\mathrm{g}} = \varepsilon_{\mathrm{o}}\varepsilon_{\mathrm{r}}\left[\frac{w}{d}+2.22\left(\frac{s}{s+0.7d}\right)^{3.19}+1.17\left(\frac{s}{s+1.15d}\right)^{0.76}\left(\frac{t}{t+4.53d}\right)^{0.12}\right] \tag{3.23}$$

Where, dielectric constant is represented by ε_{r}, which relies on the nodes of technology.

3.3 Performance analysis

For copper as well as MLGNR interconnects, delay and PDP as parameters of performance for three different nodes of technology at global lengths are examined. Interconnect (MLGNR) parasitic parameters that are estimated in Section 3.2, affect the PDP and delay perspectives. CMOS (complementary metal oxide semiconductor) inverter is utilized to drive interconnects having C_{l} (load capacitance) of 0.01fF, as shown in Figure 3.9. Interconnects performance is estimated by SPICE simulation tool. PTM "Predictive Technology Model" is used to determine

Table 3.1 ITRS 2013 parameters of simulation for global level interconnect [16]

Parameters	32nm	22nm	16nm
Width *w*(nm)	40	28	18
Thickness *t*(nm)	120	84	54
Frequency(GHz)	1	1	1
V_{DD}(volts)	0.9	0.8	0.7
Oxide Thickness(nm)	93.6	65.5	40
Aspect Ratio(A/R)	3	3	3
Repeater size(W/L)	30	30	40
Number of repeaters	2	2	2
Dielectric constant(ϵ_r)	2.77	2.59	2.31
ρ_o copper(μΩcm)	3.66	4.2	5.69
Model file(PTM)	54	54	54

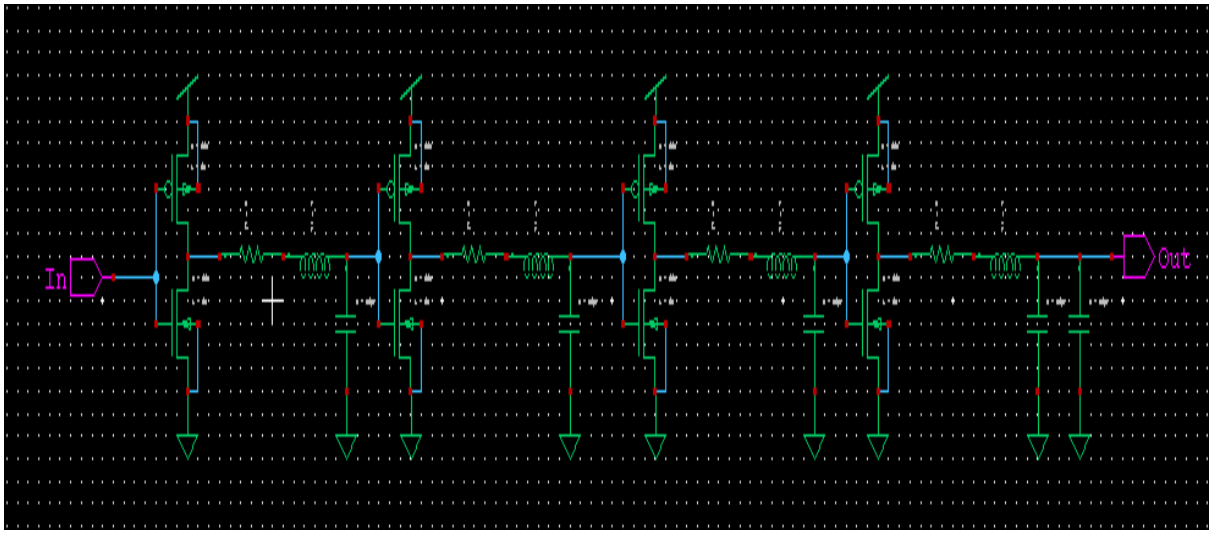


Figure 3.11 Distributed model from lumped models using optimum number of repeaters

the CMOS driver [118]. The parameters of simulation are taken into account from the ITRS 2013 edition, presented in Table 3.1. In order to analyze interconnects performance in PDP and delay terms, parasitic parameters were simulated utilizing set ups of simulation using DIL (Driver Interconnect Load) as shown in Figure 3.11.

3.3.1 Signal Delay (Fermi-Energy-Dependent) of the MLGNR

The electronics circuit operational speed is affected by the signal delay at the output of wire. Under this section, for 500–2000μm lengths, the MLGNR interconnect delay is examined at three different nodes of technology. For MLGNR interconnect, E_f is considered as 0.6eV, 0.4eV, and 0.2eV. SPICE simulation tool is utilized for different levels of Fermi energies to determine signal delay. Tables 3.2–3.4 show signal delay of MLGNR with respect variable

Fermi levels for three different nodes of technology (32nm, 22nm, and 16nm) at global lengths (500–2000μm) and graphically depicted in Figure 3.12. It is analyzed from Figure 3.12 that rising level of Fermi energies reduces the delay. Though, the reduction of percentage in signal delay is approximately 41%, 41%, 39%, as E_f varies from 0.2eV to 0.4eV and is 25%, 24%,

Table 3.2 Delay of MLGNR from 500–2000μm length with different levels of Fermi energies at 32nm technological node

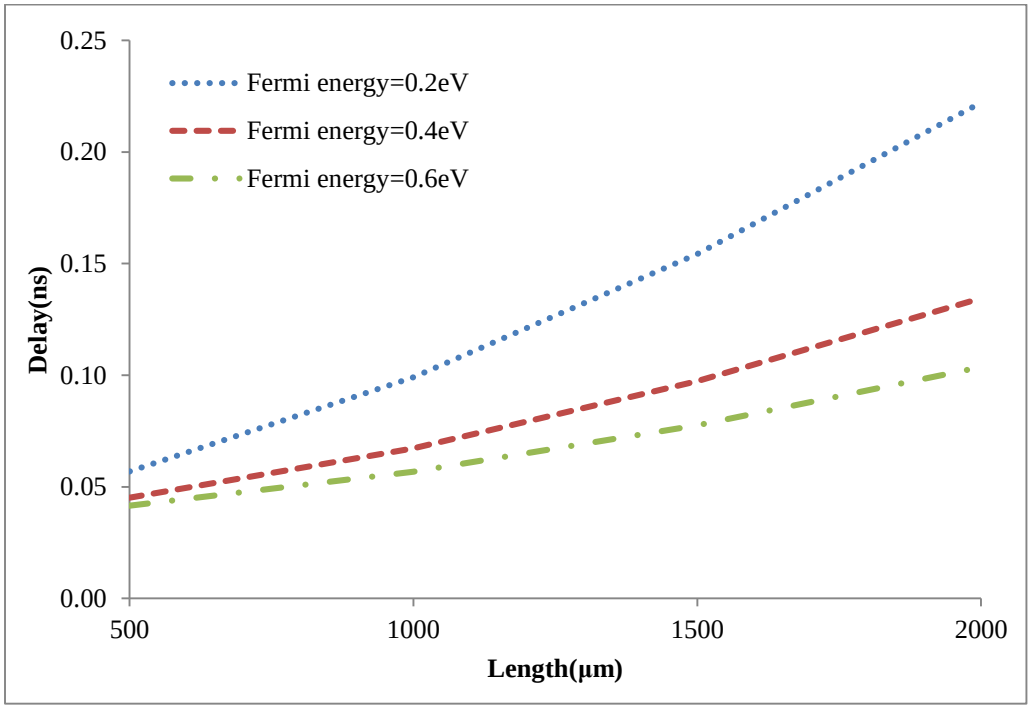
Length (μm)	Delay (ns)		
	MLGNR		
	E_f=0.2eV	E_f=0.4eV	E_f=0.6eV
500	0.0570	0.0452	0.0416
1000	0.0991	0.0672	0.0568
1500	0.1543	0.0974	0.0776
2000	0.2221	0.1345	0.1037

Table 3.3 Delay of MLGNR from 500–2000μm length with different levels of Fermi energies at 22nm technological node

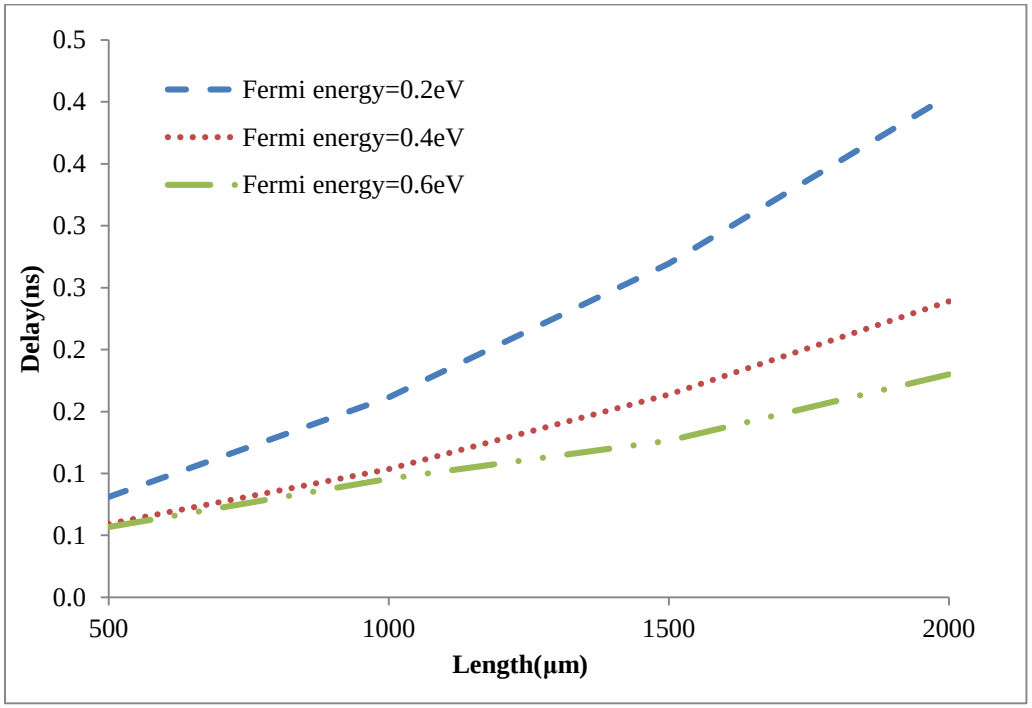
Length (μm)	Delay (ns)		
	MLGNR		
	E_f=0.2eV	E_f=0.4eV	E_f=0.6eV
500	0.08096	0.05925	0.05661
1000	0.16132	0.10353	0.09584
1500	0.26935	0.16380	0.12651
2000	0.40497	0.23884	0.18009

Table 3.4 Delay of MLGNR from 500–2000μm length with different levels of Fermi energies at 16nm technological node

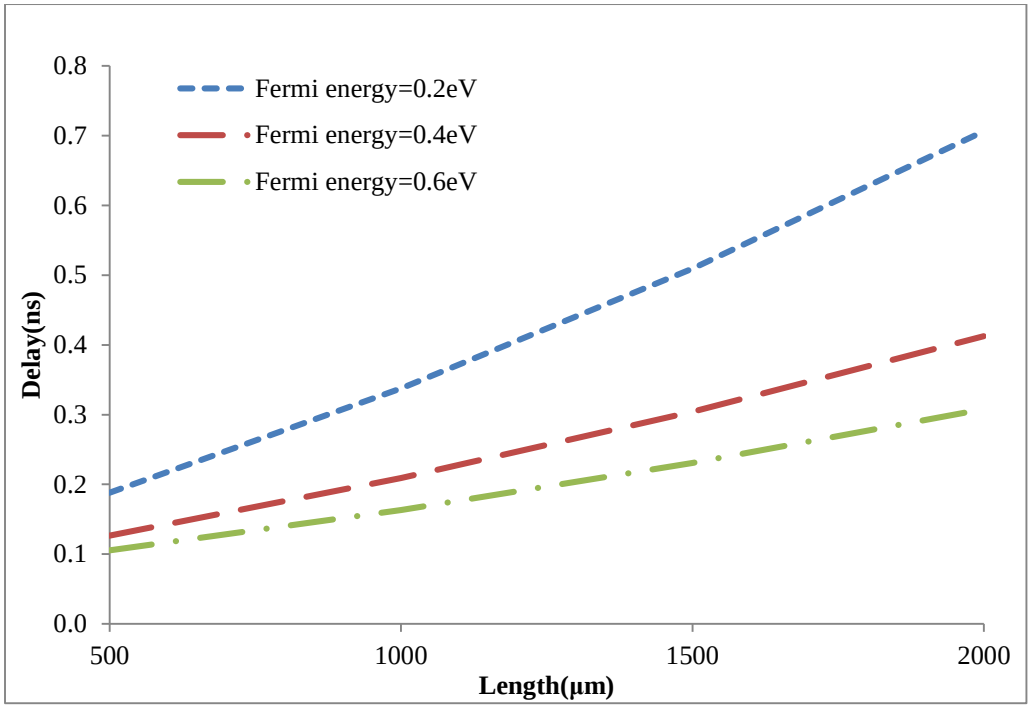
Length (μm)	Delay (ns)		
	MLGNR		
	E_f=0.2eV	E_f=0.4eV	E_f=0.6eV
500	0.18788	0.12668	0.10543
1000	0.33744	0.20923	0.16340
1500	0.50953	0.30438	0.23090
2000	0.70604	0.41249	0.30765


0.25
0.20
0.15
0.10
0.05
0.00
Delay(ns)
Fermi energy=0.2eV
Fermi energy=0.4eV
Fermi energy=0.6eV
500
1000
1500
2000
Length(µm)

(a)


0.5
0.4
0.4
0.3
0.3
0.2
0.2
0.1
0.1
0.0
Delay(ns)
Fermi energy=0.2eV
Fermi energy=0.4eV
Fermi energy=0.6eV
500
1000
1500
2000
Length(µm)

(b)



(c)

Figure 3.12 MLGNR delay with different levels of Fermi energies at (a) 32nm, (b) 22nm, and (c) 16nm nodes of technology as a function of length

22%, as it varies from 0.4eV to 0.6eV for 16nm, 22nm, and 32nm nodes of technology, respectively, at 2000µm interconnect length because the Fermi energy effects on MLGNR parasitic parameters. Moreover, the reduction of percentage in signal delay from 0.2eV to 0.6eV is 56%, 55%, 53% for 16nm, 22nm, and 32nm nodes of technology, respectively at 2000µm length of MLGNR.

3.3.2 PDP (Fermi-Energy-Dependent) of MLGNR

Impact of power dissipation, as the VLSI industry expands, is a key factor and is of great significance. Power is basically the heat dissipation corresponding to charging as well as discharging of wire capacitances. The total efficiency of an interconnect depends on the product of power dissipation and delay. Both are independent parameters but to estimate the actual performance of an interconnect, PDP must to be taken into account for elite integrated circuits and thus, the low PDP is prudent which is presented in this section. Tables 3.5–3.7 show PDP of MLGNR with respect to variable Fermi energy levels for three different nodes of technology at global lengths (500–2000µm) and graphically depicted in Figure 3.13. It is analyzed from Figure 3.13 that rising levels of E_f reduces PDP. Though, the PDP percentage reduction is approximately 43%, 42%, 40%, as E_f varies from 0.2eV to 0.4eV and is 27%, 26%, 23%, as it varies from 0.4eV to 0.6eV for 16nm, 22nm, and 32nm next-generation nodes of

technology, respectively, at 2000μm interconnect length because the Fermi energy effects on

Table 3.5 PDP of MLGNR from 500–2000μm length with different levels of Fermi energies at 32nm technological node

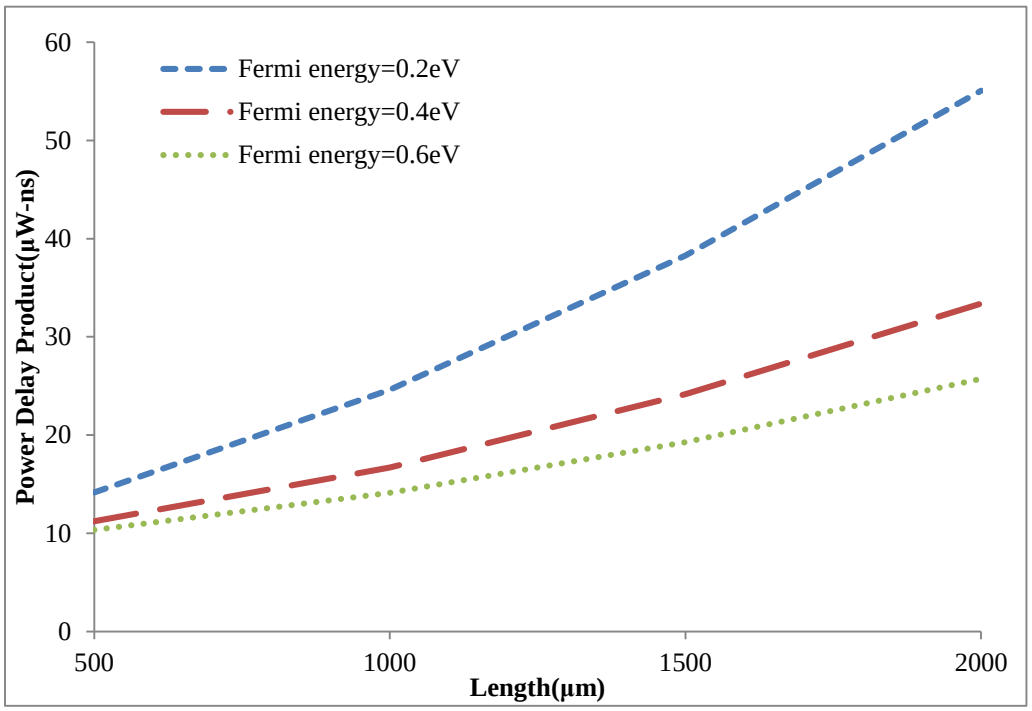
Length (μm)	PDP (μW-ns)		
	MLGNR		
	E_f=0.2eV	E_f=0.4eV	E_f=0.6eV
500	14.148	11.221	10.338
1000	24.603	16.683	14.102
1500	38.273	24.170	19.258
2000	55.056	33.374	25.742

Table 3.6 PDP of MLGNR from 500–2000μm length with different levels of Fermi energies at 22nm technological node

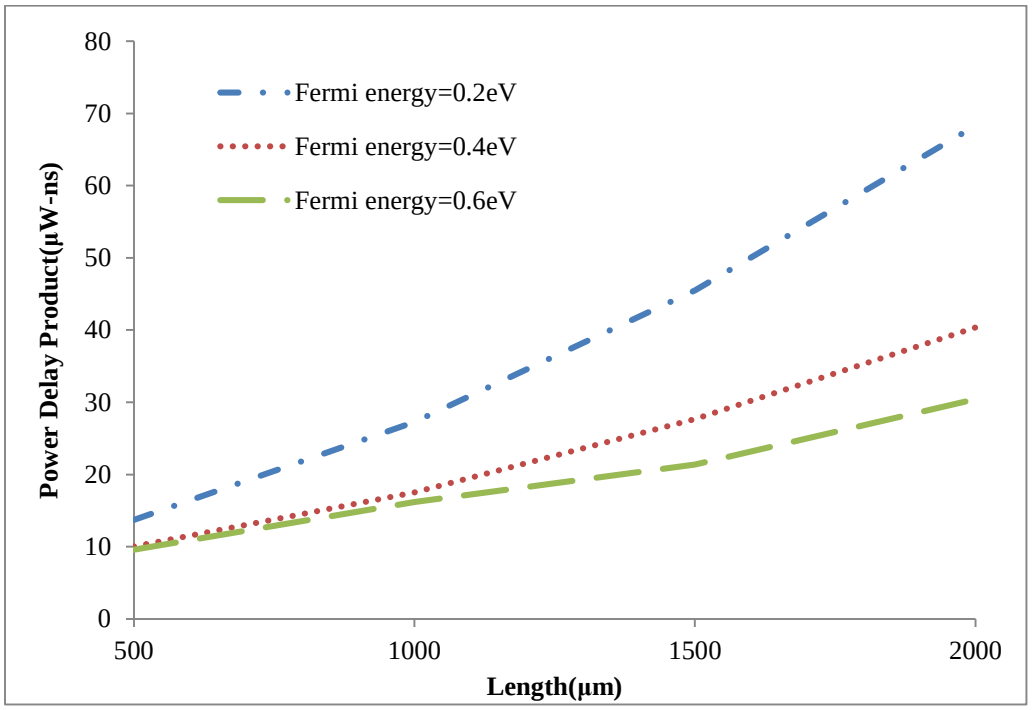
Length (μm)	PDP (μW-ns)		
	MLGNR		
	E_f=0.2eV	E_f=0.4eV	E_f=0.6eV
500	13.6962	10.0224	9.5790
1000	27.2675	17.5117	16.2126
1500	45.4778	27.6906	21.3957
2000	68.2834	40.3485	30.4432

Table 3.7 PDP of MLGNR from 500–2000μm length with different levels of Fermi energies at 16nm technological node

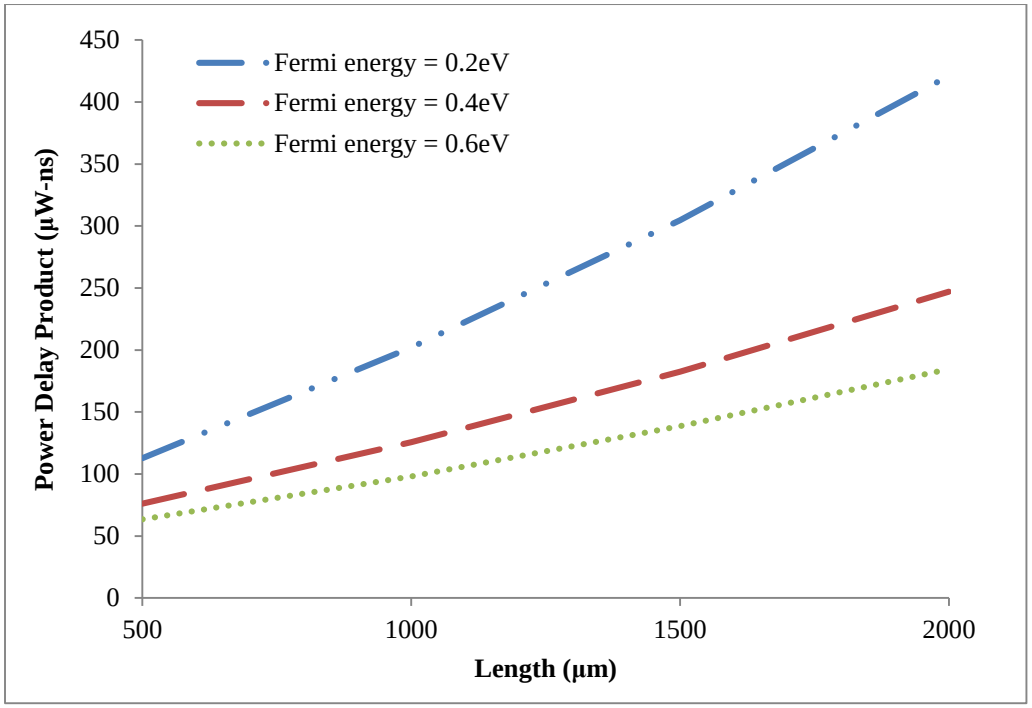
Length (μm)	PDP (μW-ns)		
	MLGNR		
	E_f=0.2eV	E_f=0.4eV	E_f=0.6eV
500	112.8363	76.14979	63.39534
1000	202.232	125.6345	98.17982
1500	304.6422	182.5414	138.6196
2000	421.0105	247.0331	184.5201


Fermi energy=0.2eV
Fermi energy=0.4eV
Fermi energy=0.6eV
Power Delay Product(µW-ns)
Length(µm)
0
10
20
30
40
50
60
500
1000
1500
2000

(a)


Fermi energy=0.2eV
Fermi energy=0.4eV
Fermi energy=0.6eV
Power Delay Product(µW-ns)
Length(µm)
0
10
20
30
40
50
60
70
80
500
1000
1500
2000

(b)



(c)

Figure 3.13 MLGNR PDP with different levels of Fermi energies at (a) 32nm, (b) 22nm, and (c) 16nm nodes of technology as function of length

the MLGNR parasitic parameters. In addition, the reduction of percentage in signal delay from 0.2eV to 0.6eV is 57%, 56%, 54% for 16nm, 22nm, and 32nm nodes of technology at 2000µm length, respectively of MLGNR.

3.3.3 Analysis and Comparison of MLGNR Interconnect with Copper

Delay as well as PDP ratio of MLGNR and copper is examined whereas for MLGNR considering different levels of Fermi energies in contrast with copper interconnect for all three various nodes of technology at global lengths. Tables 3.8–3.10 represents that MLGNR shows smaller delay as compared to copper interconnect for 32nm, 22nm, and 16nm nodes of technology. This is because of the Fermi energy impacts on MLGNR parasitic parameters. At 32nm technological node, for length 500–2000µm, the delay ratio reduced with rise in the value of copper in denominator as presented in Table 3.8 as well as graphically shown in Figure 3.14(a). It is also analyzed for 22nm and 16nm technological nodes as shown in Tables 3.9 and 3.10 and graphically in Figures 3.14(b) and (c) respectively. This illustrates that the ratio of MLGNR/Copper is decreasing with increase in interconnect length which shows that the rate of change of copper in terms of delay is high as compared to the rate of change of delay of MLGNR with increase in interconnect length.

Table 3.8 MLGNR/Cu delay ratio from 500–2000µm length with different levels of Fermi energies at 32nm technological node of MLGNR

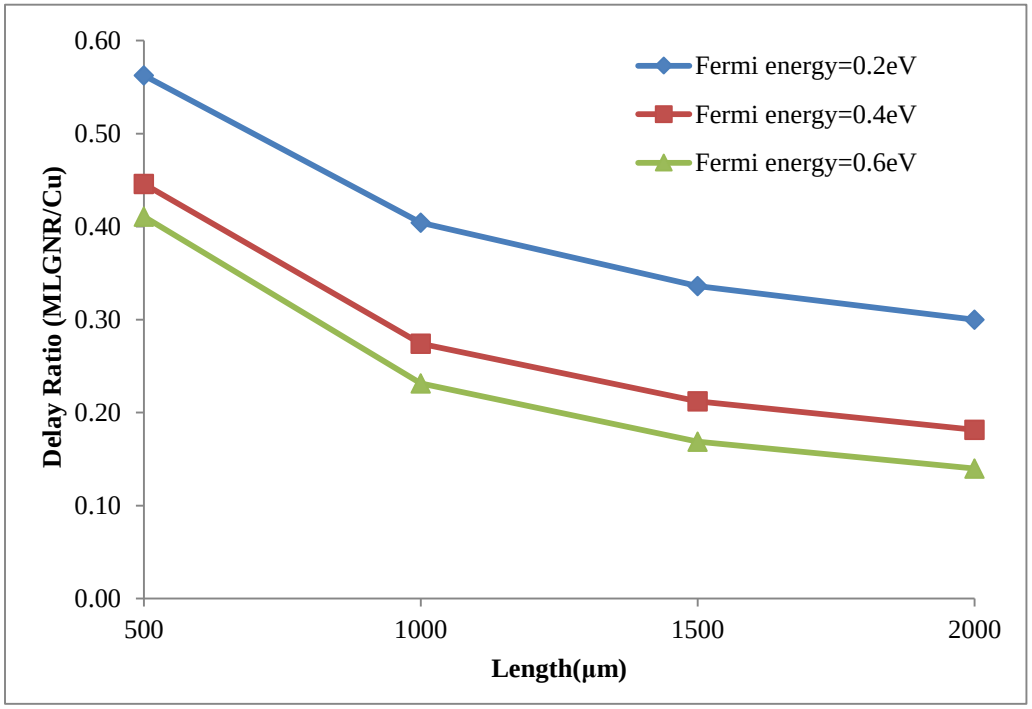
Length (µm)	Delay (ns)				Delay Ratio (MLGNR/Cu)		
	MLGNR			Cu			
	E_f=0.2eV	E_f=0.4eV	E_f=0.6eV		E_f=0.2eV/ Cu	E_f=0.4eV/ Cu	E_f=0.6eV/ Cu
500	0.0570	0.0452	0.0416	0.1013	0.5625	0.4460	0.4109
1000	0.0991	0.0672	0.0568	0.2452	0.4043	0.2741	0.2316
1500	0.1543	0.0974	0.0776	0.4592	0.3361	0.2121	0.1689
2000	0.2221	0.1345	0.1037	0.7406	0.2999	0.1816	0.1400

Table 3.9 MLGNR/Cu delay ratio from 500–2000µm length with different levels of Fermi energies at 22nm technological node of MLGNR

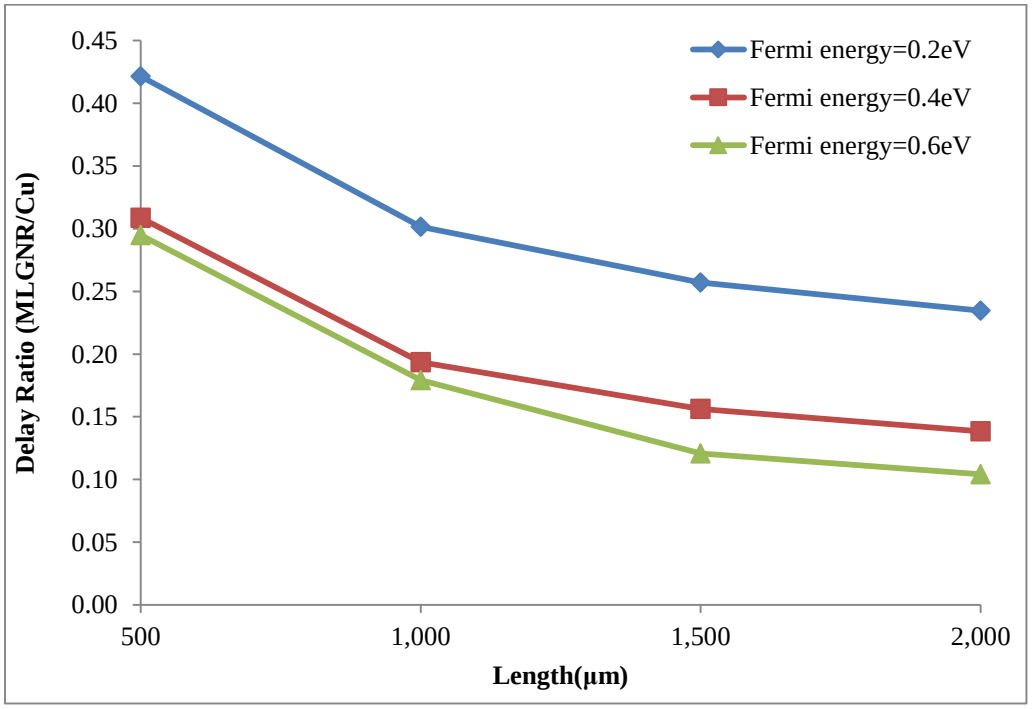
Length (µm)	Delay (ns)				Delay Ratio (MLGNR/Cu)		
	MLGNR			Cu			
	E_f=0.2eV	E_f=0.4eV	E_f=0.6eV		E_f=0.2eV/ Cu	E_f=0.4eV/ Cu	E_f=0.6eV/ Cu
500	0.08096	0.05925	0.05661	0.19207	0.42152	0.30850	0.29472
1000	0.16132	0.10353	0.09584	0.53505	0.30150	0.19350	0.17912
1500	0.26935	0.16380	0.12651	1.04820	0.25696	0.15627	0.12069
2000	0.40497	0.23884	0.18009	1.72700	0.23449	0.13830	0.10428

Table 3.10 MLGNR/Cu delay ratio from 500–2000µm length with different levels of Fermi energies at 16nm technological node of MLGNR

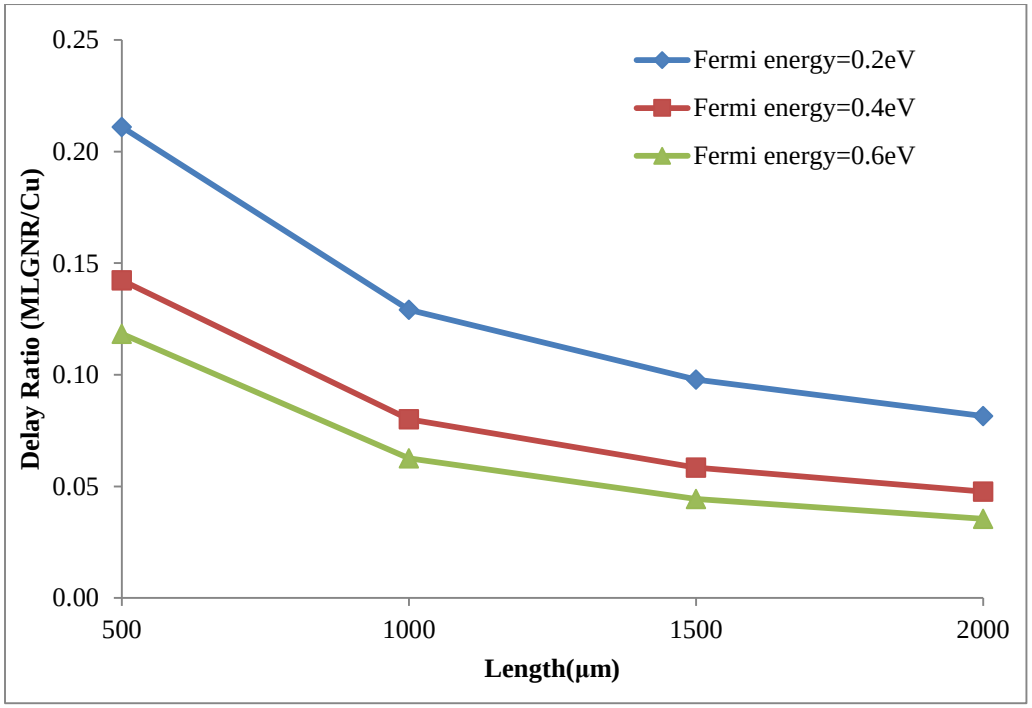
Length (µm)	Delay (ns)				Delay Ratio (MLGNR/Cu)		
	MLGNR			Cu			
	E_f=0.2eV	E_f=0.4eV	E_f=0.6eV		E_f=0.2eV/ Cu	E_f=0.4eV/ Cu	E_f=0.6eV/ Cu
500	0.18788	0.12668	0.10543	0.89021	0.21105	0.14230	0.11843
1000	0.33744	0.20923	0.16340	2.61250	0.12916	0.08009	0.06255
1500	0.50953	0.30438	0.23090	5.20510	0.09789	0.05848	0.04436
2000	0.70604	0.41249	0.30765	8.66270	0.08150	0.04762	0.03551


0.60
0.50
0.40
0.30
0.20
0.10
0.00
Delay Ratio (MLGNR/Cu)
500
1000
1500
2000
Length(µm)
Fermi energy=0.2eV
Fermi energy=0.4eV
Fermi energy=0.6eV

(a)


0.45
0.40
0.35
0.30
0.25
0.20
0.15
0.10
0.05
0.00
Delay Ratio (MLGNR/Cu)
500
1,000
1,500
2,000
Length(µm)
Fermi energy=0.2eV
Fermi energy=0.4eV
Fermi energy=0.6eV

(b)



(c)

Figure 3.14 MLGNR and copper delay ratio with different levels of Fermi energies at (a) 32nm, (b) 22nm, and (c) 16nm nodes of technology as a function of length

Similarly, MLGNRs PDP is smaller than the copper interconnects for three various nodes of technology at global lengths; shown in Tables 3.11–3.13.

Table 3.11 MLGNR/Cu PDP ratio from 500–2000µm length with different levels of Fermi energies at 32nm technological node of MLGNR

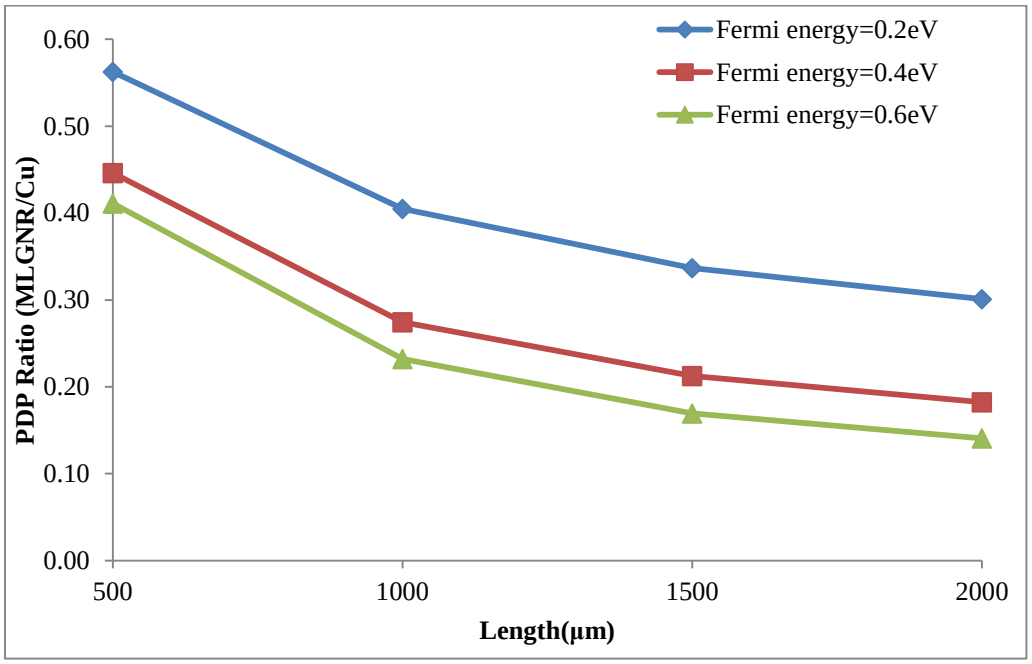
Length (µm)	PDP (ns-µW)				PDP Ratio (MLGNR/Cu)		
	MLGNR			Cu			
	E_f=0.2eV	E_f=0.4eV	E_f=0.6eV		E_f=0.2eV/ Cu	E_f=0.4eV/ Cu	E_f=0.6eV/ Cu
500	14.148	11.221	10.338	25.14742	0.56259	0.44619	0.41111
1000	24.603	16.683	14.102	60.79489	0.40469	0.27441	0.23197
1500	38.273	24.170	19.258	113.6596	0.33674	0.21265	0.16943
2000	55.056	33.374	25.742	182.9037	0.30101	0.18247	0.14074

Table 3.12 MLGNR/Cu PDP ratio from 500–2000µm length with different levels of Fermi energies at 22nm technological node of MLGNR

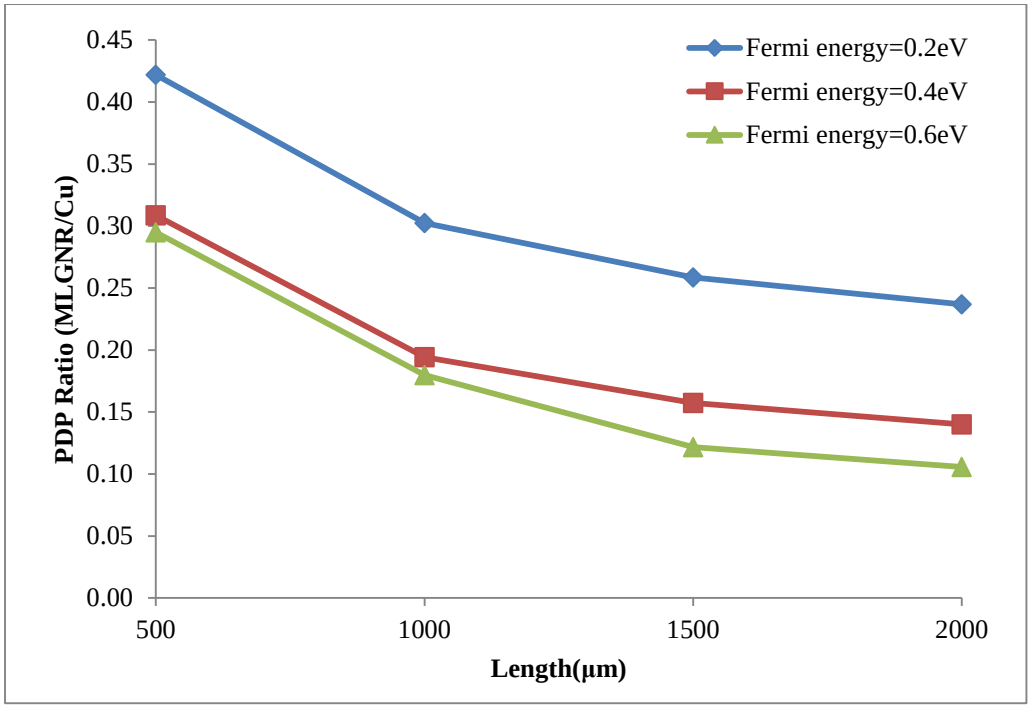
Length (µm)	PDP (ns-µW)				PDP Ratio (MLGNR/Cu)		
	MLGNR			Cu	E_f=0.2eV/ Cu	E_f=0.4eV/ Cu	E_f=0.6eV/ Cu
	E_f=0.2eV	E_f=0.4eV	E_f=0.6eV				
500	13.6962	10.0224	9.5790	32.47095	0.42180	0.30866	0.29500
1000	27.2675	17.5117	16.2126	90.2028	0.30229	0.19414	0.17974
1500	45.4778	27.6906	21.3957	175.9528	0.25847	0.15738	0.12160
2000	68.2834	40.3485	30.4432	288.2	0.23693	0.14000	0.10563

Table 3.13 MLGNR/Cu PDP ratio from 500–2000µm length with different levels of Fermi energies at 16nm technological node of MLGNR

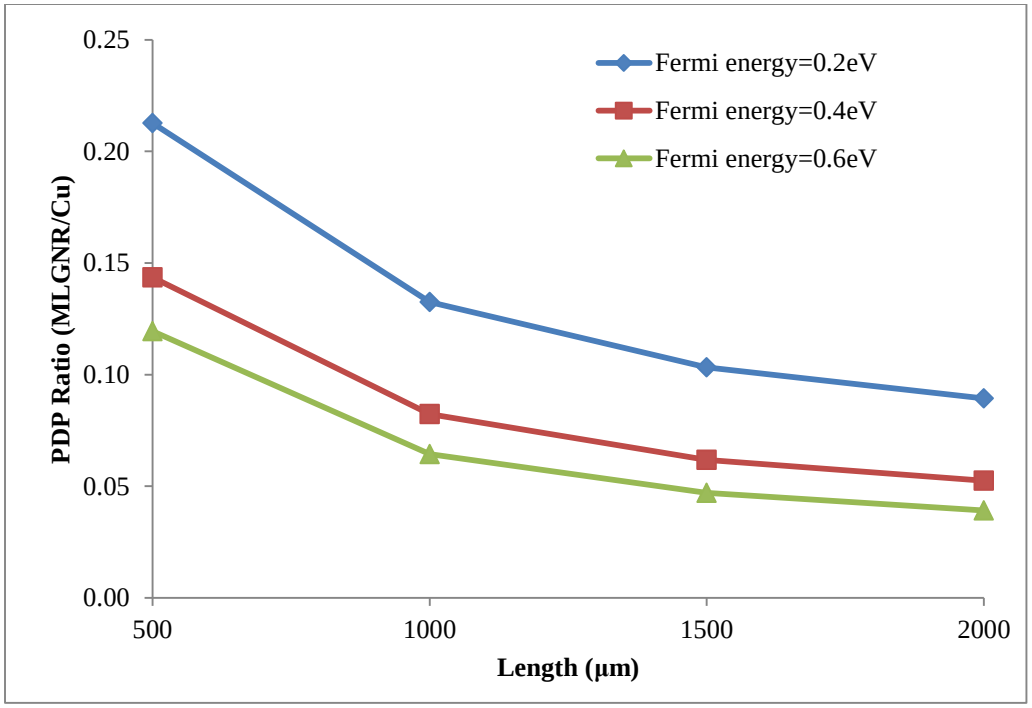
Length (µm)	PDP (ns-µW)				PDP Ratio (MLGNR/Cu)		
	MLGNR			Cu	E_f=0.2eV/ Cu	E_f=0.4eV/ Cu	E_f=0.6eV/ Cu
	E_f=0.2eV	E_f=0.4eV	E_f=0.6eV				
500	112.8363	76.14979	63.39534	530.4026	0.21274	0.14357	0.11952
1000	202.232	125.6345	98.17982	1526.134	0.13251	0.08232	0.06433
1500	304.6422	182.5414	138.6196	2950.587	0.10325	0.06187	0.04698
2000	421.0105	247.0331	184.5201	4712.605	0.08934	0.05242	0.03915



(a)



(b)



(c)

Figure 3.15 MLGNR/Cu PDP ratio with different levels of Fermi energies at (a) 32nm, (b) 22nm, and (c) 16nm nodes of technology as a function of length

The PDP ratio reduced for length 500–2000µm at 32nm technological node because of rise in the value of copper in denominator, as given in Table 3.11 as well as graphically shown in

Figure 3.15(a). The different levels of Fermi energies shows improvement in PDP ratio at global lengths. Further, it is also examined for 22nm, and 16nm technological nodes as presented in Tables 3.12 and 3.13 and graphically in Figures 3.15(b) and (c) respectively. It is observed that PDP improves due to intercalation doping with different levels of Fermi energies at three different technological nodes. Therefore, it is revealed from the results that the MLGNR is a better interconnect material than copper at global interconnect lengths for 16nm, 22nm, and 32nm nodes of technology.

3.4 Chapter Summary

Signal delay as well as PDP at 16nm, 22nm, and 32nm nodes of technology for global lengths was analyzed for MLGNR interconnects. With the help of analytical equations ESC model for the MLGNR interconnects is presented. The results reveals that the intercalation doping improves the conductivity of the MLGNR, thereby improves delay and PDP at global lengths from 500–2000μm for three different nodes of technology and the simulation parameters based on the ITRS 2013 version has been used. The percentage reduction in delay from 0.2eV to 0.6eV is 56%, 55%, 53% and PDP is 57%, 56%, 54% at length 2000μm for 16nm, 22nm, and 32nm nodes of technology respectively of MLGNR. Moreover, the delay and PDP ratio contrasts MLGNR and copper interconnects. It is evaluated from the results that the performance of MLGNR is superior than copper interconnect at global levels for all three various nodes of technology. Reasonable doping and speculative edges are required to render the MLGNR an appropriate material as interconnect than copper at global levels. Hence, the MLGNR are good option for VLSI-ICs in on-chip interconnects for electronic applications of the next decade.

Publication from this chapter

- Himanshu Sharma and Karmjit Singh Sandha, "Impact of Intercalation Doping on the Conductivity of Multi-layer Graphene Nanoribbon in On-Chip Interconnects," *Journal of Circuits, Systems and Computers, World Scientific*, Volume 29, Issue 12, pp. 2050185-1–20501852-2, September 2020. (SCIE indexed-Impact Factor- 1.278)
- Himanshu Sharma and Karmjit Singh Sandha, "Multilayer Graphene Nanoribbon (MLGNR) as VLSI Interconnect at Nano-scaled Technology Nodes," *Transactions on Electrical and Electronics Materials, Springer*, Volume 19, Issue 6, pp. 456–461, December 2018. (SCOPUS indexed)

CHAPTER 4

TEMPERATURE-DEPENDENT CIRCUIT MODEL AND PERFORMANCE ANALYSIS OF MLGNR INTERCONNECT

This chapter explores the influence of temperature on the scattering mechanism of multilayer graphene nanoribbon. A thermally aware electrical ESC model along with mathematical computations is presented for evaluating the parasitic parameters and reports the performance analysis dependent on temperature of the MLGNR at global lengths for 32nm, 22nm, and 16nm nodes of technology.

4.1 Introduction

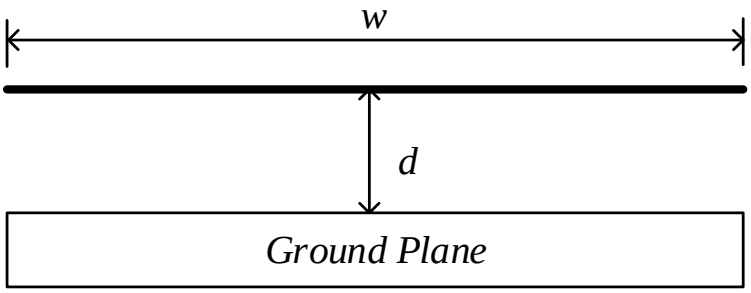
Recently, the demand for high-speed VLSI ICs reduced the chip size and increased the number of active circuits inside the ICs. With the downscaling of technology nodes, impacts of temperature on the interconnects is a key issue in designing next-generation VLSI ICs. The current density and variation of temperature affects the performance of the ICs. Therefore, the tedious process parameters at nano-scaled technological nodes in the thermally variable environment can damage and effect the IC operations. As a result, the impact of temperature on the electronic circuits should be analyzed. To understand the influence of temperature, its reliability should be examined considering the industrial applications [20, 79, 103].

The performance of ICs is mainly affected by their inconsistency to function in different temperature conditions (200K to 500K) [106]. This thermally aware variable environment has a major impact on power dissipation and signal delay, which are the performance parameters of interconnects [53]. The temperature variation above room temperature, affects the efficiency of nano-scale interconnects and it is required to estimate and analyze the MLGNRs actual performance under a thermally variable conditions. In this chapter, the temperature impact on the parasitic parameters of MLGNR as interconnect material is presented. The scaling of technological nodes introduces scattering due to surface as well as grain boundary because of the small grain size in nano-scaled wires and grain size is in the same order with respect to the thickness of wire. The meaning of small grain size is the number of electrons passing through grain boundaries more often and experience large scatterings. The temperature has significant impact on electron surface and grain boundary

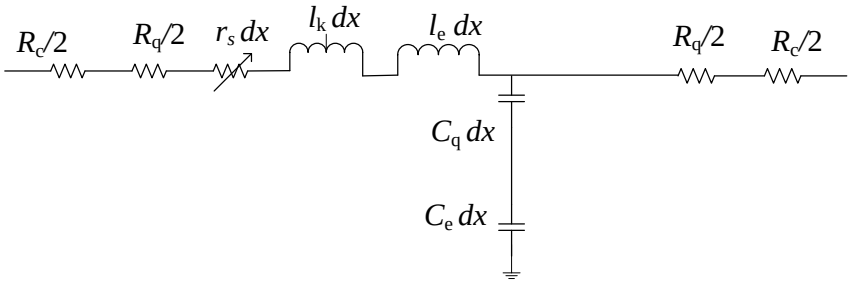
scattering. In GNR, the scattering mechanism is of two types: electron–phonon and electron–electron scattering. The electron–phonon scattering is crucial when compared with electron–electron scattering with increase in temperature and affects the effective MFP of MLGNR. The electron–phonon scattering is classified into acoustic, optical and zone boundary scatterings. The scattering mechanism lowers transmission of signal which further effects the image quality created through the imaging sensors [119]. The detailed mathematical model for evaluating the temperature-dependent parasitic parameters and effects of temperature on the scattering mechanism (acoustic phonon, optical and zone boundary scattering) of MLGNR is presented in this chapter [53, 103, 120].

4.2 Impedance model (Temperature dependent) of MLGNR

Under this section, temperature dependent analytical model is presented for MLGNR. The basic structure of SLGNR as interconnect is shown in Figure 4.1(a). Initially, the parasitic parameters such as capacitance resistance, and inductance are derived for SLGNR from its equivalent circuit model; depicted in Figure 4.1(b).



(a)



(b)

Figure 4.1 (a) Geometrical view of SLGNR interconnect (b) Equivalent circuit of an SLGNR

The GNR interconnect comprises of three different resistive components: r_s, R_q, R_c are defined as scattering resistance, quantum resistance and contact resistance respectively. The contact resistance occurs owing to the contact of the metal with MLGNR, which is quite small; in the range of few hundred of ohms to tens of kilo ohm, relies on the fabrication process [104, 111, 121, 122]. The resistance of one graphene sheet is much larger as compare to R_c. In MLGNR, each layer contributes to total current conduction, therefore its impact is negligible small and is excluded for this research. The quantum resistance (R_q) is linked with GNR having smaller length compared to the effective MFP (λ_{eff}) of electrons, and discussed in chapter 3. It is reported in literature [96, 116] that the performance of the metallic ac-GNR is better than the zz-GNR that is presumed in this research and also discussed in chapter 3. Further, it is presented that doped MLGNR with complete specular edges gives better performance than neutral one in chapter 3.

4.2.1 Scattering Resistance (r_s)

If the GNR length is more as compared to its effective MFP (λ_{eff}), there is an another resistance i.e. scattering resistance of GNR. The scattering resistance of SLGNR depending on temperature in p.u.l. (per unit length) is shown by equation 4.1 [123],

$$r_s = \frac{h}{2e^2 N_{ch_{GNR}} \lambda_{eff}(T)} = \frac{12.9}{N_{ch_{GNR}} \lambda_{eff}(T)} \quad (k\Omega) \tag{4.1}$$

Equation 4.1 demonstrates that λ_{eff} primarily relies on the scattering mechanism of the electron and phonon for determining the scattering resistance. Relative to the electron-electron scattering, the electron-phonon scattering plays a significant role [123]. Further, the electron-phonon scattering relies on the optical and zone boundary and acoustic phonon scattering. Hence, in SLGNR the effective MFP (λ_{eff}) of electrons dependent on temperature is given by,

$$\frac{1}{\lambda_{eff}(T)} = \frac{1}{\lambda^{AC}} + \frac{1}{\lambda^{OZB}} + \frac{1}{\lambda_d} + \frac{1}{\lambda_r} \tag{4.2}$$

where acoustic MFP because of acoustic phonon scattering is defined by λ^{AC}, MFP due to optical and zone boundary scattering is represented by λ^{OZB}. Edge and defect scattering is also presented with temperature dependent scattering mechanism in equation 4.2, where λ_d is the MFP caused due to defect and impurity scattering and λ_r is the MFP because of edge scattering. The role of edge scattering as well as defect scattering has been discussed in chapter 3. At low to room temperature, the GNR interconnect resistance relies upon the λ^{AC}. The scattering due to acoustic and optical phonons is basically the vibrations from the lattice structure induced due to the thermal variable conditions. Equation 4.3 is used to calculate λ^{AC} [123],

$$\lambda^{\mathrm{AC}} = 4\frac{\rho_{\mathrm{m}}\left(\frac{h}{2\pi}v_{\mathrm{f}}v_{\mathrm{s}}\right)^2}{\sqrt{\pi N_{\mathrm{s}}}D_{\mathrm{AC}}^2 K_{\mathrm{B}}T} \tag{4.3}$$

Where ρ_{m} is the graphene mass density having 7.6×10^{-7} Kg/m^2, v_{s} defines the acoustic phonons speed (20 Km/s), N_{s} is 2-D electron gas concentration in GNR having 4×10^{16}/m^2 as a approximate value and D_{AC} is acoustic deformation potential having 8eV [123]. This can be seen from equation 4.3 that acoustic mean free path is inversely proportional to temperature.

At low to room temperature the impact of optical and zone boundary (OZB) scattering is negligible. However, the impact of OZB scattering on the MFP is non-negligible at high temperatures and it needs to be evaluated to understand the actual performance of an interconnect. The scattering due to optical-zone boundary takes place when the required energy is absorbed by the electron from another optical or zone boundary phonon. Equation 4.4 is used to calculate MFP due to λ^{OZB} [123],

$$\frac{1}{\lambda^{\mathrm{OZB}}} = \frac{1}{\lambda_{\mathrm{abs}}^{\mathrm{op}}} + \frac{1}{\lambda_{\mathrm{emm}}^{\mathrm{op}}} \tag{4.4}$$

Where $\lambda_{\mathrm{abs}}^{\mathrm{op}}$, $\lambda_{\mathrm{emm}}^{\mathrm{op}}$ defines the scattering due to optical phonon (absorption) and optical phonon (emission) respectively. $\lambda_{\mathrm{abs}}^{\mathrm{op}}$ corresponds to the scattering impact due to phonon absorption and $\lambda_{\mathrm{emm}}^{\mathrm{op}}$ corresponds to the distance that electron travels before emitting the phonon are calculated by equations 4.5 and 4.6 [123], respectively.

$$\lambda_{\mathrm{abs}}^{\mathrm{op}} = \frac{\rho_{\mathrm{m}}\frac{h}{2\pi}w_{\mathrm{op}}v_{\mathrm{f}}^2}{\sqrt{\pi N_{\mathrm{s}}}D_{\mathrm{op}}^2 N_{\mathrm{op,abs}}\left(1+\frac{w_{\mathrm{op}}}{v_{\mathrm{f}}\sqrt{\pi N_{\mathrm{s}}}}\right)} \tag{4.5}$$

$$\lambda_{\mathrm{emm}}^{\mathrm{op}} = \frac{\rho_{\mathrm{m}}\frac{h}{2\pi}w_{\mathrm{op}}v_{\mathrm{f}}^2}{\sqrt{\pi N_{\mathrm{s}}}D_{\mathrm{op}}^2 N_{\mathrm{op,emm}}\left(1-\frac{w_{\mathrm{op}}}{v_{\mathrm{f}}\sqrt{\pi N_{\mathrm{s}}}}\right)} \tag{4.6}$$

Where $\frac{h}{2\pi}w_{\mathrm{op}}$ defines the optical phonon energy having 160 meV, $N_{\mathrm{op,emm}}$ and $N_{\mathrm{op,abs}}$ are the phonon occupation numbers specified by Bose-Einstein statistics for emission and absorption processes respectively and D_{op} defines the optical deformation potential with 2×10^{11} eV/m. The optical phonon number is denoted by N_{op}. Equation 4.7 is used to calculate N_{op}.

$$N_{op} = \frac{1}{e^{\frac{\frac{h}{2\pi}w_{op}}{K_B T}} - 1} \tag{4.7}$$

From equation 4.2, λ_d, λ_r are the MFP due to defects and edge scatterings respectively. In this research, complete specular edges are assumed and specular edges depends on *p* as discussed in chapter 3. For complete specular edges *p* is 1 and its impact is zero as discussed in chapter 3. The MFP due to λ_d for SLGNR is 1µm and 419nm for MLGNR. The impact of λ_d is limited rather than the scattering due to acoustic as well as optical phonons because of the different thermal environment conditions. Therefore, it is concluded the effects of λ_d, and λ_r are negligibly small and can be neglected. Hence, effective MFP of SLGNR is given by equation 4.8.

$$\frac{1}{\lambda_{eff}(T)} = \frac{1}{\lambda^{AC}} + \frac{1}{\lambda^{OZB}} \tag{4.8}$$

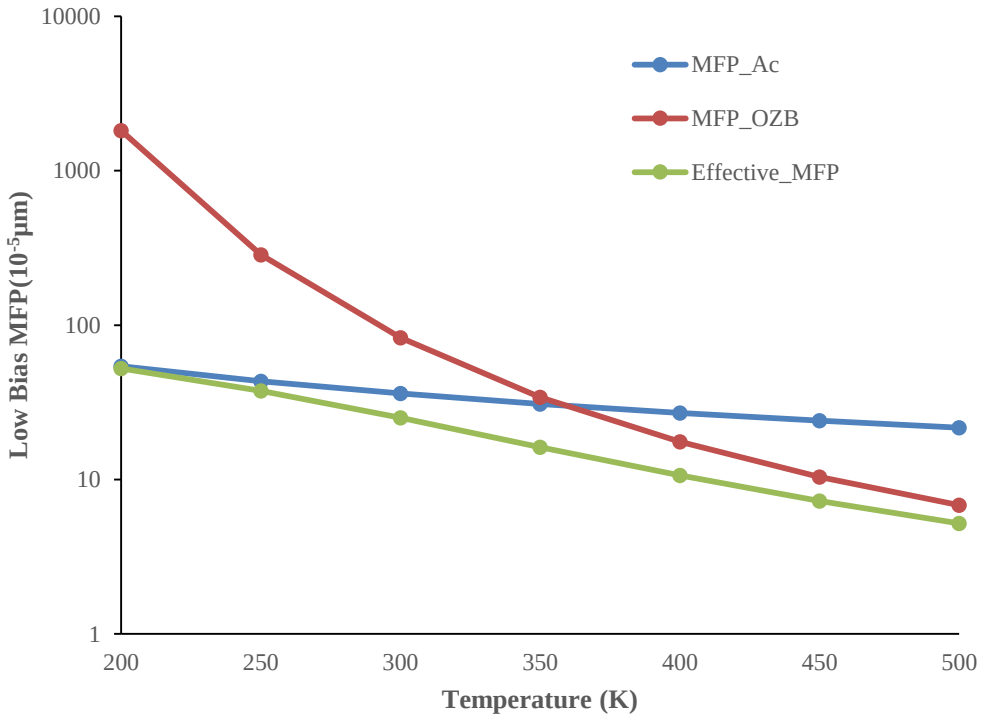


Figure 4.2 MFP of different scatterings in SLGNR (Temperature dependent)

Figure 4.2 demonstrates the effective MFP dependent on temperature with various scatterings in single layer GNR. The acoustic scattering impact is dominating from low to room temperature (200–300K) can be seen in Figure 4.2, as the optical phonon scattering value is very high and has a negligible effect on λ_{eff}. But above 300K temperature, the optical phonon

scattering shows the exponentially significant decline as temperature increases, therefore it has a significant effect on 300–500K temperature range. The effect of optical phonon scattering plays an essential role along with acoustic scattering at high temperatures. The effective MFP dependent on temperature is seen as a solid line in SLGNR (low bias). Effective MFP is affected by different temperature levels and exhibits a major role for evaluating the total resistance (temperature dependent) of the SLGNR at long interconnects provided by the equation 4.9,

$$R_{\mathrm{SLGNR}} = R_{\mathrm{q}} + r_{\mathrm{s}} = \frac{12.9}{N_{\mathrm{ch_{GNR}}}}\left(1 + \frac{l}{\lambda_{\mathrm{eff}}(T)}\right) \tag{4.9}$$

The performance of SLGNR is not better than the MLGNR because of high resistance [85]. Hence, MLGNR is presented as discussed in chapter 3, by stacking two or more layers of SLGNR in a parallel combination. SLGNRs used in parallel combination for MCC (Multi Conductor Circuit) or the MTL (Multi-Conductor Transmission line) model of MLGNR interconnects (Figure 4.3) [34].

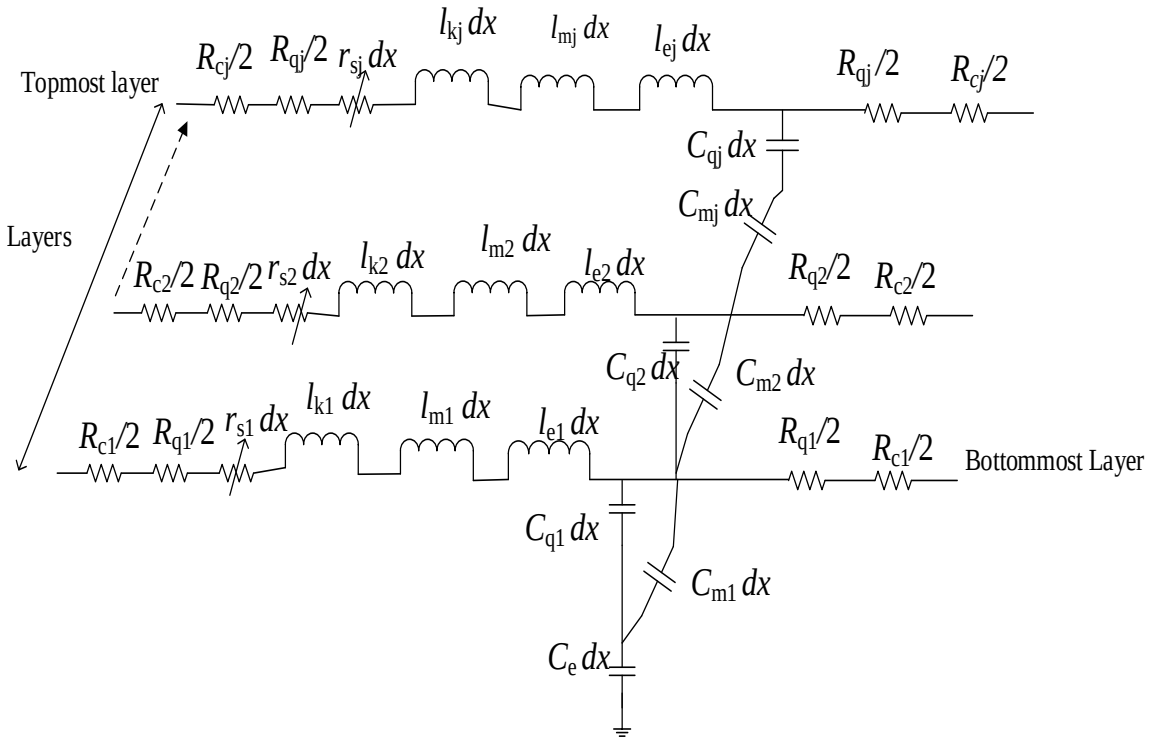


Figure 4.3 Temperature dependent equivalent MCC of MLGNR

To calculate the number (n) of conducting layers of MLGNR is discussed and presented in chapter 3.

The total resistance (temperature dependent) of MLGNR is given by equation 4.10 [123],

$$R_{\mathrm{MLGNR}} = \frac{R_{\mathrm{q}} + r_{\mathrm{s}}}{n} = \frac{12.9}{n.N_{\mathrm{ch_{GNR}}}}\left(1 + \frac{l}{\lambda_{\mathrm{eff}}(T)}\right) \tag{4.10}$$

4.2.2 Equivalent Inductance/Capacitance

The impedance parameters of GNR i.e. capacitance and inductance are presented in this section as defined in the literature [104, 105, 123]. The GNR interconnect has magnetic and kinetic inductance. The GNR l_{k} (kinetic inductance) is produced by kinetic energy due to the motion of electrons in conducting channels. The l_{e} (magnetic inductance) comes from the different levels of electric current in a wire that varies with time that generates a magnetic field around it. The p.u.l. inductance (l_{e} and l_{k}) of MLGNR interconnect are analyzed by equations 4.11 as well as 4.12 [85, 104, 105, 111, 123],

$$l_{\mathrm{e}} = \frac{\mu_{\mathrm{o}} d}{w} \tag{4.11}$$

$$l_{\mathrm{k}} = \frac{8}{n\alpha w E_{\mathrm{f}}} \quad (\mathrm{nH/\mu m}) \tag{4.12}$$

where μ_{o} is defined as the free space magnetic permeability. The adjacent MLGNR layers may function as two parallel-plate capacitors that constitute interlayer coupling capacitance (C_{m}) as well as coupling inductance (l_{m}). Moreover, each GNR layer contains C_{q} (quantum capacitance) as well as C_{e} (electrostatic capacitance). The coupling capacitance and inductance is negligibly smaller as compared to quantum capacitance and kinetic inductance, respectively [123], and is neglected in this research. The p.u.l. capacitance (electrostatic and quantum) of the MLGNR interconnect material can be given by equations 4.13 and 4.14, respectively [85, 104, 105, 111, 123],

$$C_{\mathrm{e}} = \frac{\varepsilon_{\mathrm{o}} w}{d} \tag{4.13}$$

$$C_{\mathrm{q}} = 0.1 N_{\mathrm{ch_{GNR}}}\left[1 + \sqrt{1 + 1/\alpha\beta E_{\mathrm{f}}}\right] \quad (\mathrm{fF/\mu m}) \tag{4.14}$$

where ε_{o} defines the free space relative permittivity.

Based on the aforesaid parasitic parameters, the equivalent circuit of MLGNR interconnect (length dependent), can be modeled into a thermally aware equivalent single conductor

transmission model; shown in Figure 4.4, and its equivalent parameters are specified by equations 4.15, 4.16 and 4.17,

$$R_{\mathrm{ESC}} = R_{\mathrm{MLGNR}} = \frac{12.9}{nN_{\mathrm{ch\ GNR}}}\left(1+\frac{l}{\lambda_{\mathrm{eff}}(T)}\right) \tag{4.15}$$

$$L_{\mathrm{ESC}} = l_{\mathrm{k}} + l_{\mathrm{e}} \tag{4.16}$$

$$C_{\mathrm{ESC}} = (C_{\mathrm{q}}^{-1} + C_{\mathrm{e}}^{-1})^{-1} \tag{4.17}$$

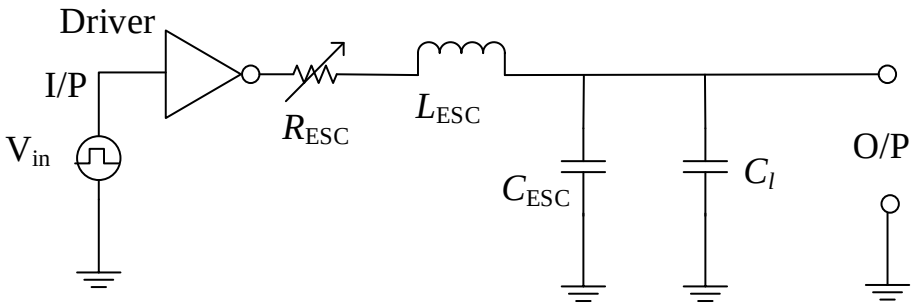
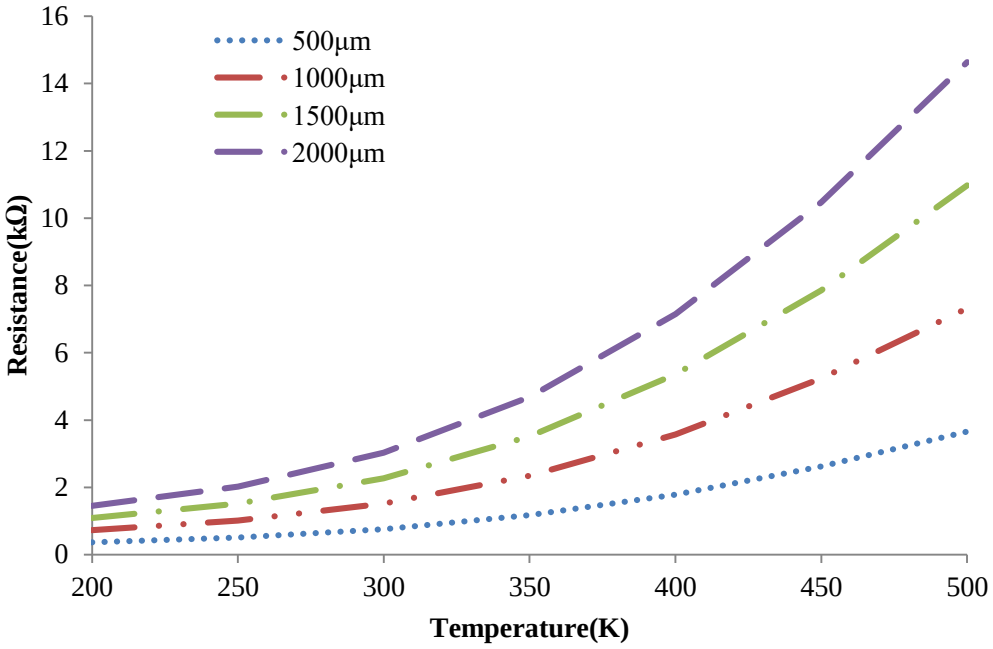


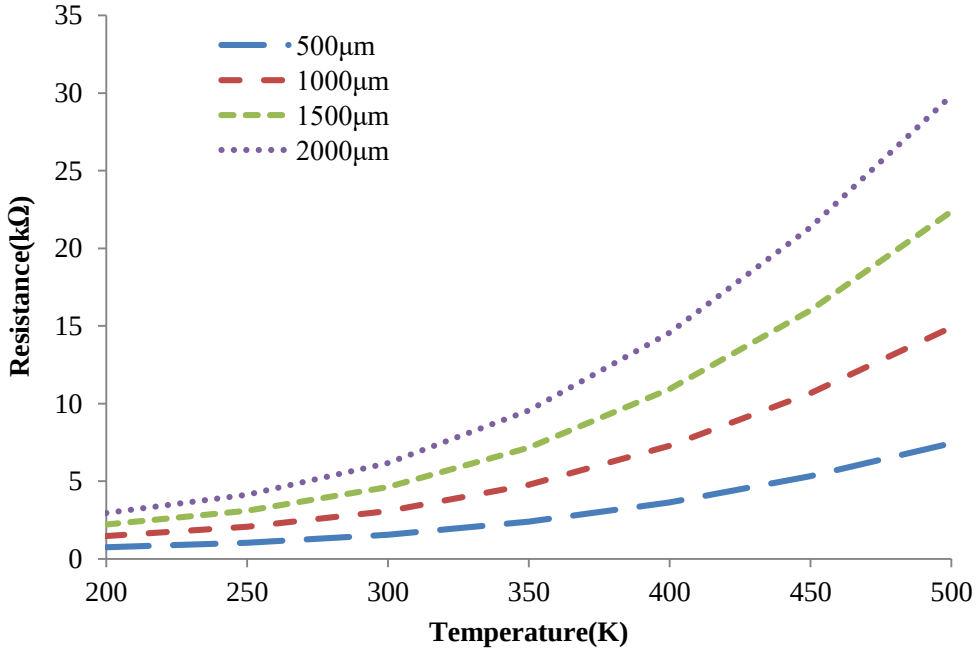
Figure 4.4 Thermally aware ESC model of MLGNR driven by CMOS driver

4.3 Performance analysis of MLGNR interconnects (Temperature dependent)

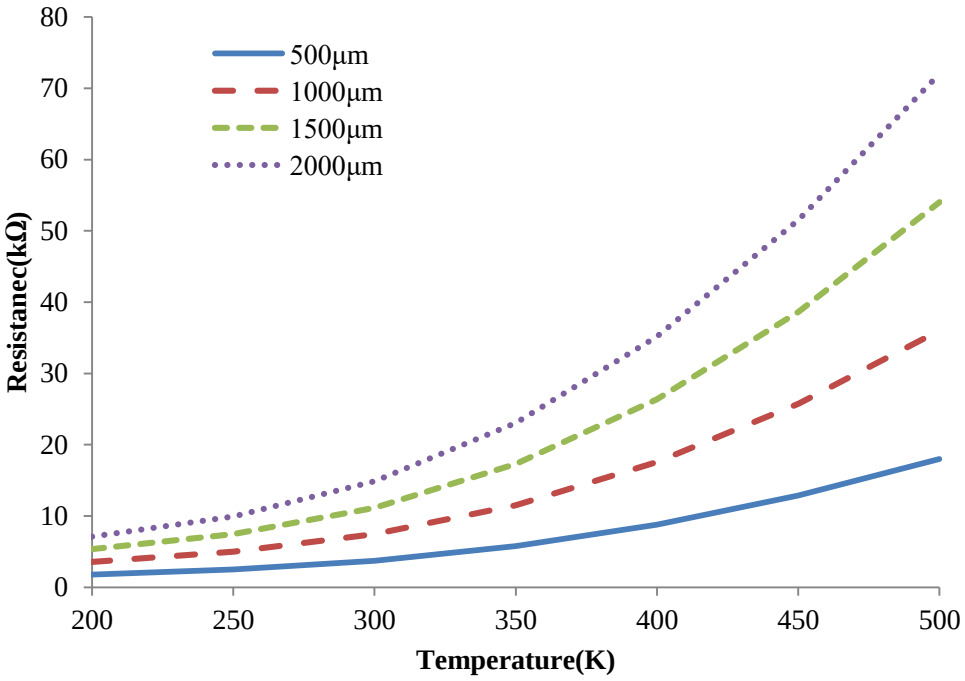
In this portion, impedance and performance analysis dependent on temperature of MLGNR are observed for three different nodes of technology i.e. 32nm, 22nm and 16nm. As elaborated, the effective MFP has a significant impact on the parasitic parameters of GNR, which further influence its performance parameters, i.e. power dissipation, delay, and PDP over 200–500K temperature range. Equations 4.1 to 4.9 are used to calculate the effective MFP of GNR. MLGNR resistance is evaluated by equation 4.10 from the calculated effective MFP of electrons, coded in MATLAB computing software for all three nodes of technology at global lengths (500–2000μm). The parameters of simulation for precise calculations are derived from ITRS 2013 and presented in Table 3.1 of chapter 3 for three different technological nodes. The resistance of MLGNR rises with increase in temperature ranging in 200–500K at global interconnect levels for 32nm, 22nm and 16nm nodes of technology, depicted in Figures 4.5(a)–(c) respectively.


500µm
1000µm
1500µm
2000µm
Resistance(kΩ)
Temperature(K)
0
2
4
6
8
10
12
14
16
200
250
300
350
400
450
500

(a)


500µm
1000µm
1500µm
2000µm
Resistance(kΩ)
Temperature(K)
0
5
10
15
20
25
30
35
200
250
300
350
400
450
500

(b)



(c)

Figure 4.5 MLGNR resistance (temperature dependent) at global lengths from 500–2000µm for (a) 32nm, (b) 22nm, and (c) 16nm nodes of technology

In addition, it is also analyzed that shrinking of effective MFP takes place with the increase in temperature at longer interconnects for three various nodes of technology, therefore resistance of MLGNR rises dramatically following 300K.

For all three nodes of technology, SPICE simulation tool is used for analyzing the performance of MLGNR interconnects dependent on temperature from power dissipation, delay and PDP perspectives.

4.3.1 Signal delay analysis

The ESC model is taken into consideration for evaluating and analyzing the MLGNR performance from power dissipation, signal delay, and PDP perspectives, as described in Figure 4.4. For three different nodes of technology, the equivalent circuit transmission model is driven by a CMOS driver, and C_l as load capacitance having 0.01fF. For analyzing the MLGNR performance, a SPICE simulation tool is used using driver interconnect load (Figure 3.11), to simulate the parasitic parameters (temperature dependent) of MLGNR.

The thermally aware delay of MLGNR is analyzed for 32nm, 22nm, and 16nm nodes of technology at 2000µm length as shown in Table 4.1 and graphically in Figure 4.6

Table 4.1 Delay (Temperature dependent) of MLGNR for 32nm, 22nm, and 16nm nodes of technology at 2000μm length

Temperature (K)	Delay (ns)		
	32nm	22nm	16nm
200	0.0468	0.0735	0.1301
250	0.0552	0.0893	0.1676
300	0.0699	0.1151	0.2275
350	0.0920	0.1545	0.3204
400	0.1223	0.2092	0.4511
450	0.1610	0.2793	0.6203
500	0.2075	0.3638	0.8264

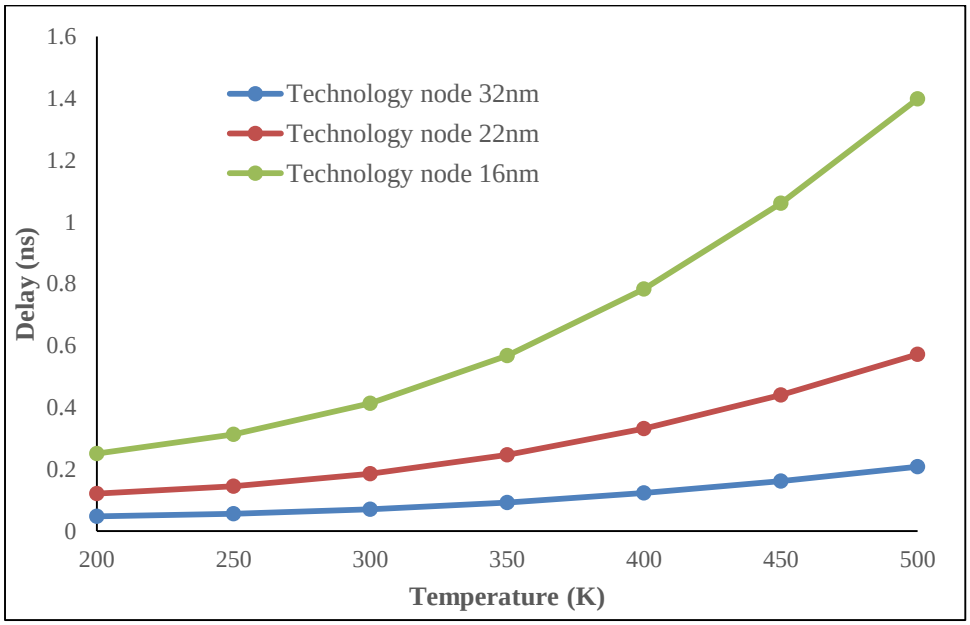


Figure 4.6 Delay (Temperature dependent) of MLGNR for 32nm, 22nm, and 16nm technological nodes at 2000μm length

It is analyzed that with the rise in temperature (200–500K), the shrinking of effective MFP takes place which increases the delay of MLGNR at 2000μm for three different nodes of technology. The delay of MLGNR at 2000 μm is roughly linear from 200–300K, but sharply increasing after 300K due to the shrinking of effective MFP.

4.3.2 PDP analysis

Nowadays, in interconnects the role of power has become a significant issue as well as major

concern with the growth of VLSI industry. Power is basically the heat dissipation corresponding to charging as well as discharging of wire capacitances. Power dissipation of MLGNR over 200–500K at 2000µm interconnect length for three different technological nodes

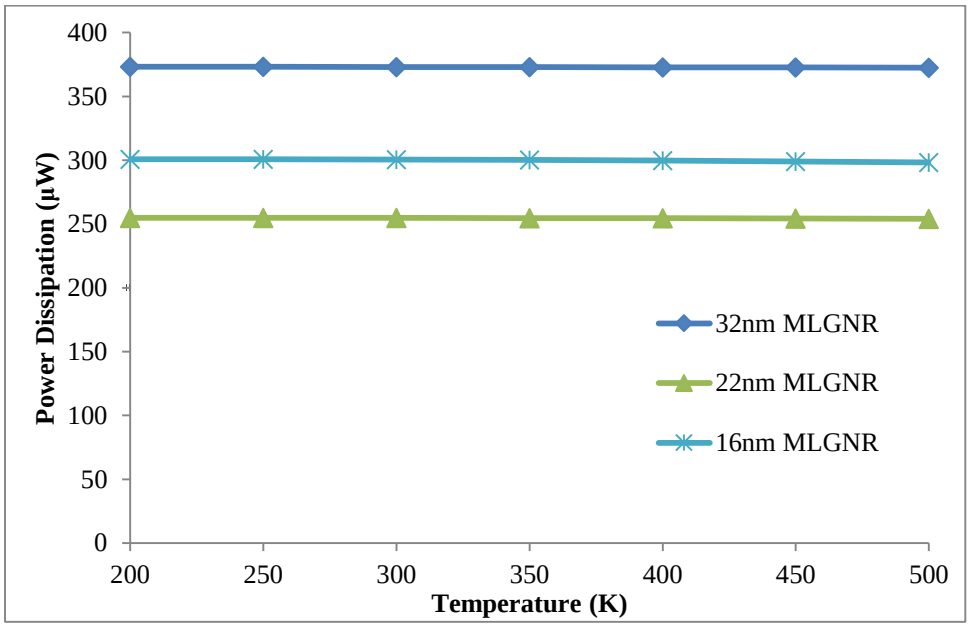


Figure 4.7 Power dissipation of MLGNR for 32nm, 22nm, and 16nm technological nodes at 2000µm length

is shown in Figure 4.7. The overall efficiency of an interconnect depends on the product of power dissipation and signal delay. PDP of MLGNR at 2000µm length for three different nodes of technology is shown in Table 4.2 and graphically depicted in Figure 4.8 over 200–500K temperature range. The MLGNR PDP is consistent for all three nodes of technology from 200

Table 4.2 PDP (Temperature dependent) of MLGNR for 32nm, 22nm, and 16nm nodes of technology at 2000µm length

Temperature (K)	PDP (ns-µW)		
	32nm	22nm	16nm
200	17.48422	18.73744	39.15068
250	20.719	22.77996	50.39186
300	26.11599	29.3353	68.38464
350	34.33941	39.35077	96.1924
400	45.63319	53.25141	135.2216
450	60.0122	71.03069	185.562
500	77.30032	92.42872	246.5696

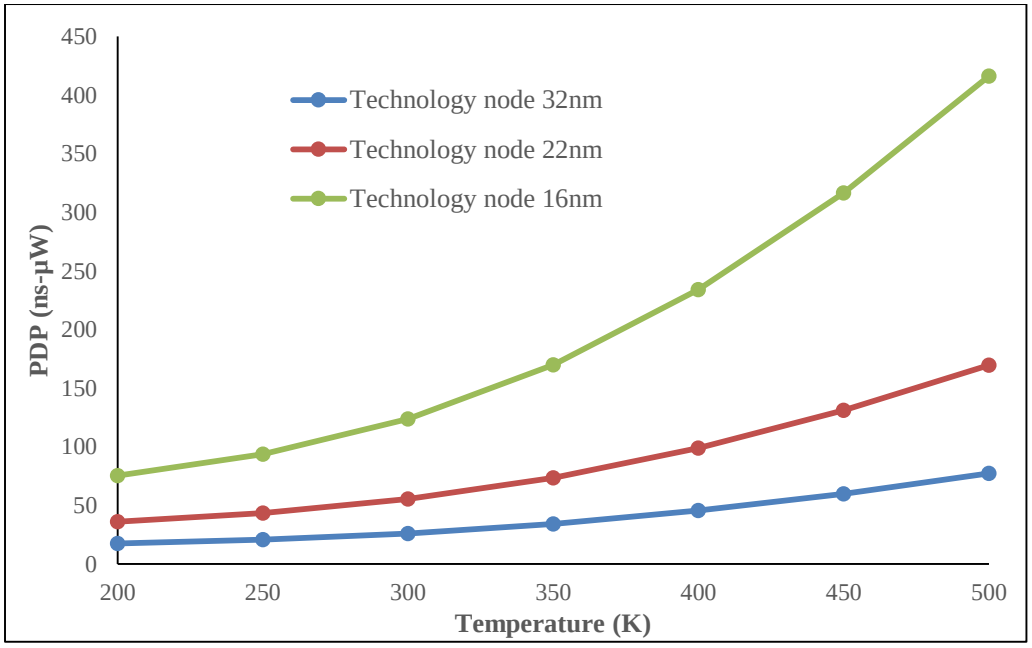


Figure 4.8 PDP (Temperature dependent) of MLGNR for 32nm, 22nm, and 16nm technological nodes at 2000µm length

to 250K but after 250K, the PDP sharply increase up to 500K because of the shrinking of effective MFP. The performance of MLGNR interconnect from delay and PDP parameters is analyzed and observed that the delay and PDP increases with rise in temperature at three different nodes of technology for global interconnect length due to reduction of the effective MFP of GNR.

4.4 Chapter Summary

In this chapter, the influence of temperature on the scattering mechanism of multi-layer graphene nanoribbon is explored. A thermally aware electrical ESC model is presented for global level interconnects which is used to calculate the effective MFP and its impact on the impedance parameters of multilayer graphene nanoribbon. MATLAB computing software is used to evaluate the impedance parameters using analytical equations. It is observed that the electron–phonon scattering is crucial when compared with electron–electron scattering with increase in temperature and affects the effective MFP of MLGNR. It is concluded from the results that the effective MFP of GNR is dominated by acoustic scattering from low to moderate range of temperatures (200–300K). Further, at high temperature range (300–500K), impact of optical and zone boundary scattering occurs along with acoustic scattering. The resistance (temperature dependent) of MLGNR is analyzed at global interconnect levels (500–2000µm) for 32nm, 22nm, and 16nm nodes of technology and observed that with the rise in temperature resistance increases for all technological nodes. Furthermore, performance of MLGNR from

delay and PDP perspectives is analyzed at global interconnect length over 200–500K temperature range for three different nodes of technology and observed that delay and PDP increases due to the reduction of effective MFP of electrons with rise in temperature.

Publication from this chapter

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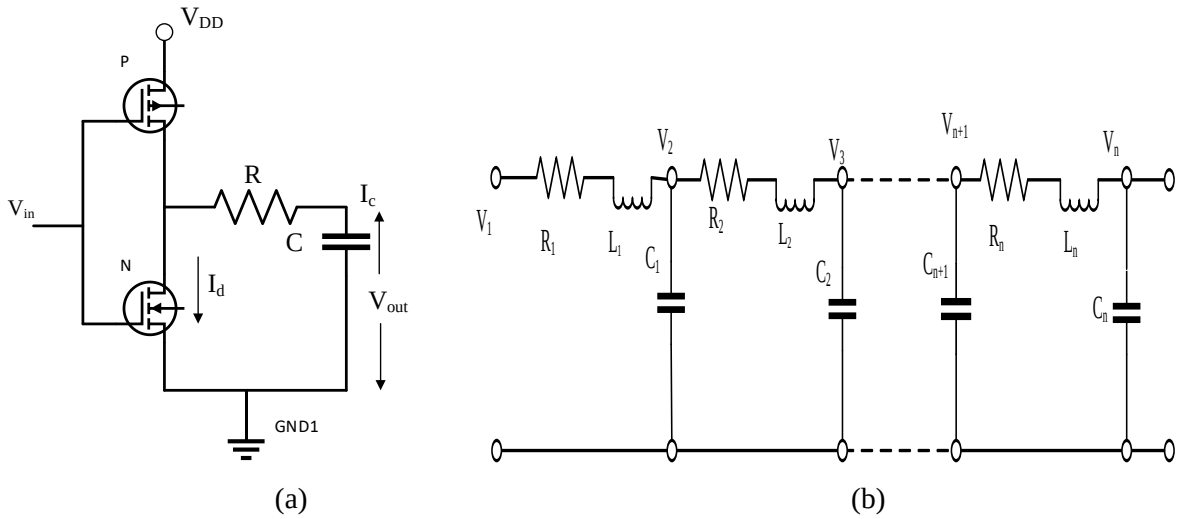
CHAPTER 5

ANALYTICAL DELAY MODEL AND STABILITY ANALYSIS FOR MLGNR INTERCONNECTS

The following chapter elaborates an analytical delay model of MLGNR interconnects dependent on temperature. The outcomes achieved from analytical delay model are compared with the simulation results presented in chapter 4. The simulation and analytical results reveal that the outcomes of the two models correspond well. The trend of the models shows the increase in delay with rising temperature levels for 32nm, 22nm, and 16nm nodes of technology. Further, relative stability analysis of MLGNR as interconnect line at three different technological nodes from 500–2000μm lengths is examined.

5.1 Introduction

The computational system to be accurate should consist of modern engineering aspects in order to structure the electrical equivalent circuit [124, 125]. The feature size of the ICs decreases at nano-scaled technology nodes. The total delay of the IC consists of two components: gate delay and interconnect delay [8]. Formerly, the gate delay was considered dominating and calculated by considering a complete interconnect tree at gate output as per lumped RC model shown in Figure 5.1(a) [30].



(a) (b)

Figure 5.1 (a) Lumped RC model-driven with CMOS inverter (b) Distributed RLC model

With the downscaling in technology nodes, the parasitic parameters of interconnects increases

and becomes more significant than the gate delays. The nano-wires as interconnects contribute more to the total delay than to the gate delay. Therefore, the lumped model approximation technique induces errors in the delay and rise time calculations [126]. Accuracy in estimating the rise time and gate delay depends on parasitic parameters of interconnects and load at the output of a gate. The equivalent parasitic of interconnects should be considered as transmission lines in deep submicron technological nodes. Hence, to estimate the accurate performance of the VLSI interconnects, highly accurate RLC distributed models are required, as depicted in Figure 5.1(b). The basic model to calculate the performance in terms of delay is the resistance capacitance (RC). An example of the RC model is the Elmore delay model, which uses RC loads for estimating performance of interconnect with respect to delay. However, this model gives imprecise results at high frequencies of input signal because of the increase in the inductive impedance [13]. The aluminum and copper interconnects can be easily transformed into equivalent single conductor transmission model for micro-scaled technology nodes. The models presented by H. B. Bakoglu *et. al.* [4], Sakurai et al. [7, 127], and Adler V. and E. G. Friedman [30] were based on RC models that estimated the delay of copper interconnects using optimum number of repeaters. A. Deutsch *et. al.* [128] and Ismail and E. G. Friedman [36, 129] reported the delay models that considered the impact of inductance through RLC models and the improvement has been reported [130, 131] in these models after the addition of effects of inductance.

Due to the limitation of electro-migration and grain boundary scattering in copper, carbon nanotubes are considered to be the suitable material for VLSI interconnects. Delay models are reported [130, 132] for CNTs, but they are not efficient to estimate precise delay owing to the structural complexity and evaluating different parasitic [130].

P. J. burke studied the SWCNT by considering equivalent transmission model based on Luttinger liquid theory [132]. Later, several models have been reported for the SWCNTs [133–135]. Boltzmann transport theory was another alternative used to model the SWCNT interconnect [136]. Early research proposed GNR as better and suitable material than the SWCNTs. The GNRs are further categorized into Single Layer and Multilayer GNR. It is reported in literature that MLGNR is better than SLGNR. An equivalent single conductor model is proposed for SLGNR, which was further extended for MLGNR [85, 104, 111]. It is reported in previous chapters that MLGNRs are suitable at global levels. Hence, estimating the optimum delay repeater-based distributed RLC circuit models should be considered.

In this chapter, closed-form equations are discussed for the estimation of the delay in MLGNR interconnects. Using the analytical model, the performance from delay perspective is estimated

at global levels for 32nm, 22nm, and 16nm nodes of technology under temperature range of 200–500K. Further, a comparative analysis is performed with the outcomes obtained from the analytical delay model and simulated results. Furthermore, while comparing performance, stability analysis must also be taken into account and evaluated for MLGNR for three various technological nodes at longer lengths.

5.2 Equivalent Single Conductor model for MLGNR Interconnect (Temperature Dependent)

The MLGNR is derived by stacking two or more layers of SLGNR in a parallel combination. The electrical equivalent (R-L-C) circuit is obtained by using the MCC (Multi Conductor Circuit) or a MTL: "Multi-Conductor Transmission line" model for MLGNR is shown in Figure 5.2 [34].

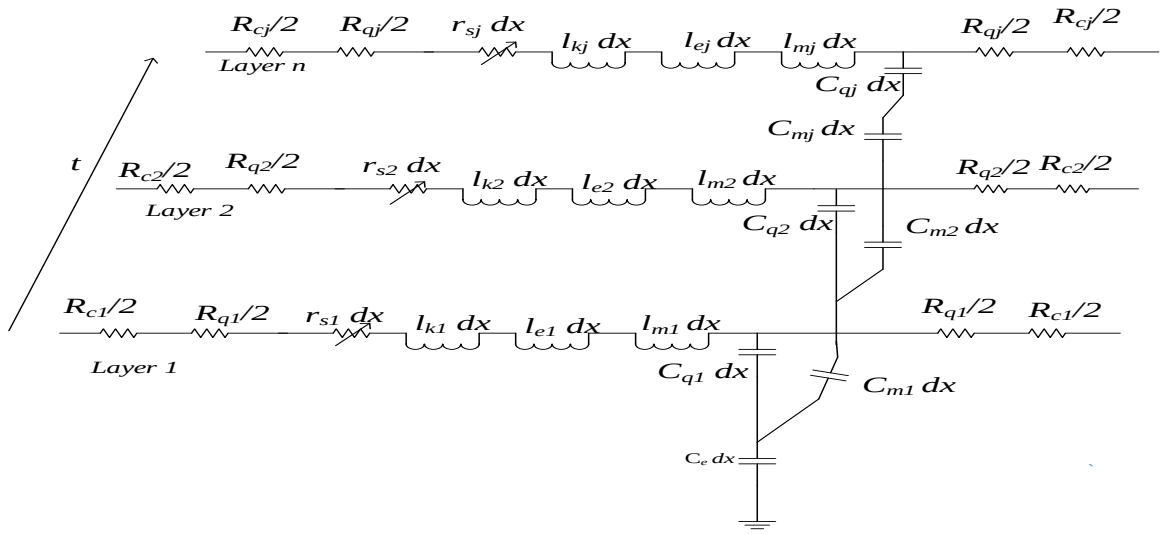


Figure 5.2 Equivalent circuit (Temperature dependent) of an MLGNR interconnect

In MLGNR bundle, the number of conducting layers (*n*) can be estimated by following equation and discussed in chapter 3.

$$n = 1 + \text{Integer}\left[\frac{t}{\delta}\right] \tag{5.1}$$

Every single layer of MLGNR interconnect consists of conducting channels that are width-dependent. Therefore, the conduction channels of the GNR interconnect can be given as [104],

$$N_{\text{ch}_{\text{GNR}}} = \alpha w E_{\text{f}} \tag{5.2}$$

Where w is interconnect width and E_f is Fermi energy.

Resistance of equivalent temperature-dependent GNR interconnect is categorized into three different resistive components: resistance due to electron phonon scattering (r_s) (considering GNR length is more than MFP), contact resistance (R_c), and quantum resistance (R_q), which are discussed in chapter 4. The contact resistance occurs owing to the contact of the metal with MLGNR and its value is small, ranging in few hundred of ohms to tens kilo ohms (depends on the fabrication process). The temperature-dependent analytical equations for resistance, capacitance, and inductance are discussed in section 4.2 of chapter 4.

Therefore, the temperature dependent resistance of MLGNR interconnect as discussed in chapter 4, is given as [123],

$$R_{\mathrm{MLGNR}} = \frac{R_q + r_s}{n} = \frac{12.9}{n.N_{\mathrm{ch_{GNR}}}}\left(1 + \frac{l}{\lambda_{\mathrm{eff}}(T)}\right) \tag{5.3}$$

It is analyzed from equation 5.3 that λ_{eff} shows a dominating impact in determining temperature-dependent effective MFP of MLGNR. The temperature-dependent mechanism of scattering of electron-phonon has been discussed in chapter 4.

The quantum resistance of GNR interconnect is given by,

$$R_q = \frac{12.9}{N_{\mathrm{ch_{GNR}}}} \qquad (\mathrm{k\Omega}) \tag{5.4}$$

The p.u.l. capacitance (electrostatic and quantum) of MLGNR material as interconnect are presented by equations 5.5 and 5.6 [104, 105, 123],

$$C_e = \frac{\varepsilon_o w}{d} \tag{5.5}$$

$$C_q = 0.1 N_{\mathrm{ch_{GNR}}}\left[1 + \sqrt{1 + 1/\alpha\beta E_f}\right] \qquad (\mathrm{fF/\mu m}) \tag{5.6}$$

Where $\varepsilon_o$is free space relative permittivity.

Total capacitance of equivalent RLC circuit of MLGNR interconnect is given by

$$C_{\mathrm{ESC}} = (C_q^{-1} + C_e^{-1})^{-1} \tag{5.7}$$

Similarly, total inductance of equivalent RLC circuit of MLGNR interconnect [85, 104, 105, 111, 123], is given by:

$$L_{\mathrm{ESC}} = l_k + l_e \tag{5.8}$$

Where l_k, l_e are the kinetic and magnetic inductance of the MLGNR interconnect. The GNR l_k (kinetic inductance) is produced by kinetic energy because of the motion of electrons in conducting channels. Magnetic Inductance (l_e) is derived from variable levels of electric

current in the wire that generates a magnetic field around it.

The p.u.l. inductance (l_e and l_k) of the MLGNR interconnects are calculated using equations 5.9 and 5.10 [104, 105, 123],

$$l_e = \frac{\mu_o d}{w} \tag{5.9}$$

$$l_k = \frac{8}{n\alpha w E_f} \quad (\text{nH/μm}) \tag{5.10}$$

Where μ_o is magnetic permeability of free space.

To estimate the analytical delay, the equivalent circuit (Temperature dependent) of MLGNR interconnect (length dependent) can be modeled into a thermally aware DIL system constituted by equivalent single conductor transmission model (Figure 5.3).

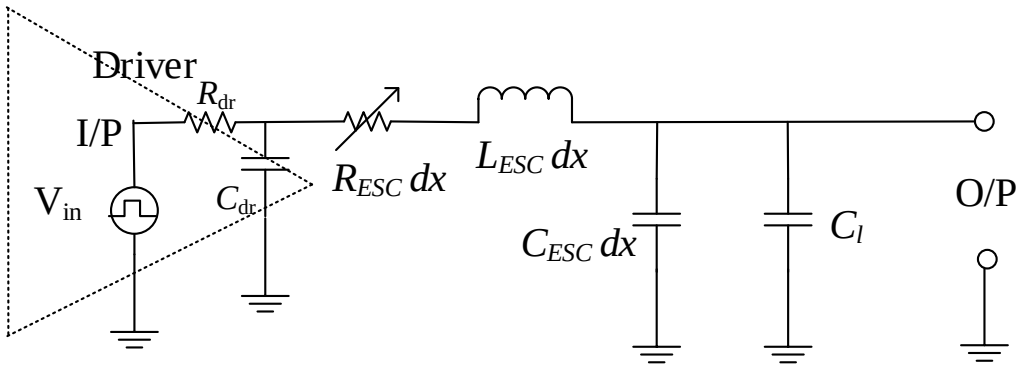


Figure 5.3 A thermally aware DIL system, constituted by ESC model of MLGNR

Considering the single conductor RLC model of MLGNR, the delay is estimated by driver interconnect load (DIL) using CMOS as driver and load as capacitance. The delay time of the DIL system is dependent on the parasitic parameters of the driver ($R_{dr,}$ C_{dr}), interconnect line ($R_{ESC,}$ L_{ESC}, C_{ESC}), and load (C_l) [137–140]. The parasitic of interconnects are linearly dependent on the length of interconnects, while the driver and load parasitic are independent of it. The performance of DIL is characterized by the 90%-time delay (τ_(90%)). The τ_(90%) is obtained using transient response of DIL set-up constituted by ESC model of a MLGNR interconnect. Using the closed form equation proposed for interconnects in [139], the delay is estimated and is given by

$$\tau_{90\%} = \frac{2T_2 \ln\left[\left(0.2.\sqrt{4T_2 - T_1^2}\right)/\left(T_1 + \sqrt{4T_2 - T_1^2}\right)\right]}{\left(\sqrt{4T_2 - T_1^2} - T_1\right)} \tag{5.11}$$

Where T_1 and T_2 are the coefficients in expression in 5.11 and are given by,

$$T_1 = \left[\frac{R_{\mathrm{ESC}} C_{\mathrm{ESC}} (n_{\mathrm{o}} dx)^2}{2} + R_{\mathrm{dr}} C_{\mathrm{dr}} + C_{\mathrm{ESC}} (n_{\mathrm{o}} dx)(R_{\mathrm{q}} + R_{\mathrm{dr}}) \right] + C_{\mathrm{l}} \left(2R_q + R_{\mathrm{dr}} + R_{\mathrm{ESC}} (ndx) \right) \quad (5.12)$$

$$T_2 = \left| \frac{L_{ESC} C_{ESC} (n_{\mathrm{o}} dx)^2}{2} + \frac{R_{ESC}^2 C_{ESC}^2 (n_{\mathrm{o}} dx)^4}{4!} + \frac{R_{ESC} R_{dr} C_{ESC} C_{dr} (n_{\mathrm{o}} dx)^2}{2} \right.$$

$$\left. + \frac{R_{ESC} C_{ESC}^2 (n_{\mathrm{o}} dx)^3 (R_q + R_{dr})}{3!} + R_q R_{dr} C_{dr} C_{ESC} (n_{\mathrm{o}} dx) \right|$$

$$+ C_l \left| \frac{R_{ESC} C_{ESC} (n_{\mathrm{o}} dx)^2}{2} (2R_q + R_{dr}) + 2R_q R_{dr} C_{dr} + \frac{R_{ESC}^2 C_{ESC} (n_{\mathrm{o}} dx)^3}{3!} \right.$$

$$+ L_{ESC} (n_{\mathrm{o}} dx) + R_q^2 C_{ESC} (n_{\mathrm{o}} dx) + R_{ESC} R_{dr} C_{dr} (n_{\mathrm{o}} dx) + R_q R_{dr} C_{ESC} (n_{\mathrm{o}} dx) \quad (5.13)$$

Where dx is the length of each segment and n_{o} is the number of distributed segments. The driver resistance and capacitance are represented by R_{dr} and C_{dr}, respectively.

5.3 Repeater Insertion

The customer satisfaction arises from maximum power standby and high speed [141]. Therefore, repeaters are proposed in between the long interconnects to reduce the delay [3, 30–33]. Figure 5.4 shows an interconnect that is divided into small subsections driven by CMOS inverters called as repeaters [34].

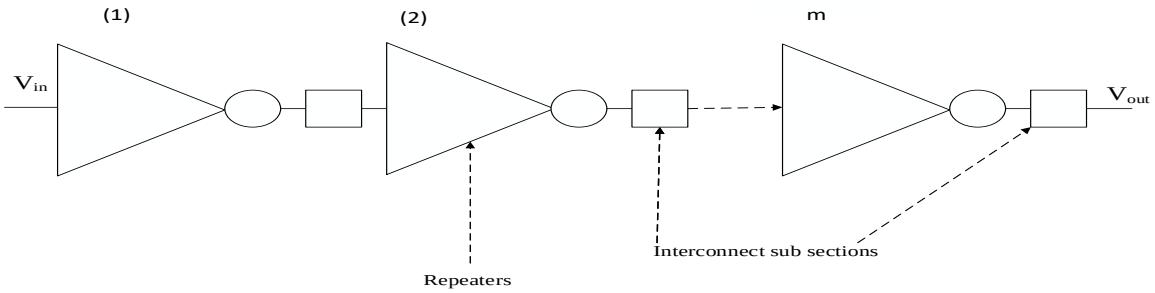


Figure 5.4 Interconnect divided into subsections with optimum number of repeaters

The signal delay is the time constant (RC) of interconnect. In this research the performance of MLGNR is enhanced at global interconnect levels using distributed circuit model by deploying optimum number of repeaters. Hence, to calculate the accurate delay at global lengths, optimum number of repeaters with optimum size [134] is required to be estimated and given as

$$n_{\mathrm{o}} = \mathrm{Int} \left[\sqrt{\frac{r_{\mathrm{t}} c_{\mathrm{t}}}{2R_{\mathrm{dr}} (C_{\mathrm{dr}} + C_{\mathrm{l}})}} \frac{1}{\left(1 + \beta \left(T_{L/R} \right)^3 \right)^{0.28}} \right] - 1 \quad (5.14)$$

Where $r_t = R_{ESC} l$ (5.15)

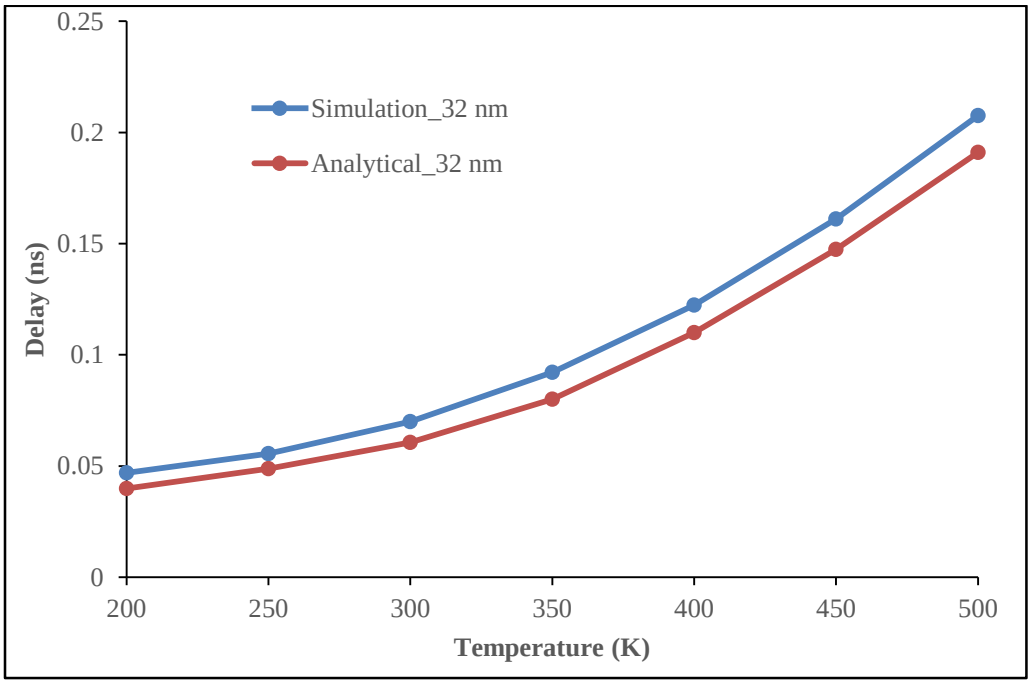
$c_t = C_{ESC} l$ (5.16)

$l_t = L_{ESC} l$ (5.17)

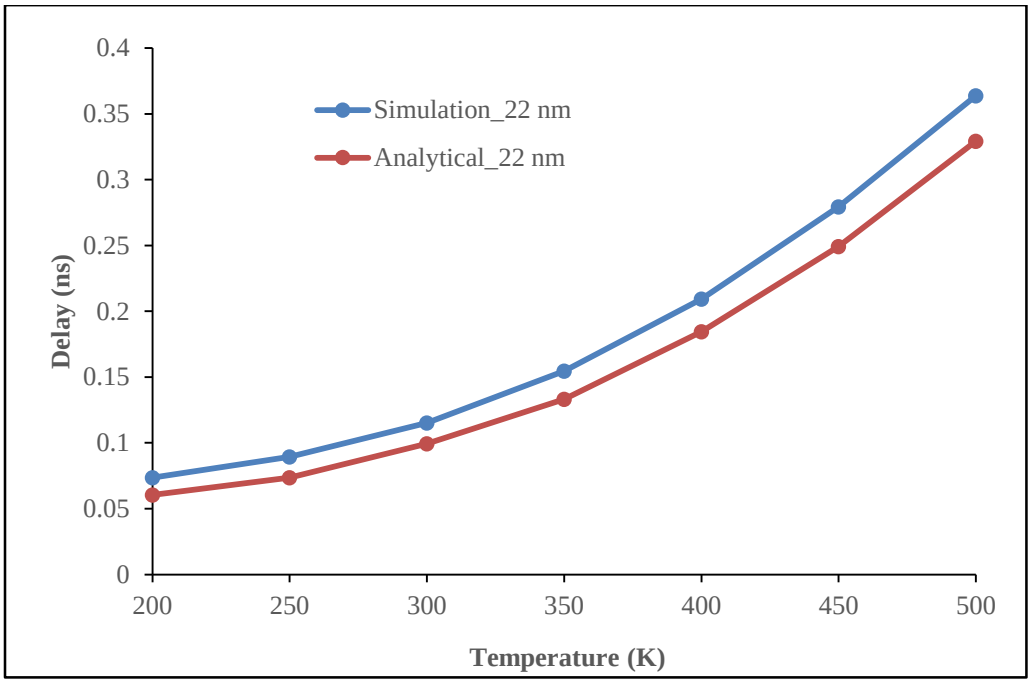
and

$$T_{L/R} = \sqrt{\frac{l_t}{r_t (R_{dr} (C_{dr} + C_l))}} \quad (5.18)$$

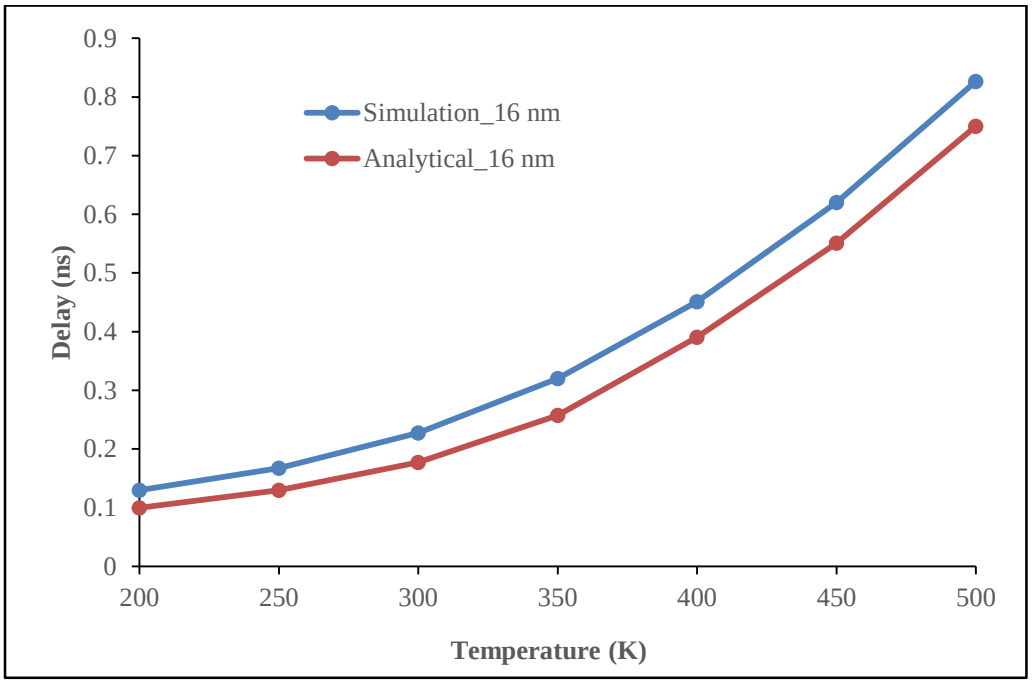
As above discussed procedure, delay is calculated at three different technological nodes (16nm, 22nm, and 32nm) under thermally variable conditions for 2mm length of multilayer GNR. Parameters of simulation are taken into account in Table 3.1 of chapter 3 from the ITRS 2013 edition are used for calculating the parasitic of MLGNR. The parasitic parameters are calculated from equations 5.1–5.10 for equivalent model of MLGNR at three different nodes of technology (16nm, 22nm, and 32nm) for 2mm length under 200–500K temperature range. The optimum number of repeaters, are calculated using equations 5.14–5.18 for accurate analytical delay of MLGNR. The delay is calculated using equations 5.11–5.13. Further, all the calculations are performed using MATLAB computing software. The comparison of analytical delay calculated from the aforementioned procedure of MLGNR with simulation delay estimated in chapter 4, is graphically depicted in Figure 5.5 for three different nodes of technology (16nm, 22nm, and 32nm).



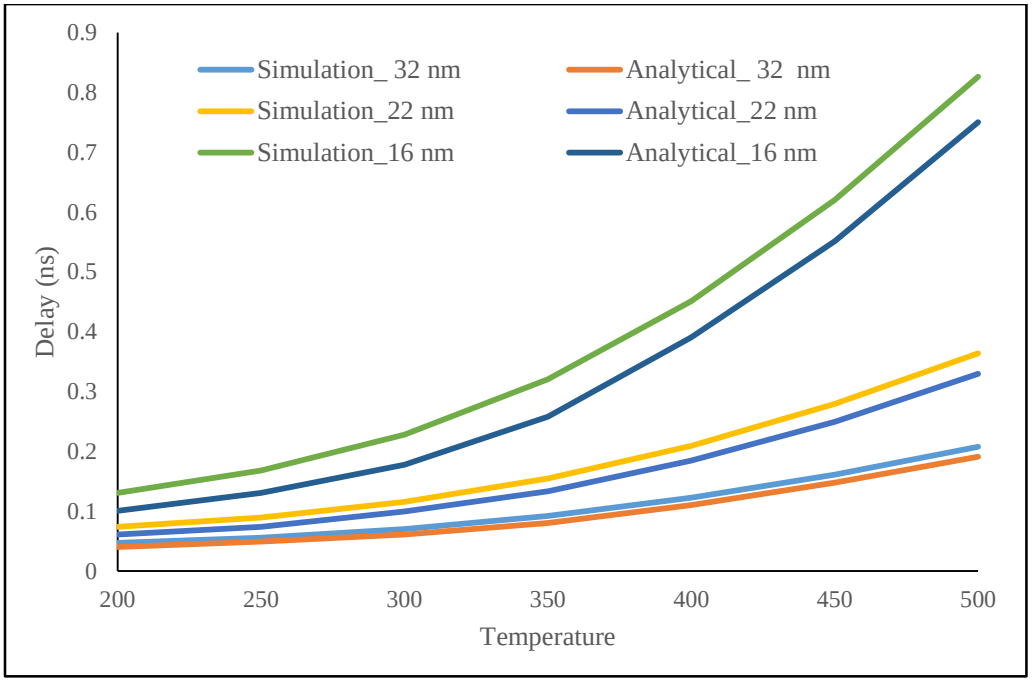
(a)


0.4
0.35
0.3
0.25
0.2
0.15
0.1
0.05
0
Delay (ns)
Simulation_22 nm
Analytical_22 nm
200
250
300
350
400
450
500
Temperature (K)

(b)


0.9
0.8
0.7
0.6
0.5
0.4
0.3
0.2
0.1
0
Delay (ns)
Simulation_16 nm
Analytical_16 nm
200
250
300
350
400
450
500
Temperature (K)

(c)



(d)

Figure 5.5 Comparison of analytical and simulated results of MLGNR for 2000-µm length at (a) 32nm, (b) 22nm, and (c) 16nm technology nodes under temperature range of 200–500 K. (d) Comparative analysis of analytical and simulated outcomes at 2000µm length of MLGNR for all three technological nodes under 200–500K temperature range

Figure 5.5 shows the comparison of simulated and analytical results at 2000µm length for 32nm, 22nm, and 16nm nodes of technology under temperature range (200–500K) of MLGNR. The comparative analysis of simulated and analytical outcomes of MLGNR at length 2000µm for three technological nodes under 200–500K temperature range as shown in panel (d). The simulation and analytical results reveal that the outcomes of the two models correspond well. The trend of the models shows the increase in delay with the rising temperature levels for 32nm, 22nm, and 16nm nodes of technology.

5.4 Stability analysis of MLGNR

The simulation and analytical results in delay terms presented above corresponds well at length 2000µm for three various technological nodes under 200–500K temperature range. Further, stability is also an important factor to determine the performance of interconnect. The stability analysis of an interconnect depend on the peak overshoot voltage (M_q) as well as switching delay (T_q) at the output. A system is considered as more stable having zero value of M_q and greater value for switching delay. With increasing value of switching delay and decreasing M_q, the input signal tend to damp more rapidly and the system becomes more stable [139]. T_q is the

time when output reaches 10-90% and expressed as [139]

$$T_{\mathrm{q}} = \frac{\pi - \cos^{-1}\xi}{\omega_{\mathrm{n}}\sqrt{1-\xi^2}} \tag{5.19}$$

Where ω_{n} is angular frequency and given as

$$\omega_n = \frac{1}{\sqrt{l_{\mathrm{t}}(c_{\mathrm{t}} + C_{\mathrm{l}})}} \tag{5.20}$$

and ξ is defined as damping coefficient and expressed as

$$\xi = 0.5(1 + C_{\mathrm{l}} / C_{\mathrm{ESC}} l)^{-1/2} \times \left[(0.5R_{ESC} l + R_{\mathrm{dr}})(C_{\mathrm{ESC}} / l_{\mathrm{ESC}}) + (R_{ESC} l + R_{dr})\sqrt{C_l^2 / l_{ESC}.C_{ESC} l^2}\right] \tag{5.21}$$

Peak overshoot voltage (M_{q}) is basically difference of the peak time and steady state output. M_{q} is expressed as

$$\%M_q = \exp\left(\frac{-(2n_x - 1)\pi\xi}{\sqrt{1-\xi^2}}\right) \times 100\% \tag{5.22}$$

Where n_x defines number of cycles.

Table 5.1 Switching delay of MLGNR from 500–2000µm lengths at 16nm, 22nm, and 32nm technological nodes

Length (µm)	T_{q} (ns)		
	32nm	**22nm**	**16nm**
500	3.5996	4.3349	6.106
1000	7.1811	8.6513	12.1908
1500	10.7656	12.9735	18.2913
2000	14.3502	17.3015	24.4076

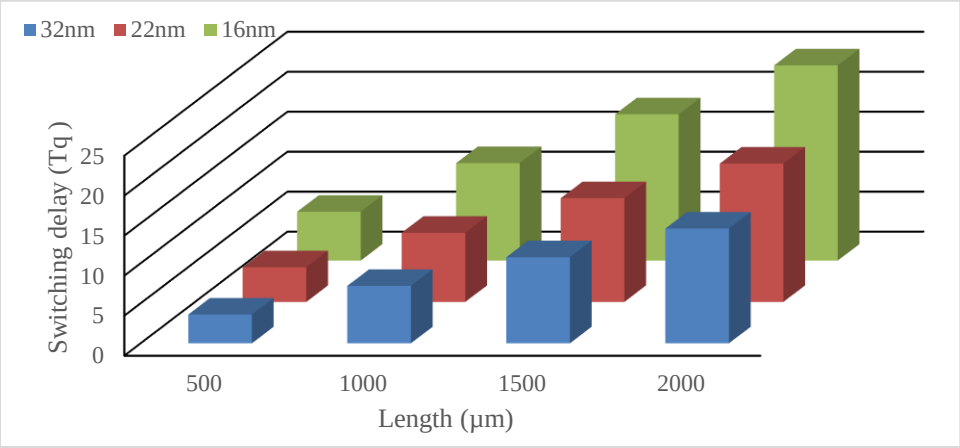
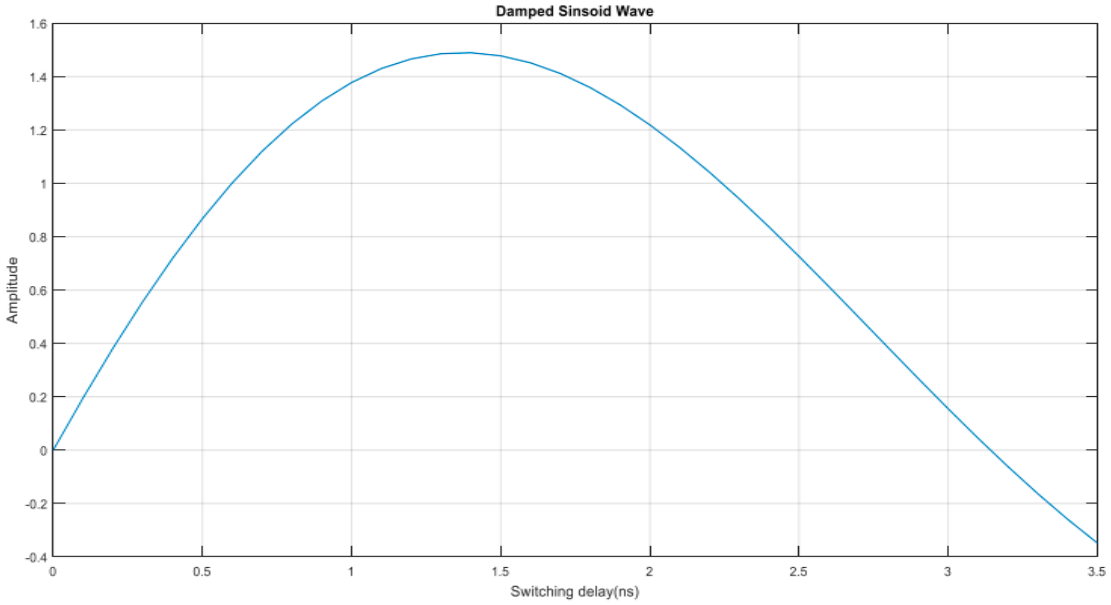
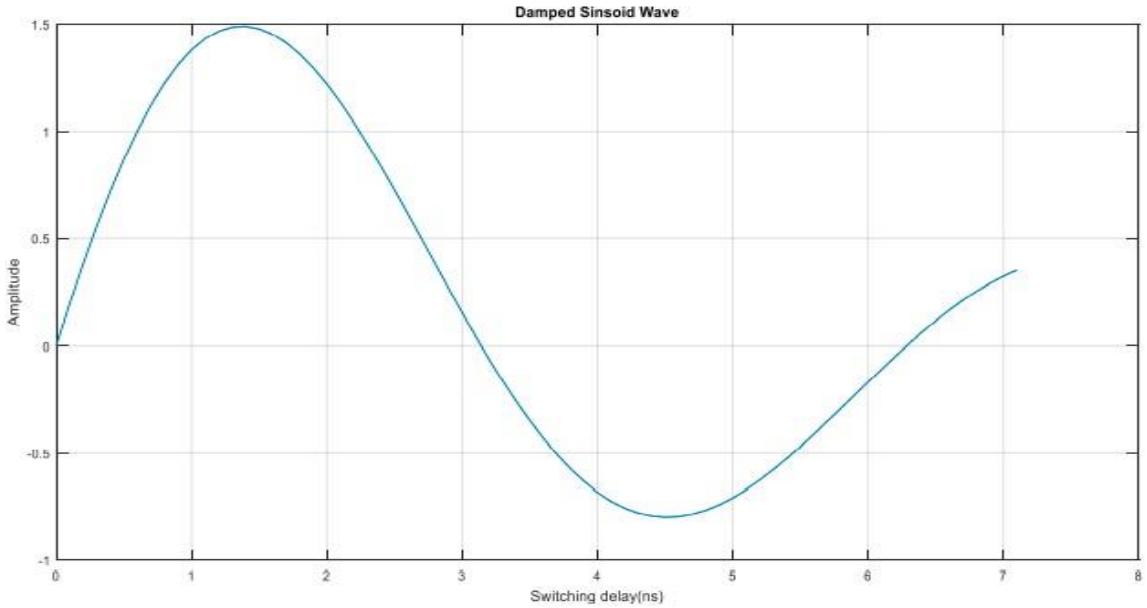


Figure 5.6 Switching delay of MLGNR from 500–2000µm length at 16nm, 22nm, and 32nm technological nodes

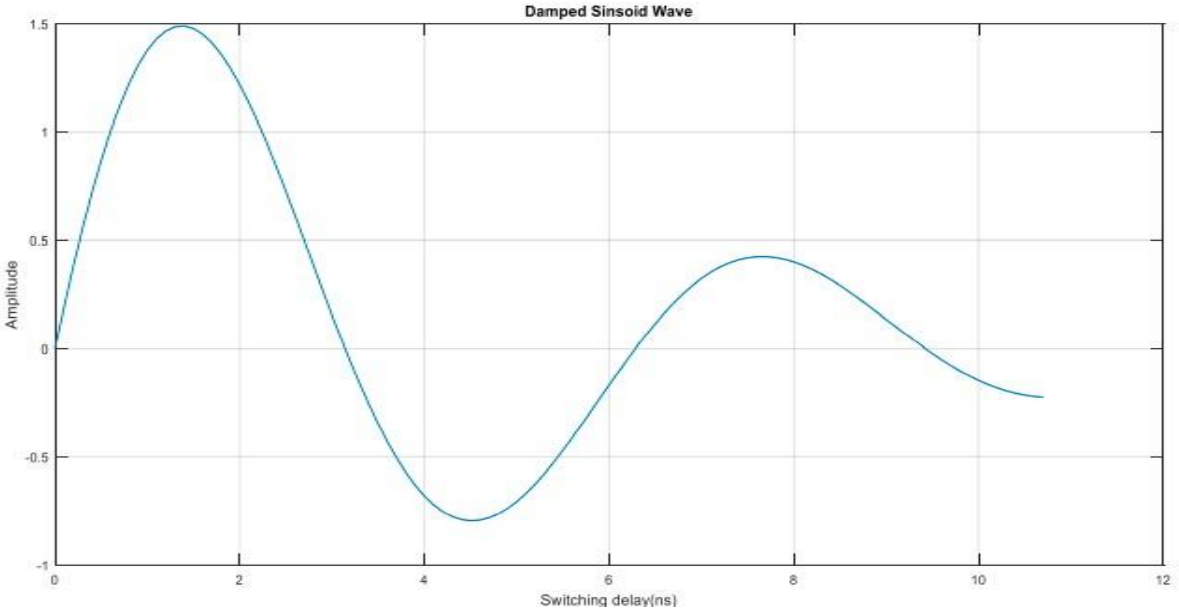
Table 5.1 presents the switching delay (T_q) which is graphically depicted in Figure 5.6 for 500–2000µm lengths of MLGNR as interconnect at 16nm, 22nm, and 32nm technological nodes. The higher values of switching delay has been noticed as we move from to 32nm to 16nm due to the rise in parasitic parameters of MLGNR. As discussed above higher the value of T_q greater will be the stability. Hence, the relative stability of MLGNR is analyzed with respect to (w.r.t.) damped sinoid wave for switching delay at three different technological nodes from 500–2000µm lengths and graphically shown in Figures 5.7–5.9.



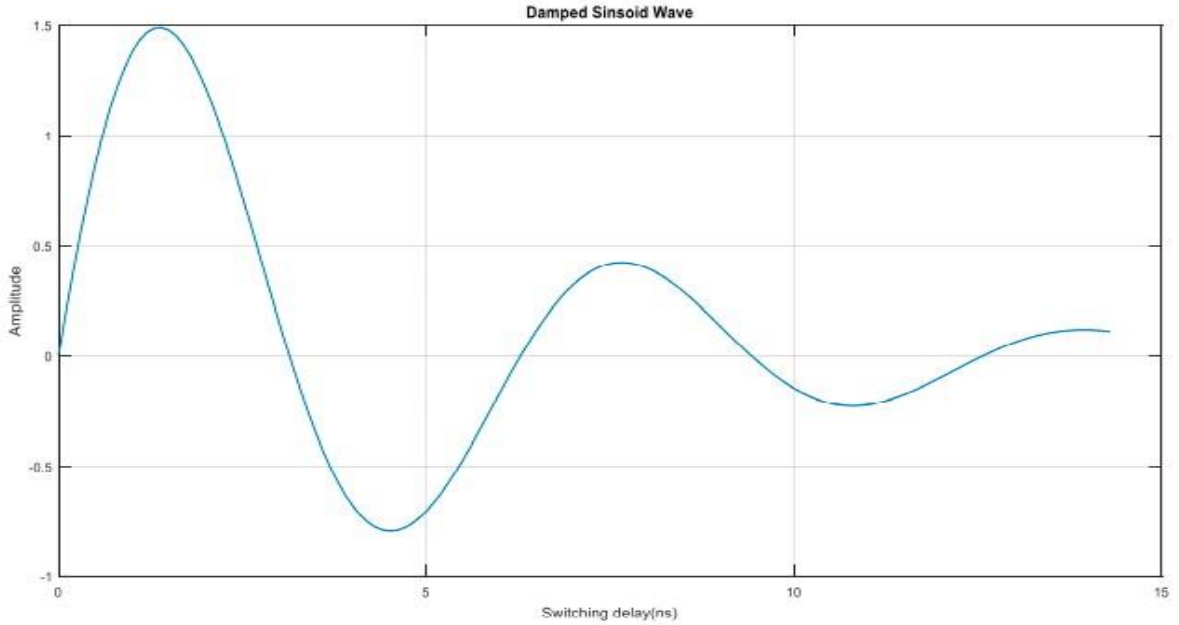
(a)



(b)

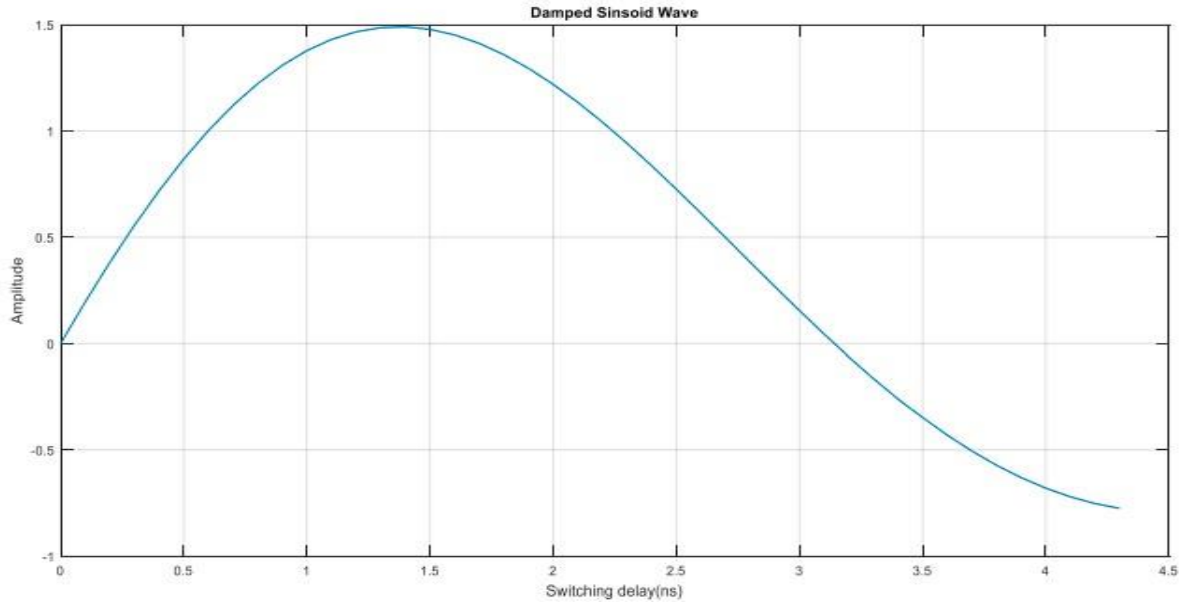


(c)

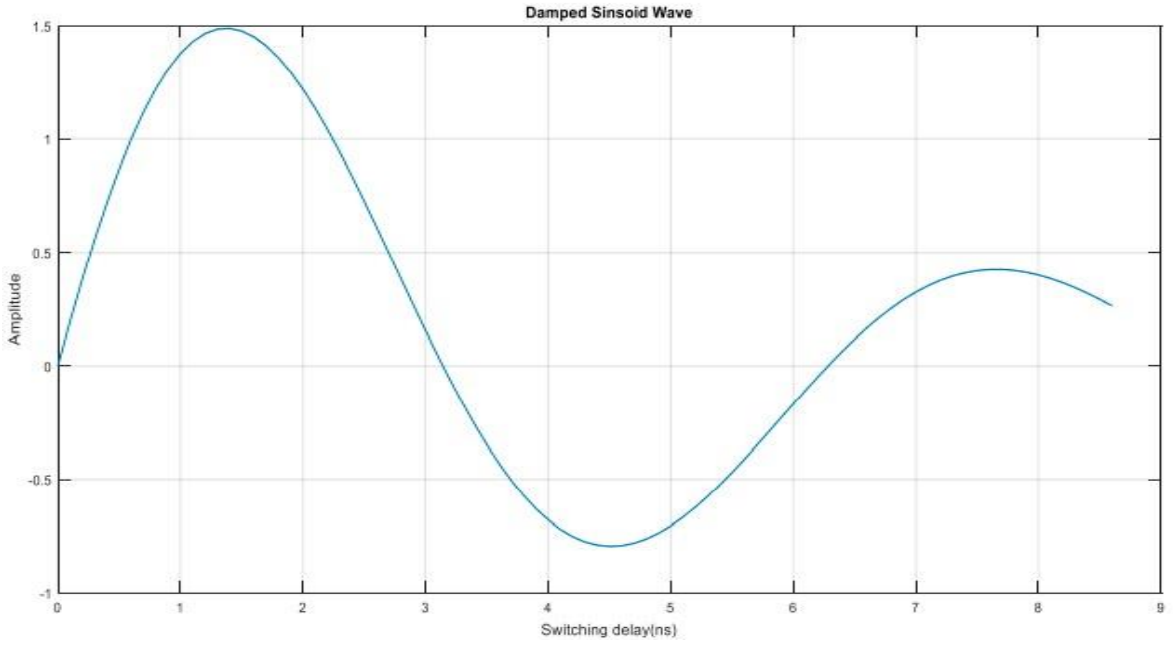


(d)

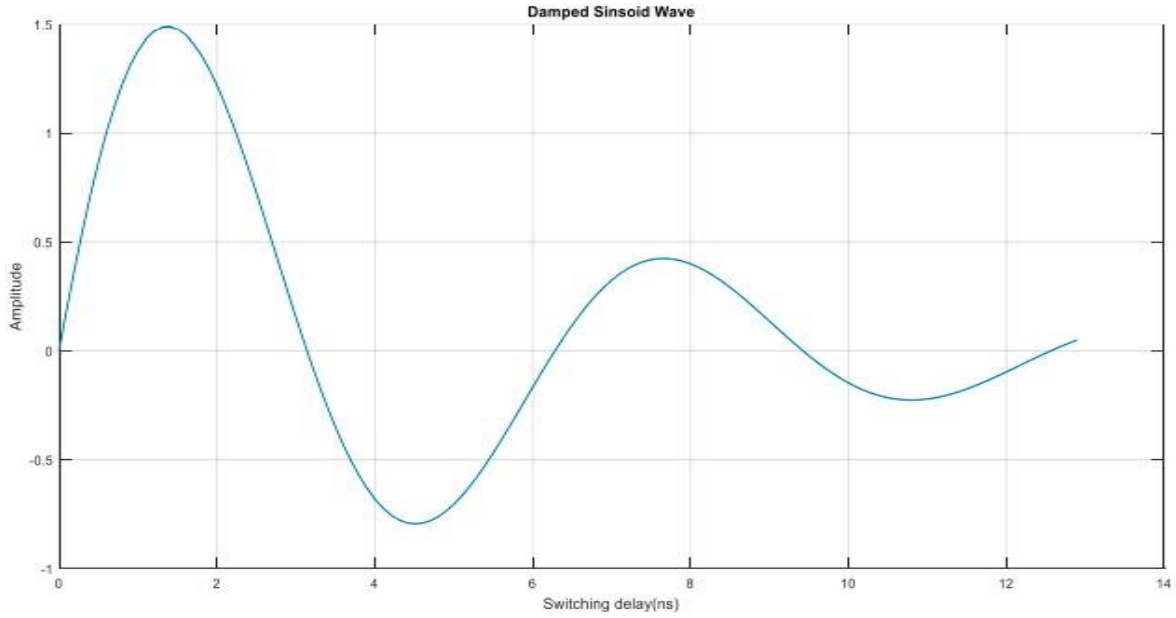
Figure 5.7 Damping wave w.r.t. switching delay time of MLGNR at (a) 500µm, (b) 1000µm, (c) 1500µm, and (d) 2000µm lengths for 32nm technological node


Damped Sinsoid Wave
Amplitude
Switching delay(ns)
1.5
1
0.5
0
-0.5
-1
0
0.5
1
1.5
2
2.5
3
3.5
4
4.5

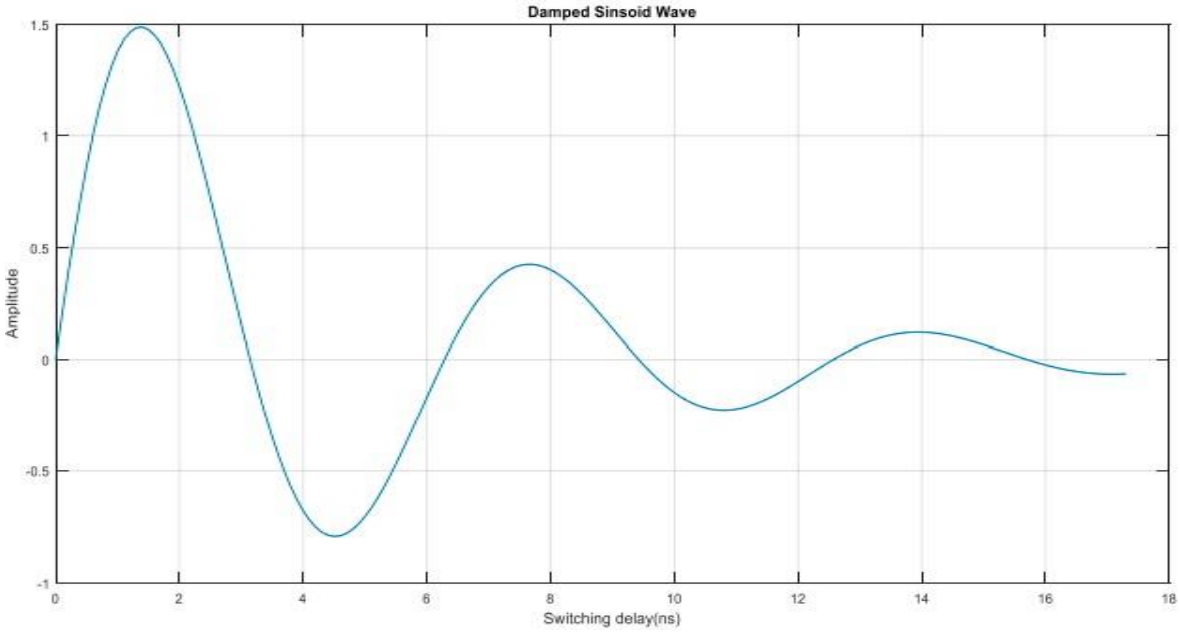
(a)


Damped Sinsoid Wave
Amplitude
Switching delay(ns)
1.5
1
0.5
0
-0.5
-1
0
1
2
3
4
5
6
7
8
9

(b)

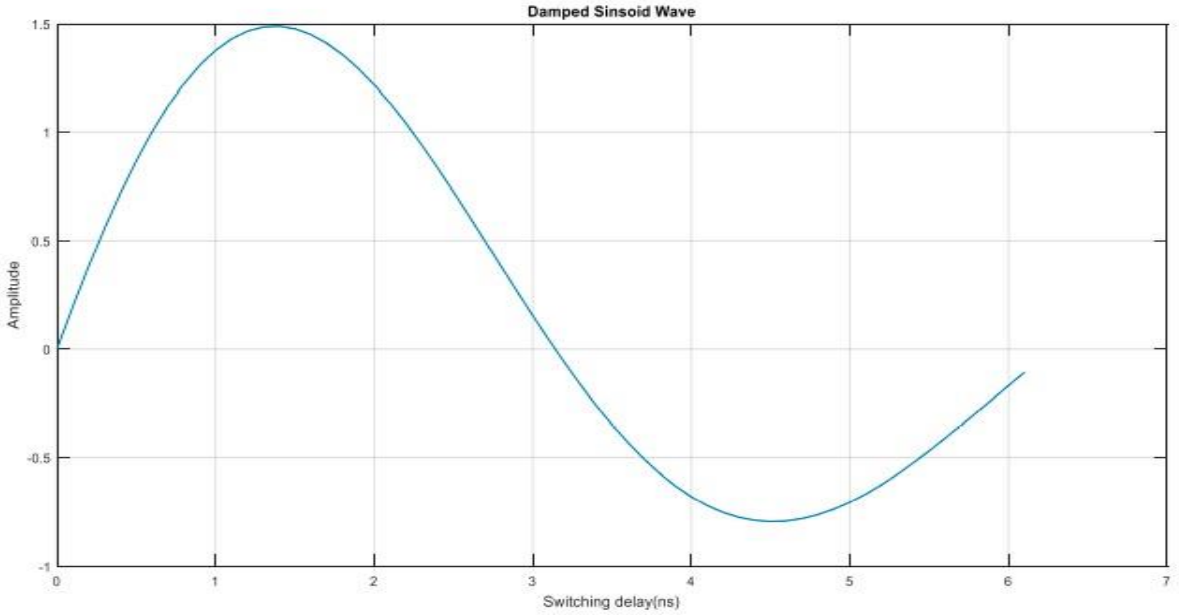


(c)

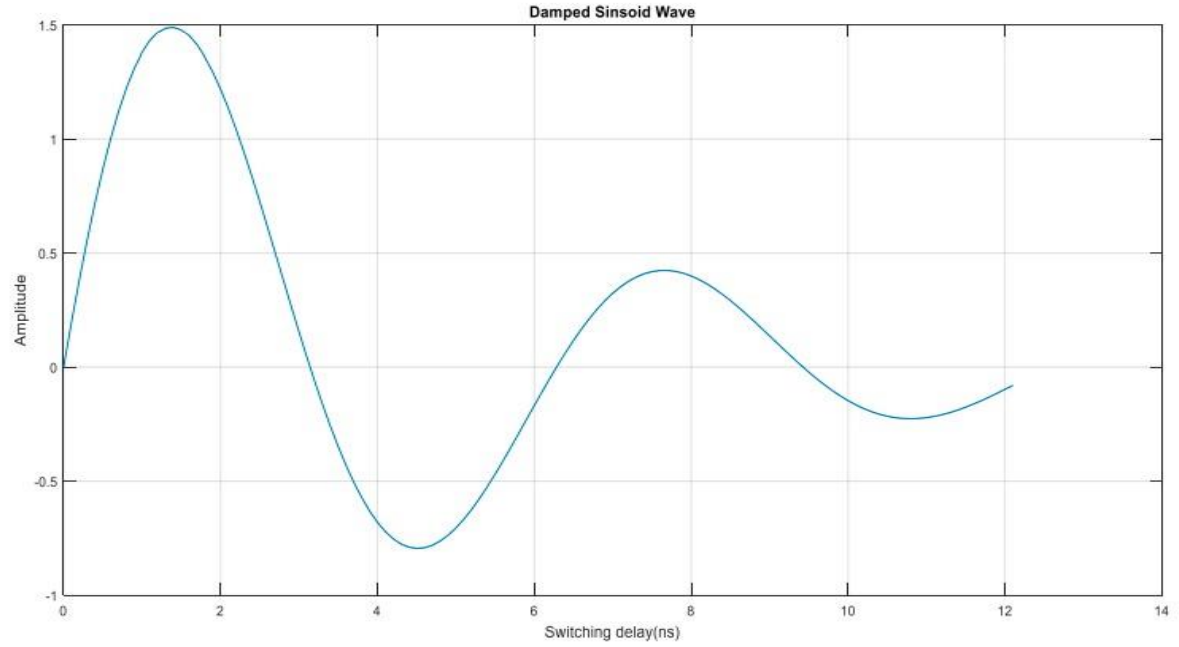


(d)

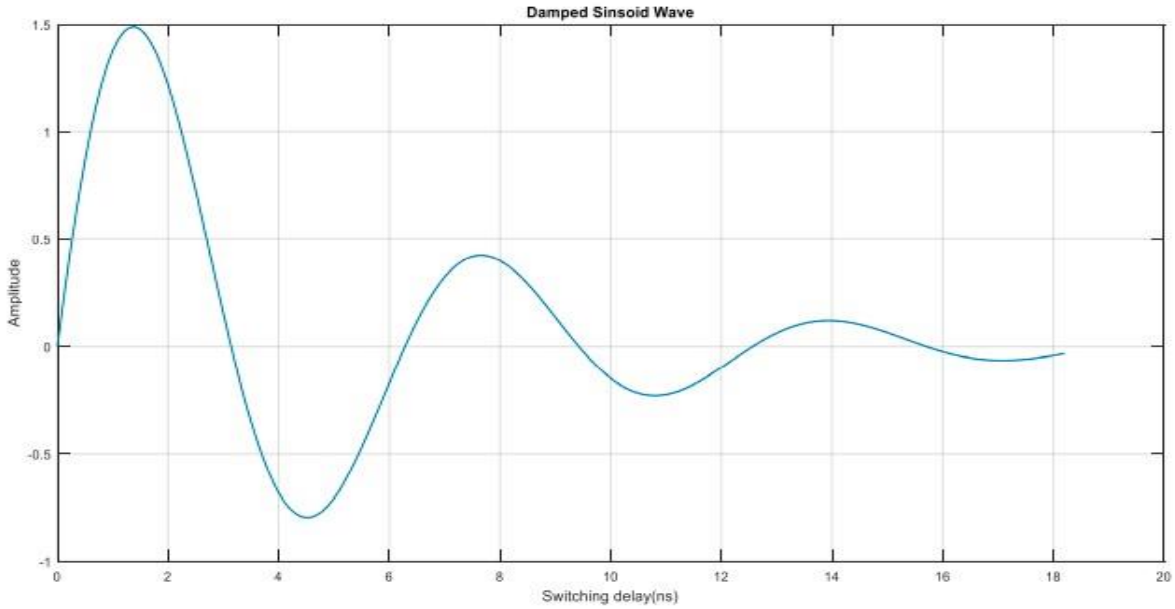
Figure 5.8 Damping wave w.r.t. switching delay time of MLGNR at (a) 500µm, (b) 1000µm, (c) 1500µm, and (d) 2000µm lengths for 22nm technological node


Damped Sinsoid Wave
Amplitude
Switching delay(ns)
1.5
1
0.5
0
-0.5
-1
0
1
2
3
4
5
6
7

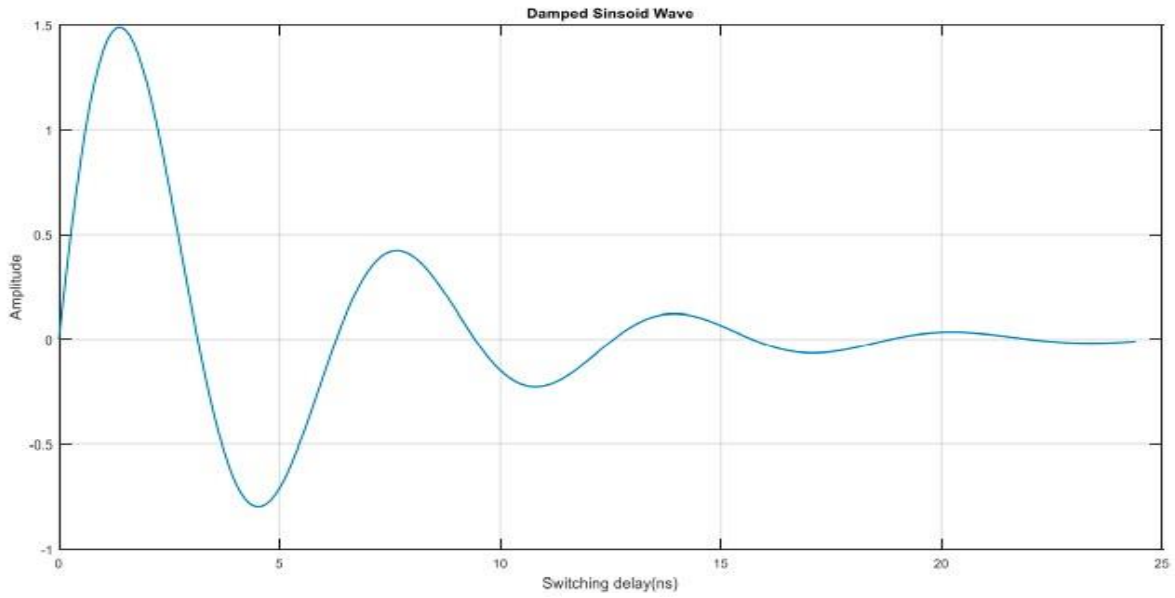
(a)


Damped Sinsoid Wave
Amplitude
Switching delay(ns)
1.5
1
0.5
0
-0.5
-1
0
2
4
6
8
10
12
14

(b)



(c)



(d)

Figure 5.9 Damping wave w.r.t. switching delay time of MLGNR at (a) 500µm, (b) 1000µm, (c) 1500µm, (d) 2000µm lengths for 16nm technological node

The peak overshoot voltage as well as switching delay depends on damping coefficient. For smaller interconnect lengths impedance values impact the damping coefficient by reducing its value less than one, therefore, input signal will exhibit under damped condition. It is analyzed that increasing length of interconnect from 500–2000µm, impedance values increases which rises damping coefficient, that leads to rise in switching delay and signal tends to damp faster and consequently system becomes stable for all three various technological nodes. Figure 5.7

presents the damped sinsoid waveform of MLGNR at 32nm technological node from 500–2000μm length and it has been analyzed that with rise in interconnect length, waveform settle down faster viz a viz damp faster which shows the stability of a system therefore, MLGNR as interconnect line is stable at global lengths for 32nm technological node. Similarly, it has been observed for 22nm, and 16nm technological nodes that with increase in interconnect length, signal damp faster which raises the stability of a system. Relative stability at 16nm technological is more compared to 22nm and 32nm technological nodes of MLGNR. All the graphs of Figures 5.7–5.9 are with respect to the values of switching delay as shown in Table 5.1.

Relative stability is also demonstrated through Nyquist diagram for MLGNR interconnects. A thermally aware, DIL model of MLGNR is taken into account and from the Pade's fourth order approximation transfer function of the system is given by [92]

$$H(s)=\frac{V_{\mathrm{o}}(s)}{V_{\mathrm{i}}(s)}\approx\left(\sum_{i=0}^{4}b_i s^i\right)^{-1} \tag{5.23}$$

Where s denotes complex frequency and coefficients of b are expressed as [92]

$$b_o=1$$

$$b_1=R_{\mathrm{dr}}(C_{\mathrm{dr}}+C_{\mathrm{ESC}}l+C_l)+R_{\mathrm{ESC}}(C_{\mathrm{ESC}}l+2C_l)+R_{\mathrm{ESC}}l(C_{\mathrm{ESC}}l/2!+C_l) \tag{5.24}$$

$$\begin{aligned}b_2 &= R_{\mathrm{ESC}}R_{\mathrm{dr}}[C_l(C_{\mathrm{dr}}+C_l)+2C_{\mathrm{dr}}C_l]+R_{\mathrm{ESC}}^2C_{\mathrm{ESC}}l^2(C_{\mathrm{ESC}}l/3!+C_l)+R_{\mathrm{dr}}R_{\mathrm{ESC}}l\\ &\times[C_{\mathrm{dr}}C_l+(C_{\mathrm{dr}}+C_l)C_{\mathrm{ESC}}l/2!+C_{\mathrm{ESC}}^2l^2/3!]+R_{ESC}^2C_{ESC}^2l^4/4!+L_{ESC}lC_l+L_{ESC}C_{ESC}l^2 2!\\ &+R_{ESC}^2C_{ESC}lC_l+R_{ESC}^2Cl^3C_l/3!\end{aligned} \tag{5.25}$$

$$\begin{aligned}b_3 &= R_{\mathrm{ESC}}R_{\mathrm{dr}}C_{\mathrm{dr}}C_{\mathrm{ESC}}lC_l(2R_{\mathrm{ESC}}l)+R_{\mathrm{dr}}C_{\mathrm{dr}}L_{\mathrm{ESC}}lC_l+(R_{\mathrm{ESC}}+R_{\mathrm{dr}}+R_{\mathrm{ESC}}C_l/C_{\mathrm{ESC}})\\ &\times(L_{\mathrm{ESC}}C_{\mathrm{ESC}}^2l^3/3!+R_{\mathrm{ESC}}^2C^3l^5/5!)+[R_{\mathrm{dr}}(C_{\mathrm{dr}}+C_l)+2R_{\mathrm{ESC}}C_l]\times(L_{\mathrm{ESC}}C_{\mathrm{ESC}}l^2/2!+R_{\mathrm{ESC}}^2C_{\mathrm{ESC}}^2l^4/4!)\\ &+R_{\mathrm{ESC}}^3C_{\mathrm{ESC}}^3l^6/6!+2R_{\mathrm{ESC}}L_{\mathrm{ESC}}C_{\mathrm{ESC}}^2l^4/4!+(R_{\mathrm{ESC}}C_{\mathrm{ESC}}^2l^3/3!)\times[R_{\mathrm{ESC}}^2C_l+R_{\mathrm{ESC}}R_{\mathrm{dr}}(C_{\mathrm{dr}}+C_l)\\ &+(L_{\mathrm{ESC}}C_l+R_{\mathrm{ESC}}R_{\mathrm{dr}}C_{\mathrm{dr}}C_l/C_l)\end{aligned} \tag{5.26}$$

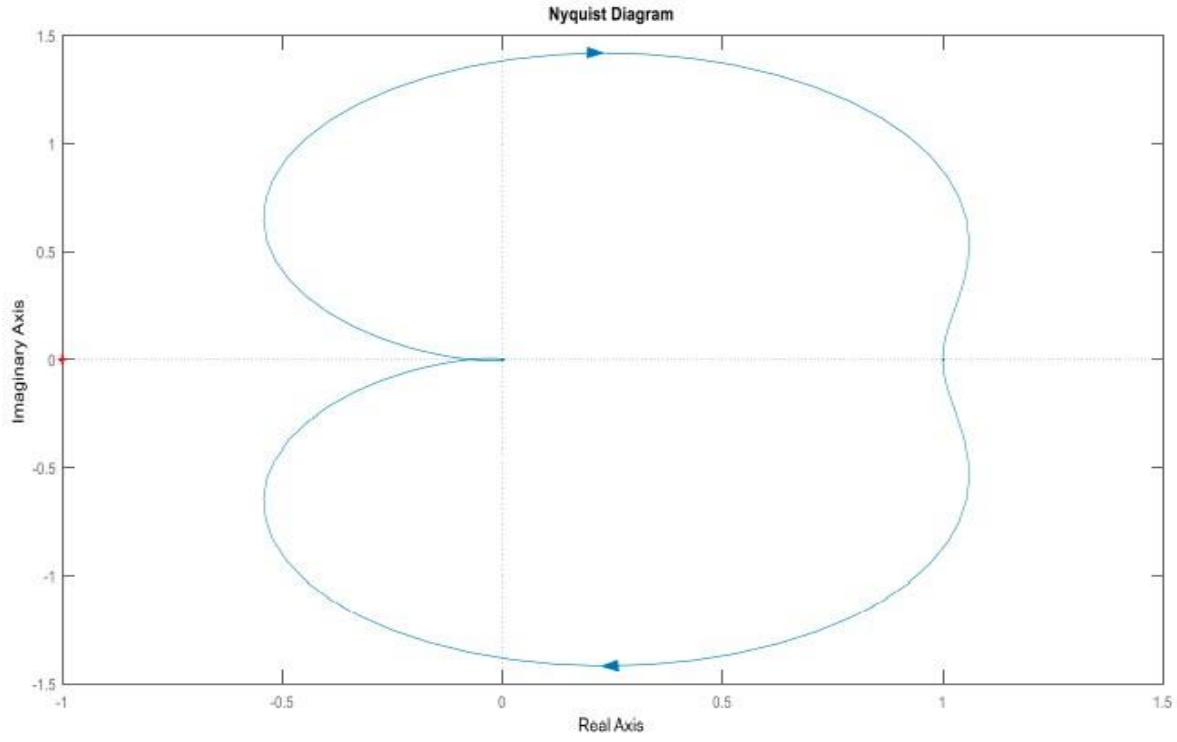
$$\begin{aligned}b_4 &= L_{\mathrm{ESC}}^2C_{\mathrm{ESC}}^2l^4/4!+3R_{\mathrm{ESC}}^2L_{\mathrm{ESC}}C_{\mathrm{ESC}}^3l^6/6!+R_{\mathrm{ESC}}^4C_{\mathrm{ESC}}^4l^8/8!+[R_{\mathrm{dr}}(C_{\mathrm{dr}}+C_l)+2R_{ESC}C_l]\\ &\times(2R_{\mathrm{ESC}}L_{\mathrm{ESC}}C_{\mathrm{ESC}}^2l^4/4!+R_{\mathrm{ESC}}^3C^3l^6/6!)+(R_{\mathrm{dr}}+R_{\mathrm{ESC}}+R_{\mathrm{ESC}}C_l/C_{\mathrm{ESC}})\\ &\times(2R_{\mathrm{ESC}}L_{\mathrm{ESC}}C_{\mathrm{ESC}}^3l^5/5!+R_{\mathrm{ESC}}^3C_{\mathrm{ESC}}^4l^7/7!)+2R_{\mathrm{dr}}R_{\mathrm{ESC}}C_{\mathrm{dr}}C_l(L_{\mathrm{ESC}}C_{\mathrm{ESC}}l^2/2!+R_{\mathrm{ESC}}^2C_{\mathrm{ESC}}^2l^4/4!)\\ &+(R_{\mathrm{dr}}R_{\mathrm{ESC}}(C_{\mathrm{dr}}+C_l)+R_{\mathrm{ESC}}^2C_l+(L_{\mathrm{ESC}}+R_{\mathrm{ESC}}R_{\mathrm{dr}}C_{\mathrm{dr}})C_l/C_{\mathrm{ESC}}\\ &\times(L_{\mathrm{ESC}}C_{\mathrm{ESC}}^2l^3/3!+R_{\mathrm{ESC}}^2C_{\mathrm{ESC}}^3l^5/5!)+R_{\mathrm{ESC}}C_{\mathrm{ESC}}^2l^3\times(R_{\mathrm{dr}}R_{\mathrm{ESC}}^2C_{\mathrm{dr}}C_l+L_{\mathrm{ESC}}R_{\mathrm{dr}}C_{\mathrm{dr}}C_l/C_{\mathrm{ESC}})/3!\end{aligned} \tag{5.27}$$

In this analysis E_{f} is assumed 0.2eV.

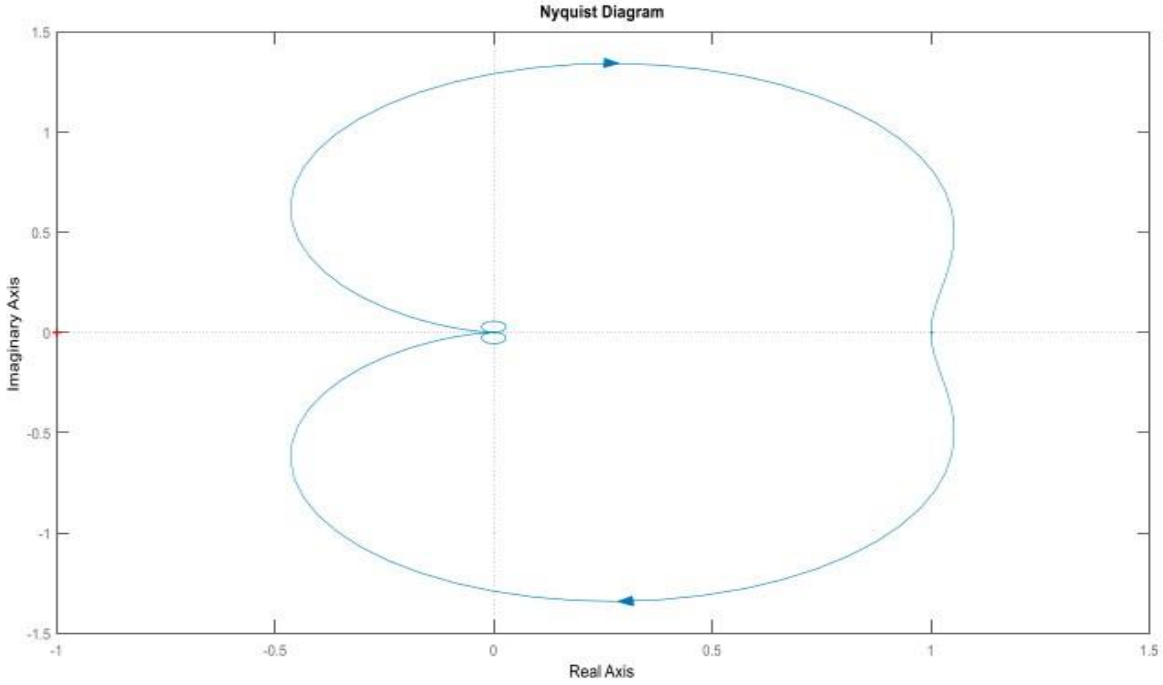
Table 5.2 shows the coefficients of transfer function and Figure 5.10 shows the relative stability through Nyquist diagrams at length 2000µm and temperature 500K of MLGNR interconnects for three different technological nodes.

Table 5.2 Coefficients of transfer function at length 2000µm, temperature 500K of MLGNR for three different technological nodes

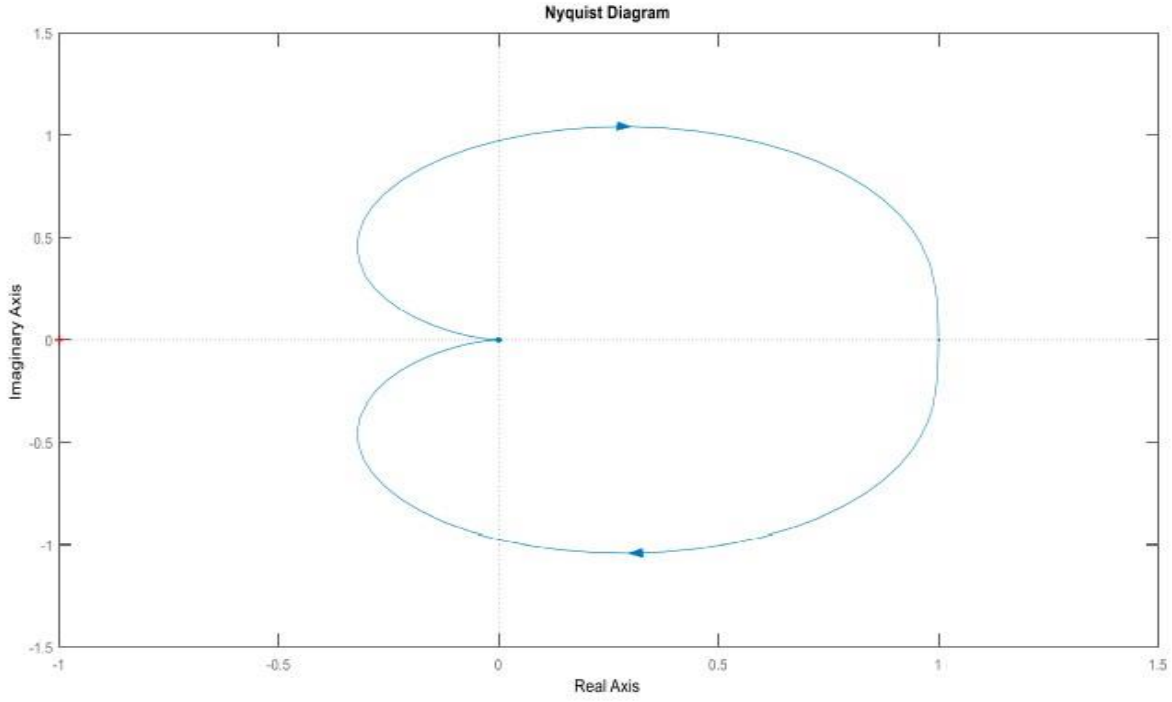
Coefficients	32nm	22nm	16nm
b_4	24.5110	42.3133	50.7651
b_3	154.6756	1.3099	3.1493
b_2	207.7872	863.3299	900.5746
b_1	11.1657	22.7596	30.8340
b_o	1	1	1



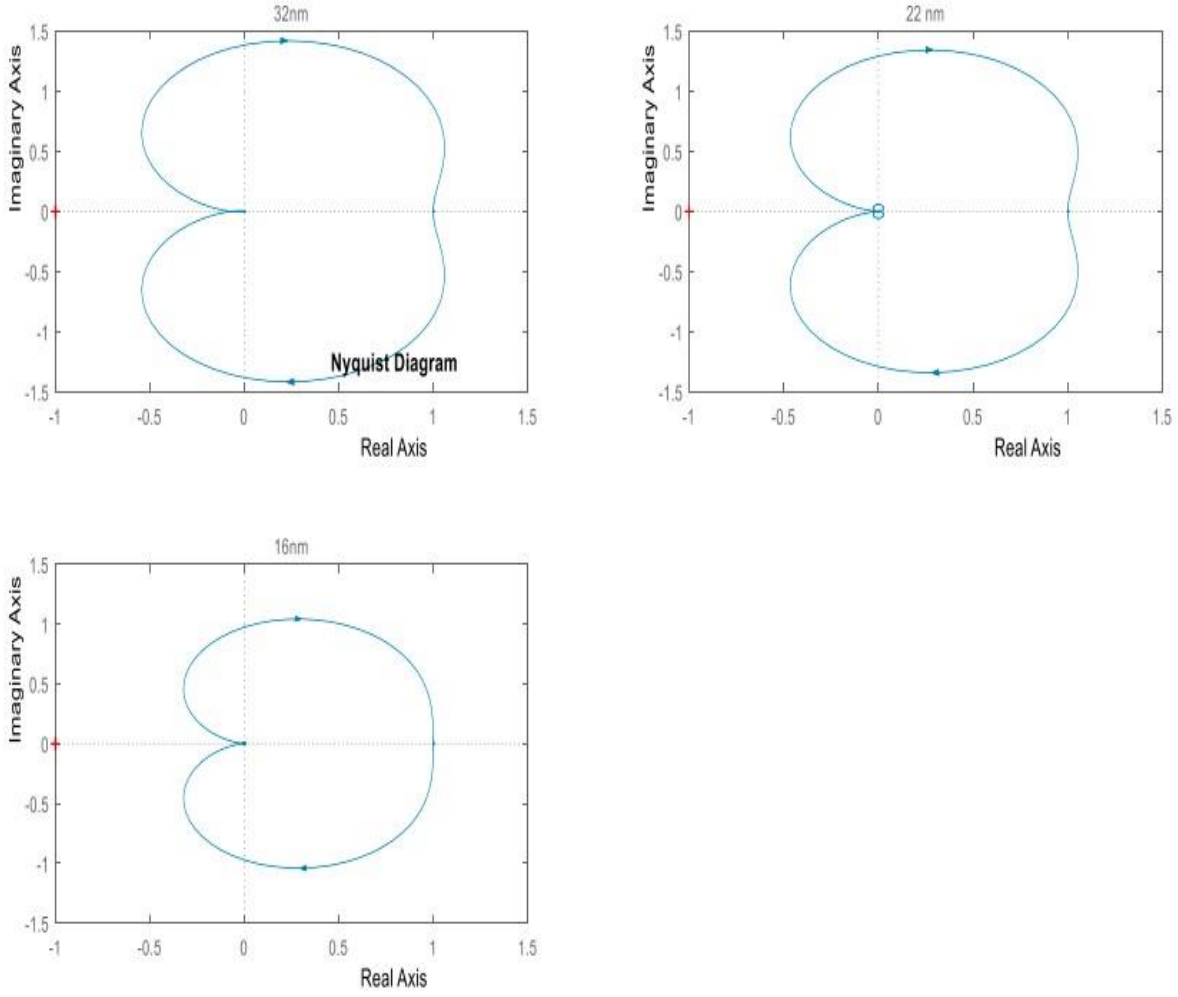
(a)


Nyquist Diagram
Imaginary Axis
Real Axis
1.5
1
0.5
0
-0.5
-1
-1.5
-1
-0.5
0
0.5
1
1.5

(b)


Nyquist Diagram
Imaginary Axis
Real Axis
1.5
1
0.5
0
-0.5
-1
-1.5
-1
-0.5
0
0.5
1
1.5

(c)



(d)

Figure 5.10 Nyquist plots of MLGNR at length 2000µm, temperature 500K for (a) 32nm, (b) 22nm, and (c) 16nm technological nodes. (d) Combined Nyquist plots for three technological nodes

As it can seen in Figure 5.10 that the critical point is located (-1,0) for all three technological nodes. With downscaling of technological nodes, impact of temperature is higher on the parasitic of MLGNR. However, the MFP of MLGNR shrinks with scaling of technological nodes and considering temperature impact results in rise of parasitic parameters and elevates stability of system. Figure 5.10(a) shows relative stability through Nyquist plot of MLGNR at 32nm technological node whereas Figure 5.10(b) and (c) shows for 22nm and 16nm nodes respectively. Nyquist plot in Figure 5.10(c) of MLGNR at 16nm technological node, achieve stability rapidly compared to 32nm and 22nm technological nodes. The combined Nyquist plots for three various technological nodes have been shown in Figure 5.10(d). Hence, it is proved through Nyquist plots that the system will be more stable having higher values of parasitic and

16nm technological node is more stable compared to 22nm and 32nm technological nodes of MLGNR. Therefore, it is concluded that the ESC circuit of MLGNR presented in this research is stable at global lengths for three various technological nodes used for simulation as well as analytical models.

5.5 Chapter summary

This chapter presents the temperature-dependent analytical delay model of MLGNR and the obtained outcomes are compared with the simulated results presented in chapter 4. The analytical expressions are presented to convert RLC multi-conductor circuit of MLGNR into a single conductor transmission line. The optimum number of repeaters are used to calculate the analytical delay at 2000µm length for three various technological nodes. The analytical and simulated results are obtained at 2000-µm interconnect length for 32nm, 22nm, and 16nm nodes of technology under 200–500K temperature range of MLGNR. The simulation and analytical results reveal that the outcomes of the two models correspond well. The trend of the models shows the increase in delay with the rising temperature levels (200–500K) for 32nm, 22nm, and 16nm nodes of technology. Relative stability of MLGNR is analyzed from 500–2000µm length w.r.t. switching delay and observed that with increasing interconnect length switching delay increases as a result input signal damp faster which upswings the relative stability of MLGNR for all three various technological nodes. Moreover, relative stability is also analyzed at length 2000µm and temperature 500K of MLGNR through Nyquist plots and observed that the system will achieve stability faster as we move from 32nm to 16nm technological node due to higher values of parasitic because of the reduction in MFP of electrons.

Publication from this chapter

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CHAPTER 6

PERFORMANCE AND COMPARATIVE ANALYSIS OF MULTILAYER GRAPHENE NANORIBBONS WITH COPPER AND SWCNT INTERCONNECTS

The combined effect of Fermi energy and temperature-dependent performance analysis of the MLGNR at global lengths for 32nm, 22nm, and 16nm nodes of technology is presented in this chapter. The impedance models dependent on temperature for SWCNT and copper interconnects are explored. Further, the comparison of MLGNR with copper, and SWCNT interconnects is presented for global lengths at different nodes of technology.

6.1 Introduction

The impact of variation of Fermi-energy on the number of conduction channels is analyzed and presented in chapter 3 for 32nm, 22nm, and 16nm nodes of technology. On the basis of an electrical model, the influence of intercalation doping in MLGNR with respect to delay and PDP as performance parameters for three different technological nodes is also discussed in chapter 3. Moreover, comparative analysis with copper interconnect is performed at equal interconnect lengths and technology nodes. Likewise, influence of temperature on the performance of MLGNR is discussed and presented in chapter 4. The equivalent transmission model of MLGNR is proposed and analyzed that the MFP depends on the variable thermal conditions of the integrated circuits. From the proposed mathematical equations, this has been observed that the MFP of GNR is inversely proportional to temperature that dominates further its own resistance at changing global lengths (500μm to 2000μm) for all three technological nodes. The impedance and performance analysis dependent on temperature of MLGNR from power dissipation, signal delay, and PDP parameters at global interconnect levels for three various technological nodes is also presented. In this chapter, the combined impact of Fermi energy as well as temperature on the performance of MLGNR in delay and PDP terms at global lengths for three various technological nodes is analyzed. The impedance model dependent on temperature for copper interconnects is presented and its performance is benchmarked with MLGNR (temperature dependent) in power dissipation, delay, as well as PDP parameters and analyzed that the performance of MLGNR is far better than copper at 2000μm length over temperature 200–500K for three different technological nodes (16nm, 22nm, and 32nm).

Moreover, impedance model dependent on temperature for SWCNT is presented and its performance is examined with respect to MLGNR and copper interconnects in delay and PDP terms and observed MLGNR performance is superior compared to SWCNT and copper at longer levels for all three nodes of technology under 200–500K temperature range.

6.2 Temperature and Fermi energy dependent performance analysis of MLGNR Interconnect

In this section, the combined impact of different levels of Fermi energies (0.2eV, 0.4eV and 0.6eV) and variable temperatures (200–500K) on the performance of MLGNR from signal delay as well as PDP perspectives at 2000μm length for 32nm, 22nm and 16nm nodes of technology is examined in detail. MATLAB computing software is used to calculate the parasitic parameters for MLGNR interconnects, based on ITRS-2013 (Table 6.1) and the derived values have been simulated in a SPICE tool.

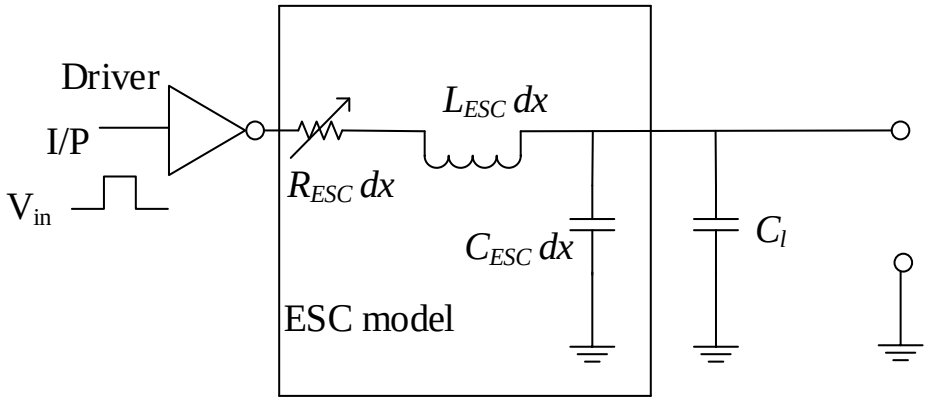


Figure 6.1 Temperature and Fermi energy dependent ESC model of MLGNR interconnect

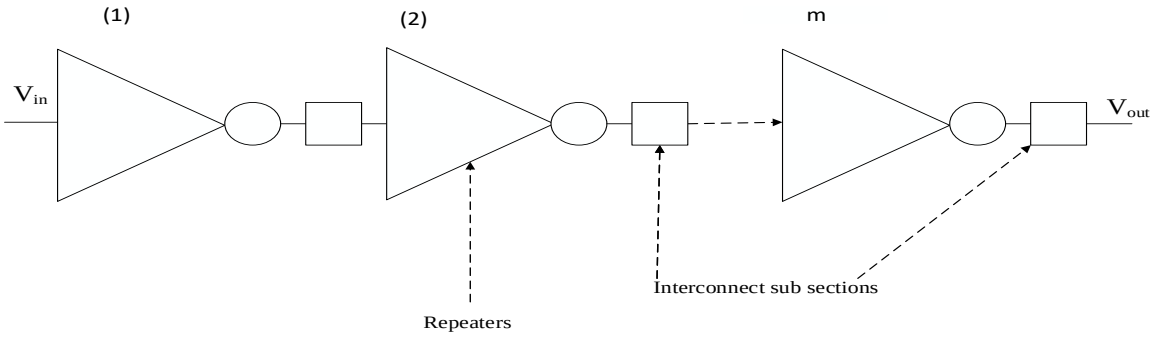


Figure 6.2 Repeaters are used to drive an interconnect divided into subsections

A CMOS inverter is used to drive the ESC model (Figure 6.1) for all three nodes of technology with 0.01fF load capacitance and RLC distributed model is used for increasing driving

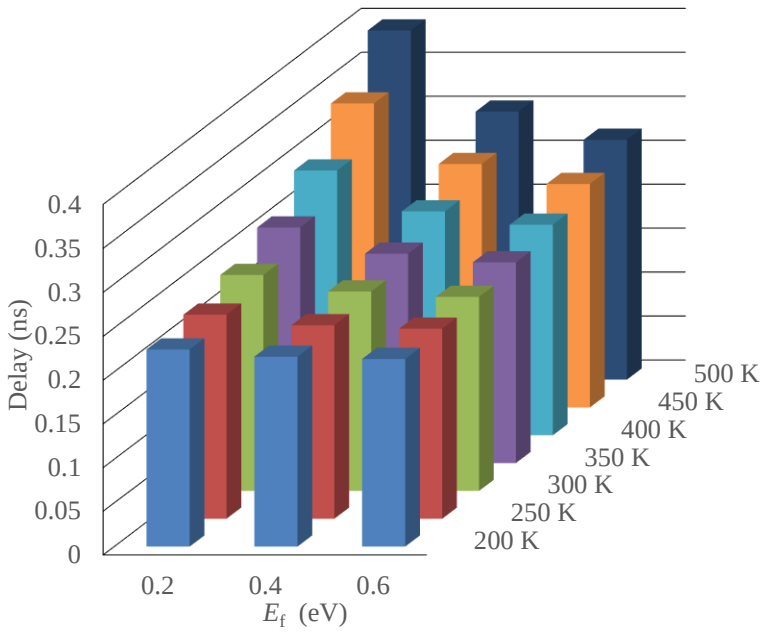
capability and reducing delay (Figure 6.2). The parameters of simulation for three different nodes of technology are shown in Table 6.1.

Table 6.1 Simulation parameters

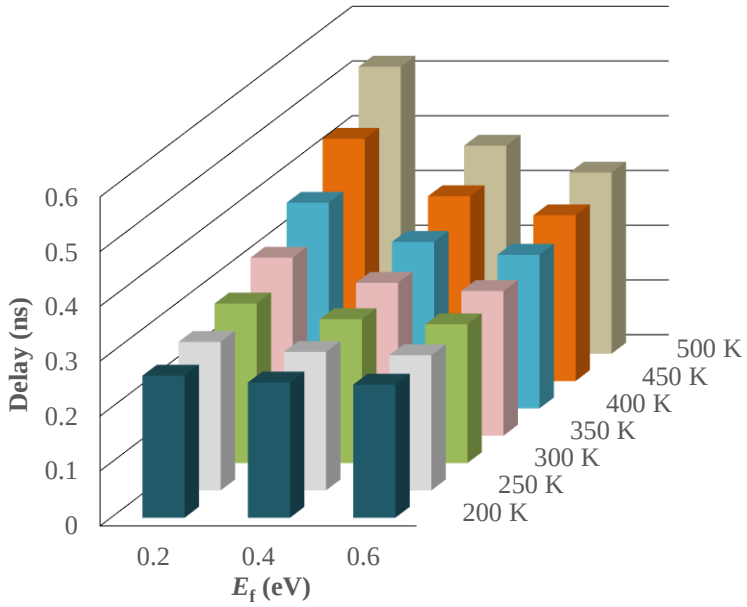
Parameters	32nm	22nm	16nm
Frequency(GHz)	1	1	1
V_{DD}(volts)	0.9	0.8	0.7
Repeater size(W/L)	30	30	40
Number of repeaters	2	2	2
Model file(PTM)	54	54	54

6.2.1 Temperature and Fermi energy dependent signal delay of MLGNR

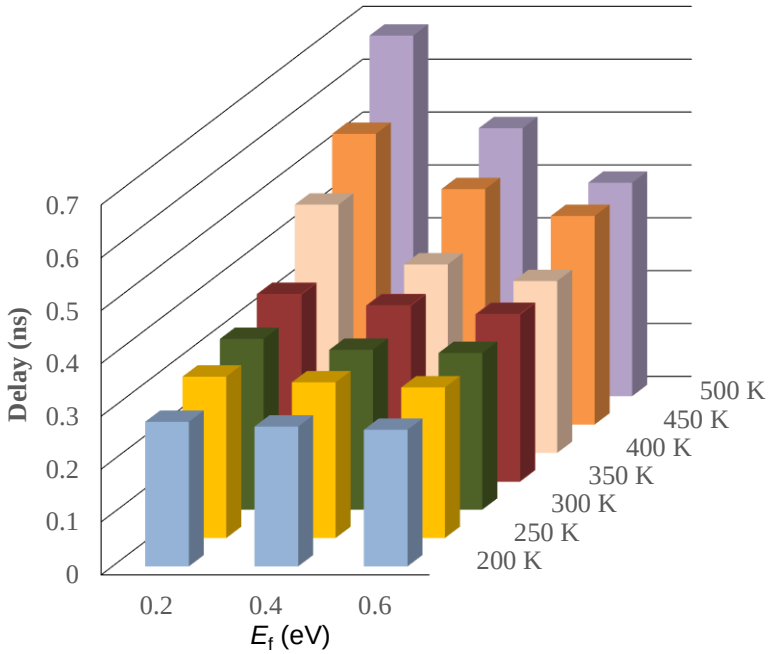
The electronics circuit operational speed is affected by the signal delay at the output of wire. The effect of Fermi energy on the MLGNR performance has been discussed in chapter 3 and effect of temperature has been presented in chapter 4. Under this sub-section, combined effect of variable temperatures and Fermi energies dependent performance has been analyzed for MLGNR with respect to delay at 2000µm for three different technological nodes (16nm, 22nm, and 32nm). Figure 6.3 shows that the MLGNR signal delay increases with rising temperatures (200–500K) due to shrinking of effective MFP as discussed in chapter 4, but, rising levels of



(a)



(b)



(c)

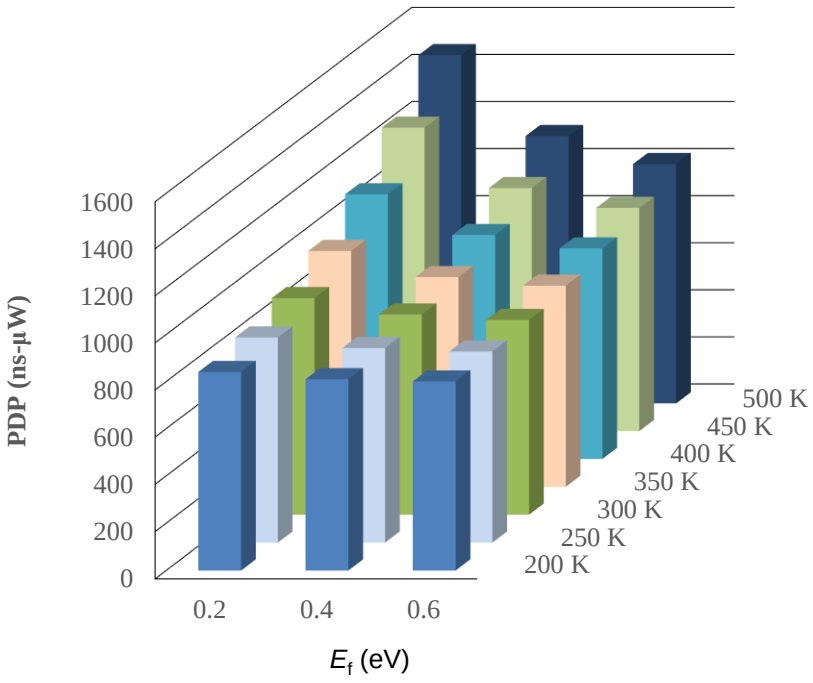
Figure 6.3 (a), (b), and (c) Temperature and Fermi energy dependent delay of MLGNR at 2000µm length for 32nm, 22nm, and 16nm nodes of technology respectively

Fermi energies (0.2eV, 0.4eV, and 0.6eV) increases number of conduction channels, and thereby decreases delay, for all three technological nodes. Therefore, it is analyzed that MLGNR performance is affected by thermal variable conditions but considering the impact of

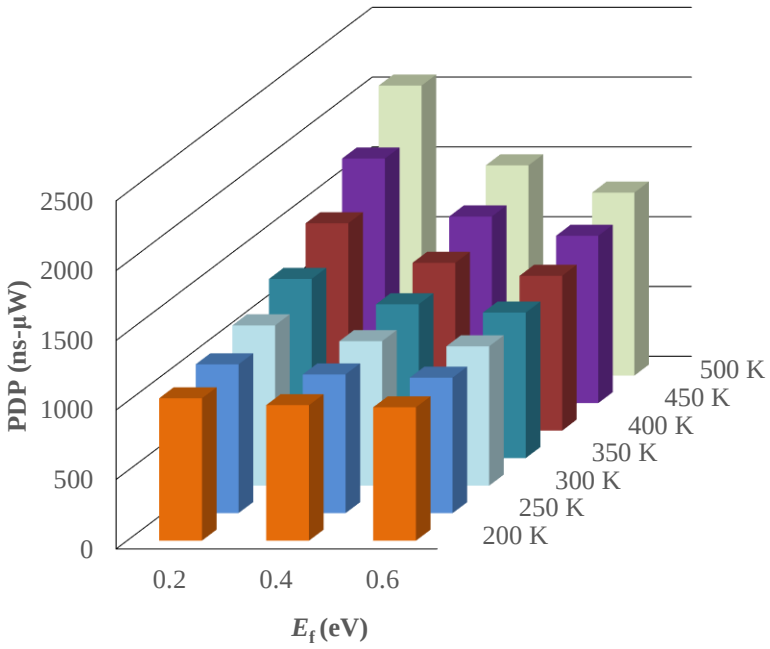
Fermi energy on MLGNR; improves its performance due to the reduction in delay at global interconnect levels for three different technological nodes.

6.2.2 Temperature and Fermi energy dependent PDP of MLGNR

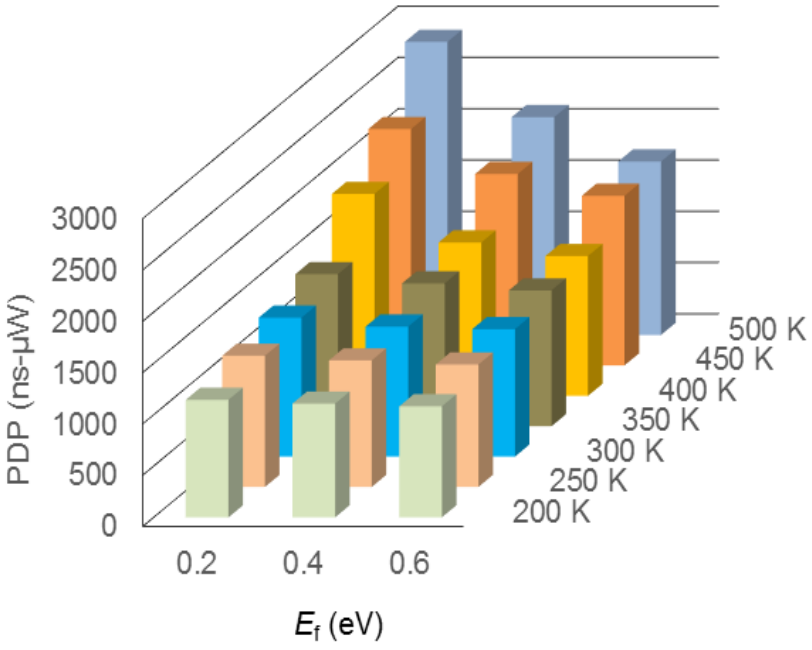
In VLSI design, power dissipation is of great concern in integrated circuits with the growth of VLSI industry. Power is basically the heat dissipation corresponding to charging and discharging of wire capacitance. The overall performance of an interconnect depends on the product of power dissipation and signal delay. Figures 6.3 and 6.4 show that, due to an increase in temperature the shrinking of effective MFP takes place, therefore the delay and PDP rises at 2000μm length for three different nodes of technology. Figure 6.4 shows that PDP decreases significantly for MLGNR at all three technological nodes as a result of the increasing level of Fermi energies.



(a)



(b)



(c)

Figure 6.4 (a), (b), and (c) Temperature and Fermi energy dependent PDP of MLGNR at 2000µm length for 32nm, 22nm, and 16nm nodes of technology respectively

It is analyzed that the actual performance depends on PDP and must be taken into account for elite integrated circuits. Thus low value of PDP is prudent which is shown in this sub-section.

6.3 Impedance model (Temperature dependent) of copper interconnect

This section demonstrates the copper interconnect under the influence of temperature. Figure 6.5 presents the 3D view of three copper interconnects in parallel combination, separated with spacing *s* from each other, and positioned at a distance *d* from the level of ground. The parasitic parameters of copper dependent on temperature are presented in this section. Therefore, temperature dependent resistance (p.u.l.) of rectangular cross-section is determined by equation 6.1 [117, 142, 143],

$$R_{Cu}(T) = R_o\left[1+\gamma(T-T_o)\right] \tag{6.1}$$

Where γ defines temperature dependent resistance coefficient having $0.0039K^{-1}$, resistance (R_o) at room temperature is estimated as $R_o = \frac{\rho_o l}{A}$

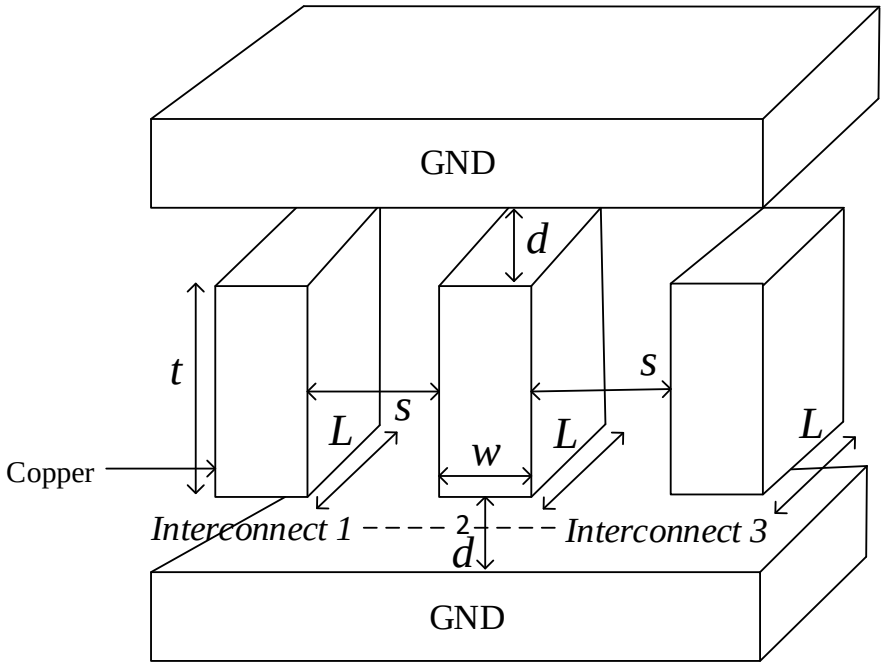


Figure 6.5 3D view of copper interconnect

At room temperature the copper resistivity is defined by ρ_o and is dependent on technological node (Table 3.1) [16].

The impedance parameters (inductance and capacitance) of copper interconnect are provided by equations 6.2 and 6.3 [16, 117,142, 143].

$$L_{Cu} = \frac{\mu_o l}{2\pi}\left[In\left(\frac{2l}{w+t}\right)+\frac{1}{2}+\frac{0.22(w+t)}{l}\right] \tag{6.2}$$

$$C_g = \varepsilon_o\varepsilon_r\left[\frac{w}{d}+2.22\left(\frac{s}{s+0.7d}\right)^{3.19}+1.17\left(\frac{s}{s+1.15d}\right)^{0.76}\left(\frac{t}{t+4.53d}\right)^{0.12}\right] \tag{6.3}$$

Where A is defined by area. ϵ_r is dielectric constant dependent on technological node [16] of copper interconnect.

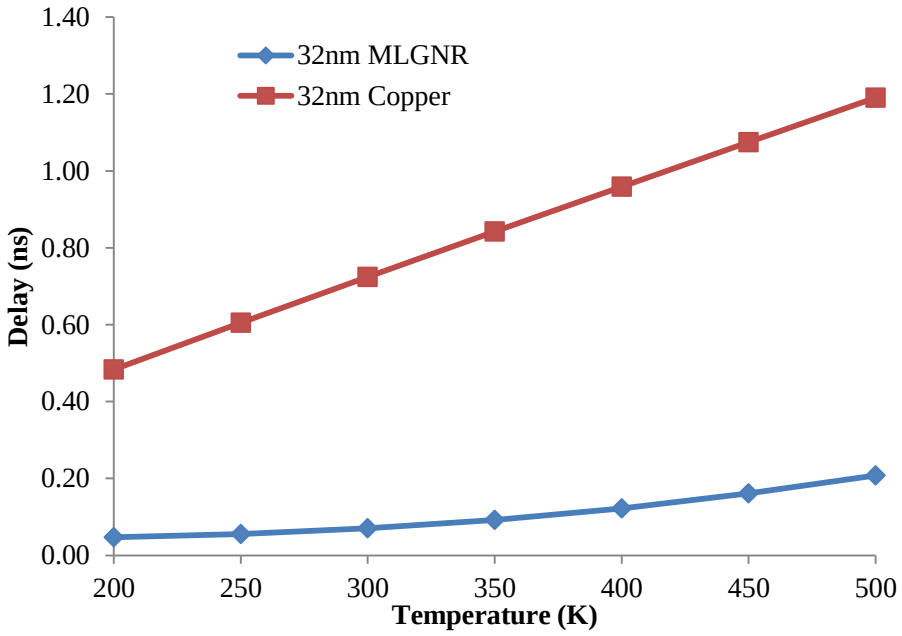
6.4 Performance analysis (Temperature dependent) of MLGNR and copper Interconnects

For all three technological nodes (32nm, 22nm, and 16nm), SPICE simulation tool is used for analyzing MLGNR and copper interconnects performance dependent on temperature from power dissipation, delay and PDP parameters. As previously explained in chapter 4, effective MFP (temperature dependent), that affect the parasitic parameters of GNR, moreover effects its performance in power dissipation, delay as well as PDP terms.

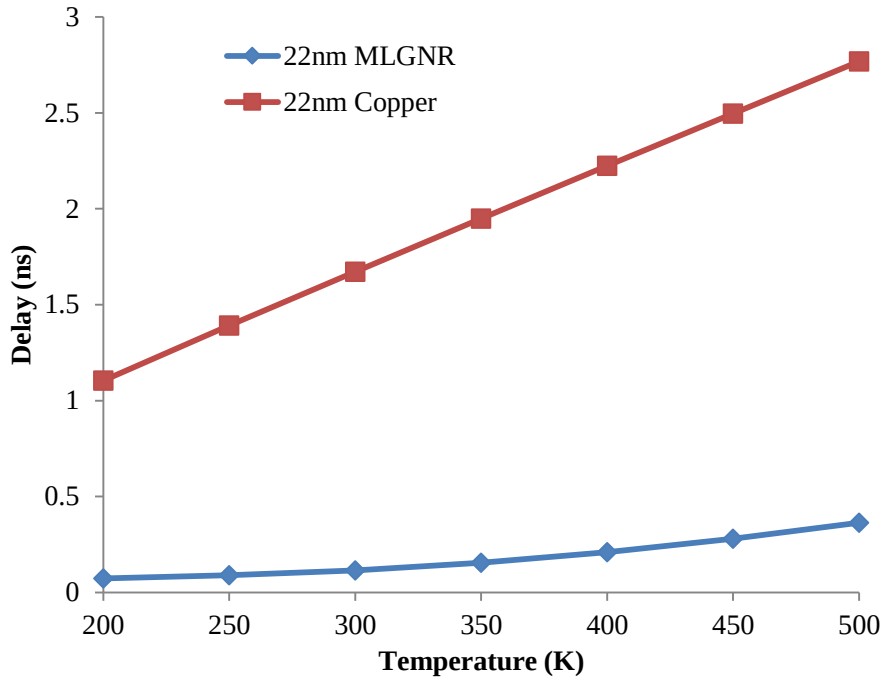
6.4.1 Signal delay analysis

The ESC model is considered driven by DIL system (Figure 3.11) for calculating and analyzing the interconnects performance from power dissipation, signal delay, and PDP perspectives, as presented in Figure 4.4. For three different nodes of technology, the equivalent circuit model is driven by a CMOS driver, with C_l as load capacitance of 0.01fF. The parameters of simulation for precise calculations are derived from ITRS 2013 and presented in Chapter 3, Table 3.1. For analyzing the MLGNR and copper interconnects performance, a simulation set up is utilized using DIL to simulate the parasitic parameters of copper and MLGNR interconnects.

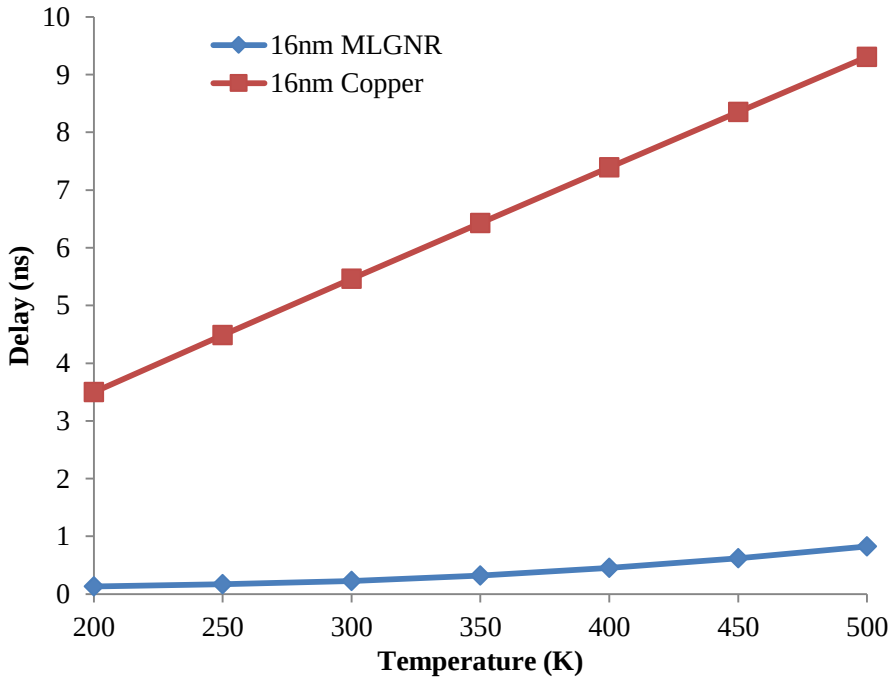
The thermally aware delay of copper and MLGNR interconnects is compared for 32nm, 22nm, and 16nm nodes of technology at 2000μm length as shown in Figures 6.6(a)–(c), respectively.



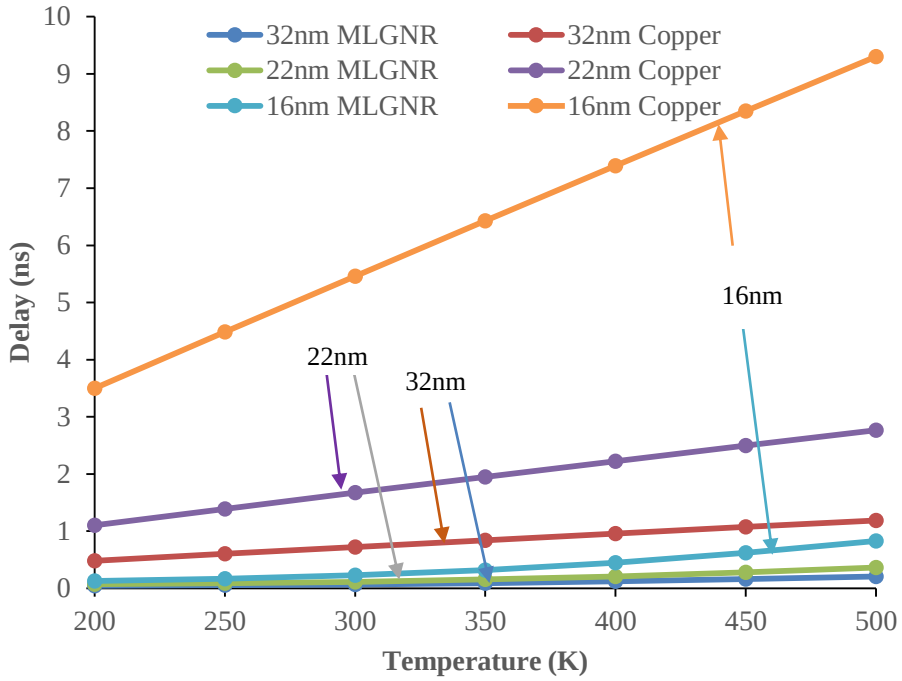
(a)


22nm MLGNR
22nm Copper
Delay (ns)
Temperature (K)
0
0.5
1
1.5
2
2.5
3
200
250
300
350
400
450
500

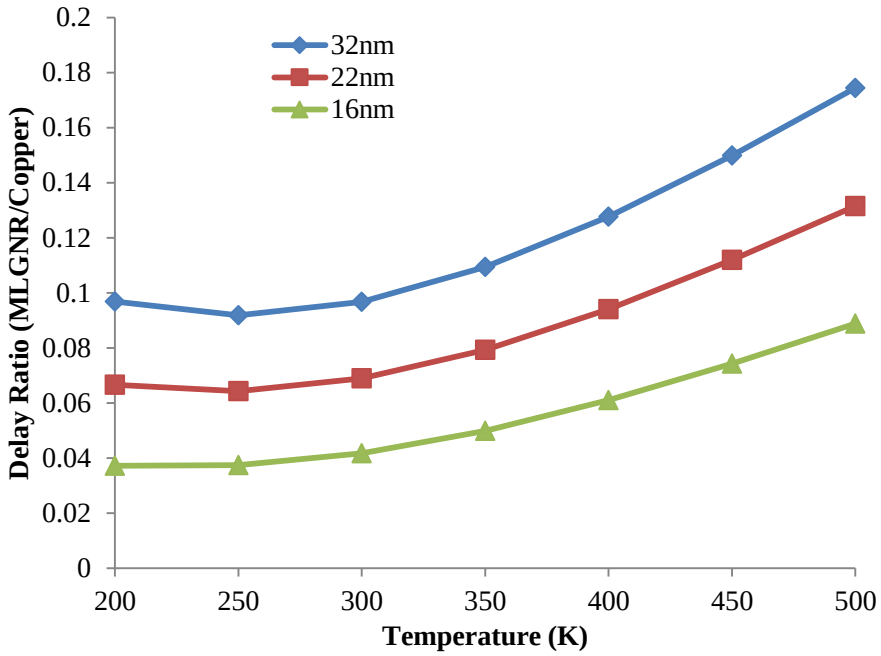
(b)


16nm MLGNR
16nm Copper
Delay (ns)
Temperature (K)
0
1
2
3
4
5
6
7
8
9
10
200
250
300
350
400
450
500

(c)



(d)



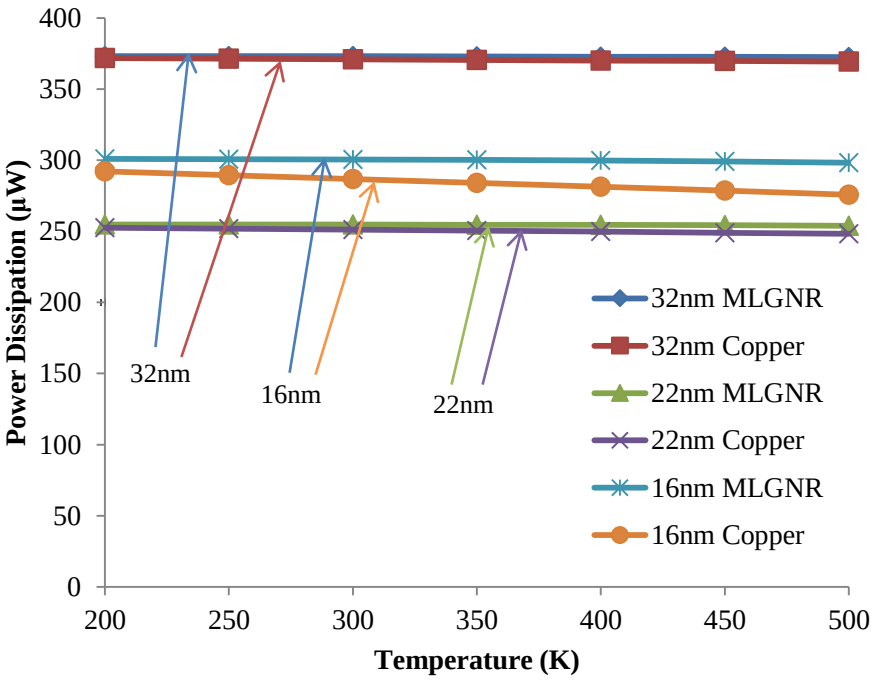
(e)

Figure 6.6 Performance analysis and comparison of copper and MLGNR at 2000µm length with respect to delay for (a) 32nm, (b) 22nm, and (c) 16nm nodes of technology. Combined delay of copper and MLGNR interconnects is depicted in panel (d). The delay ratio of MLGNR/Cu interconnects at 2000µm length for three nodes of technology as shown in panel (e)

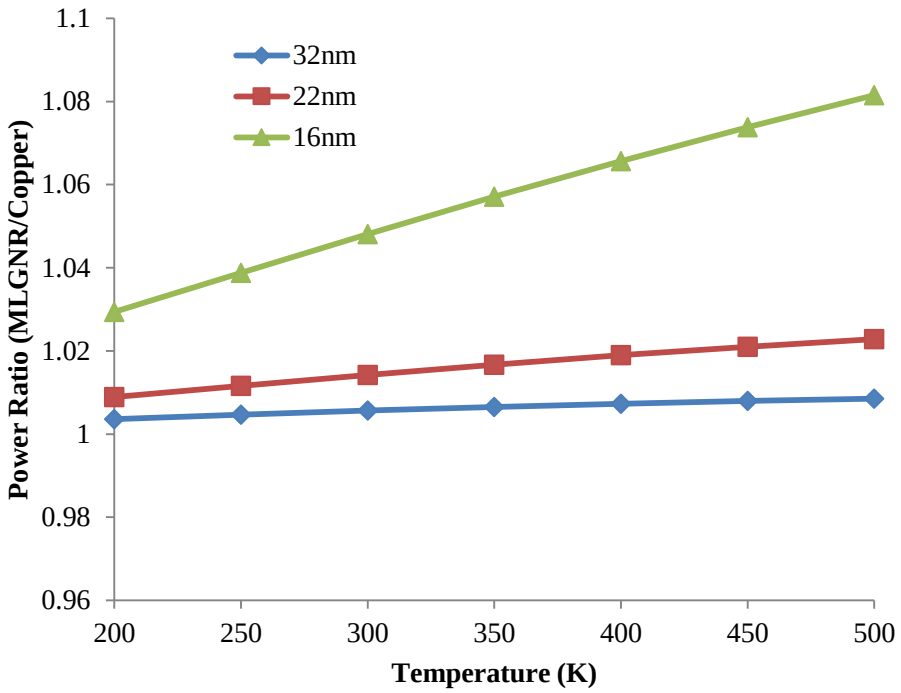
It has been examined that with rise in temperature the shrinking of effective MFP takes place at 2000µm interconnect length for three various nodes of technology of MLGNR. As a result, delay rises with rising temperature levels at global levels for all three technological nodes. Further, delay of MLGNR is smaller than copper interconnect at 2000µm length for 16nm, 22nm, and 32nm nodes of technology. Figure 6.6(d) describes the cumulative delay of the copper and MLGNR interconnects for all three technological nodes. Figure 6.6(e) demonstrates the MLGNR and copper interconnects delay ratio over a temperature spectrum of 200–500K. The delay ratio (MLGNR/Copper) is linear from 200 to 300K, but sharply increasing after 300K because of the increase in the value of copper interconnect. Therefore, it is apparent that the performance of MLGNR is far higher as compared to the copper at global interconnect length over a variable temperature range (200–500K).

6.4.2 Power dissipation and PDP analysis

Nowadays, in interconnects the role of power has become a significant issue as well as major concern with the growth of VLSI industry. Power dissipation of copper and MLGNR is shown in Figure 6.7(a) whereas their ratio at 2000µm interconnect length over 200–500K temperature range is depicted in Figure 6.7(b).



(a)



(b)

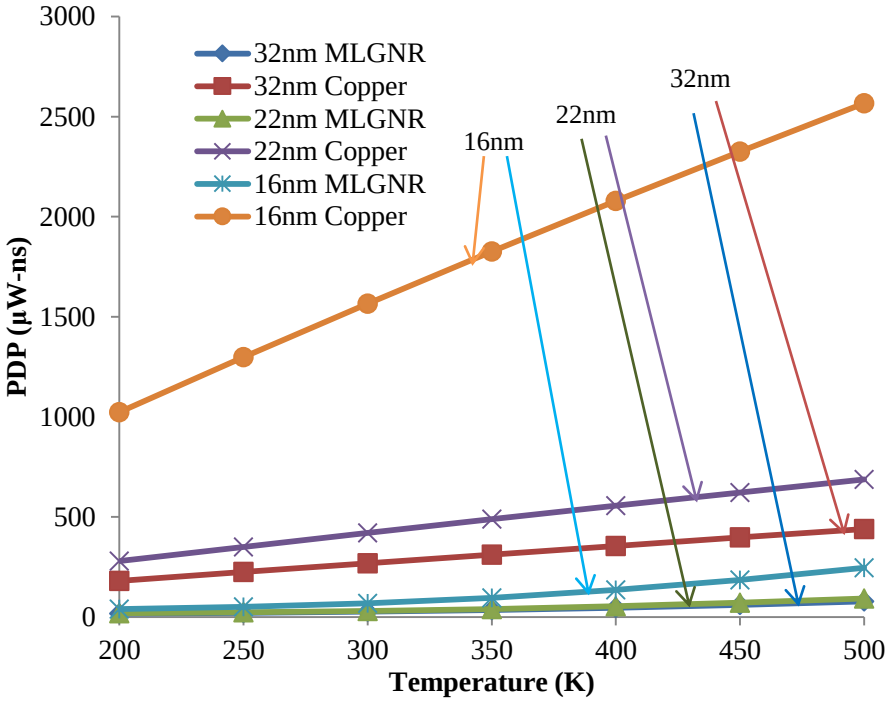
Figure 6.7 (a) Performance analysis and comparison of copper and MLGNR at 2000µm interconnect length with respect to power dissipation for 32nm, 22nm, and 16nm nodes of technology (b) The power ratio of MLGNR/Copper interconnects

Table 6.2 Cu and MLGNR PDP at 2000µm length for 16nm, 22nm, and 32nm nodes of technology

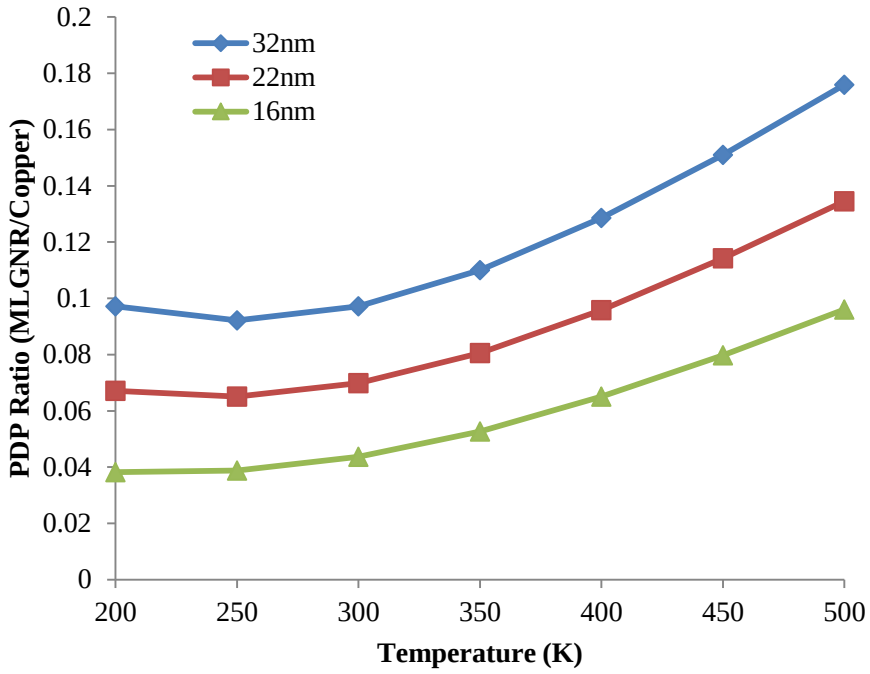
PDP (ns-µW)						
Temperature (K)	**MLGNR (32nm)**	**Cu (32nm)**	**MLGNR (22nm)**	**Cu (22nm)**	**MLGNR (16nm)**	**Cu (16nm)**
200	17.48422	179.8944	18.73744	279.0278	39.15068	1023.011
250	20.719	224.697	22.77996	350.3813	50.39186	1298.802
300	26.11599	268.6887	29.3353	420.0421	68.38464	1566.021
350	34.33941	312.0535	39.35077	488.3726	96.1924	1825.815
400	45.63319	354.9231	53.25141	555.6058	135.2216	2078.865
450	60.0122	397.3801	71.03069	621.8975	185.562	2325.642
500	77.30032	439.4739	92.42872	687.3027	246.5696	2566.445

Table 6.3 MLGNR and Cu PDP ratio at 2000µm length for 16nm, 22nm, and 32nm nodes of technology

Temperature (K)	PDP Ratio		
	MLGNR/Cu (32nm)	MLGNR/Cu (22nm)	MLGNR/Cu (16nm)
200	0.097192	0.067153	0.03827
250	0.092209	0.065015	0.038799
300	0.097198	0.069839	0.043668
350	0.110043	0.080575	0.052685
400	0.128572	0.095844	0.065046
450	0.15102	0.114216	0.07979
500	0.175893	0.13448	0.096074



(a)



(b)

Figure 6.8 (a) Performance analysis and comparison of copper and MLGNR at 2000µm interconnect length with respect to PDP for 32nm, 22nm, and 16nm nodes of technology (b) The PDP ratio of MLGNR/Copper interconnects

The power dissipation in copper is higher compared to MLGNR at 2000µm length for 32nm, 22nm, and 16nm nodes of technology at different temperature levels (Figure 6.7(a)). The power ratio MLGNR/copper is rising with increasing temperature levels due to higher power dissipation in copper interconnect (Figure 6.7(b)). Both delay as well power dissipation are independent parameters but the overall performance of an interconnect depends on product of power dissipation and signal delay. PDP of copper and MLGNR is given in Table 6.2 whereas their ratio (MLGNR/copper) is given in Table 6.3. Figure 6.8(a) presents the copper and MLGNR interconnects performance from PDP perspective at 2000µm length for 32nm, 22nm, and 16nm nodes of technology over variable 200–500K temperature range. It is analyzed that the PDP of MLGNR is smaller in comparison to copper interconnect at 2000µm length for all nodes of technology. MLGNR/Cu interconnects PDP ratio is given in Figure 6.8(b). PDP ratio is consistent for all three nodes of technology from 200 to 250K but after 250K, the PDP ratio sharply increase up to 500K because of the rise in the value of copper interconnects. The present study analyze that copper as interconnect is not appropriate in high-temperature machines for example space shuttles. Hence, MLGNR becomes eminent interconnect in high temperature operations compared to copper.

6.5 Impedance model (Temperature-dependent) of SWCNT bundle

Figure 6.9(a) presents the diagrammatical view of SWCNT shell having *D* diameter positioned at *d* distance from the level of ground, and SWCNT bundle is derived by parallel combination of SWCNT shells (Figure 6.9(b)) [142]. SWCNT bundle consist of three different resistive components i.e. r_s, R_q, R_c are the scattering, quantum, and contact resistances. The contact resistance of SWCNT bundle is within the range of few hundred ohms to tens of kilo ohm. If the SWCNT bundle length is smaller relative to the MFP of electrons, quantum resistance is examined, whereas, the scattering resistance impact is examined if the bundle length is greater as compared to MFP of electrons [53, 100, 144]. Figure 6.9(c) presents the ESC model for the proposed SWCNT bundle.

Equation 6.4 expressed the equivalent resistance (temperature-dependent) of SWCNT bundle ($R(T)_{bundle}$) having length *l* [53, 100, 144].

$$R(T)_{\text{bundle}} = \frac{R_q + r_s}{N_{\text{bundle}}} = \frac{\frac{h}{4e^2}\left[1 + \frac{l}{\lambda_{\text{eff}}(T)}\right]}{N_{\text{bundle}}} \qquad l > \lambda_{\text{eff}}(T) \tag{6.4}$$

Where electrons effective MFP is defined by λ_{eff}.

In a bundle, the total number of SWCNT tubes (N_{bundle}) are calculated from the number of columns and rows of the bundle. The number of SWCNT bundle also depends on the parity of number of rows. For the even number of rows, total tubes in a bundle can be defined by equation 6.5 [53, 100].

$$N_{\text{bundle}} = N_{\text{W(bundle)}} N_{\text{H(bundle)}} - \frac{1}{2} N_{\text{H(bundle)}} \tag{6.5}$$

For the odd number of rows, total tubes in a bundle can be defined by equations 6.6

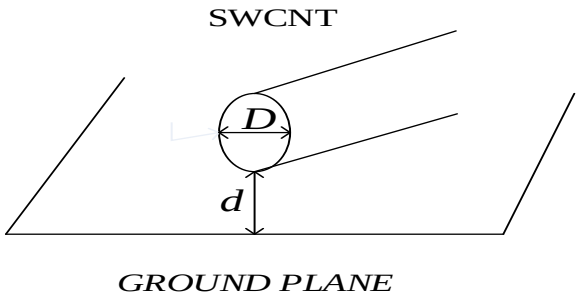
$$N_{\text{bundle}} = N_{\text{W(bundle)}} . N_{\text{H(bundle)}} - \frac{1}{2}(N_{\text{H(bundle)}} - 1) \tag{6.6}$$

Where $N_{\text{W(bundle)}}$, $N_{\text{H(bundle)}}$ are the number of columns and rows in a bundle respectively and calculated by equations 6.7 and 6.8

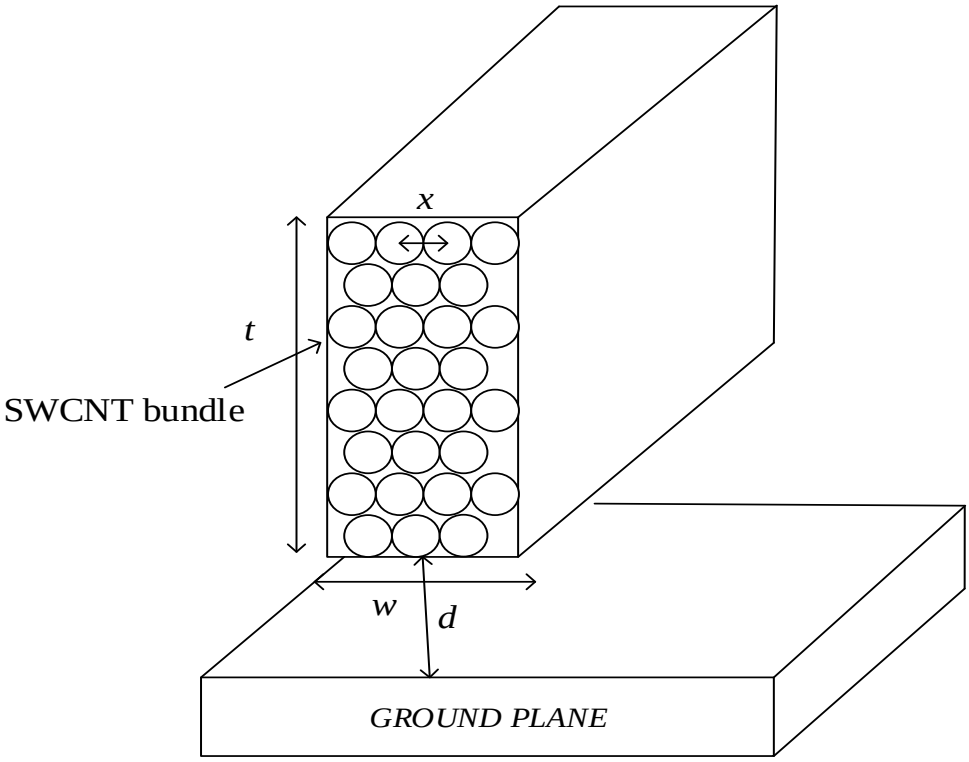
$$N_{\text{W(bundle)}} = \frac{w - D}{x} \tag{6.7}$$

$$N_{\text{H(bundle)}} = \left(\left[\frac{t - D}{\left(\frac{\sqrt{3}}{2}\right)x}\right] + 1\right) \tag{6.8}$$

Where *x*, *D* are the distance from center to center of adjoining-tubes and tube diameter respectively of the SWCNT bundle interconnects.



(a)



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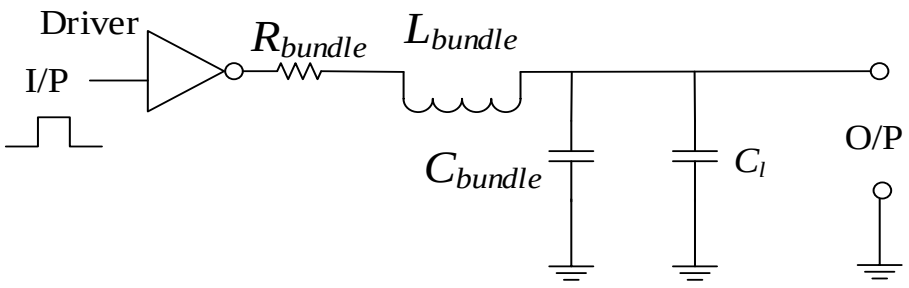


(c)

Figure 6.9 (a) Structure of SWCNT (b) The parallel combination of tube shells in SWCNT bundle (c) The ESC model of SWCNT bundle

Hence, total number of tubes in SWCNT bundle can re-written as [53]

$$N_{\text{bundle}} = \left\lfloor \frac{w-D}{x} \right\rfloor \left(\left\lfloor \frac{t-D}{\left(\frac{\sqrt{3}}{2}\right)x} \right\rfloor + 1 \right) - \frac{1}{2} \left(\left\lfloor \frac{t-D}{\left(\frac{\sqrt{3}}{2}\right)x} \right\rfloor + 1 \right) \tag{6.9}$$

With even number of rows and,

$$N_{\text{bundle}} = \left\lfloor \frac{w-D}{x} \right\rfloor \left(\left\lfloor \frac{t-D}{\left(\frac{\sqrt{3}}{2}\right)x} \right\rfloor + 1 \right) - \frac{1}{2} \left(\left\lfloor \frac{t-D}{\left(\frac{\sqrt{3}}{2}\right)x} \right\rfloor \right) \tag{6.10}$$

With odd number of rows.

The SWCNT shell has magnetic and kinetic inductances can be defined by equations 6.12 and 6.11, respectively [53, 100].

$$l_{\text{ko}} = \frac{h}{2e^2 v_{\text{f}}} \tag{6.11}$$

$$l_{\text{mo}} = \frac{\mu_{\text{o}}}{2\pi} \ln\left(\frac{d}{D}\right) \tag{6.12}$$

Therefore, the SWCNT bundle inductance can be expressed by equation 6.13.

$$L_{\text{bundle}} = \left(\frac{l_{\text{ko}} + l_{\text{mo}}}{4N_{\text{bundle}}} \right) \tag{6.13}$$

Equations 6.14 and 6.15 is used to calculate the electrostatic and quantum capacitance of SWCNT shell, respectively [53, 100].

$$C_{\text{e}}^{\text{bundle}} = 2\left(\frac{2\pi\varepsilon_{\text{ox}}}{\ln\left(s/D\right)} \right) + \left(\frac{\left\lfloor \frac{w-D}{x} \right\rfloor - 2}{2} \right) \left(\frac{2\pi\varepsilon_{\text{ox}}}{\ln\left((s+w)/D\right)} \right) + 3\left(\frac{2\pi\varepsilon_{\text{ox}}}{\ln\left(s/D\right)} \right) \left(\frac{N_{\text{H(bundle)}} - 2}{5} \right) \tag{6.14}$$

$$C_{\text{q}}^{\text{bundle}} = \left(\frac{2 \times 2e^2}{h v_{\text{f}}} \right) N_{\text{bundle}} \tag{6.15}$$

Hence, the total SWCNT bundle capacitance can be defined by equation 6.16.

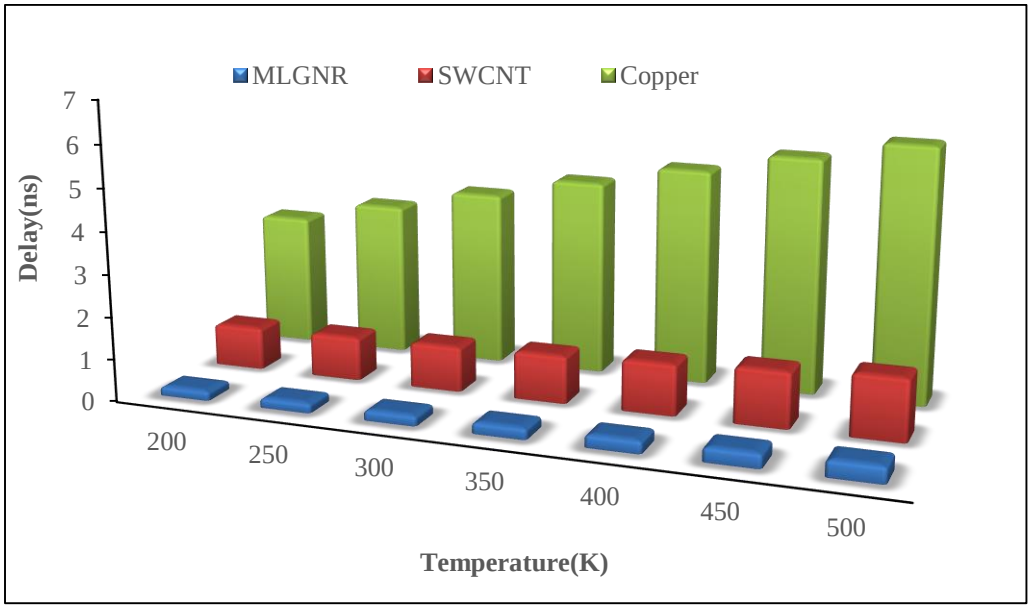
$$C_{\text{bundle}} = \left(\frac{C_{\text{e}}^{\text{bundle}} . C_{\text{q}}^{\text{bundle}}}{C_{\text{e}}^{\text{bundle}} + C_{\text{q}}^{\text{bundle}}} \right) \tag{6.16}$$

6.6 Comparison of MLGNR, Copper, and SWCNT Interconnects

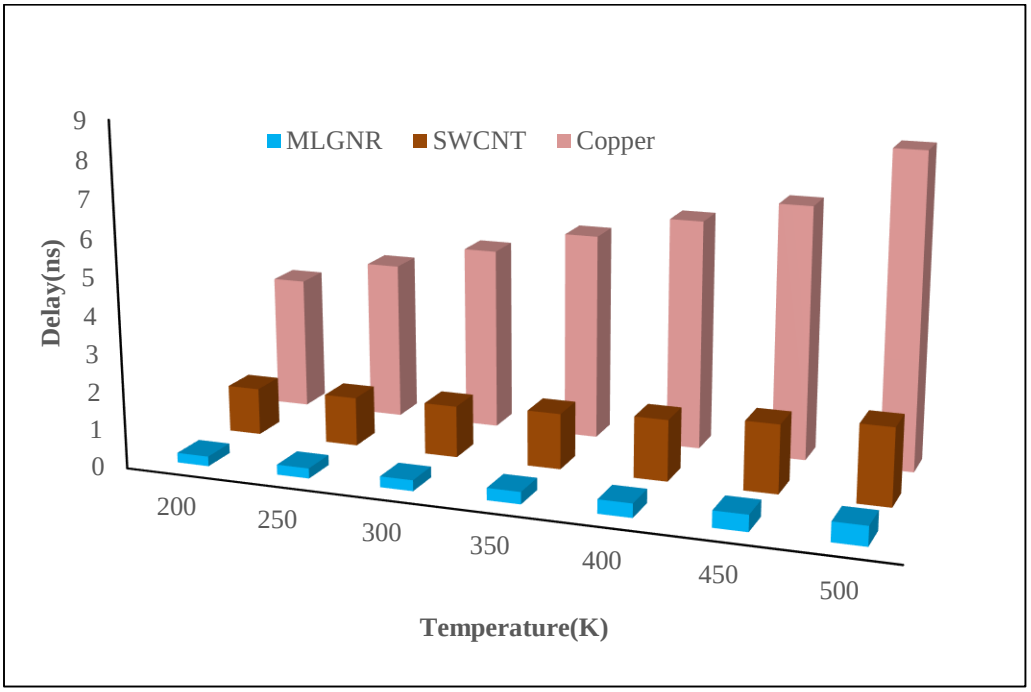
In current portion, MLGNR, copper, and SWCNT interconnects performance related to PDP and signal delay under temperature ranging in 200 to 500K at 2000μm length are compared. A 0.2eV Fermi energy is considered for MLGNR interconnect. Table 6.4 presents the signal delay for SWCNT, copper as well as MLGNR interconnects and the outcomes are presented graphically in Figures 6.10(a)–(c) graphically for 32nm, 22nm, and 16nm nodes of technology, respectively. It has been observed that as compared to copper and SWCNT, MLGNR has smaller signal delay at different levels of temperatures. It can therefore be inferred that MLGNR is an excellent material

Table 6.4 Delay of Cu, MLGNR, and SWCNT at 2000μm length for 16nm, 22nm, and 32nm nodes of technology

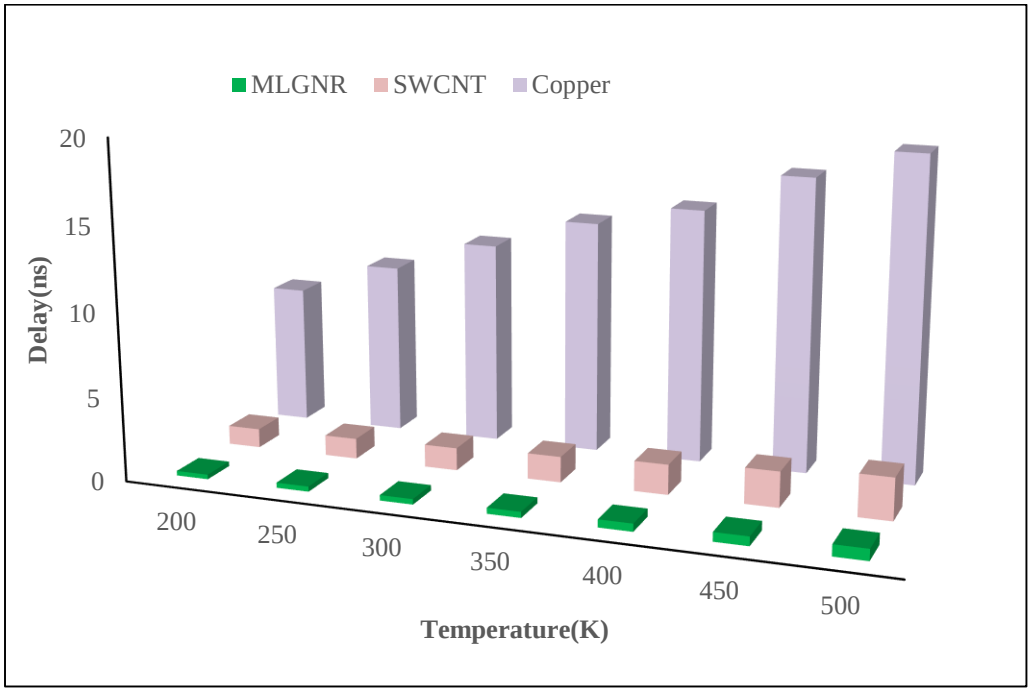
Temp. (K)	Delay(ns)								
	32nm			22nm			16nm		
	MLGNR	SWCNT	Cu	MLGNR	SWCNT	Cu	MLGNR	SWCNT	Cu
200	0.225	1.011	3.143	0.2585	1.25	3.547	0.2733	1.126	8.25
250	0.2331	1.037	3.639	0.2702	1.298	4.205	0.3052	1.212	10.17
300	0.2464	1.077	4.130	0.2906	1.368	4.847	0.3229	1.340	12.04
350	0.2685	1.137	4.614	0.3246	1.474	5.476	0.353	1.529	13.88
400	0.3015	1.223	5.093	0.3751	1.625	6.094	0.4695	1.791	15.12
450	0.3459	1.337	5.566	0.4423	1.823	6.70	0.5499	2.125	17.46
500	0.3970	1.478	6.03	0.5243	2.064	8.301	0.6821	2.52	19.22



(a)



(b)

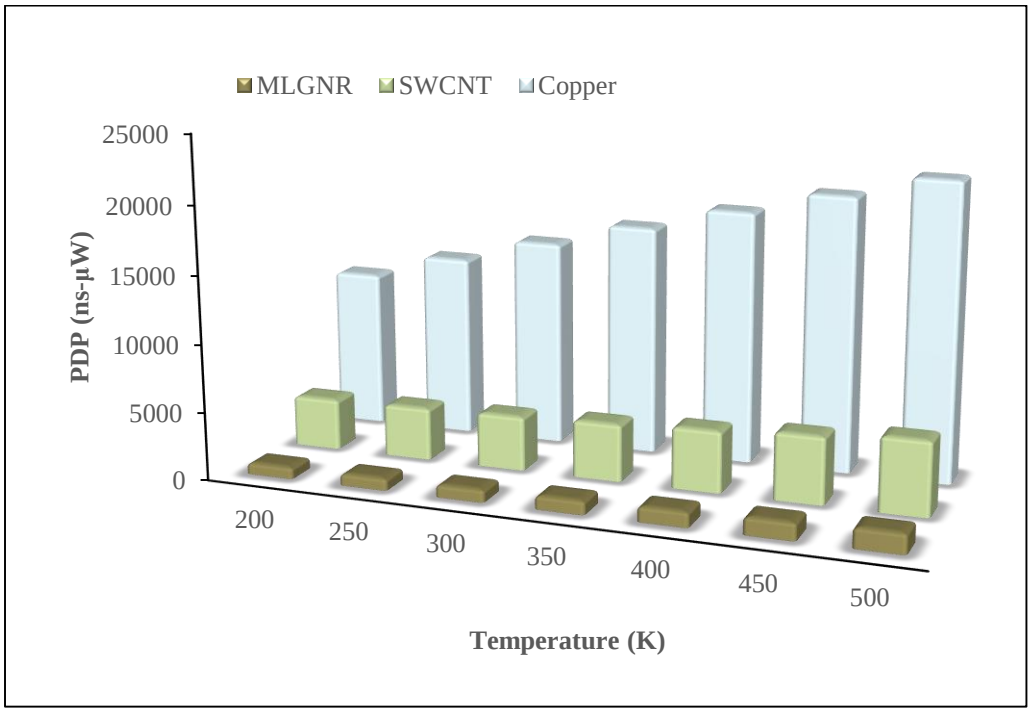


(c)

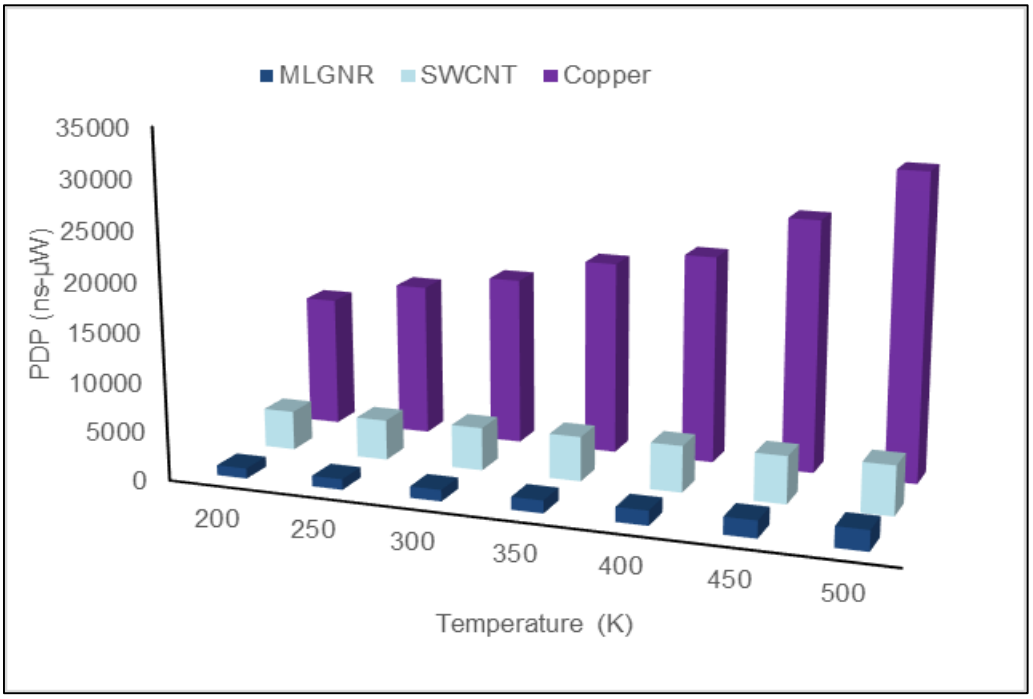
Figure 6.10 Performance analysis and comparison of delay of copper, SWCNT and MLGNR at 2000µm length for (a) 32nm, (b) 22nm, and (c) 16nm technological nodes

Table 6.5 PDP of Cu, MLGNR, and SWCNT at 2000µm interconnect length for 16nm, 22nm, and 32nm nodes of technology

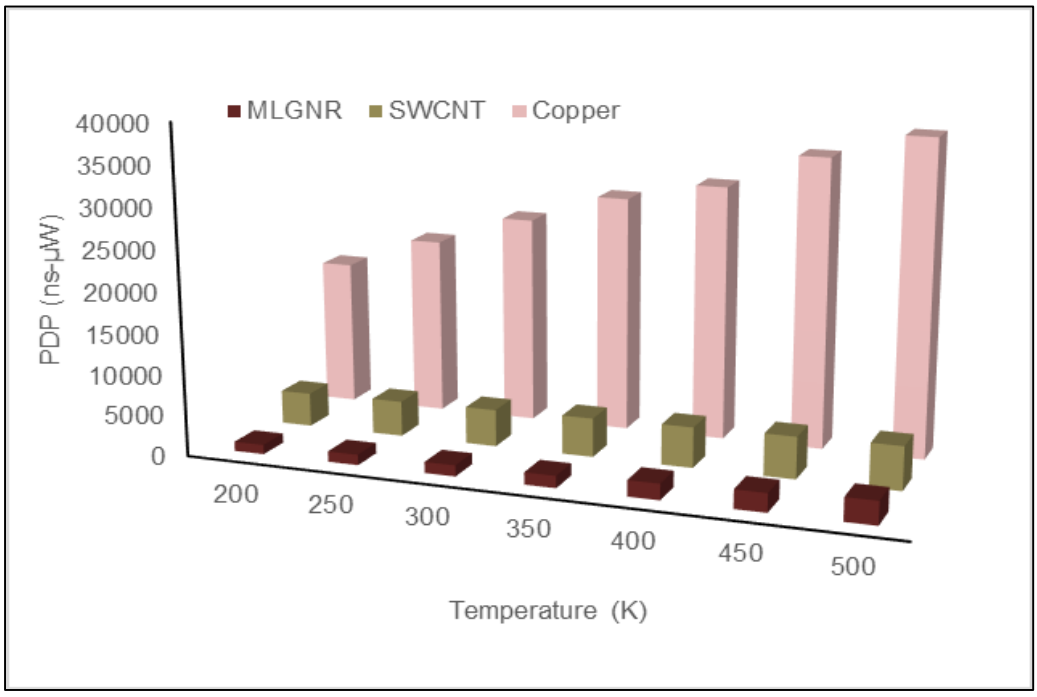
Temp. (K)	PDP (ns-µW)								
	32nm			22nm			16nm		
	MLGNR	SWCNT	Cu	MLGNR	SWCNT	Cu	MLGNR	SWCNT	Cu
200	840.831	3763.585	11599.049	1025.297	3982.568	13300.307	1145.587	4122.022	17791.442
250	869.438	3862.067	13393.774	1071.490	4101.795	15537.024	1279.245	4323.169	21661.319
300	918.971	4009.000	15163.207	1152.366	4379.522	17103.439	1353.441	4521.191	25327.089
350	1001.224	4231.694	16900.950	1287.003	4547.629	19625.534	1481.415	4750.554	28824.457
400	1123.954	4549.600	18607.591	1487.343	4727.462	21108.716	1967.283	4956.600	31079.596
450	1289.052	4970.227	20285.545	1753.205	4824.266	25557.284	2303.484	5145.941	35389.590
500	1479.330	5489.913	21936.456	1336.450	5229.527	17974.569	1534.056	5614.973	38485.124



(a)



(b)



(c)

Figure 6.11 Performance analysis and comparison of PDP of copper, SWCNT and MLGNR at 2000µm length for (a) 32nm, (b) 22nm, and (c) 16nm technological nodes

for the development of nanoelectronics (ICs) in thermally variable conditions. Table 6.5 represents the PDP of copper, SWCNT, and MLGNR interconnects and the outcomes are presented in Figures 6.9(a)–(c) graphically, for 32nm, 22nm, and 16nm nodes of technology,

respectively. This has been analyzed that comparing with copper and SWCNT interconnects for every technological node, MLGNR results are much better for PDP.

6.7 Chapter Summary

The combined effects of different levels of Fermi energies and variable temperatures on the performance of MLGNR in delay and PDP terms at 2000μm length for three various (16nm, 22nm, and 32nm) technological nodes has been examined in detail. SPICE simulation tool is used for simulating and estimating the performance of interconnects. The delay and PDP is directly proportional to temperatures (200–500 K), and inversely proportional to Fermi energies (0.6eV, 0.4eV, and 0.2eV) for three technological nodes of MLGNR. Both delay as well as PDP of MLGNR increases with rise in temperature but decreases with rise in Fermi energy. Impedance model dependent on temperature of copper is presented. The performance analysis dependent on temperature (200–500 K) of MLGNR from power dissipation, delay, and PDP parameters at global interconnect length (2000μm) is analyzed and compared with copper. The results reveals that the MLGNR has better performance than copper interconnect for all three various nodes of technology. Further, SWCNT impedance model dependent on temperature is presented. The performance and comparison analysis of MLGNR with copper and SWCNT interconnects at 2000μm length over 200–500K temperature in signal delay and PDP terms for three various nodes of technology is also evaluated. This has been investigated from the results of three different interconnects that the MLGNR with intercalation doping yielded a better performance from delay and PDP perspectives. Therefore, it can be concluded that the MLGNR is an outstanding material for the fabrication of next generation ICs in a thermally variable conditions.

Publication from this chapter

- Himanshu Sharma and Karmjit Singh Sandha, "Thermally Aware Modeling and Performance Analysis of MLGNR as On-Chip VLSI Interconnect Material," *Journal of Electronic Materials, Springer*, Volume 48, Issue 8, pp. 4902–4912, August 2019. (SCI indexed-Impact Factor-2.047)
- Himanshu Sharma and Karmjit Singh Sandha, "Investigation on the Combined Effects of Variable Fermi energies and Temperatures on the Performance of Multilayer Graphene Nanoribbon as Interconnects," *Analog Integrated Circuits and Signal Processing, Springer,* Volume 104, Issue 2, pp. 157–168, August 2020. (SCI indexed-Impact Factor- 1.321)

- Karmjit Singh Sandha and Himanshu Sharma, “Performance of MLGNR, SWCNT and Copper as Interconnects for Nanometer Technologies,” *International Journal of Engineering and Advanced Technology*, *Elsevie*r, Volume 8, Issue 5, pp. 2272–2276, June 2019. (SCOPUS indexed)

CHAPTER 7

CONCLUSION AND FUTURE SCOPE

The main outcomes and findings using the simulation and analytical work presented in the thesis are summarized in this chapter. The conclusion and scope for future work are presented in the subsequent sections.

7.1 Conclusion

The work reported in this thesis is based on the temperature and Fermi energy dependent performance analysis of MLGNR interconnects at global interconnect levels for 32nm, 22nm, and 16nm nodes of technology. First, a comprehensive literature study of the aluminum and copper interconnects was conducted. The limitations of the aluminum and copper interconnects are discussed in the introduction chapter, as technologies downscales to less than 45nm, their resistance increases sharply due to the small MFP and thereby reduces current density. Therefore, Carbon nanomaterials (GNR and CNT) are resulted to be better alternatives other than using copper as interconnect material at global lengths. CNT and GNR have similar properties but GNR is more suitable with respect to its fabrication process. Hence, GNR as possible interconnect material to replace copper is presented in this research work.

As per chirality, GNRs are of two types' ac-GNR as well as zz-GNR. Further, GNR are classified into SLGNR and MLGNR, with respect to number of layers. MLGNR is preferred over SLGNR due its smaller resistance. Initially, circuit model of a single layer graphene nanoribbon is proposed, which is used to develop the R-L-C multi-conductor model of the MLGNR interconnect. A Fermi energy-dependent circuit model is proposed for MLGNR interconnects. Analytical equations are presented to calculate the resistance, capacitance, and inductance of MLGNR for 32nm, 22nm, and 16nm nodes of technology. The effect of Fermi energy on parasitic parameters of MLGNR is discussed for three different nodes of technology at global levels. The delay and PDP of the MLGNR increases with an increase in the interconnect length but decreases with a rise in Fermi energy is analyzed. Furthermore, impact of temperature due to scattering mechanism on the proposed model of the MLGNR is discussed. The influence of temperature is presented, which is used to predict the parasitic parameters of the MLGNR interconnect. The temperature-dependent parasitic parameters are calculated for three different nodes of technology over 200–500K temperature range at global

interconnect level (500–2000μm).

The impedance parameters of the MLGNR interconnects for three different technological nodes are obtained analytically with the help of MATLAB computing software. The interconnect parameters are obtained from ITRS 2013 version. It is analyzed that with temperature rising levels (300–500K), a sharp decrease in MFP of GNR is noticed that dominates its resistance at global levels (500–2000μm) for all three nodes of technology. With rise in temperature, effective MFP plays a major role in controlling the MLGNR parasitic parameters that has direct impact on the power dissipation, delay and PDP as performance parameters.

The performance analysis of MLGNR interconnects dependent on Fermi energy and temperature from power, delay, and PDP parameters is conducted using a SPICE simulation tool for three different nodes of technology. For analyzing and calculating the interconnect performance from power, delay, and PDP, a lumped model has been used by dividing it into multi-stage RLC ladder network. Repeaters are inserted to separate the RLC ladder network. The simulation results are obtained using optimum size and optimum number of repeaters. The equivalent circuit model is driven by CMOS driver for all three various nodes of technology using PTM.

The Fermi energy-dependent MLGNR results are compared with copper interconnect with respect to the delay and PDP for equal lengths and technological nodes. Moreover, the MLGNR and copper interconnects are compared from delay and PDP ratio perspectives. The performance analysis (temperature dependent) of MLGNR in power dissipation, delay, and PDP terms was analyzed at global interconnect length for three various technological nodes. It is observed from the simulated results that with rising temperature (200–500K), power dissipation, delay, and PDP increases because of the shrinking of effective MFP at global interconnect levels for three various nodes of technology of MLGNR. The temperature-dependent analytical delay model of MLGNR interconnects is presented, and the corresponding results were compared to the simulation results. Results from simulation and analytical tests reveal that the outcomes of the two models correspond well. The trend of the models shows that the delay increases with the rise in temperature (200–500K) for 32nm, 22nm, and 16nm nodes of technology. Relative stability of MLGNR is also analyzed from 500–2000μm length w.r.t. switching delay and observed that with increasing interconnect length switching delay increases as a result input signal damp faster which upswings the relative stability of MLGNR for all three various technological nodes. Likewise, relative stability is analyzed at length 2000μm and temperature 500K of MLGNR through Nyquist plots and

observed that the system will achieve stability faster as we move from 32nm to 16nm technological node due to higher values of parasitic because of the reduction in MFP of electrons.

The combined impact of temperature and Fermi energy on MLGNR is investigated and estimated that with an increase in temperature (200–500K), the delay, and PDP increases. However, they decrease gradually with an increase in the levels of Fermi energies (0.2eV, 0.4eV, and 0.6eV) for three different nodes of technology. Therefore, variations in Fermi energy and temperature have considerable impact on performance of MLGNR interconnects at global level. The performance and comparative analysis of MLGNR with copper and SWCNT interconnects using delay and PDP as performance parameters is conducted for equal length and technological nodes. The results show that performance of the MLGNR interconnects is much superior than those of copper and SWCNT interconnects considering the impact of different levels of Fermi energies and temperature at global level interconnects for 32nm, 22nm, and 16nm nodes of technology.

In conclusion, MLGNR is a suitable alternative than copper and SWCNT interconnects at global levels for high speed ICs. The effect of Fermi energy enhances performance of MLGNR interconnect. Moreover, the impact of the temperature should be incorporated to evaluate the performance of MLGNR in a thermally variable environment.

7.2 Scope for Future Work

In this study, the limitations of the copper and SWCNT interconnects have been addressed efficiently and the MLGNR interconnects are proposed as future interconnects. To estimate the effect of Fermi-Energy on the conductivity of MLGNR interconnects, a Fermi energy-dependent circuit model is proposed, and the performance of MLGNR is analyzed at global interconnect levels for 32nm, 22nm, and 16nm nodes of technology. Further, the impact of temperature on MLGNR performance at global length for three various nodes of technology is analyzed. Furthermore, a combined effect of the temperature and Fermi energy on performance of MLGNR was discussed. A comparative analysis with the SWCNT and copper interconnects is performed. It is concluded that MLGNR exhibits better performance than that of the copper and SWCNT at global interconnect lengths for different technological nodes (16nm, 22nm, and 32nm). The performance of the VLSI design could be enhanced by exploring other fields of the proposed area. Henceforth, the following are the ideas that can be explored in future:

- The impact of intercalation doping other than material arsenic pentafluoride required to be analyzed and compared in order to enhance the conductivity of MLGNR.
- The impact of the RF frequencies on the performance of the MLGNR should be reconnoitered at global interconnect lengths.
- The delay of MLGNR dependent on temperature at global interconnect lengths for different types of repeater insertion should be analyzed.
- In deep submicron nodes, the interconnects density increase causes more coupling between neighboring wires. Thus, the temperature-dependent crosstalk for the MLGNR interconnects should be analyzed for nano-scaled technology nodes at global interconnect lengths.

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LIST OF PUBLICATIONS

Published/Accepted Papers in Journals

1. **Himanshu Sharma** and Karmjit Singh Sandha, "Thermally Aware Modeling and Performance Analysis of MLGNR as On-Chip VLSI Interconnect Material," *Journal of Electronic Materials, Springer*, Volume 48, Issue 8, pp. 4902–4912, August 2019. **(SCI indexed-Impact Factor-2.047).**

2. **Himanshu Sharma** and Karmjit Singh Sandha, "Investigation on the Combined effects of variable Fermi energies and Temperatures on the Performance of Multilayer Graphene Nanoribbon as Interconnects," *Analog Integrated Circuits and Signal Processing, Springer,* Volume 104, Issue 2, pp. 157–168, August 2020. **(SCI indexed-Impact Factor- 1.321).**

3. **Himanshu Sharma** and Karmjit Singh Sandha, "Impact of Intercalation Doping on the Conductivity of Multi-layer Graphene Nanoribbon in On-Chip Interconnects," *Journal of Circuits, Systems and Computers, World Scientific,* Volume 29, Issue 12, pp. 2050185-1–2050185-22, September 2020. **(SCIE indexed-Impact Factor- 1.278).**

4. **Himanshu Sharma** and Karmjit Singh Sandha, "Analytical Delay Model and Stability Analysis for MLGNR Interconnects," *Journal of Circuits, Systems and Computers, World Scientific,* Volume 31, Issue 15, pp. 2050260-1–2050260-23, October 2022. **(SCIE indexed-Impact Factor- 1.278).**

5. **Himanshu Sharma** and Karmjit Singh Sandha, "Multilayer Graphene Nanoribbon (MLGNR) as VLSI Interconnect at Nano-scaled Technology Nodes," *Transactions on Electrical and Electronics Materials, Springer*, Volume 19, Issue 6, pp. 456–461, December 2018. **(SCOPUS indexed).**
6. Karmjit Singh Sandha and **Himanshu Sharma**, "Performance of MLGNR, SWCNT and Copper as Interconnects for Nanometer Technologies," *International Journal of Engineering and Advanced Technology, Elsevie*r, Volume 8, Issue 5, pp. 2272–2276, June 2019. **(SCOPUS indexed).**