Tackling EM effects during Layout Development in Custom Compiler

A Thesis submitted in partial fulfillment of the requirement for the Award of the Degree of

MASTER OF TECHNOLOGY

In

VLSI Design

Submitted By

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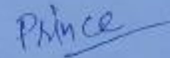
JULY, 2019

DECLARATION

I, **Prince Moudgil** hereby declare that the work presented in this thesis entitled "**TACKLING EM EFFECTS DURING LAYOUT DEVELOPMENT IN CUSTOM COMPILER**" in partial fulfillment of the requirement for the award of degree of **Master of Technology (VLSI Design)** submitted at **Electronics And Communication Engineering Department**, Thapar Institute of Engineering & Technology (Deemed to be University), Patiala is an authentic record of work carried out under supervision of **Dr. Harpreet Vohra (Assistant Professor, ECED, TIET)** and **Atul Bhargava/External Supervisor (Manager, ARCAD, STMicroelectronics)** from **June 2018** to **May 2019**. The matter presented in this has not been submitted either in part or full to any other university or institute for the award of any other degree.



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CERTIFICATE

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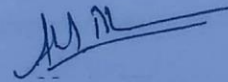

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ABSTRACT

Fixing electro migration (EM) violations towards end of the design cycle always poses a high risk to delivery schedules. Hence a mechanism is required to check and fix EM during the layout design phase. This paper addresses this challenge in two parts. In the first part, we describe how we have incorporated Custom Compiler's In-Design EM Reporter Tool in our design phase and quantify the reduction in the number of EM violations seen during Sign-off and how this contributes to faster turn-around.

In the second part, we describe the on-going collaboration with Synopsys to route the design with EM awareness. This is targeted for nets which are auto-routed, primarily power nets and signal nets that take a regular pattern. This involves automatic invocation of EM Reporter tool in the background and assignment of required widths to the automatic routing engine, thus resulting in EM clean routes by construction.

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LIST OF ABBREVIATIONS

BEOL-Back-End-of-Line

IP -Intellectual Property

EM -electromigration

Cu -Copper

TDDB -time-dependent dielectric breakdown

HCID - hot carrier induced damage (HCID)

NBTI - negative bias temperature instability

NMOS - N-type metal oxide semiconductor

PMOS - P-type metal oxide semiconductor

GCLK -Gated clock

CHAPTER 1

INTRODUCTION

Over the past few decades, semiconductor devices have continuously been scaled down in size for higher device density and performance and as the need for high speed, low power designs increase Back-End-of-Line (BEOL) interconnects encounter many challenges as it results in high electromigration (EM) currents for design due to the very small dimensions of interconnecting wires and the invention of the new materials which have weaker material properties [1]. As a result, with the passage of time, it becomes a more and more difficult task to ensure the reliability of BEOL interconnects.

Two types of reliability issues are there mainly in the VLSI industry.

- Defect-related problems.
- Wear-out.

Defect-related problems are caused due to manufacturing defects, such as a missing process step, dirt, or other unavoidable reasons. Even today, after 60 years of continuous growth of Semi-conductor industry the most advance process lines suffer from an occasional defect-related problem.

On the other hand, wear-out is a mechanism which happens due to limitations in the "perfect" material, is a problem that is a lot of concern with the designer. One of the principal wear-out failure mechanisms is electromigration.

Electromigration (EM) is one of the major reliability failure mechanisms of BEOL interconnects in the advanced technology nodes of semiconductor devices. Because of the high current density demands to meet the increasing functionality and complexity leads to continuous scaling down of Copper wire dimensions. Detection of electromigration issues at the very initial stage of circuit design is important for reliability purpose and with-in time limit delivery of IP [2]. The violations related to maximum current density limits in circuit layouts are corrected by the layout modifications and the widening of wires. Widening of wires is one of the effective ways to fix these violations.

EM is the major bottleneck as it determines the lifetime of macros such as Memory and IO over a period of time and the temperature at which it is operating. EM is taken care of accounting different mission profiles at the same time decreasing product validation time. To increase product cycle time, there is a need to improve our product development time and product validation time.

In the present work, Chapters 2, 3 and 4 describes the use of EM reporter and CustomSim-RA tool to calculate average current so that any critical net or power signal metal width is taken care at block level development only. Chapter 5 describes the EM aware auto-router to route all power and signal nets

automatically that are EM compliant to the design specifications.

1.1 THE PROCESS OF ELECTROMIGRATION :

Material migration or electromigration is a general term for various forced material transport processes in solid bodies. These include

- Chemical diffusion due to concentration gradients,
- Material migration caused by temperature gradients,
- Material migration caused by mechanical stress, and
- Material migration caused by an electrical field. This last case is often referred to as electromigration.

Electromigration is the process of transport of material in conductors under the influence of an applied electric field.

Transport of material happens due to the momentum transfer from collisions between conducting electrons and diffusing metal atoms.

When an electric field is applied across a wire electrons move along the metal wire. These electrons tend to scatter. Scattering of these electron takes place at imperfections within the lattice: vacancies, impurities, grain boundaries, dislocations and even phonon vibrations of the metal ions from their ideal positions [3].

Several types of diffusion mechanisms are possible in metal lines

- Bulk diffusion
    - Large Cross-sectional area
    - High Activation energy. Can be neglected under typical low T conditions of test and service.

- Grain boundary diffusion
    - Regions of disorders between disoriented crystals.
    - The principal mechanism in Al
- Dislocation diffusion
    - Activation energy is similar to Grain Boundary and Surface diffusion.
    - Cross-sectional area small → negligible contribution
- Surface/interface diffusion
    - Interfaces between Metals and Dielectrics in Significant disorder
    - Quality of interfaces very sensitive to fabrication variations.
    - The primary mechanism in Cu.

Electromigration is a very slow process and taking time process.

One of many factors Determines IP lifetime

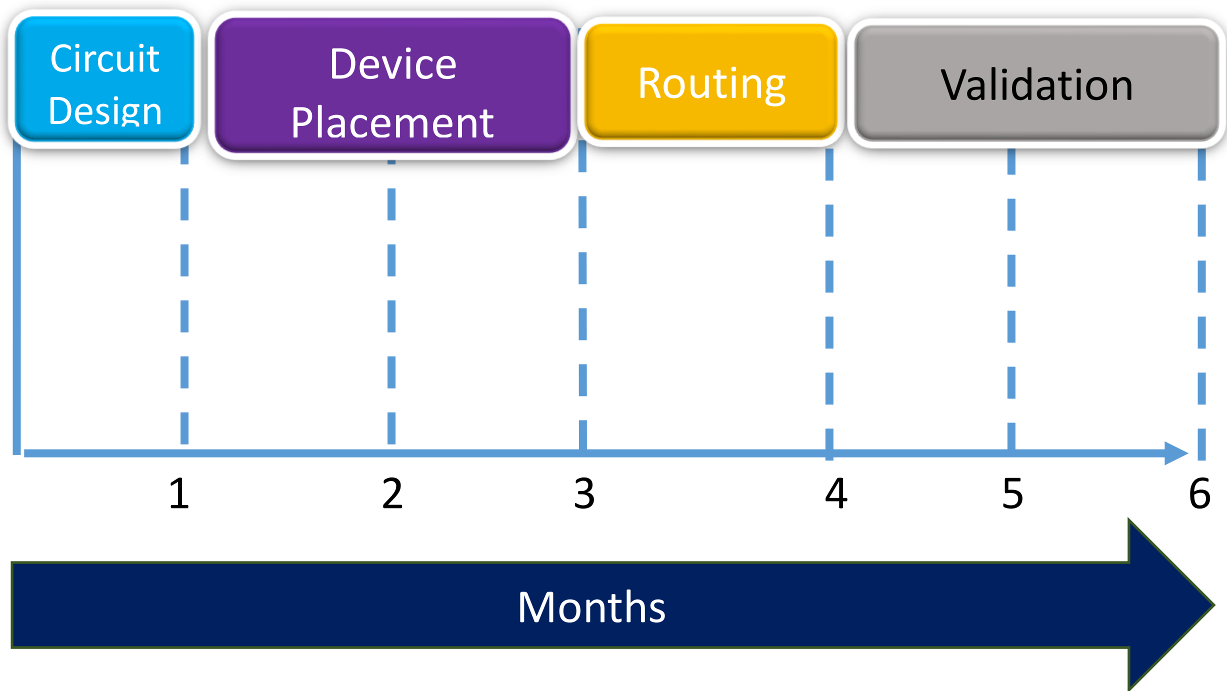


Figure 1.1 IP Development Cycle

Figure 1.1 shows important phases in the development of a general IP which are Circuit Designing Phase which took 1 to 1.5 months, Device Placement and Floor-planning which is estimated to take again 1 to 1.5 month.

Mostly Routing is done by PnR (Place and Route) tools but layout designer efforts are also required for critical nets such as power nets and finally comes the validation phase which took about two to two and half months.

EM specs for any IP are based on max:

- **Operating Voltage**
  - Operating voltage is the maximum voltage at which IP is designed to perform its functioning.
- **Operating frequency**
  - The frequency at which IP is designed to perform its proper functioning during its life cycle is called an operating frequency
- **Operating temperature**

- Operating temperature is the temperature at which IP is designed to perform its proper functioning during its life cycle [4].

In industry, the sole focus is to optimize IP Development to market reach time. And EM is a major issue which is encountered during the end of IP development cycle.

From the Figure 1.1, it is concluded that to optimize IP Development cycle then most efforts must be directed in direction of reducing the validation time.EM is one of the major bottlenecks that determines the lifetime of IP's. EM is taken care of by accounting for parameters such as Operating Voltage.

From Figure 1.1 Validation phase for IP takes about 33% ($1/3^{rd}$) of the project development time. EM violation at this stage can increase validation time and even lead to going back to designing phase

EM is the major bottleneck that determines the lifetime of IP's. The present work focus on examples of memories and IOs. EM is taken care of by accounting different mission profiles such as Operating Voltage, Period of operation and temperature at the same time decreasing product validation time. So the best way to optimize IP development cycle is by reducing the product validation time.

1.2 DAMAGE CAUSED BY EM

If the current direction is kept constant for a long-time period in metal wire, voids and hillocks appear in the metal wire. Because of this analog circuits and power supply lines in digital circuits are more prone to electromigration [5]. Suppose, if the current direction is varied, as in digital circuits with their alternating capacitive charging and discharging in conductors, there is less possibility for electromigration effects in digital circuits but still the interconnects failure possibility is there.

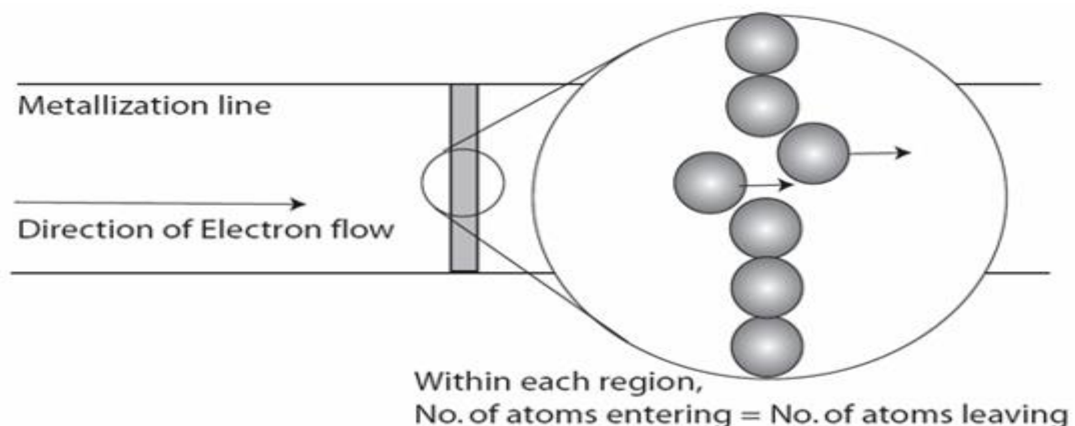


Figure 1.2 Displacement of metal ions in the direction of electron flow.

Source of image:https://www.doitpoms.ac.uk/tlplib/electromigration/damage.php

Uniform electromigration (current is flowing in both directions) within the metal lines, if it could be maintained, would not be very much damaging. This is because of the fact that along the metal line the number of atoms leaving is equal to the number of atoms arriving in a specific volume.

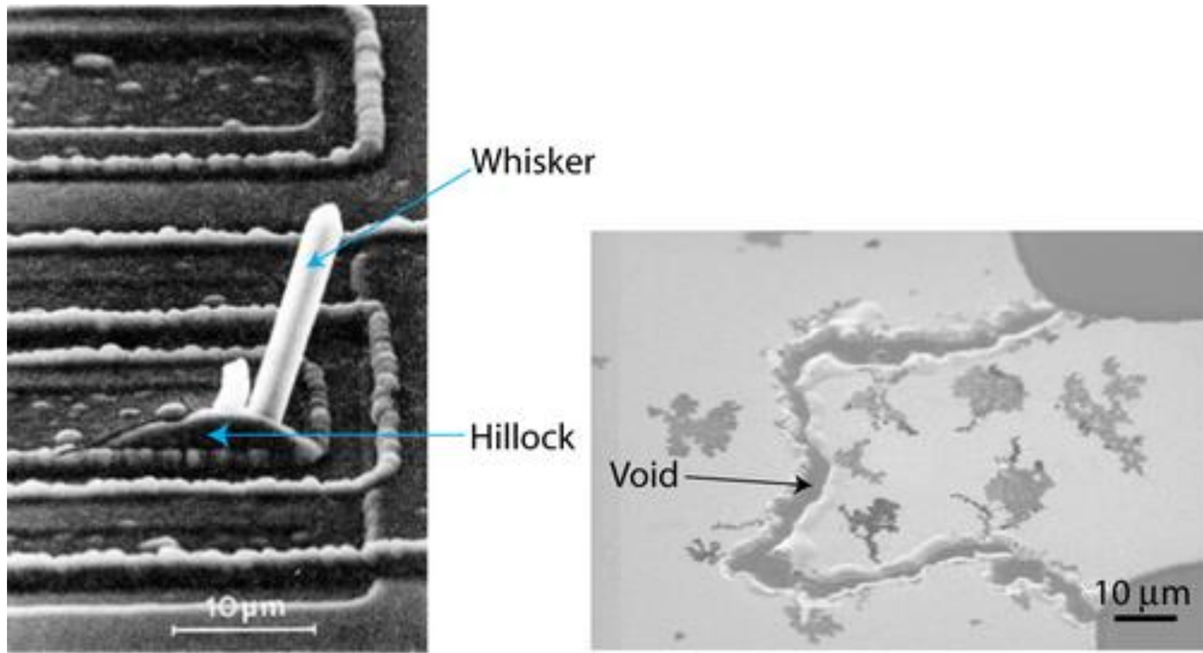


Figure 1.3 Picture showing Whisker and voids created due to electromigration

Source of images: (left) Microelectronic Materials by CRM Grovenor, IOP Publishing Ltd, Bristol (UK); (right) Dr. Lo Veng Cheong

When the amounts of matter in metal line leaving is unequal to matter entering in a specific volume, the associated accumulation or loss of material results in damage. When atomic flux into a region is greater than the flux leaving it, the matter accumulates in the form of a hillock or a whisker. If more flux is leaving the region than the flux entering, the depletion of matter ultimately leads to avoid. These regions are called flux divergences.

CHAPTER 2

LITERATURE SURVEY

With advancement in technology and usage of new materials for the fabrication process of IC's technology node are shrinking with passing time, now VLSI industry is exploring the possibilities for 10nm, 7nm and 5nm nodes in IP designs, electromigration effects need to be considered during block-level design and should be considered as an integral part of the design flow.

In early days layout designers clean EM towards the end of the complete IP design. But in today's era if layout designer will not consider the electromigration effects at the early stage of IC design this will have a serious impact on the productivity and delivery schedules. To clean EM violations after complete designing cycle will increase the cost of IP for the manufacturers and time to market. Present work describes how layout designer can run EM on per-net basis during the design phase and end up with very few EM violations during Sign-off validation.

James R. Black et al. [6] describes electro migration factors which give the brief idea of the rate of electromigration and also about the lifetime of conductors stressed at high current density. This tell about the type of metal conductor, the conductor cross-sectional area, lattice, grain boundary and surface diffusion effects, the addition of alloying elements, temperature, and current density as well as the thermal conductivity of the substrate. The effect of gradients with respect to temperature, current density, conductor composition and grain size on conductor lifetime is also discussed.

Mircea R Stan et al. [7] The most common wear-out phenomena that impact reliability are metal electromigration (EM), time-dependent dielectric breakdown (TDDB), hot carrier induced damage (HCID), negative bias temperature instability (NBTI) and thermal cycling. This paper focuses on electromigration and proposes two novel solutions. The first is the use of routing (or slotted) vias for improving electromigration performance for dual damascene copper interconnect without increasing the lateral dimensions of the wires. The second is the use of electromigration liquor liability sensors rdquo in order to detect the impending failure of interconnect. The proposed solutions show good results in simulations and measurements of test structures.

Ye, Wei, et al. [8] suggested an EM signal handling structure which includes identification of EM hotspots and fixing methods into the previous phase of physical layout procedure integrated with machine-learning-based method together with multistage mitigation. In this proposed method extracted features are used from the placement. To detect EM hotspots a classification model from the machine learning model is utilized In order to mitigate the identified EM hotspots, an incremental placement scheme is suggested. Compared to the state-of-the-art EDA instrument, the writer achieves 15× speed while attaining a comparable EM mitigation and overhead results.

Lienig, Jens et al. [9] described fundamental design challenges during interconnect design and their impacts on electromigration. By implementing electromigration-inhibiting procedures, like reservoir properties and short length, current density limits are raised. In the future, the use of these impacts in the design phase will partially solve EM issues in IC design flows. The author recommends a method which utilizes the geometry of the particular circuit and applicable current density limits for the application's task profile. The EM robustness of the produced design can be substantially improved by employing EM-optimized layout settings as limitations in synthesis measures as routing. This integration into the physical layout of EM-specific demands can alleviate serious reliability limitations in future systems.

Wachnik et al. [10] in 2000 presented a simple model which was able to relate accurately the resistance saturation during electro-migration to the length of the stripe and current density. The authors state that between the temperature ranges of 170 ^{0}C to 125 ^{0}C, resistance saturation shows no dependency on temperature. The authors making use of this observation were able to propose the design of a power grid

which was resistant to the effect of electro-migration after the development of a novel design rule methodology. The authors in their work state that below a specific length termed as critical length the electro-migration led mass transport at a given current density in the presence of a diffusion barrier is limited. This limit which opposes the driving force of electro-migration arises from a stress gradient. When multilevel layers with redundant refractory layers are taken under observation, electro-migration here causes a void to nucleate and grow at the cathode end of the line. At the lines, anode end conductor's atoms accumulation takes place causing the stress gradient which limits the growth of the void. This, in turn, puts a limit on the resistance increase of the metal structure. Further suppression of electro-migration induced damage is indicated by the saturation of resistance increase with time. The authors test the stated proposal on two-level metal structure made of Al and Cu stripes with Ti serving as the redundant layers sandwiched between the previously mentioned two metal stripes at various current densities and at varying temperatures. The authors concluded by discovering a class of meshes which had a systematic introduction of gaps in the common grid layout which allowed the construction of power distribution grids for IC's. Also, the authors state that the work presented allows a reduction in electro-migration but it also causes the net's point to point resistance increase and imposes a restriction on the placement of power pin.

Lin et al. [11] in 2009 performed an upstream EM study on various via structures and multiple copper line dimensions. EM performance showed a dependency on both the Cu line dimension and also the via layout. The authors investigated the upstream electro-migration performance of multiple via structures using copper line dimensions for the evaluation of electro-migration. The driving force of electro-migration as stated by the authors is electric current. Along with current being the EM driver, multiple via structures have complex geometries, therefore to analyze the upstream electro-migration performance all current density profiles were found out followed by the observation of their variation on the structures. Differentiation of the grain morphologies with the void modes induced due to electro-migration was performed on which failure analysis was done. The study was done on samples which were fabricated in 65nm technology (low K dielectric). It was observed that with an increase in the number of multiple via structure via's in wider and thick dimensions led to a higher chance or a greater probability of degradation due to electro-migration. This is attributed to the fact that additional diffusion paths of the additional grain boundaries would be introduced by enlargement of interconnecting geometry. On the other hand electro-migration performance for multi via structure in narrow dimensions attributed to the reservoir effect or the low current density.

Morusupalli et al. [12] in 2007 made an attempt to establish a relationship and hence observe the effect of current density on line stress. According to the authors along with performance, reliability holds the same level of importance. Any product in the microelectronic industry is expected to have a product lifetime of 10 to 15 years. The authors state that in interconnects which possess blocking boundaries electro-migration leads to depletion of atoms on the cathode end while accumulating them on the anode end of the line. With

the diffusion of atoms void formation at the cathode takes place with no source of atoms for filling the vacancy. The authors work at developing a tool aiming at electro-migration induced stress simulation in the interconnects by building a model based on the same. The proposed model provides a solution for the equations which govern stress evolution and atomic diffusion. The authors include in their simulations line geometry effects, properties of materials, overhangs and electro-migration stress conditions. The tool developed was tested on interconnects of copper (pure Cu) and the comparison of the line stress predictions was done with measured electro-migration failure times. Simulations were performed using the developed numerical schemes involving stress calculations.

Bigalke et al. [13] proposed a (pro-active) EM-aware design - where the circuit layout is designed for individual EM-robust solutions. The authors have proposed a physical EM process and present its specific characteristics that can be affected during physical design. Improvement of EM-robustness of metallization patterns are shown and application-oriented current-density limits are obtained. The increasing interaction of EM with thermal migration is investigated as well. Its methodologies, such as EM-aware routing, increase the EM-robustness of the layout with the overall goal of reducing the negative impact of EM on the circuit's reliability. EM-aware routing methodologies include net topologies (Ex. RSMT), creation of reservoirs, length limitations, cross-section widening, redundant vias, changing via-above and via below configurations along with upper and lower lead.

Bigalke et al. [14] performed most of the analysis steps within the placement and routing tools to consider the results; thus enabling early and specialized EM-robust solutions. Particularly, their methodology exploits layout structures to enable an efficient discretization inside the geometrical representations of synthesis tools. The authors have demonstrated, how to reduce the discretization effort significantly while achieving sufficient accuracy to improve EM robustness. This paper proposed a new method for an EM analysis based on algorithms to discretize placement and routing solutions within EDA tools achieving a comparable result quality to a FEM simulation while significantly reducing the problem complexity. It also proposed procedures on how to consider these EM results within the placement and routing algorithms in order to synthesize EM-robust layouts.

Bigalke et al. [15] prioritize reliability constraints, such as EM-induced stress reduction during net topology generation. The authors optimized rectilinear Steiner tree for currents and mechanical stress. The results imply a mechanical stress reduction in most cases of more than 50%, thereby significantly abating EM vulnerability. In addition, the authors show that reservoirs can further reduce the absolute mechanical stress level, and present an equation for directly calculating the optimal reservoir length. It also showed that reservoirs can further lower EM-induced stress. To utilize this factor, the authors provide an equation for calculating the optimal reservoir length.

2.1 OBJECTIVE OF THESIS:

Previously, it was difficult to find out the electromigration (EM), reliability of advanced interconnects. For today's shrinking nodes reliability is critical to product lifetime. The metal interconnects are subjected to high current densities and mechanical stress. This work done describes how to incorporate Custom Compiler's In-Design EM Reporter Tool in the design phase and quantify the reduction in the number of EM violations of latest generation shrinking nodes (28nm, 18nm, 14nm) seen during Sign-off and how this contributes to faster turn-around and the development of a flow with Synopsys utilizing Custom Compiler's In-Design EM Reporter Tool in the design phase and quantify the reduction in the number of EM violations of latest generation shrinking nodes.

CHAPTER 3

EM CRITICAL PORTIONS IN MEMORY IP

A typical SRAM memory cell is shown in Figure 3.1 consists of the bit-cell array, IO, a control row decoder, dummy column, dummy row, Dummy Word-line (DWL).

Dummy Bit-line Read (DBLR), Common NMOS. So the major bottleneck block which is more prone to EM is dummy row, dummy column, and control as there is multiple signal and power nets which have a high probability to trigger in each clock cycle given to the memory.

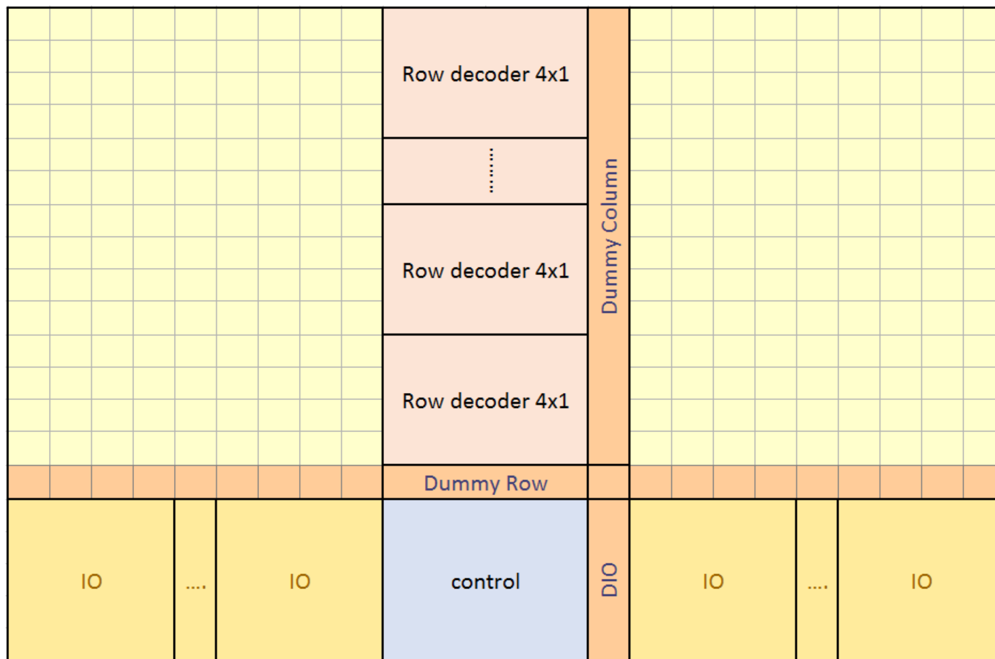


Figure 3.1 Typical block diagram for SRAM memory

Figure 3.1 is an example of a typical memory block which consists of Memory bit cell array (for storing memory content). Each bit cell store 1 bit of data.IO (for reading / writing data from memory array).

Row decoder (to provide a word-line signal to memory array for starting read/write operation)

Control (to provide basic clock and decoded signals for IO and row decoder)

- Dummy column and dummy Row decoder (for deciding the memory cycle operation)

Now out of this, the block with the high current requirement is IO which provides write driver signal to array and Q driver which provides read data, Dummy Row decoder, Dummy column and local clock signals in the control.

3.1 EM PRONE STRUCTURES IN MEMORY – DUMMY WORD LINE

3.1.1 Dummy Word-line Current Flow (current within PMOS and NMOS on condition)

Figure 3.2 shows the dummy word line signal. In this structure, there is a unidirectional current flow between PMOS and NMOS which creates EM stress making this net EM prone.

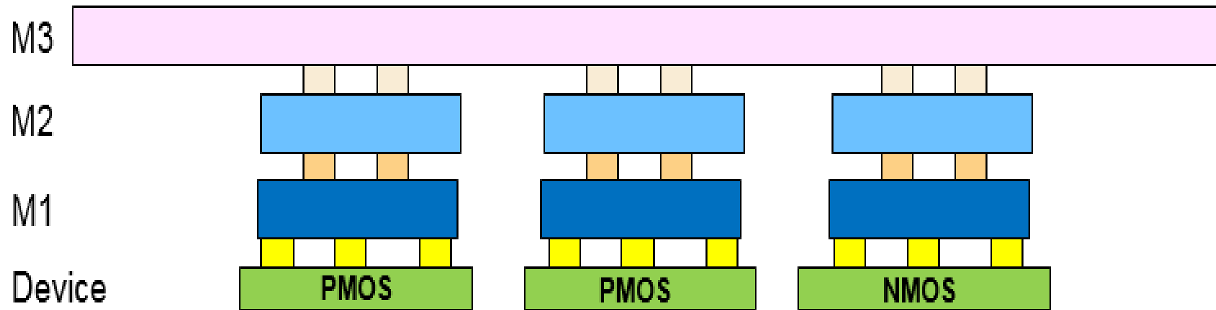


Figure 3.2 Structural configuration of various metal layers in the dummy word line

Various methodologies are deployed to design/layout EM prone nets to meet EM specs.

The first example is of Dummy word line signal which is generated in the dummy row decoder block. This block is final driver and the metal routing above it. In this structure, there is a unidirectional current flow between PMOS and NMOS which creates EM stress making this net EM prone. The current direction is shown in the Figure 3.3.

3.1.2 During word-line rise PMOS on

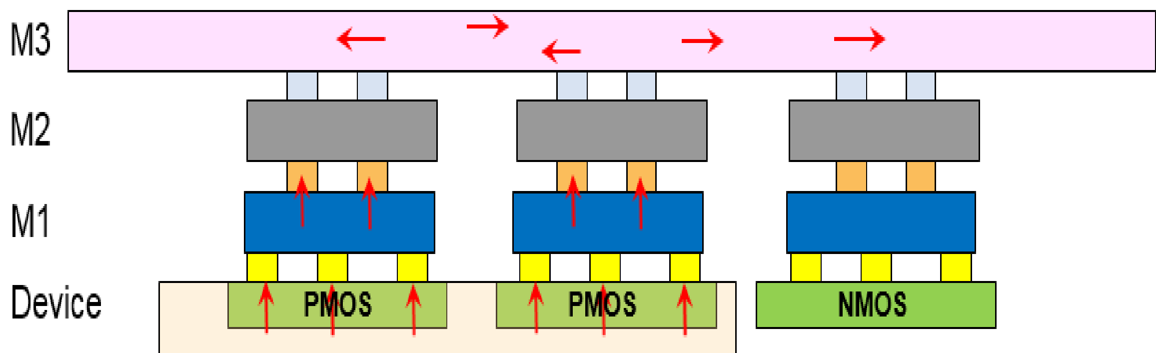


Figure 3.3 Picture show that during word-line rise PMOS on

Figure 3.3 shows the current directions will be like: when PMOS is ON the current moves from VDD in both directions on the left side above PMOS and right side above the NMOS. When NMOS is ON in Figure 3.4 the current is sinking to GND only in the right direction.

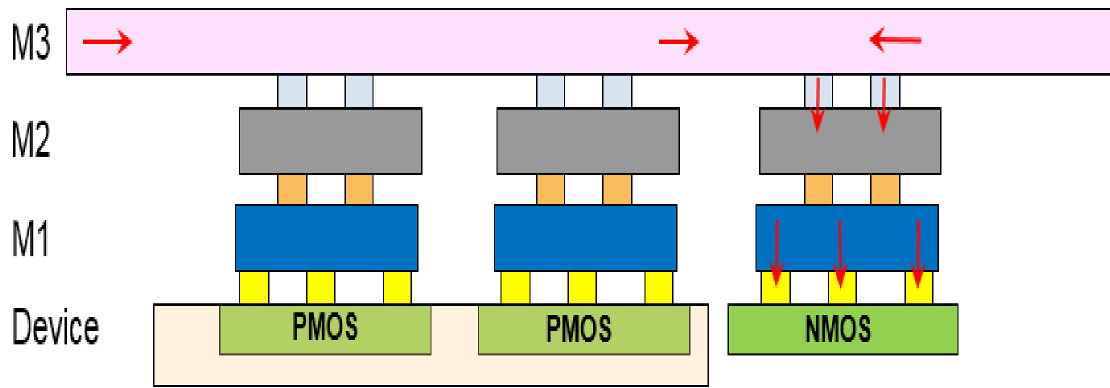


Figure 3.4 Picture shows that during word-line rise NMOS on

Figure 3.4 shows current direction arrows, the current in M3 is mostly unidirectional in the stretch between PMOS and NMOS. So due to that, there will be a need to be taken care of EM stress.

So the solution to avoid this EM stress would be to utilize the blech effect, by adding M3 to M2 jumper to reduce the EM length below blech length.

As shown in Figure 3.5 and Figure 3.6 there is a lower limit for the length of the interconnect that will allow higher current carrying capability. It is known as "Blech length". Any wire that has a length below this limit will have a stretched limit for electromigration.

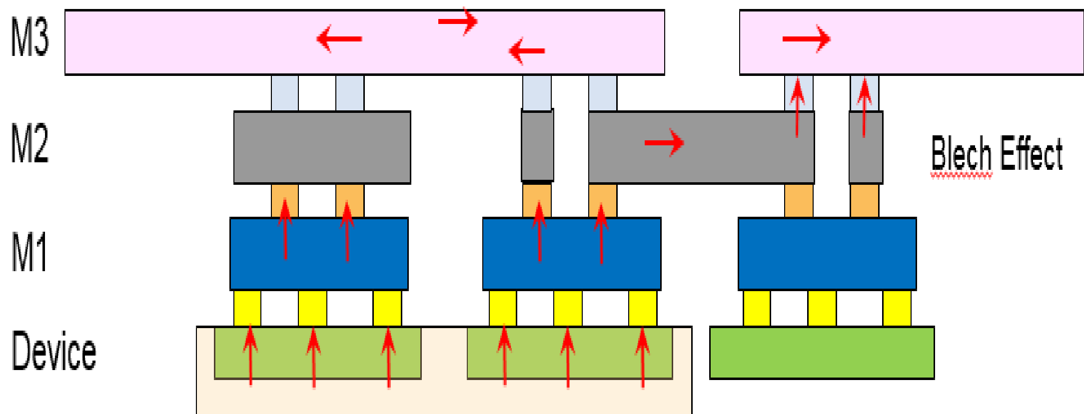


Figure 3.5 This picture shows that during word-line rise PMOS on

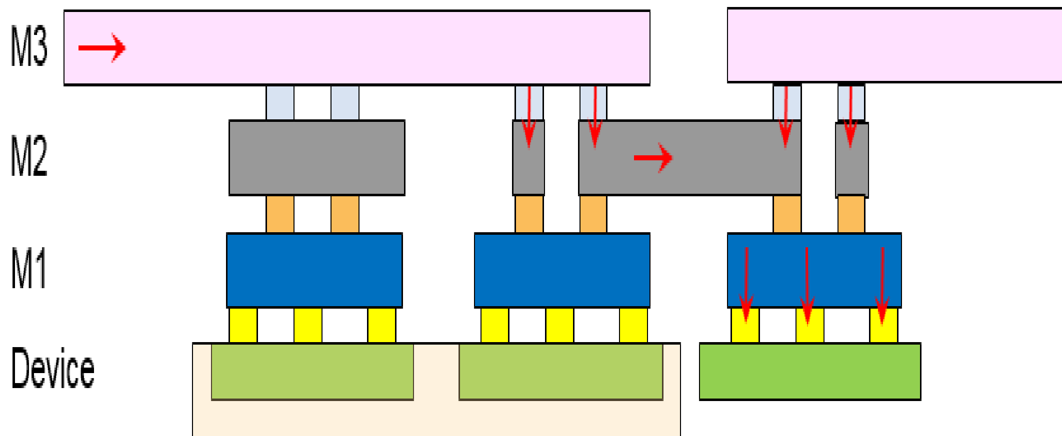


Figure 3.6 Picture shows that during word-line rise NMOS on

In 2nd example, Common NMOS is taken (Pre-Decoder, GCLK)

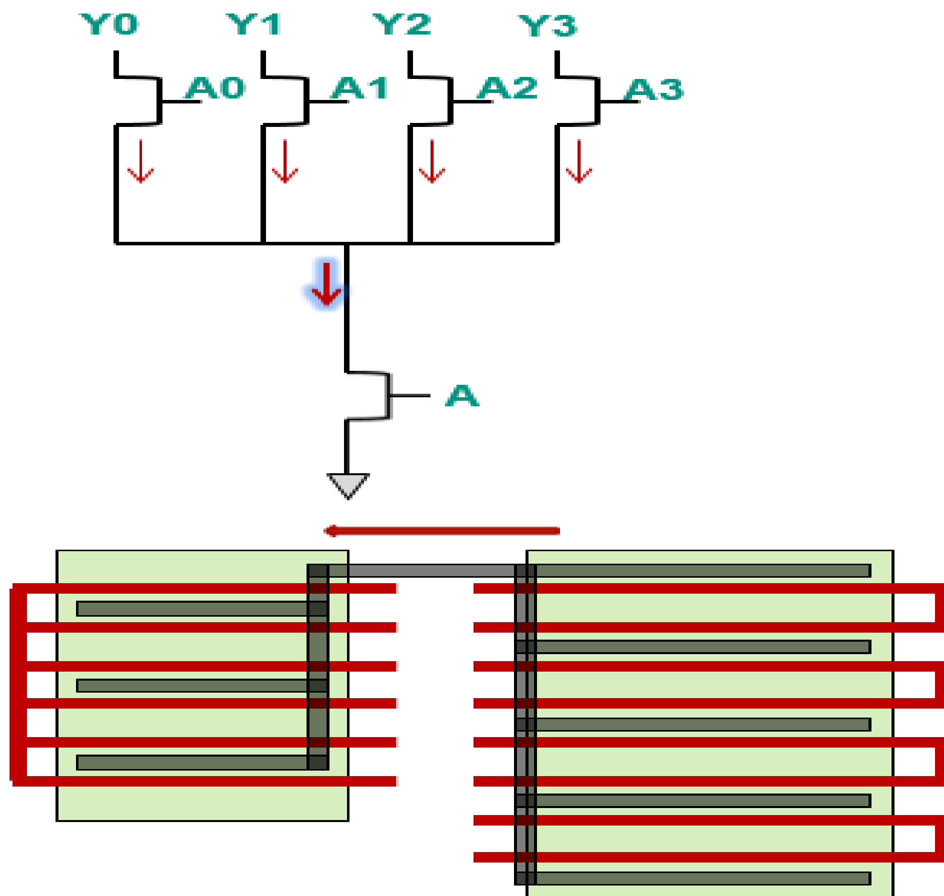


Figure 3.7 Common NMOS (Pre-Decoder, GCLK, etc.)

This is another example shown in Figure 3.7 with common NMOS structure which is used in control very often. Five input signals -A<0:1:2:3> are there in this example. In the 1 clock cycle, only 1 goes high. EM limits get relaxed due to probability. But this is not the case for the net –A. This signal goes high in every clock cycle. No relaxed limits as current passing in every clock cycle

In this structure, the Signals A <0:3> have ¼ probability for each to go high so each NMOS got relaxed. However, the signal A has a probability of 1 to be on, hence this net is critical from EM perspective. Here the current directions are shown, where the current from each above NMOS goes once in 4 cycles whereas the current from the below NMOS is always flowing so there will always be unidirectional flow of current through below NMOS.

3.1.3 Typical Layout Changes for cleaning EM

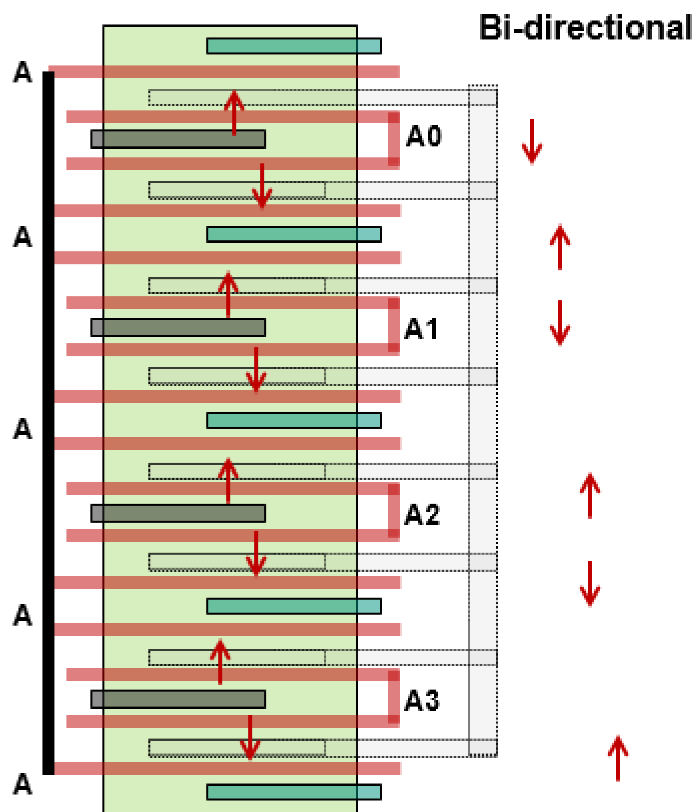


Figure 3.8 A typical layout changes to be done to clean EM

Solution for this case would be to re-layout this structure with something like shown here by breaking the common NMOS such that two of the NMOS are placed on both sides of A <0:3> making the current bidirectional hence reducing EM stress. Here the current direction as shown in Figure 3.8 is now converted from unidirectional to bi-direction thus by reducing the EM stress. Break common NMOS into 8 equal

NMOS as shown in Figure 3.9

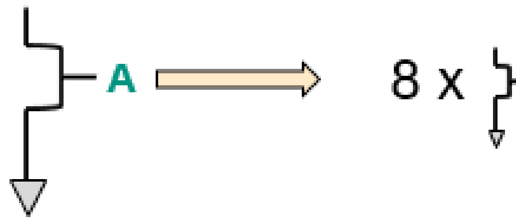


Figure 3.9 An NMOS breaks to 8 equal NMOS

Place two of this NMOS on both sides of A0, A1, A2, A3. (as shown in Figure 3.9)

This placement results in Bidirectional flow of current in most of the portion of the metal.

Final driver and metal routing above final driver. Most of the cases stacked via approach is used for metal routing to save EM problems

EM critical nets

- Nets which drive the huge load, such as the output of global drivers and address buffers, etc.
- A device whose toggling frequency is high. Example: DWL which toggles in every clock

For a particular signal or power net, EM is defined how quickly and at what probability current is triggering through it. For example, take a signal net such as dummy bit line read which is present in the dummy column block shown in the block diagram in Figure 1. This signal is used for tracking the read period to read the contents of memory and after that generating the reset signal so that memory is reset to ideal state and the bit line is pre-charged to full state Vdd after the read operation is completed. So during every read operation, dummy bit line read is discharged and pre-charged for every clock cycle at which memory is operating. Therefore, it can be said that this signal has a 50% probability to change in every clock cycle so it is very prone to EM effects.

As it is clear from the above explanation that dummy bit line read signal is very critical in dummy column, so it can be designed during layout development by taking care of all the specifications like frequency of operation, supply voltage, probability, etc. Therefore, there is a need for block-level during layout development so that the metal width or any blech effect can be defined.

Memory is typically 60% of the block area of a general IP. Memory leaf cells are with large current requirements as they are containing the below-listed components blocks.

- Write driver
- Q- output driver
- Dummy Row decoder driver
- A dummy bit line (dummy column)

- Clock drivers
- Local clock in the control
- Horizontal and vertical clocks for IO and Row-decoder

The block with the high current requirement is IO, Dummy Row-decoder, Dummy bit-line and local clock signals in the control.

Similarly, their critical signal in dummy IO and control as well because signal there also have a very high probability to trigger so are more concern to EM effects. Generally following are the nets which are trickier and more prone to EM effects:

- Dummy Word Line (DWL)
- Dummy Bit-line Read (DBLR)
- Common NMOS
- Vddma power net in Row decoder.

So there is a need to tackle EM effect during block-level layout development so that during a sign-off state of memory there is not an issue to correct any critical EM signal.

CHAPTER 4

BLOCK LEVEL ELECTROMIGRATION FLOW AND USING BLOCK LEVEL IN-DESIGN EM

4.1 INTRODUCTION

Previous chapters discuss EM introduction, EM prone structure and what is the solution to correct them. In typical memory development flow designer do EM during Memory instance generation i.e. after all the blocks are made and tiled. This report presents how to do EM before the Memory instance generation and during the block development stage. So moving forward to block-level EM flow.

4.2 TYPES OF ELECTROMIGRATION ANALYSIS

The types of electromigration (EM) analysis depends on the source of the current data:

Type of EM Analysis

- Static
- Dynamic

For Static EM Analysis:

Manual input of terminal current values in the Property Editor, or terminal current annotations derived from pre-layout simulations. The calculations are based on the sum of the terminal current values. The EM analysis is limited to 0x level only. Use this method if you want faster but rough current value estimates.

For Dynamic EM Analysis:

Waveform data from pre-layout simulations. Because waveform data are time-based, the estimated current values are more accurate for peak and root-mean Square (RMS) current reporting. The EM analysis extends below the 0x level, to the first instance terminals that have current data from the pre-layout simulations. Use this method if you want more accurate current values, and you do not mind longer analysis time.

Running XARA after completing the layout design is mandatory for advanced nodes. However, for complex designs, the corrective iterations can take up to 2-3 weeks of the development cycle. A more preventive method is needed that can reduce the EM verification cycle to a maximum of two cycles. With this vision, our company collaborated with Synopsys to adopt EM Reporter in our flow, to ensure correct by construction designs. Reporting and Checking electromigration involves the analysis of current flow through the resistance network of physically routed nets. After a net is routed, EM analysis can proceed immediately, even though other nets are not yet routed and the layout is not yet completed.

The currents are used from transient simulation, as shown in the flow chart Figure 4.1. For EM checking, same sign-off EM Rule files (RA.tcl) used in Custom Sim-RA are read in Custom Compiler.

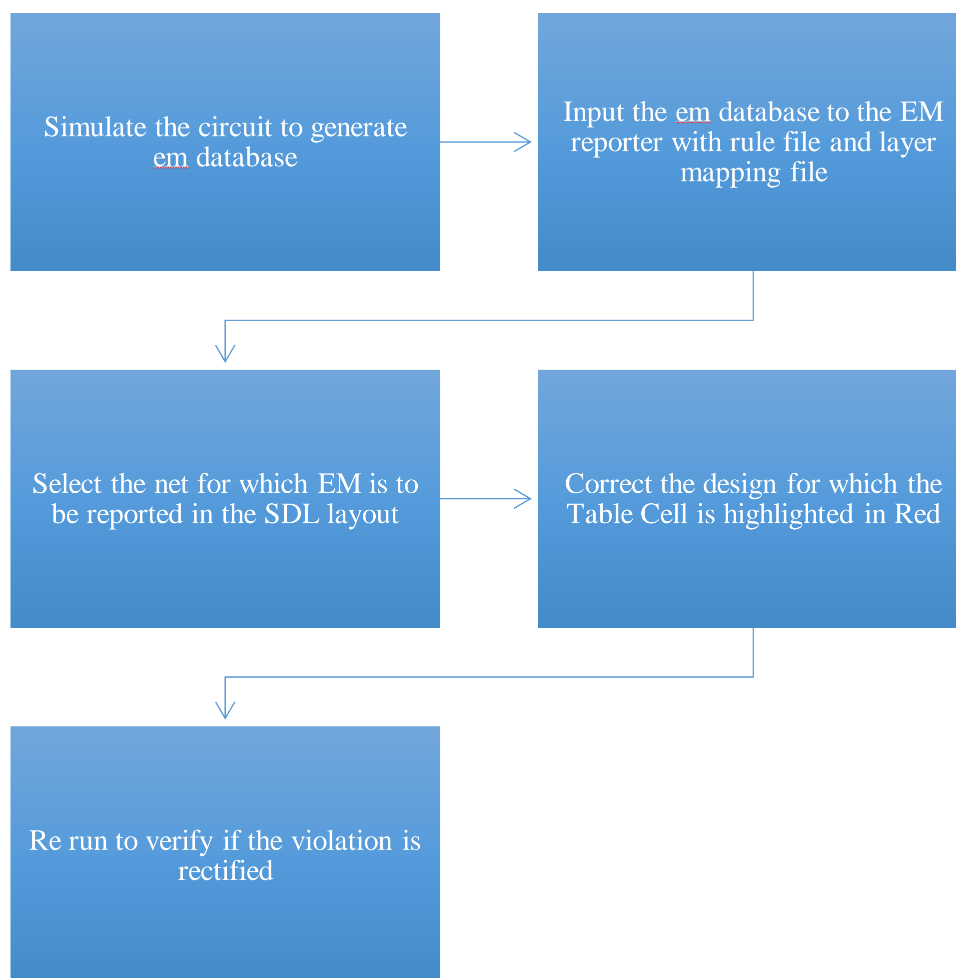


Figure 4.1 In- design EM flow

4.3 USING BLOCK LEVEL IN-DESIGN EM

Following are the steps to analyze and modify EM prone nets Block Level In-Design EM

- Simulate Netlist to generate EM currents

- EM.db generated with current values

- Feed EM.db and EM rule file to EM Reporter
    - To analyze and modify EM prone nets
    - Select EM prone nets on layout canvas
    - Correct selected net as per EM reporter guideline

These steps are also shown in Figure 4.2

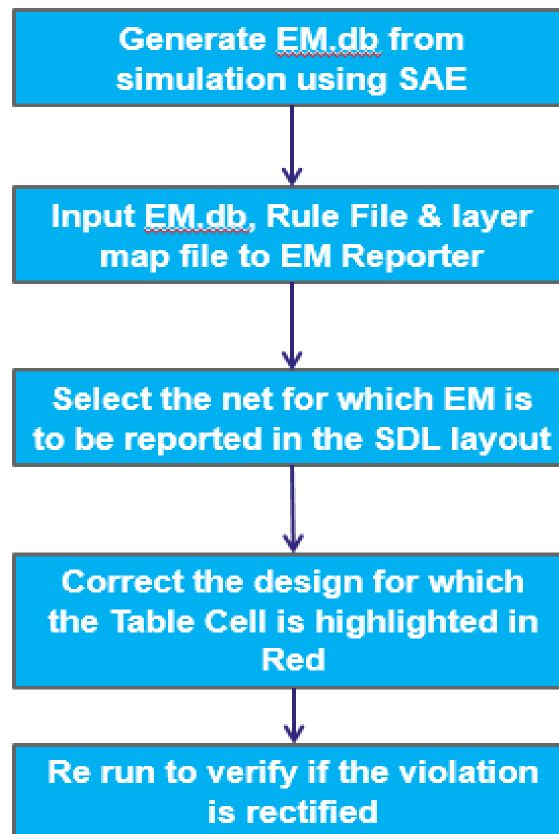


Figure 4.2 Block-level IN-Design EM flow

EM prone nets are quite complex in nature. So designers need a tool that can provide some observations while developing the layout.

The solution that is developed with Synopsys to have an in a design flow that would help the designer to make EM aware decisions while making the layout.

This correct by construction approach includes 5 basic steps.

Simulate: Firstly, simulate the netlist and generate current values from which EM.db is generated

Report: After that EM.db, EM Rule file and layer map file are given as input to EM reporter.

Highlight: Then select the net for which EM is to be reported and highlighted in SDL layout

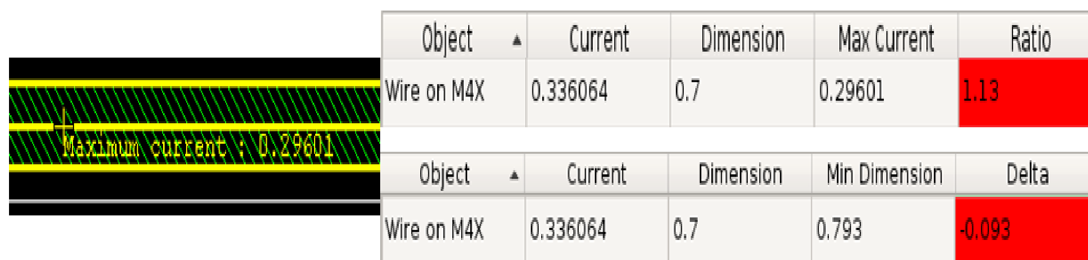
Analyze: Then analyze the net on EM reporter, the net with Red color has EM issue and it is shown either by current/dimension type comparison

Correct: correction is then done by using either increasing the metal with or solution discussed in the introduction part.

4.4 EM REPORTER

The EM reporter directly highlights the EM violated nets in the layout canvas. The only requirement is that the particular net should be completely routed, even if the design is not complete.

The report also indicates the delta width by the wire should be adjusted to correct the design. The designer can analyze Iavg, Irms, Ipeak and I/Imax. The Figure 4.3 is showing the max current that wire can carry w.r.t the given width i.e. 0.7 and the current requirement on this wire is larger than the max current it can carry so EM Reporter shows the I/Imax ratio and delta width required to meet the EM stress issue.



Object	Current	Dimension	Max Current	Ratio
Wire on M4X	0.336064	0.7	0.29601	1.13

Object	Current	Dimension	Min Dimension	Delta
Wire on M4X	0.336064	0.7	0.793	-0.093

Figure 4.3 The max current that wire can carry w.r.t the given width.

Purpose: To ensure correct by construction designs.

Approach: EM analysis on selected layout part of complete Design uses the same EM rule file used in XARA.

Output: The EM Reporter annotates net segment/ via that cause the violation, directly on layout canvas. The EM Reporter showed in Figure 4.4 and in Figure 4.5 output in tabular form for Iavg, Irms, Ipeak, and I/Imax.

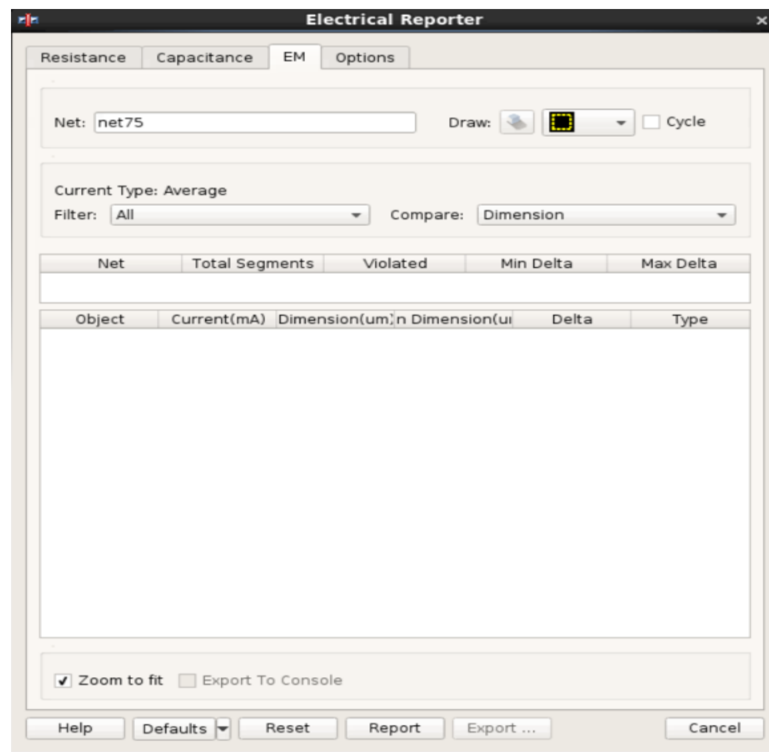


Figure 4.4 EM Reporter -GUI

There are two views available for EM Reporter as shown in Figure 4.4 and Figure 4.5. One compares current and other compares dimensions. Single Left Mouse click on any row directly highlights the wire segment/via on the Layout Canvas.

EM Reporter Reports various current data and violations in the Electrical Reporter dialog box. The EM Reporter compares calculated current values (based on path widths, vias and pin current) with the maximum allowed current values in the technology database, an ITF-EM file, or an iRCX file. The designer can view and monitor current flows in wire segments and vias. Based on the results, you can modify components in your design, such as increasing the wire width, to reduce electromigration and avoid violations. The EM Reporter reports results for the following current types: Average, RMS, and Peak.

The EM Reporter compares the wire widths and vias against current density rules and generates reports that lets you locate wire segments or vias that might cause reliability problems. Inputs required for the flow are EM database for the schematic, RA-TCL rule file and Layer Mapping file.

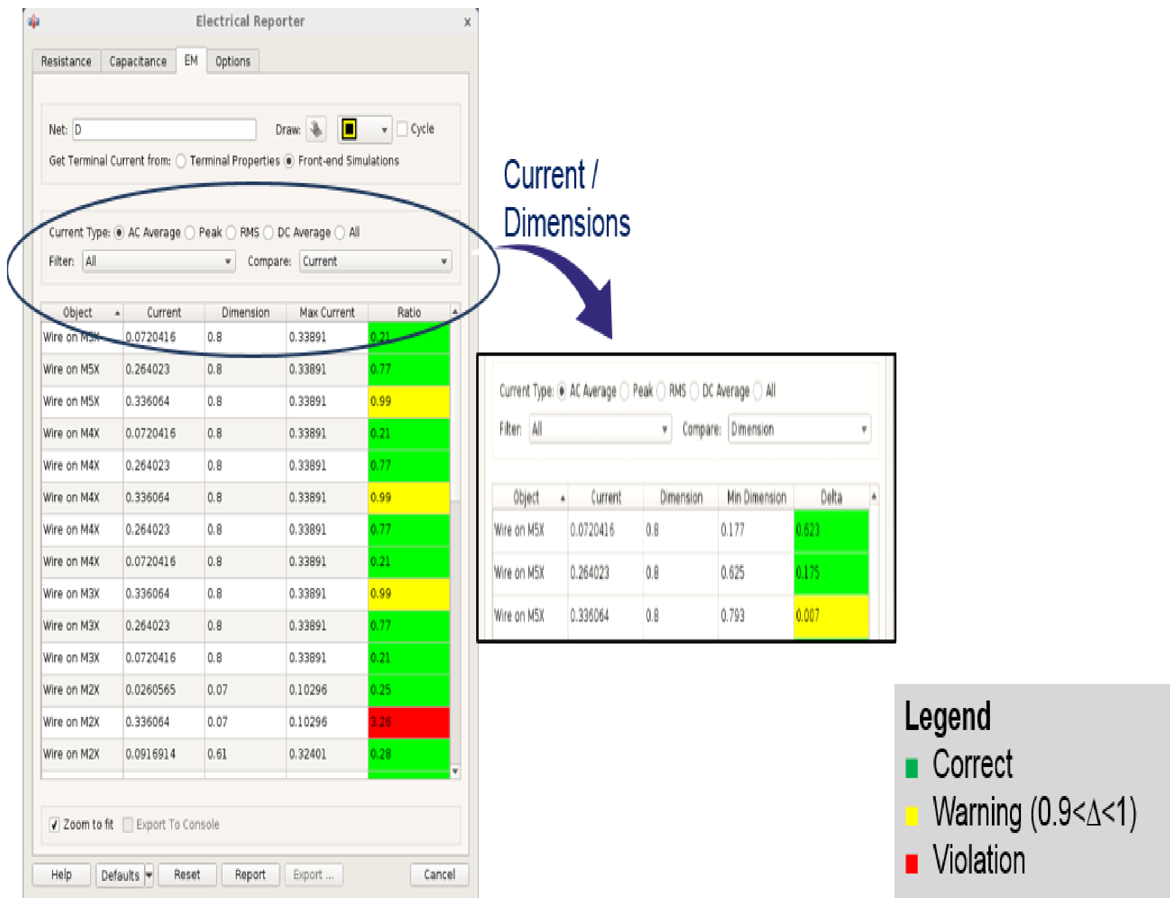


Figure 4.5 EM Report GUI, EM Reporter Features for current and Dimensions violations

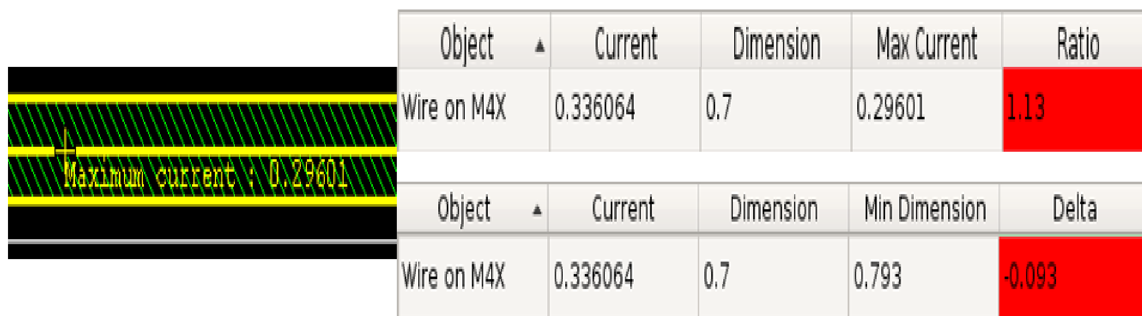


Figure 4.6 EM Reporter and annotation on layout

The EM Reporter gives information about Iavg, Irms, Ipeak, and I/Imax. The results are given in an interactive table shown in Figure 4.6 which highlights the concerned net directly on the layout canvas. Figure 4.7 provides information regarding the maximum width for the concerned net vs the actual width of the net. The designer can adjust the layout directly based on this information.

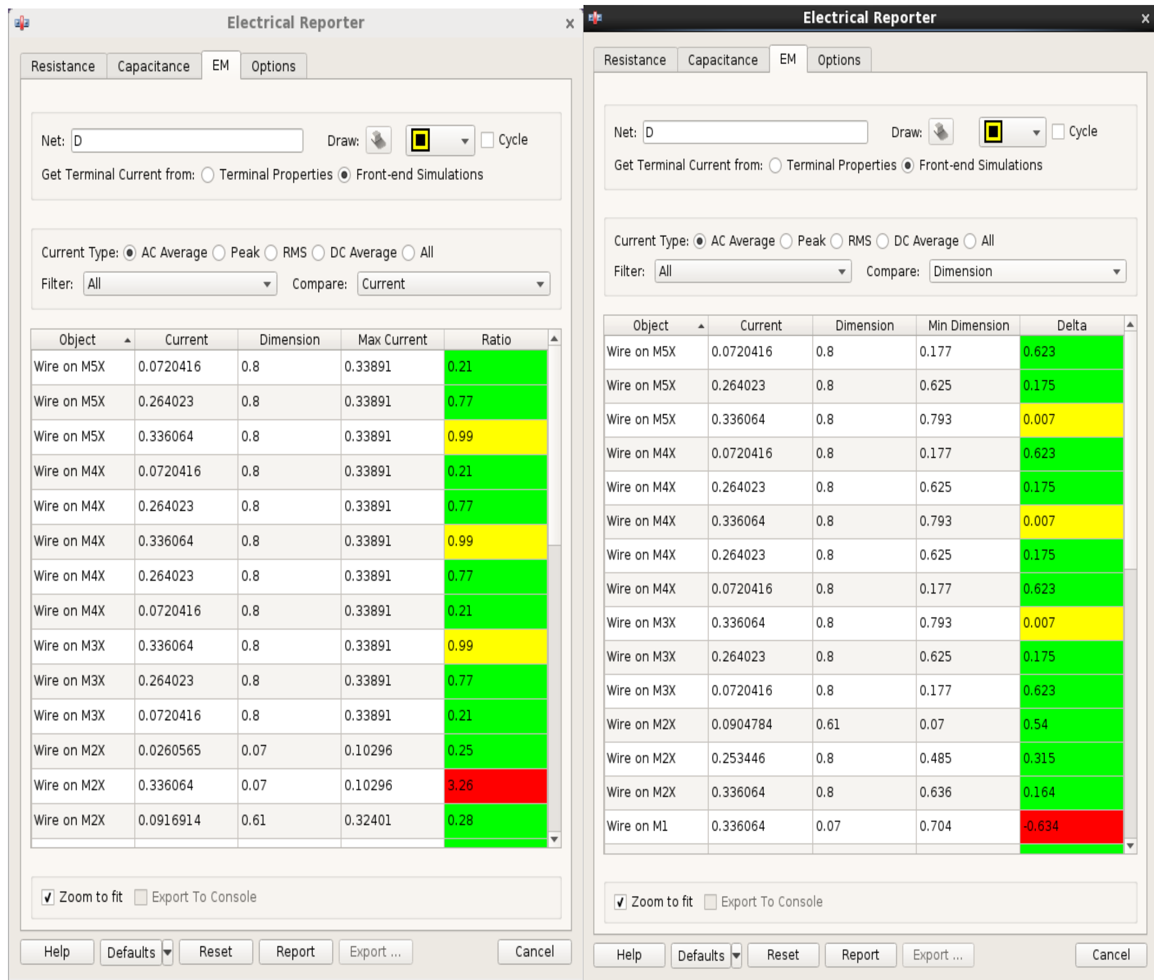


Figure 4.7 EM Reporter features for Current and Dimension Violation

Briefly, the EM Reporter provides the following information shown in Figure 4.7

Object: The layer on which the wire segment is located

Current: The calculated current of the wire segment

Dimension: The width of the wire segment.

Max Current: If you selected Compare: Current) The maximum current allowed for the wire segment.

Ratio: (If you selected Compare: Current) The ratio of the calculated current for the wire (Current column) and the maximum current allowed (Max Current column): Current/Max Current.

Ratio > 1 is a violation, and the table cell is red.

Ratio < 1 is non-optimal, and the table cell is green.

Min Dimension: (If you selected Compare: Dimension) The minimum wire width that avoids violation.

Delta: (If you selected Compare: Dimension) The difference between the actual wire width (the first Dimension column) and the minimum wire dimension (the second Dimension column): [first Dimension – second Dimension].

Difference < 0 is a violation, and the table cell is red.

Difference > 0 is non-optimal, and the table cell is green.

Type: The type of current: DC (average direct current), AC (average alternating current), Peak (peak current value), or RMS (root mean square current value).

In the presented work, the flow will run in Memory block with stimuli provided by the design engineer. The em.db is then used to analyze the currents on routed nets and correct them as required.

Comparing the results of InDesign EM versus our Sign-off CustomSim-RA flow, it can be seen that InDesign EM identifies 90% of the EM violations before the Sign-off validation phase. With this, it can be anticipated that the Sign-off validation phase can be reduced, which is two weeks today (for Memory IP) to two days.

The next chapter is about the step by step approach how to use EM reporter in our design to understand how efficient this tool is during routing in SDL.

CHAPTER 5

EM AWARE ROUTING (Running Block Level Electromigration)

5.1 INTRODUCTION

As described in previous chapters, In-Design EM Reporter is capable of reading the Foundry EM rules and providing width value to the designer to fix EM violations. However, the designer has to manually make the required changes to the layout. This is the best possible solution today when all routing is done manually. However, when some automatic routing solution is used for certain nets, instead of the designer passing metal width values to the auto-router, the required width can be passed by the EM Reporter by doing some computation. This is the main ideology.

Step 1 - Annotation of Current on Schematic

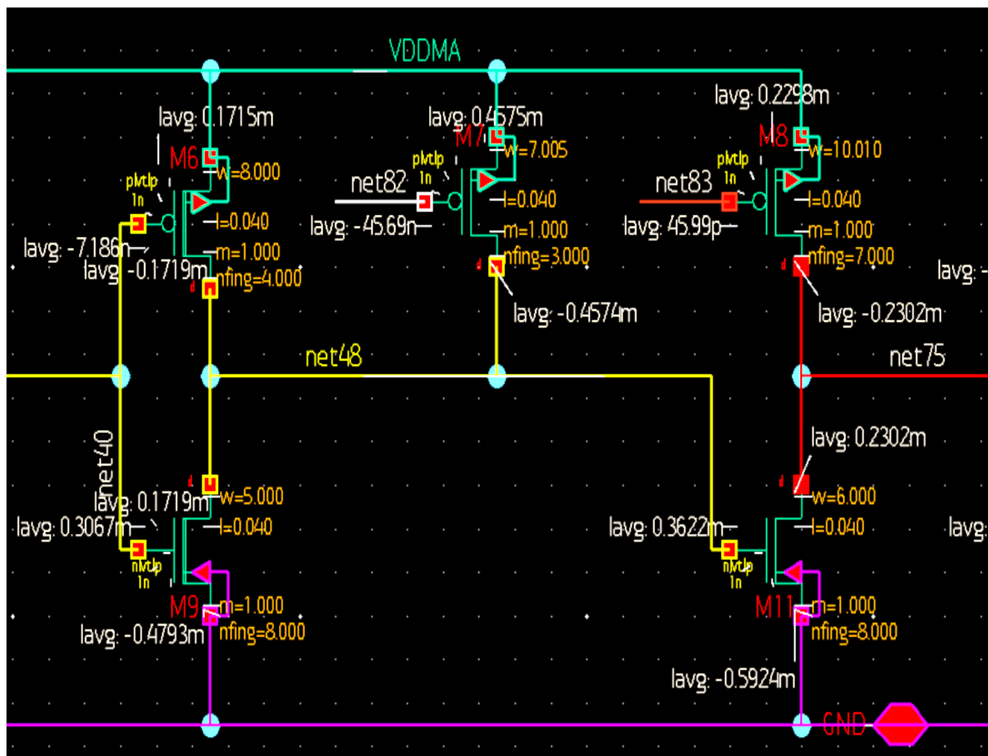


Figure 5.1 Block schematic in Custom Compiler

As shown in Figure 5.1 first step is to simulate the netlist from which .fdsb file (output plot file format) is generated which is annotated on the schematic design. Then layout designer needs to meet annotated value during the routing stage.

Step 2 - Annotation of Current on Layout

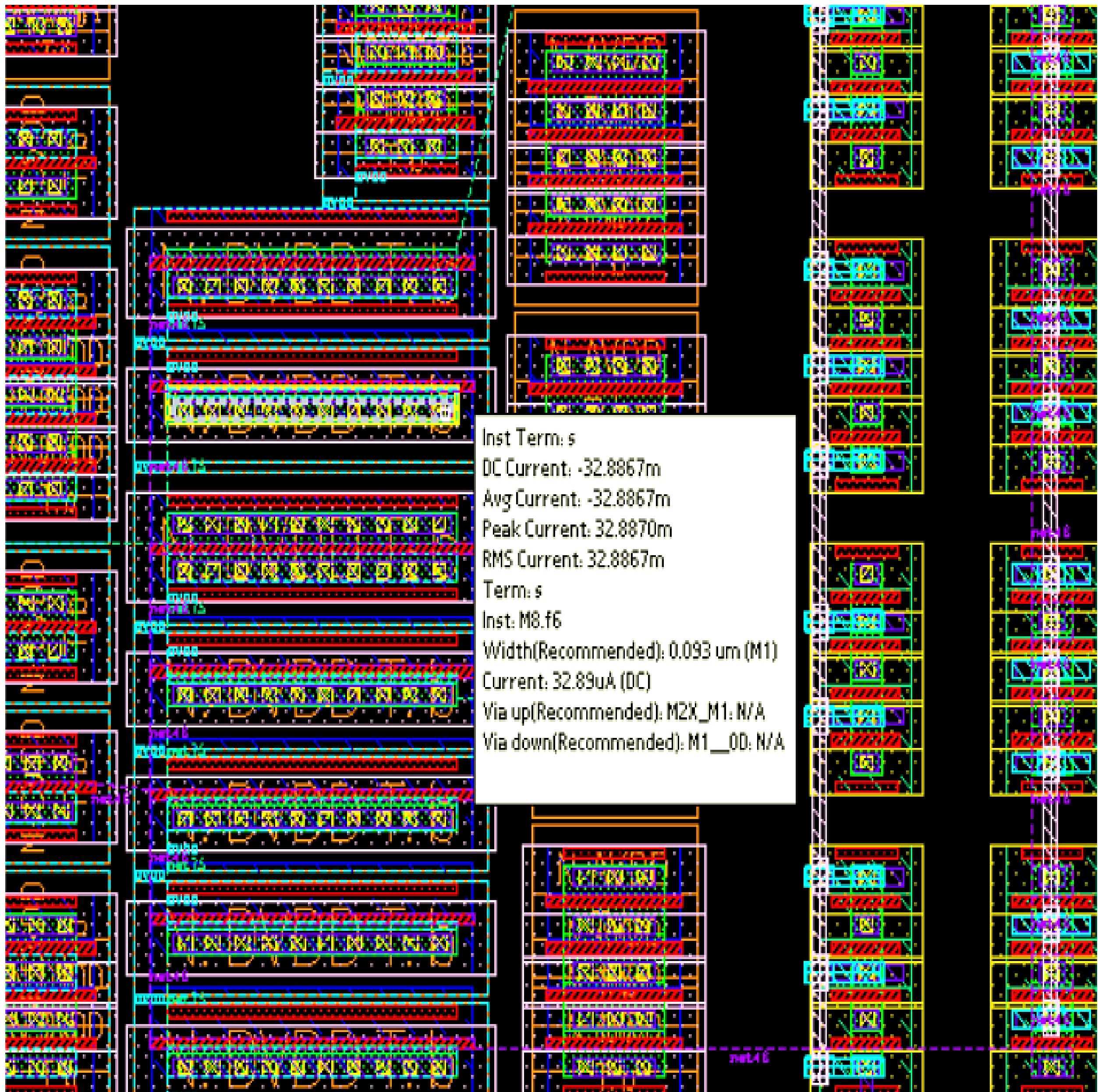


Figure 5.2 Block level layout with annotation of currents.

The same .fdsb file generated after simulation can also be annotated on to the placed devices in layout. If the cursor is moved around the placed devices then it will show the device terminal currents, also it will show the recommended width for first metal on to the terminal as shown in Figure 5.2

Step 3 – Route the nets

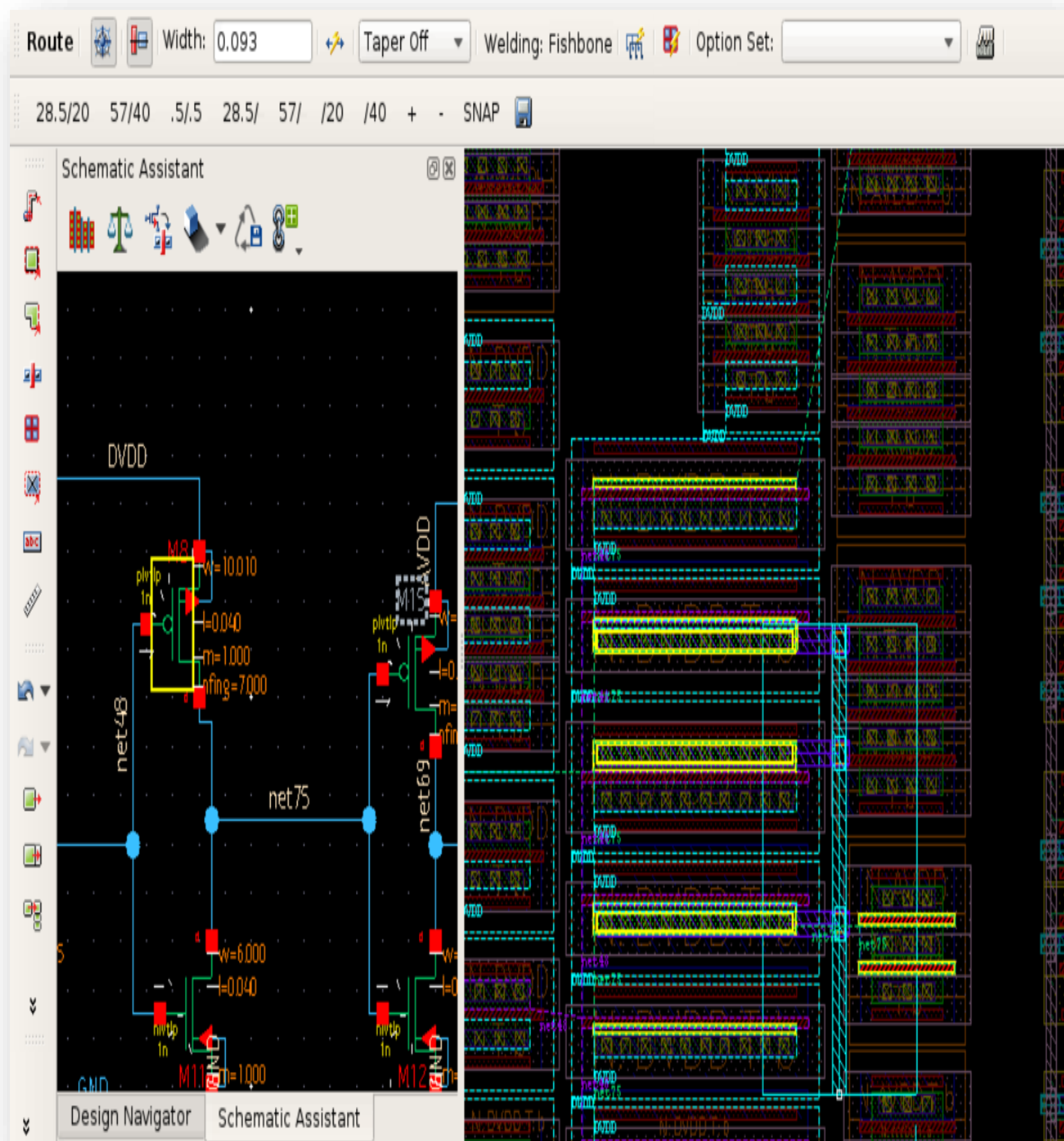


Figure 5.3 Interactive router works to place vias and placing metal lines

Then start doing routing either by create interconnect or interactive router and start moving the metal lines and placing the via's shown in Figure 5.3. Route the nets using Create Interconnect or Interactive Router start with the recommended width.

Step 4 – Run EM Reporter

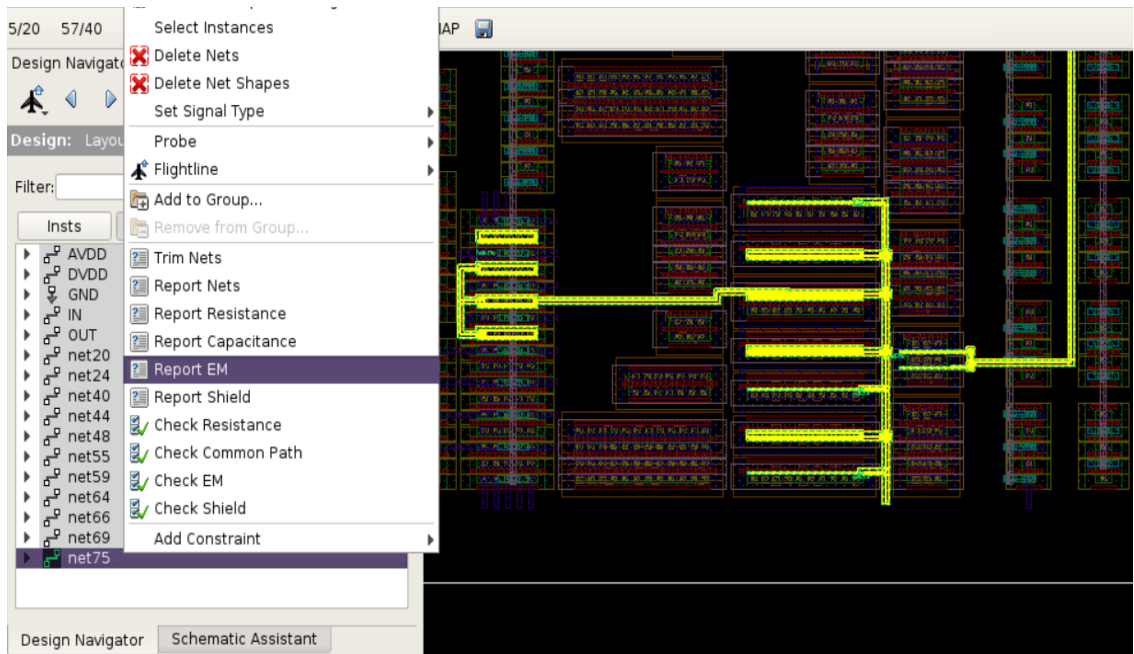


Figure 5.4 Running EM Reporter on specific nets.

Figure 5.4 shows Report EM option is selected from Electrical button in layout window in Custom Compiler. After routing, to check the EM on the particular routed net then run the EM reporter on the selected net by selecting the net and clicking Report EM.EM Reporter - GUI pops up as shown in Figure 5.5.

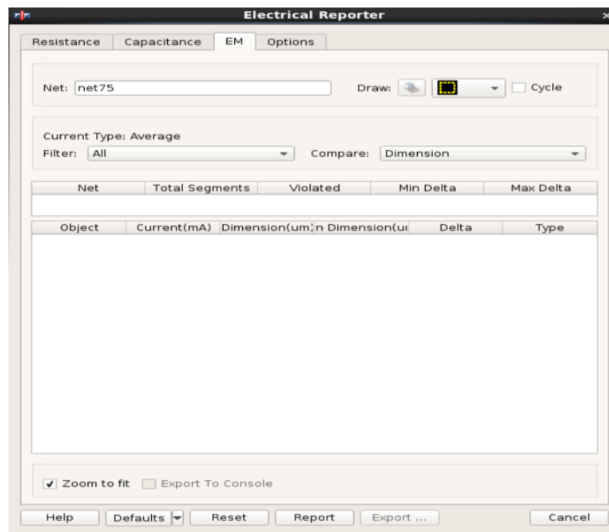


Figure 5.5 EM Reporter –GUI

Step 5 – EM Violations reported

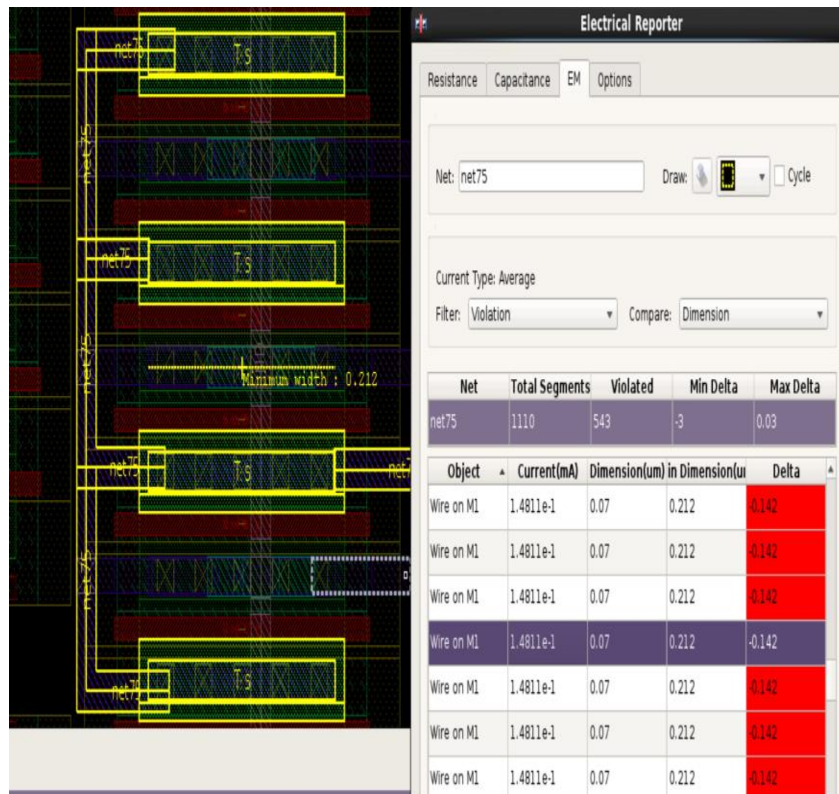


Figure 5.6 EM Reporter violations for selected nets on layout editor.

After clicking Report EM, as shown in Figure 5.6 the EM error on the segments of nets will display and will also display the delta value of width to be increased in order to meet EM.

Step 6 -Fix EM violations using the recommended width

Fix EM violations reported by EM Reporter one by one. Run EM Reporter after fixing each segment to review EM shown in Figure 5.7.

From the above procedure the following points are concluded:

- Correct by constructed Signals with this flow = ~95%
- Final Sign-off on complete design is must for a complete view
- Only a few top-level signal nets need fixes, block-level changes are very few, if at all present
- Expected to reduce the reliability validation cycle time by ~ 50%.

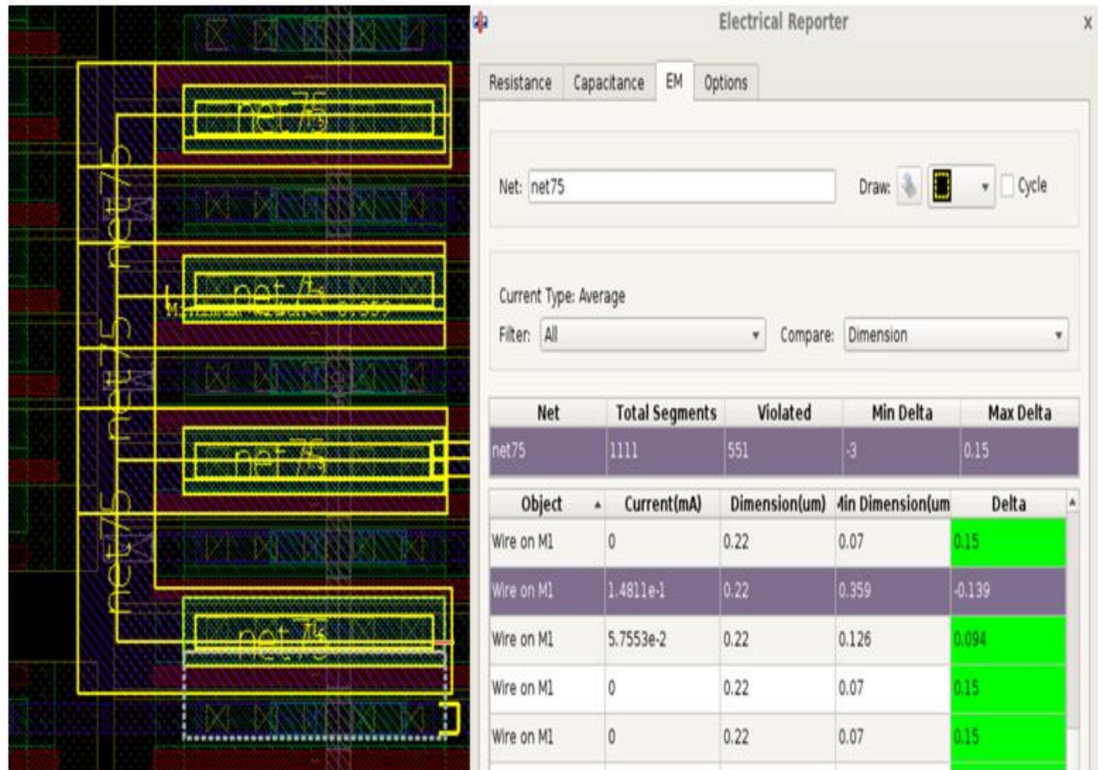


Figure 5.7 Fixing of EM violated nets.

Chapter 6

EM-AWARE AUTO ROUTER

6.1 CONCEPT OF EM AWARE ROUTING

As the need for high-speed low power designs increase, it results in high EM currents for design. To reduce product cycle time, there is a need to improve our product development time and product validation time. The previous sections have focused on reducing Production Validation time. This chapter addresses the Product Development time.

The idea behind EM Aware auto-routing is that it combines the capabilities currently available with EM reporter and Auto-Router as shown in Figure 6.1 given below. Aim of this tool is to enable layout designer to route all power and signal nets automatically that are EM compliant to the design specifications, leading to a big productivity increase in layout development time. Routes PG and signal nets automatically with meeting EM specs by Uses capabilities of EM reporter and Auto Router.

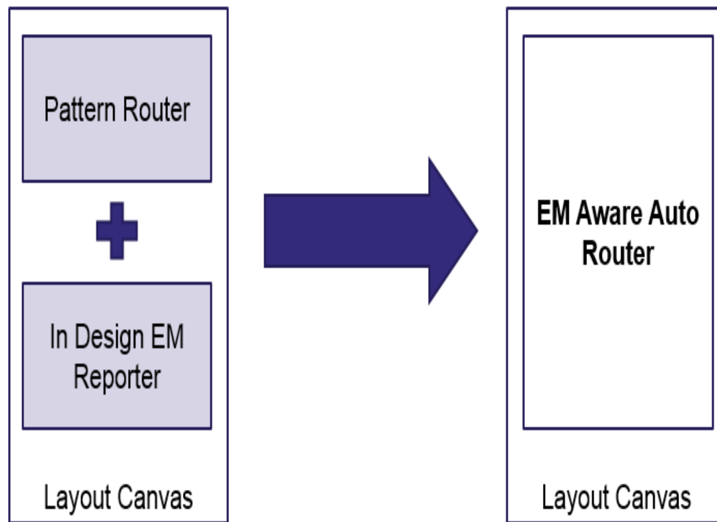


Figure 6.1 The idea to combine the pattern router and In Design EM reporter to develop EM Aware Auto Router.

This tool flow diagram is as shown below

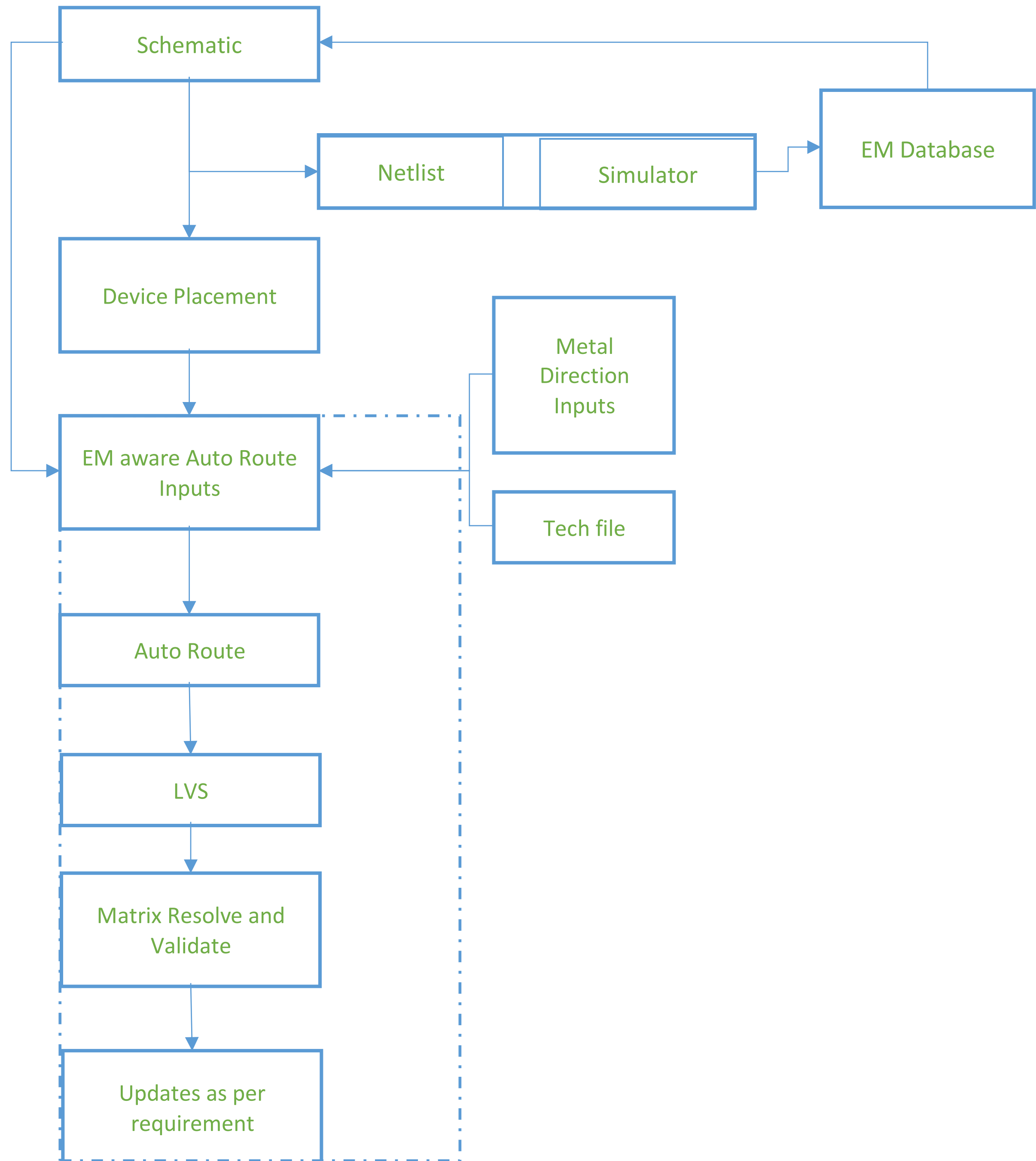


Figure 6.2 EM Aware Routing Flow

As shown in Figure 6.2 the flow starts with feeding current values to all the schematic nodes before starting layout development. These current values either be feed manually or database file derived from simulation results.

At the second step, the layout designer starts device placement using Symbolic Editor (SED) as per product

specifications and design rules. Additionally, the designer needs to draw power pins and signal pins. EM aware Auto Router will automatically route metal layers from these pins to devices.

At the third step, the role of EM aware auto-router comes into play. To use this tool designer needs to fill in following prerequisites.

- Preferred metal directions
- Technology file for EM current to width calculation
- Routing pattern to follow for Power nets and for signal nets
- Pattern Router auto routes matched nets for analog devices.

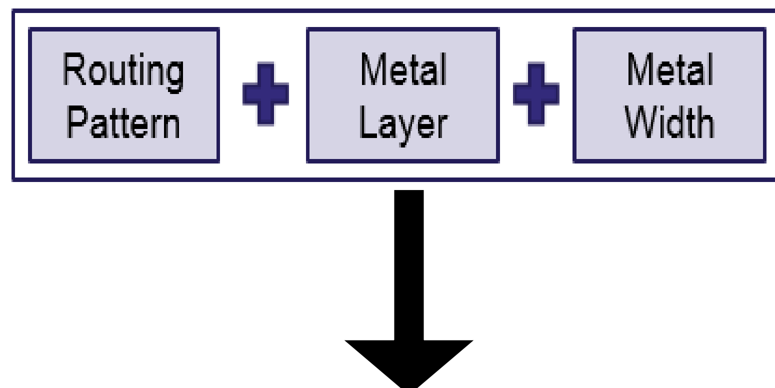
To perform routing connection designer provides the following inputs

- Routing pattern
- Metal layer
- Metal width

And Output is

- Auto Routed selected net

The designer needs to feed in the metal direction in which he/she desire to route metals and EM aware auto-router picks current values from schematic or Parametric cell or (Pycell) property and use technology file to calculate the required metal width for the power or signal node. In Figure 6.3, input data required for working of EM Router. The tool first routes all the power nodes from metal1 to top-level pin and follow the process for signals. If there is no issue, then tool resolves the matrix to validate the design using XARA. As per the results, the tool will further tweak the metal widths to meet the product specifications. In one or two iterations, the tool has become capable of automatically route an LVS (Layout VS Schematic) clean design while meeting EM specifications.



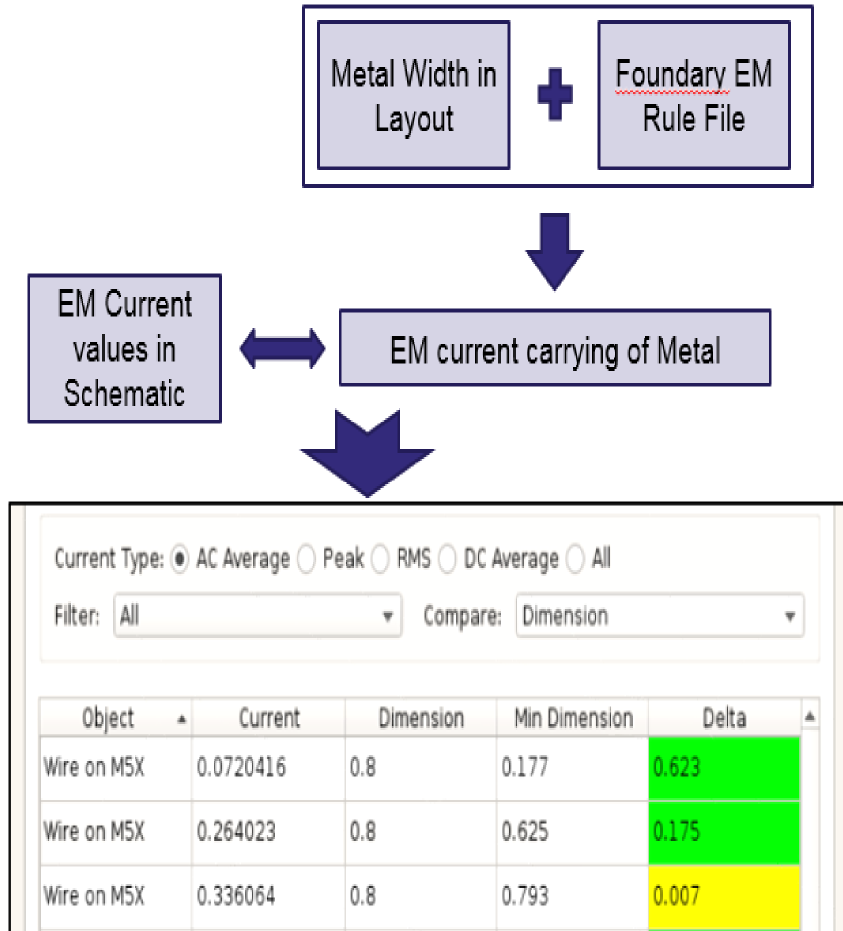


Figure 6.3 Input data required for working of EM Router.

6.2 EM Aware Auto Router: Working Principle

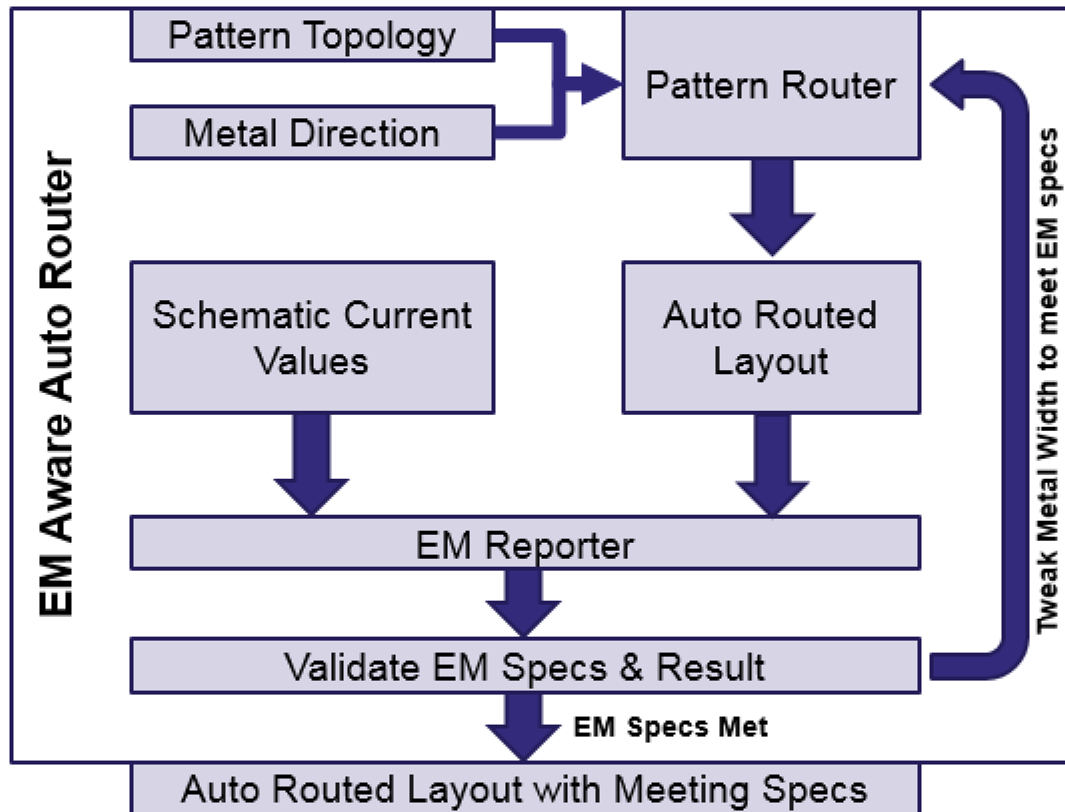


Figure 6.4 The proposed working principle for the EM Aware Auto Router

6.2.1 Simple Working Principle

Pattern Router Routes Nets as per User Inputs

- Inputs Required
- Pattern topology
- Metal Direction

EM Reporter runs in the background

- Validate
- Tweak metal widths for violation
- Re-validate

Two to three loops of iterations

- Auto Routed EM clean Layout for Selected Nets
- No User intervention required

6.3 Traditional Flow for EM Clean Development

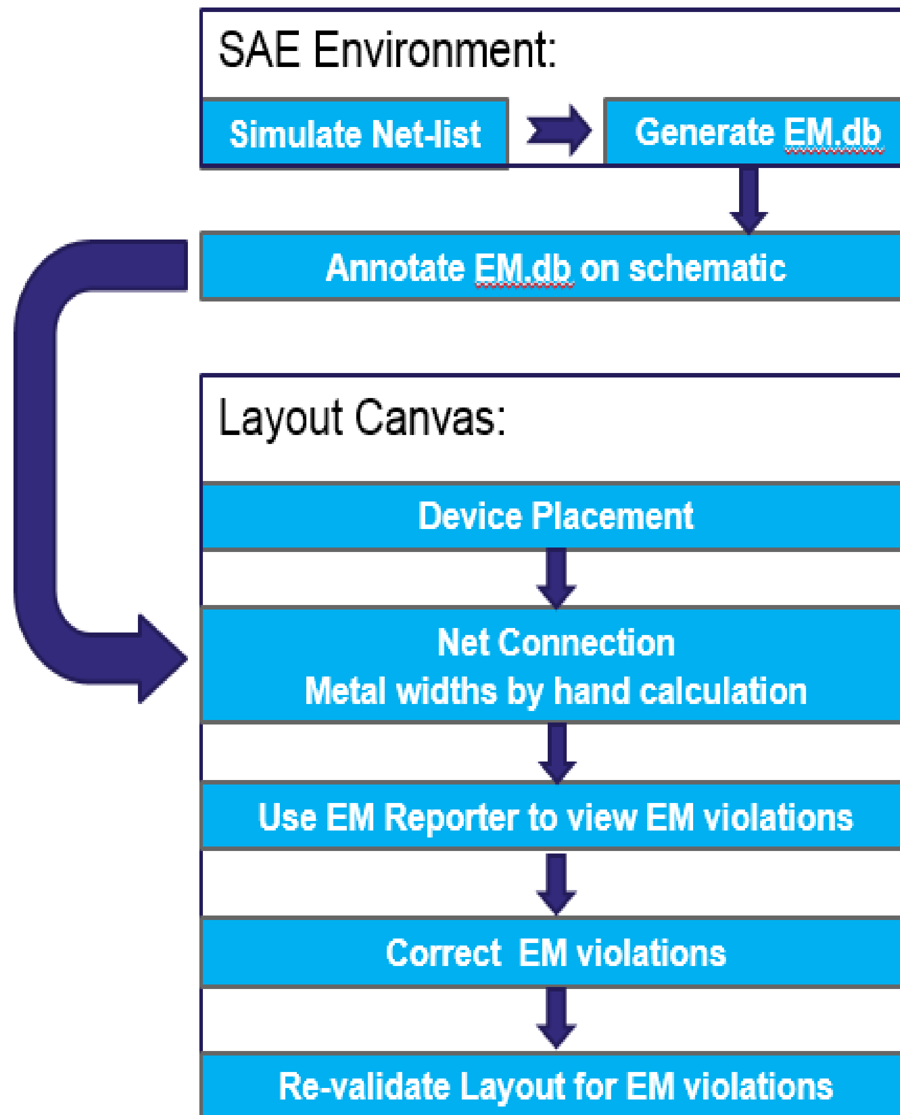


Figure 6.5 Figure shows the traditional flow designer use for EM clean development

Traditional EM Flow as shown in Figure 6.5

- Generate EM.db by Net-list Simulation
- Annotate EM.db on the schematic
- Device placement on layout canvas

Route nets

- Hand calculation for EM metal widths
- Route nets manually

EM reporter for EM violations

- Select individual net
- View Violation
- Correct EM Violation
- Re-validate net

6.3.1 Proposed Flow for EM Clean Development

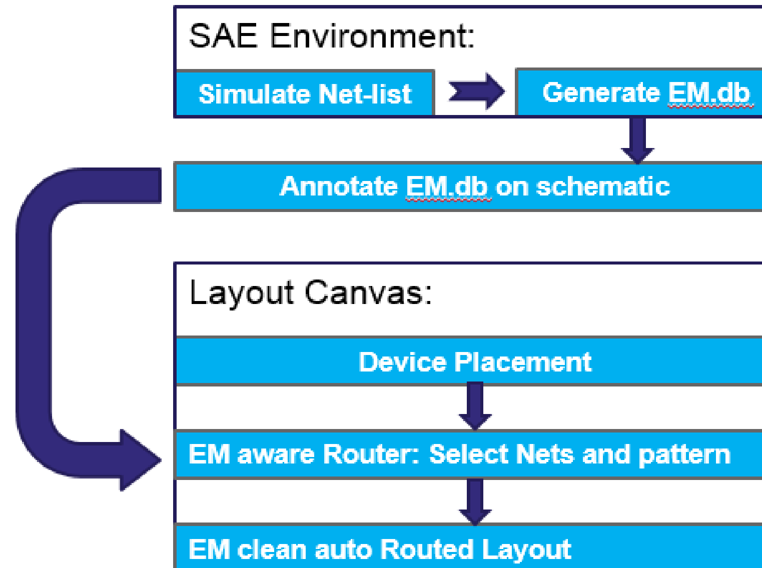


Figure 6.6 The proposed flow for the EM Clean Development

As shown in Figure 6.6 EM Aware Routing Flow

- Similar flow with few changes

Similar area of operation

- Net-list simulation for EM.db generation
- Annotate EM.db on the schematic
- Device placement on Layout Canvas

New Flow

- Open EM aware auto Router

Provide Inputs (Same as pattern router)

- Net selection
- Pattern Selection for selected net
- No need for Metal Width

Auto Routed EM clean Layout as Output -No user intervention

6.3.2 Foreseeable Challenges

The following challenges are needed to be taken care of while developing this tool.

- Fixed area of routing
- Traversing through hierarchies in layout
- LVS unclean cases
- Accuracy settings

6.3.3 Results on Power Nets of Smaller Designs

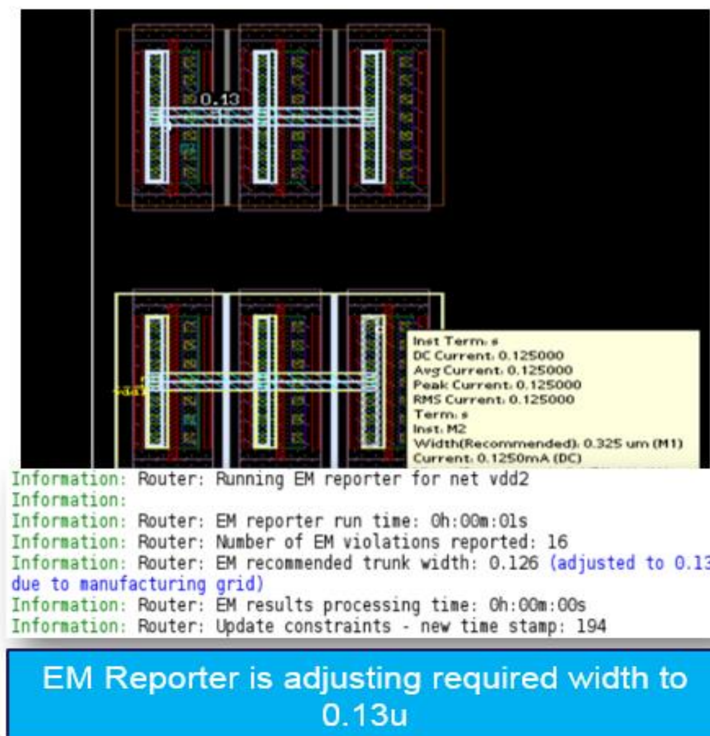


Figure 6.7 EM Aware Routing for Power nets with low current.

Our first target was to use EM Aware Routing to calculate the widths of Power nets accurately. Below are the results. In the first case, the currents in vdd1 and vdd2 pins of the transistors is 125uA each. Based on this, EM Reporter calculates the required width for vdd1 and vdd2 (0.13u) and completes the routing. It takes less than a second to run EM Reporter and finish this routing as shown in given Figure 6.7. Next, the terminal currents is increased to 150uA and run EM Aware routing again as shown in Figure 6.8. This results in fresh calculation of the required width, which is 0.19uA and the routing with this new width is completed in less than a second as shown in figure below.

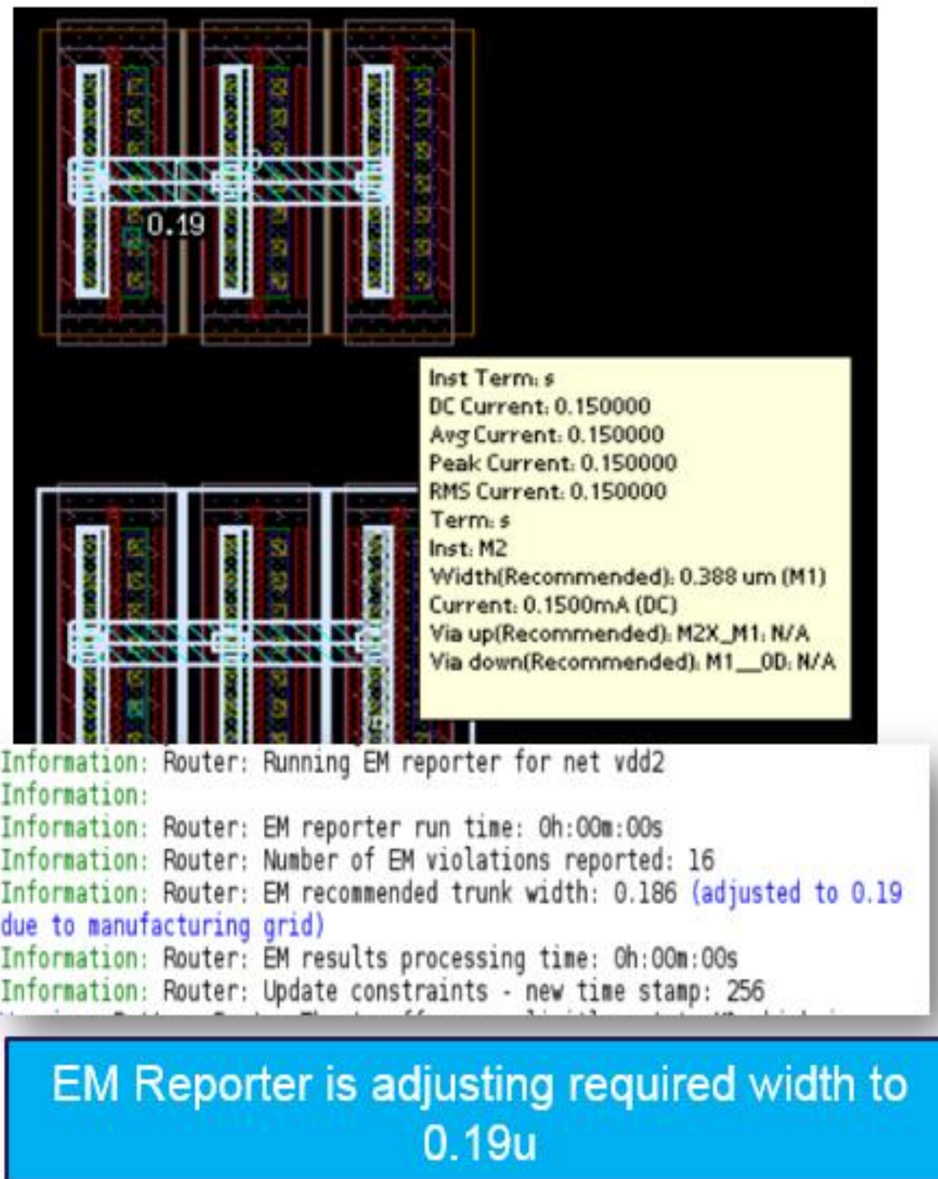


Figure 6.8 EM Aware Routing for Power nets with increased current

6.3.4 Results on Power nets of Bigger Designs

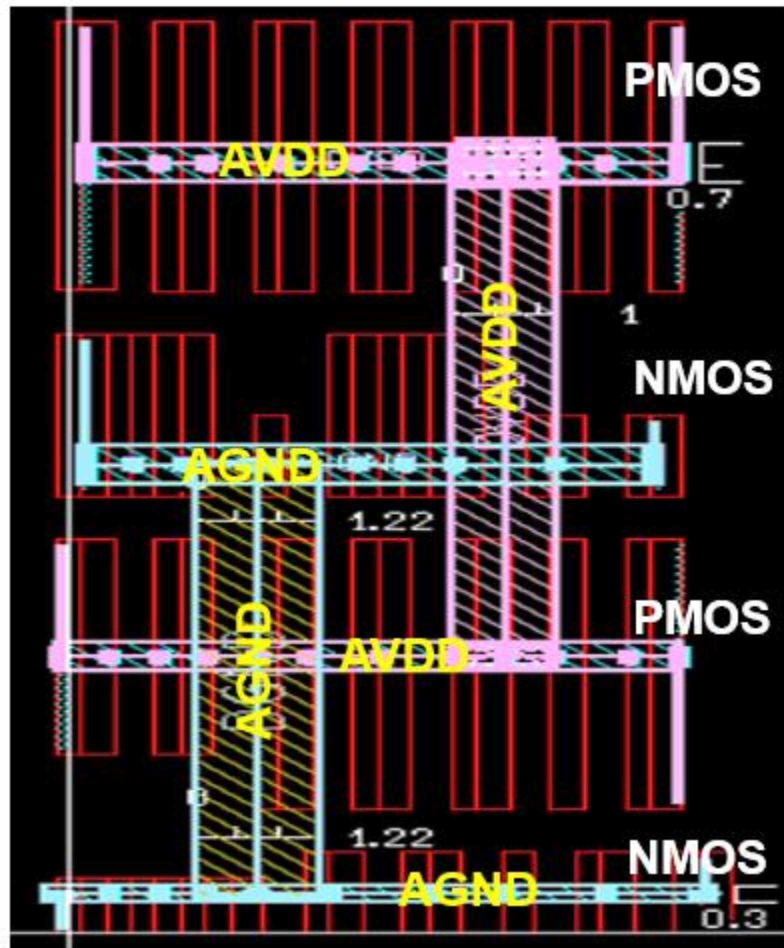


Figure 6.9 The results of EM Router on Bigger designs with high current specifications nets (such as Power Nets)

For Bigger Design EM Reporter has been also tested as shown in Figure 6.9.

The specifications of the tested design are:

- Large MOS count
- Higher EM current value specs
- Multiple Rows of devices
  - PNPN
  - NPPN
  - PNNP

Some data points for this snapshot

- AVDD width 0.7 u
- AVDD width 0.43 u
- Spine connection 1 u

6.3.5 Results on Signal Nets

Similarly, for signal nets that are regular and can be routed with Pattern Router, the following results are obtained. Net in1 and net in2 carry equal currents (125uA) and EM Reporter calculates the tap-off width to be 0.11u and trunk width to be 0.23u, which are EM clean by construction as shown in Figure 6.10

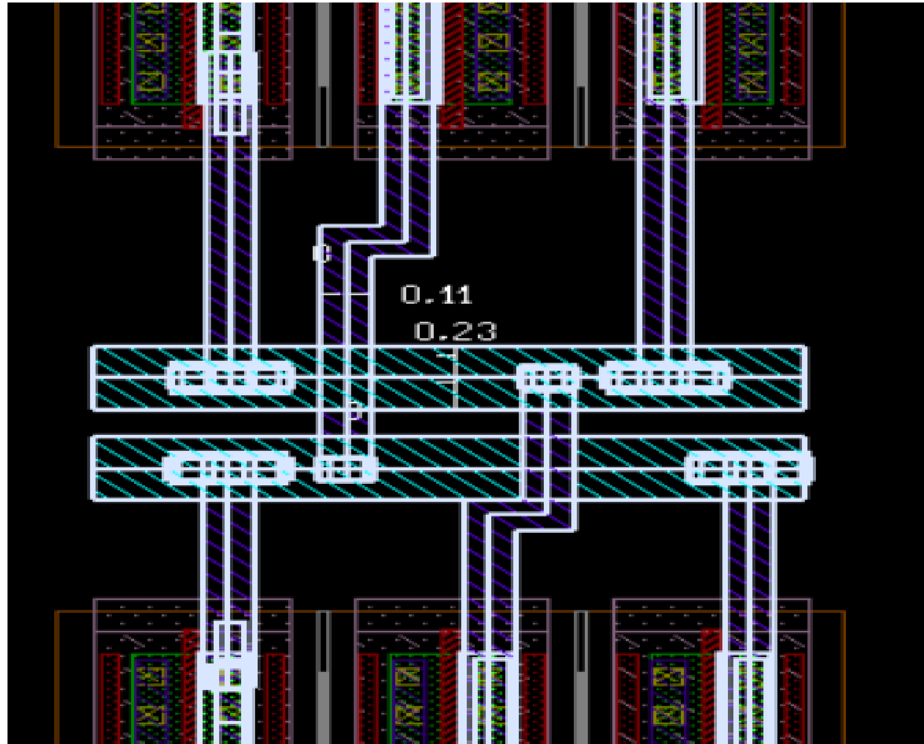


Figure 6.10 EM Aware Routing for signal nets

Automatic calculation of EM for power networks works well is concluded with this.

Promising prelim results for the simple signal nets.

CHAPTER 7

CONCLUSIONS AND FUTURE SCOPE

7.1 CONCLUSIONS:

To guarantee a better performance for longer time of the chip, the designer needs to identify critical wires in the circuit layout and to alter these critical wires which are more prone to electromigration using techniques that retard the electromigration impact on the circuit. In this work, it is proposed to identify the critical lines at the very early stage of designing and correcting them so that electromigration will appear minimum in layout at the sign off stage of IP. Electromigration effects need to be considered during block-level design and should be considered as an integral part of the design flow. Cleaning EM towards the end of the complete IP design can have a serious impact on the productivity and delivery schedules. This thesis work describes how EM on per-net basis runs during the design phase and end up with very few EM violations during Sign-off validation. For further productivity, our company is collaborating with Synopsys to get some regular routings EM correct by construction. Currently, the focus is on the automatic routing engine to come up with correct widths for power and ground connections and any regular signal nets where automatic routing is a possible solution.

7.2 FUTURE SCOPE:

EM Aware Routing is a feature that is under development in Custom Compiler (Synopsys). Layout designers see a lot of value productivity gain for the layout designers when this feature comes into production. Next steps in the future are to test more complex structures to understand all scenarios where this feature can be used. Of course, when the net is manually routed, the designer has to exercise In Design EM on per net basis as explained in the second chapter.

For future advancements, the EM reporter to work with complex signal nets including hierarchical layouts and power nets connection to pre-define power pins.

References

[1] F. Matsuoka et al., "Electromigration reliability for a tungsten-filled via hole structure," IEEE Trans. Electron Devices, vol. 37, no. 3, pp. 562-567, 1990.

[2] J. S. May, "Electromigration characteristics of vias in Ti:W /Al-Cu(2 wt%) multilayered metallization, in Proc. 1991 Int. Reliability Phys. Symp., 1991, pp. 91-96.

[3] F.S. Chen, Y.S. Lin, GA. Dixit, R. Sundaresan, C.C. Wei and F.T. Liou, "Planarized aluminum metallization for sub-O.5um CMOS technology," in EDM Tec. Dig., 1990, pp.51-54.

[4] T. Tsutsumi, H. Kotani, J. Komori, and S. Nagao, "A selective LPCVD tungsten process using silane reduction for VLSI applications," IEEE Trans. Electron Devices, vol.37, no.3, pp.569-576, 1990.

[5] Inaba, H., et al. "Antistatic protection in wafer drying process by spin-drying." *IEEE transactions on semiconductor manufacturing* 5.3 (1992): 234-240.

[6] Black, James R. "Physics of electromigration." *12th International Reliability Physics Symposium*. IEEE, 1974.

[7] Lienig, Jens. "Introduction to electromigration-aware physical design." *Proceedings of the 2006 international symposium on Physical design*. ACM, 2006.

[8] Ye, Wei, et al. "Tackling signal electromigration with learning-based detection and multistage mitigation." *Proceedings of the 24th Asia and South Pacific Design Automation Conference*. ACM, 2019.

[9].Lienig, Jens. "Electromigration and its impact on physical design in future technologies." *Proceedings of the 2013 ACM International symposium on Physical Design*. ACM, 2013.

[10] Wachnik, R. A., et al. "Practical benefits of the electromigration short-length effect, including a new design rule methodology and an electromigration resistant power grid with enhanced wireability." *2000 Symposium on VLSI Technology. Digest of Technical Papers (Cat. No. 00CH37104)*. IEEE, 2000.

[11] Lin, Mingte, et al. "Upstream electromigration study on multiple via structures in copper interconnect." *2009 IEEE International Interconnect Technology Conference*. IEEE, 2009.

[12] Morusupalli, Rao R., William D. Nix, and Jamshed R. Patel. "Comparison of Line stress predictions with measured electromigration failure times." *2007 IEEE International Integrated Reliability Workshop Final Report*. IEEE, 2007.

[13] S. Bigalke, J. Lienig, G. Jerke, J. Scheible and R. Jancke, "The Need and Opportunities of Electromigration-Aware Integrated Circuit Design," *2018 IEEE/ACM International Conference on Computer-Aided Design (ICCAD)*, San Diego, CA, 2018, pp. 1-8

[14] Bigalke, Steve, et al. "Increasing EM robustness of placement and routing solutions based on layout-driven discretization." *2018 14th Conference on Ph. D. Research in Microelectronics and Electronics (PRIME)*. IEEE, 2018.

[15] Bigalke, Steve, and Jens Lienig. "FLUTE-EM: Electromigration-optimized net topology considering

currents and mechanical stress." *2018 IFIP/IEEE International Conference on Very Large Scale Integration (VLSI-SoC)*. IEEE, 2018.

[16] M. H. Lin and A.S. Oates, "Electromigration in Dual-Damascene CuMn Alloy IC Interconnects,"in *IEEE Transactions on Device and Materials Reliability*, vol. 13, no. 1, pp. 330-332, March 2013

[17] K. Jang *et al*., "Electromigration Characteristics and Morphological Evolution of Cu Interconnects on CVD Co and Ru Liners for 10-nm Class VLSI Technology," in *IEEE Electron Device Letters*, vol. 39, no. 7, pp. 1050-1053, July 2018.

[18] M. Lin and A. S. Oates, "The Effects of Al Doping and Metallic-Cap Layers on Electromigration Transport Mechanisms in Copper Nanowires," in *IEEE Transactions on Device and Materials Reliability*, vol. 11, no. 4, pp. 540-547, Dec. 2011.

[19] P. Livshits, A. Rysin, S. Sofer and Y. Fefer, "Assessment of Influence of Impedance Mismatch in ULSI Devices on Electromigration of Copper Interconnection Lines," in *IEEE Transactions on Device and Materials Reliability*, vol. 13, no. 1, pp. 231-235, March 2013.

[20] H. Chen, S. X. -. Tan, J. Peng, T. Kim and J. Chen, "Analytical Modeling of Electromigration Failure for VLSI Interconnect Tree Considering Temperature and Segment Length Effects," in *IEEE Transactions on Device and Materials Reliability*, vol. 17, no. 4, pp. 653-666, Dec. 2017

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