Pre-Silicon Testchip (IO ring) validation

A Thesis submitted in partial fulfilment of the requirement for the Award of the Degree of

MASTER OF TECHNOLOGY

in VLSI DESIGN

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CERTIFICATE

This is to certify that this project report titled "**Pre-Silicon (IO ring) Validation** " is carried out by AMALENDU AMAN under the guidance of the undersigned. This seminar is done as a partial fulfilment for the award of the degree Master of Technology in VLSI DESIGN from Department of Electronics and communication, Thapar institute of Engineering and Technology, during JUNE-2024 to MAY-2025. This report embodies original work of candidate and has not been submitted in full or any part to other university for the award of any other diploma and degree.

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DECLARATION

I, **Amalendu Aman** hereby declare that the Seminar Research report entitled is **"Pre-Silicon Testchip(IO ring) validation"** in partial fulfilment of the requirement of the award of the degree of **Master of Technology(VLSI Design**) submitted at **Electronics and Communication Engineering Department**, Thapar Institute of Engineering & Technology(Deemed to be university),Patiala is a record of work carried out under supervision of **Dr**. **Mayank Kumar Rai (Professor, Electronics and Communication Engineering Department, Thapar Institute of Engineering & Technology(Deemed to be University) and Dr. Nisha Gupta (Team lead ST Microelectronics)** from **JULY 2024** TO **JUNE 2025.** The Matter in this has not been submitted in part to any other university or institute for the award of any other degree**.**

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ABSTRACT

The design and verification of Input/Output (IO) circuits play a crucial role in ensuring reliable communication between integrated circuits and external interfaces. This thesis presents the **layout design and verification** of **a level shifter**, focusing on **layout strategies, and verification methodologies** in CMOS technology.

The final layout was verified through Design Rule Check (DRC) and Layout vs. Schemtic (LVS) **validation using Cadence Layout Design Suite and Calibre, ensuring manufacturability and functional correctness. Additionally, the level shifter is an essential circuit for voltage translation between different power domains, especially in low-power and mixed-signal designs. The layout for the level shifter was designed from scratch using Cadence tools, following strict foundry guidelines. Rigorous DRC and LVS checks were performed using Calibre to confirm its correctness and adherence to fabrication constraints.**

This work highlights the **importance of precise layout design and validation in IO circuit**, reducing the chances of post-silicon failures and ensuring first-pass success in silicon fabrication. The successful completion of **level shifter layout, and associated verification steps** demonstrates the effectiveness of the adopted design methodologies.

By presenting a **practical implementation of level shifter design**, this thesis keeps importance in validation of IO and bridges the gap between **theoretical VLSI concepts and real-world design constraints**, providing valuable insights for future IO circuit development.

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TABLE OF CONTENTS

Sr. No.	Name of chapters	Page No.
	Pre-pages	
	Certificate …	ii
	Declaration … … … … … … ... … … … … … … … … … … … …	iii
	Acknowledgement	iv
	Abstract …	v
	List of Figures … … … … … … … … … … … … … … … … … …	Vii
Chapter 1	Introduction … … … … … … … … … … … … … … … … … … …	1
1.1	What is an IO … … … … … … … … … … … … … … … … … …	1
1.2	Why We Need IOs? … … … … … … … … … … … … … … … …	2
1.3	Types Of IOs? … … … … … … … … … … … … … … … … … …	3
1.4	Standard IO Chip Components … … … … … … … … … … … … …	5
1.5	What Is Testchip? … … … … … … … … … … … … … … … … …	6
1.6	Why Testchip? … … … … … … … … … … … … … … … … … …	8
1.7	What Is Level Shifter? … … … … … … … … … … … … … … …	9
1.8	Pre-Silicon Validation Process and Its Importance? … … … … … … …	11
Chapter 2	Literature Review … … … … … … … … … … … … … … … … … …	12
Chapter 3	Research Objectives … … … … … … … … … … … … … … … … … …	13
3.1	Objectives …	13
3.2	Methodology… … … … … … … … … … … … … … … … … … … .	13
Chapter 4	Result …	16
4.1	Parasitic Extraction and Management for ESD Performance … …	17
Chapter 5	Conclusion… … … … … … … … … … … … … … … … … … … …	19
Chapter 6	Future Scopes … … … … … … … … … … … … … … … … … … … .	18
	References … … … … … … … … … … … … … … … … … … … . … … … …	21

LISTS OF FIGURES

Sr. No	Figure Details	Page No
Figure 1.1	Input Output …	1
Figure 1.2	Bidirectional IO …	4
Figure 1.3	Input port ,Output port …	4
Figure 1.4	IO Pads and IO ring …	7
Figure 1.5	Low to high Level Shifter … … … … … … … … … … … … … … … … … …	10
Figure 3.1	Level Shifter without CDM … … … … … … … … … … … … … … … … … …	14
Figure 3.2	Level Shifter layout Without CDM… … … … … … … … … … … … … … …	14
Figure 3.3	Level Shifter With CDM …	15
Figure 3.4	Level Shifter layout Without CDM… … … … … … … … … … … … … …	15
Figure 4.1	DRC of Level Shifter Layout With CDM … … … … … … … … … … …	16
Figure 4.2	LVS of Level Shifter Layout With CDM … … … … … … … … … …	18

CHAPTER 1

INTRODUCTION

1.1 WHATIS ANIO?

An **I/O (Input/Output) as shown in figure 1.1 and 1.3 in VLSI** connects the **internal core logic** of a chip to external circuits. It includes **pads, buffers, ESD protection, and level shifters** for reliable communication. The **purpose of I/Os** is to ensure **signal integrity, voltage compatibility, and protection**. I/O circuits handle **different voltage levels, drive strength, and noise isolation**. They are essential in designing **Testchips, SoCs, and ASICs** for efficient performance.

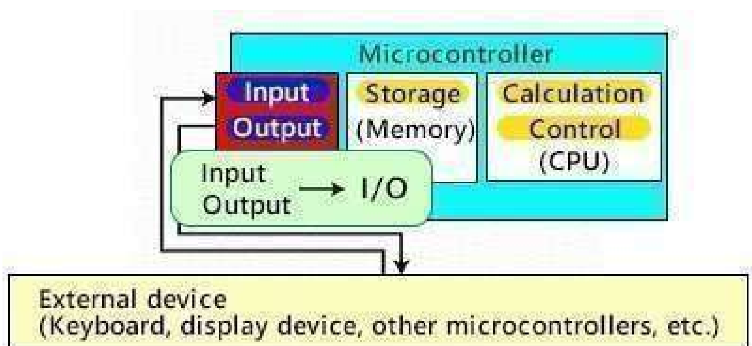

Fig-1.1 Input Output
Source:Toshib Electronic Devices & Corporation

1.2 WHY WE NEED IOs?

Input/Output (I/O) ports are a critical part of any chip, allowing it to interact with the external environment. These I/Os enable the chip to communicate, process signals, control devices, and manage power efficiently [1]. Below are the key reasons why I/Os are essential for chips:

Interfacing with External Devices – I/Os serve as a bridge between the chip and external components such as sensors, actuators, memory modules, and display systems. Without these ports, the chip would remain isolated and unable to perform any useful function in an embedded system [2].

Data Transfer & Communication – Chips need to exchange data with other devices, and I/Os provide this capability Various communication protocols such as UART, SPI, I2C, and parallel interfaces enable the transmission and reception of data, allowing chips to function in complex systems like computers, industrial automation, and IoT devices.

Noise Filtering & ESD Protection – External signals often contain noise that can interfere with a chip's operation. I/Os incorporate noise filtering techniques, such as capacitors and ferrite beads, to ensure signal integrity. Additionally, ESD protection mechanisms prevent electrostatic discharge from damaging sensitive components during handling and operation [3].

Level Shifting – In systems where components operate at different voltage levels, I/Os help in level shifting to ensure proper communication. For example, a 3.3V logic microcontroller can communicate with a 5V peripheral using level-shifting circuits integrated into the I/O design.

Control & Actuation – I/Os play a crucial role in controlling external devices such as LEDs, motors, relays, and speakers. By sending the appropriate signals through output ports, chips can regulate device behavior, enabling automation in industrial, automotive, and consumer applications.

1.3 TYPES OF IOs?

Input/Output (I/O) chips play a crucial role in interfacing digital systems with external components. These chips facilitate communication between processors, memory, and peripheral devices. I/O chips can be categorized into three main types: **Input I/O, Output I/O, and Bidirectional I/O Input I/O Chips:**

Receive data from external sources and send it to the processor.

Examples include ADCs (Analog-to-Digital Converters) and sensor interfaces. Used in applications like temperature monitoring and signal acquisition .

Output I/O Chips:

Send data from the processor to external devices.

Examples include DACs (Digital-to-Analog Converters), display drivers, and actuator controllers.

Commonly used in audio processing, motor control, and display systems [4].

Bidirectional I/O Chips:

Capable of both receiving and transmitting data.

Includes GPIO (General-Purpose I/O), communication interfaces (e.g., SPI, I2C, UART), and memory interface chips [5] .Bidirectional IO is shown in figure 1.2.

Used in embedded systems, networking, and data communication applications.

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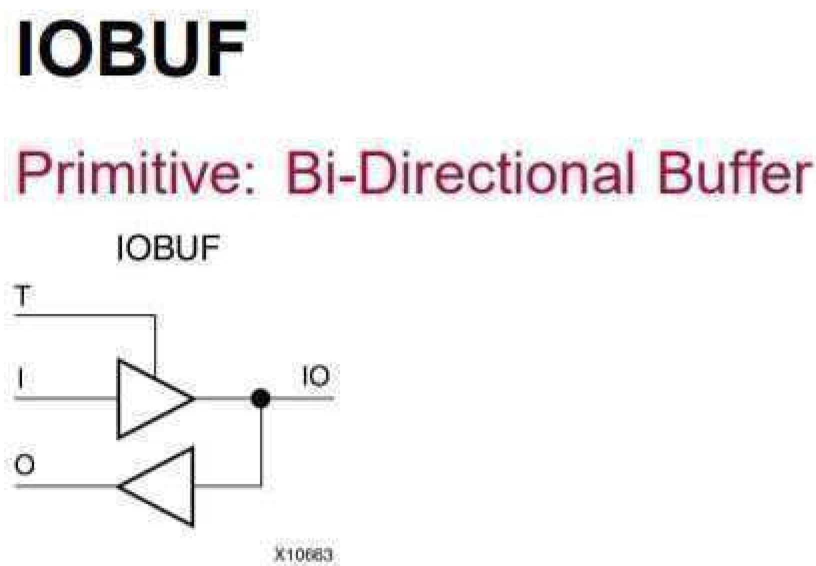

Fig-1.2 Bidirectional IO
Source:Support.xilinx.com

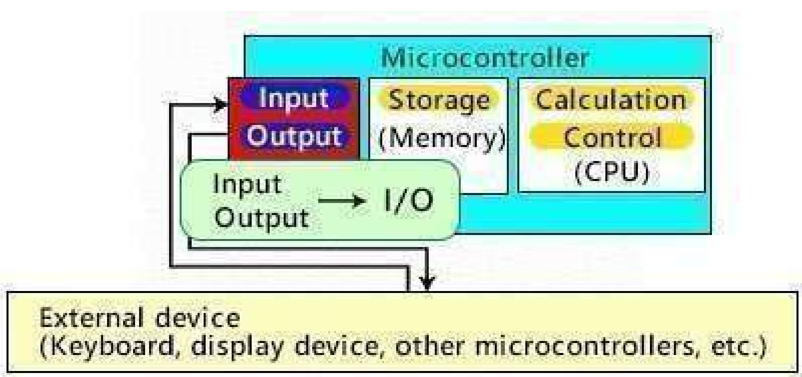

Fig-1.3 Input Port, output port
Sorce:Tohsib Electronic Device & Corporation

1.4 STANDARD IO CHIP COMPONENTS

A standard IO (Input/Output) chip is an essential element in modern integrated circuits, acting as the interface between the core logic of a chip and the external world. The design of an IO chip typically incorporates several specialized components to ensure robust and efficient communication, power distribution, and signal integrity[6].

Input Buffers: These are the first line of defense for external signals entering the chip. Input buffers condition the incoming signals by reducing noise and ensuring that voltage levels conform to the expected logic standards. Their primary function is to stabilize and protect the internal circuitry from potential damage or misinterpretation due to fluctuations in the external environment.

Output Buffers: Conversely, output buffers serve to drive signals from the chip's internal logic to external pins. They ensure that the output signals have sufficient strength and the proper voltage levels to be correctly interpreted by other devices or sub-systems.The design of output buffers is crucial because they ditrectly influence the speed and reliability of data transmission across the chip.

Supply Cells: These components are dedicated to managing the power distribution within the chip. Supply cells provide stable connections to the power (VDD) and ground (GND) rails, ensuring that all active elements of the chip receive a constant and reliable power supply. This is critical for maintaining performance consistency and reducing susceptibility to voltage fluctuations that could lead to erratic behavior or failure.

Filler and Corner Cells: Due to physical layout constraints, not every section of the chip occupied by active components. Filler cells are used to occupy these gaps, ensuring that power rails and signal paths remain continuous. Corner cells are specially designed to handle the unique geometries of chip corners, ensuring mechanical stability and proper electrical connectivity [7] .

Filler-Cuts: In some instances, specific design constraints require the deliberate "cutting" or isolation of certain regions within the IO ring. Filler-cuts are specially designed cells that create controlled breaks in the power or signal networks, accommodating layout requirements [8].

1.5 WHAT IS TESTCHIP?

A Testchip as shown in figure 1.4 is a specialized integrated circuit designed to validate and characterize various library cells—particularly Input/Output (IO) cells—under real-world conditions. By integrating a selection of these IO cells (e.g., bidirectional, I2C) on a single silicon die, the Testchip provides a focused environment where engineers can measure, analyze, and confirm that each cell meets its specified electrical and functional requirements [9]. This includes checking parameters such as voltage levels, current drive capability, timing behavior, and signal integrity. The goal is to ensure that, once these cells are used in a production chip, they will perform reliably and consistently, thus minimizing design risks and streamlining the development cycle[10]. Additionally, a Testchip enables correlation between simulation and silicon behavior, highlighting any discrepancies early. It aids in validating ESD robustness and latch-up immunity of IO cells under actual process conditions. Testchips also allow engineers to evaluate process variations across corners and their impact on IO performance. By including monitoring structures, they facilitate detailed debug during bring-up and testing phases. Overall, Testchips are a critical step in silicon- proven library development workflows [11].

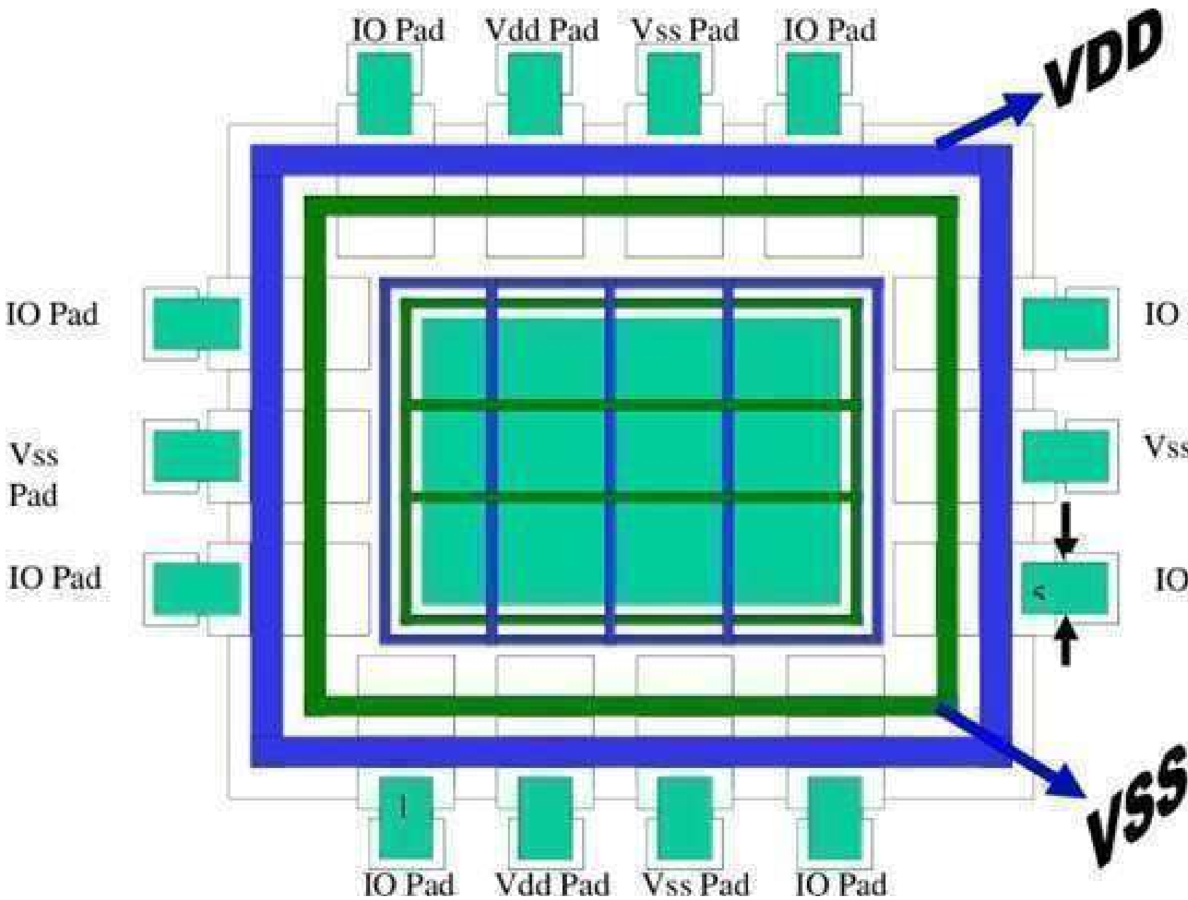

Fig-1.4 IO pads and IO ring
Source:- Power Grid Analysis in VLSI Design | Scemantic Scholar

1.6 WHY TESTCHIP?

Key Reasons for Using a Test Chip

Validation of Circuit Performance

Ensures that individual components, such as bi-directional I/O cells, I2C interfaces, and other analog/digital blocks, meet design specifications.

o Helps in verifying electrical characteristics such as voltage levels, current consumption, and signal integrity.

Process Characterization & Yield Analysis

o Used to analyze the behavior of circuits under different fabrication process conditions.

o Helps optimize semiconductor manufacturing processes to improve yield and reliability.

Early Detection of Design Flaws

o Identifies potential design issues before mass production, reducing costs and development time.

o Allows engineers to refine layouts, transistor sizing, and interconnections for optimal performance.[8].

Testing New Technology Nodes

o Essential for evaluating performance at smaller technology nodes (e.g., 7nm, 5nm, etc.).

o Helps in assessing power consumption, speed, and thermal behavior of new semiconductor materials.

Verification of I/O Interfaces

o Ensures that I/O cells, such as bi-directional pins and wire pads, function correctly under different operating conditions.

o Confirms compliance with industry standards like I2C, SPI, or USB [12].

1.7 WHAT IS LEVEL SHIFTER?

A level shifter is an essential circuit component used in electronic design to facilitate voltage level conversion between different power domains. It ensures proper communication between circuits operating at different voltage levels by translating signal voltages from one level to another. This is particularly crucial in modern semiconductor designs where different components may operate at varying voltage levels due to power efficiency, technology scaling, or compatibility reasons.

Applications

- Microprocessor and FPGA Interfacing – Used to interface logic circuits operating at different supply voltages.
- Low-Power Designs – Essential in power-efficient circuits where different blocks operate at optimized voltages.
- Mixed-Signal ICs – Ensures compatibility between analog and digital sections of integrated circuits.

LEVEL SHIFER CIRCUITRY

The circuit shown in figure 1.5 is a level shifter designed to translate signals from a lower voltage (VDD1) to a higher voltage domain (VDD2). It consists of a cross-coupled PMOS pair (MP1 and MP2) connected between VDD2 and two nodes that control the output stage. An NMOS transistor (MN1) receives the low voltage input signal (VIN at VDD1) and controls one of the cross-coupled nodes. An inverter is used in the path from VIN to control another NMOS transistor (MN2), which pulls the output node low when required. The output signal VOUT is referenced to VDD2, ensuring required. The output signal VOUT is referenced to VDD2, ensuring that the translated signal meets the higher voltage domain requirements. The cross-coupling of the PMOS transistors provides positive feedback, ensuring fast switching and robust logic level restoration during voltage translation [13].

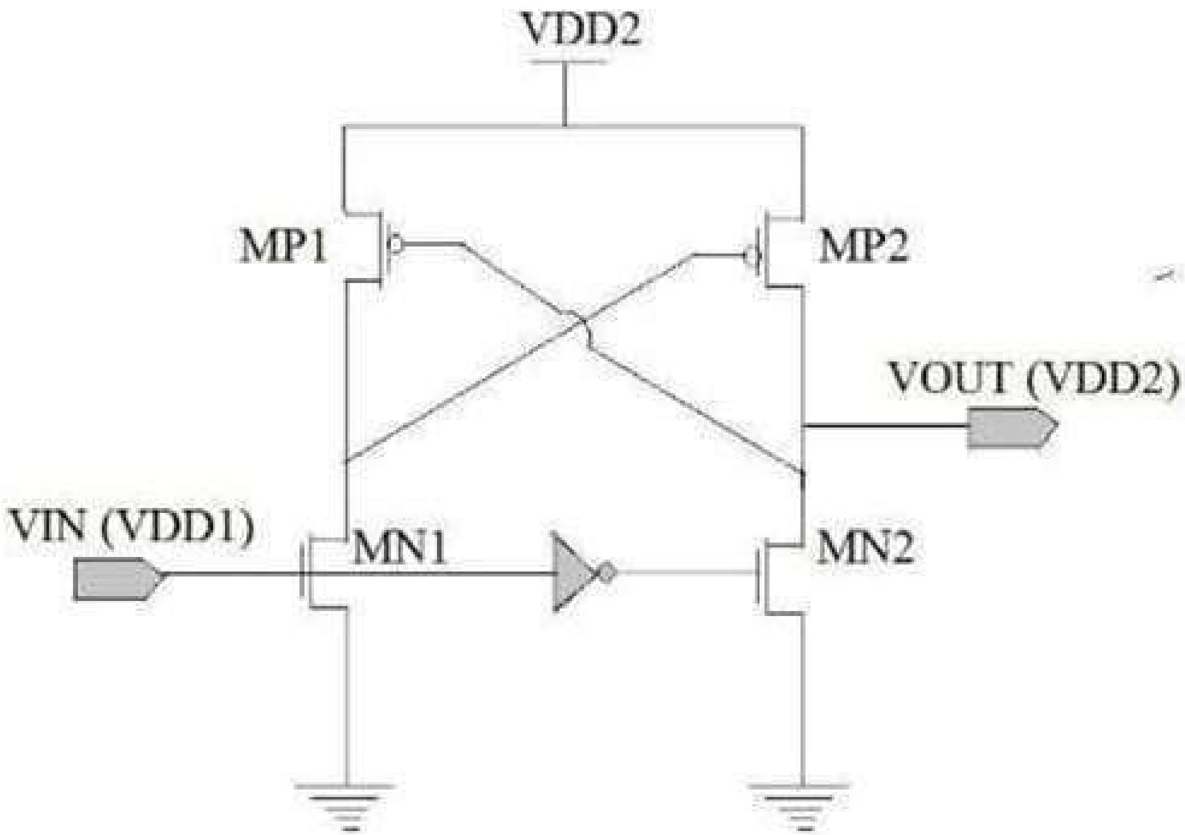

Fig-1.5 Low to high level shifter
Source:Research Gate

LEVEL SHIFTER OPEARTION

The cross-coupled level shifter translates a low voltage input signal (VIN at VDD1) to a higher voltage output signal (VOUT at VDD2). When VIN is high, MN1 turns ON, pulling one node of the cross-coupled PMOS pair low, which turns ON MP2, pulling VOUT high to VDD2. When VIN is low, MN1 is OFF, and through the cross-coupled action, MP1 turns ON, pulling VOUT low via MN2. The cross-coupled PMOS transistors ensure strong pull-up to VDD2, enabling reliable high-level output even when VIN operates at a lower voltage domain. The inverter in the path ensures correct polarity while also improving switching speed [13].

1.8 PRE SILICON VALIDATION PROCESS AND ITS IMPORTANCE

Pre-silicon validation is a critical phase in semiconductor design that ensures a circuit meets functional and manufacturing requirements before fabrication. It includes functional verification, electrical validation, and physical verification, with Design Rule Checking (DRC) and Layout vs. Schematic (LVS) being key steps in physical verification

DRC ensures that the IC layout follows foundry design rules, checking parameters like minimum width, spacing, and layer overlaps to prevent fabrication defects and yield loss. LVS verifies the electrical equivalence between the layout-extracted netlist and schematic, detecting missing or extra devices, incorrect connections, and unintended shorts [14].

Validating DRC and LVS pre-silicon prevents costly redesigns and ensures first-time silicon success.This is particularly crucial for GPIO Design in CMOS technology, where violations could lead to functional or reliability failures. By ensuring manufacturability and correctness, pre-silicon validation improves yield, performance, and overall chip reliability [14].

It also helps in identifying design bottlenecks and optimizing layout for area and power efficiency. Early detection of potential ESD and latch-up issues can be addressed during this stage to enhance IO robustness. Pre-silicon validation aids in correlating simulation results with expected silicon behavior under various process corners. It ensures that timing closure is achieved while respecting the physical constraints of the design. Overall, this phase reduces risks, shortens development cycles, and increases the confidence of achieving a successful tape out

CHAPTER 2

LITERATURE REVIEW

Voltage level shifters are essential components in modern integrated circuits, enabling communication between blocks operating at different supply voltages. Recent research has focused on optimizing level shifters for low-power, high-speed, and area-efficient performance, particularly for applications such as implantable medical devices, IoT sensors, and portable electronics [15].

Existing Level Shifter Designs

Conventional Level Shifters: Early designs, such as current-mirror-based level shifters, suffer from high static power consumption and slow switching speeds due to the lack of regenerative feedback between pull-up and pull-down networks [15].

Differential Cascade Voltage Switch (DCVS) Architectures: These designs improved speed and power efficiency by using cross-coupled pull-up networks. However, they often struggle with subthreshold operation and high dynamic power consumption during transition [15].

Recent Innovations: Advanced designs, such as those using regulated cross-coupled (RCC) pull-up networks, have achieved significant improvements in speed and power efficiency. For example, Kabirpour and Jalali (2019) proposed a level shifter capable of operating at input voltages as low as 80 mV with a power dissipation of 123.1 nW and a propagation delay of 23.7 ns. These designs, however, focus primarily on performance metrics (power, speed, area) and do not address reliability concerns such as electrostatic discharge (ESD) or charge device model (CDM) protection [15].

Traditional ESD protection techniques, such as diodes, RC-triggered clamps, and guard rings, are often added at the chip level but are not integrated into individual circuit blocks like level shifters.
There is limited research on layout-level ESD/CDM protection for level shifters, particularly in the context of subthreshold operation and ultra-low-power designs [15].

Research Gaps

1. Lack of Integrated CDM Protection: Existing level shifter designs do not incorporate CDM protection, making them vulnerable to failure in real-world applications.
2. Layout-Level CDM Techniques: Most designs neglect layout-level innovations for CDM robustness, such as optimized placement of protection devices and minimizing parasitic resistance/inductance.

CHAPTER 3

RESEARCH OBJECTIVES

3.1 OBJECTIVES

The objective of this work is to enhance the practicality and reliability of a level shifter layout by integrating GGNMOS (Gate-Grounded NMOS) for robust CDM (Charge Device Model) protection. This involves optimizing the layout to ensure effective ESD robustness while maintaining key performance metrics such as low power consumption, high speed, and small area(CMOS 28 nm Technology is used).

3.2 METHODOLOGY

The floor plan for the level shifter is structured to ensure efficient voltage transition, electrostatic discharge (ESD) protection, and device reliability. At the top, the GO1 device (1V0) is placed to handle the low-voltage operation before transitioning to higher voltage levels. Below GO1, CDM (Charged Device Model) protection circuitry is positioned to safeguardthe circuit from ESD-induced failures, ensuring robust protection for sensitive components.
At the bottom, the high-voltage (HV 5V0) devices are placed within a Deep N-Well (DNW) to provide proper isolation from the low-voltage domain. The Deep N-Well helps in reducing substrate noise coupling, preventing latch-up issues, and enhancing the reliability of high-voltage transistors. Additionally, the structured floor plan ensures efficient power routing, maintaining clear separation between VDDH (high voltage) and VDDL (low voltage) regions. Proper isolation rings and guard rings are incorporated to further improve thermal management and electrical integrity, ensuring that the design adheres to semiconductorlayout best practices for performance and manufacturability.

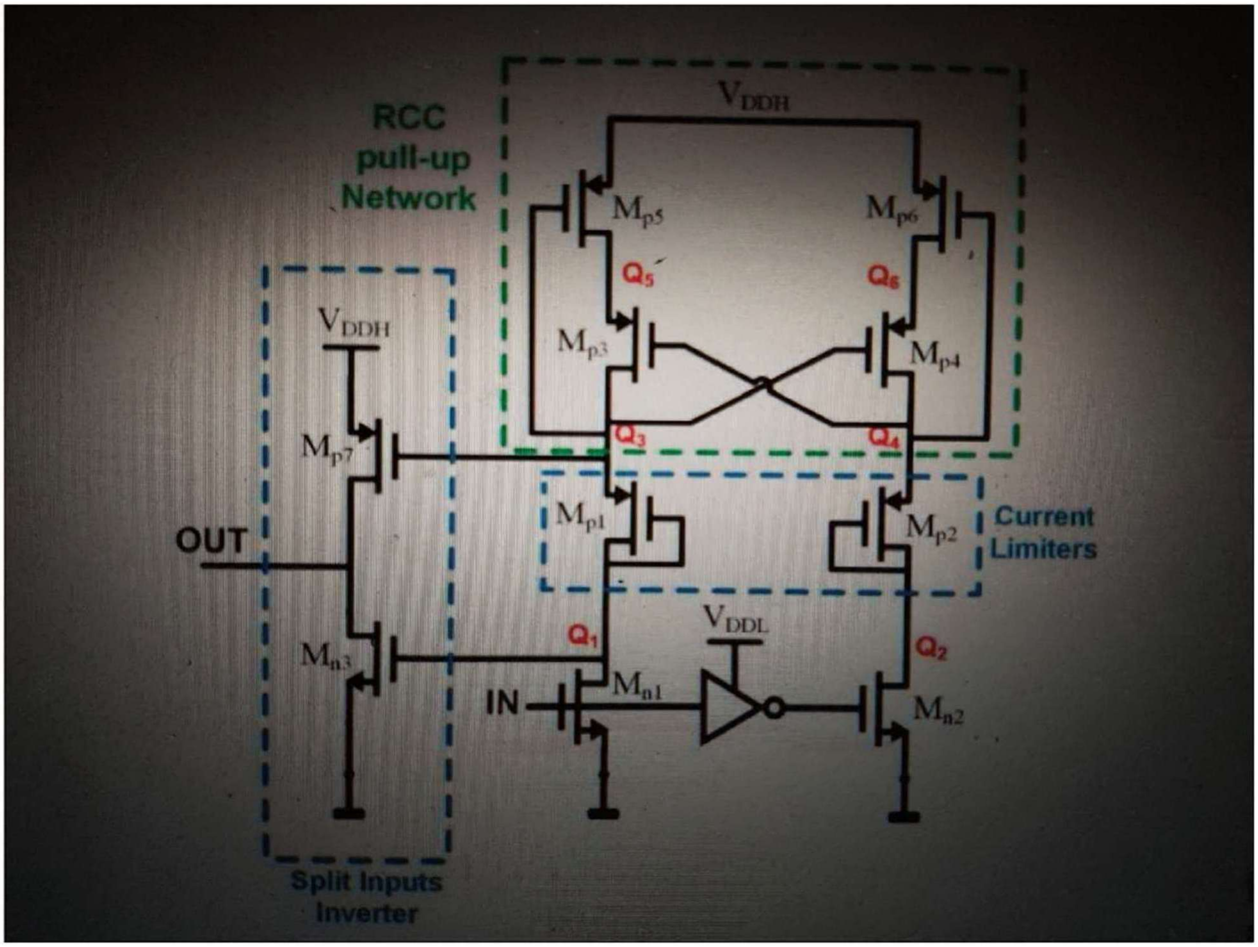

Fig-3.1 Level Shifter without CDM

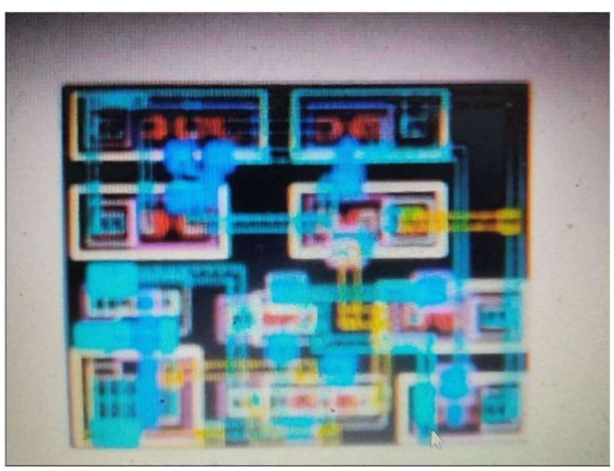

Fig-3.2 Level Shifter layout without CDM

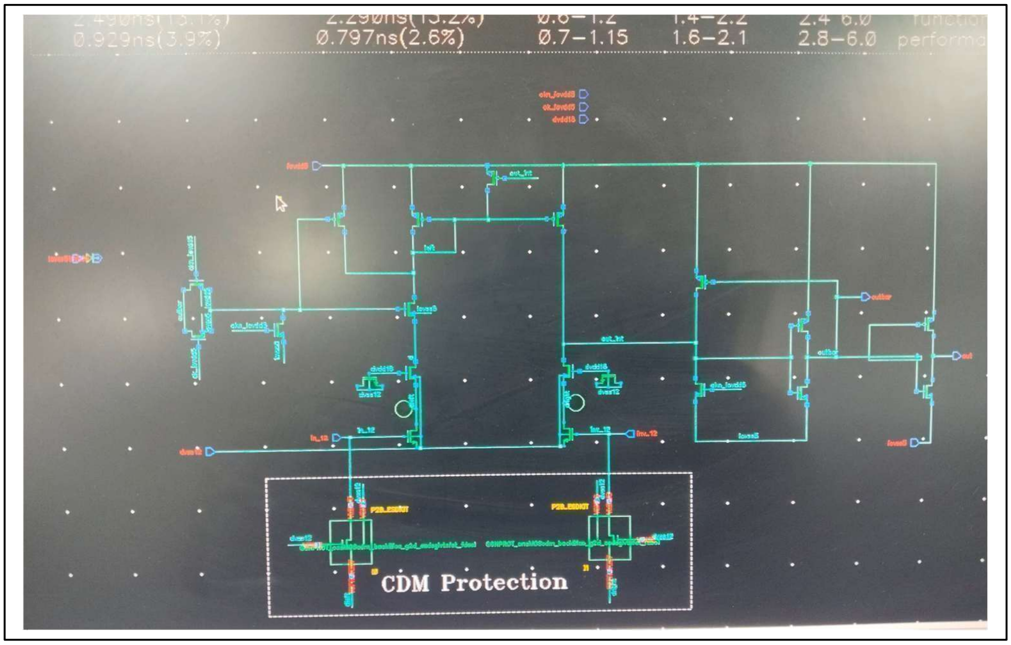

Fig-3.3 Level Shifter with CDM

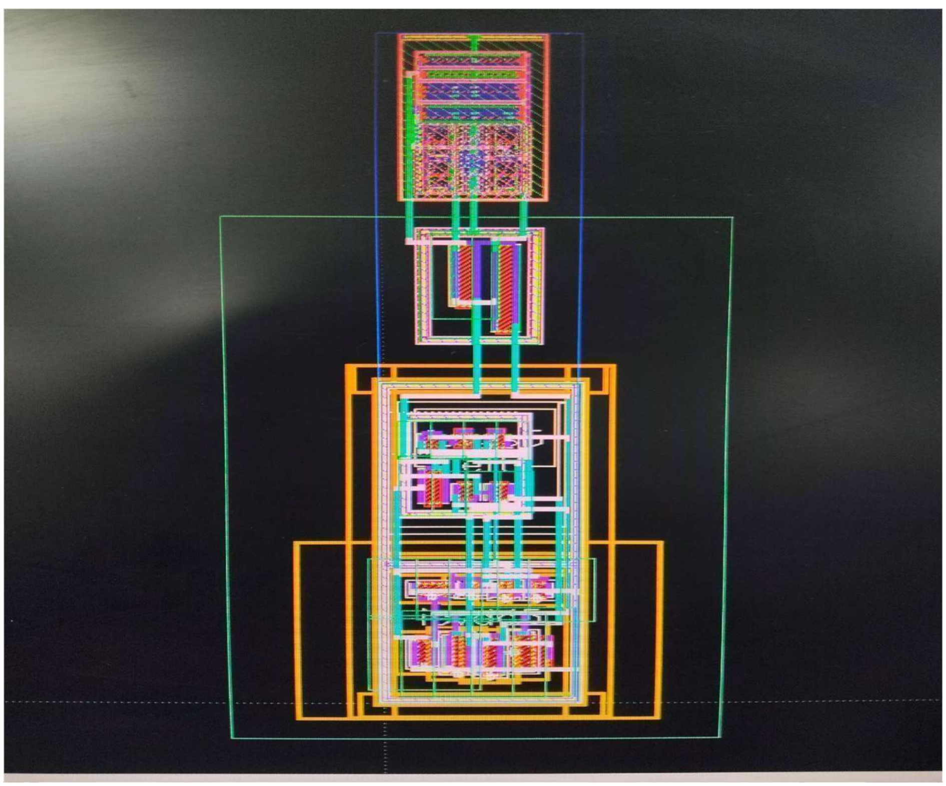

Fig-3.4 Level Shifter Layout With CDM

CHAPTER 4

RESULTS

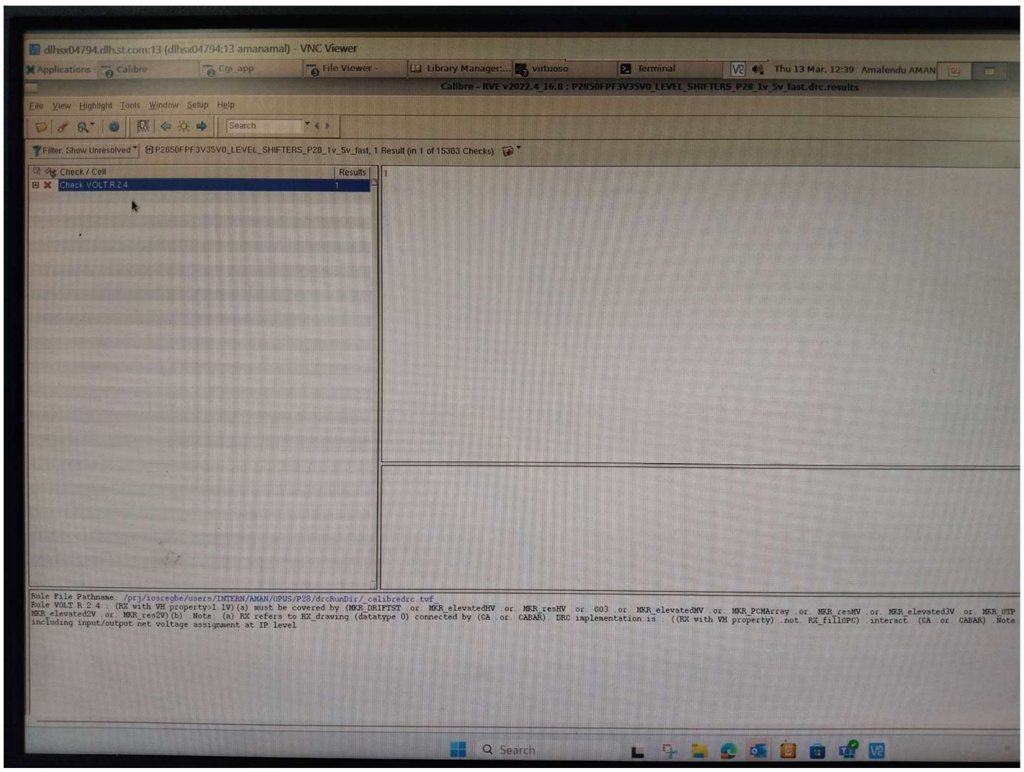

Fig-4.1 DRC of Level Shifter Layout With CDM

The level shifter layout as shown in figure 3.4 on cadence layout suite with integrated CDM protection was successfully designed and optimized for area efficiency and robustness. The layout occupies a total area of 63 µm², with the CDM protection devices (GGNMOS) placed close to the I/O pads to minimize parasitic resistance.

Multi-finger GGNMOS structures and guard rings were used to improve current handling and prevent latch-up. The layout passed all DRC checks, confirming compliance with the process technology's design rules. Integration with the IO ring was carefully planned to ensure minimal signal delay and noise coupling. This layout design is ready for pre-silicon validation and fabrication, with the CDM protection enhancing the IO ring's robustness against ESD events.

4.1 PARASITIC EXTRACTION AND MANAGEMENT FOR ESD PERFORMANCE ESTIMATED PERFORMANCE MATRICES

ESD Robustness:

Target CDM protection level: 250 V – 500 V (minimum industry standard)

Parasitic Capacitance:

Added clamps increase capacitance on IO nodes:

0.2 – 1 pF additional parasitic capacitance on the pad or IO net

Area Penalty:

ESD devices can take 3x the pad pitch area due to addition of clamp

EFFECTS OF LAYOUT PARASITICS

Increased Capacitance: ESD clamp diodes/SCRs in I/O pad inherently add junction capacitance, which loads the pad and reduces bandwidth, impacting high-speed signals.

Resistance and Signal Attenuation: Parasitic series resistance from metal interconnects and the clamp structure can lead to insertion loss and degraded signal integrity.

MANAGEMENT OF LAYOUT PARASITICS

Parasitic Capacitance: Select gated or STI diodes with smaller junction Area and minimize diode geometry.

Parasitic Resistance: Use multi-finger layouts with guard/ground rings to reduce series resistance and evenly distribute current .Optimize metal routing by adding wide local metal, avoid thin necks.

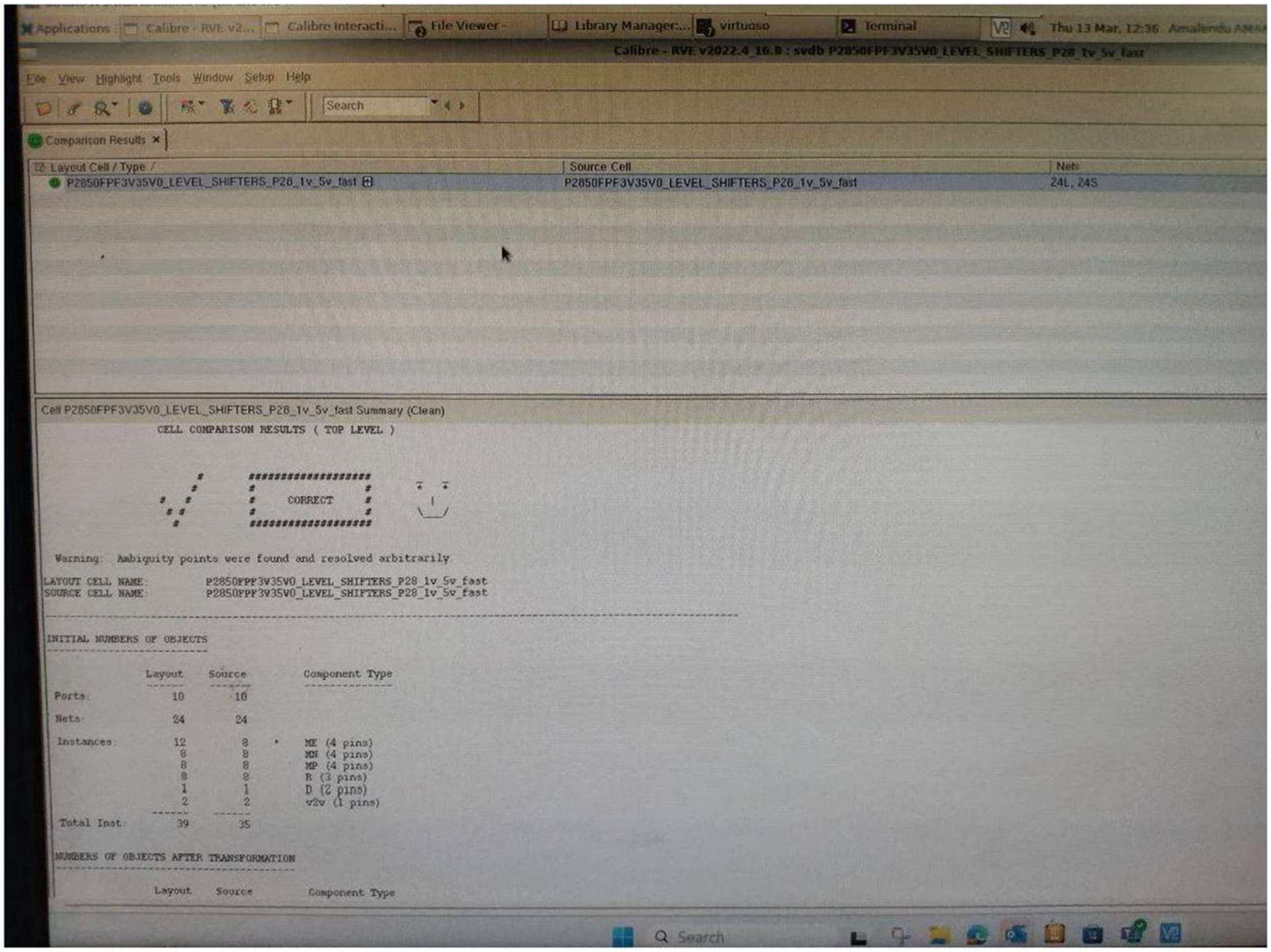

Fig-4.2 LVS is cleared

CHAPTER 5

CONCLUSION

In this thesis, the layout design of a level shifter with integrated CDM protection was successfully implemented and validated for pre-silicon test chip IO ring validation. The layout was optimized for area efficiency, robustness, and manufacturability, ensuring compliance with design rules and readiness for fabrication. Key achievements include:

- **DRC and LVS Compliance:** The layout passed all Design Rule Checks (DRC) as shown in figure 4.1, confirming its adherence to the process technology's design rules and ensuring manufacturability.Figure 4.2 shows all LVS is cleared.
- **CDM Protection**: As shown in Figure3.3 level shifter with CDM the integration of GGNMOS-based CDM protection enhances the level shifter's robustness against ESD events, making it suitable for real-world applications where ESD is a critical concern compared to level shifter without CDM as shown in Figure 3.3 and 3.2
- **Area Efficiency:** The compact layout design minimizes area overhead, ensuring seamless integration within the IO ring without significantly increasing the overall chip area. Pre- Silicon Validation: The layout is ready for pre-silicon validation, with its design ensuring minimal signal delay, noise coupling, and stable power delivery.
- **Reliability:**This work bridges the gap between performance optimization and reliability enhancement in level shifter design, contributing to the development of robust, high-performance IO rings for modern integrated circuits. Future work could focus on post-silicon validation and extending the design to other ESD protection techniques for emerging technologies.

It also demonstrates the effective application of layout best practices to achieve clean DRC and LVS closure. The design methodology followed can be extended to other voltage domains and process nodes with minimal adjustments. Emphasis was placed on maintaining signal integrity and reducing parasitic effects within the IO environment. The implemented level shifter layout serves as a silicon-proven reference for future IO library developments. Overall, this thesis strengthens the design flow from schematic to tape-out in mixed voltage IO systems.

CHAPTER 6

FUTURESCOPE

The successful implementation of the level shifter layout with CDM protection opens several avenues for future research and development. These include:

Parasitic-Aware ESD Co-Design: Perform a co-design of ESD protection devices and signal circuitry to accurately model parasitic capacitance and resistance, enabling compensation and layout improvements.

Material & Device Innovation: Investigate graphene-based ESD switches (gNEMS) and nano-electromechanical structures to reduce parasitic capacitance and die area, while maintaining robust CDM protection

Emerging Technologies: Extend the design to advanced process nodes (e.g., FinFET, GAAFET) and evaluate its performance and reliability in these technologies.

Integration with Other IO Components: Investigate the integration of the CDM- protected level shifter with other IO ring components (e.g., buffers, drivers) to develop a comprehensive ESD protection strategy for the entire IO ring.

Automation and Optimization: Develop automated tools for layout optimization and ESD protection placement to streamline the design process and improve efficiency.

System-Level ESD Integration: Develop methods to co-coordinate IC-level and board-level ESD protection, studying the interplay between on-chip clamps and external components to optimize current sharing during CDM event.

PVT and Reliability Enhancements: Design *fail-safe level shifters* with transparent back-gate control for PMOS transistors and ensure well-tie isolation under transient CDM conditions.

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