Analytical Modeling of Drain Current in the Subthreshold Region for Double-Gate Junctionless MOSFET

A

Dissertation

Submitted in the partial fulfillment of the requirements for the award of the degree

of

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in

VLSI DESIGN

Submitted by

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DECLARATION

I hereby declare that the work which is being presented in the dissertation entitled **"Analytical Modeling of Drain Current in the Subthreshold Region for Double-Gate Junctionless MOSFET"** in partial fulfillment of the requirement for the award of degree of M.Tech. (VLSI Design) at Electronics and Communication Engineering Department of Thapar University, Patiala, is an authentic record of my own work carried out under the supervision of Mr. Arun Kumar Chatterjee, Assistant Professor, ECED.

The matter presented in this dissertation has not been submitted in any other University/Institute for the award of my degree.

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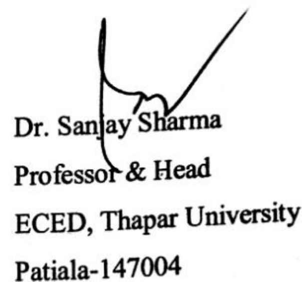

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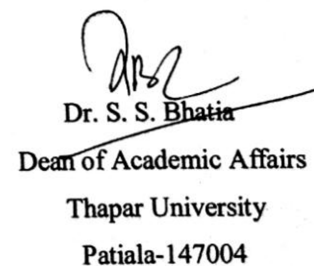

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ABSTRACT

The junctionless (JL) transistor is a resistor with uniform doping through the source, drain and channel regions. The fabricated junctionless device with a high content of impurity concentration within the channel and source/drain (S/D) regions requires no junctions and exhibits many advantages, such as the simplified flexible fabrication process, nearly ideal subthreshold slope (SS ≈ 60 mV/dec), high ON–OFF current ratio ($I_{ON}/I_{OFF} > 10^7$), low S/D series resistance, and small drain induced barrier lowering.

In this dissertation, an analytical drain current model has been obtained in the subthreshold region for a symmetrical Double Gate junctionless MOSFET. A 2-Dimensional analytical solution for Poisson's equation has been derived by using the surface potential based charge model considering only the mobile charge carriers. A relation between the surface potential and gate voltage has been obtained in terms of Lambert-W function. Using this surface potential, the mobile charge density in the channel region has been evaluated which is used in the Pao-Sah integral in order to obtain the drain current in the subthreshold region. The developed drain current model is being compared with the drain current model of a symmetric double gate (DG) MOSFET in the subthreshold region and it has been found that the developed model has better subthreshold slope than that of the double gate (DG) MOSFET.

Further, for 45 nm technologies the current-voltage characteristics of drain current model in subthreshold region for DG JL MOSFET and DG MOSFET are compared with the numerically simulated results obtained from Cogenda's Visual TCAD tool. The developed model is in good agreement with that of the simulation results.

ACRONYMS

IC	Integrated Circuit
MOSFET	Metal-Oxide-Semiconductor Field Effect Transistor
CMOS	Complementary Metal-Oxide-Semiconductor
ITRS	International Technology Roadmap for Semiconductors
SCE	Short Channel Effect
SOI	Silicon-On-Insulator
FET	Field Effect Transistor
DIBL	Drain-Induced Barrier Lowering
SS	Subthreshold Slope
PD-SOI	Partially Depleted SOI
FD-SOI	Fully Depleted SOI
DG JL MOSFET	Double Gate Junctionless MOSFET
DG MOSFET	Double Gate MOSFET

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Chapter 1

1 Introduction

1.1 Background

The central component of semiconductor electronics is the integrated circuit (IC), which combines the basic elements of electronic circuits such as transistors, diodes, capacitors, resistors and inductors on one semiconductor substrate. The two most important elements of silicon electronics are transistors and memory devices. For logic applications MOSFETs (Metal Oxide Semiconductor Field Effect Transistor) are used. MOSFETs have been the major device for ICs over the past two decades. With technology advancement and the high scalability of the device structure, silicon MOSFET-based VLSI circuits have continually delivered performance gain and/or cost reduction to semiconductor chips for data processing and memory functions.

The semiconductor industry has showcased a spectacular exponential growth in the number of transistors per integrated circuit for several decades, as predicted by Moore's law. The relentless evolution of electronics, information technology (IT), and communications has been mainly enabled by continuous progress in silicon-based CMOS technology. This continuous progress has been achieved particularly by its dimensional scaling. CMOS scaling has been the main driving force of Si technology advancement to improve both device density and performance. The reduction in cost-per-function has been steadily increasing the economic productivity with every new technology generation. Besides scalability, the other unique device properties such as input resistance, self isolation, zero static power dissipation, simple layout and process steps have made CMOS transistors as the main components of the current integrated circuits (ICs). Today CMOS ICs are found everywhere and indispensible in our daily life, ranging from portable electronics to telecommunications and transportation. A lot of research has gone into device design over the last thirty years, but the evolution of process technologies brings new obstacles as well as new opportunities to device

designers. The future technology trend predicted by ITRS (International Technology Roadmap for Semiconductors), physical dimensions and electrostatic limitations faced by conventional process and fabrication technologies will require the dimensional scaling of complementary metal-oxide-semiconductor (CMOS) devices within the next decade. However, as the device scaling continues for the 21st century, it turns out that the historical growth doubled circuit density and increased performance by about 40% every technology generation, followed by Moore's Law cannot be maintained only by the conventional scaling theory. As the CMOS technology scaling enters the nanometer regime, many serious problems called the small geometry effects or short channel effects (SCEs) comes into play. Some of these effects are such as increased leakage currents, difficulty on increase of on-current, large parameter variations, low reliability and yield, increase in manufacturing cost, and etc. In order to sustain the historical improvements, future technology scaling and to mitigate these small geometry effects to a considerable level, several strategies and new device structures have been researched and introduced. A few examples of those are; increasing electrostatic control over the channel by means of the continuous EOT scaling with high-k/metal gate stack, Multi-gate MOSFET structures, silicon-on-insulator(SOI), Strained Silicon (S-Si), Si nanowire/carbon nano tube FETs, etc. Many of these devices have been shown to have favorable device properties and new device characteristics, and require new fabrication techniques. These nanoscale devices have significant potential to revolutionize the fabrication and integration of electronic systems and scale beyond the perceived scaling limitations of traditional CMOS.

1.2 Future Technology Node Requirements

The factors or features to be distinguished between several logic technologies options are [1]:

a) High performance (HP):

The high performance corresponds to high complexity ICs that require high clock frequencies and at the same time can deal with high power consumption. The increase in clock frequency from one technology node to the next can be achieved at the device level by an improvement of the intrinsic switching time of a transistor of 17% per

year, while maintaining the transistor off state current to a value acceptable from power consumption point of view. The intrinsic switching time (τ) is the time needed by a transistor supplying on-state current to make the gate of an identical transistor switching from ground to the supply voltage

$$I = \frac{Q}{t} = \frac{CV}{\tau}$$

$$\tau = \frac{Q}{I} = \frac{CV}{I} \qquad (1.1)$$

where, $C \rightarrow$ Gate capacitance $V \rightarrow$ Supply voltage $I \rightarrow$ On-state current of the device. Therefore, the most efficient way to achieve enhanced performance is to scale the gate length of the transistor aggressively. Consequently, this will result in reduced gate capacitance while increasing the on-state current.

b) Low operating power (LOP):

The low operating power technology option mainly aims at relatively high performance mobile applications such as notebook computers. The key challenge is to increase the circuit performance while decreasing the dynamic power consumption as much as possible when the device is operating. The dynamic power consumption at the device level is a measure of power-delay product given by

$$P\tau = \frac{CV}{I} P = \frac{CV}{I} VI$$

$$P\tau = CV^2 \qquad (1.2)$$

$$P\tau \propto V^2$$

Therefore, the most efficient way to reduce the dynamic power consumption is thus to reduce the supply voltage as far as possible i.e. $V \downarrow \Rightarrow P\tau \downarrow \Rightarrow$ Dynamic Power Consumption (given by $0.5CV^2f$) decreases.

c) Low stand-by power dissipation (LSTPD):

The low stand-by power option is used for lower performance, low-cost consumer applications such as cellular phones. For such applications, the main concern or key issue is to continue increasing circuit performance while maintaining the power consumption as low as possible when the IC is idle. This static power consumption at

the transistor level is governed by the leakage current of the devices. Therefore, low stand-by power technology option requires very low transistor-off state currents as well as very low parasitic currents such as gate leakage.

1.3 Technology Scaling

The lateral geometric dimensions of devices and interconnects are reduced. This reduction in size is referred to as “scaling” of the geometric dimensions of the integrated circuits(IC). The minimum feature size is smaller size of object (e.g. gate length or interconnect line width) on IC. Over the past decades, the MOSFET has continually been scaled down in size; typical MOSFET channel lengths were once several micrometers, but modern integrated circuits are incorporating MOSFETs with channel lengths of tens of nanometers. As a consequence of this minimum feature size of ICs, the number of transistors has increased over time. The semiconductor industry maintains a “roadmap”, the ITRS, which sets the pace for MOSFET development. Historically, the difficulties with decreasing the size of the MOSFET have been associated with the semiconductor device fabrication process, the need to use very low voltages, and with poorer electrical performance necessitating circuit redesign and innovation (small MOSFETs exhibit higher leakage currents, lower output resistance, lower transconductance, interconnect capacitance, process variations, etc.)

1.3.1 Why MOSFET Scaling?

Smaller size of MOSFETs is highly desirable for several reasons. The primary reason to make transistors smaller in size is to integrate more and more number of devices in a given chip area. This results in a chip with the same functionality in a smaller area, or chips with more functionality in the same area. Since fabrication costs for a semiconductor wafer are relatively fixed, the cost per integrated circuits is mainly related to the number of chips that can be produced per wafer. Hence, smaller ICs allow more chips per wafer, reducing the price per chip. In fact, over the past 30 years the number of transistors per chip has been doubled every 23 years once a new technology node is introduced. For example the number of MOSFETs in a microprocessor fabricated in a 45 nm technology can well be twice as many as in a 65

nm chip. This doubling of transistor density was first observed by Gordon Moore ina1965 and is commonly referred to as Moore’s law. It is also expected that smaller transistors switch faster. For example, one approach to size reduction is a scaling of the MOSFET that requires all device dimensions to reduce proportionally. The main device dimensions are the channel length, channel width, andaoxide thickness. When they are scaled down by equal factors, the transistor channel resistance does not change, while gate capacitance is cut by that factor. Hence, the RC delay of the transistor scales with a similar factor. However, this has been traditionally the case for the older technologies, for the state-of-the-art MOSFETs reduction of the transistor dimensions does not necessarily translate to higher chip speed because the delay due to interconnections is more significant.

1.3.2 Moore’s Law

In the last forty-five years since 1965, the price of one bit of semiconductor memory has been droppeda100 million times. The primary engine that powered the proliferation of electronics is “miniaturization”. By making the transistors and interconnects smaller, more circuits can be fabricated on each silicon wafer and therefore each circuit becomes smaller. Miniaturization has also been responsible to the improvements in speed and power consumption in ICs. Gordon Moore made an empirical observation in 1965 that the number of devices on a chip doubles every 18 or 24 months or so as shown in Figure 1.1 [2]. This Moore’s law is succinct description of rapid and persistent trend of miniaturization. Each time minimum line width is reduced, we say that a new technology generation or a technology node is introduced.

Historically, new technology node is introduced every two-three years. The main reward for introducing new technology node is reduction of circuit size by half. (70% of previous line width means 50% reduction in area i.e., 0.7*0.7=0.49). Since nearly twice as many circuit can be fabricated on each wafer with each newer technology node, the cost per circuit reduced significantly which drive down cost of ICs. It’s intuitive that Moore’s Law cannot be sustained forever. However, predictions of size reduction limits due to material or design constraints, or even the pace of size reduction, have proven to

elude the most insightful scientists. The predicted ‘limit’ has been dropping at nearly the same rate as the size of the transistors. Further technology scaling requires major

Figure 1.1: Moore’s Law

changes in many areas, including: 1) improved lithography techniques and non-optical exposure technologies; 2) improved transistor design to achieve higher performance with a smaller dimension; 3) migration from a current bulk CMOS devices to novel materials and structures, including silicon-on-insulator, strained Si and novel dielectric materials; 4) circuit sensitivity to soft errors from radiation; 5) smaller wiring for on-chip interconnection of the circuits; 6) stable circuits; 7) more productive design automation tools; 8) denser memory cells, and 9) manageable capital cost. Metal gate and high-k gate dielectrics were introduced into production in 2007 to maintain technology scaling trend.

In addition, packaging technology needs to progress at rate consistent with on-going CMOS technology scaling at a sustainable cost/performance levels. This requires advances in I/O density, bandwidth, power distribution, and heat extraction. System architecture will also be required to maximize performance gain achieved in an advanced CMOS and packaging technologies.

1.3.3 CMOS Scaling Trends

For many years now, the shrinking of MOSFETs has been governed by the ideas of scaling. The basic idea is illustrated in the Figure 1.2 [3]: a large FET is scaled down by factor α to produce smaller FET with similar behavior.

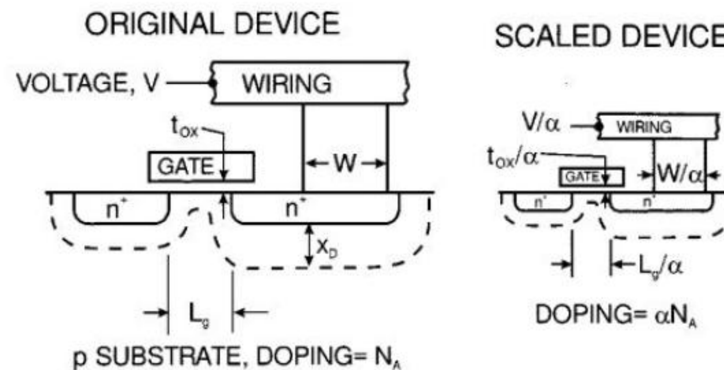


Figure 1.2: Schematic illustration of the scaling of Si technology by factor α

Device scaling is based upon simple principles; reducing the sizes of device and interconnect density, and power, speed and performance of transistors can be improved. Device scaling mainly focuses on

a) scaling of threshold voltage with feature size

b) scaling of gate oxide thickness with feature size

c) scaling of supply voltage with feature size

With technology scaling, MOS device channel length is reduced. When the dimensions of a MOSFET scaled down, both voltage level and gate-oxide thickness also reduces. The supply voltage V_{dd} has to be scaled down in order to keep the power consumption under control. The transistor V_{th} also had to be scaled down to maintain a high drive current and achieve performance improvement. In a given technology node, since the source-body and drain-body depletion widths are predefined based on the doping, rate at which barrier height increases as a function of distance from the source into the channel is a constant. Therefore, when channel length reduced, the barrier for majority carriers to enter the channel also reduces as shown in Figure 1.3 [5]. As a result threshold voltage reduces. In short channel transistors, the barrier height and therefore threshold voltage are strong function of drain voltage. Figure 1.3 [4] indicates,

the barrier reduces as the drain voltage is increased. Aggressive scaling of CMOS technology in recent years has reduced the silicon dioxide ($SiO2$) gate dielectric thickness below 20˚A. In 90 nm, the gate oxide consists of about 5 atomic layers equivalent to 1.2 nm in thickness. The thinner the gate oxide, higher the transistor current and consequently the switching speed. The scaling trend of power supply voltage (V_{dd}), threshold voltage (V_{th}), and gate-oxide thickness (T_{ox}) as function of CMOS channel length is shown in Figure 1.4 [5]. When V_{dd} is reduced towards shorter channel lengths, it becomes increasingly difficult to satisfy both the performance and the off current requirements. Trade-off between leakage current and circuit speed stems due to subthreshold no scalability. For this reason and for compatibility with the standardized power supply voltage of earlier generation systems, the general trend is that V_{dd} has not been scaled down in proportion to L and V_{th} has not been scaled down in proportion to V_{dd} as shown in Figure 1.4 [5]. When all of the voltages and dimensions are reduced by the scaling factor α and the doping and charge densities are increased by the same

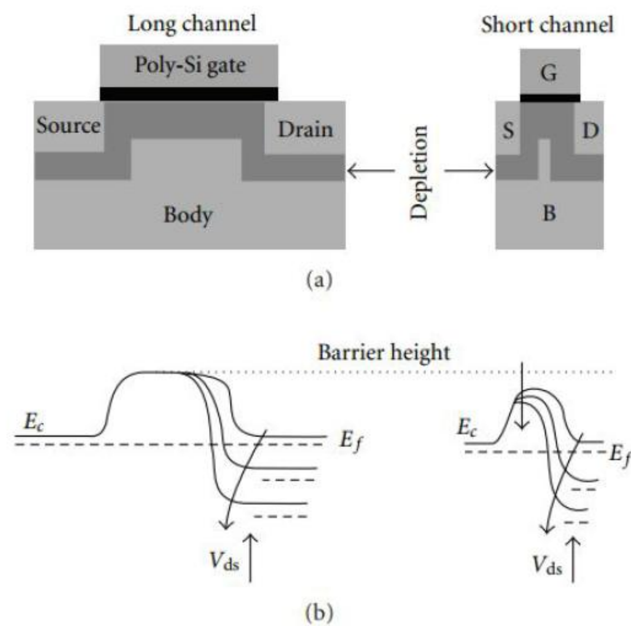


Figure 1.3: Channel length reduces the barrier for the majority of carriers to enter the channel

factor, the electric field configurations inside the FET remain the same as it was in the original device. This is called constant field scaling, which results in circuit speed increasing in proportion to the factor α and circuit density increasing as α2. These scaling relations are shown in the second column of Table 1.1 along with the scaling behavior of some of the other important physical parameters. α is the dimensional scaling parameter, ε is the electric field scaling parameter, and α_d and α_w are separate dimensional scaling parameters for the selective scaling case. α_d is applied to the device vertical dimensions and gate length, while α_w applies to the device width and the wiring.

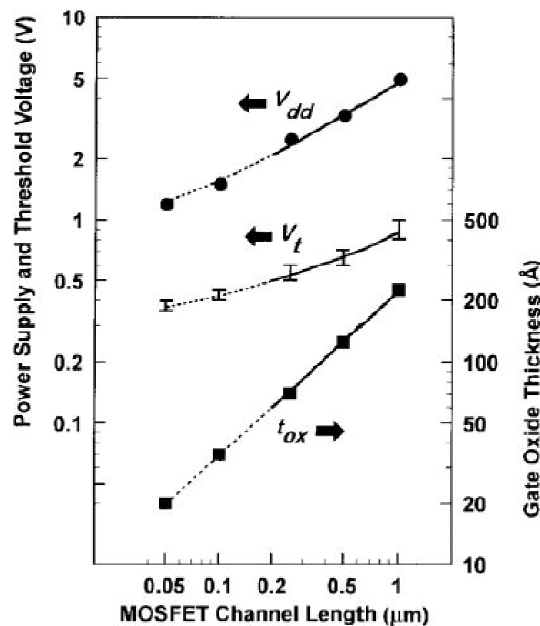


Figure 1.4: Scaling trend of power supply voltage (V_{dd}), threshold voltage (V_{th}), and gate-oxide thickness (T_{ox}) as a function of CMOS channel length

1.3.4 Challenges to Miniaturization of MOSFETs

Despite formidable challenges, however, many of those in the research community and industry do envision close variants of conventional microelectronic transistors becoming miniaturized into the nanometer-scale regime. For example, the International Technology Roadmap for Semiconductors (ITRS) [6], published by the Semiconductor Industry Association, projects that chips will be made from transistors with

Table 1.1: Technology Scaling Rules for Three Cases

Physical Parameter	$ConstantElectricField$ $ScalingFactor$	$GeneralizedScaling$ $Factor$	$GeneralizedSelective$ $ScalingFactor$
$ChannelLength,$ $InsulatorThickness$	$1/\alpha$	$1/\alpha$	$1/\alpha_d$
$WiringWidth,$ $ChannelWidth$	$1/\alpha$	$1/\alpha$	$1/\alpha_w$
$ElectricFieldindevice$	1	ε	ε
$Voltage$	$1/\alpha$	ε/α	ε/α_d
$On - Currentperdevice$	$1/\alpha$	ε/α	ε/α_w
$Doping$	α	$\varepsilon\alpha$	$\varepsilon\alpha_d$
$Area$	$1/\alpha^2$	$1/\alpha^2$	$1/\alpha_w^2$
$Capacitance$	$1/\alpha$	$1/\alpha$	$1/\alpha_w$
$GateDelay$	$1/\alpha$	$1/\alpha$	$1/\alpha_d$
$Powerdissipation$	$1/\alpha^2$	ε^2/α^2	$\varepsilon^2/\alpha_w\alpha_d$
$PowerDensity$	1	ε^2	$\varepsilon^2/\alpha_w\alpha_d$

major features (gate lengths) of 70 nm in the year 2010. Individual working transistors with 40 nm gate lengths have already been demonstrated in silicon. Transistors with gate lengths as small as 25 nm have been made using Strained Silicon (S-Si). However, to provide points of reference for contrasting nanoelectronic devices with scaled-down FETs, a few of the obstacles to FET scaling are simply enumerated below, in increasing order of their intractability [7].

a) High electric fields:

Due to bias voltage being applied over very short distances, one can cause avalanche breakdown by knocking large numbers of electrons out of the semiconductor at high energies, thus causing current surges and progressive damage to devices. This may remain problem in nanoelectronic devices made from bulk semiconductors.

b) Heat dissipation:

Heat dissipation of transistors (and other switching devices), due to their necessarily limited thermodynamic efficiency, limits their density in circuits, since overheating can cause them to malfunction. This is likely to be a problem for any type of densely packed nanodevices.

c) Vanishing bulk properties and non-uniformity of doped semiconductors on small scales:

This can only be overcome either by not doping at all (accumulating electrons purely using gates, as has been demonstrated in a GaAs heterostructure) or by making the dopant atoms form regular array.

d) Shrinkage of depletion regions:

Shrinkage of depletion regions until they are to thin to prevent quantum mechanical tunneling of electrons from source to drain when the device supposedly is turned off. The function of nanoelectronic devices is not similarly impaired, because it depends on such tunneling of electrons through barriers.

e) Shrinkage and unevenness of the thin oxide layer beneath the gate:

This prevents electrons from leaking out of the gate to the drain. This leakage through thin spots in the oxide also involves electron tunneling. Long ago, MOSFETs were big and could be described via drift currents and carrier control via the gate capacitance. Now MOSFETs are small in order to increase their operation speed. Pushing the dimensions of the gate length down influences the electrostatics of the devices. In order to preserve the electrostatic integrity of the MOSFET scaling has proceeded in a controlled way: $L_g \downarrow$ has to go together with $t_{ox} \downarrow$, $N_A \downarrow$, $t_{si} \downarrow$, $V_{dd} \downarrow$ and $W \downarrow$.

Some of the short channel effects resulting due to the scaling of device dimensions can be illustrated as follows [8]:

a) Drain induced barrier lowering (DIBL) and punch through:

When the depletion regions surrounding the drain extends to the source, so that the two depletion layer merge, punch through occurs. Punch through can be minimized with thinner oxides, larger substrate doping, shallower junctions, and obviously with longer channels. The current flow in the channel depends on creating and sustaining an inversion layer on the surface. If the gate bias voltage is not sufficient to invert the

surface ($V_{gs}<V_{T0}$), the carriers (electrons) in the channel face a potential barrier that blocks the flow. Increasing the gate voltage reduces this potential barrier and, eventually, allows the flow of carriers under the influence of the channel electric field. In small-geometry MOSFETs, the potential barrier is controlled by both the gate-to-source voltage Vgs and the drain-to-source voltage V_{ds}. If the drain voltage is increased, the potential barrier in the channel decreases, leading to drain-induced barrier lowering (DIBL). The reduction of the potential barrier eventually allows electron flow between the source and the drain, even if the gate-to-source voltage is lower than the threshold voltage. The channel current that flows under this conditions ($V_{gs}<V_{T0}$) is called the sub-threshold current.

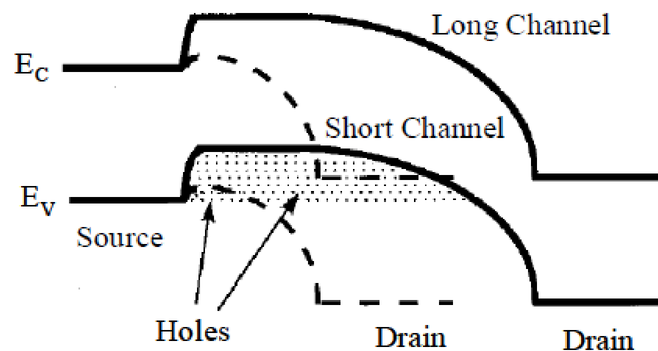


Figure 1.5: DIBL effect in short channel MOSFETs

b) Surface Scattering:

As the channel length becomes smaller due to the lateral extension of the depletion layer into the channel region, the longitudinal electric field component ε_V increases, and the surface mobility becomes field-dependent. Since the carrier transport in a MOSFET is confined within the narrow inversion layer, and the surface scattering (that is the collisions suffered by the electrons that are accelerated toward the interface by ε_X) causes reduction of the mobility, the electrons move with great difficulty parallel to the interface, so that the average surface mobility, even for small values of ε_V, is about half as much as that of the bulk mobility.

c) Velocity Saturation:

The performance of short-channel devices is also affected by velocity saturation, which reduces the transconductance in the saturation mode. At low ε_V, the electron drift velocity v_{de} in the channel varies linearly with the electric field intensity. However, as ε_V increases above 104 V/cm, the drift velocity tends to increase more slowly, and approaches a saturation value of v_{de} (sat)=107 cm/s around ε_V =105 V/cm at 300 K. Note that the drain current is limited by velocity saturation instead of pinch off. This occurs in short channel devices when the dimensions are scaled without lowering the bias voltages.

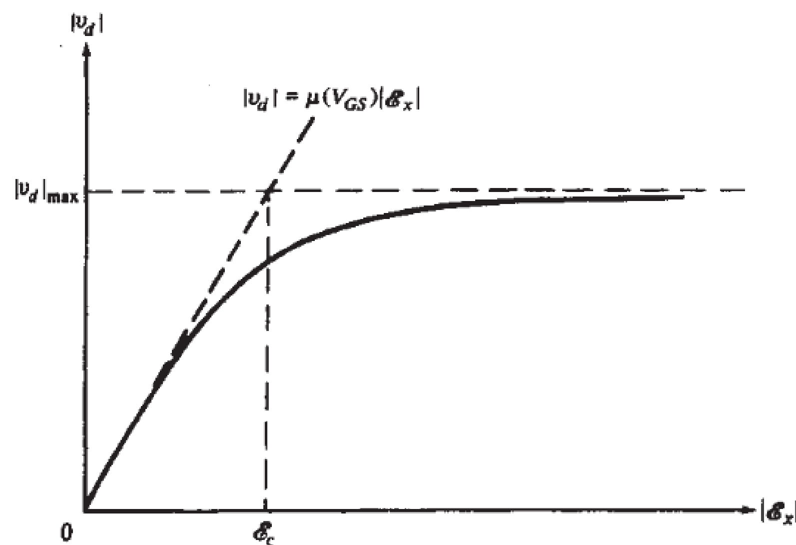


Figure 1.6: Magnitude of carrier velocity in inversion layer vs. magnitude of longitudinal component of electric field [9]

d) Impact Ionization:

Another undesirable short-channel effect, especially in NMOS, occurs due to the high velocity of electrons in presence of high longitudinal fields that can generate electron-hole (e-h) pairs by impact ionization, that is, by impacting on silicon atoms and ionizing them. It happens as follow normally, most of the electrons are attracted by the drain, while the holes enter the substrate to form part of the parasitic substrate current. Moreover, the region between the source and the drain can act like the base of an n-p-n

transistor, with the source playing the role of the emitter and the drain that of the collector. If the forementioned holes are collected by the source, and the corresponding hole current creates a voltage drop in the substrate material of the order ofa6V, the normally reversed-biased substrate-source p-n junction will conduct appreciably. Then electrons can be injected from the source to the substrate, similar to the injection of electrons from the emitter to the base. They can gain enough energy as they travel toward the drain to create new e-h pairs. The situation can worsen if some electrons generated due to high fields escape the drain field to travel into the substrate, there by affecting other devices on a chip.

e) Hot Electrons:

Another problem, related to high electric fields, is caused by so-called hot electrons. This high energy of electrons can enter the oxide, where they can be trapped, giving rise to oxide charging that can accumulate with time and degrade the device performance by increasing V_{TH} and affect adversely the gate's control on the drain current.

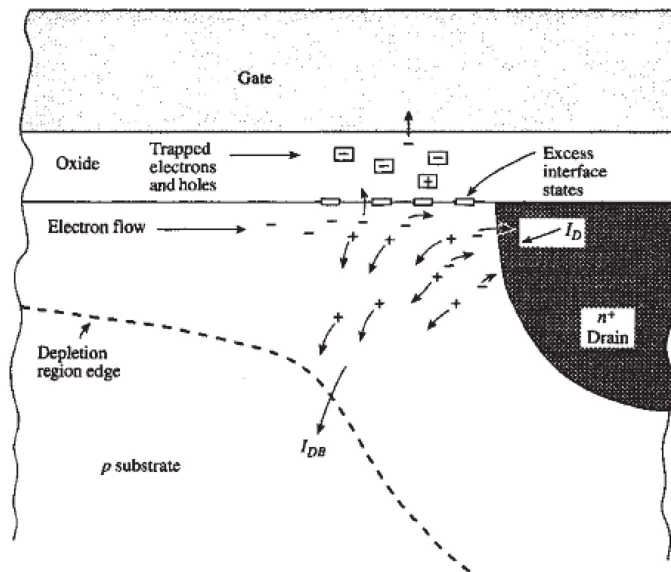


Figure 1.7: Hot electron carrier effect in a region of high longitudinal electric field in inversion channel of MOSFET [9]

1.4 Organization of the Dissertation Work

Chapter-1 Introduction: -

This chapter starts from Moore's law and then discusses about scaling in bulk MOSFETs, its challenges and their solution in the form of advance MOSFETs. Then,it looks upon the major SCEs in conventional short channel devices.

Chapter-2 Literature Survey: -

This chapter starts with small introduction about need of DG JL MOSFETs devices and then tells about DG JL MOSFETs, its advantages.

Chapter-3 Two Dimensional Subthreshold Region Drain Current Modeling of Symmetrical Double-Gate Junctionless MOSFET: -

In this chapter 2D potential function is derived and then a relation between surface potential and gate voltage is obtained for the DG JL MOSFETs in terms of Lambert-W function. Next, these derived expressions are used to model drain current in the subhtreshold region.

Chapter-4 Results and Discussion: -

This chapter contains the comparison of the device simulation results of the DG JL MOSFETs from Cogenda's TCAD tool with the model results.

Chapter-5 Conclusion and Future Scope: -

A brief conclusion and possible improvements have been discussed in this chapter.

Chapter 2

2 Literature Survey

2.1 Motivation

In a conventional, bulk-silicon micro-circuit, the active elements are located in a thin surface layer (less than 0.5 μm of thickness) and are isolated from the silicon body with a depletion layer of a p-n junction. The leakage current of this p-n junction exponentially increases with temperature, and is responsible for several serious reliability problems. Excessive leakage currents and high power dissipation limit the operation of micro-circuits at high temperatures. Parasitic n-p-n and p-n-p transistors formed in neighboring insulating tubs can cause latch-up failures and significantly degrade circuit performance.

Silicon-on-insulator (SOI) technology employs a thin layer of silicon (tens of nanometers) isolated from a silicon substrate by a relatively thick (hundreds of nanometers) layer of silicon oxide. The SOI technology dielectrically isolates components and in conjunction with the lateral isolation, reduces various parasitic circuit capacitances, and thus, eliminates the possibility of latch-up failures. Figure 2.1 [10] shows the cross-section of the bulk and SOI MOS devices. As shown in the Figure 2.1 [10], owing to the buried oxide isolation structure, SOI technology offers superior devices with excellent radiation hardness and high device density. SOI devices are more suitable with their steeper subthreshold slope (SS) which facilitates scaling of the threshold voltage for low-voltage low-power applications. Depending on the thickness of the silicon layer, MOSFETs will operate in fully depleted (FD) or partially depleted (PD) regimes. When the channel depletion region extends through the entire thickness of the silicon layer, the transistor operates in a FD mode. PD transistors are built on relatively thick silicon layers with the depletion depths of the fully powered MOS channel shallower than the thickness of the silicon layer. The PD-SOI devices have many advantages like the fabrication process of PD-SOI devices is totally compatible with bulk

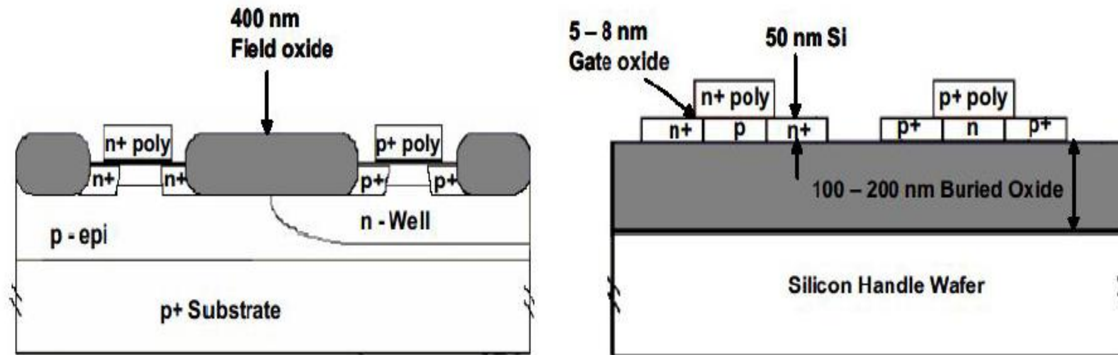


Figure 2.1: Cross-sectional view of the bulk-Si (left) and SOI (right) CMOS devices

silicon technology while fabrications of FD-SOI devices require development of ultra thin body, and, therefore needs more sophisticated technology. Hence, the design of bulk Si devices can be easily transferred to PD-SOI technology. Also V_T in PD-SOI is relatively less sensitive to the uniformity in the Si-film thickness while in FD-SOI device, V_T depends on Si film thickness and it is difficult to control the thickness of the ultra thin film body. As a result the film thickness becomes non-uniform across the surface. In spite of so many benefits, PD-SOI devices exhibit certain undesirable effect known as "kink effect". During the past few decades, excellent high-speed and performance have been achieved through improved design, use of high quality material and shrinking device dimensions. However, with the reduction of channel length, control of short-channel effects is one of the biggest challenges in further down-scaling of the technology. The predominating short-channel effects are a lack of pinch-off and a shift in threshold voltage with decreasing channel length as well as drain induced barrier lowering (DIBL) and hot-carrier effect at increasing drain voltage. Therefore, to reduce this short channel effects to a greater extent a new device structure called Junctionless (JL) Transistors have been demonstrated. Junctionless devices with a uniform doping concentration and type throughout the channel and source/drain extensions overcome the challenges faced by the conventional nano devices [11]. The schematic diagram of DG-JL MOSFET is shown in the Figure 2.2. JL MOSFETs have extremely low leakage current and simple fabrication process and are less susceptible to SCEs when compared with classical inversion-mode devices. However, the high doping concentration in the

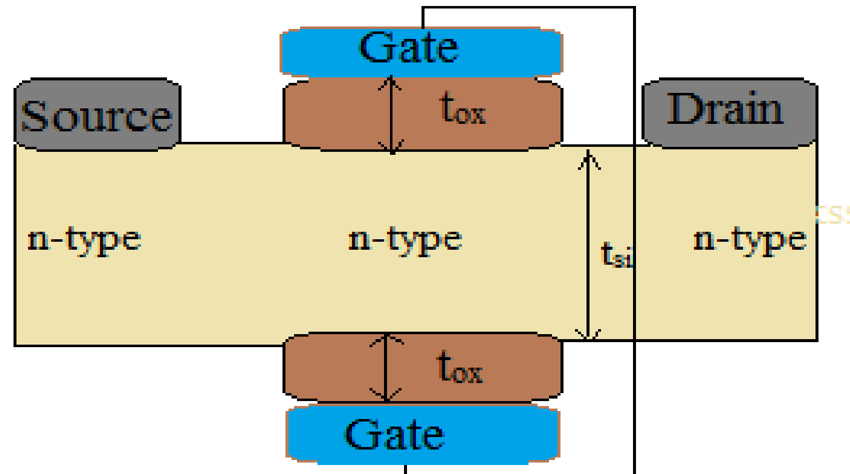


Figure 2.2: Schematic diagram of Double Gate (DG) JL MOSFET.

channel reduces carrier mobility which results in lower drive current and transconductance (*Gm*) of JL MOSFETs.

2.2 Junction-Less Transistor (JLT)

Some of the process challenges for scaling the CMOS devices can be reduced by a device which does not need any junctions and this is the main advantage of junctionless transistor. Unlike the conventional MOSFET, JLTs [12] have heavy channel doping and is fully depleted in the OFF state. For this purpose, a gate metal which has a large workfunction difference to that of the channel is needed. Gate bias need to be applied to bring the channel out-of depletion and to see a conduction between source and drain. As there is a single semiconducting silicon bar with uniform doping from the source to channel, it can be modeled as a resistor whose resistance can by modulated by the gate. However, for a reasonable conductance between source and drain, the doping of the semi-conductor bar need to be very high. On the other hand, the depletion width in a heavily doped semiconductor is very small and this demands an ultra thin silicon body for a JLT.

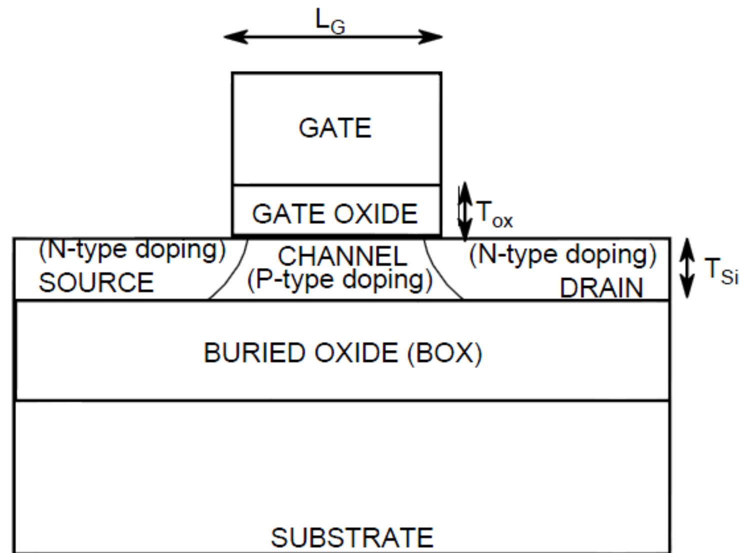


Figure 2.3: Schematic of an extremely thin silicon on insulator (ETSOI) FET.

2.2.1 Theory of junctionless transistors

The schematic representation of junctionless transistor is shown in Figure 2.4. It can be seen that for an n-channel operation [13], the source, channel and drain are of n-type doping and the gate is of a p-type workfunction (& 5.1eV). Since the workfunction difference between the n-type channel and the p-type gate is of & 1eV, there is a depletion in the channel, where the depletion is decided by the doping of the channel region (thin depletion width for high doping and vice-versa). Channel can be made fully depleted by choosing an extremely thin channel and low channel doping in the range of 10nm and 10^{19} respectively. Once the channel is fully depleted, the current between the source and drain becomes very small. The current is very small when the gate is at 0V. Also, it can be seen in the band diagram (Figure 2.5) for V_{GS} =0V [14], that there exists a barrier between the source and the channel due to depletion of carriers in the channel. There exists a similar barrier between the source and channel, even in the conventional MOSFET. Once a positive gate bias is applied (note this is for an n-channel operation), the channel is now brought out of depletion and the barrier between the source and channel is reduced. This results in a high drain current for a non-zero drain bias. When the voltage applied at the gate is approximately equal to the workfunction difference

between the gate and channel, the device is brought into the flat-band condition and the transistor is said to be turned ON.

However, all this is valid when the channel thickness is less than its depletion width, else, the device will not be turn OFF at zero gate bias. For example, if the depletion width calculated isa10nm and the channel thickness is 20nm, the device will conduct due to the drain to source bias, even for a zero gate bias, i.e., the device cannot be turned OFF. Hence it is important to maintain a very thin semiconductor thickness in junctionless transistors to have proper switching characteristics [15].

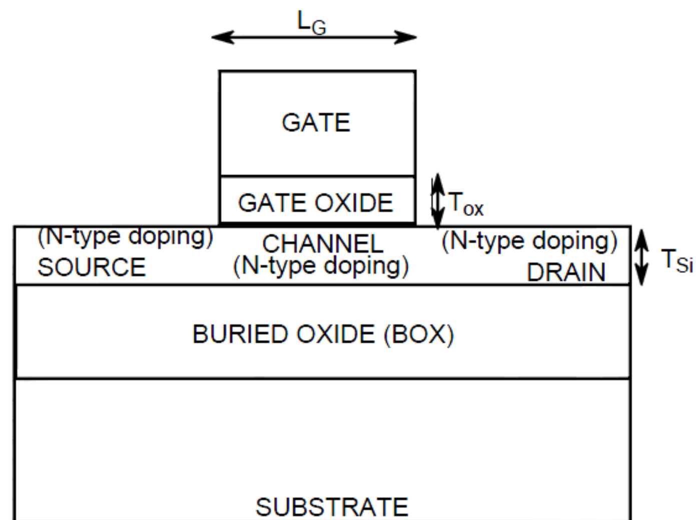


Figure 2.4: Schematic of an SOI junctionless transistor.

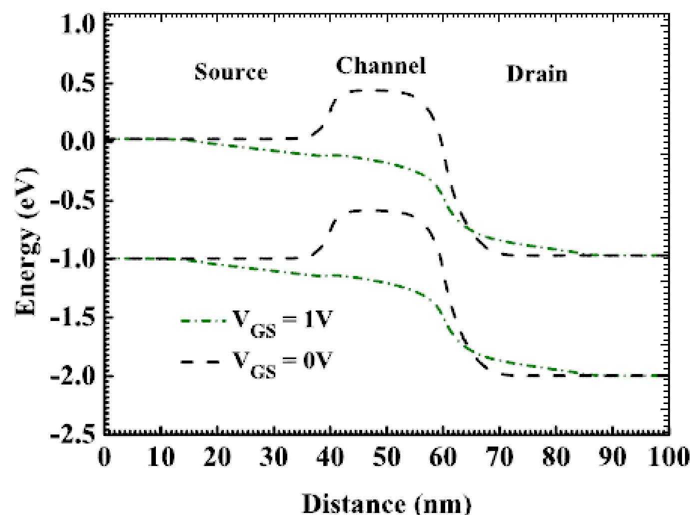


Figure 2.5: Lateral band diagram on JLT both on the ON and OFF states.

2.3 Double Gate Junctionless (DG JL) MOSFET

The down scaling of the channel length in MOSFETs poses increasingly difficult challenges as leakage current and short-channel effects increase due to the decreasing control efficiency of the gate on the channel. In a MuGFET, the gate electrode is wrapped around a silicon nanowire, forming a multigate structure with excellent control of the channel potential, which allows one to fully deplete the channel region. In very-short-channel devices, the formation of ultra sharp source and drain junctions is quite a challenge and imposes drastic conditions on doping techniques and thermal budget. The JL transistor is a resistor with uniform doping. The doping concentration is constant through the source, channel, and drain [16]. The absence of doping concentration gradient eliminates diffusion of impurities and the problem of sharp doping profile formation altogether. Any increase of temperature induces variations of the electrical parameters of MOS devices (e.g., threshold voltage shift, increase of leakage current, and reduction of mobility [17].)

Recently, a double-gate (DG) junctionless (JL) field effect transistor (DG JL FET) has been reported [16-18] as a promising candidate for future technology nodes. Technically, all undoped or lightly counter-doped DG MOSFETs are junctionless if the doping in the channel is of the same type as the source and the drain. What distinguishes the recently developed junctionless MOSFET is that the channel is heavily doped of the same type and to a similar magnitude of concentration as the source and the drain. The fabricated junctionless device with a high content of impurity concentration within the channel and source/drain (S/D) regions requires no junctions and exhibits many advantages [19-22], such as the simplified flexible fabrication process, nearly ideal subthreshold slope (SS ≈ 60 mV/dec), high ON–OFF current ratio ($I_{ON}/I_{OFF} > 10^7$), low S/D series resistance, and small drain induced barrier lowering. Moreover, the JL transistor shows many interesting characteristics, like conductance oscillations at low temperature [23] and high temperature behavior [24]. The junctionless transistor (JNT) is a heavily-doped SOI resistor with an MOS gate that controls current flow. Doping concentration is constant and uniform throughout the device and typically ranges from 10^{19} and 10^{20} cm^{-3}.aThe device features bulk conduction instead of surface channel

conduction. Figure 2.6 shows the device structure of the double gate junctionless MOSFET.

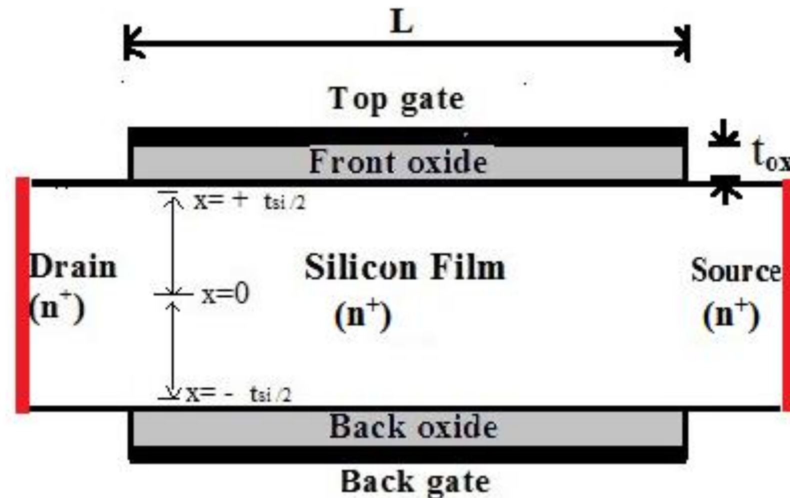


Figure 2.6 Structural view of double gate junctionless MOSFET

The operational principle of an n-channel DG JL FET is different from that of a standard n-channel DG FET. In the subthreshold region [see Figure 2.7(a)], a highly doped channel is fully depleted; hence, it can hold a large electric field.

By increasing gate voltage, the electric field in the channel reduces until a neutral region is created in the center of the channel. At this point, it is possible to define threshold voltage because bulk current starts to flow through the center of the channel [see Figure 2.7(b)]. Then, by further increasing the gate voltage, depletion width reduces until a completely neutral channel is created [see Figure 2.7(c)]. This occurs when the gate voltage equals flat band voltage. At the onset of this condition, the bulk current reaches its maximum value. Thereafter, by increasing the gate voltage further, negative charges accumulate on the surfaces of the channel [see Figure 2.7(d)]. These charges result in surface current, which is similar to the current in a standard n-channel DG FET. However, the surface current flows at a gate voltage that is much higher than the threshold voltage for the bulk current [22]. Hence, the bulk current drives the total current in the JL transistors.

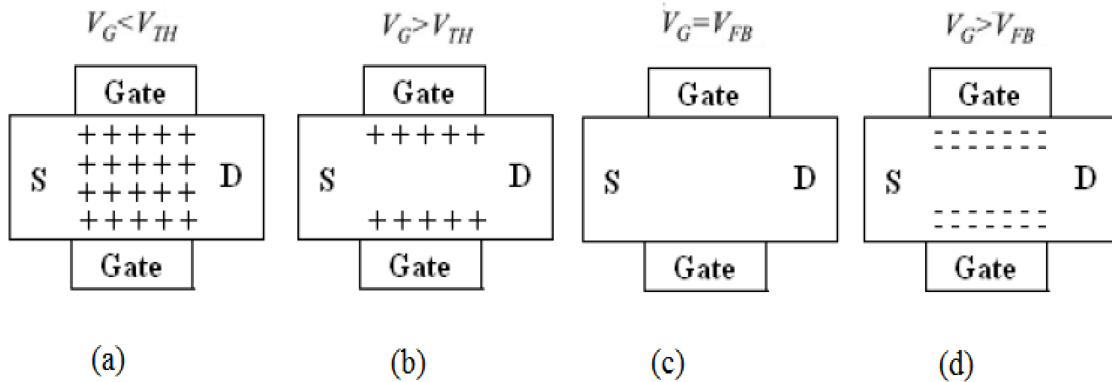


Figure 2.7 a) Fully depleted channel in subthreshold regime, b) semi depleted channel in bulk conduction mode, c) Flat band mode, d) Accumulation mode

Additionally, in contrast to the regular junction-based devices, the principle of operation of junctionless DG MOSFETs is based on a current flow in the volume of the silicon layer instead of at the Si–SiO2 interface. Ideally, the channel doping density of DG JL MOSFETs should be quite high to drive high current densities. On the other hand, turning OFF the device also needs to fully deplete the channel of mobile charges [24], which can be difficult if the doping concentration is exceedingly large. (Recently, such an argument regarding full depletion is also used to justify that SiO2 scaling in DG JL MOSFETs should follow almost the same trend as in bulk DG MOSFETs [25]). For instance, considering an n-type doped channel, if the silicon layer is too highly doped and/or too thick, it may be unfeasible to fully deplete the channel from electrons, even for the lowest gate voltage that the device can bear. Depending on the technological parameters, a hole inversion layer can also build up at the channel interface, further screening the gate electric field and preventing depletion of electrons at the center of the channel. Recently, this hypodissertation is experimentally verified [26]. Therefore, above a certain doping density and silicon thickness, what ultimately limits channel depletion and OFF-state current density is the inherent inverted hole layer at the Si–SiO2 interface. Preliminary studies are attempted to evaluate the performance of DG JL MOSFET integrated on bulk substrate [27]; however, key relationships to investigate the design space of DG JL MOSFETs are still missing today. In [28] analytical expressions

involving the silicon thickness and the doping density to assess channel depletion and related OFF-current performances are developed.

2.4 Review of Junctionless Transistors

Realizing the metallurgical junctions beyond 32nm node for a metal oxide semiconductor field effect transistor (MOSFET) has become extremely challenging due to the need of ultra steep doping profiles [29]. Recently, new kind of device designs, based on the Lilienfeld's first transistor architecture [30] which do not have any metallurgical junctions, were developed [31-32] and successfully fabricated on silicon [29,33,34]. New designs include nanowire gate all around (GAA) architectures [31, 35, and 33], vertically stacked devices [36], tri-gated nanowire architectures with silicon on insulator (SOI) [29] and bulk substrates [37]. Planar architectures on bulk substrates were also developed to further simplify fabrication process [32]. Junctionless transistors have an ultra thin device layer of highly doped semiconductor which is volume depleted in the OFF state (at zero gate bias) due to its workfunction difference with that of the gate electrode. This results in very low leakage current [29]. A positive gate bias forces the device layer to flat band and then into accumulation, resulting in an increase in the drain to source current [29]. The gate of junctionless transistor modulates the resistance of the heavily doped semiconductor; hence, the device can be seen as a gated resistor [29, 38]. Trigate junctionless transistors (JLTs) with channel length of 1 µm were demonstrated on silicon-on-insulator (SOI) substrates [29]. Recently 50nm [33] and 26nm [39] gate length JLTs performance have been reported. P-channel JLTs on Germanium-on-insulator (GeOI) substrates [40] and N-channel JLTs with poly-Si nanowire channels have also been reported [34]. It has been shown that JLT can be a good candidate for flash memory, because of which this concept was applied to NAND flash and 3D integrated flash memories like vertical stacked-array-transistor memory for solid state drives [41] and bit cost scalable memories. This device was also shown as a suitable candidate for dynamic and static random access memory [30] applications. Recent studies also include temperature dependence of electrical characteristics, effects of strain on JLT performance, its ballistic nature at shorter channel lengths, and radio

frequency (RF) performance analysis. These devices are known to offer several advantages over the conventional MOSFETs which are as follows:

1. Better scalability [42]
2. Reduced fabrication process complexity [32, 43]
3. Low electric field during the ON state of the device [32]
4. Impact ionization induced sharp sub-threshold slope at a drain bias of 1.5V [44]
5. High mobility [45].

We here list out the milestones during the evolution of JLTs. These architectures include the gate all around junctionless transistor, known as a nanowire pinch-off FET [31] and Vertical Slit FET (VeSFET) [36]. The schematics of nanowire pinch-off FET and VeSFET are shown in Figure 2.8. The VeSFET is a double gated junctionless transistor wherein the two gates can be operated independently. Independent gate architecture allows the designer to realize logic functions such as AND, OR etc. Its vertical assembly makes the VeSFET an attractive device for 3D integration [36]. However, scaling the channel length to ultra short regime would be difficult due to the circular nature of the gate. The first junctionless transistor was fabricated by Colinge et al, in 2010. They have shown the JLTs as a potential device alternative to the conventional MOSFETs. The ON current demonstrated at 1μm channel length is on par with the conventional MOSFET [29]. They have demonstrated a device with negligible DIBL, near-ideal subthreshold slope etc. Even in the recent short channel (& 50nm) junctionless transistor fabricated by Colinge et at., they show that the electrostatic integrity is intact [44]. Later, it was shown by Choi et al., [33], that a short channel length (& 50nm) GAA junctionless FET has an unacceptable variability with nanowire width variations. A large shift (& 3V) in threshold voltage is observed just by doubling the width of nanowire. An inversion mode transistor fabricated with a similar process flow does not have such variability. Very recently, Rios et al. [39], have a contradicting version of results shown by [29] and [44]. They show that for a given OFF current JLTs have lower ON current with an increased short channel effects. In view of the above mentioned shortcomings of junctionless transistors, there is a tremendous need for reducing the short channel effects to make the device an attractive alternative for low standby power applications.

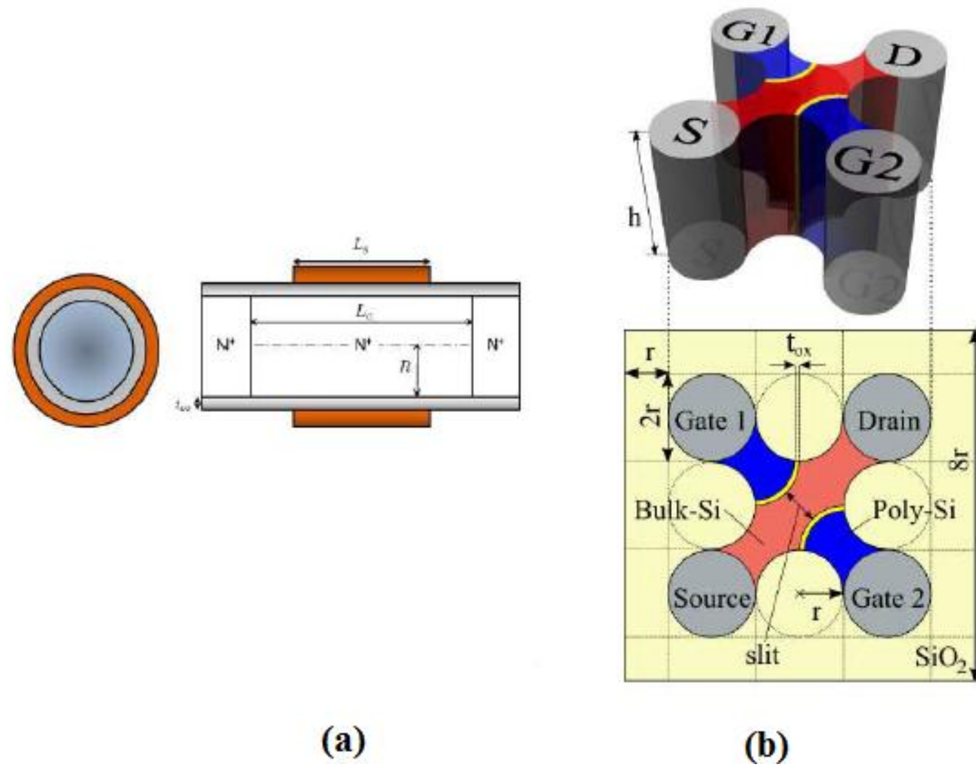


Figure 2.8: Schematic representation of (a) nanowire pinch-off FET [31] (b) Vertical Slit FET (VeSFET) [36]

2.5 Introduction to Device Modelling

The rapid developments in semiconductor technology over the past 15 years have led to a dramatic increase in interest in device modelling. The need to understand the detailed operation and optimize the design of silicon very large-scale integrated devices (VLSI), very high-speed integrated circuits (VHSIC) and compound semiconductor devices has meant that device modelling now plays a crucial role in modern technology. As the scale of the individual semiconductor devices decreases and the complexity of the physical structure increases, the nature of the device characteristics depart from those obtained from many of the classically held modelling concepts. Furthermore, the difficulty encountered in performing measurements on these devices means that greater emphasis must be put on results obtained from theoretical characteristics. Modelling also allows new device structures to be rigorously investigated prior to fabrication.

Semiconductor device models can be considered in two broad categories-physical device models and equivalent circuit models. Physical device models attempt to incorporate the

physics of device operation whilst equivalent circuit models are based on electrical circuit analogies representing the electrical behavior.

The analysis requirements for physical models are normally satisfied using numerical techniques implemented on computers. Physical device models are solved using either bulk carrier transport equations (the semiconductor equations), solutions to the Boltzmann transport equation or quantum transport concepts. Historically, bulk transport solutions have satisfied most device models, whilst Boltzmann and quantum transport solutions have provided a strong insight into the detailed device physics. However, the trend towards very small geometry devices, operating in the hot electron range, means that non-equilibrium transport conditions must be accounted for and the importance of the latter two techniques has become more significant. Table 2.1 shows the advantages and the limitation of various semi-classical and quantum-transport device models [39].

Table 2.1 Advantages and the limitation of various semi-classical and quantum-transport device models.

Approximate ↑ / Exact ↓ — Easy, fast ↑ / Difficult ↓

Approaches	Model	Improvements
Semi-classical approaches	Compact models	Appropriate for Circuit Design
Semi-classical approaches	Drift-Diffusion equations	Good for devices down to 0.5 μm, include μ(**E**)
Semi-classical approaches	Hydrodynamic Equations	Velocity overshoot effect can be treated properly
Semi-classical approaches	Boltzmann Transport Equation Monte Carlo/CA methods	Accurate up to the classical limits
Quantum approaches	Quantum Hydrodynamics	Keep all classical hydrodynamic features + quantum corrections
Quantum approaches	Quantum Monte Carlo/CA methods	Keep all classical features + quantum corrections
Quantum approaches	Quantum-Kinetic Equation (Liouville, Wigner-Boltzmann)	Accurate up to single particle description
Quantum approaches	Green's Functions method	Includes correlations in both space and time domain
Quantum approaches	Direct solution of the *n*-body Schrödinger equation	Can be solved only for small number of particles

2.5.1 Standard MOSFET models

Some semiconductor industry standard compact models, such as charge, potential and conductance based models are reviewed here.

2.5.1.1 Charge based MOSFET model

The charge based modeling approach is one of the basic and primitive modeling approaches. It is based on the computation of the inversion charge density in the MOSFET channel in terms of the terminal voltages, i.e. gate and drain voltages. This model is a regional model because it explains the behavior of the MOSFET separately in all regions of its operation. So, these models require smoothing parameters, they are somewhat empirical in the interfacing regions and, thus the device is not described accurately. The prominent charge based models are level 1, level 2, and level 3, BSIM 1, HSPICE level 28, BSIM 2, BSIM 3, BSIM 4, and BSIM 5. BSIM 5 is used for sub-100nm CMOS circuit simulation. This model is applicable to deep sub-micron region, and attempts have been made to include the modeling of strained silicon technology in the latest spice models. BSIM 4aconsiders the influence of stress of mobility, velocity saturation, threshold voltage, body effect and DIBL effect. But the equations expressed are mostly empirical and no analytical models have been given.

2.5.1.2 Potential based MOSFET model

This model approach is more accurate than the charge based models. It is based on the calculation of the potential in the channel of a MOSFET to determine the I-V and C-V characteristics. Some of the models based on the approach are SP models by Penn-state University, USA, HISIM (Hiroshima-University, STARC IGFET model) valid down to sub-100nm MOSFETs. This model is applicable to the sub micron region and attempts have been made to include the modeling of strained silicon technology.

2.5.1.3 Conductance based MOSFET model

This modeling approach is suitable for low power, short channel applications for analog design. It is known as the EKV (Enz-Krummenachar-Vittoz) model, which has been developed by the Swiss Federal Institute of Technology, Switzerland. This model keeps the substrate as the reference rather than the source, as observed in the potential based

and charge based models. Due to its complexity, it is much less used for modeling purposes. Moreover, no stress modeling has been done in this model. In all the approaches mentioned above, attempts have been made to model MOSFETs. But most of the models that have been developed are either empirical in nature. Therefore, there is a need for a more physics based approach to accurately explain the behavior of the device [46].

2.6 Summary

As dimensional scaling of CMOS transistors is reaching its fundamental limits, various researches have been actively carried out to find an alternative way to continue to follow Moore's law. Among these efforts, DG devices have been well recognized for their advantages in integrating deep sub-micron CMOS devices. However, with the reduction of channel length, short-channel effects are becoming increasingly important. SCE degrades the controllability of the gate voltage over drain current due to increased charge-sharing from the drain/source regions, which leads to the degradation of the subthreshold slope and the increase in drain off-current. The last decade has seen increasing amount of effort focused to circumvent the undesirable short channel effects (SCE). Engineering channel doping in a controlled way is prohibitively difficult with extremely thin-films and scarce and randomly positioned dopant atoms, implying yield and reliability problems. Therefore, an additional constraint, 'reliability,' has to be added to the conventional low-power, high-speed and high-density design consideration. On the other hand, buried oxides thinner than 100 nm are needed to avoid coupling, which trades-off with junction capacitance considerations. Multiple gate SOIs offer a better immunity against SCE but they are difficult to integrate in the current CMOS fabrication technology. Recently developed junctionless MOSFETs, an alternative solution in suppressing SCEs better than conventional inversion-mode devices is discussed. Therefore, a systematic analysis of the effect of junctionless MOSFETs is required to aid in understanding its efficiency in suppressing SCE in deep sub-micron CMOS devices.

Chapter 3

3 Two Dimensional Subthreshold Region Drain Current Modeling of Symmetrical Double-Gate Junctionless MOSFET

3.1 INTRODUCTION

In long channel MOSFETs the large spacing between source/drain regions provides very small value of lateral electric field component (i.e. along the channel length) thus the "edge effect" along the sides of the channel can be neglected and only perpendicular electric field (i.e. along the silicon film thickness) is assumed to exist at the surface everywhere reducing the analysis to only one dimension based on gradual channel approximation. Such one dimensional analysis fail in short channel devices as the source and drain are much closer to each other causing the drain electric field to influence the channel potential. Thus, a two dimensional analysis is required for short channel devices with large channel width and a three dimension approach is adopted for short channel devices with narrow width.

A 2-Dimensional analytical solution for Poisson's equation has been derived by using the surface potential based charge model for a symmetric double gate junctionless MOSFET by considering only the mobile charge carriers. On the basis of surface potential based charge model a relation between the surface potential and gate voltage has been obtained in terms of Lambert-W function. Then the Pao-Sah integral is evaluated to obtain the drain current in the subthreshold region. The result of the obtained drain current model is being compared with the drain current of a symmetric double gate (DG) MOSFET in the subthreshold region.

3.2 DG JL MOSFET Structure

In order to obtain the surface potential of the DG JL MOSFET the potential distribution

in the silicon film of the device is studied. Figure 3.1 represents a schematic diagram of a DG JL MOSFET where the channel length is represented by L, t_{ox} and t_{si} represents the oxide thickness and silicon film thickness. N_{si} is the doping concentration in the channel and source/drain region.

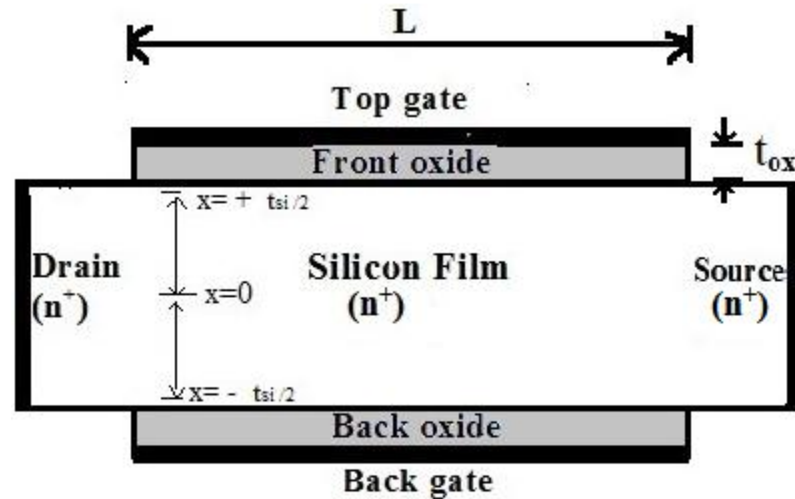


Figure 3.1 Cross-section of DG JL MOSFET

3.2.1 POISSON'S EQUATION

To model the physical behavior of symmetrical DG JL MOSFET at nanometer domain, the potential distribution across the thin silicon film under different drain and gate bias conditions must be explicitly obtained. Presence of two gates and thin silicon film causes the potential distribution in DG JL MOSFET to be different than single gate MOSFET and the maximum potential do not occur at the surface but at some depth in the film. Many different approaches have been developed to analytically determine the potential along the channel of DG MOSFET in the literature, of which depletion approximation for solving Poisson's equation is one.

Considering only the mobile charges, according to the classical model, the Poisson's equation in the channel region of Figure 3.1 is given by:-

$$\frac{d^2\Psi_{jl}}{dx^2} = \frac{qN_{si}}{\varepsilon_{si}}\left[\exp\left(\frac{\Psi - V}{v_{thermal}}\right) - 1\right] \quad \text{... (1)}$$

where $\Psi_{jl}(x)$ is the electrostatic channel potential, ε_{si} is the silicon permittivity, $v_{thermal}$ is the thermal voltage whose value is given by $(kT/q) \approx 26$ mV, V is the quasi-Fermi potential of the electron and q is the electronic charge.

DG JL MOSFET being a majority carrier device, the hole concentration is considered to be negligible compared to that of electrons in the channel with the boundary condition to be considered as:-

$$\left.\frac{d\Psi_{jl}}{dx}\right|_{x=0} = 0 \quad \ldots (2)$$

The electric potential at $\pm t_{si}/2$ is given by Ψ_{jls} termed as surface potential and the potential at the centre of the film at x=0 is denoted by Ψ_{jl0} .

Integrating (1) from Ψ_{jl0} to Ψ_{jls} once give:-

$$\frac{d\Psi_{jl}}{dx} = \sqrt{\frac{2qN_{si}v_{thermal}}{\varepsilon_{si}}\left[\exp\left(\frac{\Psi_{jls} - V}{v_{thermal}}\right) - \exp\left(\frac{\Psi_{jl0} - V}{v_{thermal}}\right) - \left(\frac{\Psi_{jls} - \Psi_{jl0}}{v_{thermal}}\right)\right]} \quad \ldots (3)$$

Now using Gauss's law, the relation between the surface potential and the gate voltage can be obtained by:-

$$Q_O = 2\varepsilon_{si}\left.\frac{d\Psi_{jl}}{dx}\right|_{x=\pm t_{si}/2} \quad \ldots (4)$$

Where Q_O, the space charge density within limits (Ψ_{jl0} to Ψ_{jls}) is given by:

$$Q_o = -2\varepsilon_{si}\frac{d\Psi_{jl}}{dx} = -2C_{ox}\left(\Psi_g - \Psi_{fb} - \Psi_{jls}\right) \quad \ldots (5)$$

Where C_{ox} is oxide capacitance, Ψ_g is the gate voltage, Ψ_{fb} is the flat band voltage ($\Psi_{fb} \approx \phi_{MS}$, the work function difference).

The channel potential by using parabolic potential approximation [47] is designated by:-

$$\Psi_{jl}(x) = \left(\frac{4x^2}{t_{si}^2}\right)\left(\Psi_{jls} - \Psi_{jl0}\right) + \Psi_{jl0} \quad \ldots (6)$$

Differentiating (6) with respect to *x* we get

$$\frac{d\Psi_{jl}}{dx} = \frac{4(2x)}{t_{si}^{2}}(-\Delta\Psi_{jl}) \qquad \ldots (7)$$

where $\Delta\Psi_{jl} = \Psi_{jl0} - \Psi_{jls}$

Using (5) and (7) we obtain

$$\frac{C_{ox}}{\varepsilon_{si}}(\Psi_g - \Psi_{fb} - \Psi_{jls}) = -\frac{4(2x)}{t_{si}^{2}}(\Delta\Psi_{jl}) \qquad \ldots (8)$$

As he channel is considered to be fully depleted Ψ_{jl0} is approximately zero.

$$\frac{C_{ox}}{\varepsilon_{si}}(\Psi_g - \Psi_{fb} + \Delta\Psi_{jl}) = -\frac{4\Delta\Psi_{jl}}{t_{si}} \qquad \ldots (9)$$

$\Delta\Psi_{jl}$ of (9) is equivalent to [48]

$$\Delta\Psi_{jl} = \frac{t_{si}}{8\varepsilon_{si}}\left(Q_{mobile} + qN_{si}t_{si}\right) \qquad \ldots (10)$$

Putting (10) in (9) and solving by assuming Q_{mobile} to be zero, the threshold voltage can be directly obtained at gate voltage, $\Psi_g = V_{th}$ as:-

$$V_{th} = \Psi_{fb} - \frac{t_{si}^{2}qN_{si}}{8\varepsilon_{si}} - \frac{qN_{si}t_{si}}{2C_{ox}} \qquad \ldots (11)$$

Solving (3) and (5) we obtain,

$$(\Psi_g - \Psi_{fb} - \Psi_{jls}) = \sqrt{\frac{2qN_{si}\gamma\varepsilon_{si}v_{thermal}}{C_{ox}}\left\{1 - \exp\left(\frac{\Psi_{jl0} - V}{v_{thermal}}\right)\left(\frac{1 - \exp(-\gamma)}{\gamma}\right)\right\}} \qquad \ldots (12)$$

Where $\gamma = -\left(\frac{\Psi_{jls} - \Psi_{jl0}}{v_{thermal}}\right)$, for subthreshold region the term inside the square root $\left(\frac{1 - \exp(-\gamma)}{\gamma}\right)$ << 1, thereby modifying the above equation as:-

$$(\Psi_g - \Psi_{fb} - \Psi_{jls}) = -\frac{qN_{si}t_{si}}{2C_{ox}}\left[1 + \frac{1}{2}\left(\frac{V - \Psi_{jl0}}{v_{thermal}}\right)\right] \qquad \ldots (13)$$

Finally the relation between the surface potential and gate voltage for DG JL MOSFET in terms of Lambert-W function is explicitly obtained as:-

$$\Psi_{jls} = \Psi_g - V_{th} - \frac{qN_{si}t_{si}^{2}}{8\varepsilon_{si}} - v_{thermal}W[A] \qquad \ldots (14)$$

where $A = \frac{N_{si}qt_{si}}{4v_{thermal}C_{ox}} \exp\left(\frac{\Psi_g - V - V_{th}}{v_{thermal}}\right)$ and W is the Lambert-W function which is defined as the inverse function of $y=xe^{x}$ [49].

3.3 POISSON'S EQUATION for DG MOSFET Structure

Figure 3.2 shows the cross-section of a symmetric DG MOSFET. Both the gates have same gate voltage having same work function.

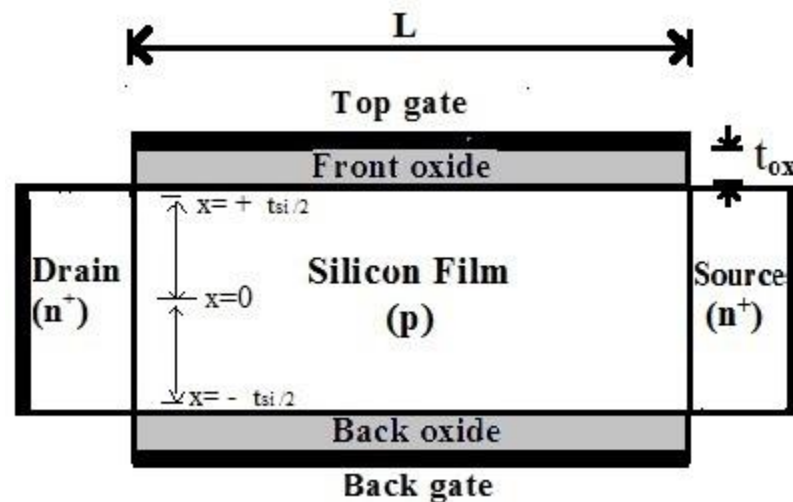


Figure 3.2 Cross-section of DG MOSFET

Considering only the mobile charge carriers, the Poisson's equation in the channel region is given by:-

$$\frac{d^2\Psi_{dg}}{dx} = \frac{qn_i}{\varepsilon_{si}} \exp\left(\frac{\Psi_{dg}}{v_{thermal}}\right) \qquad \ldots (15)$$

where $\Psi_{dg}(x)$ is the electrostatic potential for the double gate (DG) MOSFET, n_i is the intrinsic carrier concentration [50] and other parameters being same as that in case of DG JL MOSFET. Here the device considered is an nMOSFET with hole concentration

negligible to that of the electron concentration and the silicon film is considered to be lightly doped or undoped.

Integrating (15) once with boundary condition $\left.\frac{d\Psi_{dg}}{dx}\right|_{x=0} = 0$ we obtain:-

$$\frac{d\Psi_{dg}}{dx} = \sqrt{\frac{2qn_i kT}{\varepsilon_{si}}\left[\exp\left(\frac{\Psi_{dg}}{v_{thermal}}\right) - \exp\left(\frac{\Psi_{dg0}}{v_{thermal}}\right)\right]} \quad \ldots (16)$$

Where Ψ_{dg0} is the potential at centre of the silicon film at x=0. Again integrating once the potential being the function of x is obtained as:-

$$\ln\left[\cos\left\{\frac{x}{2v_{thermal}}\sqrt{\frac{2n_i kT}{\varepsilon_{si}}\exp\left(\frac{\Psi_{dg0}}{v_{thermal}}\right)}\right\}\right] = -\frac{(\Psi_{dg} - \Psi_{dg0})}{2v_{thermal}} \quad \ldots (17)$$

Thus, the surface potential $\left(\Psi_{dgs} = \left.\Psi_{dg}\right|_{x=\pm\frac{t_{si}}{2}}\right)$ is obtained as:-

$$\Psi_{dgs} = \frac{-2}{v_{thermal}}\ln\left[\cos\left\{\sqrt{\frac{n_i q}{2\varepsilon_{si} v_{thermal}}}\left(\frac{t_{si}}{2}\right)\right\}\right] \quad \ldots (18)$$

The relation between the surface potential and gate voltage is expressed by using Gauss's law as:-

$$\frac{\varepsilon_{ox}}{t_{ox}}\left(\Psi_g - \Delta\phi_i - \Psi_{dgs}\right) = \pm\varepsilon_{si}\frac{d\Psi_{dg}}{dx} \quad \ldots (19)$$

where $\Delta\phi_i$ is the work function difference between gate and intrinsic silicon.

By using (16) the relation between surface potential and gate voltage is given by:-

$$\Psi_g = \Psi_{dgs} + \Delta\phi_i + \frac{\sqrt{2qn_i kT\varepsilon_{si}\exp\left(\frac{\Psi_{dgs}}{v_{thermal}}\right)}}{C_{ox}} \quad \ldots (20)$$

The threshold voltage for a symmetrical DG MOSFET is given by [51]:-

$$V_{th} = \left[\frac{E_g}{2q} + V_{bi} + \frac{\varphi_{gfs}(1+r) - \left(\frac{Q_b}{C_{ox}} - r\frac{Q_b}{2C_{si}}\right)}{1+r} - \frac{3t_{si}t_{ox}V_{DS}}{L^2} - \frac{9t_{si}t_{ox}\left(\frac{E_g}{2q}\right)}{L^2}\right] \quad \ldots (21)$$

Where E_g is the energy band gap for silicon, V_{bi} is the built in potential $\left(\frac{kT}{q}\ln\left(\frac{N_A}{n_i}\right)\right)$ where N_A is substrate doping concentration, φ_{gfs} is the work function difference between the gate electrode and the body region, $Q_b = -qN_At_{si}$ is the depletion charge density, C_{ox} is the oxide capacitance, $C_{si}=\frac{\varepsilon_{si}}{t_{si}}$ is silicon film capacitance, r is the gate to gate coupling factor given by $r=\frac{3t_{ox}}{3t_{ox}+t_{si}}$.

3.4 DRAIN CURRENT MODEL

3.4.1 DG JL MOSFET

Using the gradual channel approximation, the drain current equation can be expressed by Pao-Sah integral as:-

$$I_{drain} = -\mu\frac{W_{jl}}{L}\int_0^{V_D} Q_{mobile}dV \quad \text{… (22)}$$

where $Q_{mobile} = Q_0 - Q_D$ is the mobile charge density, $Q_D = qN_{si}t_{si}$ being the fixed charge density, μ is the carrier mobility which is constant along the channel, W_{jl} is the width of the DG JL MOSFET and L being the channel length. V_D is the drain voltage with the source voltage assumed to be 0.

Replacing Q_0 from (5) equation (22) is obtained as:-

$$I_{drain} = \mu\frac{W_{jl}}{L}\int_0^{V_D}\left[2C_{ox}\left(\Psi_g - \Psi_{fb} - \Psi_{jls}\right) + Q_D\right]dV \quad \text{... (23)}$$

A compact analytical model for the subthreshold drain current model is developed using the surface potential equation in (14).For subthreshold region, $\Psi_g < V_{th}$ the channel of DG JL MOSFET is fully depleted. Differentiating (14) with respect to Ψ_{jls} leads to:-

$$\frac{dV}{d\Psi_{jls}} = \left[\frac{1+W(A)}{W(A)}\right] \quad \text{… (24)}$$

Solving (23) we obtain:-

$$I_{drain} = \mu \frac{W_{jl}}{L} v_{thermal} 2C_{ox} \int_{0}^{V_D} W[A] dV \qquad \dots (25)$$

Using (24) in (25) we get the subthreshold drain current as:-

$$I_{drain} = \mu \frac{W_{jl}}{L} v_{thermal} 2C_{ox} \int_{\Psi_{jls(0)}}^{\Psi_{jls(L)}} 1 + W[A] d\Psi_{jls} \qquad \dots (26)$$

where $\Psi_{jls(0)}$ and $\Psi_{jls(L)}$ being the surface potential at x=0 and L respectively.

Putting the limits, finally the subthreshold drain current of DG JL MOSFET is obtained as:-

$$I_{drain} = \mu \frac{W_{jl}}{L} (v_{thermal})^2 (1+s)(s-d) \qquad \dots (27)$$

where $s = W\left[\frac{N_{si} q t_{si}}{4 v_{thermal} C_{ox}} \exp\left(\frac{\Psi_g - V_{th}}{v_{thermal}}\right)\right]$ and $d = W\left[\frac{N_{si} q t_{si}}{4 v_{thermal} C_{ox}} \exp\left(\frac{\Psi_g - V_{th} - V_D}{v_{thermal}}\right)\right]$

with device dimension scaling, the subthreshold drain current is affected by the short channel effects such as DIBL (Drain Induced Barrier Lowering) and channel length modulation. Some parameters have been incorporated in the drain current model to account for these effects.

A drain voltage dependent parameter αV_D accounting for DIBL is being included in the exponential term of the current model which was previously only gate voltage dependent parameter [52]. The value of α as developed by Meindl and Swanson [53] for bulk MOSFET is being modified for the case of double gate structure by adding an empirical parameter H, thereby modifying the value of α as:-

$$\alpha = \frac{\varepsilon_{si} H}{C_{ox} L} \qquad \dots (28)$$

The channel length modulation parameter [54] is represented as:-

$$\text{CLM}=1+\left(\frac{\lambda}{L}\right)^{\beta-\sqrt{\frac{\lambda}{L}}\left(\frac{V_{def}}{V_{gef}-V_{th}}\right)} \quad \ldots (29)$$

where β is the empirical fitting parameter and $\lambda=\sqrt{\frac{\varepsilon_{si}t_{si}}{2C_{ox}}\left(1+\frac{t_{si}C_{ox}}{4\varepsilon_{si}}-\frac{t_{si}C_{ox}}{16\varepsilon_{si}}\right)}$ is the natural length [55].

Thus, the modified subthreshold drain current model for DG JL MOSFET is modeled as:-

$$I_{drain}=\mu\frac{W_{jl}}{L}(v_{thermal})^2(1+s_1)(s_1-d_1)(CLM) \quad \ldots (30)$$

where
$$s_1=W\left[\frac{N_{si}qt_{si}}{4v_{thermal}C_{ox}}\exp\left(\frac{\alpha V_D+\Psi_g-V_{th}}{v_{thermal}}\right)\right]$$

and
$$d_1=W\left[\frac{N_{si}qt_{si}}{4v_{thermal}C_{OX}}\exp\left(\frac{\alpha V_D+\Psi_g-V_{th}-V_D}{v_{thermal}}\right)\right]$$

3.4.2 DG MOSFET

The subthreshold region drain current model for DG MOSFET is given by the BSIM drain current model [56]. Introducing the DIBL and channel length modulation parameters to the drain current model, the final subthreshold region drain current model for DG MOSFET is given by:-

$$I_{drain_dg}=\left[\mu C_{ox}\frac{2W_{dg}}{L}(v_{thermal})^2\left(1-\exp\left(\frac{V_D}{v_{thermal}}\right)\right)\exp\left(\frac{\theta}{v_{thermal}}\right)CLM\right] \quad \ldots (31)$$

where $\theta=\frac{\Psi_g-V_{th}}{n}+\alpha V_D$, n is the subthreshold swing coefficient [18], W_{dg} is width of the device and other parameters being same as that in case of DG JL MOSFET.

Chapter 4

4 Results and Discussion

The results of the developed model are being validated with the TCAD simulation tool Cogenda. A classical drift diffusion approach is being used for the simulation process and also Fermi-Dirac carrier statistics are incorporated throughout the process. The transfer characteristics of the developed device is obtained for channel length L = 45 nm and width as W = 50 nm. The effective mobility for simplicity is considered to be 500 cm^2/Vs with the assumption that the carrier mobility is constant throughout the channel and the velocity saturation effect is neglected. The gate work function is considered to be 4.74eV. An n-type uniform channel doping for the DG JL MOSFET is considered as $N_{si} = 10^{19}$ cm^{-3} and other device parameters such as oxide thickness and silicon film thickness is considered as t_{ox} = 2 nm and t_{si} = 10 nm respectively. These device parameters are considered throughout the simulation process for both DG JL MOSFET and DG MOSFET device. For DG MOSFET the doping concentration in both n and p region is considered as $N_A = N_{si} = 10^{19}$ cm^{-3}.

4.1 Surface Potential Variation with Gate Voltage

Figure 4.1(a) and Figure 4.2(b) represents the relation between the surface potential and

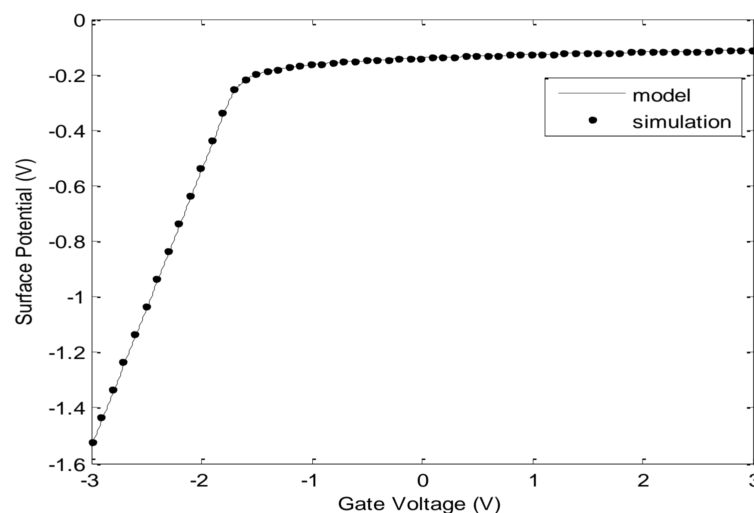


Figure 4.1(a) Surface potential variation with gate voltage for DG JL MOSFET for quasi-Fermi potential V = 0.

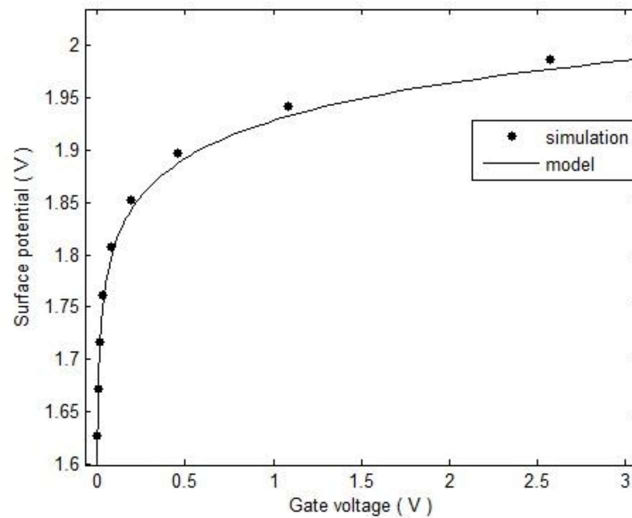


Figure 4.1 (b) Surface potential variation with gate voltage for undoped symmetrical DG MOSFET

gate voltage for JL MOSFET and DG MOSFET respectively with quasi-Fermi potential V = 0. The model is found to be in good agreement with the TCAD simulation results.

4.2 Subthreshold Region Drain Current

Figure 4.2 (a) and 4.2 (b) represents the transfer characteristics of the DG JL MOSFET in the subthreshold region for V_D = 0.1 V and V_S = 0 V. The fitting parameter values considered for the drain current model are H = 0.4 and $\beta = 1$ where the value of β can be any value from 0.6 to 1.2. The figures represent the subthreshold region drain current in both logarithmic and linear scale respectively. From both the figures it is clearly observable that the developed model and the simulation results are in good agreement with each other for the subthreshod region ($V_G < V_{th}$) and deviates after that. The same analysis is being done in Figure 4.3(a) and 4.3(b) for DG MOSFET in logarithmic and linear scale respectively and both the model and simulation results are found to be in good agreement for subthreshold region.

Figure 4.4(a) and 4.4(b) compares the transfer characteristics of the developed model for the same defined device parameters in both logarithmic and linear scale with that of a

previous study [57] in which the subthreshold region drain current for DG JL MOSFET is given by:-

$$I_{drain} = \mu \frac{W_{jl}}{L} v_{thermal} \sqrt{q N_{si} \pi v_{thermal} 2 \varepsilon_{si}} e^{X} \left(1 - e^{Y}\right) \qquad \ldots (32)$$

where X= $\left(\dfrac{\Psi_g - V_{th}}{v_{thermal}} \right)$ and Y= $\left(-\dfrac{V_D}{v_{thermal}} \right)$

From the figure it is observed that the present current model using Lambert-*W* function is more close to the simulation results than that of the previous model.

Parameters such as DIBL and channel length modulation were introduced in the developed drain current model to better the device characteristics curve at higher drain voltage. Figure 4.5(a) and 4.5(b) show the logarithmic transfer characteristics curve for both DG JL MOSFET and DG MOSFET respectively at $V_D = 1$ V and it is observed that the model is in good agreement with the simulation result at higher drain voltage.

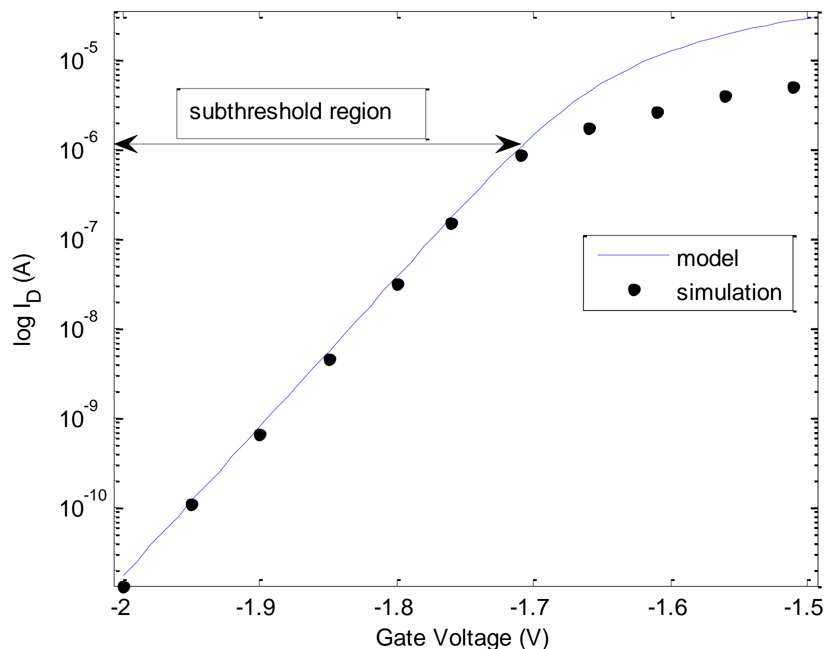


Figure 4.2 (a) Transfer characteristics for symmetrical DG JL MOSFET in logarithmic scale for the developed model compared with simulation (symbols) results.

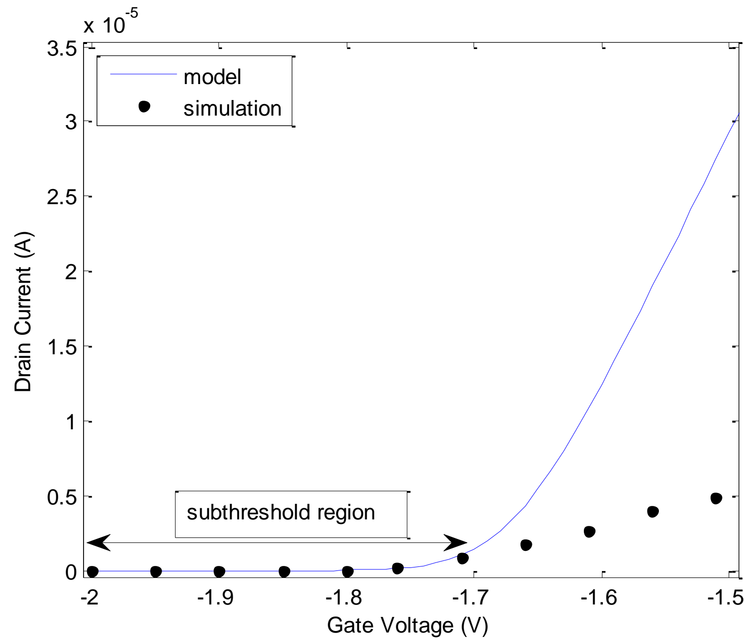


Figure 4.2(b) Transfer characteristics for symmetrical DG JL MOSFET in linear scale for the developed model compared with simulation (symbols) results.

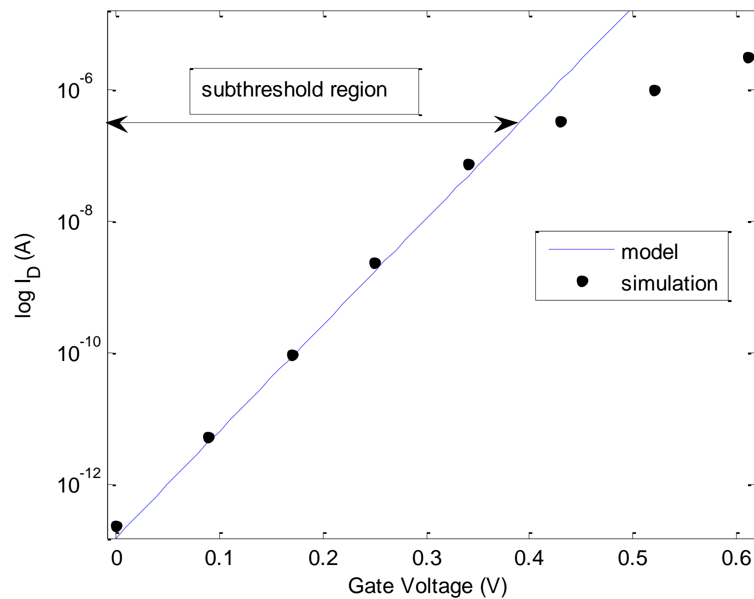


Figure 4.3(a) Transfer characteristics for symmetrical DG MOSFET in logarithmic scale for the developed model compared with simulation (symbols) results.

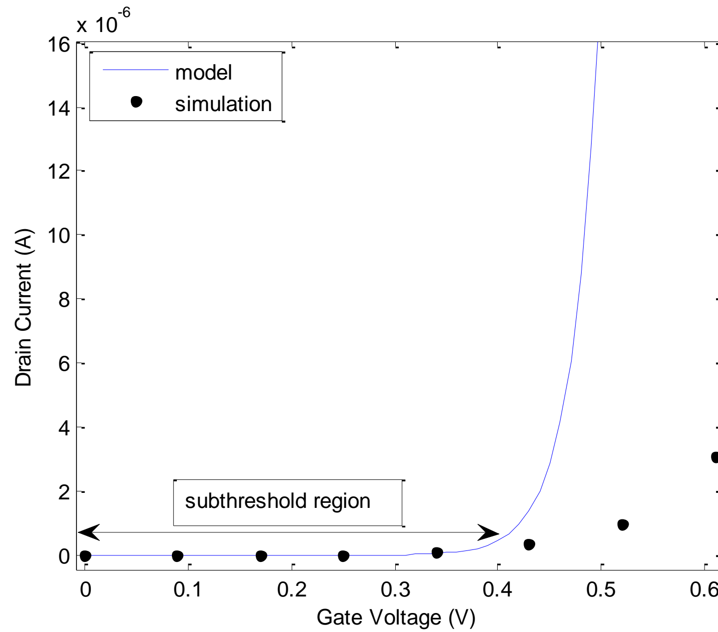


Figure 4.3(b) Transfer characteristics for symmetrical DG MOSFET in linear scale for the developed model compared with simulation (symbols) results.

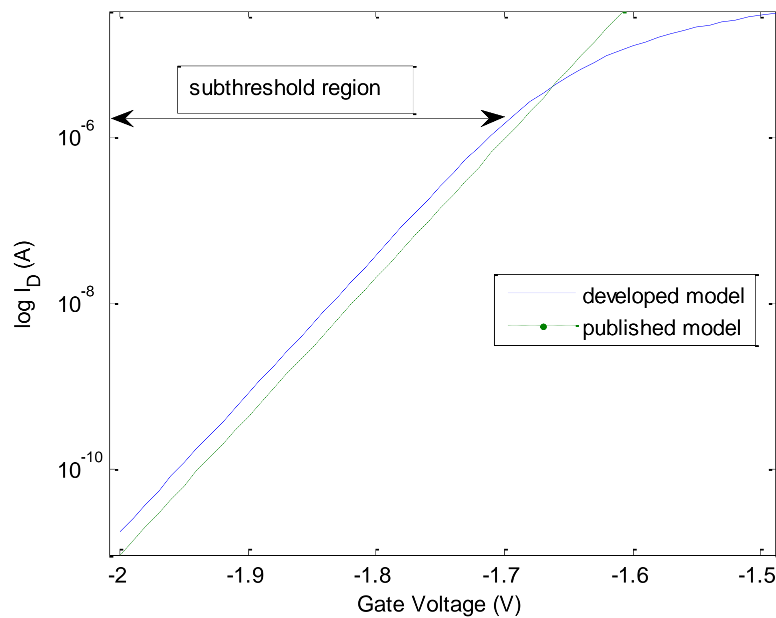


Figure 4.4(a) Transfer characteristics for symmetrical DG JL MOSFET in logarithmic scale for the developed model and published research model.

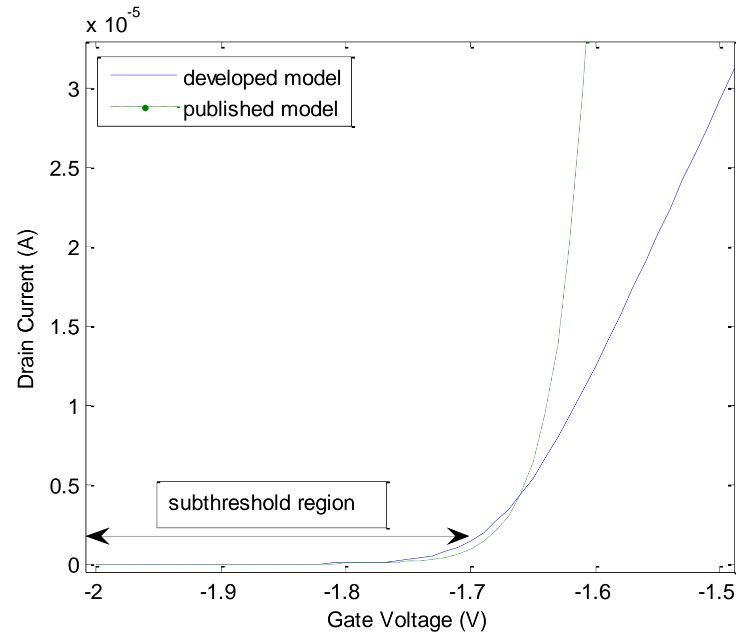


Figure 4.4 (b) Transfer characteristics for symmetrical DG JL MOSFET in linear scale for the developed model and published research model.

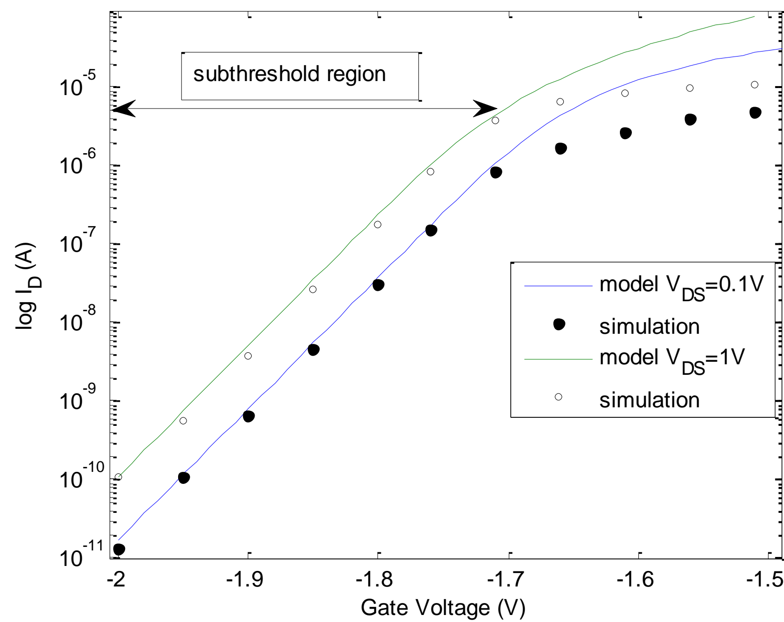


Figure 4.5(a) Transfer characteristics for symmetrical DG JL MOSFET in logarithmic scale for the developed model at $V_D = 1$ V and $V_D = 0.1$ V.

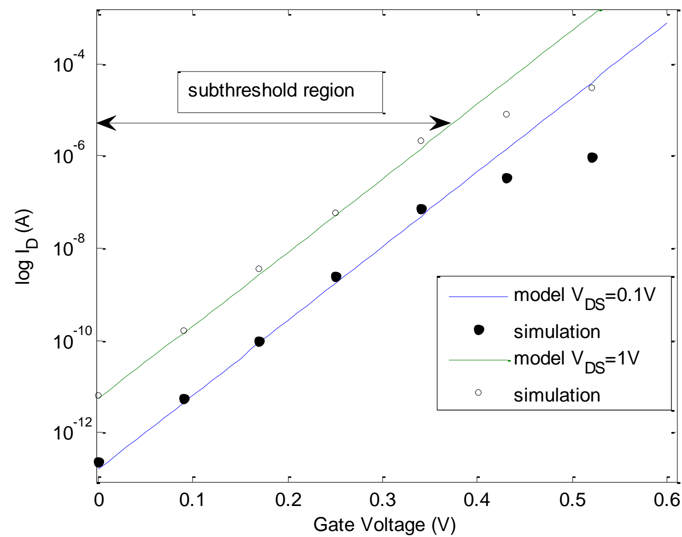


Figure 4.5(b) Transfer characteristics for symmetrical DG MOSFET in logarithmic scale for the developed model at $V_D = 1$ V and $V_D = 0.1$ V.

4.3 Threshold Voltage

In DG JL MOSFET the threshold voltage shift is larger due to the presence of heavy doping in the channel region. In order to study this effect the change in threshold voltage is studied by varying the oxide thickness from 1.5 nm to 3.5 nm in Figure 4.6.

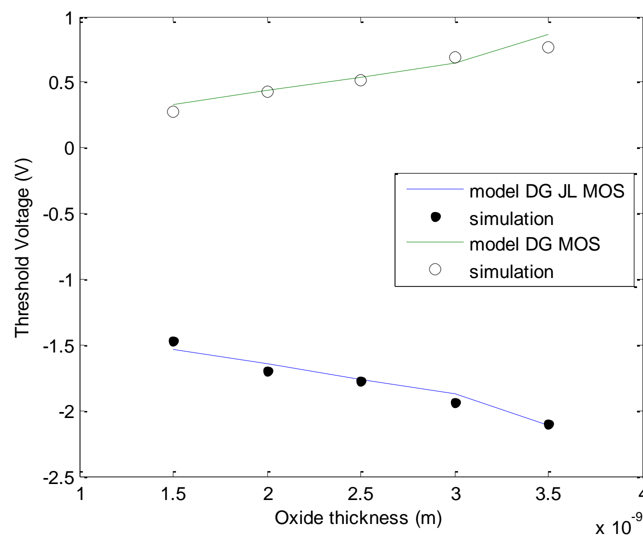


Figure 4.6 Threshold voltage comparisons between DG JL MOSFET and DG MOSFET for oxide thickness variation for the developed model and simulation results

The threshold voltage change with varying oxide thickness for DG MOSFE is also calculated and compared with that of DG JL MOSFET. In case of DG MOSFET with increasing oxide thickness threshold voltage increases and for DG JL MOSFET with increasing oxide thickness we observe that the negative gate voltage increases that are more number of majority charge carriers are required to turn the device into conduction.

4.4 Distribution of Electric Potential with Different Values of V_{DS}

Figure 4.7 shows the distribution of electric potential with varying values of V_{DS} from 0.2V to 0.8V. With the increase in value of V_{DS} the accumulation of electrons that is the majority carriers increases in the surface of the body region and with the increase in electron concentration the curvature of the electric potential also rises with the increasing drain voltage as shown in Figure 4.7.

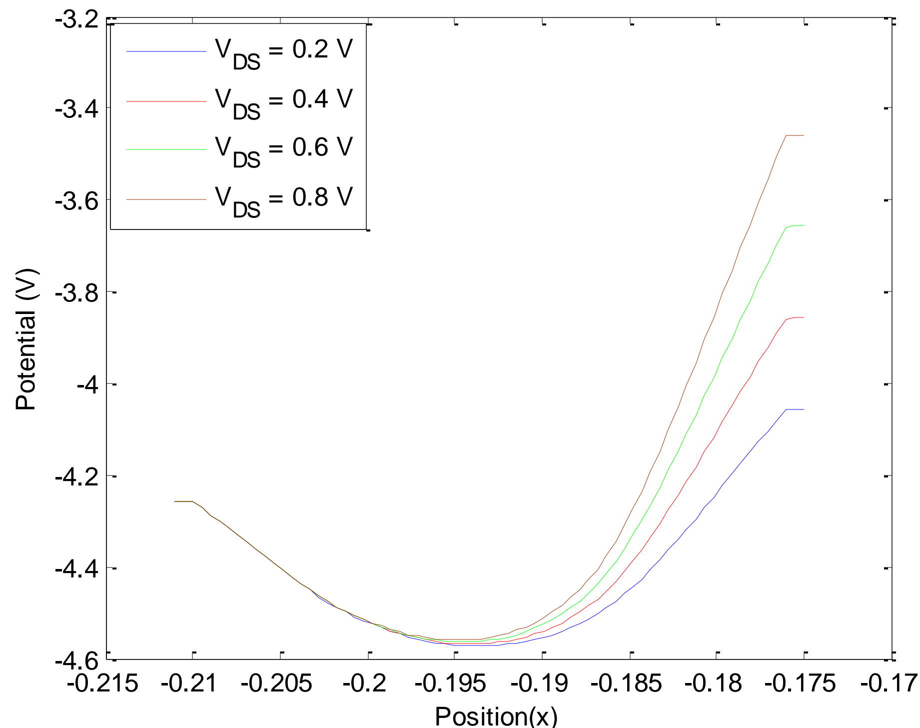


Figure 4.7 Electric potential variation with V_{DS}

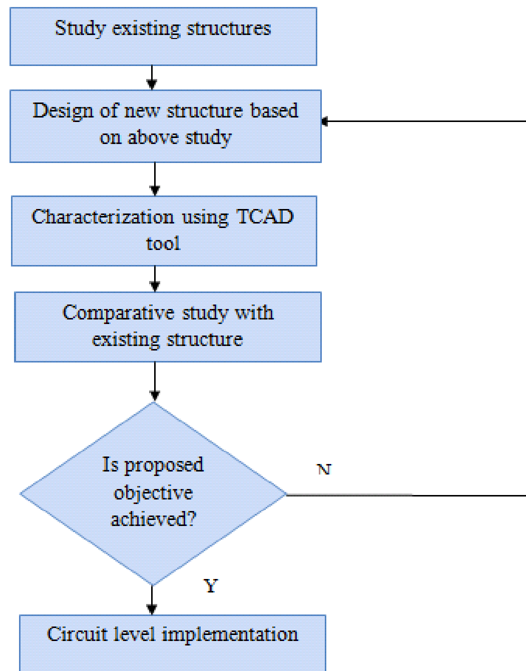
Chapter 5

5 Conclusion and Future Work

5.1 CONCLUSION

With the scaling of device dimensions, a need to suppress the short channel effects was felt and DG JL MOSFET is one of the promising future candidates in the field of device technology. In this chapter n-type DG JL MOSFET was explored to study its behavior. An analytical compact drain current model in the subthreshold region was developed and the model was validated with the simulation results and was found to be in good agreement. The developed model characteristics was compared to the DG MOSFET characteristics curve and was found that the developed model follows all the characteristics of a short channel device and has a beer subthreshold slope than DG MOSFET

5.2 METHODOLOGY



5.3 Scope for Future Work

The developed model has several possible extensions that could be attempted as ongoing research work. Some specific recommendations based on the present work are as follows:

1. The developed drain current model for the subthreshold region can be extended for a full drain current model by considering the current in depletion and accumulation region using proper boundary conditions
2. Present study can be well extended by adding other SCEs which are not considered such as GIDL, hot carrier effect etc and by taking mobility degradation and velocity saturation into consideration.
3. The present model follows classical drift-diffusion approach and can be studied for semi-classical modeling as well.
4. Quantum effects such as quantum confinement and nanoscale effects can also be incorporated into the model so that a more précised results are obtained.

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