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Modeling and Performance Analysis of Optical Interconnect for Emerging Nanoscale Technology Nodes

A Thesis

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Chapter 1

Introduction

1.1 Background

In VLSI systems, **interconnects** refer to the physical wiring or transmission paths that carry signals and power between functional blocks, including logic gates, memory units, and I/O interfaces. As technology scales down to deep submicron and nanometer nodes, interconnects increasingly dominate circuit performance, often becoming bottlenecks for speed, power, and thermal efficiency. The basic on-chip interconnect structure, shown in **Figure. 1.1**, consists of a metallic line with width (w), thickness (t), and length (l), placed at a height (h) above the ground plane and separated by spacing (s) from adjacent wires.

Driven by Moore's law, the relentless trend toward miniaturisation has dramatically increased transistor density, but has also brought interconnects to the brink of communication bottlenecks, operating at or near their ampacity (current-carrying capacity) limits [**?**]. While this trend has enabled the fabrication of highly complex, high-performance chips, it has also led to a growing disparity between transistor scaling and interconnect performance as depicted in **Figure. 1.2**. Though transistor switching becomes faster, the interconnects fail to keep pace, introducing significant latency and energy penalties. This slowed down the rapid growth of Moore's law as interconnect delays, power dissipation, and signal integrity challenges began to

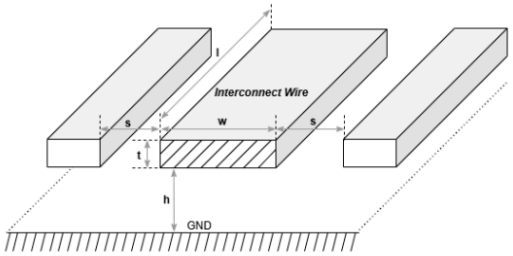


Figure 1.1: Basic VLSI Interconnect wire

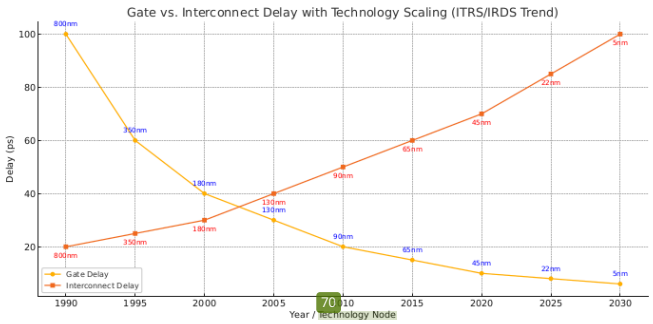


Figure 1.2: Gate vs. interconnect delay trends with technology scaling, annotated by node sizes (ITRS/IRDS projections) [**?**, **?**].

outweigh the benefits of continued device scaling [**?**].

Existing copper (Cu) interconnects have long been regarded as a standard on-chip connection material due to properties like higher conductivity, a stable chemical structure, and resistance to electromigration [**?**]. However, as interconnect dimensions shrink, several issues become pronounced:

- Increased RC delay, degrading signal integrity.
- Electromigration, reducing reliability.
- Increased power density, resulting in thermal hotspots.

These challenges collectively hinder the performance, reliability, and scalability of traditional metal interconnects in advanced VLSI technologies [**?**]. This degradation is primarily attributed to increased electron scattering at grain boundaries, surface roughness, and material interfaces. Moreover, to address reliability concerns such as electromigration and scattering, wider wire widths and barrier layers are often required, which further limit scaling efficiency and interconnect density [**?**].

These limitations prompted the exploration of alternative interconnect paradigms with increased ampacity [**?**]. Among these, optical communication systems (OCS), traditionally employed in long-haul data transmission due to their potential to bypass limitations of electrical signaling, are now being aggressively adapted for short-reach applications [**?**]. Optics aims to carry greater volumes of data across a distance without much interference and noise. Optical links transmit data using light, offering:

- High bandwidth via Wavelength-Division Multiplexing (WDM).
- Low propagation loss and no resistive heating [**?**].

- Immunity to crosstalk and electromagnetic interference [?].
- Energy efficiency at high data rates [?].

These advantages make optical interconnects (OI) especially attractive for global interconnect layers, where conventional metal lines become inefficient. OI were first introduced in 1984 by Goodman *et al.* [?], due to their real-world applications, such as in supercomputing [?, ?], data centers, telecommunications, AI/ML hardware, automotive systems, and consumer electronics [?].

OI primarily consist of three essential components: a transmitter, a waveguide, and a receiver [?]. The transmitter, located at the near end, typically includes either a modulator [?] or a laser diode [?], both of which are driven by specialized driver circuits to generate modulated optical signals [?]. The waveguide serves as the transmission medium, guiding the optical signal with minimal loss across the chip or between chips. At the far end, the receiver block is equipped with a photodetector, such as a photodiode, which converts the incoming optical signal into an electrical current. This current is then amplified and converted to voltage by a transimpedance amplifier (TIA), which acts as the core front-end circuit in the receiver chain [?]. In more advanced designs, the receiver may also include post-amplification and signal conditioning stages to enhance sensitivity, bandwidth, and overall system reliability. The design of TIA is critical in OI design as it affects the system performance in terms of data rate, sensitivity, and noise [?]. All these amplifiers in transmitter and receiver blocks are implemented using deep submicron (DSM) CMOS technology due to their high speed, low cost, and high level of integration [?]. Optical waveguides offer low signal delay and power dissipation, as communication happens through light beams travelling at the speed of light and operating wavelengths of $1300nm - 1550nm$.

Recent research highlights the clear advantage of OI at very short distances [?, ?]. As a result, comparative studies have been conducted to evaluate their performance against electrical counterparts at future technology nodes [?, ?, ?, ?, ?, ?]. In all of these studies, a fundamental CMOS-based TIA receiver circuit is employed to maintain design simplicity. However, such designs are inherently limited in bandwidth due to factors such as high input impedance, photodiode capacitance, and layout parasitics [?]. To address these constraints, more advanced TIA architectures such as those utilising shunt feedback, regulated cascode (RGC) topologies, or active feedback networks are required [?]. These techniques effectively lower the input impedance, suppress the influence of parasitic capacitances, and extend the bandwidth, thereby significantly improving the overall receiver performance [?].

Also, the temperature variations affect key device parameters, such as threshold voltage and carrier mobility, leading to unpredictable circuit behaviour [?]. These fluctuations can introduce signal delays, particularly in global interconnects operating at lower clock rates, thereby constraining overall bandwidth and system performance [?].

1.2 Problem Statement

As demand increases for high-speed, low-power, and scalable interconnect solutions, Cu interconnect results in severe RC delays [**?**]. The increasing RLC parasitics of Cu interconnects, driven by aggressive scaling and higher interconnect density, lead to significant degradation in key performance metrics, including signal propagation delay, power dissipation, and power-delay product (PDP). These effects are especially problematic in global interconnects, where long wire lengths and stronger signal coupling worsen signal integrity and energy efficiency.

In modern processors, interconnects contribute up to 50% of the total delay, and their share of power consumption continues to rise [**?**]. Moreover, the need for repeaters to drive long Cu lines adds further power and area overhead [**?**]. Thus, researchers shifted to novel technologies, namely, OI link, that offer a fundamentally different approach to interconnect scaling. By using photons instead of electrons, they are unaffected by resistive and capacitive parasitics that degrade copper wires [**?**]. A well-validated model of the OI chain *i.e.*, transmitter, waveguide, and receiver, is essential for guiding future designs and comparing them against conventional electrical links at nanoscale technology nodes. This research aims to contribute toward that goal by focusing on the design and modeling of advanced TIA architectures within OI frameworks. A lot of literature has been explored related to modeling OI and its comparison with traditional electrical counterparts in terms of performance parameters *i.e.*, signal delay, power dissipations, and PDP at nanoscale technology nodes.

While extensive comparative work has been conducted, a critical aspect remains largely unexplored: the impact of temperature fluctuations in OI across various technology nodes. Temperature variations affect key device parameters, such as threshold voltage and carrier mobility, leading to unpredictable circuit behaviour [**?**]. These fluctuations can introduce signal delays, particularly in global interconnects operating at lower clock rates, thereby constraining overall bandwidth and system performance [**?**]. Addressing these thermal effects is essential for the reliable implementation of OIs in next-generation systems. From the above discussed research problem statement, the **objectives** of this thesis have been identified as follows:

- To develop the electrical equivalent circuit model of transmitter and receiver for Optical Interconnect.
- To analyze the impact of temperature variation on the performance of Optical Interconnects.
- Comparative analysis of the results obtained from the above analysis with interconnects of CNT and copper.

The **first objective** focuses on developing and evaluating electrical equivalent models for the transmitter, waveguide, and receiver blocks of an optical interconnect system. These models are rigorously analyzed in terms of delay, power dissipation, and power-delay product (PDP) at 22*nm* and 14*nm* technology nodes to assess their performance parameters.

The **second objective** incorporates the impact of temperature variations on the transmitter, waveguide, and receiver blocks, given that silicon photonic devices in OI are temperature-sensitive. The novel TIA-based receiver, introduced in the first objective, is integrated into receiver modeling to ensure a comprehensive analysis.

The **third objective** involves a comparative analysis of Cu and CNT interconnects with the proposed OI in terms of performance parameters at 22*nm* and 14*nm* technology. This comparison helps evaluate their suitability for high-performance optical interconnect applications under varying interconnect length and temperature conditions.

1.3 Thesis Organization

This work presents the circuit-level modelling and detailed analysis of OI for the global interconnect level at 22nm and 14nm technology nodes. The OI performance is compared with traditional Cu and SWCNT-B interconnects. The content of this thesis is organized into the following chapters:

Chapter 1 provides a brief introduction to the VLSI interconnects, highlighting their requirements, applications, and key technologies. Additionally, the chapter discusses the paradigm shift towards optical interconnects (OI) due to the advantages they offer as compared to traditional interconnects.

Chapter 2 presents a comprehensive survey of the state-of-the-art research conducted by various scholars in the field of OI and its performance comparison with electrical interconnects. It discusses the types of interconnects and the importance of OI.

Chapter 3 focuses on the modeling of transmitter and receiver circuits for OI. It begins with a study of existing transimpedance amplifier (TIA) architectures, followed by a detailed discussion of the proposed AVCF-based TIA design. On the transmitter side, current design approaches are examined, and subsequently, the modeling of a tapered buffer is presented as a key component of the transmitter circuit.

Chapter 4 begins with the in-depth discussion of the proposed AVCF-based TIA architecture. A detailed theoretical analysis is conducted, including small-signal modeling, stability analysis, and noise performance evaluation. Finally, simulation results are presented, demonstrating the effectiveness of the proposed AVCF RGC-based TIA in high-speed optical communication systems and comparing its performance with conventional TIA designs.

Chapter 5 briefly states the importance of signal integrity in high-speed optical interconnects. It focuses on how the signal integrity is used to evaluate the performance of the proposed TIA and overall OI link.

Chapter 6 presents the modeling of traditional Cu and SWCNT-B interconnects as a baseline for comparison. It then analyzes the impact of temperature variations on optical and electrical interconnects, focusing on key performance metrics such as delay, power, and signal integrity. The chapter concludes with a comparative evaluation of the thermal stability and

scalability of these interconnects in nanoscale VLSI systems.

Chapter 7 concludes the thesis by summarizing the key contributions in the modeling and performance evaluation of OI. A few suggestions regarding the future work that can be done to alleviate the current interconnect performance bottlenecks are given here.

Chapter 2

Modeling and Performance analysis of Optical Interconnect-A Review

2.1 Introduction

In deep submicron (DSM) technology nodes, global on-chip interconnects pose significant challenges for high-speed integrated circuits (ICs) in terms of speed and power dissipation [**?**]. Global interconnects refer to wiring within an IC that ranges from $500\mu m$ to $2000\mu m$ and connects functional blocks across the chip. Cu is the widely used industry standard for global levels, but these wires experience significant resistance–capacitance (RC) delay, due to which power dissipation and crosstalk increase, especially as feature sizes shrink in DSM technologies [**?**]. Due to scaling, interconnect dimensions reach mean free path (MFP), leading to electromigration and scattering effects such as grain boundary and surface roughness [**?**]. These issues are more severe in Cu interconnects due to their relatively short MFP of around $40nm$. To overcome these challenges, researchers have explored carbon-based materials like carbon nanotubes (CNTs) and graphene nanoribbons (GNRs), which possess significantly larger MFPs ($\approx 1\mu m$) [**?**, **?**]. However, despite their promising electrical and thermal properties, CNTs and GNRs face several integration and reliability challenges that limit their scalability in commercial VLSI systems [**?**, **?**]. As a result, OIs have emerged as a viable alternative and use light instead of electrical signals for communication [**?**]. OIs promise high bandwidth, low latency, and low power operation, especially over global levels [**?**]. This chapter begins by introducing the fundamentals of VLSI interconnects and emerging materials, followed by a focused discussion on the modeling and performance evaluation of optical interconnects. Key performance metrics such as propagation delay, power dissipation, and power-delay product (PDP) are analyzed in detail. Additionally, thermal modeling is addressed, considering the temperature sensitivity of photonic components, which can significantly affect the behavior of transmitters, modulators, and photodetectors in optical systems. Finally, a comparative study is provided between OIs and their electrical counterparts, namely Cu and CNTs. The comparison highlights

the advantages and trade-offs in terms of performance, scalability, fabrication complexity, and suitability for future technology nodes (22nm and beyond).

2.2 Interconnect Technologies

The evolution of on-chip interconnects has been driven by the need to overcome the limitations of traditional materials as technology scales into the DSM regime. This section categorises and reviews the major types of interconnects proposed and studied in the literature, beginning with conventional electrical options such as Cu, followed by emerging carbon-based and hybrid interconnects. The final focus is on OIs, which represent a paradigm shift for global interconnect applications.

2.2.1 Copper (Cu) Interconnect and its limitations

Cu became the industry standard for on-chip interconnects in the late 1990s, replacing aluminium due to its superior electrical conductivity ($\approx$ 40% lower resistivity) and improved resistance to electromigration [**?**]. The dual damascene process enabled the effective integration of Cu into VLSI designs, but scaling has exposed critical limitations. Below 45nm when interconnect dimensions approach the electron mean free path ($\approx 40nm$), Cu interconnects experience increased resistivity due to effects such as grain boundary scattering, surface roughness, and reduced cross-sectional area [**?**, **?**]. While fabrication techniques such as chemical mechanical planarization (CMP) are effective in smoothing the top and bottom surfaces of Cu interconnects, controlling roughness along the sidewalls remains a significant challenge. Also, since Cu lacks a native oxide layer, it requires barrier layers (like Ta or TaN) to prevent diffusion into surrounding dielectrics, consuming valuable space and complicating integration processes [**?**, **?**]. These effects increase capacitance and contribute to degraded performance in terms of delay, power consumption, and power-delay product (PDP). For instance, as the technology node scales down from $45nm$ to $13nm$, a notable increase in Cu interconnect resistance, by nearly 2.6 times, is observed due to enhanced surface and grain boundary scattering. Further miniaturisation to $7nm$ leads to an approximate 13% rise in capacitance and a 37% increase in inductance, primarily driven by tighter wire spacing and increased coupling [**?**]. These changes severely degrade interconnect performance, resulting in roughly a fivefold rise in signal delay and a 5.7$\times$ increase in energy-delay product (EDP), underscoring the growing limitations of Cu interconnects in advanced technology nodes.

To address these issues, several techniques are employed by researchers. One widely used method is repeater insertion, where buffers are added along long interconnects to divide them into smaller segments to reduce RC delays [**?**]. They convert the delay dependence from quadratic ($\propto L^2$) to approximately linear ($\propto L$). Elmore delay models are commonly used to estimate the optimal number and size of repeaters that minimise total delay [**?**]. At 45nm,

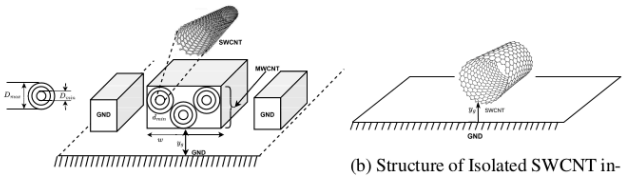
inserting 3–5 optimally sized repeaters in a 1–2mm global Cu interconnect can reduce delay by more than 50%, according to HSPICE simulations based on ITRS parameters [**?**]. For 32nm and 22nm nodes, the optimal repeater spacing decreases due to rising resistance and capacitance per unit length, often requiring 8–10 repeaters for a similar wire length to maintain minimal delay [**?**]. The tapered buffer chains are widely employed to drive long Cu interconnects efficiently, especially when the load capacitance (C_{Load}) is large and delay constraints are strict. Unlike uniform buffers, which maintain a constant size across stages, tapered buffers grow exponentially in size, typically by a factor of 2 to 4, allowing each stage to drive a proportionally larger load [**?**]. This configuration minimises the total propagation delay by balancing the capacitive load and gate drive strength across all stages.

On the materials side, introducing low-k dielectrics and air-gap structures between wires helps reduce capacitive coupling, improving both speed and power efficiency [**?**, **?**]. Additionally, replacing thick barrier layers with thinner or more conductive materials, such as cobalt (Co) or ruthenium (Ru), helps improve current flow and reduce resistance [**?**]. Together, these methods help offset the performance losses caused by continued device scaling.

2.2.2 Carbon Nanotube (CNT) Interconnects

Carbon Nanotube (CNT) interconnects have emerged as a promising alternative due to their unique electrical, thermal, and mechanical properties. CNTs, composed entirely of carbon atoms arranged in a cylindrical graphene sheet, possess high current-carrying capacity ($\approx 10^9 A/cm^2$), high thermal conductivity ($\approx 3000 W/mK$), and ballistic electron transport, making them suitable for high-performance and high-density interconnect applications [**?**]. These features make CNTs attractive for global interconnect applications in VLSI design. As an interconnect material, CNTs were first considered following the groundbreaking discovery of multi-walled CNTs (MWCNTs) by Iijima in 1991 [**?**]. This was followed by the synthesis of single-walled CNTs (SWCNTs) in the early 1990s via arc-discharge and laser ablation techniques. The structure of MWCNT and SWCNT is shown in **Figure. 2.1**.

Soon after, researchers began to explore their electrical characteristics, which revealed quasi-ballistic transport, minimal scattering, and high carrier mobility, making them ideal for



(a) Structure of MWCNT interconnect.

(b) Structure of Isolated SWCNT interconnect.

Figure 2.1: MWCNT and SWCNT Interconnect Structures.

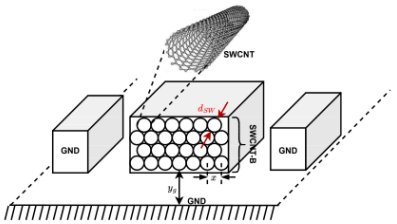


Figure 2.2: Structure of SWCNT-B interconnect.

nanoscale interconnects. Depending upon their chirality, SWCNTs can be semiconducting or metallic in nature [**?**]. The authors in [**?**, **?**] have reported the diameter of SWCNT in the range of $0.4 - 4nm$, resulting in extremely small cross-sectional areas for current flow. SWCNTs have an intrinsic resistance of 6.5 $K\Omega$, which remains constant regardless of their length, causing excess signal delay and limiting the effective current conduction required for high-speed, low-power circuits in interconnect applications.

To overcome these challenges, SWCNT bundles (SWCNT-B) are proposed that include multiple nanotubes grouped together as shown in **Figure. 2.2**. Isolated SWCNTs are aligned in parallel to collectively carry higher current and reduce the overall resistance of the interconnect line [**?**]. Bundling significantly mitigates the impact of the intrinsic quantum resistance of individual SWCNTs by allowing current to be distributed across many parallel conduction paths. This configuration improves robustness against individual tube defects and contact variability. Furthermore, the incorporation of SWCNT-B enables better scaling and thermal management in advanced nodes, where traditional metals face reliability limits due to increased resistivity and electromigration [**?**]. Due to the inherent limitations and cost constraints associated with diameter-controlled fabrication techniques, achieving CNT bundles composed exclusively of SWCNT or MWCNT with uniform diameters remains a significant challenge [**?**, **?**]. Variability in tube diameter during synthesis not only affects the electrical and thermal properties of the interconnect but also introduces inconsistencies in contact resistance and current conduction, thereby complicating the reliable integration of circuits [**?**]. On the other hand, MWCNTs are more easily synthesized with consistent diameters and fewer purity constraints but often exhibit higher resistance due to outer-shell current transport and inter-shell scattering [**?**]. Therefore, researchers mixed SWCNTs with MWCNTs within a bundle to form mixed CNT bundles (MCB) as shown in **Figure. 2.3**, which helps compensate for these deficiencies, enhancing overall current-carrying capacity while reducing the effective bundle resistance and improving resilience to defects [**?**, **?**]. To utilise CNTs for future on-chip interconnects, accurate modelling and extraction of resistance (R), inductance (L), and capacitance (C) or RLC parameters are essential, particularly to assess signal integrity, delay, and power dissipation. Compared to conventional copper interconnects, CNTs in bundled form exhibit lower resistance per unit

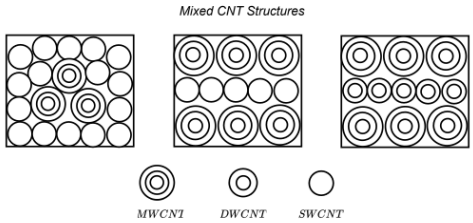


Figure 2.3: Structure of mixed CNT bundle (MCB) interconnect.

length beyond 45*nm* technology due to their ballistic or quasi-ballistic transport properties, and offer higher current-carrying capacity, thereby mitigating electromigration concerns [**?**].

The authors in [**?**, **?**] modelled a flat array of interconnects and concluded that CNTs incurred more signal delay than Cu. But the authors in [**?**] highlighted drawbacks in the analysis presented in [**?**, **?**]. Later, the authors in [**?**] highlighted the superior performance of SWCNT-B interconnects compared to Cu, particularly in terms of electrical conductivity and current-carrying capacity. However, their analysis overlooked key practical limitations, such as the low proportion of metallic SWCNTs within typical bundles and the non-ideal nature of metal-CNT contacts, both of which can significantly impact the effective resistance and reliability of the interconnect structure [**?**]. The work in [**?**] addresses these limitations, incorporating an empirical model to calculate the capacitance of SWCNT-B. Recent studies have presented more accurate capacitance estimations for CNT bundles with a width of 10*nm* [**?**].

As previously discussed, the diameter of SWCNTs significantly influences their electrical behaviour, particularly the RLC parameters critical for accurate interconnect modeling [**?**]. In their study, Nieuwoudt and Massoud introduced a diameter-dependent resistance model that differentiates between the intrinsic resistance of the nanotube and the contact resistance at the metal-CNT interface. Their findings highlight that for small-diameter SWCNTs, the contact resistance increases sharply, due to limited conduction modes and poor coupling with metal electrodes. This increased resistance not only impacts signal delay and power dissipation but also alters the overall RLC profile of the interconnect, thereby reducing performance reliability.

Temperature variations significantly influence the performance of interconnects, affecting key electrical parameters such as resistance, capacitance, and inductance, which in turn impact signal delay, power dissipation, and overall reliability of VLSI circuits [**?**]. In Cu interconnects, elevated temperatures caused by joule heating lead to increased resistivity, delay, and power dissipation, while also accelerating electromigration, a primary failure mechanism in VLSI systems [**?**]. CNT interconnects, owing to their high thermal conductivity and tolerance to current density, demonstrate superior thermal stability [**?**, **?**].

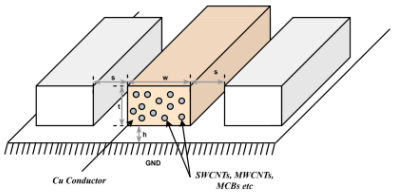


Figure 2.4: Structure of Cu-CNT composite interconnect.

2.2.3 Hybrid Interconnects

Hybrid interconnects are composite interconnect structures that combine traditional metallic conductors, such as Cu or Al, with emerging nanomaterials like SWCNTs, MWCNTs, or graphene as shown in **Figure. 2.4**. These designs aim to harness the strengths of both materials, the high electrical conductivity and process maturity of metals, and the superior thermal, mechanical, and electromigration-resistant properties of CNTs. A notable milestone was achieved by Subramaniam et al., who demonstrated that Cu-CNT composites could attain conductivity comparable to bulk Cu while offering ampacity up to 100 times greater [**?**]. The superior electromigration resistance of Cu-CNT composites, as demonstrated in [**?**], highlights their potential to deliver high performance and enhanced reliability simultaneously in on-chip interconnect applications. Cu-CNT composite interconnects are typically realized by electrodepositing Cu into the interstitial spaces of vertically aligned CNTs. In this approach, the CNT forest is first grown on a separate substrate and then transferred onto the CMOS chip to avoid the high temperatures associated with CNT synthesis. A two-stage electroplating technique is employed to fill Cu into the voids of the CNT structure, producing a composite wire with a conductive Cu matrix embedded with CNTs [**?**]. When evaluated for signal propagation delay using a distributed RLC interconnect model, Cu-CNT composites exhibit performance nearly equivalent to that of traditional Cu interconnects. Although the inclusion of CNTs leads to a marginal increase in delay compared to pure Cu, the hybrid structure still significantly outperforms pure CNT-based interconnects, particularly when kinetic inductance is considered. Notably, Cu-CNT composites show minimal sensitivity to variations in CNT kinetic inductance, thereby offering greater delay stability under fluctuating electrical conditions [**?**]. In addition to delay performance, Cu-CNT interconnects also demonstrate notable improvements in signal integrity. Owing to reduced capacitive coupling, these hybrid lines are more immune to crosstalk, a major concern in high-density, high-speed interconnect networks [**?**]. Their energy dissipation remains comparable to pure Cu due to similar parasitic capacitance values, with electrostatic capacitance dominating over the quantum component, ensuring suitability for low-power designs [**?**]. Furthermore, the fabrication method aligns well with existing CMOS processes, as the CNT growth can occur off-chip and be integrated without violating BEOL thermal limits [**?**]. Advances in analytical modeling, particularly the Matrix Rational Approxi-

mation (MRA) method, have facilitated rapid and accurate simulation of transient behavior and crosstalk noise in Cu-CNT structures, with speed-ups exceeding 100× compared to SPICE simulations [**?**]. Collectively, these features highlight Cu-CNT composites as strong candidates for near-future on-chip interconnect technology, bridging the gap between traditional metal lines and emerging carbon-based or optical solutions.

2.3 Optical Interconnects

The continuous scaling of complementary metal-oxide-semiconductor (CMOS) technology, alongside the integration of multi-core and many-core architectures, has significantly increased the demand for high-speed, energy-efficient on-chip communication. While transistor switching speeds have improved over successive technology nodes, the performance of on-chip interconnects has failed to keep pace, leading to a situation where interconnect delay and energy consumption dominate the overall system performance in nanoscale integrated circuits (ICs) [**?**, **?**]. Efficient interconnect design has thus become a critical challenge in the design of high-performance computing systems. Optical interconnects (OIs), which utilise light to transfer information, have emerged as a promising alternative, offering high bandwidth, low latency, and reduced power consumption, especially for high-performance computing (HPC), data centres, and chip-to-chip communication [**?**, **?**]. The concept of OIs was first introduced by Goodman *et al.* with a focus on backplane and board-level communication environments [**?**]. OI aims to carry greater volumes of data across a distance without much interference and noise [**?**]. Unlike electrons, photons do not experience resistive losses or RC-limited delays when propagating through optical waveguides. Moreover, optical signals are immune to electromagnetic interference (EMI) and exhibit negligible crosstalk, enabling more reliable high-density communication channels within modern chips [**?**].

The advent of silicon photonics has further accelerated the development of on-chip OIs, as silicon-based optical components such as waveguides, modulators, and photodetectors can now be fabricated using CMOS-compatible processes [**?**]. Techniques like wavelength division multiplexing (WDM) facilitate massive parallelism by allowing multiple data channels to be transmitted simultaneously through a single optical waveguide, enhancing bandwidth scalability without increasing the physical footprint [**?**]. However, despite their theoretical advantages, on-chip OIs are not without challenges. Efficient electrical-to-optical (E/O) and optical-to-electrical (O/E) conversions introduce latency and power overheads. The integration of compact, energy-efficient light sources presents a challenge, and the precise alignment of photonic components further complicates the fabrication process. Therefore, a systematic evaluation and modeling of each component, transmitter, waveguide, and receiver, is essential to accurately assess the performance benefits and trade-offs of OIs compared to traditional metal-based systems [**?**]. The block diagram of the OI system is depicted in **Figure. 2.5** showcases optical transmitter, waveguide, and receiver blocks. Each of these blocks plays a critical role in

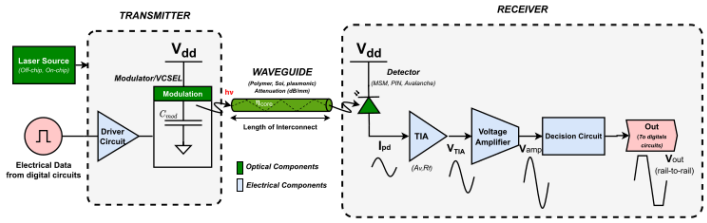


Figure 2.5: Components of the Optical Interconnect.

determining the overall efficiency, speed, and scalability of OI systems.

For instance, in Haurylau *et al.* [**?**], the authors modeled the entire OI link at the system level, focusing on performance comparison with electrical interconnects for global and intermediate communication lengths. The modeling framework considered an off-chip laser source combined with an electro-optic (EO) modulator as the transmitter, silicon strip waveguides for signal propagation, and a germanium photodetector as the receiver. The study emphasized analytical models for delay, power consumption, and bandwidth, providing a foundational performance comparison framework. This work established that OIs could potentially outperform Cu interconnects beyond critical interconnect lengths, primarily due to their lower propagation loss and higher bandwidth density. The authors in [**?**] focused extensively on device-level modeling of OI components, analysing the energy and bandwidth constraints critical to practical deployment. The transmitter was modeled using carrier-injection-based silicon modulators, considering their drive voltage, modulation bandwidth, and capacitance. The propagation medium is assumed to be a low-loss silicon waveguide with constant group velocity and minimal dispersion. The receiver was modeled as a combination of photodiodes and transimpedance amplifiers (TIAs), with detailed analysis of photodetector responsivity, capacitance, and noise performance.

In their predictive modeling study, Chen *et al.*analyzed CMOS-compatible OIs using a combination of circuit-level and system-level modeling techniques. The transmitter was modeled as a Mach-Zehnder Modulator (MZM) driven by an off-chip laser source. Signal propagation was analyzed using SOI-based silicon waveguides, incorporating propagation loss and coupling efficiency into the model. At the receiver side, germanium photodiodes paired with CMOS-based TIAs were modeled to quantify signal conversion efficiency and power consumption. The study presented predictions for propagation delay, energy consumption, and bandwidth across various interconnect lengths, suggesting that OIs are preferable to electrical interconnects for longer interconnect paths. Shacham *et al.*explored architectural-level modeling in the context of photonic networks-on-chip (NoCs) [**?**]. Their approach incorporated microring resonator-based modulators as the transmitter technology, silicon waveguides for optical routing, and photodetectors with TIAs at the receiver. The modeling framework evaluated link

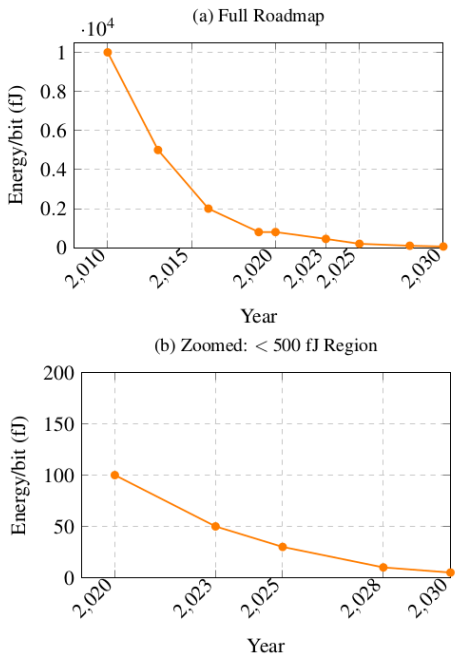


Figure 2.6: ITRS/IRDS optical interconnect energy-per-bit roadmap from 2010-2030. (a) Full view showing overall scaling trends. (b) Zoomed view emphasizing the sub-200 fJ/bit IRDS 2020/2023 targets critical for next-generation optical I/O systems.

latency, power dissipation, and bandwidth scalability, emphasizing the use of wavelength division multiplexing (WDM) to achieve high bandwidth density. This study highlighted the importance of network topology optimization and component-level co-design to fully exploit the advantages of OIs within complex multi-core processor architectures.

2.3.1 Performance Requirements of OI

As multicore and many-core architectures advance, the limitations of traditional metal interconnects, particularly in terms of bandwidth density, energy efficiency, and latency, have intensified the shift towards OIs. Leveraging the high bandwidth and low power characteristics of photonics, OIs are increasingly considered essential for meeting the communication demands of next-generation processors [**?**, **?**].

The International Roadmap for Devices and Systems (IRDS), along with various research studies, has established aggressive performance targets for optical interconnects (OIs). Earlier

projections indicated that off-chip OIs should achieve energy consumption of $\leq$100 fJ/bit, with reductions towards 50 fJ/bit by 2022 [**?**, **?**]. For on-chip OIs, the target range was set within 50-200 fJ/bit, with future goals aiming for 10-30 fJ/bit by 2022 [**?**, **?**] as shown in **Figure. 2.6** . Looking forward to 2025 and beyond, both industry forecasts and academic trends predict that on-chip OIs may need to operate at $\leq$5 fJ/bit to meet the stringent demands of ultra-dense processors and AI accelerators [**?**, **?**]. Furthermore, aggregate on-chip bandwidth is projected to exceed 1 Pbps (1000 Tbps) within the next five years, driven by high-performance computing (HPC) and data center on-chip architectures [**?**, **?**]. In parallel, latency requirements are becoming increasingly stringent, with end-to-end delays for on-chip optical paths targeted at below $5ps/mm$. To meet future requirements, ongoing research focuses on: Advanced modulators with sub-femtojoule energy per bit. High-responsivity photodetectors integrated with low-noise transimpedance amplifiers (TIAs). Thermal tuning reduction techniques to minimize power consumption associated with microring resonators and wavelength stabilization [**?**]. In summary, achieving sub-5 fJ/bit energy efficiency and multi-petabit-per-second bandwidth within the next few years is not just a research goal but an industry necessity for sustaining Moore's Law at the system level.

2.4 Components of Optical Interconnect

A typical OI system comprises a continuous-wave (CW) laser source, an optical modulator, a waveguide (or optical fibre), a photodetector, and receiver electronics. Electrical data signals are converted into optical signals using the modulator, transmitted through optical waveguides employing techniques such as WDM, and reconverted to electrical signals at the receiver end via photodetection [**?**, **?**].

2.4.1 Transmitter

A transmitter at the near end is composed of a light modulator or light emitter [**?**, **?**] with its respective driver circuits [**?**]. The light source can be classified based on its physical integration: can be **off-chip**, wherein the laser is physically located outside the silicon chip, or **on-chip**, wherein the laser is integrated directly onto the silicon chip using monolithic or hybrid integration techniques. Distributed feedback (DFB) lasers and vertical-cavity surface-emitting lasers (VCSELs) are commonly used as off-chip sources due to their stable output and mature fabrication technologies [**?**]. The off-chip approach simplifies thermal management and avoids integration issues. However, coupling losses and alignment complexity are inherent drawbacks. In contrast, on-chip lasers are integrated directly onto the silicon chip through monolithic or heterogeneous integration techniques. III-V materials such as InP or GaAs are bonded or epitaxially grown onto silicon substrates to create compact, integrated laser sources. This approach eliminates coupling losses and reduces system complexity but presents significant fabrication

challenges and thermal management issues [**?**]. The choice between on-chip and off-chip light sources impacts the overall design, scalability, and energy efficiency of the OI system. The

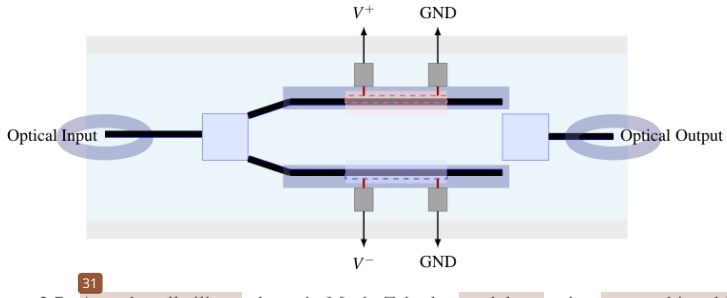


Figure 2.7: A push-pull silicon photonic Mach–Zehnder modulator using reverse-biased PN junction phase shifters in both arms.

optical modulator encodes the electrical data onto the optical carrier by modulating properties such as amplitude, phase, or frequency, as shown in the **Figure. 2.7**. Optical modulators can be broadly classified based on the physical mechanism employed for modulation. The major categories include electro-refractive modulators, electro-absorption modulators, and thermo-optic modulators. Key modulator types modeled in literature include:

- **Electro-Refractive Modulators**: Electro-refractive modulators rely on electrically induced changes in the refractive index to phase-modulate light. Two dominant effects govern this mechanism, the **Pockels effect**, which provides a linear relationship between the electric field and refractive index, and the **Kerr effect**, which yields a quadratic response. While Pockels effect-based modulators in $LiNbO_3$ have long dominated bulk electro-optic devices, recent breakthroughs in thin-film lithium niobate on insulator (LNOI) platforms have demonstrated integrated modulators with sub-volt V_π, bandwidths exceeding 100 GHz, and CMOS-compatible processing flows [**?**,**?**]. However, because silicon lacks a native Pockels effect, pure electro-refractive modulation remains impractical in silicon photonics without material integration. Hybrid approaches, such as bonding $BaTiO_3$ or using strained Si-Ge, are being explored to enable this functionality on-chip [**?**]. This phase change, when combined with interferometric techniques, such as those employed in **Mach–Zehnder Interferometers (MZIs)** or directional couplers can be converted into amplitude modulation by creating an interference pattern between two optical paths. The MZI modulator has its roots in classical optics, but its adaptation to integrated photonics began in the 1990s with the rise of silicon-on-insulator (SOI) platforms. Early implementations used carrier injection in p-n or p-i-n junctions embedded in one arm of the interferometer to induce a refractive index change, resulting in a phase shift [**?**]. MZIs

offer high linearity and broad bandwidth, making them suitable for high-speed applications [**?**]. With advances in CMOS-compatible silicon photonics, carrier-depletion-based MZIs became popular due to faster modulation speeds and reduced power consumption. This approach allowed operation in the tens of gigahertz regime, as shown by Xu *et al.* [**?**], who demonstrated a high-speed depletion-mode silicon MZI modulator operating at 10 Gbps with a compact footprint [**?**]. In Chen *et al.* [**?**], the MZI was modeled using an equivalent RC circuit, accounting for the modulator capacitance, junction resistance, and driver loading. The energy per bit was estimated using:

$$E_{\text{bit}} = \frac{1}{2} C_{\text{mod}} V_{\text{drive}}^2$$

where C_{mod} is the modulator capacitance and V_{drive} is the applied voltage swing. This model helps evaluate dynamic power in systems using MZI-based transmitters. Miller [**?**] further elaborated on the theoretical limits of modulator performance in silicon photonics and derived expressions relating $V_\pi L$ (modulator efficiency) to achievable bandwidth and energy constraints, highlighting trade-offs between size, efficiency, and drive voltage. The work by Thomson *et al.* [**?**] provided a technology roadmap for silicon photonics, identifying MZIs as reliable, manufacturable modulators suitable for data rates exceeding 25 Gbps. They also explored multi-level signaling (e.g., PAM4) using MZIs for increased bandwidth efficiency. **Microring Resonator Modulators (MRRs)** are compact, highly energy-efficient optical devices that perform signal modulation through resonance-based wavelength filtering. Due to their small footprint, compatibility with silicon photonics, and intrinsic support for wavelength division multiplexing (WDM), MRRs have emerged as a promising solution for bandwidth-constrained and power-sensitive on-chip optical interconnect (OI) systems. MRRs are inherently suitable for WDM systems, as each ring can be tuned to a distinct wavelength channel, enabling parallel data transmission. Due to their small footprint (typically $< 100\ \mu\text{m}^2$) and low energy-per-bit (on the order of a few femtojoules), MRRs are particularly valuable in dense, short-reach on-chip OI architectures, such as photonic networks-on-chip (NoCs). However, they exhibit narrow spectral linewidths (limited bandwidth), strong sensitivity to temperature variations (approximately 0.1 nm/°C), and require precise resonance alignment and active thermal tuning, which can increase control complexity and static power overhead [**?**]. Despite these limitations, MRRs have been widely adopted in research for scalable optical modulation. Their compactness, CMOS compatibility, and efficient WDM operation make them essential for high-bandwidth, power-constrained interconnect applications in multicore processors and data centres [**?**, **?**, **?**, **?**].

- **Electro-Absorption Modulators (EAMs)**: Electro-absorption modulators (EAMs) operate by exploiting the electro-absorption effect, where the absorption coefficient of a semiconductor material changes under an applied electric field, enabling direct modu-

lation of optical signals. Typically based on multiple quantum well (MQW) structures fabricated from III–V compound semiconductors such as InGaAsP, EAMs provide high-speed operation (10-50 Gbps), low drive voltages (1-2 V), and a compact footprint, making them suitable for dense photonic integration [**?**]. In the context of on-chip OIs, EAMs offer low energy-per-bit transmission and are amenable to hybrid integration with silicon photonics platforms. However, they tend to exhibit higher insertion losses compared to MZI modulators and require careful control of bias voltage to achieve optimal extinction ratios [**?**]. Additionally, their reliance on III–V materials complicates full CMOS compatibility and fabrication scalability [**?**].

Despite these limitations, EAMs are considered viable candidates for short-reach, low-power optical links in future hybrid electronic-photonic systems. These modulators have demonstrated modulation speeds exceeding 50 Gbps, extinction ratios above 10 dB, and energy consumption as low as 50–100 fJ/bit, making them ideal for on-chip high-speed optical links [**?**]. However, their lack of compatibility with standard CMOS fabrication processes presents a significant integration challenge. To overcome this, researchers have explored heterogeneous integration techniques, such as wafer bonding, flip-chip assembly, and epitaxial growth, to integrate III-V EAMs with silicon photonics [**?**].

In parallel, germanium-based electro-absorption modulators have gained attention due to their improved compatibility with silicon processes. For instance, Liu *et al.* demonstrated a high-speed Ge-Si EAM achieving 56 Gbps modulation with compact footprint and promising CMOS integration potential [**?**]. Similarly, Lee *et al.* [**?**] developed a strained GeSn-based EAM on silicon, which exhibited enhanced absorption near 1550 *nm* and lower drive voltage due to its tunable direct bandgap.

- **Thermo-Optic Modulators:** Thermo-optic modulators exploit the temperature dependence of the refractive index in materials. Silicon, with its high thermo-optic coefficient ($dn/dT \approx 1.86 \times 10^{-4}\,\mathrm{K}^{-1}$), is particularly well-suited for this modulation method [**?**]. By precisely controlling the temperature, a phase change can be induced over a waveguide segment. However, the key drawback of thermo-optic modulation is its relatively slow response time, dictated by thermal time constants, making it more suitable for tuning or reconfigurable devices rather than high-speed data modulation. Advances in integrated micro-heaters and thermal isolation structures continue to improve the response speed and stability of these modulators [**?**].

2.4.1.1 Driver Circuits for Optical Modulators

Optical modulators in silicon photonic systems present capacitive loads that require high-speed, energy-efficient driver circuits to convert digital electrical signals into analog voltage or current levels suitable for modulation. The performance of these drivers directly influences the

bandwidth, energy-per-bit, and signal integrity of the overall OI. Optical modulators typically present a capacitive load to the driver circuitry, with capacitances ranging from a few femtofarads (fF) to several hundred fFs, depending on the device structure and integration technology [**?**]. To achieve high-speed data transmission and maintain signal integrity, these modulators must be driven by optimized electrical circuits capable of providing sufficient voltage swing, bandwidth, and energy efficiency. The capacitive nature of modulators significantly impacts the bandwidth of the modulator driver interface. The $3-dB$ bandwidth of the system can be approximated using the RC time constant as:

$$f_{-3\,\mathrm{dB}} = \frac{1}{2\pi R_d C_{\mathrm{mod}}}$$

where R_d is the output resistance of the driver and C_{mod} is the modulator capacitance. For high-speed operation (e.g., $\geq 25\,$Gbps), both the driver design and the parasitic capacitance must be carefully optimized to reduce latency and maintain signal fidelity. To efficiently drive the capacitive load of optical modulators, especially in high-speed interconnects, CMOS-based driver circuits are commonly employed due to their low cost, scalability, and compatibility with digital logic processes [**?**]. The primary challenge in designing CMOS drivers lies in balancing the trade-offs between bandwidth, voltage swing, power efficiency, and signal integrity. The most fundamental form of a CMOS driver is an inverter or buffer chain, where a digital logic signal is converted into a rail-to-rail output capable of charging the modulator capacitor. However, due to the capacitive load of optical modulators (e.g., $C_{\mathrm{mod}} = 10-100\,$fF), a simple inverter is insufficient for high-speed operation. Therefore, tapered buffer chains, consisting of a cascade of inverters with exponentially increasing transistor sizes, are used to minimize propagation delay and maximize bandwidth [**?**]. The sizing of a tapered buffer chain follows the principle introduced by Sutherland and Sproull, where the optimal number of stages N and size multiplication factor f are determined as [**?**]:

$$f = \sqrt[N]{\frac{C_{\mathrm{mod}}}{C_{\mathrm{in}}}}, \quad t_{p,\mathrm{total}} \approx N \cdot t_p(f)$$

here, C_{in} is the input gate capacitance of the smallest inverter, and $t_p(f)$ is the stage delay with fanout f. Tapered buffers are especially suitable for driving high-capacitance depletion-mode MZI modulators, achieving data rates in the range of 10–25 Gbps with rail-to-rail swing [**?**]. Differential drivers, especially those based on current-mode logic (CML), are widely used for OIs targeting speeds above 25 Gbps. Existing designs for transmitter driver circuits are discussed in **section 3.2** where transmitter driver circuit is modelled with corresponding analytical equations.

2.4.2 Waveguides

Optical waveguides are critical passive components used to guide light in on-chip OI, enabling high-speed, low-loss signal transmission within integrated photonic circuits. They confine light through total internal reflection or photonic bandgap mechanisms and serve as the primary medium for linking photonic devices such as modulators, multiplexers, and detectors. Several types of waveguides are commonly used in on-chip OI platforms, each offering unique trade-offs in loss, integration density, fabrication ease, and spectral bandwidth. **Silicon-on-Insulator (SOI)** waveguides dominate modern CMOS-compatible photonics due to their high refractive index contrast between the silicon core ($n \approx 3.48$) and the silicon dioxide cladding ($n \approx 1.44$). This enables tight optical confinement and a compact footprint. Two principal geometries are employed:

- **Strip waveguides**: These are fully etched silicon structures offering strong mode confinement and compact layout, making them ideal for dense photonic integration. However, the tight confinement increases sensitivity to sidewall roughness, leading to higher scattering losses [**?**].
- **Rib waveguides**: These are partially etched, preserving a silicon slab beneath the core. This reduces interaction with rough sidewalls, thereby lowering propagation loss while maintaining single-mode operation and better fabrication tolerance [**?**].

SOI waveguides offer high integration density and are suitable for short-range interconnects. However, they are susceptible to thermal variations due to silicon's high thermo-optic coefficient [**?**, **?**].

Silicon Nitride (Si_3N_4) waveguides have emerged as a compelling alternative to silicon-based waveguides for passive photonic circuits, primarily due to their ultra-low propagation losses, typically less than $0.1\,\mathrm{dB/cm}$—and their negligible nonlinear absorption. While the refractive index contrast between Si_3N_4 (n ≈2.0) and SiO_2 (n ≈1.44) is lower than that of SOI platforms, resulting in slightly larger bend radii and mode areas, this trade-off is often acceptable for applications prioritising low-loss and broadband performance. Si_3N_4 waveguides are particularly well-suited for passive routing, delay lines, and wideband filters due to their wide transparency window (from visible to mid-infrared) and excellent thermal stability. These properties make them ideal candidates for WDM, high-fidelity signal distribution, and long-reach photonic paths in on-chip OIs [**?**].

Polymer Waveguides waveguides, typically with $n_{\mathrm{core}} \approx 1.6$ and $n_{\mathrm{cladding}} \approx 1.1$, are utilised for long-distance on-chip clock distribution networks due to low refractive index contrast. These waveguides exhibit low propagation loss, high thermo-optic tunability, and flexibility in fabrication. However, their lower index contrast results in larger mode areas and bend radii, which limit miniaturization. Polymer waveguides are being explored in hybrid systems for power-efficient global interconnects [**?**]. In the domain of *on-chip OIs*, polymer waveguides

have attracted attention for implementing long-distance global links and clock distribution networks. Additionally, polymers exhibit high thermo-optic coefficients (up to $2 \times 10^{-4}\,\mathrm{K}^{-1}$), making them suitable for tunable and reconfigurable photonic systems. Hybrid integration of polymers with silicon photonics is also being explored to combine the dense routing capability of SOI platforms with the low-loss, thermally tunable, and fiber-aligned advantages of polymer layers. Consequently, polymer waveguides continue to play an essential role in the development of energy-efficient, large-scale photonic interconnect fabrics [**?**].

Photonic Crystal Waveguides (PhCWs) employ periodic dielectric structures to confine and guide light using photonic bandgap effects. By introducing line defects in an otherwise periodic lattice, PhCWs can support highly confined optical modes and enable ultra-compact integration. A key advantage of PhCWs is their ability to produce slow light effects, significantly reducing the group velocity of light, which enhances light-matter interactions and is particularly beneficial for nonlinear optical applications and compact delay lines. However, despite these theoretical advantages, PhCWs remain highly sensitive to fabrication imperfections. Variations in hole size, lattice period, and sidewall roughness can induce strong scattering, resulting in increased insertion loss and limited bandwidth. These factors currently restrict their use in low-loss, large-scale optical interconnects [**?**]. Despite their theoretical advantages, PhCWs are extremely sensitive to fabrication imperfections and tend to exhibit higher scattering losses, which limits their adoption in practical OI [**?**].

Plasmonic waveguides utilise surface plasmon polaritons (SPPs), electromagnetic waves coupled to free electron oscillations at the interface between a metal or heavily doped semiconductor and a dielectric. These waves enable light confinement beyond the diffraction limit, allowing ultra-compact photonic components [**?**]. However, this comes at the cost of significant propagation loss, as SPPs dissipate energy into the metal, severely limiting transmission distances. Propagation lengths are typically below $100\mu m$, and often not exceeding $1cm$ for highly confined SPP modes. Additionally, energy-per-bit increases exponentially with interconnect length, rendering plasmonic waveguides inefficient for global signaling. Nevertheless, their deep sub-wavelength confinement and inherently low crosstalk make them promising for short-range links, such as modulator-to-detector connections in ultra-dense photonic circuits [**?**].

Slot Waveguides are a relatively recent innovation in silicon photonics, first introduced by Almeida *et al.* in 2004 [**?**]. Unlike conventional waveguides that confine light within high-index cores, slot waveguides utilize a narrow low-index region, typically around 50 nm wide, sandwiched between two high-index materials. Due to the discontinuity in the electric field at the high- and low-index interface, the optical field becomes highly concentrated in the low-index slot, allowing strong light confinement in sub-wavelength regions. This field enhancement enables the integration of compact and energy-efficient photonic components on-chip, addressing the mismatch between electronic and photonic feature sizes. Slot waveguides have been successfully implemented in devices such as ring resonators and directional couplers, proving their compatibility with dense photonic integration [**?**]. Various strategies have been proposed to ex-

tend the transmission length of slot waveguides. Xieng *et al.*combined slot confinement with long-range surface plasmon polaritons (SPPs) at a metal-dielectric interface [**?**], achieving a propagation length of up to $14.55\,mm$, although the inclusion of silver poses incompatibility issues with CMOS [**?**]. Further work by Li *et al.*demonstrated a III–V semiconductor-based slot waveguide using InGaAsP with a propagation loss of $1.5\,dB/cm$ at $1.55\mu m$ and a $650\,nm$ confinement region [**?**]. This shows the potential for integrating slot waveguides into PICs beyond silicon. Bending performance, often a limitation in total internal reflection (TIR) based guides, was investigated by Anderson *et al.*and Ishizaka *et al.*, who proposed solutions for improving transmission efficiency at sharp bends from 33.8% to 84.2% in slot-based interconnects [**?**, **?**].

2.4.3 Receiver

The receiver block at the far end comprises a transimpedance amplifier (TIA) as the primary front-end receiver to convert the small current of the detector into a corresponding voltage [**?**]. This voltage is amplified by a voltage amplifier and is fed to a decision circuit that provides a digital voltage output to the back-end circuits for processing of the received data [**?**]. The receiver block is critical in OI design as it affects the system performance in terms of data rate, sensitivity, and noise. Designing a receiver block is tedious as it requires several trade-offs between gain, bandwidth, input-referred noise, and power consumed [**?**].

2.4.3.1 Detectors

Optical detectors play a pivotal role in on-chip optical interconnect systems by converting optical signals into electrical current. The design of these photodetectors must balance multiple trade-offs, including responsivity, bandwidth, capacitance, dark current, and compatibility with CMOS processing [**?**]. The detector must operate at high speed, with minimal power consumption and footprint, to enable scalable photonic integrated circuits (PICs). Optical detectors operate based on the *internal photoelectric effect*, wherein incident photons with energy $h\nu$ greater than the semiconductor bandgap E_g excite electrons from the valence band to the conduction band. This results in the generation of electron-hole pairs (EHPs). When an electric field is present, either through a built-in potential (e.g., in a *p-i-n* junction) or an externally applied bias, the EHPs are separated and collected, producing a photocurrent that is proportional to the incident optical power (IOP) [**?**]:

$$I_{\text{pd}} = R \cdot P_{\text{opt}} \tag{2.1}$$

where I_{pd} is the generated photocurrent (A), and R is the responsivity of the photodetector (A/W), P_{opt} is the IOP in watts. The detector's speed of response is primarily limited by three factors: (i) the **quantum efficiency** of the photodetector, which governs how many EHPs are generated per incident photon; (ii) the **transit time** of carriers across the depletion region,

which affects the temporal response; and (iii) the **RC time constant** resulting from the photodiode's junction capacitance and the input impedance of the subsequent TIA. For high-speed on-chip OIs, minimising the photodiode's capacitance and maximising bandwidth while maintaining high responsivity and low dark current is essential to ensure energy-efficient and reliable data conversion at multi-gigabit rates [**?**].

Photodetectors must meet stringent requirements in terms of speed, responsivity, capacitance, power consumption, and compatibility with CMOS fabrication. Among the most widely adopted photodetectors are P-N, or PIN commonly fabricated using semiconductor materials such as silicon (Si), germanium (Ge), and III–V compounds, as well as Schottky junctions. To meet the demands of low-power and high-speed applications, a key design objective is the reduction of junction capacitance, often achieved by scaling down the device dimensions to the nanoscale. In the domain of silicon photonics, Ge-based detectors on Si substrates are among the most widely implemented structures. These devices are typically configured as either PIN photodiodes or avalanche photodiodes (APDs) [**?**]. While APDs offer enhanced sensitivity compared to standard PIN detectors, they suffer from increased noise and reduced bandwidth. Additionally, APDs require high operating voltages and precise voltage control, which significantly limit their practicality in integrated systems [**?**]. **Ge-on-Si)** photodiodes, which offer high responsivity (> 0.8 A/W) and broad absorption in the near-infrared range (1300-1600 nm), making them ideal for Si photonics platforms.

Metal–semiconductor–metal (MSM) photodetectors, characterised by interdigitated Schottky contacts and lateral electric fields, offer simple fabrication and low capacitance, making them suitable for ultra-fast response; however, their responsivity is typically lower than PIN structures [**?**]. Ultimately, the choice of photodetector is driven by application-specific requirements, with particular emphasis on CMOS compatibility, bandwidth, power efficiency, and seamless integration with transimpedance amplifier (TIA) circuitry.

2.4.3.2 Transimpedance Amplifiers (TIA)

Transimpedance amplifiers (TIAs) serve as the critical interface between photodetectors and digital processing stages in optical receivers. They convert weak photocurrents into usable voltage signals while preserving signal integrity, bandwidth, and noise performance. In the context of on-chip optical interconnects, where data rates exceed 25 Gbps and energy efficiency is paramount, TIA design must balance low input impedance, high transimpedance gain, and CMOS process compatibility. As described by Razavi [**?**], a TIA employs negative feedback to achieve a low input impedance, thereby minimizing the voltage swing across the photodiode and suppressing the effects of parasitic capacitance. The transimpedance gain is typically defined as $R_T = V_{\text{out}}/I_{\text{in}}$, and under high open-loop gain conditions, it closely approximates the value of the feedback resistor R_F. Early TIA designs employed resistive feedback architectures, which provided simplicity but were limited by the gain-bandwidth trade off. The

introduction of the *regulated cascode* (RGC) topology significantly improved bandwidth performance by lowering input impedance and isolating the photodiode from capacitive loading. Razavi [?] proposed RGC-based TIAs with inductive peaking to further enhance bandwidth. Inductive peaking extends bandwidth by introducing a second order network at the input, while current-biasing techniques across R_F improve voltage headroom and open-loop gain.

There are primarily two major topologies of TIAs *i.e.*, open loop TIAs and feedback TIAs. The most common open loop and shunt feedback TIAs are common gate (CG) and common source (CS) TIA with shunt resistor, respectively [?]. Several open loop and closed TIA structures incur tight trade-offs [?] between gain, noise, bandwidth and power consumption. Therefore, structural modifications are incorporated by researchers to come up with new TIA topologies such as shunt feedback TIAs [?], regulated gain cascode (RGC) TIA [?], common source (CS) shunt feedback TIA [?], inverter-based TIA [?], cross-coupled current conveyer TIA [?], active voltage-current feedback (AVCF) TIA [?]. Each topology allows trade-offs between the design parameters according to the specifications set for the design.

Bandwidth enhancement techniques such as gain boosting [?], [?], inductive peaking [?], [?], capacitive coupling [?], capacitive degeneration [?], [?], and feedback techniques [?], [?], [?] are applied to existing TIA topologies for performance improvements. Various gain boosting techniques are reported in the literature, such as positive feedback gain enhancement scheme [?], cascading multiple stages [?], and cascoding structures [?]. In positive feedback, gain is enhanced by reducing output conductance, but at the expense of system stability. The cascading of amplifiers increases the gain, but at the expense of power consumption and area. A Self-cascode structure increases the gain, but at the expense of voltage headroom. M. Seifouri *et al.* [?] propose a low-power optical TIA optimised for high-speed optical communication systems. Their design achieves a high transimpedance gain of 80 $dB\Omega$ and a bandwidth of approximately 12 GHz, which is suitable for multi-Gbps data rates. The TIA incorporates an active voltage-current feedback mechanism to ensure low input impedance ($\approx$20 $dB\Omega$), enhancing stability and bandwidth. Power consumption is kept low at around 1.2 mW, making it ideal for energy-efficient integrated optical receivers. Their analysis demonstrates that this TIA meets the stringent requirements of next-generation optical networks, balancing gain, bandwidth, input matching, and power efficiency effectively. In optical receivers, the TIA must balance bandwidth (typically 70% of the data rate) and input-referred noise current. For instance, a 40 Gbps receiver requires $\sim$28 GHz bandwidth. The core amplifier often consists of a common-source stage with inductive peaking, possibly followed by a source follower to buffer the output. Noise analysis reveals that both the core amplifier and feedback resistor R_F contribute to the total input-referred noise current. Razavi notes that to maintain $I_{n,\text{in}} < 10\,\text{pA}/\sqrt{\text{Hz}}$ with $R_F = 1\,\text{k}\Omega$, the core voltage noise must be under $9.1\,\text{nV}/\sqrt{\text{Hz}}$ [?]. In conclusion, TIA-based optical receivers are continuously evolving to meet the demands of high-speed, low-energy OI. Their performance is dictated by careful trade-offs among gain, noise, bandwidth, and power, with architectural innovations enabling improved integration and scalability at the

nanometer scale in CMOS.

2.4.4 Open-Loop vs. Closed-Loop TIAs

2.4.4.1 Open-Loop TIA

In an open-loop configuration, the photocurrent from the detector is directly translated into voltage across the input device or load without employing feedback. The effective transimpedance can be expressed as:

$$Z_T \approx g_m R_L, \tag{2.2}$$

where g_m is the transistor transconductance and R_L is the load resistance. Since the photodiode with capacitance C_d is connected to this high input impedance, the bandwidth is limited by the input RC pole:

$$\omega_p \approx \frac{1}{R_{in} C_d}. \tag{2.3}$$

Here, R_{in} is relatively large (often on the order of $1/g_m$), resulting in a narrower bandwidth. The absence of feedback also means that the input node voltage swing is not constrained, leading to potential nonlinearities if the photocurrent i_{pd} induces large voltage variations. This effect worsens at higher data rates, as large voltage excursions across the photodiode degrade linearity and increase distortion.

From a noise perspective, the dominant contribution comes from the load resistor and device thermal noise, with an equivalent input-referred noise current given by:

$$i_{n,eq}^2 \approx \frac{4kT}{R_L}. \tag{2.4}$$

Because the gain and bandwidth depend heavily on device parameters, process and temperature variations strongly affect performance. Consequently, open-loop TIAs are typically reserved for low-data-rate or low-power systems where simplicity is prioritized over high bandwidth and linearity.

2.4.4.2 Closed-Loop TIA

In contrast, the closed-loop topology employs negative feedback, typically through a resistor R_f, wrapped around a high-gain amplifier. This feedback maintains the input node at a virtual ground, reducing the input impedance to:

$$R_{in} \approx \frac{R_f}{1 + A_0}, \tag{2.5}$$

where A_0 is the open-loop gain of the core amplifier. The transimpedance in this case is largely determined by the feedback resistor:

$$Z_T \approx R_f, \tag{2.6}$$

making the gain predictable and less sensitive to device variations. Since the effective input impedance is lowered by the loop gain, the input pole shifts to:

$$\omega_p \approx \frac{1}{R_f C_d (1 + A_0)}, \tag{2.7}$$

which represents a significant bandwidth improvement over the open-loop case.

Noise performance is also improved because the feedback resistor dominates the input-referred noise, while the low input impedance suppresses the effect of detector capacitance. The input-referred noise current can be approximated as:

$$i_{n,eq}^2 \approx \frac{4kT}{R_f}. \tag{2.8}$$

Additionally, since the voltage swing at the input is reduced approximately by a factor of $(1 + A_0)$, closed-loop TIAs exhibit superior linearity and reduced distortion.

The trade-off lies in the requirement for the amplifier core to provide both high gain and wide intrinsic bandwidth. To ensure stable operation, the amplifier's bandwidth must typically exceed 70% of the target data rate, which often leads to increased power consumption and circuit complexity.

Open-loop TIAs are simple and power-efficient but suffer from high input impedance, bandwidth limitations, and reduced linearity. Closed-loop TIAs, by contrast, employ feedback to achieve low input impedance, stable gain, wide bandwidth, and improved noise performance, making them the preferred choice for high-speed optical receiver front-ends. The choice between the two depends on the application: open-loop for short-range, low-data-rate systems, and closed-loop for high-speed multi-gigabit links.

2.5 Existing TIA Designs

A variety of transimpedance amplifier (TIA) architectures have been proposed to achieve high bandwidth, low noise, and stable gain in optical receivers. The choice of topology depends on the desired data rate, photodetector capacitance, and trade-offs between power and complexity. This section reviews TIA designs reported in the literature, providing an in-depth explanation of their operating principles and performance trade-offs.

2.5.1 Passive Resistive Load TIA (High-Impedance Front-End)

The simplest form of TIA is a passive resistive load, where a single resistor is used to convert the photodiode's current to a voltage, as depicted in **Figure. 2.8**. In this approach, the transimpedance equals the resistor value R. However, the photodiode's capacitance C_{pd} and the

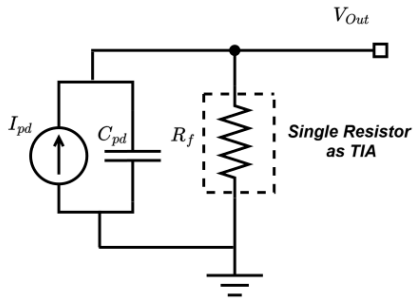


Figure 2.8: Resistor as TIA

resistor create an RC-limited bandwidth:

$$f_{3\text{dB}} \approx \frac{1}{2\pi RC_d}. \tag{2.9}$$

This means a higher gain or larger R directly reduces the bandwidth for a given C_{pd} [**?**]. For example, if very high gain and a large C_{pd} are required, the bandwidth becomes prohibitively low [**?**]. Due to this trade-off, passive resistive TIAs are only practical in low-speed or DC applications such as sensitive photodiode measurements or very low-frequency links. They offer ultra-low power consumption and excellent simplicity/stability, as there are no active devices to introduce noise or instability. However, their noise performance is poor for high-speed use [**?**]. In summary, while a resistive load provides a baseline solution for current-to-voltage conversion, its gain–bandwidth product is severely limited by the photodiode capacitance; thus, it is rarely used in modern high-speed optical receivers, except as a reference or in very low-bandwidth scenarios.

2.5.2 Common-Gate (CG) TIA

The common-gate (CG) TIA as shown in **Figure. 2.9** employs a transistor or a pair of transistors in a CG configuration as the input stage. In CMOS, the photodiode current (I_{pd}) is injected into the source of an NMOS whose gate is biased at a fixed DC voltage. The key advantage is the inherently low input impedance, approximately

$$R_{\text{in}} \approx \frac{1}{g_m}, \tag{2.10}$$

where g_m is the transconductance of a transistor. By making $1/g_m$ small, the C_{pd} is effectively isolated from the input node, greatly suppressing the RC time constant that limits bandwidth [**?**]. The transimpedance is set primarily by the load (or current mirror) at the drain,

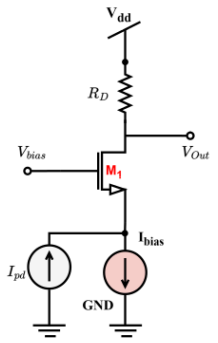


Figure 2.9: Common gate TIA topology

while input impedance is set by g_m [?]. CG TIAs are unconditionally stable and can be very broadband and power-efficient for high-speed operation, and are widely used as first stages in multi-Gb/s receivers [?]. Drawbacks include higher input-referred noise at the input and limited voltage headroom when a large load resistor is used [?].

2.5.3 Shunt-Feedback TIA (Resistive Feedback Amplifier)

The shunt–shunt feedback TIA is the classical and most widely used architecture in optical receivers. A feedback resistor R_f from the output to the input of an amplifier creates a closed-loop gain as shown in **Figure. 2.10**. For current sensing, this topology presents a low input impedance to the photodiode and a near-constant transimpedance gain approximately equal to R_f over the amplifier's bandwidth [?]. The input resistance is lowered by the loop gain of the amplifier:

$$R_{\text{in}} \approx \frac{R_f}{1+A_0}, \tag{2.11}$$

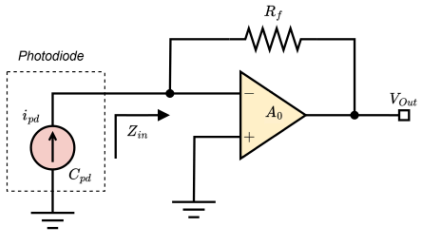


Figure 2.10: Shunt Shunt Feedback TIA topology

where A_0 is the open-loop gain at low frequency [**?**]. As a result, the photodiode's capacitance has a much smaller effect on bandwidth than in the previous case. The feedback network also makes the gain more stable and process-tolerant, since variations in amplifier parameters have reduced impact on the closed-loop gain [**?**, **?**]. Overall, a resistive-feedback TIA achieves a good trade-off between TIA gain and bandwidth, moderate noise, and good linearity, which is why it has long been a default choice for multi-Gb/s optical receivers.

Despite its strengths, the shunt-feedback TIA faces challenges as speed and C_{pd} increase. The amplifier must have a very high unity-gain bandwidth to maintain loop gain at high frequencies, and large C_{pd} can lead to poles/zeros that cause frequency peaking or stability issues if not properly compensated. In fact, there is a theoretical "transimpedance limit" for a given technology: achieving very wide bandwidth and high gain simultaneously will dramatically increase input-referred noise [**?**]. This is because the amplifier's noise and the feedback resistor's noise both contribute to the input when broadening the bandwidth [**?**]. Nonetheless, with careful design and topology considerations, shunt-feedback TIAs can support data rates in the tens of gigabits per second range. They offer excellent gain accuracy and linearity, making them suitable for general-purpose optical receivers.

2.5.4 Regulated Gain Cascode (RGC) TIA or Active Feedback TIA

The regulated cascode improves upon CG by adding a local feedback amplifier that regulates the input device's drain (or source) voltage, further reducing effective input impedance:

$$R_{\text{in}} \approx \frac{1}{g_m\,(1+A_{\text{aux}})}, \tag{2.12}$$

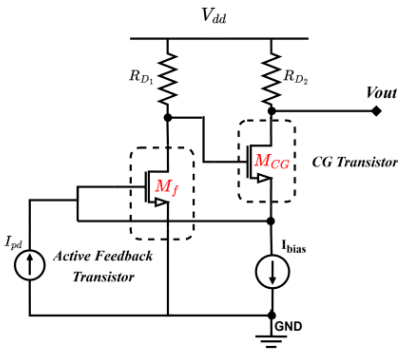


Figure 2.11: RGC TIA topology.

where A_{aux} is the gain of the auxiliary amplifier [**?**]. The ultra-low R_{in} suppresses the influence of C_d and pushes the input pole to a much higher frequency, enabling tens-of-Gb/s operation and large-C_d photodiodes. RGC often provides better noise than plain CG (higher effective g_m for the same current), but at the cost of extra power/complexity and headroom constraints in scaled CMOS [**?**].

2.5.5 Inverter-Based TIA

With CMOS scaling, inverter-based TIAs leverage the high transconductance efficiency of a biased CMOS inverter; both NMOS and PMOS contribute to g_m, enabling high GBW at low power. A feedback element R_f commonly stabilizes bias and sets the transimpedance; a simple model is

$$Z_T \approx g_{m,\text{inv}} R_L, \tag{2.13}$$

where $g_{m,\text{inv}}$ is the inverter's effective transconductance [**?**]. These TIAs are compact and energy-efficient for nanoscale technologies, but require careful common-mode control and may exhibit higher input capacitance and limited swing [**?**].

2.5.6 Inductive-Peaked TIA

Inductive peaking augments many cores (CG, RGC, shunt-feedback) to extend bandwidth by introducing series/shunt inductors that partially cancel capacitive roll-off. Proper tuning can yield

$$f_{3\text{dB,new}} \approx k\, f_{3\text{dB,RC}}, \quad k \approx 2\text{–}3.5, \tag{2.14}$$

with near-Butterworth responses [**?**]. Inductors add no DC power but consume area and can introduce peaking/overshoot if underdamped; modern designs balance speed and time-domain flatness [**?**]. Inductive peaking is a widely adopted CMOS technique for extending the bandwidth of TIA front-ends without incurring DC power. The literature converges on three practical families that can be applied to CG, RGC, or shunt–feedback cores. [**?**].

Table 2.1 compares key trade-offs across major TIA architectures (input impedance, bandwidth, gain stability, and power). Generally, CG/RGC inputs excel in bandwidth due to their low R_{in}, but they require a noise-aware design. In contrast, shunt-feedback offers excellent gain accuracy with loop-stability considerations at very high speeds. Inverter-based and active-feedback TIAs are compelling in scaled CMOS for energy efficiency and tunability, while inductive peaking remains a powerful technique for extending speed.

Table 2.1: Key trade-offs across major TIA architectures.

Architecture	Input Impedance	Bandwidth	Gain Stability	Power
Resistive Load (Passive)	High ($\approx R$)	Very Low	Excellent (no loop)	Very Low
Shunt–Feedback	Low ($\approx R_f/(1+A_0)$)	High	Excellent	Medium
Common-Gate (CG)	Very Low ($\approx 1/g_m$)	High	Moderate	Medium
Regulated Cascode (RGC)	Ultra-Low ($\approx 1/(g_m(1+A_{\text{aux}}))$)	Very High	Good	High
Inverter-Based	Low (tunable)	High	Moderate	Very Low
Active Feedback	Low (tunable)	Very High	High (tunable)	Med–High
Inductive-Peaked†	Low (tuned)	Very High	Good (Q-dependent)	Med–High

2.6 Performance Evaluation of Optical Interconnects

The exponential growth in data processing demands and miniaturization of integrated circuits (ICs) has placed immense pressure on conventional electrical interconnects, which suffer from limitations such as resistive losses, capacitive loading, signal crosstalk, and increased latency. As CMOS technology scales into the deep sub-micron regime, these constraints significantly hinder the overall system performance and energy efficiency. To overcome these challenges, researchers and industry alike are exploring OIs as a promising alternative. OIs offer significant advantages in bandwidth, signal integrity, and energy efficiency. This section focuses on the performance evaluation of OIs using three critical metrics: **signal delay, power dissipation, and the power-delay product (PDP)**, which are essential for assessing the effectiveness and viability of OI systems at the global level. Signal delay determines latency, while power dissipation affects thermal management and operational costs. PDP combines delay and energy consumption into a single efficiency metric. This section provides a detailed analysis of these parameters.

2.6.1 Signal Delay

Signal delay, also known as propagation delay, is a critical performance parameter for any interconnect technology, as it directly impacts both the maximum achievable data rate and the overall system latency. It is defined as the time required for a signal to travel from the transmitter to the receiver and is therefore directly linked to other performance metrics such as bandwidth and the power-delay product (PDP) [**?**, **?**]. In high-speed VLSI systems, delay is influenced by both the transmission medium and the interface circuitry. For OIs, the total delay comprises contributions from the transmitter (tapered buffer driving the modulator), the waveguide propagation, and the receiver (transimpedance amplifier) [**?**]. The propagation delay in an optical waveguide arises from the finite velocity of light within the guiding medium. This velocity is lower than that in a vacuum due to the waveguide's effective refractive index (n_{eff}), which accounts for both the core material's refractive index and the modal confinement characteristics [**?**]. The group velocity of light in the waveguide is expressed as $v_g = \frac{c}{n_{\text{eff}}}$, where c is the speed of light in vacuum. Consequently, the time required for an optical signal to

traverse an interconnect of length L_{int} is proportional to n_{eff} and L_{int} [?]. For typical polymer or silicon-based waveguides used in on-chip OIs, n_{eff} lies in the range of 1.4-2.0, leading to propagation delays on the order of a few picoseconds for millimetre-scale lengths [?]. At on-chip scales, this delay remains nearly constant with respect to interconnect length and is significantly smaller than the delays introduced by the transmitter and receiver circuitry, which therefore dominate the overall signal delay [?].

2.6.2 Power Dissipation

Power dissipation is a fundamental performance parameter for interconnect technologies, as it determines the energy efficiency of data transmission and directly impacts the overall thermal budget of an integrated circuit. In high-performance VLSI systems, excessive interconnect power can limit achievable clock frequencies, put stringent thermal requirements, and reduce system reliability [?]. For electrical interconnects such as Cu and SWCNT-B, total power consumption is typically composed of two major components: *dynamic power* and *static power* [?]. The dynamic component arises from the charging and discharging of the line capacitance during signal transitions and is given by: $P_{\text{dyn}} = C_{\text{tot}} V^2 f$, where C_{tot} is the total switched capacitance, V is the signal voltage swing, and f is the operating frequency. In long, high-speed electrical links, additional static power is dissipated in termination resistors or biasing networks, which can be substantial at gigahertz data rates [?, ?]. For SWCNT-B interconnects, the higher intrinsic capacitance compared to Cu leads to increased switching power consumption [?]. In contrast, OIs exhibit fundamentally different power dissipation characteristics. Since data is transmitted via photons in a waveguide, there is no need to charge and discharge a distributed capacitance along the length of the link, eliminating the dominant dynamic power term present in electrical interconnects [?]. Instead, in optical interconnects (OIs), the dominant sources of power dissipation differ fundamentally from those in electrical links. The Transmitter power is the static bias and dynamic modulation energy required to drive the optical source, such as a vertical-cavity surface-emitting laser (VCSEL) or multiple quantum well (MQW) modulator, along with the associated driver circuitry. The Receiver power is the bias currents and amplification energy consumed by the TIA and any post-amplifier stages needed to restore the signal to logic levels. Another factor is the Laser or light source power that is needed from the laser source itself, which may be distributed in a single channel or among multiple channels in case of employing WDM. Thus, the total power consumption of an optical link can therefore be approximated as:

$$P_{\text{OI}} \approx P_{\text{Tx}} + P_{\text{Rx}} + P_{\text{Laser}}, \tag{2.15}$$

where P_{Tx} and P_{Rx} account for both static bias power and a small amount of dynamic switching power [?]. A key performance indicator is the *critical length* beyond which the total power dissipation of an OI falls below that of an equivalent electrical link. Beyond these lengths, optical links become increasingly advantageous due to their length-independent power scaling.

Furthermore, unlike electrical interconnects, where power scales unfavorably with frequency ($P_{\text{dyn}} \propto f$), the static nature of OI power means that high data rates can be achieved without a proportional increase in power consumption [**?**].

2.6.3 Power Delay Product (PDP)

The power–delay product (PDP) is a widely used figure of merit (FOM) for evaluating interconnect performance, as it combines both energy consumption and speed into a single metric [**?**]. It is defined as:

$$\text{PDP} = P_{\text{avg}} \times t_{\text{delay}}, \tag{2.16}$$

where P_{avg} is the average power dissipated by the interconnect, and t_{delay} is the signal propagation delay. A lower PDP indicates that an interconnect technology can transmit data both quickly and with low energy per bit, making it highly desirable for energy-efficient, high-performance VLSI systems. For electrical interconnects such as Cu and SWCNT-B, both P_{avg} and t_{delay} scale unfavorably with interconnect length due to increasing resistance, capacitance, and inductive effects [**?**]. Even with repeater insertion, PDP grows significantly for long links, since the repeaters themselves introduce additional power consumption while only partially mitigating delay. In OIs, however, the propagation delay component is nearly independent of link length at on-chip scales, and the power consumption is dominated by fixed biasing and modulation energy in the transmitter and receiver [**?**]. This means that PDP remains relatively constant across a wide range of interconnect lengths, offering a substantial advantage over electrical solutions, particularly at global and inter-chip distances.

2.6.4 Comparative Analysis of Cu, SWCNT-B, and Optical Interconnect.

Over the past two decades, numerous researchers have compared the performance of OIs with traditional Cu and emerging CNT interconnect technologies to identify their respective advantages in nanoscale VLSI systems. These comparisons are generally based on three key performance parameters: *signal delay*, *power dissipation*, and the *power–delay product (PDP)*. The work in [**?**] models maximum optical I/O count and per I/O circuit complexity for current and future generations, using scaling trends in transistor parameters such as gate oxide thickness, supply voltage, and transconductance. The methodology includes device parameter assumptions, receiver modeling, particularly for transimpedance-based optical links, leading to quantified limits and trade-offs that inform OE-VLSI performance analysis and design. The authors in [**?**] present a preliminary performance comparison between chip-level OI and board-level electrical inteconnects, focusing on time-of-flight (ToF) limited propagation delay as the key metric. For a 45 nm technology node implementing a 4.1 billion transistor single-cycle architecture on a 572 mm^2 die, they show that replacing all global interconnects longer than 32 mm with optical waveguides, with embedded air gap cladding, low-k lower cladding, and an

SiO_2 core enables a ToF limited global clock frequency of 4.4 GHz. In contrast, replacing interconnects longer than 36 mm with board-level electrical interconnects yields a maximum clock frequency of 3.95 GHz, while purely electrical global wiring is limited to 2.9 GHz due to RC delays. This translates to a 34% performance improvement over conventional electrical on-chip wiring and roughly 10% over board-level interconnection. Furthermore, the optical solution requires approximately 32% of total chip area for routing, compared to the 180% area demand for board-level interconnections, highlighting the superior density and performance potential of chip-level OIs. In contrast, for electrical links, Cu wire delay per unit length is evaluated by accounting for surface scattering and barrier layer effects, showing that even with repeaters, delay increases to 65–93 ps/mm at future 50–35 nm nodes. Moreover, delay-optimized repeaters approximately double wire capacitance, thereby increasing dynamic power dissipation to nearly 1.7 mW for a chip-edge length wire at the 50 nm node with 15% switching activity. Comparative results show that optical interconnects outperform electrical links beyond a critical interconnect length, where waveguide propagation delay becomes favourable despite receiver power overheads. The delay–power trade-off curves indicate that for long global wires, optical systems achieve significantly lower delays with comparable or reduced power, while electrical interconnects retain an advantage for shorter links due to their lower energy per transition. Miller [**?**] first highlighted the length-independent propagation delay of optical links compared to the length-dependent RC delay in electrical interconnects, suggesting a clear advantage for optics in long-distance on-chip communication. The study in [**?**] extended this analysis by modeling both Cu and OI links under identical technology constraints, showing that optical links maintain significantly lower delays beyond millimeter-scale lengths. The analysis is built upon rigorous delay and power modelling of each component in the signalling chain, incorporating ITRS '99 parameters. On the optical side, transmitter delay is considered for a typical 100 fF modulator load driven by a CMOS buffer chain, yielding values of approximately 75 ps at the 50 nm node. The waveguide delay is evaluated using the effective index method and shown to scale close to the idealised c/n_{eff} relation, with variations primarily due to aspect ratio and cladding choice. Receiver delay is modelled using a transimpedance front-end design with a target bit error rate (BER) of 10^{-12}, where a detector capacitance of 250 fF is assumed, values experimentally demonstrated for on-chip photodiodes. Importantly, the results highlight that receiver power, dominated by static dissipation, is the primary contributor to overall optical link energy, whereas transmitter power is comparatively negligible at low input optical powers. Chen et al. [**?**] further validated these results through SPICE-based modelling of CMOS-compatible optical links, demonstrating delay improvements of up to 80% over Cu at global lengths.

The authors in [**?**] conduct a detailed comparative study on the performance of OIs against traditional electrical interconnects, highlighting critical parameters such as delay, bandwidth, and energy efficiency. Their analysis shows that while electrical interconnects at advanced technology nodes face severe RC-delay bottlenecks, OIs exhibit delay scaling primarily limited by

the speed of light in the waveguide medium. For example, chip-level optical links demonstrate propagation delays on the order of tens of picoseconds per centimetre, independent of interconnect length, compared to several hundred picoseconds in global copper wires at the 45 nm node. Bandwidth density is markedly enhanced in OIs, with reported values exceeding 1 Tbps/mm^2 due to WDM, far beyond the multi-Gbps/mm^2 range achievable with electrical wiring. In terms of energy consumption, experimental OI prototypes operate at 10-40 fJ/bit, while advanced CMOS electrical interconnects remain in the 0.5-2 pJ/bit range, representing nearly two orders of magnitude difference. Furthermore, OIs eliminate signal degradation from skin effect, crosstalk, and electromagnetic interference, enabling reliable long-distance on-chip and chip-to-chip communication. These results underscore that OIs not only surpass electrical counterparts in delay and bandwidth metrics but also offer significant improvements in energy efficiency and scalability for future VLSI systems.

The authors in [**?**] further extended the analysis to off-chip applications, where optical links also demonstrated significant promise. A broader investigation into on-chip comparisons has been carried out, and this paper builds upon those conference publications with substantial enhancements. In particular, it incorporates detailed modeling of resistance, capacitance, and inductance for both Cu and CNT wires, explores the significance of inductive effects through simulated step responses, and expands model accuracy beyond what was previously feasible. Furthermore, OIs modeled with realistic modulator driver energy, laser wall-plug efficiency, and photodetector responsivity, achieve distance-independent delays ($\sim$5 ps/mm), ultra-low energy per bit ($\leq$10 fJ/bit beyond $\sim$5-10 mm), and Tbps-scale bandwidth via WDM [**?**], while being immune to crosstalk and thermal-induced electrical variations. Despite integration hurdles such as larger waveguide footprints and thermal tuning overhead, the authors conclude that OIs are the most promising technology for meeting International Roadmap for Devices and Systems (IRDS) [**?**] targets for latency, bandwidth density, and energy efficiency in long-range on-chip and inter-chip communication.

Rakheja and Kumar [**?**] examined the PDP for electrical, optical, and plasmonic interconnects, demonstrating that optical links offer a substantially lower and length-independent PDP at on-chip scales. This was attributed to the combination of near-constant delay and static power scaling in OIs, in contrast to the superlinear PDP growth observed in Cu and CNT links. Krishnamoorthy and Miller [**?**] had earlier predicted this trend in their technology roadmap, emphasising PDP as a key metric for future interconnect evaluation.

2.7 Summary

Optical interconnects are presented as a practical way to overcome the limits of deeply scaled electrical wiring. This contrasts reviews copper (Cu) and carbon-nanotube bundles (CNT-B) interconnects. Cu is mature and dense, but long wires slow down due to RC delay with added skin effect, crosstalk, and electromigration. CNT-B offers promising current density but still

faces variability and contact challenges. Alternatively, Optical links carry data as light in silicon waveguides, so delay grows roughly linearly with length, and multiple wavelengths can share the same path (WDM). After setting performance goals *i.e.*, multi Gb/s to tens-of-Gb/s per lane, sub-pJ/bit energy, very low BER, compact footprint, and CMOS compatibility, this chapter reviews building blocks *i.e.*, drivers and modulators at the transmitter, low-loss waveguides/couplers, and at the receiver a photodetector plus a transimpedance amplifier (TIA) that converts diode current to voltage while setting bandwidth and noise.

The receiver discussion centres on TIA architectures and trade-offs. Passive resistive TIAs are the simplest but RC-limited. Common-Gate (CG) inputs offer very low input impedance and high bandwidth, but modest gain, and higher input-referred noise. Regulated gain Cascode (RGC)/active-feedback inputs push R_{in} even lower and bandwidth higher at the cost of power and complexity. Closed-loop shunt-feedback TIAs provide accurate, process-robust gain and low effective input impedance, but loop stability must be managed as capacitance grows. Inverter-based TIAs are energy-efficient in scaled CMOS when carefully controlled for bias and common-mode. Bandwidth can be extended with inductive peaking techniques.

Finally, the performance parameters such as; delay, power, and power–delay product (PDP) are compared. Electrical links exhibit RC delay that scales with length squared and often require many repeaters, thereby increasing power and area. Optical links introduces latency due to driver and receiver circuits and device chosen *i.e.*, modulator, photodiode, TIA. Optical energy is driven by source efficiency, coupling loss, modulator swing, and receiver bias; reducing losses/capacitances lowers required optical power and TIA gain. Overall, optics tends to win on PDP and latency for long or bandwidth-critical paths, while Cu remains preferred for short local interconnects, with CNT-B promising but not yet production-robust.

Chapter 3

Design and Analysis of Active voltage current feedback (AVCF) Regulated gain cascode (RGC) based TIA

3.1 Introduction

The receiver block is crucial in OCS design, as it significantly impacts system performance in terms of data rate, sensitivity, and noise. Designing a receiver block is tedious as it requires several trade-offs between gain, bandwidth, input-referred noise, and power consumed [**?**]. All these amplifiers in transmitter and receiver blocks are implemented using deep submicron (DSM) CMOS technology due to their high speed, low cost and high level of integration [**?**].

The most crucial element in the receiver block is the transimpedance amplifier (TIA) that converts the small input photocurrent into a corresponding voltage suitable for the follow-up stage [**?**]. The transimpedance gain ($\delta V_{TIA}/\delta I_{PD}$) of the amplifier must be high so that even a tiny current level produced by the photodiode is amplified, thereby reducing the number of required amplification stages and contributing to noise reduction. Thus, the sensitivity issue is addressed by the high gain of the TIA. However, as the gain increases, the bandwidth of the TIA is significantly affected [**?**]. The input capacitance introduced by the photodiode also limits the bandwidth. So, to avoid this, the input impedance of the TIA should be reduced, shifting the input pole towards the right, thereby achieving the desired bandwidth. The noise contributed by TIA will be dominant; thus, it should be kept low, as it is the first stage of the receiver block. The TIA specifications, high gain, low noise, low input impedance, and low output impedance, can be achieved by implementing transimpedance amplifiers using various techniques and topologies. There are primarily two major topologies of TIAs *i.e.*, open loop TIAs and feedback TIAs. The most common open-loop and shunt feedback TIAs are common gate (CG) and common source (CS) TIA with a shunt resistor, respectively [**?**]. Several open-loop and closed-loop TIA structures incur tight trade-offs [**?**] between gain, noise,

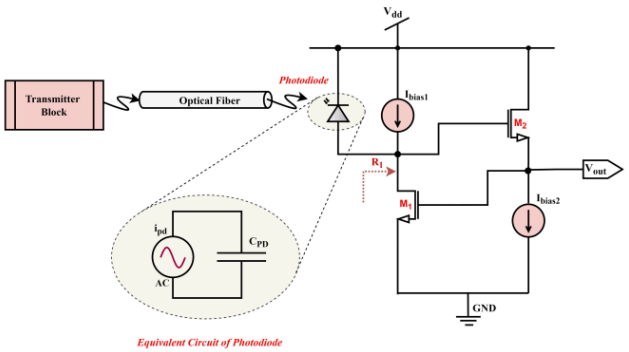


Figure 3.1: Traditional AVCF Structure

bandwidth and power consumption. Therefore, structural modifications are incorporated by researchers to come up with new TIA topologies such as shunt feedback TIAs [**?**], regulated gain cascode (RGC) TIA [**?**], common source (CS) shunt feedback TIA [**?**], inverter-based TIA [**?**], cross-coupled current conveyor TIA [**?**], and active voltage-current feedback (AVCF) TIA [**?**]. Each topology allows trade-offs between the design parameters according to the specifications set for the design. Bandwidth enhancement techniques such as gain boosting [**?**, **?**], inductive peaking [**?**, **?**], capacitive coupling [**?**], capacitive degeneration [**?**, **?**], and feedback techniques [**?**, **?**, **?**] are applied to existing TIA topologies for performance improvements. Various gain-boosting techniques are reported in the literature, such as the positive feedback gain enhancement scheme [**?**], cascading multiple stages [**?**], and cascoding structures [**?**]. In positive feedback, the gain is enhanced by reducing output conductance, but at the expense of system stability. The cascoding of amplifiers increases the gain but at the expense of power consumption and area. A Self-cascode structure increases the gain but at the expense of voltage headroom. In this chapter, an AVCF-based TIA [**?**] is presented that employs a gain boosting technique, which aids in increasing the effective transconductance of the amplifier. It also reduces the input impedance, thereby reducing the effect of parasitics and photodiode capacitance at the input and enhancing the bandwidth of the presented TIA. Further, a CS amplifier is cascaded to achieve the desired TIA gain.

3.2 Active Voltage Current Feedback TIA

The traditional AVCF TIA is schematically depicted in **Figure. 3.1**, where I_{pd} of the photodiode is applied at the drain of transistor M_1, which acts as a feedback device. It senses the voltage at the output, sending a proportional current to the input; as a result, the impedance at the input reduces. The gate voltage of M_1 is $\frac{I_{pd}}{g_{m_1}}$ because I_{pd} is applied at the drain of M_1. The

transistor M_2 is used in a source follower topology and acts as a buffer, so that the TIA gain is not significantly affected. The output of this source follower topology, as shown in **Fig. ??**, can be written as $V_{out} = \frac{I_{pd}}{g_{m_1}}$. Thus, the input and output impedance of this configuration can be written as Eq. (3.1) and (4.22):

$$R_{in} = \frac{1}{g_{m_1}}, \tag{3.1}$$

$$R_{out} = \frac{1}{g_{m_2}(1 + g_{m_1}R_1)}, \tag{3.2}$$

where g_{m_1} and g_{m_2} are transconductance of transistor M_1 and M_2 respectively, and R_1 is the total resistance at the input side due to biasing current source I_{bias_1}, the parasitic resistance of photodiode, and the channel length modulation of transistor M_1. This topology has low output impedances; thus, the gain can be increased by increasing the number of stages without any trade-off with the bandwidth. As seen from Eq. (3.1), by selecting a value of g_{m_1}, R_{in} introduces trade-offs between gain and bandwidth for achieving a target gain. In this configuration, the feedback path has a dimension of conductance. This transconductance is converted into transimpedance as the input current is converted into voltage by M_1 itself. This functionality can be achieved with a simple resistor (R_f), but the time constant $R_f C_{pd}$ introduces significant trade-offs between TIA gain, bandwidth, and noise. The transfer function of the AVCF structure, taking into account the intrinsic resistances and parasitic capacitances, is given by Eq. (3.3):

$$\begin{aligned} Z_{TIA}(s) = \frac{sC_0 + g_{m_2}R_2R_1}{s^2[R_2R_1(C_1C_2 - C_0^2)] + s[(g_{m_2} + g_{mb_2})R_2R_1C_1 + R_2C_2 + R_1C_1} \\ +(g_{m1} - g_{m2})R_2R_1C_0] + [(g_{m_2} + g_{mb_2})R_2 + g_{m_1}g_{m_2}R_1R_2 + 1], \end{aligned} \tag{3.3}$$

where $C_1 = C_{in} + C_o$, $C_o = C_{gd_1} + C_{gs_2}$, $C_{in} = C_{pd} + C_{gd_2}$. C_{gd_1} and C_{gs_2} in Eq. (3.3) represents gate drain capacitance of M_1 and gate source capacitance of M_2 respectively, C_{pd} is parasitic capacitance of photodiode, C_{gd_2} is gate drain capacitance of M_2. Further, R_2 is the total resistance observed at the output side. Comparing Eq. (3.3) with the standard transfer function of second order, the ζ and ω_n are calculated as follows:

$$\zeta = \frac{(g_{m_2} + g_{mb_2})R_2R_1C_1 + R_2C_2 + R_1C_1 + (g_{m_1} - g_{m_2})R_2R_1C_0}{2\sqrt{R_2R_1(C_1C_2 - C_0)((g_{m_2} + g_{mb_2})R_2 + g_{m_1}g_{m_2}R_2R_1 + 1)}}, \tag{3.4}$$

$$\omega_n = \sqrt{\frac{(g_{m_2} + g_{mb_2})R_2 + g_{m_1}g_{m_2}R_2R_1 + 1}{R_1R_2(C_1C_2 - C_0)}}, \tag{3.5}$$

where ω_n is the natural angular frequency, and ζ is the damping ratio. A system will have two roots that are imaginary when $\zeta = 0$, real and equal when $\zeta = 1$, real but not equal when

$\zeta > 1$, and complex conjugate when $0 < \zeta < 1$. So, according to the value of ζ, the poles will have a corner frequency ω_n. By incorporating a gain-boosting structure into the existing AVCF TIA design, which increases the gain and bandwidth while reducing the input and output impedances.

$$Z_{TIA}^{AVCF}(0) = \frac{g_{m_2} R_2 R_1}{(g_{m_2} + g_{mb_2}) R_2 + g_{m_1} g_{m_2} R_2 R_1 + 1}. \tag{3.6}$$

The values of R_1, R_2, and g_m are selected for 0.18 μm technology, such that the required gain is achieved without significantly affecting the bandwidth. At low frequencies, the impact of parasitic capacitances is eliminated. Therefore, gain depends only on intrinsic resistances and g_m of the transistors. So, boosting the circuit's overall g_m will increase the circuit's gain and bandwidth. Moreover, as seen from Eq. (3.1) and (4.22), R_{in} and R_{out} depend inversely on g_m, which implies that boosting the g_m will also decrease the input and output impedance of the circuit. Therefore, in the next section, a gain-boosting structure is incorporated into the existing AVCF TIA design, which increases the gain and bandwidth while reducing the input and output impedances of the proposed circuit.

3.3 The Proposed TIA-based Optical Receiver

The small g_m, along with the photodiode capacitance (C_{pd}), creates a dominant pole at the input, limiting the bandwidth of the TIA. Therefore, a lot of gain boosting structures are presented in literature [?, ?, ?, ?, ?, ?], but in this paper, the RGC structure is used because of its improved sensitivity and stability [?]. RGC structure enhances the g_m, which relaxes the effect of input parasitic and further reduces the noise contribution in the TIA. This RGC structure is introduced as a gain boosting structure in the traditional AVCF TIA to enhance the performance of the

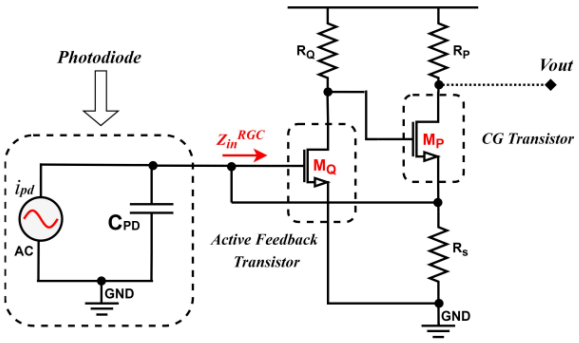


Figure 3.2: RGC Structure.

TIA-based optical receiver.

3.3.1 RGC Structure

The RGC structure depicted in **Figure. 3.2** consists of two transistors M_Q and M_P, where M_Q acts as a boosting amplifier, and M_P acts as an amplifier in CG configuration. The booster amplifier, comprising transistor M_Q and drain resistance R_Q in the RGC structure, acts as local feedback, reducing the input impedance by a factor of its voltage gain. This local feedback is responsible for peaking in frequency response due to the introduction of a zero [**?**]. The low-frequency input impedance of the RGC structure is given by:

$$Z_{in}^{RGC}(0) \cong \frac{1}{g_{m_p}(1+g_{m_q}R_Q)}, \tag{3.7}$$

This factor $g_{m_p}(1+g_{m_q}R_Q)$ increases the overall transconductance and the gain of the proposed TIA, as it also appears in Eq. (3.18), which is the DC gain of the proposed TIA. The DC gain of the RGC structure is:

$$Z_{DC}^{RGC}(0) \approx R_P, \tag{3.8}$$

Thus, R_P must be high to maintain a high gain. Moreover, to maintain the stability, a large g_{m_q} and small R_Q is preferred [**?**]. Also, the approximate transfer function of the RGC structure is given by:

$$Z_{T_{RGC}} \cong \frac{R_P}{\left(1+s\frac{C_{in}}{g_{mp}(1+g_{mq}R_Q)}\right)(1+sR_P(C_{out})}, \tag{3.9}$$

where C_{in} is the capacitance at input side that includes C_{pd} and C_{gs_q}, and C_{out} is the capacitance at the output side that includes C_{gd_p} and the load capacitance of the following stage. It can be inferred from Eq. (3.9) that the RGC stage contributes mainly two pole frequencies, one at the input side given by:

$$\omega_{in}^{RGC} \cong \frac{g_{mp}(1+g_{mq}R_Q)}{C_{in}}, \tag{3.10}$$

, and one at the output side given by:

$$\omega_{out}^{RGC} \approx \frac{1}{R_P C_{out}}, \tag{3.11}$$

As the input impedance of RGC is much smaller, the dominant pole that affects the 3-dB frequency of the RGC input stage is ω_{out}^{RGC}, which can be calculated as:

$$f_{3-dB} \approx \frac{1}{2\pi R_P C_{out}}. \tag{3.12}$$

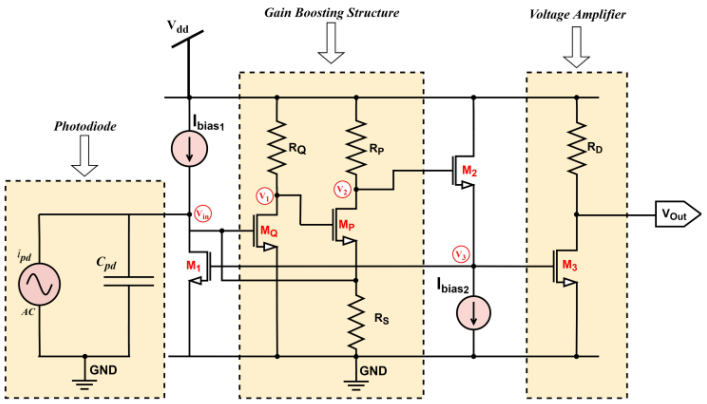


Figure 3.3: The proposed receiver front end with g_m boosting.

Table 3.1: (W/L) values of the transistors used in the proposed TIA structure.

S.No.	Variables	Values
1	$(W/L)_1$	83.33
2	$(W/L)_P$	166.67
3	$(W/L)_Q$	166.67
4	$(W/L)_2$	277.78
5	$(W/L)_3$	222.22

However, due to the presence of an input pole, the 3-dB frequency is lower than stated. Therefore, the RGC structure helps isolate the input capacitance, enabling a larger bandwidth to be achieved. In the next section, the proposed structure of TIA will be analysed, which incorporates the RGC stage in the AVCF-TIA structure.

3.3.2 Analysis of the Proposed TIA

As depicted in **Figure. 3.3**, the proposed TIA includes a photodiode at the input side that receives an optical signal from the transmitter block and converts this signal into a corresponding photocurrent. The photodiode is replaced with a simple electrical equivalent circuit consisting of a photocurrent (I_{pd}) and a photodiode capacitance. The transistor M_1 feeds the variations in the voltage at node V_3 to the current at the drain of M_1, which helps in further reduction in the input impedance.

This feedback current, along with the I_{pd} received at the source of M_P, is amplified to be a voltage at the drain of M_P by this CG configuration. This voltage is sensed by the gate of transistor M_2 in source follower topology and drives the load connected at the source of M_2 *i.e.*,

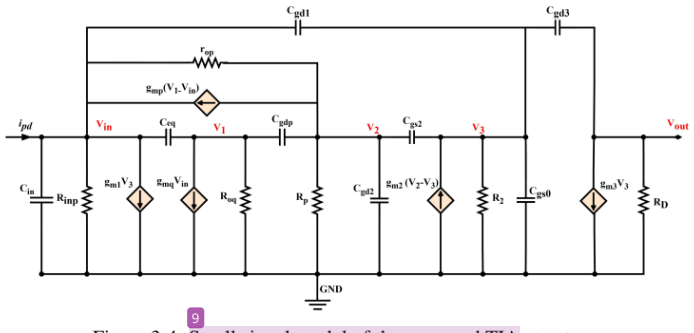


Figure 3.4: Small signal model of the proposed TIA structure.

R_S and the transistor M_3 in this case. One advantage of using the source follower (SF) topology is to reduce the output impedance of the circuit due to its body effect, *i.e.*, $R_{out_{SF}} = \frac{1}{g_{m_2}+g_{mb_2}}$. However, the source followers don't increase the gain, so an additional stage is needed in the circuit to achieve the desired gain, thereby significantly amplifying the weak signal produced by the photodiode. Consequently, a common source (CS) stage is cascaded with TIA to increase the gain without affecting the bandwidth. This statement is supported by Eq. (4.27) where the 3-dB frequency is independent of the transconductance of transistor M_3. In this design, our goal is to integrate the proposed TIA with the main amplifier in the future, thereby avoiding the need for output load matching to 50Ω, which relaxes the tradeoffs between power dissipation, bandwidth, and gain [**?**]. The biasing currents I_{bias_1} and I_{bias_2} are provided in this circuit in such a way that all the transistors are in saturation. The W/L ratios of all the transistors are mentioned in **Table 3.1**. The aspect ratios of transistors are selected to reduce trade-offs between design parameters such as gain, bandwidth, power consumption, and input-referred noise.

The small signal model of the proposed RGC-based TIA is shown in **Figure. 3.4**. The effects of gate-source and gate-drain capacitances of the transistors are considered when constructing the equivalent high-frequency model of the TIA-based optical receiver. The transconductance of the transistors is represented by g_m. C_{in} is the total capacitance seen at the input node *i.e.*, $C_{in} \cong C_{pd} + C_{gs_q}$, where C_{gs_q} is the gate-source capacitance of the MOSFET M_Q. R_{inp} is the resistance at the node V_{in} that includes the effect of channel length modulation of the transistor M_1, resistance contributed by biasing current source I_{bias_1}, and the source resistance R_S of transistor M_P. R_2 is the resistance seen at the node V_3, which comprises the effect of channel length modulation of the transistor M_2, and the resistance contributed by biasing current source I_{bias_2}. The gate-source capacitances of transistors M_1 and M_3 are in parallel to each other at node V_3, thus C_{gs_0} is introduced as the sum of C_{gs_1} and C_{gs_3}. To find the transfer function of the proposed TIA, KCL is applied at the nodes V_{in}, V_1, V_2, V_3, and V_{out}. The equations at these

Table 3.2: Variables used in Eq. (3.13)-(3.18)

Variable	Description
R_D	Resistance seen at the drain of M_3.
$C_{gs_{eq}}$	C_{gs_2}+C_{gs_0}
C_{eq}	C_{gd_q}+C_{gs_p}
C_2	C_{gs_2}+C_{gd_2}+C_{gd_p}
C_3	C_{eq}+C_{gd_p}
C_4	C_{in}+C_{gd_1}
R_{op}	$R_P \parallel r_{op}$
R_{oq}	$R_Q \parallel r_{oq}$
$R_{in_{eq}}$	$R_{inp} \parallel r_{op}$
R_2	Resistance seen at the node V_3.

nodes are as follows:

$$V_3 = V_{out}\frac{1+sC_{gd_3}R_D}{sC_{gd_3}R_D - g_{m_3}R_D}, \tag{3.13}$$

$$\Big[s\big(C_{gd_3}+C_{gs_{eq}}\big)+g_{m_2}\Big]V_3 - \Big[g_{m_2}+sC_{gs_2}\Big]V_2 = \Big[sC_{gd3}\Big]V_{out}, \tag{3.14}$$

$$s\left[C_2+\frac{1}{R_{op}}\right]V_2 - g_{m_p}V_{in} - \Big[sC_{gd_p}-g_{m_p}\Big]V_1 = \Big[sC_{gs_2}\Big]V_3, \tag{3.15}$$

$$s\left[C_3+\frac{1}{R_{oq}}\right]V_1 - \Big[sC_{gd_p}\Big]V_2 = \Big[sC_{eq}-g_{m_p}\Big]V_{in}, \tag{3.16}$$

$$I_{in} = s\Big[C_4+g_{m_p}+\frac{1}{R_{in_{eq}}}\Big]V_{in} - \Big[sC_{eq}+g_{m_p}\Big]V_1 - \frac{V_2}{r_{op}} + \Big[g_{m_1}-sC_{gd_1}\Big]V_3, \tag{3.17}$$

where the variables used in above equations are defined in **Table 3.2**. These equations can be solved for $Z_{TIA}(s) = \frac{V_{out}}{I_{in}}$ by eliminating V_{in}, V_1, V_2, and V_3 from Eq. (3.13), (3.14), (3.15), (3.16), and (5.11). The transfer function $Z_{TIA}(s)$ has seven poles and five zeros. By putting s=0 in $Z_{TIA}(s)$, low-frequency gain of the proposed TIA can be computed as:

$$Z_{TIA}(0) \cong \frac{g_{m_3}g_{m_p}(1+g_{m_q}R_{oq})R_{in_{eq}}R_{op}R_{oq}r_{op}}{R_{oq}R_D r_{op}\big[1+g_{m_p}R_{in_{eq}}(1-g_{m_q}R_{oq})\big] - \big[g_{m_3}g_{m_p}R_D R_{oq}(1+g_{m_q}R_{oq})(1-g_{m_1}r_{op})R_{in_{eq}}R_{op}\big]}. \tag{3.18}$$

By comparing Eq. (3.6) with (3.18), it can be concluded that the gain at low frequencies has been increased because of the factor $(1+g_{m_q}R_{oq})$ contributed by the RGC structure as discussed in **Section 3.3.1**. So, by selecting a large value of R_P and R_Q in Eq. (3.18), the gain can be increased, but there are constraints in increasing the values so that the noise of the circuit is not

Table 3.3: Parameter Values of the proposed TIA structure.

S.No.	Parameters	Values
1	C_{pd}	300 fF
2	I_{bias_1}	300 μA
3	I_{bias_2}	5 mA
4	R_D	800 Ω
5	R_S	800 Ω
6	R_P	500 Ω
7	R_Q	500 Ω

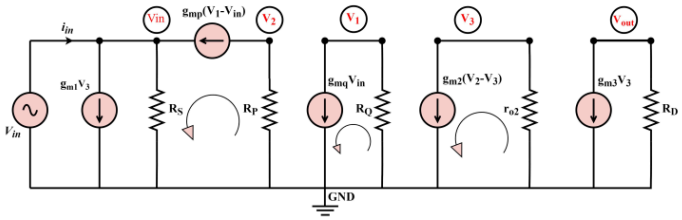


Figure 3.5: Small signal model for calculating $R_{in_{TIA}}$

increased much. Hence, the optimum values as shown in **Table 3.3** are chosen for R_P and R_Q. The input resistance of the proposed TIA is calculated by applying Kirchhoff's laws (KCL and KVL) in a small signal model as shown in **Figure. 3.5**. It is obtained as:

$$R_{in_{TIA}} \cong \frac{1}{g_{m_p}(1+g_{m_q}R_q)(g_{m_1}+g_{m_p})R_p - g_{m_p}}, \tag{3.19}$$

If Eq. (5.13) is compared to Eq. (3.1), it can be concluded that the input impedance of the proposed circuit is reduced extensively by incorporating the RGC gain boosting structure. The 3-dB bandwidth of the circuit is calculated by assuming the input pole to be a dominant pole due to the presence of a large photodiode capacitance. Thus,

$$\omega_{3-dB} \approx \frac{1}{C_{in}R_{in_{TIA}}}, \tag{3.20}$$

$$\omega_{3-dB} \approx \frac{g_{m_p}(1+g_{m_q}R_q)(g_{m_1}+g_{m_p})R_p - g_{m_p}}{C_{pd}+C_{gs_q}}. \tag{3.21}$$

Again, the factor $(1+g_{m_q}R_q)$, contributed by the RGC input stage, is responsible for extending the bandwidth of the proposed TIA structure. In this way, the proposed TIA based optical receiver is capable of isolating the photodiode's input capacitance and achieving a high gain.

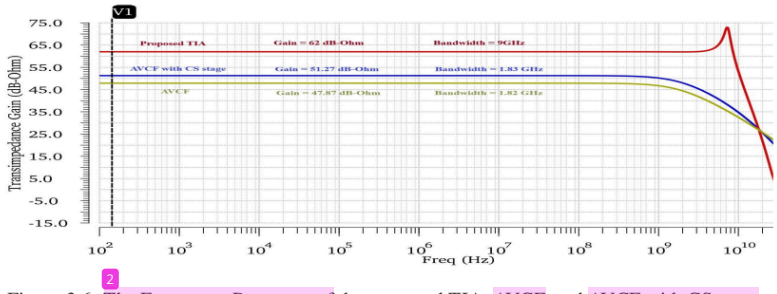


Figure 3.6: The Frequency Response of the proposed TIA, AVCF, and AVCF with CS stage.

3.4 Results and Discussions

The proposed circuit is simulated using the Cadence Virtuoso EDA tool in 0.18 μm technology node at 1.8 V supply voltage. The active and passive components used in the TIA circuit are assigned the optimum values, as mentioned in **Tables 3.1** and **3.3**, to achieve low noise, high gain, high bandwidth, and low power consumption. Simulation results reveal that the best trade-off is achieved using these values. The AVCF TIA with and without a CS gain stage is also implemented and simulated for comparison. **Figure. 3.6** represents the frequency response of the proposed RGC-based TIA, AVCF TIA, and AVCF TIA with a CS gain stage. It can be seen that the proposed circuit has achieved a gain of 62 dBΩ, which is higher than that achieved in the case of AVCF (51.27 dBΩ) and AVCF with CS gain stage (47.87 dBΩ). The introduction of the RGC gain boosting structure in the traditional AVCF structure has also extended the bandwidth from 1.83 GHz to 8.2 GHz.

3.4.1 DC Analysis

DC analysis refers to the evaluation of a circuit's steady-state behaviour when subjected to constant (time-invariant) inputs, usually with all capacitors treated as open circuits and inductors as short circuits. The objective is to determine the biasing conditions of active devices (tran-

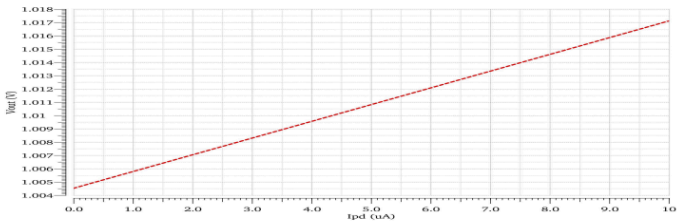
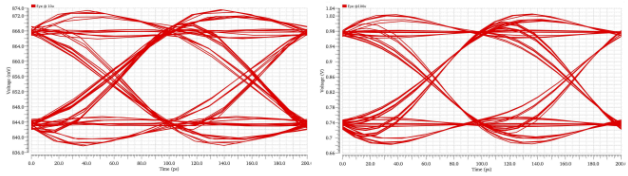


Figure 3.7: DC transfer characteristics of the proposed TIA.

sistors) and the operating point (Q-point) of the circuit. This analysis ensures that the circuit operates in the correct region of the device's I–V characteristics, such as keeping MOSFETs in saturation for amplification. For DC analysis, a DC source is applied at the input, and DC transfer characteristics are plotted in **Figure. 3.7**. It can be depicted from the plot that the transfer characteristics of output voltage and input current are linear.

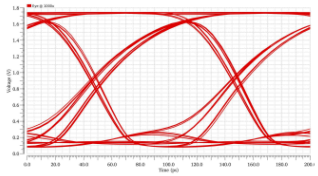
3.4.2 Eye Diagram Analysis

An eye diagram is a widely used method for evaluating the quality of high-speed digital signals, formed by overlaying multiple bit periods of a waveform on a common time axis to create a characteristic eye-shaped pattern. The openness of the eye conveys critical information about signal integrity, with the vertical eye opening indicating noise margin and the horizontal eye opening reflecting timing margin against jitter. In the design of transimpedance amplifiers (TIAs), eye diagram analysis serves as a crucial diagnostic tool, as it captures the combined effects of bandwidth limitations, noise, inter-symbol interference (ISI), and jitter on the output signal. **Figure. 3.8** shows the eye diagram analysis at the output for a 10 Gb/s Pseudo-random binary sequence (PRBS7) for peak-to-peak input current levels of 10 μA, 100 μA, and 1000 μA. The results show that the eye is wide open at these current levels, suggesting negligible distortions in the output. Also, the peak-to-peak jitter varies from 13.9 pS to 7.5 pS when the input current level is varied from 10 μA to 1000 μA. In all these simulations, C_{pd} is kept at 300 fF.



(a) Output eye diagram for 10μA input peak-to-peak current.

(b) Output eye diagram for 100μA input peak-to-peak current.



(c) Output eye diagram for 1000μA input peak-to-peak current.

Figure 3.8: Simulated output eye diagram of the proposed TIA with 10 Gb/s $2^7 - 1$ PRBS.

3.4.3 Effect of Temperature and C_{pd}

on Bandwidth The gain and bandwidth of a TIA are significantly affected by both operating temperature and photodiode junction capacitance (C_{pd}). An increase in temperature reduces carrier mobility in MOS transistors, which lowers the transconductance (g_m) and degrades the amplifier's open-loop gain, while also increasing thermal noise and photodiode leakage current, thereby reducing sensitivity and the signal-to-noise ratio (SNR). On the other hand, a larger C_{pd} increases the effective input capacitance at the TIA front-end, forming a dominant RC pole with the feedback resistor R_f that reduces the -3 dB bandwidth according to

$$f_{-3dB} \approx \frac{1}{2\pi R_f (C_{pd} + C_{in})}.$$

The effect of C_{pd} on the gain and bandwidth of the proposed TIA is shown in **Figure. 3.9**. The photodiode capacitance is swept from 100 fF to 500 fF, resulting in the variation of the frequency response of the proposed TIA. It can be observed that with an increase in the value of C_{pd}, the bandwidth deteriorates; however, this change is not significant, as shown in **Figure.3.9**. In practical conditions, temperature also affects the system's performance. Thus, the effect of temperature on bandwidth is plotted in **Figure. 3.10** at $27°, 54°, 81°$, and $108°C$. As the temperature rises, there is a reduction in bandwidth. This phenomenon occurs because the

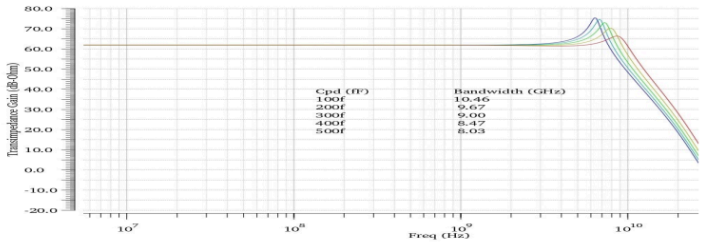


Figure 3.9: Effect of varying photodiode capacitance on the Bandwidth.

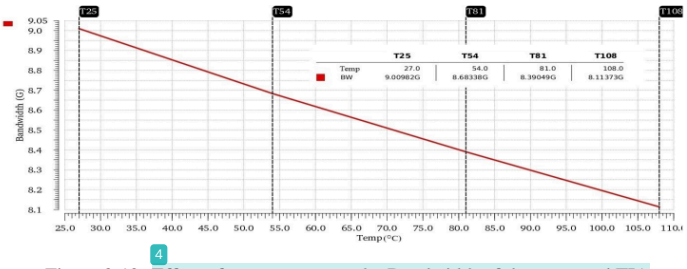


Figure 3.10: Effect of temperature on the Bandwidth of the proposed TIA.

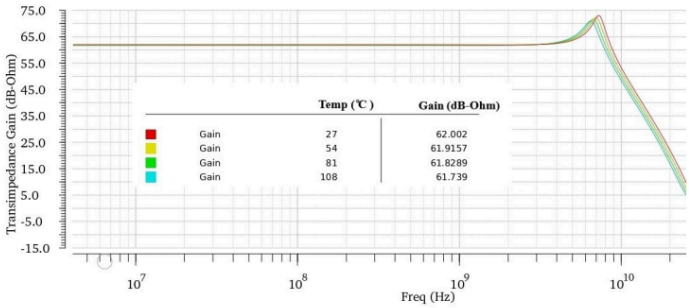


Figure 3.11: Effect of Temperature on the Gain of the proposed TIA.

resistance also increases due to scattering, which ultimately imposes a constraint on the bandwidth, as mentioned in references [**?**, **?**]. The effect of temperature on the frequency response of the proposed TIA is also illustrated in **Figure. 3.11**, indicating a slight decrease in gain as the temperature rises.

3.4.4 Monte Carlo and Process Corner Simulation

Monte Carlo (MC) simulation is a statistical verification methodology used to quantify the impact of random process variations and device mismatch on key TIA specifications, *i.e.*, transimpedance gain Z_{TIA}, bandwidth $f_{-3\text{dB}}$, input-referred noise, output swing, offset, and stability margin. MC captures *stochastic* spreads arising from local (intra-die) mismatch *i.e.*, threshold voltage ΔV_T, mobility $\Delta\mu$, resistor ratio error $\Delta R/R$, capacitor variation $\Delta C/C$) and global (inter-die) variations. In a typical flow, each run samples device and component-level parameters from specified probability distributions, re-solves the circuit operating point, and evaluates performance metrics. Repeating this N times produces empirical distributions for each metric, from which the yield can be estimated. The end goal is a statistically robust TIA meeting *simultaneous* gain, bandwidth, noise, and stability targets with sufficient yield margin across manufacturing and operating uncertainties.

In practical fabrication conditions, device mismatch and process variations affect the proposed circuit's behaviour [**?**]. Therefore, the MC simulation with device mismatch and process variations is iterated 500 times. The results obtained are illustrated in **Figure. 3.12** and **Figure. 3.13**. MC simulations of gain and bandwidth reveal that the proposed circuit achieved a gain in the range of 58.26-62.68 $dB\Omega$, and the bandwidth achieved peaked between 6-9 GHz with a standard deviation of 946.111 MHz, which is 1.58 % of the maximum achievable gain. Process corner analysis is also executed with two corners *i.e.*, Fast (F) and Slow (S). **Figure. 3.14** show the frequency response at two corners, concluding that it has a marginal effect on

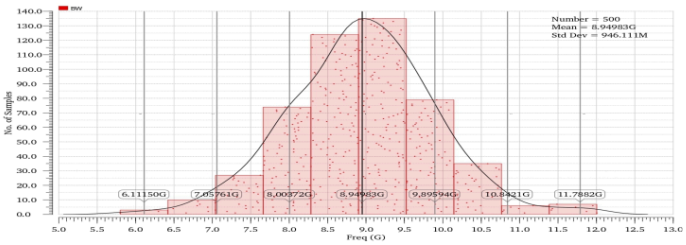


Figure 3.12: The histogram showing Monte Carlo Analysis on Bandwidth with 500 sample size.

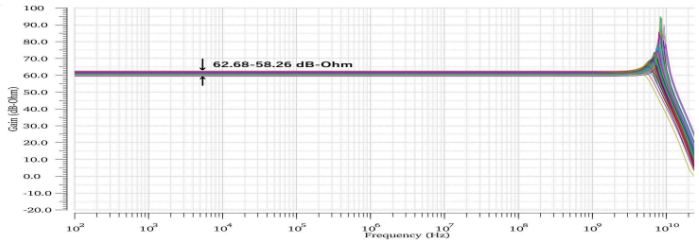


Figure 3.13: Monte Carlo analysis on frequency response with 500 sample size.

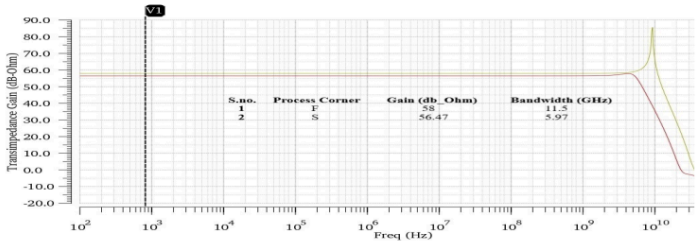
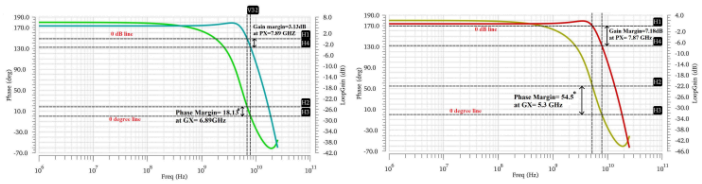


Figure 3.14: Frequency Response using Process Corner Simulation.

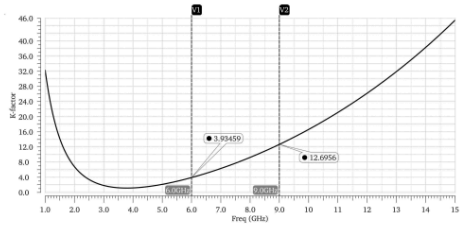
the gain and affects the bandwidth more than the gain. The bandwidth varies from 5.97 GHz to 11.5 GHz at the S and F corners, respectively. This analysis proves that our proposed TIA design is also robust in practical environmental conditions.

3.4.5 Stability Analysis

Stability analysis is the process of ensuring that the amplifier and photodiode system remains free of oscillations and excessive peaking across all expected operating conditions. The pho-



(a) Bode plot of loop gain at $W_1 = 15\mu m$. (b) Bode plot of loop gain at $W_1 = 10\mu m$.



(c) Stability factor, K_f

Figure 3.15: Stability analysis of the proposed circuit showing Bode plots of loop gain and K-factor.

todiode introduces a junction capacitance (C_{pd}) which, together with the amplifier's input capacitance (C_{in}) and the feedback network, creates frequency-dependent poles and zeros in the loop response. If not properly controlled, these reactive components can reduce the phase margin, leading to signal peaking, ringing, or even oscillation at high data rates. Stability analysis, therefore, involves evaluating the loop gain and the noise gain of the system, identifying the locations of poles and zeros, and determining whether sufficient phase margin (typically $\geq 60°$) is maintained at the unity-gain frequency of the loop. Thus, various techniques are employed to achieve stability, as it is essential for guaranteeing reliable, oscillation-free operation in high-speed optical receivers, thereby enabling robust gain and bandwidth performance across diverse operating conditions.

To verify the stability of the proposed TIA between the peak frequencies of 6-9 GHz, a stability analysis is performed in the Cadence Virtuoso analogue design environment at room temperature. This analysis involves introducing a test probe into the negative feedback loop to calculate the loop gain, gain margin, and phase margin. **Figure. 3.15(a)** and **Figure. 3.15(b)** shows the loop gain and phase plots for W_1= 15 μm and W_1= 10 μm respectively. At W_1= 15 μm, the Gain margin is 3.13 dB at a phase crossover frequency of 7.89 GHz, and the phase margin is 18.13° at a gain crossover frequency of 6.89 GHz. At W_1= 10 μm, the Gain margin is 7.18 dB at a phase crossover frequency of 7.87 GHz, and the phase margin is 54.5° at a gain crossover frequency of 5.3 GHz. It can be concluded from these figures that the phase margin has been increased to 54.5° from 18.13° by reducing the width of the transistor M_1, thus

making the system more stable. Due to the dominant pole approximation, the system's stability depends on the transconductance of the gain-boosting stage and the parasitics associated with the input node, and it can be further improved by decreasing the width of transistor M_P. However, decreasing the width reduces the transconductance, thus increasing the noise contribution. Hence, this tradeoff must also be considered when designing the TIA-based optical receiver [**?**]. Further, the Rollet's stability factor (K_f) is plotted using the S-parameter analysis. **Figure. 3.15(c)** shows that K_f is always greater than one in the frequency of interest, ensuring the stability of the system.

3.4.6 S-Parameter Analysis

S-parameter analysis is a powerful technique for evaluating input/output matching, forward gain, and stability across a frequency range. While low-frequency small-signal models rely on lumped RC approximations, S-parameters provide a frequency-domain description of the circuit under realistic loading and interconnect conditions.

For a TIA, the input port is defined at the photodiode interface, while the output port is the voltage node driving subsequent post-amplifiers. The most important S-parameters include:

- S_{11} **(Input Reflection Coefficient):** Indicates the degree of signal reflection at the TIA input. A low $|S_{11}|$ ensures maximum current transfer from the photodiode into the amplifier. Since a TIA ideally presents a virtual ground, maintaining a low $|S_{11}|$ over the entire bandwidth is critical.

- S_{21} **(Forward Gain):** Represents the transimpedance transfer function from input current to output voltage. The magnitude of S_{21} determines the frequency-dependent gain, while the -3 dB point of $|S_{21}|$ defines the effective bandwidth. The phase response of S_{21} also provides group delay information, which is important for analysing inter-symbol interference (ISI).

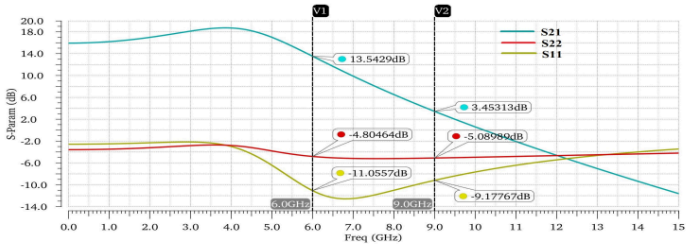


Figure 3.16: S-parameter analysis for the proposed TIA showing the S11, S21, S22 in dB vs frequency.

- S_{22} **(Output Reflection Coefficient):** Describes the matching of the TIA output to its load. A low $|S_{22}|$ reduces output reflections and ringing, ensuring a robust interface with limiting amplifiers or measurement systems.

- S_{12} **(Reverse Isolation):** Characterizes the amount of output signal that couples back into the input. A low $|S_{12}|$ prevents noise or interference from degrading photodiode performance and overall receiver sensitivity.

Beyond matching and gain, S-parameters are also used for stability verification. The Rollet stability factor K and the stability measure μ, derived from the two-port S-matrix, must satisfy $K > 1$ and $\mu > 1$ across the operating frequency range for unconditional stability. Furthermore, the group delay extracted from the phase of S_{21} provides insight into waveform distortion at high data rates. **Figure. 3.16** shows the simulated S11, S12, and S22 parameters, which represent the reflection coefficient at the input, power gain, and reflection coefficient at the output. It can be seen that a good impedance matching is seen at the input as S11 is better than -10 dB. The power gain of the proposed TIA S21 is 13.5 dB at 6 GHz and 3.5 dB at 9 GHz. The output reflection coefficient S22 is around -5 dB as the output load is not matched to 50Ω as mentioned in **Section 3.3**.

3.4.7 Layout and Post layout Simulation

The layout of the proposed TIA circuit, as depicted in **Figure. 3.17**, is extracted using the layout XL editor in the Cadence design environment. It occupies an area of $28.5 \times 32.3\ \mu m^2$ without including bond pads. The size comparison is illustrated in **Table. 3.4**.

Further, the parasitic capacitance values of the layout are extracted using the Assura tool in Cadence, and the post-layout simulation of frequency response at different temperatures is shown in **Figure. 3.18**. The impact of parasitic capacitances on the design becomes evident as they increase the ripples in the frequency response, resulting in a decrease in overall band-

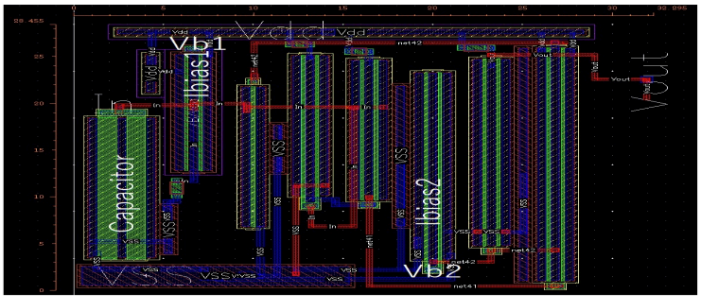


Figure 3.17: Layout of the proposed circuit. (The scale of the Ruler is in μm.)

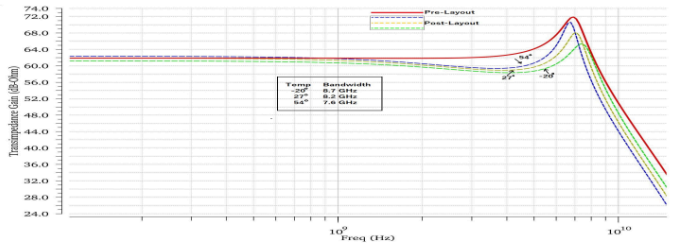


Figure 3.18: Post-layout frequency response at different temperature conditions.

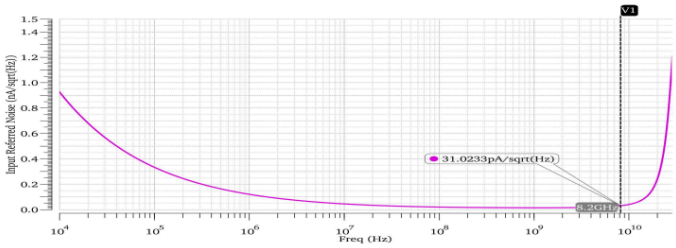


Figure 3.19: Post-layout current spectral density of input referred-noise.

width. When subjected to different temperature conditions, the post-layout frequency response indicates that circuit operation remains desirable. The bandwidth of the circuit decreases with temperature, which validates the results achieved in **Figure. 3.10**. **Figure. 3.19** shows the current spectral density of input-referred noise, which is equal to 31 $\frac{pA}{\sqrt{Hz}}$ at the circuit bandwidth (8.2 GHz).

In **Table 3.4**, a comparative analysis is executed between existing designs of TIA's with the proposed TIA. According to the table, the proposed TIA design achieves high gain, wide bandwidth, and low input-referred noise while consuming a very low power of 14.5 mW, compared to other existing TIA's in the literature. The proposed TIA layout occupies an area of 0.0008 mm^2 without including bond pads. To have a fair comparison, two figures of merit (FOM^1 and FOM^2) are defined using the following expressions:

$$FOM^1 = \frac{Bandwidth\ (GHz) \times Gain\ (\Omega)}{Power\ (mW)} \tag{3.22}$$

$$FOM^2 = \frac{Bandwidth\ (GHz) \times Gain\ (dB\Omega) \times Cpd\ (fF)}{Power\ (mW) \times Noise\ (pA/\sqrt{Hz})} \tag{3.23}$$

The FOM^1 serves as a metric for comparing the performance of various TIA's based on parameters like gain, bandwidth, and power consumption. Additionally, the FOM^2 considers

Table 3.4: Performance comparison of the proposed inductorless TIA with state-of-the-art designs.

Parameter	[?] [1] 2009	[?] [2] 2017	[?] [3] 2018	[?] [4] 2015	[?] [5] 2016	[?] [6] 2013	**This Work 2025**
Technology (nm)	180	180	65	180	180	180	**180**
Transimpedance Gain (dBΩ)	55	59	62	50.3	58	46	**62**
Bandwidth (GHz)	7.0	7.9	11.0	9.0	8.1	4.0	**8.2**
Photodiode Capacitance (fF)	200	300	200	300	300	250	300
Power Consumption (mW)	18.6	18.0	66.0	30.0	34.8	31.5	**14.5**
Supply Voltage (V)	1.8	1.8	–	1.8	1.8	1.8	1.8
Input-Referred Noise ($pA/\sqrt{Hz}$)	17.5	23.0	30.0	13.4	15.0	18.0	31.0
Number of Inductors	1	2	2	3	2	0	**0**
Result Type	Meas.	Post	Meas.	Pre	Pre	Meas.	**Post**
Core Area (mm^2)	0.10	0.11	0.08	–	–	0.35	**0.0008**
FOM^1 (GHzΩ/mW)	207	391	209	98	185	25	**707**
FOM^2 (GHzΩ/(mW·pF))	237	281	69	338	270	81	**339**

not only these factors but also the impact of C_{pd} and noise. By utilising Eq. (4.28) and (4.29), the FOM^1 and FOM^2 are computed for the proposed circuit and the similar TIA's offered in the literature. While the proposed circuit outperforms other TIA's in terms of achieved bandwidth, with the exception of designs in references [**?**] and [**?**], these alternatives consume more power and exhibit lower FOM^1 values, as depicted in **Table 3.4**. Although FOM^2 of [**?**] aligns comparably with the proposed design, it uses three inductors in its design, leading to a substantial chip area requirement. In conclusion, it is evident from **Table 3.4** that our proposed design surpasses the performance of the other TIA's outlined in the existing literature in terms of parameters defined in FOM^1 and FOM^2.

3.5 Summary

This chapter presented the design and analysis of a high-speed Transimpedance Amplifier (TIA) based on an Active Voltage–Current Feedback (AVCF) assisted Regulated Gain Cascode (RGC) topology. The discussion began by outlining the limitations of conventional TIA architectures and establishing the motivation for adopting an RGC structure enhanced with AVCF. The proposed design aims to achieve a low input impedance, improved bandwidth, and controlled gain behaviour, all of which are essential for high-speed optical receiver operation. A small-signal analysis was included to clarify the gain mechanism and the influence of feedback on the overall frequency response.

A comprehensive set of simulations was carried out to evaluate the performance of the proposed TIA. DC and AC analyses demonstrated that the amplifier delivers a high transimpedance gain along with a wide bandwidth suitable for multi-gigabit data rates. Eye-diagram evaluations

showed clean signal transitions, indicating reliable data reception. The influence of temperature variations and photodiode capacitance was also examined, confirming the stability of the design under realistic operating conditions. Process-related variations were assessed using Monte Carlo and corner simulations, and the results indicated strong robustness against fabrication-induced fluctuations. Stability was verified using phase-margin analysis and S-parameter evaluation. Post-layout simulations, which incorporate parasitic effects, showed close agreement with schematic results and validated the practical feasibility of the proposed circuit.

Overall, this chapter demonstrated that the AVCF–RGC based TIA achieves a balanced combination of gain, bandwidth, stability, and tolerance to environmental and process variations, making it a suitable choice for high-speed and low-power optical interconnect receiver applications.

Chapter 4

Modeling and Analysis of Receiver and Transmitter for Optical Interconnects (OIs)

4.1 Introduction

This chapter presents a comprehensive modeling of the transmitter and receiver circuits that form the essential building blocks of OIs. The transmitter circuits are designed to efficiently drive the capacitive load of optical modulators, while the receiver circuits amplify and restore the weak photocurrent into reliable digital signals. Several existing transmitter designs reported in literature are studied and modeled, including inverter-based buffers, tapered buffers, differential drivers, current-mode logic (CML) drivers, etc. The receiver section is modeled using a conventional TIA-based architecture. Together, these provide a baseline system model against which the performance of the proposed AVCF-RGC receiver (**Chapter 3**) will be compared.

This chapter develops a comprehensive, circuit-level model of the transmitter and receiver building blocks that enable high-speed, energy-efficient on-chip optical interconnects (OIs). On the transmitter side, the primary challenge is to drive the strongly capacitive optical modulator with minimal delay and controlled waveform distortion. On the receiver side, the objective is to convert sub-microampere photocurrents into rail-to-rail logic with wide bandwidth, low input-referred noise, and predictable gain. The transmitter path is modeled using existing topologies *i.e.*, superbuffers, inverter-based buffers and tapered buffers, while the receiver path is modeled using a novel transimpedance amplifier (TIA) topology discussed and designed in **Chapter 3**.

4.2 Circuit Modeling of Transmitter

Optical modulators are indispensable components in on-chip and off-chip OIs, as they serve as the electrical-to-optical (E/O) conversion interface between the electronic domain of CMOS

logic and the photonic domain of silicon waveguides. The primary role of a modulator is to encode high-speed electrical data onto an optical carrier, thereby enabling transmission over low-loss and high-bandwidth optical channels. The performance of the entire optical link is strongly determined by the efficiency, bandwidth, and energy consumption of the modulator, making it both a critical bottleneck and an enabler in photonic interconnects. Typical modulators have a load capacitance in the range of 50-100 fF [**?**]. To drive such a large capacitance with minimum delay, a buffer circuit is required, which is essentially a **single CMOS inverter** or **chain of CMOS inverters** or a specially designed driver stage inserted between the logic core and the load device. Its primary purpose is to amplify current-driving capability while preserving logic functionality, thereby ensuring fast charging and discharging of the modulator's capacitive load. A minimum-sized inverter has limited drive capability due to the finite on-resistance (R_{on}) of its PMOS and NMOS transistors. The propagation delay of the inverter is approximately expressed as:

$$t_{pd} \approx R_{on} \cdot C_L \tag{4.1}$$

From the above relation, it is evident that as C_L increases, the propagation delay increases proportionally, causing a significant degradation in performance. When the load capacitance is large, the charging and discharging currents provided by the inverter transistors are insufficient to achieve fast voltage transitions, thereby increasing the rise and fall times of the signal.

The degradation of slew rate due to a large capacitive load not only affects timing but also compromises signal integrity. Slow transitions may result in short-circuit currents in the subsequent gates, since both the PMOS and NMOS transistors in those gates remain momentarily conductive during the transition. This increases dynamic power dissipation and can lead to erroneous logic levels under high-speed operation.

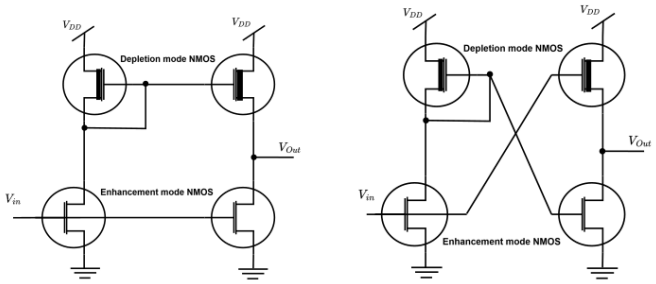
Furthermore, a single inverter faces practical limitations in terms of fanout. If an inverter is required to drive multiple gates simultaneously, the effective load capacitance is given by:

$$C_L = N \cdot C_{in} \tag{4.2}$$

where N is the fanout factor and C_{in} is the input capacitance of one gate. Thus, the delay scales linearly with fanout. For large values of N, the delay can become several times the intrinsic gate delay, making the circuit unable to meet performance requirements. In cases where interconnects extend off-chip, the capacitance is often orders of magnitude larger than the intrinsic gate capacitance, leading to even more severe performance bottlenecks.

4.2.1 Super Buffers

A superbuffer is a modified buffer circuit that overcomes the asymmetry of conventional CMOS inverters in sourcing and sinking currents when driving large capacitive loads. In a standard



(a) Inverting Superbuffer. (b) Non Inverting Superbuffer.

Figure 4.1: Inverting and Non Inverting Superbuffers.

inverter, the pull-down NMOS transistor provides higher drive strength compared to the pull-up PMOS transistor due to the difference in carrier mobilities ($\mu_n >> \mu_p$), resulting in unequal rise and fall delays. The propagation delay of a standard inverter driving a capacitive load C_L can be expressed as

$$t_p \approx \frac{C_L V_{DD}}{I_{\text{drv}}}, \tag{4.3}$$

where I_{drv} is the effective drive current of the pull-up or pull-down device. Since the pull-up current in a conventional inverter is weaker, the high-to-low transition is typically faster than the low-to-high transition. In a superbuffer, this asymmetry is resolved by employing a *depletion-mode NMOS transistor* as the pull-up device and an enhancement-mode NMOS as the pull-down. The gate of the pull-up transistor is tied to the complement of the input signal, ensuring that whenever the pull-down is off, the pull-up is strongly turned on. The effective pull-up current in a superbuffer is approximately $I_{Pullup} \propto (V_{GS} - V_T)^2$ with V_{GS} being close to V_{DD}, thereby yielding nearly four times the current sourcing capability of a standard inverter of the same size. Similarly, the pull-down current is given by $I_{Pulldown} \propto (V_{DD} - V_T)^2$ and is comparable to that of the pull-up device, making the rise and fall transitions nearly symmetrical. Consequently, the propagation delay of a superbuffer is reduced and can be approximated as

$$t_{p,SB} \approx \frac{C_L V_{DD}}{I_{Pullup}} \approx \frac{C_L V_{DD}}{I_{Pulldown}}, \tag{4.4}$$

which is significantly smaller than the delay of a conventional buffer when driving the same capacitive load. This property makes superbuffers particularly attractive for **optical modulators**, whose input capacitances are typically in the range of tens to hundreds of femtofarads.

The two types of superbuffer circuits that are widely used are inverting and noninverting superbuffers (as shown in **Figure. 4.1**) that are symmetrical in their capability of sourcing and sinking charge into a capacitive load. In the *inverting* topology (Fig. 7a), a small inverter gener-

ates $\overline{V_{\text{in}}}$ that drives the pull-up gate, while the pull-down gate is driven by V_{in}. Hence, for $V_{\text{in}} = 0$ the pull-down is OFF and the pull-up sees a near-V_{DD} gate drive, sourcing strongly so that V_{out} rises; for $V_{\text{in}} = 1$ the pull-down turns ON and rapidly discharges the load, producing logic inversion with nearly symmetrical rise and fall times. In the *non-inverting* topology (Fig. 7b), the internal control nodes are cross-coupled such that the pull-up is driven ON when $V_{\text{in}} = 1$ and the pull-down is driven ON when $V_{\text{in}} = 0$, so V_{out} follows V_{in} while retaining balanced drive. In practice, depletion NMOS devices may be unavailable and NMOS pull-ups can limit V_{OH} to $\approx V_{DD} - V_T$; therefore, modern implementations often prefer a CMOS tapered inverter chain to obtain rail-to-rail swing and robust PVT performance.

4.2.2 Tapered Buffers

Tapered buffers are geometrically sized CMOS inverter chains where each successive stage is larger than the previous one by a fixed scale factor, also known as tapering factor (β). They are particularly attractive for purely capacitive loads [**?**]. For resistive loads, typically for long interconnect lines, repeater chains are used that constitute a chain of CMOS inverters [**?**]. The first inverter in the chain is a standard minimum-sized gate (W_{min}) as shown in Fig. Each subsequent inverter is larger, meaning its transistors are wider by a factor of β. This increases its current drive, making it faster at charging the next stage's input capacitance, but also increases its own input capacitance, resulting in a slowdown of the previous stage. Mathematical analysis shows there is an optimal scale factor (typically between 3 and 4 for CMOS) that minimises the total delay through the entire chain [**?**].

A tapered buffer is interposed between the logic registers and a large capacitive load to provide impedance isolation and sufficient drive strength. Its input exhibits high impedance, thereby preventing excessive loading of the upstream registers, while its geometrically sized stages can source and sink large currents to charge and discharge the load rapidly. Consequently, the buffer decouples the load from the logic, restores logic levels, and amplifies drive capability. Tapered buffers are a well-established CMOS structure, and numerous methodologies have been proposed that target different performance objectives. The most commonly addressed criteria are propagation delay, power dissipation, physical area, and, more recently, circuit reliability. Prior work generally employs analytic expressions to determine the β and the number of stages (N), yet these methods are heterogeneous, rarely consider all four criteria concurrently, and often produce conflicting recommendations. The work in [**?**] introduces a unified methodology that jointly selects the tapering factor- stage buffer, numbered 0 to $N-1$. The unification is realised by adopting consistent device and interconnect models to derive analytic expressions for all four metrics, yielding similarly structured formulas that can be composed into a single, multi-objective tapering framework.

The most simplistic version of the tapered buffer is Jaeger's model, where each stage of the buffer is represented by one conductor and one capacitor, as shown in **Figure. 4.2**. This

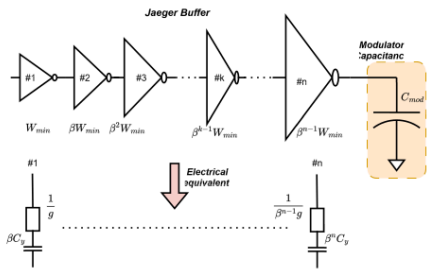


Figure 4.2: Jagaers Buffer Model

is an N stage buffer numbered 0 to $N-1$ with C_i and g being the logic level capacitance and conductance, respectively. The stage k has conductance, capacitance, and time constant given by:

$$g_k = \beta^k g \tag{4.5}$$

$$C_k = \beta^{k+1} C_i \tag{4.6}$$

$$\tau_k = \beta \tau_i \tag{4.7}$$

where τ_i is the logic level time constant given by $\tau_i = \frac{C_i}{g}$. The overall delay of a tapered buffer can be expressed as the sum of the time constants of its stages:

$$\tau_o = \sum_{k=0}^{n-1} \tau_k = n\beta\tau_i, \tag{4.8}$$

The effective load capacitance at the output stage is related to the input capacitance C_i by the geometric progression

$$C_L = \beta^n C_i. \tag{4.9}$$

From this relation, the number of stages required to drive a load C_L can be written as

$$n = \frac{\ln(C_L/C_i)}{\ln(\beta)}. \tag{4.10}$$

Substituting (4.10) into (4.8), the total buffer delay becomes

$$\tau_o = \tau_i \cdot \ln\left(\frac{C_L}{C_i}\right) \cdot \frac{\beta}{\ln(\beta)}. \tag{4.11}$$

Minimizing (4.11) with respect to β yields the well-known optimum taper factor

$$\beta^* = e \approx 2.72, \tag{4.12}$$

which leads to a minimum delay of

$$\tau_o^{\min} = e \cdot \left[\ln\left(\frac{C_L}{C_i}\right) \right] \tau_i. \tag{4.13}$$

The associated buffer penalty factor, which represents the normalized delay overhead due to insertion of the buffer chain, is

$$B_p = e \cdot \ln\left(\frac{C_L}{C_i}\right). \tag{4.14}$$

For more accuracy, the capacitance of each stage can be decomposed into an inherent output capacitance C_x (including diffusion, gate, and short-circuit contributions) and an incidental load capacitance C_y. Thus the reference stage capacitance becomes $C_i = C_x + C_y$. The equivalent short-circuit capacitance is estimated as

$$C_e \approx \frac{I_p}{3V_{DD}(\tau_r + \tau_f)}, \tag{4.15}$$

where I_p is the peak short-circuit current of the inverter, and τ_r and τ_f are the rise and fall times, respectively. With an effective transconductance g, the logic-level time constant is

$$\tau_i = \frac{C_x + C_y}{g}. \tag{4.16}$$

For the k-th stage in the tapered chain, the time constant becomes

$$\tau_k = \frac{\beta^k C_x + \beta^{k+1} C_y}{\beta^k g}, \tag{4.17}$$

which simplifies to

$$\tau_k = \frac{C_x + C_y + (\beta - 1)C_y}{g}, \tag{4.18}$$

or equivalently,

$$\tau_k = \left[1 + (\beta - 1)p\right] \tau_i, \tag{4.19}$$

where

$$p = \frac{C_y}{C_x + C_y}. \tag{4.20}$$

This formulation highlights the design trade-off: larger β reduces the number of stages needed but inflates the per-stage delay through the $(\beta - 1)p$ term, while moderate taper ratios (close to e) strike an optimal balance between speed and area overhead.

In this thesis work, a tapered buffer is designed having a tapering factor β with the above-discussed modeling equations. Typically β greater than $e = 2.72$ is selected [**?**]. The minimum-sized inverter, with width W_{min}, is used as the first stage, and the last inverter, having width $W_N = W_{min} \times \beta^{N-1}$, will drive the capacitive load of the modulator. As depicted in **Figure. 4.3**,

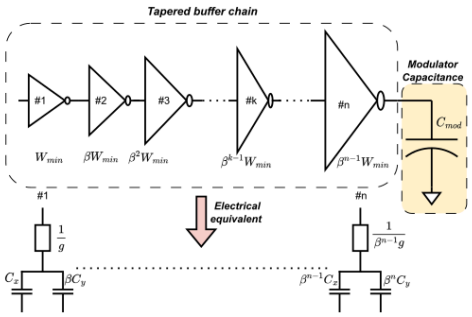


Figure 4.3: Tapered Buffer with split capacitor model

a split capacitor model of the buffer is considered where logic level capacitance is divided into two capacitances, *i.e.*, output capacitance (C_x) and incidental load capacitance (C_y). Depending on the ratio of $\frac{C_x}{C_y}$, the optimal value of β is selected. The value of N, as determined in [**?**], is dependent on β, modulator capacitance C_{mod}, and incidental load capacitance C_y [**?**]. It may be expressed as:

$$N = \frac{log\frac{C_{mod}}{C_y}}{log\beta}. \tag{4.21}$$

In DSM regimes, short-channel effects, such as velocity saturation effects, also play a vital role. Therefore, the alpha-power law MOSFET model is considered here for the delay and power calculations of the tapered buffer, as described in [**?**].

4.2.2.1 Waveguide

An optical signal propagating through a waveguide experiences a finite propagation delay, primarily determined by the effective refractive index of the guiding medium and the physical length of the interconnect. In this work, a strip polymer waveguide is considered with a core cross-sectional area of 2.25 μm^2 and an effective refractive index (n_{eff}) of 1.48, as reported in [**?**]. The waveguide is assumed to operate in a single mode regime, which simplifies the delay analysis by avoiding mode-dependent dispersion and multimode interference.

The time delay incurred by the optical signal traveling through the waveguide, denoted as t_{wg}, can be approximated using the following expression:

$$t_{wg} = \frac{n_{\text{eff}} \times L_{\text{int}}}{c}, \tag{4.22}$$

where L_{int} is the physical length of the OI, n_{eff} is the effective refractive index of the waveguide, and c is the speed of light in vacuum (approximately 3×10^8 m/s).

This expression stems from the fundamental definition of phase velocity in a waveguide

medium, where the signal velocity is reduced compared to free-space propagation due to the waveguide's refractive index. In this context, n_{eff} effectively models the modal confinement of the optical field within the core and cladding structure of the waveguide. The delay expression assumes negligible material and waveguide dispersion, and ignores any frequency-dependent or temperature-induced variations in n_{eff}.

Furthermore, the influence of waveguide geometry, such as width, height, and sidewall roughness, on n_{eff} and dispersion is not considered in this model. While such effects can become significant in high-precision photonic circuit design, their exclusion here allows for a simplified first-order analysis suitable for system-level modeling and estimation.

This delay metric is crucial in evaluating the performance of on-chip optical interconnects, particularly in applications that involve high-speed data transmission and tight timing budgets. The ability to accurately model waveguide delay enables more efficient design of photonic networks and better synchronization with electronic subsystems.

4.3 Receiver Modeling

For receiver modeling, a TIA is employed that converts the current generated by an MSM photodetector I_{pd} to the corresponding voltage (V_{TIA}) while holding the input node at very low impedance (virtual ground) to suppress the RC pole formed by detector and wiring capacitances, as shown in **Figure. 2.10**. Its behavior is compactly described by the transimpedance $Z_T(s)$ via $V_{\text{out}}(s) = Z_T(s) i_{\text{pd}}(s)$, with dc gain $R_T \equiv Z_T(0)$. A low input impedance ($R_{\text{in}} \approx R_f/(1+A_0)$ is created at he input using a negative feedback configuration by placing a feedback resistance R_f around the amplifier with loop gain A_0 is large, allowing high gain without the bandwidth penalty of a simple load resistor. A single grounded resistor can also perform the same function and yield an equivalent transimpedance gain, but the impedance observed by the input current i_{pd} encounters a high impedance R_f as shown in **Figure. 2.10**. On the other hand, the introduction of a TIA offers a significant advantage, as the input pole is given by $\omega_{p0} = \frac{1}{RC_F(1+A_0)}$, in contrast to the expression $\omega_p = \frac{1}{RC_F}$ shown in **Figure. 2.10**. This reduction in the pole frequency due to the gain term $(1+A_0)$ effectively results in a higher bandwidth. Also, if I_{in} suffers from nonlinearity due to large voltage swings across it, the TIA structure mitigates this effect by reducing these swings approximately by a factor of $(1+A_0)$. For optimal performance, the core amplifier with gain A_0 must be carefully designed so that the TIA simultaneously achieves wide bandwidth, low input-referred noise current, and adequate gain to minimize noise contributions from subsequent stages. In practice, the amplifier is typically implemented as a single-stage design, with its bandwidth selected to be at least 70% of the target data rate [**?**].

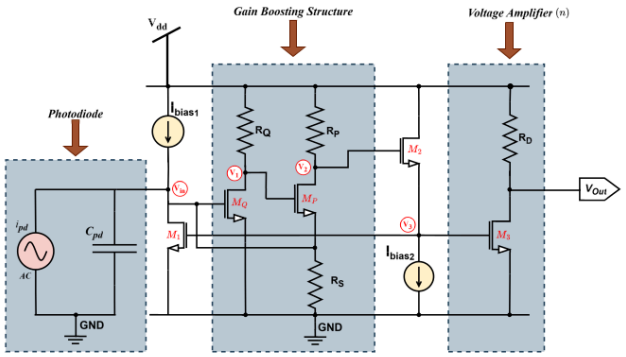


Figure 4.4: The Schematic of AVCF-RGC TIA.

4.4 Receiver modeling using novel AVCF RGC TIA

In this work, an AVCF-based RGC TIA, as shown in **Figure. 4.4** is incorporated into the OI receiver block [**?**]. This novel structure consists of an Active voltage current feedback (AVCF) based TIA employing a regulated gain cascade (RGC) stage in its path that aids in increasing the effective transconductance of the proposed TIA with a factor of $1+g_{m_q}R_{oq}$. This TIA is preferred over an open-loop common gate (CG) or RGC configuration due to the inclusion of local voltage-current feedback that acts as negative feedback. Additionally, this TIA decreases the input impedance, minimizing the impact of parasitics and photodiode capacitance at the input, further extending the bandwidth of the receiver [**?**]. By constructing the equivalent small signal model of the AVCF based RGC TIA, the expression for the DC gain of this TIA is calculated as [**?**]:

$$Z_{\text{TIA}}(0) \cong \frac{g_{m_3}g_{m_p}(1+g_{m_q}R_{oq})R_{in_{eq}}R_{op}R_{oq}r_{op}}{R_{oq}R_D r_{op}\left[1+g_{m_p}R_{in_{eq}}(1-g_{m_q}R_{oq})\right]-g_{m_3}g_{m_p}R_D R_{oq}(1+g_{m_q}R_{oq})} \\ (1-g_{m_1}r_{op})R_{in_{eq}}R_{op}. \quad (4.23)$$

where g_{m_i} are the transconductances of the MOSFETS M_i as shown in **Figure. 4.4**, r_{o_p}, r_{o_q} are the output resistances of MOSFET's M_P and M_Q, respectively. R_D is the drain resistance of M_3. R_{op}, R_{oq}, and $R_{in_{eq}}$ are given by $R_P \parallel r_{op}$, $R_P \parallel r_{op}$, and $R_P \parallel r_{op}$ respectively.

Assuming the input pole is the dominant pole, the 3-dB frequency of the TIA is given by [**?**]:

$$\omega_{3-dB} \approx \frac{g_{m_p}(1+g_{m_q}R_q)(g_{m_1}+g_{m_p})R_p - g_{m_p}}{C_{pd}+C_{gs_q}}. \quad (4.24)$$

So, from the above equation, the component responsible for bandwidth extension is the gain of

the local feedback stage. It can be further increased, but care must be taken as this could bring stability and linearity issues to the circuit, leading to more power consumption [**?**].

Only a single stage of the TIA is used, ensuring stability is not an issue [**?**]. The delay of the front-end stage will be the dominating factor as the input pole holds the position of the dominant pole. Therefore, considering the 10-90% rise time of an *RC* circuit, which is given by 2.2 times the *RC* product of the input stage. The delay of the receiver circuit ($T_{d_{rec}}$) is determined solely by the receiver's bandwidth requirements, measured in radians per second. Therefore, it can be expressed as follows:

$$T_{d_{rec}} \cong 2.2 \times R_{in}^{TIA} \times C_{input}. \tag{4.25}$$

The above equation states that $T_{d_{rec}}$ can be reduced by increasing the width of the transistors; however, power consumption will increase. This trade-off must be carefully dealt with for an optimised design. A common source (CS) amplifier stage is integrated into the front-end TIA to boost the signal up to the supply voltage V_{dd}. The gain of the CS stage is given by:

$$A_v = -g_{m_3}\left(r_{o_3} \parallel R_D\right). \tag{4.26}$$

where g_{m_3} is the transconductance and r_{o_p} is the output resistance of the M_3. To calculate the number of gain stages (n) used, the voltage swing constraint of V_{dd} is applied at the output. Hence:

$$V_{out} = V_{dd} = (I_{pd} \times Z_{TIA}) \times A_v^n. \tag{4.27}$$

Next, the MSM photodetector is modeled as having responsivity R, a measure of optical conversion efficiency to electrical. It is expressed as follows:

$$R = \frac{I_{pd}}{IOP}. \tag{4.28}$$

Its value lies in the $0.4 - 0.9$ A/W range. The incident photons are converted into electron-hole pairs, which generate I_{pd}. The ratio of the number of electron-hole pairs generated to the number of incident photons is expressed as quantum efficiency η. The R is related to η by the following expression:

$$R = \eta \frac{q}{h\nu}. \tag{4.29}$$

where q is the electronic charge, $h\nu$ is the energy of a single photon, h is the Planck constant. ν is the frequency of the incident light with wavelength λ, and is expressed as $\nu = c/\lambda$, where c is the speed of light in vacuum. A high quantum efficiency is desirable in order to withstand high optical losses within the waveguide without increasing the IOP. To model the delay of MSM photodetectors, the initial step involves calculating the response time, which depends on

electrode width as outlined in ref. [?]:

$$\tau_{response} = \sqrt{\tau_{tr}^2 + \tau_{RC_{det}}^2}. \tag{4.30}$$

where τ_{tr} is the carrier transit time, which represents the time taken for the photo-generated carriers to drift to the electrical contact, and $\tau_{RC_{det}}$ is the RC time constant of the detector due to load resistance R, and the detected capacitance C_{det}. The delay of the MSM photodetector can be described as [?]:

$$\tau_d = 0.315 \times \sqrt{\tau_{tr}^2 + \tau_{RC_{det}}^2}. \tag{4.31}$$

The 3-dB bandwidth of this MSM photodetector also depends upon the response time and is given by Eq. (4.32) [?]:

$$f_{3-dB}^{det} = \frac{0.35}{\sqrt{\tau_{tr}^2 + \tau_{RC_{det}}^2}}. \tag{4.32}$$

The τ_{tr} in MSM photodetectors sets a limit on their delay and bandwidth as dictated by equation (4.31) and (4.32), respectively.

The signal delay, power dissipation, and PDP of all three components *i.e.*, transmitter, waveguide, and receiver, are obtained for the OI system by performing transient analysis using SPICE simulations. Next, the Cu and SWCNT-B interconnect will be modelled, and performance parameters will be compared later with the OI system.

4.5 Summary

This chapter presented the modelling framework for the transmitter and receiver circuits used in optical interconnect (OI) systems. The discussion began with an overview of the key functional blocks in a typical OI link and the motivation for modelling them at the circuit level. The modelling of the modulator driver, optical modulator, photodetector, and the front-end TIA was described in detail, with emphasis on capturing the electrical and electro-optic interactions that determine overall link behaviour. Particular attention was given to device capacitances, parasitic elements, and nonlinearities that influence modulation efficiency, bandwidth, and signal integrity.

Analytical expressions and compact models were developed to represent the behaviour of each component under realistic operating conditions. The transmitter model incorporated the modulator's voltage-dependent characteristics and the driver's ability to provide the required swing at high data rates. On the receiver side, the photodiode model included responsivity, junction capacitance, dark current, and thermal noise, while the TIA model accounted for gain, bandwidth, and noise contributions. These models were subsequently integrated to study end-to-end link behaviour.

Simulation results obtained from the proposed models were presented to evaluate delay,

energy per bit, output eye quality, voltage swing, and sensitivity of the OI link. The results highlighted the influence of device parameters, load capacitances, and biasing conditions on link performance and provided insight into important design trade-offs involving speed, power consumption, and signal quality. Overall, this chapter established the essential modelling foundation required for system-level analysis and set the stage for the temperature-aware and comparative evaluation discussed in the next chapter.

Chapter 5

Thermally Aware Modeling and Comparative Analysis of OI with CNT and Cu

5.1 Introduction

The relentless miniaturization in nanoscale VLSI circuits has pushed conventional interconnects to performance bottlenecks, including delay, power dissipation, and thermal challenges. This chapter investigates the temperature-dependent performance of OIs at 22 nm and 14 nm nodes, employing a novel AVCF-RGC TIA, designed in **Chapter 3**. A detailed circuit-level model is developed, accounting for temperature effects on carrier mobility, waveguide propagation loss, photodetector responsivity, and receiver transconductance. A comparative analysis of OI with CNT and Cu interconnect is also performed, taking into account the performance metrics. For this, the modeling of Cu and SWCNT-B is also performed at both technology nodes. Thermal effects are also incorporated in the modelling and later compared with OI in terms of delay, power dissipation, and power delay product (PDP). In deep submicrometer regimes, Cu interconnects suffer from parasitic capacitance and resistivity increases due to electron scattering and electromigration, leading to substantial power dissipation and signal delay bottlenecks [**?**, **?**, **?**, **?**, **?**, **?**]. Temperature fluctuations exacerbate these issues by degrading carrier mobility and shifting threshold voltages, further slowing down propagation and limiting bandwidth [**?**]. This thermal sensitivity underscores the need for interconnect solutions that can maintain high-speed operation even at elevated temperatures [**?**, **?**]. Optical interconnects (OIs) offer compelling advantages of high bandwidth, minimal crosstalk, and immunity to electromagnetic interference [**?**, **?**].

5.2 Temperature-Dependent Modeling of Optical Interconnects (OI)

Temperature fluctuations can degrade or enhance the performance of OIs by altering several critical parameters. Although data modulation in this system is performed by a multiple quantum well (MQW) modulator, the modulated optical signal still depends directly on the laser source's output power. The laser provides the continuous-wave (CW) optical carrier, which the MQW modulator modulates according to the data signal. The complete circuit configurations used for the photodiode front-end receiver and the optical modulator driver are presented in **Figure 3.3** and **Figure 4.3**, respectively. These figures illustrate the AVCF–RGC transimpedance amplifier topology and the tapered buffer chain that collectively enable high-speed, low-distortion optical signal processing.

5.3 Temperature Effect

Temperature has a significant impact on the laser's slope efficiency (η_s), output optical power (P_{laser}), and threshold current (I_{th}), all of which directly influence the received optical power at the photodetector. The temperature-dependent laser output power is given by

$$P_{\text{laser}}(T) = \eta_s(T)\,(I_{\text{bias}} - I_{\text{th}}(T))\,, \tag{5.1}$$

where $\eta_s(T)$ is the temperature-dependent slope efficiency and $I_{\text{th}}(T)$ is the threshold current. The slope efficiency typically decays exponentially with temperature:

$$\eta_s(T) = \eta_s(T_0)\,e^{-\gamma(T-T_0)}, \tag{5.2}$$

where γ is the thermal degradation coefficient and T_0 is the reference temperature. The threshold current increases approximately linearly with temperature:

$$I_{\text{th}}(T) = I_{\text{th}}(T_0) + \frac{dI_{\text{th}}}{dT}\,(T - T_0), \tag{5.3}$$

with $\frac{dI_{\text{th}}}{dT} \approx$ 1–2 mA/K for typical semiconductor lasers [**?**].

In multi-quantum-well (MQW) modulators, temperature variations shift the resonant wavelength through the thermo-optic effect:

$$\Delta\lambda_{\text{res}}(T) = \lambda_0\,\alpha_{\text{TO}}\,(T - T_0), \tag{5.4}$$

where α_{TO} is the thermo-optic coefficient (typically $\sim 1.86 \times 10^{-4}$/K for silicon [**?**]) and λ_0 is the nominal resonance wavelength. The effective refractive index also changes with tempera-

ture:

$$n_{\text{eff}}(T) = n_{\text{eff}}(T_0) + \alpha_{\text{TO}}(T - T_0). \tag{5.5}$$

Waveguide propagation loss increases approximately linearly with temperature:

$$\alpha_{\text{wg}}(T) = \alpha_{\text{wg}}(T_0) + \beta\,(T - T_0), \tag{5.6}$$

where $\beta \approx 0.005$–0.01 dB/mm/K [**?**]. These variations increase insertion loss and reduce modulation efficiency.

Photodiode responsivity decreases with temperature due to reduced quantum efficiency and increased dark current:

$$R_{\text{PD}}(T) = R_{\text{PD}}(T_0)\,[1 - \delta_{\text{PD}}(T - T_0)], \tag{5.7}$$

where δ_{PD} is the temperature coefficient of responsivity.

In the receiver circuit, temperature variations influence the transconductance (g_m), parasitic capacitances, and output resistance of the AVCF–RGC TIA. The DC gain may be approximated as

$$Z_{\text{TIA}}(T) \propto g_{m_p}(T)\,\left(1 + g_{m_q} R_{oq}\right) R_{op}(T), \tag{5.8}$$

where $g_{m_p}(T)$ decreases with temperature while $R_{op}(T)$ and parasitic capacitances increase. As a result, the bandwidth reduces as

$$f_{3\,\text{dB}}(T) \propto \frac{g_m(T)}{2\pi\left(C_{pd} + C_{gs}(T)\right)}. \tag{5.9}$$

5.3.1 Impact on Optical Link Performance

The cumulative effect of the above temperature-dependent variations degrades the received optical power, expressed as:

$$P_{\text{rx}}(T) = P_{\text{laser}}(T)\,L_{\text{mod}}(T)\,e^{-\alpha_{\text{wg}}(T)L}\,\eta_{\text{couple}}, \tag{5.10}$$

where $L_{\text{mod}}(T)$ represents the temperature-dependent modulator insertion loss, L is the waveguide length, and η_{couple} is the coupling efficiency. A reduction in $P_{\text{rx}}(T)$ yields a lower photocurrent at the photodetector, reducing link margin and degrading BER performance. Consequently, incorporating temperature-dependent models for the laser, modulator, waveguide, photodiode, and TIA is essential for accurate prediction of OI link metrics such as delay, power, and PDP in thermally constrained VLSI systems.

The subsequent section introduces the analytical modeling of Cu and SWCNT-B interconnects, after which the framework is expanded to account for temperature-dependent electrical, thermal, and reliability characteristics. A comprehensive comparison is later performed, first as a function of interconnect length at room temperature, and subsequently as a function of

temperature across the device's operational range.

5.4 Modeling of Cu and SWCNT-B interconnect

5.4.1 Modeling parameters of Cu Interconnect

A Cu interconnect is represented by a conductor with a rectangular cross-section, as shown in **Figure. 5.1**, having equivalent impedance parameters such as resistance, inductance, and capacitance (RLC). The variables l, w, t, and s represent length, width, thickness, and inter-wire distance, respectively, for a Cu wire adjacent to the ground (GND) plane and other wires. In the DSM regime, the effective resistivity of Cu increases as the scaled dimensions become comparable to the electron mean free path (MFP), due to which electrons experience collisions due to surface and grain boundary scattering [**?**].

To calculate the technology-dependent resistivity (ρ_{total}) of the Cu wire, a Fuchs and Sondheimer model is considered for surface scattering [**?**], and a Mayadas and Shatzkes model for grain boundary scattering [**?**]. As a result, the total resistivity is given by:

$$\rho_{total} = \rho_0 \left[\left(1 + \frac{3}{4}(1-p)\frac{l_0}{w} \right) + \left(\frac{1}{3} \Big/ \left(\frac{1}{3} - \frac{\alpha}{2} + \alpha^2 - \alpha^3 \left(1 + \frac{1}{\alpha} \right) \right) \right) \right], \tag{5.11}$$

with

$$\alpha = \frac{l_0}{d}\left(\frac{R}{1-R} \right),$$

The bulk resistivity of Cu material is assumed to be $\approx 1.9\mu\Omega \cdot cm$. p is the specular scattering modeling parameter of an electron at the interface (≈ 0.6 [**?**]), l_0 is the The bulk MFP of

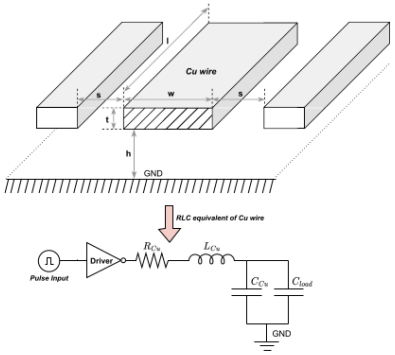


Figure 5.1: The cross-section view of Copper interconnect and its equivalent RLC circuit.

electrons is taken $\approx 40nm$, and w is the width of wire dictated by ITRS [**?**]. d is the average size of grain (assumed $d \approx w$), and R is the reflectivity coefficient at grain boundary (≈ 0.5 [**?**]). After calculating resistivity, the above modeling, ρ_{total} is calculated for 22nm and 14nm technology, from which, after calculating the resistivity, the resistance value of the Cu wire is calculated by Eq. (5.12):

$$R_{Cu} = \rho_{total}\left(\frac{l}{w \cdot t}\right). \tag{5.12}$$

Next, the capacitance of the Cu wire is modeled using the model proposed by Sakurai and Tamaru in [**?**]. The ground capacitance of a single line in the vicinity of two neighbouring wires is given by:

$$C_g = \varepsilon \cdot l\left[1.15\frac{w}{y} + 2.80\left(\frac{t}{y}\right)^{0.222}\right], \tag{5.13}$$

and the total coupling capacitance between them is given by:

$$C_{cc} = \varepsilon \cdot l\left[\left(\left(0.03\frac{w}{y} + 0.83\frac{t}{y} - 0.07\left(\frac{t}{y}\right)^{0.222}\right) \cdot \left(\frac{y}{s}\right)^{1.34}\right]\right), \tag{5.14}$$

The total capacitance (C_{cu}) of the Cu wire is calculated as:

$$C_{cu} = \varepsilon \cdot l\left[\left(1.15\frac{w}{y} + 2.80\left(\frac{t}{y}\right)^{0.222}\right) + \left(0.06\frac{w}{y} + 1.66\left(\frac{t}{y}\right) - 0.14\left(\frac{t}{y}\right)^{0.222}\right) \cdot \left(\frac{y}{s}\right)^{1.34}\right]. \tag{5.15}$$

where t is the thickness of the wire dictated by the aspect ratio (AR) of the wire in the particular technology given by ITRS [**?**], y is the inter-metal layer spacing ($\approx 4t$), and $s = w$. The first component in Eq. (5.15) is due to the ground capacitance of a single line in the vicinity of two neighboring wires, and the second component is due to the coupling capacitance.

The inductance of the Cu wire is modeled as [**?**]:

$$L_{Cu} = \frac{\mu_0}{2\pi} \cdot l\left[ln\left(\frac{2l}{w+t}\right) + \frac{1}{2} + 0.33\left(\frac{w+t}{l}\right)\right]. \tag{5.16}$$

where μ_0 is the free space permeability ($4\pi \times 10^{-7} H/m$), and l is the length of the wire.

5.4.2 Modeling parameters of SWCNT Bundle Interconnect

This section will develop the electrical circuit model of SWCNT-B to compare it with OI and Cu interconnects. The RLC of the SWCNT-B interconnect is extracted. When densely packed isolated SWCNTs are placed in parallel, a SWCNT-B structure is formed as shown in **Figure. 5.2** . Here, it is assumed that all the SWCNTs are metallic and the spacing x between the centre of two SWCNT tubes is $x = d_{sw}$, as this gives the best VLSI interconnect performance [**?**]. The

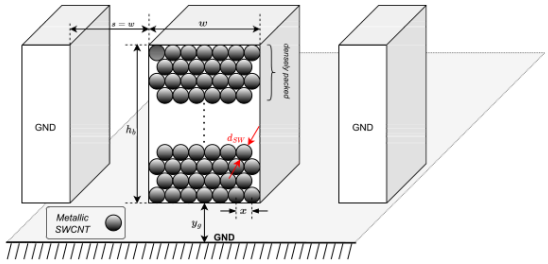


Figure 5.2: The cross-section view of SWCNT-B interconnect.

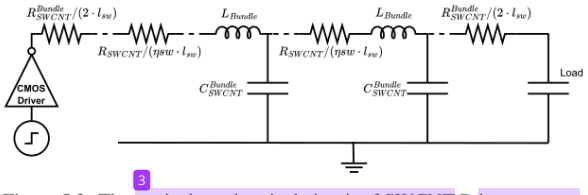


Figure 5.3: The equivalent electrical circuit of SWCNT-B interconnect.

equivalent electrical circuit of SWCNT-B interconnect is shown in **Figure. 5.3**.

The metal-CNT imperfect contact resistance ($R_{contact}$) is also assumed, having a value around a few kΩs per tube. Consequently, the total resistance of an SWCNT-B interconnect is expressed as [**?**]:

$$R_{SWCNT}^{Bundle} \approx \frac{h}{4e^2}\left(\frac{l_{SW}}{l_{0_{SW}}}\right)\Big/\eta_{sw} \tag{5.17}$$

where η_{sw} is the number of metallic SWCNT tubes in a bundle and is expressed by a number of rows (n_{ro}) and columns (n_{co}) in a bundle as:

$$\eta_{sw} = \begin{cases} n_{ro}n_{co} - \frac{n_{ro}}{2} & \text{if } n_{ro}\text{is even,} \\ n_{ro}n_{co} - \frac{n_{ro}-1}{2} & \text{if } n_{ro}\text{is odd.} \end{cases} \tag{5.18}$$

where $n_{co} = (w - d_{sw})/x$, and $n_{ro} = \left((h_b - d_{sw})/\frac{\sqrt{3}}{2}x\right) + 1$. The variable h_b is the thickness of the CNT bundle (dictated by AR) as depicted in **Figure. 5.2**. At small bias voltages, and $d_{sw} = 1nm$, $l_{0_{sw}}$ assumes a value of 2.8 $\mu m/nm$ and 0.9 $\mu m/nm$ for ideal and practical models respectively [**?**].

For the SWCNT-B, the total capacitance is the series combination of the C_E^{Bundle}, and C_Q^{Bundle} expressed as [**?**]:

$$C_{SWCNT}^{Bundle} = \frac{C_E^{Bundle} \cdot C_Q^{Bundle}}{C_E^{Bundle} + C_Q^{Bundle}}. \tag{5.19}$$

where C_E^{Bundle} and C_Q^{Bundle} are the expressions for electrostatic capacitance and quantum capacitance of an SWCNT-B interconnect, respectively, and the expressions for the same can be found in [?,?].

The total inductance of the SWCNT-B is given by [?]:

$$L_{SWCNT}^{Bundle} = \frac{L_{sw}^{kin}}{\eta_{sw}} + L_{sw}^{mag}. \tag{5.20}$$

5.5 Temperature dependent modeling of Copper and CNT interconnects

A generalized accurate model of the Cu and SWCNT-B interconnect placed on the SiC substrate is crucial for predicting temperature-dependent performance parameters and later comparing with OI. In addition to bias and geometrical effects, thermal effects such as acoustic and optical phonon effects are also considered in the modeling to validate the measurement results [?, ?]. The different types of scattering phenomena at elevated temperatures are considered to determine the effective MFP of the conducting electrons. For the best performance of the VLSI interconnect, all the CNTs considered are metallic [?]. Therefore, electron-phonon scattering is considered to include optical, acoustic, and zone-boundary scattering [?]. Acoustic scattering, which is directly dependent upon temperature and diameter, is given by:

$$\lambda_{aco} = \frac{\lambda_{aco}(300)}{d_0}\frac{300d}{T}, \tag{5.21}$$

where $\lambda_{aco}(300)$ is 1600 nm for $d_0 = 1.8nm$ at 300K [?]. An electron can undergo scattering as a result of electric field acceleration as well as the absorption of an optical or zone boundary phonon. Therefore, the MFP due to acceleration is given by:

$$\lambda_{op-zb,field}(T) = \frac{h\Omega - k_bT}{eV/L} + \left[\lambda_{op,zb}(300)\frac{d}{d_0}\frac{N_{op-zb}(300)+1}{N_{op-zb}(T)+1}\right], \tag{5.22}$$

and due to absorption is given by:

$$\lambda_{op-zb,abs}(T) = \lambda_{op-zb}(300)\frac{d}{d_0}\left[\frac{N_{op-zb}(300)+1}{N_{op,zb}(T)}\right], \tag{5.23}$$

where $\lambda_{op,zb}(300) \approx 15nm$ [?], k_b is the boltzman's constant, $\lambda_{op-zb}(300) = 1/[exp(h\Omega/k_bT)-1]$ is the optical or zone-boundary phonon state density. Therefore, the effective MFP due to the emission field and absorption is given by:

$$\frac{1}{\lambda_{eff}^{op-zb}(T)} = \frac{1}{\lambda_{op-zb,field}(T)} + \frac{1}{\lambda_{op-zb,abs}(T)}, \tag{5.24}$$

Also, in graphene materials, the surface roughness (λ_{sr}) effect is prominent, which modifies the length of the inter-carbon bond and hopping parameters [**?**], and is given by:

$$\lambda_{sr} = \frac{C}{\delta_{sr}^4}(nm), \tag{5.25}$$

where $C = 2.07 \times 10^9$ is the fitting parameter and δ_{sr} is the substrate roughness amplitude, which is assumed to be 10 pm for SiC substrate [**?**]. Thus, the temperature-dependent effective MFP of the rough interconnect is given by:

$$\lambda_{eff}(T) = \left(\frac{1}{\lambda_{aco}} + \frac{1}{\lambda_{op-zb,field}(T)} + \frac{1}{\lambda_{op-zb,abs}(T)} + \frac{1}{\lambda_{sr}} \right)^{-1}. \tag{5.26}$$

This $\lambda_{eff}(T)$ affects the resistance of the SWCNT-B interconnect, which includes contact resistance (R_C), intrinsic quantum resistance $\left(\frac{h}{4e^2}\right)$, and scattering resistance $\left(\frac{h}{4e^2}\frac{L_{SW}}{\lambda_{eff}(T)}\right)$. For Cu interconnect, temperature-dependent resistivity affects the resistance of the Cu wire by the following expression:

$$\rho(T) = \rho_{tech}(1 + a(T - T_0)). \tag{5.27}$$

where ρ_{tech} is technology dependent resistivity, a is the temperature coefficient of resistivity for Cu, T_0 is the room temperature. Thus, the temperature variations affect the RLC parameters, thereby affecting the ampacity in terms of delay, power, and PDP of the interconnects.

5.6 Comparative Analysis of OI, Cu, and SWCNT-B interconnect

For comparison of optical, Cu, and SWCNT-B interconnect at 22nm and 14nm technology nodes, the Tanner EDA tool is utilized, taking into account the PTM model files (level 54). A transient analysis evaluates the performance metrics *i.e.*, delay, power, and PDP for the three technologies using SPICE analysis. This analysis involves subjecting the circuits to a step input pulse terminated by a load, usually a capacitive load. The propagation delay is calculated by the average value of 50 % rise and fall times in the SPICE measure.

For the OI system, all simulation and analytical parameters are summarized in **Table 5.3**. The RLC parameters of the Cu and SWCNT-B interconnects are derived using the global interconnect definitions listed in **Table 5.3**. To effectively mitigate the large distributed RLC loading inherent in long global interconnects, CMOS inverter-based repeaters are utilized, exploiting the repeater-insertion technique to minimize delay and optimize overall link performance. Introducing n_{rep} repeater stages partitions the interconnect into n_{rep} segments, thereby reducing the effective RLC loading per segment by the same factor, as depicted in **Figure 5.4**. The network is terminated with a load capacitance, and the CMOS driver transistors are sized with

Table 5.1: Optical interconnect parameters.

Parameter	Value
β (tapering factor)	3.6
C_{Mod} (fF)	50
C_{det} (fF)	50
η_{eff} (waveguide)	1.48
I_{pd} (μA)	100
R_{D_1} (kΩ)	970
R_{D_2} (kΩ)	1.1
R_S (kΩ)	1

Table 5.2: Electrical interconnect parameters.

Technology (nm)	22	14
Width, w (nm)	28	16
Aspect ratio (AR)	2.34	2.34
Height, t (nm)	65.5	37.5
n_{rep} (no. of repeaters)	15	12
ε_r (dielectric constant)	2.5	2.3
Y_{ILD} thickness, y_g	57	36

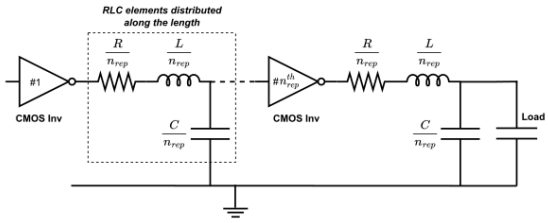


Figure 5.4: The simulation setup for Cu and SWCNT-B interconnect.

$(W/L)_n \approx 100$, ensuring sufficient drive strength for global interconnects.

Figure. 5.5a shows the total delay of the OI incorporating a novel AVCF RGC TIA at global interconnect lengths.

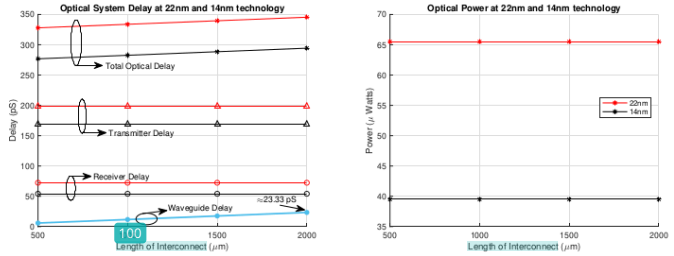
At global interconnect lengths ($\geq 1000\mu m$), the delay introduced by the waveguide is significantly less than the transmitter and receiver delay, as depicted in **Figure. 4.1a**. This is due to the fact that most of the delay is introduced in end devices rather than in waveguides. For instance, at a global length of 2000 μm, the value of t_{wg} is only 23.33pS (**Figure. 5.5a**).

The receiver delay is due to the dominant pole assumption at the input of the AVCF RGC TIA due to the presence of a large $C_{det} \approx 50fF$.

The transmitter delay arises because the CMOS tapered buffer drives the modulator load ($C_{mod} \approx 50fF$). It is investigated from the **Figure. 5.5a** and **5.5b** that as the technology node advances, the total optical system delay and power are decreased due to the enhanced perfor-

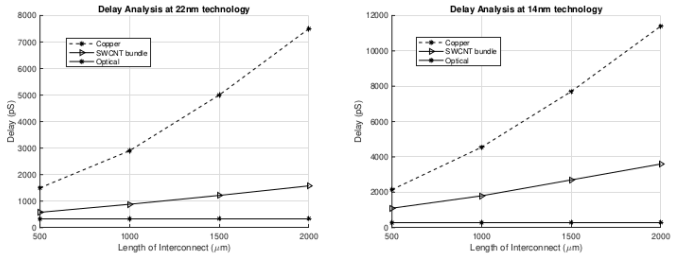
Table 5.3: Simulation parameters for Electrical Interconnects [**?**].

Technology (nm)	**22**	**14**
Width, w (nm)	28	16
Aspect ratio (AR)	2.34	2.34
Height, t (nm)	65.5	37.5
n_{rep} (no. of repeaters)	15	12
$\frac{W}{L}$ (driving size)	100	100
ε_r (dielectric constant)	2.5	2.3
Y_{ILD} thickness, y_g	57	36



(a) Delay (b) Power dissipation

Figure 5.5: Delay and Power dissipation of OI for different lengths at 22*nm* and 14*nm* technology.

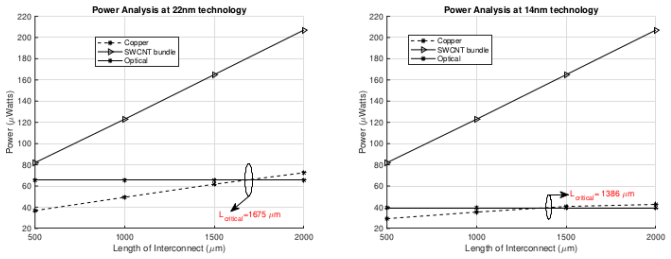


(a) Delay analysis at 22nm technology. (b) Delay analysis at 14nm technology.

Figure 5.6: Delay comparison of Optical, Cu, and SWCNT-B interconnect for different lengths.

mance of the transmitter and receiver electrical circuits.

Figure. 5.6b and **5.6a** demonstrate the delay introduced by optical, Cu, and SWCNT-B interconnect for global lengths at 22*nm* and 14*nm* technology. It is evident from the figure that the OI delay is minimal at global lengths. This is because the optical transmitter and receiver circuits are located at opposite ends of the waveguide, in contrast to Cu and SWCNT-B, which are spread out along its whole length. The results in **Figure. 5.5** illustrate that the delay of Cu and SWCNT-B interconnect increases rapidly with length attributed to the rising RLC charac-



(a) Power analysis at 22nm technology. (b) Power analysis at 14nm technology.

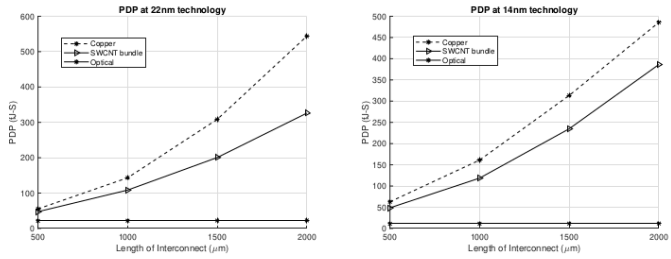
Figure 5.7: Power comparison of Optical, Cu, and SWCNT-B interconnect for different lengths.

teristics of these materials as technology progresses from 22*nm* to 14*nm*. However, the delay for the OI is diminished because the MOSFET-based circuits exhibit enhanced performance. For instance, at a global length of 1000μm, OI shows an improvement of 88.47 % and 62.15 % over Cu and SWCNT-B interconnect delay, respectively. Similarly, for 14*nm* technology, the delay improvement increases to 93.68 % and 84.29 %, respectively.

The power in OI is minimized by optimizing the number of stages in the transmitter and receiver circuits. The total power dissipation for all three technologies is plotted for 22*nm* and 14*nm*. **Figure. 5.7** illustrates that the SWCNT-B dissipates more power than Cu and optical for all global lengths. This is because the capacitance of SWCNT-B is greater than that of Cu, resulting in the dominant energy component, the switching energy (CV^2), reaching a maximum for SWCNT-B interconnects. OI is more power efficient than Cu at global lengths greater than the critical length since the nature of power dissipation is static rather than dynamic. For 22*nm* and 14*nm* technology, the critical length is calculated as ≈1600μm and ≈1300 μm, respectively, as shown in **Figure. 5.7a** and **Figure. 5.7b**. Additionally, OI exhibits higher resistance to interference and crosstalk, thereby diminishing the need for supplementary circuitry that would have consumed more power.

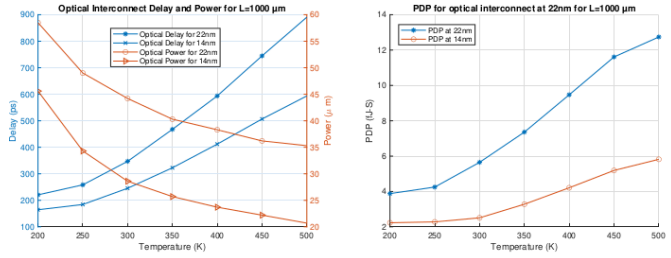
For a fair comparison, a figure of merit known as the PDP is defined, taking into account the effects of delay and power dissipation for all three technologies. It is evident from **Figure. 5.8** that the PDP of OI (C_{mod}=C_{dec}= 50fF) lies in the range of 21-23 *fJs* at all lengths, which is the lowest among SWCNT-B and Cu for 22*nm* technology. The same trend is followed for 14*nm* technology, where the PDP of OI lies in the 10-13 *fJs* range. These findings highlight the potential advantages of using OI as an interconnect technology for future VLSI IC applications at global interconnect lengths.

Figure. 5.9a shows the delay, power, and PDP of the OI that incorporates a novel AVCF-based RGC TIA at various temperatures ranging from 200K to 500K with a step of 50K. It is investigated from the **Figure. 5.9a** and **5.9b** show that with increasing temperature, the total delay of the optical system increases. At the same time, the power dissipation decreases, but the



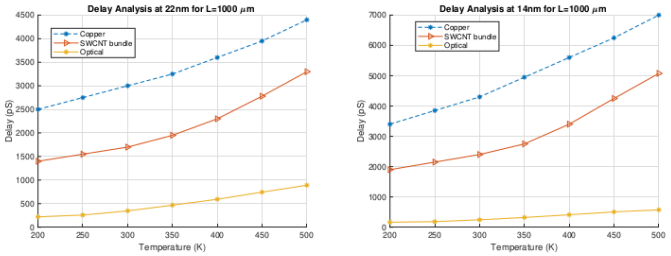
(a) PDP at 22nm technology. (b) PDP at 14nm technology.

Figure 5.8: PDP comparison of Optical, Cu, and SWCNT-B interconnect for different lengths.



(a) Delay and Power (b) PDP

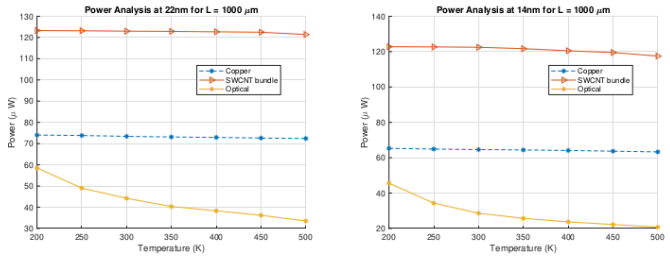
Figure 5.9: Delay and Power dissipation of OI for different temperatures.



(a) Delay analysis at 22nm (b) Delay analysis at 14nm

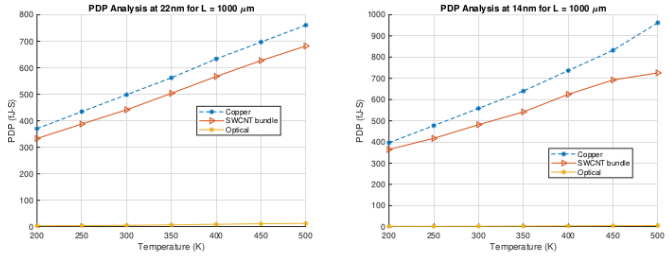
Figure 5.10: Delay of Cu, SWCNT-B, and OI for different temperatures.

effect of delay is dominant, as depicted by PDP analysis in **Figure. 5.9b** for both technology nodes. The PDP increases with temperature, and the rise is steeper for 22*nm*, indicating that higher temperatures cause a more significant deterioration in performance.



(a) Power analysis at 22nm (b) Power analysis at 14nm

Figure 5.11: Power dissipation of Cu, SWCNT-B, and OI for different temperatures.



(a) PDP analysis for 22nm (b) PDP analysis at 14nm

Figure 5.12: PDP of Cu, SWCNT-B, and OI for different temperatures.

Figure. 5.10 depicts the delay analysis for Cu, SWCNT-B and OI at different temperatures for global length, i.e. 1000 μm. OI shows superior performance in terms of delay, especially at higher temperatures, compared to traditional Cu and SWCNT-B interconnects for both technology nodes. This is because the RLC of the Cu and SWCNT-B interconnects increases with temperature, leading to greater delays. In contrast, the delay in the OI is primarily determined by the end devices, making it less sensitive to temperature changes.

Figure. 5.11 shows that OIs consume significantly less power than Cu and SWCNT-B, with power dissipation further decreasing as temperature rises across both technology nodes. This highlights their strong suitability for energy-efficient, low-power designs. The delay and power improvements of OI compared to Cu and SWCNT-B are also reflected in **Table. 5.4**.

Figure. 5.12 shows that the OI has significantly lower PDP values compared to the Cu and SWCNT-B interconnects, especially at higher temperatures.

The OI results are validated by comparing them with existing published data, as shown in **Table 5.5**. The table details the structure/material used for the transmitter, waveguide, and receiver, and compares the delay and power consumption between the existing design and the

Table 5.4: Delay and power improvement of optical interconnects (OI) compared to Cu and SWCNT bundle interconnects at different temperatures.

Temp. (K)	**Delay Improvement (%)**				**Power Improvement (%)**			
	vs Cu		**vs SWCNT-B**		**vs Cu**		**vs SWCNT-B**	
	22 nm	14 nm	22 nm	14 nm	22 nm	14 nm	22 nm	14 nm
200	91.7	95.2	84.2	91.3	21.0	30.0	52.5	63.0
250	90.6	95.2	83.3	91.4	33.0	47.0	60.0	72.0
300	88.4	94.3	79.6	89.7	40.0	55.0	64.0	76.5
350	85.6	93.5	76.0	88.2	44.0	60.0	67.2	78.9
400	83.5	92.7	74.2	87.9	47.0	63.0	68.8	80.3
450	81.2	91.9	73.2	88.0	50.0	65.0	70.5	81.5
500	79.8	91.8	73.0	88.7	53.0	67.0	72.5	82.4

Table 5.5: Comparison of the proposed design of OI with existing designs in the literature.

Parameters	[?]	[?]	[?]	[?]	[?]	**This work**
Transmitter Driver	Superbuffer	Tapered Inverters	Buffer Chain	-	Buffer Chain	Tapered Buffer
Waveguide	Polymer & silicon-on-insulator (SOI)	Free Space OI	$Si-SiO_2$ core cladding	-	-	Polymer Waveguide
Receiver TIA	Common source with current source load and R_F	CMOS Inverter with R_F	CMOS inverter with R_F	Push pull amplifier	CMOS inverter with R_F	AVCF RGC based TIA
Technology (nm)	100	22	22	100	50	22 & 14
Delay (ps)	-	114.9	80	-	250	325 & 270
Power (mW)	-	11.5	12.2	-	3.5	0.065 & 0.04

proposed design for the OI. This indicates that OIs remain the most temperature-resistant and energy-efficient, further highlighting their suitability for future technology nodes.

Summary

This chapter focused on the temperature-aware modelling and comparative evaluation of three major interconnect technologies: copper (Cu) interconnects, single wall carbon nanotube bundles (SWCNT-B), and optical interconnects (OI). The chapter began by discussing how temperature variations affect the electrical, optical, and material properties of these technologies, and highlighted the need for incorporating temperature dependence into nanoscale performance models. Key temperature-sensitive parameters, such as resistivity in Cu, carrier mobility in

CNTs, refractive index and absorption in optical components, and thermal noise contributions, were included to ensure accurate and realistic modelling.

For Cu interconnects, the influence of increased resistivity at elevated temperatures on delay, energy consumption, and signal integrity was analysed. In the case of CNT bundles, temperature-dependent modifications in mean free path, quasi-ballistic transport, and equivalent RC parameters were modelled. For optical interconnects, the effects of temperature on modulator efficiency, wavelength shift, insertion loss, photodiode responsivity, and TIA performance were considered. These temperature-aware models were used to evaluate interconnect delay, energy per bit, power dissipation, and signal quality across a broad operational temperature range.

A comparative analysis of Cu, CNT, and OI technologies was then presented using the developed models. The results showed that copper interconnects exhibit substantial degradation in both delay and energy efficiency with rising temperature. CNT bundles demonstrated better thermal resilience but still suffered from notable performance variations at higher temperatures. Optical interconnects, by contrast, maintained stable delay and energy characteristics due to their reduced sensitivity to electrical RC effects. Eye diagrams, sensitivity plots, and analytical performance curves consistently indicated the thermal robustness of optical links.

Overall, this chapter demonstrated the significance of temperature-aware modelling and established that optical interconnects offer the most stable and energy-efficient operation among the evaluated technologies. These insights support the adoption of OI architectures for high-speed and thermally constrained future computing systems.

Chapter 6

Conclusion and Future Scope

6.1 Conclusion

This thesis has delivered an integrated investigation of circuit design, interconnect modeling, and thermally aware performance analysis aimed at enabling next-generation optical interconnects (OIs) for high-speed global communication in advanced VLSI systems. The work is organised around three core technical contributions: the realisation of a high-performance transimpedance amplifier (TIA), the formulation of a complete OI link model and its benchmarking against state-of-the-art electrical alternatives, and an extensive temperature-dependent evaluation at deeply scaled CMOS nodes. Collectively, these contributions outline a coherent design methodology for achieving energy-efficient, scalable, and thermally resilient optical communication infrastructures for future integrated circuits.

The first segment of the research concentrated on the design of a novel active voltage current feedback regulated gain cascode based transimpedance amplifier (AVCF RGC TIA) in a 0.18 µm CMOS process. By employing AVCF, the architecture simultaneously reduces input impedance, improves gain linearity, and extends bandwidth without relying on bulky inductive components. The implemented TIA achieved a transimpedance gain of 62 dBΩ, a bandwidth of 8.2 GHz, and an input-referred noise spectral density of 21 $pA/\sqrt{Hz}$ while operating at a power level of only 14.5 mW. These results demonstrate that the proposed receiver front-end satisfies the key requirements of compactness, low power consumption, and high-speed operation, making it highly suitable for on-chip and chip-to-chip photonic communication systems. The design outcomes confirm the AVCF RGC TIA topology as a promising circuit-level solution for CMOS-compatible photonic receivers.

The second major contribution of the thesis expanded the scope from device-level design to system-level OI modeling. Analytical and SPICE models were developed for all major optical components, including the laser transmitter, polymer waveguide, photodetector, and the newly proposed AVCF RGC TIA based receiver. These models were then used to compare the performance of optical links with that of copper (Cu) and single-wall carbon nanotube bundle

(SWCNT-B) interconnects over global interconnect lengths ranging from 500 µm to 2000 µm. The evaluation revealed that OIs offer substantial improvements in delay, power consumption, and power delay product (PDP), especially at longer distances. A critical length was identified, approximately 1600 µm at the 22 nm node and 1300 µm at the 14 nm node, beyond which OIs become significantly more advantageous than electrical interconnects. This behavior validates the growing importance of photonic links as electrical interconnects approach their scaling limits due to resistive losses, RC delay, and signal integrity constraints.

In the third portion of the research, temperature effects were introduced to create a realistic evaluation framework for future VLSI systems. Temperature-dependent models were constructed for photonic devices, waveguide loss mechanisms, photodetector responsivity, and the AVCF–RGC TIA. These models were evaluated across a wide thermal range of 200–500 K at 22 nm and 14 nm technology nodes. The results show that Cu and SWCNT-B interconnects experience considerable performance degradation at elevated temperatures due to increased resistivity and enhanced phonon scattering, whereas OIs maintain significantly better performance. Quantitatively, OIs demonstrate improvements of up to 90% in delay and nearly 80% in power consumption compared to electrical alternatives at high temperatures. The temperature study also identified the receiver TIA as the principal thermal bottleneck, primarily due to temperature-induced reductions in transconductance and increases in parasitic capacitances. This insight emphasizes the necessity of thermally optimized receiver circuits in practical photonic integrated circuit (PIC) platforms.

These three interconnected studies lead to several broader conclusions. First, OIs inherently provide superior scalability in bandwidth, latency, and energy efficiency as technology nodes continue to shrink and global communication distances increase. Second, the integration of advanced TIAs such as the AVCF RGC architecture is essential for harnessing the advantages of photonic signal propagation and converting them into tangible system-level improvements. Third, although OIs are naturally more immune to thermal effects than electrical interconnects, the thermal behavior of the transmitter and receiver circuits remains a critical factor that must be addressed to guarantee reliable operation under realistic on-chip temperature gradients.

In closing, this thesis establishes a comprehensive framework—encompassing circuit design, interconnect modeling, and thermal analysis—for the evaluation and optimization of optical interconnects in deeply scaled VLSI technologies. The collective findings strongly advocate for the adoption of CMOS-compatible photonic signaling to overcome the inherent delay, energy, and reliability challenges of traditional electrical interconnects. Furthermore, the presented work lays the foundation for future research in thermally adaptive receiver architectures, wavelength-division-multiplexed (WDM) photonic NoCs, and full electro-photonic co-design strategies. These advancements hold the potential to shape the next generation of high-performance computing systems built upon robust and energy-efficient optical communication fabrics.

6.2 Future Scope

While this thesis has established a comprehensive foundation for the design, modeling, and thermal evaluation of OIs, several research directions remain open for exploration to further advance the practical deployment of photonic communication systems in next-generation VLSI technologies.

A natural extension of this work is to incorporate process-induced variations and statistical uncertainty into the interconnect models. Variations in waveguide dimensions, photodetector responsivity, and transistor parameters can significantly influence link performance, particularly as feature sizes continue to scale. Integrating Monte Carlo simulations and spatial temperature-gradient modeling would enable a more rigorous assessment of reliability under combined process and thermal fluctuations. Such analyses are essential for developing robust design guidelines for large-scale photonic systems.

Future work may also explore multi-wavelength and dense wavelength-division multiplexing (WDM) architectures. While this thesis has focused on single-wavelength links, practical photonic networks-on-chip (NoCs) increasingly rely on multi-channel communication to achieve higher throughput. Studying resonance drift, thermal crosstalk among closely spaced microring modulators, and wavelength-dependent dispersion effects could provide deeper insights into the scalability and stability of WDM-based optical fabrics under real operating conditions.

Thermal management remains a critical area of importance. Although OIs exhibit inherent resilience to temperature variations compared to electrical interconnects, the receiver TIA, modulator biasing circuits, and laser drivers remain sensitive to thermal fluctuations. Incorporating active and passive thermal-control techniques—such as integrated micro-heaters, thermoelectric coolers, adaptive bias circuits, and temperature-compensated front-end architectures—may substantially improve link robustness. Co-optimizing these mechanisms with the AVCF–RGC TIA topology could yield thermally adaptive receivers capable of sustaining high-speed operation across wide temperature ranges.

Another promising avenue is the co-design of complete electro-photonic systems. Joint optimization of modulator drivers, laser bias networks, TIA architectures, and digital backend circuits (e.g., CDR and equalization) would enable tighter control over energy-per-bit and help address signal integrity challenges at high data rates. Such a holistic approach is increasingly important as photonics becomes more deeply integrated with advanced CMOS nodes.

The emerging domains of chiplet-based architectures and 3D integrated circuits open additional opportunities for optical interconnect research. Optical through-silicon vias (O-TSVs), interposer-level photonic routing, and vertical thermal gradients introduce new modeling and reliability challenges. Extending the thermal and interconnect framework developed in this thesis to these platforms can provide valuable insights into heterogeneous integration strategies that combine electronics, photonics, and packaging technologies.

Experimental validation represents another crucial future milestone. Fabricating a silicon photonic testchip that incorporates microring modulators, waveguides, germanium photodetectors, and the AVCF–RGC TIA would allow direct measurement of the temperature-dependent behaviors predicted by the models. Such measurements would strengthen confidence in the simulation framework and guide further refinement of device and circuit models.

Finally, the use of machine learning and data-driven modeling techniques has significant potential to accelerate design exploration. Neural-network-based surrogate models, physics-informed learning frameworks, and reinforcement learning for adaptive biasing could markedly improve accuracy, reduce simulation time, and enable real-time optimization of photonic link parameters under dynamic thermal conditions.

In summary, expanding the scope of this work toward variability modeling, WDM architectures, advanced thermal management, electro-photonic co-design, heterogeneous system integration, experimental validation, and AI-assisted compact modeling will further enhance the applicability and reliability of optical interconnects in future high-performance computing systems.

6.3 Publications

The following publications have been derived from the work developed in this thesis:

1. Singh, Amoldeep, Karmjit Singh Sandha, and Mayank Kumar Rai. "Design and Analysis of Active Feedback RGC-Based Transimpedance Receiver Circuit for Optical Interconnects." Journal of Circuits, Systems and Computers 33.07 (2024): 2450125. **(Published)**

2. Singh, Amoldeep, Karmjit Singh Sandha, and Mayank Kumar Rai. "Investigation of Optical Interconnects for nano-scale VLSI applications." Micro and Nanostructures 196 (2024): 207987. **(Published)**

3. Singh, Amoldeep, Karmjit Singh Sandha, and Mayank Kumar Rai. "Assessing Thermal Effects and Performance of Optical Interconnects vs. Copper and CNT Interconnects in Deep-Submicron Technologies", special issue in Journal of Nonlinear Optical Physics & Materials. **(Communicated)**

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