A

Thesis Report

On

"A Novel all Digital 4-bit Flash ADC"

Submitted towards the partial fulfilment of requirement for the award of degree of

Master of Technology

In

VLSI Design

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DECLARATION

I, Ashima Gupta hereby declare that the work presented in this thesis entitled "**A Novel all Digital 4-bit Flash ADC**" in partial fulfillment of the requirement for the award of degree of Master of Technology in VLSI DESIGN submitted at Electronics and Communication Engineering Department, Thapar University, Patiala is an authentic record of work carried out under supervision of Dr. Alpana Agarwal (Associate Professor), ECED, Thapar University from 2015 to 2017. The matter presented in this has not been submitted either in part or full to any other university or institute for the award of any other degree.

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Place: Patiala

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It is certified that the above statement made by the student is correct to the best of my knowledge and belief.

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Ashima Gupta

ABSTRACT

In recent years, Digital signal processing has progressed drastically with technology. However it with not provide the same level of advantage as of analog IC. To get the more accurate output, we will process the signal into digital form. Most of the communication need wireless signal i.e. digital signal but in the real world, all outputs are analog in nature so we have to convert analog signal to digital signal to communicate to the real world. For an efficient system, all blocks should be fast. This fact has led researchers to develop and implement high speed analog-to- digital converters (ADCs) with low power consumption.

This research work describes the highly digital 4-bit 200-MS flash ADC whose major part can be synthesized from verilog code thus achieving low power and reduces the much needed time to market. The comparator circuit is created by CMOS using Inverter and NAND-NOR logic gates. The proposed circuits are simulated in Cadence Virtuoso Analog Design Environment and Anolog Mixed Signaling (AMS) in SCL 180 nm CMOS technology with a supply voltage of 1.8V. Also, the proposed digital-in-process flash ADC has been proposed. The SNDR, SNR and SFDR equal to 24.4566 dB, 25.9533 dB and 30.2788 dB. It provides an effective number of bits (ENOB) equal to 3.7702. The DNL of this flash ADC is $\pm$0.25 LSB and INL is $\pm$0.6 LSB.

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LIST OF ACRONYMS

IC	Integrated Circuits
ADC	Analog-To-Digital Converters
MOSFET	Metal Oxide Semiconductor Field Effect Transistor
DNL	Differential Non-Linearity
INL	Integral Non-Linearity
FFT	Fast Fourier Transform
SNR	Signal To Noise Ratio
THD	Total Harmonic Distortion
SFDR	Spurious Free Dynamic Range
SNDR or SINAD	Signal To Noise And Distortion Ratio
ENOB	Effective Number Of Bits
CML	Current-Mode Logic
PDP	Power-Delay Product
TG	Transmission Gate
MUX	Multiplexer
PLA	Programmable Logic Array
ROM	Read Only Memory
SHA	Sample And Hold Amplifier
PMOS	Positive-Channel Metal-Oxide Semiconductor
CMOS	Complementary Metal-Oxide Semiconductor
NMOS	Negative-Channel Metal-Oxide Semiconductor
PVT	Process-Voltage-Temperature
DQOS	Differential Quasi One Junction SQUID
SDSW	Symmetric Differential SQUID Wheel Comparator
DSW	Differential SQUID Wheel Comparator
CVTC	Complementary Voltage-To-Time Converter
DAC	Digital To Analog Converter
ADE	Analog Design Environment
SCL	Semi Conductor Laboratory
VLSI	Very Large Scale Integration
MOSCAP	Metal-Oxide Semiconductor Capacitor
DC	Direct Current
SAR	Successive Approximation Register

ICMR	Input Common-Mode Range
DP	Differential Pair
MIMCAP	Metal Insulator Metal Capacitor
PIPCAP	Poly Insulator Poly Capacitor
MOMCAP	Metal Oxide Metal Capacitor
AMS	Anolog Mixed Signaling

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CHAPTER 1
INTRODUCTION

1.1 MOTIVATION

With the rapid growth of technology and shrinking device size, low power is an important parameter in lightweight portable and battery operated devices. To reduce the power dissipation either the value of capacitance should be less which is partially dependent on device size or lower the supply voltage that debases the performance of the circuit. With the reduction in supply voltage, threshold voltage should be reduced. Moreover, as technology scales down according to Moore's law, it does not have more effect on dynamic power but it has a great impact on static power dissipation [1]. So power dissipation has become a critical design metric for a large number of CMOS circuits. The digital ICs are more advantageous than analog ICs in the exploding market with new lightweight portable devices [2]. Digital IC (Integrated Circuits) design focuses on maximizing circuit density, logical correctness and placing circuits so that clock and timing signals are routed efficiently whereas analog IC designs are more complex and costly than digital IC design to meet the similar performance constraints. Also, with the advancement in wireless technology, the world without wires come into the picture so digital signal processing has evolved dramatically in recent time. Most of the communication need wireless signal i.e. digital signal but in the real world, all outputs are analog in nature so there is a need to convert analog signal to digital signal to communicate to the real world. To make the world a digital platform, the analog design can be re-constructed into digital form.

1.2 SYSTEM ARCHITECTURE OF FLASH ADC

Flash analog-to-digital converters have high data conversion speed due to its parallel operation, low resolution and large chip area. Flash ADC has three main blocks: Resistive network, comparator and thermometer to binary encoder. It is suitable for the applications where high speed and low resolution is required like magnetic read channel applications, optical data recording and digital communication system. For N-bit flash ADC 2^N resistors are required to generate reference voltage for 2^N-1 comparators. The comparator will compare input voltage (Vin) with the reference voltage (V_{ref}). If V_{in} is greater than V_{ref} the output of the comparator goes high and when V_{in} is less than the V_{ref} then the output of the comparator goes low. Hence the output of comparator is a string of '0's and '1's called thermometer code. A thermometer contains all zeros where the reference level is less than input voltage and all ones where the reference level is greater than the input voltage. A simple 2^N-1: N

encoder will convert thermometer code to binary code. Flash ADC is designed for 4-bit (N = 4) so number of resistors required are 2^4=16 and number of comparators required are 2^4-1=15. The important block of flash ADC is comparator on which the speed of the ADC depends. ADC is used in many applications like high speed instrumentation, radar, wireless sensor network, digital oscilloscopes, digital TVs, camera and optical communications.

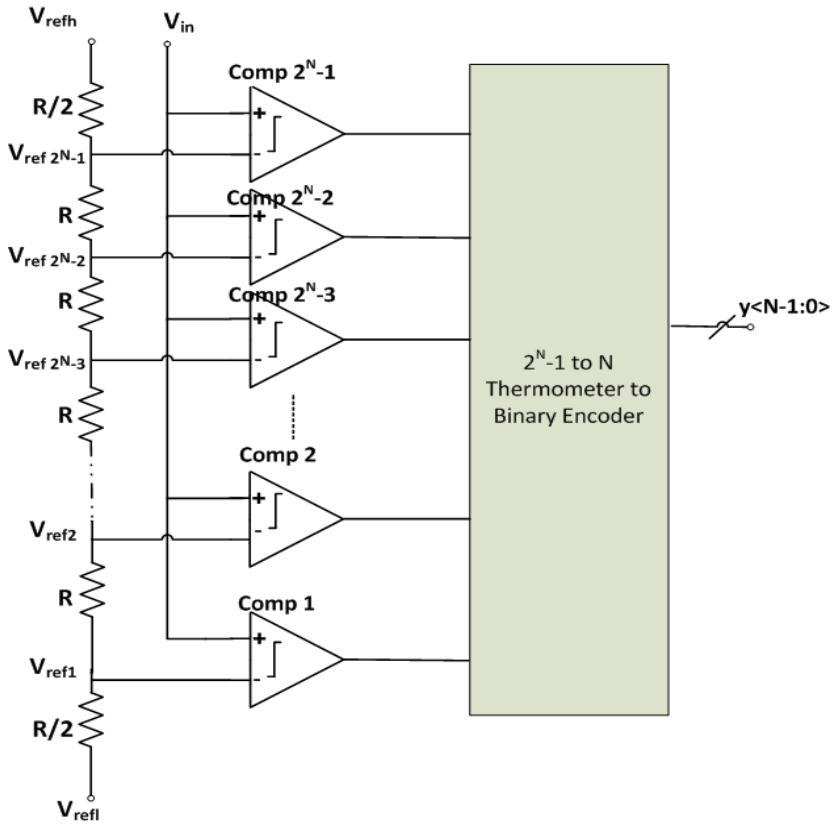


Figure 1.1 Conceptual block diagram of flash ADC.

Figure1.1 shows basic block diagram of flash ADC which comprises of reference ladder, comparator and an encoder. For N-bit flash ADC 2^N resistors are required to generate the reference voltage for 2^N-1 comparators [3]. The reference ladder generate the reference voltage that is compared with the input and the outputs of comparators are series of 1's and 0's which forms thermometer code [4], that is converted to binary output patterns using a Wallace tree encoder [5] through a bubble error correction logic. A simple 2^N-1: N encoder will convert thermometer code to binary code.

1.3 FLASH ADC PERFORMANCE METRICS

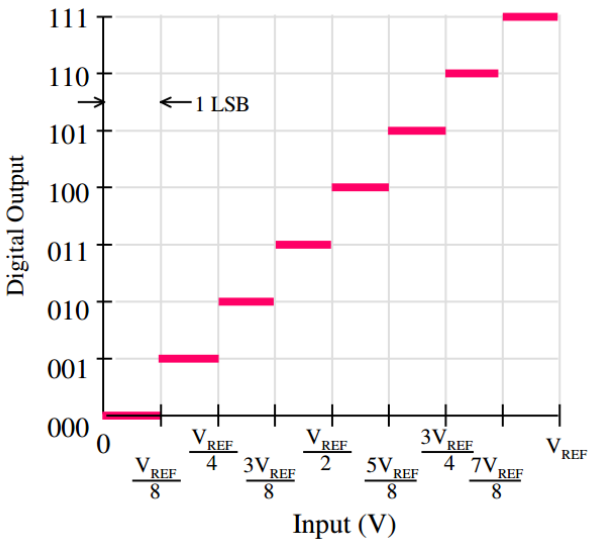


Figure 1.2: Transfer function of an ideal 3-bit ADC [6]

Figure 1.2 shows the transfer characteristics of an ideal 3-bit ADC with high level reference voltage V_{ref} = 8V. Practically, on conversion from analog to digital a certain level of inaccuracy is introduced and the input-output characteristic stair-case is not so perfect. First, converting continuous time signal to discrete time signal causes loss of information at the times lying between two consecutive sample instants. Second, the samples chosen also do not get converted to digital equivalent accurately. In order to improve accuracy, resolution needs to be improved by using more number of bits and hence smaller step size. To get smaller steps using same number of bits, the reference voltage can be reduced. But small reference voltage means that it can process only small range of input voltages *i.e*. lower input dynamic range. This can also cause a small signal to be lost in noise thus reducing signal to noise ratio.

It is important to analyze the performance of an ADC before use. It can be done using some performance metrics. Performance metrics for any type of ADC including pipelined ADC can be categorized into two groups *viz*. static and dynamic parameters.

1.3.1 Static Performance Metrics

Static metrics are measured with respect to low frequency signals, ramp signals or even DC signals. These parameters include gain, offset, differential non-linearity (DNL), integral non-linearity (INL). Static metrics can be determined from ADC input-output characteristics as follows:

- **Quantization error:** Referring to characteristics in Figure 1.2, ADC input of 0 V produces output code of 0 0 0. As voltage increases towards $V_{ref}/8$, output code still remains 0 0 0. Thus, as input approaches towards $V_{ref}/8$, error increases as the input is no longer 0 V.

Again, at V_{ref}/8 V, code changes to 0 0 1 *i.e.* output accurately represents input and hence error is reduced to zero. Plot for quantization error is shown in Figure 1.3.

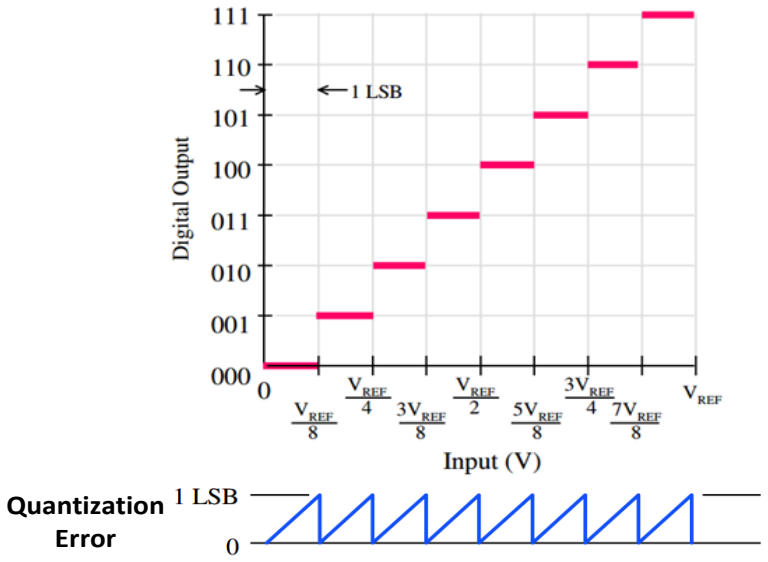


Figure 1.3: Quantization error in ideal 3-bit ADC [6]

Magnitude of error ranges from 0 to 1 LSB, and this range is called quantization uncertainty. Maximum quantization uncertainty is called quantization error. Cause of quantization error is finite resolution of ADC. An *n*-bit ADC can resolve the input into 2^n discrete levels only. Each output code represents a range of input values called 'quanta' (q) [6].

By adding half LSB offset to the ADC input, the output digital level would change half LSB before it would have changed without offset. Thus, quantization error ranges from -0.5 LSB to +0.5 LSB instead of 0 to 1 LSB as shown in Figure 1.4.

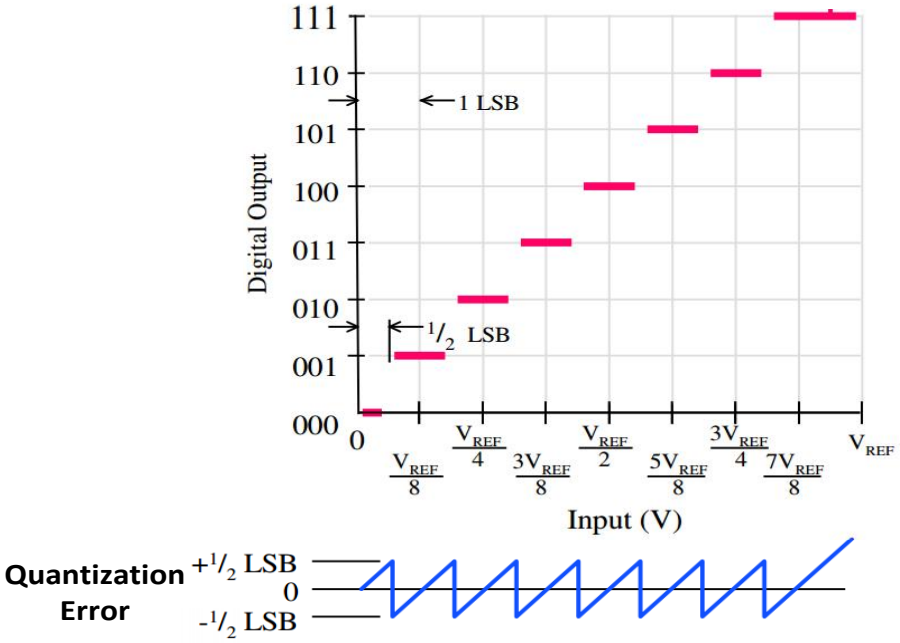


Figure 1.4: Quantization error in 3-bit ADC with added half LSB offset to input [6]

- **Offset error**: Ideally, an input voltage of quanta/2 *i.e.* q/2 should cause transition from zero to next digital code. Difference between this ideal input voltage and practical input voltage where first output digital code transition takes place is known as zero scale offset error, shown in Figure 1.5.

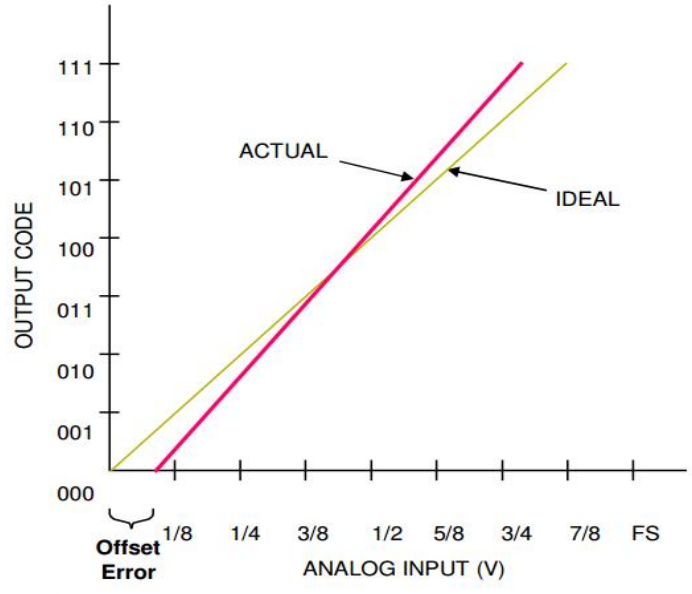


Figure 1.5: Zero scale offset error in ADC transfer function [6]

If first transition input voltage is higher than the ideal, offset error is said to be positive. If first transition input voltage is lower than the ideal, offset error is said to be negative. Error in real full scale output transition point from the ideal value is called full scale offset error, shown in Figure 1.6.

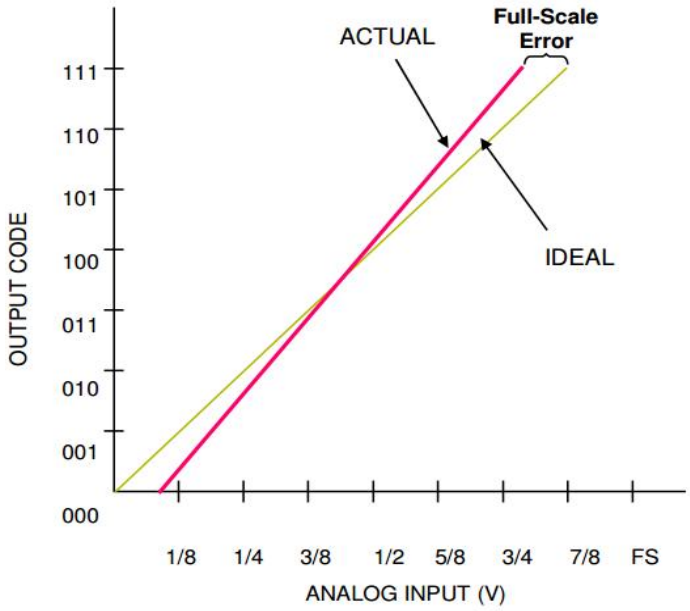


Figure 1.6: Full scale offset error in ADC transfer function [6]

Full scale offset error is caused partly due to offset error and partly due to error in slope of input-output characteristic. Since offset error is constant, it can easily be eliminated. Offset error is measured in percent of full scale voltage (Volts) or in terms of LSBs.

- **Gain error**: Full scale gain error is defined as difference between ideal and practical slopes of transfer function.

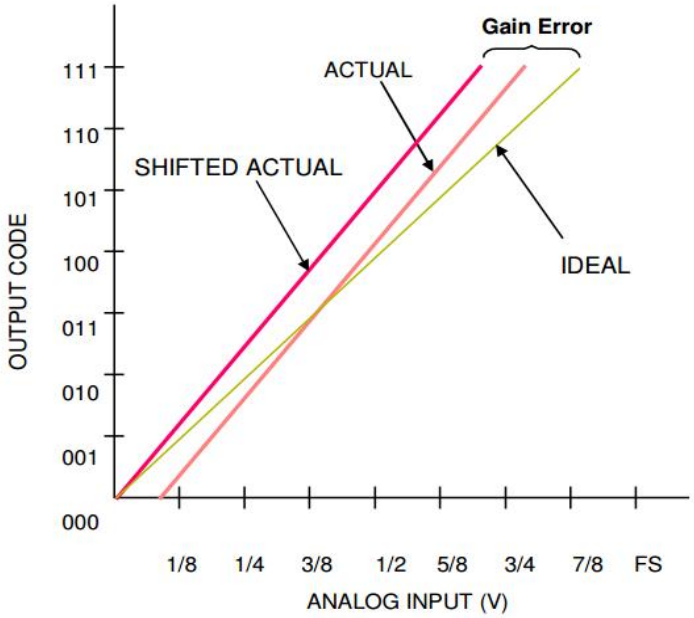


Figure 1.7: Gain offset error in ADC transfer function [6]

Thus, if actual transfer function is shifted in a way such that zero scale offset error gets nullified, then the difference between actual and ideal last transitions in ADC transfer stair case is called gain error, as demonstrated in Figure 1.7.

$$gain\ error\ =\ full\ scale\ error - offset\ error \tag{1.1}$$

It is measured in terms of LSBs or as percentage of ideal full scale voltage.

- **Non-Linearity**: There are the following two kinds of non-linearity errors measured to quantify the effect of errors in ADCs.

(i) Differential non-linearity or differential linearity error

(ii) Integral non-linearity or integral linearity error

- **Differential non-linearity or differential linearity error:** Differential non-linearity describes the error in step size. In ideal converter, output digital code transitions occur exactly after each LSB. Thus, step size of transfer characteristic stair case shown in Figure 1.8 should be 1 LSB. The difference between ideal step size and maximum practical step size

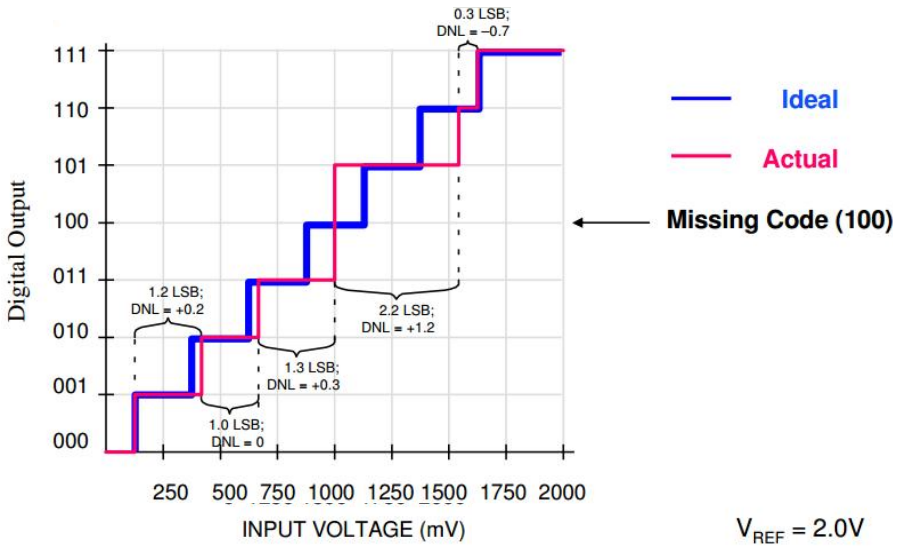


Figure 1.8: Differential non-linearity error and missing code [6]

occurring in transfer function is called differential non-linearity. Referring Figure 1.8, digital output level does not change even if input changes from 1000 mV to above 1500 mV. Code 1 0 0 never appears at output. This is called missing code.

- **Integral non-linearity or integral linearity error:** Integral non-linearity describes the bow in transfer function *i.e.* describes deviation from ideal linear transfer curve as shown in Figure 1.9. Integral linearity error is the measure of straightness of transfer function. Quantization, offset and gain errors are not included in INL. The size of differential non-linearity determines the integral linearity of the ADC.

- **Total unadjusted error**: It is a comprehensive specification that includes linearity errors, gain error, offset errors. It is worst case deviation from ideal device performance [6].

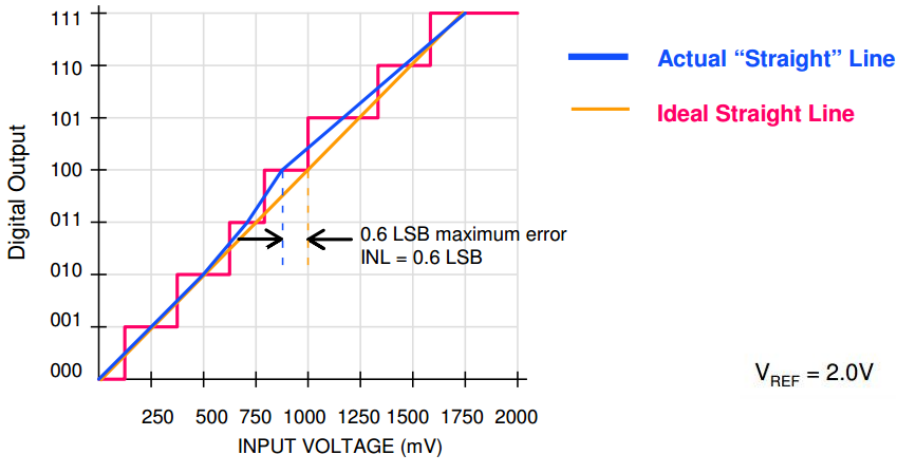


Figure 1.9: Integral non-linearity error [6]

1.3.2 Dynamic Performance Metrics

Analysis of dynamic metrics of ADC is based on frequency response of ADC. Therefore, dynamic parameters are determined using high frequency signals. A high frequency signal is fed at input of the ADC which provides quantized version of the same signal after reconversion of ADC digital output. Frequency spectrum of this reconstructed high-frequency signal obtained by taking Fast Fourier Transform (FFT) is analysed to determine dynamic parameters of the ADC under test. These dynamic parameters are explained below.

- **Signal to noise ratio (SNR)**

Ratio of signal power to noise power is called SNR. For an ADC of resolution *N*, maximum SNR (dB) that can be achieved is given as,

$$SNR_{max}(dB) = 6.02 \times N + 1.76$$

Apart from linearity errors, other factors mentioned in section 1.1.4 like clock jitter, thermal noise also contribute to degradation of SNR. Thus, SNR is the ratio of signal power to the sum of different noise powers. Since jitter increases due to increase in input signal frequency, and signal power decreases with decrease in input signal amplitude, thus SNR can be said to be input signal dependent. A high SNR indicates good ADC performance

- **Total harmonic distortion (THD)**

Spectrum of ADC output obtained from a non-ideal ADC contains harmonics at the frequencies which are multiples of signal frequency. Total harmonic distortion is defined as ratio of sum of power of all the harmonics to the signal power.

$$THD = \frac{\sum_{h=2}^{m} P(h)}{P(s)}$$

where *m* is the total number of harmonics present in spectrum, *P(h)* represents power of h^{th} harmonic, *P(s)* represents signal power or power of fundamental harmonic.

- **Spurious free dynamic range (SFDR)**

All the tones occurring at integer multiples of input frequency are called harmonics. Frequencies at non-integer multiples of input frequencies, where unwanted tones occur are called spurious frequencies. SFDR is the ratio of signal power to any spectral component except the DC component. The spectral component in denominator can be a tone occurring at harmonic frequency or a tone occurring at spurious frequency.

$$SFDR = \frac{P(s)}{\max\left(P(spectrum)\right)}$$

Here *P(s)* represents signal power, *P(spectrum)* represents power of other spectral components occurring at integer or non-integer multiples of signal frequency.

- **Signal to noise and distortion ratio (SNDR or SINAD)**

SNDR is a complete dynamic metric that covers effect of noise as well as distortion. SNDR is defined as ratio of signal power to sum of powers of all the harmonics (as in numerator of THD) and sum of power of noise components (as in denominator of SNR).

$$SNDR = \frac{P(s)}{\sum_{h=2}^{m} P(h) + P(n)}$$

Here *P(s)* represents signal power, *P(h)* represents power of h^{th} harmonic, *P(n)* represents noise power which further is sum of jitter, DNL, thermal noise powers.

- **Effective number of bits (ENOB)**

Due to non-idealities, there can be difference in ideal resolution of ADC and real resolution of ADC. According to the SNDR obtained for ADC under test, real resolution of ADC can be determined using below formula. This is called effective number of bits.

$$ENOB\ (bits) = \frac{SNDR - 1.76}{6.02}$$

1.4 THESIS ORGANIZATION

The thesis is organized into six chapters as follows:

Chapter1 describes the system architecture of flash ADC and Performance Metrics of flash ADC

Chapter2 reports literature survey of analog circuits, thus emphasizing on the complexity and performance limitations of analog circuits. The flash ADC presented in literature has also been discussed.

Chapter3 describes the conventional and the proposed comparators and its simulation results.

Chapter4 discusses the study of bubble error and implementation of Wallace tree encoder with and without pipelining.

Chapter5 describes the design and implementation of 4 bit flash ADC and its simulation results.

Chapter6 concludes the thesis and provides future scope.

CHAPTER 2
LITERATURE SURVEY

2.1 DETAILED STUDY OF COMPARATORS AND DIFFERENT ADCS

In this chapter, the research work that has been done in the field of flash ADC and comparators is reported. A brief review based on the study of papers is as follows:

Samad Sheikhaei et al. [7] proposed a flash ADC based on the low signaling swing for all sub-block including an encoder that is implemented in current-mode logic (CML). To increase the speed of ADC, 2-stage pipelining is used which enhance the performance by 40% compared to non-pipelining design. In this paper, bubble error is solved by the conversion of thermometer code to gray code than to binary code. Speed is improved by implementing the pipelined encoder with CML.

Pedro M. Figueiredo et. al. [8] explained latched comparators affected from a disruption called kickback noise. In flash ADC large number of the comparator are used according to the resolution, which will strike the reference voltages of the converter. The transition of voltage may be altered according to the kickback noise. Also, there is degradation in settling of the amplifiers in pipelined stage due to this phenomenon. This paper analyzes existing kickback noise reduction techniques and proposed some new techniques. The Most common technique is to use source follower or pre-amplifier. But it enhances power consumption and offset voltage. Some new techniques introduced are insert sampling switches before input differential pair, detect only when the comparator output is ready and reduce voltage changes on the drains of differential-pair etc.

Sunghyun Park et al. [9] implemented a 4bit non-interleaved flash ADC at a sampling rate of 4 GS/s. In this inductor are used to enhance the tracking and reset mode time constants and regeneration mode time constant. Also, inductor consumes less area than resistor which is used as a load resistance. Additional latches are used to enhance the overall voltage gain of the comparator. Minimum gate length transistors are used to increase the sampling frequency in a high-speed path. DAC trimming and comparator redundancy rectify both dynamics and static offset.

M.B. Guermaz et al. [10] proposed a clocked comparator based on switched-capacitors using a two-phase non-overlapping clock, for RF WLAN applications. The clocked comparator includes a positive feedback stage after preamplifier stage. Dynamic latches are

used to reduce the power consumption as compared to static latches. Also, this arrangement has buffer which will reduce gain and increase bandwidth. Buffers are also used as memorizer circuit and during pre-charge, it will erase the memory. Large MOSFET are added in pre-amplifier stage to decrease the offset voltage and gain is moderately increased. But it will further affect the conversion speed of comparator. Hence, a differential comparator configuration was employed to obtain an offset voltage of 77.3 mV, 0.8 mW of power consumption and a delay of 17.3 ns.

D. Meganathan et al. [11] proposed an approach for low-power pipelined ADC. To reduce the thermal noise and power consumption, a modified two-stage high gain operational transconductance amplifier having wide bandwidth is used in the sample-and-hold amplifier. The signal swing of the analog functional blocks is allowed to go above the supply voltage (1.8 V). Dynamic range is increased and due to the charge sharing kickback noise and dynamic power dissipation of comparator is reduced. Bottom plate sampling technique and bootstrap technique is in use to reduce nonlinearity error that causes SNDR of 58.72 at 2 MHz and 57.57 dB at a Nyquist frequency.

Hugues J. Achigui et al. [12] focused on comparator presented in this paper had a differential input stage and a flipped voltage follower cell that has high input common-mode range and therefore high swing. It has low input resistance, which is good for current-mode applications. It also allowed to the source of large currents, speed is improved by adding inverters to loop. It offered class AB which improves input resistance and push-pull digital inverter use class B concept for low voltage. At 1V supply voltage, it consumed 30μW power and Power-delay product (PDP) I/tp is 1μA/15ns.

Bing-Nan Fang and Jieh-Tsorng Wu [13] fabricated a 10-bit pipelined ADC using switching op-amps with short turn on time were used to reduce consumption of power. Digital background calibration scheme was used to correct the gain error. A biasing scheme was used in order to maintain the settling behavior of the op-amp against temperature variations. Simulation results proved that DNL and INL improve to +0.52/ 0.4 LSB and +0.99/ 1.65 LSB respectively.

Oktay Aytar [14] introduced a flash ADC in which the comparator based on Common gate differential pair, Cross-coupled NMOS, and push-pull inverters. The dynamic latch is used for the holding and transmission of the encoder output which is based on the PLA-ROM structure. Also, thermometer code decoder logic is implemented using TG (Transmission

Gate) based MUX circuit. This ADC is functioning on high speed and wide bandwidth applications.

Samaneh Babayan et al. [15] presented the dynamic and double tailed comparator in this paper. Clocked comparator are used in wide applications and due to the positive feedback in the regenerative latch, they can make a decision in a faster way. Due to some stacked MOS, the supply voltage is required a proper delay. Also, there is a single current path where transistor operated in triode region and current depend on the common-mode-input voltage. In conventional double-tailed comparator, intermediate nodes are charge and discharge during reset and phase respectively. In reset phase nodes are charge up to VDD and the set phase it will evaluate the logic according to the inputs, therefore, this will increase the power consumption. Also, mismatching in the controlling transistor will affect the output. Largely sized transistors have a high parasitic capacitance which will further affect the delay. This paper proposed a new double tailed comparator, which does not need high voltage and stacking too many MOSFET. In this small size, MOSFETS are added to the conventional double tail comparator which further reduces the delay of the circuit. Also, it will save the power compared to the conventional double-tail comparator. At 0.8V power supply, average power dissipation (at 500 MHz) =329μW, worst case delay =294ps/dec. & offset (σ_OS) of 7.8mV were observed.

M. Abdelhamid et al. [16] introduced a 12-bit pipeline Analog to Digital Converter (ADC) using 1.2V and 0.13μm CMOS technology. Embedded sample and hold technique is used in order to avoid the power-hungry sample-and-hold circuit. Op-amp's finite open loop gain and non-linearity are taken care of using low gain op-amps, and a foreground digital calibration scheme. The ADC power consumption is 65mW and reaches the highest SNDR of 68.5 dB and SFDR up to 80 dB.

I-Chyn Wey et al. [17] approached to upgrade the speed by making comparator based on dynamic CMOS comparator. The main focus is to reduce power, lessen transistor count and enhancing speed. The rearrangement and reordering of the transistor are main ideas behind this comparator. These can be used as 0/1 detector, equality, and the mutual comparator. Compared to conventional circuits, this approach result in 37.8% less number of transistor count and noise immunity is better. Delay is also less as there are only two comparators present in series which reduces pull down delay. The speed was increased by combating 'weak 0'problem in the PMOS of pull-down network. Instead, an NMOS combined with an

inverter was employed. It resulted in the low power-delay product (PDP). The proposed 64-bit comparator consumed 0.176 mW power and a delay of 0.38 ns was reported.

Ghil-Geun Oh et. al. [18] introduced the simplified ADC that exclude non-necessary building blocks such as a sample-and-hold amplifier (SHA), Reference ladder and level shifters. Now the main specification of ADC is low power due to its portability in various applications. It explains new clock generation circuit which will eliminate SHA that reduces the need for higher frequency clock. It explains the clock generator made up from the delay-locked loop which lessons the burden of the clock source. The conversion rate is 400MS/s with the supply voltage of 2V.

Skyler weaver et al. [19] demonstrated a stochastic flash ADC which is made up from the standard digital library and Verilog code. Analog circuits are very reactive to noise, non-linear and its layout is very difficult. Digital circuit gives rail to rail swing; automated synthesized and automatic layout is easily generated. This removes the reference ladder from the circuit and uses comparator input referred piecewise linear inverse Gaussian offset for the linear reference voltage generation. The comparator is made up of two cross-coupled 3-input NAND gates. This ADC requires no calibration, fabricated in 90nm CMOS technology. SNDR improves to 35.9dB at 210MS/s.

Xiaochen Yang and Jin Liu [20] presented a new partially active flash ADC. As the name suggests, in this only few comparators are powered ON which are close to input level; this will significantly reduce the power consumption. This 6b flash ADC are divided into two parts first part consist of 2-bit ADC and second part consist of 4 bit ADC which is made up of 4-different slices which are chosen according to 2-bit output. Moreover, to reduce kickback noise and enhances the bandwidth source-follower based bootstrap sample and hold circuit is used. Four phase clocks are used in this ADC to enhance the resolution.

Jong-In Kim et al. [21] fabricated 2GS/s 7-bit flash ADC using Cascade latch interpolation technique. Conventional interpolation technique using static comparator but in this only dynamic comparators are used to achieve 4 times interpolation factor. Cascaded latch interpolation is vulnerable to PVT (Process-Voltage-Temperature). This technique reduces the number of the comparator as two stages cascaded latch is used. The robustness and design issue are discussed in this paper.

Oktay Aytar et al. [22] presented 5-bit CMOS flash ADC uses the concept of differential pair comparator with a positive feedback loop to balance the output resistance and to boost up

the gain. Further common source PMOS amplifier is used to amplify the first stage and CMOS inverter gives higher gain. Encoder suggested is a combination of 1 to N decoder and fat tree encoder. 1 to N decoder is implemented using 2:1 MUX; therefore power consumption and active die area are decreased.

Amol Inamdar et al. [23] proposed multiple bit flash ADC with single bit periodic comparators. The comparator is based on three different techniques are differential quasi one junction SQUID (DQOS); (SDSW) symmetric differential SQUID wheel comparator and differential SQUID wheel comparator (DSW) with time interleaving clocks. Multiple beat frequencies are used for restoration of the signal. Also, clock network is optimized by EM simulations.

Gregor Tretter et al. [24] designed a 3-bit single core flash ADC which is fabricated in 28nm CMOS technology. Sample-and-hold circuit with a buffer at the output of that and bandwidth calculation is explained in this paper. Single ended reference differential comparator is used. The main idea is to reduce power, cost and enhances the conversion speed of ADC. By combining with time interleaving, ultra-high-speed ADC can be achieved.

D.R Oh, D.S. Jo et al. [25] describe a flash ADC which consists of Complementary Voltage-to-time converter (CVTC). Power consumption in VTC is high due to different charging and pre-charging operations in each clock. This letter proposed a CTCV structure to reduce the power consumption by making a single path for conversion and reset so clock frequency is decreased by 50%. Also, speed is increased except T/H circuit and overall power is enhanced by 27 %.

Hokyu Lee et al. [26] proposed time-interleaved SAR ADC which shares the resistor array of DAC. By using this technique power consumption is reduced by 69 % and inter-channel error is compensated by different calibration technique. It is fabricated in 65nm technology and consumes 22mW at the supply of 1.2V.

Zbigniew Jaworski [27] presented a new ADC design which contains resistive ladder, MCML based comparator with pipelined latches and an innovative 2-segment MCML encoder block. To boost the performance of design interpolation and averaging techniques are used. The number of preamplifiers is reducing using these techniques and a triple-cross connection is used to advance the averaging efficiency. Also, the encoder can bear the bubble error.

2.2 GAPS IN STUDY

A lot of research work has been done on flash ADC to optimize its performance in terms of its resolution, area, power etc. The architectures proposed in the recent years are studied and following gaps are identified:

- Full rail-to-rail input and output swings are difficult to achieve, with the trend of scaling, in analog circuits.
- Analog circuits are prone to process & temperature variations.
- Power dissipation in analog circuits is more as compared to digital circuits, because of continuous current flow. While in digital CMOS circuits, there is direct current path from supply voltage to ground at switching instants.
- The digital circuits amplify the signal to rails and also less sensitive to the noise, automated synthesis, and physical layout.
- With technology scaling the digital circuits achieve higher efficiency in terms of area, speed and power density, on the other hand, analog circuit face problem to keep the same pace.

Hence, it is required to re-design analog circuits through a novice approach which combat the shortcomings of analog design methodologies discussed in recent in literature. Thus, in the following chapters, digital-based designs of analog circuit have been presented.

CHAPTER 3
COMPARATOR DESIGN

3.1 INTRODUCTION TO COMPARATOR

Everything is going digitized in today's analog world. So there is a need to convert analog data into digital form. The main building block of all types of analog-to-digital (ADC) converters is comparator [28]. The important parameters for any comparator are power dissipation, offset, gain and speed. According to the performance parameter we will choose the architecture of comparator. The basic aim of comparator is that input voltage is compared with the reference voltage then comparator provides an output logic level 0 or 1 based on the comparison. A comparator provides an output signal that is equal to the difference of two input voltage signals and is independent to the common mode voltage. V_{IN} voltage is applied to the positive terminal and V_{REF} voltage is applied to the negative terminal. Output will be logic high or low according to the V_{IN} is greater or less than V_{REF}. Typically, comparators are difficult to map out. In static comparator offset is less but power consumption is high and speed is low. Contrary to static comparators, dynamic comparators have high input impedance, full-swing output, low power consumption and fast speed.

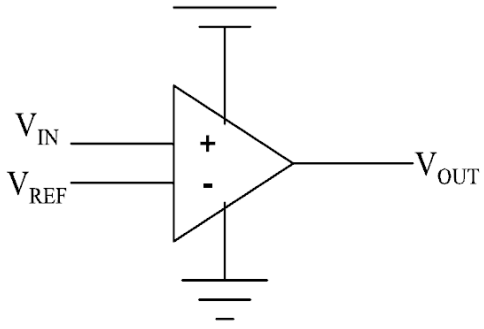


Figure 3.1 Block diagram of basic comparator

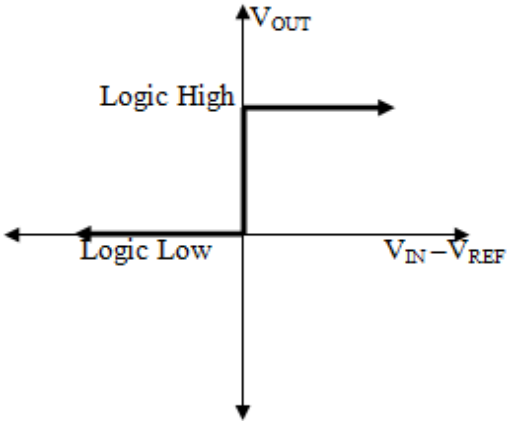


Figure 3.2 Transfer characteristics of ideal comparator

Mathematically,

If $V_{IN} > V_{REF}$, V_{OUT} = logic high

If $V_{IN} < V_{REF}$, V_{OUT} = logic low

3.1.1 Comparator characteristics

The performance of the comparator is defined in terms of static and dynamic characteristics [28]. Static characteristics comprises of gain, input offset voltage, resolution and noise and Dynamic characteristics mainly consist of propagation delay and speed. Power dissipation is also important design specification for a comparator.

- **Offset Calculation**

The input static offset of the comparator arise from conflict in same devices. Therefore the comparator may give the random change in output *i.e*. the comparator output may be reversed. The output switches from one logic level to another as soon as the inputs

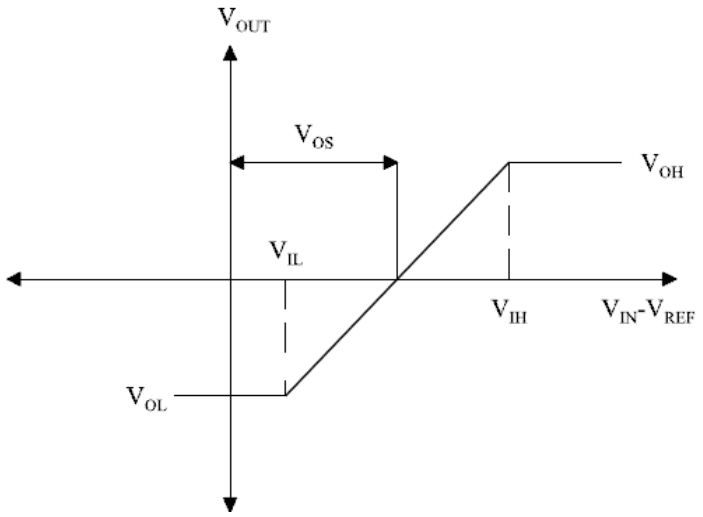


Figure 3.3 Transfer curve of a comparator including input offset voltage

difference becomes zero. If the output doesn't switch until the inputs difference reaches a value V_{os}, then this difference is termed as the offset voltage as shown in Figure 3.3:

This offset voltage poses a problem for circuit designers as it varies randomly from circuit to circuit, and is hard to predict.

- **Resolution**

The smallest difference at the input voltage which is identified by a comparator that give a logic 1 or 0 is called resolution. The restricting factor that affect the resolution are noise and input offset voltage. The minimum resolution that an A/D can have is V_{LSB} . The comparator should be able to determine V_{LSB} that is $1/2^N$ for N bit ADC .

- **Gain**

Gain is defined as output is changing with the change in input ΔV, where ΔV approaches to zero. The voltage gain of comparator can be written as

$$Gain = A_v = lim_{\Delta V \to 0} \frac{V_{OH} - V_{OL}}{\Delta V} \quad (3.1)$$

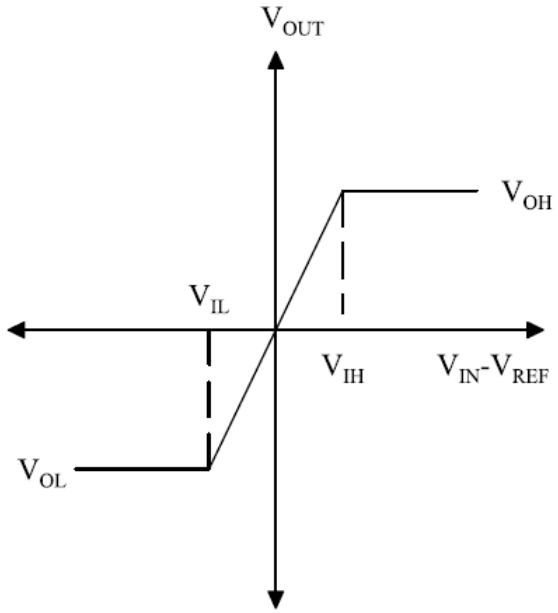


Figure 3.4 Transfer curve of a comparator with finite gain

Fig. 3.4 shows the practical dc characteristic curve of a comparator. Thus,

$$A_v = \frac{V_{OH} - V_{OL}}{V_{IH} - V_{IL}} \quad (3.2)$$

where V_{IH} and V_{IL} represent the input voltage difference needed to just saturate the output at its upper and lower limit, respectively. Also, ICMR for a comparator is the range of input common mode voltage over which the comparator functions, perfectly.

- **Propagation delay**

The comparator basically compares two input signal and changes (trip) the output when one level exceeds other. But the output can't be changed at the same instance; there is some delay called propagation delay tells how fast the comparator changes its output according to the input. Delay is there because signal propagates through the internal circuitry. It defines the speed of the comparator. It also deteriorates ADC performance. Propagation delay time is the average time of both rising edge and failing edge.

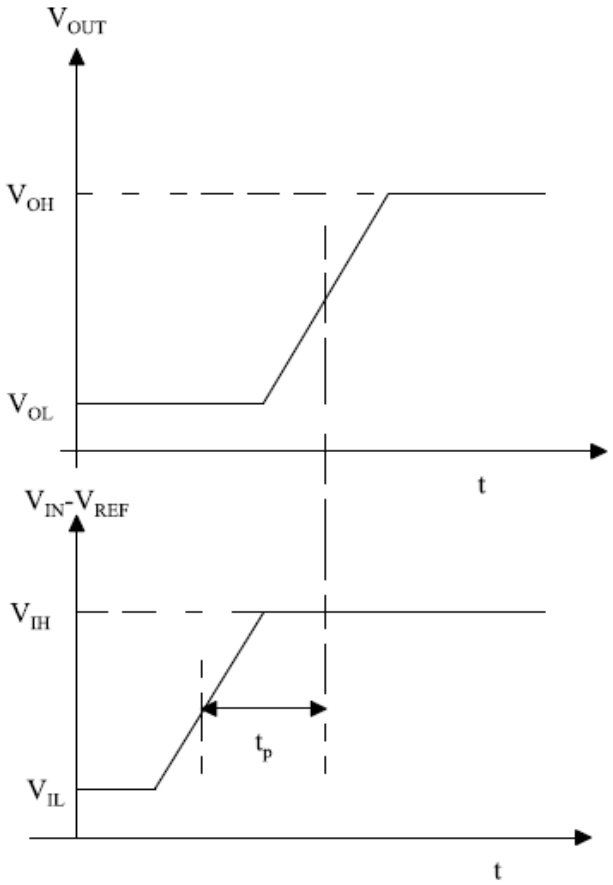


Figure 3.5 Propagation delay time of comparator

The rising propagation delay is given by 50% of rising edge of the input and 50 % of the transition edge of the output signal level and falling propagation delay is given by 50% of falling edge of the input and 50 % of the transition edge of the output signal level. The propagation delay (t_p) is given by

$$T_{propagation\ delay} = t_p = \frac{T_{rise}+T_{fall}}{2} \tag{3.3}$$

Where T_{rise} is the rising time and T_{fall} is the falling time. In clocked circuit i.e. comparator's propagation delay can be calculated between the 50 % transition points of the clock signal & output signal i.e. difference of high level and low level (V_{OH}-V_{OL}).

- **Power dissipation**

Power dissipation is a crucial design specification for the comparator. When Analog CMOS design circuits are compared with digital CMOS design circuits, Analog CMOS circuit will consume more power.

Total power dissipated in a digitally designed CMOS circuits is specified by the sum of dynamic (or switching) power dissipation (P_{dyn}), short-circuit power dissipation (P_{sh}) and leakage power dissipation (P_{leak}).

$$P_{total} = P_{dyn} + P_{sh} + P_{leak} \tag{3.4}$$

P_{dyn} is the power dissipated because of switching which transpire when a node capacitance is charged or discharged, P_{sh} is the power dissipated due to the crowbar current (direct path current or short circuit current) that flows from supply voltage vdd to lower voltage i.e. ground potential and P_{leak} is the power dissipated, even when there is no switching. It plays an important factor in ultra-deep sub-micron technologies. But, it can be easily neglected in the present case of 180 nm technology. Thus, power dissipation, in our case, is mainly due to P_{dyn} and P_{sh}.

3.2 BASIC OF ANALOG DIFFERENTIAL CIRCUIT

An analog differential circuit is quite a common circuit, which is being used in the first stage of opamp generally.

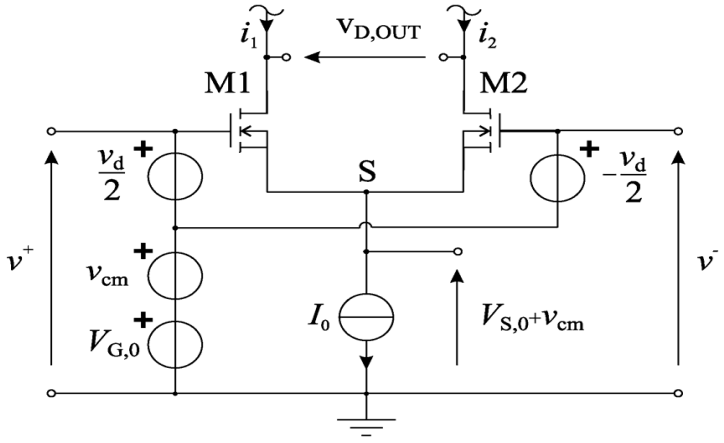


Figure 3.6. A CMOS differential pair [28]

An analog differential circuit can be designed using two identical source-coupled MOSFETs M1 and M2. A constant current source is used to bias both the transistors in the saturation region, as depicted in Figure. 1. The output currents i_1 and i_2 flowing through M1 and M2, respectively, are independent of the CM input voltage.

A CMOS DP, however, suffers from various limitations like ICMR, minimum supply voltage, output voltage swing, power dissipation [29-31]. Thus, digital-based design of analog comparator is presented [28].

3.3 EXISTING ANALOG COMPARATOR

The existing analog comparator is shown in Figure 3.7. The differential pair (DP) made from NMOS (M2-M3) which is driven by transistor M4 producing a tail current. PMOS cross couple transistor M0-M1 are connected with DP forms a positive feedback loop to advance the voltage gain of DP and to balance the output resistance. M9-M10 form a current mirror in which reference current is supplied by M7-M5. The common source PMOS amplifier M8 is used for the amplification of Ist stage Inverter connected at the output gives the higher gain

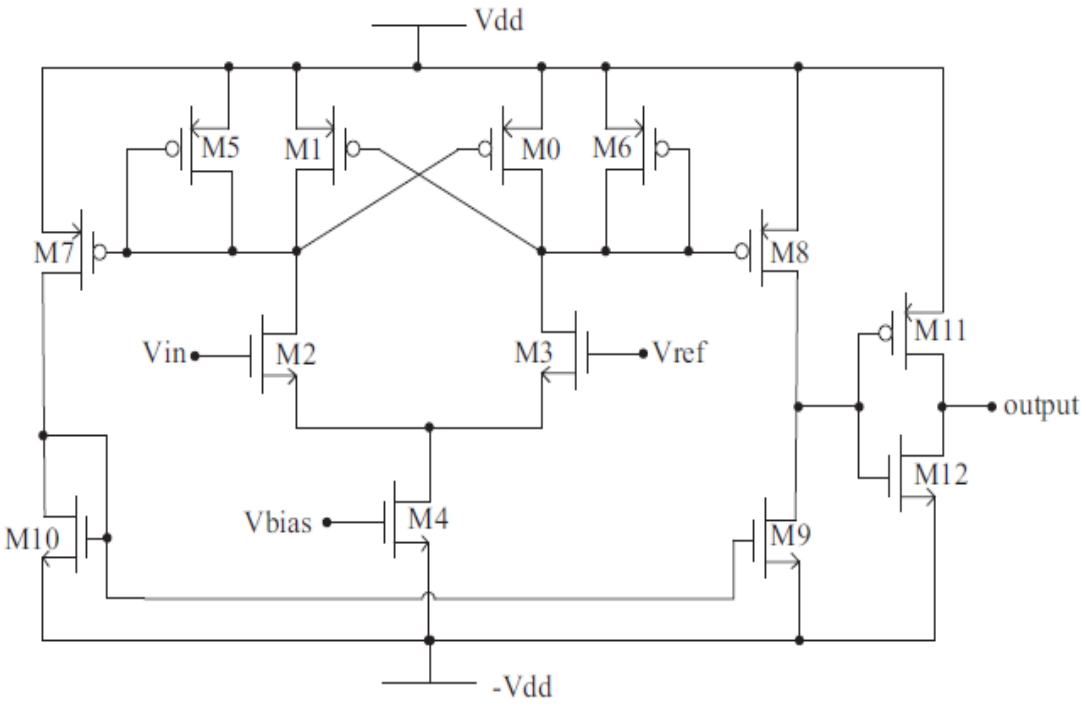


Figure 3.7 Existing Analog comparator schematic [14]

The DC transfer characteristics of existing comparator in which input voltage is varied from 0V to 1.8V and reference voltage is 0.9V is shown in Figure 3.8. Offset voltage of this comparator is obtained i.e. 45mV.

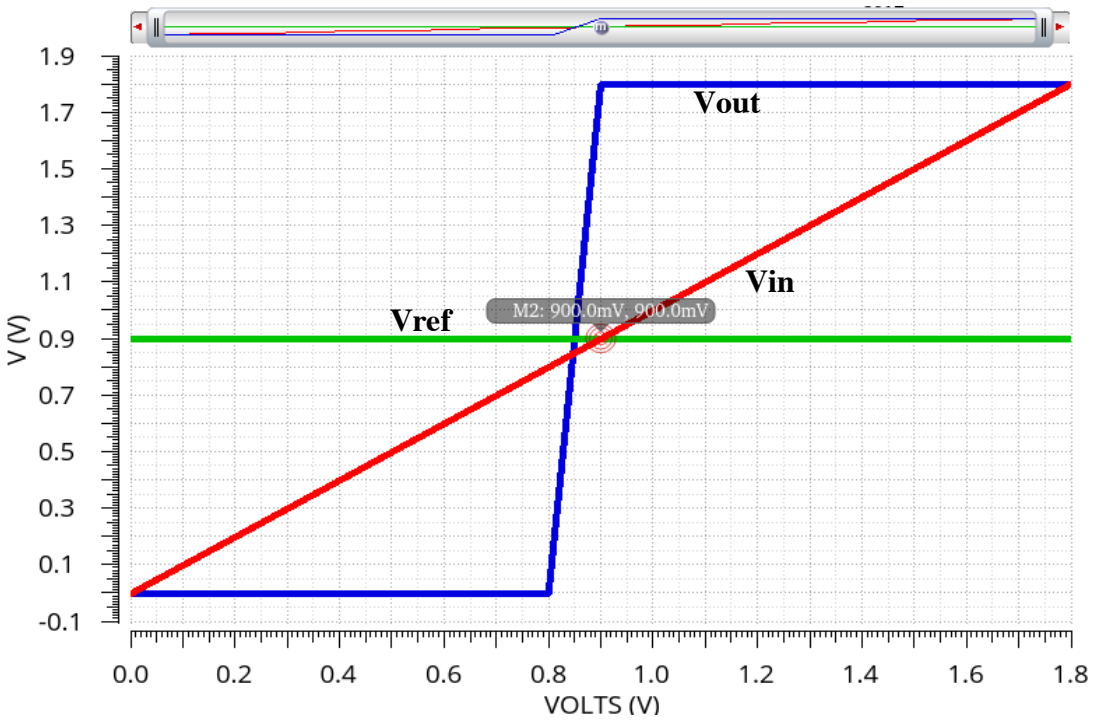


Figure 3.8 Offset voltage of the existing comparator

The transient response of existing comparator is shown in Figure 3.9. It is seen that input is compared with the reference voltage accordingly output voltage is obtained.

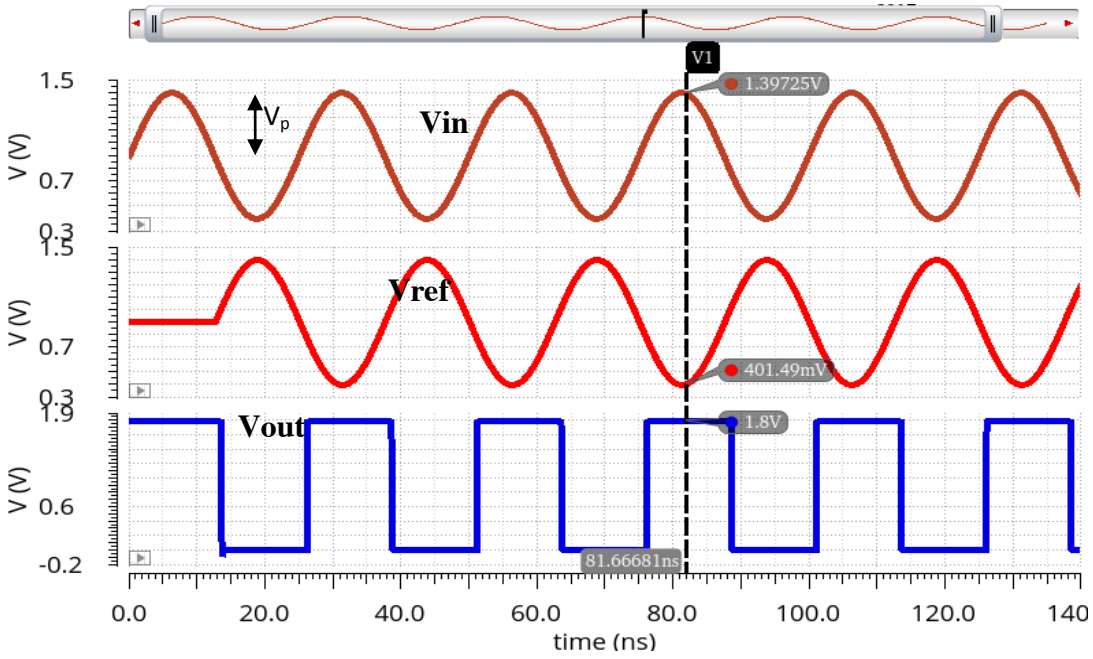


Figure 3.9 Transient response showing voltages at different nodes in the circuit

The delay is calculated for the different values of input voltage amplitude Vp and its plot is shown in Figure 3.10. Minimum delay with change in Vp is 0.87ns and power dissipation of this analog comparator is 411.8µW.

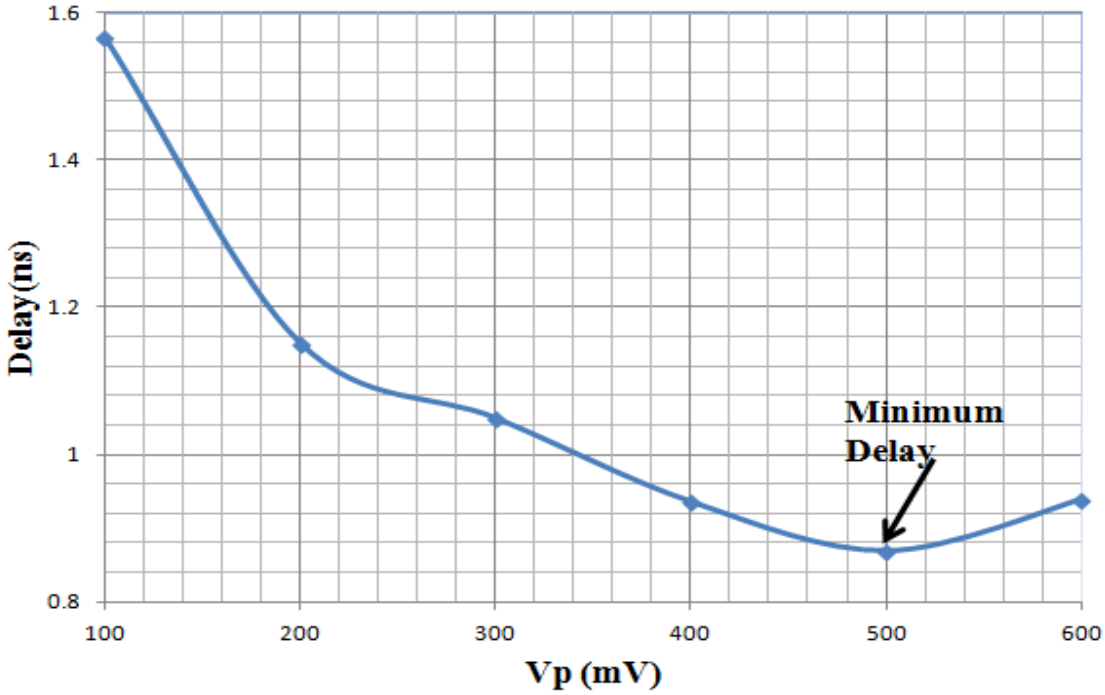


Figure 3.10 Variation of propagation delay with change in input voltage amplitude Vp

3.4 DIGITAL GATE BASED COMPARATOR IMPLEMENTED USING VERILOG

A Fully Differential Voltage Comparator schematic is shown in Fig 3.11. It is based on the concept of digital-based differential circuit [28] and is composed of standard CMOS based Inverter, NAND and NOR gates. This comparator is designed, implemented and simulated in Cadence Virtuoso ADE-L using SCL 180nm CMOS technology. It has summer logic comprising of four resistors of equal value. Summer provides the average of the external inputs and the feedback signal V_f, The capacitor (C_f) in the feedback block has been implemented by MOSCAP (MOSFET capacitor) [32, 33]. MOSCAPs require less area, lesser number of fabrication mask layers and can be implemented in standard digital CMOS technology and offers more capacitance density as compared to MIMCAP (metal insulator metal capacitor), MOMCAP (metal oxide metal capacitor), PIPCAP (poly insulator poly capacitor) etc.

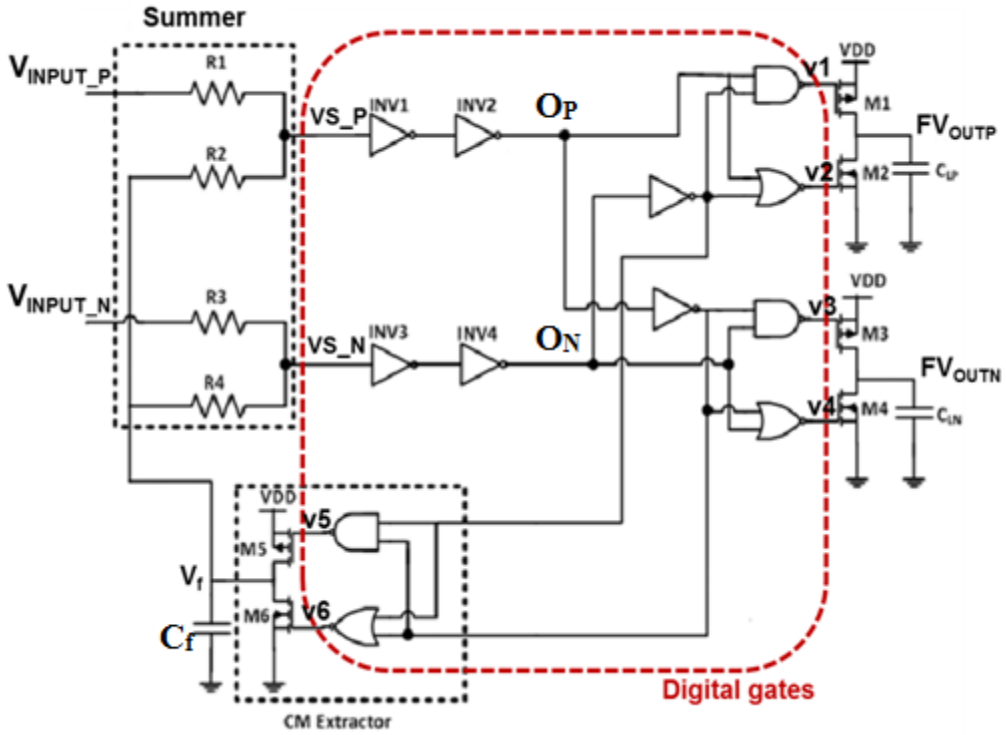


Figure 3.11 A digital gate based voltage comparator implemented using verilog

The digital gates are the major part of this circuit which are synthesized using verilog code. Complete internal working is further explained. An inverter provides a logic high output when a signal greater than threshold voltage (V_{th}) is applied at its input & a logic low output when input voltage less than V_{th} is applied. The voltage at which input changes the output is called as switching or trip voltage. Thus, if two inverters with different input are taken and

input voltage less than V_{th} is applied at one inverter and voltage greater than V_{th} is applied at the input of other inverter, then differential output will be 1 or 0. But, in case the input voltages applied at both the inverters are same i.e. both voltages are greater than V_{th} or less than V_{th}, the circuit becomes non-responsive to the differential mode component and hence, the output will be uncertain.

The solution to this impasse situation is a common mode negative feedback signal (V_f), which is generated with the help of feedback block. V_f gets added up with both the input voltages V_{INPUT_N} & V_{INPUT_P} with the help of summer. Summer comprises of four resistors. Summer provides the average of the feedback signal (V_f) and the external inputs, and such that the outputs of summer are $VS\_P = \frac{V_{INPUT\_P}+V_f}{2}$ and $VS\_N = \frac{V_{INPUT\_N}+V_f}{2}$. All inverters used in this circuit are symmetric such that their switching threshold voltage $(V_{th}) = \frac{V_{DD}}{2}$. These voltages (VS_P and VS_N) are passed from inverters to get O_P and O_N, which are the digital inputs of the circuit. Thus, O_P and O_N are compared and the correct output is obtained, eventually. The feedback block comprises of M5-M6 transistors, loaded by a capacitor C_f.

Thus, when the input voltages, V_{INPUT_P} and V_{INPUT_N} are less than V_{th}, then M5 transistor turns ON to increase V_f. And, when both V_{INPUT_P} and V_{INPUT_N} are greater than V_{th}, then M6 transistor is turned ON to decrease V_f. This is done to obtain V_f in such a range that after adding up, it leads to distinguishable values of the digital inputs of the circuit. In these two cases, output transistors are OFF, until comparable digital inputs are obtained through feedback mechanism. And as soon as valid digital inputs are obtained, correct outputs are provided by the output stage. In the case of different input voltages, V_f signal is not required, hence feedback block is in off condition and the transistors present at the output stage (M1-M4) are ON accordingly, to provide correct outputs.

Considering the case of differential inputs, let V_{INPUT_P} be higher than V_{INPUT_N} once VS_N and VS_P cross the V_{th} of the inverters INV1-INV4, respectively, O_P rises to logic '1' and O_P decreases to logic '0'. Thus, M1 transistor turns ON and M2 transistor turns OFF. Therefore, FV_{OUTP} becomes '1' and FV_{OUTN} becomes '0'. Similarly, when V_{INPUT_P} decreases and V_{INPUT_N} rises, FV_{OUTP} becomes '0' and FV_{OUTN} becomes '1'.

The Figure 3.12(a) and (b) show the verilog code for digital comparator and synthesized design of comparator.

Verilog Code

```
module top_mod (v1,v2,v3,
v4,v5,v6,VS_P,VS_N);
   output v1,v2,v3,v4,v5,v6;
   input VS_P,VS_N;
   wire OP,ON,x,y,a1,a2;
      inv21 inv_1(a1,VS_P);
      inv21 inv_2(a2,VS_N);
      inv21 inv_3(OP,a1);
      inv21 inv_4(ON,a2);
      inv21 inv_5(x, ON);
      inv21 inv_6(y, OP);
      nand21 nand2_1(v1,OP,x);
      nand21 nand2_2(v3,ON,y);
      nand21 nand2_3(v5,x,y);
nor21 nor2_1(v2,OP,x);
      nor21 nor2_2(v4,ON,y);
      nor21 nor2_3(v6,x,y);
    endmodule
```

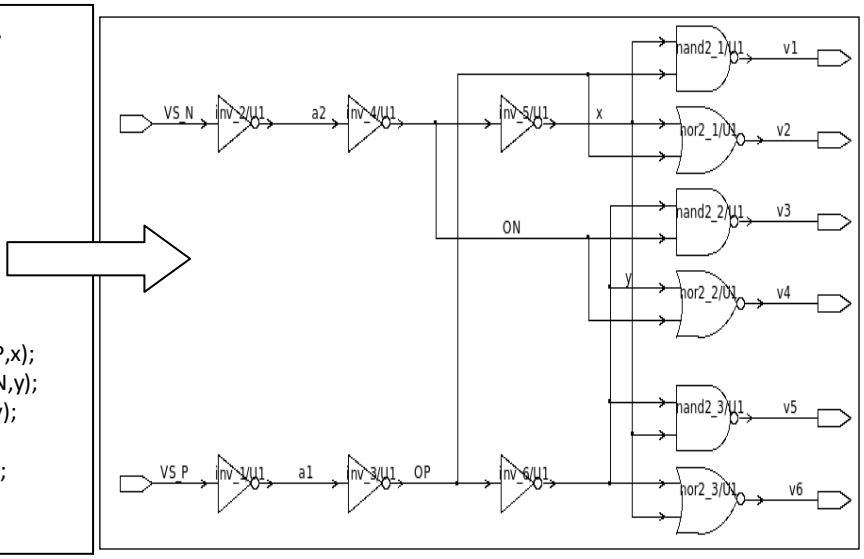


Figure 3.12 (a) Verilog code for digital comparator. (b) Synthesized design of comparator

As compared to [28], the two output signals FV_{OUTP}& FV_{OUTN} have been derived in the proposed circuit. As fully differential circuits have certain benefits over single-ended circuits like error subtraction, large output swings, rejection of common-mode noise, a high closed-loop speed, etc [34]. Usually all this is achieved at the cost of large power requirements [8, 15]. But as the proposed comparator circuit is synthesized using digital gates so the power required is less. Another advantage of the proposed circuit is the use of universal NAND-NOR gates in the design.

3.4.1 Input offset voltage

The performance of digital based differential voltage comparator in terms of input voltage based on the delay of the buffers, mismatch in resistance and mismatch in the threshold voltages is shown in Figure 3.11. As there is voltage divider at input side so process variation in resistive network does not affect the voltages at VS_P and VS_N. So summing network does not affect the offset voltage. Both inverting and non inverting inputs are connected together. Therefore, flow of current in the resistive network and at the internal nodes VS_P and VS_N are not same despite of any resistance value. Inverters (INV1, INV2, INV3, INV4) are designed to achieve rail to rail swing. Inverters provide proper amplification to the signal. The main component of offset in this circuit are mismatch in rising(falling) time delay t_{d_rise1}, t_{d_rise2} of digital buffer which may increase the offset voltage $V_{offset1} = (Io/Co)dV$ and

mismatch in threshold voltages $V_{offset2} = Vth1 - Vth2 = dV$. Total offset voltage is given below [28].

$$V_{OFFSET} = \frac{Io}{Co} dV + Vth1 - Vth2 \tag{3.5}$$

The simulation result of differential voltage comparator with verilog code is shown in figure 3.13. It is seen that the delay between input and output is 2.96ns.

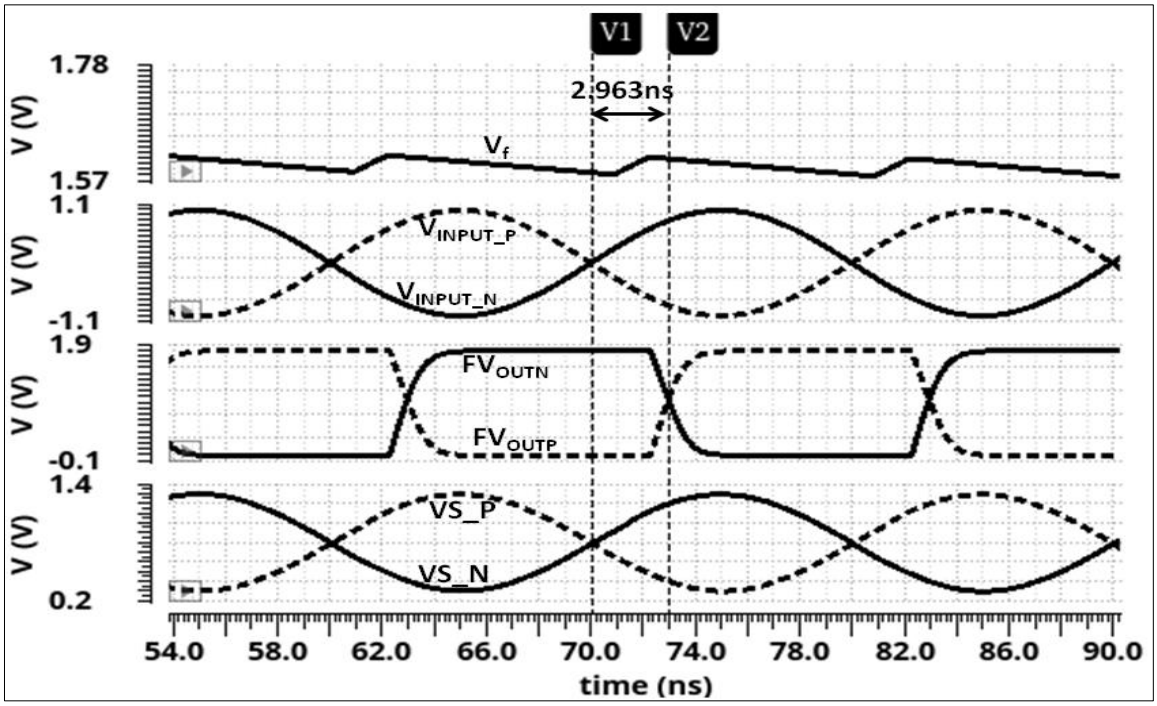


Figure 3.13 Simulation result of differential voltage comparator with verilog code

The Monte Carlo Simulations for 200 runs is performed and is shown in Figure 3.14. It is observed that the mean value of the offset voltage is 4.97 mV.

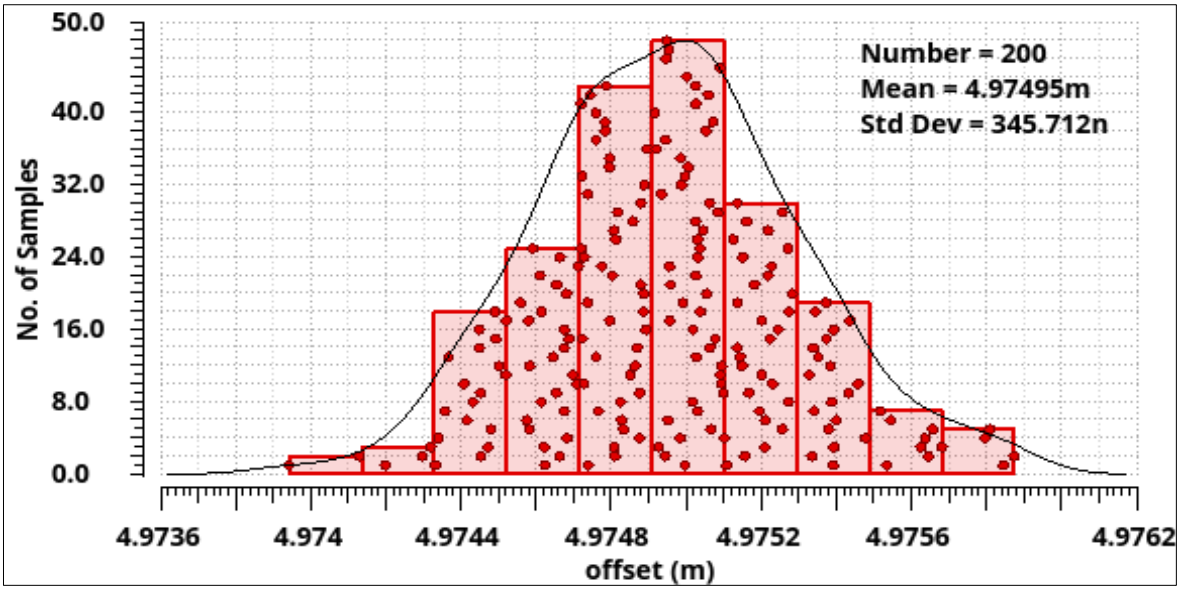


Figure 3.14 Monte Carlo Simulations for 200 runs

3.4.2 DELAY ANALYSIS OF COMPARATOR

The critical path from input to output can be observed in the Figure 3.11 from V_{INPUT_P} to FV_{OUTN} and V_{INPUT_N} to FV_{OUTP} node or it can also be called as worst case delay. It includes the delay elements as follows: delay from input V_{INPUT_P} to VS_P node and is due to $(R1||R2)C_f$ value offered by resistor where C_f is parasitic capacitance at V_f node, which is mostly due to the capacitance present at the input side of inverter INV1. Next, delays are from VS_P to OP node and from OP node to final output. Hence, the total delays from V_{INPUT_P} to FV_{OUTN} is approximately 2.963ns which is shown in Figure 3.13 at SS corner. A similar propagation delay analysis can be done for the path from V_{INPUT_N} to FV_{OUTP}.

3.5 MOSFET BASED PROPOSED COMPARATOR IMPLEMENTED WITH VERILOG

In the proposed circuit shown in Figure 3.11 resistive network is replaced by the transmission gate. The schematic of MOSFET based comparator with verilog code is shown in Figure 3.15. also the capacitor is replaced by the MOSCAP.

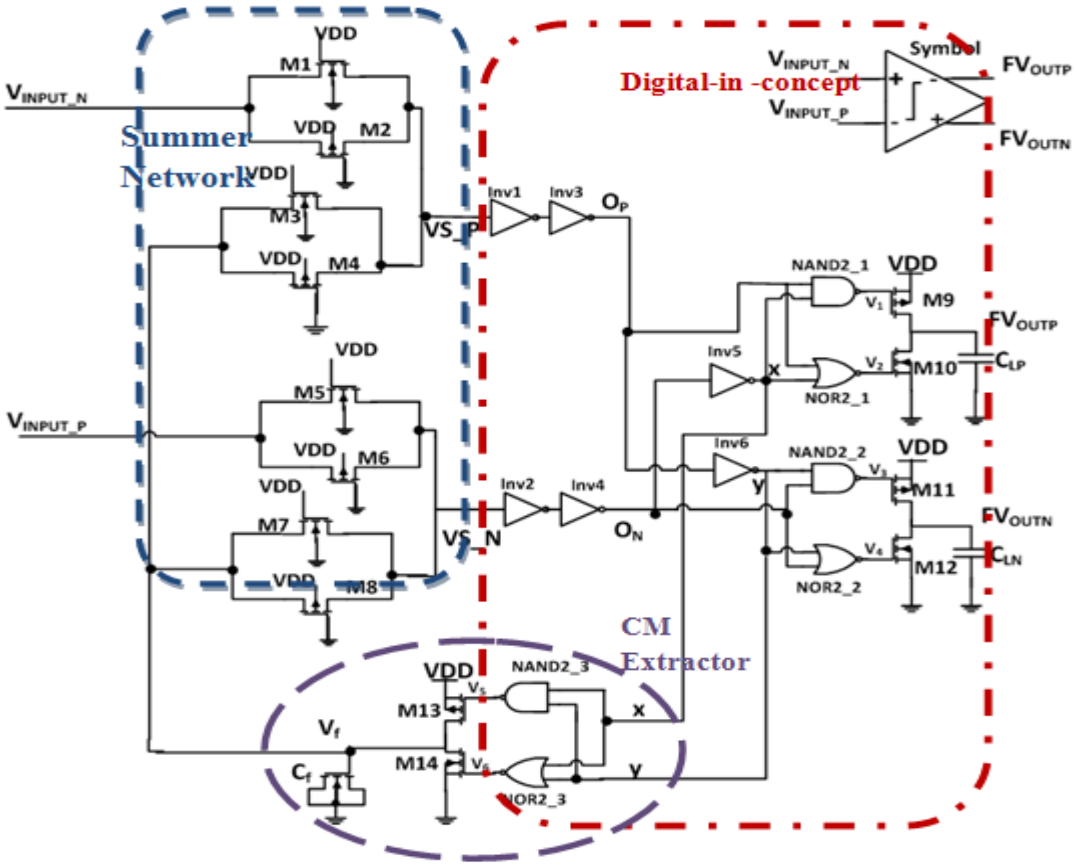


Figure 3.15 MOSFET based proposed comparator implemented with verilog

The transient analysis and DC transfer characteristics of MOSFET based differential voltage comparator with verilog code is shown in Figure 3.16 and 3.17. It is seen that delay is 2.46ns.

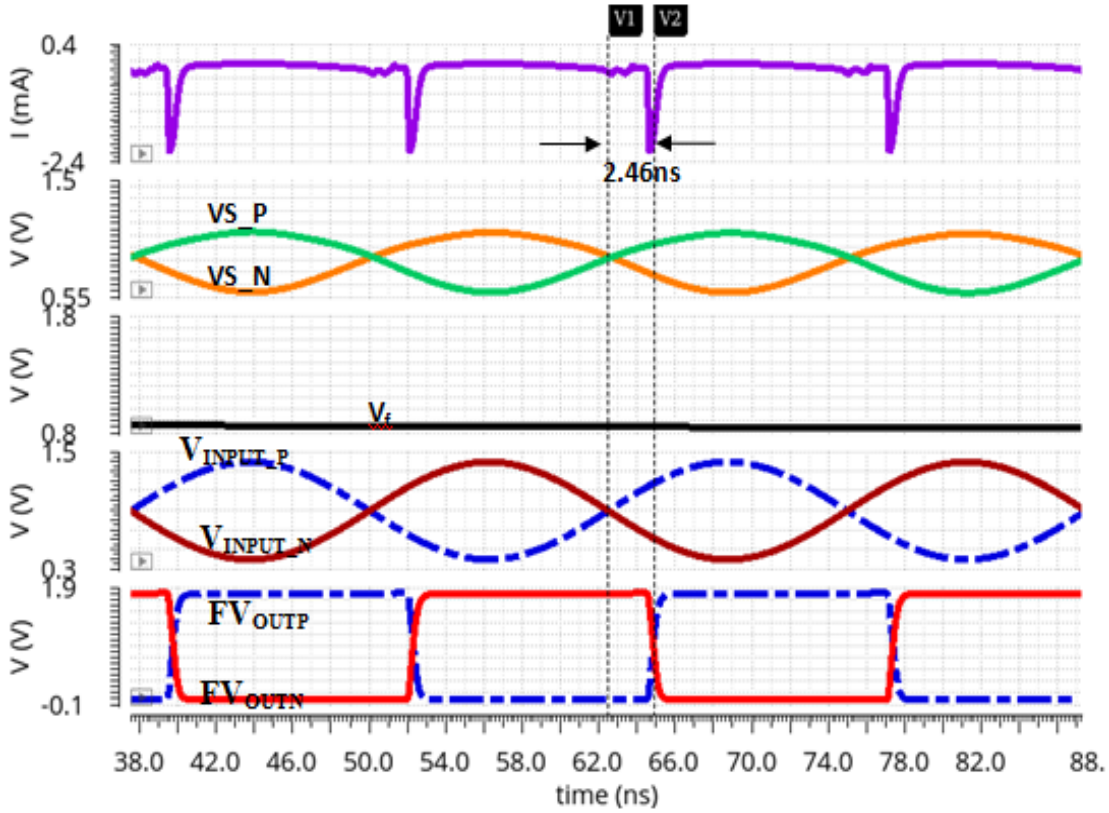


Figure 3.16 Simulation result of MOSFET based differential voltage comparator with verilog code

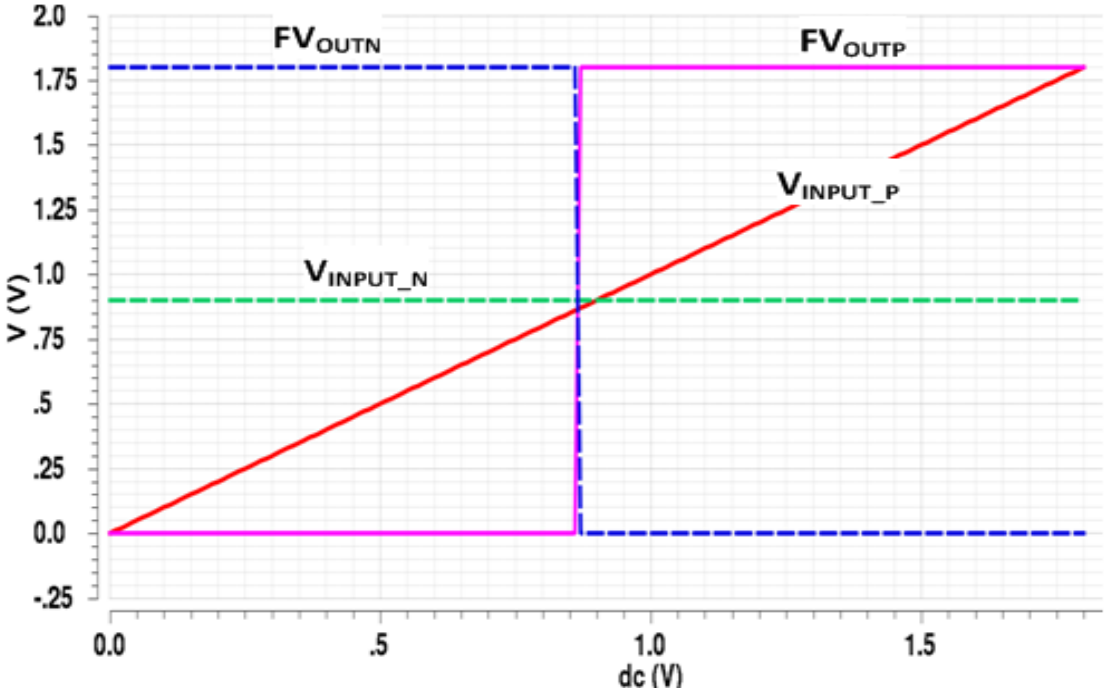


Figure 3.17 DC analysis of transmission-gate based comparator

From DC analysis of the proposed comparator as shown in Figure 3.18, an offset voltage was measured as 4.83 mV. Though, output voltage is supposed to reach $0.5V_{DD}$ at the DC bias applied at the input. But, instead of switching at this $0.5V_{DD}$, Output switched at some other voltage, this difference is referred to be the offset voltage. Here too, 0.9 V was applied as DC bias to the input. But, instead of switching at this 0.9 V, FV_{OUTP} switched at 904.833 mV. This leads to an offset voltage of 4.833 mV. A digital-in-concept implementation technique has been presented to design efficient fully differential voltage comparators. This is highly cost effective as digital-domain design is less tedious and time-consuming as compared to pure analog implementations.

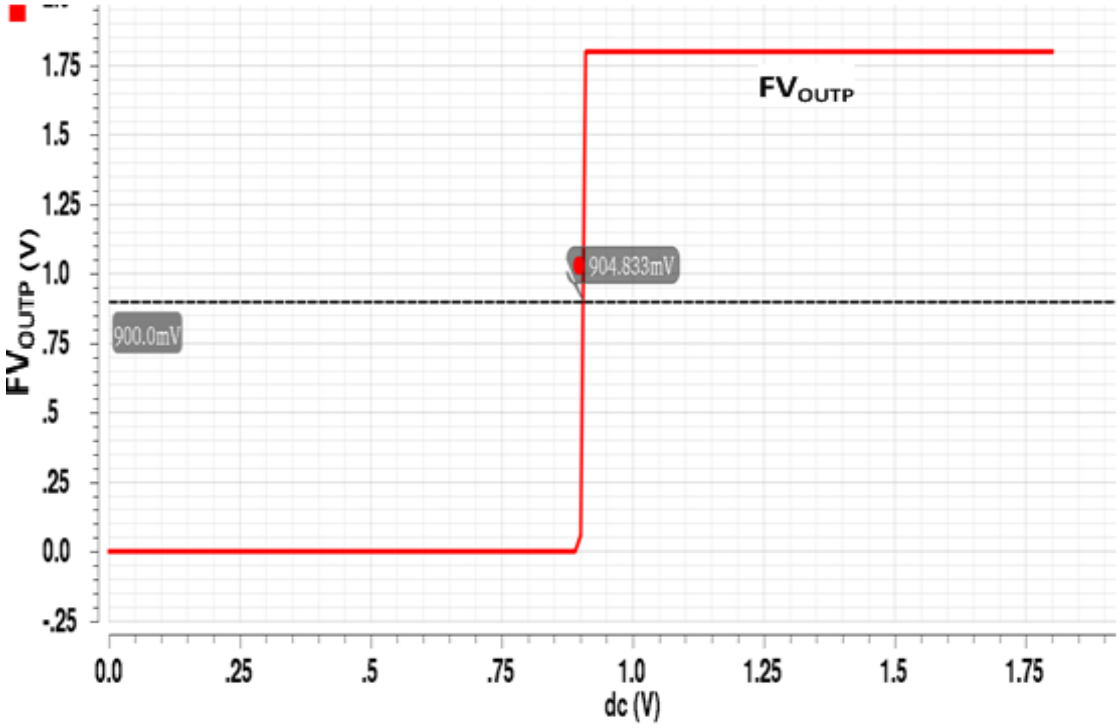


Figure 3.18 Offset voltage of transmission-gate based comparator

3.6 MOS BASED PROPOSED COMPARATOR WITH PIPELINING CONCEPT IMPLEMENTED BY USING VERILOG

An efficient fully differential voltage comparator with low power, low offset voltage and less delay is designed. This comparator based on digital NAND and NOR gates with some transmission gate transistor. This concept is used for the reduction of power dissipation and offset voltage. The schematic of this Synthesized Proposed pipelined comparator with verilog is shown in Figure 3.19.

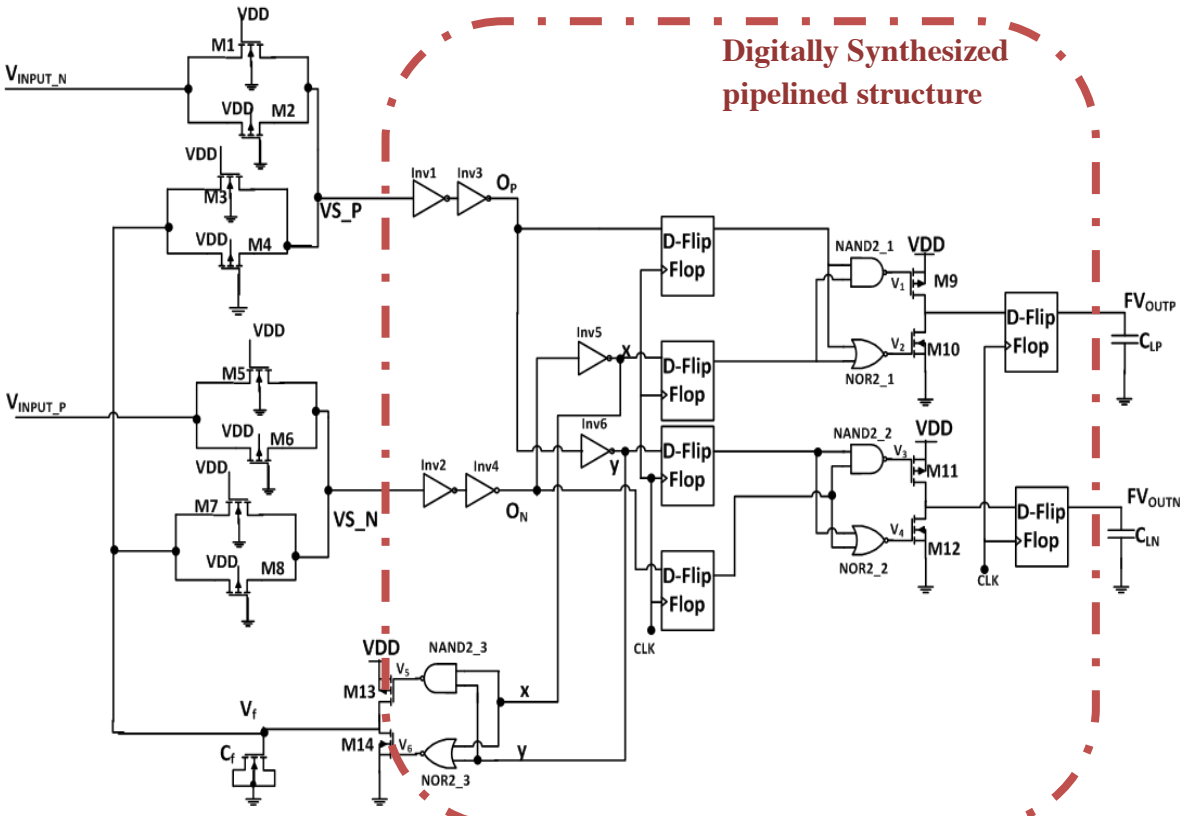


Figure 3.19 Synthesized Proposed pipelined comparator with verilog code except transmission gate

The transient analysis of MOSFET based Synthesized Proposed pipelined comparator with verilog code is shown in Figure 3.20. It is seen that delay is 2.2ns.

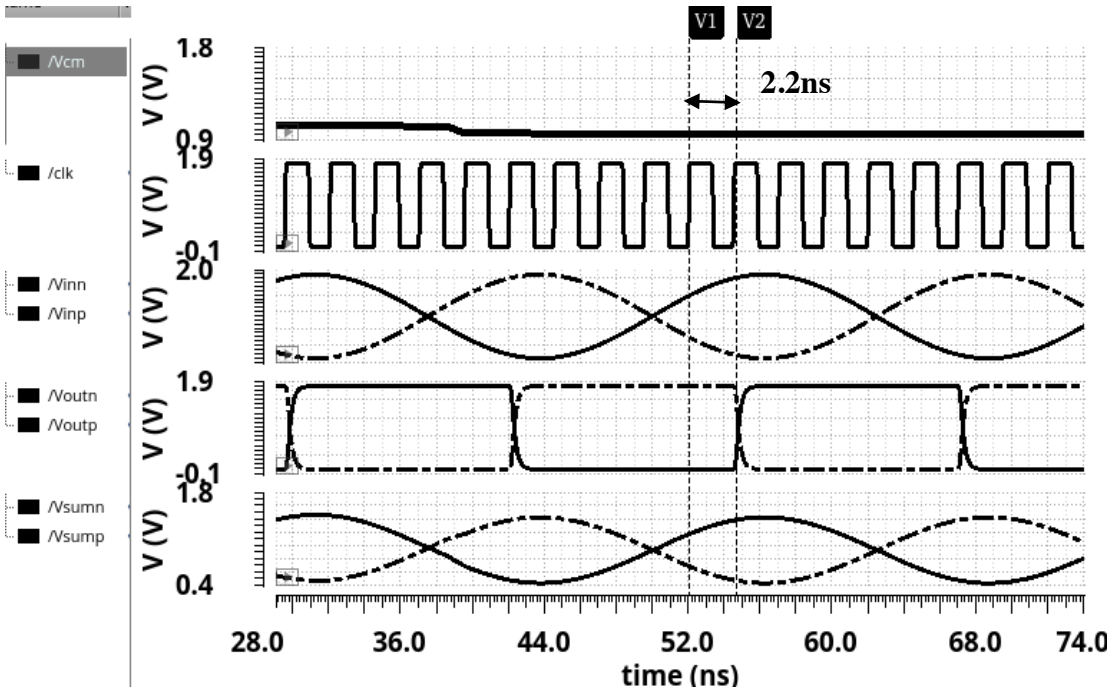


Figure 3.20 Simulation result of Synthesized Proposed pipelined comparator with verilog code

Table 3.1 shows that the proposed comparators have better values of all the parameters. With the load capacitance of 1pF, the comparator was simulated. In analog comparator, with the scaling of supply voltage performance degrades. But this digital based comparator adds good trade-off between power dissipation and delay, with the scaling technology these digital comparators further design for low power application. The main advantage of this proposed comparator is less time to market.

Table 3.1 Comparison of Comparator characteristics

Parameter	[39]	[10]	[15]	[40]	[14]	This work (1)	This work (2)	This work (3)
Design Methodology	Analog	Switched capacitor used in clocked compara-tor	Dynamic dual tail compara-tor	Current mode	Analog	Fully Digital	Fully Digital with verilog code	Pipelined Fully Digital with verilog code
CMOS Technology (µm)	0.5	0.8	0.18	0.18	0.18	0.18	0.18	0.18
Supply Voltage (V)	1	5	1.2	1.8	1.8	1.8	1.8	1.8
Offset Voltage (mV)	-	77.3	7.8	-	45m	4.9	4.83	4.83
Average power Dissipation (µW)	-	800	329	158	418	221.4	150.01	180.1
Delay	4µs	17.3ns	550ps	0.4ns	870ps	2.96ns	2.46ns	2.2ns

CHAPTER 4
ENCODER DESIGN FOR FLASH ADC

The flash ADC is the fastest method to convert analog information to digital information. It is suitable for the applications where high speed and low resolution is required like magnetic read channel applications, optical data recording and digital communication system. In flash ADC output of comparator which is in the form of thermometer code is fed to encoder. Under good condition, the output of the comparators for which input is below reference level is 1 and for comparators when input is more than reference level output is 0. So, in this thermometer code can be effortlessly changed into binary code. There are different ways to convert the thermometer code to binary code. Programmable logic array (PLA), MUX based design, Fat tree encoder, Read-Only-Memory (ROM) and Wallace tree encoder are generally used for encoder. The ROM based encoder is slow in speed and consumes large power because of its two stages. First stage include array of NAND gate and second stage choose the row of encoder accordingly. Fat tree encoder has high speed and less power dissipation compared to ROM encoder. Wallace tree encoder is the simple method for the conversion of thermometer code to binary. The main advantage of this encoder is that all the inputs in the encoder are traversing through same number of full adders. So, the propagation delay from input to output is same. By applying the pipelined stages in between different stages of encoder, speed of operation can be increased. Also, the bubble error i.e. sparkle problem for flash ADC mainly occur in these existing encoders. For very high speed input signal, small timing difference between the response time of comparators causes 1 above the 0 at the output which will lead to bubble error in thermometer code. It resembles with mercury in

Table 4.1 Bubble Errors in ADC Thermometer code

First Order	Second Order	Third Order	Correct Logic
0	0	0	0
0	0	1	0
0	1	***0***	0
1	***0***	***0***	0
0	***0***	***0***	1
1	1	1	1
1	1	1	1
1	1	1	1

thermometer. The following encoder explained in section 4.1 and 4.2 can solve the problem of higher ordered bubble error. Different logics are there to solve the bubble error like conversion of thermometer code to 1-to-N using AND gate but it can only solve the first order bubble error. So, Wallace tree encoder can be used for this flash ADC because it will solve the bubble error of higher orders also. Table 4.1 explains the bubble error of three orders referring the number of 0's between two 1's.

4.1 IMPLEMENTATION OF ENCODER USING WALLACE TREE

One of the bottlenecks in high speed flash analog-to-digital design is the conversion of the thermometer code to binary code. The thermometer code can be converted to binary code using Wallace tree encoder which consists of full adder. It is also called as ones counter because it will count number of one's [35, 36] and according to that it will give the binary output. One more stage is added to the design for every 1-bit increase at the output. The first stage counts the numbers of ones at the entry and gives the output in 2-bit binary code. The second stage adds 2-bit words of adjacent cells to give 3-bit output and this will continue till final binary code is available. The encoder structure based on this technique is very good for removing bubble error.

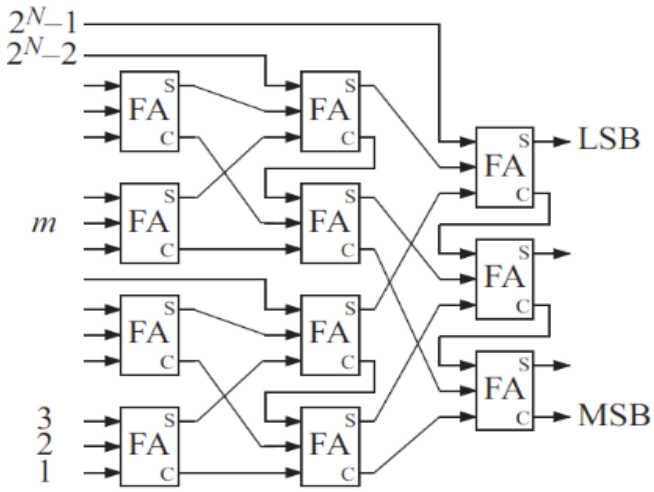


Figure 4.1 Block structure of Wallace tree

As Wallace tree counts number of ones so it will remove bubble error of any order [37]. Power dissipation of Wallace tree encoder is less than ROM based encoder. Other advantages of this encoder are that all the inputs traverse through the equal number of full adders so propagation delay is same. Also, it gives good result for any resolution but with less speed. This circuit is implemented with verilog code and is digitally synthesized. Figure 4.1 explains the N-Bit encoder for N-Bit flash ADC. The total number of full adders required for N-bit encoder is 2^N-N-1. Figure 4.2 shows the synthesized design of 4-bit Wallace tree encoder

with zoomed full adder design. With the help of digital design, placement and routing can also be done easily. The Verilog code of Wallace tree encoder is shown below in Figure 4.3.

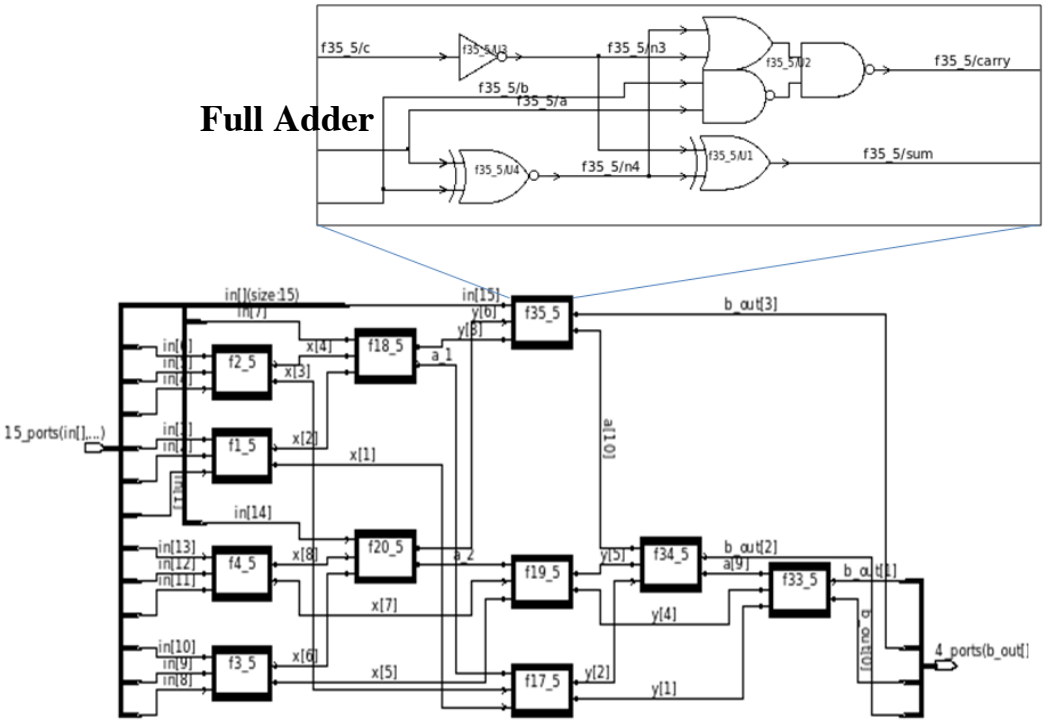


Figure 4.2 Synthesized design of 4-bit Wallace tree Encoder with zoomed full adder design showing above.

```
Module Wallace _4bit (in,b_out);
   input [15:1] in;
output [3:0] b_out;
   wire [32:1] x;
   wire [24:1] y;
   wire [16:1] z;
   wire [26:1] a;
   wire [10:1] k;
   // level 1 full adder
   fa f1_5 (x[2],x[1],in[3],in[2],in[1]);
   fa f2_5 (x[4],x[3],in[6],in[5],in[4]);
   fa f3_5 (x[6],x[5],in[10],in[9],in[8]);
   fa f4_5 (x[8],x[7],in[13],in[12],in[11]);
  // level 2
   fa f17_5 (y[2],y[1],a[1],x[3],x[1]);
   fa f17_5 (y[2],y[1],a[1],x[3],x[1]);
   fa f18_5 (y[3],a[1],in[7],x[4],x[2]);
   fa f19_5 (y[5],y[4],a[2],x[7],x[5]);
   fa f20_5 (y[6],a[2],in[14],x[8],x[6]);//level3
   fa f33_5 (b_out [1],b_out [0],a[9],y[4],y[1]);
   fa f34_5 (b_out[2],a[9],a[10],y[5],y[2]);
   fa f35_5 (b_out[3],a[10],in[15],y[6],y[3]);
endmodule
module fa_1 (sum_1, carry_1, a_1,b_1,c_1);
   output sum_1 ,carry_1;
   input a_1,b_1,c_1;
   assign sum_1 = a_1 ^ b_1 ^c_1;
   assign carry_1= (a_1 & b_1) | (b_1 & c_1)|
(c_1 & a_1);
endmodule
```

Figure 4.3 Verilog code for 4-bit Wallace Encoder

The Design vision Synopsys tool is used to synthesize the encoder design by applying timing constraints. The minimum delay of encoder without pipelining is obtained as 1.89ns by inserting buffers. The resistance of thin wires is more which increases the delay in signal processing. The insertion of buffers reduces the wire delay in long wires by maintaining the same signal strength.

Figure 4.4 shows synthesized design of 4-bit Wallace tree Encoder after applying timing constraints. As comapre to the Figure 4.2 insertion of buffer is there to reduce the delay.

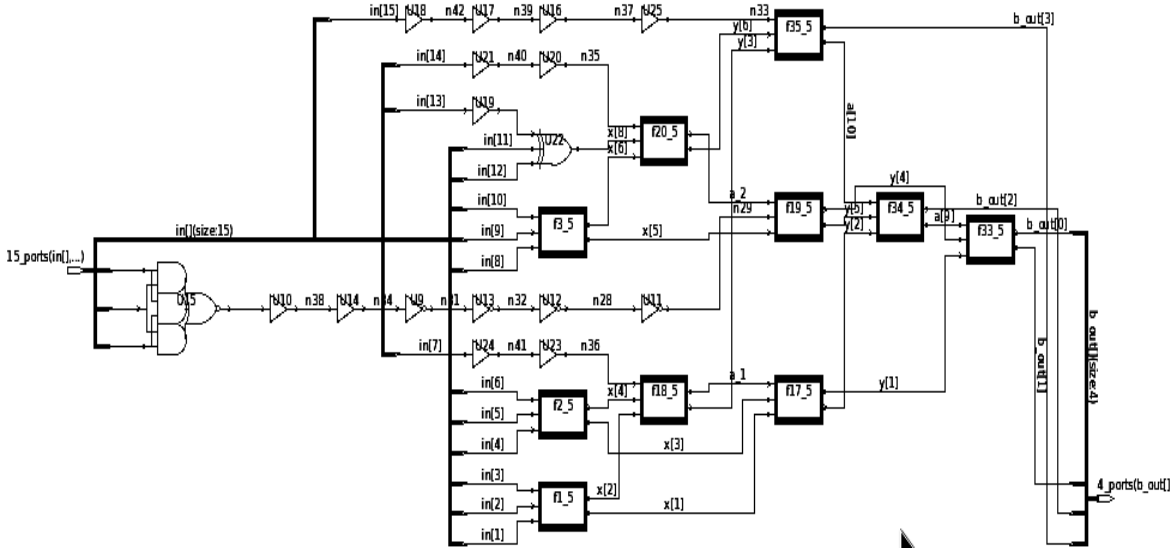


Figure 4.4 Synthesized design of 4-bit Wallace tree Encoder after applying timing constraints

The Wallace tree encoder is tested for all combinations which are presented in truth table and results are verified from truth table. Table 4.2 contains the truth table of thermometer to binary code. Figure 4.5 gives the simulation result of 4 bit Wallace tree encoder.

Table 4.2 Four bit thermometer to binary code truth table

Thermometer Code	y3	y2	y1	y0
000000000000000	0	0	0	0
000000000000001	0	0	0	1
000000000000011	0	0	1	0
000000000000111	0	0	1	1
000000000001111	0	1	0	0
000000000011111	0	1	0	1
000000000111111	0	1	1	0
000000001111111	0	1	1	1
000000011111111	1	0	0	0
000000111111111	1	0	0	1
000001111111111	1	0	1	0
000011111111111	1	0	1	1
000111111111111	1	1	0	0
001111111111111	1	1	0	1
011111111111111	1	1	1	0
111111111111111	1	1	1	1

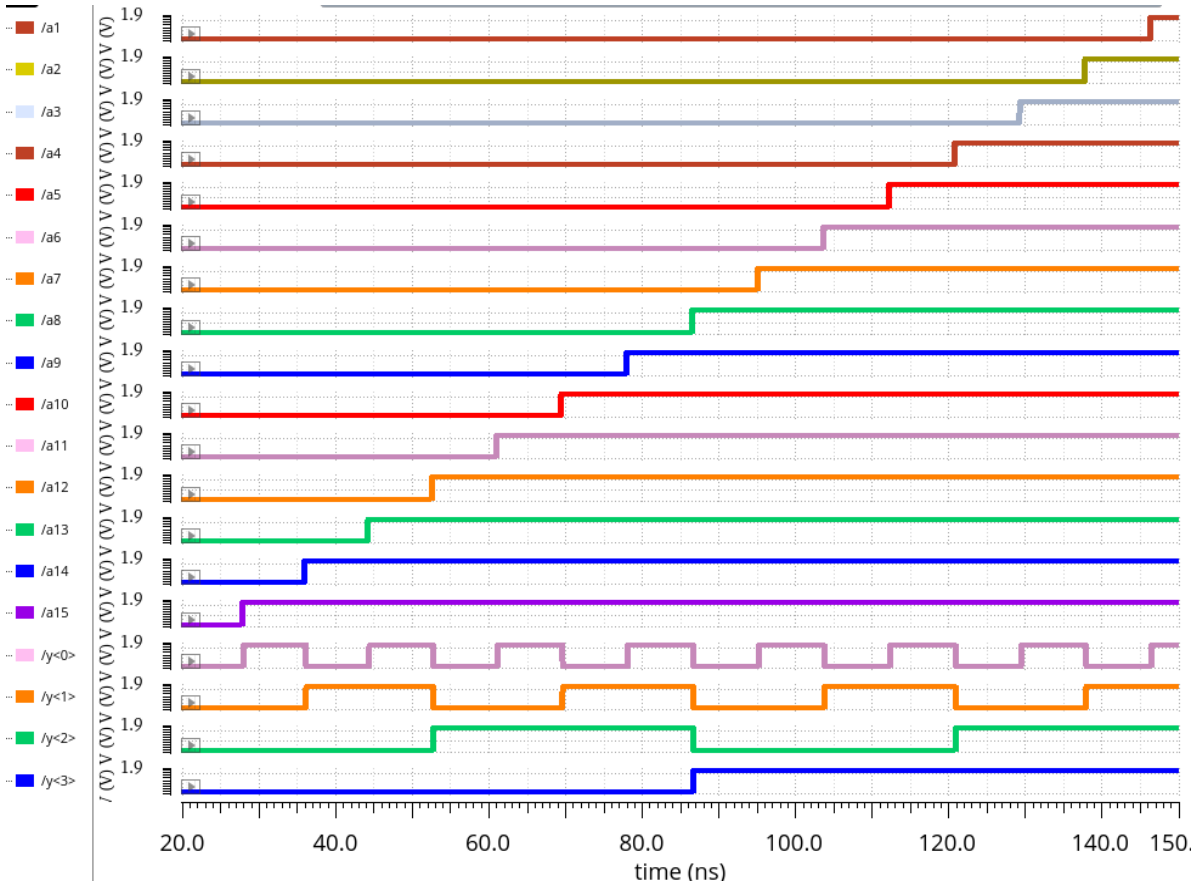


Figure 4.5 Simulation result of Wallace tree encoder without pipelining

4.2 IMPLEMENTATION OF PIPELINED WALLACE TREE ENCODER

The main application of this encoder is high speed 1's addition and is proficient. Figure 4.6 shows the structure of this pipelined Wallace tree encoder. It is like conventional carry look ahead adder. This method is fast as in one stage only one full adder is present but in ripple carry adder more number of stages are present. To boost the speed of encoder, pipeline is inserted by adding D flip flop between each layer. It will increase the throughput and also it enhances the speed of the circuit.

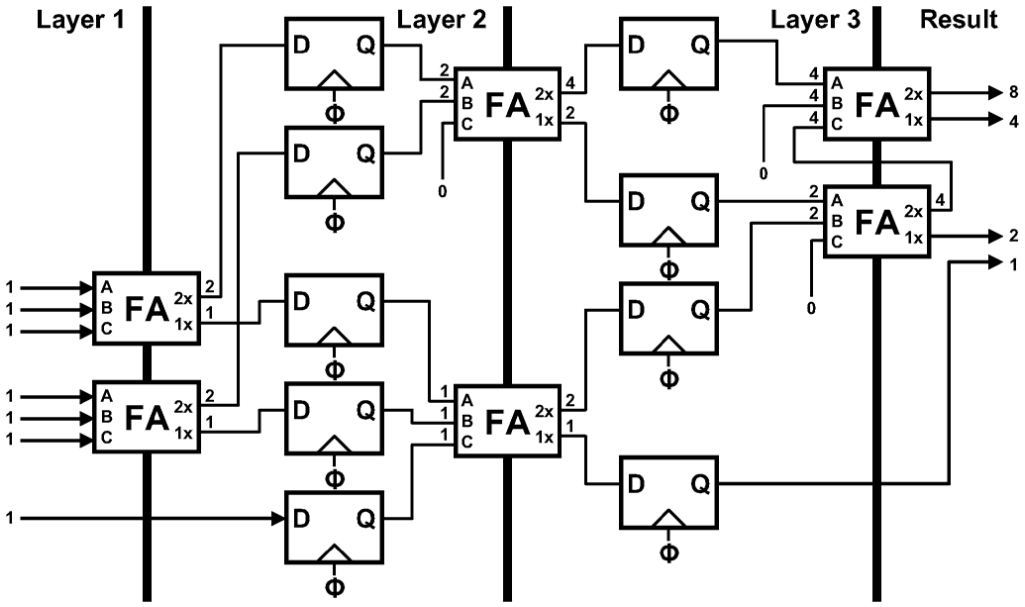


Figure 4.6 Block diagram of a pipelined Wallace tree

In Figure 4.7 synthesized design of 4-bit Pipelined Wallace tree Encoder after applying timing constraints is shown. Simulation result of Wallace tree encoder with pipelining concept shown in Figure 4.8. Thermometer to binary output with respect to clock is shown in the simulation result.

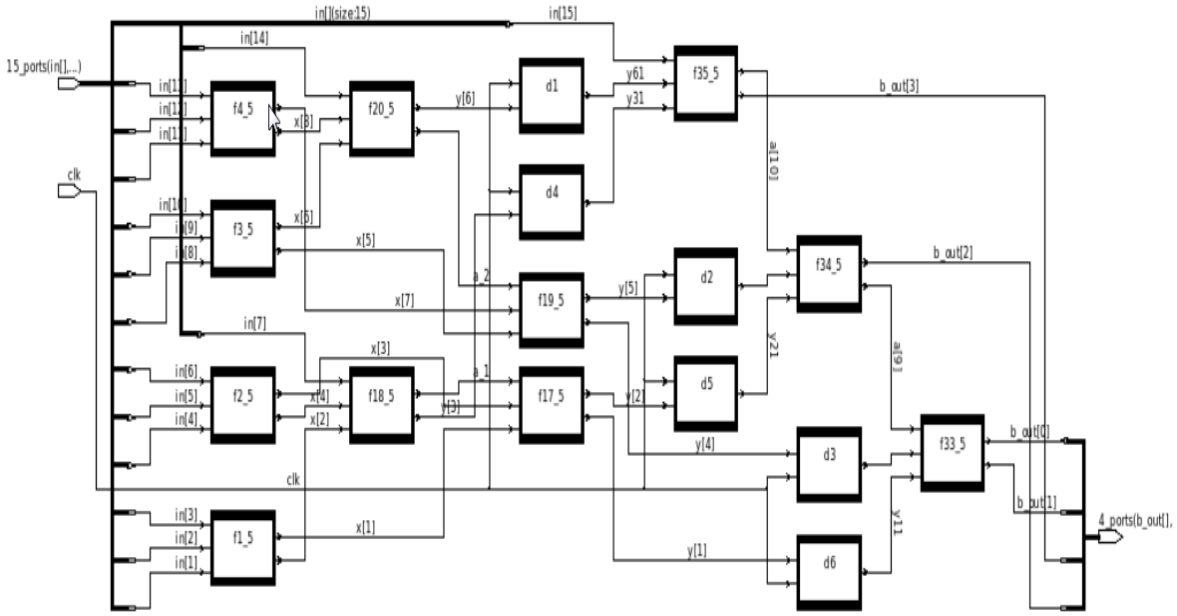


Figure 4.7 Synthesized design of 4-bit Pipelined Wallace tree Encoder after applying timing constraints

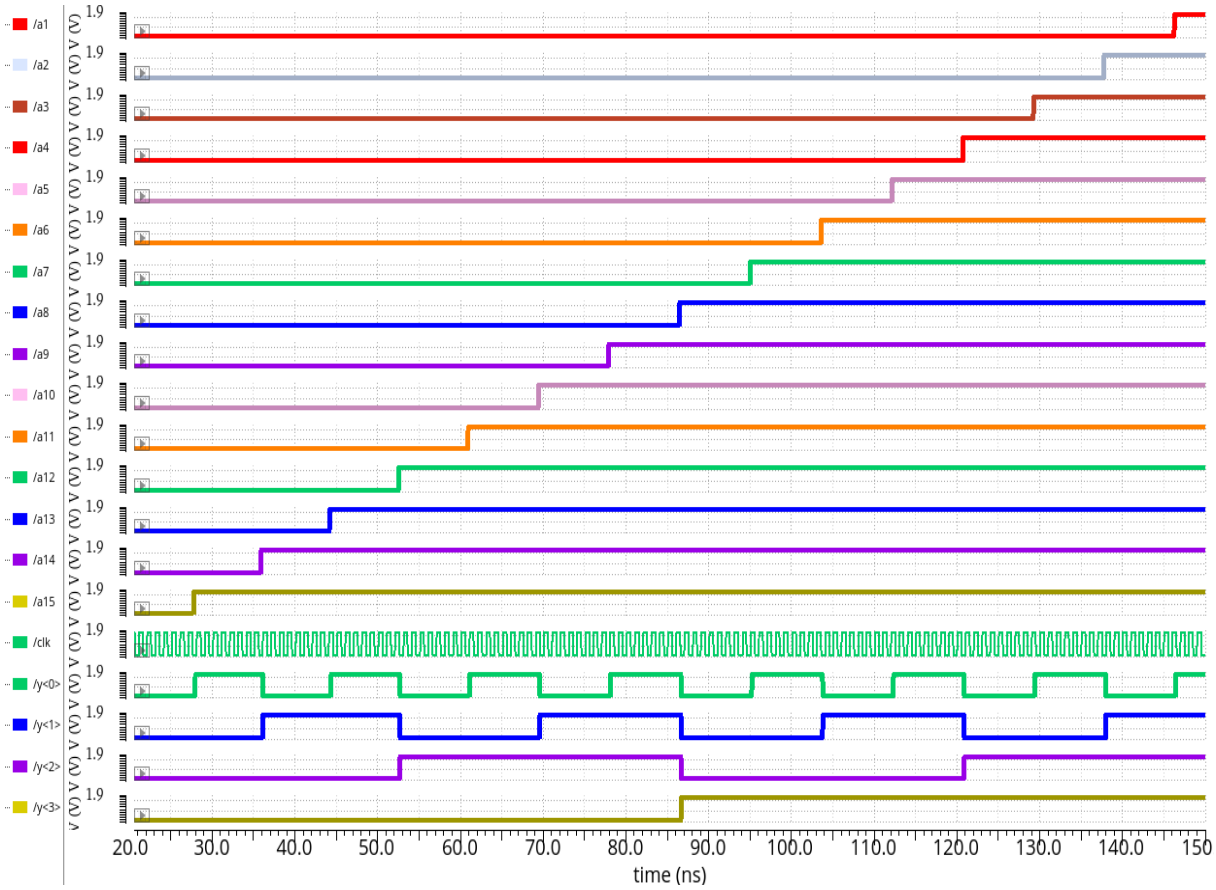


Figure 4.8 Simulation result of Wallace tree encoder with pipelining

CHAPTER 5
SIMULATION AND EXPERIMENTAL RESULTS OF FLASH ADC

The preceding chapters illustrate verilog code based digital-in-concept synthesizable with or without pipelining comparator and bubble error tolerant Wallace tree encoder for a four bit flash ADC. Flash ADC has three main blocks: Resistive network, comparator and thermometer to binary encoder. In this chapter, a 4-bit flash ADC is designed by the combination of all blocks which is mentioned above. Also, various dynamic and static characteristics are measured. Different block of ADC has been discussed in next sections.

5.1 RESISTOR LADDER

A stable voltage reference is provided by resistor ladder to the comparators. Ladder network is created by 16 resistors that will generate the reference voltages. There is a difference of one LSB between each comparator. The ladder divides the reference voltages with same spacing of voltage as shown in Figure 5.1. In the proposed 4-bit flash ADC implementation *Vrefh*=1.5V and *Vrefl*=0.5V. So, the LSB of this flash ADC is

$$LSB = \frac{Vrefh - Vrefl}{2^4}$$

$$LSB = \frac{1.5 - 0.7}{16} = 50mV$$

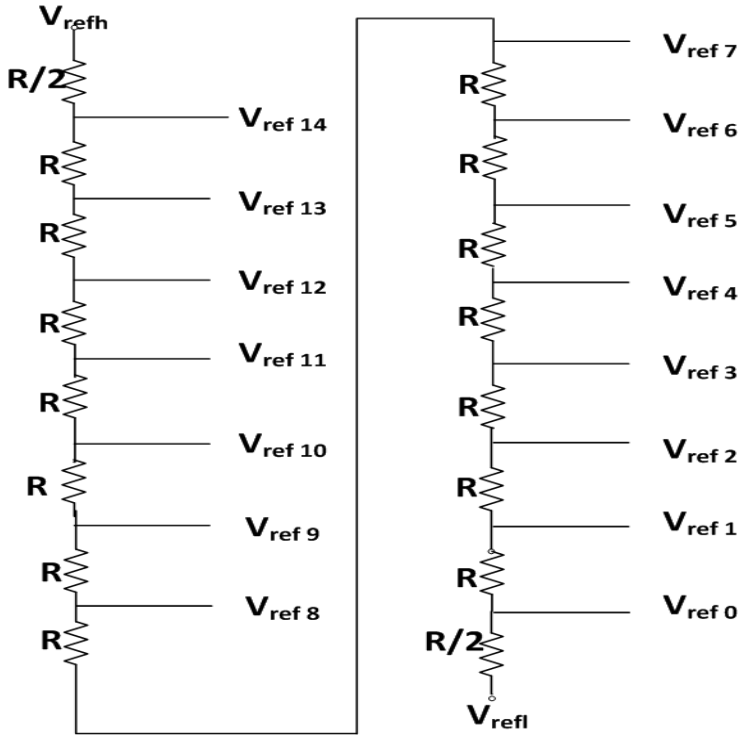


Figure 5.1 Resistor ladder

5.2 COMPARATOR

The comparator will compare input voltage (V_{in}) with the reference voltage (V_{ref}) that is generated by the reference ladder. If V_{in} is greater than V_{ref} the output of the comparator goes high and when V_{in} is less than the V_{ref} then the output of the comparator goes low. Hence the output of comparator is a string of '0's and '1's called thermometer code. The comparator structure designed in section 3.4 is used in this flash ADC which is created by using CMOS inverter and NAND-NOR logic gate whose major part is synthesized from verilog code. Number of comparator required for bit flash ADC is 15. The comparator works at the frequency of 200 MHz with the power dissipation of 221.4µW at 1.8 supply voltage. The delay and offset voltage of this comparator is 2.96ns and 4.9 mV which is discussed in chapter 3.

5.3 ENCODER

Bubble error tolerant high speed pipelined encoder is chosen for designing a 4-bit flash ADC due to its less time to market and less delay. This design is also be synthesizable because of verilog code. Minimum delay of encoder without pipelining is 1.89ns by the insertion of buffers and with pipelining delay further reduces to 1V. The performance of pipelining encoder increases over an un-pipelined encoder depending on the number of stages.

5.4 FLASH ADC TOP LEVEL IMPLEMENTATION

Based on the architecture explained in Figure 1.1, complete design of 4-bit flash ADC circuit combining all above-mentioned block is shown in Figure 5.2. The design is simulated and verified in Cadence Virtuoso with a model parameter of SCL 180nm CMOS technology.
Figure.5.2 shows the block level representation of 4-bit Flash ADC. The Flash ADC is verified by different input signals.

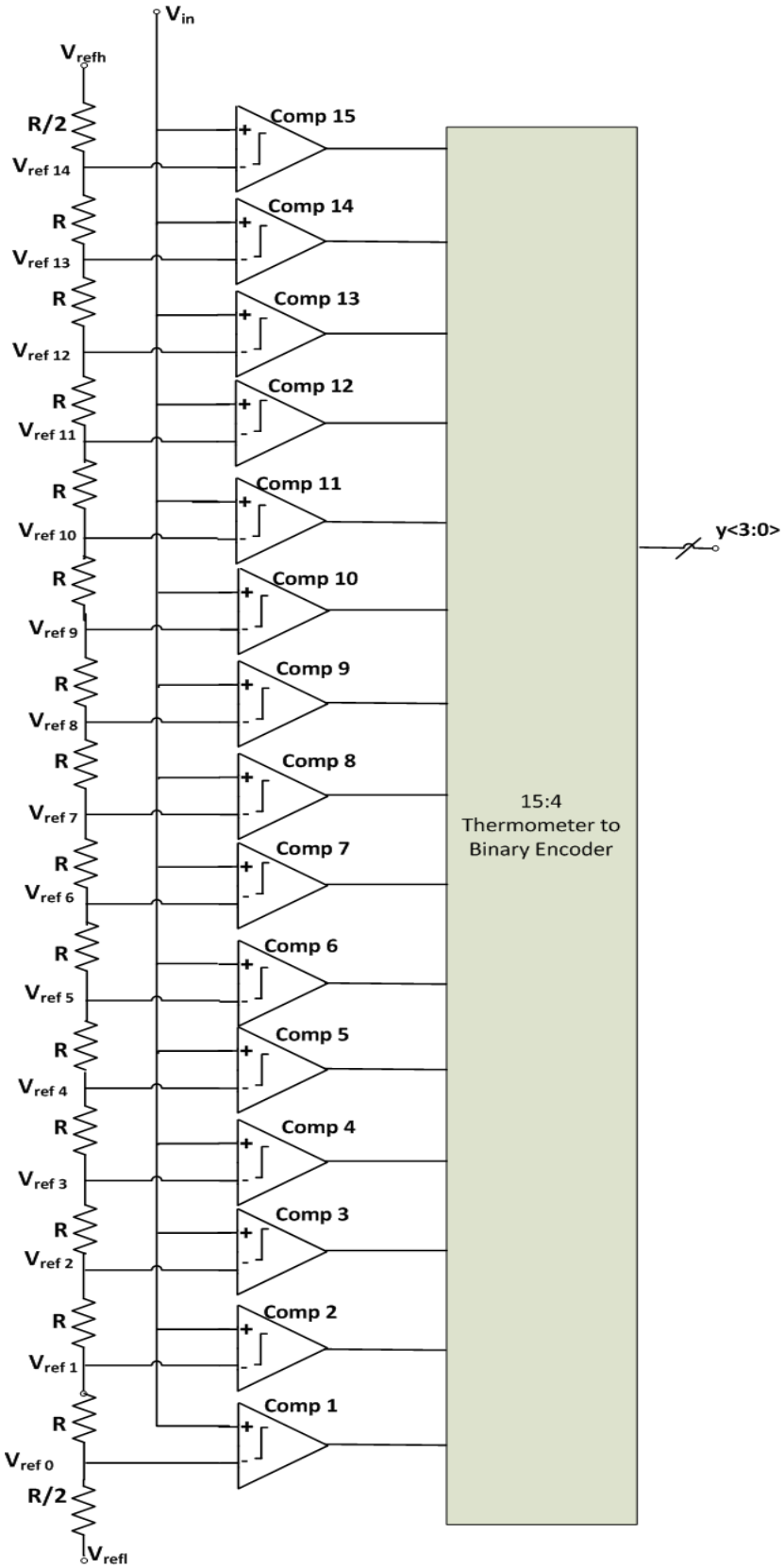


Figure 5.2 Block diagram representation of 4-bit flash ADC

The transient analysis of complete 4-bit flash ADC is shown in Figure.5.3. The digital 4-bit output (y3, y2, y1, y0) with respect to input ramp signal (Vin) is seen in this figure.

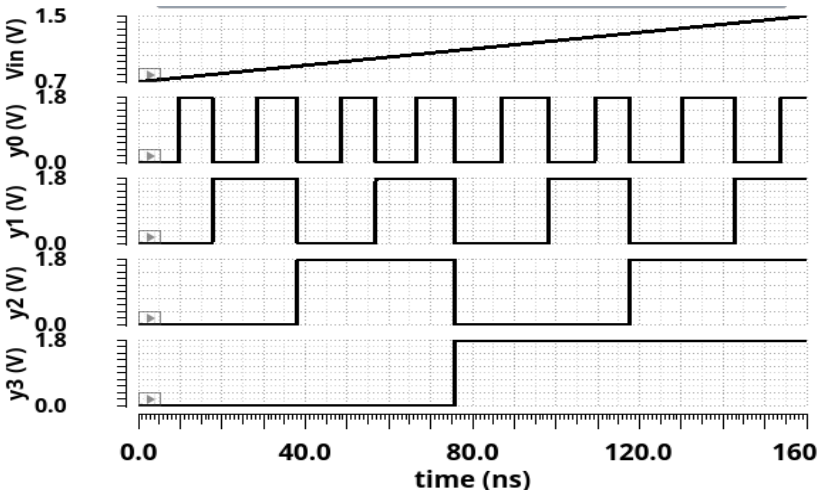


Figure 5.3 The simulation result of 4-bit flash ADC with ramp signal as input

The transient analysis of complete 4-bit flash ADC with the sinusoidal input is shown in Figure.5.4. Vout is constructed from the input sinusoidal signal at 10MHz frequency.

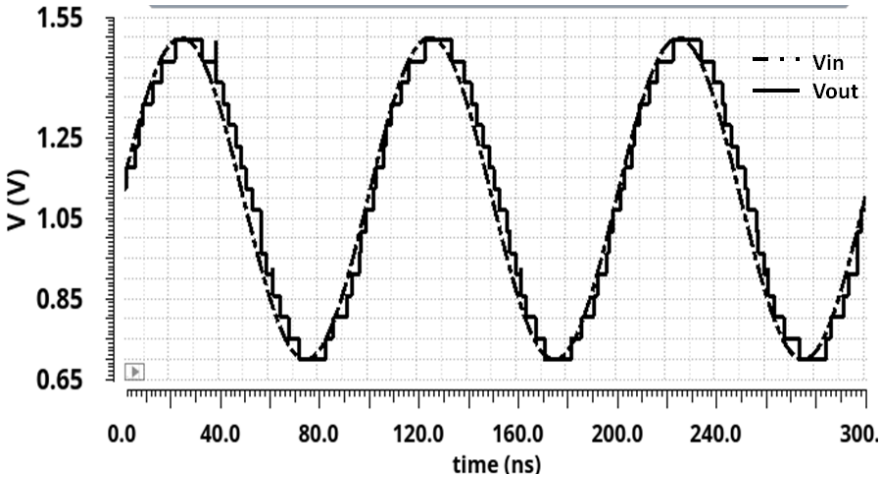


Figure 5.4 The simulation result of 4-bit flash ADC with Sin as input where input frequency is 10MHz

A DNL (differential non-linearity) error specification of less than and equal to 1LSB promises a monotonic transfer function with no missing codes. INL (integral non-linearity) is cumulative sum of DNL code. The DNL and INL of four bit flash ADC is measured and is shown in Figure 5.5. The DNL of this proposed flash ADC is $\pm$0.25 LSB and INL is $\pm$0.6 LSB. The linearity is restricted is between 1 LSB.

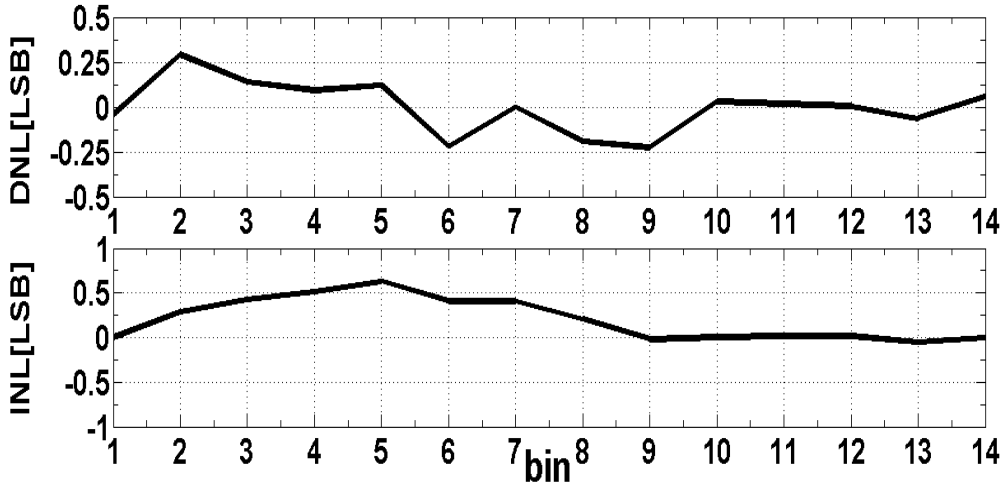


Figure 5.5 The INL and DNL of proposed 4-bit flash ADC

The FFT spectrum of reconstructed signal is used to calculate the dynamic performance of flash ADC. Fig.5.6 and Fig.5.7 show the reconstructed signal spectrum for an input signal frequency of 1.66MHz and 31MHz and sampled at 100MHz and 200MHz respectively.

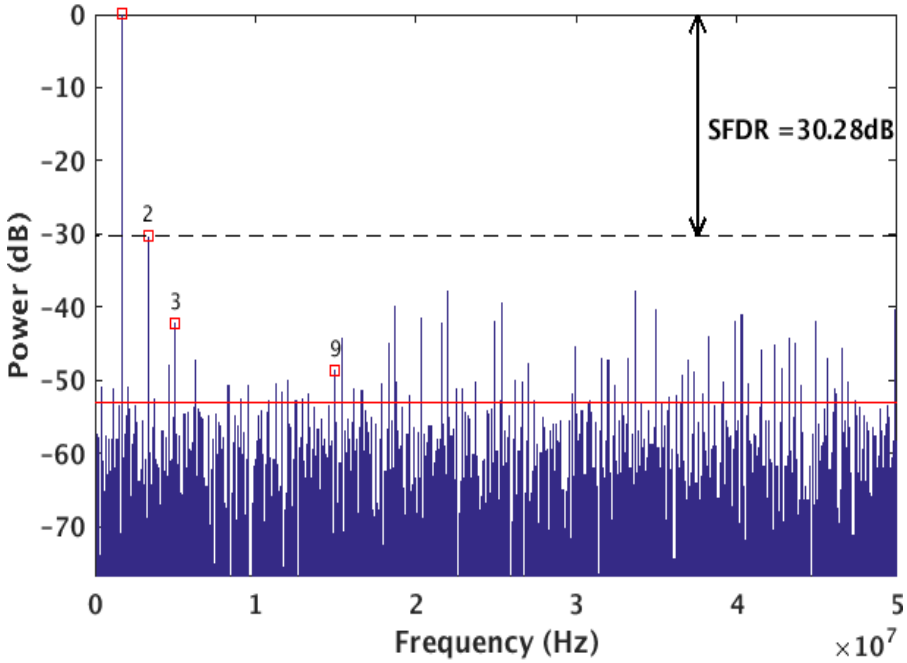


Figure 5.6 The FFT of proposed 4-bit flash ADC with input frequency of 1.66MHz

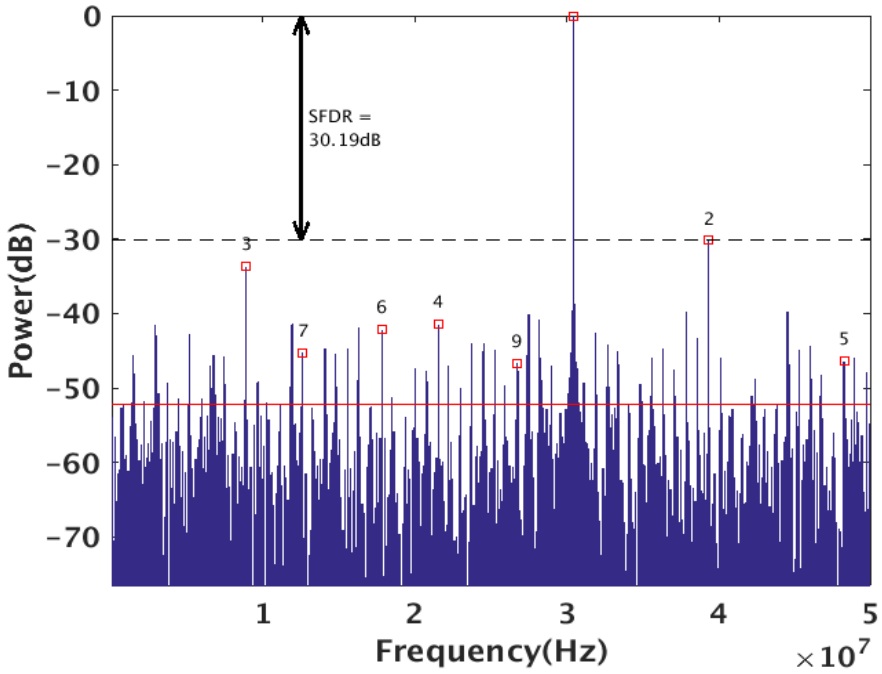
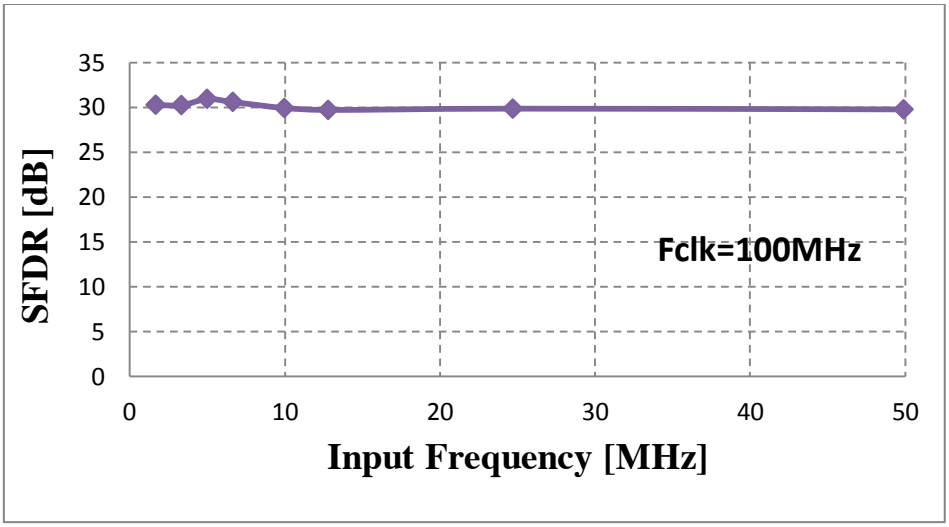
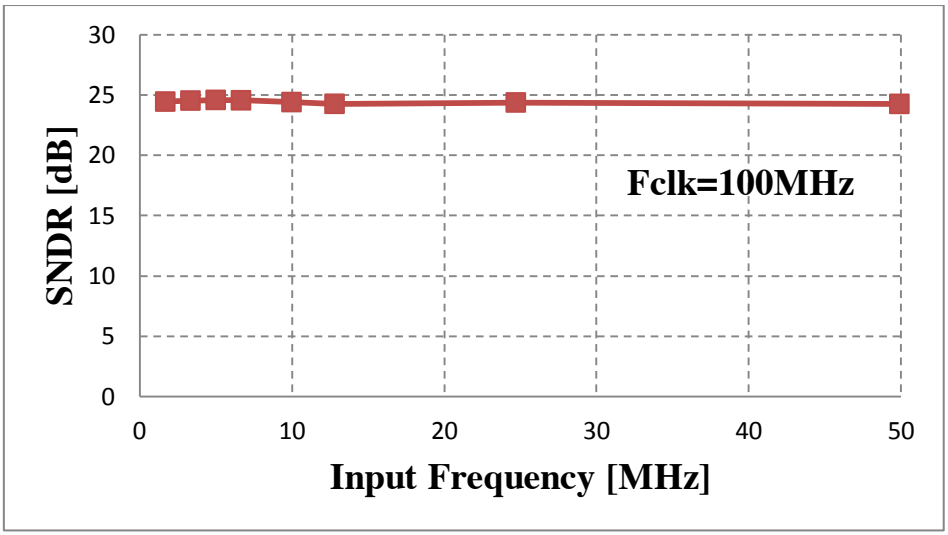


Figure 5.7 The FFT of proposed 4-bit flash ADC with input frequency of 33.20MHz

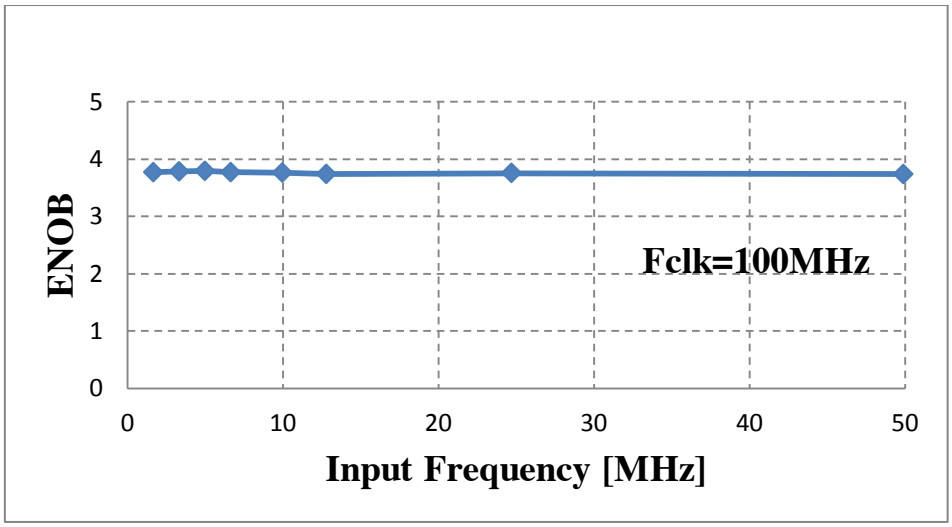
The dynamic performance of ADC is shown in Figure 5.8 and 5.9. When input frequency is 1.66MHz and clock frequency is 100MHz, the value of ENOB, SNDR, SNR and SFDR are obtained as 3.7702, 24.4566dB, 25.9533dB and 30.2788dB respectively. The value of ENOB, SNDR, SNR and SFDR are obtained as 3.5890, 23.3656dB, 25.2093dB and 30.1819dB respectively, when input frequency is 1.66MHz and clock frequency is 100MHz. Figure 5.8 shows the values of ENOB, SNDR, SFDR, SNR with the variation in input frequency at clock frequency of 100MHz. Figure 5.9 shows the values of ENOB, SNDR, SFDR, SNR with the variation in input frequency at clock frequency of 200MHz. The total delay of ADC is 4.853ns.



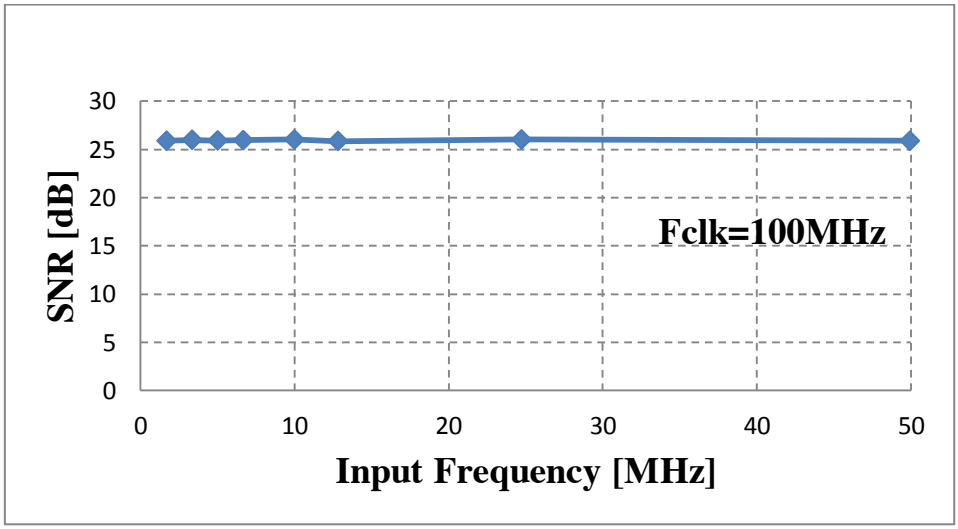
(a)



(b)

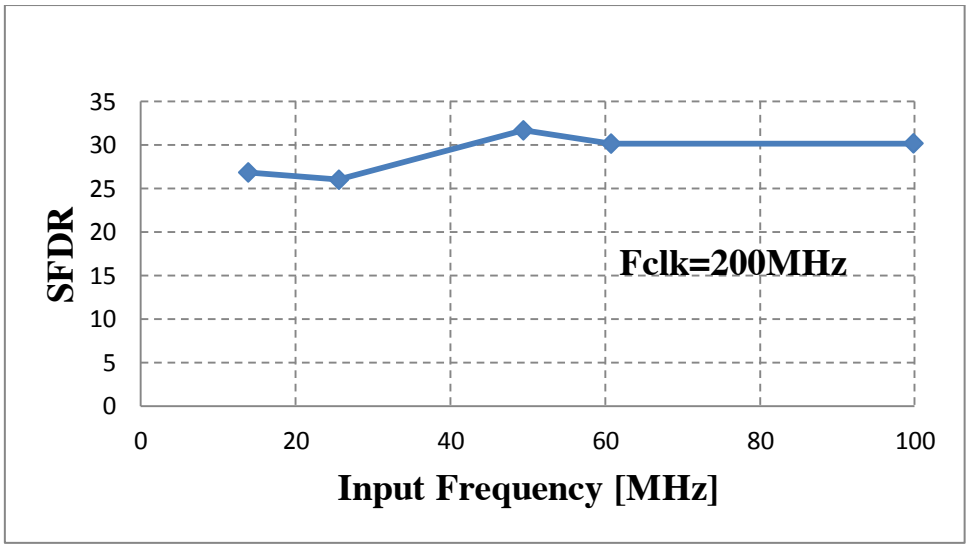


(c)

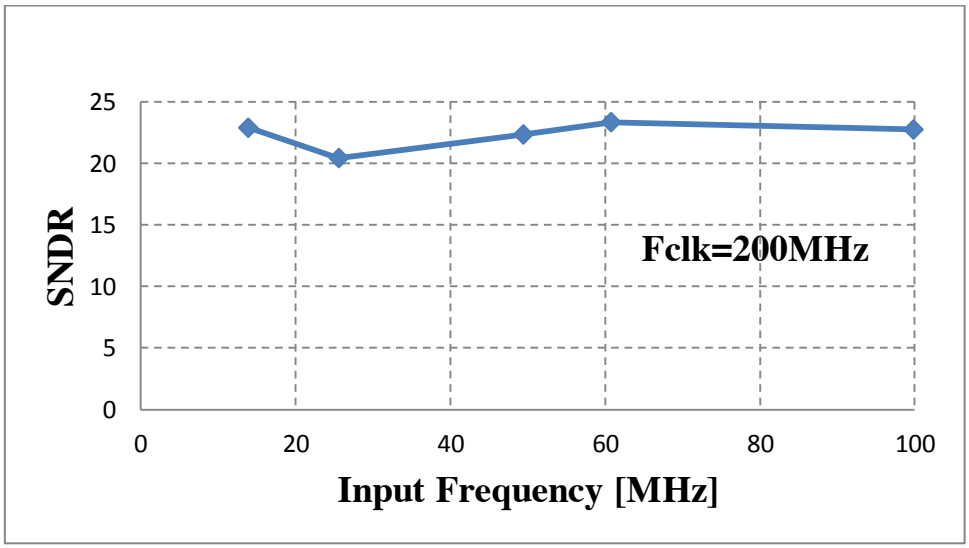


(d)

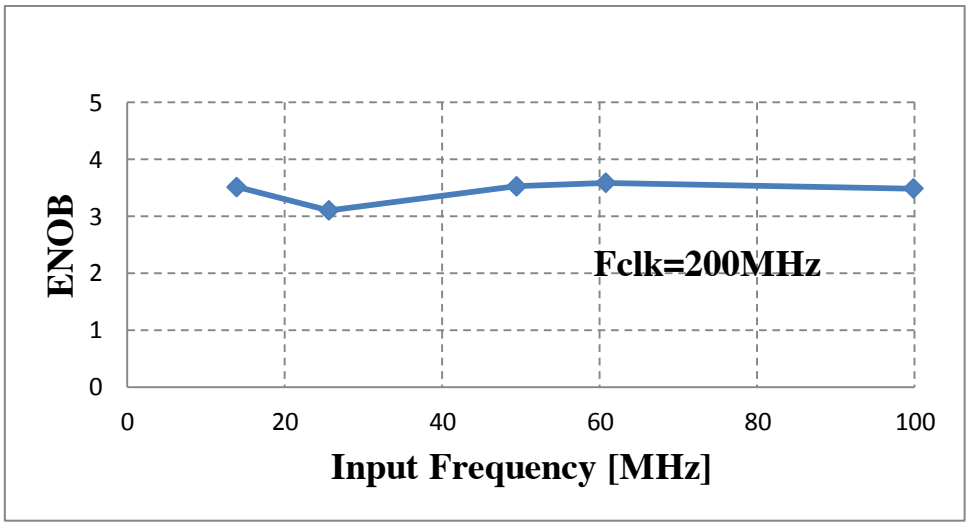
Figure 5.8 Measured dynamic performance of comparator a) SFDR b) SNDR c) ENOB d) SNR at clock frequency of 100MHz


SFDR
35
30
25
20
15
10
5
0
0
20
40
60
80
100
Fclk=200MHz
Input Frequency [MHz]

(a)


SNDR
25
20
15
10
5
0
0
20
40
60
80
100
Fclk=200MHz
Input Frequency [MHz]

(b)


ENOB
5
4
3
2
1
0
0
20
40
60
80
100
Fclk=200MHz
Input Frequency [MHz]

(c)

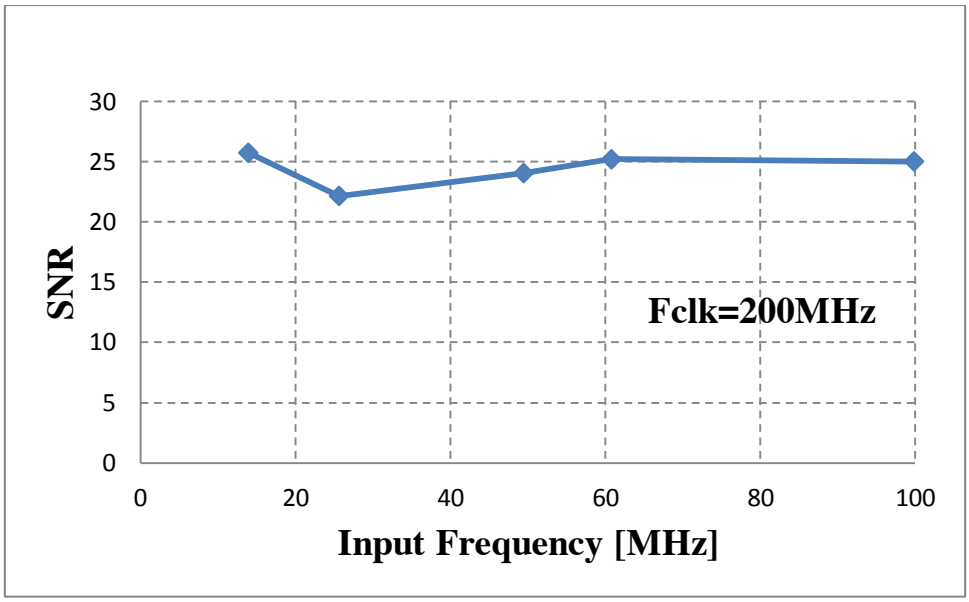


Figure 5.9 Measured dynamic performance of comparator a) SFDR b) SNDR c) ENOB d) SNR at clock frequency 200MHz

CHAPTER 6
CONCLUSION AND FUTURE SCOPE

6.1 CONCLUSION

In recent years, Digital signal processing has progressed drastically with technology. However it with not provide the same level of advantage as of analog IC. To get the more accurate output, we will process the signal into digital form. Most of the communication need wireless signal i.e. digital signal but in the real world, all outputs are analog in nature so we have to convert analog signal to digital signal to communicate to the real world. For an efficient system, all blocks should be fast. This fact has led researchers to develop and implement high speed analog-to- digital converters (ADCs) with low power consumption.

The research work in this thesis presents the highly digital 4-bit 200-MS flash ADC whose major part can be synthesized from verilog code thus achieving low power and reduces the much needed time to market. The comparator circuit is created by CMOS using Inverter and NAND-NOR logic gates. The proposed circuits are simulated in Cadence Virtuoso Analog Design Environment and Anolog Mixed Signaling (AMS) in SCL 180 nm CMOS technology. Based on the comparison of different comparator available in literature, it is concluded that synthesized proposed pipelined comparator with verilog code is more efficient in terms of power, delay and offset etc. Also, the proposed digital-in-process flash ADC has been proposed.

6.2 FUTURE SCOPE

The parameter of flash ADC is considered for low resolution and characteristic are compared with other ADCs. To reduce the offset voltage, the offset cancellation scheme which enhances the efficiency of flash ADC can be applied. The proposed flash ADC is all digital-in-concept except the resistive network which can also be replaced by MOS based structure. Also, the high speed and low power can be achieved with different calibration scheme which leads to simplify the design.

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