PERFORMANCE INVESTIGATION OF ASYMMETRICAL CASCADED H-BRIDGE MULTILEVEL INVERTER BASED DSTATCOM IN DISTRIBUTION NETWORK

A dissertation submitted in fulfillment of the requirements for the degree of

MASTER OF ENGINEERING

in

Power Systems

Submitted by

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CERTIFICATE

I hereby certify that the work which is being presented in this thesis entitled "**Performance Investigation of Asymmetrical Cascaded H-Bridge Multilevel Inverter Based DSTATCOM in Distribution Network**" in partial fulfillment of the requirement for the award degree of Master of Engineering in *Power Systems* submitted in Electrical and Instrumentation Engineering Department, Thapar University, Patiala is an authentic record of my own work carried out under the guidance of **Dr. Parag Nijhawan,** Assistant Professor, EIED, Thapar University, Patiala & **Dr. Surya Prakash,** Assistant Professor, EIED, Thapar University, Patiala.

The work presented in this thesis has not been submitted for the award of any other degree of this or any other university.

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ACKNOWLEDGEMENT

I am thankful to the Electrical and Instrumentation Engineering Department for giving me the opportunity to do research work for assassinating dissertation which is an essential part of the curriculum in M.E., Power Systems at Thapar University, Patiala.

I would like to express my genuine thanks and concern to my supervisors **Dr. Parag Nijhawan,** Assistant Professor, EIED and **Dr. Surya Prakash,** Assistant Professor, EIED for their guidance, encouragement and support throughout the dissertation work. They helped me a lot in clarifying my all doubts which boosted my confidence level and this made me easy to carry out my work.

I would like to express my gratitude towards **Dr. Ravinder Agarwal,** Professor and Head of EIED for their inspiration and guidance throughout this dissertation course and all the faculty members of the EIED for their scholarly cerebral backing.

I would also like to express my cordial thanks to my family members and my classmates for their support and motivation.

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ABSTRACT

Asymmetrical cascaded H-bridge multilevel inverter based on the series connection of single phase inverter has the ability to resolve the power quality issues such as elimination in harmonic contents when used with DSTATCOM in the distribution network. By using many separate dc sources, it can produce high number of ac voltage levels. Asymmetrical multilevel inverters are well-suited for high power and medium applications due to their several advantages. In this work, firstly a comparison is done between the different voltage levels (7, 9, 11 and 13) of Asymmetrical cascaded H-bridge multilevel inverter on the basis of THD. After that, performance of seven level asymmetrical cascaded H-bridge inverter based DSTATCOM in the 11 kV/ 400V secondary distribution network is emphasized. The work focuses on the mitigation of harmonics and compensation of load balance during disturbances in the distribution system. Level Shifted Alternate Phase Opposition Disposition PWM control strategy is used for the generation of all the gate pulses. For the generation of reference source currents for DSTATCOM, Synchronous Reference Frame (SRF) theory based on Park's transformation is employed.

TABLE OF CONTENTS

LIST OF TABLES

LIST OF FIGURES

LIST OF ABBREVIATIONS

ACRONYMS	FULL FORM
MLI	Multilevel Inverter
PWM	Pulse Width Modulation
FACTS	Flexible AC Transmission System
CHB	Cascaded H-bridge
THD	Total Harmonic Distortion
DSTATCOM	Distribution Static Compensator
APOD	Alternate Phase Opposition Disposition
VSC	Voltage Source Converter
VSI	Voltage Source Inverter
DC-MLI	Diode Clamped Multilevel Inverter
FC-MLI	Flying Capacitor Multilevel Inverter
DVR	Dynamic Voltage Restorer
UPQC	Unified Power Quality Conditioner
IRP	Instantaneous Reactive Power
SRF	Synchronous Reference Frame
IEEE	Institute of Electrical and Electronics Engineers
PQ	Power Quality
MATLAB	Matrix Laboratory
FOC	Field Oriented Control
DTC	Direct Torque Control
PI	Proportional Integral
SDCSs	Separate DC sources
IGBT	Insulated Gate Bipolar Transistor
MOSFET	Metal Oxide Semi-conductor Field Effect Transistor
VAR	Volt-Ampere Reactive
ACHBMIL	Asymmetrical cascaded H-bridge multilevel inverter

LIST OF SYMBOLS

SYMBOL	MEANING
V_{0n}	Output voltage with respect to ground
N	No. of H-bridge cells
V_i	Inverter voltage
V_H	Voltage of H-bridge
M	Number of levels
N_s	Number of switches
V_0	Total output voltage
V_{dc}	DC voltage
V^*	Magnitude of sine wave
m_f	Frequency ratio
m_a	Modulation index
V_s	Source voltage
θ	Transformation angle
α	Conduction angle
β	Dead angle
v_a, v_b, v_c	Three phase system voltages
v^*_{dc}	Reference dc voltage
V_{dc}	Actual dc voltage
ΔV_{dc}	Error of dc voltage
I_d	Direct axis current
I_q	Quadrature axis current
i^*_{sd}	Reference source current of d-axis
i^*_{sq}	Reference source current of q-axis
$i^*_{s\alpha}, i^*_{s\beta}$	Reference source current of $\alpha - \beta$ components
$i^*_{sa}, i^*_{sb}, i*_{sc}$	Reference source current of a, b and c components
$i^*_{ca}, i^*_{cb}, i^*_{cc}$	Reference compensating currents

CHAPTER 1
OVERVIEW

1.1 Introduction

Multilevel inverters also known as power converters are becoming popular day by day due to their excellent features like they have tendency to satisfy high power and high voltage that are required in the industries, give less harmonics when compared to a 2 level voltage source inverter, it has overcome the problem of using passive filters, give reduced switching losses, improved efficiency [1], [2], [3]. MLI refers to the inverter that gives either voltage levels 3 or more than three voltages. We can operate MLI either at fundamental frequency or high switching frequency PWM. The stair case waveforms produced by multilevel inverters produces AC output stepped waveform pure sinusoidal. MLI can effectively eliminate electromagnetic interference using many dc voltage levels.

Power electronics acts like a backbone of a power systems. It is an umbrella for power system based applications like improving reactive power compensation, low harmonic distortions, balancing the changing load, achieving sinusoidal voltage and current, and power quality improvement [44]. The main reason behind the increasing demand of power electronics is its voltage source inverter which is the basic building for FACTS and custom power devices for generating voltage or current with having equal magnitudes. Multilevel inverters have failed a simple 2level inverter and have a great reach in the applications of medium as well as high distribution networks in improving power quality. Multilevel inverters use many switching devices as compared to a 2level VSI that is generally good for the high power applications [6], [38]. There is a main advantage of using multilevel inverters that as we increase the number of levels, harmonics get reduced. Switching devices are non-dependent in multilevel inverters. A good quality output is achieved by MLI. There are different topologies of multilevel inverter; Diode clamped, Cascaded H-bridge, flying capacitor but Cascaded H-bridge multilevel inverter has a great extent in power quality based applications [8], [39]. CHB multilevel inverters use many separate dc sources and two or more than two single phase inverters connected in a series with each other. These inverters are cheap when compared with the other topologies. CHB inverters can be realized either in symmetric or asymmetric arrangement [11], [12].But implementing in asymmetrical form is better option than symmetrical arrangement. It uses further less switching components for realizing the same number of levels as in the case of symmetrical CHB inverters. So,

asymmetric inverters are cheaper than symmetric inverters. Further, it gives reduced THD than symmetric cascaded H-bridge multilevel inverters. Just like symmetric cascaded H-bridge inverter uses one extra dc source and one more H-bridge with the simultaneous increment in the number of levels, this does not happen in the case of asymmetrical CHB multilevel inverters.

There are some disadvantages of classical pulse generator used for generation of switching pulses. It does not give satisfactory results of harmonics. For achieving sinusoidal voltage or current signals and to reduce harmonics, multicarrier based sinusoidal PWM is the best choice to overcome the limitations of a pulse generator. For the realization of inverter in the high power applications, simple pulse generator is not effective to use, while multicarrier sinusoidal PWM

strategies are more productive to use [25], [40]. Thus, in order to get sinusoidal, balanced and very much reduced THD, the combination of asymmetric CHB inverters with multicarrier sinusoidal PWM combination is a good approach.

Since improvement of power quality is a major anxiousness for power quality engineers, custom power devices are used in improving power quality [30], [31], [41], [42]. The limitations of a 2 level VSC are overcome by multilevel inverters. Nonlinear loads are mostly seen connected in the distribution networks which are responsible for the harmonics and effects the source. DSTATCOM is one of the custom power devices that prevents the supply side from getting affected by the harmonics due to nonlinear load [41], [42]. The main function of DSTATCOM is to make the source current balanced with reduced effects of harmonics in the load current. With DSTATCOM, sinusoidal current waveforms are achieved and it ceases the disturbances in the load current waveforms during any fault event to effect the source current waveforms. Using asymmetrical multilevel CHB multilevel inverters in place of a 2 level inverter in DSTATCOM will give comparatively reduced THD. and more sinusoidal current waveforms we achieve.

1.2 Scope of Work

As far as high power and medium voltage applications are concerned, two level voltage source inverter is not so effective to be realized in comparison with the multilevel inverters. In distribution systems, where load harmonics effect the ac source, presence of multilevel inverter in place of a 2 level inverter nullifies the effect and make the source balanced. So, in this thesis among various topologies of multilevel inverter, cascaded H-bridge multilevel inverter in asymmetrical arrangement of dc voltages is implemented. Various levels of

asymmetrical cascaded H-bridge inverters are first realized with different algorithms of dc source voltage arrangement and then a comparative analysis is done on the basis of harmonic contents, sinusoidal waveforms, switching devices. Out of these different levels, one level is implemented with DSTATCOM for the enrichment of power quality in distribution network by reducing THD. in the source current and making it balanced.

1.3 Aim and Objectives of Thesis

The main objectives of the work are:

- Realization of four different asymmetrical cascaded H-bridge multilevel inverters with using different methods of calculating magnitude of dc voltages through simulation.
- To develop a control strategy for the generation of gate pulses of the inverter. For this, APOD control strategy is chosen.
- To make a comparative analysis between different levels of asymmetrical CHB inverter.
- Implementation of asymmetrical cascaded H-bridge inverter in DSTATCOM in place of a conventional two level VSC and to investigate the performance of this inverter with DSTATCOM in the distribution network for the intensification of power quality.

1.4 Organization of Thesis

The thesis is sub-grouped into 6 chapters:

Chapter 1 constitutes the brief introduction along with the scope of work, aims and objectives of this work and framework of this thesis.

Chapter 2 presents the related work done by various researchers. It shows the brief review of work done so far.

Chapter 3 describes the cascaded H-bridge multilevel inverters including its types. This chapter depicts asymmetrical CHB multilevel inverter in detail covering different types of methods for selecting dc source voltages and revealing Alternate Phase Opposition Disposition PWM control strategy for the inverter. This chapter also shows the results from realization of different asymmetrical cascaded H-bridge inverters and presents the comparative analysis between these inverters on the basis of THD.

Chapter 4 describes DSTATCOM with its principle, operating modes and control strategy used for DSTATCOM.

Chapter 5 gives the description of test system that is DSTATCOM is analyzed in the distribution network. This chapter also discusses the performance of asymmetrical CHB inverter based DSTATCOM through simulation results.

Chapter 6 consists of conclusions and future scope.

CHAPTER 2
LITERATURE SURVEY

A brief synopsis of the related work carried out earlier is presented in this chapter.

Nabae et al. [1] introduced the concept of multilevel inverters. The author defined the multilevel inverters and claimed that the inverter starting with three level or more than three is referred to be a multilevel inverter. The main aim was to overcome the limitations of a 2 level inverter. Nabae realized that with using more than 2 levels of voltage source converter, it would produce multiple ac voltages. Later on in 1981, the author proposed neutral point clamped MLI starting with three levels from which he introduced the idea of multilevel inverter. He assumed the medium voltage of the three level inverter as neutral point. The three level inverter was the initial primary improvement of the two level inverter.

Lai et al. [2] had discussed the various topologies of multilevel inverter. The researcher developed the fundamentals, qualities, contents including applications of multilevel inverters in high power. Since multilevel inverter inverters generate many voltage levels by translating dc voltage levels into multiple ac voltages, these are in great demand to use in the high power applications. Multilevel inverter uses dc source of voltages for incorporating voltage waveform with stair case approach and reduces harmonic contents.

R.H. Baker et al. [3] introduced the concept of series inverter connection in the form of H-bridge. The aim was behind was that multiple voltages can be generated with the series connection of one phase inverter.

Following the above concept of series inverter connection, Marchesoni M. et al. [4] had proposed the inverter topology known as cascaded H-bridge multilevel inverter. Since other topologies of MLI; Diode clamped and Flying capacitor inverter use clamping diodes and flying capacitor respectively make the circuit complex, to overcome these disadvantages, cascaded H-bridge inverter was proposed. From here, the basic idea was generated [1990] to connect single phase inverter in series with several separate dc sources.

Further F.Z. Peng et al. [5] successfully realized the cascaded H-bridge multilevel inverter and labeled the disadvantages of DC-MLI and FC-MLI over cascaded inverters. Cascaded inverter was fully implemented for reactive power compensation in the high power applications. It was instantly linked in series with the electrical system.

L.M. Tolbert et al. [6] analyzed cascaded H-bridge inverter in large electric drives. In this research work, it was proved that cascaded H-bridge inverter is superior to be used in electric drive applications as these inverters use many separate dc sources which makes it possible to achieve high ratings of power.

Keith Corzine [7] described the basic idea of producing output of 15 level by the series connection of 5 level with three level inverter. His aim through this thought was to suggest that high number of voltage levels could be generated by the series connection of many H-bridges each having dc source voltage and approximate number of voltage steps.

Zhong Du et al. [8] first realized symmetric seven level and fifteen level cascaded H-bridge inverter. The aim was to mitigate harmonics. The disadvantage of using several dc voltage sources in the same inverter which other topologies use are overcome in this research work in which individual dc voltage source is used for each single phase inverter in both the levels.

Mariusz Malinowski et al. [9] has done a comparative analysis of cascaded H-bridge multilevel inverters with other topologies and this survey came out with the noteworthy qualities of cascaded H-bridge multilevel inverters in comparison to the other topologies. The attributes include that cascaded inverters have good fine-tune, cost effective solution and high power quality can be attained.

Domingo Caballero et al. [10] had established modified symmetric converter topology for utilizing in the high power and medium voltage applications. In account with the limitations of the symmetric inverters, the type of cascaded H-bridge multilevel inverter is introduced through this work known as asymmetric configuration of cascaded H-bridge inverter which uses unequal dc voltages. The researcher suggested the idea of using asymmetrical inverter because with symmetric multilevel inverter, many sources of dc have to be used along with so many switches, but with asymmetric structure for generating the same number of voltage levels, less switching devices and dc sources are needed which give cost effective solution over symmetric arrangement of the inverter. With less number of switches, high voltage levels can be achieved with asymmetric inverters. So, from this research work, concept of asymmetrical cascaded H-bridge multilevel inverter was introduced.

Farid Khoucha et al. [11] first realized asymmetrical multilevel inverter. For this, symmetrical inverters were also realized for the comparison analysis purpose on the basis of switching components, dc sources, and switch losses. Using five and seven level, a comparison was done. Both were realized in symmetric and asymmetric way and implemented for the applications in ac drives feeding direct torque control arrangement. A

conclusion was made that with equal number of generation of voltage levels in both the cases, asymmetrical require less number of components than symmetrical multilevel inverters.

Javad Ebrahimi [12] proposed different algorithms for selecting the values of separate dc sources. By using these procedures of arranging dc voltages, any level of asymmetrical inverter can be employed over cascaded sub cells. These methods give independency for designing any number of asymmetric voltage level.

Javad Ebrahimi et al. [13] further proposed a new method for determine the values of dc voltages and inserted in the asymmetric arrangement of the inverter with using only three switching components and dc sources for achieving absolute number of levels. The choice of the arrangement was dependent on the analysis of requirement of reduced switching devices, dc source voltages and decrement in dv/dt stresses for attaining high voltage levels.

Kaliamoorthy et al. [14] gave description about the cascaded topology in which two H-bridges were incorporated with different frequency operation. The inverter was implemented in symmetric arrangement with one H-bridge administered at frequency high and another one was at fundamental which is at 50 Hz frequency for producing five levels of ac output voltage. Two levels were generated from the first H-bridge with high frequency and another 2 levels were got from the second H-bridge and one zero level thus making it a five level.

In paper [15] asymmetrical 15 level cascaded H-bridge inverter is proposed. For comparison analysis, symmetrical level is also analyzed. In 15 level with asymmetric arrangement, binary algorithm which is in 1:2 ratio is used for calculating the values of dc sources while in symmetrical, same voltages are used. The topology is used for the high power applications. The paper presented a brief conclusion that with same number of switching components and dc sources, many voltage levels are produced as compared to the symmetrical inverters since with using only 3 H-bridges, we can get 15 levels of ac voltages in asymmetrical multilevel inverter while with symmetrical inverter, with the same number of bridges, we get only 7 level of voltages. The advantages of asymmetrical cascaded H-bridge inverter is revealed here.

Paper [16] presents the performance analysis of three phase seven level asymmetrical MLI at different modulation indices. The author made variations in the modulation index so as to reach the value of minimum THD. which is successfully achieved in this research work. The advantages of the proposed topology are revealed in this work as asymmetrical inverters are meant for using less switching components and individual dc sources.

In paper [17], binary based asymmetrical inverter is reported. Two H-bridges are used in the inverter to make output voltage of seven levels. Both the H-bridges are made to operate at different values of frequencies.

Paper [18] describes the proposed 27 level cascaded H-bridge inverter topology. The proposed topology can be used for locomotives for the voltage influence there. The aim behind this research is that this topology is efficient in the increment of the productivity of inverter and can suppress the destruction of the voltage. The topology can reduce the THD. in various devices that are related to electronics.

In paper [19], the author discusses the comparative investigation between various levels of asymmetrical topology on the basis of losses in the switches, harmonic contents. These inverters operated at low frequency.

For proving the superiority of asymmetrical cascaded H- bridge inverters over symmetrical inverter, performance of 15 level asymmetrical inverter is in the binary ratio is reported in paper [20]. The topology uses three H-bridges.

Paper [21] presents the proposed method for selecting values for dc voltages for the asymmetrical inverter topology. The main objective of the proposed topology is to reflect the less IGBT switches and reduced cost.

In paper [22], a reduced topology of asymmetrical cascaded H-bridge multilevel inverter is proposed. in this paper, it is shown that more number of voltage levels can be attained even with the reduced switch components, the paper also discusses the different algorithms such as binary, ternary for the calculation of separate dc sources. In this paper, ternary based asymmetrical cascaded H-bridge inverter is proposed.

For producing 13 levels of voltages with using reduced topology is presented in paper [23]. In this paper, four dissimilar dc voltage sources are used with 10 switches. The topology is cascaded sub-multicell in which asymmetric configuration is possible to be implemented. The performance of the proposed topology comes out to be good and it satisfies the harmonic limits that is less than 5%.

Giuseppe Carrara et al. [24] described a short conclusive test on a sub-harmonic PWM strategy for multilevel inverters for the triggering of switching pulses. For the high frequency applications, sub-harmonic PWM methods are effective to use. In order to overcome the demerits of pulse generator or any other PWM controller, concept of sub-harmonic control method was introduced for giving better reduced results of THD.

Martina Calais et al. [25] first utilized the multi-carrier control strategy in one phase five level cascaded inverter for the reduction of harmonics. One reference signal is compared with four triangular carrier signals. The researcher carried out the performance of multi-carrier method. The multi-carrier is based on a sinusoidal PWM strategy.

Bhuvaneswari et al. [26] represented multi carrier method being implemented for both symmetrical and asymmetrical cascaded H-bridge multilevel inverter to limit THD. The three different types of multi carrier method were proposed namely level shifted, similar switching frequency, different frequency and phase shifted method were introduced.

Five different multi carrier sinusoidal PWM control strategies namely level shifted based fixed frequency Phase Disposition, Phase Opposition Disposition, Alternate Phase Opposition Disposition multicarrier PWM, Variable frequency and Phase shifted are studied in paper [27]. For the comparative analysis between all these methods of PWM, these are realized in five level cascaded H-bridge inverter.

In order to find the superiority of asymmetrical as well as symmetrical cascaded multilevel inverters, when performed with all the five carrier based PWM strategies, paper [28] presents the comparative test between the two topologies of MLI with all these PWM control methods. The results conclude that asymmetrical inverter gives very less THD.

Paper [29] shows the seventeen level inverter proposed in symmetrical and asymmetrical configuration. Aim was to apply the level shifted, phase shifted and variable frequency based multicarrier PWM methodologies over symmetric and asymmetric inverters. Then a comparison is done between all these methods of PWM on the basis of better performance.

N.G. Hingorani gave the concept of custom power devices [30]. The term introduced as a result of the disturbances in the quality of power which is fed to the consumers. The harmonics in the distribution network are responsible for the poor quality of power. These are present due to the nonlinear loads in the distribution network. Custom power devices refer to the devices that boost the power quality in the distribution network. Custom power devices aim in developing the improved condition of power and to provide accurate power that is delivered to the customers. There are various custom power devices [31] that are DSTATCOM, DVR and UPQC. These are based on different applications for improving the power quality in the distribution system. DSTATCOM is used to enhance the power quality from the current harmonics; DVR is responsible for the reduction of voltage harmonics while UPQC eliminates the effect of both current and voltage harmonics.

Bhim Singh et al. [32] evaluated the three various methods for driving reference source currents of DSTATCOM. The three methods employed are synchronous reference frame theory, instantaneous reactive power and adaline control theory including PI controller used as a control scheme for DSTATCOM.

Parag Nijhawan et al. [33] presented five level cascaded H-bridge multilevel inverter based DSTATCOM for conditioning the power quality of the distribution system feeding nonlinear load. In this research work, two modulation strategies, Phase Disposition and phase shifted multicarrier sinusoidal PWM is incorporated.

Paper [34] presented the power quality improvement by implementation of symmetric 7 level CHB inverter in DSTATCOM. The aim is to eliminate harmonics, unbalancing of load. Here IRP theory is employed for calculating current signals which are the reference.

Performance of DSTATCOM with the photo- voltaic array is shown in the paper [35] in the distribution system to suppress the effect of load harmonics to the source side which causes distractions in the power quality. Here IRP and SRF control theories for DSTATCOM are used.

Satisfaction of harmonics along with reactive power transfer in the distribution system is analyzed in paper [36]. Five level cascaded H-bridge inverter topology is used with DSTATCOM for attaining many levels of voltages.

The guidelines for harmonic control recommended by IEEE 519-1992 standards are mentioned in [37]. The limits of harmonic contents that should be controlled in the power system is mentioned in the guidelines.

CHAPTER – 3

Cascaded H-bridge Multilevel Inverter

3.1 Introduction

These days, modern industries are acquiring power level ranging in megawatt generally for high voltage and power applications. So, it is mandatory to have multiple semiconductor switches that can be connected to the grid of medium voltages. Also, it will enhance power quality if we are using high power and medium voltage devices. Conventional two level voltage source inverter cannot be employed for the high power applications and harmonic distortions we get from this VSC is sufficiently high and it cannot cope up with the problems of power quality. And since it does not produce less stresses of switching devices and many voltage levels, industrialists are preferring multilevel inverters which has overcome the limitations of a simple 2 level converter [38]. The term multilevel inverter indicates the inverter producing three or more than 3 levels of voltages that is + V_{dc} , zero and - V_{dc}[1], [2]. The main advantage of using multilevel inverters is that we can achieve high number of voltage levels and it is true that as the number of levels increase, THD gets reduced as this advantage cannot be achieved in a two level inverter. However, there are different topologies of multilevel inverter and each topology perform in its own fashion and has different methods of producing switching sequences, but there are some challenges that MLI faces offered by its topologies. Like, diode clamped and flying capacitor multilevel inverter, cascaded H-bridge MLI does not use separate dc sources. The concept of using separate dc sources in individual bridges is that achievement of various voltage levels without occurrence of short circuit which can take place with same dc sources [7], [8]. DC-MLI needs so many clamping diodes which make generally the circuit complex. Also. FC-MLI uses capacitors which are known for balancing, cause voltage sag problems. To overcome the limitations of both topologies cascaded H-bridge multilevel inverter had been proposed [3], [4], [5].

By cascaded H-bridge MLI, we mean one or more elements of H-bridge are connected in a series link to produce the desired ac output voltages. These bridges are look – alike of an alphabet ‘H’. H-bridge represents electronic circuit in which voltage is applicable across the load. These H-bridges are mostly used in the dc-ac converters/ power inverters, ac to ac converters etc. this topology is used either for single or three phase. H-bridge consists of switching devices like IGBT or MOSFET along with main diodes which are known as feedback diodes. CHB MLI uses separate dc sources and does not require clamping diodes

and capacitors as needed by DC-MLI and FC-MLI respectively. This topology is quite cheaper than the other two. This is the latest topology among researchers and industrialists or scientists. Its tremendous advantages has attracted everyone. It promises low harmonic content and has excellent features in high power and high voltage applications. CHB-MLI has overcome the disadvantages of DC-MLI and FC-MLI in the sense that number of switching components required in cascaded H-bridge inverter are less compared to the others [7], [8], [10]. So, it reduces the cost. The series connection allows it to achieve high as well as medium voltages and power also [39]. Separate dc voltage sources and H-bridge are the basic blocks for CHB-MLI. Cascading is basically done so that output we obtain is equal to the addition of all individual H-bridges.

The idea for cascaded H-bridge MLI was given by R.H. Baker and L.H. Banister in 1975. Since it has many advantages over other topologies, so it has been gaining importance. This topology is widely used for power quality improvement. The output voltage with respect to the ground is given by the equation:

$$V_{0n} = \sum_{i=1}^{N} Vi \qquad (3.1)$$

where N is the number of H-bridge cells. The above equation is showing the final voltage is equal to the addition of voltage of each H-bridge cell.

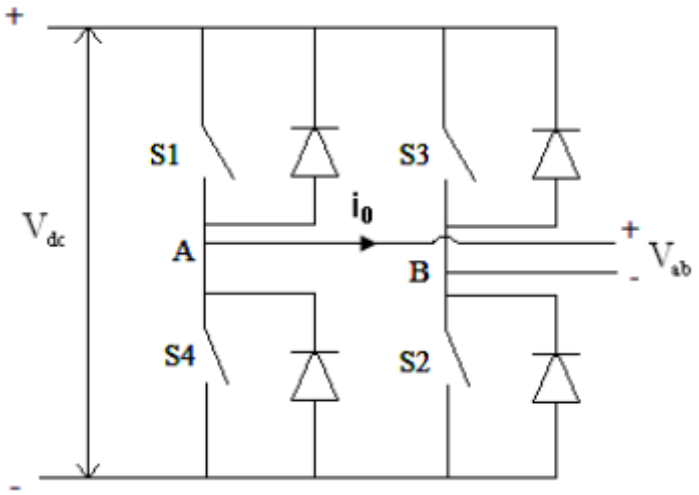


Figure 3.1 Basic Three Level Cascaded H-bridge MLI

The above figure shows the basic single cascaded H-bridge inverter, which is basically three level. Three level is the basic level for each multilevel inverter topology. With one H-bridge, the inverter produces three output voltages that is $+V_{dc}$, zero and - V_{dc}. It will contain 4 switches and four main diodes based on the number of H-bridges. Main diodes are known as feedback diodes as they are meant for feeding back the energy to the source. In cascaded H-

bridge multilevel inverter, the switching components depend on the H-bridges used. Here, V_{dc} is the desired ac output voltage. There are two legs in the circuit. Each leg is having two switching devices. In three level CHB there is only one dc source voltage.

S1 and S2 will generate positive voltages and S3 and S4 generate negative voltages. S4 is the complementary switch of S1 while switch S3 is the complimentary of switch S2. The operation of the inverter takes place during when switch S1 and switch S2 are turned ON, it generates $+V_{dc}$, while switches S3 and S4 are turned ON - V_{dc} voltage whereas zero level is generated when either switch S1 and S3 are ON or switches S4 and S2 are ON. Figure 2.2 shows the output phase voltage of a three level cascaded H-bridge multilevel inverter.

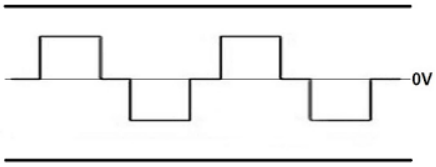


Figure 3.2 Three level output voltage waveform

The total voltage which is phase voltage is equal to the sum of the total H-bridges. In this case, output voltage, $V_{ab} = V_{H1}$

The number of output voltage level also depends on the switching devices required that is;

$$m = N_s + 1 \quad (3.2)$$

where m= number of levels and N_s = number of switches.

Phase to ground voltage is equivalent to m number of levels and line voltage is given by the following equation:

$$V_{ab} = V_{bc} = V_{ac} = 2m\text{-}1 \quad (3.3)$$

The components required in cascaded H-bridge multilevel inverter is summarized below.

Table 3.1 Component requirements in CHB-MLI

Switching devices	(m-1)*2
Main diodes	(m-1)*2
Dc source voltages	$\frac{(m-1)}{2}$
Number of h – bridges	Number of dc source voltage

In the above table, ‘m’ is referring to number of levels.

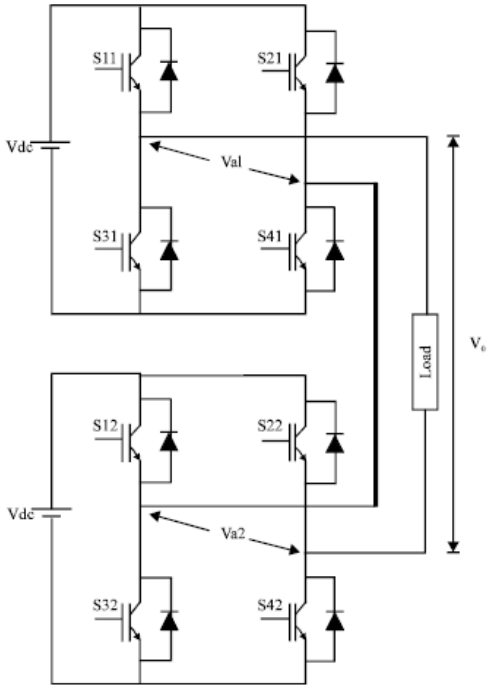


Figure 3.3 Five level CHB-MLI

The above shows the circuit having two H-bridges which is generally five level. Each H-bridge is consisting of four switches giving a total of 8 switching components. Two voltages will be generated in the positive half and rest two will be in the negative half and one zero level makes it a five level means a total of five desired ac output voltages will be achieved. In the same fashion, it also consists of complementary switches. In this case, SDCSs (separate dc sources) are two. The total output voltage is the sum of all the H-bridges. Therefore,

$$V_0 = V_{H1} + V_{H2} \tag{3.4}$$

The operation of a five level CHB MLI takes place when the positive switches of h – bridge 1 $S_{11}$and S_{41} during the positive half cycle generate positive dc voltage and during the negative half cycle switches S_{31} and S_{21} generate negative voltage whereas zero voltage is obtained either when S_{11} and S_{21} or switches S_{31} and S_{41} are ON simultaneously then the power will be zero because no current will flow. In the second H-bridge, switches S_{12} and S_{42} will generate a positive voltage during the positive half cycle and S_{32} , S_{22} will generate negative voltage during the negative half cycle. Zero level will be achieved when both switches S_{12} and S_{22} are turned ON or S_{32} and S_{42} are ON.

The values of output voltage takes place with the combinations of switching sequence as follows:

For $V_0 = \frac{Vdc}{2}$; switches S_{11}, S_{41} will get turned on.

For V_0 = +V_{dc}; switches S_{11} and $S_{41}$from bridge 1 will be on and from bridge 2, S_{12} and S_{42}will get turned on

For V_0 = - $\frac{Vdc}{2}$; switches S_{21} and S_{31} will be on.

For V_0 = -V_{dc}; S_{21} and S_{31} of H-bridge 1 turns on and S_{22} , S_{32} from bridge 2 get turned on.

For V_0 = 0 ; when either switch combinations S_{11} , S_{21} and S_{32} , S_{42} get turned on or S_{31} , S_{41} and S_{12} , S_{22} turned on.

The below figure shows the five levels based on the different switching sequences of the inverter.

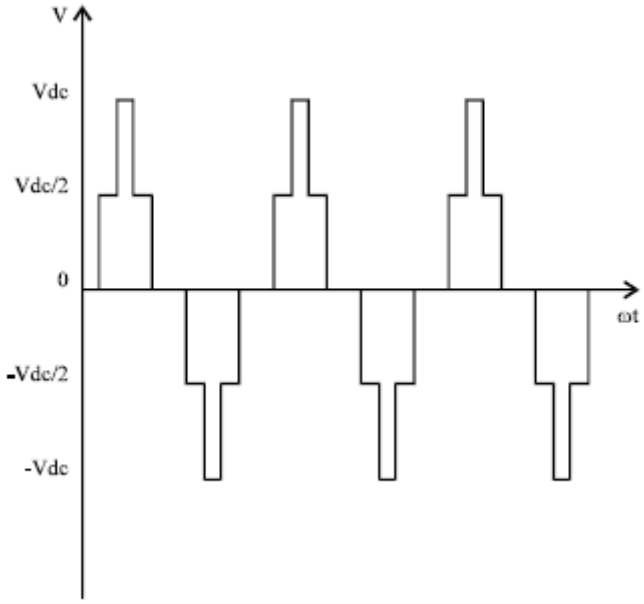


Figure 3.4 Output phase voltage waveform showing five level CHB MLI

3.2 Attributes of Cascaded H-bridge MLI

- It offers cost effectual solution. As the number of switching devices required are low in comparison to the other two topologies of multilevel inverter. In cascaded H-bridge, dc source voltages required are according to the factor $\frac{m-1}{2}$ whereas in diode clamped and flying capacitor multilevel inverter the dc source voltages are chosen according to the equation (m-1) where m is the voltage levels. We can say that this factor varies a lot in these two topologies which makes the cost of the system ineffective. For example, if the number of levels, m = 7 and for this voltage level we require number of dc source voltages 3 and in case of other two topologies, it would be 6. Hence, the number of component requirement is less in CHB MLI.
- It can be used at both 50 hertz frequency and high frequency as well.

- The waveform which we get from CHB MLI is somewhat similar to the sinusoidal waveform which means low harmonic contents.
- The structure of cascaded H-bridge multilevel inverter is simple in comparison to the DC and FC MLI.
- As the number of levels increase, harmonics get reduced.
- We can use low ratings of switching devices.
- Separate dc sources (SDCSs) are used for conversion of power from ac-dc and vice versa.
- Power factor is nearly equal to unity.
- No requirement of the circuits for matching of voltages of switching components.

3.3 Advantages of Cascaded H- bridge Multilevel Inverter

- It gives lower common – mode voltage resulting in the reduction of stresses in the motor drives.
- It suppresses the voltage stress problems and resulting in very low electromagnetic interfaces.
- It does not require clamping diodes, balancing capacitors, transformers that are bulky which makes the inverter complex.
- It produces low switching losses especially in high power drives and offers the system a low THD.
- Least number of components are requires in CHBMLI thereby reducing the cost.
- It has overcome the limitations of diode clamped and flying capacitor multilevel inverter.

3.4Applications of Cascaded H- bridge multilevel inverter

- The topology is widely used in high power ranging from 0.2- 40 MW and medium voltage applications (2.3 – 13.8 kV).
- Best suited for the use in medium distribution networks to eliminate harmonics that are feeding non- linear loads which result in high harmonic content.
- It can be used in FACT's devices or custom power devices.
- Useful in plug in hybrid vehicles, HVDC power transmission network, uninterruptible power supplies
- Utilized in dc power sources, air conditioners.

- Without the use of clamping diodes, cascaded H-bridge inverters are best suitable for motor drive applications that uses high power and so many clamping diodes.

3.5 Limitations of CHBMLI

- The only limitation of cascaded H-bridge multilevel inverter is that it needs so many number of separate dc sources (SDCSs).

3.6 Classification of Cascaded H- Bridge Multilevel Inverter

There are two types of CHB MLI. These are shown below.

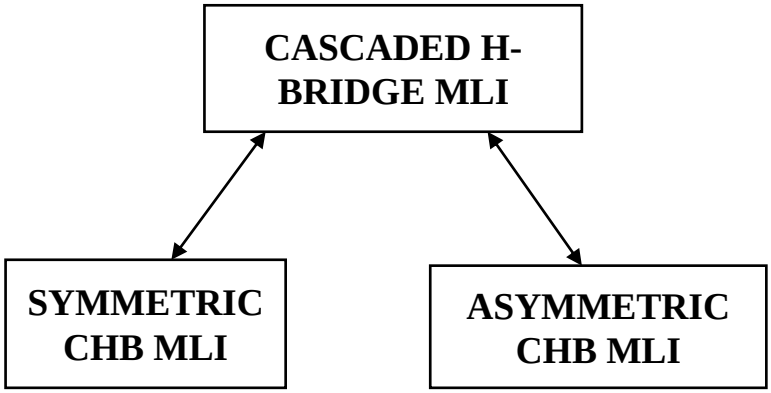


Figure 3.5 Block diagram showing types of cascaded H-bridge MLI

Table 3.2 Comparison between symmetric and asymmetric CHB MLI

SYMMETRIC	ASYMMETRIC
• The configuration having equal dc source voltages is known as symmetric CHB.	• The inverter uses unequal separate dc sources.
• Dc source voltages are increased as number of levels get increased.	• Here dc source voltages depend upon the different voltage generation methods used in asymmetric topology.
• More number of components required compared to asymmetric converter.	• For the same number of levels, least number of components are needed.
• Cost of the switching devices is more.	• In contrast to this, cost is reducible.
• Higher switching losses compared to asymmetric.	• Lower switching losses and reduced dv/dt stresses.
• THD content is more.	• With asymmetric configuration, we achieve lower harmonic contents and with increased efficiency and ripples get reduced.

Table 3.3Component requirement in symmetric and asymmetric CHB MLI

	Symmetric	**Asymmetric**			
		Binary	Ternary	Fifnary	Two equal and one unequal SDCSs
m levels	2N+1	2^{N+1}-1	3^N	5^N	m
DC sources	N	N	N	N	N
No. of switches	4N	4N	4N	4N	4N
V_0max (PU)	N	2^N-1	$3^N - 1/2$	$5^N - 1 /2$	$(m-1)/2$

The above table shows the switching components, number of dc sources, voltage levels and maximum output voltage for both symmetric and asymmetric cascaded H-bridge multilevel inverter. Binary, ternary, fifnary, unnatural sequence of the numbers represent the different methods of selecting dc voltages used in the asymmetrical topology. Here 'm' is representing the number of voltage levels, 'N' is the number of H-bridges used in the inverter. V_0 represents the upper half voltages generated during positive cycle and it also represents the same for negative half cycle voltages. Number of H-bridges depend on the type of voltage generation methods in asymmetric inverter which uses less bridge cells when compared to the symmetric inverter thus reflecting the plus point over symmetric configuration. The topology selected in this thesis work is asymmetrical cascaded H-bridge multilevel inverter. The main focus and interest was on this topology of CHB-MLI during the work.

3.7 ASYMMETRICAL CASCADED H- BRIDGE MLI

These multilevel inverters are those having unequal voltage magnitude [11], [12]. The values of dc source voltages are not symmetric. For providing large number of output voltage levels without using so many number of components, asymmetrical inverters are preferred. Asymmetrical inverters were first successfully realized by Farid Khoucha et.al. (2010) In his research he observed that for the same number of levels, the number of switching components, dc source voltages, number of H-bridge units are very less in asymmetric when compared to symmetric. So, this is the limitations of symmetric inverters. These are overcome by asymmetric inverters. Since then, asymmetric inverters are in a great demand these days. By using this topology, the cost is effectively reduced. With fewer number of components, we can get reduced THD. Javad Ebrahimi et al. (2013) presented different methods for calculating the dc voltage magnitudes based on this one can get to know about component requirements, number of H-bridges. With unequal dc voltage sources we can

achieve more number of levels. Asymmetric inverters ensures lesser components. The main disadvantage of cascaded H-bridge MLI and even in symmetric inverters is that they use so many separate dc sources which is the main limitations of cascaded H-bridge MLI. This disadvantage of SDCSs has been eliminated in asymmetric configuration of the inverter. Asymmetric inverters are known to be topology with reduced number of switches.

There are different methods used for calculating the magnitude of dc voltages (Javad Ehbrahimi et al., 2013).These are binary, ternary, fifnary, quasi linear, two equal and one unequal voltage sources which is usually unnatural way of sequences of numbers. These methods are based on the unequal values of dc voltage magnitudes. These methods are used for determination of values of dc source voltages. Based on these methods, we can select the values of voltages for the realization of asymmetric inverters in any level. These methods are applicable to symmetric inverters. Binary, ternary, fifnary methods use geometric progression with a factor of two, three, five respectively. These methods can be implemented in any level of voltages. Seven level is the basic recommended units for binary method whereas three and five level are the basic units for ternary and fifnary respectively. However, we can also use these methods in cascaded sub multilevel cells (i.e. levels 11, 13,17,25,29 etc.) for choosing dc voltage source values. If any extra switches are added to the basic unit then the converter is known as cascaded sub multilevel cells. Using the arrangement of dc sources by keeping two voltages in symmetric and one in asymmetric manner, can be used for realizing any level. In this thesis, binary method and the arrangement of having two identical voltages with one unequal voltage for selecting the values of dc voltage sources have been used for the realization of different levels of asymmetric inverter.

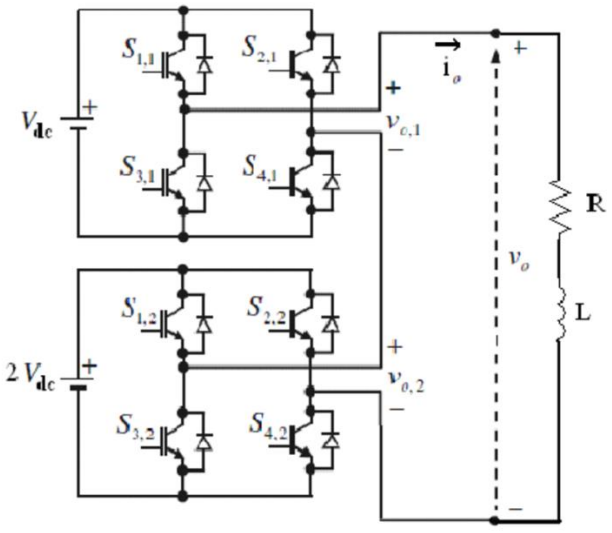


Figure 3.6 Asymmetrical Cascaded H-bridge multilevel inverter

Figure 3.6 shows the configuration of asymmetric cascaded H-bridge multilevel inverter having RL load. It shows the series connection of single phase inverters that are having their own dc source voltages. It consists of two H-bridges. Based on this, two unequal dc voltage sources are used. The magnitude of dc source voltages can be selected from any method of voltage generation. We can see here that voltage of first H-bridge is $1V_{dc}$ and second bridge is having 2 V_{dc} which are unequal in magnitudes. Since, the number of H-bridges is 2, the switching components as well as the main diodes are 8. If the H-bridge is feeding voltage as 1 volts and another H-bridge is having voltage magnitude of 2 volts then the ratio of these voltages varies as 1:2 ratio which is known as binary method. In ternary method voltage ratio varies as 1:3 ratio whereas in fifnary method ratio will vary as 1:5.

In the above figure, we will get $+1V_{dc}$ when the switches $S_{1,1}$ and $S_{4,1}$ are turned on. Switches $S_{1,2}$ and $S_{2,2}$ are also turned on in this case and rest of the switches or turned to be in off state. $+2V_{dc}$ is achieved when $S_{1,2}$ and $S_{4,2}$ are in on condition and $S_{1,1}$,$S_{2,1}$ are also in working condition. For getting $+3V_{dc}$,$S_{1,2}$,$S_{4,2}$ and $S_{1,1}$, $S_{4,1}$ are turned on. These are the positive voltage levels in the first half cycle. During negative half cycle, switches $S_{2,1}$ and $S_{3,1}$ from first bridge get turned on and simultaneously from the second bridge, $S_{1,2}$ and $S_{4,2}$ are switched on and it gives -1 V_{dc}. -2 V_{dc} is generated by turning on the switches $S_{3,2}$ and $S_{2,2}$ while from bridge one either switching pairs $S_{1,1}$, $S_{2,1}$ are switched on or pair $S_{3,1}$, $S_{4,1}$ are turned on. $S_{2,1}$, $S_{3,1}$, $S_{2,2}$ and $S_{3,2}$ are all turned on for producing -3 V_{dc}. Zero level is produced when either $S_{1,1}$ and $S_{2,1}$ from H-bridge one and $S_{3,2}$, $S_{4,2}$ from bridge 2 are turned on or switches in the first bridge $S_{3,1}$, $S_{4,1}$ and switches in the second bridge that is $S_{1,2}$,$S_{2,2}$ are on. We will achieve total of 7 levels; three in the upper half cycle and three in the lower half cycle and one is the zero level thus making it a seven level.

3.7.1 Need of asymmetrical cascaded h- bridge multilevel inverter

- Larger number of voltage levels with the same number of h- bridges as in symmetric inverters can be obtained by using asymmetric CHB MLI. For instance, if we have to produce five voltage levels in symmetric inverter, we need two h- bridges and eight IGBT and 8 main diodes and for the same number of H-bridges, IGBT and main diodes, we can produce 7 levels, 9 levels in asymmetric cascaded H-bridge inverter based on the generation of dc voltage methods. In other words, we can say that with the same number of components we can produce high number of voltage levels. And as we increase the number of levels, THD reduces. Asymmetric inverters are

considered to be efficient in reducing harmonic content as compared to the symmetric inverters.

- Since, symmetric inverters require more number of components as we increase the number of levels one by one. As a result, for higher number of levels, the cost of the components gets increased. This problem is reduced in ACHBMLI. No matter, how many number of levels are there in asymmetric inverter, cost of the switching devices decreases.
- Sometimes, extra filter circuits are required for minimization of harmonics in symmetric CHB MLI, but these are not needed by the asymmetric inverters.
- We get more sinusoidal output voltage waveform with asymmetric topology which is advantageous for dealing with power quality problems.
- This is mandatory in CHB MLIs to increase the number of levels for achieving very low distortions but when number of levels get increased, simultaneously SDCS also increases and more number of SDCS causes somewhat complex arrangement of the circuit because more number of devices in the arrangement would lead to the logic circuit more complex. This problem has been resolved in ACHBMLI. There we require sufficiently least amount of SDCS. So that is why ACHBMLI is being preferred.
- Lesser number of components will result in a reduced switching losses and low voltage stresses. This benefit is achieved in asymmetric inverters having high efficiency.
- The main aim of using asymmetric CHB MLI is to achieve more number of output voltage levels with sufficiently reduced number of components. With using unequal dc voltages can lead to better output quality.
- For these reasons, asymmetric inverters are preferred in high voltage and power applications.

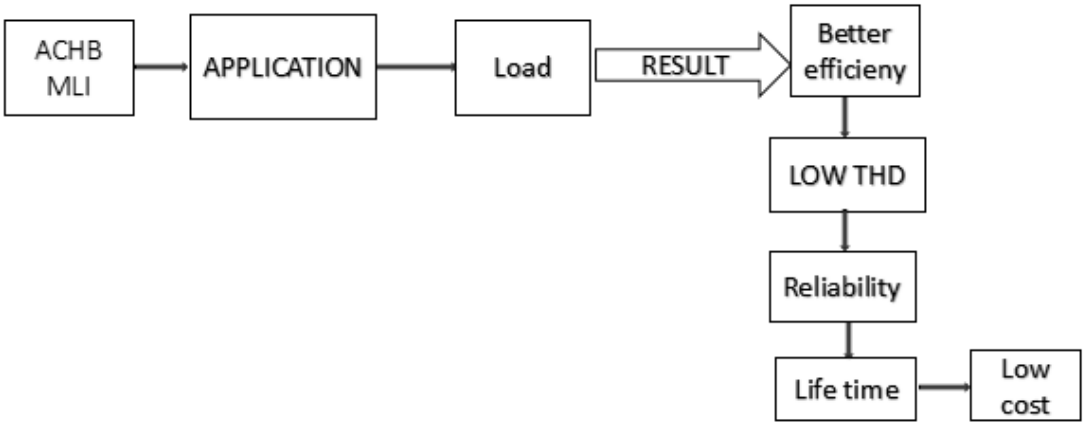


Figure 3.7 Block diagram showing the performances of ACHBMLI

3.7.2 Binary method for arrangement of dc sources

The method is based on the calculating of magnitude of un-identical dc source voltages [12], [13]. In this method, the voltage sources of dc are in the ratio 1:2:4:8….and so on. Means, if there are two H-bridges in the inverter then the ratio of two dc voltage sources should be 1:2 ratio. Binary means a factor of two. The value of dc source voltages are chosen in accordance to the geometric progression by a factor of 2. Binary method can be applicable to the cascaded sub-multilevel cells. This method uses less number of components and aims at producing many number of voltage levels thus giving good modularity. It offers flexibility to the multilevel inverter.

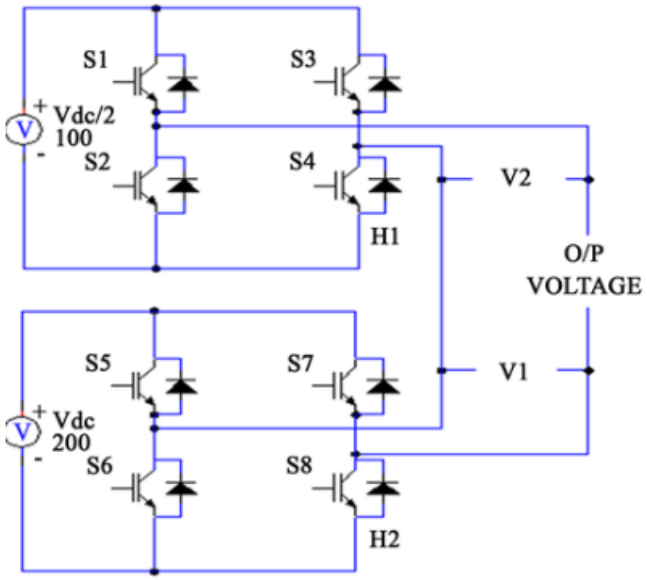


Figure 3.8 Example of binary asymmetrical cascaded H-bridge multilevel inverter

The above figure shows the basic circuitry arrangement for a single phase binary based asymmetric cascaded H-bridge multilevel inverter consisting of two H-bridges and two SDCS which is in binary arrangement with four switching devices and main diodes. The ac

output is cascaded means connected in series so as to obtain the desired voltage waveform of ac which is equal to the addition of the voltages of both H-bridges. It gives synthesized stepped ac output voltage waveform. The ratio of two dc source voltages is 1:2 (or it can be ratio of 100 volts to 200 volts).V_1 represents the output voltage of H-bridge cell 1 while V_2 is the output voltage of H-bridge cell 2. V_0 is the output voltage of binary asymmetric cascaded H-bridge inverter. V_0 is equal to the sum of the voltages of two H-bridge units.

$$V_0 = V_1 + V_2 \quad (3.5)$$

With two separate dc source voltages having ratio 1:2 (with values $V_{dc}$and $2V_{dc}$ or $V_{dc}/2$ and V_{dc}) produces 7 level of voltages that is $3V_{dc}$, $2V_{dc}$, V_{dc}, 0 -$3V_{dc}$, -$2V_{dc}$, -$1V_{dc}$. Using three dc source voltages with ratio 1:2:4 it synthesizes 15 output levels and with 4 H-bridges 31 levels of output voltages will be produced. The basic recommended level for binary based method is seven levels of voltages.

The value of magnitude of dc source voltages in binary based asymmetric multi -level inverter is estimated according to the following equation:

$$V_i = 2^{(i-1)}V_{dc}, \text{ i= 1,2,……,N} \quad (3.6)$$

Using these dc sources, we can obtain any number of output voltage levels. The number of switching devices (S), number of output phase voltage levels (m), and maximum output voltage ($V_{0\,max}$) in terms of H-bridges are obtained from the following equations respectively:

$$S = 4N \quad (3.7)$$

$$m = 2^{(N+1)} - 1 \quad (3.8)$$

$$V_{0\,max} = (2^N - 1)\, V_{dc} \quad (3.9)$$

Number of line to line voltages can be written as:

$$V_{l-l} = 2m-1 \quad (3.10)$$

3.7.3 DC voltage arrangement with two equal and one non- equal SDCS

This method uses the arrangement in which separate dc voltage sources of any two inverters are kept similar to each other and the voltage source of the other bridge units is taken to be different from the others making asymmetrical structure of the inverter (Javad Ebrahimi et al.,2013) In other words, we can say that two voltages are in symmetric arrangement and one is in asymmetric with the other two. In this arrangement number of H-bridges are taken to be three. Based on this arrangement we can generate any voltage levels. The arrangement can be

in unnatural form of sequence of numbers. We can achieve high number of levels as well using this unique arrangement.

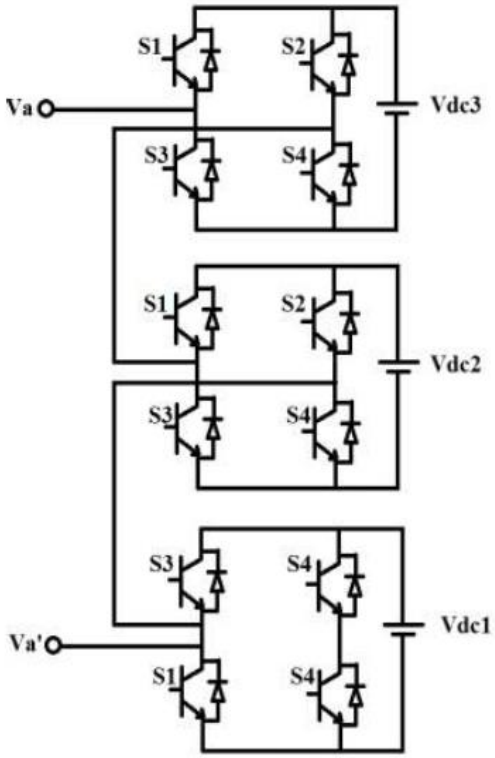


Figure 3.9 Asymmetrical arrangement with three SDCSs

The above figure representing the basic circuit of asymmetric arrangement of unequal voltages. There are three separate dc source voltages with 12 IGBT or MOSFET's with twelve main diodes. The magnitude of dc source voltage of first H-bridge and third H-bridge can be similar to each other but different to the voltage of second H-bridge unit. Or, it can be like this that dc voltages of second and third H-bridge units are equal to each other and the value in the first bridge cell is different from the others. The output voltage of this inverter is the sum of voltages of all H –bridges;

$$V_0 = V_{dc1} + V_{dc2} + V_{dc3} \quad (3.11)$$

The magnitude of dc source voltages can be written in the following way:

$$V_i = V_{i+2} \neq V_{i+1} \text{ ; where i = 1} \quad (3.12)$$

Or, it can be written in another form also that is:

$$V_i \neq V_{i+2} = V_{i+1} \text{ ; where i =1} \quad (3.13)$$

Number of output phase voltages obtained is equal to the "m" no. of levels.

Number of line voltages is given by:

$$V_{l-l} = 2m\text{-}1; \text{ where m is the number of levels} \quad (3.14)$$

Number of switches requirement are calculated by the following equation:

S_w = 4N ; where N is the number of H-bridges. (3.15)

Number of dc sources required depend on the no. of H-bridges of the inverter and is equivalent to the:

SDCSs = N ; N represents the total number of bridges used in the asymmetric inverter.

3.7.4 Advantages of Asymmetrical Cascaded h- bridge MLI

- Reduces voltage imbalance problems and requirement of long cables by employing less number of dc source voltages and H-bridges required by the inverters.
- Using unequal voltages, higher number of voltage levels with reduced number of components and same number of h- bridges of the inverter can be achieved that is not possible in symmetric multilevel inverters that uses equal dc source voltages.
- Has overcome the limitations of symmetric MLI which reduces too many separate dc sources.
- Reduces the cost of the switching devices complexity of the inverter and harmonic contents.

3.8 Control Strategy for Asymmetrical MLI

Control strategies refer to the different PWM switching techniques that are used to generate the switching pulses. The switching devices which we often use in the converter are triggered using PWM strategy. PWM methods acts like a controller for multi-level inverters as these control the desired ac output voltage. The ON and OFF states or periods of switches of the inverter are adjusted by different PWM strategies. The aim of PWM techniques is to provide the desired waveform with having no harmonics and is nearly sinusoidal. Control strategy is the systematic series of switching operation of the power electronic devices. For getting the output voltage or current waveforms of the inverter, it is mandatory to induce the final switching signals that are prompted by PWM methods. The control of the various switches is all done by PWM. So, that's why we need control strategies. Control techniques also aim at keeping voltage sources to be balanced.

There are various control strategies for elimination of THD which we could not achieve from a simple pulse generator that contains so many harmonics. PWM techniques are classified according to the high switching frequency and fundamental frequency (Jose Rodriguez et al., 2007). Multi-carrier based sinusoidal PWM is the latest approach which can be preferable for the industrial purposes [24], [40]. These are applicable for high power applications. These are effective in reducing harmonics as produced by non - linear loads in the distribution network and thereby high efficiency is achieved.

3.8.1MULTI-CARRIER SINUSOIDAL PWM STRATEGY

Multi – carrier refers to the control strategy of PWM that uses more than one carrier. If the carrier is one then it is said to be single carrier based SPWM which is normally used for generating two levels of voltages. This PWM method is known as triangulation method. Carriers are in triangular shaped. Now-a-days, this type of techniques has been in a great demand. Since, there are many PWM strategies that are not applicable to the high power applications. So, in order to deal with the problem, multicarrier based SPWM is usually preferred over other strategies. These are effective in reducing switching losses and harmonic contents. This PWM is also known as sub-harmonic or sub-oscillation method (Carrara et al., 1992).

This strategy uses (m-1) carriers for m-levels for producing the desired multilevel inverter ac output voltages. Triangular shaped carriers are compared with the sinusoidal signal the sinusoidal signal is the reference wave switching instants are determined when the sinusoidal wave intersects carrier wave. This method of PWM is based on the comparison between triangular waves and sinusoidal signals. For any level m, $\frac{m-1}{2}$ carrier signals are given or applied across the positive half cycle and rest $\frac{m-1}{2}$ waves are given during the negative half cycle. When the sinusoidal wave is more than the carrier signal then there are positive voltages levels generated. And $\frac{m-1}{2}$ carriers are generated above the reference levels. When the carrier signal is more than the sinusoidal signal, negative voltage levels are generated. Pulses are generated for positive half cycles. $\frac{m-1}{2}$ carriers are produced below the reference level which means negative carriers of $\frac{m-1}{2}$ levels are generated below the zero level. Pulses will be generated for negative cycle. Frequency of carrier signal is taken to be high.

Each leg of the inverter consists of one positive switch and one negative switch. For generating positive pulses in the output, positive switch is controlled by the comparator signal which is usually meant for comparison of reference and sinusoidal signals and corresponding to the other switch which is complementary of the first switch is controlled by 'NOT GATE' which is known as inverting signal in the logic circuit of multicarrier PWM. Negative pulses in the output will be generated during negative half cycle. Width of the pulses is directly proportional to the magnitude of sine wave. The control circuit of the PWM technique is very simple as compared to the other strategies of PWM which are having quite complex structure. m-levels of carriers are produced in the waveform by taking m-1 carriers in the logic circuit.

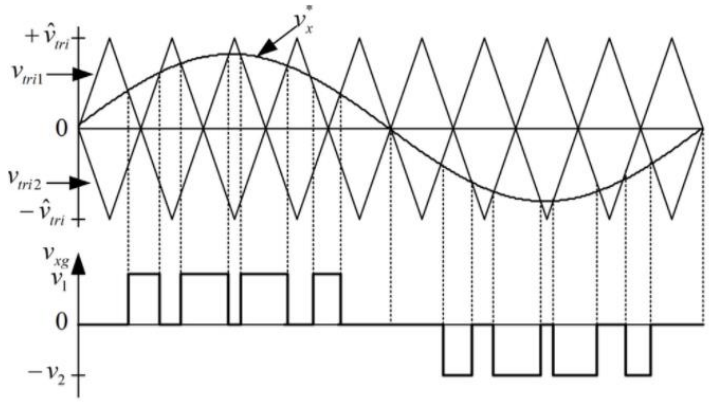


Figure 3.10 Multicarrier Sinusoidal PWM

Figure 3.10 shows the reference and carrier signals. There are two triangular carriers, so it is obvious that it will produce 3 levels of carriers and voltages. These two carriers are compared with the reference signal which is sine wave. Positive pulses will be generated when amplitude of sine wave is greater than amplitude of triangular wave. Active devices will be switched ON. Corresponding to the carrier, positive voltage level is generated. When sine wave is less than the carrier waves, negative pulses are generated. In this case, the magnitude of sine wave has become negative and magnitude of carrier wave becomes positive. So, pulses are generated for negative half cycle. Switches will conduct in the lower half cycle and the switching pulses are produced in the lower sequence.

Frequency of the sinusoidal signal is 50 Hertz whereas frequency of carrier waves are usually taken as 1 kHz or more. Usually, in this method amplitude of carriers are equal having identical frequency. The modulation index in the carrier based PWM refers to the ratio of amplitude of the reference waveform to the carrier signal amplitude.

$$m_a = \frac{Am}{Ac} \tag{3.16}$$

where m_a is amplitude modulation index; A_m is the amplitude of sine wave and $A_c$is the amplitude of carrier signal.

For different types of multi-carrier PWM method, the above equation of modulation ratio varies. The value of modulation index lies between 0 and 1. If this value exceeds 1 then there is the occurrence of over-modulation which means the desired output waveform is just like a square wave as in the case of a 2 level inverter. The shape of the waveform remains no longer sinusoidal.

The reference signal frequency (f_m) indicates the output fundamental frequency that is 50 Hz. The carrier frequency (f_c) indicates number of pulses for particular switch per one cycle. The ratio of carrier frequency (f_c)to the reference wave frequency (f_m) is called frequency ratio.

$$M_f = \frac{fc}{fm} \tag{3.17}$$

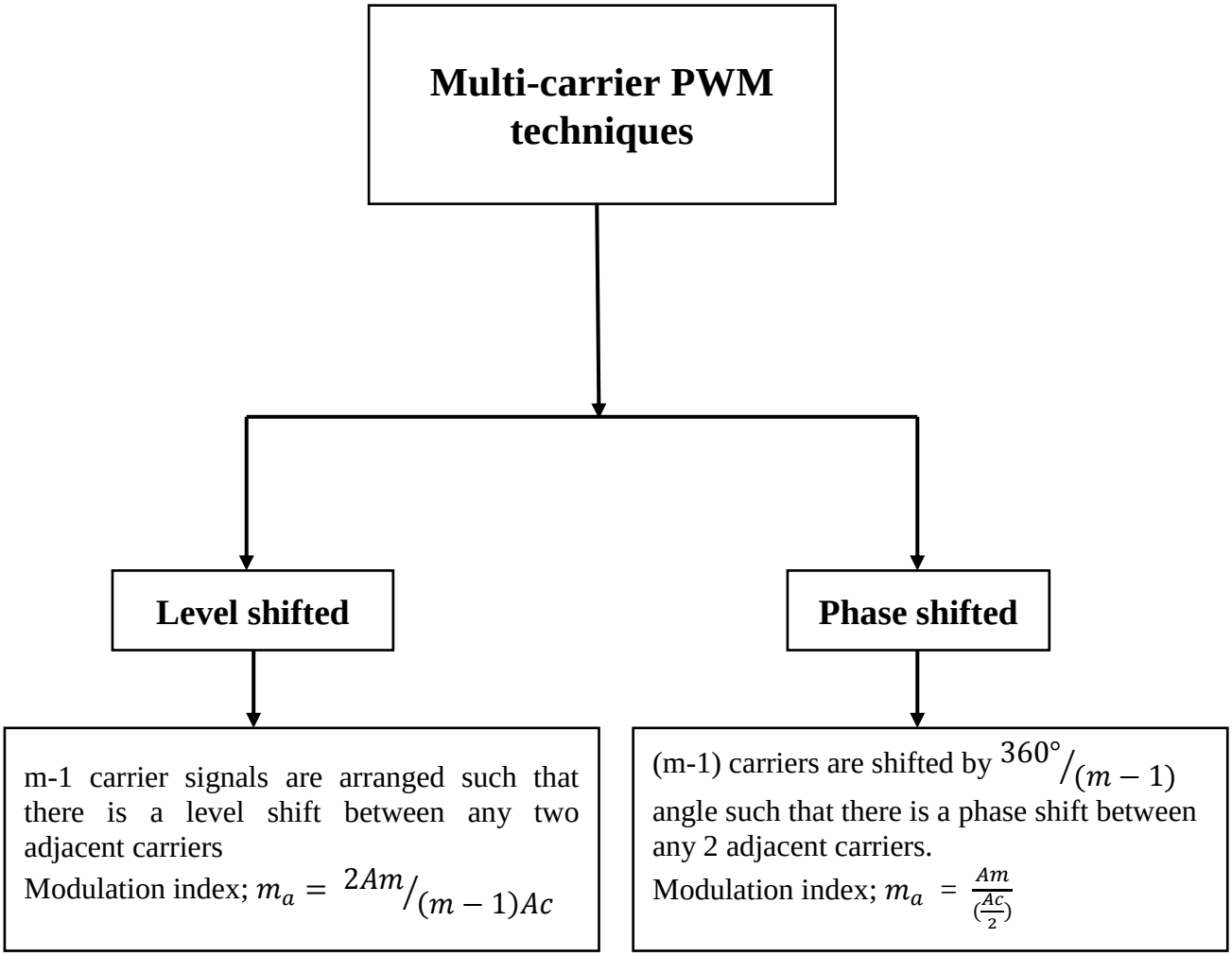


Figure3.11 Block diagram showing various multi-carrier PWM methods

3.8.1.1 Advantages of multi-carrier sinusoidal PWM

- Best suited in high frequency applications.
- Reduces switching losses.
- Can be implemented in FACTS or custom power devices for reactive power compensation and power quality improvement by ensuring load voltages or currents to be balanced and reducing the harmonics.
- Logic circuit is simple and its design is flexible.
- For a single 50 Hz frequency, the switching devices have so many commutations which creates complications. This strategy has overcome this limitation as we can use switches with many carrier frequencies which are greater than fundamental frequency.
- Since this modulation strategy uses high switching frequency which gives low harmonic contents.

3.8.2 LEVEL SHIFTED MULTI-CARRIER SPWM

Known to be a famous multi-carrier sinusoidal based PWM strategy. For m-level inverter, (m-1) carriers are arranged in a manner that the bands they are holding should be persistent or continual. This PWM uses same frequency and amplitude of triangular signal as well. As it is a multi-carrier based strategy, comparison between reference signal and carrier wave is done. This technique is better than phase-shifted MC-PWM in the way that it provides better quality of voltage with reduced harmonic contents and switching losses. That's why this category of PWM has been given a great importance.

3.8.3 Classification of Level shifted MC-SPWM

It consists of three types with same frequency and amplitude of carrier and sinusoidal signal.

- **PHASE DISPOSITION:** (m-1) carriers are organized in such a way that every carrier is in phase.
- **PHASE OPPOSITION DISPOSITION:** (m-1) carriers are organized in such a manner that $\frac{m-1}{2}$ carriers above the zero reference are in phase with each other and are 180° opposite to the rest of $\frac{m-1}{2}$ carriers which are below the reference value.
- **ALTERNATE PHASE OPPOSITION DISPOSITION:** Here (m-1) carriers are disposed such that each carrier is 180° out of phase to its neighboring carriers or adjacent carriers.

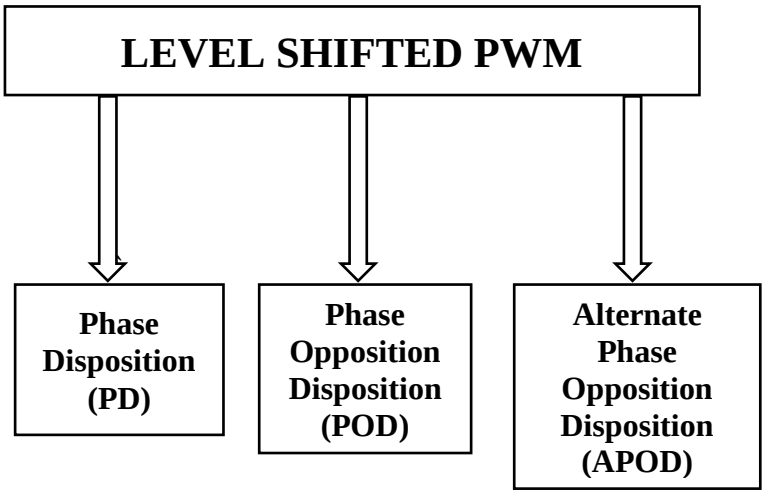


Figure 3.12 Block diagram showing different level shifted PWM methods

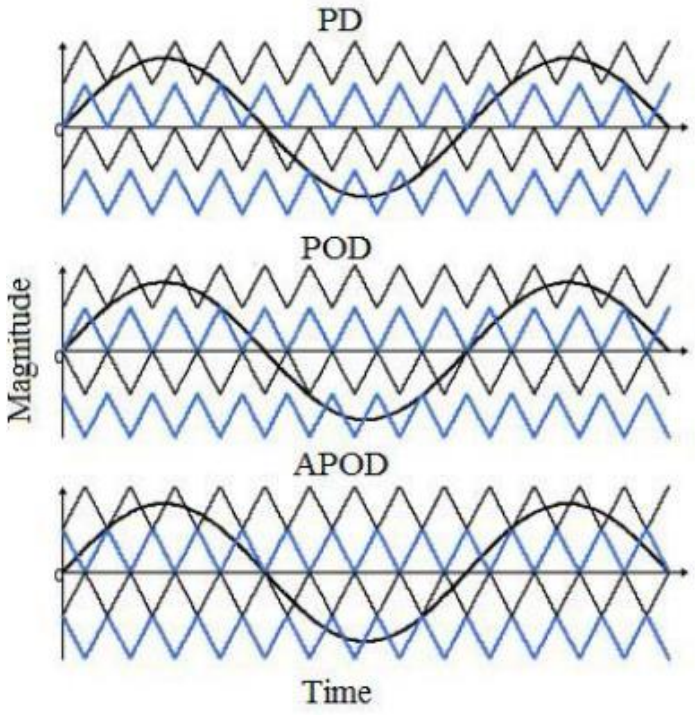


Figure 3.13 Reference and carrier arrangement for three types of level shifted PWM

The above figure shows the carrier arrangement for phase disposition, phase opposition disposition and alternate phase opposition disposition level shifted PWM.

In this thesis work, the main stress is given to Alternate Phase Opposition Disposition (APOD) PWM strategy with using same frequency and amplitude of carriers and reference signal for the desired output waveforms of MLI.

APOD is discussed in detail in the next section.

3.8.4 ALTERNATE PHASE OPPOSITION DISPOSITION PWM TECHNIQUE:

One of the popular multi-carrier level shifted PWM strategies for triggering of switching pulses for producing different voltage levels which are usually in sinusoidal shape. The technique uses m-1 carriers for the generation of 'm' levels of carrier arrangements. This is based on the identical switching frequency. The carriers are organized in a manner that each carrier is 180° opposite to its adjacent carrier in both the reference levels.

During the first half cycle or upper half cycle, the inverter gives positive voltages when the reference signal is more than carrier wave and the switching device corresponding to the triangular carrier and first leg of the inverter gets turned on and in contrary to this, if the reference wave is less than carrier wave, the inverter produces negative voltage and complementary switch gets activated. Whenever positive switch gets turned off, it means its complementary switch is on during that condition.

During the second half cycle, which refers to the lower half cycle in which magnitude of sine wave becomes negative and magnitude of carrier wave is positive. In this case, pulses will be generated for negative half cycle. Sinusoidal wave is less than reference signal so switch corresponding to the triangular wave and another leg of the inverter gets in active mode. In lower half cycle, when magnitude of the reference wave is more than sine wave, complementary switch of leg 2 of the inverter comes in active state.

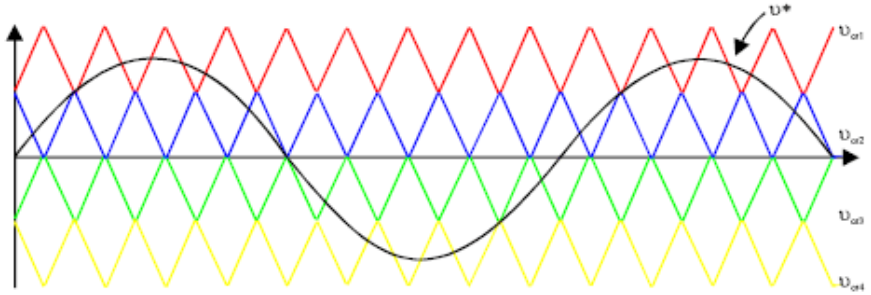


Figure 3.14 Example of Alternate phase opposition disposition reference-carrier diagram

Figure 3.14 shows four carriers needed for producing five voltage levels. v_{cr1}, v_{cr2}, v_{cr3} and v_{cr4} are the peak amplitudes of four triangular carriers. v^* is the amplitude of sinusoidal wave. Here sinusoidal signal is compared with carrier signal and based on this generation of switching pulses in positive and negative half cycles is decided.

3.8.4.1 Advantages of APOD

- Able to produce better quality of voltage waveform which achieves almost sinusoidal shape and gives less THD for line voltages compared to PD and POD.
- Effective to be used in the closed loop configuration of custom power devices like DSTATCOM where closed loop PWM strategies like hysteresis current control, linear current control method etc. which are limited to be performed up to some power level. APOD PWM gives better performance in eliminating harmonics.
- Control algorithm of APOD PWM is simple whereas algorithm of closed loop PWM methods is complex.

3.9 Simulation study of Asymmetrical CHB-MLI

In this work, performance analysis of three phase asymmetrical cascaded H-bridge multilevel voltage source inverters has been carried out. For this, different levels of asymmetric CHB MLI are realized in MATLAB software. Simulation of 7 level, 9 level, 11 level and 13 level is modeled in the software. A comparative analysis has been done between these different levels on the basis of their THD levels and as the number of levels are increased harmonic content should also get reduced and more the sinusoidal waveform is achieved. These four

levels of inverter are realized based on the un-identical magnitudes of dc voltage sources with IGBT switches. For this, two methods of arrangement of dc sources are used. For implementation of 7 level, binary based method is used for calculating the magnitude of dc source voltage. Two unequal dc voltages are taken. The binary method is based on the ratios of dc source voltages 1:2 which has already been explained above. Accordingly, the equations for determination of number of components to be taken are used in realizing 7 levels. For realization of 9 level, dc source voltages are taken in such a manner that voltage of first H-bridge and source voltage of third H-bridge are identical to each other but the value of second H-bridge voltage is different. Total three H-bridges are used. 11 level is implemented using binary method and it is cascaded sub-cell unit. So, binary method is applicable. Here three H-bridges are used and the values of magnitudes of all the three voltages are in the ratios of 1:2:4. Thirteen level is implemented again with the same dc source voltage arrangement manner as in case of 9 levels. Here also three dc source voltages are used; two voltages are symmetric to each other but third one is asymmetric to the other two voltages. So, in this simulation work, two levels are based on the binary method which is 7 and 11 which are implemented on the same method and whereas 9 and 13 uses same method of dc voltage selection. Block diagram of these methods are already explained in sections 2.6.2 and 2.6.3 respectively. The control strategy used for generation of switching pulses for the desired output voltage waveform is Alternate Phase Opposition Disposition (APOD) PWM technique which is based on the comparison of sinusoidal signal with the carrier wave. This method controls the switching of multilevel inverter. For generating the carrier arrangements for voltage levels, (m-1) carriers are required for every level. The objective of using APOD strategy is to achieve less harmonics. Carrier and reference frequency is taken same in each level. Reference frequency of each level is 50 Hz while carrier signal frequency is taken as 5 kHz for all levels. Simulation results for 7, 9, 11, 13 levels are carried out THD of each level are observed.

3.9.1 Simulation parameters of different levels of Asymmetrical CHB-MLI

The system parameters for different levels are listed below in the table.

Table 3.4 Parameters of the Simulink model

LEVELS	SYSTEM PARAMETERS						
	DC Voltages (Volts)			Reference frequency (Hz)	Carrier frequency (kHz)	Load resistance (ohms)	Load inductance (mH)
	V_{dc1}	V_{dc2}	V_{dc3}				
7	100	200	---	50	5	1	3
9	100	200	100	50	5	1	3
11	100	200	400	50	5	1	3
13	100	400	100	50	5	1	3

Table 3.5 shows the requirement for switching components and number of H-bridges and dc sources used in the different levels of inverter

Table 3.5 Component requirements in different levels

LEVELS	NUMBER OF H-BRIDGES	NUMBER OF SDCSs	NUMBER OF IGBT	MAIN DIODES
7	2	2	8	8
9	3	3	12	12
11	3	3	12	12
13	3	3	12	12

3.9.2 Simulink model of APOD logic circuit

Figure 3.15 is showing the model for logic circuit of APOD which generates the gate pulses for the respective levels. This model is shown for the seven level with six carriers. In 7 level we have total of two H-bridges and eight switches. Here out of six carriers, first three carriers indicate positive switches of two H-bridges and next three carriers indicate for the negative switches of the two h –bridges. The first three carriers are merged with one XOR gate and the next three carriers are merged with another XOR gates. From both the XOR gates we take total eight switching pulses that creates seven levels in the output voltages for particular one phase. Different pulses are assembled with these two XOR gates for the generation of accurate signals. Likewise, we achieve seven levels for the other phases also. So, similar procedure follow for other levels also. The only difference occurs in the number of carriers and switches used. NOT gate is representing the inverting signal for the complementary

switches. Relational operator is used for comparison between sine signal and carrier signal. (m-1) relational operators are used for m levels. During upper half cycle, switch pairs from one leg of the first H-bridge and another pair from another leg of second bridge are given to the control circuit. Each leg has one positive and negative switch. In the same fashion, during lower sequence, one positive switch and its complementary switch from the second leg of bridge-1 and two switches from the leg 2 of bridge-2 are sent.

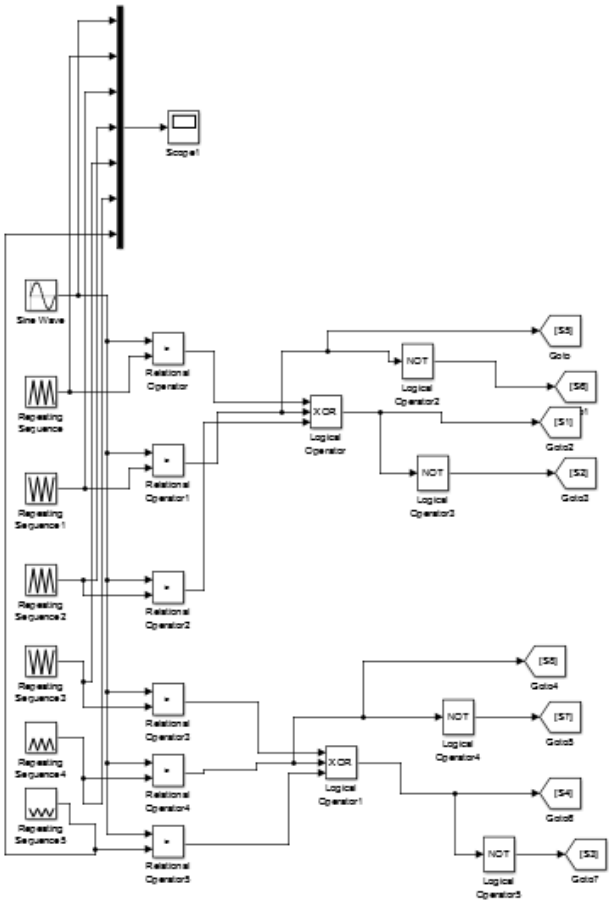


Figure 3.15 APOD logic circuit

3.9.3 Analysis of waveforms

Complete results for different three phase asymmetrical multilevel inverters are monitored in MATLAB Simulink model. Results are shown below.

1. Seven level asymmetric cascaded H-bridge inverter

Reference and carrier waveforms for APOD for generation of seven level asymmetrical cascaded H-bridge inverter. In this case, amplitude modulation index value m_a = 1 and frequency ratio, m_f = 100.

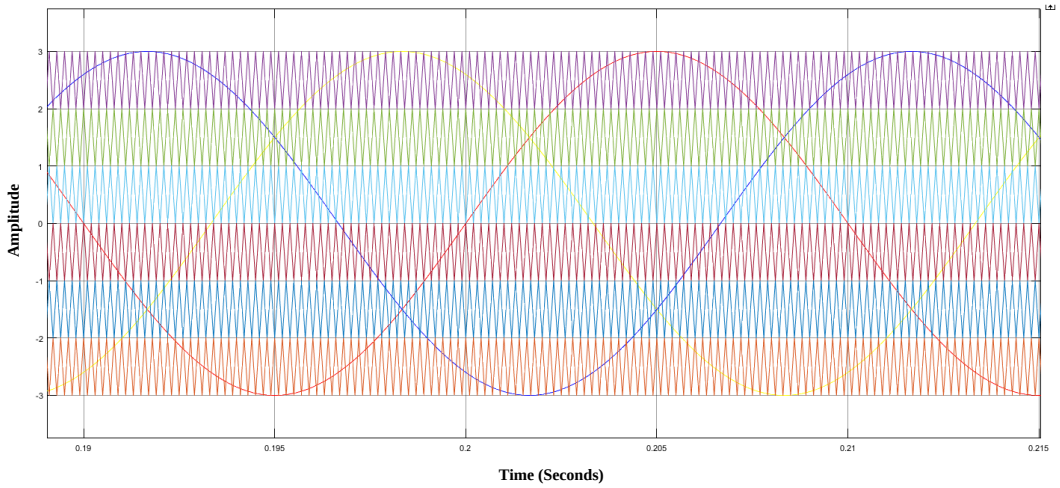
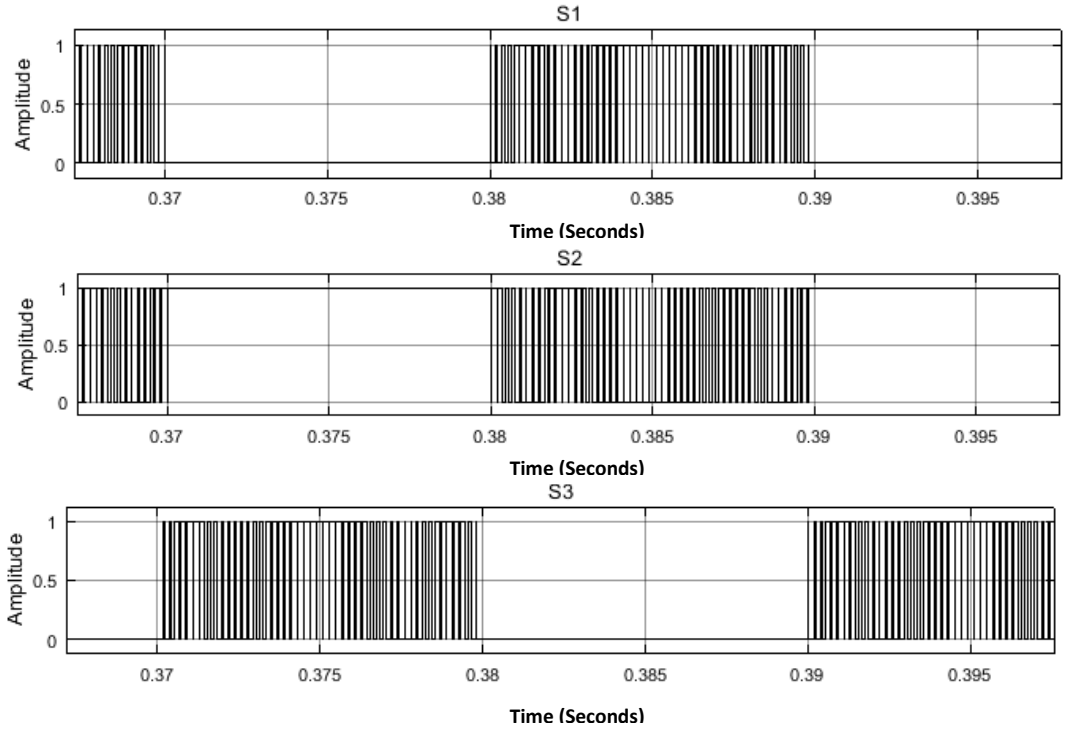


Figure 3.16 Carrier and reference waves for three phase 7 level asymmetric cascaded H-bridge inverter

Gate signals for producing the desired output voltages generated by control circuit of APOD. Eight switching pulses are generated as shown in the below figure. Eight switches are used in the H-bridge of the inverter. Each H-bridge consists of four switches. Inverter leg 1 has positive switch S1 and its complimentary switch S2 and another leg of this bridge 1 consists of switches S3 and S4. Switch S3 is the complementary of S4. Leg one of the second H-bridge consists of S5 and S6. S5 is a positive while S6 is the negative switch. Another leg of the bridge 2 consists of one positive switch S8 and one negative switch S7 (complementary switch). When any positive switch is turned on its complementary switch is off and vice versa. Four switches (S1-S4) of bridge one are shown in figure 3.17 (a) and four switches (S5-S8) of bridge 2 are shown in figure 3.17 (b).



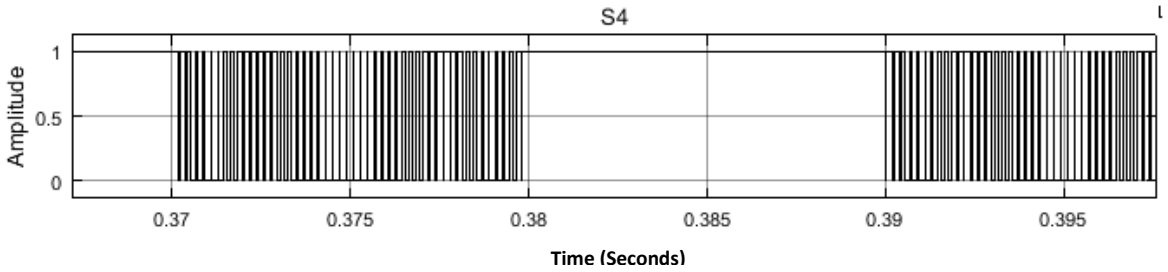


Figure 3.17 (a) Waveform of switching pulses for S1-S4

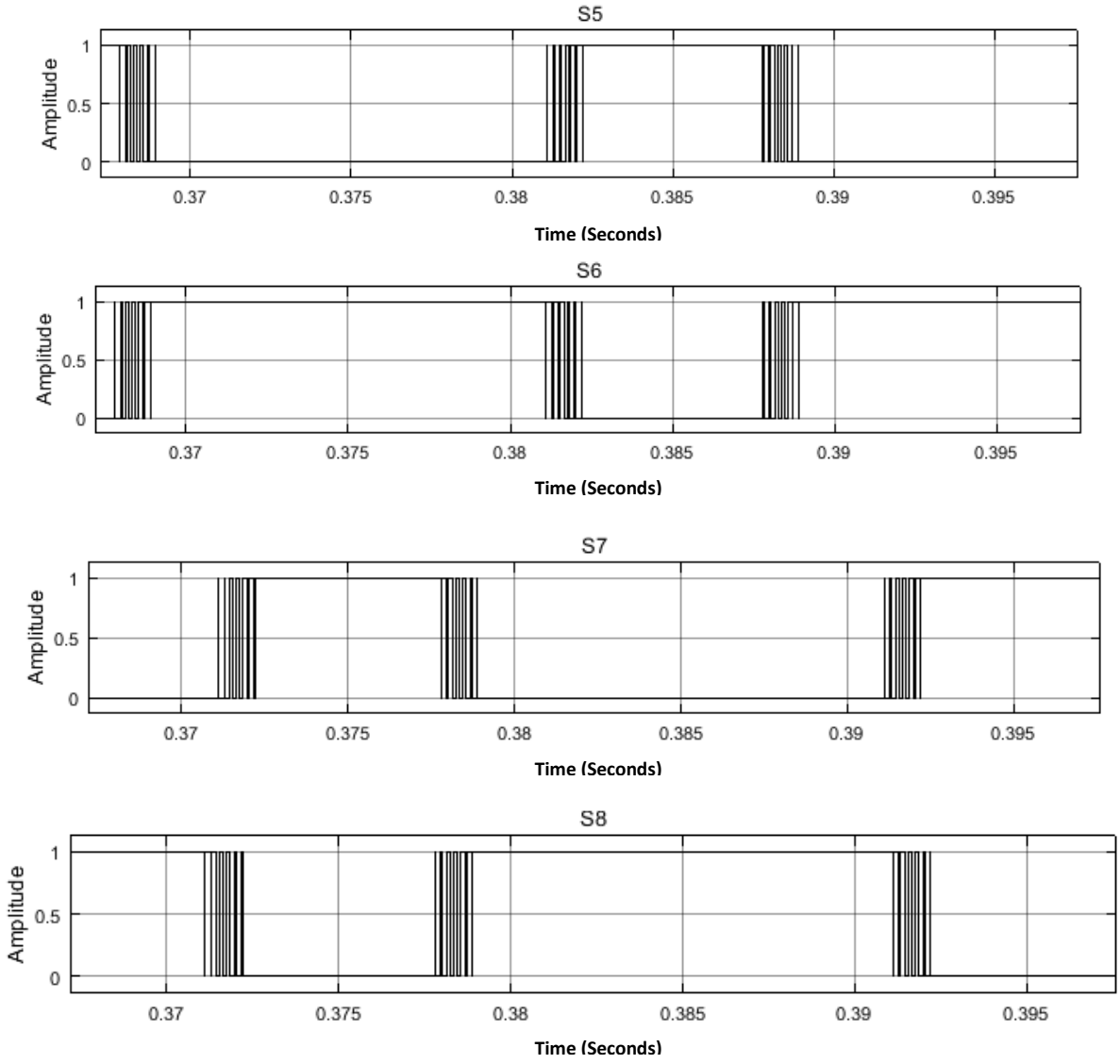


Figure 3.17 (b) Switching pulse waveforms for switches S5-S8

Table 3.6 Switching pattern for asymmetrical cascaded 7 level inverter

Voltage output (V)	S1	S2	S3	S4	S5	S6	S7	S8
+300	1	0	0	1	1	0	0	1
+200	1	0	1	0	1	0	0	1
+100	1	0	0	1	1	0	1	0
0	0	1	0	1	1	0	1	0
-100	0	1	1	0	1	0	1	0
-200	1	0	1	0	0	1	1	0
-300	0	1	1	0	0	1	1	0

1 and 0 represents the on and off states of the switches respectively. So, 7 levels of output voltages are achieved in the form of staircase.

The results of binary based seven level asymmetric cascaded H-bridge for three phase obtained from the simulation are shown below.

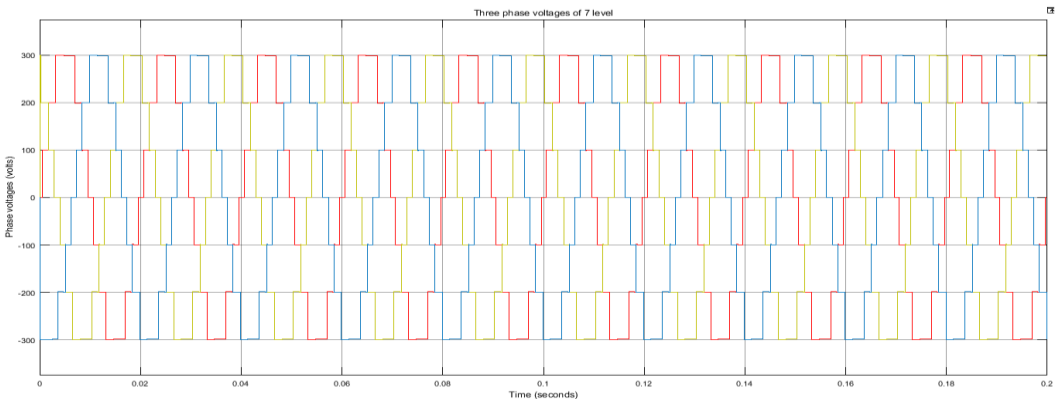


Figure 3.18 Three phase voltage waveform of binary based asymmetrical cascaded H-bridge7 level inverter

Harmonic analysis for 7 level output voltage is shown below in FFT window.

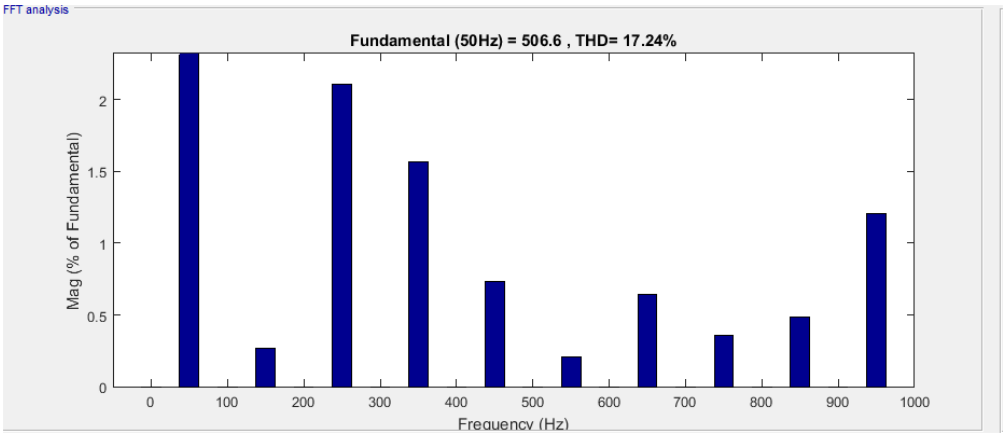


Figure 3.19 FFT window showing harmonic outline of 7 level asymmetrical CHB inverter

2. Analysis of Nine level asymmetrical cascaded H-bridge inverter

Simulation results of carrier and sinusoidal waves from APOD for nine level ACHB inverter obtained from the logic circuit of control strategy. Eight carriers are used in the control circuit for comparison with sinusoidal wave using a comparator that is relational operator and after controlling signals are selected for generation of switching pulses for the desired output levels. Reference and carrier arrangement waveform for 9 level asymmetrical inverter is shown in the figure 2.20. Here amplitude modulation index, m_a= 1 and frequency ratio is coming to be, m_f= 100. In this method two equal voltages are used and one voltage is taken as unequal. So, 3 H-bridges are needed. Based on that 12 IGBT are used as switching devices.

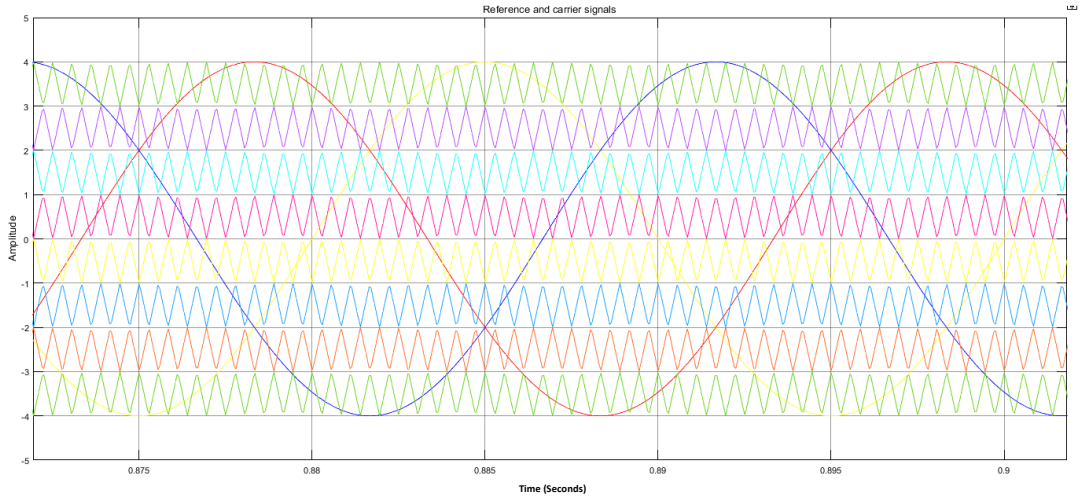
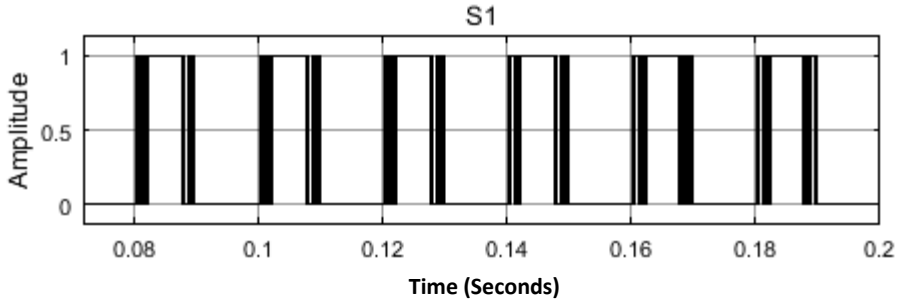


Figure 3.20 Reference and carrier waveforms for nine level asymmetric cascaded H-bridge inverter

In the three H-bridges of 9 level asymmetrical inverter, it consists of 12 switches S1-S12 each H-bridge is having four switches. The gate pulses for 9 level are shown below in the figure. Switches S1-S4 corresponding to the first H-bridge, S5 to S8 switches belong to second bridge of the inverter and rest four switches S9-S12 correspond to the last bridge. Each positive switch has complementary switch means when positive switch gets turned OFF, switch corresponding to it will automatically be ON.



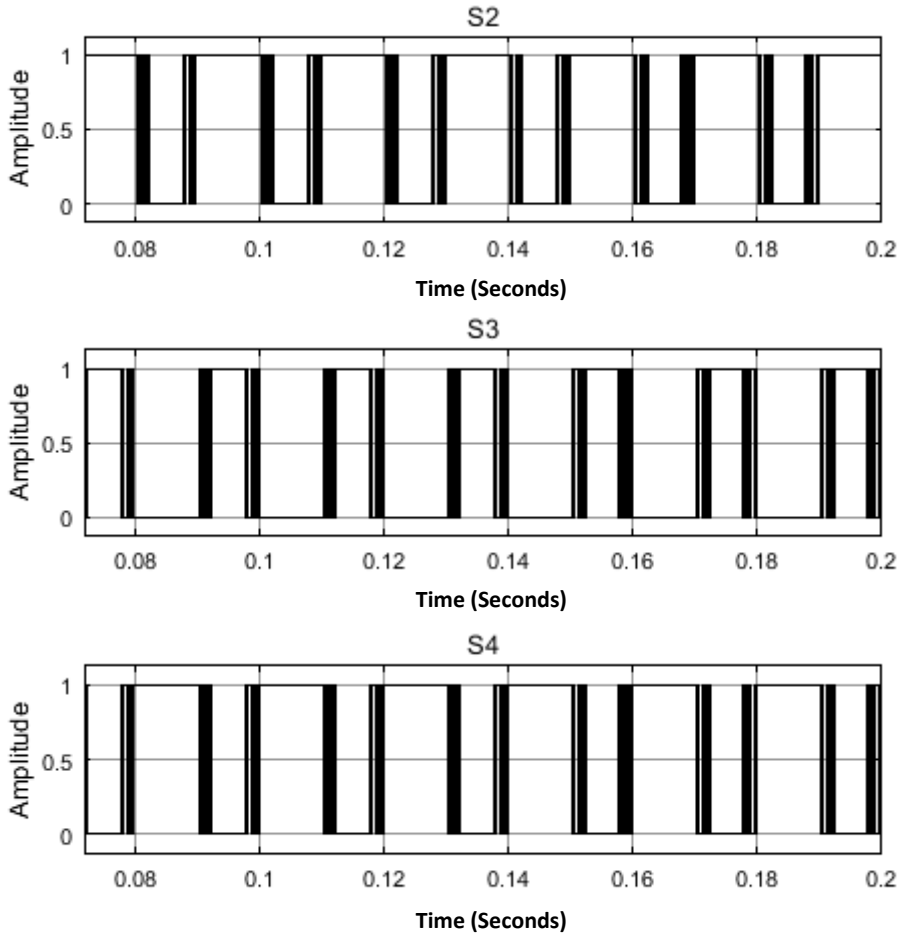
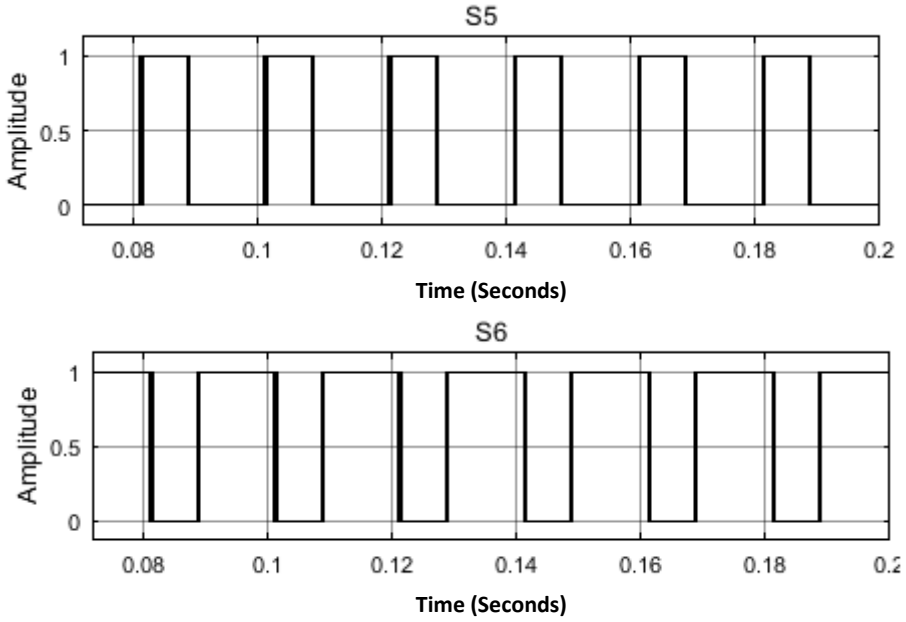


Figure 3.21 (a) Gate signals for switches S1-S4



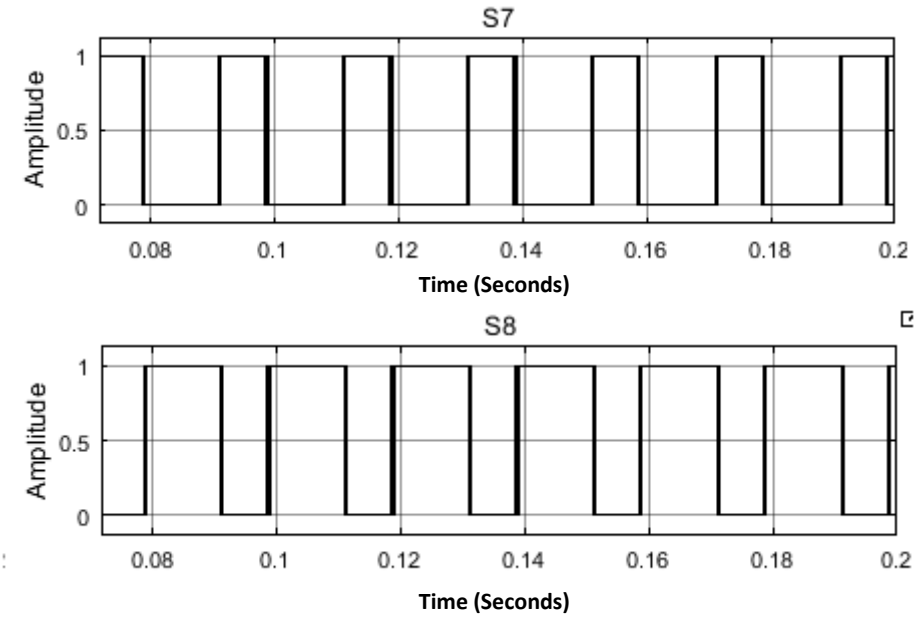
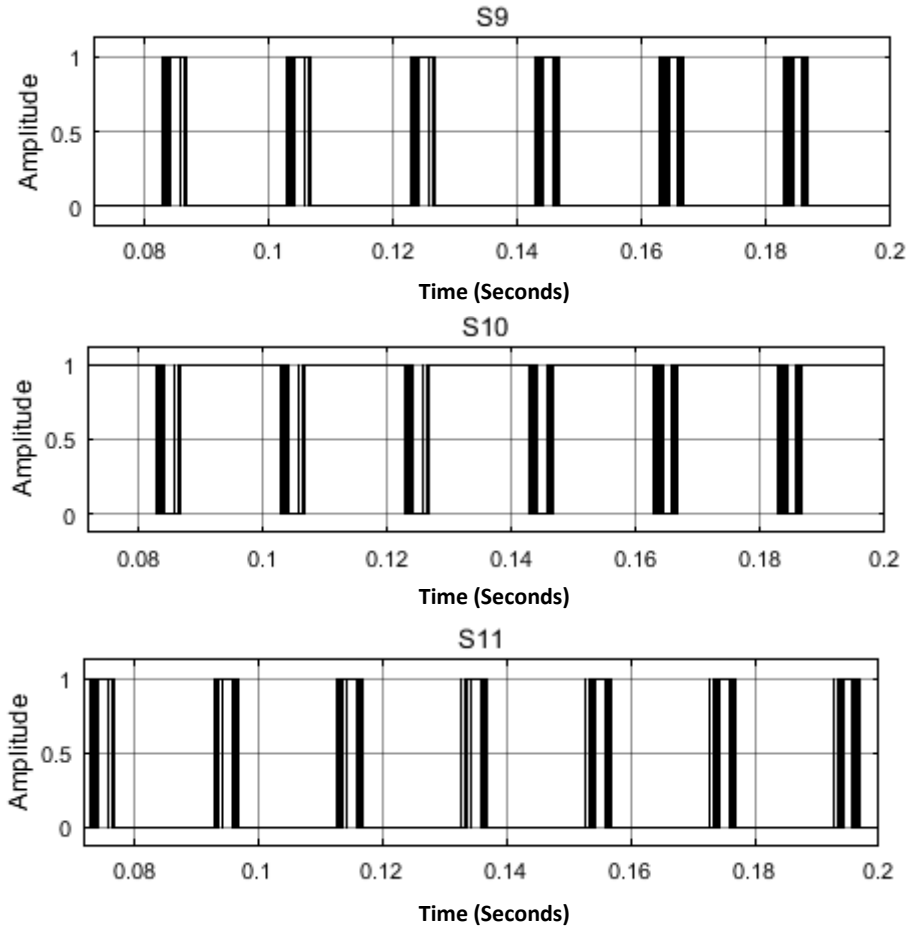


Figure 3.21 (b) Gate signals for switches S5 to S8



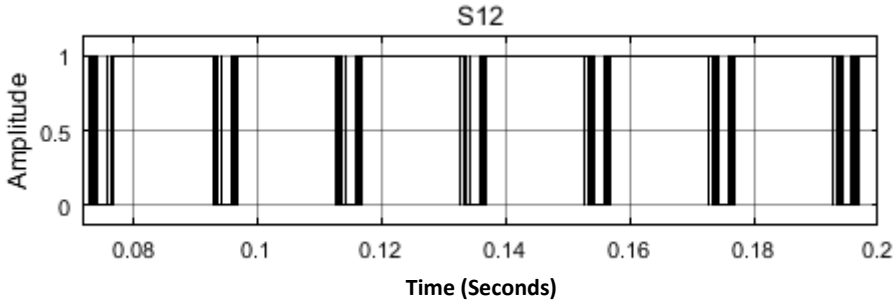


Figure 3.21 (c) Gate signals for switches S9-S12

Table 3.7 Switching sequences for 9 level asymmetrical cascaded H-bridge inverter

Voltage (volts)	S1	S2	S3	S4	S5	S6	S7	S8	S9	S10	S11	S12
400	1	0	0	1	1	0	0	1	1	0	0	1
300	1	0	0	1	1	0	0	1	1	0	1	0
200	1	0	1	0	1	0	0	1	1	0	1	0
100	1	0	0	1	1	0	1	0	1	0	1	0
0	0	0	0	0	0	0	0	0	0	0	0	0
-100	1	0	1	0	1	0	1	0	1	0	1	0
-200	1	0	1	0	0	1	1	0	1	0	1	0
-300	0	1	1	0	0	1	1	0	1	0	1	0
-400	0	1	1	0	0	1	1	0	0	1	1	0

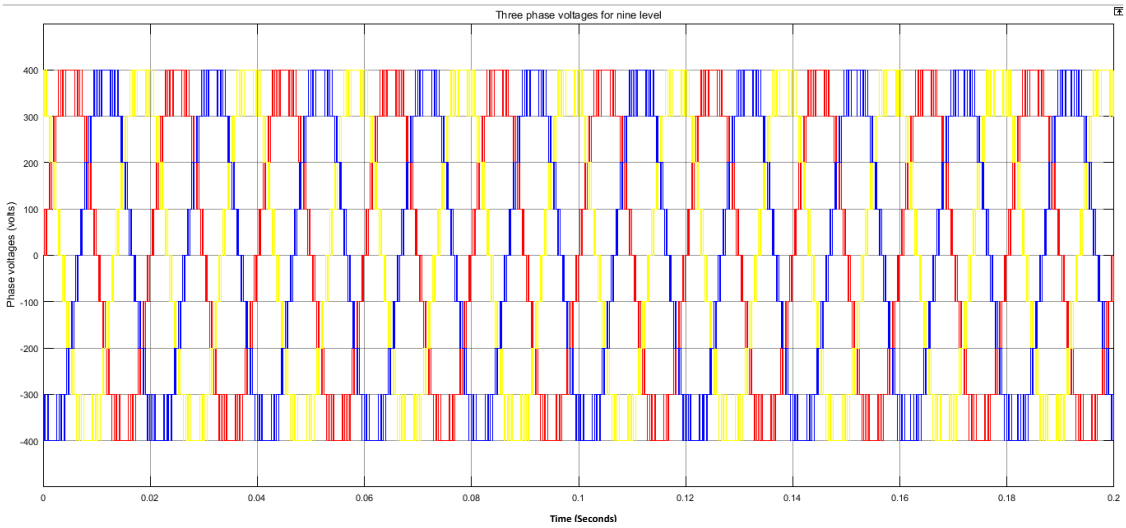


Figure 3.22 Three phase output voltage waveforms of 9 level asymmetrical cascaded inverter

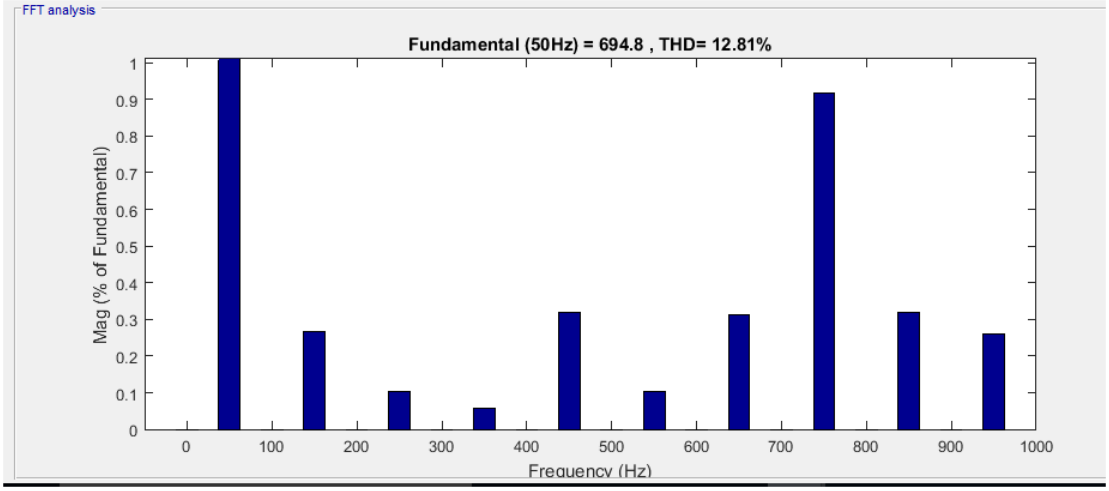


Figure 3.23 THD. of nine level asymmetrical cascaded H-bridge inverter

3. Results of eleven level asymmetrical inverter

Ten carriers are used for the generation of switching pulses required for producing desired output. Five of these carriers are merged with one XOR gate and rest of the carriers are combined with another XOR gate and after that exact controlling signals is selected for generation of final output. This level is realized using binary based method with having three H-bridges and three separate dc sources. The values of magnitude of dc voltage sources are given in table 3.8. Twelve switching devices are used. The simulation results of reference-carrier waveform generated from the logic circuit is shown below. Value for amplitude modulation index in this case is; m_a = 0.5 and frequency ratio, m_f = 100.

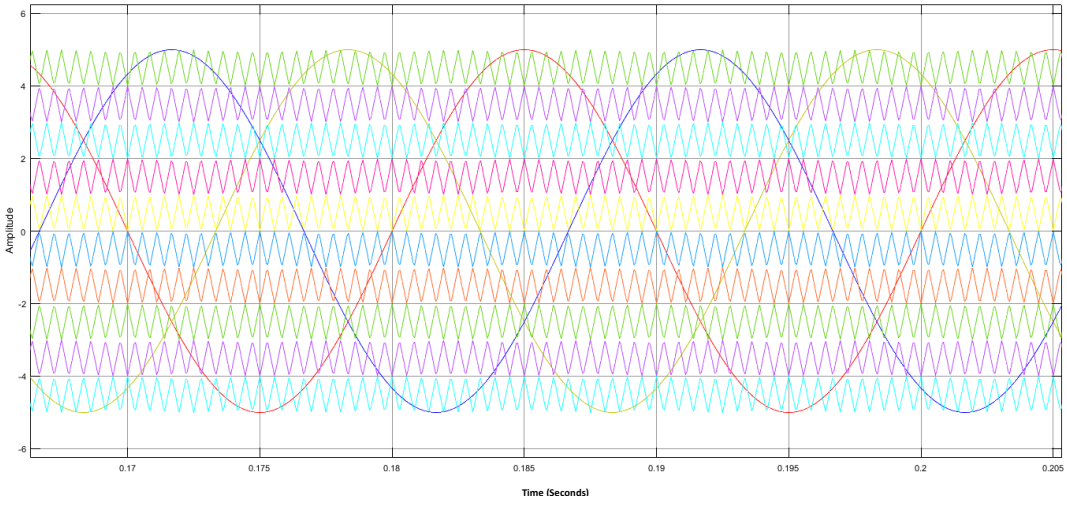


Figure 3.24 Reference and carrier arrangement for eleven level binary asymmetrical cascaded inverter

This level with three H-bridges constituting four switches in each H-bridge. S1-S4 are used in the first bridge of the inverter while S5-S8 are in the second bridge and likewise S9-S12 in the third bridge making a total of twelve switches. The magnitude of dc voltages are calculated according to the binary method. Switching pulse waveforms for these 12 switches

of eleven level asymmetrical cascaded H-bridge inverter are shown in the figure 3.25 (a), (b), (c).

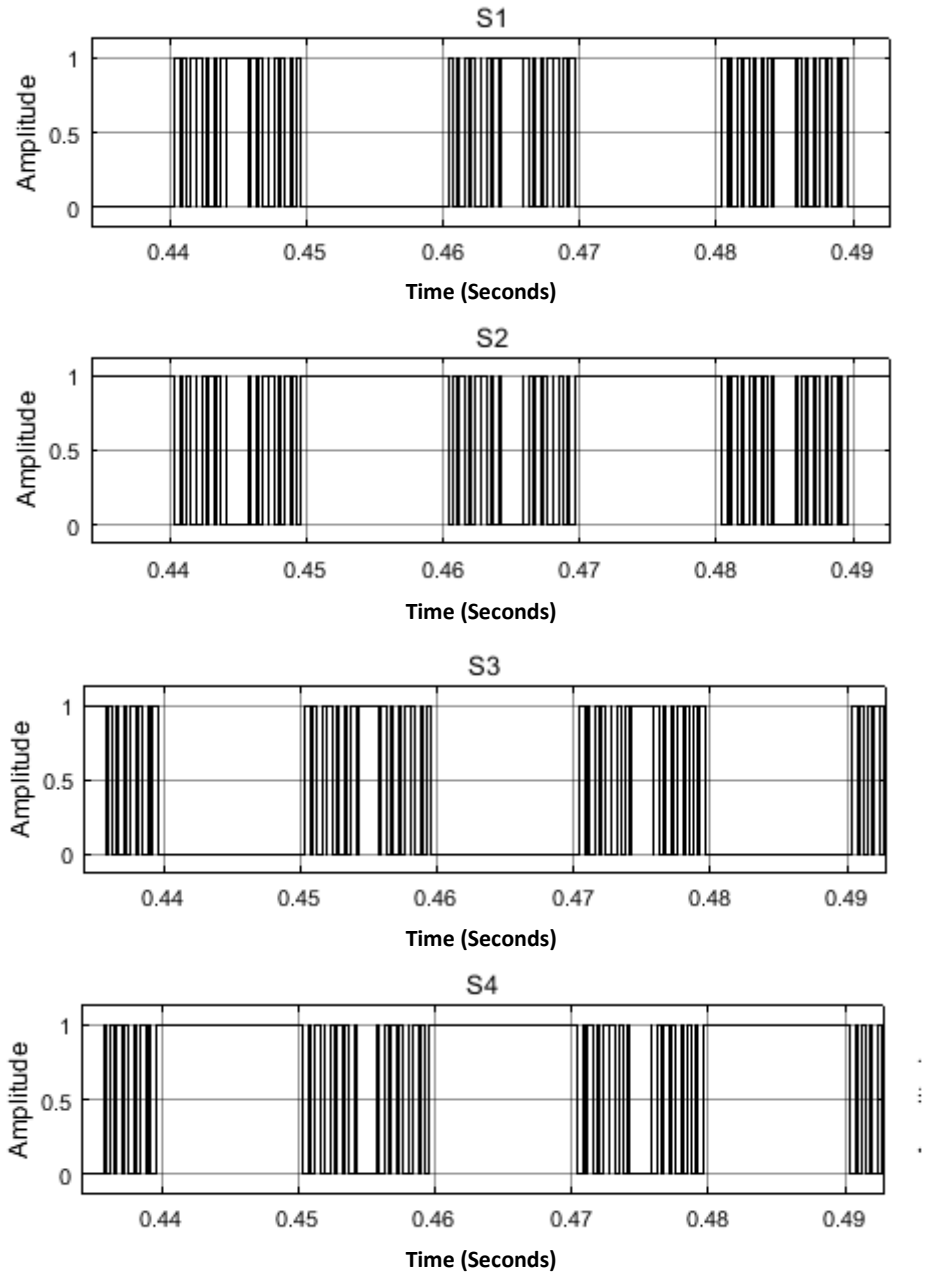


Figure 3.25 (a) Gate signals (S1-S4) for 11 level asymmetrical inverter

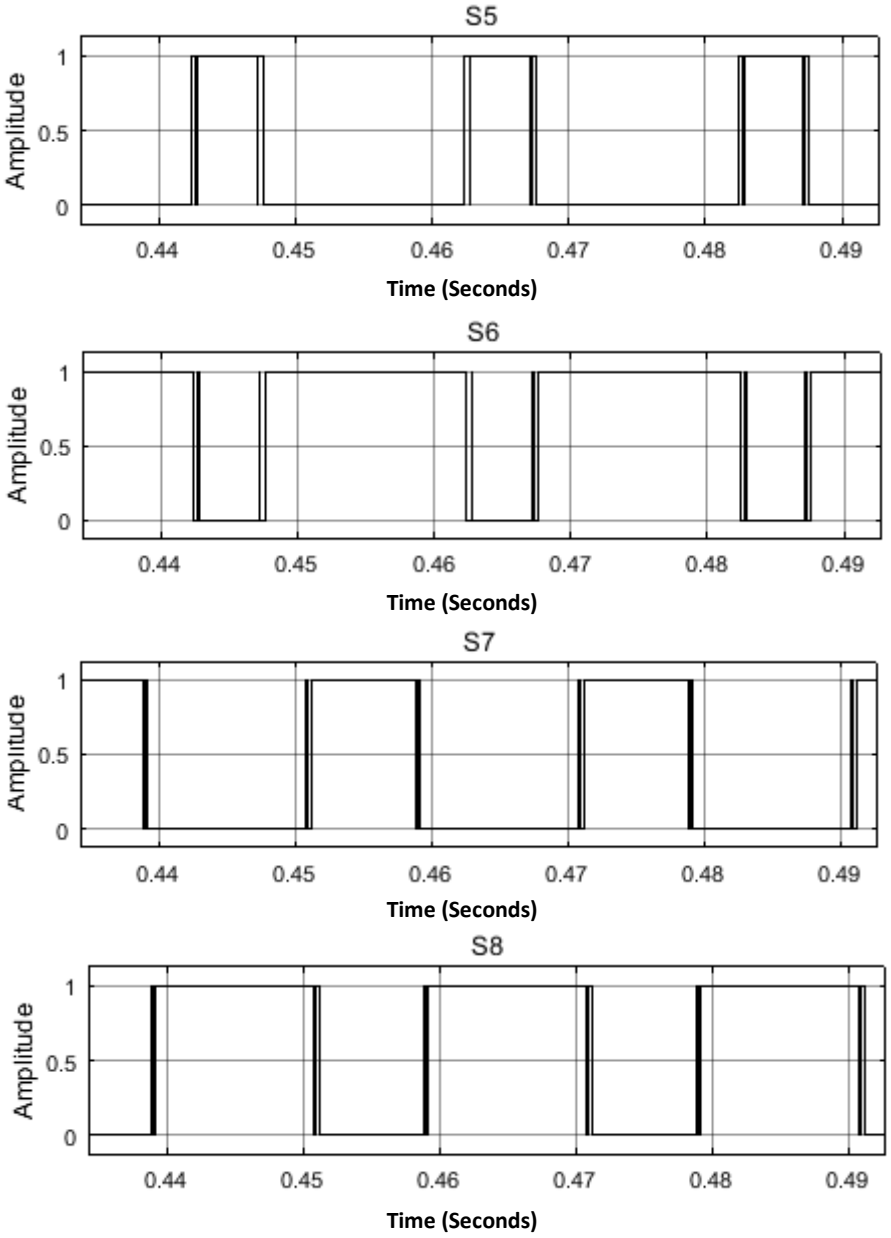
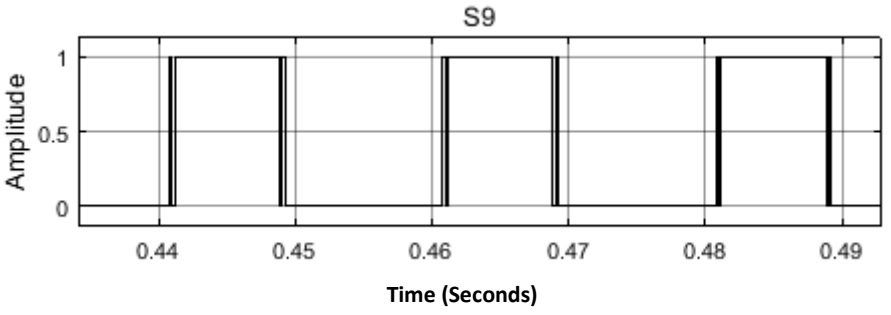


Figure 3.25 (b) Switching pulse waveforms for switches S5-S8



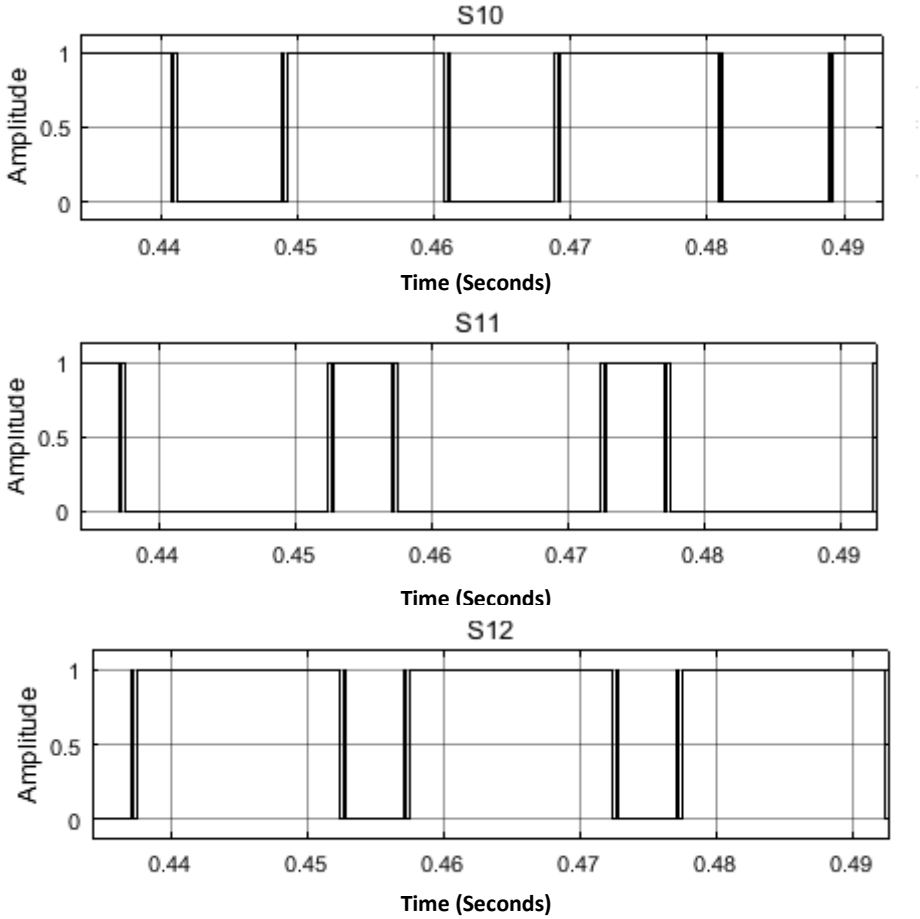


Figure 3.25 (c) Switching pulse waveforms for switches S9-S12

Switching sequences of eleven level asymmetrical cascaded H-bridge inverter are shown in table 3.8.

Table 3.8 Switching pattern for eleven level asymmetrical inverter

Voltages (volts)	**S1**	**S2**	**S3**	**S4**	**S5**	**S6**	**S7**	**S8**	**S9**	**S10**	**S11**	**S12**
100	1	0	0	1	1	0	1	0	1	0	1	0
200	1	0	1	0	1	0	0	1	1	0	1	0
300	1	0	0	1	1	0	0	1	1	0	1	0
400	1	0	1	0	1	0	1	0	1	0	0	1
500	0	1	1	0	1	0	0	1	1	0	0	1
0	0	0	0	0	0	0	0	0	0	0	0	0
-100	0	1	1	0	1	0	1	0	1	0	1	0
-200	1	0	1	0	0	1	1	0	1	0	1	0
-300	0	1	1	0	0	1	1	0	1	0	1	0
-400	1	0	1	0	1	0	1	0	0	1	1	0
-500	1	0	0	1	0	1	1	0	0	1	1	0

Three phase voltage waveforms produced for eleven level based binary asymmetric inverter are shown in the following figures.

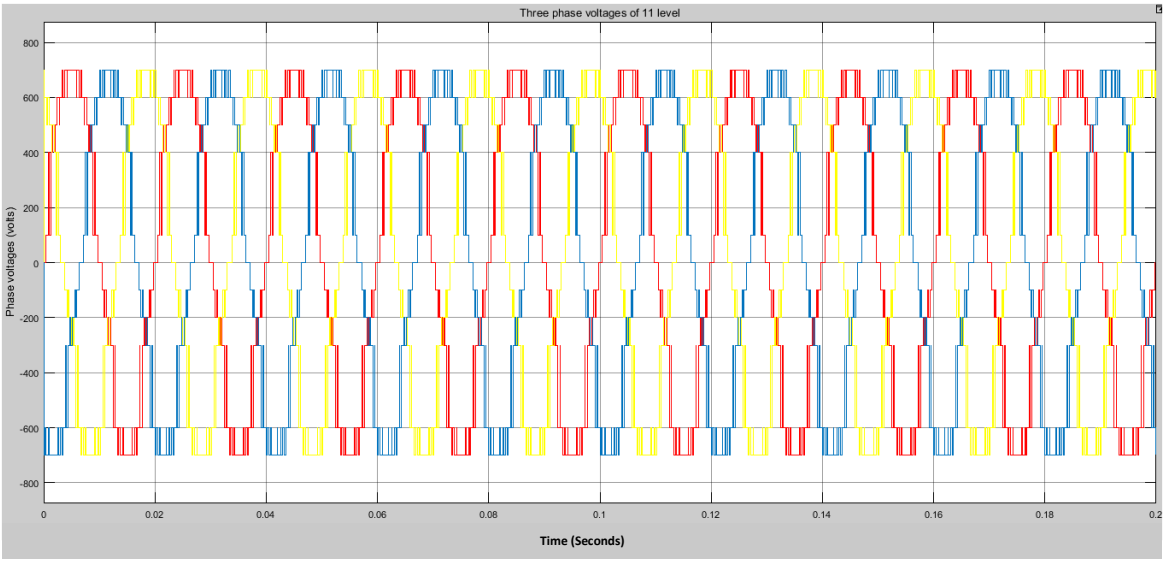


Figure 3.26 Three phase output voltage waveforms for eleven level binary asymmetric cascaded H-bridge inverter

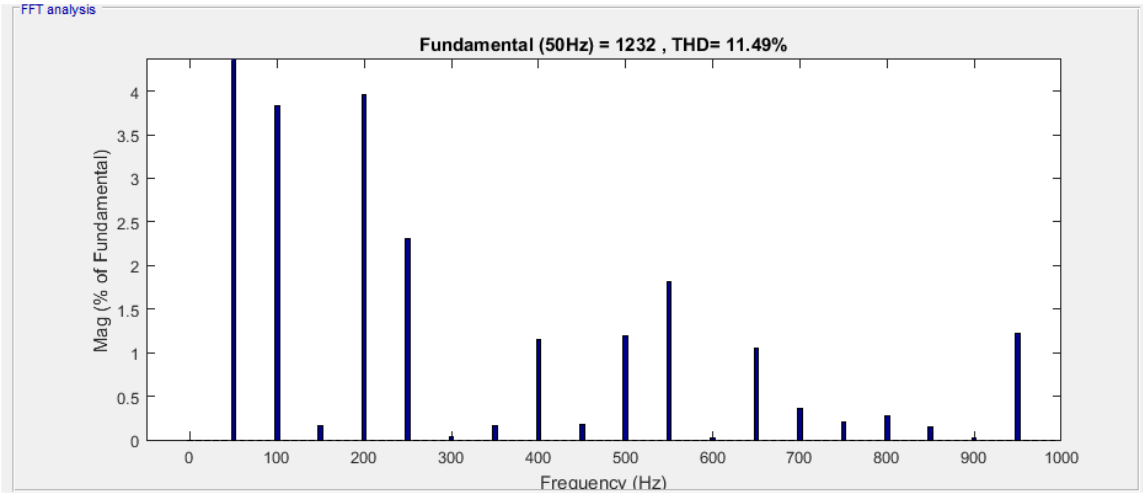


Figure 3.27 FFT analysis of eleven level binary asymmetrical cascaded H-bridge inverter

4. Waveform analysis of thirteen level asymmetric cascaded H-bridge inverter

Twelve carriers are used for comparison in this case. The magnitude of dc source voltages are taken in a way that the voltage across first H-bridge and third bridge are equal while second bridge has different voltage from these two. Based on this thirteen voltage levels are generated using APOD PWM. Modulation index value for 13 level, m_a = 1 and frequency ratio m_f = 50

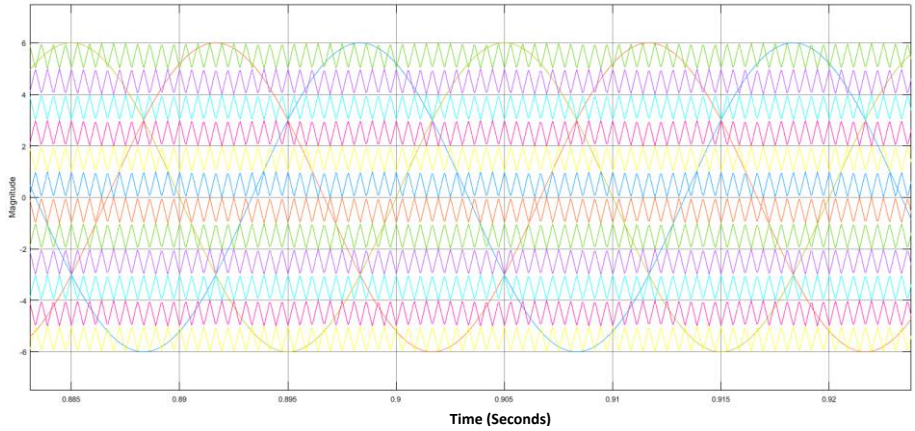


Figure 3.28 Reference and carrier waveforms for 13 level asymmetric cascaded H-bridge inverter

Twelve switches with three H-bridges are used to generate the gating pulses for 13 level asymmetrical voltages through control circuit.

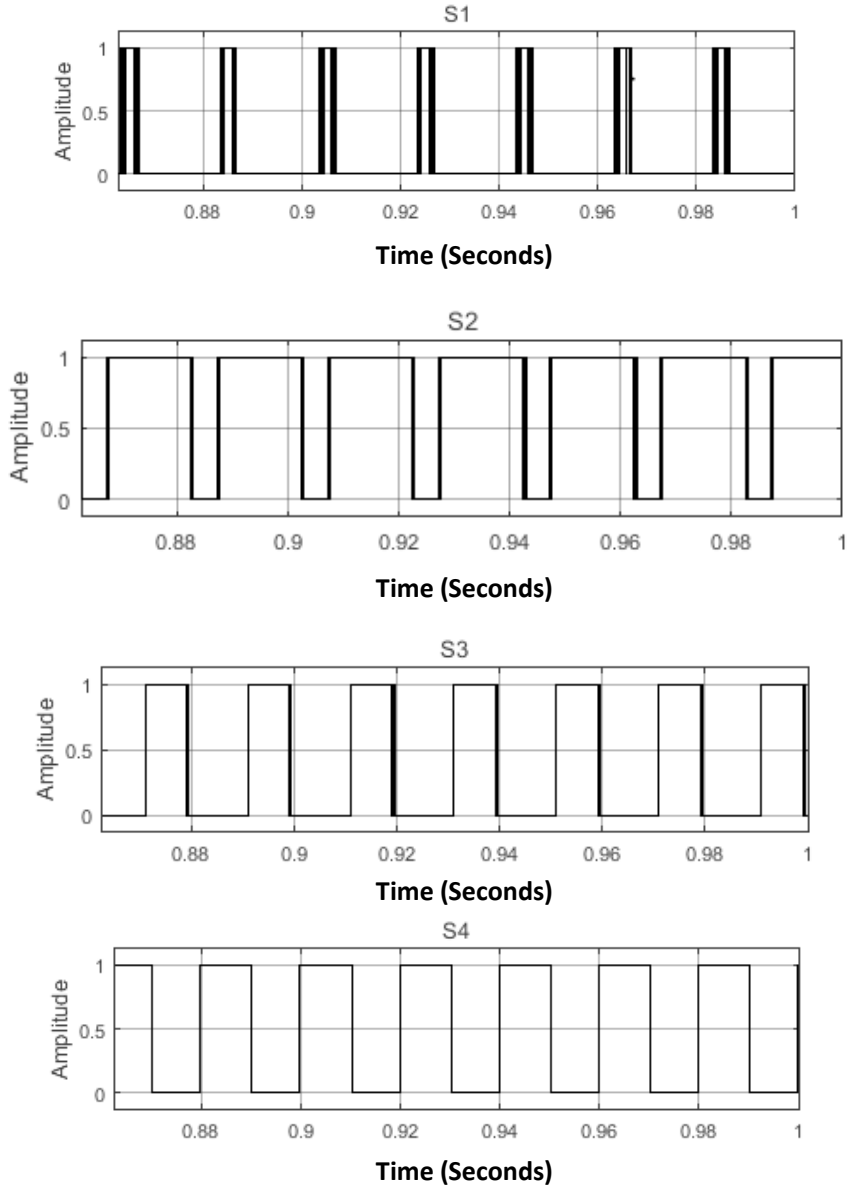


Figure 3.29 (a) Gate signal waveforms for switches S1-S4

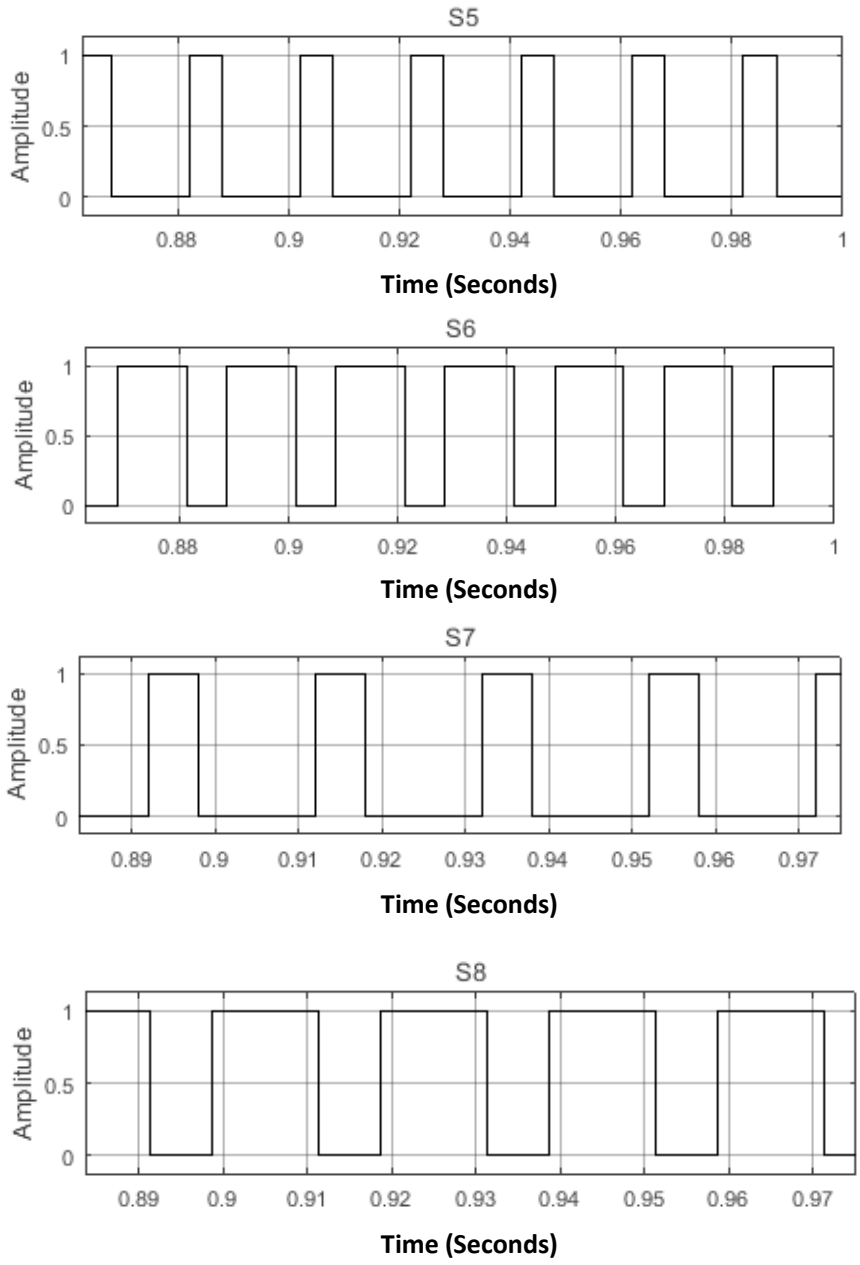
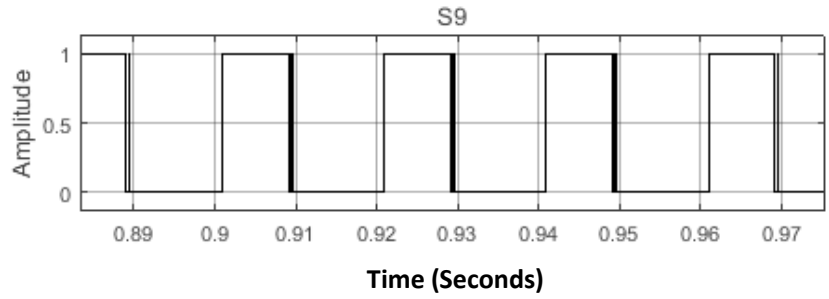


Figure 3.29 (b) Pulse waveform for switches S5-S8



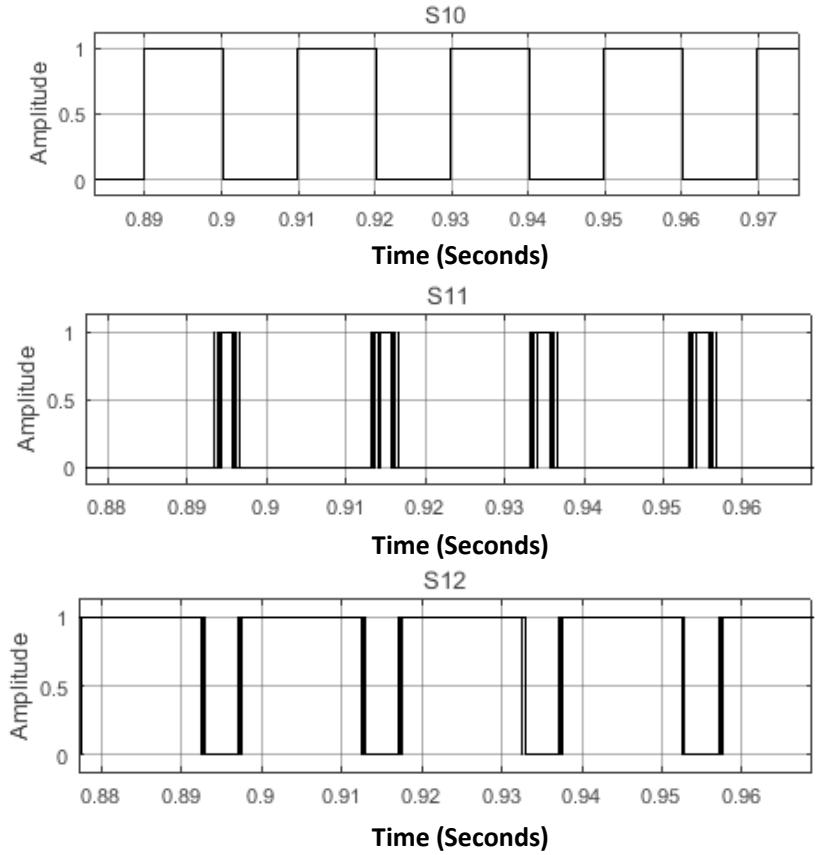


Figure 3.29 (c) Pulse waveforms for switches S9-S12

Table 3.9 Switching sequences for thirteen level asymmetric cascaded H-bridge inverter

VOLTAGES (V)	S1	S2	S3	S4	S5	S6	S7	S8	S9	S10	S11	S12
600	1	0	0	1	1	0	0	1	1	0	0	1
500	1	0	0	1	1	0	0	1	1	0	1	0
400	1	0	1	0	1	0	0	1	1	0	1	0
300	0	1	1	0	1	0	0	1	1	0	1	0
200	0	1	1	0	1	0	0	1	0	1	1	0
100	1	0	0	1	1	0	1	0	1	0	1	0
0	0	0	0	0	0	0	0	0	0	0	0	0
-100	0	1	1	0	1	0	1	0	1	0	1	0
-200	1	0	0	1	0	1	1	0	1	0	0	1
-300	1	0	0	1	0	1	1	0	1	0	0	1
-400	1	0	1	0	0	1	1	0	1	0	1	0
-500	0	1	1	0	0	1	1	0	1	0	1	0
-600	0	1	1	0	0	1	1	0	0	1	1	0

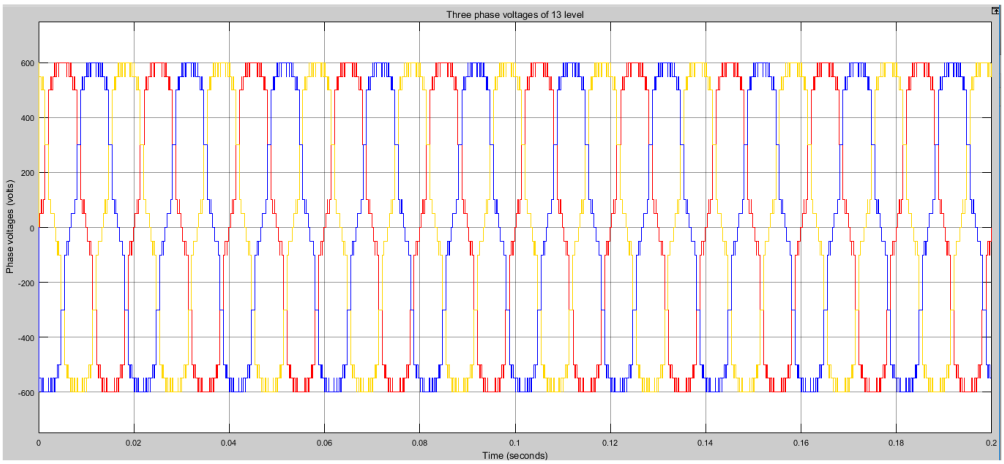


Figure 3.30 Three phase voltage waveforms for thirteen level asymmetric cascaded H-bridge inverter

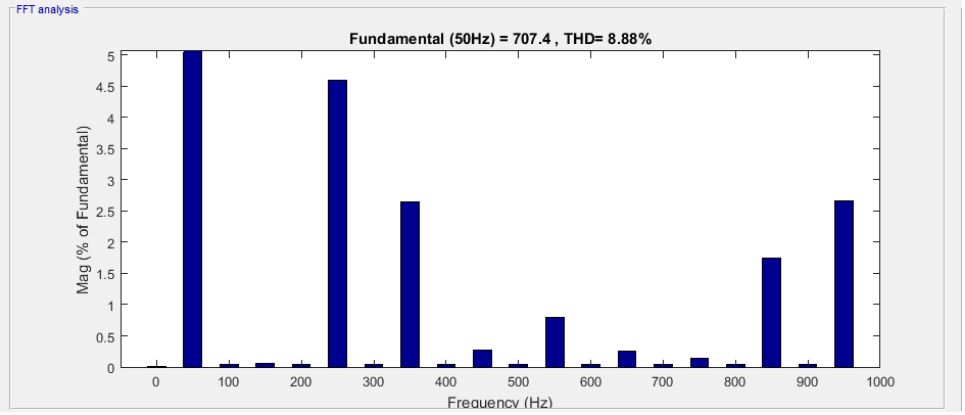


Figure 3.31 THD analysis for 13 level asymmetric cascaded H-bridge inverter

Table 3.10 Comparison between THD for different asymmetrical inverter levels

Sr. No.	Asymmetrical levels	THD
1	SEVEN	17.24%
2	NINE	12.81%
3	ELEVEN	11.49%
4	THIRTEEN	8.88%

So, from the above results we can say that as we increase the number of levels, THD gets reduced and more sinusoidal voltages we achieve. Asymmetrical inverter uses less switching devices and separate dc sources for the same no. of levels generation in comparison to the symmetrical inverters. Modulation index values of the different asymmetric levels lie between 0 and 1. From the simulation results of output phase voltages, we can see that shape of the waveforms are near to the sinusoidal especially in the case of eleven level and thirteen levels. It is observed that output waveforms of each level are balanced.

CHAPTER 4
DISTRIBUTION STATCOM

4.1 INTRODUCTION

Distribution systems are more prone to suffer from power quality problems. These power quality complications are the outcomes of non-linear loads that are generally reactive which are connected in the load side of power distribution network. These loads are responsible for the nativity of current harmonic, disequilibration of voltages, and high burden of reactive power. These problems effect the power quality and the waveforms remain no longer sinusoidal as a result consumers get a very high exaggeration unbalanced voltage supply which results in poor power quality due to voltage flickers, sag, swells, and interruptions. Mainly in the distribution network, AC loads are connected that devour reactive power which badly effects the quality of power since there is not any discipline for reactive power. The modish load devices used in the industries are responsible for the adverse effects in power quality as these are based on electronic supervisions. Nonlinear loads cause drenching in the voltage which turns to be sensitive for the whole entire system in the distribution network. Power factor of the loads become very low which should not be. Occurrences like starting of motors, switching of capacitor, faults also enforce power quality problems. Bad power quality refers to the non-sinusoidal waveform of voltages and currents. Harmonics caused by the non- linear loads which are fed to the source are beyond the IEEE-519 standards. Enormous reactive power boosts the losses in the feeder. Harmonic current distortion is primarily due to non-sinuosity of load currents**.**

According to IEEE Std. 1100; power quality refers to the "Image of powering and grounding of unstable equipment in the approach which is relevant to the operation of that equipment". Power quality is the combo of both voltage and current quality. In order to meet the above challenges some counteracts are proposed so that utility can provide the distortion less balanced supply voltage to the consumers and deal with the challenging issues of demand of reactive power. These remedies aim in load compensation. These techniques are called as custom power devices. Custom power devices are meant for the governing of the problems related with the distribution network. [30], [31]. These devices strengthen the service of power quality which are delivered to the customers from the distribution network. These devices are constructed in order to operate at both medium and low voltages. These are the shelter for distribution networks that compensate the harmonics, reactive power, correct the

power factor, improves the voltage regulation and balance the load. These prevent the destruction of equipment in the distribution network from the worst situations of the nonlinear loads that usually cause currents with lagging power factor and these give birth to the reactive power burden in the distribution systems. The main aim of these custom power devices are to eliminate the harmonics produced by non-linear loads which are given to the supply side. These devices compensate the harmonics sufficiently less than 5 % according to IEEE -519 standard. So in order to improve the power quality and to face the challenges offered by the nonlinear loads, custom power devices are needed (N.G. Hingorani, 1995).There are various types of custom power devices namely shunt linked, series linked and both shunt-series associated devices. DSATCOM is a shunt associated device that eliminates current harmonics present in the distribution network. DVR is based on the series connection which is linked in series with the network and compensated for voltage harmonics while UPQC is referred to both shunt and series linked device which reduces harmonics present in both load current and voltage [45], [46]. In this thesis, performance of custom power device DSTATCOM is inspected.

DSTATCOM is a shunt linked device which aims in mitigating the harmonics raised due to nonlinear loads and that are provided to the supply side [41], [42], [43], [47]. When DSTATCOM compensates the harmonics in the load side, then these are not present in the source and as a result balanced load is achieved. DSTATCOM enhances the power quality by improving the power factor to unity, voltage regulation and compensate the demand of reactive power. During unbalanced load conditions, there is the distortions in the waveforms like when load voltage increases during this event, load current gets decreased and sometimes load voltage gets short circuited and during that time period current suddenly increases and as a result unbalancing of load takes place which effects the power quality. DSTATCOM acts as shunt active filter that mitigate the problem of unbalancing of load. DSTATCOM effectively compensates the problems in the three phase four wire distribution system. It also reduces voltage sag and swell problems. It can transfer both active and reactive power with the distribution network. In order to reduce the unsatisfactory load current constituents, DSTATCOM insert currents into the point of common coupling. DSTATCOM satisfies the losses in the system by providing fundamental component of active current. DSTATCOM can be either voltage or current source. It provides good quality of current for nonlinear loads. DSTATCOM is allied near the nonlinear loads. For system to be stable, DSTATCOM should present either lagging or leading reactive VAR especially when transient events occur.

The plus point of DSTATCOM is that it does not require any capacitors for the transaction purposes of reactive power between the DSATCOM and the ac network.

4.2 CONFIGURATION OF DSTATCOM

Figure 3.1 shows the DSTATCOM which is linked parallel to the source and the load. It is resided in between source and the load. The structure of DSTATCOM mainly comprises of inverter which is generally 2 level voltage source inverter. VSI's produce required voltages and currents. The coupling transformer is used to connect the DSTATCOM between the point of common coupling that is between the source and the load. Dc link capacitance acts as energy storage device which provides the dc source voltages for the converter. That's why it is generally used at the sources of inverter. It also removes the distortion and maintains constant voltage across the inverter. Leakage inductance provides transaction of reactive power among DSTATCOM and the network. It also acts as a filter for currents. The coupling transformer also acts as a dis-connector for DSTATCOM from the distribution network. The control unit in the configuration is meant for the developing of switching pulses of the inverter for the required output waveforms that are given to the PWM. Once, the inverter gets the dc voltage from the energy storage device, PWM switches the inverter for generating the signals to achieve the desired output voltage and current. The converter DC-AC which converts the dc source voltages into three phase ac voltages. The on and off mode of the switches are commanded by PWM. Before generating the switching pulses, first the voltages and currents are deliberated and after that given to the controller of DSTATCOM for comparison. For this, controller can use any type of control algorithms such as Instantaneous reactive power theory, synchronous reference frame theory etc. for the extraction of reference currents. Then the controller executes the observation and then results in the switching signals of the inverter through the PWM. The switching devices of the inverter get activated for generating the sinusoidal ac output.

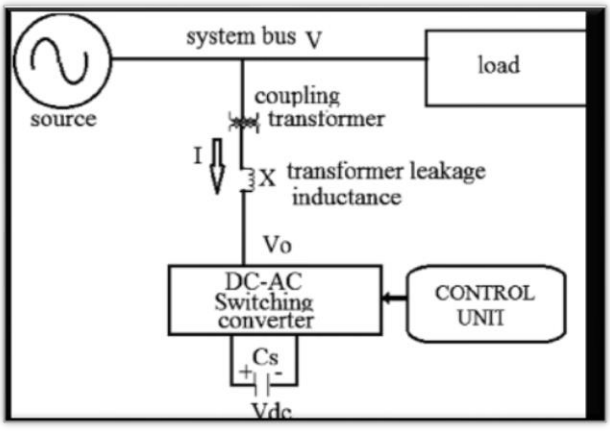


Figure 4.1 Configuration of DSTATCOM

4.3 Principle of DSTATCOM

The basic principle of DSTATCOM is based on a voltage source converter. DSTATCOM compensates the harmonics present in load side and to supervise the flow of reactive power. It protects the source from the harmonics generated due to nonlinear loads. It works on the current harmonic compensation principle. The lesser will be the harmonics, more we achieve sinusoidal balanced waveforms. It gives set of three phase ac output voltages through its voltage source inverter. DSTATCOM can either yield or consume reactive power. It can generate lagging or leading reactive VAR. The DSTATCOM is connected parallel to the system. The fundamental components of DSTATCOM are voltage source converter consist of power electronic based switching devices like IGBTs. When these switches are sent to the PWM control, switching pulses are generated for the desired output voltages. Coupling transformer connects the DSTATCOM between the source and load known as point of common coupling where it compensates the problem. It consists of the dc link capacitance which provides the dc voltage source to the inverter. These dc voltages are converted into three phase ac voltages through the voltage source inverter which appear at the point of common coupling. These are in- phase and tied up with the ac system by reactance of the coupling transformer. The required voltages and currents are computed and correlated with the rules of the controller of DSTATCOM. Feedback control is achieved by the controller. From the controller, references for the PWM signal are produced and from the PWM, switching pulses are triggered which are given to the switches for the final output driven by the converter.

The compensated current is the difference of source current from the load current.

$$I_{comp} = I_{load} - I_{source} \quad (4.1)$$

Transaction of reactive power between the distribution network and DSTATCOM is obtained by allocating the magnitude and phase of DSTATCOM inverter output voltages.

4.4 Operating modes of DSTATCOM

There are 3 modes of DSTATCOM in which it operates, it can be; no load, injection or absorption mode.

1. No load mode: in this case, output voltage of voltage source inverter, V_i= voltage of AC system,V_s. So, there will be no reactive power supply. This mode is also known as stand-by mode. Neither generation nor absorption of reactive power exchange will take place. Reactive power is zero in this case. Phasor diagram and waveforms at no load is shown below.

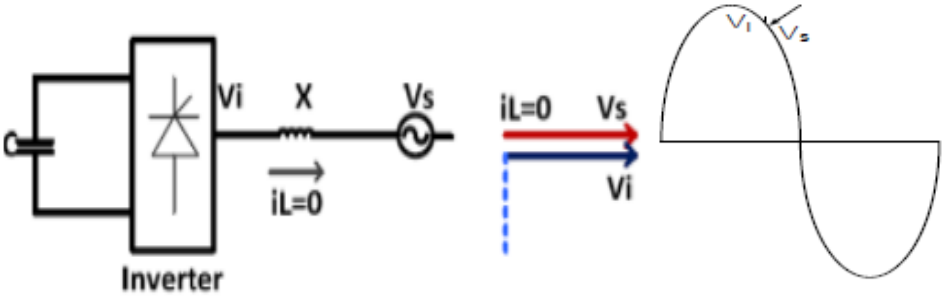


Figure 4.2 No load operating mode ($V_i = V_s$)

2. Injection Mode: In this case, output voltage of VSI is more than the AC voltage of the system. DSTATCOM will itself contribute reactive power to the ac system. This mode is also known as capacitive mode in which custom power device, DSTATCOM provides the capacitive nature of reactive power to the distribution system. Capacitive nature means reactive power is leading. The current will move through the coupling inductor of DSTATCOM to the distribution system and capacitive reactive power is generated to the ac system. Real power exchange will take place only when any independent DC source is provided to DSTATCOM. In this mode, active power will be given to the ac system. Its phasor representation and waveforms associated with this mode is shown below.

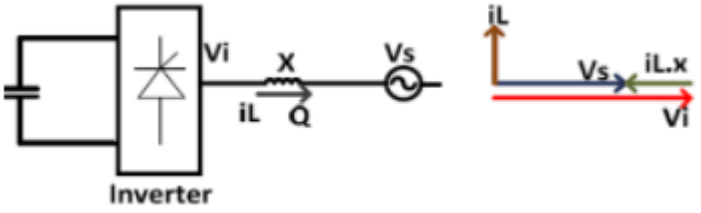


Figure 4.3 Injection mode of DSTATCOM($V_i > V_s$)

3. Absorption Mode: When the inverter voltage, V_i is less than the AC system voltage,V_s DSTATCOM consumes inductive reactive power. The current from the ac system moves to DSTATCOM. The inductive reactance power is lagging. Since, the voltage of inverter is least than the voltage of distribution system, the inverter will abstract real power from the distribution system that is DSTATCOM will absorb real power. The phasor diagram and waveform corresponding to this mode is shown below.

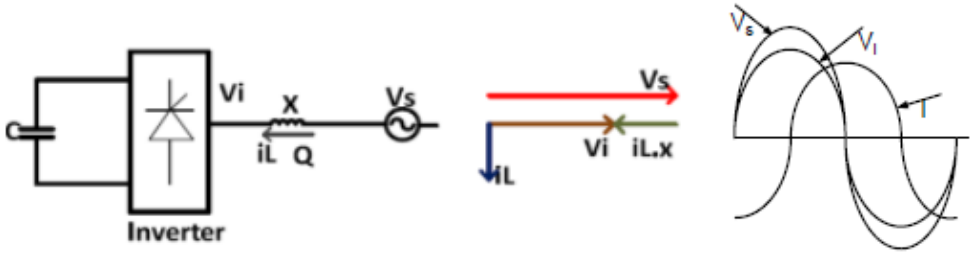


Figure 4.4 Absorption mode of DSTATCOM ($V_i < V_s$)

4.5 Control Scheme of DSTATCOM

The control scheme plays crucial role in custom power devices for the purpose of extraction of reference signals in the form of either current or voltage. These may include either closed loop or open loop control algorithms which give the explanation of variation of load signals. The generation of reference signals is the primary element of the control scheme. The evaluation of reference signals is proposed through the identification of required current or voltage signals. The evaluation of reference signals in conditions of voltage and current are ferried out in time domain path or frequency domain access. Open loop path follows Fourier analysis. Time domain path refers to the closed loop algorithm. These control techniques are used for the authority of custom power devices like DSTATCOM. The need of control scheme is to extract the reference source signals which is important for the custom power devices to be noticed as a result the non-linearity due to the presence of nonlinear load in the distribution network does not give the effect of its harmonic components fed to the supply side. The administration of any custom power device actually depends on its control methodologies of reference currents or voltages. These techniques are usually meant for the cancellation of the harmonic components and also break- off the unbalancing of load. These effects will not be present in the source side.

There are various control schemes of DSTATCOM for derivation of reference current signals based on frequency or time paths. The most popular control schemes which follow path of time are Synchronous Reference Frame Theory, Instantaneous Reactive Power Theory, Sine-Multiplication Theorem etc. this thesis expresses synchronous reference frame theory technique based on Park's transformation principle for calculation of reference currents. For the generation of pulses, APOD PWM control strategy is used and is discussed in detail in chapter-3.

4.5.1 Synchronous Reference Frame Theory (SRF)

This theory is the most popular control algorithm used for the abstraction of reference currents in DSTATCOM. This theory is relevant only to the systems having all the three phases. This method is based on the study of calculation of desired signals with respect to

time. This theory actually focuses on the determination of reference currents from the disturbed load current signals for which DSTATCOM is to be used in the distribution network to compensate the harmonics in the load current and to balance its waveforms. SRF theory works on the principle of Park's Transformation which means conversion of three phase stationary currents or voltages into two phase similar revolving components. In SRF theory, the conversion of the three phase stationary components is in the form of direct axis and quadrature axis which is also known as d-q theory. SRF theory acts like a harmonic current abstractor. It assesses the volume of harmonics present in current signals that are compensated through DSTATCOM. These refunded harmonic currents become the reference currents. This method takes three steps for the measurement of reference currents and achievement of compensator currents by involving Clark's and Park's transformation. Clark's transformation refers to the conversion of the components in α - β structure while Park's principle is the d – q rotating structure and finally reverse Park's and Clark's conversion is done for achieving reference source currents as well compensating currents.

This method also uses a phase locked loop block in its control circuit for the mechanism of three phase terminal voltages of the system; v_a, v_b and v_c. The purpose of PLL is to develop sine and cosine angles while doing transformation based on Park's as well as reverse conversion of Park's and Clark's method. PI controller is used to make the voltage of dc link to be same or it can be used for maintaining the ac voltage of the system. The error of reference and actual dc voltage is exercised through the PI controller.

$$\Delta V_{dc} = V_{dce} = V^*_{dc} - V_{dc} \qquad (4.2)$$

The output of this PI controller is added with the dc component of direct axis current, $i_{d(dc)}$ and then source currents are generated. A low-pass filter is used to remove the components of ac. For calculating the reference source currents, quadrature axis current (i_q) is taken to be zero and can be usually added without the use of PI controller whose output is generally summed up with the component of dc of quadrature axis current. I_q represents the reactive component of current. I_d representing the active constituent of current. Firstly, the procedure of SRF theory starts with the conversion of three phase load currents into Clark's transformation that is in α - β structure. Three phase voltages, dc voltage and the load currents are taken as inputs and fed to the controller. PLL is incorporated for producing angles in the conversion blocks.

In the step one. Three phase load currents which are in a, b, c components are first converted into two phase components in α – β structure based on Clark's transformation. The

transformation of current is shown in the equation below. This transformation equation is also equivalent in case of three phase voltages.

$$\begin{bmatrix} i_\alpha \\ i_\beta \\ i_0 \end{bmatrix} = \sqrt{\frac{2}{3}} \begin{bmatrix} 1 & \frac{-1}{2} & \frac{-1}{2} \\ 0 & \frac{\sqrt{3}}{2} & \frac{-\sqrt{3}}{2} \\ \frac{1}{\sqrt{2}} & \frac{1}{\sqrt{2}} & \frac{1}{\sqrt{2}} \end{bmatrix} \begin{bmatrix} i_{La} \\ i_{Lb} \\ i_{Lc} \end{bmatrix} \quad (4.3)$$

Now in step two, the α-β-0 structure is converted into d-q-0 components which is called as Park's transformation.

$$\begin{bmatrix} i_d \\ i_q \\ i_0 \end{bmatrix} = \begin{bmatrix} \cos\theta & \sin\theta & 0 \\ -\sin\theta & \cos\theta & 0 \\ 0 & 0 & 1 \end{bmatrix} \begin{bmatrix} i_\alpha \\ i_\beta \\ i_0 \end{bmatrix} \quad (4.4)$$

Here θ is the angle of transformation. After the conversion of components in α-β into the d-q structure, these dc currents are then filtered so as to remove the components of ac from which harmonics are produced. So that is why a low pass filter is used for this reason. After filtering, the required source currents i^*_{sd}, i^*_{sq} are obtained in d-q structure. In the last step, reverse procedure is done. The reference currents achieved after filtering which we convert into d-q transformation are converted into structure of α – β.

$$\begin{bmatrix} i^*_{s\alpha} \\ i^*_{s\beta} \end{bmatrix} = \begin{bmatrix} \cos\theta & \sin\theta \\ -\sin\theta & \cos\theta \end{bmatrix}^{-1} \begin{bmatrix} i_{d\,(dc)} \\ i_{q\,(dc)} \end{bmatrix} \quad (4.5)$$

Now these α–β components are transformed into three phase a, b, c elements.

$$\begin{bmatrix} i^*_{sa} \\ i^*_{sb} \\ i^*_{sc} \end{bmatrix} = \sqrt{\frac{2}{3}} \begin{bmatrix} 1 & 0 & \frac{1}{\sqrt{2}} \\ -\frac{1}{2} & \frac{\sqrt{3}}{2} & \frac{1}{\sqrt{2}} \\ -\frac{1}{2} & \frac{-\sqrt{3}}{2} & \frac{1}{\sqrt{2}} \end{bmatrix} \begin{bmatrix} i_\alpha \\ i_\beta \end{bmatrix} \quad (4.6)$$

These are the calculated allusion source currents and the compensating currents are got through the subtraction of reference source currents from the load current. The three phase reference compensating currents can be written as.

$$i^*_{ca} = i_{La} - i_{sa} \quad (4.7)$$

$$i^*_{cb} = i_{Lb} - i_{sb} \quad (4.8)$$

$$i^*_{cc} = i_{Lc} - i_{sc} \quad (4.9)$$

Now these reference currents are fed to the PWM control circuit of the inverter for the generation of the switching pulses for getting the desired current and voltage signals. The block diagram of SRF control scheme is shown in the figure 3.5.

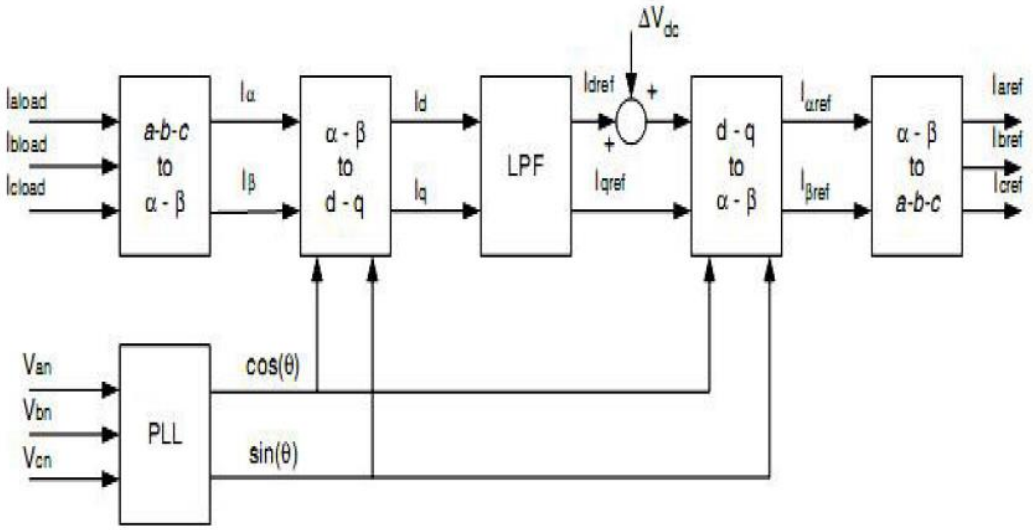


Figure 4.5 Block diagram of SRF control scheme

4.5.2 Advantages of SRF method

- It permits rapid recognition of harmonics.
- The control circuit is simple and easy to understand.
- Easily clarifies the components which are non dc.
- Activity of the controller based SRF method is fast.
- It can provide quick torque feedback in case of induction machines.
- Calculations are simple that are performed on the dc quantities.

CHAPTER 5
TEST SYSTEM AND SIMULATION RESULTS

5.1 Objectives of work

In this work, the performance of DSTATCOM in the distribution network is inspected during load disturbance state. For this, three phase to ground fault is created and this unbalances the load. The objective of DSTATCOM is to stable the effect of unbalancing of load in the source side. Since nonlinear load is connected in the load side which causes harmonics but DSTATCOM promises to eliminate the effect of harmonics of the load current to the source current and according to harmonic limit of IEEE-519 standards, it mitigates the harmonics which are more than 5% due to nonlinear load which produces effect in the source. When the harmonics are effectively compensated from the load to the supply side and when waveforms of source become balanced, power quality will get enhanced. In this thesis, it is shown how DSTATCOM prevents the source from the effects of harmonics at the load side and when the load becomes unbalanced and there is a rise in current quantity. The test system is designed in MATLAB having version 16(a). Three phase diode rectifier non- linear load with R-L is placed in the three phase four wire, 50 Hz distribution network. Generally, DSTATCOM is designed with a two level VSI but in this work, multilevel inverter is implemented in place of the conventional two level inverter. Since, MLI are meant for reducing harmonic distortions by using many number of voltage levels. The topology of multilevel inverter used is asymmetrical cascaded H-bridge inverter. For this, seven level binary based asymmetrical inverter is incorporated with DSTATCOM. The realization of seven level inverter is already described in the chapter 3. For the control of DSTATCOM, SRF method based on Park's transformation principle is used. For the triggering of switching pulses of the inverter, Alternate Phase Opposition Disposition PWM control method is used. The main objective of the work is to carry out the task performed by DSTATCOM with seven level binary asymmetrical cascaded H-bridge multilevel inverter in improving the source currents which are the reference in this case from the disturbances and unbalancing in the load in the distribution system.

5.2 Block Diagram of the Test system

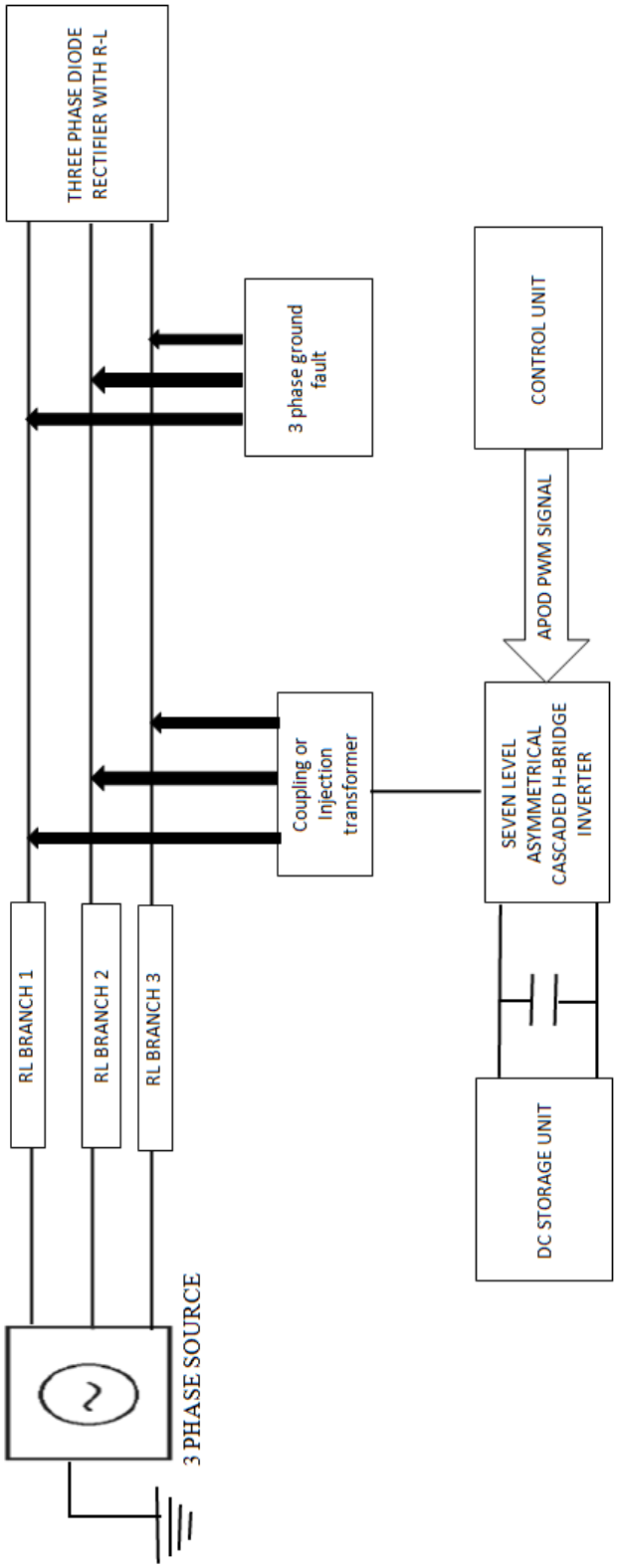


Figure 5.1 Block Diagram of Test System

The above figure shows the block diagram of the test system connected in 11 kV, 50 Hz distribution system. DSTATCOM is installed between the source and the load known as point of common coupling. Seven level asymmetrical cascaded H-bridge inverter with APOD control strategy proposed which aims to mitigate the harmonic effects. Three phase diode rectifier nonlinear load is connected in the system which causes harmonics in the load side which DSTATCOM reduces these harmonics in the source side. When a three phase to ground fault occurs in the system, load becomes unbalanced but with the installation of DSTATCOM, it makes the source balanced. For the determination of reference source currents, SRF method is employed. Injected shunt current is achieved from the difference between load and the source current. Seven level CHB inverter consists of 2 H-bridges in each phase with 8 IGBT switching devices per phase. When the procedure of calculating reference source current gets finished, all the current and voltage signals are sent to the APOD PWM control circuit of the 7 level inverter for generating the switching pulses for producing desired current and voltage waveforms. The control circuit of the proposed PWM strategy controls the performance of IGBT based switching devices used in the inverter.

5.3 SIMULATION PARAMETERS

Table 5.1 Parameters of test system

Parameters of the system	Ratings
Base Voltage	11 kV
Source Voltage	400 V
Single phase to neutral voltage	230 V
Frequency	50 Hz
Dc voltage of each phase of inverter	100 V, 200 V
Dc bus capacitance of 7 level inverter; C1, C2 for each phase	0.012F, 0.024F
Source resistance	0.1 ohm
Source inductance	0.9mH
Load resistance	30 ohm
Load inductance	1mH
Fault resistance, ground resistance	0.001 ohm, 0.01 ohm
Inverter series inductance	1mH
Reference frequency	50 Hz
Carrier frequency	5 kHz

5.4 WAVEFORM ANALYSIS

The results of simulation for load voltage and load current, constituting unbalancing source voltage, source current and compensating current of DSTATCOM are analyzed below.

5.4.1 Load Voltage and Load Current

A three phase to ground fault is occurred between duration of 0.2 seconds to 0.4 seconds. In this duration, load voltage becomes zero and there is a sudden rise in the load current. This causes load unbalancing in the system. Little bit effect of non-linearity is coming in the load voltage. The magnitude of the load current and voltages are not similar. These loads can affect the source which is fed to the consumers which results in poor power quality of power.

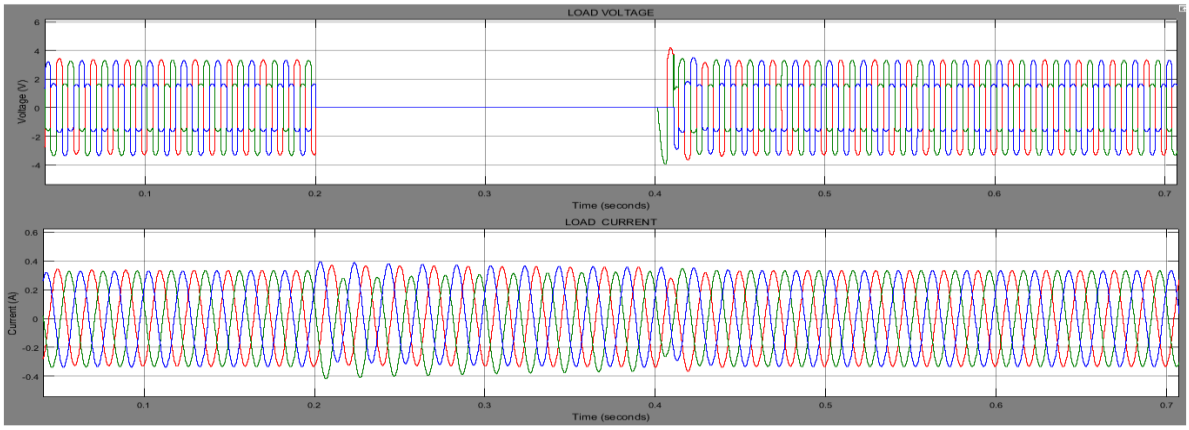


Figure 5.2 Waveforms of load voltage and load current

5.4.2 Source voltage and Source current

DSTATCOM effectively satisfies the load unbalancing caused by the three phase ground fault. The main function of DSTATCOM is to make the source current balanced with each phase having equal in magnitudes. The load currents which are having changing load condition as shown in the figure are supplied by DSTATCOM to satisfy the unbalancing condition to make the source currents balanced which are supplied to the consumers resulting in improved power quality. The unaffected source voltage and current waveforms are shown below.

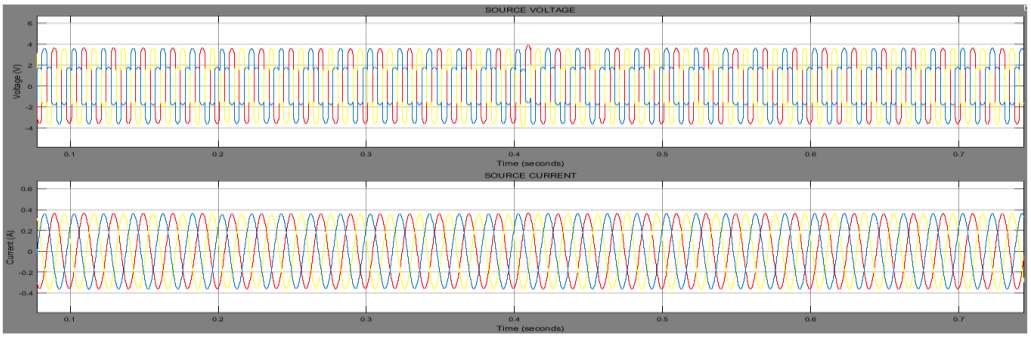


Figure5.3. Waveforms of source voltage and source current

5.4.3 Compensator Current

The compensator current is the shunt injected current of DSTATCOM. It is equal to the difference between load current and the source current. After the reference source currents of all the three phases get extracted from the SRF control method of DSTATCOM, these reference source currents get subtracted from the three phase load currents to obtain desired compensating current of DSTATCOM. The waveforms of compensating current is shown below. In starting, initially capacitor is uncharged. When the capacitor is getting charged through switching pulses. The current flowing up to some duration of fully charged, the current is unbalanced. After all capacitors are balanced then DSTATCOM current is balanced with the source current.

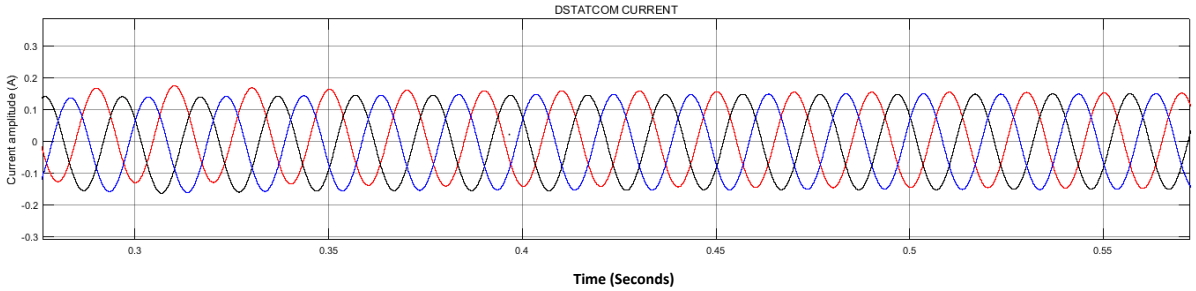


Figure 5.4 Compensator current

5.5 Harmonic Analysis

The harmonics in the load current and source current are shown below in figure 5.5. Load current has harmonics more than source current.

1. LOAD CURRENT 2. SOURCE CURRENT

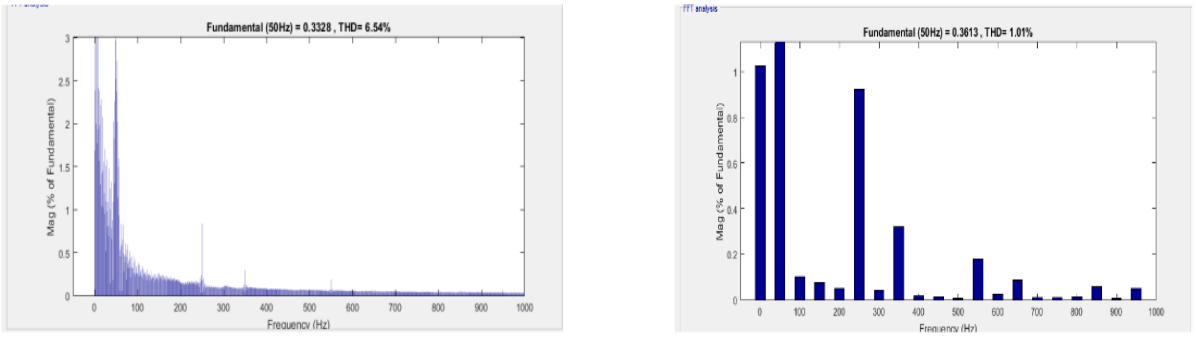


Figure 5.5 THD analysis of load and source current

Table 5.2 Comparison between load and source current

PARAMETER	THD (%)
LOAD CURRENT	6.54
SOURCE CURRENT	1.01

DSTATCOM has successfully compensated the harmonics present in the load current having 6.54% due to presence of nonlinear load to 1.01% at the source side which is below than 5% according to IEE-519 standards. Connecting DSTATCOM in the distribution network is next to the power quality improvement. DSTATCOM balances the source with the changing load condition and reduces the harmonics present in the load side that are given to the source side.

CHAPTER – 6
CONCLUSIONS AND FUTURE SCOPE

6.1 Conclusions

In this work, role of MLI with DSTATCOM for improving power quality is investigated. For this, Asymmetrical Cascaded H-bridge topology of multilevel inverter is selected. Seven, Nine, Eleven and Thirteen levels of asymmetrical topology are realized in MATLAB software. A comparative analysis is done between these four levels on the basis of THD. through the simulation results. The magnitude of calculating dc voltage sources for each level is selected through the methods of arrangement of values of dc sources. Level shifted based Alternate Phase Opposition Disposition multicarrier sinusoidal PWM strategy with fixed switch frequency is used for the generation of gate signals. From the analysis of harmonic contents, it is observed that as we increase the number of levels, THD gets decreased and more the waveform almost reaches in the sinusoidal shape.

After realizing all these four inverters, seven level out of the four levels is used for the implementation in the custom power device, DSTATCOM for reducing the harmonics in the distribution network and load changing conditions.

DSTATCOM is proposed in the distribution system with asymmetrical seven level cascaded H-bridge inverter in place of a 2 level VSI. The SRF control algorithm based on d-q conversion principle used for the calculation of reference currents. Alternate Phase Opposition Disposition Multicarrier Sinusoidal PWM strategy is used in this case also for producing the required current and voltage waveforms. Performance of seven level Asymmetrical Cascaded H-bridge inverter based DSTATCOM in the distribution network is investigated. A conclusion is drawn that seven level inverter based DSTATCOM is found to be effective in reducing the harmonics present from load current due to the nonlinear load which affect the source current. It has compensated current harmonics from 6.54% to 1.01% which is less than 5%. Balanced waveform of three phase source current is achieved.

The performance of asymmetrical cascaded H-bridge inverter is quite better than a simple 2 level VSI in resolving PQ problems by eliminating harmonics and unbalancing effect of the load. It can also be concluded that with the effect of APOD PWM technique, all the harmonics are get mitigated.

6.2 Future Scope

Some of the future proposals for the further research work in this area can be:

- Further higher level of asymmetrical inverter can be implemented with DSTATCOM.
- Instead of classical PI controller, latest techniques such as artificial neural network, fuzzy logic controller can be used for DSTATCOM.
- Different control schemes for the generation of reference source currents such as Instantaneous Reactive Power control or Adaline based control can be used.
- Variable-frequency multi-carrier sinusoidal PWM, phase shifted SPWM or inverted sin PWM strategies can be used in asymmetrical CHB MLI. For the generation of switching pulses in the case of DSTATCOM, closed loop PWM methods like hysteresis current controller can be incorporated.
- Performance of asymmetrical cascaded H-bridge multilevel inverter can be investigated in remaining other two custom power devices and FACTS devices also.
- Different algorithms of dc source voltage arrangement like ternary, fifnary, quasinary etc. can be used in asymmetrical multilevel inverters.
- Different ac drives that feed FOC or DTC scheme can also be used for testing DSTATCOM.

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