Performance Analysis of Mixed-MWCNT as VLSI Interconnects for Nano-Scaled Technology Nodes

A Thesis Submitted in Fulfillment of the Requirement for the Award of the Degree of

MASTER OF TECHNOLOGY

in

VLSI DESIGN

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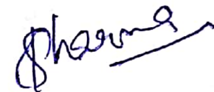
JUNE, 2017

DECLARATION

I, **Shairy Sharma** hereby declare that the work presented in this thesis entitled **"Performance Analysis of Mixed-MWCNT as VLSI Interconnects for Nano-Scaled Technology Nodes"** in partial fulfillment of the requirement for the award of degree of Master of Engineering submitted at Electronics and Communication Engineering Department, Thapar University, Patiala is an authentic record of work carried out under supervision of **Dr. Karmjit Singh Sandha** (Assistant Professor, ECED, Thapar University, Patiala). The matter presented in this has not been submitted either in part or full to any other university or institute for the award of any other degree.



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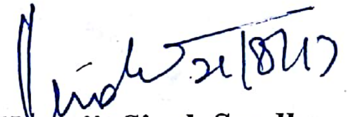

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ACKNOWLEDGEMENT

I take this opportunity to express my profound sense of gratitude and respect to all those who helped me through the duration of this dissertation. I acknowledge with gratitude and humility my indebtedness to **Dr. Karmjit Singh Sandha, Assistant Professor,** Electronics and Communication Engineering Department, Thapar University, Patiala, under whose guidance I had the privilege to complete this dissertation. I wish to express my deep gratitude towards him for providing individual guidance and support throughout the dissertation work. I convey my sincere thanks to **Head of the Department, Dr. Alpana Aggarwal** as well as **PG Coordinator; Dr. Hem Dutt Joshi** and **Program Coordinator; Dr. Anil Arora of ECED,** entire faculty and staff of Electronics and Communication Engineering Department for their encouragement and cooperation.

My greatest thanks to all who wished me success especially my family. Above all, I render my gratitude to the Almighty who bestowed ability and strength in me to complete this work.

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ABSTRACT

With the scaling in technology, the resistivity of the copper initially being used as an interconnect material is increasing due to surface roughness and various kind of scattering. The carbon nanotubes (CNTs) as a better choice of material for VLSI interconnects have been studied. These are further of two types single walled carbon nanotubes (SWCNTs) and multi-walled carbon nanotubes (MWCNTs). The Multi-walled carbon nanotubes (MWCNTs) have become the preferred interconnect material for the nanoscale technology nodes than SWCNTs due to its longer mean free path and other properties. It is important to grow MWCNT bundle structures as interconnect for silicon chip design.

In this report the performance analysis of MWCNT bundles containing several MWCNTs, with identical and different number of shells is presented. The structures are categorized into two types: MWCNT bundle (MW) which contains all the MWCNTs with same number of shells and Mixed MWCNT bundle (MMW) which contains MWCNTs having different number of shells. The Equivalent Single Conductor (ESC) model is produced by employing, Multi-conductor transmission line (MTL) model theory for all the structures. Further, by using proposed ESC model the performance on the basis of propagation delay, power dissipation and power-delay product (PDP) measurements is estimated through driver interconnect load (DIL) model for different interconnect lengths between different structures.

The performance evaluation is presented for at nano-scaled technology nodes (viz. 32nm, 22nm and 16nm). It's shown through the results that the performance of mixed MWCNT (MMW) structures is better in all aspects as compared to MWCNT (MW) for nano-scaled technology nodes.

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LIST OF ABBREVIATIONS

IC	Integrated Circuit
CNT	Carbon NanoTube
MFP	Mean Free path
SWCNT	Single Walled carbon Nanotube
MWCNT	Multi walled Carbon Nanotube
ESC	Equivalent Single Conductor
MCC	Multi Conductor Circuit
MW	Multi Walled bundle
MMW	Mixed Multi Walled bundle
PDP	Power Delay Product

CHAPTER 1

INTRODUCTION:

With the technology advancement, device size has compacted year by year and at the same time, the transistors' number on an integrated circuit (IC) has been increased. In fact, the co-founder of Intel; Gordon Moore, in 1965 after carefully observing the emerging trends, has made a prediction that the number of transistors per square inch of the ICs will almost get doubled every year, which will although lower the relative cost but will significantly increase the required power. Moore estimated this trend would be followed in the coming future; however the technology advancement rate has long been surpassed his expectations and at present deep sub micron technology levels have been reached.

The transmission-line effects have not been a serious concern in CMOS VLSI chips until recently, since the gate delays due to capacitive load components dominated the line delay in most cases. But as the fabrication technologies move to finer submicron design rules, the intrinsic gate delays tend to decrease significantly. By contrast, the overall chip size and the worst-case line length on a chip tend to increase mainly due to increasing chip complexity, thus, the importance of interconnect delay increases in submicron technologies. In addition, as the widths of metal lines shrink, the transmission line effects and signal coupling between neighboring lines become even more pronounced [1].

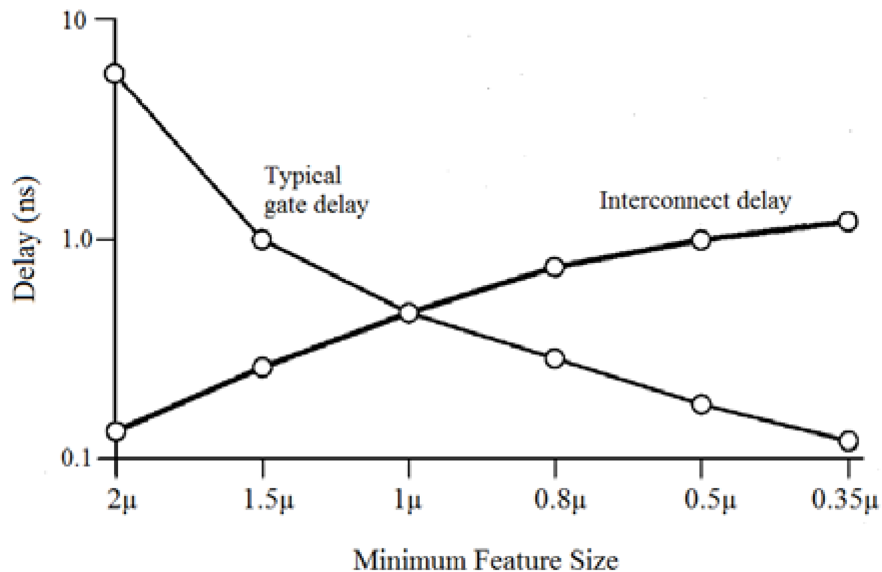


Figure 1.1: Variation in the Interconnect and gate delay over the technology scaling [1]

In Figure 1.1 it is been observed that after reaching the submicron technology level, the interconnect delay starts to dominate gate delay.

1.1 INTERCONNECTS:

Electrical connections between two or more nodes of the circuit or system formed in the silicon chip are formed by VLSI interconnects which are a thin film of conducting material. All components in an IC are connected with interconnects. Interconnections are used to provide clock, power and ground supply to the device and also to connect various devices by giving output of one as an input to another [2].

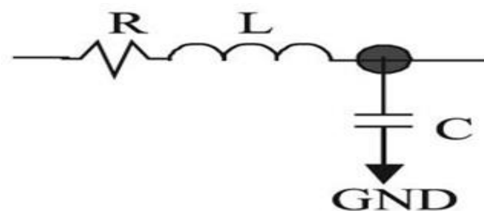


Figure 1.2: RLC equivalent of interconnect wire [3]

It is a 3D structure with resistance and capacitance associated to it as shown in Figure 1.2. Interconnects act as a transmission line and delay caused by them in the circuit is a factor of important concern as technology is scaled down because with scaled down technology more number of transistors etc. are able to be placed on a single chip, so length of interconnects connecting them increase which can lead to increase in delay.

1.1.1 Types Of Interconnects

Interconnects are categorized on the basis of their length as local, semi-global and global [4].

Local interconnects**:** These interconnects are lowest level of interconnects. These are used in localized region of a chip to provide electrical path between nearby nodes. They commonly connect gates, sources and drains in MOSFETs. In MOSFET technology, polycrystalline silicon, a local interconnect, also serves as gate electrode material. Silicidal drain, source and gate regions also serve as local interconnects.

Semi-global interconnects**:** These interconnects are used for conducting nodes which are at distances more than those of local interconnects but lesser than those of global interconnects. These are usually used to connect devices within a block.

***Global interconnects*:** These interconnects are used for connecting nodes which are at considerable distance from each other. These usually connect between blocks which include power, ground and clocks. These often travel large distances between different devices and through different parts of the circuit.

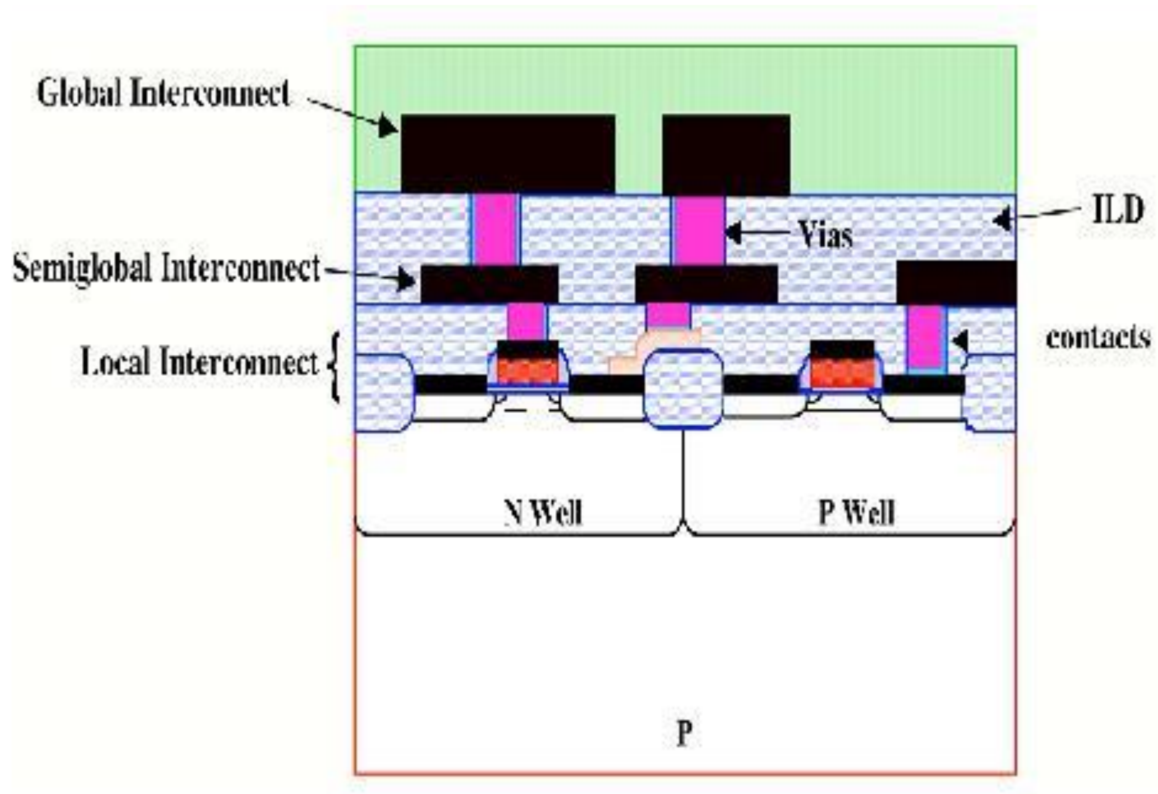


Figure 1.3: Various levels of interconnect on the basis of their length [4]

1.1.2 Materials Used As VLSI Interconnects And Problems With Existing Materials

1.1.2.1 Aluminum As An Interconnect

The most widely used material as interconnect earlier was aluminum due to its good conductivity and adherence on silicon dioxide. But due to scaling down of technology as the density of device increased current density for interconnects increased. In case of aluminum at higher current density considerable amount of electromigration takes place. Electromigration is the transport of material caused by the gradual movement of the ions in a conductor due to the momentum transfer between conducting electrons and diffusing metal atoms. In microelectronics and related

structures this effect is important as high current density is involved. This effect increases with decrease in structure size such as integrated circuits [5].

1.1.2.2 Copper As An Interconnect

Due to limitations imposed by aluminum, copper with higher conductivity and a material with higher resistance to electromigration than aluminum is considered as an interconnect with scaling down of technology. Copper is capable of withstanding five times more current density than aluminum with equal reliability for IC applications. Copper due to its higher electrical conductivity and relatively higher melting point and other advantages over aluminum has evolved as interconnect material especially for submicron and deep sub micron high density and high performance chips. Table 1.1 represents the comparison in properties of Al and Cu.

Table 1.1: Comparison between Copper and Aluminum for interconnect applications

Property	Aluminium	Copper
Bulk resistivity (μΩ-cm)	2.67	1.70
Melting Point(K)	933	1357

Due to these advantages copper is a good choice for interconnect material for sub-micron and deep sub-micron higher performance chips. As the technology further scales down, the copper interconnects’ cross-sectional area decreases substantially owing to which the effects like grain boundary scattering and surface roughness become more significant leading to the increased resistivity. This leads to an increase in propagation delay, power dissipation and electro migration [6, 7].

The problems which arise with scaling down of feature size are discussed.

Electro migration*:* Electro migration is caused by the gradual movement of ions in a conductor due to the due to the transfer of momentum between the conducting electrons and the diffusing metal atoms. It can eventually lead to loss of connection or circuit failure. The resistivity of copper to electro migration is high. Continuous scaling can lead to high current densities. Under such conditions, interconnects can experience el1 ectrical failure due to electro migration.

Grain boundary effect: Grain boundaries are the internal interfaces that separate neighboring disoriented single crystals in a polycrystalline solid [8]. The interface between two grains, or

crystallites, which are disoriented with respect to each other in a polycrystalline material is called a grain boundary. Grain boundary areas contain the atoms that have been perturbed from their original lattice sites, dislocations and impurities that have migrated to lower energy grain boundary. Grain boundaries are defects in the crystal structure which tends to decrease the electrical and thermal conductivity of the material. Copper has a crystalline structure normally, but when it is engineered for use it becomes polycrystalline in nature. This new structure is made up of many small single crystals having different orientation with respect to each other. Grain boundary causes scattering of electrons leading to reduction in mobility of electrons. The resistance of such conductor is inversely proportional to the size of grains. The smaller the grains, the larger will be the resistance and electrons would travel slowly.

Surface scattering*:* As the wire dimensions are decreasing, the electron mean free path becomes comparable to the wire dimensions causing scattering from the interface. The mobility of electrons decreases as the dimensions decrease. The mathematical expression that governs the scattering theory leads up to the following expression for surface-scattering-dependent resistivity [8].

Figure 1.4 Surface scattering phenomena in a copper wire of smaller lateral dimensions [9]

Diffusion Barrier Width**:** Copper diffuses into neighbouring dielectric silicon as it is very mobile in SiO2. This causes contamination of silicon devices and damage in FETs. To prevent this, copper wires are bounded by the diffusion barrier. Due to high resistivity of this barrier, there is increase in effective resistivity of copper wire. With the technology scaling, there is a in cross sectional area of the copper wires, but the diffusion barriers do not scales as quickly due to the reliability constraints.

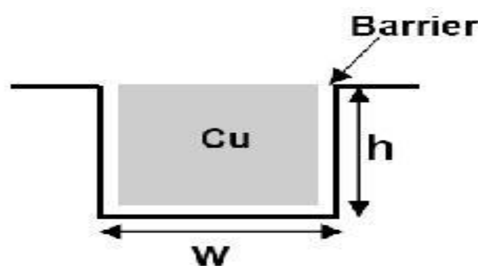


Figure 1.5: Cross-sectional view of interconnect showing barrier deposited [8].

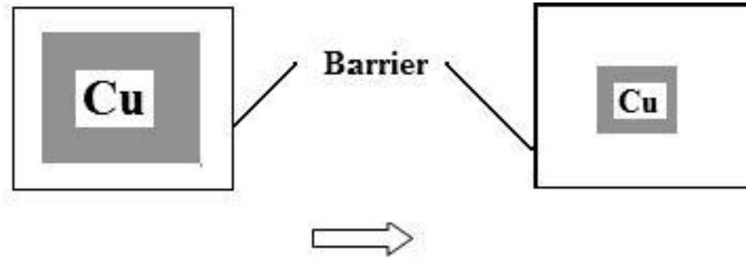


Figure 1.6: Variation in barrier width with scaling of interconnects [8].

This gradually leads to larger fraction of the cross sectional area being occupied by the diffusion barrier. This ultimately leads to an increase in the resistivity of wire. So, next we see how Carbon nanotubes are becoming the most sought after material for next generation VLSI interconnect technology**.**

1.1.2.3 Carbon Nanotube As A VLSI Interconnect

Carbon nanotubes were formally found by Sumo Lijima of NEC-Japan in 1991. Scientists have found out that CNTs have exceptional current carrying capabilities of 10^9 A/cm^2 which makes them suitable for interconnect applications and hence can be used as very long and thin interconnects at more scaled down technology nodes than copper.

Carbon nanotube(CNT) are hollow cylinders of graphite sheets (called graphene) with a radius of nanometer scale and length ranging from hundreds of nanometres to microns or even millimetres. Carbon nanotubes are carbon allotropes that are made up of carbon atoms in the form of hexagons and are covalently bonded (each bond being a sp^2 bond or bonded to three atoms) to each other and rolled into tubes.
The aspect ratio (length to diameter ratio) of CNTs is very high and is of the order of 10^4. So, it is essentially a 1D quantum wire with special characteristics. Ballistic conduction takes place in these 1D conductors. Hence the electron movement is non diffusive in nature. This phenomenon reveals that electrons travel like waves in the structure and also they have large mean free paths (MFPs). So, CNT based interconnects are suitable for high frequency integrated circuits that is the future of the technology [10].

Table 1.2: Properties of CNTs [11] [12]

Property	Value
Density	1.33 g/cm^3
Bandgap	0eV for conducting 0.5eV for semiconducting
Current density	10^{14} A/m^2
Thermal conductivity	5800 W/mK
Phonon mean free path	100 nm
Resistance range	7kΩ-100kΩ

1.2 CLASSIFICATION OF CNTS:

1.2.1 On The Basis Of Chirality:

There are many ways to roll a sheet into a cylinder thus resulting in different diameters and microscopic structures of the tubes. The angles at which the graphene sheets are rolled are known as the chiral angles. By using the unit vectors a1 and a2, as in Figure 1.7, with chiral indices given by n and m, geometric parameters of carbon nanotube can be defined.

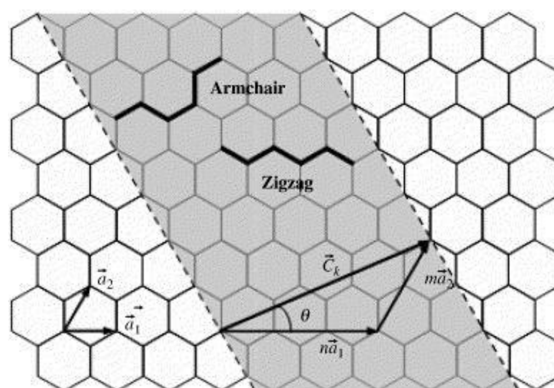


Figure 1.7: Illustraition of chiral vector C in terms of vector a_1 and a_2 [13]

The two main aspects of nanotubes that determine their electrical properties are their chirality and diameter. The chiral vector C represents where the graphite sheet attaches to itself to form the nanotube. The vector is directed along the circumference of the tube and perpendicular to its

axis. The magnitude of the vector is equal to the diameter of the tube, while its direction indicates its chirality. Carbon nanotubes have three distinct categories classifying their chirality:

- Armchair.
- Zigzag.
- Chiral.

CNT tubes are also classified as being either metallic or semi conducting. All armchair tubes, described by n = m, are metallic. Zig-zag tubes, described by m=0, are metallic if n is a multiple of three. The condition for a nanotube to be conducting can be stated as the difference between n and m must be a multiple of three or zero. The conditions for the nanotubes to be metallic are equivalent to the chiral vector intersecting the points were valence and conduction bands in the first brillouin zone of the equivalent graphite sheet are degenerate and therefore no band gap occurs. For the tubes having a band gap, the band gap is inversely proportional to the diameter of the tube [14].

1.2.2 On The Basis Of Structure And Number Of Shells As:

- Single Walled Nanotubes (SWCNT)
- Multi Walled Nanotubes (MWCNT)

1.2.2.1 Single-Walled Carbon Nanotubes

Single Walled CNT (SWCNT) consists of a single layer of graphene sheet seamlessly wrapped into a cylindrical tube as shown in Figure 1.8. They are generated when a two dimensional graphene sheet of a certain size that is wrapped in a certain direction. SWCNTs have only one layer of grapheme sheet with diameters of 0.7 to 10 nm.

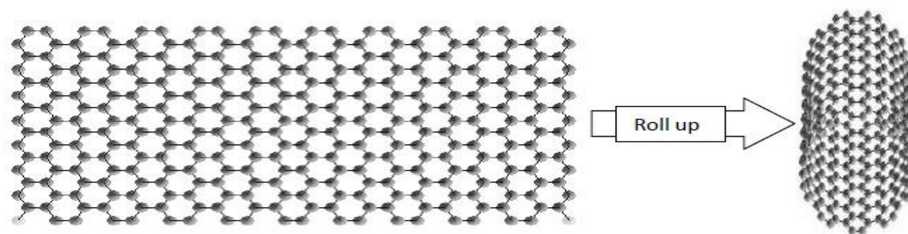


Figure 1.8: Rolling of grapheme sheet to form SWCNT [15]

1.2.2.2 Multi-walled carbon nanotubes

Multi walled carbon nanotubes (MWCNT) consist of concentric CNT cylinders held within each other by vander Waals forces. The distance between shells is approximately 3.4Å, which is the vander Waals distance for two graphite carbon lattices [15]. An example of a MWCNT is shown in Figure 1.9. There are two models which can be used to describe the structures of multi-walled nanotubes. In the Russian Doll model, sheets of graphite are arranged in concentric cylinders. In the Parchment model, a single sheet of graphite is rolled in around itself, resembling a scroll of parchment or a rolled up newspaper.

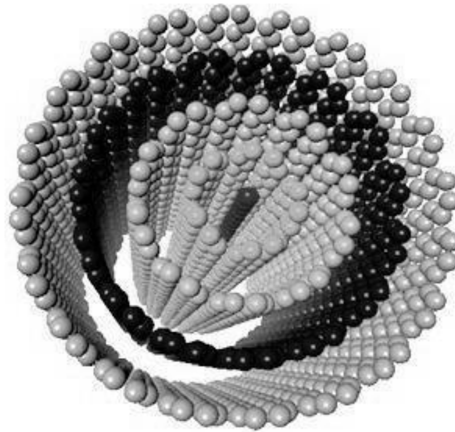


Figure 1.9 Multiwalled carbon nanotube (MWCNT) [15]

1.3 SWCNT AS AN INTERCONNECT

SWCNT is the basic structure of CNT consisting of one shell of rolled up Grapheme sheet. Depending upon the way it is rolled or its chirality it can have armchair, zig zag or chiral configuration making it metallic or non-metallic in nature. It is a zero bandgap semiconductor. The high current density of electron carriers (~10^9 A/cm^2) in metallic CNTs is due to the reduced electron-phonon scattering, strong bonding and ability to conduct at very high temperatures [16, 17]. These properties make them ideal for interconnect applications. Distribution of metallic and semiconducting CNTs in bundle is very significant for optimizing the conductance. Diameter dependence of resistance of SWCNT bundles is also important to determine the overall conductivity. The factors that are responsible for the resistance of CNT bundles are individual nanotube diameters, density of nanotubes in the bundle and the bundle's geometric configuration. Resistance of SWCNT bundles reduces 90% in comparison to Cu interconnects if the diameter is 0.5nm whereas it reduces by 50% when the diameter is 1nm. The diameter of a single walled nanotube is normally considered as 1nm [18]. Therefore, one third of an SWCNT

bundle contains metallic CNTs in it. So, in scaled technologies, more metallic CNTs are needed to keep bundle resistance independent of bias voltage. CNTs in a bundle have weak coupling and hence carry currents independent of each other [19-22]. Ideally, the CNT is considered to be placed over a ground plane as shown in Figure 1.9

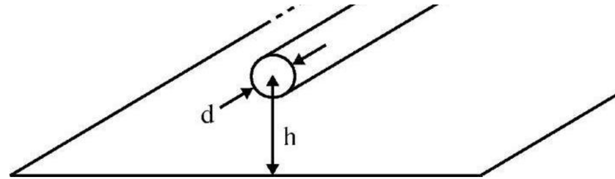


Figure 1.10: CNT placed over a ground plane, Equivalent Structure of Carbon nanotube [2].

This equivalent circuit is then used in analysis and simulation of interconnect performance. The separation between the nanotube and the ground is ‘y’ and the diameter of the SWCNT is‘d’. Assuming SWCNT to be in cylindrical form, an electrical equivalent of the structure as shown in Figure 1.10 as-

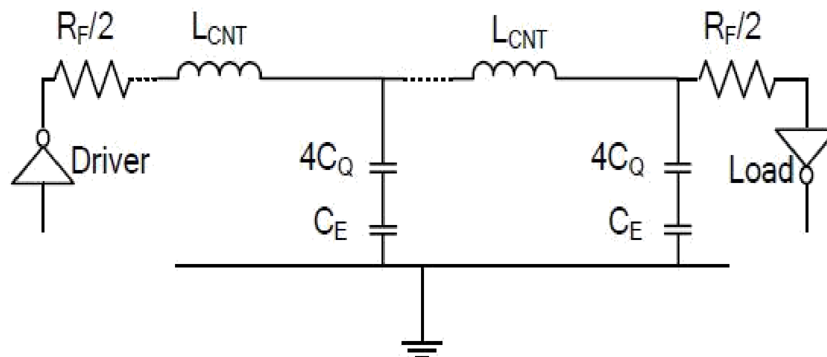


Figure 1.11: Equivalent RLC circuit for an isolated SWCNT [2].

In practical reality, not all CNTs of a bundle are metallic. Non-metallic SWCNTs are treated as not contributing to current conduction and their presence is taken into account by considering “Sparsely” populated bundles.

Due to the lack of control on chirality, any bundle of SWCNTs consists of metallic as well as semi-conducting nanotubes (the semi-conducting CNTs do not contribute to current conduction in interconnects). Although multi-walled CNTs (MWCNTs) are predominantly metallic, it is difficult to achieve ballistic transport over long lengths with them. Single-walled CNTs (SWCNTs) on the other hand, have electron mean free paths of the order of a 1 micron. Hence, in the domain of interconnects, metallic SWCNTs are the preferred candidates.

1.4 MWCNT AS AN INTERCONNECT:

The structure of MWCNT is more complex than SWCNT. MWCNTs have concentric shells that are either metallic or semiconducting. The adjacent shells in an MWCNT are separated by 0.34nm due to the vander Waal force of attraction. The number of conducting channels per shell depends on K_BT, where K_B and T are Boltzmann constant and temperature respectively. Each shell has different band structure and hence, complex analysis is required for studying its properties. The structure of an MWCNT placed over a ground plane is shown in Figure 1.11. This is the most widely used model for MWCNT interconnect design.

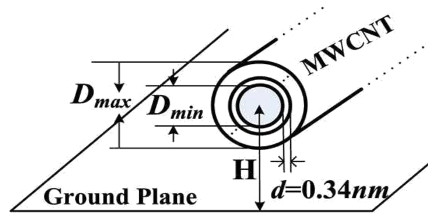


Figure 1.12: Structure of a MWCNT over a ground plane [23].

The MFP of an MWCNT is directly proportional to its diameter irrespective of whether it is metallic or semiconducting. Due to the presence of more conduction channels, MWCNTs exhibit better conductivity than SWCNTs. However, perfect contacts should be made to all the shells to avoid high contact resistance. Multiple shell conduction is possible at higher temperatures because of more conducting channels inside. An isolated MWCNT is placed on an infinite ground plane and the concept behind conduction of multiple shells was explained earlier [23]. MWCNTs are best suited for both intermediate and global interconnects. When compared with Cu, MWCNTs have shown enhanced improvements of signal delay.

Figure 1.12 shows the equivalent distributed circuit model for an individual shell of MWCNT where R_{mc} is the imperfect contact resistance, R_Q is the quantum contact resistance, R_S is the scattering-induced resistance, L_K and L_M are the kinetic and magnetic inductances respectively, and C_Q and C_E are the quantum and electrostatic capacitances, respectively.

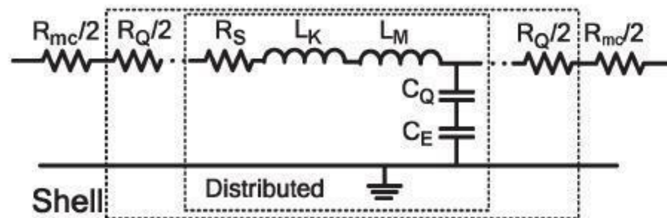


Figure 1.13: Equivalent distributed circuit model of an individual shell [23].

MWCNTs are proposed as long global interconnects as they have large conductivities at long lengths. As these nanotubes are long and have large diameters, their MFP also is large. The spacing between two adjacent shells is given by the van der Waals force of attraction (0.34 nm). Conductivity models of MWCNTs are further studied in a comprehensive distributed circuit model for MWCNTs is described in [23]. Here, an isolated MWCNT is considered on an infinite ground plane. The concept behind conduction of multiple shells is further explained here.

The various resistances associated with MWCNTs are quantum contact resistance R_Q (=12.9kΩ), scattering induced resistance R_S, and imperfect contact resistance R_{mc}. R_S and R_Q are intrinsic and R_{mc} is due to fabrication process. R_S is present in only larger than MFP nanotubes. Figure 1.13 shows the circuit of an MWCNT interconnects. The MFP of a MWCNT is directly proportional to its diameter irrespective of whether it is metallic or semiconducting.

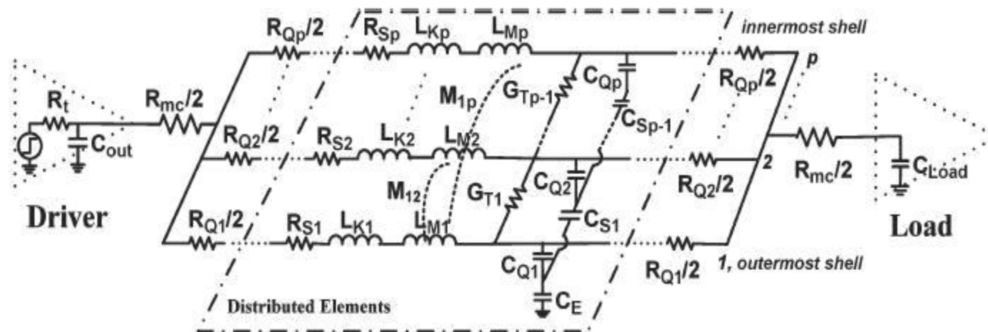


Figure 1.14: Equivalent distributed circuit model of an MWCNT with p shells [23].

Normally, the magnetic and kinetic inductances are measured per unit length. The magnetic inductance L_M is one to two orders smaller than the kinetic inductance L_K and hence, is neglected in the literature. The quantum capacitance C_Q is calculated as ≈193 aF/µm. Unlike SWCNT bundles, MWCNT structures cannot be converted into simple circuit models since they have shells with varying diameters. This means different shells have different channel numbers and varying MFPs giving rise to different circuit parameters. So, these parameters cannot be combined in a way like in SWCNT bundles. Also, the potentials are different for different diameters and hence, shell to shell electrostatic coupling capacitance is present. It will be very high due to small separation between adjacent shells. The tunneling phenomenon in MWCNTs is explained and the equivalent circuit with RLC parameters is shown [23]. The attractiveness in MWCNTs lies in their independence on chirality. They are very useful in immediate applications as global and intermediate interconnects. Further, they are studied as power interconnects at

intermediate level [22]. At 50 nm diameter, they provide 2.3 times smaller sheet resistance compared to Cu.

As the diameter of each CNT and length of the CNT bundles increases, the relative stability increases. M.S. Sarto, *et al.* [24] presents a rigorous work on the equivalent single conductor (ESC) transmission line model of MWCNTs that is derived from the complex multi-conductor model. Generally, metallic nanotubes are modelled as 1-D conductors having *n* conducting channels in parallel and 6only one of the two sub bands crossing the Fermi level. Including the spin degeneracy, CNTs have *n* =2. The ESC model is applicable till 10GHz with a relative percent error of 1% and another few percent as the frequency increases to 50GHz and beyond.

1.5 MIXED MWCNT BUNDLES AS AN INTERCONNECT:

SWCNT has a drawback that its growth type is not controllable, it can either be metallic or semiconductor and this cannot be determined beforehand. SWCNTs with metallic chirality are better conductor than Copper [25, 26], but this cannot be said for SWCNTs with semiconductor chirality Therefore, nowadays multi walled carbon nanotubes (MWCNTs) is attracting researchers more because of the unique electrical, conductive and thermal properties they exhibit [27-30]. MWCNTs have large diameter and diameter dependent MFP as compare to SWCNT bear higher number of conducting channels at deep sub-micron technology nodes. Moreover, the current carrying capacity of MWCNTs is comparable to SWCNTs, and former can be fabricated more easily than latter, due to more efficient control of the growth process [31]. The former experimental researches [32] concluded that only the outermost shell in MWCNT was the only contributor of conductance because of its contact with metal, whereas the inner shells are being isolated which results in almost negligible effect on conductance. However, with recent fabrication facilities, several researchers have reported low resistance obtained with the proper contacts made for the inner shells as well. [33-35]

Yilmazoglu et al. [36] said that, a lot many of free space is wasted upon in the fabrication MWCNTs bundle containing all MWCNTs with equal diameters, thus inadequately utilizing the space. Also, the fabrication of densely packed bundle, which contains all the MWCNTs of same number of shells (i.e. equal diameters) has turn out to be even hard. Thus, in present state of affairs, researchers have started analyzing the models and structures for bundles in which different diameter MWCNTs are being used [37], but the impact of technology scaling on the various Mixed MWCNTs bundles structures had not been considered. This paper proposed the

diameter dependent parasitic such as resistance, inductance and capacitance for different Mixed-MWCNT interconnects structures along with the propagation delay, power and PDP comparison for different technology nodes. To achieve the required results, this paper categorizes MWCNT bundles into two parts: one with all the MWCNTs having same number of shells (i.e. equal diameters) called as MWCNT bundle (MW) and secondly those containing MWCNTs with dissimilar number of shells (i.e. different diameters) called Mixed MWCNT bundle (MMW). An Equivalent Single Conductor (ESC) model has also being developed for these structures and performance for delay, power and PDP is evaluated.

1.6 THESIS ORGANIZATION

The organization of the report is as follows:-

CHAPTER 1 – This chapter gives an introduction to CNT as an interconnect. Various types of CNTs are discussed. Parameters required for the analysis of MWCNT as an interconnect is also studied in this chapter and an introduction to the Mixed MWCNT bundles are also talked about.

CHAPTER 2 – This chapter discusses various literature surveys on origin of CNT as a VLSI interconnect and performance analysis of SWCNT, MWCNT and Mixed MWCNT as an interconnect.

CHAPTER 3 - This chapter describes the methodology used for evaluating the objectives proposed in previous chapter.

CHAPTER 4 - In this chapter simulation results are obtained for various parameters and reasons for the variation in results are provided.

CHAPTER 6 – Based on results obtained, this chapter describes the conclusion and future scope with respect to the work done.

CHAPTER 2

LITERATURE SURVEY:

Comprehensive study of the resistivity of copper wires with lateral dimensions of 100 nm and smaller [6]

-W. Steinhögl, G. Schindler, G. Steinlesberger, M. Traving, M. Engelhardt

In this paper, the experimental results on the resistivity of the copper wire for various dimensions have been studied and the root cause for the pattern followed by these resistance values is being explained. The values of the resistances are evaluated by the resistance temperature coefficient analysis. The lateral dimensions for copper ranges from 40nm to 1000nm for width and the heights are taken to be 50, 155 and 230nm. It has been seen that for these dimensions perpendicular to the flow of current being less than 100nm, the value of resistivity increases significantly for copper wire. This increase in the value is contributed to the two scattering processes i.e. surface scattering and grain boundary scattering.

Alteration of Cu conductivity in the size effect regime [7]

-S. M. Rossnagela, T. S. Kuan

The resistance of the copper as an interconnect starts affecting by the thickness of the wire, if this thickness is of the order of mean free path (MFP) of the copper. The main contributors to this resistance increase due to reduced thickness are: surface roughness, surface and grain boundary scattering. After that, the effect of the presence of other metals on the copper has been studied and it has been found that, the presence of the metals like- Ta and Pt increases the resistivity due to more scattering by more multifaceted Fermi surfaces of theses metals. However, this process may slow down with oxidation of these metals. On the other hand, the presence of other metals like Al and Au decreases the resistivity and again followed by the oxidation of Al and further reduction in the resistivity.

Transient analysis of mixed carbon nanotube bundle interconnects [10]

-P. Uma Sathyakam, P.S. Mallick

This paper presents the hierarchal approach of modeling for the mixed CNT bundle (MCB). For this, the equivalent single conductor (ESC) model has been developed for both SWCNT and MWCNT, which is then joined to form a multiple ESC model. This model is then used to develop the multi conductor circuit (MCC) model for the complete MCB structure. These two

models are then analyzed and there delays are being compared with the conventional SWCNT bundle and MWCNT. It's found that, the performance of MCB is better than SWCNT and MWCNT in all aspects.

Performance Comparison between Carbon Nanotube and Copper Interconnects for Gigascale Integration (GSI) [11]

-Azad Naeemi, Reza Sarvari, James D. Meindl

The performance comparison is made between copper and carbon nanotubes through the physical models at the different technology nodes. Since, the propagation of wave is slow in the Single Walled Carbon Nanotubes (SWCNTs) due to the large value of kinetic inductance, the SWCNT bundles are used with the higher wave speeds. It has been found that the improvement in the interconnect performance for SWCNT bundle is not as significant at 45nm technology node. However, at 22nm technology node these SWCNT bundles can perform 80% better than copper interconnects. Thus, these performance enhancements are vital for the upcoming technology nodes and the CNTs are the future VLSI interconnects material.

Carbon Nanotubes: Synthesis, Properties, and Applications [12]

-Susan B. Sinnott, Rodney Andrews

This paper presents an insight into the various properties and processing techniques of the CNTs. Different structures of the nanotubes can be developed using various processing techniques, which has been discussed in this paper. It also emphasis on the requirement of the further study on these techniques in order to get better growth control and hence better utilize the properties of CNTs that are dependent on this growth process and it's chirality. At the end the various properties of CNTs have been discussed, which make them them the attractive material for future interconnects applications.

Single-Walled Carbon Nanotube Electronics [16]

-Paul L. McEuen, Michael S. Fuhrer, and Hongkun Park

The electronic properties and the fabrication process of the Single Walled Carbon Nanotubes (SWCNTs) are reviewed. It has been found that the SWCNTs possessing metallic and semiconducting behavior are better interconnect material than the other metals and the semiconductors. For metals they provide better conductivity and for semiconductors, they have better mobility and trans-conductance. There are however some manufacturing challenges being

faced, such as it is somehow possible to control the diameter in the growth process, but it's difficult to control the chirality and hence there metallic or semiconducting nature.

Compact Physical Models for Multiwall Carbon-Nanotube Interconnects [20]

- Azad Naeemi, James D. Meindl

This paper presents the relation between the conductivity and diameter for the Multi Walled Carbon Nanotubes (MWCNTs) at different lengths. It has been deduced that for a critical length that is around 10µm the conductivity or the number of conducting channels of the tube are independent of the shell diameters. However, it has been found that for the interconnect lengths above this critical length; the number of conducting channels are directly proportional to the diameter, whereas for the smaller lengths conductivity and diameter are inversely proportional to each other. The comparison between MWCNTs and Single Walled Carbon Nonotubes (SWCNTs) has also been performed and the SWCNTs are being found better conductors at smaller lengths. Hence, this modeling method provides a close insight on the application of Carbon Nanotubes as the VLSI interconnect at Giga scale Integration (GSI) technologies.

Interconnects in Gigascale Systems [22]

Azad Naeemi, James D. Meindl

In this paper the performance of Single Walled Carbon Nonotubes (SWCNTs), Multi Walled Carbon Nanotubes (MWCNTs) and copper are analyzed at different interconnect level applications from local to global. It has been found that, the all of these three viz. copper, SWCNTs and MWCNTs have distinctive pros and cons at different levels of interconnect lengths. Hence, there is a need of a hybrid network consisting of all these three so as to obtain the minimal delay and power dissipation.

Performance Modeling for Single- and Multiwall Carbon Nanotubes as Signal and Power Circuit Modeling and Performance Analysis of Multi-Walled Carbon Nanotube Interconnects [23]

- Hong Li, Wen-Yan Yin, Kaustav Banerjee, Jun-Fa Mao

This paper presents difference in the structure of SWCNT and MWCNT and it also provide the analysis of MWCNT as interconnect. It provides the formula for the calculation of RLC parameters in an MCC model and then based on these parameters an ESC model of a MWCNT is been derived. The simulations are performed for global, intermediate and the local

interconnect lengths. The delay analysis and its simulation results provide the effectiveness of MWCNT as compared to SWCNT and copper at intermediate and global length. This paper also discusses the impact of imperfect contact resistance. The paper concludes that for a longer interconnects (mainly global or intermediate levels); the delay caused by MWCNT is much lesser than that caused by the copper. However, for short length local interconnects copper is better than MWCNTs.

Single-Conductor Transmission-Line Model of Multiwall Carbon Nanotubes [24]

-Maria Sabrina Sarto, Alessio Tamburrano

In this paper the analytical analysis is performed to obtain the Equivalent Single Conductor (ESC) model form the Multi Conductor Circuit (MCC) model for an MWCNT interconnects. The equivalent value of the quantum capacitance and kinetic inductance for the MWCNT are derived from that of the individual shell through the various critical derivations and calculations. It has been found that, the derived results are valid for most of the MWCNT structures.

On the Applicability of Single-Walled Carbon Nanotubes as VLSI Interconnects [26]

-Navin Srivastava, Hong Li, Franz Kreupl, Kaustav Banerjee

In this paper, the complete analysis of SWCNT as a VLSI interconnect for nanoscale technology nodes is performed. The resistance values of SWCNTs are evaluated while taking the other physical parameters and imperfect contact resistance into account. The complete 3D capacitance structure is also formulated and then the delay and power are analysed and compared with copper interconnects. It's been found that CNTs can provide a reduction in delay of as low as 40% as compared to copper at global interconnects having length in order of some millimeters and that reduction in power is around four times at 22n and eight times at 22nm technology node. Hence, this paper focuses on the uses of isolated and bundle SWCNTs applicability as a better alternative from copper on nanotechnology interconnects circuits.

Current Saturation and Electrical Breakdown in Multiwalled Carbon Nanotubes [27]

-Philip G. Collins, M. Hersam, M. Arnold, R. Martel, Ph. Avouris

This paper is based on the study of the maximum energy limits that can be transported in a multi walled carbon nanotube (MWCNT). In comparison to the metal wires, MWCNTs do not suffer from the failure due tom electromigration, but may fail because of the equally sized sharp current

edges. Moreover, the chances of this failure become more pronounce with exposure to the air. As the air exposure may initiate the process by oxidizing at a particular power. Therefore, it shows better current carrying capacity and power densities in the vacuum and can reach it's maximum current withholdings efficiency.

Delay and crosstalk reliability issues in mixed MWCNT bundle interconnects [37]

-Manoj Kumar Majumder , Pankaj Kumar Das , Brajesh Kumar Kaushik

The Multi-walled carbon nanotubes (MWCNTs) have become the preferred interconnect material for the nanoscale technology nodes. It is important to grow MWCNT bundle structures as interconnect for silicon chip design. This research paper presents the analysis and performance of MWCNT bundles with several MWCNTs in a bundle, containing identical and different number of shells. The structures are categorized into two types: MWCNT bundle (MB) which contains all the MWCNTs with same number of shells and Mixed MWCNT bundle (MMB) which contains MWCNTs having different number of shells. The Equivalent Single Conductor (ESC) model is produced by employing, Multi-conductor transmission line (MTL) model theory for all the structures. Further, by using proposed ESC model the performance on the basis of propagation delay, power dissipation and power-delay product (PDP) measurements is estimated through driver interconnect load (DIL) model for different interconnect length at nano-scaled technology nodes.

Multichannel Ballistic Transport in Multiwall Carbon Nanotubes [39]

-H. J. Li, W. G. Lu, J. J. Li, X. D. Bai, C. Z. Gu

In this paper, the electrical properties of the MWCNT were studied through an experiment in a scanning type electron microscope vacuum chamber at room temperature. It was established that the MWCNT tube has a very large current carrying capacity, with the maximum current being reaching to the level of 7.27mA with a very low resistivity. This shows that the MWCNTs show almost ballistic flow of electrons. It can be attributed to the fact that, the MWCNTs with larger diameters have longer mean free path and moreover, the multiple walls also contribute to the electrical transport mechanism.

Study on Equivalent Single Conductor Model of Multi-Walled Carbon Nanotube Interconnects [44]

- Min Tang, Jiaqing Lu, Junfa Mao

In this paper, the study on equivalent single conductor (ESC) model is investigated. The ESC model provides a more easier and efficient approach for the analysis of various CNT structures. This paper, the validity and the accuracy of ESC model is determined when the impact of the imperfect contact resistance and tunneling conductance are introduced both for single and coupled multi walled carbon nanotubes. It is seen that the ESC model is accurate for the variations in tunneling conductivity, but the accuracy reduces for the changes in contact resistance.

Various bonding configurations of transition-metal atoms on carbon nanotubes: Their effect on contact resistance [46]

-Antonis N. Andriotis, Madhu Menon, George E. Froudakis

In this paper, the various factors affecting the carbon nanotubes and transition metals have been discussed. Also, the range of all values, the contact resistance may have is determined. The effect of the various metal types making contact with the carbon nanotubes (CNTs) has also been discussed. It is found that the early 3d elements i.e. Sc, Ti, V provides less metal-contact resistance as compared to late 3d elements.

Mixed carbon nanotube bundles for interconnect applications [48]

Suraj Subash, Masud H. Chowdhury

This paper portrays the usefulness of the carbon nanotubes (CNTs) as the VLSI interconnects material over the previously used materials. In the beginning, the helicity and chirality of the CNTs based on the various methods of rolling of CNTs are discussed, and its effect on the properties of CNTs has been discussed. It has been observed that, both SWCNT and MWCNT individually posses some properties that can be even better oppressed if the combination of the two is used. For this purpose, in this paper the mixed CNT bundle is formed, with the MWCNTs at the sides and SWCNTs placed at the center. The motive behind such structure is to provide the effective structures with minimum delay and crosstalk between the two bundles.

A New Spatially Rearranged Bundle of Mixed Carbon Nanotubes as VLSI Interconnection [49]

-Suraj Subash, Jayanth Kolar, Masud H. Chowdhury

The paper demonstrates the effect of scaling on the delay and crosstalk of the interconnect wires and how carbon nanotubes have emerged as a better interconnect material. It provides the structure containing both single walled and multi walled carbon nanotubes. It is shown that, although there is no significant reduction in delay or power dissipation by this structure, but the capacitive crosstalk between the bundle structures have been reduced. This is attributed to the shielding provided between two lines.

Modeling and fast simulation of multiwalled carbon nanotube interconnects [50]

-Tang Min, Junfa Mao

In the paper, the MWCNT models are developed and their fast simulation analysis is performed The ESC model is also derived from the MCC model. This ESC model is then employed to find the delay for fast simulation in a delay extraction algorithm. The impact of the contact resistance and the intershell tunneling conductance has also been studied. Through the delay analysis of MWCNTs, it has been found that the imperfect contact resistance affects it's electrical properties.

Estimation of Time Delay and Repeater Insertion in Multiwall Carbon Nanotube Interconnects [59]

- Feng Liang, Gaofeng Wang, Wen Ding

In this paper, for the equivalent single conductor model, FDTD (finite difference time domain) method is used to do delay analysis. The propagation delay variation at different lengths is being plotted for 14 and 22nm technology. Optimum number of repeaters, at different lengths for the MWCNT and Cu wires has also been determined. It finally concludes that, at global lengths the delay offered by MWCNTs is much less than Cu wires. Also, the number of repeaters required in MWCNT interconnects is much less as compared to copper.

CHAPTER 3

PROPOSED METHODOLOGY:

This chapter is divided into four parts; the first part shows the various proposed structures of the MWCNT bundles, both containing similar and different number of MWCNTs and the second part gives the MCC and ESC model for these structures. The structures are modeled with respect to the number of shells in the individual MWCNTs contained in each structure. The third section explains the need and the method of inserting repeaters in order to minimize the delay and power. At last, the forth section shows the method of delay analysis.

For the delay, power dissipation and power delay product (PDP) analysis of these structures as a VLSI interconnect; the given structures are simulated on SPICE simulator through the Driver Interconnect Load (DIL) system as shown in Figure (3.1). The structure uses the CMOS inverter as the driver for the interconnect wire. Each interconnect line is being converted into equivalent RLC model. For this the Equivalent Single Conductor (ESC) model for all the structures is being derived from the Multi Conductor Circuit (MCC) or a multi-conductor transmission line (MTL) model using mathematical analysis in MATLAB. Finally, the capacitor is employed as a load for the RLC equivalent circuit.

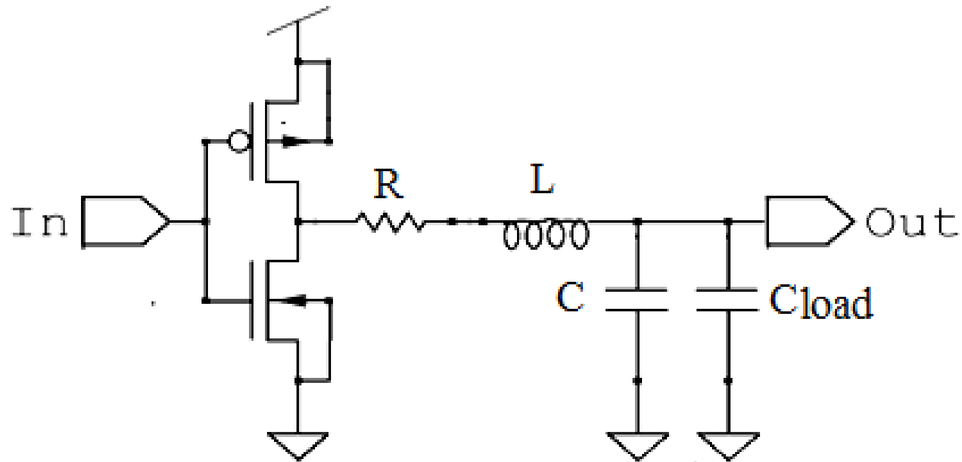


Figure 3.1: Driver Interconnect Load (DIL) system for SPICE simulation [35]

The simulations are done at different driver size, so as to obtain the optimum driver size for minimum value of PDP. ESC model for a fixed length and technology and optimized driver size is distributed into N sections by insertion of repeaters (buffers). The value of N is chosen using simulation which provides minimum PDP.

3.1 DIFFERENT BUNDLE STRUCTURES:

To understand the basic structure of MWCNT as interconnect, an MWCNT above ground plane has been shown in Figure 3.2. It consists of number of graphene sheets rolled up in the form of concentric cylinders having innermost and outermost shell diameter represented as D_{min} and D_{max}.

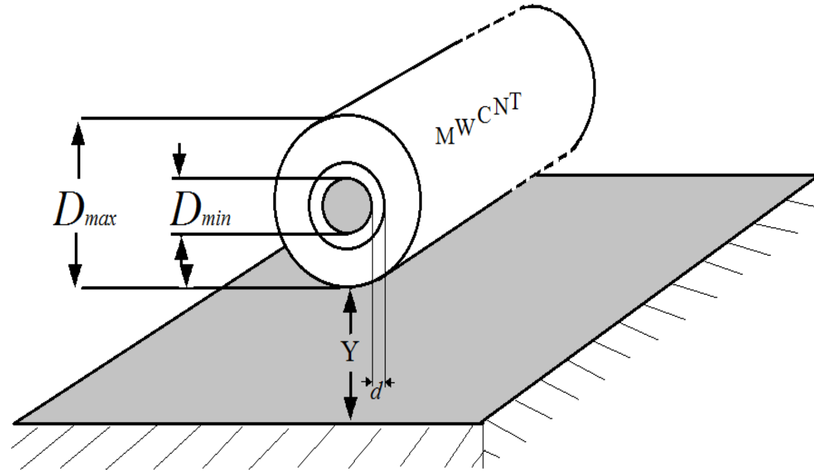


Figure 3.2: MWCNT above a ground plane. [38]

The spacing between any two shells is called Vander–Waal's gap *(d)* and is approximately equal to 0.34nm [38]. *Y* represents the outermost shell's distance from the ground plane. With the total number of shells being *n*, the diameter of the outer most shell of MWCNT can be expressed as:

$$D_{max} = D_{min} + 2d(n-1) \tag{3.1}$$

The ratio of D_{min} to D_{max} is taken as 0.5 through the experimental results in [20, 39]. Therefore, the above formula for calculation of D_{min} can be reduced to:

$$D_{min} = 2d(n-1) \tag{3.2}$$

Hence, knowing the value of number of shells (n) the value of diameter of all shells can be determined and vice versa. The number of MWCNTs for given number of shells in a particular structure is thus calculated by this knowledge of the relationship between, diameter of shells and number of shells in each MWCNT.

The different structures of MWCNT bundle with uniform number of shells are shown in Figure 3.3 (a-c) for MW1, MW2 and MW3 structures respectively for 32nm technology node.

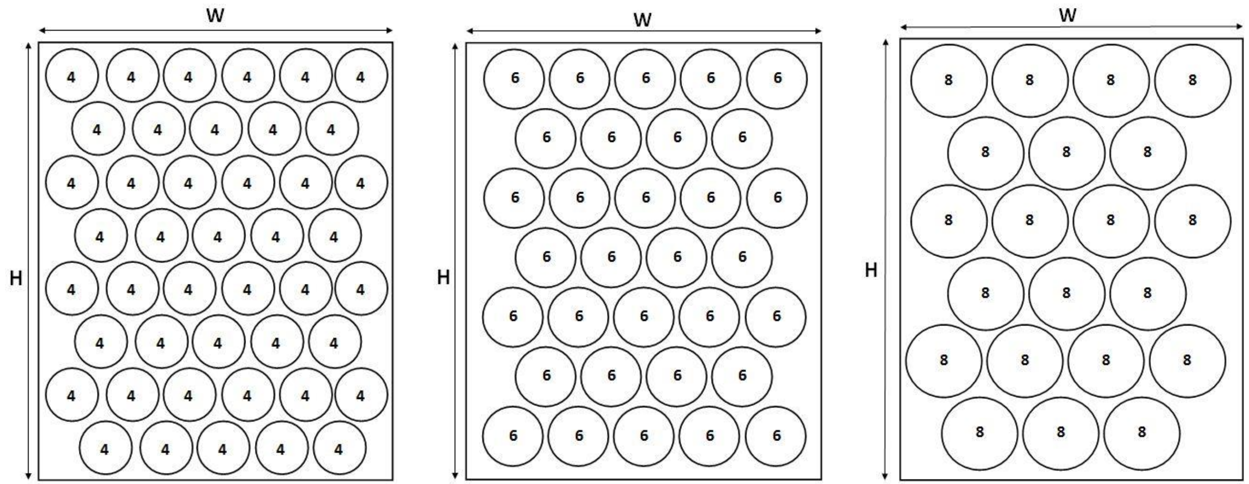


Figure 3.3: MWCNT bundles (MW) structures containing MWCNTs with (a) 4shells (b) 6 shells (c) 8 shells

The structure MW1 has a bunch of MWCNT with identical size of four shells. Similarly, structures MW2 and MW3 consist of 6 and 8 shells respectively. These structures are shown for 32nm technology and identical structures will be employed for 22nm and 16 nm technology nodes by changing the bundle parameters (viz. Height, Width and oxide thickness etc.) as defined by the ITRS 2013 as shown in table(3.1) [40].

Table 3.1: ITRS 2013 based simulation parameters for global interconnects [40]

Technology Node	**32nm**	**22nm**	**16nm**
Width W(nm)	40	28	18
Thickness H (nm)	120	84	48
Aspect Ratio(A/R)	3	3	3
Oxide thickness (nm)	93.6	65.5	40
VDD (volts)	0.9	0.8	0.7
Dielectric constant,	2.77	2.59	2.31
Dratio(Dmin/Dmax)	0.5	0.5	0.5

The total number of MWCNTs for these structures is obtained through the knowledge of technology dependent bundle width *(W)* and height *(H)* as:

$$N_{MWCNT} = N_H N_V - \text{Integer}\left[\frac{N_V}{2}\right] \tag{3.3}$$

Where, N_H and N_V represent the number of MWCNTs in horizontal and vertical directions respectively and are calculated as:

$$N_H = \frac{W - D_{max}}{D_{max} + d} + 1 \tag{3.4}$$

$$N_V = \frac{h - D_{max}}{(D_{max} + d)\sqrt{3}/2} + 1 \tag{3.5}$$

Further, the Mixed MWCNT (MMW) bundle structures are shown in Figure 3.4(a-c). In these structures, the MWCNTs containing large diameter and more number of shells are being layered at the top and bottom of the bundle and those containing small diameter with lesser number of shells are being located in center as shown in Figure 3.4.

The motive behind such structure is to fully utilized bundle area in order to obtain a densely packed bundle [41]. The MMW1 structure is thus fashioned by MWCNTs containing 6 numbers of shells being placed at the top and bottom layers and the remaining area being filled by those containing 4 numbers of shells. Similarly, for MMW2 structure the MWCNTs contain 8 and 6 number of the shells and MMW3 contain 10 and 8 number of the shells respectively.

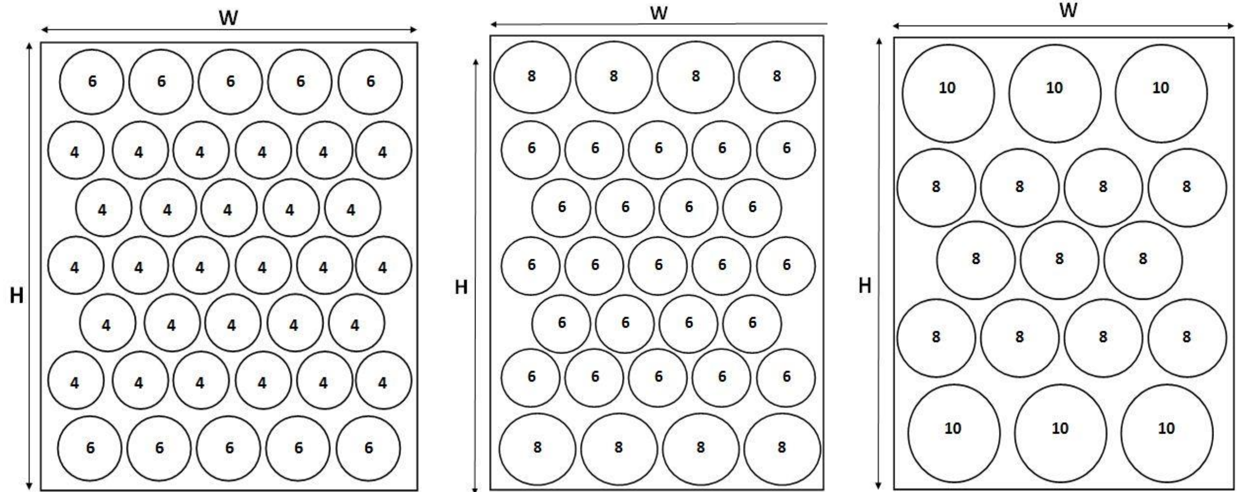


Figure 3.4: Mixed MWCNT (MMW) bundle structures containing (a) MMW1 (6-4 shells) (b) MMW2 (8-6 shells) and (c) MMW3 (10-8 shells)

The total number of MWCNTs for MMW1-3 structures is calculated by individually calculating the number of MWCNTs at the center (i.e. layers with smaller diameter) and layers at the top and bottom of the bundle (i.e. layers with larger diameter). The total number of MWCNTs layers in

one structure will be the sum of the layers at top, bottom and center, where the cross-sections of interconnects will be technology dependent. Let, $N_{MWCNT,\,l}$ are the number of MWCNTs with larger diameter and placed at top and bottom of the structure. Similarly, $N_{MWCNT,\,s}$ is the number of MWCNTs with smaller diameter and placed at center, inside every structure as shown in Figure 3.4, Therefore, $N_{MWCNT,\,l}$ can be calculated as:

$$N_{\mathrm{MWCNT,l}} = N_{H,l} \times N_{V,l} \tag{3.6}$$

Where, $N_{H,l}$ and $N_{V,l}$ are number of MWCNTs of larger diameter in horizontal and vertical direction within one structure and can be given as:

$$N_{\mathrm{H,l}} = \frac{W - D_{\max,\,l}}{D_{\max,\,l} + d} + 1 \tag{3.7}$$

$$N_{\mathrm{V,l}} = 2 \tag{3.8}$$

Where, $D_{\max,\,l}$ is the outermost diameter of the MWCNT with larger diameter or more number of shells. The value of $N_{V,l}$ will always "2" as there are two layers of the MWCNTs containing larger diameter at the top and bottom ends of the bundle. Similarly, $N_{MWCNT,\,s}$ for can be calculated as:

$$N_{\mathrm{MWCNT,s}} = N_{H,s} N_{\mathrm{V,s}} - Integer\left[\frac{N_{\mathrm{V,s}}}{2}\right] \tag{3.9}$$

Where, $N_{H,s}$ and $N_{V,s}$ are number of MWCNTs of smaller diameter in horizontal and vertical direction:

$$N_{\mathrm{H,s}} = \frac{W - D_{\max,\,s}}{D_{\max,\,s} + d} + 1 \tag{3.10}$$

$$N_{\mathrm{V,s}} = \frac{(H - 2 \times D_{\max,\,l}) - D_{\max,\,s}}{(D_{\max,\,s} + d)\sqrt{3}/2} + 1 \tag{3.11}$$

Therefore, total number of MWCNTs in the Mixed MWCNT bundle structure is:

$$N_{MWCNT} = N_{MWCNT,l} + N_{MWCNT,s} \tag{3.12}$$

The total number of MWCNTs containing different shells for MW (1-3) structures is obtained for 32, 22 and 16nm technology nodes, by using Eqs. 3.2-3.4. similarly, the total number of

MWCNTs for MMW (1-3) structures is calculated by using Eqs. 3.5-3.11. The total number of MWCNTs for proposed structures are shown in Table 3.2.

Table 3.2: Number of MWCNTs of each type in the given MW and MMW structures

Different MWCNT bundle structures	MWCNTs containing different shells	On 32nm technology node			On 22nm technology node			On 16nm technology node		
		N_H	N_V	N_{MWCNT}	N_H	N_V	N_{MWCNT}	N_H	N_V	N_{MWCNT}
MW1	4 shells	9	31	264	6	21	116	4	14	49
	6 shells	0	0	0	0	0	0	0	0	0
	8 shells	0	0	0	0	0	0	0	0	0
	10 shells	0	0	0	0	0	0	0	0	0
MW2	4 shells	0	0	0	0	0	0	0	0	0
	6 shells	5	19	100	4	13	51	3	8	21
	8 shells	0	0	0	0	0	0	0	0	0
	10 shells	0	0	0	0	0	0	0	0	0
MW3	4 shells	0	0	0	0	0	0	0	0	0
	6 shells	0	0	0	0	0	0	0	0	0
	8 shells	4	14	49	3	9	23	2	6	9
	10 shells	0	0	0	0	0	0	0	0	0
MMW1	4 shells	9	27	240	6	18	108	4	10	38
	6 shells	5	2	10	4	2	8	3	2	6
	8 shells	0	0	0	0	0	0	0	0	0
	10 shells	0	0	0	0	0	0	0	0	0
MMW2	4 shells	0	0	0	0	0	0	0	0	0
	6 shells	5	16	83	4	10	35	2	5	12
	8 shells	4	2	8	3	2	6	2	2	4
	10 shells	0	0	0	0	0	0	0	0	0
MMW3	4 shells	0	0	0	0	0	0	0	0	0
	6 shells	0	0	0	0	0	0	0	0	0
	8 shells	4	11	40	3	7	8	2	3	5
	10 shells	3	2	6	2	2	4	1	2	2

3.2 MCC OR MTL AND ESC MODEL:

For the calculation of power dissipation and propagation delay at first interconnect parasitic (R, L, C) are calculated in the MCC (Multi Conductor Circuit) model and then the ESC (Equivalent Single Conductor) model is developed for different structures to calculate delay and power dissipation and Power Delay Product (PDP) through the interconnect wire. The purpose of this simulation is to obtain the optimized value of PDP.

The interconnect parasitics are sculptured using the number of conducting channels. The number of conducting channels in each shell of MWCNT can be expressed as [38]:

$$N_i(D_i) = k_1 T D_i + k_2, \qquad D_i > 4.3nm$$
$$= 2/3 \qquad\qquad D_i \le 4.3nm \tag{3.13}$$

Where, k_1 and k_2 are 3.87×10^{-4} nm^{-1} K^{-1} and 0.2, respectively [38] and D_i represents i^{th} shell diameter. For D_i greater than 4.3nm, the number of conducting channels of a particular shell becomes directly proportional to the diameter of the shell [35]. The total number of conducting channels in an MWCNT can be represented as the summation of the number of conducting channels of all shells as [37]:

$$N^{CHANNEL} = \sum_{i=1}^{n} N_i \qquad (3.14)$$

Where, n denotes the total number of shells in an MWCNT. Similarly the total number of conducting channels for the complete bundle can be calculated as:

$$N_{TOTAL}^{BUNDLE} = \sum_{i=1}^{N_{MWCNT}} N_j^{CHANNEL} \qquad (3.15)$$

Where, N_{MWCNT} represents total number of MWCNTs in a bundle structure. This is because the number of conducting channels for each MWCNT in the bundle is same, as the number of shells and there diameter is same for all the MWCNTS in MW structures. Similarly for MMW structures the total number of conducting channels will be evaluated by adding the number of conducting channels of each type of MWCNT in a particular structure. The conduction through the Carbon nanotubes is ballistic; this is because they posses large mean free paths (MFPs) in the range of few micrometers. The diameter dependent MFP of each shell can be represented as [42]:

$$MFP(\lambda_{mwcnt}) = 1000D_i \qquad (3.16)$$

On the basis of multi-conductor transmission line theory [43], the RLC model of an MWCNT +bundle is shown in Figure (3.5), which is further simplified to obtain ESC model as shown in Figure (3.6) [44]. In the ESC model all shells in MWCNT and also all the MWCNTs in the bundle are considered to be in parallel.

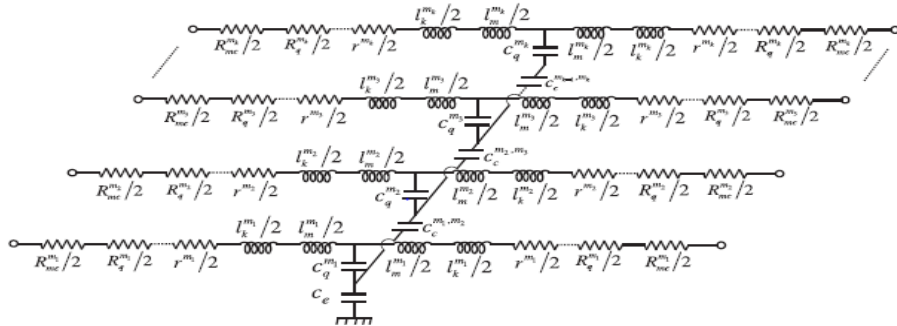


Figure 3.5: MCC or MTL model of bundle structure [37]

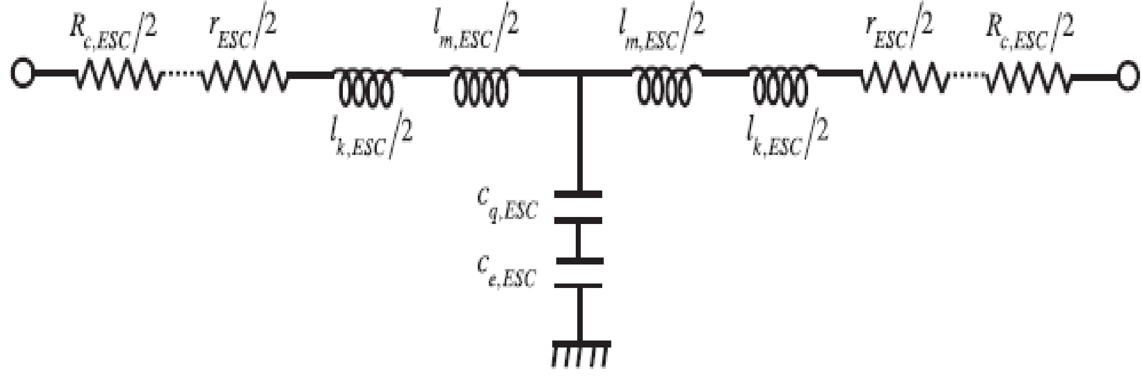


Figure 3.6: ESC Model for MWCNT bundle structure [37]

R, L and C values for single shell and bundle:

Every shell of MWCNT bundle have three types of resistances: quantum resistance, also called as an intrinsic resistance *(R_c)* due to the quantum confinement of electrons in a nano-wire, fabrication process dependent imperfect metal contact resistance *(R_{mc})* has range 0-100 kΩ and scattering resistance *(R_S)* that exists if interconnects length is greater than the MFP of the MWCNT. [45-47]

For a single shell, the value of quantum contact resistance (R_c) and scattering resistance (R_S) will be [23]:

$$R_c = \frac{h}{2e^2 N} \tag{3.17}$$

$$R_S = \frac{h}{2e^2 N\lambda} \tag{3.18}$$

Where, $h/2e^2$ has the value approximately equal to 12.9KΩ, N represents the number of conducting channels in a single shell. Now for the complete MWNCT these resistances values can be calculated by dividing the intrinsic resistance ($h/2e^2$) by the total number of shells in MWCNT as all the shells are considered to be in parallel:

$$R_c = \left[\left(\frac{R_q}{\sum_{i=1}^{n} N_i} \right)^{-1} + \text{.................................} \left(\frac{R_q}{\sum_{i=1}^{n} N_i} \right)^{-1} \right]^{-1} \tag{3.19}$$

$$R_S = \left[\left(\frac{R_q}{\sum_{i=1}^{n} N_i \lambda_{mfpi}} \right)^{-1} + \text{........................} \left(\frac{R_q}{\sum_{i=1}^{n} N_i \lambda_{mfpi}} \right)^{-1} \right]^{-1} \tag{3.20}$$

Now, if we consider the whole bundle structure the resistance values will be further divided by the total number of MWCNTs of a particular type in a bundle structure as all the MWCNTs are considered to be in parallel. Therefore, the final values of quantum contact resistance ($R_{c,\ ESC}$) including contact resistance (R_{mc}) and scattering resistance (R_{ESC}) for the bundle structure will be:

$$R_{c,ESC} = \left[\left(\frac{1}{(N_{MWCNT})_{m_1}}\left(\frac{R_q}{\sum_{i=1}^{n} N_i} + R_{mc}\right)\right)^{-1} \cdots\cdots\cdots\cdots \left(\frac{1}{(N_{MWCNT})_{m_k}}\left(\frac{R_q}{\sum_{i=1}^{n} N_i} + R_{mc}\right)\right)^{-1}\right]^{-1} \tag{3.21}$$

$$R_{ESC} = \left[\left(\frac{1}{(N_{MWCNT})_{m1}}\left(\frac{R_q}{\sum_{i=1}^{n} N_i \lambda_{mfpi}}\right)\right)^{-1} + \cdots\cdots\cdots\cdots \left(\frac{1}{(N_{MWCNT})_{mk}}\left(\frac{R_q}{\sum_{i=1}^{n} N_i \lambda_{mfpi}}\right)\right)^{-1}\right]^{-1} \tag{3.22}$$

$$R_{equ} = R_{c,ESC} + R_{ESC} \times L \tag{3.23}$$

Similarly, the equivalent single conductance (ESC) capacitance of MWCNT bundle can be classified as electrostatic capacitance *(C_E)* that arises due to difference in potential between the bundle and ground plane and quantum capacitance *(C_Q)* that represents the finite density of electronic states in a quantum wire.

For one shell, the quantum capacitance will be:

$$C_Q = 2C_{q_0} \times k_1 TD + k_2 \tag{3.24}$$

and for complete bundle,

$$C_{Q,ESC} = 2C_{q_0} \times N_{Total}^{Bundle} \tag{3.25}$$

Where,

$$C_{q_0} = \frac{2e^2}{hv_F} \tag{3.26}$$

Similarly, Electrostatic capacitance can be defined as:

$$C_{E,Esc} = \frac{2\pi\varepsilon_r\varepsilon_0}{\cosh^{-1}\left[{(D_n + Y)}/{D_n}\right]} \times N_H \tag{3.27}$$

Where, N_H is the number of MWCNTs facing the ground in the horizontal direction. The other variables i.e. and *$v_f = 8x10^5$ m/s* are fermi velocity respectively [46]. In addition to this, each shell in the MWCNT bundle experiences two more capacitances; inter-shell *(C_s)* and inter CNT coupling *(C_c)* capacitance that depends on shell diameter and center to center distance between

two CNTs respectively. The value of inter CNT coupling *(C_c)* capacitance is negligible small as compared to the quantum capacitance and electrostatic+ capacitance, it can be neglected [48, 49]. Therefore, the total Equivalent capacitance *(C_{equ})* is calculated recursively as [50]:

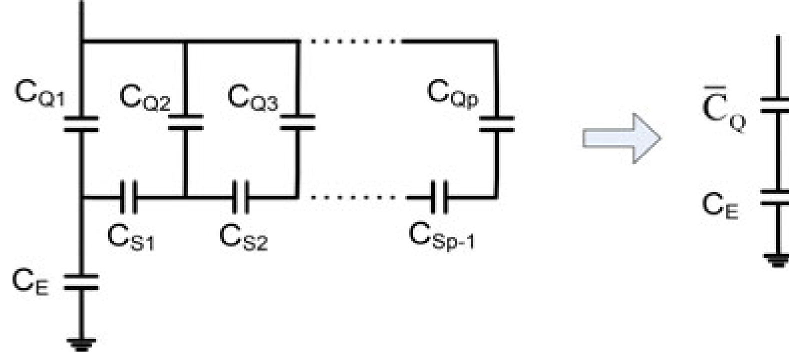


Figure 3.7: Recursive way of finding the equivalent capacitance [50]

Where, $\overline{C_Q}$ represents the equivalent Capacitance and C_{Qj} is Quantum Capacitance C_S is Scattering Capacitance

Hence, the total capacitance will be:

$$C_{equ} = \frac{\overline{C_Q} \times C_{e,ESc}}{\overline{C_Q} + C_{e,ESC}} \tag{3.28}$$

The Equivalent Inductance consists of: kinetic inductance *($l_{k,ESC}$)* because of the kinetic energy of electrons and magnetic inductance *($l_{m,ESC}$)* that comes into play when the current is flowing in a nanotube which induces the magnetic field. The Inductance values for one shell and per unit length can be expressed as:

$$l_k = \frac{l_{k0}}{k_1 TD + k_2} \tag{3.29}$$

For complete bundle:

$$l_{k,ESC} = \frac{l_{k0}}{2N_{Toatal}^{Bundle}} \tag{3.30}$$

and magnetic inductance will be:

$$l_{m,ESC} = \frac{\mu_0}{2\pi} \cosh^{-1}\left(\frac{D_n + 2Y}{D_n} \right) \tag{3.31}$$

Therefore, the total Inductance value *(L_{equ})* can be calculated as:

$$l_{equ} = (l_{k,ESC} + l_{m,ESC}) \times L \tag{3.32}$$

Where, L is the length of interconnect wire in μm.

3.3 REPEATER INSERTION

The repeater are used to reduce the propagation delay in interconnects by dividing interconnects into small segments.

Need of Repeater Insertion

The interconnect delay and power dissipation were very small and can be neglected in earlier technologies. But in recent technology nodes number of interconnections are required to be used to connect the millions of devices. Thus resistance of the wires increases resulting in rise in propagation delay and power dissipation. Interconnects can be modeled as lumped (*RC* or *RLC)* or distributed depending on the operating frequency. Initially interconnect circuits were modeled with *RC* equivalent circuits and the propagation delay was calculated using a structure of Elmore delay through *RC* [51], which gave the good time constant approximation. But at higher frequency, length of interconnect becomes equal to a multiple fraction of the operating wavelength, which gives rise to distortion that do not exist at lower frequencies [52] .Therefore lumped impedance interconnect models is not sufficient for delay calculation. Lumped *RC* and *RLC* equivalent circuit models are shown below in Figure 3.8 [53].

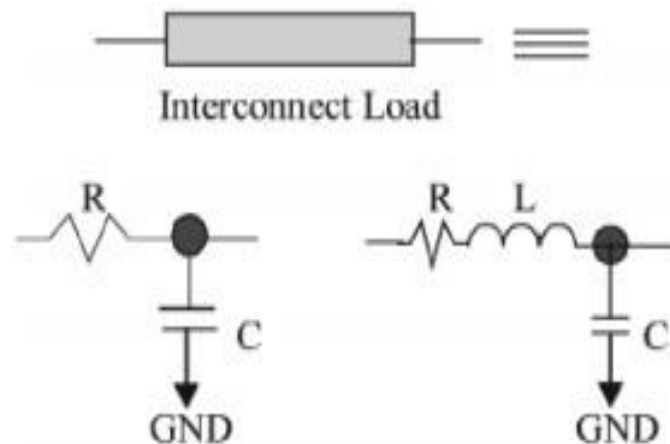


Figure 3.8 Lumped *RC* and RLC models for interconnect [53]

Technology scaling causes a linear increase in capacitance and resistance values which further raise the signal propagation delay and power dissipation thus affecting the performance of the ICs. To enhance the performance, both delay and power dissipation has to be minimized. The increase in load capacitance in VLSI circuits due to long interconnect and large fan-outs, driver circuits should be able to discharge theses capacitances with acceptable speed. This can be obtained by the insertion of repeater or multi-layering [54]. Interconnection multilayers have

partially solved the delay problem. Layers of interconnect in the x-and y-directions inter-connected by vias at different levels allows long-distance signal propagation without using polysilicon. The cross-sectional area of the top layers can also be optimized to decrease propagation delay. The lower levels can be used for local interconnection and the long-distance signal propagating wire can use at the upper levels, which are wider and thicker, yield in shorter signal propagation delays. As the larger of the chip area is covered with interconnect lines, multilayers approach can also reduce chip size and improve the RC time constant because the average interconnection length is inversely proportional to the level number. [54]

On the other hand, repeaters are used to minimize the overall interconnect propagation delay by reducing the effect of resistance and capacitance.

A lot of work has been done regarding Repeaters (inverters). Figure 3.9 shows a CMOS repeater drives an interconnect wire and its equivalent symbol representation in the design. [55]

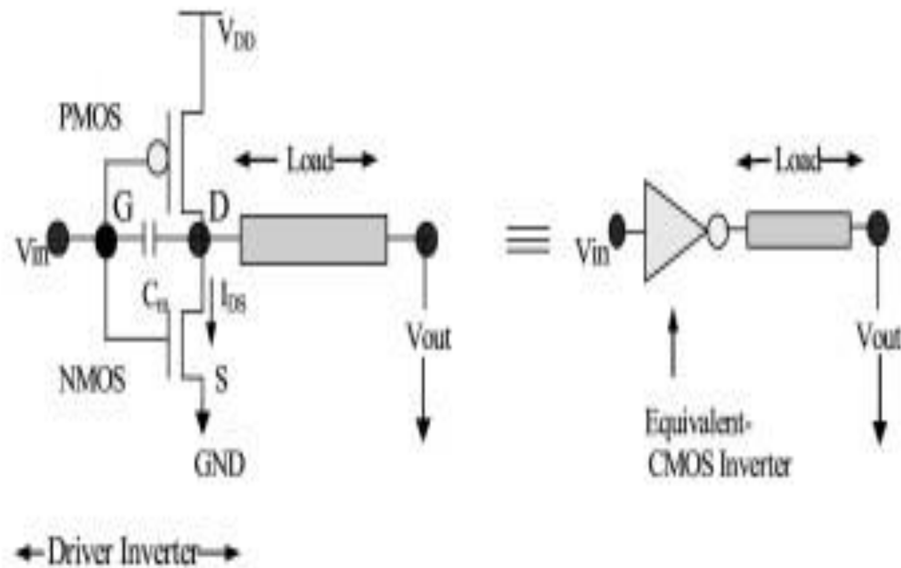


Figure 3.9: CMOS inverter drives in interconnect load and its equivalent symbol [55]

Insertion of Repeaters in Interconnect

When the on resistance of driver is comparable or larger than the wire resistance, propagation delay increases as the square of the wire length because both capacitance and resistance increase linearly with wire length. By dividing the long wires into small segments and inserting a repeater between every two segments (Figure 3.10) the propagation delay of the resulting wire becomes a linear function of the number of segments. Repeaters reduce the interconnect wire propagation delay by reducing the effect of capacitance and resistance of

interconnect. Therefore interconnect with repeater inserted in it has small delay value than a conventional interconnect. This technique is called repeater (or buffer) insertion. [56]

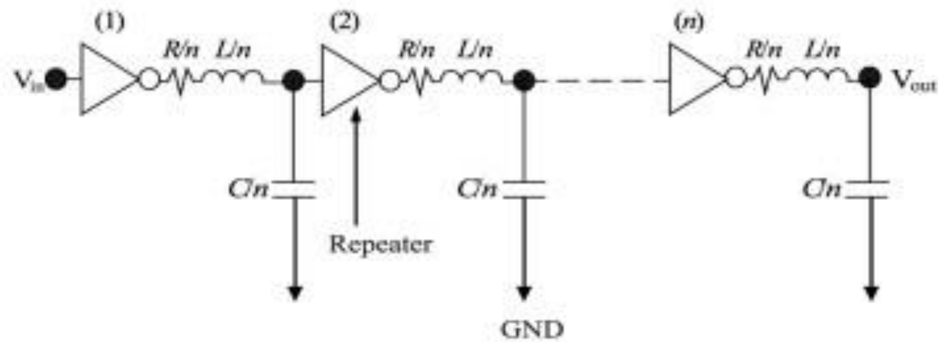


Figure 3.10: Distributed RLC Interconnect with Repeaters inserted in between [56]

Meindl et al. and Ismail et al [57] [58] have derived various models for delay calculation for repeater inserted RLC interconnect lines. Figure 3.11 below shows N number of buffers inserted in between wire, thus dividing it into small interconnects wire.

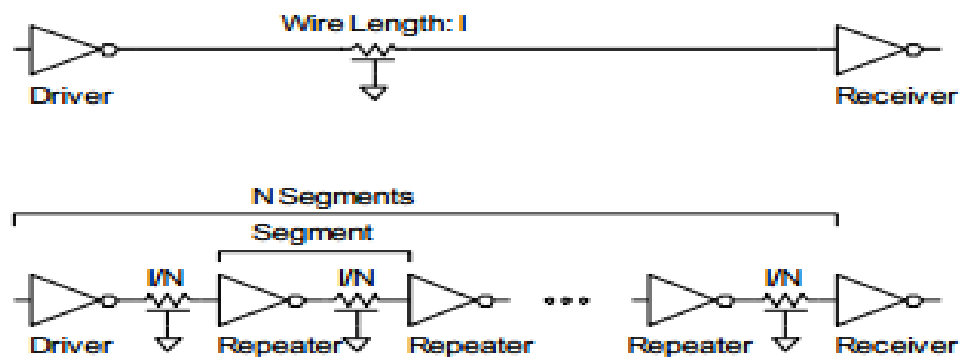


Figure 3.11: N number of repeaters inserted in between an interconnect [59]

If a interconnect wire is divided into small segments, the total RC time constant is reduced. An additional delay due to the inserted repeaters should be taken into the measure for the final calculation of the propagation delay. The number of buffers that can be inserted in an interconnect are limited because at some point, the sum of the delay caused by the repeater will become comparable, or may exceed to the propagation delay of the interconnect. Therefore, we can insert repeater only up to certain limits [59]. A methodology is developed to reduce power dissipation by calculating the optimum repeater size and length of interconnect. Therefore Power dissipation can be minimized by repeater insertion technique. Power dissipation minimization is done at some value of delay penalty [60] [61].

3.4 DELAY ANALYSIS:

The propagation delay of an interconnect wire is measured using the SPICE tool, through the driver interconnect load (DIL) system as mentioned in the beginning of the chapter. The input waveform with 50% duty cycle is fed to the CMOS inverter acting as a driver, and the output waveform is obtained at the output node connected to load capacitance (CL). The propagation delay is measured as:

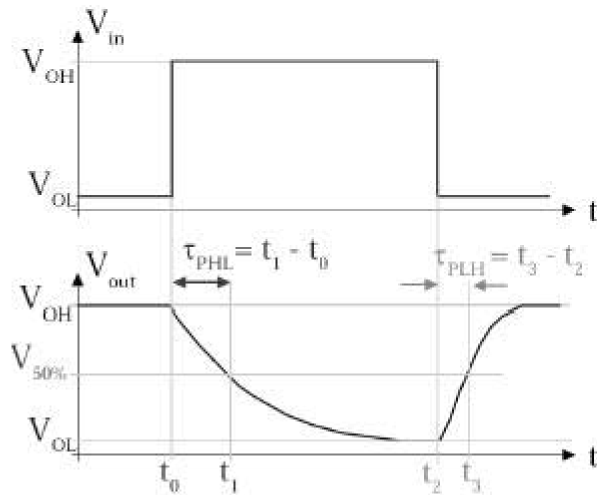


Figure 3.12: Input waveform and delayed output waveform [62]

$$\tau_p = \frac{\tau_{PHL} + \tau_{PLH}}{2} \tag{3.33}$$

Where, τ_{PHL} and τ_{PLH} defines the fall time and rise time respectively, as shown in the Figure 3.12.

CHAPTER 4
RESULTS AND DISCUSSION

This chapter analyzes and compares the performance on the basis of delay; power and power delay product for different structures of MWCNT bundles for variable interconnect lengths (500µm-2000µm). The study is further extended to estimate and compare the performance for different technology nodes i.e. 32, 22 and 16nm. On the basis of this comparative analysis the best structure suited for optimum delay, power and PDP is discovered.

The chapter is mainly divided into following parts: Firstly, in section 4.1, the equivalent R, L and C parasitic values of the various structures are given at different technology nodes (viz. 32nm, 22nm, 16nm) and the comparison between resistance and capacitance values for different structures is shown. In 4.2, the use of repeater insertion is described and the power delay product (PDP) for the different number of repeaters has been compared both in tabular and graphical form. Also, in this section the variation of the PDP with the driver size over a particular range is shown to obtain the optimum value of PDP. Section 4.3 shows the comparison between MW structure and its corresponding MMW structure at different technologies and interconnect lengths. Section 4.4 compares all the structures all together at a particular technology node and varying lengths. At last, section 4.5 compares all the structures on a particular length ranging from 500µm-2000µm and varying technology nodes to determine the structure having minimum PDP at all technology nodes.

4.1 RLC PARAMETERS OF THE VARIOUS MWCNT BUNDLE (MW) AND MIXED MWCNT BUNDLE (MMW) STRUCTURES AND THE RESISTANCE AND CAPACITANCE COMPARISON OF VARIOUS STRUCTURES:

The propagation delay, power and PDP are primarily depend on the impedance parameters i.e. resistance, inductance and capacitance of the MWCNT bundle which is dependent on number of conducting channels of each MWCNT in a bundle. The total number of MWCNTs in one structure, number of shells in MWCNT bundle and number conducting channels in each shell of MWCNT depend upon the technology node as calculated by using Eqs. 3.1-3.15 and are as shown in Table3.1

Further, by using proposed single conductor equivalent (ESC) model, the equivalent resistance (Requ), inductance (Lequ) and capacitance (Cequ) are calculated for all the proposed structures at 32, 22, 16nm technology nodes by using Eqs. 4.16-4.31 and are shown in table 4.1-4.4. All the

parasitic for different structures at different technology nodes are calculated by using the parameters as predicted by ITRS 2013 [18]. All parasitic of different technology nodes are obtained by writing the script in MATLAB. Table 4.1-4.4 represents the values of these parasitics at 500, 1000, 1500 and 2000µm length respectively.

Table4.1: The values of equivalent Resistance, Inductance and Capacitance at 500µm length for all technology nodes.

Different Bundle Structure	32nm Technology node			22nm Technology node			16nm Technology node		
	R_{equ}	C_{equ}	L_{equ}	R_{equ}	C_{equ}	L_{equ}	R_{equ}	C_{equ}	L_{equ}
MW1	3.0411	142.0644	6.18	6.9246	103.6812	13.56	16.42338	79.1988	31.5
MW2	2.9904	90.2004	10.14	5.5908	79.8234	18.66	12.8586	69.6258	42.24
MW3	2.1888	79.473	10.32	4.6632	66.4272	21.66	11.9172	52.0806	54.66
MMW1	2.961	90.2808	6.3	6.0384	79.9176	12.78	14.1504	69.7596	31.5
MMW2	2.339	86.0864	12.06	5.2056	66.4584	18.84	11.907	52.149	44.76
MMW3	2.0694	64.3782	10.26	4.1442	42.8892	20.58	11.9982	21.4212	60.96

Table4.2: The values of equivalent Resistance, Inductance and Capacitance at 1000µm length for all technology nodes.

Different Bundle Structure	32nm Technology node			22nm Technology node			16nm Technology node		
	R_{equ}	C_{equ}	L_{equ}	R_{equ}	C_{equ}	L_{equ}	R_{equ}	C_{equ}	L_{equ}
MW1	6.6066	284.1294	12.42	13.8078	207.3624	27.12	32.68805	158.3976	63.12
MW2	5.9496	180.4008	20.28	11.1234	159.6468	37.26	25.5846	139.2516	84.54
MW3	4.3452	158.9466	20.7	9.258	132.8544	43.26	23.6604	104.1612	109.38
MMW1	5.9028	180.5616	12.66	12.0372	159.8358	25.62	28.2018	139.5186	63.06
MMW2	5.0046	170.9892	18.06	10.3524	132.9168	37.68	23.6718	104.2992	89.58
MMW3	4.1076	128.745	20.58	8.2236	85.7796	41.22	23.8026	42.8424	121.98

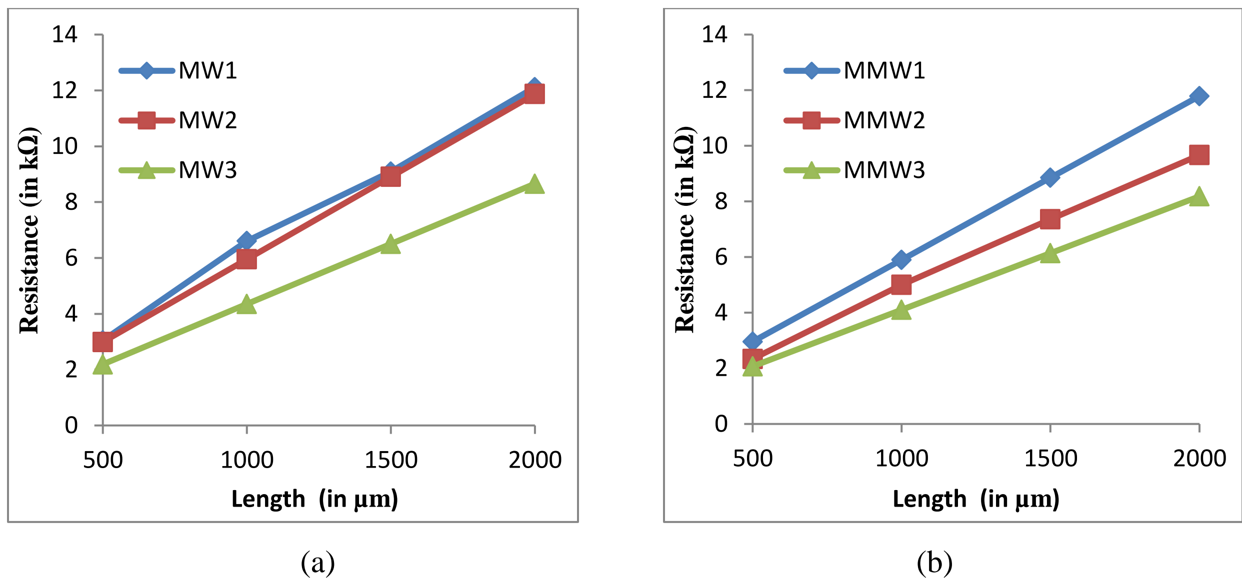
Table4.3: The values of equivalent Resistance, Inductance and Capacitance at 1500µm length for all technology nodes.

Different Bundle Structure	32nm Technology node			22nm Technology node			16nm Technology node		
	R_{equ}	C_{equ}	L_{equ}	R_{equ}	C_{equ}	L_{equ}	R_{equ}	C_{equ}	L_{equ}
MW1	9.0912	426.1938	18.66	20.691	311.043	40.74	48.9828	237.5964	94.56
MW2	8.9088	270.6018	30.48	16.6566	239.4702	55.86	38.3088	208.8774	126.78
MW3	6.5022	238.4196	31.08	13.8534	199.2816	64.86	35.403	156.2418	164.1
MMW1	8.8482	270.8424	18.9	18.0366	239.7534	38.46	42.2526	209.2782	94.56
MMW2	7.1452	238.6296	18.15888	15.4992	199.3758	56.58	35.4366	156.4482	134.34
MMW3	5.3568	193.1172	30.84	12.3036	128.6694	61.86	35.6076	64.2636	182.94

Table4.4: The values of equivalent Resistance, Inductance and Capacitance at 2000μm length for all technology nodes.

Different Bundle Structure	32nm Technology node			22nm Technology node			16nm Technology node		
	R_{equ}	C_{equ}	L_{equ}	R_{equ}	C_{equ}	L_{equ}	R_{equ}	C_{equ}	L_{equ}
MW1	12.1158	568.2588	24.9	27.5736	414.7242	54.3	65.2776	316.4946	126.12
MW2	11.8686	360.8022	40.62	22.1886	319.2936	74.46	51.0336	278.5032	169.08
MW3	8.6592	317.8932	41.46	18.4482	265.7094	86.52	47.1462	208.3218	218.82
MMW1	11.7876	361.1226	25.26	24.0348	319.6716	51.3	56.3034	279.0378	126.12
MMW2	9.1834	318.1728	24.18	20.646	265.8342	75.42	47.2014	208.5978	179.16
MMW3	6.6666	257.4906	41.16	16.383	171.5586	82.5	47.4126	85.6848	243.96

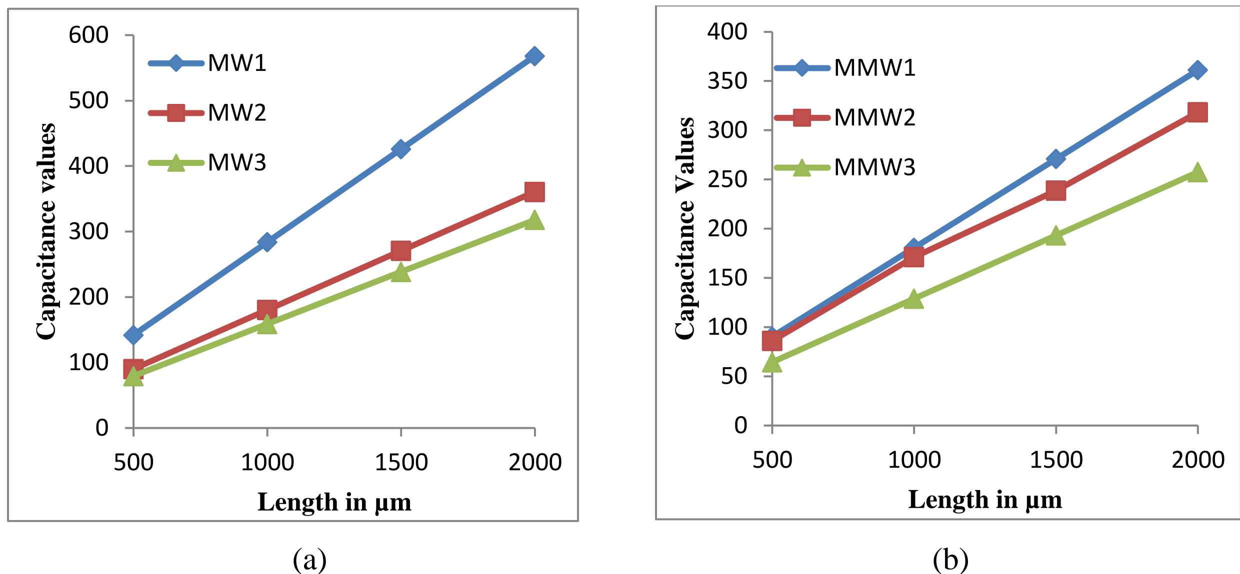
Further, as the Propagation delay and power dissipation are mainly dependent on the resistance and capacitance of an interconnect. Therefore, the variation of the resistances and capacitances of all the structures with respect to the length are shown in Figure (4.1) and (4.2) for 32nm technology node. The similar results can be inferred for 22 and 16 nm technology node. Also, the graphs show the comparison for these values between various MW and MMW configurations.



(a) (b)

Figure 4.1: Comparison between Resistance values (in kΩ) for (a) MW1-3 and (b) MMW1-3 structural arrangements.

Figure 4.1 and 4.2 shows that, as the length of the interconnect is increasing the value of resistances for different structures goes on increasing. It can also be inferred that the minim um value of resistance is obtained for MW3 and MMW3 structures respectively in Figures 4.1 (a) and (b) respectively.



(a) (b)

Fig 4.2: comparison between Capacitance values for various (a) MW and (b) MMW structures.

These comparison show that, the value of capacitances for the various MW and MMW structures also increases over the interconnect lengths. Also, it shows that, the minimum value for the capacitance is obtained for MW3 and MMW3 structures among other MW and MMW structures respectively.

4.2 REPEATERS OR BUFFER INSERTION:

Repeaters are nothing but the buffers or inverters used in order to reduce the propagation delay. The role of repeaters is to reduce the length of interconnect into ‘N’ segments, where N represent number of repeaters and as it is already shown that propagation delay is dependent on Length of interconnect and therefore insertion of repeaters results in reduction of propagation delay. The repeater insertion causes reduction in the distributed parameters of interconnects by the factor of N. For the simulation of ESC model the repeaters used are CMOS inverters. The simulation results in Figure 4.7. For the value ‘N’ that is the number of repeaters at which the power Delay Product (PDP) reaches to its minimum value is considered to be optimum number of repeaters to be inserted. Table shows the values of delay, power and PDP for number of repeaters to be inserted in the given interconnect length at 32nm technology node and 1000µm length.

Table4.5: Relationship between number of repeaters and PDP for 32nm technology node.

Repeaters	Delay	power	PDP
3	5.6465	6.5547	37.01111
5	3.0335	9.6087	29.14799
7	2.4892	12.4759	31.05501
9	2.2533	15.3891	34.67626
11	2.1523	18.3348	39.46199

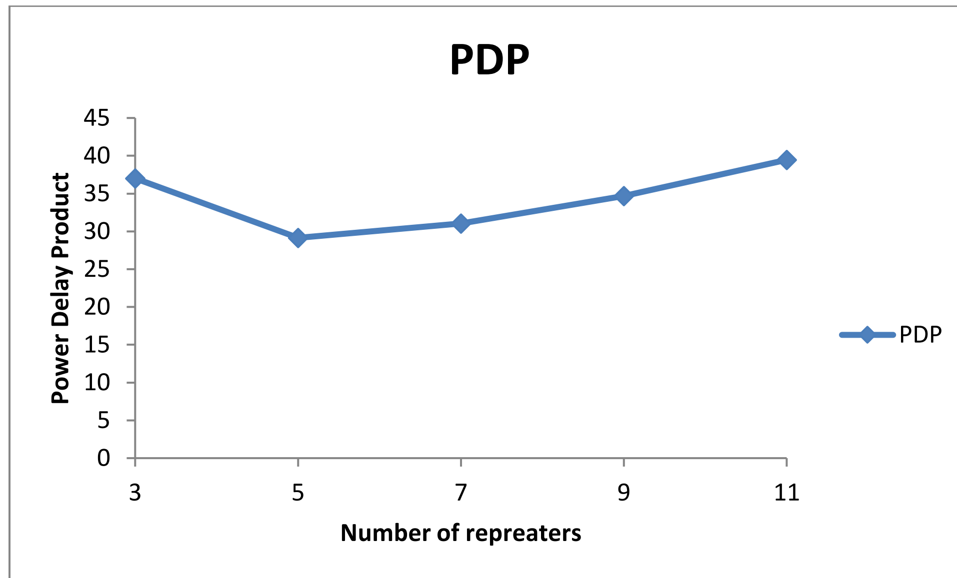


Figure 4.3: PDP V/s Number of repeaters graph at 32nm technology node.

The graph and the table clearly indicate that, the minimum PDP is obtained for the 5 repeaters to be used for the 1000μm length and 32nm technology node.

4.3 COMPARISON BETWEEN MWCNT BUNDLE (MW) STRUCTURES AND THERE CORRESPONDING MIXED MWCNT (MMW) BUNDLE STRUCTURES AT VARYING LENGTHS AND DIFFERENT TECHNOLOGY NODES:

Depending on these parasitic values for different proposed structures as given in section 4.1, the propagation delay, power dissipation and PDP are simulated through driver interconnect load (DIL) model for different interconnect lengths at nano-scaled technology nodes. All the simulations are performed by using SPICE tool for different bundle structures. The estimated performance of different structures in terms of propagation delay for different interconnects length and technology nodes is given in Table 4.6 for the comparison between MW1 and MMW1 and the graphical representation for the same is shown in Figure (4.4).

Table4.6: Delay values for MW1 and MMW1 at different technology nodes

Length of Bundle (in µm)	Delay of different structures (in nsec)					
	MW1	MW2	MW3	MMW1	MMW2	MMW3
500	0.1485	0.1070	0.0851	0.1072	0.0906	0.0749
1000	0.4101	0.2757	0.1993	0.2750	0.2197	0.1641
1500	0.8122	0.5317	0.3706	0.5297	0.4146	0.2978
2000	1.3551	0.8751	0.5979	0.8711	0.6737	0.4746

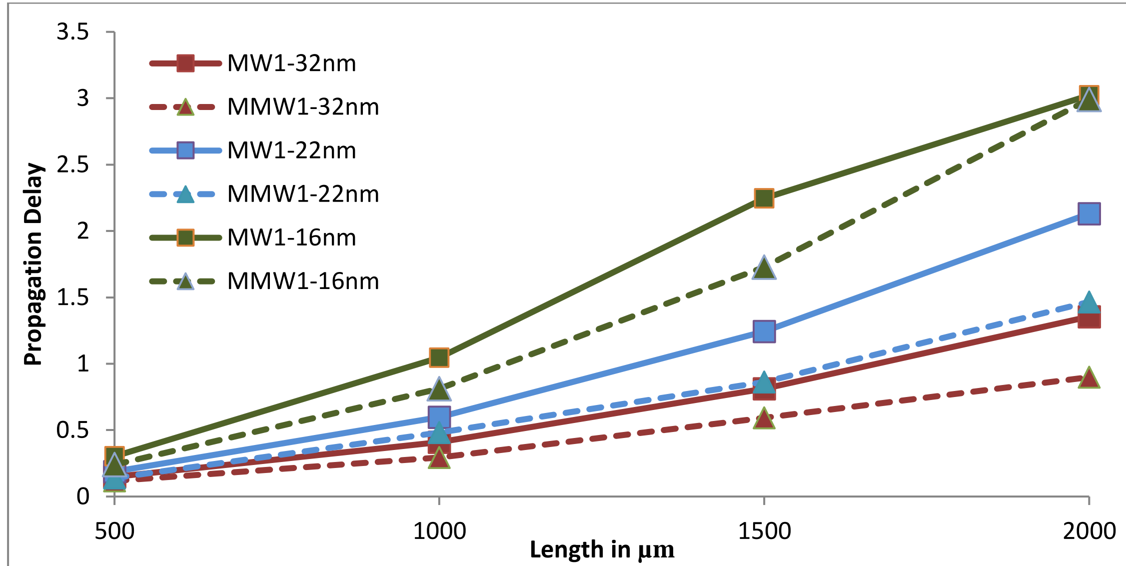


Figure 4.4: Delay comparison between MW1 and MMW1 structures at different technology nodes

It can be seen from the table and the graph that for all technology nodes and interconnect lengths, the propagation delay for the mixed MWCNT (MMW) structure is always less than that of MWCNT bundle (MW) structure. Similarly, the delay comparison for MW2 V/s MMW2 and MW3V/s MMW3 are shown in Figure (4.5) and (4.6) respectively, and the similar kinds of results are obtained.

Table4.7: Delay values for MW2 and MMW2 at different technology nodes

Length of Bundle (in µm)	Delay of different structures (in nsec)					
	MW1	MW2	MW3	MMW1	MMW2	MMW3
500	0.107	0.075767	0.13202	0.11059	0.22019	0.16469
1000	0.27576	0.16932	0.39313	0.31652	0.73982	0.52357
1500	0.53174	0.30586	0.80253	0.63761	1.5714	1.1167
2000	0.80512	0.48537	1.3599	1.0733	2.7149	1.9169

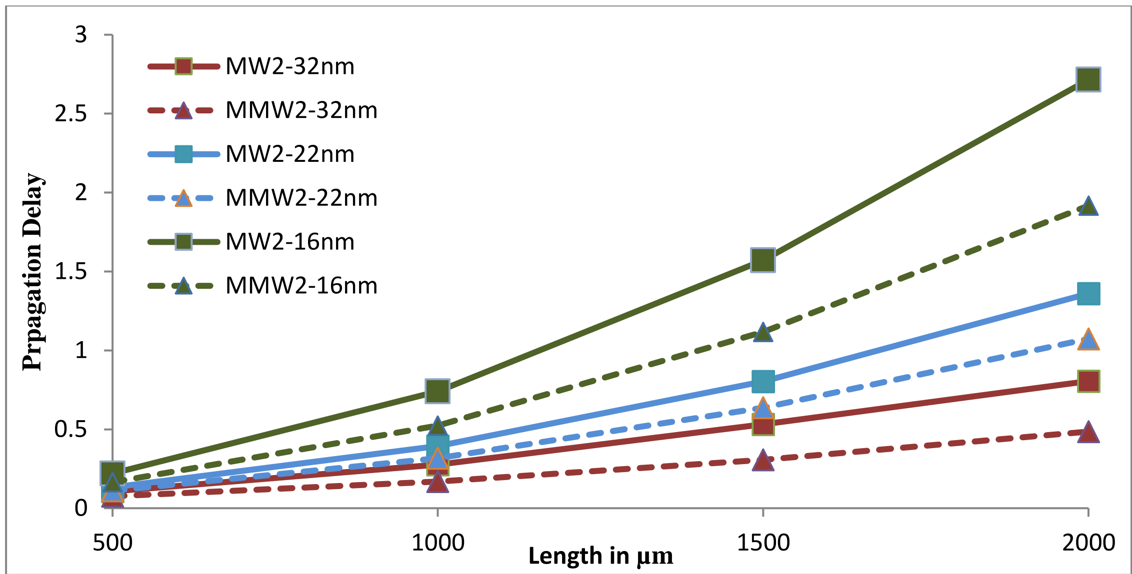


Figure 4.5: Delay comparison between MW2 and MMW2 structures at different technology

Table4.8: Delay values for MW3 and MMW3 at different technology nodes

Length of Bundle (in µm)	Delay of different structures (in nsec)					
	MW1	MW2	MW3	MMW1	MMW2	MMW3
500	0.085128	0.074916	0.10381	0.0763	0.17457	0.09585
1000	0.1993	0.1641	0.3585	0.18519	0.53159	0.2604
1500	0.37063	0.29781	0.57708	0.40607	1.0141	0.5175
2000	0.59793	0.47462	0.9679	0.8396	1.512	0.8638

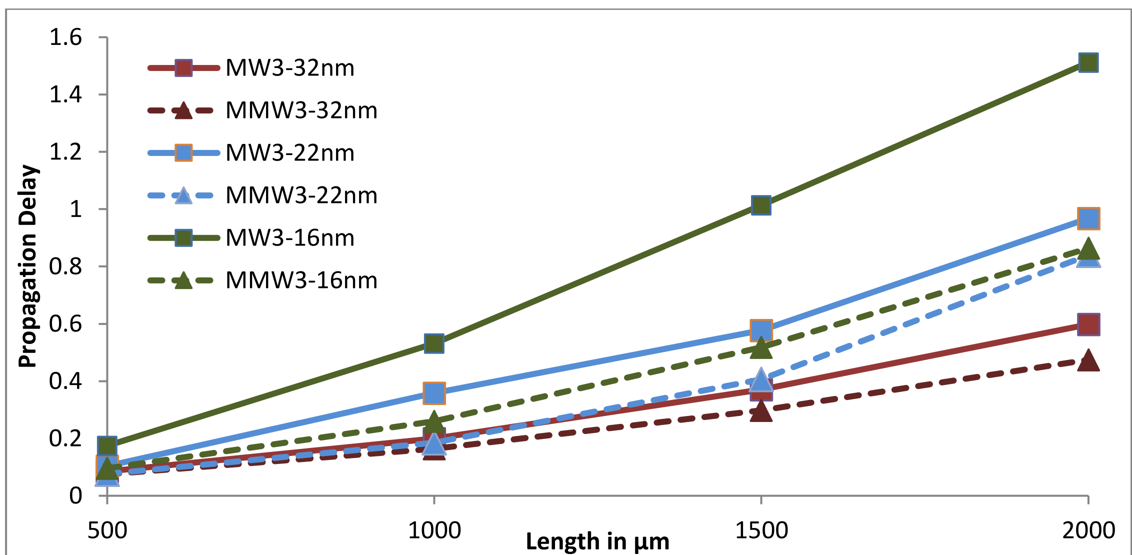


Figure 4.6: Delay comparison between MW3 and MMW3 structures at different technology nodes

Hence, from above analysis it is concluded that, the propagation delay of the MMW structures is always less than that of their corresponding MW structures at all technology nodes and lengths.

4.4 COMPARISON OF DELAY AND POWER BETWEEN ALL BUNDLE STRUCTURES AT A PARTICULAR TECHNOLOGY NODE AND VARYING INTERCONNECT LENGTHS:

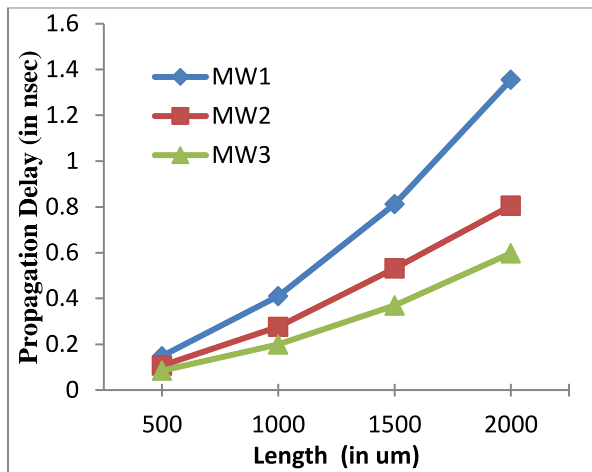
4.4.1 Delay Analysis:

At 32nm Technology Node:

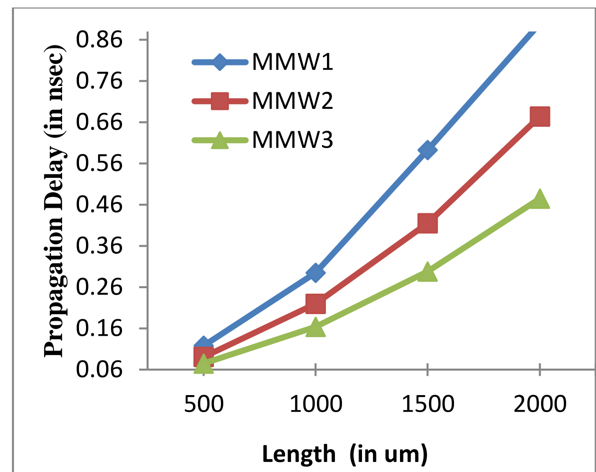
Table 4.9 gives the values of Propagation Delay (in n sec) for different bundle structures at 32nm for varying interconnect lengths. It can be inferred from the table that the minimum delay is being offered by MMW3 for all interconnect lengths, the same can be represented more clearly through graphical method. The comparison between the propagation delay at different interconnect lengths for different MW and MMW bundle structures is shown in Figure. 4.7 (a) and (b) respectively. It can be seen from these Figures that although the propagation delay for all the structures increases with increase in length, the minimum delay is obtained in MW3 and MMW3 structures in the two graphs respectively. It is revealed from the results shown in Table 3 that MW3 and MMW3 offered the least delay among the two groups of structures i.e. MW1-3 with similar number of shells and MMW1-3 with different number of shells as shown in Fig. 4.7 (a) and (b). Figure. 4.7 (c) shows a combined comparative analysis of all the proposed structures (MW1-3 and MMW1-3). It is also concluded from the results that the propagation delay offered by MW1 structure is higher as compare to MMW1 structure for all the interconnect lengths under consideration. Similar results are also obtained from the comparison of MW2 with MMW2 and MW3 with MMW3.

Table 4.9: Propagation Delay in (nsec) for different bundle structures at 32nm

Length of Bundle (in µm)	Delay of different structures (in nsec)					
	MW1	MW2	MW3	MMW1	MMW2	MMW3
500	0.1485	0.1070	0.0851	0.1072	0.0906	0.0749
1000	0.4101	0.2757	0.1993	0.2750	0.2197	0.1641
1500	0.8122	0.5317	0.3706	0.5297	0.4146	0.2978
2000	1.3551	0.8751	0.5979	0.8711	0.6737	0.4746



(a)



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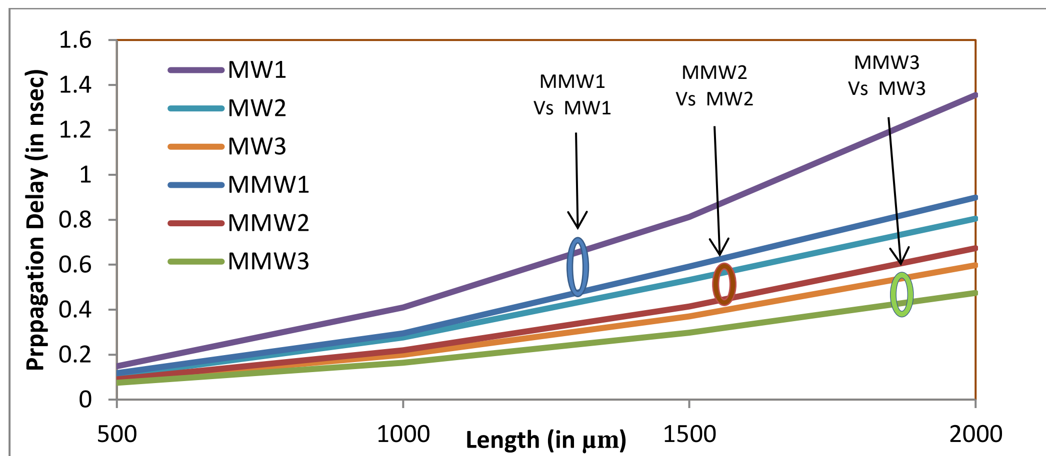


(c)

Figure 4.7 Individual comparative analyses in term of propagation delay for (a) MW1-3 and (b) MMW1-3 structures, for variable interconnects length at 32nm technology nodes (c) Combined comparative analysis for MW1-3 and MMW1-3 structures.

Further, it is also revealed from the results that MMW3 structure offered the optimum delay compared to the other structures. To verify the results in favour of MMW3, the percentage reduction in delay for MMW3 structure as compared to other structures has also been calculated and summarized in Table 4.10.

Table 4.10: Percentage reduction in delay for MMW3 structure as compared to other structures

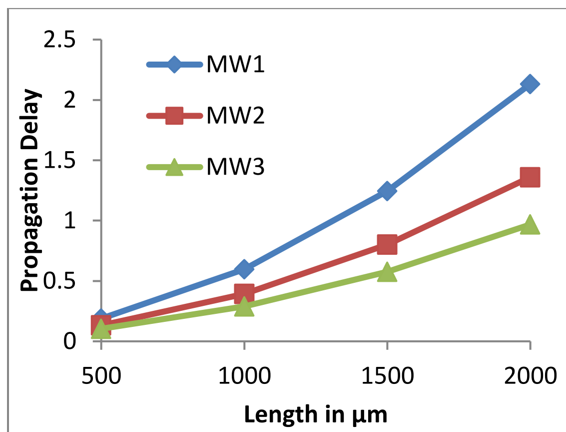
Length of Bundle (in µm)	%age reduction in propagation delay of MMW3 in comparison to				
	MW1	MW2	MW3	MMW1	MMW2
500	49.5752	29.9850	11.9960	30.1287	1.1231
1000	59.9941	40.4917	17.6618	40.3446	3.0829
1500	63.3329	43.9933	19.6476	43.7786	2.6319
2000	64.9752	45.7651	20.6228	45.5154	2.2148

At 22nm technology node:

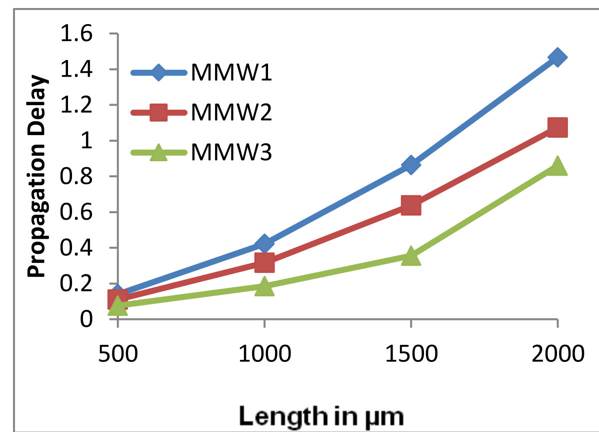
Similarly, analysis is performed for 22nm technology node as shown:

Table 4.11: Propagation Delay in (nsec) for different bundle structures at 22nm

Length of Bundle (in µm)	Delay of different structures (in nsec)					
	MW1	MW2	MW3	MMW1	MMW2	MMW3
500	0.18828	0.13202	0.10381	0.13965	0.11059	0.0763
1000	0.59679	0.39313	0.2885	0.4211	0.31652	0.18519
1500	1.2446	0.80253	0.57708	0.86339	0.63761	0.35607
2000	2.1315	1.3599	0.9679	1.4663	1.0733	0.8596



(a)



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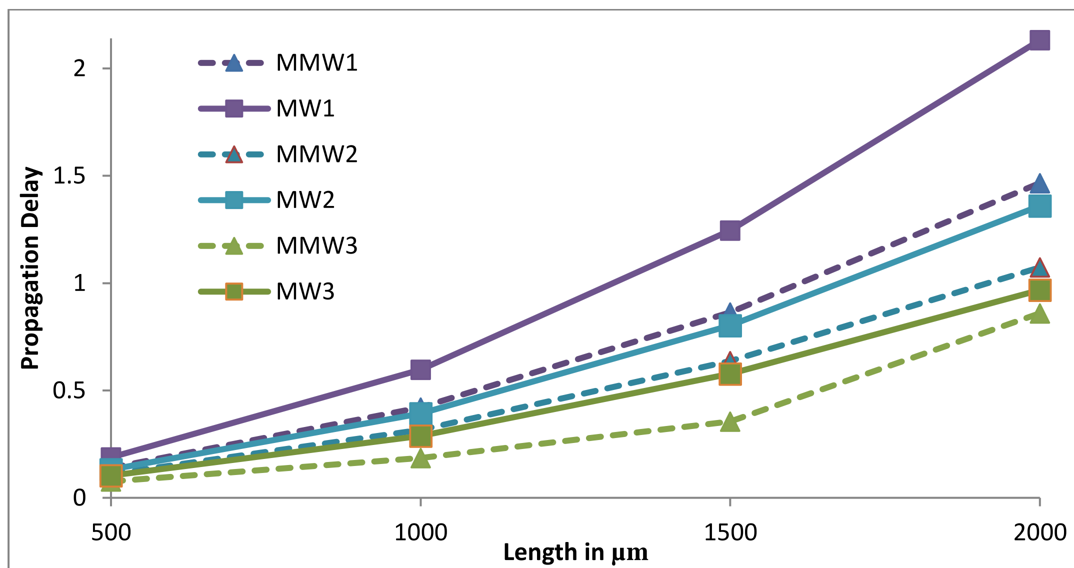
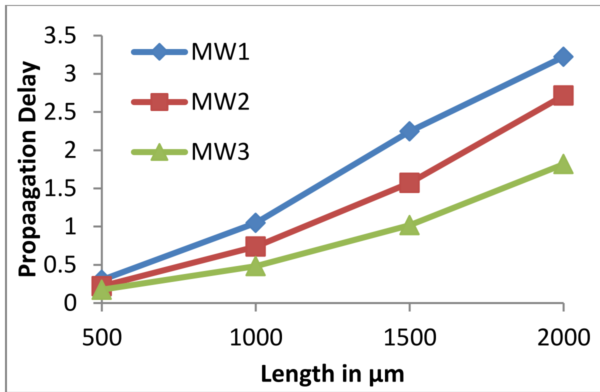


Figure 4.8: The comparison of delay at different lengths for (a) MW and (b) MMW structures and (c) Combined comparative analysis for delay of MW1-3 and MMW1-3 structures at 22nm technology node

***At 16nm technology node*:**

Table 4.12: Propagation Delay in (nsec) for different bundle structures at 16nm

Length of Bundle (in μm)	Delay of different structures (in nsec)					
	MW1	MW2	MW3	MMW1	MMW2	MMW3
500	0.30263	0.22019	0.17457	0.23972	0.15469	0.09585
1000	1.0469	0.73982	0.48357	0.81195	0.53159	0.2604
1500	2.2455	1.5714	1.0167	2	1.1141	0.5175
2000	3.2223	2.7149	1.8169	2.9916	1.912	0.8638



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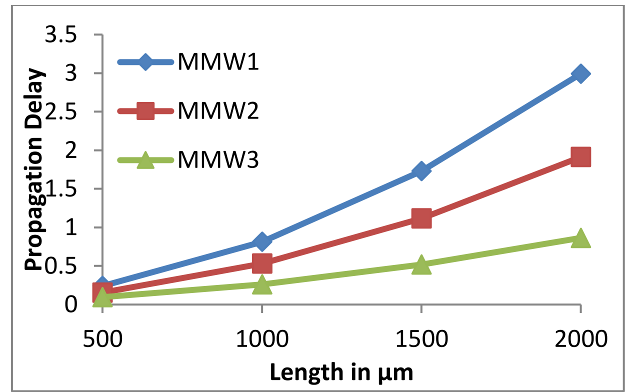

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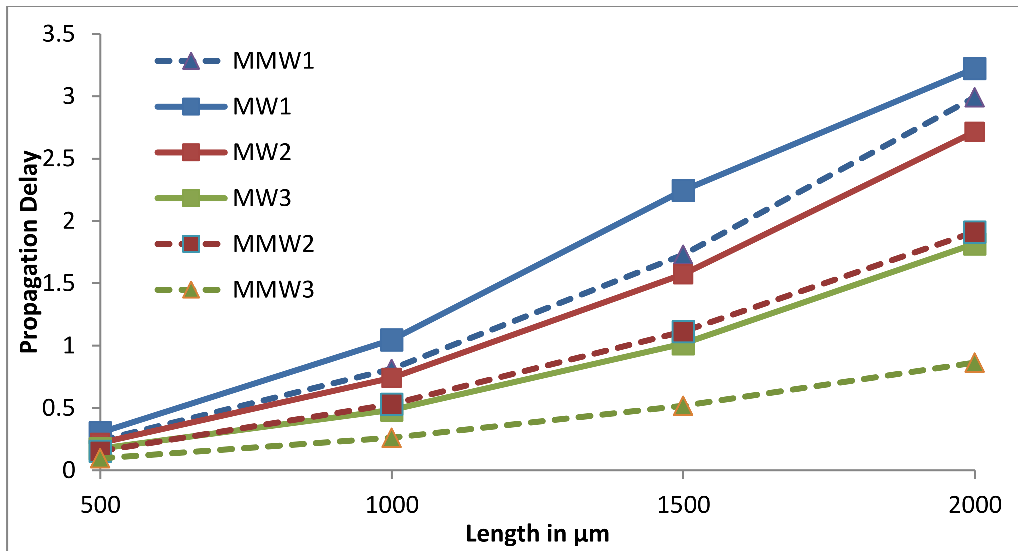


(c)-

Figure 4.9: The comparison of delay at different lengths for (a) MW and (b) MMW structures and (c) Combined comparative analysis for delay of MW1-3 and MMW1-3 structures at 16nm technology

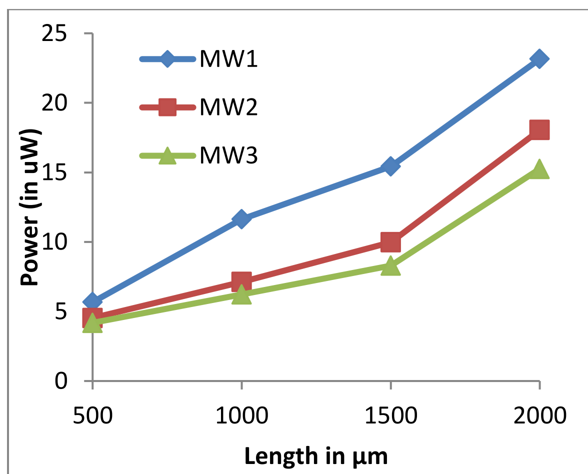
4.4.2 Power Analysis:

The comparative analysis in terms of power dissipation for all the structures is also performed and presented in Table 4.13, 4.14 and 4.15 for 32, 22 and 16nm technology node respectively. The comparison between the power dissipation in graphical form for different lengths and structures (MW and MMW) are shown in Figure 4.11, 4.12 and 4.13 for 32, 22 and 16nm technology node respectively. It can be summarized from the results shown in these Figures that the value of power dissipation for MMW3 is minimum as compared to all other structures at different interconnect lengths.

At 32nm technology node:

Table 4.13: Power dissipation for different structures (in µm) at different interconnect lengths

Length of Bundle (in µm)	Power Dissipation in different structures (in µW)					
	MW1	MW2	MW3	MMW1	MMW2	MMW3
500	5.6680	4.5300	4.1841	4.5202	4.2345	3.8741
1000	11.6370	7.1330	6.2305	6.4922	6.2420	5.5050
1500	15.4350	9.9808	8.2859	10.5298	9.0924	5.8361
2000	23.1481	18.0403	15.2550	15.1910	12.4031	9.8241



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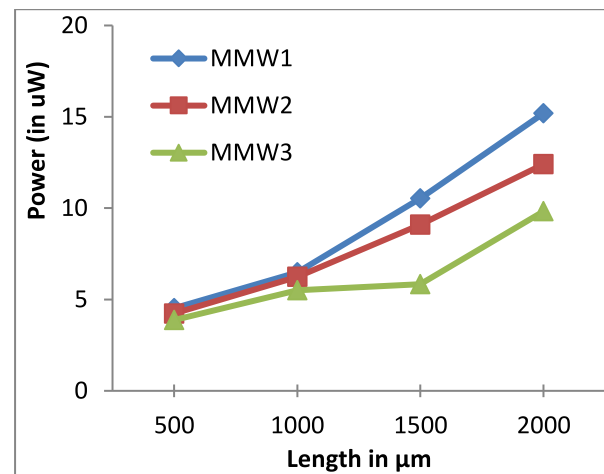


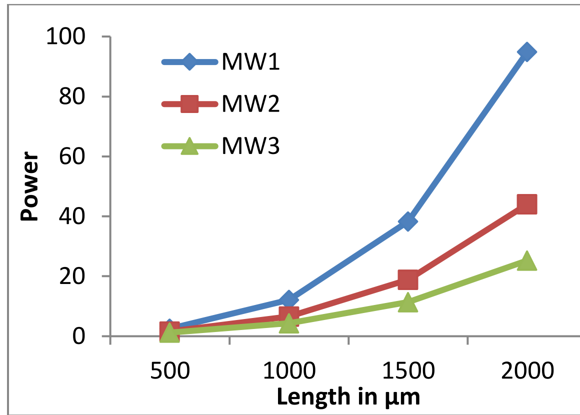
(b)

Figure 4.10: Comparison of power dissipation of different structures (a) MWCNT (MW) bundle structures and (b) Mixed MWCNT (MMW) bundle structures

At 22nm technology node:

Table 4.14: Power dissipation for different structures (in μm) at different interconnect lengths at 22 nm technology node

Length of Bundle (in μm)	Power Dissipation in different structures (in μW)					
	MW1	MW2	MW3	MMW1	MMW2	MMW3
500	13.3844	12.30156	11.7505	12.4278	11.8442	11.07604
1000	20.344	16.8349	14.996	17.2948	15.4277	12.9842
1500	30.7393	23.5596	19.821	24.5109	20.7454	15.86107
2000	44.5027	32.3905	26.127	34.003	27.7073	19.6233



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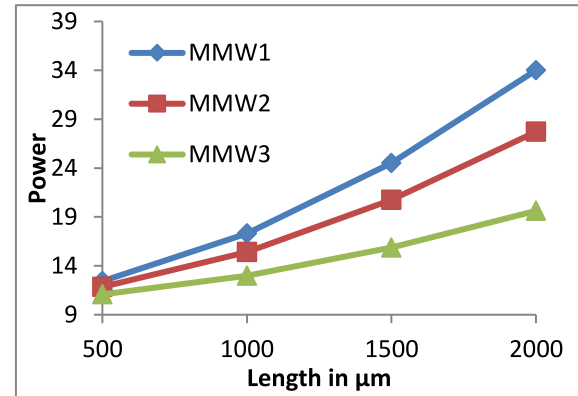


(b)

Figure 4.11: Comparison of power dissipation of different structures (a) MWCNT (MW) bundle structures and (b) Mixed MWCNT (MMW) bundle structures at 22nm technology node

At 16nm technology node:

Table 4.15: Power dissipation for different structures (in μm) at different interconnect lengths at 16nm technology node

Length of Bundle (in μm)	Power Dissipation in different structures (in μW)					
	MW1	MW2	MW3	MMW1	MMW2	MMW3
500	96.7867	94.5343	93.385	95.1418	93.01452	90.9997
1000	115.39	107.634	102.22	109.5435	102.356	95.27135
1500	144.73	128.137	116.68	132.1134	116.8602	101.8245
2000	163.54	155.998	136.2357	162.818	136.4664	110.5029

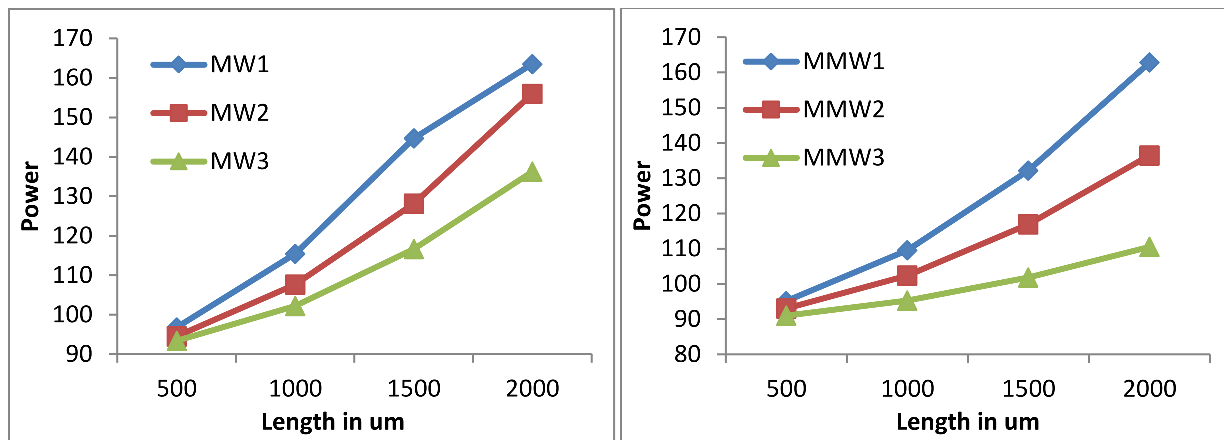


Figure 4.12: Comparison of power dissipation of different structures (a) MWCNT (MW) bundle structures and (b) Mixed MWCNT (MMW) bundle structures at 16nm technology node

Further, the percentage reduction in power dissipation for MMW3 structure as compared to other structures is shown in Table 4.16 at 32nm technology. The similar results are also obtained at 22 and 16nm technology.

Table 4.16: Percentage reduction in power dissipation for MMW3 structure as compared to other structures at 32nm technology node

Length of Bundle (in µm)	%age reduction in power dissipation of MMW3 in comparison to				
	MW1	MW2	MW3	MMW1	MMW2
500	31.6494	14.4788	7.4088	14.2934	7.6119
1000	52.6939	22.8235	11.6451	15.2059	9.9606
1500	62.1891	41.5267	29.5658	44.5754	30.5829
2000	57.5596	2.1532	35.6005	35.3293	12.5422

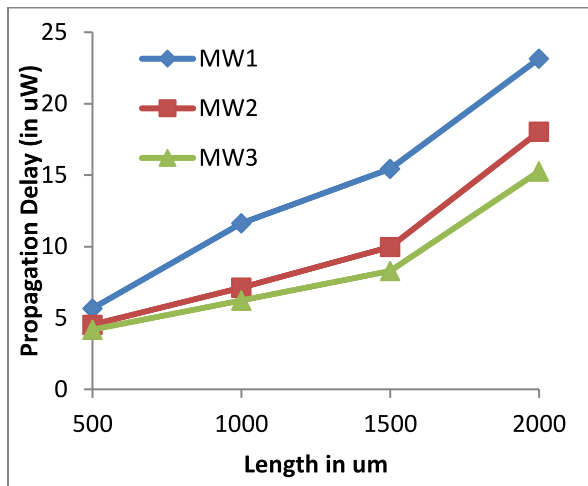
4.4.3 PDP Analysis:

Table 4.17 presents the Power Delay Product (PDP) values of MW1-3 and MMW1-3 structures at different interconnect lengths at 32nm technology node. Similarly, table 4.18 and 4.19 presents the PDP values for 22nm and 16 nm technology nodes respectively. It is evident from the table that the optimum values for the PDP is obtained for MMW3 structure. The analysis for the same is also presented graphically as shown in Figure 4.13. These Figures also demonstrate the PDP comparison between MW1 and MMW1 structural arrangements, in which MMW1 always bears a smaller PDP value in comparison to MW1 for all the interconnect lengths. The same can be concluded for the comparison between MW2-3 and MMW2-3 respectively.

For 32nm technology:

Table 4.17: Power Delay Product (PDP) values for different structures at 32nm technology node

Length of Bundle (in μm)	Power Delay Product (PDP) of different structures					
	MW1	MW2	MW3	MMW1	MMW2	MMW3
500	0.8420	0.4847	0.3561	0.4846	0.3799	0.2902
1000	4.7733	1.9669	1.2417	1.7858	1.3432	0.9033
1500	12.5363	5.3071	3.0710	5.5777	3.4856	1.7380
2000	31.3679	15.7874	9.1214	13.2330	7.5676	4.6627



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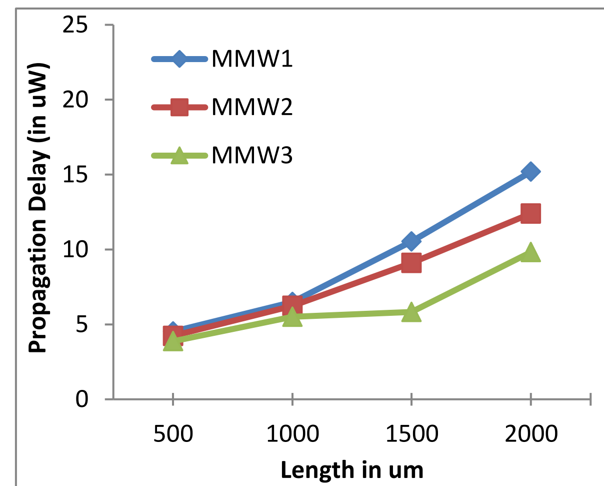
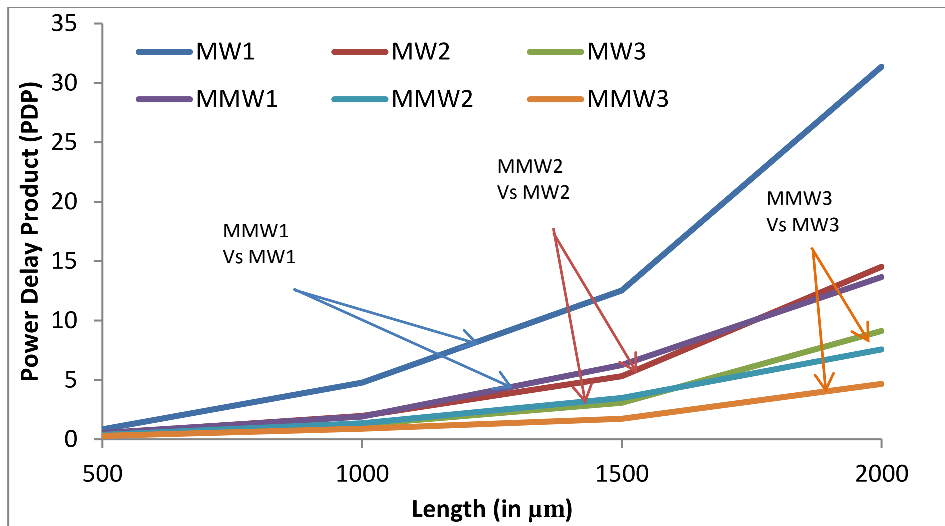


(b)

Figure 4.13 (a) and (b) Individual comparative analysis in term of power delay product for MW1-3 and MMW1-3 structures respectively, for variable interconnects length at 32nm technology node



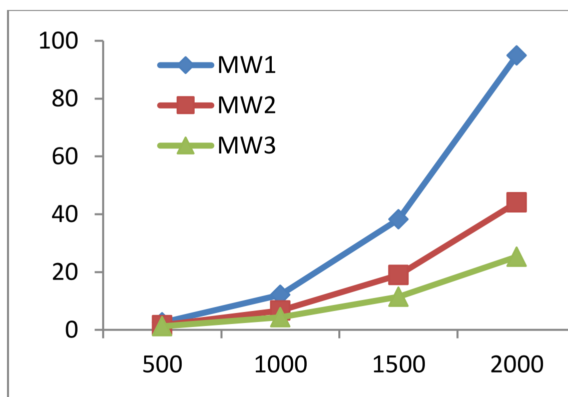
(c)

Figure 4.14: Combined comparative analysis for PDP of MW1-3 and MMW1-3 structures

For 22nm technology:

Table 4.18: Power Delay Product (PDP) values for different structures at 22nm

Length of Bundle (in µm)	Power Delay Product (PDP) of different structures					
	MW1	MW2	MW3	MMW1	MMW2	MMW3
500	2.520015	1.624052	1.219819	1.735542	1.30985	0.845102
1000	12.1411	6.618304	4.326346	7.28284	4.883176	2.404544
1500	38.25813	18.90729	11.4383	21.16247	13.22747	5.647651
2000	94.85751	44.04784	25.28832	49.8586	29.73825	16.86819



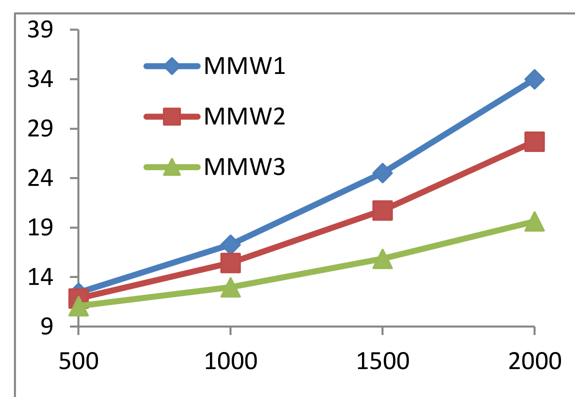


Figure 4.15 Individual comparative analysis in term of power delay product for (a) MW1-3 and (b) MMW1-3 structures respectively, for variable interconnects length at 22nm technology node.

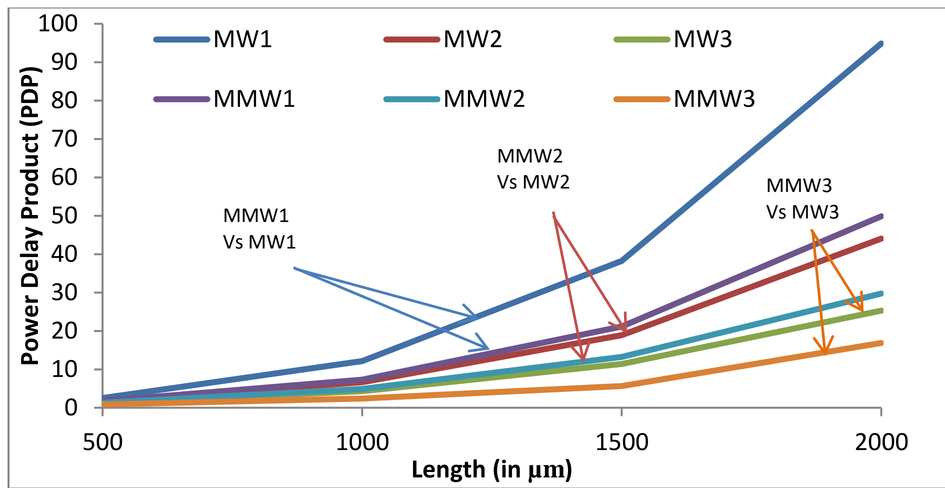
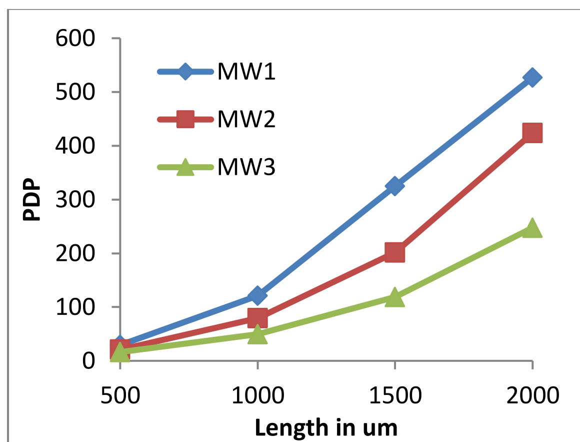


Figure 4.16: Combined comparative analysis for PDP of MW1-3 and MMW1-3 structures at 22nm technology node.

For 16nm technology:

Table 4.19: Power Delay Product (PDP) values for different structures at 16nm

Length of Bundle (in µm)	Power Delay Product (PDP) of different structures					
	MW1	MW2	MW3	MMW1	MMW2	MMW3
500	29.29056	20.81551	16.30222	22.80739	14.38842	8.722321
1000	120.8018	79.62979	49.43053	88.94384	54.41143	24.80866
1500	324.9912	201.3545	118.6286	228.4505	130.1939	52.69418
2000	526.9749	423.519	247.5266	487.0863	260.9238	95.45241



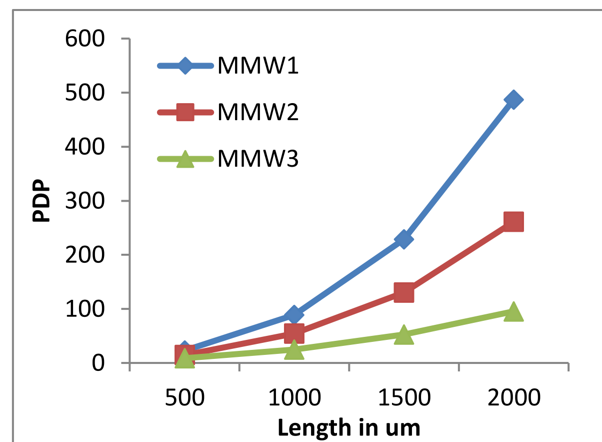


Figure 4.17 Individual comparative analysis in term of power delay product for (a) MW1-3 and (b) MMW1-3 structures respectively, for variable interconnects length at 16nm technology node.

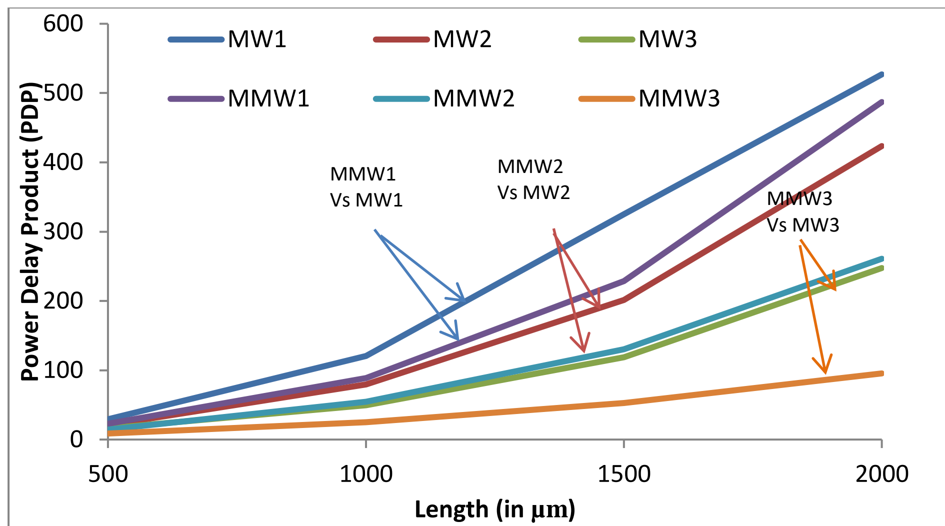
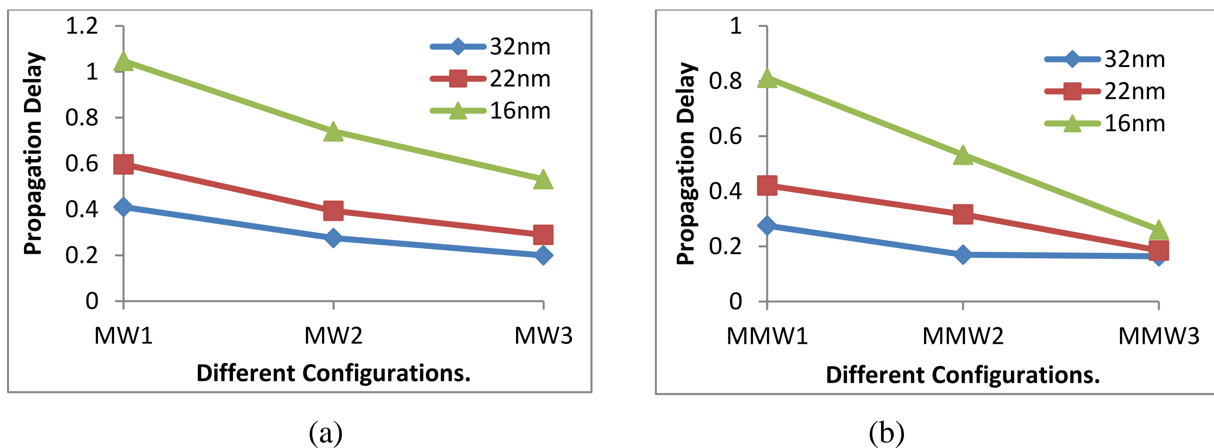


Figure 4.18 Combined comparative analysis for PDP of MW1-3 and MMW1-3 structures

4.5 Comparison Between Different Structures At A Given Interconnect Length And Different Technology Nodes:

At last a comparison between 32, 22 and 16nm technology nodes is also presented and shown in Figure 4.19. Figure 4.19 (a) and (b) shows the comparison of delay for different technology nodes (viz. 32nm, 22nm, 16nm) at 1000um interconnects length for MW1 and MMW1 structures respectively. It can be seen from the results that with scaled down technology nodes the delay increases and this increase in delay is minimum for MW3 and MMW3 structures as shown in Figure 4.19 (a) and (b) respectively.

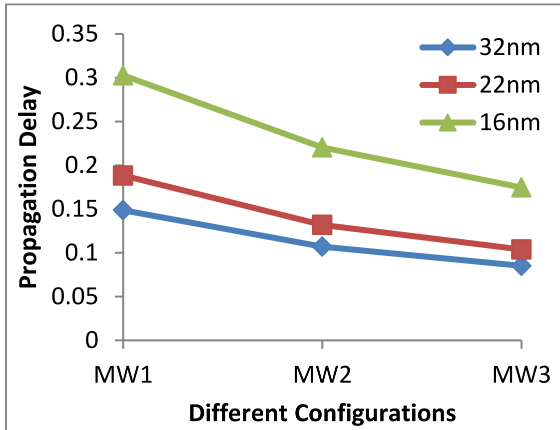


(a) (b)

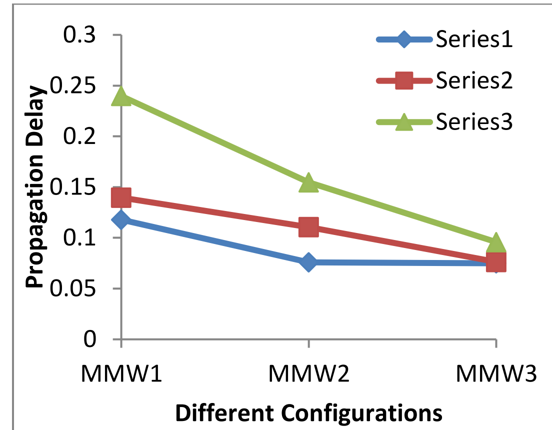
Figure 4.19: Delay comparison for different structures (a) MW and (b) MMW at different technology nodes and at 1000µm length

The similar analysis can be performed at other lengths viz. 500, 1500 and 2000µm as shown in Figures 4.20, 4.21 and 4.22 respectively.

At 500µm Length:



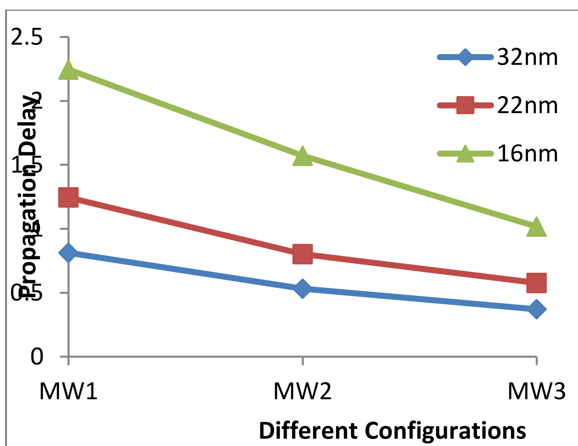
(a)



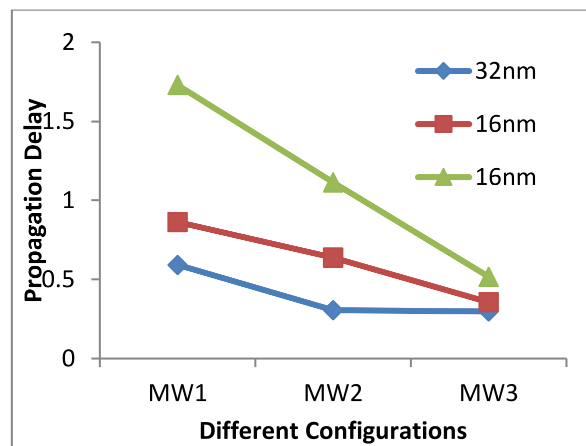
(b)

Figure 4.20: Delay comparison for different structures (a) MW and (b) MMW at different technology nodes and at 500µm length

At 1500µm Length:



(a)

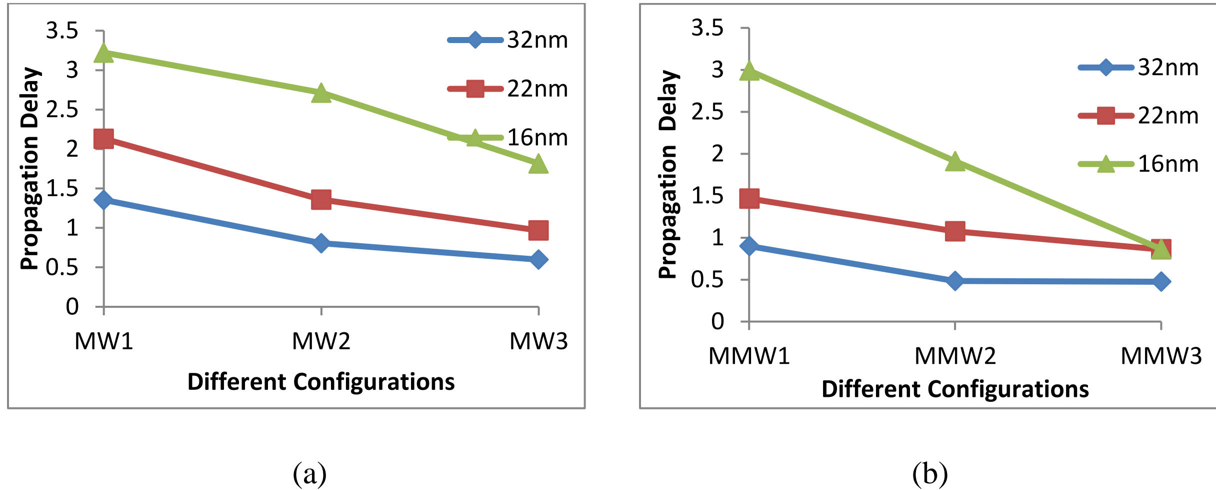


(b)

Figure 4.21: Delay Comparison for Different Structures (a) MW and (b) MMW At Different Technology Nodes And At 1500µm Length

At 2000μm Length:

Figure 4.22: Delay comparison for different structures (a) mw and (b) mmw at different technology nodes and at 2000μm length



(a) (b)

The above results can be inferred from the fact that for the given dimensions and area of the bundle the number of MWCNTs in MMW3 reduces and hence the number of conducting channels reduces. Due to this, there is decrease in C_{equ} and increase in R_{equ}. However, the diameter of MMW3 is large; the mean free path (MFP) is large which leads to overall decrease in Requ. Due to this, there are on the whole decrease in both capacitance and resistance values which reduced the propagation delay, power dissipation and PDP for MMW3 structure as compared to other structures. Hence, mixed multi walled carbon nanotubes (MMW) are always better than MWCNT bundles (MW) as predicted by the section 4.3, and among all the MMW structures MMW3 provides the best performance as demonstrated by section 4.4 and 4.5.

CHAPTER 5
CONCLUSION AND FUTURE SCOPE

5.1 CONCLUSION:

This report provided a detailed description for the various MWCNT bundle structures with identical and different number of shells of individual MWCNTs inside the bundle. The Multi-conductor Transmission Line (MTL) model of different structures is proposed. The ESC model for the proposed structure is presented and comparative analysis for all the structures in terms of propagation delay, power dissipation and PDP is also presented. It is concluded from the results that the propagation delay, power dissipation and PDP offered by all MW structures is higher as compared to MMW structures for the interconnect length ranging from 500µm-2000µm and at different technology nodes i.e. 32nm, 22nm, 16nm. Therefore, it is concluded that Mixed-multiwalled structures are more suitable alternatives for long interconnects as compared to conventional MW structures. Further, it is also revealed from the results that the performance of MMW3 structure is better in all aspect compared to the other structures. Hence, the Mixed MWCNT (MMW) bundle structures can be considered as the future VLSI interconnects for high performance and power efficiency.

5.2 FUTURE SCOPE:

1. The effect of tunneling conductance in the equivalent single conductor (ESC) model is neglected in most of the studies. The derivation of ESC model considering tunneling conductance needs to be studied.
2. The effect of the mutual inductance has not been considered in calculating the equivalent Inductance. Hence, more research work is needed to be done on this.
3. Further study on the more accurate fabrication process of CNTs is also required.

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