STUDY THE TEMPERATURE EFFECTS ON CROSSTALK IN GRAPHENE NANORIBBON INTERCONNECTS

Dissertation submitted in partial fulfilment of the requirements for the award of the degree of

Master of Technology

In

VLSI Design

Submitted by

Ramneek Sidhu

Roll. No. 601662015

Under the supervision of

Dr. Mayank Kumar Rai

Associate Professor, ECED

THAPAR INSTITUTE
OF ENGINEERING & TECHNOLOGY
(Deemed to be University)

Department of Electronics & Communication Engineering

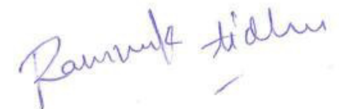
Thapar Institute of Engineering and Technology
(Deemed to be University),
Patiala, Punjab

June, 2018

DECLARATION

I Ramneek Sidhu hereby declare that the work presented in this thesis entitled "**Study the Temperature Effects on Crosstalk in Graphene Nanoribbon Interconnects**" in fulfilment of the requirement for the award of degree of Master of Technology (VLSI Design) submitted at ECED , Thapar Institute of Engineering & Technology (Deemed to be University), Patiala is an authentic record of work carried out under supervision of Dr. Mayank Kumar Rai, Assosiate Professor ,ECED, Thapar Institute of Engineering & Technology (Deemed to be University), Patiala. The matter presented in this has not been submitted either in part or full to any other university or institute for the award of any other degree.

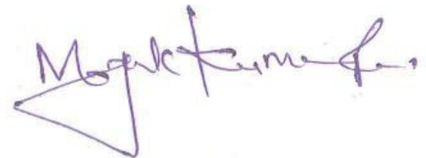
Date: ..23..June..2018



(Ramneek Sidhu)

(601662015)

It is certified that the above statement made by the student is correct to the best of my knowledge and be



Date : 23/06/2018

Dr. Mayank Kumar Rai,

Assosiate Professor, ECED,

Electronics And Communication Engineering Department

Thapar Institute Of Engineering & Technology

(A Deemed To Be University), Patiala, Punjab

ACKNOWLEDGEMENTS

I take this opportunity to express my profound sense of gratitude and respect to all those who helped me through the duration of this dissertation. I acknowledge with gratitude and humility my indebtedness to **Dr. Mayank Kumar Rai, Associate Professor,** Department of Electronics and Communication Engineering, Thapar Institute Of Engineering And Technology, Patiala, under whose guidance I had the privilege to complete this dissertation. I wish to express my deep gratitude towards him for providing individual guidance and support throughout the dissertation work.

I convey my sincere thanks to **Head of the Department, Dr. Alpana Agarwal**, entire faculty and staff of Electronics and Communication Engineering Department for their encouragement and cooperation.

My greatest thanks are to all who wished me success especially my family. Above all I render my gratitude to the Almighty who bestowed ability and strength in me to complete this work.

Ramneek Sidhu

ABSTRACT

Scaling plays an important role in the performance of a chip. But the effect of the parameter scaling in VLSI field has not been investigated in detail. Many researchers showed that multilayer graphene nanoribbons (MLGNR) are the best promising candidates for next generation of VLSI interconnect. Multilayer graphene nanoribbons (MLGNR) are preferred over copper interconnects and carbon nanotubes due to easy patterning by high resolution lithography and lower interconnect line resistance due to multiple conduction paths. So, it's the need of the hour to study the impact of parameter scaling in the MLGNR interconnects.

In this dissertation, the complete analysis of the functional and dynamic crosstalk and the impact of parameter scaling on the crosstalk in temperature-dependent capacitive coupled MLGNR interconnects is presented at 14 nm technology node. A capacitively coupled MLGNR model is used to find temperature-dependent impedance parameters for the three scaling conditions and results are compared with existing temperature-independent MLGNR interconnect impedance parameters at same technology node. Further, the dynamic and functional crosstalk occurring in the temperature-dependent MLGNR interconnect under the three scaling conditions is studied and compared with copper. The effect of various parameters such as interconnect length on crosstalk noise in temperature dependent and temperature-independent MLGNR interconnects propagation has been analysed.

LIST OF CONTENTS

Declaration		i
Acknowledgement		ii
Abstract		iii
Table of Content		v
List of Figure		viii
List of Tables		xi
List of Glossary		xii
Chapter 1:	**Introduction And Statement of Analysis**	1
1.1	Introduction	1
1.2	Statement of Problems	3
1.3	Organization of Thesis	3
Chapter 2:	**Literature Review**	4
2.1	Introduction	4
2.1.1	Types Of Interconnects	4
2.1.2	Materials Used	4
2.1.3	GNRs	5
2.1.4	Modeling Of Interconnects	7
2.1.4.1	Temperature Independent	7
2.1.4.2	Temperature dependent	12
2.1.5	Crosstalk	12
2.1.5.1	Temperature Independent	13
2.1.5.2	Temperature dependent	19
2.1.6	Scaling	20
2.2	Conclusion	21
Chapter 3:	**Temperature Dependent Circuit Modeling And Impedence Analysis Of MLGNR**	22
3.1	Introduction	22
3.2	Temperature Dependent Modeling Of MLGNR	22
3.2.1	RLC Computation of MLGNR interconnects	25

3.2.1.1 Resistance values at variable temperature for different MLGNR lengths 26
3.2.1.2 Inductance values at variable temperature for different MLGNR lengths 28
3.2.1.3 Capacitance values at variable temperature for different MLGNR lengths 30
3.3 Impedence Parameters Of Copper 32
3.4 Conclusion 33
Chapter 4: Effect Of Scaling On Temperature Dependent Crosstalk Analysis 34
4.1 Introduction 34
4.2 Scaling 34
4.3 Crosstalk Analysis In MLGNR 38
4.4 Conclusion 51
Chapter 5: A Comparative Analysis Between Results Obtained Through Temperature-Dependent And Temperature -Independent Models 52
5.1 Introduction 52
5.2 Analysis 52
5.3 Conclusion 54
Chapter 6 Concluding Remarks And Future Scope 55
5.1 Introduction 55
5.2 Summary 55
5.3 Future Scope 56

References 57

LIST OF FIGURES

Fig.2.1	Arm chair and zigzag GNR	5
Fig.2.2	MLGNR	6
Fig.2.3	Band structures of a semiconducting and b metallic armchair GNRs	6
Fig.2.4	Per unit length resistance values of various types of GNRs, monolayer SWNT interconnects, and copper wires versus width for lengths larger than the MFP	7
Fig.2.5	.(a) Multi-conductor circuit model of a dz-length MLGNR interconnect	9
	(b) ESC model of the MLGNR interconnect with its length	9
Fig.2.6	Percentage increase in resistance due to interlayer resistance for different length	11
Fig.2.7	Propagation delay of MLGNR for temperature-dependent and temperature-independent resistance models at different lengths	12
Fig.2.8	Coupled-line configuration	13
Fig.2.9	Typical noise waveforms for capacitive- and inductive-coupling noise explained using even–odd-mode theory	14
Fig.2.10	Measured and calculated noise peak for various input aggressor transition time	15
Fig.2.11	Absolute peak-noise voltage versus linewidth for capacitive, inductive and capacitive + inductive coupling	15
Fig.2.12	Noise waveforms for capacitive and inductive coupling (left) and for capacitive + inductive coupling (right) for three different linewidth	16
Fig.2.13	Absolute peak-noise voltage versus line self-inductance for capacitive, inductive, and capacitive + inductive coupling	16
Fig.2.14	Noise waveforms for capacitive and inductive coupling (left) and for capacitive + inductive coupling (right) for three different line self-inductances.[	17
Fig.2.15	Absolute peak-noise voltage versus line-to-line spacing for capacitive, inductive, and capacitive + inductive coupling	17
Fig.3.1	Schematic of an MLGNR	22
Fig.3.2	An equivalent RLC model of MLGNR interconnect	25
Fig.3.4	(a) Resistance plot for L_{MLGNR} 0.2mm	26

	(b)	Resistance plot for L_{MLGNR} 0.4mm	26
	(c)	Resistance plot for L_{MLGNR} 0.6mm	27
	(d)	Resistance plot for L_{MLGNR} 0.8mm	27
	(e)	Resistance plot for L_{MLGNR} 1 mm	27
Fig.3.5	(a)	Inductance plot for L_{MLGNR}=0.2mm	28
	(b)	Inductance plot for L_{MLGNR}=0.4mm	28
	(c)	Inductance plot for L_{MLGNR}=0.6mm	28
	(d)	Inductance plot for L_{MLGNR}=0.8mm	29
	(e)	Inductance plot for L_{MLGNR}=1mm	29
Fig.3.6	(a)	Capacitance plot for L_{MLGNR}= 0.2mm	30
	(b)	Capacitance plot for L_{MLGNR}=0.4 mm	30
	(c)	Capacitance plot for L_{MLGNR}=0.6mm	31
	(d)	Capacitance plot for L_{MLGNR}=0.8mm	31
	(e)	Capacitance plot for L_{MLGNR}=1 mm	31
Fig.4.1	Resistance values at different temperature for varied scaling cases.		37
Fig.4.2	Inductance values at different temperature for varied scaling cases.		38
Fig.4.3	Capacitance values at different temperature for varied scaling cases		38
Fig.4.4	MLGNR interconnect model		38
Fig.4.5	Crosstalk noise for s=w at temp 300 K		46
	(a) MLGNR		46
	(b) Cu		46
Fig.4.6	Crosstalk noise for s=3w/2 and w=w/2 at 300K		47
	(a) MLGNR		47
	(b) Cu		47
Fig.4.7	Crosstalk noise for s=w/2 and w=3w/2 at 300K		48
	(a) MLGNR		48
	(b) Cu		48
Fig.4.8	Crosstalk induced positive peaks with temperature for different scaling conditions		49
	(a) MLGNR		49

	(b) Cu	49
Fig.4.9	Time duration variation of victim output with temperature for different scaling conditions	50
	(a) MLGNR	50
	(b) Cu	50
Fig.4.10	Normalized delay of aggressor line w.r.t temperature	51
Fig.5.1	Crosstalk induced positive peaks for the different lengths at the far end of the victim line	53
Fig.5.2	Time duration of victim output interconnect length	53

LIST OF TABLES

Table 3.1	Resistance values for 0.2mm length	26
Table 3.2.	Resistance values for 0.4mm length	26
Table 3.3.	Resistance values for 0.6mm length	27
Table 3.4.	Resistance values for 0.8mm length	27
Table 3.5.	Resistance values for 1mm length	27
Table 3.6	Inductance values for L_{MLGNR}=0.2mm	28
Table 3.7	Inductance values for L_{MLGNR}=0.4mm	28
Table 3.8	Inductance values for L_{MLGNR}=0.6mm	28
Table 3.9	Inductance values for L_{MLGNR}=0.8mm	29
Table 3.10	Inductance values for L_{MLGNR}=1mm	29
Table 3.11	Capacitance values for L_{MLGNR} =0.2mm	30
Table 3.12	Capacitance values for L_{MLGNR} =0.4mm	30
Table 3.13	Capacitance values for L_{MLGNR} =0.6mm	31
Table 3.14	Capacitance values for L_{MLGNR} =0.8mm	31
Table 3.15	Capacitance values for L_{MLGNR} =1mm	31
Table 4.1	Simulation parameters	35
Table 4.2	R,L and C values for temperature dependent and temperature independent models for varied scaling cases at l=1mm.	36
Table 4.3	R,L and C values for temperature dependent and temperature independent models for varied scaling cases at l=0.8mm.	36
Table 4.4	R,L and C values for temperature dependent and temperature independent models for varied scaling cases at l=0.6mm.	36
Table 4.5	R,L and C values for temperature dependent and temperature independent models for varied scaling cases at l=0.4mm.	37
Table 4.6	R,L and C values for temperature dependent and temperature independent models for varied scaling cases at l=0.2mm.	37
Table 4.7	Functional Crosstalk for s=w.	40
Table 4.8	Functional crosstalk for s=3w/2 and w=w/2.	41
Table 4.9	Functional crosstalk for s=w/2 and w=3w/2.	42

Table 4.10 Dynamic Crosstalk for s=w 43

Table 4.11 Dynamic Crosstalk for s=3w/2 and w=w/2 44

Table 4.12 Dynamic Crosstalk for s=w/2 and w=3w/2 45

Table 5.1 Time duration improvement 54

LIST OF GLOSSARY

AR	Aspect Ratio
IC	Integrated Circuit
LSI	Large Scale Integration
CMOS	Complementary Metal Oxide Semiconductor
CNT	Carbon Nanotube
EM	Electo-Magnetism
FET	Field Effect Transistor
GNR	Graphene Nanoribbon
MLGNR	Multilayer Graphene Nanoribbon
GaAs	Gallium Arsenide
GHz	Giga Hertz
MFP	Mean Free Path
MSI	Medium Scale Integration
MWCNT	Multi Walled Carbon Nanotube
RC	Resistance-Capacitance
RLC	Resistance-Inductance-Capacitance
SPICE	Simulation Program with Integrated Circuit Emphasis
SWCNT	Single Walled Carbon Nanotube
VLSI	Very Large Scale Integration

CHAPTER-1

INTRODUCTION AND STATEMENT OF ANALYSIS

1.1 INTRODUCTION

Interconnects are physical connecting mediums chip used to transmit signals from one point to another, made of thin metal films and are present between several electrical nodes in a semiconducting VLSI chip [1-3]. There are a variety of materials used to design interconnects as Aluminum, Copper, Carbon Nanotubes (CNTs), Graphene Nano Ribbons (GNRs) etc [4-7]. The most recent interconnect materials evolved are Carbon Nanotubes (CNTs) and Graphene Nano ribbons (GNRs). These materials are more reliable as compared to copper as they exhibit better thermal conductivity, higher current carrying capability, lower electrical resistivity, and have larger mean free path (MFP) [7]. CNTs are rolled up hollow cylindrical sheets of graphene. CNTs conduct large current without signal deterioration and electromigration [8]. Another material used is GNR. The unrolled version of CNTs form GNRs. As compared to CNTs, the patterning of GNR interconnects is easy and can be done by high resolution lithography plus multi-layer GNRs(MLGNRs) offer lower interconnect line resistance due to multiple conduction paths[9-12]. Thus, MLGNRs are preferred over SLGNRs (Single Layer Graphene Nano Ribbons) and CNTs. MLGNRs can be of the type, viz., Armchair GNRs (ac-GNRs) and Zigzag GNRs (zz-GNRs) based upon their chirality. Further, the ac-GNRs are metallic or semi conducting, whereas zz-GNRs are always used as metallic interconnects [6]. Multi-layer GNR interconnects having N -layers can be classified as top-contact and side-contact MLGNRs depending upon the type of contacts. Top contact MLGNRs (TC-MLGNRs) have only the topmost layer coupled with contacts however, in the case of side-contact MLGNRs (SC-MLGNRs), all the layers are in physical connection with contacts [12].

Crosstalk is an undesirable voltage glitch degrading the performance of interconnects. When a transition occurs in an interconnect, it causes crosstalk in adjacent interconnects [20]. The crosstalk can be categorized as functional and dynamic crosstalk. In functional crosstalk noise, a voltage spike is experienced by the victim line because of the switching of the aggressor line, itself being fixed. The dynamic crosstalk occurs for synchronous switching. The lines switchng in the same direction,

lead to the occurrence of the even mode dynamic crosstalk and the switching in the opposite direction causes odd mode dynamic crosstalk [19,20]. All the works reported to date have analyzed and evaluated the temperature dependent crosstalk induced noise voltage in CNTs [17,19,20,21]**.** Very less work has been done on the temperature dependent crosstalk in MLGNRs. M.K. Rai et.al [37] studied the impact of variations in the temperature on delay, power dissipation, and crosstalk –induced voltage noise waveform of capacitively coupled MLGNR interconnects for the temperature varying from 300 to 500 K at the far end of the victim line. The results were compared with that of copper.. It was demonstrated that MLGNR has better performance as compared to copper.

In deep submicron (DSM) technology a node, the major challenge to next generation carbon material based interconnects are thermal issues [36]. The temperature dependent variations above room temperature affect the delay, power dissipation and crosstalk in the interconnect materials [35-37].In the case of CNTs, the simulation results showed that delay occurring due to the crosstalk increases significantly and performance and reliability degrade while the temperature is raised. However, in MLGNR the temperature-dependent delay and the power-dissipation is less for global interconnects.It is obligatory to analyze the temperature dependent behavior of MLGNR in more detail [37].

In deep nanometer scale technologies, it is necessary to present a detailed analysis of thermal scaling in multilevel interconnects. These results are helpful in augmenting the reliability, performance, for generating thermal awareness in interconnect design issues and for backend thermal management [40].Various researchers have studied the temperature-independent effect of scaling in Cu interconnects [42-45]. S.Sarkar et.al [46] presented the effects of scaling the interconnect dimensions for the capacitively coupled CNT model and found that capacitive coupling provided better reduction in crosstalk noise but no work has been reported on the scaling effect on the interconnect dimensions using the temperature dependent model of the MLGNR interconnect. In this paper, the impact of interconnect dimension scaling on the crosstalk noise voltage using the capacitively coupled temperature dependent model was studied. The induced noise peaks and time duration of the crosstalk noise voltage for the different scaling conditions are then plotted against temperature. The results are further compared with copper. This paper also analyses the effect of interconnect length on

the crosstalk induced voltage noise for the temperature dependent and temperature independent circuit models. The temperature dependent circuit models for different scaling conditions are analyzed with respect to interconnect length.

1.2 STATEMENT OF PROBLEMS

The objectives of the research work are:

1. Development of temperature dependent circuit parameters of side contacts and top contacts MLGNR based interconnects.
2. To review the effect of temperature dependent parameter variations on crosstalk in capacitively coupled MLGNR based interconnects.
3. To analyse the temperature-dependent crosstalk induced voltage noise.
4. Comparison of result obtained from above analysis with results for copper interconnects at 14nm technology

1.3 ARRANGEMENT OF THESIS

Chapter 1 presents the brief introduction of the complete dissertation. The statement of problems and the objective of the complete research work.

Chapter 2 describes the brief introduction of the MLGNR interconnects. The types of MLGNRs and the materials used for fabricating MLGNRs are studied.

Chapter 3 presents the complete impedance analysis of the MLGNR inters connects. With the help of the suitable model, the temperature- dependent R.L.C values are computed and plotted for the capacitively coupled MLGNR model. Accordingly, various results are verified.

Chapter 4 presents the impact of scaling the interconnect parameters on the MLGNR performance. The three cases of scaling the width and spacing parameters in an MLGNR interconnect are presented and the behaviour of the inter connect is studied under these cases.

Chapter 5 presents the performance comparison of the temperature-independent and temperature-dependent models of capacitively coupled MLGNR model. The role of the interconnect length in also analysed in this chapter.

Chapter 6 demonstrates the conclusions and future scope of the research.

CHAPTER 2

PERFORMANCE ANALYSIS – A REVIEW

2.1 INTRODUCTION

This chapter involves the basic introduction about VLSI interconnects and interconnect materials for VLSI design. As the demand for more number of circuit components on a single chip is increases, it necessitates the generation of nano-electronic devices and their interconnects. Interconnects is a physical connecting medium used to transmit signals from one point to another, made of thin metal films and present between several electrical nodes in a semiconducting VLSI chip It is a connection between elements. Interconnects in an IC are physical connections between two transistors and/or the external world. They can be employed for connecting components on a VLSI chip, chips on a multichip and multichip modules on a system board. Based on the dimension, interconnects can be of the type -

2.1.1 Types Of Interconnects

1. Local- It is used to make connection of the gates and transistors to a functional block on the chip.
2. Intermediate/semi global- Within a functional block, it provides clock and signal distribution within length of 3-4mm.
3. Global-It delivers powers and ground to all functions in the chip longer than 4mm

Based on the signaling, interconnects can be defined as Clocking and Power/ground distribution interconnects.

2.1.2 Materials Used

There is a wide variety of interconnect materials. However, the earliest material used as an interconnect was the aluinium. Aluminum has a wide range of properties as low cost, easily purified, low resistivity, good adherence to Si and SiO_2, good pattern ability and ease of deposition. But it caused limitation of decreased device dimension which caused increase in the current density and decreased reliability. So, the solution was the use of alternative metals .Thereby, copper was the preferred interconnect material. For IC-applications, copper presents superior performance and can endure about five times more current density with equal reliability. Because of the higher conductivity, higher melting point (1357K) than Al (933K) ,it is several times more

resistant to electro migration than aluminum. The grain boundary scattering and surface roughness causes decrease in the cross-section of the copper interconnect and increase in the resistivity thereby causing increase in power dissipation, propagation delay and electromigration. The next was the development of the Carbon Nano Tubes (CNT).They conduct large current without signal deterioration and electro migration problems. Even when the feature size deceases, CNTs supports ballistic flow of electrons with an electron free mean path. Another material used is Graphene Nanoribbons (GNR). Graphene can be defined as a sheet of graphite packed tightly in a two-dimensional (2D) honeycomb lattice structure. Further, a single sheet of graphene layer resulting in a one-dimensional structure, that is very thin and limited in width is termed as a graphene nanoribbon and. The unrolled CNTs form GNRs.

2.1.3 GNRs

. Graphene can be defined as a sheet of graphite packed tightly in a two-dimensional (2D) honeycomb lattice structure.. . Further, a single sheet of graphene layer resulting in a one-dimensional structure, that is very thin and limited in width is termed as a graphene nanoribbon and. The unrolled CNTs form GNRs. In comparison with CNTs, GNR interconnects can be patterned easily by high resolution lithography plus multi-layer GNRs(MLGNRs) offer lower interconnect line resistance due to multiple conduction paths.

GNRs can be divided into armchair (ac) or zigzag (zz) GNRs depending on termination of their width,.

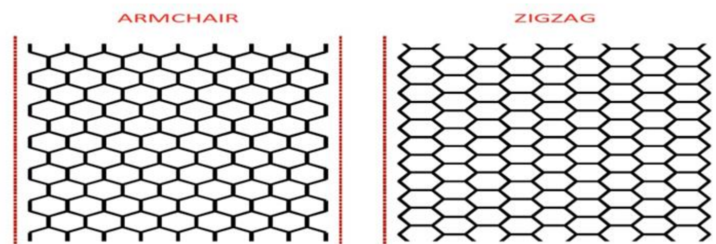


Figure 2.1: Arm chair and zigzag GNR [1].

GNRs can be discriminated as single-layer GNR (SLGNR) or multilayer GNR (MLGNR) based upon the stacking of the graphene sheets. The higher current

carrying capability of MLGNRs as compared to the SLGNR makes MLGNRs as the most promising interconnect solution for VLSI interconnect.

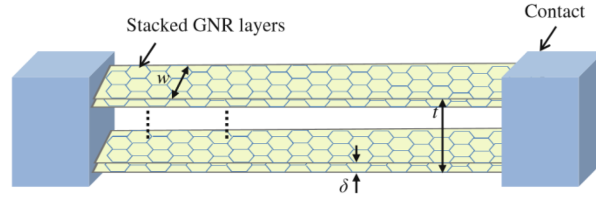


Figure 2.2: MLGNR [2].

GNR can be of the type metallic or semiconducting. In the case of the metallic GNRs, there is zero bandgap, whereas in the case of the semiconducting GNRs 0.2 eV band gap exists. The zigzag GNRs are always metallic in nature. The armchair GNRs can be of the type, either metallic or semiconducting .The ac GNR are metallic in nature, if Nc =3 a + 2 and acts as semiconducting, if Nc =3 a + 1 or 3. Here a is an integer and N_c is the no. of carbon atoms across its width.

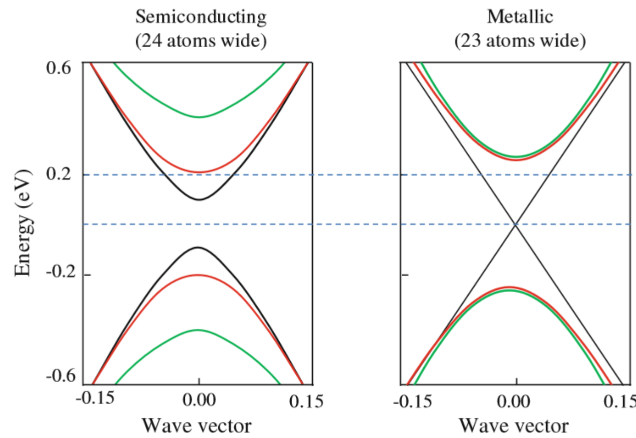


Figure 2.3: Band structures of a semiconducting and b metallic armchair GNRs whose widths are 6.02 nm (24 atoms wide) and 5.78 nm (23 atoms wide), respectively [3].

The MLGNR interconnect is formed of N layers of SLGNR stacked over one-another.The multi-layer GNR interconnects,i.e., the MLGNRs can be classified as top-contact and side-contact MLGNRs depending upon the type of contacts. In the case of Top contact MLGNRs (TC-MLGNRs) there is only the topmost layer coupled with contacts however, in the latter, all the layers are physically connected to contacts. The equivalent resistance of side-contact MLGNRs (SC-MLGNRs) is found to be

lesser than that of top-contact MLGNR (TC-MLGNRs)[16] because of the lower interlayer resistance per unit interconnect length. Hence, side-contact MLGNRs (SC-MLGNRs) stand better performance characteristics. In the present study, MLGNR is assumed to be side-contact MLGNR (SC-MLGNR).

2.1.4 Modeling Of Interconnects

2.1.4.1 *Temperature Independent*

Most of the earlier work has been done on the temperature independent modelling of GNRs. In these papers, firstly the conductance of the GNR was studied thoroughly with all the factors affecting it. In the band structure of graphene, all sub bands whose En ≤ Ef are populated and provide one conduction channel contributing one quantum conductance G0 = 2e^2/h = 1/(13 kΩ). The total conductance in a GNR can be computed as:

$$G = \frac{2e^2}{h} \sum_n \frac{1}{1 + L(1/l_D + 1/l_n)} \quad (1)$$

where L is the GNR's length, l_D is the MFP corresponding to scatterings by defects and phonons and *ln* is the MFP associated with the diffusive scatterings at the edges of the MLGNR. Wide (> 100 nm) metallic and semiconductor GNRs have similar conductances, narrow semiconductor GNRs have larger resistances, and below 5-nm widths, they become virtually insulators. The increase in the Fermi level makes more sub bands populated and, therefore, increases conductance. It does not improve the performance of narrow GNRs.[3]

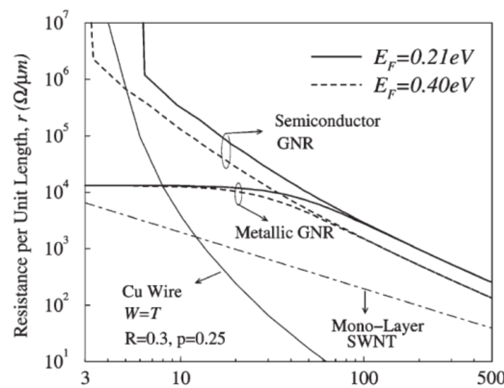


Figure 2.4: Per unit length resistance values of various types of GNRs, monolayer SWNT interconnects, and copper wires versus width for lengths larger than the MFP [3].

Further, T. Ragheb et. al [5], further worked on a comprehensive model for modelling of resistance and also studied the effect of scattering on the resistance. The

scattering is caused due to defects λ_S, static impurities λ_L and diffusive edge scattering λ_E^m and can be represented as:

$$\frac{1}{\lambda_{eff}^m} = \frac{1}{\lambda_S} + \frac{1}{\lambda_L} + \frac{1}{\lambda_E^m} \quad (2)$$

According to the above discussion, the total conductance of the graphene nanoribbon is given as:

$$G = \frac{2e^2}{h} \sum_m \frac{1}{1 + L / \lambda_{eff}^m} \quad (3)$$

Further, the impact of stacking of GNR layers on the performance of multi-layer GNR interconnects was modelled. The performance of multilayer GNR interconnects was compared with both copper interconnects and SWCNT bundle interconnects using the developed models. The results showed that the GNRs have superior performance over conventional copper interconnects for small widths (< 15 nm).[5]

Later, C.Xu et. Al [6], analyzed monolayer, neutral multilayer, and intercalation-doped multilayer zz-GNR interconnects from both conductance and propagation delay point of view. A comparative analysis (with other interconnect materials: Cu, CNTs, and W) revealed that GNRs have some fabrication advantages over CNTs (for horizontal interconnects) and Cu at both the global and local levels. Therefore, zz-MLGNRs should be designed with proper intercalation doping and very specular edges (p > 0.8) to be better than Cu or CNT interconnects at either the global or local level. However, intercalation-doped multilayer zz-GNRs at the local level have better performance than even that of tungsten (even for p = 0), implying possible application as local interconnects in some cases.[7]

Further, more models for MLGNRs were developed and studied. ESC model was studied next with inductive and capacitive couplings between neighboring layers. With the help of ESC model, all lumped elements in the multilayer GNR interconnect are extracted and compared with that of Cu wires. It is shown that MLGNR interconnects can provide smaller per-unit-Iength resistance and better performance than those of Cu wire with the same size in nano-scale [11].

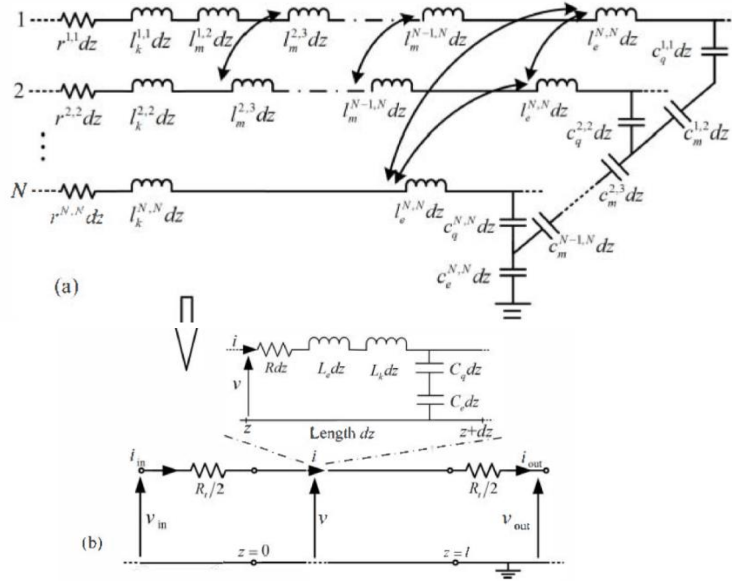


Figure 2.5: (a)Multi-conductor circuit model of a dz-length MLGNR interconnect. (b) ESC model of the MLGNR interconnect with its length I[11].

S.Rakheja et.al [12] discussed the detailed prospects of using graphene as an interconnect material that could replace copper in future Si microchips. Signal transport mechanisms and models for graphene were presented and compared to copper. The possibility of electron spin injection in graphene wires was further explored. It was analysed that the electron mobility in grapheme and edge roughness limits the performance of graphene-based devices. MLGNRs are preferred to provide more conduction channels and lower the resistance. In the spintronic applications, long spin-relaxation time is affected by metallic atoms and speed is limited by electronic MFP. While short, local interconnects may be used to transfer spin currents, global MLGNR interconnects are likely to be electrical.

Analytical times domain models for side contact and top contact multilayer graphene nanoribbon (MLGNR) interconnect were proposed in the following papers [16].

The top an d side contact resistance can be calculated as:

$$(R_N)_{TC} = \left(\frac{1}{R_{N-1} + R_Y} + \frac{1}{R_X} \right)^{-1} \tag{4}$$

$$(R_N)_{SC} = \left(\frac{R_X}{N} \right) \tag{5}$$

The interlayer resistance turns out to be:

$$R_Y = \frac{\rho_c \delta}{w \Delta x} \quad (6)$$

The kinetic inductance be

$$L_k = \frac{h / 4e^2 v_F}{nN_{ch}} \cong \frac{8nH}{nN_{ch}} (um) \quad (7)$$

The capacitance can be calculated by

$$C_q = \frac{4e^2 nN_{ch}}{hv_F} \quad (8)$$

$$C_e = \varepsilon M \left[\tanh\left(\frac{\pi w}{4y} \right) \right] \quad (9)$$

$$M(a) = \begin{cases} \dfrac{2\pi}{\ln \dfrac{2.\left(1+\sqrt[4]{1-a^2}\right)}{\left(1-\sqrt[4]{1-a^2}\right)}}, 0 \le a < \dfrac{1}{\sqrt{2}} \\ \dfrac{2}{\pi} \ln \dfrac{2\left(1+\sqrt{a}\right)}{\left(1-\sqrt{a}\right)}, \dfrac{1}{\sqrt{2}} \le a \le 1 \end{cases} \quad (10)$$

The overall parameters can be found as

$$\begin{aligned} R &= R_N \\ L &= L_K + L_M \approx L_K \\ C &= (C_Q^{-1} + C_Q^{-1})^{-1} \end{aligned} \quad (11)$$

It was also presented that the performance of MLGNRs can be analysed by introducing the optimization terms as g(the ratio between the improved and the normal interlayer conductance for TC-MLGNR interconnect) and delay ratio(ratio of delay for SC- and TC-MLGNRs, respectively). Thereby, an optimum TC-MLGNR interconnect was designed that exceeded the performance of Cu and optical interconnects. The performance optimization of TC-MLGNRs was done by considering various factors that include interlayer conductance, Fermi energy, and line geometry. Further, our optimized top contact interconnect matches the theoretical

performance limits of side contact GNRs reducing the need for complex fabrication process required for making side contacts.

M.K.Rai, A.K.Chatterjee, S.Sarkar and B.K.Kaushik et al[17] addressed the impact of interlayer resistance due to c-axis resistivity and contact resistance on performance of MLGNRs in terms of delay, power dissipation and power delay product (PDP) .

$$R_{eq} = \frac{R_{MC}}{N} + M.R_S \qquad (l_{GNR} > \lambda) \tag{12}$$

The impact of model parameter i.e. Fermi energy (EF) on performance of MLGNR was also discussed.

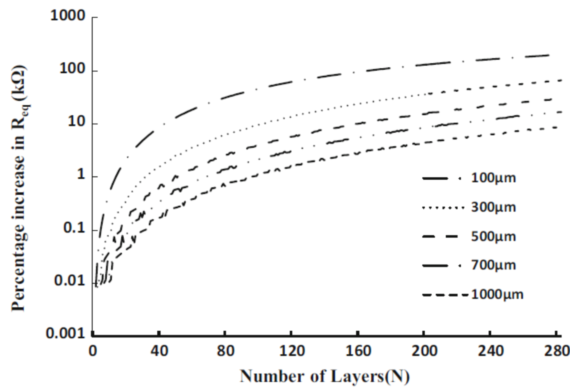


Figure 2.6: Percentage increase in resistance due to interlayer resistance for different lengths [17].

A similar analysis has been performed for copper interconnect and results are compared with MLGNR at 22nm technology node. The impact of interlayer resistance on equivalent resistance of MLGNR was critically analysed. In this analysis, inductive and capacitive couplings between the adjacent layers were included. It was found that the MLGNR with interlayer resistance gives better performance in terms of delay, power dissipation and PDP with higher value of Fermi energy for semi global to global lengths of interconnect (300–1000μm) compared to copper, whereas reverse is true for local lengths 100–200 (μm). It was further demonstrated that the performance gap between MLGNR with and without interlayer resistance decreases with rise in Fermi energy.

2.1.4.2 *Temperature Dependent*

The influence of temperature variations on delay, power dissipation, and crosstalk-induced voltage noise waveform at the far end of victim line of MLGNR interconnects has been examined at temperature ranging from 300 K to 500 K. It was revealed that, compared with copper, the delay and power dissipation in MLGNR interconnects was significantly low with increase in the temperature due to low resistance and capacitance of MLGNR. It shows an average relative improvement of 37.24% in 90% propagation delay and corresponding improvement in power dissipation of approximately 19.59% with interconnect lengths varying from 200 to 1000 μm. The temperature-dependent model of MLGNR resistance achieves an average relative improvement of approximately 35% in the time duration reduction of the capacitively coupled victim output over these interconnect lengths. Thus, these results show that MLGNR interconnects are found to have better performance and more reliable in DSM technology at 22 nm technology node than that of copper counterpart due to weak dependence of MLGNR resistance on temperature. To comprehend the extraordinary thermal properties of MLGNRs, it is necessary to analyses the temperature dependent behavior of MLGNR in more detail.[18]

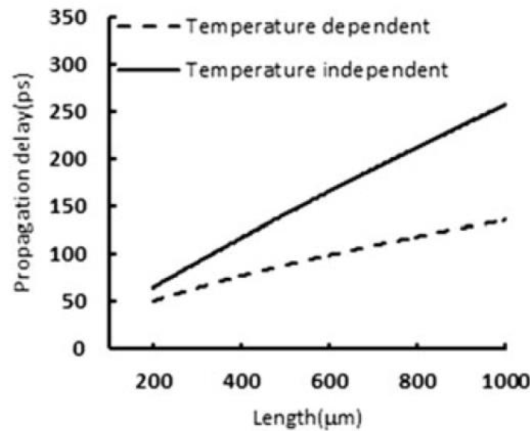


Figure 2.7: Propagation delay of MLGNR for temperature-dependent and temperature-independent resistance models at different lengths [18].

2.1.5 Crosstalk

Crosstalk is an undesirable voltage glitch degrading the performance of the interconnects. It occurs due to transition in one or more adjacent interconnects. The switching line is the aggressor line and the quiet line is the victim line. Thus, crosstalk leads to noise peaks and delay at the near end and the far end of the aggressor line and

the victim lines. The crosstalk can be categorized as functional and dynamic crosstalk. In functional crosstalk noise, a victim line experiences a voltage spike due to switching of the aggressor line, itself being fixed. The dynamic crosstalk occurs for synchronous switching. Further when both the lines switch in the same direction, the even more dynamic crosstalk occurs and when they switch in the opposite direction, they cause odd mode dynamic crosstalk

2.1.5.1 Temperature Independent

Modeling and analysis of crosstalk noise in coupled RLC interconnects was earlier proposed by K. Agarwal, D. Sylvester and D. Bllaauw [20].They proposed that at current operating frequencies, inductive-coupling effects can be significant and should be included for accurate crosstalk-noise analysis. The paper presented an analytical framework to model crosstalk noise in coupled RLC interconnects.

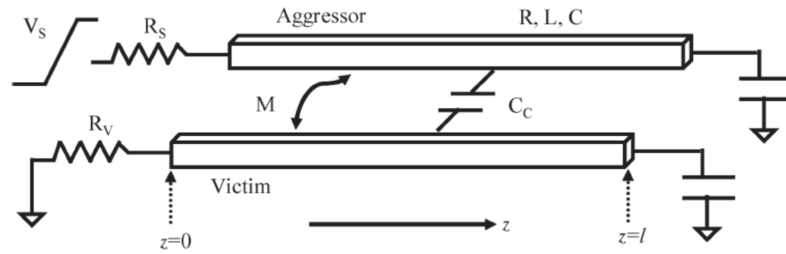


Figure 2.8: Coupled-line configuration. [20].

The even- and odd-mode characteristic impedances and times of flight for capacitive and inductive coupling are given by the following expressions. For capacitive coupling only

$$t_{fe} = l\sqrt{CL} \qquad \text{And} \qquad Z_{Oe} = \sqrt{\frac{L}{C}}$$
$$t_{fo} = l\sqrt{(C+2C_C)L} \qquad\qquad Z_{Oo} = \sqrt{\frac{L}{(C+2C_C)}} \qquad (13)$$

Similarly, for inductive coupling only

$$t_{fe} = l\sqrt{C(L+M)} \qquad \text{and} \qquad Z_{Oe} = \sqrt{\frac{(L+M)}{C}}$$
$$t_{fo} = l\sqrt{C(L-M)} \qquad\qquad Z_{Oo} = \sqrt{\frac{(L-M)}{C}} \qquad (14)$$

For pure capacitive coupling, the even-mode time of flight is less than the odd-mode time of flight. On the other hand, for pure inductive coupling, the negative odd-mode step travels faster than the positive even-mode step, thereby resulting in a negative-polarity noise pulse

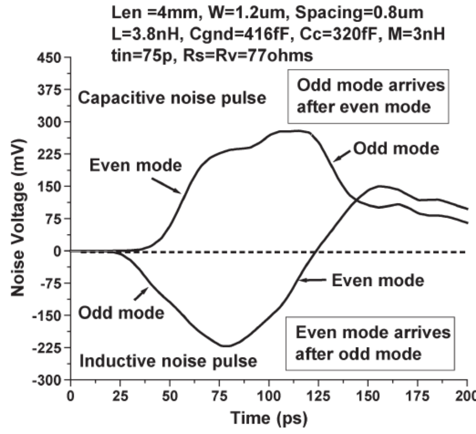


Figure 2.9: Typical noise waveforms for capacitive- and inductive-coupling noise explained using even–odd-mode theory [20].

Similarly, the case of two coupled lines with different line parasitics can be computed as

$$t_{fe} = l\sqrt{\frac{(a_1 + a_2) + \sqrt{(a_1 - a_2)^2 + 4b_1b_2}}{2}}$$

$$t_{fo} = l\sqrt{\frac{(a_1 + a_2) - \sqrt{(a_1 - a_2)^2 + 4b_1b_2}}{2}}$$

(15)

Further, the validation of the model was verified by comparing it to SPICE simulations.

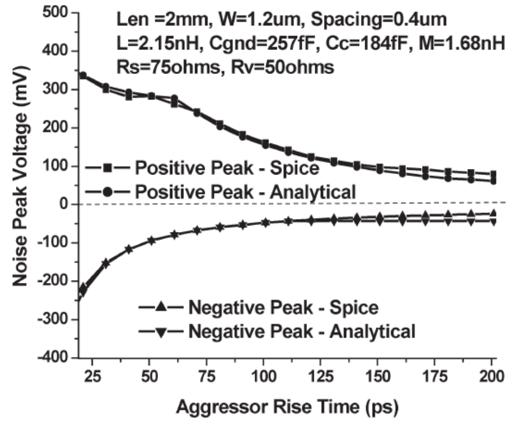


Figure 2.10: Measured and calculated noise peak for various input aggressor transition time. [20].

The figure shows that the proposed model works well over a wide range of aggressor rise time typically observed in high-frequency interconnects.

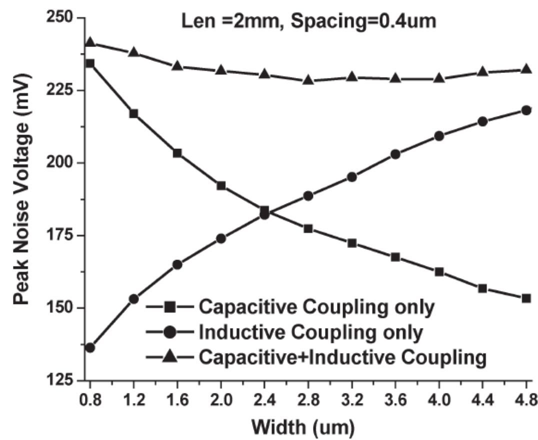


Figure 2.11: Absolute peak-noise voltage versus linewidth for capacitive, inductive and capacitive + inductive coupling [20].

The figure shows that as the linewidth increases, noise peak due to capacitive coupling reduces, while the noise peak due to inductive coupling increases. The actual noise peak is not very sensitive to the width.

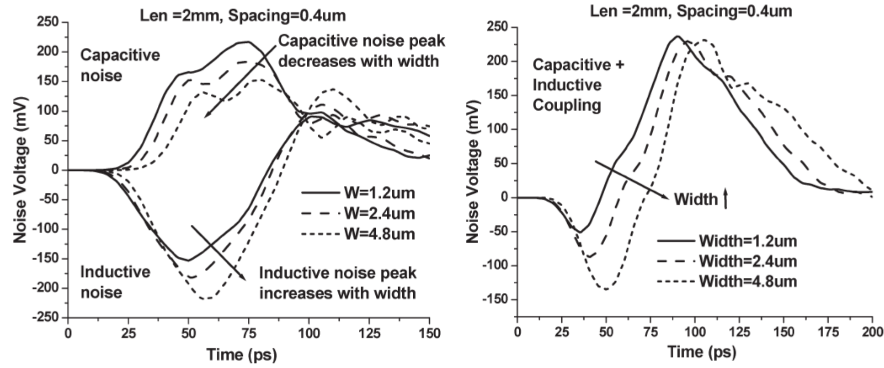


Figure 2.12: Noise waveforms for capacitive and inductive coupling (left) and for capacitive + inductive coupling (right) for three different linewidth [20].

Above figure showed the waveforms for capacitive, inductive, and both coupling cases for three different linewidths.

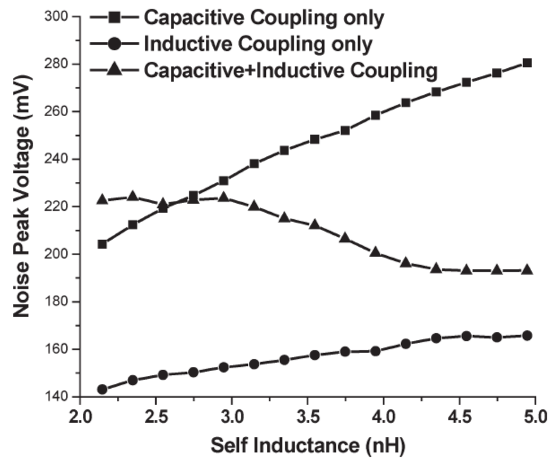


Figure 2.13: Absolute peak-noise voltage versus line self-inductance for capacitive, inductive, and capacitive + inductive coupling [20].

The figure shows that as self inductance increases, noise peak due to capacitive coupling increases significantly. Noise peaks while considering inductive coupling only as well as the total noise considering both couplings are not very sensitive to the width.

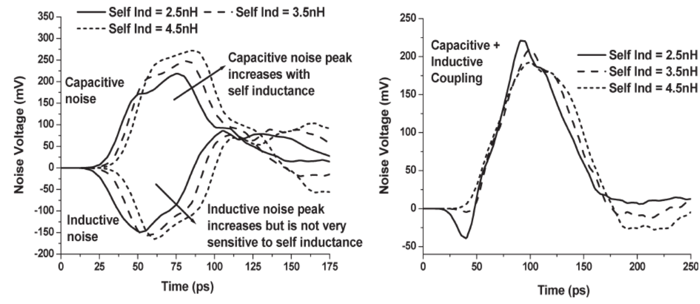


Figure 2.14: Noise waveforms for capacitive and inductive coupling (left) and for capacitive + inductive coupling (right) for three different line self-inductances.[20]

It shows SPICE waveforms for capacitive, inductive, and total coupling cases for three different self-inductances.

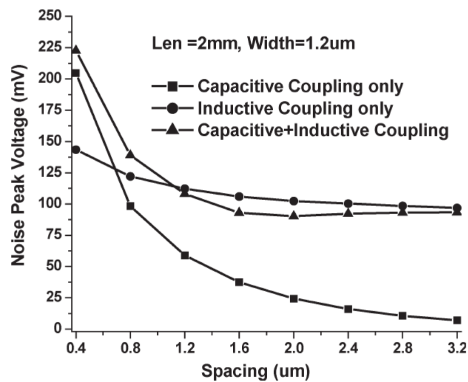


Figure 2.15: Absolute peak-noise voltage versus line-to-line spacing for capacitive, inductive, and capacitive + inductive coupling [20].

The figure showed that with increased spacing, noise peaks due to both capacitive and inductive coupling reduce. As expected, the reduction in inductive noise was not as significant as that in the capacitive noise. The analysis shows that in the presence of mutual inductance, crosstalk noise behaves very differently as compared to the noise behavior under purely capacitive coupling. It was concluded that traditional capacitive coupling based physical-design noise optimizations are not always effective when both capacitive and inductive coupling are considered together, and new layout guidelines must be developed for effective reduction of crosstalk noise in coupled RLC wires.[21].

B.K.Kaushik and S. Sarkar et. al[22] dealt with crosstalk analysis of a CMOS driven capacitively and inductively coupled interconnect. The Alpha Power Law model of MOS transistor is used to represent a CMOS driver. This is combined with a

transmission line-based coupled RLC model of interconnect to develop a composite model for analytical purpose. On this basis a transient analysis of crosstalk noise is carried out. Comparison of the analytical results with SPICE extracted results shows that the error involved is nominal.

In the tables, the accuracy of proposed model is tested by comparing the analytically obtained results with SPICE simulations. The comparisons with SPICE show that the model captures noise peaks, timing and waveform shape quite well. The proposed model is useful for accurate no is estimation in the presence of inductive effects, and would be extremely effective in guiding noise aware physical design optimizations.[21].

Using transmission line modelling along with step response and Nyquist stability diagrams, it had been shown that due to the existence of coupled capacitive and mutual-inductive coupling between two lines in crosstalk effect modeling, the near-end output is more stable than the single line output and the far-end output is less stable. Therefore, both coupled crosstalks affect the output stability.In the far-end output, the maximum overshoot increases and it is less stable. This is because by increasing the length, the maximum overshoot and switching delay of the far-end output increase. Also, increasing the width gives rise to the number of conducting channels and conductivity and decreases the switching delay.[26]

Daniele Rossi et al. [28] proposed an RLC equivalent model for CNT bus architecture. The effects of crosstalk on performance are evaluated by simulaton. The result showed that the proposed CNT bus arrangement improves the circuit performance.

S.N. Pu, W.Y. Yin, J.F. Mao and Q. H. Liu et.al [29] investigated the crosstalk effects in single- and double-walled carbon-nanotube (SWCNT and DWCNT) bundle-interconnect architectures. Some modified equivalent-circuit models were proposed for both SWCNT and DWCNT bundles. These circuit models are further used to predict the performance of SWCNT and DWCNT bundle interconnects in comparison with that of the Cu wire counterpart.

D Das and H Rahman [30] developed an equivalent circuit model to perform the crosstalk analysis. The impact of crosstalk on gate oxide reliability in terms of failure-

in-time (FIT) rate was calculated and comparisons were made with copper interconnect. The results showes that the CNT based interconnects are more suitable in VLSI circuits as far as the gate oxide reliability is concerned.

Abinash Roy et al.[31] analyzed the effect of capacitive and inductive coupling on interconnect delay and clock skew was analyzed in. The result showed that capacitive coupling and mutual inductance have opposite impact on interconnect delay.

A B Khang aet al [32] developed delay model for coupled RC lines and this model was applied along with SPICE simulation to perform various studied related to interconnect delay. It was concluded that delay uncertainty on victim is high for global interconnect as compared to local interconnect.

D K Sharma et al [33] presented the effect of coupling parasitics such as capacitive coupling and mutual inductance on propagation delay and peak overshoot for lox K-dielectric material. The effect of these parasitics was captured by SPICE simulation result. It was observed that capacitive coupling and mutual inductance have opposite impact on interconnect delay.

2.1.5.2 Temperature Dependent

Crosstalk is an undesirable voltage glitch degrading the performance of interconnects. It occurs due to transition in one or more adjacent interconnects [34]. The crosstalk can be categorized as functional and dynamic crosstalk. In functional crosstalk noise, a victim line experiences a voltage spike due to switching of the aggressor line, itself being fixed. The dynamic crosstalk occurs for synchronous switching. Further when both the lines switch in the same direction, the even more dynamic crosstalk occurs and when they switch in the opposite direction, they cause odd mode dynamic crosstalk [20,21]. All the works reported to date have analyzed and evaluated the temperature dependent crosstalk induced noise voltage in CNTs.

M.K.Rai and S. Sarkar et al.[35] presented the temperature-dependent, crosstalk-induced, noise voltage waveform and its frequency spectrum, in capacitive coupled single-walled carbon nanotube (SWCNT) bundle interconnects, at the far end of victim line at 22-nm technology node. It was revealed that, with rise in interconnect temperatures coupled interconnects of SWCNT bundle filter more noise frequency components compared with copper interconnects. Based on these comparative results,

an improved model has been proposed for extracting inter-bundle, real life, coupling capacitances between SWCNT bundles.

A. Hosseini and V.Shabro et al.[36] demonstrated an accurate thermally-aware model for single-walled carbon-nanotube (SWCNT) based interconnects which is an integration of temperature-dependent electrical parasitic model and thermal equivalent circuit that captures both self-heating and heat conduction phenomena. Based on the simulation results, it was found that SWCNT-based interconnects offer more than 5reduction in delay at dimensions of about 10–20 nm for 27– 127 C temperature range.

Very less work has been done on the temperature dependent crosstalk in MLGNRs. M.K. Rai et.al [37] studied the effect of temperature variations on the delay, power dissipation and crosstalk –induced voltage noise waveform at the far end of the victim line of capacitively coupled MLGNR interconnects for the temperature ranging from 300 to 500 K in comparison to copper was examined. It was demonstrated that MLGNR has better performance as compared to copper.

2.1.6 Scaling Of Parameters

It is necessary to present a comprehensive thermal scaling analysis of multilevel interconnects in deep nanometer scale technologies. These results are helpful in enhancing backend thermal management, performance, reliability and for incorporating thermal awareness in interconnect design issues [40].Various researchers have studied the temperature-independent effect of scaling in Cu interconnects.

Various researchers investigated the EM reliability of Cu and Cu (Mn) interconnects, focusing on the scaling effect on grain structure and mass transport. The microstructure of Cu and Cu(Mn) interconnects was characterized up to the 22 nm node using a high-resolution TEM diffraction technique. [44].

A comprehensive thermal scaling analysis of multilevel interconnects in deep nanometre scale CMOS technologies was studied. Three-dimensional electro thermal finite element methods, combined with accurate calculations of temperature- and size-dependent Cu resistivity and thermal conductivity of low- interlayer dielectrics (ILD) have been performed It is demonstrated that even after considering densely embedded

vies, the interconnect temperature is expected to increase. Significantly with scaling, due to increasing current density, increasing surface and grain boundary contributions to metal resistivity, and decreasing ILD thermal conductivity. [45]

S. Sarkar et.al [15] presented the effects of scaling the interconnect dimensions for the capacitively coupled CNT model and found that capacitive coupling provided better reduction in crosstalk noise but no work has been reported on the scaling effect on the interconnect dimensions using the temperature dependent model of the MLGNR interconnect. This paper presents the effect of scaling the interconnect dimensions on the crosstalk noise voltage using the capacitively coupled temperature dependent model. The induced noise peaks and time duration of the crosstalk noise voltage for the different scaling conditions are then plotted against temperature. The results are further compared with copper. This paper also analyses the effect of interconnect length on the crosstalk induced voltage noise for the temperature dependent and temperature independent circuit models. The temperature dependent circuit models for different scaling conditions are analyzed with respect to interconnect length.

2.3 CONCLUSION

The basic introduction of the MLGNRs is presented in this chapter. In this chapter, it is observed that MLGNRs are more favorable at deep submicron level because of their distinct properties and have tendency to fight with Electromigration and scattering effects. MLGNRs possess a way more better performance than copper when used as interconnects at nanotechnology. MLGNRs are preferred to reduce the overall resistance of wire which in turn reduce the delay of interconnect and increases the performance. Researchers have worked on different fields related to interconnects. Recent research shows the impact of tube parameters on performance of MLGNR interconnects. Some of the scientists have explained the performance analysis on the basis of delay and power dissipation of interconnects at deep submicron level. A few researchers have investigated the performance of MLGNRs within integrated circuit from a thermal point of view. As all the integrated circuit works above the room temperature it is necessary to study the effect of temperature on the performance of MLGNR bundle interconnects.

CHAPTER-3

TEMPERATURE DEPENDENT CIRCUIT MODELING AND IMPEDANCE ANALYSIS OF MLGNR

3.1 INTRODUCTION

In this chapter, temperature-dependent parameters of the MLGNR interconnect are calculated using the evaluated equations. Then these parameters i.e. R,L and C are plotted against temperature.

3.2 Temperature Dependent Modeling of MLGNR

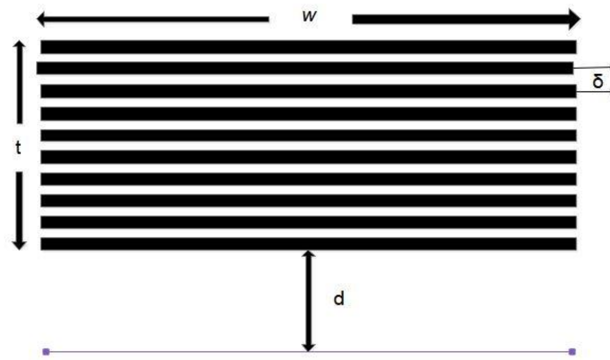


Figure 3.1: Schematic of an MLGNR [16].

The MLGNR interconnect cross sectional schematic is shown in Fig.15.The MLGNR interconnect is formed of N layers of SLGNR stacked over one- another. In an N-layer GNR interconnect, the MLGNR can be classified as top-contact and side-contact MLGNRs depending upon the type of contacts. Top contact MLGNRs (TC-MLGNRs) have only the topmost layer coupled with contacts however, in the case of side-contact MLGNRs (SC-MLGNRs), all the layers are physically connected to contacts. The equivalent resistance of side-contact MLGNRs (SC-MLGNRs) is found to be lesser than that of top-contact MLGNR (TC-MLGNRs) [16] because of the lower interlayer resistance per unit interconnect length. Hence, side-contact MLGNRs (SC-MLGNRs) stand better performance characteristics. In the present study, MLGNR is assumed to be side-contact MLGNR (SC-MLGNR) [16]. The GNR interconnect has width *w*, thickness *t* and height above the ground *h*. The

interlayer distance δ is kept as 0.35 nm. An equivalent RLC circuit is shown in Fig.2.The total temperature dependent resistance of a single GNR layer can be formulated as [12]:

$$R_{layer} = \frac{R_q l_{GNR}}{\lambda_e} = \frac{h/2e^2}{N_{ch}\lambda_e} = \frac{12.9}{N_{ch}\lambda_e} \quad (16),$$

here, λ_e denotes the mean free path , h is the planck's constant N_{ch} is the conducting channels number in a layer and e is the electronic charge.

$$R_q = \frac{h/2e^2}{N_{ch}} = \frac{12.9}{N_{ch}} \quad (17),$$

N_{ch} is given by

$$N_{ch} = \sum_{i=1}^{n_c} [e^{(E_i - E_F)/kT} + 1]^{-1} + \sum_{j=1}^{n_v} [e^{(E_i + E_F)/kT} + 1]^{-1} \quad (18),$$

here, i =1,2,3….is the positive number, n_c is the count of conduction sub bands and n_v is the count of valence sub bands. The number of sub bands in the case of zz-GNR is given by $n_c = \frac{2w}{\sqrt{3}a}$ and $a = \sqrt{3}b$, where b is the interatomic distance. E_F represents the fermi energy and E_i is the minimum energy of the ith conduction sub band and is computed by[12]:

$$E_i = \frac{h v_F}{2w}\left[\frac{1}{2} + |i|\right], i \neq 0 \quad (19),$$

An additional scattering resistance occurs if the length of the GNR is larger than that of the MFP. The scattering resistance as a function of temperature is calculated by:

$$R_s = \frac{h}{2e^2 N_{ch}} \frac{1}{\lambda_e(T)} = \frac{12.9}{N_{ch}\lambda_e(T)} k\Omega \quad (20),$$

where the MFP in GNR is further determined by:

$$\frac{1}{\lambda_e(T)} = \frac{1}{\lambda^{AC}} + \frac{1}{\lambda^{op}_{abs}} + \frac{1}{\lambda^{opp}_{em}} \quad (21),$$

λ^{AC} is caused by acoustic phonon scattering, λ_{abs}^{op} is caused by non-polar optical phonon (absorption) and λ_{em}^{op} is caused by scattering of non-polar optical phonon(emission). λ^{AC} Is given by:

$$\lambda^{AC} = \frac{4\rho_m \left(\frac{h}{2\pi} v_F v_s \right)^2}{\sqrt{\pi} N_s D_{AC}^2 kT} \quad (22),$$

ρ_m denotes the mass density of graphene i.e. 7.6×10^{-7}, v_F denotes Fermi velocity of electrons 8×10^5 *m/s*, v_s is the speed of acoustic phonons 20 *km/s*. Here, N_s is the concentration of 2-D electron gas in graphene ($=4\times10^{16}$ /m^2) and D_{AC} denotes the acoustic deformation potential (8eV).Mean Free Paths due to optical emission and optical absorption are negligible. For the case of the longer SC-MLGNRs, the total resistance can be given by:

$$R_{SC-MLGNR} = \frac{R_S}{n} = \frac{12.9}{nN_{ch}} \left(1 + \frac{1}{\lambda_e(T)} \right) \quad (23)$$

Here, n is the total number of layers in MLGNR and is given by:

$$n = 1 + round\left(\frac{t}{\delta} \right) \quad (24),$$

GNR has kinetic inductance (L_k) and magnetic inductance (L_m).In each conducting channel of the GNR, the kinetic inductance is expressed as[12]:

$$L_k = \frac{h/4e^2 v_F}{nN_{ch}} \cong \frac{8nH}{nN_{ch}} (um) \quad (25),$$

$$L_m = \frac{\mu_0 y}{w} \quad (26),$$

here, v_F denotes Fermi velocity and y is the height above ground.

The GNR capacitance consists of electrostatic capacitance (C_e) and quantum capacitance (C_q). The of electrostatic capacitance (C_e) and quantum capacitance (C_q) is expressed as[18]:

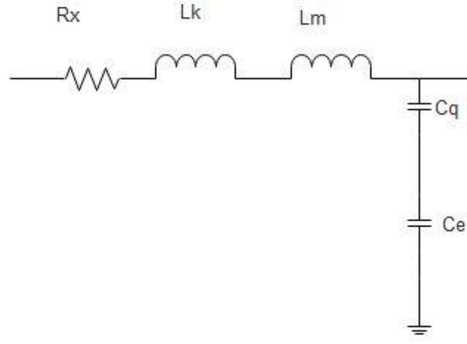


Figure 3.2:An equivalent RLC model of MLGNR interconnect [16].

$$C_q = \frac{4e^2 nN_{ch}}{hv_F}$$

$$C_e = \varepsilon M\left[\tanh\left(\frac{\pi w}{4y}\right)\right] \quad (27),$$

The electrostatic capacitance (C_e) is calculated by:

$$M(a) = \begin{cases} \dfrac{2\pi}{\ln\dfrac{2.\left(1+\sqrt[4]{1-a^2}\right)}{\left(1-\sqrt[4]{1-a^2}\right)}}, 0 \le a < \dfrac{1}{\sqrt{2}} \\ \dfrac{2}{\pi}\ln\dfrac{2\left(1+\sqrt{a}\right)}{\left(1-\sqrt{a}\right)}, \dfrac{1}{\sqrt{2}} \le a \le 1 \end{cases} \quad (28),$$

here, ε denotes the permittivity of the medium and a represents the hyperbolic function tangent of function having distance *y* above the ground and of width *w*.

$$\begin{aligned} R &= R_N \\ L &= L_K + L_M \approx L_K \\ C &= (C_Q^{-1} + C_Q^{-1})^{-1} \end{aligned} \quad (29)$$

3.2.2 RLC Computation of MLGNR interconnects

The impedance analysis of the temperature-dependent capacitively coupled MLGNR based interconnect and copper based interconnect is presented at 14 nm technology

node. Using the matlab codes, resistance .inductance and capacitance values were calculated at different lengths i.e.0.2mm, 0.4mm, 0.6mm, 0.8mm and 1mm

3.2.2.1 Resistance values at variable temperature for different MLGNR lengths

Table 3.1: Resistance values for 0.2mm length.

Temperature(K)	Resistance(Kohm)
300	2.72
350	3.18
400	3.61
450	4.05
500	4.47

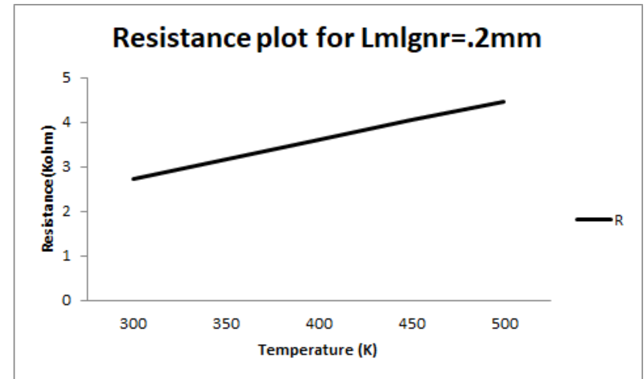


Figure 3.3(a): Resistance plot for L_{MLGNR} 0.2mm.

Table 3.2:Resistance values for 0.4mm length.

Temperature(K)	Resistance(Kohm)
300	5.44
350	6.36
400	7.23
450	8.1
500	48.95

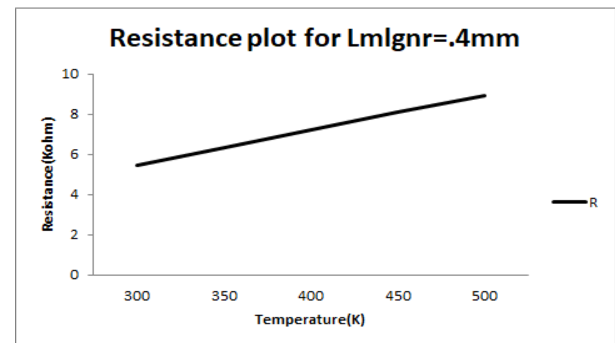


Figure 3.3(b): Resistance plot for L_{MLGNR} 0.4mm.

Table 3.3: Resistance values for 0.6mm length.

Temperature(K)	Resistance(Kohm)
300	10.88
350	12.72
400	14.46
450	16.2
500	17.91

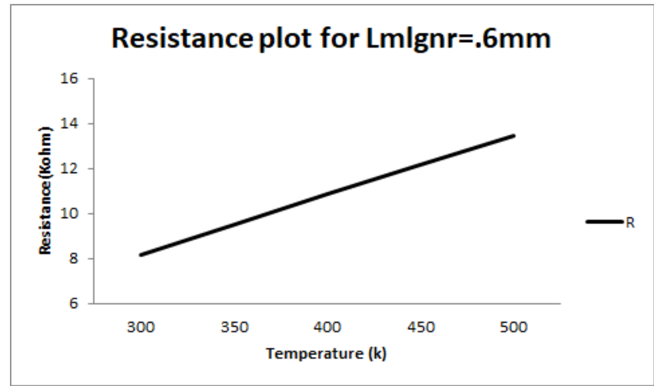


Figure 3.3(c): Resistance plot for L_{MLGNNR} =0.6mm.

Table 3.4: Resistance values for 0.8mm length.

Temperature(K)	Resistance(Kohm)
300	10.88
350	12.72
400	14.46
450	16.2
500	17.91

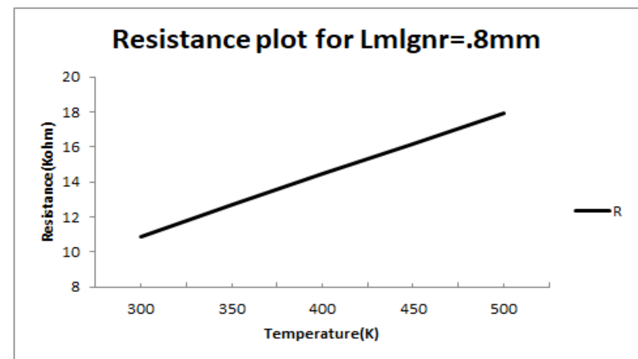


Figure 3.3(d): Resistance plot for L_{MLGNR} 0.8mm.

Table 3.5: Resistance values for 1mm length.

Temperature(K)	Resistance(Kohm)
300	13.6
350	15.9
400	18.08
450	20.25
500	22.39

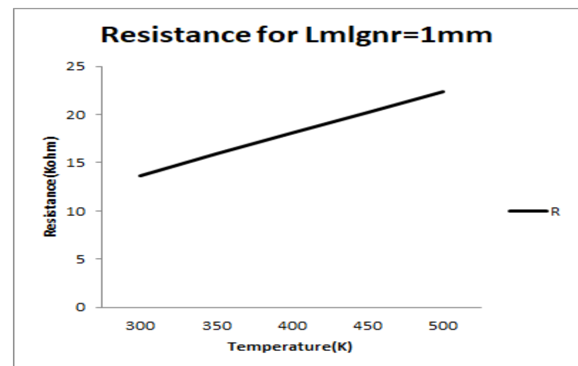


Figure 3.3(e): Resistance plot for Lmlgnr 1mm.

3.2.2.2 Inductance values at variable temperature for different MLGNR lengths

Table 3.6:.Inductance values for L_{MLGNR}=0.2mm.

Temperature(K)	Inductance(nH)
300	6.11
350	6.08
400	6.04
450	6.02
500	5.98

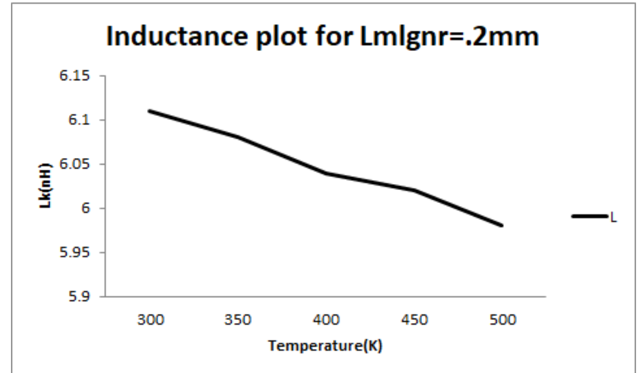


Figure 3.4(a): Inductance plot for L_{MLGNR}=0.2mm.

Table 3.7: Inductance values for L_{MLGNR}=0.4mm.

Temperature(K)	Inductance(nH)
300	12.2
350	12.16
400	12.08
450	12.04
500	11.96

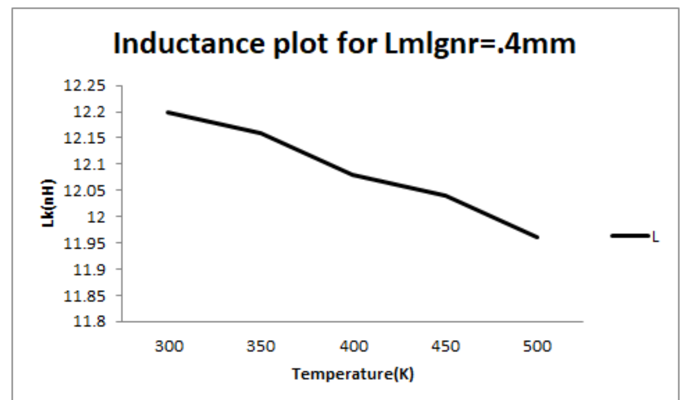


Figure 3.4(b): Inductance plot for $L_{MLGNR=}$0.4mm.

Table 3.8: Inductance values for L_{MLGNR}=0.6mm.

Temperature(K)	Inductance(nH)
300	24.4
350	24.32
400	24.16
450	24.08
500	23.92

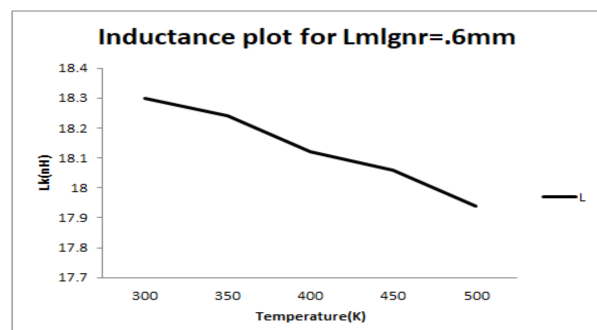


Figure 3.4(c): Inductance plot for L_{MLGNR}=0.6mm.

Table 3.9: Inductance values for L_{MLGNR}=0.8mm.

Temperature(K)	Inductance(nH)
300	18.3
350	18.24
400	18.12
450	18.06
500	17.94

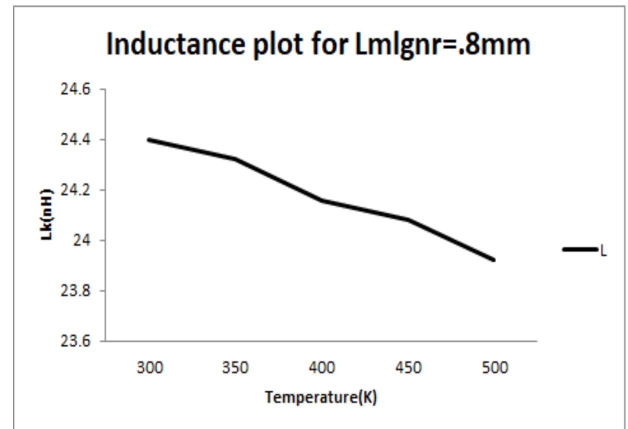


Figure 3.4(d): Inductance plot for L_{MLGNR}=0.8mm.

Table 3.10: Inductance values for L_{MLGNR}=1mm.

Temperature(K)	Inductance(nH)
300	30.5
350	30.4
400	30.2
450	30.1
500	29.9

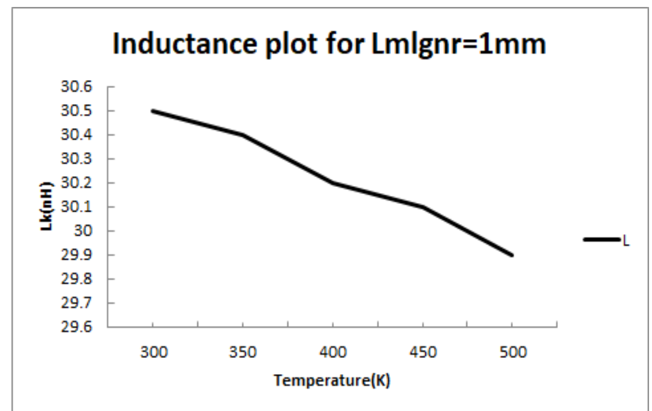


Figure 3.4(e): Inductance plot for L_{MLGNR}=1mm.

3.2.1.3 Capacitance values at variable temperature for different MLGNR lengths

Table 3.11: Capacitance values for L_{MLGNR} =0.2mm.

Temperature(K)	Capacitance(fF)
300	0.00979
350	0.00979
400	0.00979
450	0.00979
500	0.00979

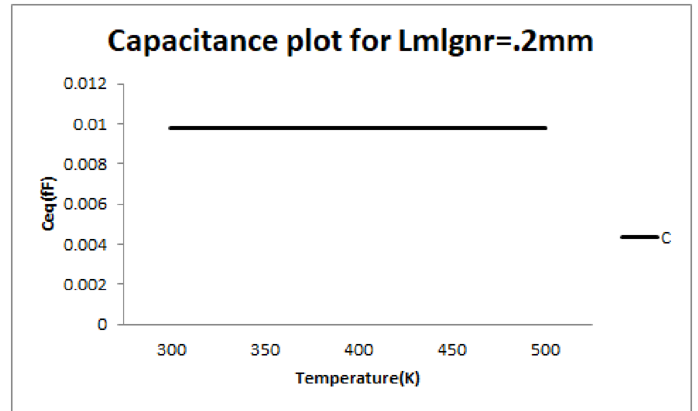


Figure 3.5(a): Capacitance plot for L_{MLGNR}=0.2.

Table 3.12: Capacitance values for L_{MLGNR} =0.4mm.

Temperature(K)	Capacitance(fF)
300	0.01958
350	0.01958
400	0.01958
450	0.01958
500	0.01958

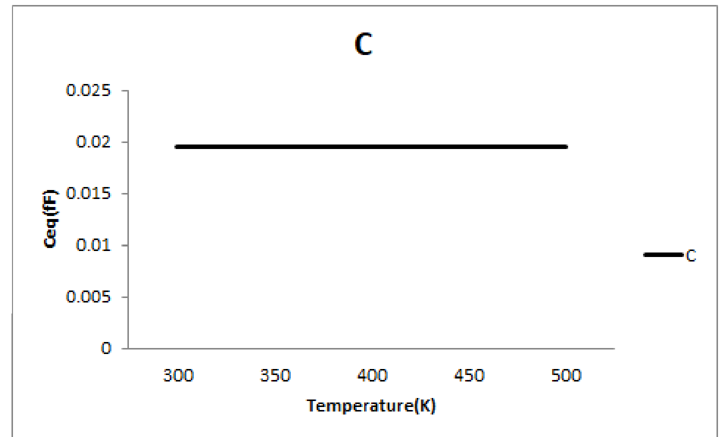


Figure 3.5(b): Capacitance plot for L_{MLGNR}=0.4mm.

Table 3.13: Capacitance values for L_{MLGNR} 0.6mm.

Temperature(K)	Capacitance(fF)
300	0.0293
350	0.0293
400	0.0293
450	0.0293
500	0.0293

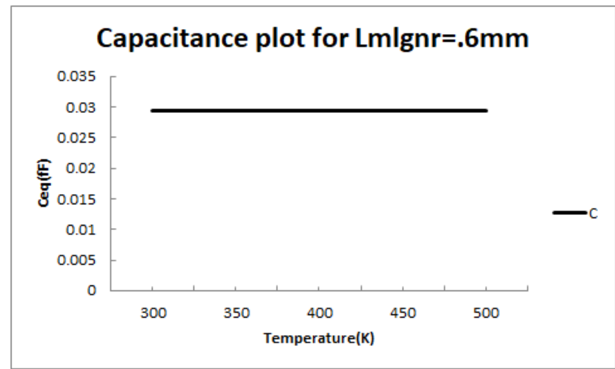


Figure 3.5 (c): Capacitance plot for L_{MLGNR}=0.6mm.

Table 3.14: Capacitance value s for L_{MLGNR} = 0.8mm.

Temperature(K)	Capacitance(fF)
300	0.03916
350	0.03916
400	0.03916
450	0.03916
500	0.03916

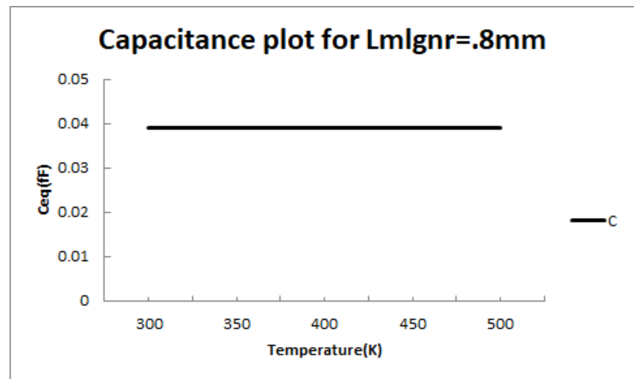


Figure 3.5(d): Capacitance plot for L_{MLGNR}=0.8mm.

Table 3.15: Capacitance values for L_{MLGNR} =1mm.

Temperature(K)	Capacitance(fF)
300	0.04895
350	0.04895
400	0.04895
450	0.04895
500	0.04895

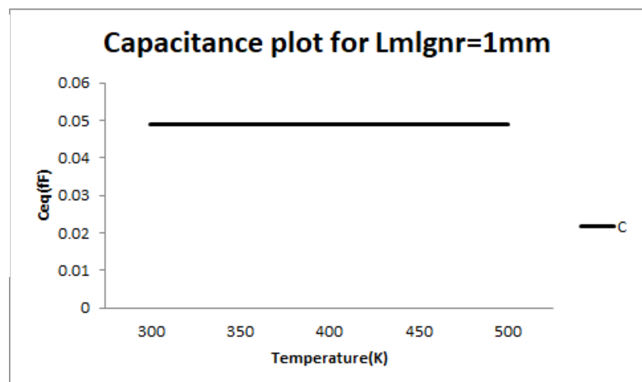


Figure 3.5(e): Capacitance plot for L_{MLGNR}=1 mm.

The results show [Fig.3.4 -3.6] that as the temperature is varied from 300 K to 500 K. the resistance rises with the temperature. This behaviour is observed at different MLGNR lengths .In terms of inductance, the value decreases with the increase in temperature.The inductance values are obtained in nano Henry for different MLGNR lengths.For capacitance, there is a very low change in values.It remains almost constant in terms of femto Farads.The expressions obtained are from ref.18.

3.3 IMPEDANCE PARAMETERS OF COPPER

The impedance parameters of copper can be computed from the following expressions as [15][18] :

$$R = \frac{\rho L}{wt} \tag{30}$$

$$R(T) = R_0\left[1+\alpha\left(T-T_0\right)\right] \tag{31}$$

where $$R_0 = \frac{\rho l}{w_0 t} \tag{32}$$

$$L_s = \frac{\mu_0 l}{2\pi}\left[\ln\frac{2l}{w+t}+0.5+\frac{0.22(w+t)}{l}\right] \tag{33}$$

$$C_g = \varepsilon\left[\begin{array}{l}\frac{w}{d}+2.22\left(\frac{s}{s+0.7d}\right)^{3.19} \\ +1.17\left(\frac{s}{s+1.15d}\right)^{0.76}\left(\frac{s}{H+4.53d}\right)^{0.12}\end{array}\right] \tag{34}$$

$$C_c = \varepsilon\left[\begin{array}{l}1.14\frac{t}{s}\left(\frac{d}{d+2.06s}\right)^{0.09}+ \\ 0.74\left(\frac{w}{w+1.59s}\right)^{1.14}+ \\ 1.16\left(\frac{w}{w+1.87s}\right)^{0.16}\left(\frac{d}{d+0.98s}\right)^{1.18}\end{array}\right] \tag{35}$$

where, C_g is the ground capacitance, C_c is the coupling capacitance, *R(T)* is the resistance, L_s is the self inductance, l is the interconnect length, w is the interconnect width, t is the interconnect thickness, d is the height above the

ground, s is the spacing between the interconnects, μ_0 is the permeability and ε is the dielectric constant.

3.4 CONCLUSION

Impedance parameters of MLGNR are critically analysed and are compared with copper interconnects. The effect of temperature on impedance parameters is also analysed. The resistance and inductance values increase with temperature however the capacitance values almost remain constant.

CHAPTER-4

EFFECT OF SCALING ON TEMPERATURE DEPENDENT CROSSTALK ANALYSIS

4.1 INTRODUCTION

This chapter explains the effect of scaling on the temperature-dependent crosstalk in capacitively coupled MLGNR interconnects. In deep nanometer scale technologies, it is necessary to analyze the thermal scaling of multilevel interconnects. . These results are helpful in augmenting the reliability, performance, for generating thermal awareness in interconnect design issues and for backend thermal management [22].Various researchers have studied the temperature-independent effect of scaling in Cu interconnects [22-25]. S.Sarkar et.al [15] presented the effects of scaling the interconnect dimensions for the capacitively coupled CNT model and found that capacitive coupling provided better reduction in crosstalk noise but no work has been reported on the scaling effect on the interconnect dimensions using the temperature dependent model of the MLGNR interconnect. In this paper, the impact of interconnect dimension scaling on the crosstalk noise voltage using the capacitively coupled temperature dependent model was studied. The induced noise peaks and time duration of the crosstalk noise voltage for the different scaling conditions are then plotted against temperature. The results are further compared with copper. The effect of interconnect length on the crosstalk induced voltage noise for the temperature dependent and temperature independent circuit models has also been analyzed. The temperature dependent circuit models are found to have significant improvement in the time-duration as compared to the temperature-independent MLGNR interconnect.

4.2 SCALING

The impedance analysis of the temperature-dependent capacitively coupled MLGNR based interconnect and copper based interconnect is presented at 14 nm technology node.The interconnect dimensions control the impedance parameters of the interconnect models [12].Table 4.1 is used for the calculations. In this case, the effect of the scaling and the width on the temperature-dependent R, L and C parameters is discussed.The space between the two interconnects and width of the interconnect can be formed into three cases:

Case 1: Space (s) between the two interconnects is equal to s=w is 18nm and width (w) is 18 nm.

Case 2: Space (s) between the two interconnects is equal to $s+w/2=3w/2=$ 27 nm and width (w) is s-w/2=$w/2$ with value 9 nm.

Case 3: Space (s) between the two interconnects is equal to s-w/2=$w/2=$ 9 nm and width (w) is $s+w/2=3w/2$ with value 27 nm.

Cc (Coupling capacitance) of MLGNR is assumed to be same as that of copper based interconnect with same dimension and it is calculated by equation 19. [12]

Table 4.1.Simulation parameters [18].

Technology node	14nm
Width of the global interconnect(w)	18nm
Separation between adjacent interconnects(δ)	.35nm
Thickness of interconnect *(t)*	42nm
ε_r	1.75

Under, the three different cases, temperature dependent line parasitics are extracted. The computed values of temperature dependent resistance, inductance and capacitance under the three different cases for temperature dependent and temperature independent models varying length from 0.2mm to 1mm are represented in Tables 4.2 to 4.6 using the equations 23 to 29. We find that temperature-independent resistance and capacitance is higher than that of temperature independent resistance and capacitance respectively. However, temperature-independent inductance is lower than that of temperature-dependent inductance.

In Figs.4.1, 4.2 and 4.3, the resistance, Inductance and capacitance values are plotted against temperature for the three cases. From the Figs.21, 22 and 23, it can be noted that with respect to temperature resistance increases, inductance decreases and capacitance remains almost constant. It is also observed that with increased spacing and decreased width, the resistance and inductance values increase. On contrary, capacitance presents an opposite behavior. The capacitance values decrease with increased spacing and decreased width [1].

Table 4.2:R,L and C values for temperature dependent and temperature independent models for varied scaling cases at l=1mm.

l=1mm	case 1	case 2	case 3
Cc	43.99fF	25.92fF	98.34fF
R=f(T)	13.6kohm	28.9kohm	8.18kohm
R≠f(T)	44.2kohm	88.2kohm	29.61kohm
L=f(T)	30.5nH	62.9nH	18.26nH
L≠f(T)	16.5nH	33.05nH	11.01nH
C=f(T)	4.8fF	3.674fF	6.02fF
C≠f(T)	8.02fF	4.2fF	11.68fF

Table 4.3:R,L and C values for temperature dependent and temperature independent models for varied scaling cases at l=0.8mm.

L=0.8mm	case 1	case 2	case 3
Cc	43.99fF	25.92fF	98.34fF
R=f(T)	10.88Kohm	22.5Kohm	6.54Kohm
R≠f(T)	32.36Kohm	70.56Kohm	23.68Kohm
L=f(T)	24.4nH	50.32nH	14.6nH
L≠f(T)	13.2nH	26.44nH	8.8nH
C=f(T)	3.916fF	2.93fF	4.816fF
C≠f(T)	7.55fF	3.36ff	9.34fF

Table 4.4:R,L and C values for temperature dependent and temperature independent models for varied scaling cases at l= 0.6mm.

L=0.6mm	case 1	case 2	case 3
Cc	43.99fF	25.92fF	98.34fF
R=f(T)	8.16Kohm	16.91Kohm	4.9Kohm
R≠f(T)	26.52Kohm	52.92Kohm	17.76Kohm
L=f(T)	18.3nH	37.74nH	10.95nH
L≠f(T)	9.9nH	19.83nH	6.6nH
C=f(T)	2.93fF	2.1fF	2.408fF
C≠f(T)	5.74fF	2.4fF	7.00fF

Table 4.5:R,L and C values for temperature dependent and temperature independent models for varied scaling cases at l=0.4mm.

L=0.4mm	case 1	case 2	case 3
Cc	43.99fF	25.92fF	98.34fF
R=f(T)	5.44Kohm	11.27Kohm	3.27Kohm
R≠f(T)	17.68Kohm	35.28Kohm	11.84Kohm
L=f(T)	12.2nH	25.16nH	7.304nH
L≠f(T)	6.6nH	13.22nH	4.04hH
C=f(T)	1.958fF	1.457fF	2.406fF
C≠f(T)	3.65fF	1.69fF	4.6fF

Table 4.6:R,L and C values for temperature dependent and temperature independent models for varied scaling cases at l=0.2mm.

L=0.2mm	case 1	case 2	case 3
Cc	43.99fF	25.92fF	98.34fF
R=f(T)	2.72Kohm	5.63Kohm	1.63Kohm
R≠f(T)	8.84Kohm	17.64Kohm	5.9Kohm
L=f(T)	6.21nH	12.58nH	3.65nH
L≠f(T)	3.3nH	6.61nH	2.2nH
C=f(T)	0.979fF	0.734fF	1.19fF
C≠f(T)	1.89fF	0.8fF	2.3fF

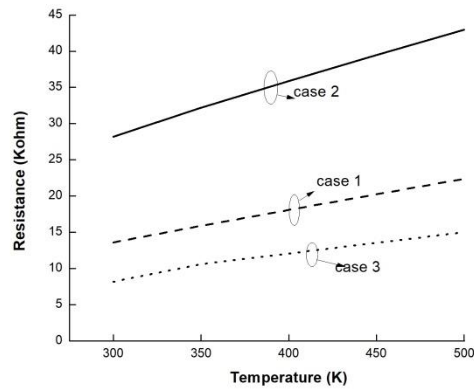


Figure 4.1: Resistance values at different temperature for varied scaling cases.

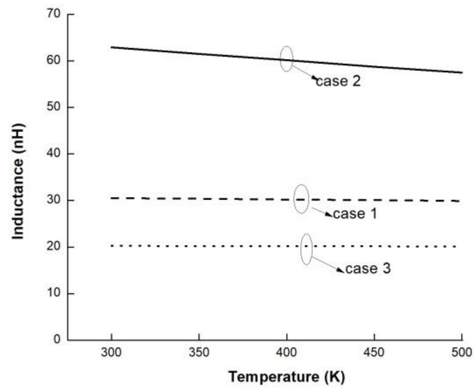


Figure 4.2: Inductance values at different temperature for varied scaling cases.

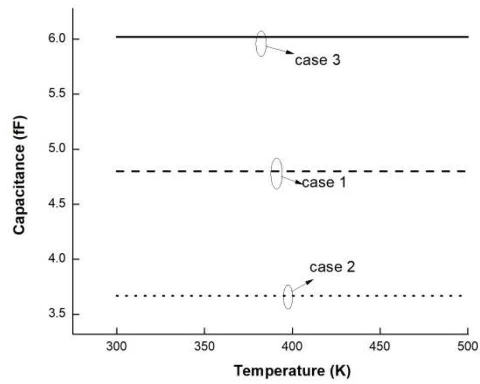


Figure 4.3: Capacitance values at different temperature for varied scaling cases.

4.3 CROSSTALK ANALYSIS IN MLGNR

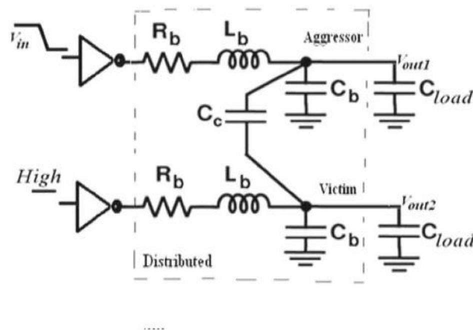


Figure 4.4: MLGNR interconnect model [12].

For the complete analysis, a capacitively coupled distributed RLC circuit has been considered as shown in Fig.4.4. A CMOS driver at 14nm technology node drives the distributed segment with a capacitive load (C_L) of 0.001fF. Table 1 is used for accurate calculations. The clock frequency is 0.2 GHz .The rise time and fall time is kept as 0.5 ns. For the complete analysis of the functional crosstalk, the aggressor transits from 0 to 1 or 1 to 0 while the victim line is kept fixed at 1 or 0.The analyzed results for the functional crosstalk are presented in Table 4.7, 4.8 and 4.9. It is observed that a significant delay is introduced at the far end of the aggressor line. However, the impact is more at the victim line. The near and the far ends of the victim line are significantly affected by the crosstalk leading to undershoot, overshoot and glitches. It is observed that the far end aggressor delay increases with increase in the spacing and decrease in the width.

Table 4.7: Functional Crosstalk for s=w.

S.No.	Aggressor Transition	Victim Transition	Aggressor far end delay(ns)	Victim			
				Near End		Far End	
				Result	Impact	Result	Impact
1	0 to 1	0	0.21	Overshoot with peak 16.03 mV	Reliability	Larger overshoot with peak 0.16 V	Reliab-ility
2	0 to 1	1	0.255	Positive glitches with peak 19.6 mV	Functio-nality	Larger positive glitches with peak 152.6 mV	Function-ality
3	1 to 0	0	0.215	Undershoot with 4 mV	Reliability	Larger Undershoot with 18 mV	Reliab-ility
4	1 to 0	1	0.3	Negative glitches with peak -23.81 mV	Function ality	Larger negative glitches with peak -191.04 mV	Function-ality

Table 4.8: Functional crosstalk for s=3w/2 and w=w/2.

S.No.	Aggressor Transition	Victim Transition	Aggressor far end delay	Victim			
				Near End		Far End	
				Result	Impact	Result	Impact
1	0 to 1	0	0.305	Overshoot with peak 16.3 mV	Reliability	Larger overshoot with peak 0.16 V	Reliability
2	0 to 1	1	0.32	Positive glitches with peak 19.95 mV	Functio-nality	Larger positive glitches with peak 150.55 mV	Function-ality
3	1 to 0	0	0.25	Undershoot with 2 mV	Reliability	Larger Undershoot with 166 mV	Reliabi-lity
4	1 to 0	1	0.275	Negative glitches with peak -2.11 mV	Functio-nality	Larger negative glitches with peak -16.80 mV	Function-ality

Table 4.9: Functional crosstalk for s=w/2 and w=3w/2.

S.No.	Aggressor Transition	Victim Transition	Aggressor far end delay	Victim			
				Near End		Far End	
				Result	Impact	Result	Impact
1	0 to 1	0	0.475	Overshoot with peak 20.83 mV	Reliab-ility	Larger overshoot with peak 0.16V	Reliab-ility
2	0 to 1	1	0.505	Positive glitches with peak 23.94 mV	Functio-nality	Larger positive glitches with peak 200.17 mV	Functio-nality
3	1 to 0	0	0.49	Undershoot with 26 Mv	Reliability	Larger Undershoot with 199 mV	Reliab-ility
4	1 to 0	1	0.475	Negative glitches with peak -2.63 mV	Functio-nality	Larger negative glitches with peak -203.92 mV	Functio-nality

This is due to the dominance of coupling capacitance. It has been analyzed that coupling capacitance increases with decrease in space and decreases with decrease in width of the adjacent interconnects [16]. The dynamic crosstalk analysis is discussed in the Tables 4.10, 4.11 and 4.12. Similar trend is observed in the far end of the aggressor line for the various spacing and width cases. The effect of dynamic crosstalk is observed in the terms of delay in rise time at the near end and far ends outputs of the victim line.

Table 4.10: Dynamic Crosstalk for s=w.

S.No.	Aggressor Transition	Victim Transition	Aggressor far end delay	Victim			
				Near End		Far End	
				Result	Impact	Result	Impact
1	0 to 1	1 to 0	0.45	Output with rise time 0.02ns	Timing	Output with rise time 0.5ns	Timing
2	1 to 0	0 to 1	0.48	Output with rise time 0.01ns	Timing	Output with rise time 0.51ns	Timing
3	1 to 0	1 to 0	0.035	Output with rise time 0.04ns	Timing	Output with rise time 0.05ns	Timing
4	0 to 1	0 to 1	0.035	Output with rise time 0.04ns	Timing	Output with rise time 0.05ns	Timing

Table 4.11: Dynamic Crosstalk for s=3w/2 and w=w/2.

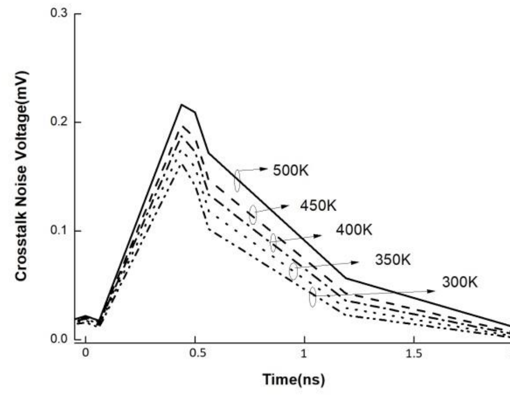
S.No.	Aggressor Transition	Victim Transition	Aggressor far end delay	Victim			
				Near End		Far End	
				Result	Impact	Result	Impact
1	0 to 1	1 to 0	0.52	Output with rise time 0.01ns	Timing	Output with rise time 0.4ns	Timing
2	1 to 0	0 to 1	0.53	Output with rise time 0.02ns	Timing	Output with rise time 0.42ns	Timing
3	1 to 0	1 to 0	0.04	Output with rise time 0.04ns	Timing	Output with rise time 0.04ns	Timing
4	0 to 1	0 to 1	0.04	Output with rise time 0.04ns	Timing	Output with rise time 0.04ns	Timing

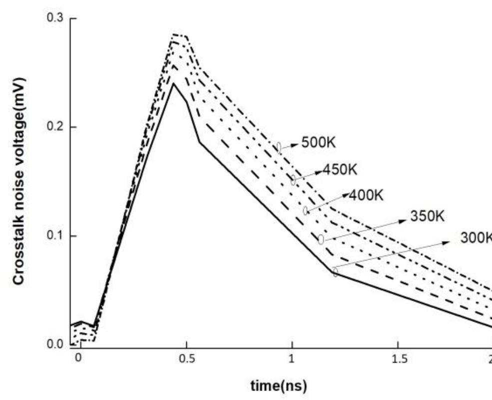
Table 4.12: Dynamic Crosstalk for s=w/2 and w=3w/2.

S.No.	Aggressor Transition	Victim Transition	Aggressor far end delay	Victim			
				Near End		Far End	
				Result	Impact	Result	Impact
1	0 to 1	1 to 0	0.52	Output with rise time 0.03ns	Timing	Output with rise time 0.63ns	Timing
2	1 to 0	0 to 1	0.53	Output with rise time 0.04ns	Timing	Output with rise time 0.64ns	Timing
3	1 to 0	1 to 0	0.04	Output with rise time 0.04ns	Timing	Output with rise time 0.04ns	Timing
4	0 to 1	0 to 1	0.04	Output with rise time 0.03ns	Timing	Output with rise time 0.03ns	Timing

The Fig.4.5, 4.6 and 4.7 illustrate the temperature dependent transient responses at the far end of the victim line under the three cases. The crosstalk noise voltage displays a linear increase with temperature. This is because of the dominant impact of the even time of flight. With the increase in the temperature, the even time of flight decrease causing a decrease in the delay. This decreased delay causes the crosstalk noise peaks to rise with the rise in temperature. It is demonstrated in equations 13, 14. Similar trend is observed in the three cases of interconnect dimensions. Comparing the crosstalk induced noise voltage of copper with MLGNR, it is observed that the coupled noise voltage levels are

more significant in the case of copper. This is attributed to the larger value of resistance and capacitance and smaller values of inductance in the case of copper.



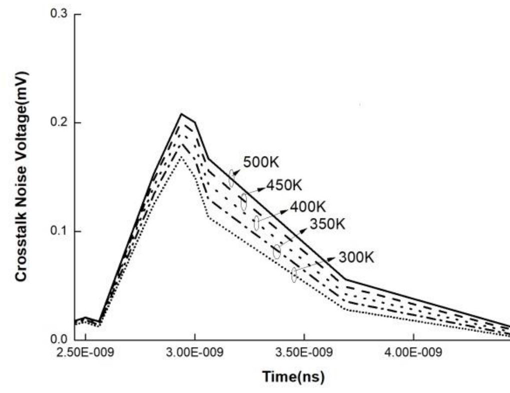


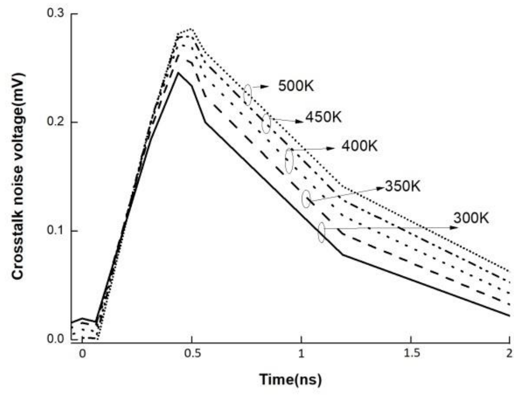
(a)

(b)

Figure 4.5: Crosstalk noise for s=w at temp 300 K

(a) MLGNR (b) Cu.





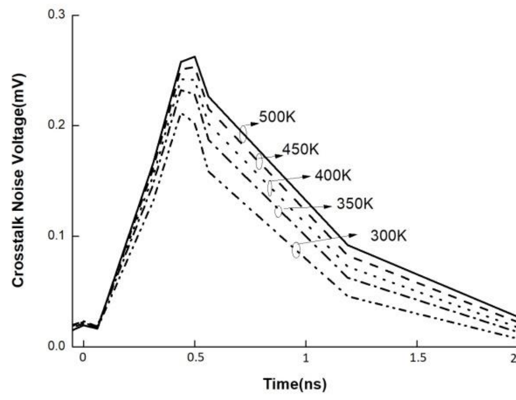
s

(a)

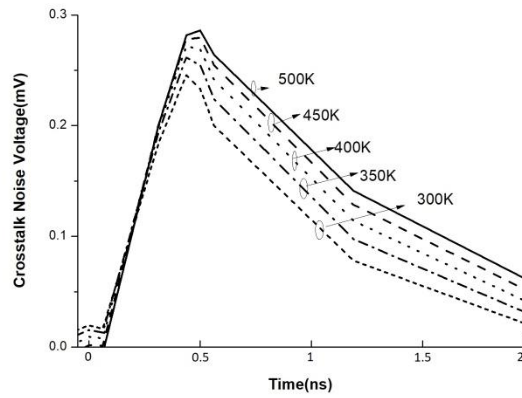
(b)

Figure 4.6: Crosstalk noise for s=3w/2 and w=w/2 at 300K

(a) MLGNR (b) Cu.



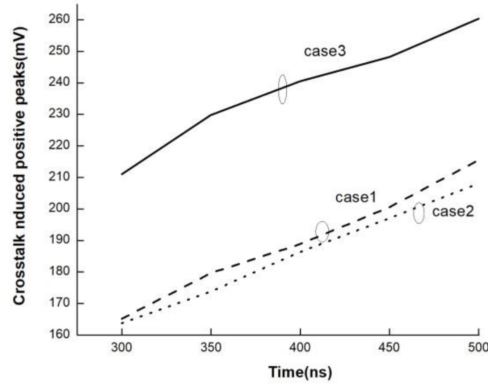
(a)



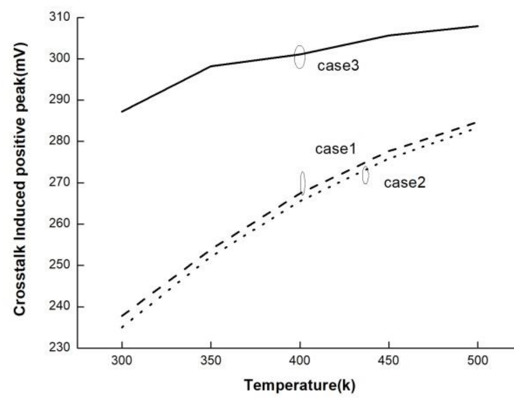
(b)

Figure 4.7: Crosstalk noise for s=w/2 and w=3w/2 at 300K

(a) MLGNR (b) Cu



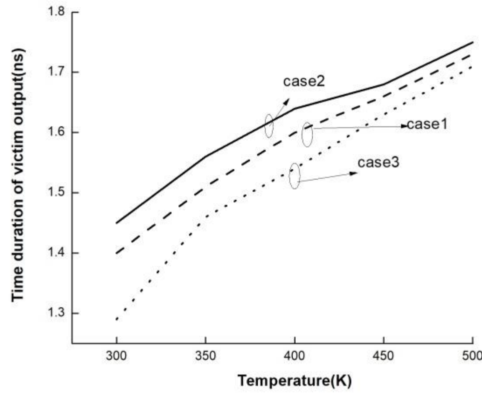
(a)



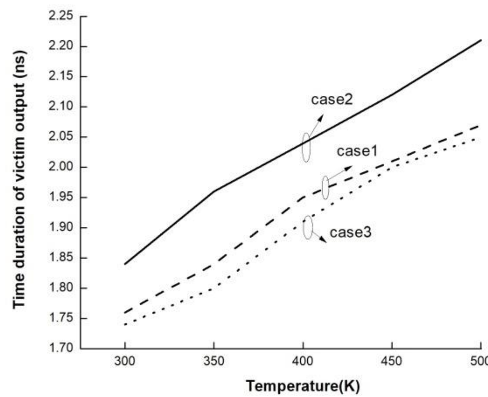
(b)

Figure 4.8: Crosstalk induced positive peaks with temperature for different scaling conditions (a) MLGNR (b)Cu.

In Fig.4.8, crosstalk induced positive peaks in the transient analysis are plotted against temperature shows that positively coupled peaks increase linearly with the increase in the temperature. Comparing the three cases, the highest peaks are obtained for case 3 as compared to case 1 and case 2. It demonstrates that as the spacing increases, the noise peak in terms of voltage reduces. As explained earlier, this is due to the fact that with increased spacing, coupling capacitance decreases and thus, we can conclude that crosstalk noise can be controlled by increasing the space. In addition, when compared to an MLGNR interconnect, copper-based interconnects have higher crosstalk induced noise peaks.



(a)



(b)

Figure 4.9: Time duration variation of victim output with temperature for different scaling conditions (a)MLGNR (b)Cu.

Fig. 4.9 illustrates the time duration of the victim output with respect to the temperature. The maximum time duration is obtained for case 2 as compared to case 1 and case 3.This is because of the dominant effect of the line resistance over inductance and capacitance [Table 4.2-4.6]. As the resistance increases, the noise peak widens and the time duration increases [12]. Further, in comparison to copper, MLGNR has a significant improvement in the time duration of the crosstalk induced peaks.

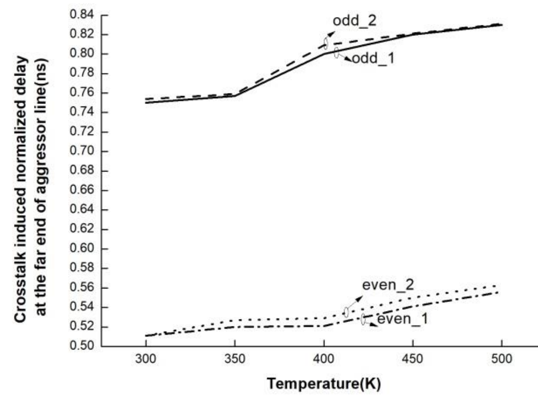


Figure 4.10: Normalized delay of aggressor line w.r.t temperature.

Fig.4.10 illustrates the normalized delay at the far end of the aggressor line w.r.t. temperature. The normalized delay is obtained by dividing the MLGNR aggressor delay to the copper aggressor delay at the near end of the aggressor line. It is observed that normalized delay is more in the case of odd mode dynamic crosstalk as compared to the even mode dynamic crosstalk. The even mode dynamic crosstalk when both the lines switch in the same direction, and when they switch in the opposite direction, they cause odd mode dynamic crosstalk.[12].

4.4 CONCLUSION

It was found that equivalent resistance and capacitance of temperature-dependent MLGNR interconnect is much lower than that of temperature-independent MLGNR interconnects, however equivalent inductance is higher than that of temperature-independent MLGNR interconnects The performance of the MLGNR interconnects are analysed in terms of scaling of parameters. The spacing and width between the adjacent MLGNR interconnects is scaled and the functional and dynamic crosstalk is studied for the three cases of scaling the width and spacing. It was found that Crosstalk induced peak decreases with spacing and time duration increases with spacing. The performance of MLGNR interconnect is compared with copper interconnect. The result reveals that performance of MLGNR is better than copper. Also it was found that temperature-dependent MLGNRs perform better

CHAPTER-5

A COMPARATIVE ANALYSIS BETWEEN RESULTS OBTAINED THROUGH TEMPERATURE-DEPENDENT AND TEMPERATURE -INDEPENDENT MODELS

5.1 INTRODUCTION

This chapter presents a comparative analysis between results obtained through temperature-dependent and temperature-independent models of MLGNR. The impact of interconnect length on the temperature-dependent and temperature-independent MLGNR performance and the arising crosstalk noise circuit modeling is discussed in this section.The values of resistance, inductance and capacitance for different scaling conditions under varying length are computed in Tables 4.2 to 4.6 .Thereby, a comparative analysis between temperature-dependent and temperature-independent model in terms of crosstalk induced peaks and time duration is presented.

5.2 ANALYSIS

The impact of interconnect length on the temperature-dependent and temperature-independent MLGNR performance and the arising crosstalk noise circuit modeling is discussed in this section. The values of resistance, inductance and capacitance for different scaling conditions under varying length are computed in Tables 4.2 to 4.6.Thereby, a comparative analysis between temperature-dependent and temperature-independent model in terms of crosstalk induced peaks and time duration is presented Fig.5.1 illustrates the crosstalk induced positive peaks at the far end of the victim line for temperature-dependent and temperature-independent models are plotted as a function of interconnect length. We conclude that, higher peaks are obtained in the case of temperature-independent model in comparison to temperature-dependent case. This is because of the lower capacitance values of the temperature-independent model. With decrease in capacitance, the characteristic impedance increases and causes a rise in the peak [Table 4.2-4.6].

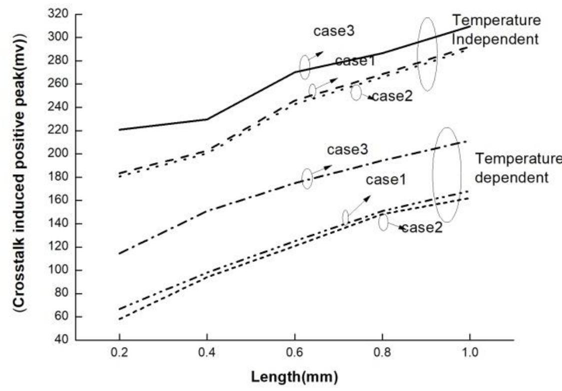


Figure 5.1: Crosstalk induced positive peaks for the different lengths at the far end of the victim line.

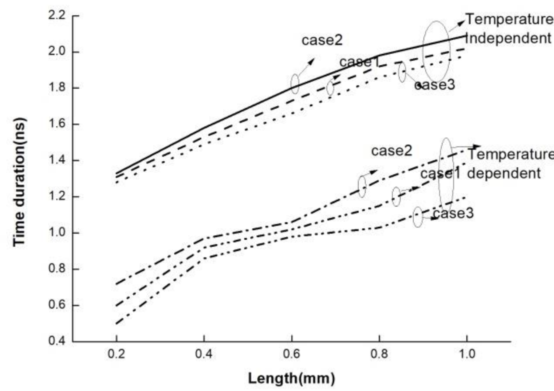


Figure 5.2: Time duration of victim output interconnect length.

In addition, for the temperature-dependent and temperature-independent cases, the maximum peak is obtained in case 3 as compared to case 1 and case 2. It can be attributed to the dominant effect of coupling capacitances. The coupling capacitance increases with decrease in space and decreases with decrease in width of adjacent interconnects. From Fig.5.2, we conclude that the time duration is more in the case of temperature-independent model as compared to temperature-dependent model. The increased resistance with respect to length compensates the increase in the time duration of the temperature-independent case as compared to temperature dependent case. Further, for the temperature-independent and temperature-dependent cases, case 2 has the maximum time duration as compared to case 1 and case 3.

Temperature-dependent MLGNR presents a significant improvement in the time duration with respect to temperature independent case as a function of the interconnect length. This can be examined from Table 5.1.There is approx. 39% improvement in time duration for case 1. For cases 2 and 3, the improvement figures are 35.6% and 46.6 % .It can be concluded that with increase in width and decrease in spacing, the improvement percentage increases.

Table 5.1: Time duration improvement.

Length(mm)	Time duration improvement with respect to temperature independent case		
	Case1	Case2	Case3
0.2	54	45	61
0.4	30	36	43
0.6	41	38	43
0.8	40	32	46
1	31	27	40
average	39	35.6	46.6

5.3 CONCLUSION

The performance of temperature-dependent MLGNR interconnect is compared with temperature-independent MLGNR interconnect with respect to interconnect length in the three scaling and width conditions. The result reveals that performance of temperature-dependent MLGNR is better than temperature-independent in terms of positively induced peaks and time duration

CHAPTER-6

CONCLUDING REMARKS AND FUTURE SCOPE

6.1 INTRODUCTION

There is a need to evolve new materials to implement electrical interconnects in conventional charge-based CMOS technologies. Graphene is such a new material offering rich physics and ample opportunities to implement it as an electrical interconnect. The most crucial feature is the the design of an optimal substrate to maximize the performance of graphene-based devices.There are numerous parameters affecting the performance of the interconnects. Interconnect dimensions, Fermi-energy shift, edge roughness, diffusion coefficient, mobility, conductance, crosstalk, electron mean free path (MFP), resistance per unit length etc. affect the performance of interconnects. Therefore GNRs suffer from challenges as well as they present ample opportunities to use them in the VLSI applications

In this research, the temperature dependent capacitively coupled RLC model of MLGNR is studied and analysed in terms in terms of crosstalk noise is at 14nm technology. The crosstalk noise at the far and near end of the victim and aggressor lines is studied. The impact of the different scaling on the spacing and width parameters in the crosstalk induced peaks and time duration of the crosstalk noise in the adjacent interconnects is examined. The results are compared with copper in terms of performance and crosstalk. Further, the impact of interconnect length on the crosstalk noise in temperature dependent and temperature independent models under the three different cases is discussed.

6.2 SUMMARY

The following conclusions are made:

1. Impedance parameters of MLGNR are critically analysed and are compared with copper interconnects. The effect of temperature on impedance parameters is also analysed. The effect of temperature on impedance parameters is also analysed. The resistance and inductance values increase and decrease with temperature however the capacitance values almost remain constant (Chapter 3).

2. It was found that equivalent resistance and capacitance of temperature-dependent MLGNR interconnect is much lower than that of temperature-independent MLGNR interconnects, however equivalent inductance is higher than that of temperature-independent MLGNR interconnects The performance of the MLGNR interconnects are analysed in terms of scaling of parameters. The spacing and width between the adjacent MLGNR interconnects is scaled and the functional and dynamic crosstalk is studied for the three cases of scaling the width and spacing. It was found that Crosstalk induced peak decreases with spacing and time duration increases with spacing.(Chapter 4).

3. The performance of MLGNR interconnect is compared with copper interconnect. The result reveals that performance of MLGNR is better than copper. Also it was found that temperature-dependent MLGNRs perform better (Chapter 4).

4. The performance of temperature-dependent MLGNR interconnect is compared with temperature-independent MLGNR interconnect with respect to interconnect length in the three scaling and width conditions. The result reveals that performance of temperature-dependent MLGNR is better than temperature-independent in terms of positively induced peaks and time duration (Chapter 5).

6.3 FUTURE SCOPE

The following are some of the future implementations that can be possibly made:

1. The performance of the interconnect can be compared by using analytical timing model.
2. Temperature dependent analysis can be done in MLGNR interconnects.
3. Performance can be examined in more advanced technologies.
4. Performance of GNR based devices and interconnects can be evaluated simultaneously.

REFERENCES

[1] S. Ghosh, I. Calizo, D. Teweldebrhan, E. P. Pokatilov, D. L. Nika, A. A. Balandin,W. Bao, F. Miao, and C. N. Lau, “Extremely high thermal conductivity of graphene: Prospects for thermal management applications in nanoelectronic circuits,” *Appl. Phys. Lett.*, vol. 92, no. 15, p. 151 911, Apr. 2008.

[2] A. A. Balandin, S. Ghosh, W. Bao, I. Calizo, D. Teweldebrhan, F. Miao, and C. N. Lau, “Superior thermal conductivity of single-layer graphene,” *Nano Lett.*, vol. 8, no. 3, pp. 902–907, Mar. 2008.

[3] A.Naeemi and J. D. Meindl, “Conductance modeling for graphene nanoribbon (GNR) interconnects”, *IEEE electron device letter*s, vol. 28, no. 5, pp. 428-431, 2007.

[4] S. H. Nasiri,M. K. M. Farshi, and R. Faez, “Stability analysis in graphene nanoribbon interconnects,” *IEEE Electron. Device Lett.*, vol. 31, no. 12, pp. 1458–1460, Dec. 2010.

[5] T. Ragheb and Y. Massoud, “On the modeling of resistance in graphene nanoribbon (GNR) for future interconnect applications”, *IEEE international conference on computer aided design*, 2008.

[6] C. Xu, H. Li and K. Banerjee, “Modeling, analysis, and design of graphene nanoribbon interconnects*”, IEEE transactions on electron devices*, vol. 56, no. 8, pp.1567-1578, 2009.

[7] Y. Fang, W. Zhao, Xu Wang, F. Jiang, and W. Y. Yin, “Circuit modelling of multilayer graphene nanoribbon (MLGNR) interconnects”, *Asia-Pacific Symposium On electromagnetic compatibility*, pp. 625-628, 2012.

[8] D.Das and H. Rahaman, “Analysis of crosstalk in single and multiwall carbon nanotube interconnects and its impact on gate oxide reliability”, *IEEE transactions on nanotechnology*,vol.10,no. 6,1362-1370,2011.

[9] L. Akbari and F. Rahim,“ Crosstalk stability analysis in multilayer graphene nanoribbon interconnects”, *Circuits, system and Signal Processing,* vol. 32, no. 6, pp. 2653–2666, 2013.

[10] K. I. Bolotin, K. J. Sikes, J. Hone, H. L. Stormer, and P. Kim, “Temperature dependent transport in suspended graphene,” *Phys. Rev. Lett.*, vol. 101, no. 9, p. 096 802, Aug. 2008.

[11] W. Zhao and W. Y. Yin, “Comparative study on multilayer graphene nanoribbon (MLGNR) interconnects*”, IEEE transactions on electromagnetic compatibility*, vol. 56, no. 3,pp. 638-645,2014.

[12] S. Rakheja, V. Kumar, and A. Naeemi, “Evaluation of the potential performance of graphene nanoribbons as on-chip interconnects”, *IEEE* , vol. 101, no. 7, pp.1740-1765, 2013.

[13] *Predictive Technology Model*, 2008, [Online]. Available: http://ptm.asu.edu/.

[14] Eric Pop, David A. Mann, Kenneth E. Goodson and Hongie Dai, “Electrical and thermal transport in metallic single-walled carbon Nanotubes on insulating substrates”, *Journal of Applied Physics* 101, no.9, pp. 093710(1-11),2005.

[15] M.K. Rai, R. Khanna, S. Sarkar, “Crosstalk Analysis in CNT Bundle Interconnects for VLSI Application”, *IEEJ Transactions On Electrical And Electronic Engineering,* pp.391-397, 2014.

[16] A.K. Nishad and R. Sharma, “Analytical time domain models for performance optimization of multilayer GNR interconnects”, *IEEE journals of selected topics in quantum electronics*,vol.20,no.1,2014.

[17] M.K.Rai, A.K. Chatterjee, S.Sarkar and B.K. Kaushik, “Performance analysis of multilayer grapheme nanoribbon (MLGNR) interconnects”, *Journal of computational electronics*,vol.15,no.2,358-366,2016.

[18] MK Rai, H Garg, BK Kaushik ,“ Temperature-Dependent Modeling and Crosstalk Analysis in Mixed Carbon Nanotube Bundle Interconnects”, *Journal of Electronic Materials*,pp. 5324-5337,2017.

[19] H. Li et al., ‘‘Carbon Nanomaterials for Next-Generation Interconnects and Passives:Physics, Status, and Prospects,’’ *IEEE Trans. Electron Devices*, vol. 56, no. 9, 2009, pp. 1799-1821.

[20] K. Agarwal, D. Sylvester, and D. Blaauw, “ Modeling and analysis of crosstalk noise in coupled RLC interconnects”, *IEEE transactions on computer-aided design of integrated circuits and systems*, vol. 25, no. 7,pp. 1273-1288, 2006.

[21] B.K. Kaushik and S.Sarkar, “Crosstalk analysis for a CMOS gate driven inductively and capacitively coupled interconnects”, *Journal on microelectronic*, vol. 39, no.12, pp.1834-1842, 2008.

[22] L.Jia and W.Y.Yin, “Temperature effects on crosstalk in carbon nanotube interconnects*”, IEEE Asia-Pacific Microwave Conference*,pp.1-4,2008

[23] M. Radosavljevi´c, J. Lefebvre, and A. T. Johnson, “High-field electrical transport and breakdown in bundles of single-wall carbon nanotubes,” *Phys. Rev. B, Condens. Matter*, vol. 64, no. 24, p. 241 307, Dec. 2001.

[24] Y. Massoud and A. Nieuwoudt, "Performance analyses of Optimized carbon nanotube interconnect," in *IEEE Symposium on Circuits and Systems*, Seattle, WA, 2008, pp. 792-795.

[25] A. Maffucci and et al., "A New Circuit Model for Carbon Nanotube Interconnects With Diamter-Dependent Paramters," *IEEE Transactions on Nanotechnology*, vol. 8, no. 3, pp. 345-354, December 2008.

[26] A. Naeemi, R Sarvari, and J. D. Meindl, "Performance comparison between carbon nanotube and copper interconnects for gigascale integration (GSI)," *Electron Device Letters*, vol. 26, no. 2, pp. 84-86, Feb 2005.

[27] M.K. Rai et al, “Control of SWCNT-interconnect Performance by Tube-diameter,” *TENCON IEEE Conference*, *pp.* 23-26, Jan. 2009.

[28] D.Rossi, J.M.Cazeaux, C.Metra and F.Lombardi, “Modeling crosstalk effects in CNT bus architectures”, *IEEE Transactions on Nanotechnology*, vol.6,no.2,2007.

[29] S.N.Pu, W.Y.Yin, J.F.Mao and Q.H.Liu, “Crosstalk prediction of single and double walled carbon nanotube (SWCNT/DWCNT) bundle interconnects”, *IEEE Transaction on electron devices*,vol.56,no. 4,pp.560-588,2009.

[30] D. Das and H. Rahaman, “Crosstalk and gate oxide reliability analysis in graphene nano ribbon interconnects”, *International Symposium on Electronic System Design*, 2008.

[31] A. Roy, N. Mahmoud and M. H. Chowdhury, “Effects of Coupling Capacitance and Inductance on Delay Uncertainty and Clock Skew” *Design Automation Conference*, pp. 184-187, June 2007.

[32] A. B. Kahng, Sudhakar Muddu and Devendra Vidhani, “Noise and Delay Uncertainty Studies for Coupled *RC* Interconnects”, Proc. on *twelfth Annual IEEE International ASIC/SOC Conference*, pp.3-8, 1999.

[33] D. K. Sharma, B.K.Kaushik, and R.K.Sharma, “Effect of Mutual Inductance and Coupling Capacitance on Propagation Delay and Peak Overshoot in Dynamically Switching Inputs*” ICETET 2010*, pp. 765-769, Nov.2010.

[34] N. Alam, A. K. Kureshi, Mohd. Hasan and T. Arslan (2009) “Analysis of carbon nanotube interconnects and their comparison with Cu interconnects,” *Multimedia, Signal Processing and Communication Technologies*., pp. 124-127, 2009.

[35] M.K.Rai and S. Sarkar , “Temperature dependent crosstalk analysis in coupled single walled carbon nanotube (SWCNT) bundle interconnects”, *International journal of circuit theory and applications*,2014.

[36] M.K.Rai, S. Arora and B.K. Kaushik, “Temperature dependent modeling and performance analysis of coupled MLGNR interconnects”, *International journal of circuit theory and applications*,2017.

[37] A.Hosseini , V.Shabro . ,“Thermally-aware modeling and performance evaluation for single-walled carbon nanotube-based interconnects for future high performance integrated circuits.” *Microelectronic Engineering* ,vol.87, no.10, pp.1955-1962, 2010.

[38] M.K. Rai, Nivedita and S. Sarkar, “Carbon Nanotube Based Interconnects for VLSI Application*,” IE (I) Journal-ET*, vol. 91, pp. 3-6, 2011.

[39] M. K. Rai and R. Khanna, "Control of tube prameters on SWCNT bundle interconnect dely and power dissipation," *Microelectronics International, Emerald*, vol. 31, no. 1, pp. 24-31, 2014.

[40] K. C. Saraswat and F. Mohammadi, “Effect of scaling of interconnections on the time delay of VLSI circuits,” *IEEE J. Solid-State Circuits*, vol. SC-17, pp. 275-280, Apr. 1982.

[41] S.Im; N. Srivastava; K. Banerjee; K. E. Goodson ,“Scaling analysis of multilevel interconnect temperatures for high-performance ICs*”, IEEE Transactions on Electron Devices*,vol.52,pp. 2710 – 2719,2005.

[42] M. H. Lin, K. P. Chang, K. C. Su and Tahui Wang ,“Effects of Width Scaling, Length Scaling, and Layout Variation on Electromigration in Dual Damascene Copper Interconnects”, *IEEE International Reliability Physics Symposium Proceedings* ,pp. 671 - 672,2006.

[43] Y.L.Cheng, B.J. Wei and Y.L. Wang ,“Scaling effect on electromigration in copper interconnects”, *16th IEEE International Symposium on the Physical and Failure Analysis of Integrated Circuits*, pp. 698 – 701,2009.

[44] L. Cao, L. Zhang, P. S. Ho, Patrick Justison and Meike Hauschildt ,“Scaling effects on microstructure and electromigration reliability for Cu and Cu(Mn) interconnects*”, IEEE International Reliability Physics Symposium*, pp. 5A.5.1 - 5A.5.5,2014.

[45] L. Spinella, M. Park, J. Im, P. Ho, Nobumichi Tamura and Tengfei Jiang ,“Effect of scaling copper through-silicon vias on stress and reliability for 3D interconnects”, IEEE International Interconnect Technology Conference/Advanced Metallization, pp. 80 - 82 Conference (IITC/AMC),2016.

[46] International Technology Roadmap for Semiconductors (ITRS) reports, 2006. [Online]. Available: http://www.itrs.net/reports.html.

[47] Kang, S.M. and Leblebici, Y., CMOS Digital Integrated Circuits, “Analysis and Design,”

[48] P. Kumar, A. Singh, A. Garg and R. Sharma, “Compact Models for Transient Analysis of Single-Layer Graphene Nanoribbon Interconnects.” *15th International Conference on Computer Modelling and Simulation (UKSim)*, pp. 809-814, April, 2013.

[49] M.K. Majumder , “Comparison of Propagation Delay in Single- and Multi-layer Graphene Nanoribbon Interconnects,” *5th international conference on computers and Devices for communication (CODEC)*, 2012.

[50] Online http://www.osa-opn.org/ home/ articles/ volume_20/ issue_6/ features/ green_silicon_photonics/ U5XCIPldXEQ.

[51] Y. Shin and H. O. Kim, "Analysis of Power Consumption in VLSI Global Interconnects," in *IEEE International Symposium on Circuits and Systems*, 2005, pp. 4713-4716.

[52] B. K. Kaushik and et al., "Effect of equal and mismatched signal transition time on power dissipation in global VLSI interconnects," *International Journal of VLSI design & Communication*, vol. 3, no. 4, pp. 111-119, 2012.

[53] D. Giancoli, "Electric Currents and Resistance," in *Physics for Scientists & Engineers with Modern Physics*, J. Phillips, Ed. New Jersy, US: Pearson New International Edition, 4th edition, 2013, ch. 25, p. 658.

[54] S. Frank and et al. (1998) [Online].
http://electra.physics.gatech.edu/group/labs/tubelab.html