Study and Analysis of 3C-SiC DIMOSFET with Gaussian Profile in the Drift Region for High Breakdown Voltage

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CERTIFICATE

This is to certify that the thesis entitled " **Study and Analysis of 3C-SiC DIMOSFET with Gaussian Profile in the Drift Region for High Breakdown Voltages**" which is being submitted by **Mr. Parag Parashar** (Roll No. 801061021) in partial fulfillment for the award of the degree of **Master of Engineering in Electronics & Communication Engineering from Thapar University, Patiala** is an authentic record of the student's own work carried out under my supervision and guidance. The matter presented in the thesis has not been submitted elsewhere in part or full to any other University or Institute for the award of any other degree.

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ABSTRACT

Silicon carbide (SiC) possesses electrical and mechanical properties that make it a very promising semiconductor superior to silicon for high environments and high power applications. SiC is a potential semiconductor for high temperature, high frequency and high power electronic devices due of its wide band gap, highly saturated electron velocity, high breakdown electric field and high thermal conductivity. The fact that wide band gap semiconductors are capable of electronic functionality at much higher temperatures than silicon has partially fuelled their development, particularly in the case of SiC. 3C-SiC is a potentially useful material for high temperature devices because of its refractory nature, high thermal conductivity, wide band gap (2.2eV) and high electron mobility comparable to that of Si. The present work aims at the design of 3C-SiC Double Implanted Metal Oxide Semiconductor Field Effect Transistor (DIMOSFET) with Gaussian function doping profile in drift region for high breakdown voltages. By varying the device height h, function constant m and peak concentration N_0, analysis has been done for an optimum profile for high breakdown voltage. With Gaussian profile peak concentration $N_0 = 10^{16}\ cm^{-3}$ at drain end and m as 1.496×10^{-2}cm, highest breakdown voltage of 6.84kV has been estimated with device height of 200μm. However, substantial deviation found to exist between the punch through and avalanche breakdown voltages for each of three Gaussian profile that have been used.

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CHAPTER 1
INTRODUCTION

Silicon Carbide is a wide energy gap semiconductor that possesses a combination of parameters that make it ideal for various applications in electronic industry. Its physical properties such as high electric field strength, high saturation drift velocity and high thermal conductivity has placed SiC at the centre of renewed focus of semiconductor material and device research amongst other wide energy gap semiconductors. SiC is an ideal semiconductor for high temperature, high frequency and high power electronic devices for its various properties. High thermal conductivity and breakdown electric field suggests that integration of the devices made from SiC is possible with higher package densities. The high breakdown fields in Silicon Carbide allow for drift regions that are eight to ten times thinner than Silicon high voltage devices. This makes silicon carbide power devices feasible even in kilovolt range and beyond. Hence, the improvement in the current handling capability of these devices can be achieved [1-5]. More explicitly, due to the high Si-C bonding energy of about 5.0eV, SiC is resistant to high temperature and radiation.

Its intrinsic resistance to oxidation, corrosion and creep at high temperatures makes it desirable for harsh environment device applications. It is also an excellent heat sink because of its very high thermal conductivity. The combination of excellent semiconducting and mechanical properties therefore makes SiC the most promising material of choice for device application.

SiC offers various application opportunities :

- High voltage and power electronics applications such as lamp ballasts, motor control, medical electronics, automotive electronics, high-density high-frequency power supplies and smart-power application-specific integrated circuits.
- High-temperature sensor applications for aircraft engines, oil drilling and automotive electronics with controlling fuel efficiency and emissions.
- SiC offers the advantages of eliminating expensive cooling systems needed in industrial equipment essential to factories worldwide.

1.1 SiC Polytypes :

Silicon carbide exists in hundreds of different polytypes, the most common being 3C-SiC,4H-SiC and 6H-SiC. Furthermore, islands of 15R-SiC can be found on 4H-SiC and 6H-SiC wafers and small crystals of 2H-SiC have been grown. The difference between the polytypes is the staking order between the double layers of carbon and silicon atoms. In Figure-1.1, the stacking sequence is shown for the three most common polytypes 3C, 4H and 6H-SiC. Cubic and hexagonal crystal structures of Silicon Carbide are shown in Figure-1.2. If we assign a Si-C atom pair in an A- plane in a close packed lattice as A, and in the B-plane as B, and in the C-plane as C, then we can generate a series of lattice unit cells by variation of SiC plane stacking sequence along the principal crystal axis as in Figure1.1.

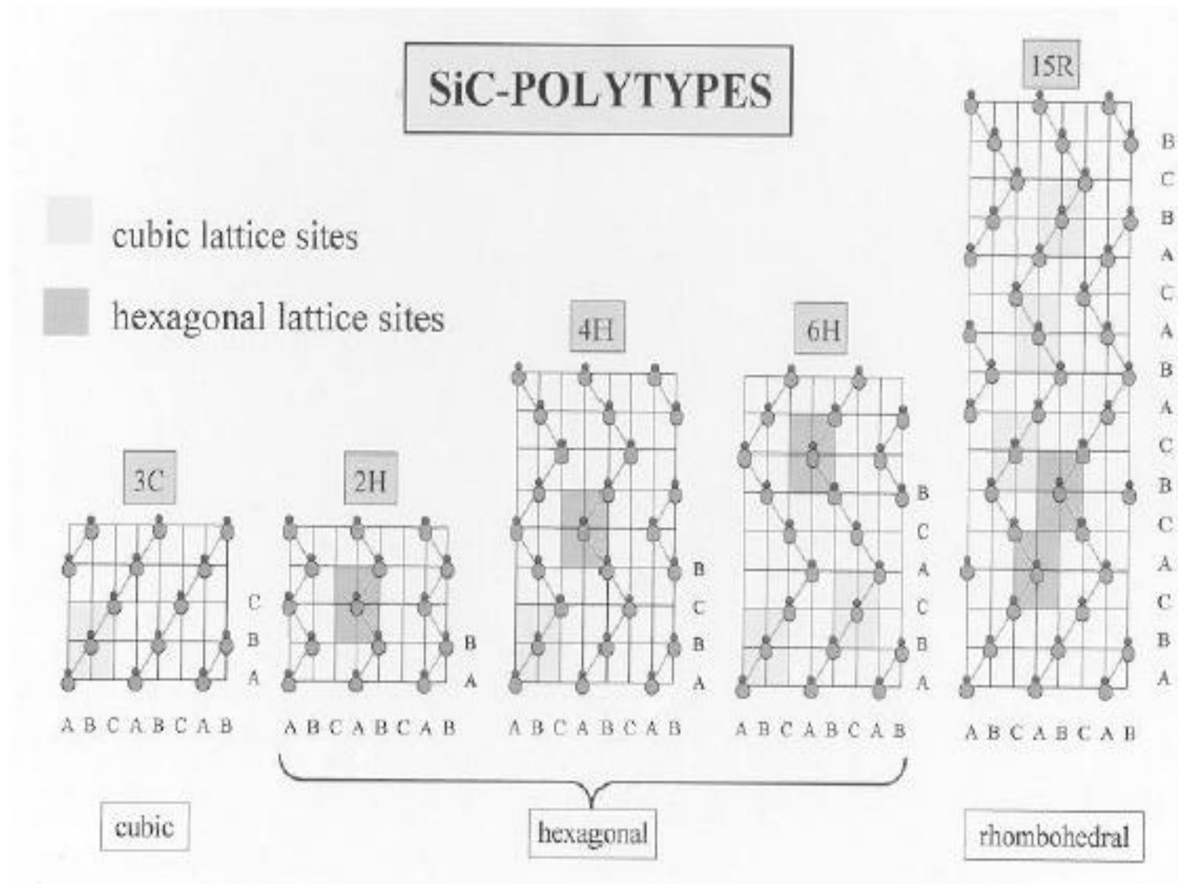

Figure 1.1 Stacking sequence of the most common polytypes of SiC(After Hudgins, Ref.[6])

The ABCABC... stacking, will engender the 3C-SiC zinc-blende lattice and ABAB... stacking on the other hand will produce the 2H-SiC wurtzite lattice. Other stacking sequences such as ABACABAC.. and ABCACB... will generate 4H-SiC and 6H-SiC lattice structures respectively. The number of atoms per unit cell varies from polytype to polytype, significantly affecting the number of electronic energy.

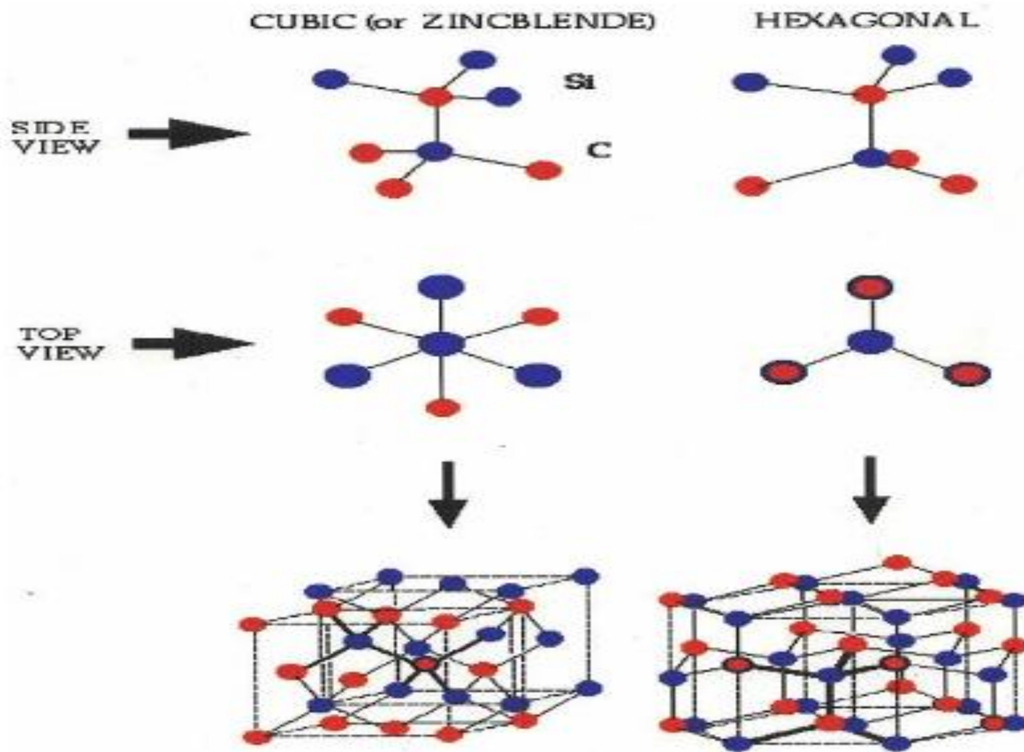

Figure 1.2 Crystal structure of Silicon Carbide (After Munish Vashishath, Ref.[73])

1.1.1 6H-SiC :

Due to the long repetition length in the crystallographic lattice 6H-SiC has a large anisotropy structure. Mobility in the perpendicular direction to the c- axis (commonly parallel to the surface) is four times higher than in the c- axis direction. Mobility in 6H-SiC is about 25% in the direction perpendicular to the c-axis as compared to Si and 7% in the direction parallel to it.

The saturation velocity for 6H-SiC is 2×10^7 cm/s in the direction perpendicular to the c axis, but only $0.6\times$cm10^7cm/s in the direction parallel to it.

1.1.2 4H-SiC :

With a small anisotropy (20% higher in the direction parallel to the c-axis) low-field mobility for 4H-SiC is about half that of silicon. The anisotropy in 4H-SiC depends on the electric field distribution and at high electric fields the saturation velocity is 20% lower in the c axis direction.4H-SiCand 6H-SiC are the most common poly types which have been characterized most thoroughly in literature so far. The transport properties are better for 4H-SiC and at present, this poly type forms the basis for most of the commercial electronics products [7].

1.1.3 3C-SiC :

This polytype can be grown on silicon substrates hence there is significant interest for low cost, large-size 3C-SiC wafers for microelectronic applications. Another advantage is that 3C-SiC does not suffer from stacking faults growth. 3C-SiC has larger electron mobility than for 4H-SiC but has reduced hole mobility. The main disadvantages when compared to other polytypes are the lower band-gap and breakdown field. Thus advantage of replacing existing silicon devices thus strongly hampered[7].

1.1.4 15R-SiC :

15R-SiC is very complex structure with 15 atomic layers ordered in a rhombohedral structure. A few years ago, much attention was given on 15R-SiC because of improved experimental MOSFET performance when compared to the other polytypes [8]. These devices have been manufactured on 4H-SiC or 6H-SiC substrates, where pieces of 15R-SiC were found. Mono-crystalline 15R- SiC wafers are however not a reality in the near future.

1.1.5 2H-SiC:

2H-SiC is not a commercially available substrate, but small mono-crystalline pieces have been grown successfully. The performance perpendicular to the c-axis direction is quiet similar to 4H-SiC, but the mobility is better in the direction parallel to the c axis [8].Research is going on in order to study this polytype at a greater depth.

Table1.1 lists some electrical properties of the most common SiC polytypes in comparison to that of Si, GaAs and GaN [9-10]. The most important SiC property of all is the large bandgap, which is nearly three times larger than that of silicon. The large Si-C bonding energy makes SiC

resistant to chemical attack and radiation. Silicon carbide belongs to a class of semiconductors commonly known as wide band gap semiconductors, where conventional semiconductors like Si and GaAs cannot adequately perform under extreme conditions. The wider band gap of SiC also enables one to design smaller, higher density devices that will withstand high voltages. Also, the thermal conductivity of SiC (4.9 W/m-K) is much larger than that of Si and GaAs and its a major advantage for SiC based devices. The high thermal conductivity of SiC decreases the need for special packaging and system cooling for successful device operation.

1.2 Transport Properties :

Analysis of transport parameters is required for reliable and efficient device performance. Published measurements are the main source of information used in the tuning process of various transport models and the immature nature of silicon carbide and lack of measurements for many transport properties implies that the available set of transport parameters is incomplete.

1.2.1 Mobility :

The mobility is defined as how easily the electrons and holes can be move inside a specimen under the influence of an electric field. Due to random scattering within the crystal, the velocity does not increase linearly with electric field. The electron velocity rather quickly reaches an equilibrium mean-velocity proportional to the mobility and the electric field. The mobility in Silicon Carbide is somewhat lower in comparison of silicon. The low mobility in SiC devices is compensated by its ability to withstand high electric fields taking advantage of the higher carrier velocity. To some extent the mobility can be described using the same models as those used for silicon. The parameters for the mobility models are collected from measurements for a temperature dependent mobility model [12].

1.2.2 Saturation Velocity :

At high electric fields, due to increased scattering the velocity ceases to be proportional to the electric field. The velocity saturates at v_{sat}, which for SiC is approximately twice the value than that for silicon. A high saturation velocity allows faster devices with shorter switching times.

1.2.3 Band Gap :

A forbidden zone in the energy spectra for a crystal is known as band gap. Crystal is a metal without a band-gap and with a large band-gap, the crystal is an insulator. A semiconductor has a band-gap up to a few eV. For some traditional semiconductors the band gaps are:

1.11 eV for Si, 0.7 eV for Ge, and 1.4 eV for GaAs. Many of the favourable transport parameters in SiC are related to the large band-gap, which is of the order of 3 eV. For such a large band gap the intrinsic carrier concentration(responsible for the thermal noise and also partly responsible for the leakage current) is negligible at temperatures up to 600°C. The minimum energy required to create an electron-hole pair is equal to the band-gap and in case of SiC this energy falls within the 3 eV range corresponding to a photon with wavelength close to 400 nm. SiC devices are thus also insensitive to the main part of the visible spectrum, making SiC suitable as a detector material for UV radiation with minimal noise from the visible background [13].

1.2.4 Critical Electric Field :

With high electric fields, the carriers energy increases and the probability of an impact ionization event increases as the energy exceeds the band-gap. In an impact-ionization event the carrier knocks out one electron from the valence-band thus creating an electron-hole pair (EHP) in turn. Now according to conservation of energy principle, the energy for the incident carrier is reduced by the band gap energy plus the initial energy for the created electron and hole. The critical electric field is related to the impact ionization rate, which increases as the carrier energy exceeds the band-gap value. Due to the large band- gap the critical electric field is thus about 10 times higher in SiC than for small band-gap materials such as Si and GaAs. With high E_c devices can be much smaller for the same voltage, alternatively operate at much higher voltages.

Table 1.1 Comparison of electronic properties of SiC polytypes with Si, GaAs and GaN, After Hudgins,Ref.[6])

	Si	**GaAs**	**GaN**	**6H-SiC**	**4H-SiC**	**3C-SiC**
Bandgap (eV)	1.1	1.412	3.39	3	3.26	2.2
Breakdown field @ 10^{17}cm^{-3} (MV/cm)	0.6	0.6	3.3	3.2	3.0	1.5
Electron mobility @10^{16}cm^{-3} (cm^{2}V-s)	1100	6000	1000	370	800	750
Hole mobility @10^{16}cm^{-3} (cm^{2}V-s)	420	320	200	90	115	40
Saturated electron drift velocity (cm/s)	10^7	10^7	2.5×10^7	2×10^7	2×10^7	2×10^7
Intrinsic concentration n_i (cm^{-3})	1.5×10^{10}	1.9×10^{-10}	2.1×10^6	2.3×10^{-6}	8.2×10^{-9}	6.92×10^{-9}
Thermal conductivity (W/cm-K)	1.5	0.55	1.3	4.9	4.9	5

1.2.5 Thermal Conductivity :

Thermal conductivity is a very important quality in power semiconductor devices in order to conduction of heat in the device. For high power devices the thermal effects constitute one of the main limiting factor of the performance. One of SiC´s competitors is gallium nitride (GaN), which is a material with similar properties to those of SiC but gallium nitride has lower thermal conductivity than silicon (1.3 W/cmK) and silicon carbides. However, gallium nitride is often

grown on SiC substrates, with its better thermal conductivity. Nevertheless, the GaN-SiC interface has lower thermal conductivity than GaN itself which leads to a degradation of the performance.

1.3 Advantages of 3C-SiC:

- The electron Hall mobility is isotropic and higher compared with these of 4H and 6H polytypes due to low density of interface states.
- This polytype can be grown on silicon substrates hence there is significant interest for low cost, large-size 3C-SiC wafers for microelectronic applications.
- Due to the smaller band gap of 3C-SiC, the interface states observed in 6H-SiC and 4H-SiC , a parameter for poor performance are located in the conduction band and have no effect on the transport properties of the channel.
- The specific junction capacitance will be lower in the 3C-SiC devices as compared to the 4H-SiC and 6H-SiC ones because of lower drift region doping, a factor arises due to lower energy band gap for a given blocking voltage. This is an advantage for the high speed MOSFETs.
- Smaller band gap permits "inversion" at lower electric field strengths, a boost for better performance of MOSFETs.

1.4 Need of Vertical DIMOSFET :

- There is no requirements for post-optical lithography techniques such as x-ray, extreme ultra-violet, electron projection lithography, ion projection lithography or direct write e-beam which are quiet expensive as Vertical MOS transistor channel length is not defined by lithography.
- Vertical MOS transistors have high packing density of at least a factor of four as compared to horizontal transistors as it can be made with both front gate and back gate, which doubles the channel width per transistor area. Another key factor is the use of very narrow pillars with the gate surrounding the entire pillar with the help of which fully depleted transistors can be manufactured that will have all the advantages of SOI transistors.

- Vertical MOSFET with added features such as a polysilicon source to reduce parasitic bipolar effects or a dielectric pocket to reduce drain induced barrier lowering (dibl), eliminates the concept of short channel effect from dominating in these transistors.

1.5 Objective of current work:

3C-SiC DIMOSFET with Gaussian function profile for obtaining High breakdown voltage:

The 3C-SiC is a potential material for MOSFET devices because of high channel mobility due to lower density of interface states compared with 4H-SiC. High breakdown voltages can be achieved for 3C-SiC vertical DIMOSFET by the use of Gaussian function doping profile in the drift region of the device. This profile can be generated by ion implantation from the drain end of the device, so that the projected range is close to the drain end of the device. In this work study of various Gaussian profiles will be done by changing different function parameters. For each profile, punch through and avalanche breakdown voltage will be calculated. Minimum of these calculated breakdown voltages will be considered as breakdown voltage of DIMOSFET for that profile.

In this work maximum breakdown voltage of 6.84kV has been achieved theoretically in DIMOSFET with Gaussian profile in drift region.

CHAPTER 2
LITERATURE SURVEY

Silicon carbide (SiC) is WBG (wide band gap) semiconductor that acquire a high quality native oxide(SiO_2) for use as an insulator in electronic devices. Advantages of silicon carbide includes high field strengths, better heat sinking capacity. Due to high thermal conductivity and high breakdown electric field strength, SiC can be used at high temperature, high power ,high voltage, and high frequency applications.

Thermal oxidation of Silicon Carbide produces a insulating layer of SiO_2 on the surface while the carbon atoms escapes as gas(CO) from the SiC. Thus it is possible to make all devices found in silicon IC technology today with silicon carbide with high quality, stable Metal oxide semiconductor transistors and MOS integrated circuits. Some of the examples of WBG semiconductors are: gallium nitride (GaN, E_g=3.4eV), aluminum nitride (AlN, E_g= 6.2eV) and silicon carbide (SiC, E_g between 2.2-3.25 eV depending on the polytype). Because of thermal stability of SiC, diffusion coefficients are very low. Hence dopant impurities cannot be diffused at any practical temperature. Although SiC offers significant advantages over silicon, it is still undeveloped as a semiconductor material. The main limitations of the technology are in the area of single crystal growth.

2.1 Crystal Growth:

In the year 1955, a laboratory simulation process was developed by J. A. Lely[14] for growing SiC crystals through sublimation process. In that process, the nucleation of individual crystals were uncontrolled and the resulting crystals were randomly sized hexagonal-shaped SiC platelets. In 1978, Tairov and Tsvetkov [15] introduced the growth of SiC single crystals by the vapour transport process. In 1983, modified sublimation process for growing SiC single crystals was introduced by Ziegler [16]. In year 1987, a research team under R. F. Davis at North Carolina State University (NCSU) announced a modification to the original Lely sublimation process [17]. In the improved version of this process, only one large crystal of single polytype is grown. In this process, a charge of polycrystalline SiC is heated in a graphite crucible containing argon at200 Pa. and it is the basis of current commercial systems.

In 1987, Cree Research, small company founded by a team of students from the NCSU group produced silicon carbide commercially. The introduction of 25 mm single crystal wafers of 6H-SiC by Cree in 1990 has ignited the interest in SiC research and device development in this material. At present commercially available, 35 mm diameter wafers of both 4H- and 6H-SiC are provided by Cree. Research (Durham, NC, USA) and from Advanced Technology Materials, Inc. (Danbury, CT, USA). Blue LEDs with 50 mm diameter wafers are used at Cree and 75 mm diameter wafers have been prototyped by both Cree and Westinghouse(now Northrup Grumman).

Present research of crystal growth revolves around increasing the deposition rate, increasing the diameter of wafers and reducing the defects of material. Current SiC wafers have etch pit densities of the order of $10^4 \mathrm{cm}^{-2}$. Nakata, et al. [18] classified these defects as EP-1, EP-2 and EP-3.The EP-1 defects are known as "micropipes" and are the open cores of giant screw dislocations with large Burgers vectors. Micropipes are holes about 0.5 - 10 microns in diameter that run completely through the wafer and subsequently grown epilayers, and hence are harmful to most of the devices. In recent years, micropipe densities have been steadily declining. Current Cree production wafers have micropipe densities in the 50-100 cm^{-2} range and wafers with a nominal 3.5 micropipes cm^{-2} have already been reported [10]. Doping of silicon carbide can be done during epitaxial layer growth or after crystal growth by ion implantation.

Chemical vapour deposition (CVD) is used for epitaxial layer growth on slightly off-axis substrates (3.5 degrees for 6H- and 8 degrees for 4H-SiC). These off-axis substrates helps in step-controlled epitaxy [19] in which several alternating silicon and carbon planes are exposed on the growth surface, which resulted in stacking information that preserves the polytype in the epitaxially grown film. Typical growth rates are in the range of 1-5microns/hour at a temperature window of 1200 - 1500° C with SiH_4, C_3H_8 and H_2[20] in chamber. Recently development in site-competition epitaxy has increased the doping range achievable by CVD, with doping as low as 1×10^{14} $\mathrm{cm}^{-3}$and as high as >1×10^{19} cm^{-3} have already been demonstrated [21]. E. Janzen, et al. [22] of Linkoping University recently developed a modified CVD technique that is capable of growing films up to100 microns thick with a doping level of 1×10^{14} cm^{-3}. With the help of these results, theoretically fabrication of power devices having blocking voltages in excess of 10 kV is possible. In 2008, a process suitable to produce high-quality 3C-SiC hetero-epitaxial films of single crystal morphology has been developed in a hot-wall CVD reactor. Epitaxial film

deposition on planar (100) Si substrates was performed at a growth rate ranging between 15 and 30 μm/h[75].

Selective doping of SiC is achieved by ion implantation, since the diffusion coefficients of aluminium and nitrogen are so low that thermal diffusion is practically impossible at all temperatures. Implantation and activation with concentrations above 1×10^{19} cm^{-3} of nitrogen to produce n-type regions is studied well and can be obtained routinely. Current research however lies in the area of P-type selective doping. The two most common dopants (p-type) aluminium and boron, produce relatively deep acceptor levels but aluminium with smaller ionization energy is generally chosen. During implantation, amorphization is reduced by using elevated temperatures, typically around 650°C for nitrogen and up to 1100° C for aluminium. However boron can be implanted successfully at room temperature. Amorphization thresholds of 4×10^{15} cm^{-3} for nitrogen, 1×10^{15} cm^{-3}for aluminium and 5×10^{15} cm^{-3} for boron have been reported by Kimoto, et al. [23-24] .

Recently HOYA Corporation, Japan, has come up with a new technology for the production of large mono-crystal 3C-SiC wafers. Before this only 13μm 3C-SiC wafers were commercial available. But with new process, large mono-crystal 3C-SiC substrates (at least 200 micro-meter thick, six inch in diameter, after removing the Si base layer), can be manufactured [25] and are expected to hit the market in 2013[76]. HOYA's 3C-SiC substrate has the same geometry as typical Si wafers and can be used in conventional Si semiconductor device production lines without hardware modifications.

2.2 Development of Power MOSFETs:

In the late 1980s, it was observed that power silicon devices were heading towards their theoretical limits and that these limits could be appreciably extended by fabricating power devices in the materials with higher breakdown electric fields, such as silicon carbide [26].

Silicon carbide MOS characteristics were demonstrated in a paper by Brown et al [27] in 1994. This paper analysed data that characterized the SiC/SiO_2 interface and explained one of the previously mysterious abnormalities observed in the characteristics of SiC MOSFETs. The exceptional eccentricity between the MOS characteristics on p and n type SiC wafers pointed that the difference is probably caused by the fact that the p type wafers are Al doped and the n type wafers are N doped. A similar approach can be seen with the relocation of impurities that

occurs during the thermal oxidation of SiC and Si. P type dopants are incorporated into the oxide whereas n type dopants are discarded by the oxide during growth**.** Hence the Al dopant in the oxide is likely to be the causes of the p type SiO_2/SiC interface characteristics.

The first MOSFETs in SiC were reported in the late 1980s whereas the first power MOSFETs were introduced in 1994 [28]. Vertical-trench MOSFETs or UMOSFETs were the only power devices. UMOSFETs are lucrative because of epitaxially growth of base and source regions without the need for ion implantation and coupled high temperature annealing. In UMOSFETs, the MOS channel is formed on the sidewalls of trenches created by RIE. However, two serious problems were reported with SiC UMOSFETs:

- A high electric field in the gate oxide caused by higher electric fields in the SiC drift region. This problem leading to cataclysmic failure of the gate oxide at higher drain voltages originates at the trench corners, thus restricting the maximum operating voltage to less than 40% of ideal breakdown voltage.
- The low inversion layer mobility along the trench sidewalls results in high specific on-resistance, which eliminates the advantage of lightly doped drift region in SiC [29-32].

By 1995 breakdown voltage of about 260V on the carbon face of SiC had achieved for UMOSFETs. In the year 1995 with a self aligned process, surface channel n-MOSFET devices in 6H-SiC are fabricated with n^+polysilicon gates on 80 nm thick gate oxide. The mobility and sub-threshold slope, 40 cm^2/Vs and 500mV/decade respectively were equivalent to MOSFETs fabricated with a non self aligned process. These MOSFETs exhibit a saturation drain current density of 18mA/mm^2 (approximately three times higher than the paramount self aligned 6H silicon carbide MOSFETs reported to date and roughly five times higher if scaled to the same oxide thickness [33-36]) at 340°C when the gate is 9V above threshold. The presence of aluminium in thermally grown oxides on 6H-silicon carbide has been established in 1996. N-type and p-type 6H-silicon carbide wafers along with p-type sifvflicon control wafers were oxidized in dry oxygen at 1275°C for 45 minutes. Capacitance-voltage calculations on the SiO_2 films formed on the n-type 6H-SiC and the silicon control wafers yielded near ideal characteristics while high effective charge and interface state densities were revealed with SiO_2 films on 6H-SiC.

In 1996, US Air Force (WPAFB, Dayton Ohio) and Office of Naval Research, Arlington, Virginia demonstrated the advantages and limitations of 4H-SiC power UMOSFET structure. According to this report, higher breakdown voltage can be achieved by the use of p+ polysilicon gate because it reduced the Fowler Nordheim injection from the gate electrode. It was also concluded that the insulator reliability is the limiting factor and therefore the high temperature operation of these devices may not be practical feasible [37-39].

In year 1997, A UMOSFET was introduced by Denso Corporation Japan. This UMOSFET achieved a blocking voltage of 450V [40], a specific on-resistance of 10.9 $m\Omega cm^2$and $V_B^2/R_{on-sp}$of 18.6 MW per cm^2 . In the same year, Northrop Grumman Science and Technology Centre fabricated the 4H-SiC UMOSFETs with the blocking voltages of 1.1kV and 1.4 kV [41]order. 4H-SiC DIMOSFETs at a blocking voltage of 900V [42] was also introduced by it.

In the year 1998, a SiC accumulation-channel UMOSFET with new structural features that shield the trench oxide from high electric fields in the blocking state [43-44] was by demonstrated Purdue University. Introduction of p-type region in the trench bottom by self-aligned ion implantation and a thin n-type epilayer incarcerated between the n-drift region and the p-type base were some new features. The oxide breakdown problem at the trench corners was solved in 1996 with the introduction of planar implanted DMOSFETs [43-45] where elimination of trenches was done. A threefold improvement in the device blocking voltage had been seen with the elimination of the trench corners. The 760 V blocking voltage was achieved using 6H-SiC.

In 1998, 4H-SiC UMOSFET was with a breakdown voltage of 1.4 kV was fabricated by CREE Research Inc and a specific on-resistance of the order of 311 $m\Omega cm^2$ had been calculated [44]. The fabricated device required drift region impurity concentration of $1x10^{15}/cm^3$ and required n^-epitaxial layer thickness of 15μm. For the prototype module three kinds of 2.0 kV UMOSFETs with different chip areas (0.7x0.7, 1.5x1.5, and 3.0x3.0 mm^2)were designed. All were fabricated in CREE Research Inc by using 4H-SiC wafers.

The effectiveness of silicon carbide for the device application was demonstrated in the year 1999 at greater length [46]. In the same year, the theoretical and numerical analysis of SiC JFET and MOSFET at 6.5 kV was given. Improvement of on-state/breakdown performance of the JFET by buring layers in conjunction with a highly doped buffer layer was elaborated in this report. In order to achieve a 6.5 kV breakdown voltage, the 60μm long n-drift region length with a doping concentration of $2x10^{15}$ cm^{-3} was proposed. The distance between the gate and the source was

taken as 0.6 μm. For a trench MOSFET, the p-well doping was $5x10^{17}cm^{-3}$ and its length was equal to 3.8 μm was calculated. The doping concentration of the n-drift region had been decreased to $1.7x10^{15}cm^{-3}$ and the gate oxide thickness for the simulated structure was chosen as 0.2μm [47-48].

In the year 1999, a fabrication process was established for high voltage (400V) planar SiC DIMOS devices to minimize step bunching by using aluminium as the p-well dopant with reduced temperature (Tmax=1400°C) processing. Electron mobility of 30 cm^2/Vsec at room temperature was obtained in inversion layer on aluminium implanted p-type regions. With the use of unique JFET spacer implants, the p-well spacing was scaled to 5 μm without affecting R_{on-sp} for promoting higher packing densities for silicon power devices. R_{on-sp} with the value 42 mΩcm^2 has been observed on the 2 μm spacer implanted devices that can be further reduced (35%) by decreasing the source window length in the process design [49].

In 1999, certain 6H-SiC enhancement mode n-channel MOSFETs parameters including inversion layer mobility, threshold voltage, intrinsic mobility reduction factor and interface state density were examined in great detail. The inversion layer mobility and threshold voltage were found to be dependent on substrate doping concentration level and device operating temperature. The interface state density was studied for different substrate doping concentrations. The inversion layer mobility was found to inversely proportional to substrate doping level. Hence fundamental dependencies of inversion layer and threshold voltage on these two parameters (substrate doping concentration and temperature) are quiet similar to silicon devices to some extent. Nevertheless the experimental data testify that these dependencies are modified by the presence of high density of interface states near the conduction band edge [50].

In 2000, characterization of SiC epitaxial channel MOSFETs were verified and demonstrated. Silicon Carbide epitaxial channel MOSFETs were fabricated with n^+epitaxial source and drain electrodes on 6H-SiC substrates.The electrical characteristics were modelled in the sub pinch off depletion and accumulation modes of operation. Under a 50% activation of channel donor impurities [51] a buried channel mobility of 230cm^2/V-sec and an accumulation-mode surface mobility of 45cm^2/V-sec were measured at room temperature. N_2O oxide on both n- and p-type 6H-SiC wafers was successfully fabricated for the first time in the year 2000 only. Improved SiC/SiO_2 interface and oxide qualities were analysed in N_2O grown MOS devices, especially for p-type devices. Smaller flat band voltage shift than N_2O nitrided and thermal oxide devices,

under high field stress was observed with enhanced device reliability. These advantages attributed to significant inclusion of nitrogen near the SiC/ SiO_2 interface during N_2O oxidation. So N_2O oxidation technique can be derived as potentially oriented process for making high quality and high reliability SiC MOSFET's, especially n-channel type [52].

4H-SiC RF power MOSFET was fabricated and characterised first time in early 2001[53] and the two-metal layer process improved the performance of this device which optimises the conflicting requirements of the acceptable inversion-layer mobility and the low contact resistance. The cut-off frequency of this device with 1μm gate length was above the 7 GHz mark. A breakdown voltage of the order of 950 V was achieved in MOSFETs with specific on-resistance of $24\Omega mm^2$. Dopant activation and post metallisation annealing reduced the parasitic resistances to small values. The sheet resistances of the n+ source/drain and n-drift regions were measured to be 300 Ω per sq and 3400 Ω per sq respectively. The resistivity of the ohmic contact was found to be $1.5x10^{-5}\Omega cm^2$.

In 2002, an analytical model of a SiC MOSFET came into light[54] and experimental results showed a semi-empirical formula for electric field intensity, dopant concentration and temperature dependent carrier mobility(μ). Based on this formula, suitable analytical mathematical-physical model were designed for simulation of current-voltage characteristics, trans-conductance and conductance of MOSFET. All models designs had two things common. First, the dependence of threshold voltage on temperature and impurity concentration in the channel and second is the effect of the channel narrowing. A 2.4 kV power, 10 A and high-voltage 4H-SiC DIMOSFET with characteristics of large area (3.3x3.3 mm^2) were also reported [55] in 2002. The MOSFETs demonstrated a peak MOS channel mobility of 22 cm^2/V-sec and a threshold voltage of 8.5 V at room temperature. The DIMOSFETs showed an on-resistance of 42 $m\Omega cm^2$ at room temperature and 85 $m\Omega cm^2$/V-sec at 200 ºC. Stable avalanche characteristics at about 2.4 kV were observed and high switching speed along with an on-current of 10 A were measured on a 0.103cm^2device. The MOS channel length(1.5μm) was defined by the p-well and n-implants, cell pitch was measured as 16 μm, the packing density of the gate periphery was around 1250 cm/cm^2 and a 20μm thick drift layer with a doping concentration of $2.5x10^{15}cm^{-3}$ chosen for a 2000 V blocking voltage design were depicted in that paper.

Introduction of total dose effects of gamma-ray radiation on enhancement mode 6H-SiC p-channel MOSFETs were demonstrated in the year 2003. The electrical characterization of these

transistors was measured before and after irradiation up to a total dose of 10^8 rad(SiO_2) by analysing drain-source current as a function of gate voltage and drain-source voltage. Comparisons were made between these transistors and 6H-SiC n-channel MOSFETs. It was found that the p-channel devices remained fully functional up to 10^6rad(SiO_2) whereas the n-channel devices were fully functional through 10^8 rad(SiO_2) . In that paper an observation was made that the generation of interface states induced due to radiations in the n-channel transistors was substantially lower than that of the p-channel devices [56].

Numerical device simulations on a 4H-SiC vertical MOSFET were reported [57-58] in 2003 and 2004. These simulations mainly targeted on reverse blocking voltage, threshold voltage and on-state resistance. The simulated gate MOSFET had a source depth of 0.2 micron, a gate oxide thickness of 50nm and a p-well depth of 1 micron while the channel length was proposed as 1micron.

Comparison of modern SiC power devices was presented in 2004. Static and dynamic behaviour of a 2 kV SiC MOSFET and IGBT were analysed in that paper. It was concluded that IGBT is at-least two times faster than MOSFET [59] in circuit performances comparison. The reliability of SiO_2 in a SiC MOS based device is determined by tunnelling current and if an intrinsic Fowler-Nordheim regime of tunnelling assumption is made, tunnelling current is exponentially dependent on the electric field in the dielectric medium and barrier height to carriers. Band offsets between metal/SiC and the dielectric mainly decides this barrier height. Since band offsets for SiC to most dielectrics are smaller than those with respect to Si. Then for same oxide electric field, a lower reliability is expected for SiC-dielectric based devices as compared to MOS devices. Channel mobility is affected by presence of interface states of SiC-dielectric and are useful for determine the barrier height for Fowler-Nordheim tunnelling. A trade-off exists between SiC-dielectric reliability and on-state resistance, that is dependent on dielectric thickness in a forward biased SiC-dielectric structure. The uses of alternative dielectrics to improve trade off was demonstrated in this paper [60].

1600V 4H-SiC UMOSFET with a dual buffer layer structure was presented in 2005 [61]. The fabricated device exhibited specific on-resistance of 50m$\Omega$$cm^2$ with 1µm of the channel length that could be further be altered to smaller values. The n-type drift layer was 25µm thick with 3-5x10^{15} cm^{-3} concentration. Two n-type buffer layers were grown on top of the p type drift layer. The first n type buffer layer was 3µm thick and 1-2x$10^{16}$$cm^{-3}$ doped with nitrogen while

the second layer was 0.5-1x10^{17} cm^{-3} doped with nitrogen and ~0.5μm thick, followed by the 0.8-1x$10^{17}cm^{-3}$ aluminium doped p-type 2μm thick base layer. Nitrogen implantations with high energy (up to 700 KeV) is used to form n+ region with ~1μm channel length. UMOSFET trench gates were perpendicular to the primary flat of the SiC wafers to achieve high inversion channel mobility [61]. On-state performance of trench oxide-protected SiC UMOSFETs for blocking voltages up to 14 kV on 115μm-thick n-type 4H-SiC epilayers was also presented [62]. A current density of 137A/$cm^2$and a specific on-resistance of 228 mΩcm^2 were achieved at a gate bias of 40 V in this paper and the effect of current spreading on the specific on-resistance for finite-dimension devices was also reported. First layer was of n^--4H-SiC, 115μm-thick, 7.5x$10^{14}cm^{-3}$ n+ type doped, cut 8° off axis and followed by 0.4 μm, 2x$10^{17}cm^{-3}$ n-type current spreading epilayer and finally a 1.5 μm, 2x$10^{17}cm^{-3}$ p-type epilayer to form the base region of the UMOSFET. Source contacts were formed by implanting 4x $10^{15}cm^{-2}$nitrogen at 650°C using a Ti-Au mask. Reactive ion etching with Ni mask was used to form gate trenches that were approximately 2 μm deep. Sacrificial oxidations were performed to smooth the trench sidewalls and the active area of the device was .018cm^2 that required a of current of 2.5 A. The device required a current density of 137A cm^{-2} . Layers of doping and the thickness used here were theoretically capable of blocking 14 kV but practically only 10 kV can be achieved. However further problems such as edge terminations limited the blocking voltage in the range of 5 kV [62].

4H-SiC DIMOSFETs with breakdown voltages of 1.2 kV and 1.8 kV were demonstrated [63] in the year 2006. An epilayer with doping concentration of 6x$10^{15}cm^{-3}$, a thickness of 12 μm could be used for 1.2 kV breakdown voltage and for 1.8 kV 4H SiC DMOSFET, the device had a gate oxide thickness of 500Å with corresponding electric field limited to approximately 3 MV/cm. 0.0936 cm^2 was the active area of this device. An on-resistance of 85 mΩ ($R_{on-sp}m\Omega cm^2$) with a drain current of 50 A (534 A/cm^2) at a forward drop of 5.7 V were the room temperature values. For RF applications in year 2006, GaN HEMTs allowed the use of highly efficient Class E circuit topologies presenting a high power of 63 W at 2 GHz with 75% power added efficiency. There was a reduction of 25% in losses in power supplies for computers and servers when power factor correction circuits used SiC Schottky diodes and when the SiC Schottkys were combined with a SiC MOSFET as the switch, 22% reduction in losses can be

observed further. SiC Schottky for motor control allowed a >35% reduction in losses as demonstrated for a 3 HP motor drive [64].

A compact circuit simulator model was constructed in 2007 and it was used to describe the efficient performance of a 2kV 4H-SiC power DIMOSFET. With the help of this model a comparison is made with the widely used 400V, 5A Si power MOSFET. Uniqueness of this model was due to two factors:

- Channel current expressions where they include the channel regions at the corners of square and hexagonal cells that could be turn on at lower gate voltages.
- The enhanced linear region trans-conductance .

The static and dynamic performance of both the Si and SiC devices were also actively described by this model. Detailed device comparisons in this paper showed that between the 400V Si and 2kV SiC MOSFETs ,both the on-state performance and switching performance at 25 °C were similar with a difference emphasized that SiC device required twice the gate drive voltage. The main fact involved between the devices was that SiC has a five times higher voltage rating without an increase in the specific on-resistance [65].

2.3 DIFFERENT SILLICON CARBIDE DEVICES:

Silicon carbide has several unique properties that can lead to enhanced and efficient performance of semiconductor devices. These properties include higher breakdown field, wider band gap, higher thermal conductivity, lower thermal generation rate, and lower intrinsic carrier concentration.

2.3.1 IMPATT diodes:

IMPATT diodes deliver the highest RF power to any semiconductor microwave oscillator and are used to produce carrier signals for microwave transmission systems, particularly airborne and ground-based radar.

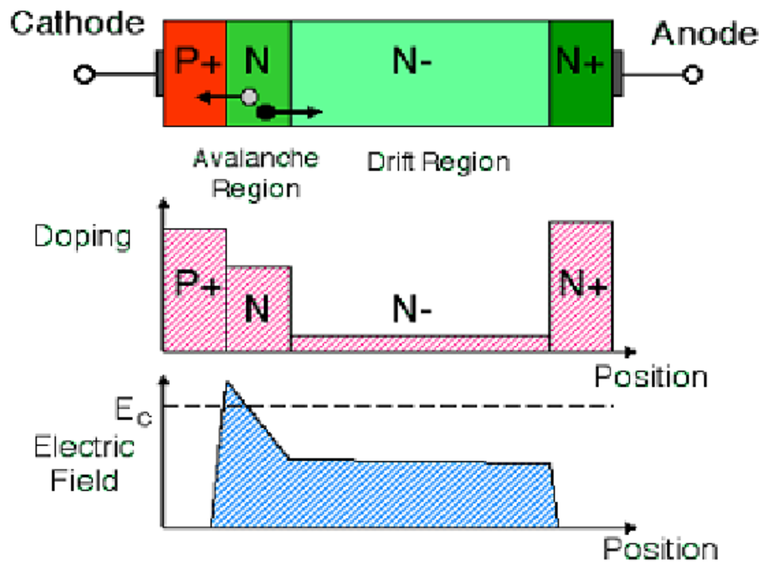

Figure2.1 Cross section of a SiC IMPATT diode(After L.Yuan et al., Ref. [66])

The frequency operation for IMPATT diodes ranges from few GHz to few hundred GHz. Due to high electric field, electron-hole pairs are generated in the “Avalanche Region”. Holes are swept across into the cathode but a displacement current in the external circuit is produced by the drifting of electrons toward the anode. Figure 2.1 indicates the build up of microwave oscillations in the diode current and voltage, when the diode is ingrained in a resonant cavity and when proper biasing is applied at breakdown.

2.3.2 Charge Coupled Devices:

A charge-coupled device (CCD) is a device for the movement of electrical charge, usually from within the device to an area where the charge can be manipulated, for example conversion into a digital value. This is achieved by "shifting" the signals between stages within the device one at a time. CCDs move charge between capacitive bins in the device, with the shift allowing for the transfer of charge between bins. Thus CCDs are linear shift registers created by a series of closely-spaced MOS plates on the surface of a semiconductor. Proper biasing voltages at MOS plates helps in the creation of localized potential wells in the semiconductor. Charge packets can be confined in these potential wells and can be shifted along the surface under the influence of suitable clocking waveforms applied to the gates. Silicon CCDs are widely used as image sensors primarily in digital still cameras and hand-held video cameras. SiC can be used as a specialized image sensor because of its wide band gap property that makes it transparent to

visible light, resulting in an ultraviolet (UV) sensor which is virtually canopy to solar radiation. These sensors can be used in a number of applications such as aerospace research, UV astronomy and in military systems.

2.3.3 Digital CMOS Integrated Circuits in 6H-SiC:

Low power consumption, full rail-to-rail output swing and enhanced noise margins, these are some of the advantages of CMOS technology with respect to NMOS circuits and thus it is attractive for digital logics. CMOS also provides active current sources for linear applications. It is expected that CMOS technology with SiC will provide low power, high temperature controlled circuits as well as reliable control circuitry for smart power integrated circuits. CMOS structure includes an implanted n-well and deposited oxides but due to other processing problems the PMOSFETs exhibits a very high threshold voltage. Implanted p-well and thermally grown oxide is used to fabricate this device.

The fabrication process is as follows:

- P-wells are grown on n-type epilayers doped at $8\text{x}10^{15}\text{cm}^{-3}$ by boron implantation. Al and N are then implanted through polysilicon masks to form P+ and N+ source/drain regions respectively.
- PMOSFETs are implanted on n-type epilayers and NMOSFETs are formed on p-wells. Then annealing is done at 160° C for 40 minutes in argon , followed by 2 hour wet oxidation at 115°C to form a 40 nm gate oxide layer.
- Polysilicon is then deposited and patterned to form gates at this structure. Al-Ni is used for p-type ohmic contacts while Ni is used for n-type contacts. After this a silicon oxynitride layer is deposited as an inter-metallic dielectric.
- Through the opening, interconnecting metal is deposited and patterned.

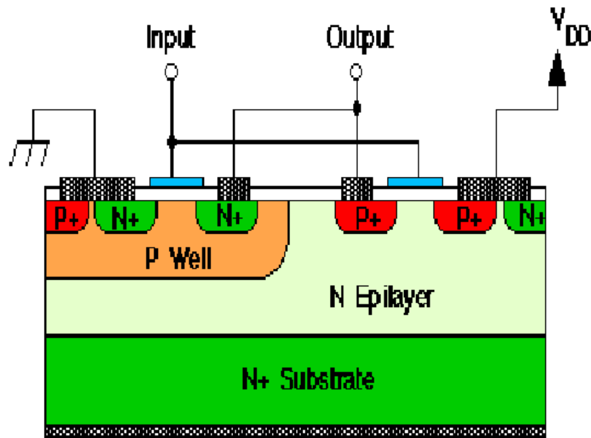

Figure 2.2 Cross section of a CMOS inverter in the implanted p-well process
(After Munish Vashishath and Ashoke K. Chatterjee, Ref. [67])

2.3.4 Schottky Barrier Diodes:

Schottky barrier diodes (SBD's) do not store minority carriers in the on-state and hence find its use in major application as power rectifiers. These devices can be switched off quickly with negligible reverse current. It was widely felt that SBD's will be the first SiC power devices to go into commercial scale production. The present fabricated SBD's on 4H-SiC have blocking voltages of the range of 1720 Volts.

2.3.5 Power MOSFETs:

The breakdown electric field of SiC is approximately 8-10 times higher than that of silicon. This property makes it possible to analyse and design power switching devices having correspondingly higher blocking voltages than their silicon counter parts. More significantly, the specific on-resistance (i.e. resistance-area product) of a power device scales inversely as the cube of the breakdown field, a property manifesting on-resistance of SiC power MOSFETs to go 100-200 times lower than comparable devices in silicon technology.

Power MOSFET can be classified under the following headings:

(i) Double implanted or DIMOSFET

(ii) UMOSFET

(iii) Lateral or LDMOSFET.

2.3.5.1 Double implanted or DIMOSFET:

Power switching devices are reaching the upper limits imposed by low breakdown field of silicon and this restraint can only be eliminated with a semiconductor with a higher breakdown field. Silicon carbide among other compound semiconductors with its wide band gap solved this problem in an efficient manner. Another feature includes its native oxide is SiO_2, the same oxide as of silicon. This means that power devices used in silicon can all be fabricated in SiC, a great boon in cost reduction. Double implanted MOS(DMOS) as shown in Figure 2.3. SiC DIMOSFETs have been fabricated with the blocking voltage of 760V. To obtain the blocking voltage greater than 760 V for 6H-SiC depends on the drift region thickness, doping level, specific on-resistance and electric field strength. By adjusting all these parameters we intend to get the blocking voltage greater than 760V. In these devices, the edge of the poly silicon gate serves as a common window for the diffusion of p-base and n+-source regions. Difference in the lateral diffusion between the p-base and n+ source region defines the surface channel region. The forward blocking capability is achieved by the p-n junction between the p-base region and the n-drift region. By applying a positive bias to the drain and short-circuiting the gate to the source, the p-base and n-drift region junction becomes reverse-biased thus supporting the drain voltage by the extension of a depletion layer on both sides of the junction. However, the depletion layer extends primarily into the n-drift region due to its lower doping level as compared to p-base region. A conductive path extending between the n+-source region and the n-drift region is formed by applying positive bias to the gate electrode.

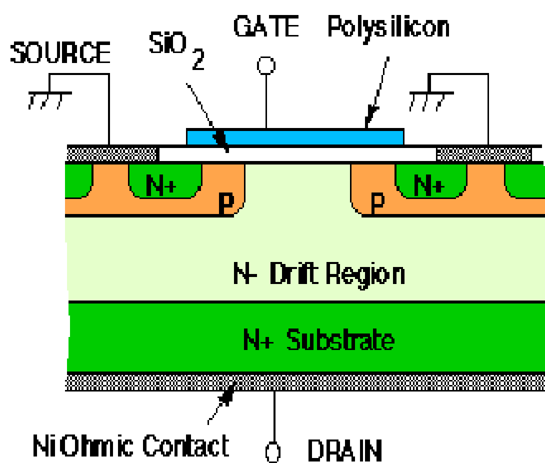

Figure 2.3 Double implanted MOSFET (After J. N. Shenoy et al., Ref.[68])

2.3.5.2 UMOSFET:

Fabrication of UMOSFETs are done by reactive ion etching because the electrical fields at the bottom corners are lower than that of at the tip of the V- groove MOSFETs. The substrate is lightly doped, thick to ensure a high blocking voltage and performs the function of drain electrode. The p-type base layer is grown epitaxially and it is grounded. As shown in Figure 2.4 the UMOS forms the necessary p-n junction and the MOS channel. Gate is grounded in the blocking state, that turns off the MOS channel . The large drain voltage is supported by the reverse-biased p-n junction and the MOS capacitor. The electric fields in various regions of device are also shown at the right of the Figure 2.4. It has been observed that the electric field at the trench corners is high due to two-dimensional effects and in the oxide at the trench bottom it is 2.5 times higher than the peak field in the semiconductor. Such high fields may damage the oxide before the p-n junction breaks down. Therefore in UMOSFETs, the maximum blocking voltage depends on oxide breakdown and not on the semiconductor breakdown [69]. The maximum breakdown voltage provided by this device structure is 260V. In order to eradicate this constraint of oxide breakdown, a new device structure with integral oxide protection has been developed which limits the electric fields in the trench and simultaneously reduces the on-resistance.

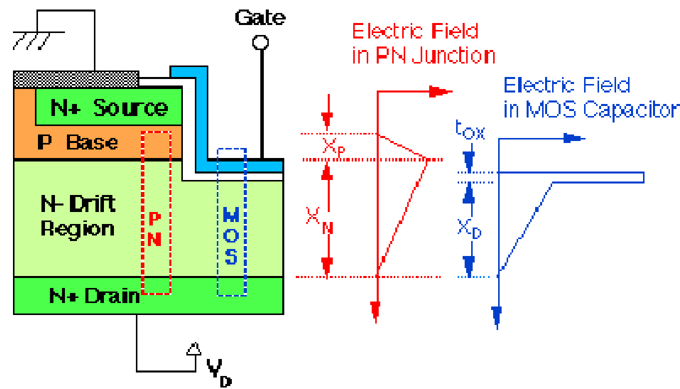

Figure 2.4 Cross section of 4H-SiC UMOSFET(After J.Tan et al., Ref. [69])

This new structure is shown in Figure 2.5 with electric fields in the blocking state. A new p-region is introduced at the bottom of the trench by ion-implantation thus reducing the electric field at the oxide/semiconductor interface to zero. Also a new n-type current spreading layer is grown epitaxially between the n-drift region and the p-type base layer that prevents the pinch-off

of the conducting channel in the on state. Introduction of this layers also facilitates the lateral current flow into drift region.

The various features of IOP-UMOSFET includes:

- The blocking voltage of the device is 1.4KV

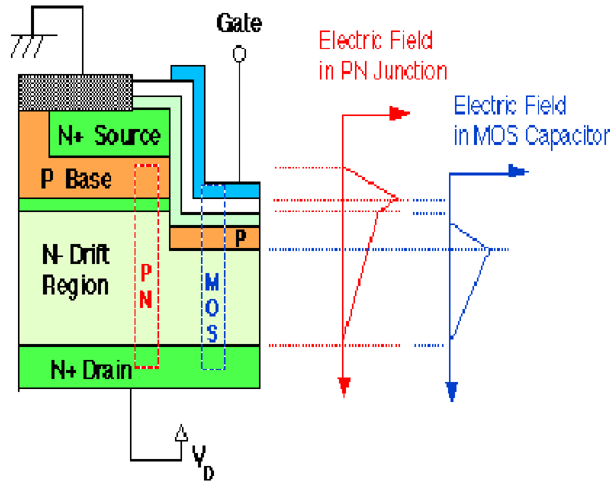

Figure 2.5 Cross section of 4H-SiC IOP-UMOSFET(After J. Tan et al., Ref.[69])

- The oxide breakdown failure does not occur.
- The specific on-resistance of device is 15.7 mΩcm^2.
- The figure-of-merit is 125 MW/cm^2, the highest value ever reported for a power MOSFET in any material system and 25 times higher than the theoretical limit for silicon power MOSFET.

2.3.5.3 Lateral MOSFET:

MOSFETs and thyristors ruled the semiconductor industry before power devices of SiC came into picture. These devices had been fabricated as vertical structures with the substrate acting as an anode. In the off state, the voltage was supported by reverse-biased p-n junction and for high blocking voltage the drift region should be lightly doped and thick. For a given device thickness, maximum possible blocking voltage was observed to be independent of doping level. In order to overcome the limitations of vertical-type MOSFETs we use lateral type MOSFET[70]. For SiC lateral MOSFETs with a 10 μm drift region, the maximum possible voltage 1600V has been achieved. The Structure of lateral DMOSFET is depicted in Figure 2.6. Insulating substrate is of Silicon Carbide and the depletion layer spreads mainly into the lightly-doped drift region. When depletion width reaches the insulating substrate, it continues to spread toward the drain. Here the

maximum voltage is not limited by the thickness of the layer. So above discussion does point to a fact that device should be fabricated laterally rather than vertically because there is no necessity for an increase of surface area required for the device.

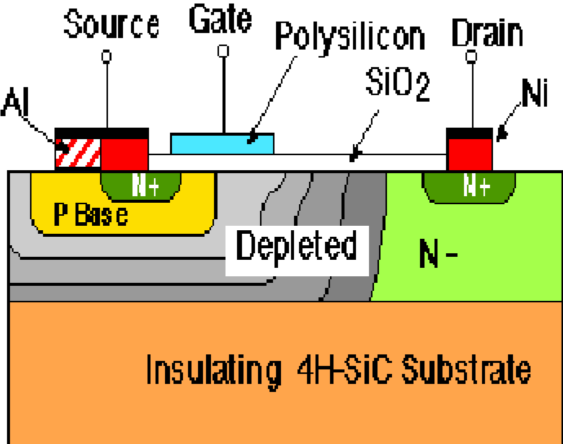

Figure 2.6 Cross section of lateral MOSFET (After J. Spitz et al., Ref. [70])

CHAPTER 3
THEORY OF DIMOSFET

Power switches works as the heart of all electronic power systems. With reduced costs, ease of control and increased power capabilities of power switches have made power electronic systems important in a large number of applications. Thyristors and bipolar transistors were the first power switches . Thyristors, due to their ratings scaled at a faster pace than bipolar transistors were used in higher power systems . Bipolar transistors with faster switching capabilities were used for low and medium power applications. The rating of these devices grew steadily until the late 1970s, the years in which the first power MOSFETs were introduced. With the introduction of the first power MOSFETs, Silicon power MOSFETs have been developed at a faster rate and have become the dominant device technology till 1980s for many device applications. MOSFETs are superior than bipolar transistors in many aspects. Firstly, MOSFET with very high input impedance provides the simplest gate drive requirements. The creation of various layers, accumulation, depletion or inversion layers under the MOS channel can be controlled using integrated circuits as small gate current is required for charging and discharging of high input gate capacitance. Secondly, the MOSFET is a majority carrier device. Therefore, there is no need for minority charge storage operation, a boost for faster switching operations. Thirdly, MOSFETs have superior ruggedness and forward biased safe operating area as compared to the bipolar transistors which eliminates the use of snubber circuits for protection of the switch during operation during typical hard-switching applications. Fourthly, resistivity increases with temperature in silicon with majority carriers, hence thermal runaway behaviour is also avoided in MOSFETs. With this advantage, MOSFET devices are formed with parallel combination of many thousands of individual MOSFET. Additionally, as compared to power bipolar transistors MOSFETs show better output characteristics for paralleling. Hence, power MOSFETs are more desirable for high voltage/power and high frequency electronic applications.

However, the blocking voltage capability of the MOSFET depends upon the ratings of the reverse body diode of the drift region. This blocking voltage is a function of distance between source and drain end. High blocking voltage capability due to geometry indicates high resistance, so a trade-off exists between diode voltage capability and low drift region resistance.

A theoretical first-order analysis based only on the drift-region of ideal Si and SiC MOSFET's has been performed to determine specific on-resistance $R_{on, sp}$ to demonstrate the superiority of the SiC MOSFET's over the Si MOSFET's. This evaluation is in terms of the reduction in the on-resistance and consequent improvement in the current-handling capability of SiC power MOSFET's at higher breakdown voltages.

3.1 Basic working of DIMOSFET:

The fabrication of DIMOSFET structure is done by using planar diffusion technology with a gate such as poly silicon. In these devices, the edge of the poly silicon gate serves as a common window for the diffusion of p-base and n+-source regions. Fig.3.1 shows a cross section of a power DIMOSFET structure. Difference in the lateral diffusion between the p-base and n+ source region defines the surface channel region. The forward blocking capability is achieved by the p-n junction between the p-base region and the n-drift region. During the device operation, a fixed potential to the p-base region is provided by the connection of base to the source metal through a break in the n+ source region. By applying a positive bias to the drain and short-circuiting the gate to the source, the p-base and n-drift region junction becomes reverse-biased thus supporting the drain voltage by the extension of a depletion layer on both sides of the junction. However, the depletion layer extends primarily into the n-drift region due to its lower doping level as compared to p-base region. A conductive path extending between the n+-source region and the n-drift region is formed by applying positive bias to the gate electrode. The application of a positive drain voltage results in a current flow between drain and source through the n-drift region and conductive channel.

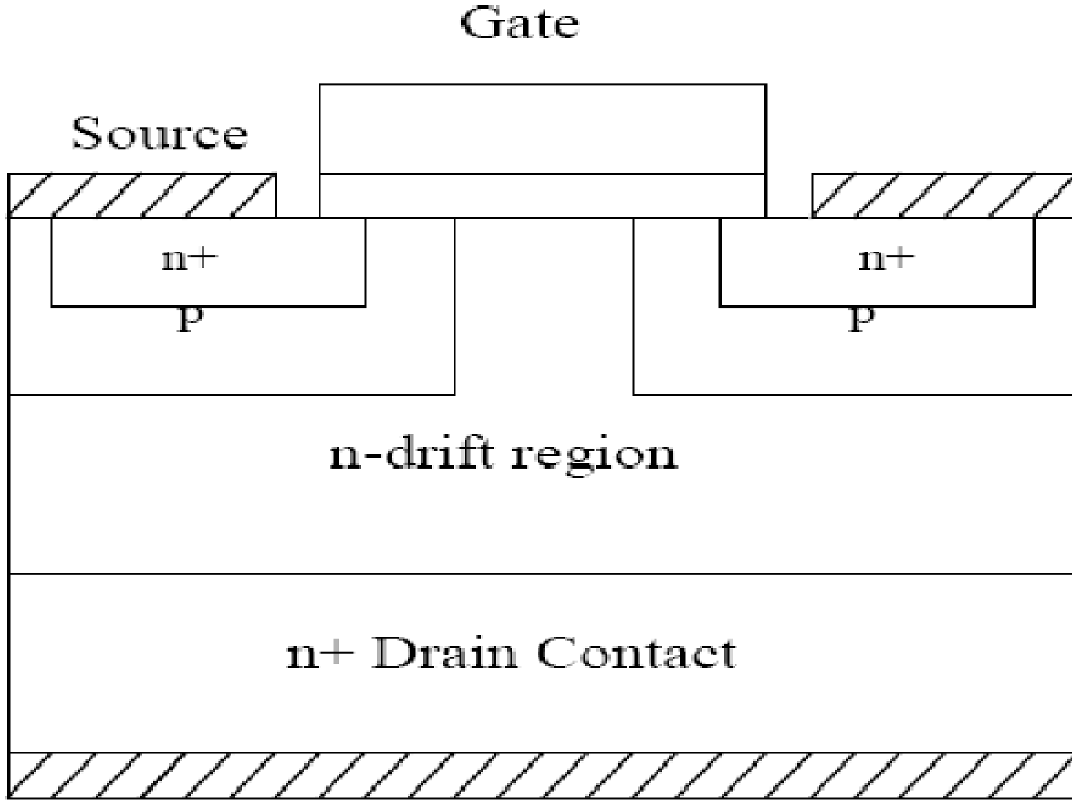

Figure 3.1 Structure of basic DIMOSFET

(After Munish Vashishath and Ashoke K. Chatterjee, Ref. [71]

With the application of a positive drain voltage , current starts flowing between drain and source through the conductive channel and n-drift region in the trapezoidal form. Gate bias voltage modulates the conductivity of the channel and flow of current is decided by the resistance of various resistive components shown in Fig.3.2 .

The total $R_{on,\,sp}$ is determined as

$$R_{on,\,sp} = R_{+} + R_C + R_A + R_J + R_D + R_S \quad (3.1)$$

where R_{+} is the contribution from the n+-sources, R_C is the surface channel resistance, R_A is the accumulation layer resistance, R_J is the resistance in the drift region between the p-base regions due to the JFET pinch off action, R_D is the drift region resistance and R_S the substrate resistance. For an idea DMOSFET, the resistances associated with the n+-source, the n-channel, the JFET, the accumulation region, and the n+-substrate are assumed to be negligible. Specific on-resistance of the power MOSFET is thus determined by the drift region only. This assumption is not valid at lower breakdown voltages where the drift region resistance R_D is comparable to the

other resistive components. However, at higher breakdown voltages, R_D is significantly higher than other resistances and $R_{on,\,sp}$ could be approximated by R_D .

Figure 3.2. Cross section area of DIMOSFET

(After Munish Vashishath and Ashoke K. Chatterjee, Ref. [71])

The drift region analysis for an ideal DMOS structure can be performed by approximating the depletion layer in the drift region as an abrupt one-dimensional junction fabricated in a uniformly doped semiconductor. The doping level N_B (cm^{-3}) required to support a given break down voltage V_B and depletion width W (cm) at the breakdown can be calculated as follows [72] :

$$N_B = \epsilon \,.\, E_C^2 \,/ 2.q.\, V_B \qquad (3.2)$$

$W=2.V_B/ E_C$ (3.3)

The specific on-resistance ($\Omega.cm^2$) associated with drift region to support V_B is:

$R_{on, sp} = W /q. N_B . \mu_n$

$= 4 V_B^2 / \epsilon . E_C^3. \mu_n$ (3.4)

where ϵ is the permittivity (C/V cm) , E_C is the breakdown field (V/cm), q is the electronic charge (C), and μ_n is the electron mobility (cm^2/V.s).

3.2 3C-DIMOSFET using Gaussian profile in drift region:

This section includes the device structure of vertical DIMOSFET with Gaussian Profile in the drift region. Doping profiles used in semiconductor industry commercially usually have non-linearly graded profile inside semiconductor layers. These profiles usually adopt Gaussian or a Complementary Error Function distribution. The effective doping level of the Gaussian profile has been evaluated with the Gaussian peak being displaced towards the drain end of the device and the impurity concentration may be expected to fall to very small values near the n-drift region and p-body junction. This would also give a low parasitic series resistance near the drain and a large depletion region in the drift region near the junction .The overall doping level called the effective doping level (Neff) has been obtained by integrating the Gaussian profile within specified ranges of the depth into the semiconductor from source to drain of the MOSFET.

3.3 Effective Concentration (N_{eff}):

The drift region used here has a non uniform doping level, a Gaussian function with a peak values of N_0 near the drain decreasing upwards to very low values near the n-drift region and p-body junction.

The equation for Gaussian profile may be written as[73]

$$G(x) = N_0 e^{-\left(\frac{h-x}{m}\right)^2}$$

(3.5)

here N_0 is maximum concentration at drain end, m is constant, h is the device height and x is the distance from the junction as shown in figure 3.3.

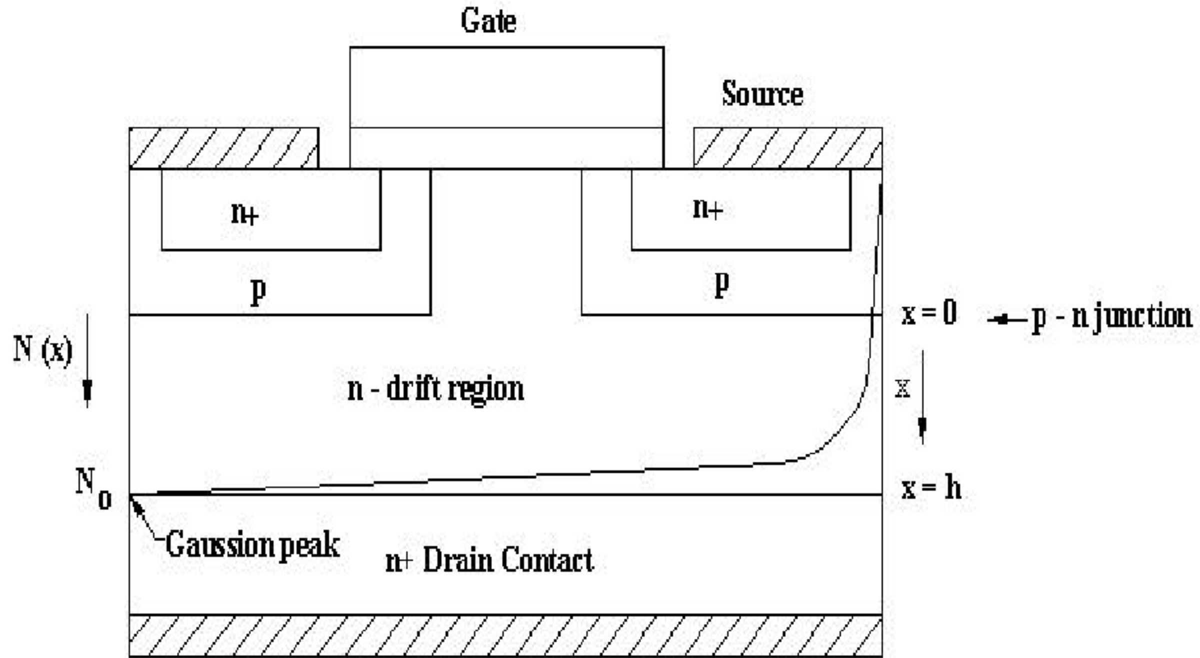

Figure 3.3 Cross-sectional structure of DIMOSFET showing Gaussian profile in the drift region (After Munish Vashishath , Ref.[73])

The carrier concentration N_{Total} in the device can be written down as[73]:

$$N_{Total} = \int^{h} G(x)Adx = \int^{x} N_0 e^{-\left(\frac{h-x}{m}\right)^2} Adx \, , \qquad (3.6)$$

where A is the cross-sectional area of the device.

Since the integral of a Gaussian function is an error function formulated as[73]:

$$\mathrm{erf}(x) = \frac{2}{\sqrt{\pi}} \int_0^h G(x)dx \qquad (3.7)$$

So, N_{Total} can be written as[73]:

$$N_{Total} = \frac{N_0 m A \sqrt{\pi}}{2} \mathrm{erf}\left(\frac{h}{m}\right) \qquad (3.8)$$

Hence, effective carrier concentration (**N_{eff}**) of the drift region per cc can be expressed as[73]:

$$N_{eff} = \frac{N_{Total}}{Ah} = \frac{N_0 m\sqrt{\pi}}{2h}\operatorname{erf}\left(\frac{h}{m}\right) \tag{3.9}$$

3.4 Depletion Region Width 'W'[73] :

The depletion region width at any given reverse voltage, V_R can be obtained by solving the Poisson's equation for the system. For the Gaussian function G(x) , the Poisson's equation becomes[73]:

$$-\frac{\partial^2 V}{\partial x^2} = \frac{e}{\varepsilon_s}G(x) = \frac{eN_0 e^{-\left(\frac{h-x}{m}\right)^2}}{\varepsilon_s} \tag{3.10}$$

where ε_s is the relative permittivity of the medium.

Integrating above eq. from 0 to x will give electric field E [73]:

$$E = -\frac{dV}{dx} = -\frac{\sqrt{\pi}eN_0 m}{2\varepsilon_s}\operatorname{erf}\left(\frac{h-x}{m}\right) + C\ , \tag{3.11}$$

where C is a constant of integration

Since at x=h, E=0 therefore C=0. So Eq.(3.12) then becomes,

$$E = -\frac{\sqrt{\pi}eN_0 m}{2\varepsilon_s}\operatorname{erf}\left(\frac{h-x}{m}\right) \tag{3.12}$$

The maximum field E_m occurs at x=0, giving [73]

$$E_m = -\frac{\sqrt{\pi}eN_0 m}{2\varepsilon_s}\operatorname{erf}\left(\frac{h}{m}\right)$$

Finally integrating eq.(3.12) again from 0 to x gives the potential V(x)[73]:

$$-V(x) = -\int_0^x \frac{\sqrt{\pi}eN_0 m}{2\varepsilon_s}\operatorname{erf}\left(\frac{h-x}{m}\right)dx \tag{3.13}$$

For $x \to h, \frac{(h-x)}{m} < 1$, the error function can be expressed as:

$$\mathrm{erf}\left(\frac{h-x}{m}\right) = \frac{2}{\sqrt{\pi}}\left[\left(\frac{h-x}{m}\right) - \frac{1}{3}\left(\frac{h-x}{m}\right)^3 + - - - - -\right]$$

Substituting above eq. in eq.(3.13) retaining the first two terms and integrating gives[73]

$$-V(x) = \frac{eN_0}{\varepsilon_s}\left[\frac{x^4}{12m^2} - \frac{hx^3}{3m^2} - \frac{x^2}{2}\left(1 - \frac{h^2}{m^2}\right)\right] \tag{3.14}$$

At x=W, the depletion region width under a reverse bias V_R is given as:

$V(W) = V_{bi} + V_R$

Where V_{bi} is the built in potential.

Substituting x=W and V(W)= $-V_R$ because $V_R >> V_{bi}$ in eq. (3.14) and simplification gives[73]:

$$\frac{W^4}{12m^2} - \frac{hW^3}{3m^2} - \frac{W^2}{2}\left(1 - \frac{h^2}{m^2}\right) - \frac{\varepsilon_s V_R}{eN_0} = 0 \tag{3.15}$$

Above eq. will be used to calculate the depletion region width W at a given reverse bias voltage V_R between the p-body and n-drift region of DIMOSFET.

3.5 Critical Electric field:

For the calculations of critical electric field, Gaussian profile distribution in drift region of DIMOSFET has been approximated as linearly graded profile distribution.

For linearly graded profile critical electric field is given as[74]:

$$E_c = (e\ \alpha\ W'^2 / 8\varepsilon_s) \qquad (3.16)$$

where ε_s is relative permittivity of medium, α is concentration gradient , W' is depletion width at breakdown.

Concentration gradient α was obtained by taking the difference of carrier concentrations at the source and drain end, then dividing it by device height h .

Depletion width at two breakdown voltages(punch through and avalanche) have been set equal to each other.

3.6 Punch through breakdown voltage V_{BPT} and Avalanche breakdown voltage V_{BAV} :

The maximum attainable depletion region width at highest value of reverse voltage V_R in eq.(3.15) for a given value of m gives the punch through voltage V_{BPT} .

The device height has been set at 200µm and 150µm for various values of m and doping level in the drift region. Analysis of equation (3.15) has been done in order to increase the voltage V_R to a value for which maximum depletion width does not go beyond the device height .That maximum value of reverse voltage is taken as Punch through Breakdown voltage V_{BPT}.

Avalanche Breakdown voltage V_{BAV} calculations have been done by approximating Gaussian profile as linearly graded profile in the drift region. For linearly graded profile avalanche breakdown voltage is given by[74]:

$$V_{BAV} = 2/3\ E_c W' \qquad (3.17)$$

here E_c is the critical field and W' is depletion width at breakdown.

CHAPTER 4
RESULTS AND DISCUSSION

Calculations of Punch through breakdown voltages (V_{BPT}) and Avalanche breakdown voltages(V_{BAV}) were made for three main Gaussian profiles with the following parameters whose details are quoted below:

Permittivity of free space $\varepsilon_0 = 8.854\times 10^{-14}(\Omega\text{cm})^{-1}$sec

Permittivity of 3C-SiC semiconductor $\varepsilon_s = 9.66\ \varepsilon_0$

Electronic charge e = 1.6×10^{-19} coulomb

Three Gaussian profiles are given as :

1. $N_0 = 0.67\times 10^{15}$/cc , m= 10^{-2}cm , Height h= 200×10^{-4} cm
2. $N_0 = 1.1\times 10^{15}$/cc,m=0.78×10^{-2}cm,Height h= 150×10^{-4} cm
3. $N_0 = 10^{16}$/cc , m= 1.496×10^{-2}cm , Height h= 200×10^{-4} cm

The Gaussian profiles that are given above are shown in figure 4.1 with peak concentration values N_0 as given above. Doping level is minimum near the source end and maximum at the drain end.

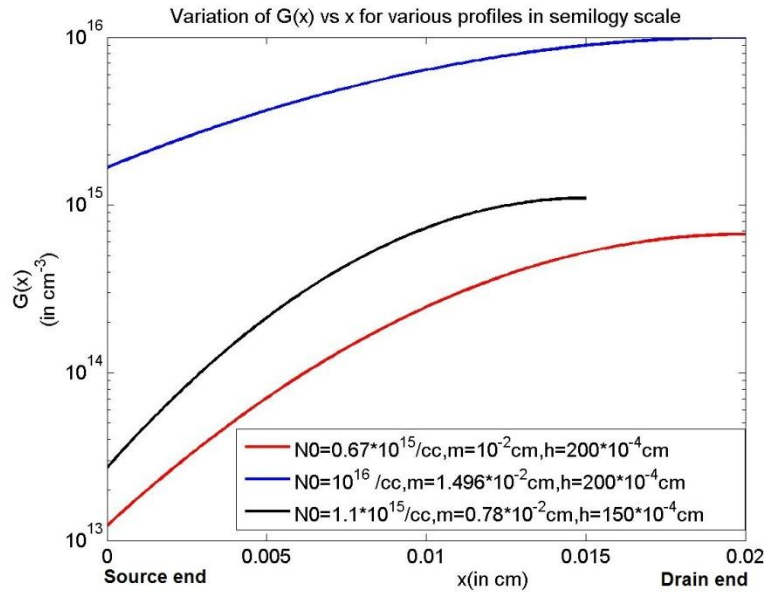

Figure 4.1 Variation of G(x) vs x for various profiles in semilogy scale.

For the first and third profiles, the drain to source distance or device height h has been set as 200µm. The profile number second utilises a device height of 150µm, as increasing the device height beyond this thickness leads to a decline in the avalanche breakdown voltage. Hence, a device thickness of 150µm has been found to be the ideal device height for this profile.

Calculation of depletion region width and reverse voltages for the first profile quoted above has been made and are shown in table 4.1. It has been found that the punch through breakdown voltage(V_{BPT}) of 25KV can be used for this profile with a device height of 200µm.The corresponding avalanche breakdown voltage was found to be 4.106 kV. For lesser value of device height as given by the depletion region width of say 188.258 µm, the V_{BAV} was found to be 3.6 kV. Hence the maximum device height that can be used for this profile is 200 µm for the maximum avalanche breakdown voltage of 4.106 kV. Similar results have been obtained for a device height of 200 µm for profile 3 that has given V_{BPT} of 25 kV and corresponding V_{BAV} as 6.84 kV.

Table 4.1 Results of depletion width and reverse voltage for profile1.

N0=0.67× 10^{15}/cc , m= 10^{-2}cm , h= 200× 10^{-4} cm

Reverse Voltage V_R(kV)	Depletion Width(μm)
25 (V_{BPT})	199.199
24	188.258
23	178.651
22	169.958
21	161.93
20	154.406
19	147.273
18	140.447
17	133.865
16	127.475
15	121.235
14	115.107
13	109.059
12	103.057
11	97.073
10	91.08
9	85.02
8	78.87
7	72.58
6	66.096
5	59.314
4	52.111
3	44.272
2	35.383
1	24.379

Table 4.2 Results of depletion width and reverse voltage for profile3.

N0=1.1$\times 10^{15}$/cc , m=0.78$\times 10^{-2}$cm , h= 150$\times 10^{-4}$ cm

Reverse Voltage(kV)	Depletion Width(μm)
19.6 (V_{BPT})	149.218
19	141.815
18	131.693
17	123.143
16	115.546
15	108.586
14	102.078
13	95.897
12	89.954
11	84.18
10	78.51
9	72.92
8	67.31
7	61.67
6	55.93
5	49.98
4	43.74
3	37.022
2	29.48
1	20.22

Table 4.3 Results of depletion width and reverse voltage for profile2.

N0= 10^{16}/cc , m= 1.496×10^{-2}cm , h= 200$\times 10^{-4}$ cm

Reverse Voltage(kV)	DEPLETION WIDTH(µm)
25 (V_{BPT})	101.687
24	92.475
23	86.832
22	82.25
21	78.24
20	74.58
19	71.17
18	67.94
17	64.83
16	61.93
15	58.90
14	56.02
13	53.17
12	50.34
11	47.50
10	44.65
9	41.78
8	38.83
7	35.81
6	32.68
5	29.39
4	25.88
3	22.05
2	17.67
1	12.22

Table 4.3 shows the calculation of depletion width and reverse voltage for this profile.
However , for second profile of device height of 150 μm, punch through breakdown voltage (V_{BPT}) is 19.6 kV corresponding to avalanche breakdown voltage (V_{BAV}) of 3.77 kV.

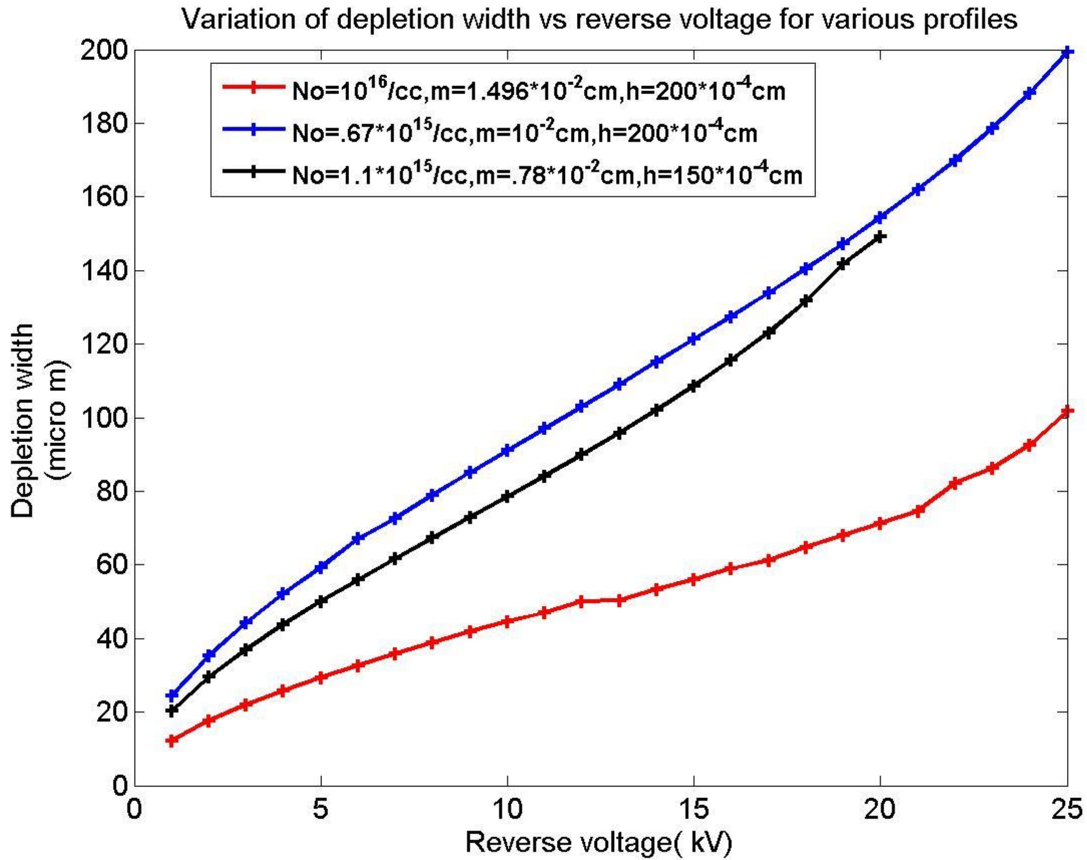

Figure 4.2 Variation of depletion width vs reverse voltage for various profiles.

It was also found that the critical field for breakdown was highest for profile 3 with the value of 10.09×10^5 V/cm, significantly less in profile 2 with 3.767×10^5 V/cm and least in the case of profile 1with the value of 3.08×10^5 V/cm.
The analysis of depletion width and reverse voltage for all three profiles is shown in figure 4.2. To a first approximation the relationship between the two can be considered as almost linear over the range of 0 to 25 kV of reverse voltages for a device height of 150 to 200 μm . A slight amount of non linearity seemed to exist in three profiles for reverse voltages lying between 0 to 5 kV and 20 to 25 kV. Analysis for the nature of this ambiguity is under way. Hence it is clear that

profile 3 with a device height of 200 μm, m=1.496$\times 10^{-2}$cm, N_0= 10^{16}/cc, α= 4.17$\times 10^{17}$ cm^{-4} provided the highest avalanche breakdown voltage of 6.84 kV corresponding to a punch through voltage of 25 kV.

Table 4.4 Results of breakdown voltages (V_{BPT} and V_{BAV}) for various profiles.

Profiles	Device Height (μm)	m (μm)	N_0 (cm^{-3})	α (cm^{-4})	E_C (V/cm)	V_{BPT} (kV)	V_{BAV} (kV)
1.	200	100	0.67$\times 10^{15}$	3.29$\times 10^{16}$	3.08$\times 10^{5}$	25	4.106
2.	150	78	1.1$\times 10^{15}$	7.16$\times 10^{16}$	3.767$\times 10^{5}$	19.6	3.767
3.	200	149.6	10^{16}	4.17$\times 10^{17}$	10.09$\times 10^{5}$	25	6.84

Analysis quoted above does give breakdown voltage of 6.84 kV for Gaussian profile in profile 3 but the design procedure does point to one disadvantage , that there is significant difference in the values of punch through breakdown voltage V_{BPT} and avalanche breakdown voltage V_{BAV} in all the profiles that have been studied.

CHAPTER 5
CONCLUSIONS AND FUTURE WORK

The equations for breakdown voltages for 3C-SiC Vertical DIMOSFET, using Gaussian function doping profile in drift region, were taken into account. Equations showed that the value of breakdown voltages depends on height (h) of drift region and doping level . For different values of height (h), constant(m) and doping level of drift region, breakdown voltages (Punch through and Avalanche) and its corresponding depletion region width were calculated and were given in table 4.4 . For the drift region height h=200μm, $N_0 = 10^{16}/cm^3$ and m= 1.496×10^{-2} cm, the punch through breakdown voltage was found to be 25kV and corresponding avalanche breakdown voltage was calculated as 6.84kV when Gaussian profile was approximated as linearly graded profile in drift region . It could be seen that avalanche breakdown will occur much before than punch through breakdown. More detailed analysis is required in the use of Gaussian profile in drift region that can yield almost equal values for punch through and avalanche breakdown voltages for 3C-SiC DIMOSFET. Having attained this, it would be advisable to analyses the theory for attaining breakdown voltages far in excess of the avalanche breakdown voltage of 6.84 kV obtained here. So that this can provide sufficient space for the design and development of the 3C-SiC DIMOSFET with Gaussian profile in drift region for the operation in the range of breakdown voltages approaching 10 kV or more.

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