Analysis of 4H Silicon Carbide Double Implanted MOSFET using Complementary Error Function Doping Profile in Drift Region for increased Breakdown Voltage and Low Power Dissipation

A Dissertation Submitted In Partial Fulfillment of the Required for the Degree of

MASTER OF TECHNOLOGY

IN

VLSI DESIGN

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DECLARATION

I hereby declare that the work which is being presented in the dissertation titled "Analysis of 4H Silicon Carbide Double Implanted MOSFET using Complementary Error Function Doping Profile in Drift Region for Increased Breakdown Voltage and Low Power Dissipation" in partial fulfillment of the requirement for the award of degree of Master of Technology in VLSI Design submitted in Electronics and Communication Engineering Department of Thapar University, Patiala is an authentic record of my study carried out under the guidance of Dr.A.K.Chatterjee (Professor, ECED) during 2014-2016.

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Acknowledgement

Though my research work has reaped expected results, it would be really unfair not to acknowledge the guidance and assistance I had received from many people towards the comple-tion of my thesis. As I delved deeper and deeper into the dynamics of Silicon Carbide(SiC), the analysis and calculations started becoming more complex, thankfully, because of inputs from many intellectuals I was able to find simpler solutions to those problems. First and foremost, I would like to express my heart-felt gratitude to my mentor and my guide Dr. A.K. Chatterjee for helping me throughout my work. He has been my inspiration from the very beginning and am lucky enough to have such an experienced faculty and a wonderful person as my guide.

I am also thankful to Dr. Sanjay Sharma, Professor and Head, Electronics and Communication Engineering Department, for providing me with the adequate infrastructure for carrying out the work and to Dr.Amit Kumar Kohli, P.G. Coordinator, Electronics and Communication Engineering Department, for the continuous support during the course of work. I would like to acknowledge all my friends especially Nickson P Jose, for the valuable discussions we had on SiC(which eventually helped me a lot with my calculations). Finally, I owe everything to my parents who have always been my constant source of encouragement and my sibling for their support throughout my work. Above all, thanks to the Almighty for His blessings.

I would like to conclude by saying that, the study, so far, has indeed helped me to explore dif-ferent avenues of Silicon Carbide and I am sure it will help me in my future research work. And as far as the thesis work is concerned, I have a positive feeling that my work, if acknowledged, might be a great help to the semiconductor power industry.

SAGAR

Abstract

The work carried out here on 4H-Silicon Carbide Double Implanted MOSFET(DIMOSFET) is to understand the performance of the above device related to Power Dissipation and Break-down Voltage for Complementary Error Function doping profile in the drift region. The doping profile which is used here can be obtained by mechanism like Molecular Beam Epitaxy(MBE). This profile helps to increase the breakdown voltage while at the same time reduces the series parasitic resistance at the lower end of the device thereby lowering the power dissipation, all of which has also been successfully observed in theoretical analysis here.

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List of Symbols

E_c	Critical electric field
W_j	Depth of p-body
I_{DS}	Drain current
N_{eff}	Effective carrier concentration
$_n$	Electron mobility
n_i	Intrinsic carrier concentration
L	Length of channel
$_e(\ _p)$	Lifetime of an electron(lifetime of a hole)
W_d	On-state depletion region width
C_{ox}	Oxide capacitance
v_{sat}	Saturated drift velocity of electron
m	Straggle value of Ion-Implantation
W_t	Total device height
W	Width of channel

List of Abbreviations

ACCUFET	Accumulation mode Field Effect Transistor
AlN	Aluminium Nitride
DIMOSFET	Double Implant Metal Oxide Semiconductor Field Effect Transistor
FET	Field Effect Transistor
GaN	Gallium Nitride
JFET	Junction Field Effect Transistor
MBE	Molecular Beam Epitaxy
MOS	Metal Oxide Semiconductor
MOSFET	Metal Oxide Semiconductor Field Effect Transistor
P_D	Power dissipation
$R_{on\ sp}$	Specific on-resistance
Si	Silicon
SiC	Silicon Carbide
UMOSFET	U - shape MOSFET
V_{BAV}	Avalanche breakdown voltage
V_{BPT}	Punch through breakdown voltage
V_T	Threshold voltage
WBG	Wide Band Gap
eV	electron Volt

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Chapter1

INTRODUCTION

1.1 Preamble

Recently in few years Silicon Carbide gained high attention as a potential material for high frequency and high power device applications. Its fine properties like large breakdown electric field, high saturated drift velocity, wide bandgap, small dielectric constant, high electron mo-bility and high thermal conductivity makes silicon carbide an attractive for fabrication of power devices with reduced die size and low power losses. The higher breakdown voltages in silicon carbide is about eight to ten times higher than silicon high voltage devices. The other properties such as high thermal conductivity and breakdown electric field ensures the integration of the devices made from SiC is possible woth smaller die size and higher densities.

The high thermal and chemical stability of SiC makes certain types of fabrications difficult. Diffusion co-efficients for dopant atoms are extremely low at temperatures typically used for silicon device processing and for this reason selective doping of SiC are accomplished by ion implantation. Implant activation typically requires annealing at temperatures between 1000 and 1700C. Chemical etching is impractical owing to the high chemical stability of SiC and selective etching is accomplished by reactive ion etching (RIE) using fluorinated gases.

The SiC lattice consists of alternating planes of silicon and carbon atoms, and the stacking sequence of these planes defines different polytypes of the material identified by the repeat distance of the stacking sequence (e.g. 3C, 4H and 6H). The lattice constant in the basal plane is virtually identical for all polytypes, but important electrical properties such as band gap energy, electron mobility and critical field differ significantly between the polytypes.

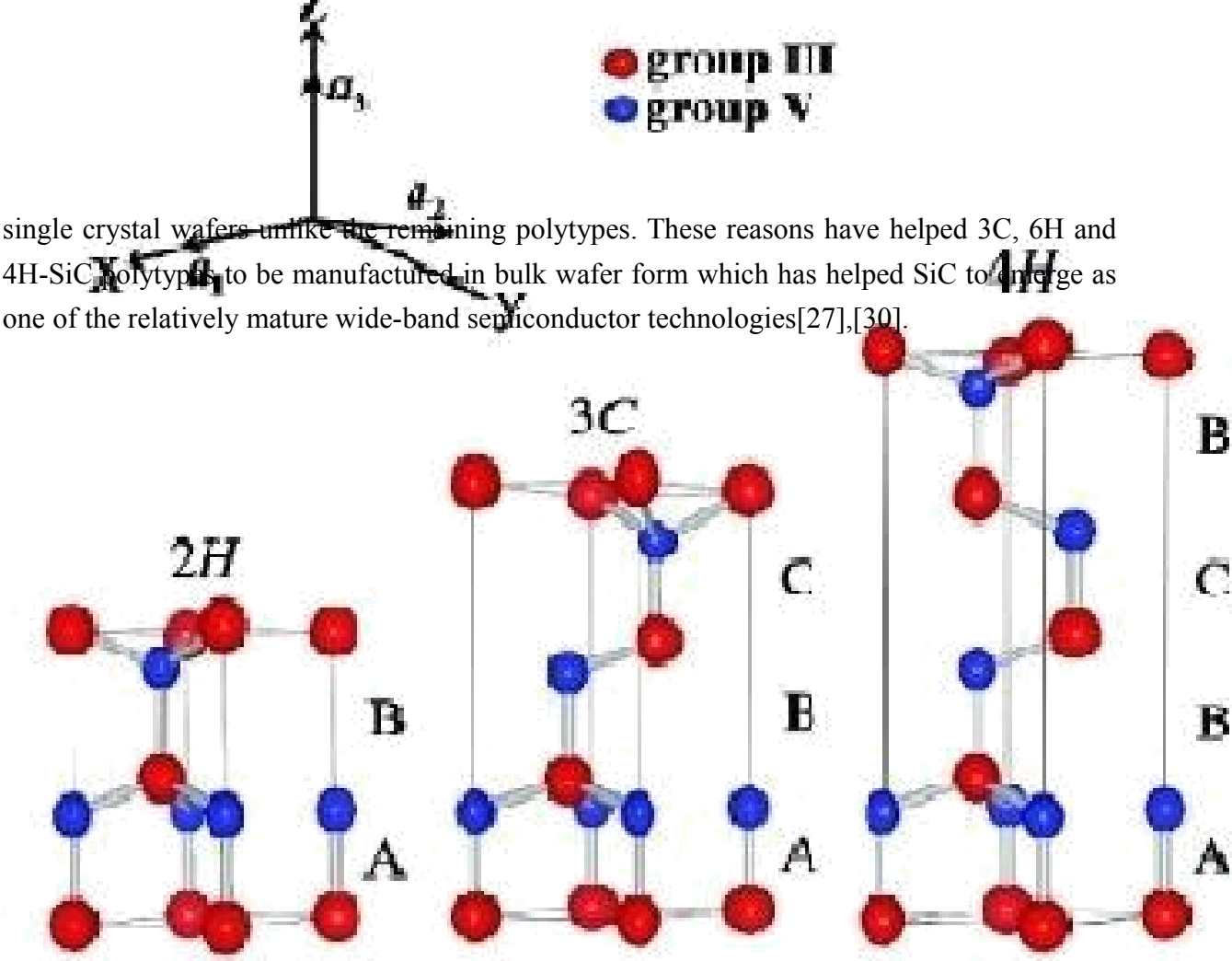
SiC offers significant advantages for power electronics applications such as lamp ballasts, motor control, medical electronics, automotive electronics, high-density high-frequency power supplies and smart-power application-specific integrated circuits. Hence, Silicon Carbide based MOSFET can be used in high power applications.

1.2 Polytypes of Silicon Carbide

Silicon is the material dominating the electronics industry today. Silicon Carbide (SiC), however, has superior properties for power devices as compared to Silicon. In recent years, activity in silicon carbide (SiC) device development has increased considerably due to the need for electronic devices capable of operation at high power levels and high temperature. The main strength of Silicon Carbide is that it can withstand high field strengths, it offers better heat- conducting capacity than copper at room temperature and it has a large energy band gap, which means that electrical components made from SiC continue functioning even when the mercury starts climbing. With very high thermal conductivity (5.0 W/cm), high saturated elec-tron drift velocity (2.7 10^7) and high breakdown electric field strength (3 MV/cm), SiC is a material of choice for high temperature, high voltage, high frequency and high power applica-tions.Polytypes refer to the different crystal/lattice structures of the same element. For Silicon Carbide there are nearly 200 polytypes which differ from each other only in their stacking se-quences(stacking sequence refer to how each layer of Silicon and Carbon are aligned/stacked over each other.).

In Figure-1.1, the stacking sequence is shown for the three commonly used polytypes of SiC, viz. 3C, 4H and 6H-SiC(devices based on only these three polytypes have been successfully developed so far). In 4H, if a layer is designated as A, then next layer is not centered above A due to tetrahedral configuration of Si, this layer is named B.The third layer is centered above A but is complemented, this layer is $\bar{A}$ and the fourth layer is not centered above A or B which appears as complemented thus, assigned C. Hence, the stacking sequence in 4H-SiC is AB$A\ C\bar{A}\ C$... as shown in Figure-1.1. On the similar lines, 6H-SiC has the stacking sequence as ABCB$A\ C\bar{A}\ C$... [30]. The change in the lattice structure affects the electrical properties a lot. Some of these differences are listed in Table-1.1.

Among those many polytypes of Silicon Carbide 3C, 4H and 6H-SiC electronic devices presently are the most widely experimented as they are readily available and due to high quality



single crystal wafers unlike the remaining polytypes. These reasons have helped 3C, 6H and 4H-SiC polytypes to be manufactured in bulk wafer form which has helped SiC to emerge as one of the relatively mature wide-band semiconductor technologies[27],[30].

Figure 1.1: Stacking sequence of the most common polytypes of SiC[30]

As per the discussions above, it has been proved that Silicon Carbide is indeed a better alter-native for Silicon in power device. However, there are many crucial issues like single crystal growth, device fabrication issues etc. that have to be looked upon before SiC can be accepted as a reliable material for semiconductor power industry[25]. Table 1.1 lists some electrical properties of the SiC polytypes and compares them with that of Si.

As seen in Table 1.1, the band gap of SiC is almost thrice of Silicon, mobility is comparable to that of Silicon(4H and 3C polytypes) while thermal conductivity is way higher than Silicon. Intrinsic concentration of SiC is almost negligible compared to Si. This lower value is due to higher band gap and this results in lower leakage as temperature rises, making it more favored material than silicon for high power applications.

Among the polytypes of Silicon Carbide, 4H and 6H-SiC electronic devices presently are

Table 1.1: Comparison of electronic properties among Si and different polytypes of SiC[30]

Parameters	Si	6H-SiC	4H-SiC	3C-SiC
Bandgap (eV)	1.1	3	3.26	2.2
Breakdown field @ 10^{17}cm ^{3}(MV/cm)	0.6	3.2	3	1.5
Electron mobility @ 10^{16}cm ^{3} (cm^{2}/V-s)	1100	370	800	750
Saturated electron drift velocity (cm/s)	10^{7}	2x10^{7}	2x10^{7}	2x10^{7}
Intrinsic concentration, n_i (cm ^{3})	1.5x10^{10}	2.3x10^{6}	8.2x10^{9}	6.92x10^{9}
Thermal conductivity (W/cm-K)	1.5	4.9	4.9	5

the most promising because of the availability and quality of reproducible single-crystal wafers. The availability of 6H-SiC and 4H-SiC polytypes in bulk wafer form has helped SiC to emerge as one of the relatively mature wide-band semiconductor technologies[31]. SiC is a material with immense potential for use in hetero structure electronic devices, which take advantage of differing band gaps, carrier mobilities etc. However, there are many crucial issues, crystal growth and device fabrication to name a few, that have to be addressed before SiC-based de-vices and circuits can be scaled up and reliably incorporated into electronic systems. The most important issue being controlled and repeatable doping in SiC device structures.

1.3 Power MOSFETs

Compared to their bipolar counterpart, MOSFETs are undoubtedly superior with faster switching time, high input impedance(which leads to a simpler driver circuitry), lower leak-age devices(as they are majority carrier device)[31]. MOSFETs are voltage-controlled device while a bipolar transistor is a current controlled device. The presence of majority carriers makes MOSFET a faster switching device than bipolar devices(BJTs), which is useful during hard switching. However, carrier mobility decreases with increase in temperature(due to impurity vibrations at higher temperature) which results in slower device at elevated temperatures. This makes MOSFET more resistive at higher temperatures but they are immune to thermal-runaway problem as experienced by bipolar devices. This property eliminates the need for additional heat sink circuitry requirements[27][30].

There is no doubt that power switches are the heart of all power electronic systems. Many reasons have made power electronic systems affordable in large number of applications; the increased power capabilities, ease of control and reduced costs of power switches to name a few. Thyristors and bipolar transistors were the first power switches. Until the late 1970s, the rating of these devices grew steadily. It was around this time that the first power MOSFET was introduced. Since then, power MOSFETs based on silicon have drastically improved and become the dominant device technology since 1980s for many applications(and is continuing so till now). The reasons why MOSFETs are preferred over their bipolar counterparts are[22][30]:

MOSFETs have relatively simpler gate drive circuitry due to high input impedance. As the input impedance is high, just simple integrated circuits can be used to control the drive of gate as it requires very low gate current.

MOSFETs possess higher switching speeds than bipolars as they are majority carrier device. This absence of minority charge carriers also lead to low leakage at higher temperature for power devices.

MOSFETS have better ruggedness and safe operating forward biased area, which eliminates the need of protective snubber circuits during hard switching, unlike bipolar transistors.

As the resistivity of majority carriers increases with temperature, the thermal runaway behavior is avoided in MOSFETs, which eliminates the need for additional heat sinking circuitry.

1.4 Device structure and analysis of 4H-SiC DIMOSFET

A power MOSFET is a voltage driven device whose gate terminal is electrically isolated from its Silicon Carbide body by a thin layer of silicon dioxide (SiO_2). Due to very few minority charge carriers the speed of operation of MOSFET is higher. DIMOS(Double Implant MOS) transistors are common in silicon power device technology where the p-base and n^+ source regions are formed by diffusion of impurities through a common mask opening. However, owning to very low diffusion constant for SiC, impurity diffusion is impractical, the favored doping technique is ion implantation.

The first attempt in doping SiC using ion implantation was done by Purdue group. The implantation required two separate masks for doping p-base and n^+ regions respectively, as shown

in Figure-1.2, this is the reason for the nomenclature Double Implant. The device fabrication is started with an n-type epitaxial layer grown on a heavily doped n^+ substrate. The channel is formed by the difference in lateral extension of the p-base and n^+ source regions produced by their diffusion cycles. Both regions are self-aligned to the left-hand-side and right hand- side of the gate region during ion-implantation to introduce the respective dopants.

Without the application of a gate bias, a high voltage can be supported in the DIMOS structure when a positive bias is applied to the drain. In this case, a reverse bias junction is formed between the p-base and the n-drift region. Drain current that flows in the DIMOSFET structure is induced by the application of a positive bias to the gate electrode. This produces an inversion layer at the surface of the p-base region under the gate electrode. This inversion layer channel provides a path for transport of electrons from the source to the drain. After transport from the source region through the channel, the electrons enter the n-drift region at the upper surface of the device structure. They are then transported through a relatively narrow JFET region located between the adjacent p-base regions within the DIMOSFET structure. After being transported through the JFET region, the electrons enter the n-drift region. The current spreads from the relatively narrow JFET region to the entire width of the cell cross-section. This non-uniform current distribution within the drift region enhances it's resistance making the internal resistance of the DIMOSFET structure larger than the ideal specific on-resistance of the drift region[23].

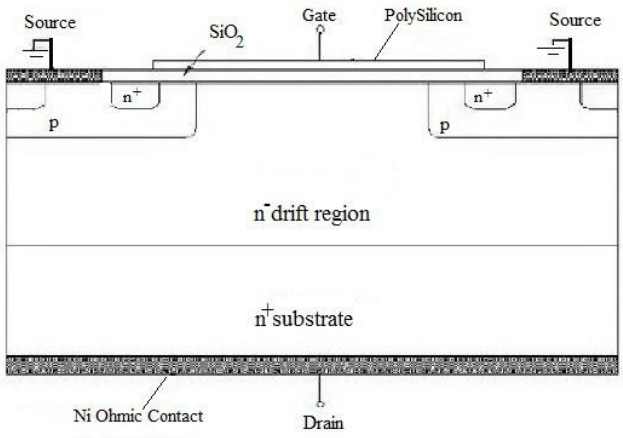


Figure 1.2: Structure of DIMOSFET[29],[30]

1.4.1 Forward Conduction Characteristics

The current flow in DIMOSFET can be understood by analyzing the device structure.Unlike

planar structure, DIMOSFETs are vertical structures with source terminal located at the top and drain terminal at the bottom.The vertical structure also enhances the current flowing along the device.The channel formation(between the n^+ source and the p-body) is due to the potential applied at the gate terminal.The channel is formed in the gap between p-base and n^+ diffusion regions.The current flow in the power DIMOSFET during forward conduction is limited by the total resistance between the source and drain.The resistance is limited and comprise of many components. These several components are as shown in Fig.1.3.Here, R_{n+} is the contribution from n^+ source diffusion region, R_C is the channel resistance, R_A is the accumulation layer resistance, R_D is the drift region resistance, R_S is the substrate resistance and the portion of the drift region that comes to the upper surface between cells that contribute R_J that is enhanced at a higher drain voltage due to pinch-off action of depletion layer extending from the p-base regions due JFET action.

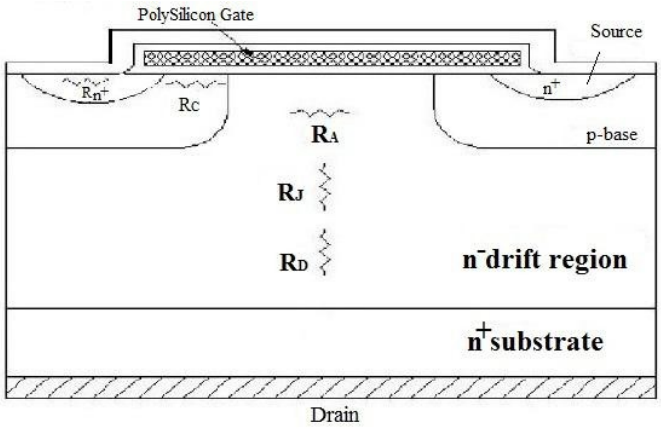


Figure 1.3: On-state resistance distribution in DIMOSFET[29],[33].

The on-resistance of the device is the total resistance between the source and drain terminals in the on-state [23],[30],[32].This parameter is responsible for the current rating of the device and consequently the power dissipation. The cell structure with each component of the specific on-resistance ($R_{on\ sp}$) is as shown in Figure-1.3.The application of positive gate bias results in a current flow between drain and source through the n-drift region and conductive channel. The conductivity of the channel is modulated by the gate bias voltage and the current flow is determined by the resistance of various resistive components as shown in Figure-1.3. The total specific on-resistance ($R_{on\ sp}$) is determined as[29],[30]:

$$R_{on\ sp} = R_{n+} + R_C + R_A + R_D + R_J : : : (1:1)$$

Under lower breakdown voltages, all the resistances come into picture while at higher break-downs the drift region resistance (R_D) dominates.

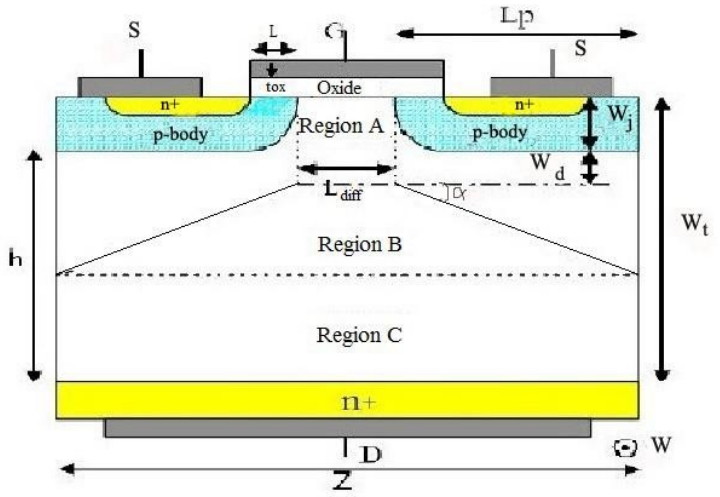


Figure 1.4: Cross section of DIMOSFET[30].

In a power MOSFET, the blocking voltage is supported across the drift layer, and thus the drift region resistance is considered to be the minimum possible theoretical limit for the on-resistance of a MOSFET. For an ideal DIMOSFET, the resistances associated with the n^+ source, the n-channel, the accumulation region and the n^+ substrate are assumed to be negligible and the specific on-resistance of the power MOSFET is determined by the drift region only. This assumption is not accurate at lower breakdown voltages where the drift region resistance R_D is comparable to the other resistive components and these resistances should be included in calculating $R_{on\ sp}$. However, at higher breakdown voltages, R_D is significantly higher than other resistances and $R_{on\ sp}$ can be approximated to R_D [30].

Fig.1.4 depicts the direction of current flow in the power MOSFET. The mathematical formulas pertaining to various resistance values is given as follows. If the linear cell is considered with 1-cm extension perpendicular to the cross section as shown in Figure-1.3, the resistance per square centimeter due to the n^+ region is given by[30]:

$$R_{n+} = 1=2\ _{ON}\, L_E(L_G + 2m) : : : (1:2)$$

where, $_{ON}$ is the sheet resistance of n+ diffusion and parameters L_E and L_G are the emitter and gate lengths respectively, 2m is the cell diffusion window. The channel resistance per square

centimeter for the linear cell is given by [25],[30]:

$$R_C = \frac{1=2L(L_G + 2m)}{(\ _nC_{ox}(V_G \quad V_T))} \ldots (1{:}3)$$

The resistance of the accumulation layer R_A determines the current spreading from the chan-nel into drift region. The accumulation layer resistance is dependent on the charge in the accu-mulation layer and the mobility for free carriers at the accumulated surface. For the linear cell geometry, the accumulation layer resistance per square centimeter is [25],[30]:

$$R_A = \frac{K(L_G + 2m)(L_G \quad 2x_p)}{(\ _nC_{ox}(V_G \quad V_T))} \ldots (1{:}4)$$

where, K is a factor introduced to account for the two dimensional nature of the current flow from the accumulation layer into the bulk. The resistance of drift region between the p-base diffusion can be calculated if the voltage drop along the vertical direction is neglected. Under the assumption that the depletion layer width of the p-base-n-drift layer junction is negligibly small and the current is flowing uniformly down from the accumulation layer into the JFET region. The resistance of the JFET region can be analyzed as a resistance with increasing cross section when proceeding downward from the surface and is calculated by[25],[30]:

$$R_J = 2\ _D(L_G + 2m)[\ \frac{1}{\sqrt{\quad}} \tan^{I}(0{:}414) \sqrt{\frac{(L_G + 2x_p)}{(L_G \quad 2x_p)}} \ ] \ldots (1{:}5)$$

where, $_D$ is the resistivity of the drift region. For the current spreading at an angle as shown in Figure-1.3, the drift region resistance per square centimeter is given by [30]:

$$R_D = \ _D \frac{(L_G + 2m)}{} \ln[1 + 2(h{=}a) \tan\ _I] \ldots (1{:}6) \tan$$

where, dimensions h and are indicated in Figure-1.3.

A good approximation for $_I$ in theory is provided by[29],[30]:

$$_I = 28^o \qquad (h{=}a) \ if \ h \qquad a \ldots (1{:}7)$$

$$_I = 28^o \qquad (a{=}h) \ if \ h \qquad a \ldots (1{:}8)$$

Finally, the equation for power dissipation for 50% duty cycle can be evaluated from the equation given as[18]:

$$P_D = \frac{1}{2}((J_{ON})^2 AR_{on} + J_L A V_B) \quad (1.9)$$

where, J_{ON} is the on-state current density, J_L is the leakage current density, V_B is the breakdown voltage and A is the cross-sectional area of the device. The leakage current density (J_L) is given as[18]:

$$J_L = \frac{en_i W}{\tau_e} + e\left(\frac{D_h}{\tau_h}\right)\frac{n_i^2}{N_d} \quad (1.10)$$

where, n_i is the intrinsic carrier concentration (cm^{-3}), W is the width of the space-charge region (cm), τ_e is the lifetime of electrons in the space-charge region (s), N_D is the concentration of donor atoms (cm^{-3}), D_h is the diffusion constant of holes in the n-type region (cm^2/s) and τ_h is the lifetime of holes(s). Thus, the equations from eq.(1.1) to eq.(1.10) describes all the equations required for theoretical analysis.

1.5 Motivation

Silicon MOSFETs are already the dominant technology in simpler low power, high switching electronic devices. However, the relative lower breakdown field strength of Silicon limits their usage in applications required to operate at higher temperatures (500^o and above).The advantages of SiC material properties, in particular breakdown field, makes SiC MOSFETs a very promising candidate for fast switching devices required at higher temperature.SiC has much lesser power dissipation at higher temperatures than Silicon due to less specific on-resistance(which is almost 100-200 times less).Lower thermal minority carrier generation implies lower leakage currents and device operation at higher temperatures,arising from self heat-ing due to power dissipation is more tolerable. Moreover, the thermal conductivity of SiC is three times higher than Si which eliminates the need for additional circuits for heat sinking purpose.

1.6 Scope and Objectives

Scope:

Due to excellent physical and electrical properties such as high breakdown electric field, wide band gap, high thermal conductivity and high electron saturation velocity, silicon carbide offers great potential for development of high temperature, high power and high voltage devices. Significant progress in SiC power MOSFETs have been demonstrated with the fabrication of UMOS, DIMOSFET(Double Implant MOSFET), triple implanted vertical MOSFET and accu-mulation mode MOSFET (ACCUFETs)

Objective:

The objective of this thesis work is to analyze one of the poly types of SiC (4H-SiC) for higher breakdown voltage and lower specification on-resistance (and consequently lower power dissi-pation).The profile considered for the drift region is a distorted Gaussian profile.The objectives are summarized as:

Study and Analysis of Double Implanted MOSFET on 4H-SiC wafer.

Analysis and Design of Double Implanted MOSFET with optimum power dissipation for large breakdown voltages.

Analysis and Design of 4H-DIMOSFET with Gaussian doping profile of the drift region

.

1.7 Organization of the Report

In this report, the Chapter 1 is an introduction to Silicon Carbide (SiC) material and the working of the device(DIMOSFET). Recent advancements in this field is discussed.A brief dis-cussion on different polytypes of SiC and and on why only 4H, 6H and 3C polytypes are con-sidered in power devices is included.SiC is superior to Silicon(Si) due to properties like higher critical electric field, wider band gap, higher thermal conductivity to name few. A comparison table is drawn to indicate the differences among different polytypes of SiC and comparing it against Si. The device under consideration is DIMOSFET,which unlike the planar MOSFET devices is a vertical device. Vertical devices have the source and drain terminals located at the top and bottom respectively. This arrangement ensure higher current flow along the device height.

Chapter 2 covers the reviews of literature that were used as reference during the research work in chronological order. The first MOSFET came up in 1970s and power MOSFETs based on silicon has been the dominant technology since 1980s. Many of the works carried out on SiC

power devices have been implemented using uniformly doped or linearly graded profile. There has been almost no reference to any work wherein non-linear doping profile has been used. All the limitations and advancements over the years has been mentioned in detail in this chapter.

Chapter 3 covers a comparative study between the two widely used doping profiles in power industries for power MOSFETs namely, uniformly doped profile and linearly graded profile. Results from previous work based on uniformly doped profile and linear one have been com-pared against each other. A linearly graded profile gives smaller device height than a uniform doped one for the same breakdown voltage. There is a limit to the breakdown voltage that can be achieved using uniform doping profile and there exists a trade-off between power dissipation and breakdown voltage in such profiles. A non-linear profile, like Gaussian and complementary error, overcomes this trade-off by the virtue of their non-linearity.

This is followed by Chapter 4 which carries the analysis of the distorted Gaussian doping profile. The distorted Gaussian profile (a more practical non-linear doping profile) is approx-imated by a dual-slope linearly graded profile. The analysis includes calculation of effective carrier concentration in the drift region(N_{eff}), channel voltages. The critical field and the break-down voltages, avalanche breakdown and punch through breakdown voltage, is then derived for the above profile in this chapter. This is followed by the required calculations and the respec-tive plots. The various plots includes current density versus power dissipation, current density versus on-state depletion width for different peak carrier concentration, current density versus drain-source voltage, effective carrier concentration versus concentration gradient, avalanche breakdown voltage versus critical electric field, avalanche breakdown voltage versus device height, avalanche breakdown voltage versus punch through breakdown voltage and on-state de-pletion width versus specific on-resistance. The chapter is concluded by a comparison between uniformly doping profile and distorted Gaussian profile. Finally, all the discussion of the results based on plots and tables in the work is discussed in Chapter 5. This chapter also contains the future scope of the work. All the references used in the work are enlisted in the final chapter.

Chapter2

LITERATURE REVIEW

The rise of Silicon Carbide was in the late 1980s, when it was observed that power devices based on Silicon were reaching it's theoretical limits and that limit could be extended significantly by using material with higher breakdown field[3]. However, it was only in 1994 that the MOS characteristics of silicon carbide was explained in a paper by Brown et al[5]. This paper also came up with an explanation characterizing the SiC/SiO_2 interface states which was due to rejection of n-type dopants and incorporation of p-type dopants into oxide during growth. However, both Si and SiC showed the same impurity redistribution during the thermal oxida-tion. It was in late 1980s that the first SiC based MOSFET was designed but the first SiC based power MOSFET came up only in 1994 which were basically vertically trenched MOSFET or UMOSFET[6]. But UMOSFETs had two major issues[7-8]:

Due to U shape of the trenches, at the corners fringing of field happened leading to failure of gate oxide at higher drain voltages thereby limiting the breakdown voltage much lower than the theoretical value.

Lower specific on-resistance (hence higher power dissipation) due to low inversion layer mobility of carriers along the trench sidewalls.

In 1994, silicon carbide MOS characteristics were explained in a paper by Brown et al [18]. This paper produced data which characterized the SiC/SiO2 interface and explains one of the previously unexplained abnormalities observed in the characteristics of SiC MOSFETs. The outstanding distinction between the MOS characteristics on p and n type SiC wafers obviously indicates that the difference is probably caused by the fact that the p type wafers are Al doped and the n type wafers are N doped. The redistribution of impurities that occurs during the thermal oxidation of SiC and Si behaves in a similar fashion. N type dopants are rejected by

the oxide during growth whereas p type dopants are incorporated into the oxide. Hence, the Al dopant in the oxide is likely to be the causes of the p type SiO2/SiC interface characteristics.

The first MOSFETs in SiC were reported in the late 1980s and the first power MOSFETs in 1994 [25]. The power devices were the vertical-trench MOSFETs or UMOSFETs. UMOSFETs are attractive because the base and source regions are formed epitaxially without the need for ion implantation and associated high temperature annealing. In UMOSFETs, the MOS channel is formed on the sidewalls of trenches created by RIE. However, SiC UMOSFETs were re-ported to have two serious problems: (i) A high electric field occurs in the gate oxide caused by higher electric fields in the SiC drift region. This problem occurs at the trench corners leading to catastrophic failure of the gate oxide at higher drain voltages, thus restricting the maximum operating voltage to less than 40 percentage of ideal breakdown voltage, and (ii) The low in-version layer mobility along the trench sidewalls results in high specific on-resistance, which nullifies the advantage of lightly doped drift region in SiC. By 1995, UMOSFETs fabricated on the carbon face of SiC had achieved the breakdown voltage of about 260V.

In 1995, a SiC U-MOSFET with maximum breakdown voltage of only 260V was designed. B.Jayant Baliga in his journal[9] described the applications of different SiC devices that were commercially available in the year 1996.More and more testing and fabrication of many SiC MOSFETs started in the years that followed. Year 1998 saw the mention of 4H-SiC UMOS-FETs and DIMOSFETs with measured blocking voltages of 1400 V and 900 V respectively in [10]. The paper also highlighted carrier mobility, high interface state density, the difficulties of forming high quality oxide on the sidewalls of the vertical trenches(for UMOSFETs). An year later(in 1999), the numerical and theoretical analysis of 6.5kV SiC based JFET and MOSFET came up[11].The same year elucidated the usefulness of Silicon Carbide in device applications. For the above said device, the n-doped drift region was 60 m long with 2 10^{15}cc doping con-centration and the gate and source diffusion were 0.6 m apart. The gate oxide thickness was 0.2 m for the simulated structure. All the simulations and optimizations of the above device structure were done in MEDICI simulator. The different MOSFET parameters like density of interface states, intrinsic mobility reduction factor, inversion layer mobility etc. were studied and examined in depth for 6H SiC enhancement mode n channel MOSFET[12]. It was found that with increase in substrate doping concentration, there was a reduction in inversion layer mo-bility. There was an analogy to silicon devices with regard to dependencies of inversion layer on substrate doping. However, these dependencies are modified by high concentration of interface states near the edge of conduction band. The concept of interface states was described in detail in[13] including the effect of these states on the carrier mobility for 4H and 6H-SiC.This study

was necessary to understand why carrier mobility decreases for 4H and 6H-SiC and not for 3C-SiC.The same year J.Wang et al in his paper[14] came up with a trade-off between break-down voltage and drift region on-resistance and evaluated the high blocking capacity of 4H-SiC DIMOSFET while compromising for low on resistance.

The year 2000 saw the characterization of Silicon Carbide epitaxial channel MOSFETs. These MOSFETs were fabricated on 6H SiC substrates with n+ epitaxial source and drain terminals. Under 50% channel donor impurity concentration, a buried channel mobility of 230 cm^2/V-s and accumulation channel mobility of 45 cm^2/V-s were extracted[16]. The fu-ture of SiC switching devices was discussed in[18]. In the same year, for the first time,N_2O grown oxide on both n and p-type 6H SiC wafers was successfully demonstrated and fabri-cated. This N_2O grown oxide showed better oxide qualities and improved SiC/SiO^2 interface characteristics. This N_2O oxidation technique showed highly reliable and improved quality SiC MOSFETs. In the following year 4H-SiC RF MOSFET was fabricated for the first time. The enhanced performance of this device was due to two-metal layer process which optimized the complementing requirements of acceptable value of inversion- layer mobility and low contact resistance. The enhanced performance included a breakdown voltage of 950V attained in MOS-FET with specific on-resistance of 24Ω-mm^2. Electron mobility model for three of the main SiC poly types, namely 3C, 4H and 6H were developed.

A. Mihaila et al in the paper[17] presented a systematic analysis of breakdown mechanisms in silicon carbide MOSFET and JFET. Trench technology was used for the MOSFET and the devices designed for 1.2kV were simulated and optimized using MEDICI and ISE TCAD soft-ware packages. However many drawbacks in SiC trench MOSFET (like gate oxide breakdown, low channel mobility and the tight trade-off between the punch-through premature breakdown and the threshold voltage in the channel) were eliminated by using the SiC JFET. In the years that followed many developments took place in SiC MOSFETs. Specific behaviour of interface states were measured which indicated that at 0.1eV below the conduction band the interface state density decreased from 2 10^{13} to 2 10^{12} eV^{1} cm^{2} following annealing in N_2O for 2hours[19].A 2D drift-diffusion based simulator was designed for SiC in the same paper. Even by this time fabricating SiC devices had their limitations which included material quality, ion implantation, the SiC-Si_2 interface and the thermal stability of contacting systems which called for further work[20]. Evaluations were done for SiC based Schottky and PIN diodes against their Silicon counterparts.

In the year 2002, a breakdown of only 760V have been attained from 6H- DIMOSFET devices [21].Pyrogenic re-oxidation, as discussed in[13], could reduce the specific on-resistance and thereby significantly reduce the power dissipation along the device. In the same year,an analytical model of a SiC MOSFET came up in[23]. In this paper, a semi-empirical relation for carrier mobility dependency on dopant concentration, electric field intensity and temperature was formulated which was based on experimental results. Based on this dependencies, apt analytical-physical model of V-I characteristics, trans-conductance and conductance were developed. These proposed models led to the design of a simulation algorithm which then was used to simulate the MOSFET performance. In the same year, the first SiC MOSFET with breakdown in kV range was demonstrated - a 10A, 2.4kV 4H SiC DIMOSFET. This MOSFET, at room temperature, showed a peak channel mobility of 22 cm^2/V-s,a threshold voltage of 8.5V and exhibited a specific on-resistance of 42 mΩ-cm^2. At a temperature of 200degC increased to a value of 85 mΩ-cm^2. However, a stable value for avalanche breakdown of 2.4kV was observed. The MOS channel length, in the paper, as defined by the p-well and n-implant was 1.5 m. In this vertical device, the charge carriers flow laterally from the n-source through the channel on the implanted p-well and then vertically through the drift region which is spread at an angle. The device dimensions chosen for a breakdown of 2kV was a 20 m thick drift region with a doping concentration of 2:5 10^{13} cc. Apart from all the above specifications, the paper also pointed out that these devices were capable of high breakdown, low loss switching and high frequency applications.

One of the main reasons why SiC based devices have found their place in power industry is because of their higher breakdown voltage than Si. To extend its viability in high power applications, its required to enhance the breakdown voltage. Numerical device simulations on 4H-SiC vertical MOSFETs were presented in [24-25]. Reverse blocking voltage, onresistance and threshold voltage were the main focus in these simulations. The simulated model had a gate oxide thickness of 50nm, p-well depth as well as channel length of micron and a source depth of 0.2 m. As shown in [26], breakdown of 910V could be attained from one-step field plate termination and 1100V from the embedded mesa with step field plating. Reliability and performance became the next concern for SiC devices.

In the paper[27], the same were studied for advanced power applications. All these years, the analysis and models were developed for uniformly and linearly doped profiles only. First theoretical analysis to consider non-linear doping profiles on 6H-SiC DIMOSFET (like Gaussian, complementary error profile) appeared in [29-30]in the year 2008. The advantage these non-

linear profiles seemed to have over uniformly doped and linearly graded profile was that it could give higher breakdown while keeping lower values for parasitic resistances. The profile had a very low value of impurity concentration near the p-well and n-drift region while a higher concentration at the lower end of the device. However, practical implementation of such a structure is yet to be seen. In paper[30], the power dissipation for the linearly graded profile evaluated at a current density of 1000 A/cm^2 was found to be minimum, whereas a maximum breakdown voltage of 20kV was found for the Complementary Error Function profile. Device structure of a 6H-SiC vertical Double-Implanted MOSFET (DIMOSFET) to provide a high breakdown voltage of about 10 kV and a low power dissipation for a rise in device temperature of 600 ^oC was studied in[29].For the same temperature, the device showed optimum doping levels of the drift region lying between 5 $10^{13} cm^{-3}$ and 5 $10^{15} cm^{-3}$ for a breakdown voltage of 10 kV.

The recent years saw a major leap in the SiC device technology with a recently(year 2014) developed 2nd generation, large-area (56 mm^2 with an active conducting area of 40 mm^2) 4H-SiC DMOSFET, which reliably blocked 1600 V with very low leakage current under a gate-bias (VG) of 0 V at temperatures up to 200. The device also exhibited a low on-resistance ($R_{on\ sp}$) of 12.4 mΩ at 150 A and VG of 20 V. DC and dynamic switching characteristics of the SiC DMOSFET were also compared with a commercially available 1200 V/ 200A rated Si trench gate IGBT[33].This paper also presented a comprehensive study on intrinsic reliability of this 2nd generation SiC MOSFET to build consumer confidence and to achieve broad market adoption of power switch technology. In another paper[34] to obtain widespread usage in SiC DMOSFETs, their long-term operational ability to handle the stressful transient current and high temperatures common in power electronics were further verified. The long-term reliability of a single 4H-SiC DMOSFET, the effects of extreme high current density were evaluated. The 4H-SiC DMOSFET, which was studied, had an active conducting area of 40 mm^2, and ratings of 1200 V and 150 A. The device was electrically stressed by hard switching transient currents in excess of four times the given rating (600A) corresponding to a current density of 1500 A/cm^2. Periodically throughout testing, several device characteristics including $R_{on\ sp}$and $V_{GS(th)}$ were measured. The hard switching was done 500000 times, the first 16000 switching cycles were done under the temperature range varying from 25^oC to 100^oC. For each slot, the device performance was monitored and analyzed over the given temperature range. The results showed SiC DMOSFET had robust long-term reliability in high-power applications that are susceptible to pulse over currents, such as pulsed power modulators and hard-switched power electronics.

Chapter3

STUDY ON UNIFORMLY DOPED PROFILES

3.1 Introduction

This chapter analyzes the basic doping profile for the drift region- uniformly doped profile respectively. The entire behavior of DIMOSFET(like other MOSFETs) revolve around the characteristics of p-n junction, which in this case is formed between the p-well and the n drift region. Due to the lower doping concentration at the drift region, the depletion region width extends entirely into the drift region and this charge free region sustains the reverse breakdown voltage for which the device is designed.

Here the analysis is made for a breakdown voltage as well as the power dissipation. A comparative discussion is done based on results present in [29]. As mentioned above, the base of device design is dependent on depletion width that extends into the lightly doped drift region which in turn is used to estimate the drift region thickness.

3.2 Vertical DIMOSFET with Uniformly Doped Profile

This type of profile has a uniformly doped concentration in the drift region(Region C) as shown in Fig.1.4. This is a special case of abrupt p-n junction when $N_D << N_A$, where N_A is the acceptor concentration of the p-body and N_D is the donor concentration of the drift region. The main objective to reduce the magnitude of $R_{on\ sp}$ is to reduce the power dissipation, P_D across the vertical DIMOSFET, since[9]:

$$P_D \quad J_{on}^{2} R_{on\ sp} A : : : (3:1)$$

where J_{on} is the on-state current density and A is the cross-sectional area of the vertical device. Fig.3.1 illustrates the uniformly doped profile in the drift region of DIMOSFET. The peak doping concentration, N_o is constant and is same as N_{eff} for uniformly doped profile.

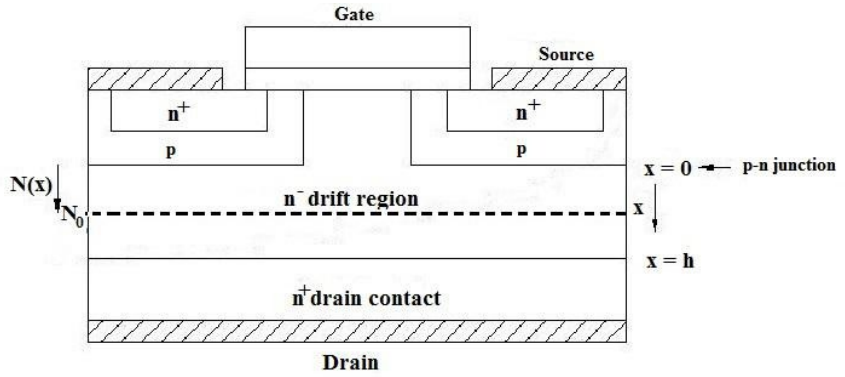


Figure 3.1: Uniformly Doped Profile for DIMOSFET

3.3 Discussion of results

Based on the results stated in [29], a device height of 73 m gave a V_{BAV} (Avalanche Breakdown Voltage)of 6.4kV and $V_{BP\,T}$ (Punch through Breakdown Voltage) of 5kV. But a linear doping profile gave V_{BAV} equal to 6.74kV and $V_{BP\,T}$ of 6.75kV for value of 1.58 10^{18}cm ^{4} and device height of 65 m. For a device design both the above voltages ($V_{BP\,T}$ and V_{BAV}) are needed to be made equal to each other, however in the calculations in [29] the lower of the two voltages is considered as the breakdown voltage of the device. Thus, the former with uniformly doped profile had a breakdown voltage, $V_{BP\,T}$, of 5kV while the latter with, V_{BAV} , equal to 6.74kV. At h=82 m, using linear graded profile a maximum breakdown of 8.75kV was achieved though designed for 10kV.

Chapter4

ANALYSIS AND DESIGN OF 4H-DIMOSFET USING COMPLEMENTARY ERROR DOPING PROFILE

4.1 Introduction

This chapter analyzes structure of 4H-SiC DIMOSFET using Complementary Error Func-tion doped profile in the drift region of the device. The device dimensions were determined by different parameters like the drift region doping level, blocking voltage, depletion region width, specific on-resistance and power dissipation. In the analysis carried out here, the device height was decided by iterations over the effective carrier concentration(N_{eff}). The slope of the profile(concentration gradient) was kept more steep along the lower end of the device to ensure lower values of parasitic resistances.Low doping (10^{12} 10^{13} per cc)near the source end ensured higher breakdown for the device. The final effective carrier concentration (N_{eff})was obtained by iterations and the device height was calculated for each iteration based on N_{eff} value from the previous iteration. Separate calculations were done for effective doping concentration(N_{eff}) and depletion region width. This was followed by the evaluation of the drain as well as channel voltages, specific on-resistance,power dissipation and breakdown voltages for current densities varying from 1-1000 A/cm^2. The results so obtained have been analyzed by considering varia-tions of current density versus power dissipation for different values of peak carrier concentra-tion (N_o), current density versus power dissipation for different N_o, punch through breakdown voltage versus avalanche breakdown voltage, avalanche breakdown voltage versus critical elec-tric field and N_o versus concentration gradient.

4.2 Vertical DIMOSFET with Complementary Error Function Profile in the Drift Region

It has already been mentioned earlier that there exists a trade-off between breakdown volt-age and the specific on-resistance of drift region. Ideally, for any high power application we would want a lower value of parasitic resistance and at the same time a high reverse breakdown voltage. The trade-off exists because a lower resistance value requires higher doping levels and a smaller device height while a higher breakdown voltage requires low doping with a larger height of device. The main goal in reducing the $R_{on\ sp}$ of DIMOSFET is to reduce it's power dissipation(P_D) which is given by eq.3.1. The objective suggested in this chapter has been achieved by using a dual slope linearly graded profile in the epitaxial layer of the device with a lightly doped region near the p-well-n junction to a linearly increasing doping level near the lower end of device. Such a profile is shown in Fig.4.1 below.Referring to the earlier discussion on Fig.1.4 the profile has a linearly graded profile in region A(accumulation-region), region B(JFET-region) with a steeper slope in region C(drift-region) of the DIMOSFET. Such a device structure should give a wide depletion region width due to low doping level in JFET region and low parasitic resistance in region C owing to higher level of dopant concentration here.

4.3 Theoretical Analysis

The basic structure of the DIMOSFET for the analysis with the device dimensions and the respective symbols is shown in Fig.4.2. This section discusses the device with a distorted Gaus-sian profile in the drift region which is simplified by a dual slope linearly graded profile. The formula for power dissipation, P_D as given by eq.3.1 was just an approximate value in which the effects of leakage current density (J_L) was ignored. For a 50% duty cycle for various current levels, the basic equation is given by[30]:

$$P_D = \frac{1}{2}(J_{on}^2 A R_{on\ sp} + J_L V_B A) : : : (4.1)$$

where J_{on} is the on-state current density, J_L is the reverse leakage current density of junction between the p-well/n drift region, V_B is the breakdown voltage of the device and A is the area of the device. Equation 4.1 is simplified to eq.3.1 since the value of J_L is negligible compared to the on-state current density(typically in A/cm^2).

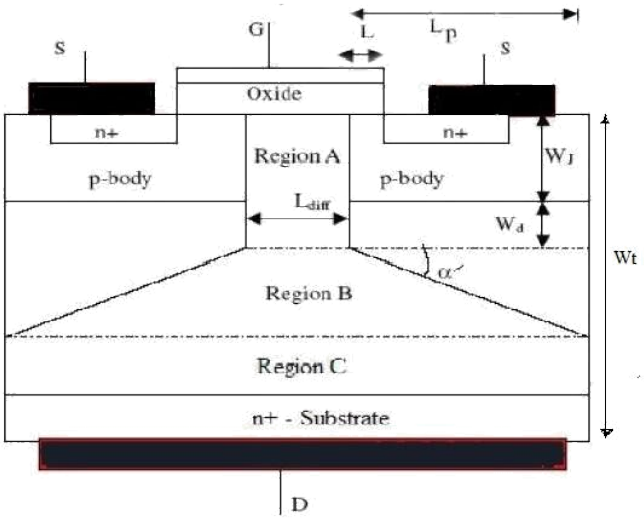


Figure 4.1: Basic Device Structure of DIMOSFET[30]

The drain current(I_{DS}) which equals the channel current(I_{CH}) is given by[24]:

$$I_{DS} = \frac{W_n}{2L[1 + (_n=2v_{sat}L)V_{ch}]} V_{ch}[2C_{ox}(V_{GS} \quad V_T) \quad (C_{ox} + C_{do})V_{ch}] \quad ::: \quad (4:2)$$

where W is the width of the device, channel length is given by L, $_n$ is the effective zero field doping dependent carrier mobility related to the doping level of the drift region, V_{ch} is the channel voltage,v_{sat} is the saturated carrier drift velocity with a value of 2 10^7 cm per sec, C_{ox} is the oxide capacitance per unit area, V_{GS} is the gate-source voltage and C_{do} is the depletion capacitance of the body. C_{do} is neglected as it's value is negligible compared to C_{ox}. In the equation above, the effect of field on mobility is considered while formulating the value of drain current. The voltage drops across the three regions, viz. region A,B and C have been found as [24]:

$$V_A = \frac{I_{DS}(W_j + W_d)}{W(L_{diff} \quad qN_{eff}) \quad _n \quad I_{DS} = E_c} \quad ::: \quad (4:3)$$

$$V_B = \frac{I_{DS}}{W\,qN_{eff}\,_n cot} log[\frac{W\,qN_{eff}\,_n(L_{diff} + L_p) \quad I_{DS}=E_c}{W\,qN_{eff}\,nL_{diff} \quad I_{DS}=E_c}] \quad ::: \quad (4:4)$$

$$V_C = \frac{I_{DS}(W_t \quad W_j \quad W_d \quad L_p tan)}{W\,qN_{eff}\,n(L_{diff} + 2L_p) \quad I_{DS}=E_c} \quad ::: \quad (4:5)$$

where all the parameters are as shown in Fig.4.2. L_{diff} is the p-body separation, W_t is the device height which is set by using the depletion width at punch through breakdown, W_j is the p-well thickness and W_d is the on-state depletion region width. V_A, V_B and V_C are the voltage drops across regions A, B and C respectively. The drain to source voltage (V_{DS}) is obtained by

adding V_A, $V_B$and V_C and V_{ch}, i.e, $V_{DS}= V_A+ V_B+ V_C + V_{ch}$.

4.3.1 Calculation of effective carrier concentration(N_{eff})

To calculate the N_{eff} we use the iteration method by varying the slope of the doping profile to calcite various values of device height which further help in calculation of the effective concentration (N_{eff}).The calculation is done by assuming a small volumetric element of thickness dx asnd integrating it from x = 0 to h provides total impurity concentration as a result.

$$N_T = \int AN(x)dx \quad :::(4:6)$$

which on integration gives

$$N_T = AN_0 \; p^{\overline{2}} \; [=frac\sqrt{}(\;)2h \qquad +12\,]ldots(4:7)$$

the effective carrier concentration N_{eff} *iscalculatedbydividingthisbytotalvolumei:e:AH* :

$$N_{eff} = \frac{2N_0 \quad 2 \; [\quad (\;)2\,h\,]ldots(4:8)}{\sqrt{\;}(\;)\sqrt{\;}(\;) \qquad 2}$$

where the higher order terms of h are neglected as h <1. Thus Eq.4.7 is used to calculate the effective carrier concentration N_{eff} for the drift region with known values of N_0:

4.3.2 Calculation of Channel Voltage (V_{ch})

V_{ch} is evaluated by using eq.4.2. In this equation we had discussed that the value of C_{do} is much less compared to C_{ox} and hence can be neglected. Keeping V_{GS} =40V and V_T = 1V, eq.4.2 becomes[30]

$$I_{ch} = \frac{W \; _nC_{ox}V_{ch}[78 \quad V_{ch}]}{2L[1 + (\;_n=2v_{sat}L)V_{ch}]} \quad :::(4:9)$$

On simplifying the above equation we get

$$Ich = \frac{W \quad C \; V \; [78 \quad V_{ch}]}{2v \; L + \quad V} \quad :::(4:10)$$

eq.4.15 can again be written as

$$W\ _n v_{sat} C_{ox} V_{ch}^2 + (\ _n I_{ch} \quad 78 W\ _n v_{sat} C_{ox}) V_{ch} + 2 v_{sat} L I_{ch} = 0 : : : (4:11)$$

eq.(4.11) being a quadratic equation, the value of V_{ch} can be evaluated as:

$$V_{ch} = \frac{(\ I_{n\ ch} \quad 78 W\ v_{n\ sat}\ C_{ox}) \quad \sqrt{(\ I_{n\ ch} \quad 78 W\ v_{n\ sat}\ C_{ox})_2 \quad 8 L W I\ v_{ch\ n\ sat}\ {}_2 C_{ox}}}{2 W\ v_{n\ sat}\ C_{ox}} : : : (4:12)$$

The last parameter to be evaluated is the specific on-resistance($R_{on\ sp}$) of the DIMOSFET, which is defined as the product of device area(A) and the resistance of drift region(R). $R_{on\ sp}$ is expressed as[30]:

$$R_{on\ sp} = RA = :l = \frac{(W_t \quad W_j \quad W_d \quad L_p tan\ )}{qN_{eff\ eff}} : : : (4:13)$$

4.3.3 Critical Field, E_c and Breakdown Voltage Calculations

The two device breakdown mechanisms considered here is - Punch through and Avalanche Breakdown.The lower of these two breakdown voltages is considered as the breakdown voltage of the DIMOSFET. The depletion width at breakdown, W is first estimated by estimating the width at punch through voltage, $V_{BP\ T}$ obtained by[35]:

$$W = \left[\ \ \right] \frac{12 \epsilon_s (V_{BP\ T} + V_g)}{qN_{eff}} : : : (4:14)$$

where ϵ_s is the permittivity value for 4H-Silicon Carbide equal to $9.66 \epsilon_o$. Now as V_g <<$V_{BP\ T}$, where V_g is the gradient voltage for linearly graded profile in the drift region. This assumption reduces eq.(4.14) to:

$$W = \left[\ \ \right] \frac{12 \epsilon_s V_{BP\ T}}{qN_{eff}} : : : (4:15)$$

The critical field, E_c corresponding to the depletion region width(W) obtained as above could be obtained by using the equation[35]:

$$E_c = \frac{(\ q\ W^2\ )}{8 \epsilon_s} : : : (4:16)$$

The avalanche breakdown voltage (V_{BAV}) can then be calculated using the equation[35]:

$$V_{BAV} = \frac{2}{3} E_c W : : : (4:17)$$

where the depletion width at the two breakdown voltages is set equal to each other. To begin with we set the $V_{BP\ T}$, calculate the depletion width W corresponding to the punch through breakdown voltage. The value of W is then used to calculate the critical field Ec*; V_{BAV}* is finally calculated by using eq.(4.16). The minimum of the two breakdown voltages' values is considered as the breakdown voltage of the device.

4.4 Calculations and Related Graphs

The dimensions of 4H DIMOSFET has been set so that height of region I, h equals the deple-tion region width, W under a reverse bias voltage of 10kV applied on the p-n junction formed between the p-body/n -epitaxial layer. The DIMOSFET was thus, designed for a maximum blocking voltage of 10kV.The dimensions of other variables labeled in Fig.4.2 have been taken as : W_t=1 m,L_p=25 m. The value of W_t is taken 1 m as the implant depth in 4H and 6H-SiC is of this order[29].The cross-sectional area of the device is 24000 10^{-8} cm^2(300 m 80 m) but the analysis is carried out for only one half of the device due to symmetrical device structure, i.e, A=12000 10^{-8} cm^2.

Calculations of various parameters of the 4H-SiC DIMOSFET with a complementary er-ror function profile in drift region is made by using a doping level of 10^{12} per cc near the source end to 10^{15} per cc over height h and 10^{15} per cc to 10^{16} per cc near the drain end in region II. The device height h has been set by iterations over the effective carrier con-centration. Initially the value of alpha (slope) is calculated with the known values of the N_0*andthethevaluesof ef f ectivecarrierconcentrationandthedeviceheightiscalculated:T heaboveproce* equal to 5 10^{14}, 8 10^{14}, 10^{15},1.6 10^{15} and 1.6 10^{15}*percc:T hespecif icon resistance*($R_{on\ sp}$)
is then obtained from the calculated value of N_{eff} as per eq.(4.18).

The values of power dissipation, P_D are then calculated for different current densities, J_f (same as J_{on}) ranging from 1-1000 A/cm^2. This is then repeated for different concentration gra-dients. The results of the calculations are shown in Tables 4.1 to 4.4. This is followed by plots of current density versus power dissipation for different values of N_o, current density versus on-state depletion width(W_d) for different values of N_o.The variation of concentration gradient(1) for various values of N_o is shown in Fig.(4.7). The variations of avalanche break-down voltage(V_{BAV}) versus critical field (E_c) and punch through breakdown voltage ($V_{BP\ T}$) and avalanche breakdown voltage for various values of N_o are shown in Fig.(4.8) and Fig.(4.10)

respectively. Fig.(4.11) illustrates the variation of on-state depletion width to specific on-resistance, the four successive nodal points on each plot corresponds to the values of current density varying from 1 A/cm^2 to 1000 A/cm^2.

Table 4.1: Results of currents,voltages, $R_{on\ sp}$ and P_D for doping 5 10^{14}, h=0.0147cm,N_{eff} =4.8768 10^{14}; = 5:549 10^{14}cm ^{4}

J(A/cm^2)	W_d(cm)	E_c(V/cm)	$R_{on\ sp}$(Ω cm^2)	P_D(W)
1	9.14e-5	1.64e6	0.3189	1.91e-5
10	2.89e-4	1.64e6	0.3142	0.0019
100	9.15e-4	1.64e6	0.2990	0.1794
1000	2.9e-3	1.64e6	0.2504	15.0222

Table 4.2: Results of currents,voltages, $R_{on\ sp}$ and P_D for doping 8 10^{14}, h=0.0116cm,N_{eff} =7.844 10^{14}; = 8:906 10^{14} cm ^{4}

J(A/cm^2)	W_d(cm)	E_c(V/cm)	$R_{on\ sp}$(Ω cm^2)	P_D(W)
1	5.754e-5	1.74e6	0.1521	9.12e-6
10	1.82e-4	1.74e6	0.1502	9.0122e-4
100	5.761e-4	1.74e6	0.1443	0.0866
1000	1.8e-3	1.74e6	0.1252	7.5112

Table 4.3: Results of currents,voltages, $R_{on\ sp}$ and P_D for doping 10^{15} , h=0.0104cm,N_{eff}=9.8 10^{14}; = 1:1152 10^{15}cm ^{4}

J(A/cm^2)	W_d(cm)	E_c(V/cm)	$R_{on\ sp}$(Ω cm^2)	P_D(W)
1	4.631e-5	1.7949e6	0.1067	6.4025e-6
10	1.4648e-4	1.7949e6	0.1055	6.3304e-4
100	4.6375e-4	1.7949e6	0.1017	0.0610
1000	1.5e-3	1.7949e6	0.0894	5.3613

Table 4.4: Results of currents,voltages, $R_{on\ sp}$ and P_D for doping 1.5 10^{15}, h=0.0085cm,N_{eff} =1.4786 10^{15}; = 1:6845 10^{15} cm ^{4}

J(A/cm^2)	W_d(cm)	E_c(V/cm)	$R_{on\ sp}$(Ω cm^2)	P_D(W)
1	3.1445e-5	1.8396e6	0.0557	3.344e-6
10	9.9456e-5	1.8396e6	0.0552	3.34e-4
100	3.1507e-4	1.8396e6	0.0535	0.0329
1000	1.05e-3	1.8936e6	0.0477	2.8613

Table 4.5: Results of currents,voltages, $R_{on\ sp}$ and P_D for doping 1.6 10^{15}, h=0.0082cm,N_{eff} =1.57 10^{15}; = 1:797 10^{15}cm ^{4}

J(A/cm^2)	W_d(cm)	E_c(V/cm)	$R_{on\ sp}$(Ω cm^2)	P_D(W)
1	2.9559e-5	1.9098e6	0.0502	3.013e-6
10	9.3619e-5	1.9098e6	0.0497	2.9843e-4
100	2.966e-4	1.9098e6	0.0482	0.0289
1000	9.936e-4	1.9098e6	0.0430	2.5808

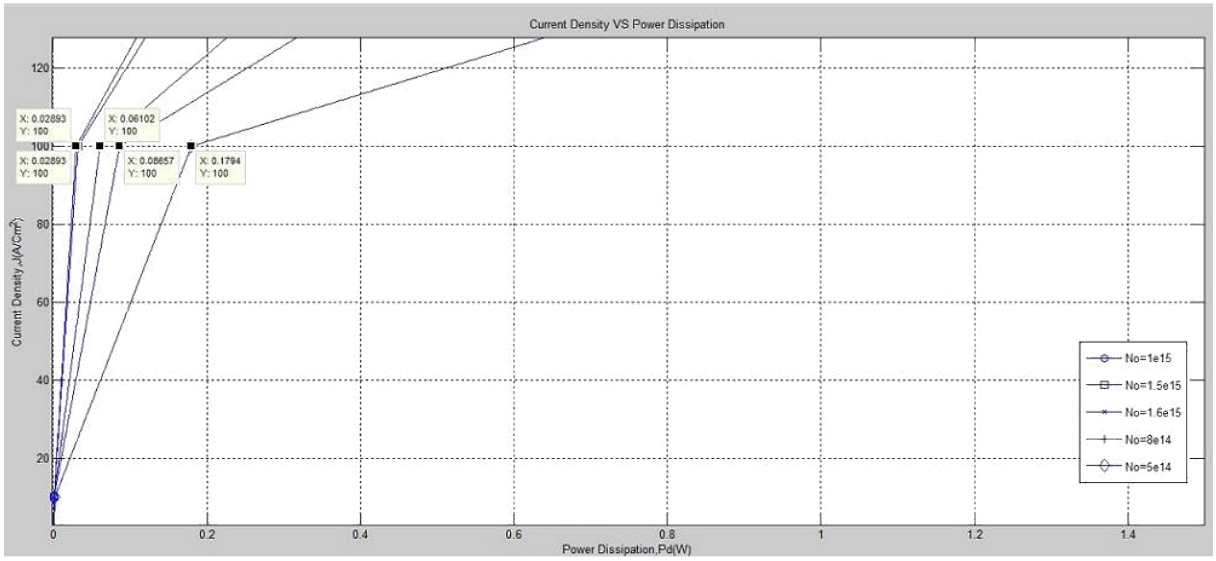


Figure 4.2: Plot of current density vs power dissipation for 4H-SiC DIMOSFET for different values of N_o

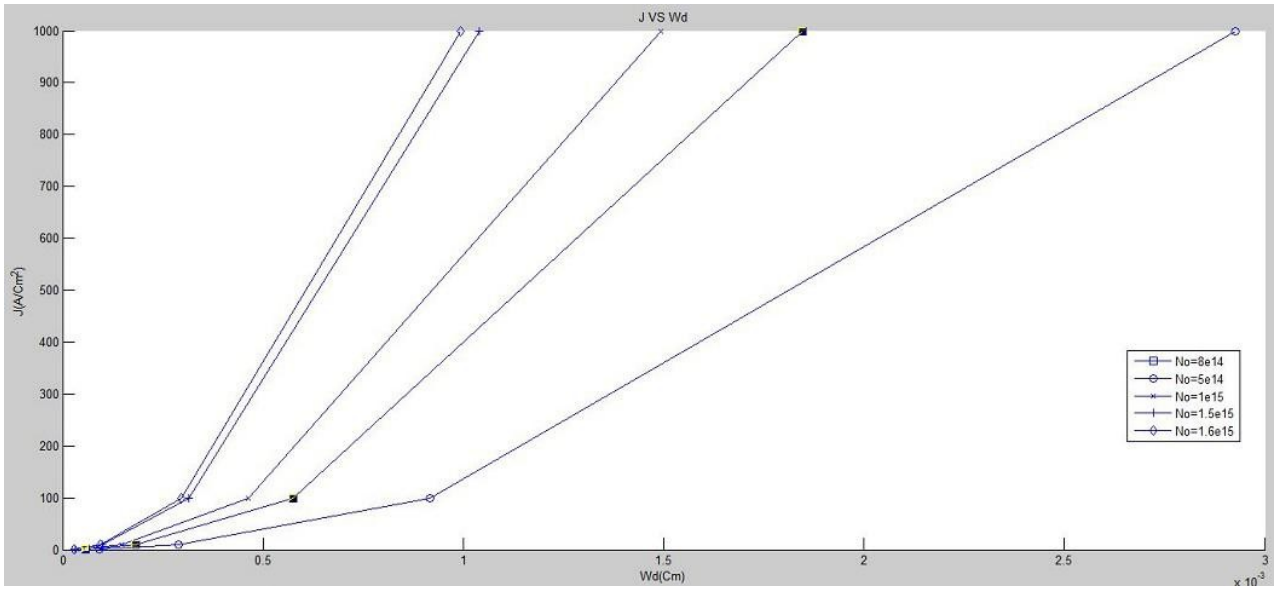


Figure 4.3: Plot of current density vs on-state depletion width for 4H-SiC DIMOSFET for different values of N_o

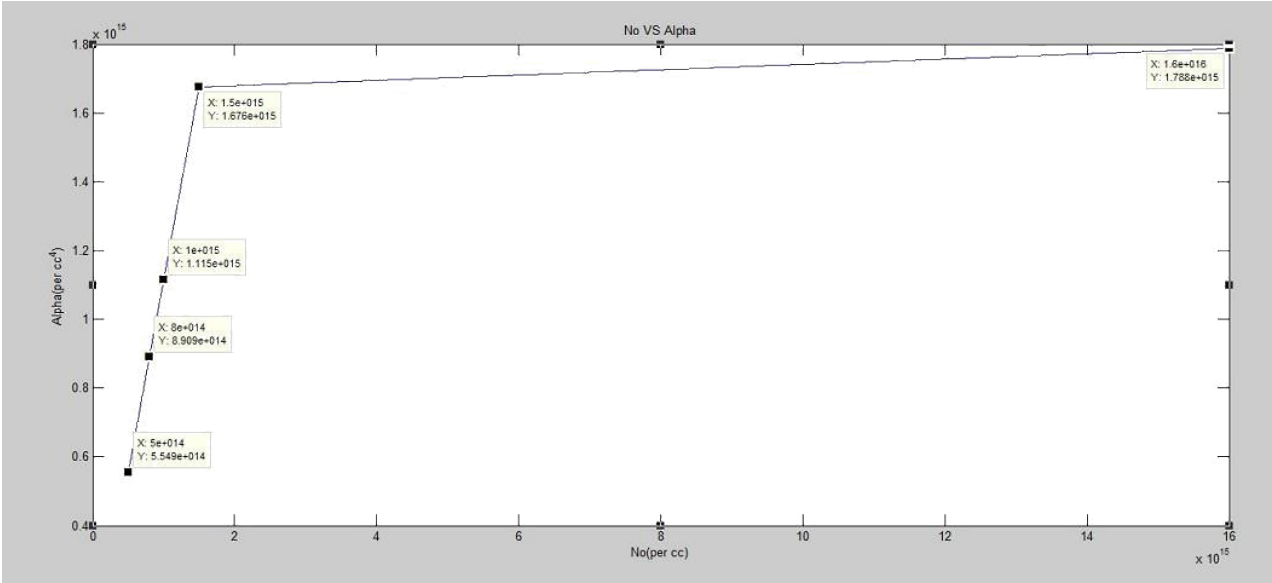
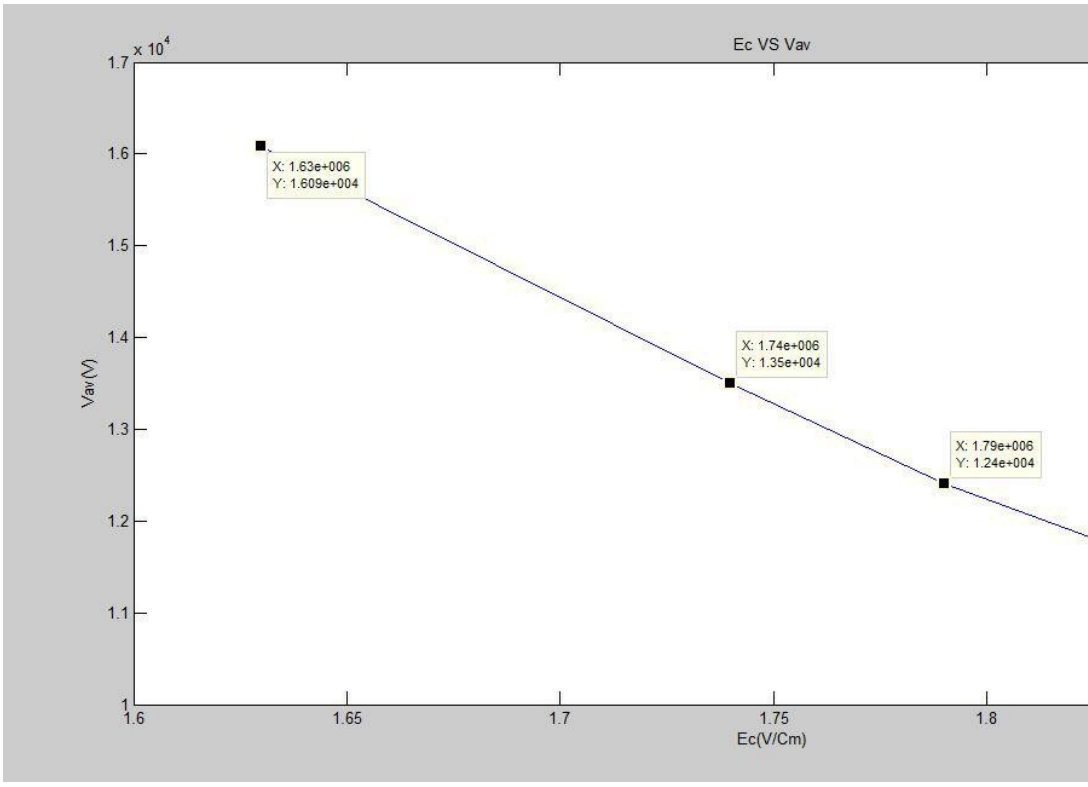
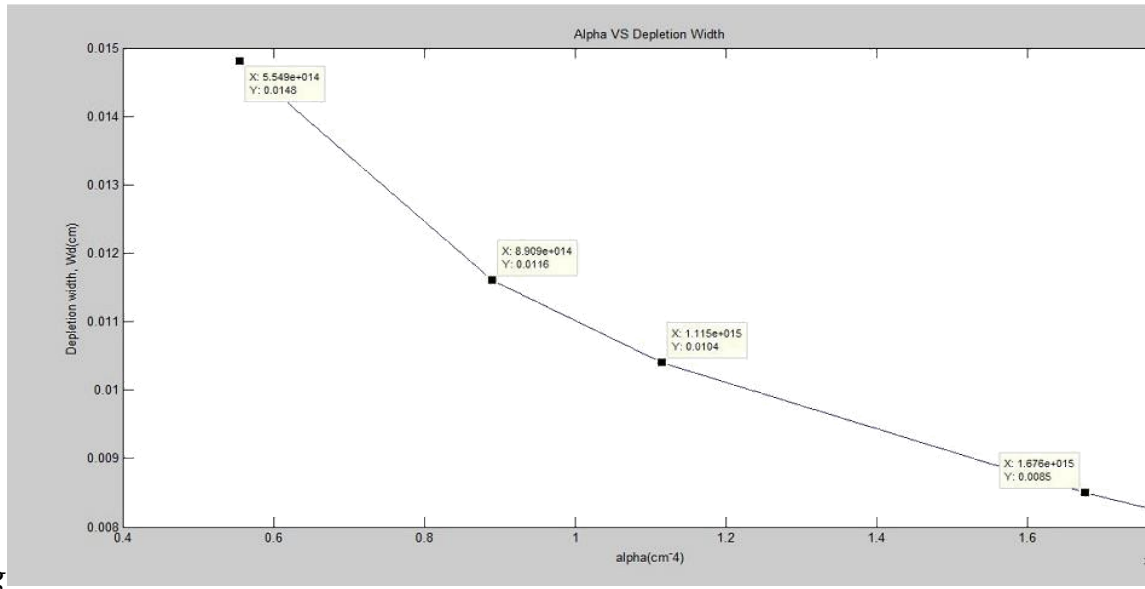


Figure 4.4: Plot of effective doping concentration vs concentration gradient for 4H-SiC DI-MOSFET



V SV av:jpgV SV av:jpg

Figure 4.5: Plot of avalanche breakdown voltage vs critical field for 4H-SiC DIMOSFET for different values of N_o



V SW :jpgV SW :jpg

Figure 4.6: Plot of concentration gradient vs device height for different values of N_o

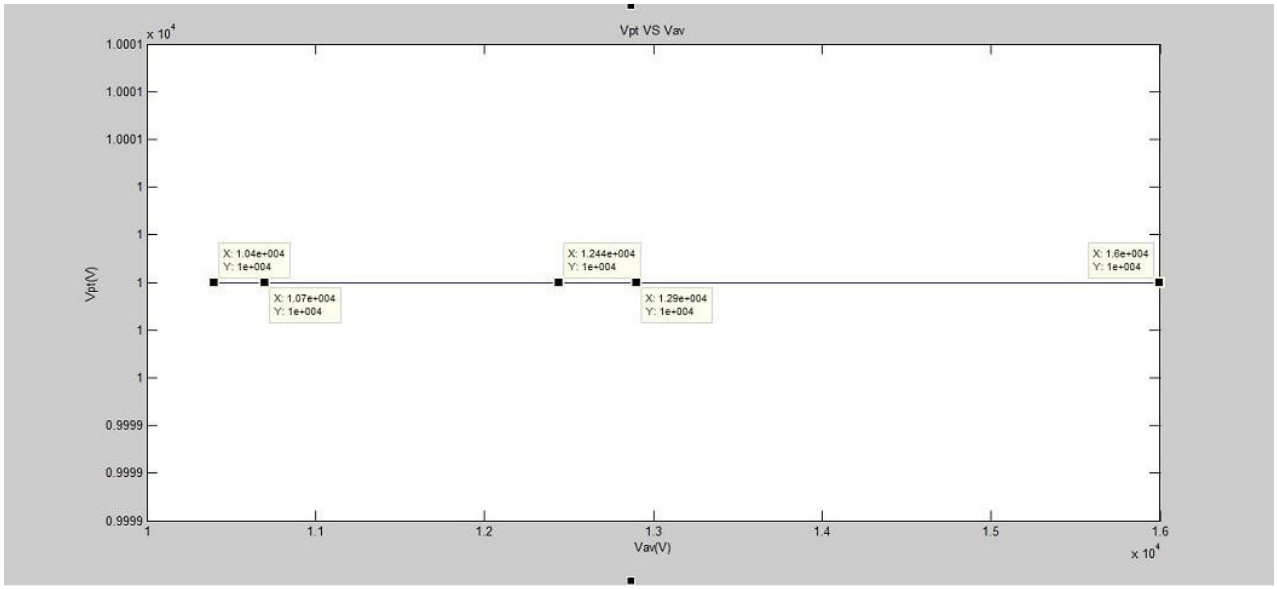


Figure 4.7: Plot of punch through breakdown voltage vs avalanche breakdown voltage for different values of N_o

4.4.1 Calculation of Breakdown Voltages(V_{BAV} and $V_{BP\,T}$)

As indicated in sub section(4.3.3), two breakdown voltages are considered here the avalanche breakdown voltage(V_{BAV}) and punch through voltage($V_{BP\,T}$). The device design requires the two voltages to be made equal to each other(or almost equal) for a given voltage. Here, the lower of the two is considered as the breakdown voltage of the DIMOSFET.

For the doping profile considered, the punch through breakdown voltage is set to 10kV and the device height h is set equal to the depletion region width.The value of critical field, E_c is calculated using eq.(4.21),the value of E_c so obtained is then used to calculate V_{BAV} from equation eq.(4.22). The results obtained is shown in table(4.5) below:

Table 4.6: Results of breakdown voltages,V_{BAV} for a punch through breakdown,$V_{BP\,T}$ set to 10kV

$_1$(cm ^{4})	E_c(V/cm)	V_{BAV} (V)
8.901 10^{14}	1.74 10^6	12.9
1.1152times10^{15}	1.7949 10^6	12.44
1.6845 $_{15}$ .797 10	1.8936 $_6$ 1.9098 10	10.71 10.4

4.5 Comparison between uniformly doping profile and complementary error function profile

As discussed in Section(3.4), the maximum breakdown voltage for which uniformly doping can be used is 5kV. Here we use the same device dimensions and doping concentrations (peak doping concentration for distorted profile) to compare the results of the two above mentioned doping profiles. Table(4.7) lists out the different parameters for uniformly doping profile and Table(4.6) lists the same set of parameters for distorted profile. For the comparison of break-down voltages, a punch through breakdown voltage, $V_{BP\,T}$ of 5kV is set for both the profiles. Table(4.8) compares the avalanche breakdown voltage(V_{BAV}), critical electric field(E_c), device height and carrier concentrations for both profiles.

Table 4.7: Results of currents,voltages, $R_{on\ sp}$ and P_D for doping 10^{15}/cc, h=0.0073cm for uniformly doped drift region

J(A/cm^2)	W_d(cm)	E_c(V/cm)	$R_{on\ sp}$(Ω cm^2)	P_D(W)
1	2.61e-5	1.78e6	0.0359	2.16e-6
10	8.3e-5	1.78e6	0.0331	2.11e-4
100	2.67e-4	1.78e6	0.0292	0.0199
1000	8.82e-4	1.78e6	0.024	1.552

Table 4.8: Results of currents,voltages, $R_{on\ sp}$ and P_D for doping 1.6 10^{15}, h=0.0082cm,N_{eff} =1.57 10^{15}; = 1:797 10^{15}cm ^{4}

J(A/cm^2)	W_d(cm)	E_c(V/cm)	$R_{on\ sp}$(Ω cm^2)	P_D(W)
1	2.9559e-5	1.9098e6	0.0502	3.013e-6
10	9.3619e-5	1.9098e6	0.0497	2.9843e-4
100	2.966e-4	1.9098e6	0.0482	0.0289
1000	9.936e-4	1.9098e6	0.0430	2.5808

Table 4.9: Results of calculation of breakdown voltages,V_{BAV} for a set punch through voltage, $V_{BP\ T}$ =5kV for uniformly doped profile and complementary error function profile

Parameters	Uniformly-doped	complementary error function
V_{BAV}	6.4 kV	5.9 kV
E_c(V/cm)	1.78 10^6	1.96 10^6
Device height,h(m)	73	58
(cm^4)	–	1.79 10^{15}
N_{eff} (/cc)	10^{15}	1.58 10^{15}

4.6 Discussion of Results

Tables 4.1 - 4.5 shows the variations of on-state depletion width W_d, power dissipation P_D, specific on-resistance $R_{on\ sp}$ and critical electric field E_c for peak impurity concentration N_o values 5 10^{14}, 8 10^{14}, 10^{15},1.5 10^{15} and 1.6 10^{15} per cc over the range of current densities considered i.e, 1-1000 A/cm^2. These five tables also indicate that value of N_{eff} increases in almost linear fashion with 1,as it can be observed in fig.4.6. Since critical field E_c decreases with lower avalanche breakdown voltage, the values of increasing N_o reduces the value of which also reduces the value of E_c. V_{BAV} is seen varying linearly with changing E_c which is as per eq.4.16. Table 4.9 compares the different parameters of uniformly doped and complementry error function doping profile for a set punch through breakdown voltage of 5kV. The device height for latter profile is almost half of that of former for the same breakdown voltage. The avalanche breakdown voltage then calculated for uniformly doped profile is 6.4kV for device height of 73 m and 5.9kV for complementary error function doping profile with a device height of 58 m. Similar to the discussion in section 3.4, for a device design both the above breakdown voltages($V_{BP\ T}$ and V_{BAV})are needed to be made equal to each other and as in calculations in [29], the lower of the two voltages is considered as the breakdown voltage of the device.

Chapter5

CONCLUSION AND FUTURE SCOPE OF WORK

The results of the calculations based on the proposed model using slope varying method of complementary error function profile in the drift region of a 4H- DIMOSFET have been presented in Chapter 4 of this work and have been quoted graphically through figures Fig.4.2 to Fig.4.7. The main variables that have been used are namely, the current density J, the depletion region width W_d in the drift region, the drain-source voltage V_{DS}, the effective concentration of impurities N_{eff} in the drift region, the critical electric field E_c, the avalanche breakdown voltage V_{BAV} , the punch through breakdown voltage V_{BAV} , the power dissipation P_D, the device height h and also the specific on-resistance $R_{on\ sp}$ of the device, which equals to a first approximation to the $R_{on\ sp}$ of the drift region for high voltage devices.

The variations of current density versus power dissipation of the device treating the peak concentration N_o as a parameter have been shown in Fig.4.2. It has been observed that the P_D rises steeply from low values of current density to a value of J of about 1000 A/cm^{2}. The values of P_D continue to rise steeply with J for N_o equal to 1.6 10^{15} and 1.5 10^{15} per cc. There is however, a crossover at very low values of P_D between the two graphs close to the origin . For the other three graphs, namely for N_o equal to 5 10^{14}, 8 10^{14} and 10^{15} per cc, the P_D versus J graph has an inflexion point much less than 0.01 W. The former concentration rises more steeply than the latter with increasing values of J.

The current density J versus depletion region width W_d shows a gradual rise in W_d as the value of N_o rises from N_o= 5 10^{14} to 1.6 10^{15}. The similar profiles are observed for higher

values of W_d versus J for N_o = 1.6 10^{15} and 1.5 10^{15} per cc as shown in Fig.4.3.

The graph of N_{eff} versus concentration gradient has a linear plot with the lowest value at N_o =5 10^{14}/cc to N_o =1.6 10^{15}/cc. No such inflexion point has been observed in this graph as has been quoted earlier. The variations of critical field E_c with the avalanche breakdown voltage has been plotted in Fig.4.5 with N_o as a parameter. Since the critical field E_c decreases with lower avalanche breakdown voltage, the values of increasing N_o reduces the value of which also reduces the value of E_c.

The device height h was pre-calculated on the basis of the different iterations of the slope varying method to calculate alpha which then is used to find depletion region width obtained by the normal device equation. Hence, an increase in the value of N_o lowers the value of and hence the punch through breakdown voltage giving a lower value of depletion region width which had been set equal to the device height h. It can be concluded that a 10kV DIMOSFET using the complementary error function profile approximated to a linearly graded profile will have an increasing value of h with decreasing value of N_o. The variation in values of punch through breakdown voltage $V_{BP\ T}$ with the avalanche breakdown voltage V_{BAV} is shown in Fig.4.7. It can be seen that the two voltages are equal at the pre-designed breakdown voltage of 10kV for which N_o= 1.6 10^{15}/cc. This is the ideal device using complementary error function profile in the drift region of the 4H-SiC DIMOSFET, as the best device design is the one in which these two breakdown voltages equal each other. For other points on this graph, the design can't be approved as the breakdown voltage having a lower value will come into force before the other breakdown voltage can be reached.

In order to conclude, it can be said that the best device using this type of profile is the one which can be obtained from Fig.4.7 with N_o= 1.6 10^{15} per cc, = 1.797 $10^{15} cm^{4}$ (refer Fig.4.4) having $V_{BP\ T}$ = V_{BAV} = 10kV. The crossover points shown in Fig.4.2 couldn't be explained on the basis of current analysis. This can be undertaken by other researchers for future work on these devices having different polytypes of SiC.

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