“TEMPERATURE DEPENDENT PERFORMANCE ANALYSIS OF SINGLE WALL CARBON NANOTUBE IN VLSI INTERCONNECTS”

A dissertation Submitted towards the partial fulfillment of requirement for the award of degree of

MASTER OF TECHNOLOGY

In

VLSI Design

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DECLARATION

I hereby declare that the work presented in the dissertation report entitled, **"TEMPERATURE DEPENDENT PERFORMANCE ANALYSIS OF SINGLE-WALL CARBON NANOTUBE IN VLSI INTERCONNECTS"** is an authentic record of my study carried out as requirements for the award of degree of M. Tech (VLSI DESIGN) at Thapar University, Patiala, under the guidance of **Mr. Karamjit Singh** (Assistant Professor), Electronics and Communication Engineering Department, Thapar University, Patiala and refers other researcher's work which are duly listed in the reference section.

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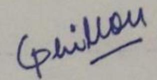

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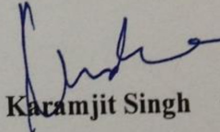

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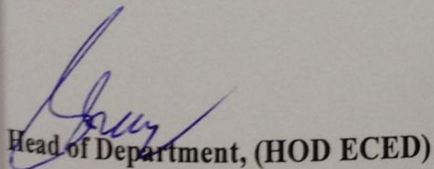

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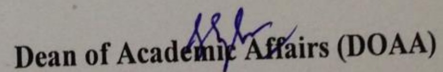

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ABSTRACT

World is changing rapidly and is becoming a better place to live in with the advancement in technology. With the up gradation of electronic devices into smaller and faster phases, the associated complexity that increases with the increase in packing density and functionality of circuits, certain issues related to area and power consumption are faced. One certain issue that comes into scene is the delay associated with the interconnect material. Propagation delay of interconnect is an important parameter which helps in determining the performance of high speed VLSI circuits. With the advancement in technology, certain problems like electromigration, surface roughness and grain boundary scattering prevail in copper; so CNTs are introduced with excellent thermal conductivity and current carrying capacity at scaled technology nodes. Due to high resistance in isolated ones; SWCNT bundle are used comprising of number of parallel isolated CNTs. In this dissertation report, the performance of copper and CNT interconnect are studied and compared at 32nm and 22nm technology. The effects of various parameters like length and diameter of interconnect, number of repeaters and size of driver transistor and temperature have been analyzed. Delay analysis is done using SPICE simulation. The thermal heating effects are one of the most important and indispensable consideration of VLSI designers responsible for maximum IC failures at increased packing densities of the circuits. Different types of electron- phonon scattering mechanisms in metallic SWCNT bundle interconnects that reduce electron mean free path have been studied. Results reveal that resistance of interconnects thus increases due to rise in temperature and thereby delay increases. However, the delay of copper is always more than CNT bundle at raised temperatures. SWCNT bundle gives better result than copper and provides appropriate solution as an interconnect material in deep submicron technology at semi-global and global interconnect lengths for high speed circuits.

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LIST OF ABBREVIATIONS

IC	Integrated Circuit
VLSI	Very Large Scale Integration
MOSFET	Metal Oxide Semiconductor Field Effect Transistor
NMOS	N-channel Metal Oxide Semiconductor
PMOS	P-channel Metal Oxide Semiconductor
CMOS	Complementary Metal Oxide Semiconductor
RLC	Resistance, Inductance and Capacitance
CNT	Carbon Nanotube
SWCNT	Single Wall Carbon Nanotube
MWCNT	Multi Wall Carbon Nanotube
ITRS	International Technology Road map for semiconductors
SPICE	Simulation Program with Integrated Circuit Emphasis
MFP	Mean Free Path
K	Kelvin
Temp	Temperature

CHAPTER 1

INTRODUCTION

Interconnect wires are used to connect various components on a VLSI chip. Basically, VLSI Interconnect is a thin conducting material film that helps in providing an electrical connection between nodes of the circuit or the system. Many materials have been used as an interconnect material and are also replaced by other materials because of shortcomings in existing material at certain technology and also depending upon the application for its use. The interconnect material used in the circuit plays very crucial role in determining circuit performance parameters.

The associated impedance parasitic such as resistance, inductance and capacitance needs to be considered at submicron and deep submicron technologies as they introduce certain delay in propagating signals in the system. With the advancement in VLSI technology, as the feature size of ICs diminishes, supply and threshold voltages are also scaled down for maintaining its electric field constant. As a result, interconnect dimensions must be scaled down also. Also with the increase in chip size, the associated complexity and functionality due to scaling of impedance parameters also rises. The feature size of VLSI chips is also shrinking to yield better improvement in propagation delay, area needed, power consumption and other cost considerations.

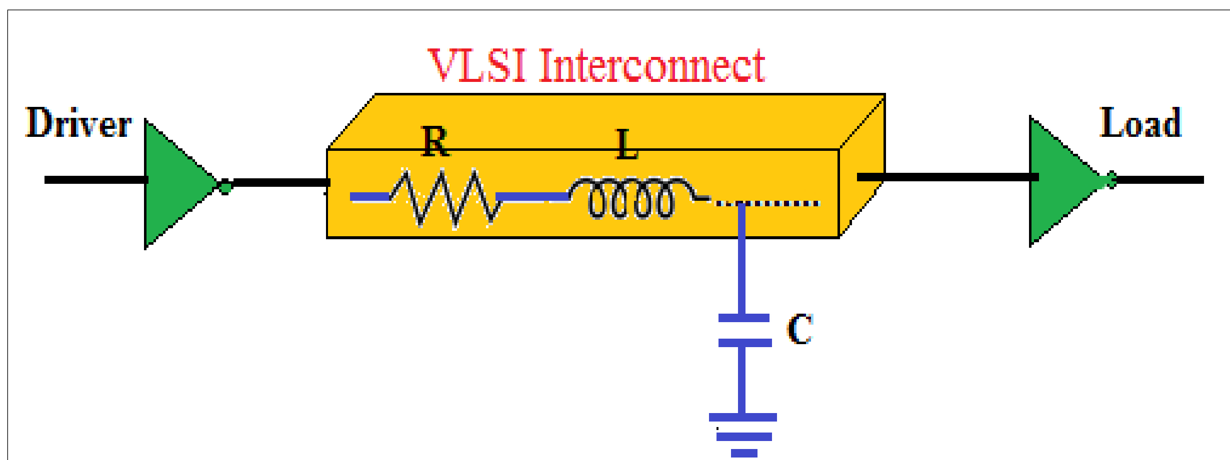

Figure 1.1 A VLSI Interconnect

1.1 Aluminum as an Interconnect

In earlier technology nodes until 180nm, aluminum material was widely used as an interconnect material for circuits due to its excellent characteristics[1] such as it has good conductivity, forms good ohmic contact with silicon and it also adheres nicely on silicon dioxide. At advanced technology nodes with scaling, interconnect current density rises. So, at increased current densities, electromigration problem is faced for aluminum. As the feature size further decreases, significance of electromigration increases and degrades the performance of system. Due to the transfer of momentum between the conducting electrons of material and the diffusing metal atoms, transport of material thus takes place by the gradual movement of ions; this phenomenon is referred to as electromigration.

The next problem which occurred in using aluminum is that for pure Al, its resistivity is of the order 2.7 μΩ–cm which is far higher than that of pure copper with resistivity of the order 1.7 μΩ–cm. Therefore, pure Al cannot be used for interconnect applications. Actual Al interconnections are alloys mixed with copper and silicon and are used for global and semi global interconnects where low resistivity is needed. So, an alternative i.e. Copper was introduced and used as an interconnect material in VLSI design circuits[1,7].

1.2 Copper as an Interconnect

Copper was considered as an obvious alternative to aluminum due to shortcomings in it at scaled technologies for submicron and deep submicron high density and high performance chips. In comparison with aluminum, copper material with higher conductivity is more resistant to electromigration and can also withstand more current density about five times as interconnect in IC applications.

Also copper has high electrical conductivity and high melting temperature (1,357K) than aluminum (933K) thus, making copper thermally more stable than aluminum[1,6] also shown in Table1.1. However certain issues are also addressed in copper at aggressive technologies-

- Surface roughness
- Grain Boundary scattering (Resistivity of material increases due to formation of interfaces between two grains in a polycrystalline material)

Table 1.1 Comparison of different properties of Copper, Silver, Aluminum, Gold and Tungsten material

Properties\Material	Copper (Cu)	Silver (Ag)	Gold (Au)	Aluminum (Al)	Tungsten (W)
Resistivity[μΩ–cm]	1.7	1.6	2.35	2.7	5.65
Melting Point[K]	1357	1062	1264	933	3387
Corrosion in Air	Poor	Poor	Excellent	Good	Good
Adhesion to SiO_2	Poor	Poor	Poor	Good	Poor

As the cross section of copper interconnects decreases, there is increase in propagation delay of the signal, power dissipation is more and electromigration issues are faced[6,7]. At nano-metric dimensions in future VLSI electronic systems, the interconnection cross sections will become small and smaller. Due to certain problems faced in copper interconnect, carbon nanotubes are proposed to be used as interconnect material to overcome the problems faced in existing materials[2]. There has been parallel increase in die size with continuous reduction of feature size; as a result, increase in the length of chip interconnects. The length of interconnect can be categorized as local, intermediate or semi-global and global.

1.3 Types of Interconnects on the basis of Length

Interconnect length plays a crucial role in determining performance of the circuit in VLSI applications[7]. The hierarchy of interconnects is as follows[7]-

- **Local (Short) Interconnects**- used for localized region of a chip to provide electrical path between different nodes/components of the circuit. Local interconnects are typically a few hundred nanometers and no more than a few microns in length. Hence it can be assumed that local interconnect lengths are typically within the length of mean free path of electrons in a CNT.
- **Semi-global (intermediate length) interconnects**- used for lengths between local and global level and intermediate interconnects are typically few tens of microns.
- **Global (Long) interconnects-** with longest die size (few hundreds of μm) and is used to provide electrical connection path over considerable length of the chip including power, ground and clock lines and are typically hundreds of microns or even more[7].

1.4 Carbon Nano Tubes as an Interconnect

CNT comprises of carbon material and is hollow in the shape of tube diameter in nanometer scale. Thus, their name is derived from as they are grown in the form of hollow seamless cylinders by one atomic layer of graphene.

Table1.2 Properties of CNT compared to copper[2]

Properties\Material	CNT	Cu
Maximum current density[A/cm^2]	~ 10^{10}	~ 10^6
Thermal Conductivity[W/mK]	~ 6000	~ 400
Mean free Path[nm]	~ 1000	~ 40
Mechanical Strength	High	Low
Switching Delay	Fast	Slow
Process of Fabrication	Difficult	Easy

CNT promises to be a suitable alternative to copper and a suitable candidate for interconnects of future VLSI circuits because of its high mechanical stability, high thermal stability and conductivity and large current carrying capability as shown in Table1.2. Thus, proves to be the strongest and stiffest material yet discovered.

1.4.1 Categorization of CNTs

There are two types of CNTs based on its layered structure as shown in Figure 1.2-

a. **Single walled CNT (SWCNT)** – consists of single thin wall of graphene sheet [diameter of nanotubes(d)-(1-2nm.)]
b. **Multiwall CNT (MWCNT)**–consists of a many concentric SWCNTs [d-(2-25nm.)]

Nanotubes can be further of two types- metallic or semiconductor depending upon the way the tube is rolled[1,6]. In single atomic layer of graphite i.e. Graphene; a 2-d honeycomb structure sp^2 bonded carbon atoms are present. With its unusual band structure, conducting states are present only at some specific points in momentum space along specific directions. Also out of metallic and semiconducting, metallic CNTs are attractively used in interconnect applications due to-

- High thermal stability
- High mechanical stability
- High Thermal conductivity [5800W/mK]
- High Current density [10^{14} A/m^2] at Temperature>200^oC

Any bundle of SWCNTs may contain metallic and semiconducting nanotubes because of lack of control of chirality. Semiconducting CNTs are not useful in conducting current in interconnects. Although, multi-walled CNTs are mostly metallic in nature and are required for interconnects. SWCNTs on the other hand, have an electron MFP of the order of a one micron. Metallic SWCNTs are the preferred candidates in the domain of interconnect.

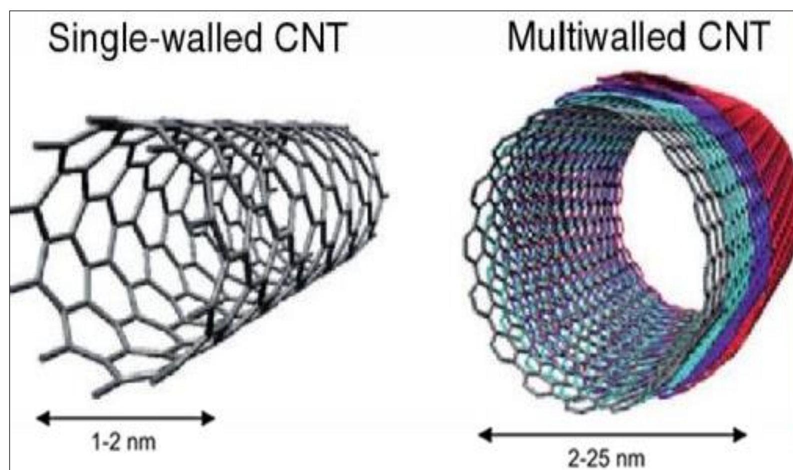

Figure1.2 Single-wall CNT and Multi-wall CNT[5]

- **Multiwall CNT**

MWCNT consists of many SWCNT enrolled in concentric form[1]. For lengths more than 10µm, it has resistivity lower than copper and can be used as its substitute. For such global lengths, delay in copper is thus more than delay in MWCNT. With further increase in length there is improvement in delay than copper.

Large diameters in MWCNT yields better performance. Although at local lengths of interconnect which have smaller cross section and more resistivity, MWCNT can have more delay than copper. Over this range copper shows better performance than MWCNT. However at intermediate levels, MWCNT can replace copper and can be used extensively.

1.5 Significance of Using Repeaters

As the length of interconnect increases, impedance parameters increases linearly, thus the propagation delay also increases with length whenever resistance of interconnect becomes larger or even comparable to on resistance of driver transistor. Repeaters are therefore used to decrease the delay; it divides complete section (long wire line) into smaller subsections/segments and is used between and before each segment pair of short wire[3,10].

RC time constant i.e. propagation delay helps in determining the performance of VLSI circuits and it increases sharply as chip/interconnect dimensions is scaled down with technology up gradations. As feature size diminishes, the propagation delay increases and affect the speed of circuit. Therefore, to reduce this time delay and improve the speed of circuit, optimum number and optimum sized repeaters can be used.

1.6 Importance of Scaling

Scaling of MOS transistors is related to systematic decrease or reduction of device dimensions as permitted by technology while geometric ratios remains preserved. The designing of high density and high performance portable chips in VLSI needs that the packing density of MOSFETs used in the circuits must be as high as possible, therefore their sizing needs to be small. So, scaling of transistors is required to meet area considerations [13]. The total area acquired by MOS Transistor is scaled down by shortening the channel width and channel length. Generally used, in constant field or ideal scaling, all the dimensions of device i.e. width, length, voltage applied, line resistance and capacitance are scaled down by a factor of 1/s so as to maintain constant electric field.

1.7 Interconnect Models

1.7.1 Lumped Model

In lumped element model of electronic circuits, the attributes of the circuit i.e. resistance, capacitance, inductance, and gain, are concentrated into ideal electrical components; resistors, capacitors, and inductors, etc. and these are joined by a network of perfectly conducting wires. The different configurations of RC interconnect models are shown below in Figure1.3.These are L-model, T-model and Π-model depending upon the way and the

shape they are connected. RC model is divided into N-segments to make the distributed configuration[14].

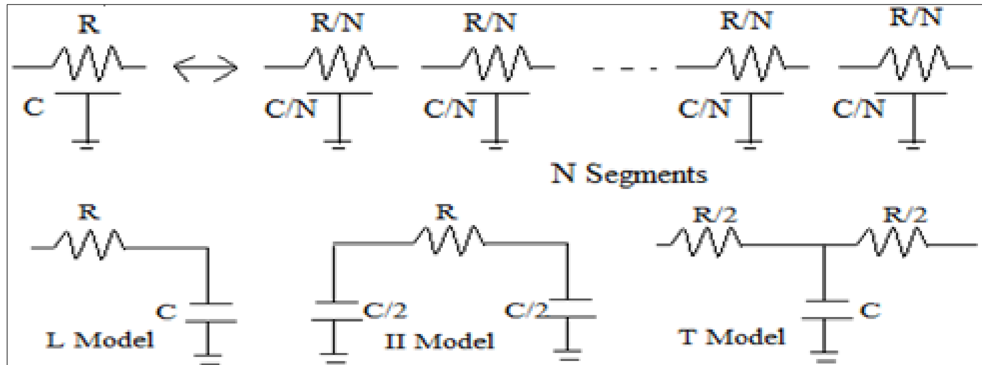

Figure 1.3 Different Configurations of RC Interconnect Models[14]

1.7.2 Distributed Model

In distributed element model or transmission line model of electrical circuits, the attributes of the circuit like resistance, capacitance, and inductance are distributed continuously throughout the material of the circuit. The proposed distributed RLC line model can be approximated by a lumped multi-stage RLC network can be depicted as and shown in Figure 1.4 as shown-

$$R_N = \frac{R}{N},\ L_N = \frac{L}{N},\ C_N = \frac{C}{N} \tag{1.1}$$

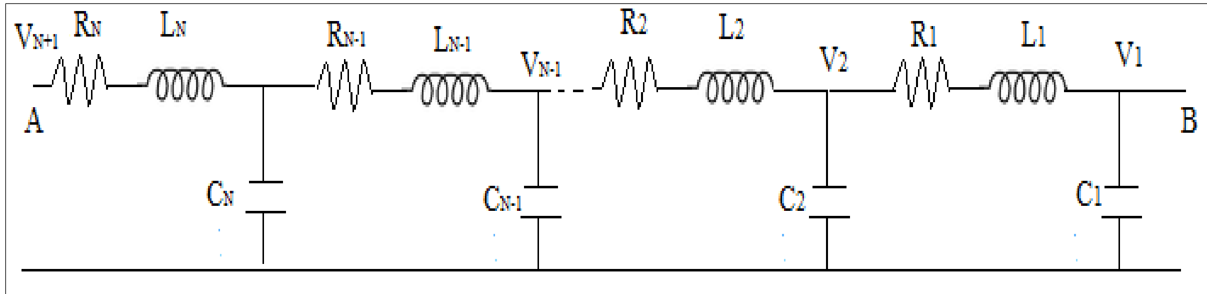

Figure 1.4 Distributed RLC Model (with N Segments)[14]

1.8 Role of Temperature in IC circuits

Although lots of work is done in the domain of carbon nanotubes as VLSI interconnect in the last decade, still less research is done on the effect of temperature and how it can affect the performance of mSWCNT as a VLSI interconnect. High performance VLSI circuits have to operate with great variance at elevated temperature range above room temperature. Temperature effects are one of the most important factors that must be considered while

designing of VLSI chips at increased scaling nodes to maintain healthy performance of the device. Temperature effects must be analyzed thoroughly as they can seriously affect circuit performance like its reliability and IC damage failures. As a result, performance of device degrades at high temperature. Large temperature variation also have a crucial effect on the propagation delay of signal passing through the interconnect material. So, different parameters and different types of phonon scattering mechanisms that can affect interconnect performance by lowering mean free path of conducting electrons due to collisions and scatterings at increased temperature are presented in this dissertation report.

1.9 Outline of the Work

This dissertation report presents carbon nanotubes as an emerging material in the domain of VLSI interconnects. The report is sectioned as follows-

Chapter 1 introduces the need of interconnect in circuits, its types and the conventional material used as an interconnect. A brief overview of the problems that arouse in existing materials and comparison between properties of different materials is discussed. Also an outlook of CNT is given. Chapter 2 discusses the research work done for carbon nanotubes as VLSI interconnect. Chapter 3 provides equivalent models and RLC equations for SWCNT and copper and their values are determined for 32nm and 22nm technology nodes. Chapter 4 presents delay simulation results. Concept of Repeaters is also discussed. Different parameters like diameter and length of interconnect are also taken into account. It is analyzed that CNT offers less propagation delay than copper. Chapter 5 introduces the role of temperature and its effect on its performance. Different scattering mechanisms that exist at high temperature, their effect and temperature dependent equations are expressed and then values of impedance parameters are obtained. The temperature dependent performance simulation and comparison of copper and CNT is performed. Chapter 6 concludes that parameters like diameter, length and temperature plays important role in determining delay. CNT can easily replace copper and be used as VLSI interconnects for high speed applications.

CHAPTER 2

LITERATURE REVIEW

VLSI interconnects helps in connecting two or more points or nodes of the circuit/system. Interconnect is a wire made from a material with good electrical conductivity and is responsible for estimating circuit performance parameters like power, speed and noise.

The below mentioned papers provide a brief overview of the recent researches and developments in the area of carbon nanotubes as a VLSI interconnect-

2.1 Interconnect Delay Models

- **Optimal Interconnection Circuits for VLSI-1985 [3]**

H. B. Bakoglu, et al. proposed propagation time delay model of interconnects considering the effects of transistor sizing and dimensions of chip. The propagation delay of aluminum and poly silicon lines are compared. With the advancement in technology, chip dimension increases and feature size decreases. As a result, the resistance of interconnect becomes prominent and delay increases rapidly. To minimize the delay, capacitance and resistance should be reduced. For this some of the techniques are mentioned. Either by using low resistance aluminum lines for longer lengths and by incorporating interconnection with multilayers for thick and wide lines in upper layers. Or the other widely used technique is by using optimum number of optimally sized inverters with cascaded first stage to drive the signal till the last stage. These techniques can be employed for lowering propagation delay of the signal.

- **Performance analysis of carbon nanotube interconnects for VLSI applications-2005 [7]**

Navin Srivastava, et al. compared the performance of CNT bundles and copper as VLSI interconnects. For global lengths CNT bundles with perfect contacts has less resistance than copper beyond 45nm technology node has been demonstrated. However, CNT bundles have higher resistance than copper with imperfect contacts and have a degraded performance. Capacitance of CNT bundles is always higher than copper for all technologies. With

decreased packing density of CNT bundles, CNT's effective resistance increases thus degrading delay. At local levels, lower density CNT bundle can show better performance where the capacitance effect dominates.

- **Analysis of Carbon Nanotube Interconnects and their Comparison with Cu Interconnects-2009 [5]**

Naushad Alam, et al. reported that due to certain shortcomings like high resistivity and electromigration faced by copper at advanced technology nodes, CNT bundles proves to be a suitable candidate as VLSI interconnects for deep submicron technology. Also reported that CNT bundles have lower value of resistance and capacitance for semi-global and global lengths of interconnect. Although for local interconnect levels, copper can be continued to be used as it has smaller value of resistance than CNT bundles. However, it was observed that the resistance of CNT bundle interconnects can be optimized by varying the average diameter of CNTs and the density of tubes in the bundle. Despite of high nominal values of Inductances, they can be ignored in the performance analysis because the resistive impedances are very much higher than the inductive impedances at any length of interconnects.

- **Influence of tube diameter on carbon Nanotube interconnect delay and power output -2011 [6]**

Mayank Kumar Rai, et al. addressed that diameter of CNT can affect its delay and power dissipation in VLSI applications. CNT bundle interconnect has low values of resistance and inductance than copper at 32nm and 22nm technology nodes, thus offers lower delay comparatively at small diameters while the value of capacitance of CNT bundle is more than copper. Capacitance can be further decreased by choosing larger diameter and also decreases power dissipation. Large diameter offers less resistance but more capacitance therefore more power dissipation and smaller diameters offers less capacitance and more resistance as less number of CNTs will be placed in bundle and therefore more propagation delay in this case. So, an optimum diameter should be chosen depending upon the application in use as trade-off is faced between delay and power where either resistance or capacitance of CNT dominates.

- **Performance Comparison between carbon Nanotube and Copper Interconnects for GSI-2005 [8]**

Azad Naeemi, et al. studied the performance of copper and CNT as VLSI interconnects. With technology scaling, in ideal scaling feature size shrinks to maintain constant electric fields. At scaled technologies, a problem like surface roughness and grain boundary scattering are seen in copper, thereby increase its resistance and degrades its speed. For global lengths, wires used for power and ground lines are more prone to electromigration as current densities increases rapidly. Carbon Nanotubes show ballistic flow of electrons with longer mean free path in microns than copper. Also CNTs can carry large current densities and therefore are potential candidates for interconnect applications.

- **Control of SWCNT-interconnect Performance by Tube-diameter-2009 [4]**

Mayank Kumar Rai, et al. studied and compared the resistance of copper interconnects with CNT. Metallic SWCNT bundle have been studied extensively. CNT can overcome electromigration problem in copper and can withstand more current density than copper and can be used at 32nm technology or below. For 32nm technology, with the increase in tube diameter, capacitance dominates till a diameter is reached. Beyond this value, resistance dominates and increases delay. So at this technology, optimum diameter should be chosen. At 22nm technology, increase in diameter increases resistance. So, tube diameter can be restricted to 22nm. Undoubtedly, power dissipation decreases with increase in diameter as capacitance dominates. Another parameter is the length of interconnect that plays attractive role in determining power and delay. It is shown that for local level, copper can be used; however for global and semi global level CNT can replace copper successfully.

- **Effects of Inductance on the Propagation Delay and Repeater Insertion in VLSI Circuits-2000 [10]**

Yehea I. Ismail, et al. introduced the expression for estimating the propagation time delay of CMOS gate driving a distributed RLC line. The expressions to calculate the optimum number of repeaters and the optimum size of driver inverter are also given. It is shown that if interconnect is considered to be as RC interconnect and inductance is neglected than the percentage error can be more than 30%. As the inductance effect is considered, the

propagation delay has a linear dependence which was earlier quadratic. Therefore, Inductance should also be considered as it has prominent effect on high performance high density ICs. This is also because of the fact that repeaters needed if the inductance is considered are less in number than it is ignored. So, including inductance in distributed line models not only decreases delay but also reduces area and help in achieving high density and high speed chips. It is concluded that inductance cannot be neglected in distributed model of interconnect line.

- **Repeater insertion in global interconnects in VLSI circuits-2005 [15]**

Rajeevan Chandel, et al. reported that propagation delay and power dissipation are main factors in determining the performance of VLSI circuits. The voltage-scaled repeaters are inserted into the interconnect model that helps in minimizing delay and power dissipation in case of long/global lengths of interconnect. Global and semi-global lengths of interconnect also have larger value of impedance values and thus show more time delay and power dissipation in propagating signal across the length of interconnect. The analytical results for delay analysis at 0.8µm and 0.18µm have been matched and verified by SPICE simulations and it has been concluded that by using optimum voltage scaled repeaters, the number of repeaters and thereby there is decrease in silicon area and therefore lesser heating of the chip.

- **Circuit modeling and Performance analysis of Multi-walled Carbon Nanotube Interconnects-2008 [16]**

Hong Li, et al. studied CNTs based performance and showed that they are a possible alternative to copper. An RLC equivalent model is evaluated and compared against traditional copper interconnects at all levels (short/local, semi-global/intermediate and long/global) for technology nodes. At intermediate (500-µm) and global (1000-µm) levels, MWCNTs can have smaller impedance values and thus lower delay than copper. However at local levels, copper continued to be in use. Also for SWCNT bundles to show better performance than MWCNT interconnects, their density should be high and CNTs should be mostly metallic while MWCNTs are also easier to fabricate with no consideration of density control. SWCNT bundles continued to be used in VLSI circuits at semi-global and global levels.

2.2 Temperature Dependent Interconnect Models

- **Electrical and thermal transport in metallic single-wall carbon nanotubes on insulating substrates-2007 [9]**

Eric pop, et al. analyzed transport phenomenon and impedance parameters in mSWCNT over low bias. Various factors that are responsible for giving net temperature dependent resistance are also addressed. The temperature dependent resistance of SWCNT is given by considering the effect of various phonon scattering phenomenon like acoustic, optical field and optical absorption phonons. The net temperature dependent MFP (which in this case is smaller than usual) is thus obtained and gives net resistance of SWCNT. The calculated temperature dependent parameters have generally more values. Further study shows that unlike in metals, in metallic SWCNTs electrons are less responsible for its net total conductivity considering effect of temperature. For interconnect applications, the effect of temperature must be accounted. Simulated results reveal that although temperature increases impedance as well as delay of SWCNT, yet it performs better than copper at 32nm technology node and below. Further thermal conductivity can be improved by optimizing diameter. In this way, both size and temperature are responsible for the conductivity of SWCNTs.

- **Thermally-aware modeling and performance evaluation for single-walled carbon nanotube-based interconnects for future high performance integrated circuits-2010 [11]**

Amir Hosseini, et al. presented thermally aware model for SWCNT interconnects that takes into the account of effect of temperature by considering different scattering phenomenon and also gave expressions for its temperature dependent impedance parameters. The performance and reliability of conventional copper interconnect and SWCNT are then compared for future VLSI high performance industry. The effect of size and temperature are captured. Finally the temperature independent and dependent models of SWCNT as VLSI interconnect and the values of its impedance parameters and then delay are calculated. Also the thermal model of SWCNT and copper is compared. The results show that SWCNT can outperform copper showing improvement in delay at advanced technology nodes at and beyond 32nm taking into account the effect of temperature from range 250K-450K. Simulated results show

improvement (about 4-5 times) in delay of SWCNT than copper. Longer i.e. global and semi-global level lengths of interconnect shows better and improved performance than shorter interconnects is also concluded. SWCNT can easily replace conventional copper and also proves to give high density and high speed interconnects for future VLSI industry demands.

- **Size and Temperature Effects on the Resistance of Copper and Carbon Nanotubes Nano-interconnects-2010 [17]**

Andrea G. Chiariello, et al. introduced metallic SWCNT bundles as an emerging material in field of VLSI interconnects used in circuit design due to excellent electrical, mechanical and thermal properties. The effects of temperature and size on electrical performances of copper and SWCNT are also addressed because these factors can considerably reduce their current density and reliability. The temperature and technology dependent models are developed to first calculate their impedance parameters and then their simulation results are matched. However, capacitance and inductance remains unchanged. The parameters increase with the increase in temperature range, however still SWCNT proves to be better than copper with considerable less delay in CNT bundle than copper. The delay is analyzed for 22nm technology and is reported less for SWCNT, making it a suitable candidate with excellent thermal strength at elevated temperatures.

- **Electro-thermal Characterization of Single-Walled Carbon Nanotube (SWCNT) Interconnect Arrays-2009 [20]**

Wen Chao Chen, et al. studied electro-thermal effect of metallic SWCNT arrays. These arrays are biased at low and high bias; by using temperature dependent and independent finite difference methods, parameter equations for SWCNT parameters are first solved and then simulated upon. Then CNT length dependent, voltage dependent, temperature dependent and diameter dependent response are captured and compared with copper. The effect of temperature is studied thoroughly and investigated that thermal effects can effect signal propagating through SWCNT interconnect, particularly time-delay. It is thus concluded that effect of temperature must be considered while designing SWCNT interconnects.

CHAPTER 3

SWCNT AND COPPER AS VLSI INTERCONNECTS

In this chapter the analysis of copper and one-dimensional SWCNT bundle as future interconnects for VLSI Industry is done. Equivalent circuit models are used to obtain parameters for SWCNT and copper on the basis of interconnect geometry. Further delay analysis is done by the help of Tanner EDA tools using equivalent circuit and technology spice files. The electronic properties of graphene are studied to understand the properties and conductivity of carbon nanotubes better. Graphene, in its most directions has an enough band gap that does not permit electrons to move freely and help in conduction unless given extra energy; thus named a zero-gap semiconductor. These electrons can however flow freely when graphene is metallic. This property does not hold true in bulk graphite, because there is always a conducting path between two points; thus graphite conducts electricity. A special direction for flow of electrons along the axis is selected by rolling a graphene in tube shape; some CNT are metallic and other is semiconducting. So, nanotubes are suitable candidates for further technologies as both metals as well as semiconductors are made from same carbon system.

3.1 Equivalent Circuit Model for Copper Interconnect

Figure 3.1 represents the model used to obtain the parameters for copper as interconnect [18]. R_{cu}, L_{cu} and C_{cu} are resistance, inductance and capacitance of copper interconnect.

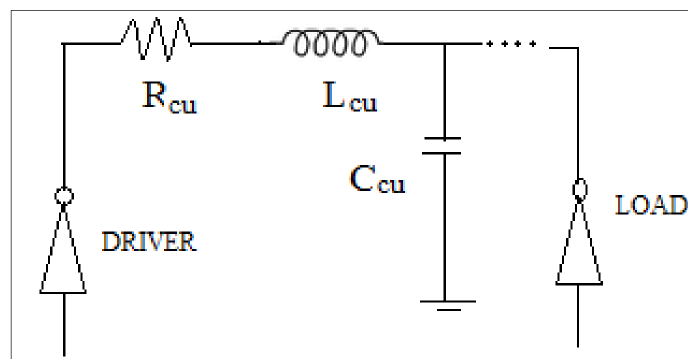

Figure 3.1 Equivalent circuit model of copper as interconnect

3.1.1 Equivalent Resistance of Copper

The resistance of Copper Interconnect[18] is given below in equation(3.1)-

$$R_{Cu} = \frac{\rho l}{w.t} \tag{3.1}$$

Where, ρ is the resistivity of copper and its value depends upon the technology.

3.1.2 Equivalent Capacitance of Copper

The area associated with underlying plane as shown in Figure 3.2 below, gives capacitance of copper as an interconnect material as-

$$C_{cu} = \mathcal{E}\left[\frac{w}{h} + 2.22\left(\frac{s}{s+0.70h}\right)^{3.19} + 1.17\left(\frac{s}{s+1.51h}\right)^{0.76}\left(\frac{t}{t+4.53h}\right)^{0.12}\right] \tag{3.2}$$

Where, $\mathcal{E}$ is dielectric permittivity and its value is given as in equation(3.3)-

$$\mathcal{E} = \mathcal{E}_r\,\mathcal{E}_0 \tag{3.3}$$

Where, $\mathcal{E}_r$ is relative permittivity and $\mathcal{E}_0$ is absolute permittivity (8.86×10^{-12} F/m.) Based on the model, l, w and t are length, width and thickness of interconnect respectively and h is the height of interconnect placed above ground plane as shown in Figure 3.2.

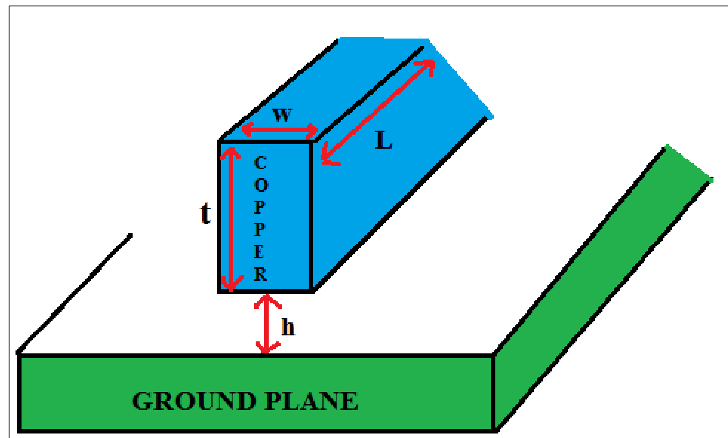

Figure 3.2 Copper Interconnect above Ground plane

3.1.3 Equivalent Inductance of Copper

The Inductance of copper wire when used as an interconnect is given in equation(3.4) as-

$$L_{Cu} = \frac{\mu_0 l}{2\pi}\left[\ln\left(\frac{2l}{w+t}\right) + \frac{1}{2} + 0.22\left(\frac{w+t}{l}\right)\right] \tag{3.4}$$

Where, μ_0 is absolute permeability and its value is defined as $4\pi \times 10^{-7}$ H/m.

3.2 Equivalent Circuit Model for SWCNT Interconnect

3.2.1 Resistance of an Isolated SWCNT

Figure 3.3 shows the equivalent circuit used to obtain parameters for SWCNT. 1-d system of SWCNT has N parallel conducting channels, with Planck's constant ħ, electron charge e and T as electron transmission coefficient[1,7]. There are 4 parallel conducting channels in CNT due to sub lattice and spin degeneracy of electrons. Assumed perfect contacts (T=1) and substituting values of constants, the fundamental resistance is given in equation(3.5) as-

$$R_f = \frac{\hbar}{4e^2} \tag{3.5}$$

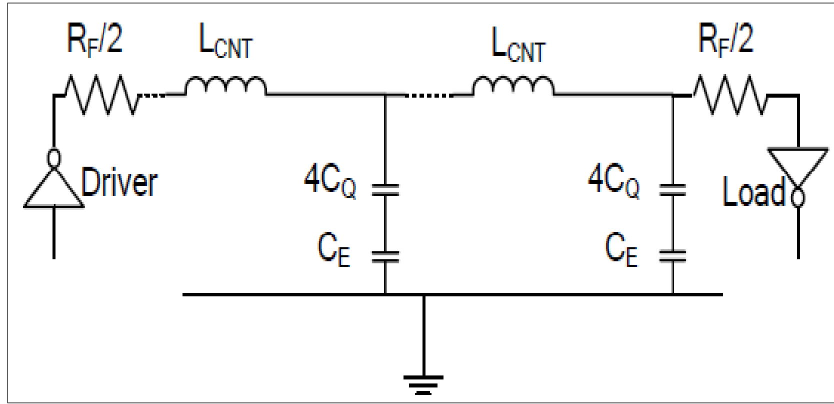

Figure 3.3 Equivalent circuit model of Isolated SWCNT[4]

By substituting values of above constants, the fundamental resistance yields large value around 6.45KΩ. If tube length (L) exceeds MFP of electron then additional resistance i.e. scattering resistance also comes into scene which increases with increase in length[4,6].

$$R_{CNT} = \left(\frac{\hbar}{4e^2}\right)\frac{L}{L_0} \tag{3.6}$$

Contact Resistance is also distributed at two ends of the circuit. So, the total resistance is given by the sum of three resistances.

3.2.2 Capacitance of an Isolated SWCNT

Single Wall Carbon nanotube has its two associated capacitances with different origins-

a. Electrostatic capacitance (C_E)

This capacitance comes due to charge stored by the SWCNT of diameter d when placed above ground at distance y as shown in Figure 3.4 below is expressed as-

$$C_E = \frac{2\pi\varepsilon}{\ln\frac{y}{d}} \tag{3.7}$$

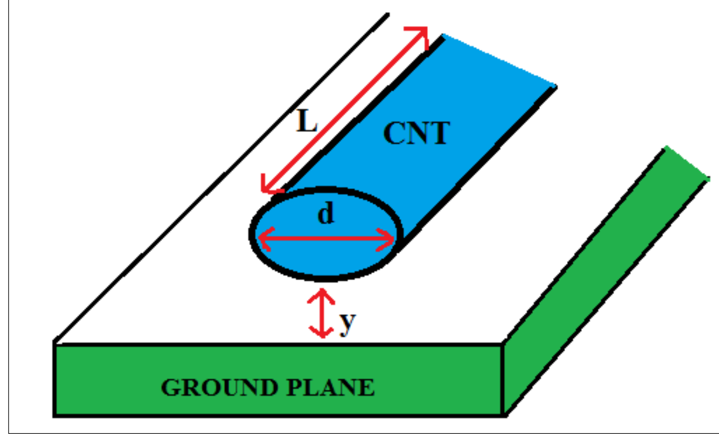

Figure 3.4 SWCNT placed above Ground plane[7]

b. Quantum capacitance (C_Q)

This capacitance is due to stored quantum electrostatic energy in the nanotube when it conducts carries current and is given in equation(3.8)-

$$C_Q = \left(\frac{2e^2}{\hbar v_f}\right) \tag{3.8}$$

Where v_f is Fermi velocity of electron and e is the electron charge. With four conducting channels in CNT, net quantum capacitance is $4C_Q$. As current flows, C_E and $4C_Q$ appear in series in SWCNT.

3.2.3 Inductance of an Isolated SWCNT

SWCNT has two associated inductances[4]-

a. Magnetic inductance (L_M)

This inductance is due to the current flowing in wire and stored as total magnetic energy in the wire.

$$L_M = \frac{\mu_0}{2}\left(\ln\frac{y}{d}\right) \tag{3.9}$$

b. Kinetic inductance (L_K)

This inductance comes from each conducting channel of CNT stored in the form of kinetic energy when CNT conducts. In CNT the four parallel conducting channels results in a net kinetic inductance of $L_K/4$.

$$L_K = \frac{\hbar}{2e^2 v_f} \tag{3.10}$$

An isolated CNT is not preferred due to its high resistance in range from 7 KΩ - 100 KΩ. Over isolated, SWCNT bundle interconnects provides the advantage at semi-global and global lengths. So, bundle of CNTs are used in parallel to form SWCNT bundle resulting in net decrease of resistance[4].

3.3 Equivalent Circuit Model for SWCNT Bundle as Interconnect

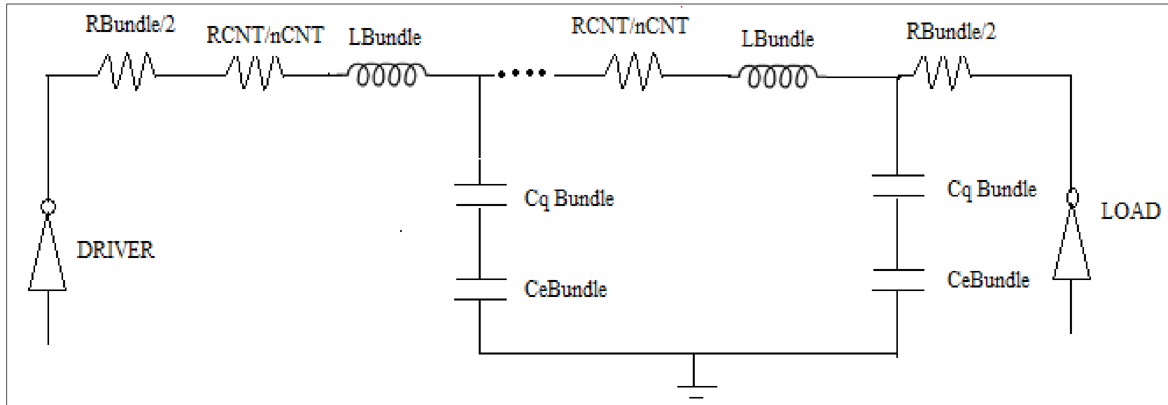

Figure 3.5 Equivalent circuit model of SWCNT bundle[1]

Figure 3.6 shows the equivalent circuit model of CNT bundle. SWCNT bundle comprises of identical metallic CNTs packed in hexagon shape. The Centre of each CNT is separated by a uniform distance ‘x’ and each nanotube has six neighbors. Based upon packing type, different types of CNT bundles are shown in Figure 3.5. With densely packed structure i.e. ‘x’=‘d’, CNT gives the best performance[7].

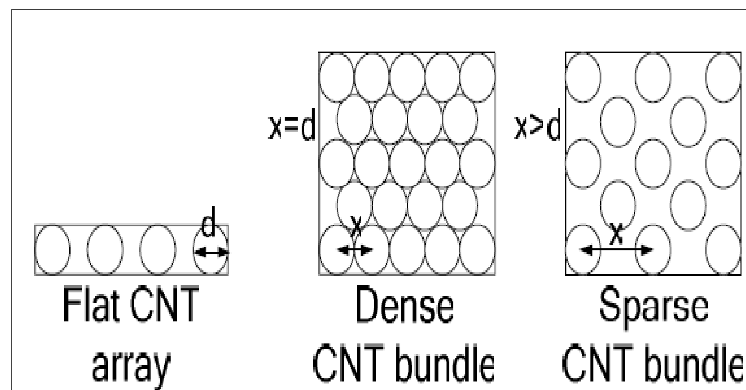

Figure 3.6 Different types of CNT bundles[7]

The expressions which helps to calculate the number of CNTs present in the bundle are written below[7], where number of rows in the interconnect bundle is n_h and number of

columns in the bundle is n_W, and total number of CNTs present in the SWCNT bundle is n_{CNT}. The number of columns in SWCNT Bundle is given by-

$$n_w = \frac{(w-d)}{x} \tag{3.11}$$

The number of rows in SWCNT Bundle is given by-

$$n_h = \frac{(h-d)}{\frac{\sqrt{3}}{2}x} + 1 \tag{3.12}$$

If the numbers of rows (n_h) are even, then number of CNTs in bundle is given by-

$$n_{CNT} = n_w n_h - \frac{n_h}{2} \tag{3.13}$$

Otherwise if the numbers of rows (n_h) are odd, then number of CNTs in bundle is given by-

$$n_{CNT} = n_w n_h - \frac{n_h - 1}{2} \tag{3.14}$$

3.3.1 Equivalent Resistance of SWCNT Bundle

It is assumed that all CNTs in bundle are metallic and conducting, therefore effective resistance of SWCNT bundle is given by dividing isolated resistance by number of CNTs present as-

$$R_{CNT(Bundle)} = \frac{R_{isolated}}{n_{CNT}} \tag{3.15}$$

$$R_{CNT\ (Bundle)} = \frac{\frac{\hbar}{4e^2}\ [1 + \frac{L}{L_0}]}{n_{CNT}} \tag{3.16}$$

3.3.2 Equivalent Capacitance of SWCNT Bundle

The effective equivalent capacitance (C_{Bundle}) of SWCNT Bundle is obtained by the series combination of quantum capacitance and electrostatic capacitance of SWCNT bundle[1] is given as-

$$C_{Bundle} = \left(\frac{C_{EBundle} . C_{QBundle}}{C_{EBundle} + C_{QBundle}}\right) \tag{3.17}$$

Where the values of $C_{Ebundle}$ and $C_{Qbundle}$ are given by equations below-

$$C_{EBundle} = 2\left(\frac{2\pi\epsilon}{\ln\left(\frac{s}{d}\right)}\right) + \text{floor}\left[\left(\frac{w-d-2}{x}\right)\right]\left(\frac{2\pi\epsilon}{\ln\left(\frac{s+w}{d}\right)}\right) + \frac{3(n_h-2)(2\pi\varepsilon)}{5\ln\left(\frac{s}{d}\right)} \tag{3.18}$$

$$C_{QBundle} = \left(\frac{2e^2}{\hbar v_f}\right) n_{CNT} \tag{3.19}$$

3.3.3 Equivalent Inductance of SWCNT Bundle

The equivalent inductance of SWCNT bundle can be expressed as the parallel combination of two inductances associated i.e. magnetic and kinetic inductance corresponding to each CNT present in SWCNT bundle and is expressed as[6]-

$$L_{Bundle} = \frac{L_M + L_K}{4n_{CNT}} \tag{3.20}$$

3.4 Impedance Analysis

The values of impedance parameters of SWCNT and copper are calculated from the equations mentioned in this chapter and are plotted in the figures below-

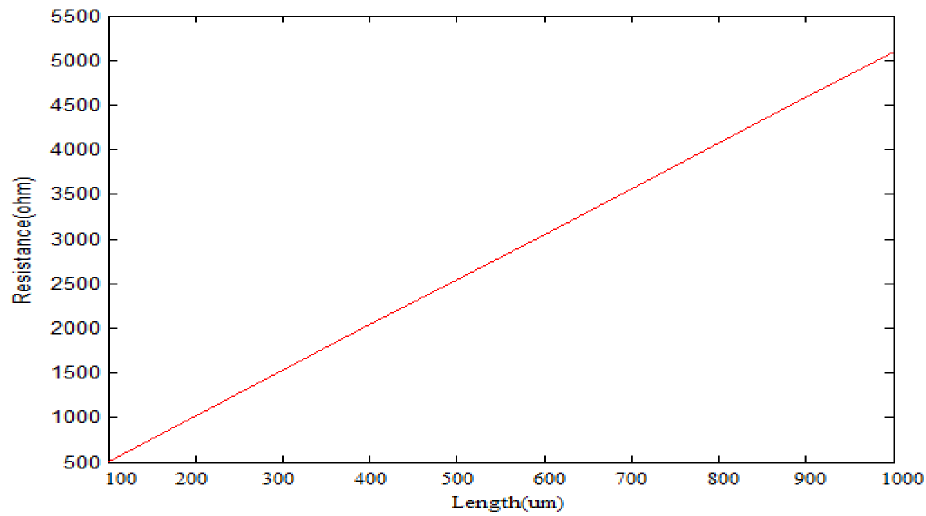

Figure 3.7 Resistance vs. Length of copper at 32nm technology node

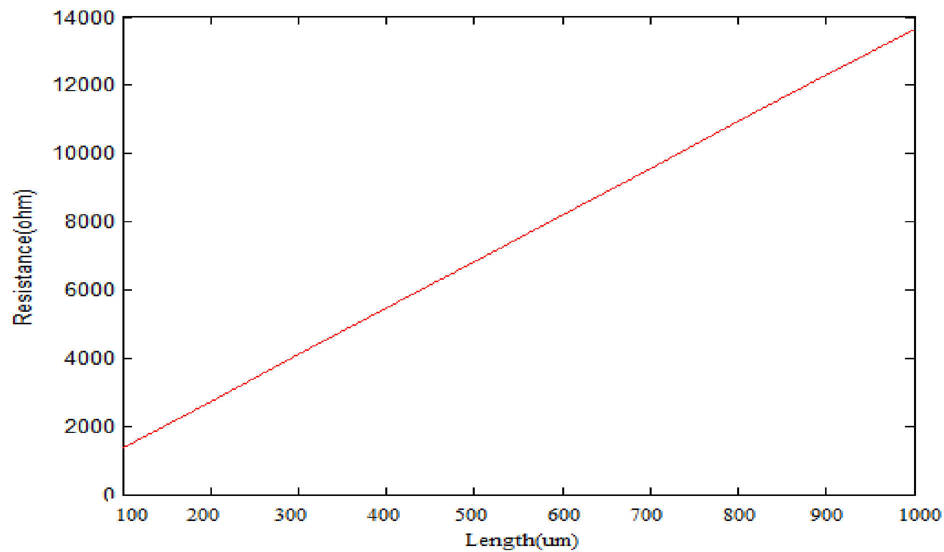

Figure 3.8 Resistance vs. Length of copper at 22nm technology node

Figure 3.7 and Figure 3.8 plots the values of resistance vs. length of Copper at 32nm and 22nm technologies. As the length of interconnect increases from 100µm to 1000µm, the value of resistance increases linearly. However, the value of resistance of copper at 22nm technology is more than that of 32nm technology due to introduction of certain problems like electromigration and surface roughness.

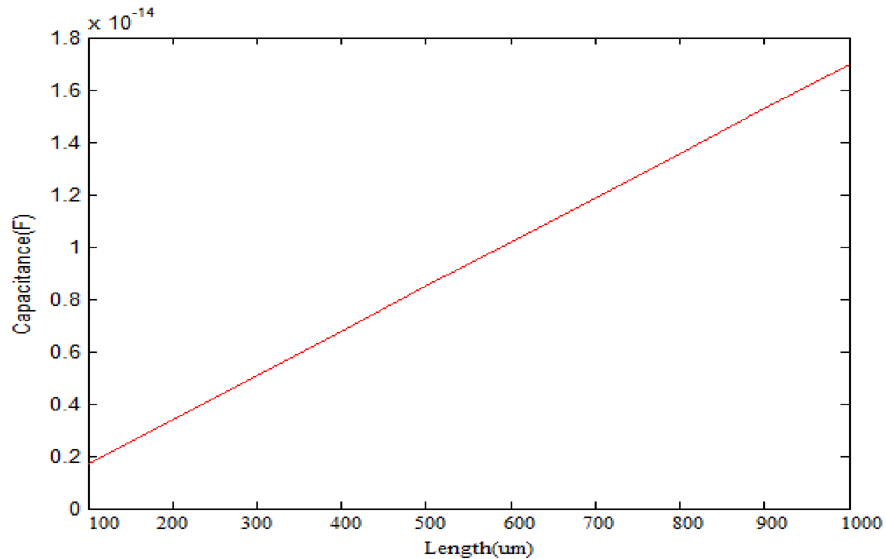

Figure 3.9 Capacitance vs. Length of copper at 32nm technology node

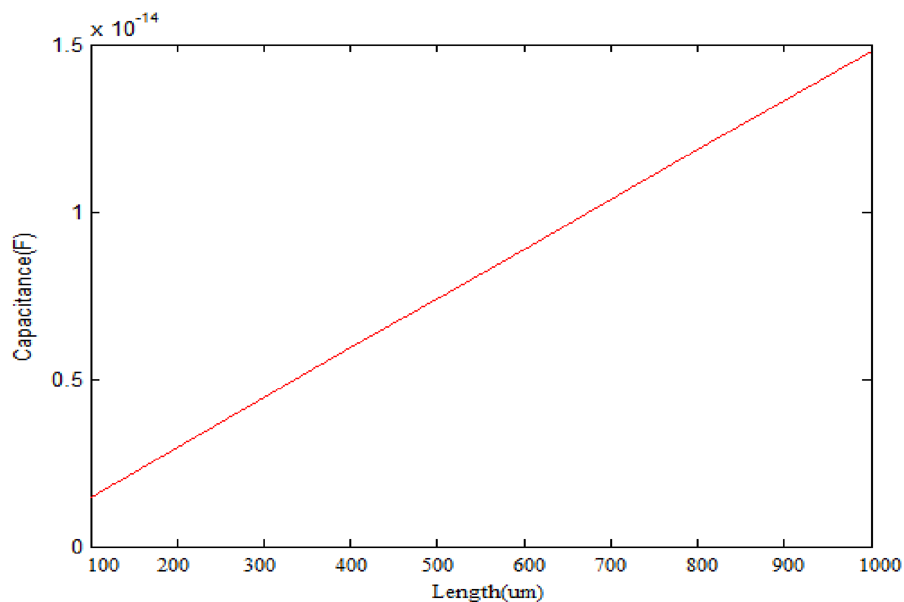

Figure 3.10 Capacitance vs. Length of copper at 22nm technology node

As the length of interconnect increases, the values of impedance parameters also increases with the length. Figure 3.9 and Figure 3.10 shows the variation of capacitance of copper at

32nm and 22nm technologies with its length at semi-global and global levels of length of interconnect.

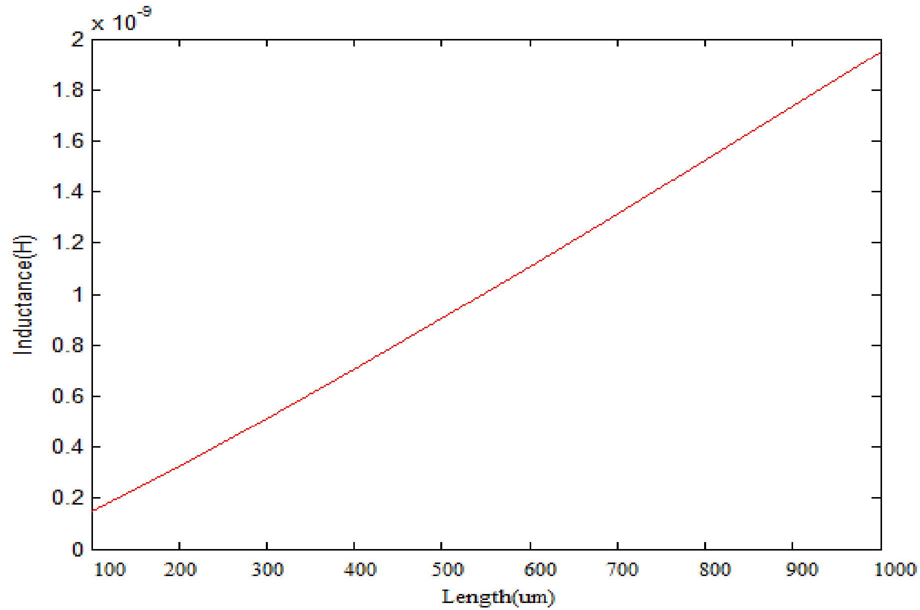

Figure 3.11 Inductance vs. Length of copper at 32nm technology node

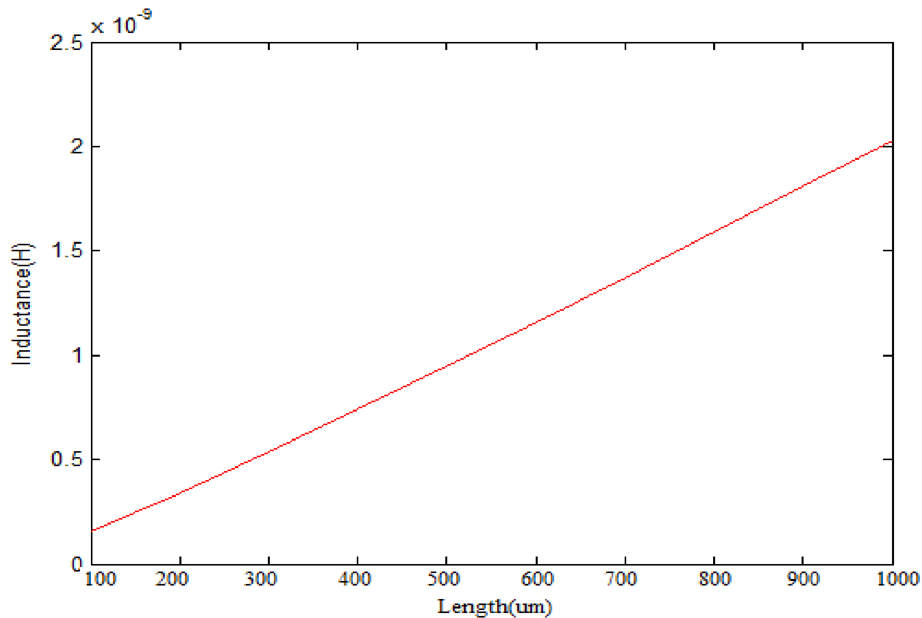

Figure 3.12 Inductance vs. Length of copper at 22nm technology node

Figure 3.11 and Figure 3.12 shows the effect of length on the inductance of copper based interconnect. Inductances of copper increases along with increase in length of interconnect. The obtained values of RLC of copper are then compared with the parameters of SWCNT. Figure 3.13-3.18 shows the values of parameters of SWCNT taking into account the effect of both diameter of nanotube and the length of interconnect for both 32nm and 22nm

technology nodes. It is very much evident from the figures that all three parameters of SWCNT i.e. R, L and C increase with the increase in length of interconnect; however this is not the case with the diameter of the nanotube used.

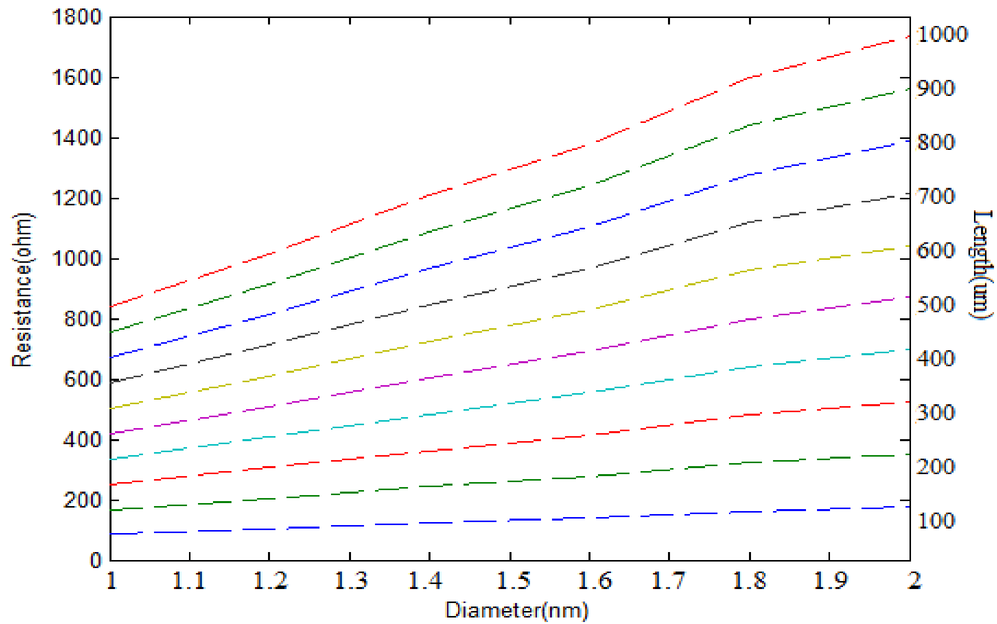

Figure3.13 Resistance vs. Diameter of SWCNT at 32nm technology node

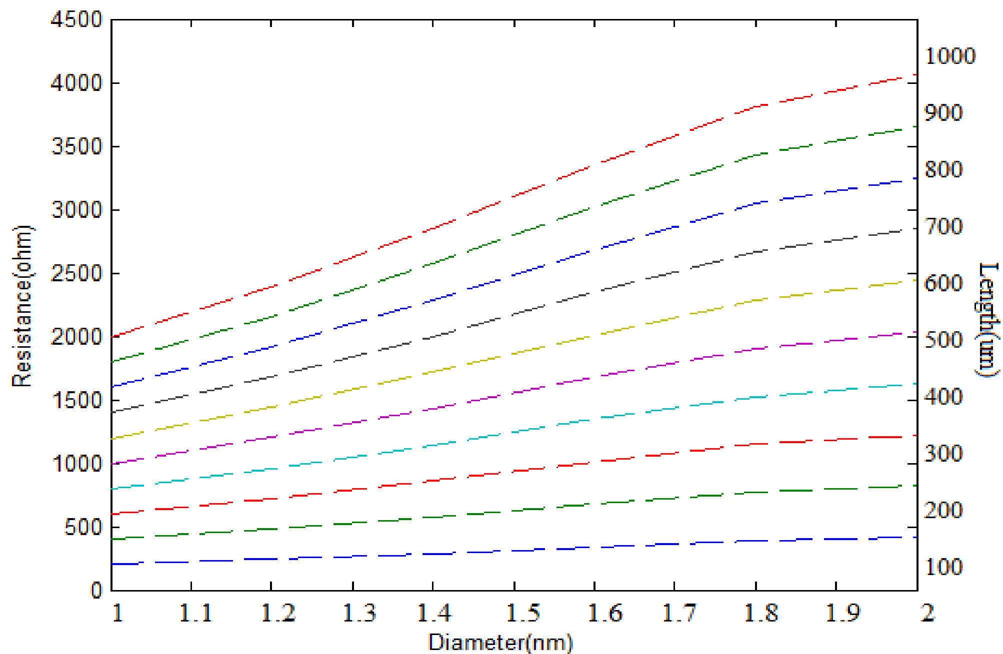

Figure3.14 Resistance vs. Diameter of SWCNT at 22nm technology node

Figure 3.13 and Figure 3.14 plots the value of resistance of single wall carbon nanotube with diameter ranging from 1nm to 2nm for lengths ranging from 100µm to 1000µm. As the

diameter is increasing, the number of CNTs that can be placed parallely in a bundle decreases that ultimately enhances the net resistance. As a result, resistance increases with the increase in length as well as diameter as shown above.

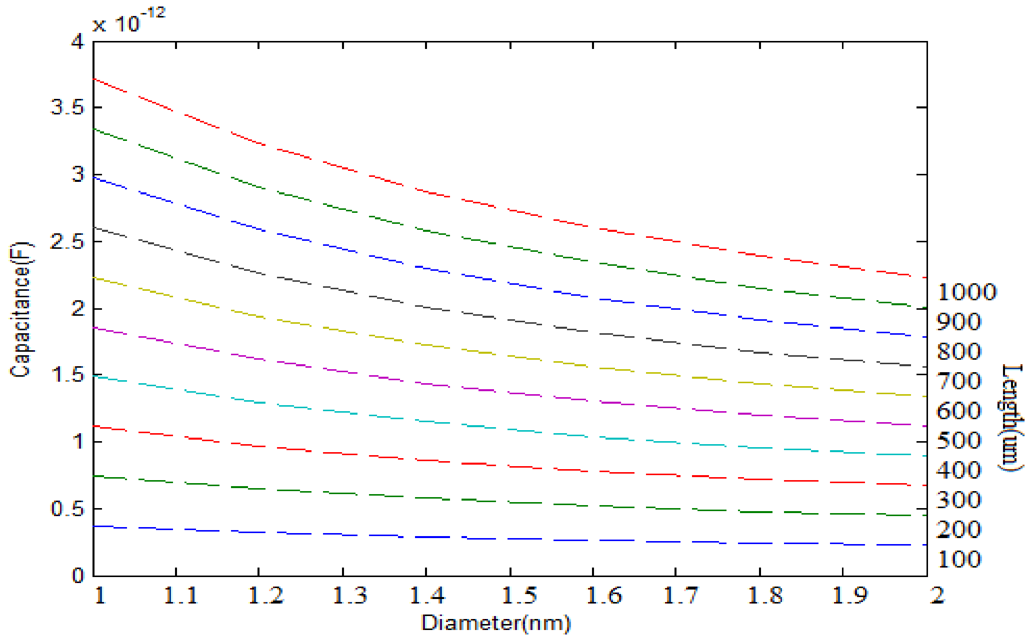

Figure3.15 Capacitance vs. Diameter of SWCNT at 32nm technology node

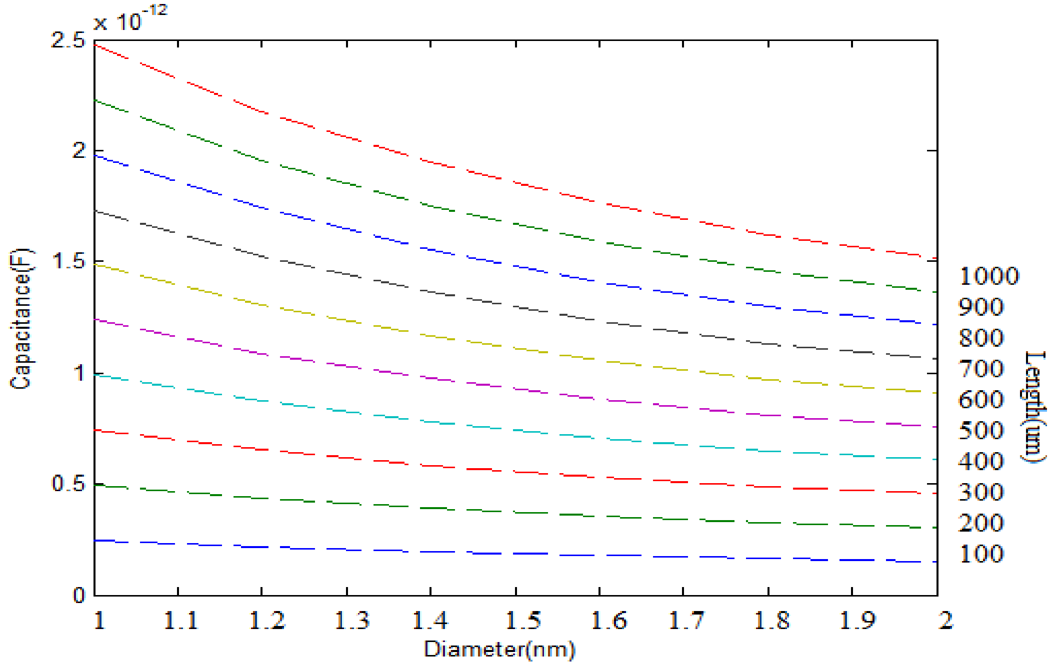

Figure3.16 Capacitance vs. Diameter of SWCNT at 22nm technology node

Figure 3.15 and Figure 3.16 plots the values of capacitance vs. diameter and length of SWCNT at 32nm and 22nm technology respectively. As the diameter increases, associated

capacitance of SWCNT decreases while it increases with length. Therefore, power dissipation is also more for SWCNT than copper.

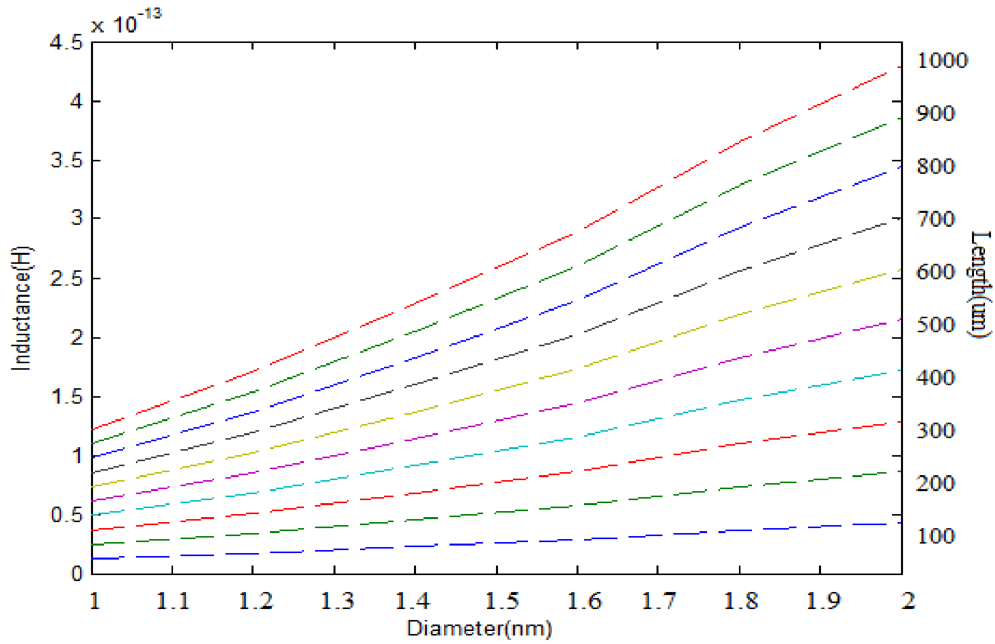

Figure3.17 Inductance vs. Diameter of SWCNT at 32nm technology node

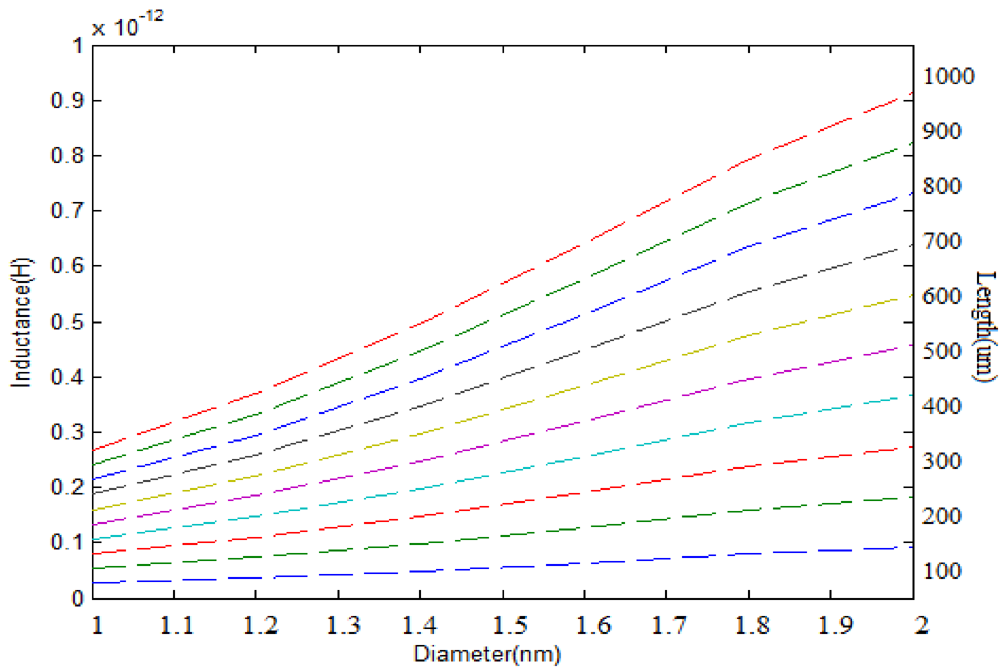

Figure3.18 Inductance vs. Diameter of SWCNT at 22nm technology node

Figure 3.17 and Figure 3.18 shows the effect of inductance of SWCNT bundle with diameter and length. Inductance of SWCNT increases with the increase in length and diameter. The values of parameters of CNT are then compared with the values of copper.

Table 3.1 Impedance Parameters of Copper and SWCNT at 32nm Technology

	Copper			SWCNT		
Length (μm)	**Resistance (ohms)**	**Capacitance (Farad)**	**Inductance (Henry)**	**Resistance (ohms)**	**Capacitance (Farad)**	**Inductance (Henry)**
200	1018.51	3.39×10^{-15}	3.26×10^{-10}	168.34	7.43×10^{-13}	2.44×10^{-14}
400	2037.03	6.79×10^{-15}	7.07×10^{-10}	335.84	1.49×10^{-12}	4.88×10^{-14}
600	3055.55	1.02×10^{-14}	1.11×10^{-9}	503.35	2.23×10^{-12}	7.31×10^{-14}
800	4074.07	1.36×10^{-14}	1.52×10^{-9}	670.85	2.97×10^{-12}	9.75×10^{-14}
1000	5092.59	1.69×10^{-14}	1.95×10^{-9}	838.36	3.71×10^{-12}	1.22×10^{-14}

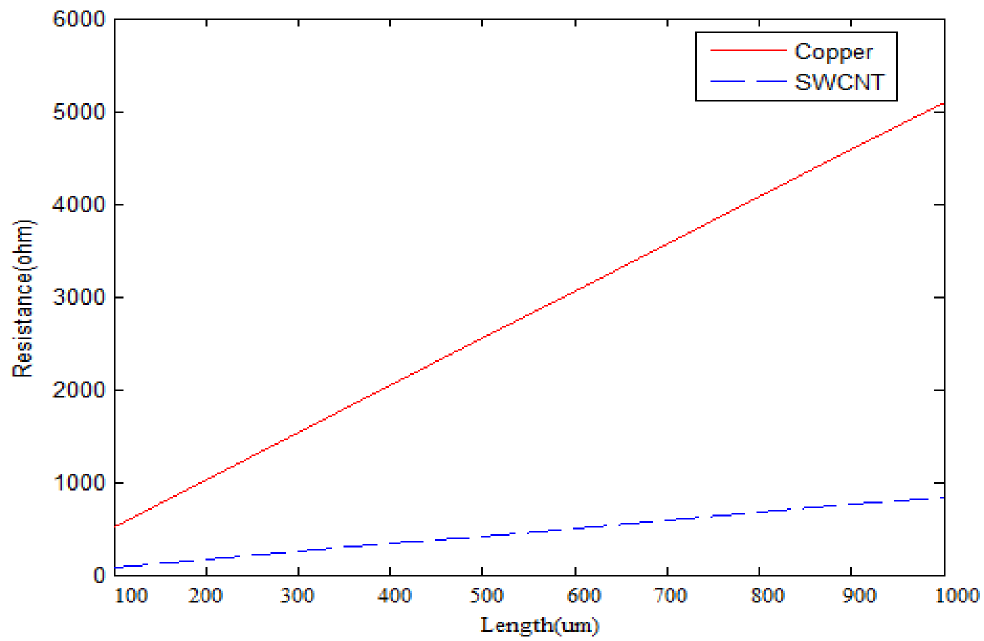

Figure 3.19 Comparison of Resistance between SWCNT and copper at 32nm technology

Table 3.2 Impedance Parameters of Copper and SWCNT at 22nm Technology

	Copper			SWCNT		
Length (μm)	**Resistance (ohms)**	**Capacitance (Farad)**	**Inductance (Henry)**	**Resistance (ohms)**	**Capacitance (Farad)**	**Inductance (Henry)**
200	2734.37	2.96×10^{-15}	3.42×10^{-10}	400.44	4.95×10^{-13}	5.35×10^{-14}
400	5468.75	5.92×10^{-15}	7.39×10^{-10}	798.89	9.89×10^{-13}	1.07×10^{-13}
600	8203.12	8.89×10^{-15}	1.16×10^{-9}	1197.34	1.48×10^{-12}	1.61×10^{-13}
800	10937.50	1.18×10^{-14}	1.59×10^{-9}	1595.79	1.98×10^{-12}	2.14×10^{-13}
1000	13671.87	1.48×10^{-14}	2.03×10^{-9}	1994.23	2.47×10^{-12}	2.68×10^{-13}

Table 3.1 and Table 3.2 shows calculated values of impedance parameters of copper and CNT bundle at 32nm and 22nm technology respectively and are obtained from the equations given in this chapter.

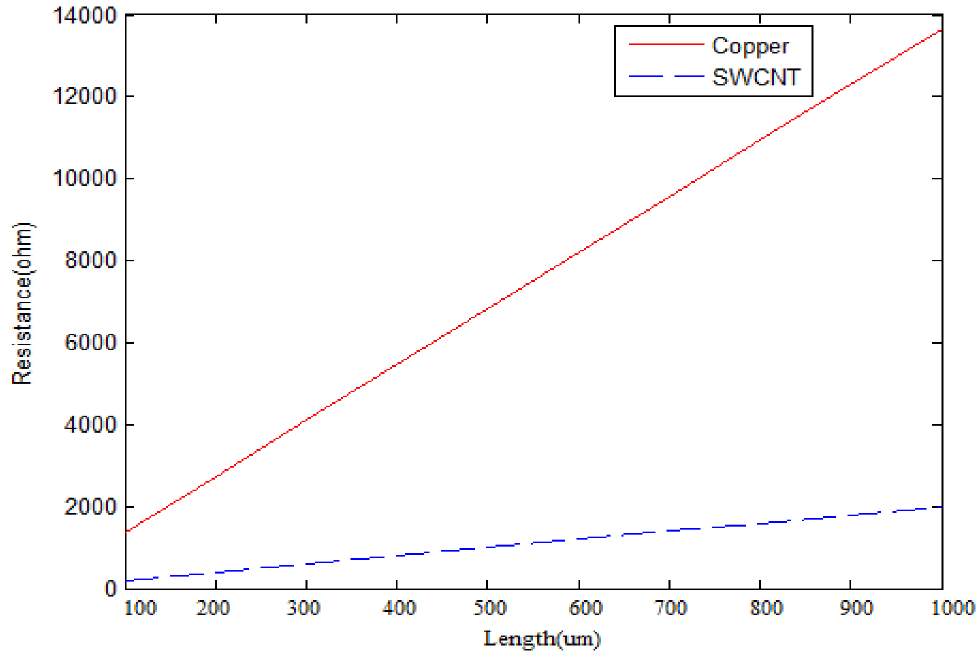

Figure 3.20 Comparison of Resistance between SWCNT and copper at 22nm technology

Figure 3.19 and Figure 3.20 compares the values of resistance of SWCNT with 1nm diameter and copper at 32nm and 22nm technology respectively. SWCNT has lower value of resistance than copper at both technology nodes. However, this difference increases and the value of resistance of copper becomes relatively more than SWCNT at 22nm technology than at 32nm technology. Thereby, it enhances the use of SWCNT at 32nm technology and below. Table 3.3 compares the resistance values of copper and CNT at different technologies.

Table 3.3 Comparison of resistance of Copper and SWCNT different technology nodes

	Resistance (ohms)	
Technology (nm)	**Copper**	**SWCNT**
45	2193.93	452.91
32	5092.59	838.36
22	13671.87	1994.24
14	37052.34	4153.59

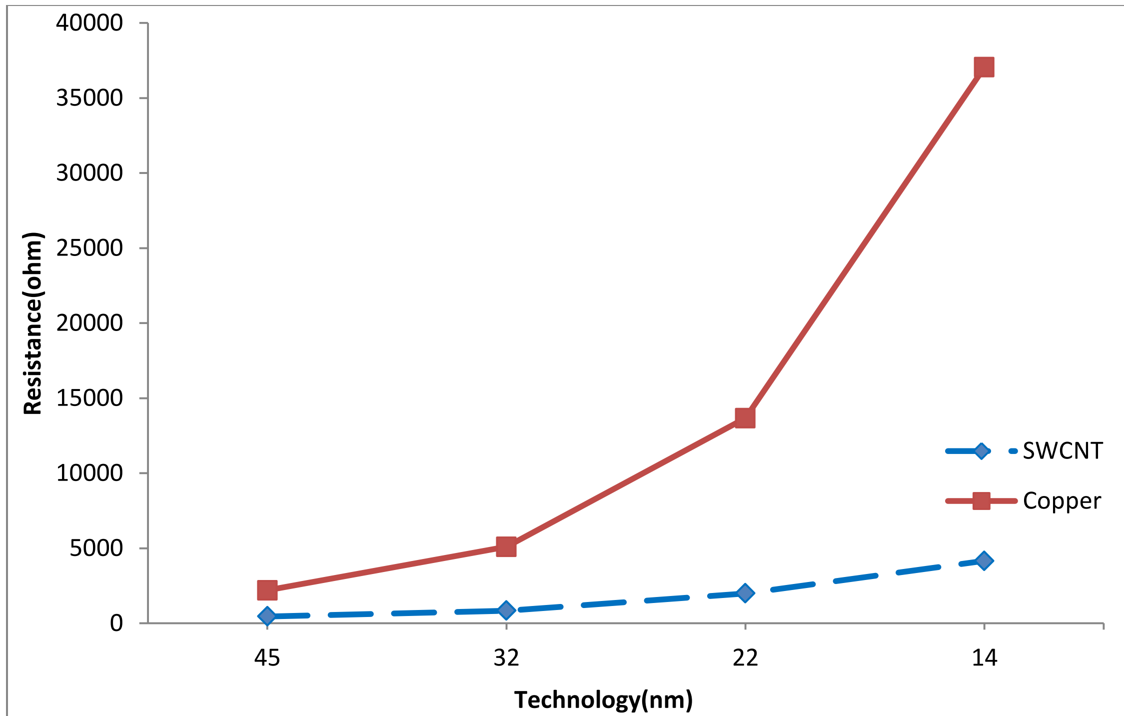

Figure 3.21 Comparison of Resistance between copper and SWCNT at different technology nodes

Figure 3.21 shows the difference in the values of resistance of SWCNT and copper at technology nodes from 45nm to 14nm. The figure shows very clearly that resistance increases for both CNT and copper with technology scaling. As shown at 45nm technology, although the value of resistance of copper is more than SWCNT, but this difference in values increases with technology advancement from 45nm to 14nm technology. This increase in gap is due to certain problems that prevail in copper at nano-scaled technologies beyond 45nm node.

CHAPTER 4

DELAY ANALYSIS

Propagation delay of the signal conveyed in the VLSI circuit is an important factor that determines the performance of the circuit. Delay should always be minimum to obtain high speed signal. Delay analysis of copper and SWCNT is done using the impedance values obtained in previous chapter. The obtained values help in performing analysis by Tanner EDA tool using spice model files at 32nm and 22nm technology nodes.

4.1 Parameters used for Simulation

Table 4.1 below shows values of different parameters as defined by ITRS at 32nm and 22nm technology used during simulation.

Table 4.1 ITRS 2005 based parameters for calculation at 32 nm and 22nm technology[1,21]

Parameters	32nm	22nm
Vdd	0.9	0.7
Width(w) of global interconnect	48nm	32nm
Aspect Ratio(global)	3	3
Thickness(H) of global interconnect	144nm	96nm
Width(w) of local interconnect	32nm	22nm
Aspect Ratio(local)	2	2
Thickness(H) of local interconnect	64nm	44nm
Diameter	1nm	1nm
Length(l)	1000µm	1000µm
Separation between adjacent bundle(global)	48nm	32nm
Separation between adjacent bundle(local)	32nm	22nm
ε	2.25	2.05

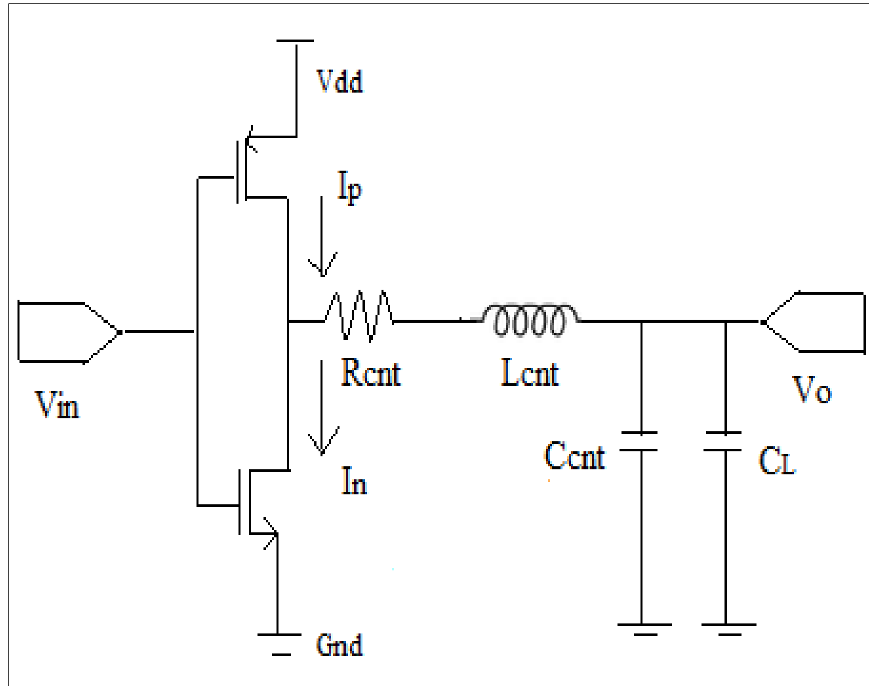

Figure 4.1 CMOS gate driving an Interconnect

Figure 4.1 shows an equivalent model in which CMOS gate is driving interconnect. As all impedance parameters increase with the interconnect length. Therefore, it becomes necessary to use repeaters. Repeaters are inserted in the circuit. By employing repeater insertion technique, long wires interconnect are divided into small segments and thereby it decreases propagation delay.

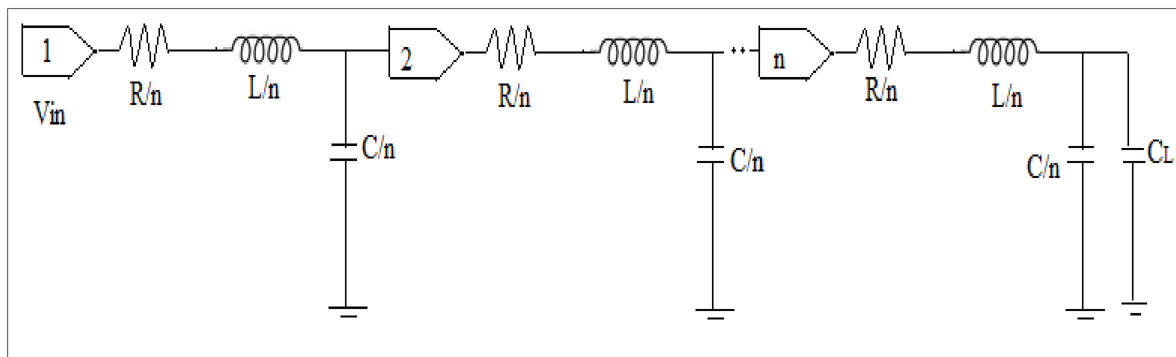

Figure 4.2 Repeater Insertion Techniques[10]

For inserting repeaters in the circuit, next aim is to obtain optimum number and optimum size of repeaters which is essential for minimizing delay. Since VLSI circuits also consider area an important factor. Large area overhead limits the size of IC by making it bulky. However, little compromise is often made as always a trade-off is faced between area and speed factor.

4.2 Repeater Optimization

The propagation delay(Γ) of interconnect[3] with the insertion of repeaters having size 'α' more than that of minimum sized inverter and with 'n' number of repeaters as shown in Figure 4.3 is given by equation(4.3).

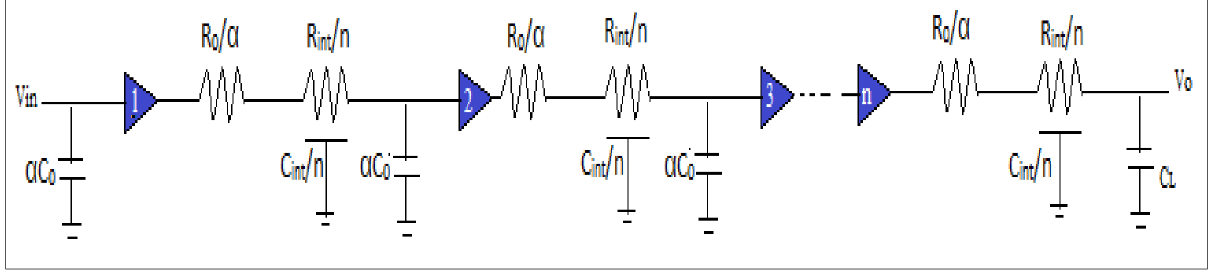

Figure 4.3 Optimal Repeaters[3]

$$\text{No. of Repeaters, n} = \sqrt{\frac{R_{int}C_{int}}{2.3\ R_0 C_0}} \tag{4.1}$$

$$\text{Size of inverter, } \alpha = \sqrt{\frac{R_0 C_{int}}{R_{int} C_0}} \tag{4.2}$$

where, R_{int} and C_{int} are resistance and capacitance of interconnect and R_o and C_o are the output resistance and input capacitance of driver transistor. The shortest delay can be obtained if the delay of the segments connected by the repeaters across a line becomes comparable with that of a repeater.

$$\Gamma = n\left(2.3\ \frac{R_o}{\alpha}\left(\frac{C_{int}}{n} + \alpha C_o\right) + \frac{R_{int}}{n}\left(\frac{C_{int}}{n} + 2.3\alpha C_o\right)\right) \tag{4.3}$$

For global lengths, C_{int} is of the order of pico-farads(10^{-12} F) and C_o is of the order of femto-farads(10^{-15}F) , and R_{int} and R_{tr}, have values around kilo-ohms(kΩ); therefore, $R_oC_{int} >> R_{int}C_o$, and the time delay expression in equation(4.3) can be simplified in equation(4.4) as-

$$\Gamma = 2.3\ R_o C_o \tag{4.4}$$

To drive large RC loads, Repeaters are a good choice and can be used efficiently.

4.2.1 Optimum Number of Repeaters

Propagation delay of the signal passed in the circuit increases with the square relation to the length of interconnect due to the fact that capacitance and resistance which helps in determining RC time delay constant of the signal increases linearly with the length when

interconnects resistance is larger or even equal to the conducting/on- resistance of the driver driving the circuit[19]. To convey a signal at longer lengths i.e. globally repeaters are used extensively. Hence, next step is to determine optimum number of repeaters.

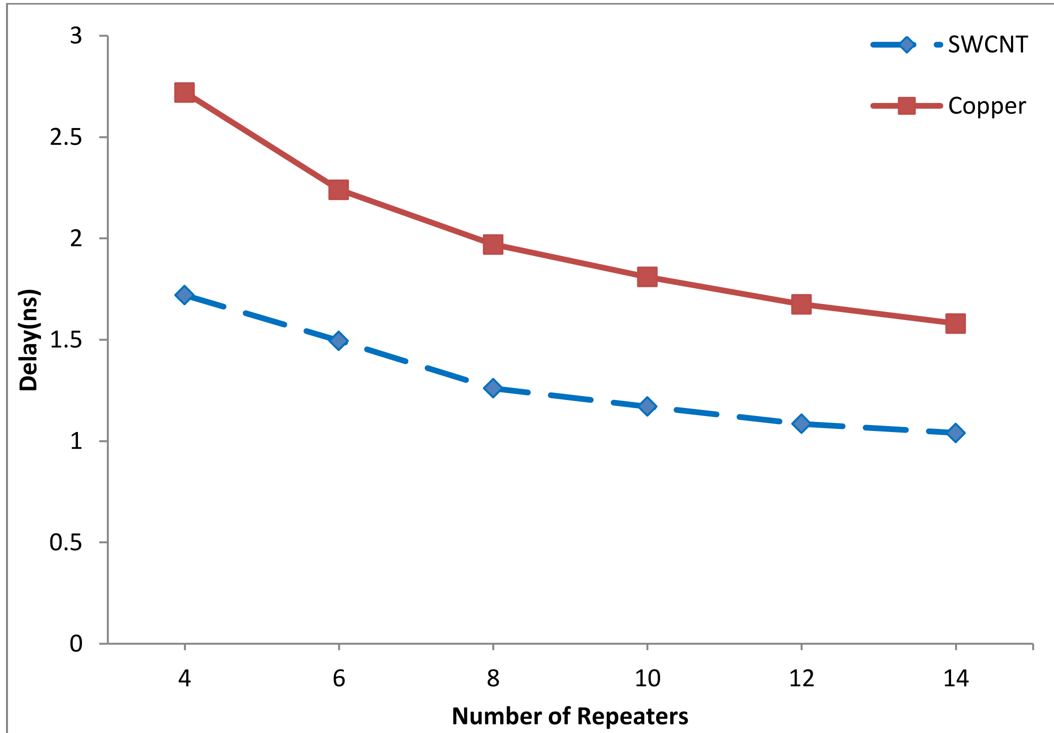

Figure 4.4 Delay vs. Number of Repeaters of CNT and copper

Figure 4.4 reveals average propagation delay of signal versus number of repeaters of SWCNT and copper. The graph clearly shows that with the increase in number of repeaters, since as the number of repeaters inserted increases; the long wire segment gets divided into more sub-sections resulting in the decrease of impedance parameters; it finally reduces delay.

The above can also be used to compare the delay of SWCNT and copper interconnect. Irrespective of the number or repeaters, at all points, the delay of copper is more than delay of SWCNT Bundle Interconnect. This is due to the fact that the value of resistance is more in copper than CNT.

4.2.2 Optimal Sizing of Driver Transistor

Table 4.2 shows values of average delay of copper and CNT at 32nm and 22nm technology using different number of repeaters. Figure 4.5 and Figure 4.6 plots propagation delay as

function of driver transistor size at different number of repeaters ranging from eight to twelve for Copper and SWCNT Bundle interconnects respectively. It is evident from figures that with the increase in size of driver transistor, resistance will reduce and capacitance increases; also with the increase in number of repeaters and number of sub-sections, delay will reduce rapidly by decreasing impedance values for global lengths of interconnect wires.

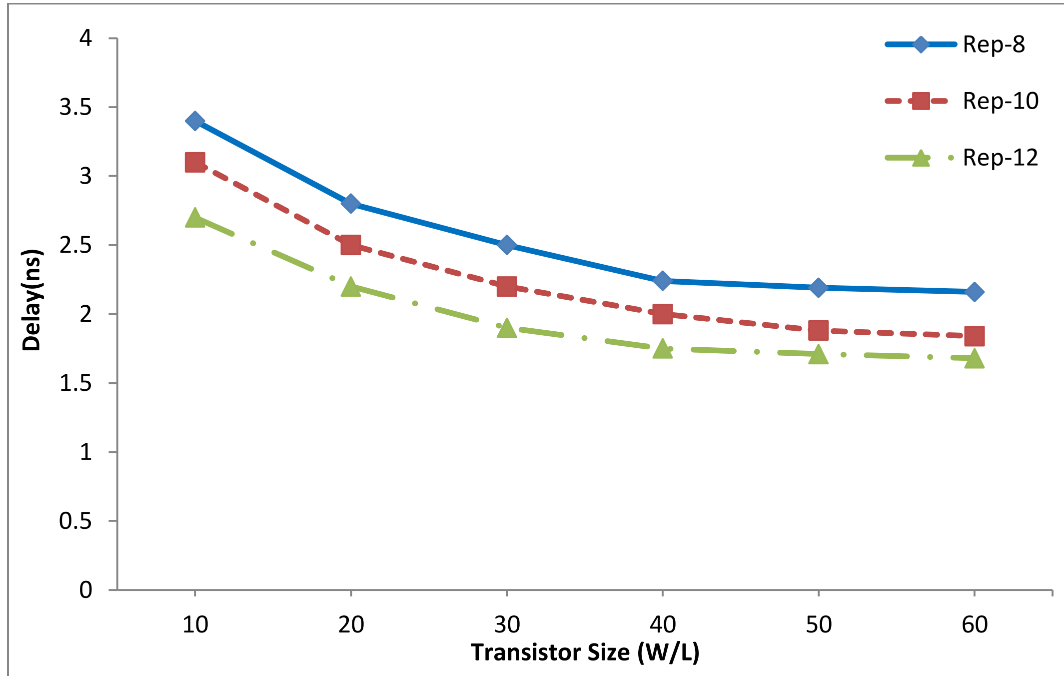

Figure 4.5 Delay vs. Transistor Size at different Repeaters of copper

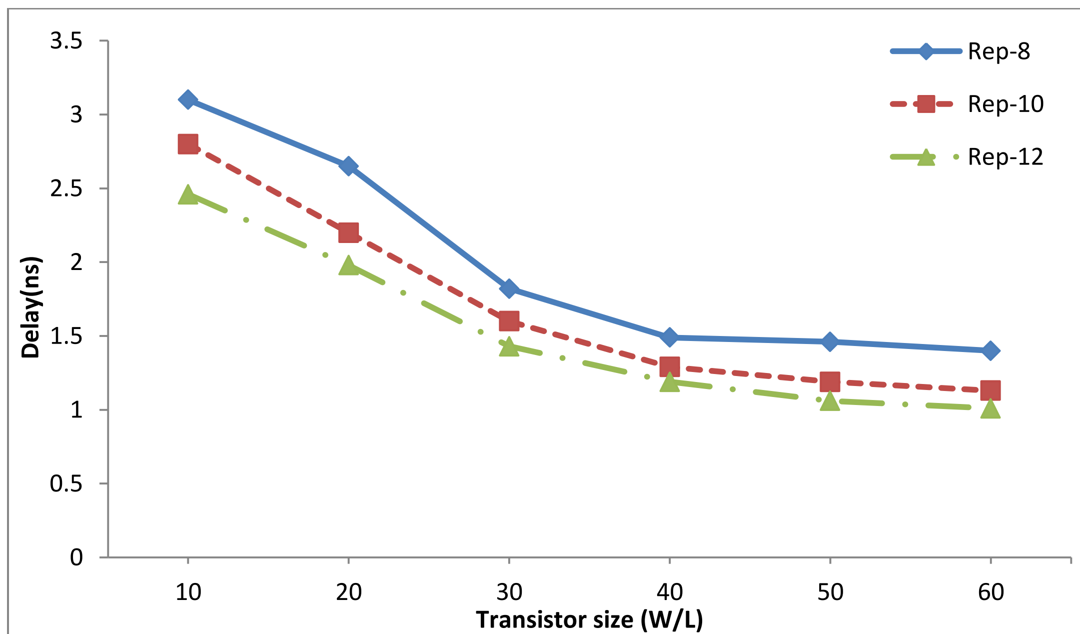

Figure 4.6 Delay vs. Transistor Size at different Repeaters of SWCNT

Table 4.2 Average Delay of copper and CNT using 8, 10 and 12 Repeaters

Transistor Size (W/L)	**Delay of Copper (ns)**			**Delay of SWCNT (ns)**		
	Rep-8	**Repe10**	**Rep-12**	**Rep-8**	**Rep-10**	**Rep-12**
10	3.4	3.1	2.7	3.1	2.8	2.46
20	2.8	2.5	2.2	2.65	2.2	1.98
30	2.5	2.2	1.9	1.82	1.6	1.43
40	2.24	2	1.75	1.49	1.29	1.19
50	2.19	1.88	1.71	1.46	1.19	1.06
60	2.16	1.84	1.68	1.4	1.13	1.01

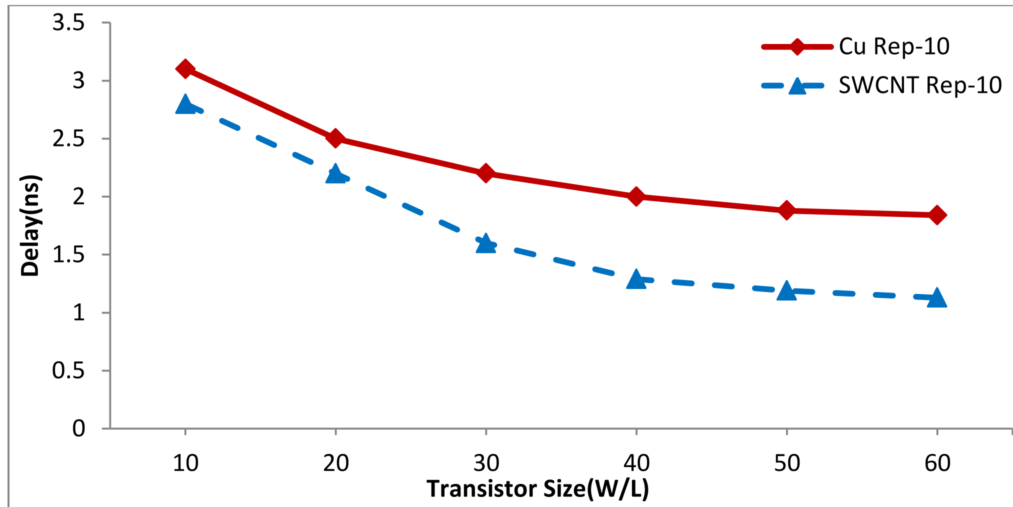

Figure 4.7 Comparison of Delay vs. Transistor Size of copper and SWCNT using 10 Repeaters

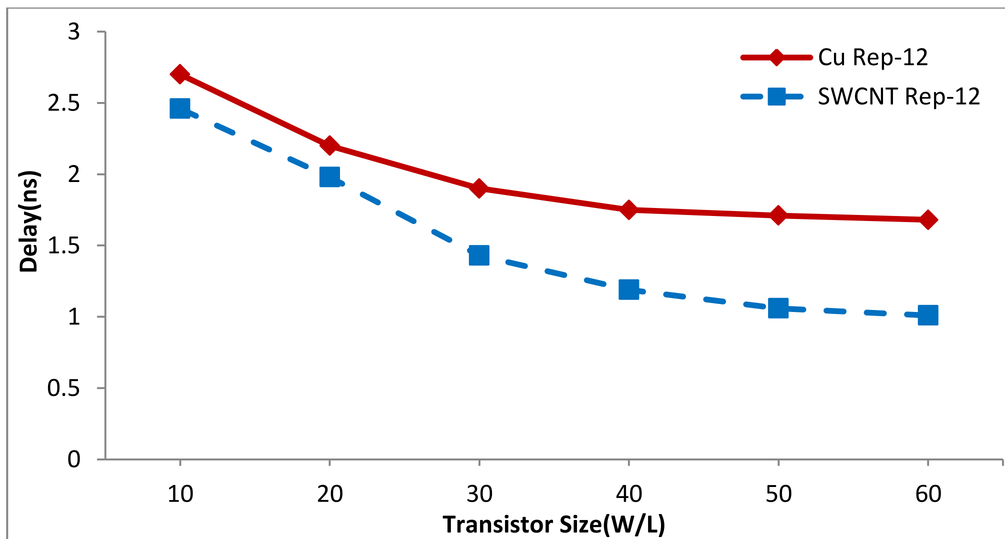

Figure 4.8 Comparison of Delay vs. Transistor Size of copper and SWCNT using 12 Repeaters

Figure 4.7 and Figure 4.8 represents the comparison of delay versus size of driver transistor for 10 and 12 repeaters for both copper and CNT interconnect respectively. For both interconnects, increasing number of repeaters and driver size reduces delay undoubtedly. Also for the same number of repeaters in Copper and SWCNT, copper exhibits more delay than CNT Bundle due to more resistance than CNT. Therefore, SWCNT provides high speed interconnect in VLSI applications.

4.3 Delay Comparison of SWCNT and Copper

Propagation delay should always be a smaller value for transferring signal in high speed VLSI applications. Table 4.3 shows values of normalized delay for 32nm and 22nm technology with variation in length of interconnects. Figure 4.9 and Figure 4.10 shows normalized delay results obtained from Tanner tool using model files for 32nm and 22nm technologies at 0.1 GHz frequency of operation.

Table 4.3 Normalized Delay at 32nm and 22nm technology with Length Variation

Length(µm)	**Normalized Delay (Γ_{CNT}/Γ_{CU}) At 32nm technology**	**Normalized Delay (Γ_{CNT}/Γ_{CU}) At 22nm technology**
200	0.660	0.575
400	0.501	0.489
600	0.426	0.420
800	0.419	0.380
1000	0.406	0.376

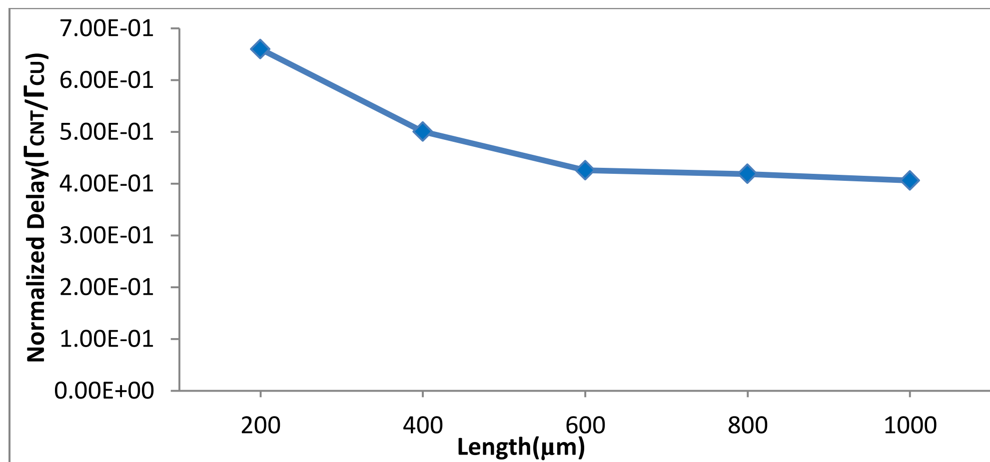

Figure 4.9 Normalized Delay(Γ_{CNT}/Γ_{CU}) vs. Length of Interconnect at 32nm technology

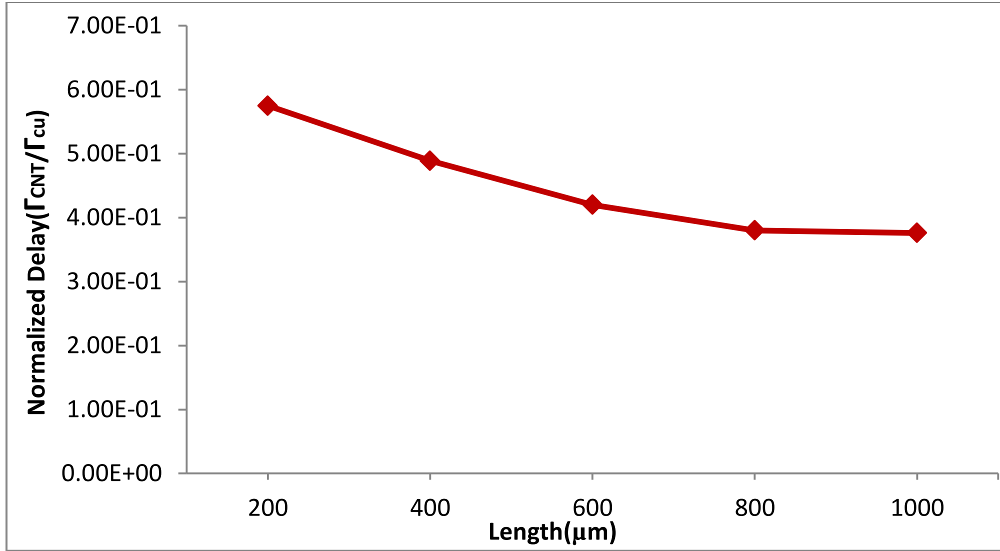

Figure 4.10 Normalized Delay(Γ_{CNT}/ Γ_{CU}) vs. Length of Interconnect at 22nm technology

Normalized delay is calculated by dividing propagation delay of CNT with that of copper. Result reveals that since propagation delay of copper is more than CNT, hence normalized delay is a value less than unity. And also the results are much better at 22nm technology node. Hence, CNT bundle can replace copper interconnects.

Table 4.4 Normalized Delay at 32nm and 22nm technology with diameter variation of CNT

Diameter(nm)	**Normalized Delay (Γ_{CNT}/ Γ_{CU}) At 32nm technology**	**Normalized Delay (Γ_{CNT}/ Γ_{CU}) At 22nm technology**
1.0	0.427	0.372
1.2	0.433	0.405
1.4	0.452	0.434
1.6	0.463	0.444
1.8	0.473	0.469
2.0	0.494	0.487

Table 4.4 shows values of normalized delay for 32nm and 22nm technology with variation in diameter of nanotube interconnects. Figure 4.11 and Figure 4.12 shows normalized delay as a function of diameter of CNT bundle interconnect ranging from 1nm-2nm for 32nm and 22nm technology respectively. Normalized delay is value less than unity and represents that with

increase in diameter of CNT bundle interconnect, resistance increases, but delay of copper is independent with diameter; hence value of normalized delay will increase with increase in diameter of CNT bundle interconnect. But delay of CNT bundle is always less than copper at entire diameter range and at both technologies.

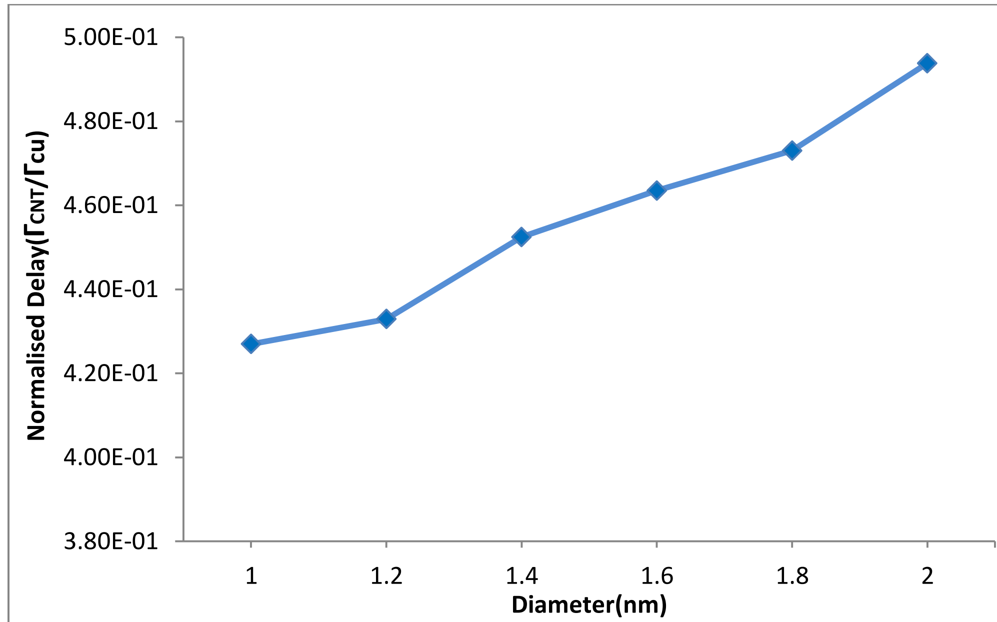

Figure 4.11 Normalized Delay($\Gamma_{CNT}/\ \Gamma_{CU}$) vs. Diameter of SWCNT Interconnect at 32nm technology

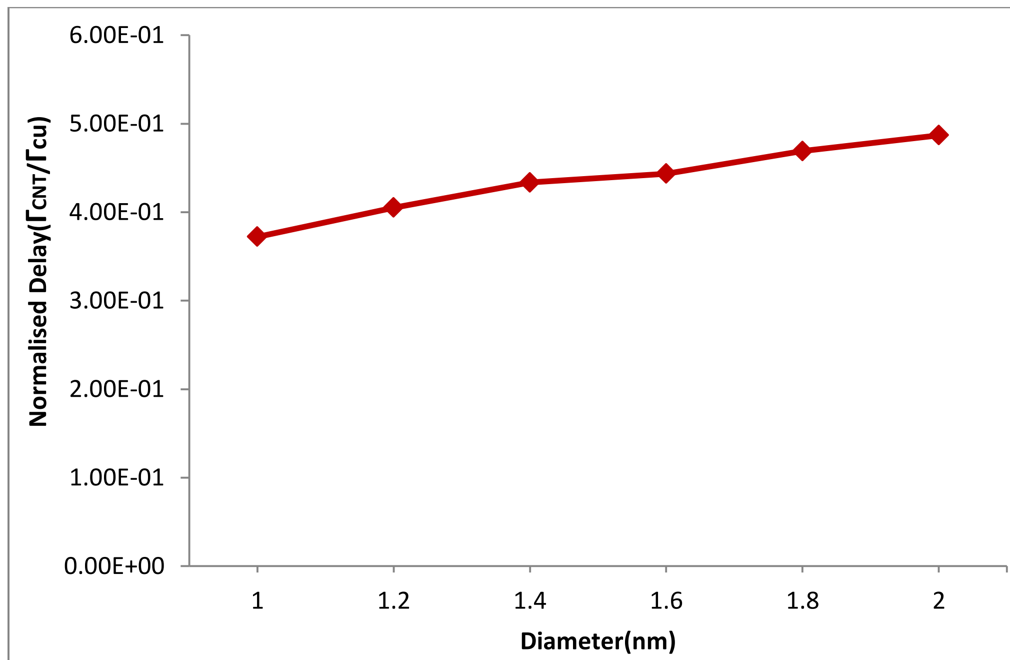

Figure 4.12 Normalized Delay($\Gamma_{CNT}/\ \Gamma_{CU}$) vs. Diameter of SWCNT Interconnect at 22nm technology

CHAPTER 5

EFFECT OF TEMPERATURE

The prime-most demands that are driving todays VLSI design industry are “Smaller” and “Faster” and they mean high performance than existing higher. However, certain issues like high power densities, high operating temperature and thus, reduced reliability are faced. The thermal effects are one of the most important considerations of VLSI designers with increased scaling and increased packing densities of the circuits. Due to increased variation of process parameters in nanometer regime CMOS technologies, thermal issues can seriously limit IC operations. Most of the IC failures are due to thermal issues only. So, temperature relation in VLSI circuits needs to be analyzed thoroughly. To understand the effect of thermal conductance i.e. rise in temperature and the integrity of manufacturing process is indispensable for the successful working of any electronic circuit.

High performance VLSI circuits have to operate with great variance in temperature range from 250K to 450K. This large temperature variation have a tremendous effect on the propagation delay of signal passing through the interconnect material. This is only possible by studying different parameters of the circuit that are temperature dependent and can affect its performance. This chapter includes the equations and the dependence of the parameters of copper and metallic SWCNT interconnects with temperature that change due to rise in temperature above room conditions. Several effects that arise in CNT above room temperature have been captured to take temperature dependence into account. Different types of phonon scattering mechanisms in metallic SWCNT bundle interconnects that reduce electron mean free path have been studied. Further their delay analysis and then conductance comparison is done at different lengths of interconnect and at different diameters of the CNT employed in circuit. Studies also show that longer length interconnects has better capability of handling signal at high temperature range. Based on the simulation results, it is shown that SWCNT bundle interconnects offer more reduction in delay at elevated temperature range above 300K.

5.1 Temperature Dependent Resistance of Copper

The resistivity of copper as an interconnect material is also affected by temperature and is expressed in terms of temperature[17] as-

$$\rho(T) = \rho_0[\,1 + 0.0039(T - T_0)] \tag{5.1}$$

In the above equation, $T_0 = 300K$, T is temperature in Kelvin ranging from 250K to 450K and ρ_0 is temperature independent resistivity and has values 3.52×10^{-8} Ωm and 4.2×10^{-8} Ωm respectively for global interconnects[16]. Thus, the temperature dependent resistance of Copper Interconnect is-

$$R_{Cu} = \rho(T)(\frac{l}{w.t}) \tag{5.2}$$

Where, ρ(T) is the temperature dependent resistivity of copper.

5.2 Temperature Dependent Resistance of SWCNT Bundle Interconnect

SWCNT Bundle temperature dependent resistance is determined by considering the effect of temperature on electron mean free paths of elastic acoustic and inelastic optical phonons due to considerable scattering at high temperature which may drastically affect the performance of device and degrade its operation[9]. The electron-electron scattering is negligible and does not contribute in thermal conduction and the main cause of scattering is electron-phonon scattering in metallic CNTs at high temperatures. The electron-phonon scattering mean free path λ metallic SWCNTs can be written as-

$$\lambda = v_f\, t \tag{5.3}$$

Where, v_f is the velocity of electron is considered comparable to Fermi velocity (8×10^5 m/s) and *t* is the mean free time between electron phonon scattering. The main source of resistance at low temperature in metallic SWCNT is acoustic scattering which is directly dependent on temperature, diameter of CNT bundle and mean free path[9,23]. As a function of temperature and MFP at 300K, the elastic Acoustic scattering MFP $(\lambda)_{AC}$is expressed as-

$$(\lambda)_{AC} = (\lambda)_{AC,300}(\frac{300}{T}) \tag{5.4}$$

Where,$(\lambda)_{AC,300}$=1600nm is the standard given and is described as acoustic scattering MFP length at room temperature(300K). For temperature higher above room temperature conditions, electrons get accelerated by the electric field and acquires sufficient kinetic

energy to reach optical phonon energy level($h\Omega$=0.16-0.2eV). SWCNTs with larger values of diameter have their sub-bands extended to Fermi level that plays role in its conductance by creating channels for the flow of electrons. The optical phonon occupation is defined as the density of states for the final electron state after scattering and is given by equation below as-

$$N_{OP}(T) = \frac{1}{[\exp(h\Omega/k_B T) - 1]} \tag{5.5}$$

Where, k_B is the Boltzmann constant and its value is 1.38×10^{-23}J/K. Depending upon the optical phonon occupation states optical absorption length$(\lambda)_{OP,abs}$ is given by-

$$(\lambda)_{OP,abs}(T) = (\lambda)_{OP,300}\frac{N_{OP}(300)+1}{N_{OP}(T)} \tag{5.6}$$

Where, $(\lambda)_{OP,300}$=15nm is defined for spontaneous OP emission length at 300K. Optical inelastic emission $(\lambda)_{OP,ems}$ can occur in two ways i.e. after these excited electrons gain sufficient energy from the electric field; in simple words certain distance that electron needs to cover and gain some energy to emit phonon and second term is for energy related after an optical absorption event(abs) i.e. distance that an electron traverse before emission of phonon and after gaining enough energy and is expressed as sum of two as written below-

$$(\lambda)_{OP,ems} = \left(\frac{1}{(\lambda)_{OP,ems^{fld}}} + \frac{1}{(\lambda)_{OP,ems^{abs}}}\right)^{-1} \tag{5.7}$$

The net optical field emission $(\lambda)_{OP,ems}^{fld}$ helps in determining the distance electrons of average energy $k_B T$ should travel in the electric field F=V/L needed to overcome the Optical emission threshold energy and in relating the temperature beyond this threshold with optical emission length and is expressed as sum of two as-

$$(\lambda)_{OP,ems}^{fld}(T) = \frac{(h\Omega_{OP} - k_B T)}{qV/L} + (\lambda)_{OP,300}\frac{N_{OP}(300)+1}{N_{OP}(T)+1} \tag{5.8}$$

The temperature dependent Optical Absorption Emission MFP $(\lambda)_{OP,ems}^{abs}$beyond the threshold is obtained as-

$$(\lambda)_{OP,ems}^{abs}(T) = (\lambda)_{OP,abs}(T) + (\lambda)_{OP,300}\frac{N_{OP}(300)+1}{N_{OP}(T)} \tag{5.9}$$

The elastic acoustic scattering, inelastic optical emission and absorption scattering phenomenon contribute to give $(\lambda)_{eff}$ as-

$$(\lambda)_{eff} = ((\lambda)_{AC}^{-1} + (\lambda)_{OP,ems}^{-1} + (\lambda)_{Op,abs}^{-1})^{-1} \tag{5.10}$$

The total resistance is given as the sum of Contact Resistance(R_c)which depends on the metal used in contact with CNT(almost 24k for Palladium), intrinsic quantum resistance(R_i) which is diameter and temperature dependent due to four parallel conducting channels in SWCNT bundle and due to scattering due to successive collisions between electron and phonon depending upon CNT length(L), CNT diameter(d), bias voltage(V), and temperature(T)[9,11]. Taking only the effect of temperature into account the resistance is given as-

$$R(T) = R_c + \frac{h}{2\,N(T).e^2}\left[1 + \frac{L}{\lambda_{eff}(T)}\right] \tag{5.11}$$

Where, h is the Planck's constant (6.62×10^{-34} m^2kg/sec), e is the electron charge(1.6×10^{-19} C); N is the number of conducting channels and $(\lambda)_{eff}$ is the average distance that an electron travels between successive scatterings at elevated temperature range and is called as effective mean free path (MFP) of an electron.

5.3 Simulation Results

The temperature dependent impedance parameters i.e. resistance for copper and CNT are calculated using the equations given in this chapter in sections 5.1 and 5.2.

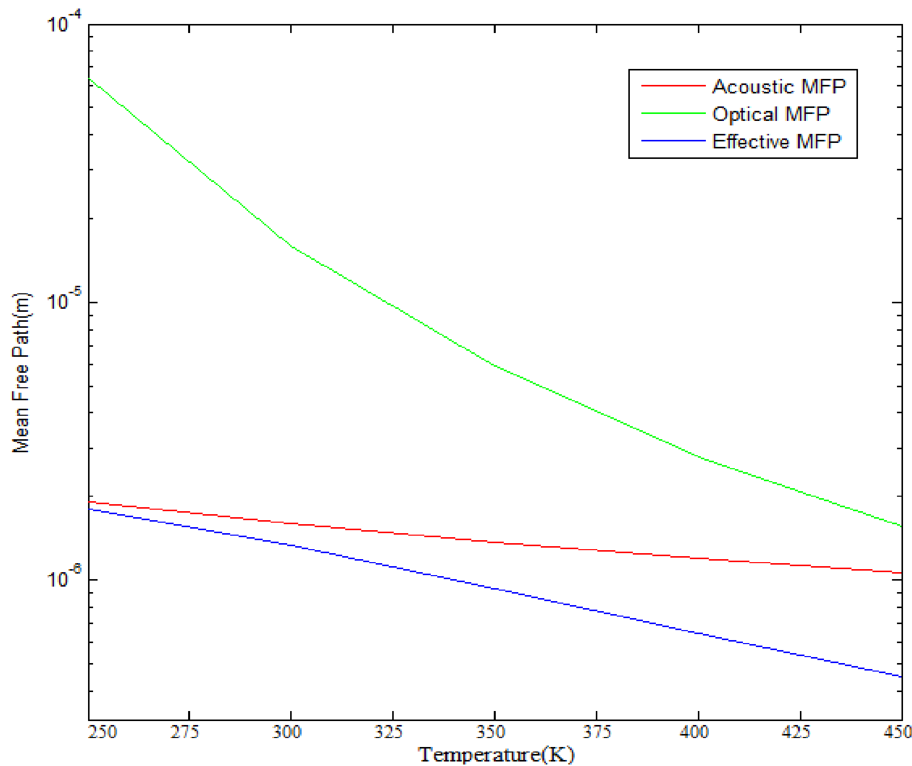

Figure 5.1 Dependence of MFP with Temperature

Table 5.1 Values of MFP over Temperature range250K-450K)

Temperature(K)	Acoustic MFP (m)	Optical MFP (m)	Effective MFP (m)
250	1.920×10^{-6}	6.3785×10^{-5}	1.8109×10^{-6}
300	1.600×10^{-6}	1.5853×10^{-5}	1.3311×10^{-6}
350	1.371×10^{-6}	5.8652×10^{-6}	9.3406×10^{-7}
400	1.201×10^{-6}	2.7822×10^{-6}	6.4344×10^{-7}
450	1.066×10^{-6}	1.5575×10^{-6}	4.4888×10^{-7}

Table 5.1 shows values of mean free path over wide temperature range(250K-450K). Figure 5.1 reveals that at room temperature, elastic acoustic mean free path is dominant at low bias (for E= 200V/cm or 60 mV across 3µm length of interconnect tube.) However, with the increase in temperature above room temperature, inelastic optical phonon scattering increases and also comes into scene. Both acoustic and optical scattering are summed up to give net effective mean free path. As a result, net effective mean free path decreases with rise in temperature. This decrease in effective mean free path leads to increase in the resistance of CNT material. Finally, propagation delay of the signal used in circuit is increased.

Table 5.2 Values of Temperature dependent resistance of copper and CNT
at 32nm and 22nm technology

Temperature (K)	Resistance of Copper (ohms)		Resistance of CNT (ohms)	
	32nm Tech.	**22nm Tech.**	**32nm Tech.**	**22nm Tech.**
250	4099.537	11005.859	1597.439	3806.161
275	4596.065	12338.867	1849.264	4406.176
300	5092.593	13671.875	2168.700	5167.284
325	5589.12	15004.883	2575.065	6135.515
350	6085.648	16337.891	3085.743	7352.29
375	6582.176	17670.898	3715.167	8851.995
400	7078.704	19003.906	4474.352	10660.88
425	7575.231	20336.914	5370.854	12796.94
450	8071.759	21669.922	6409.0133	15270.52

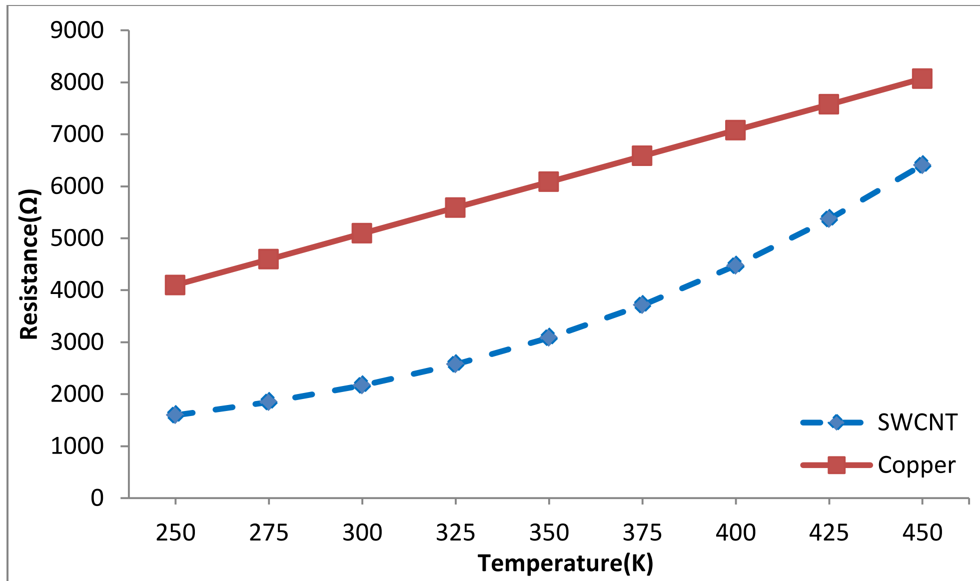

Figure 5.2 Comparison of Temperature dependent resistances of CNT and copper at 32nm technology

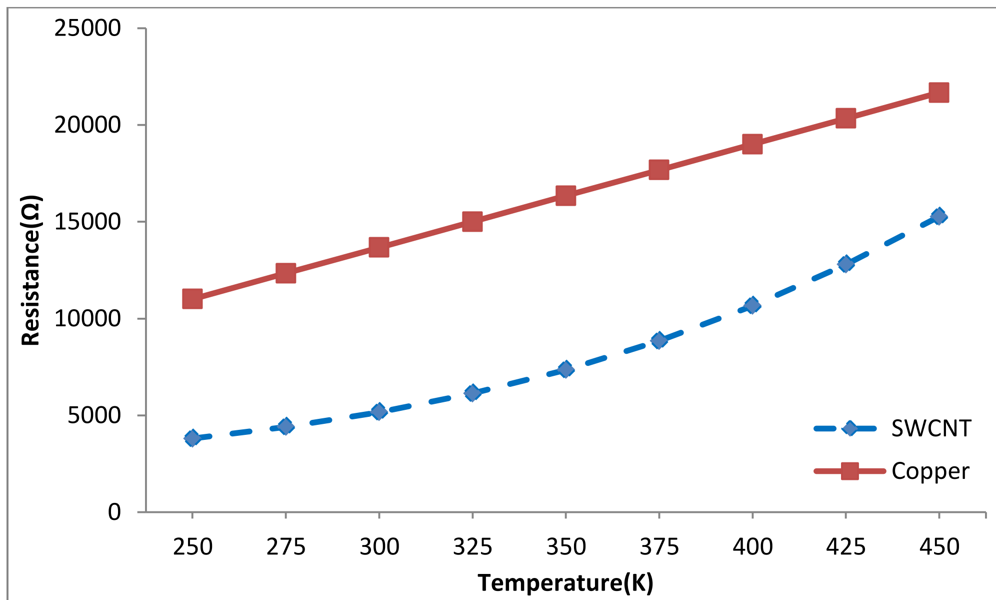

Figure 5.3 Comparison of Temperature dependent resistances of CNT and copper at 22nm technology

Table 5.2 shows temperature dependent resistance values for copper and CNT at 32nm and 22nm technology. As shown in Figure 5.2 and Figure 5.3 above resistance of interconnect increases with the increase over a wide temperature range. The reason behind increase in resistance with temperature is the facts that effective mean free path shows decrease at elevated temperatures due to electron-phonon scattering phenomenon. On the other hand, CNT has its electron MFP in the range of microns as compared to few tens of nm paths of

that of copper material. However, at both 32nm and 22nm technologies copper offers more resistance than SWCNT bundle.

Table 5.3 Delay Comparison of copper and CNT over Temperature range (200K-450K) for L=1000μm

Temperature (K)	Delay of Copper (ns)		Delay of CNT (ns)		Normalized Delay (Γ_{CNT}/Γ_{CU})	
	32nm Tech.	22nm Tech.	32nm Tech.	22nm Tech.	32nm Tech.	22nm Tech
200	8.65×10^{-10}	1.93×10^{-9}	6.83×10^{-10}	1.12×10^{-9}	0.789	0.582
250	1.02×10^{-9}	2.41×10^{-9}	7.53×10^{-10}	1.27×10^{-9}	0.739	0.527
275	1.11×10^{-9}	2.65×10^{-9}	7.66×10^{-10}	1.43×10^{-9}	0.692	0.539
300	1.19×10^{-9}	2.87×10^{-9}	8.28×10^{-10}	1.52×10^{-9}	0.695	0.531
325	1.29×10^{-9}	3.09×10^{-9}	9.10×10^{-10}	1.73×10^{-9}	0.708	0.561
350	1.35×10^{-9}	3.28×10^{-9}	1.01×10^{-9}	1.96×10^{-9}	0.751	0.597
375	1.42×10^{-9}	3.47×10^{-9}	1.13×10^{-9}	2.19×10^{-9}	0.798	0.632
400	1.49×10^{-9}	3.61×10^{-9}	1.29×10^{-9}	2.47×10^{-9}	0.862	0.684
425	1.56×10^{-9}	3.79×10^{-9}	1.44×10^{-9}	2.94×10^{-9}	0.926	0.774
450	1.65×10^{-9}	3.99×10^{-9}	1.58×10^{-9}	3.39×10^{-9}	0.961	0.851

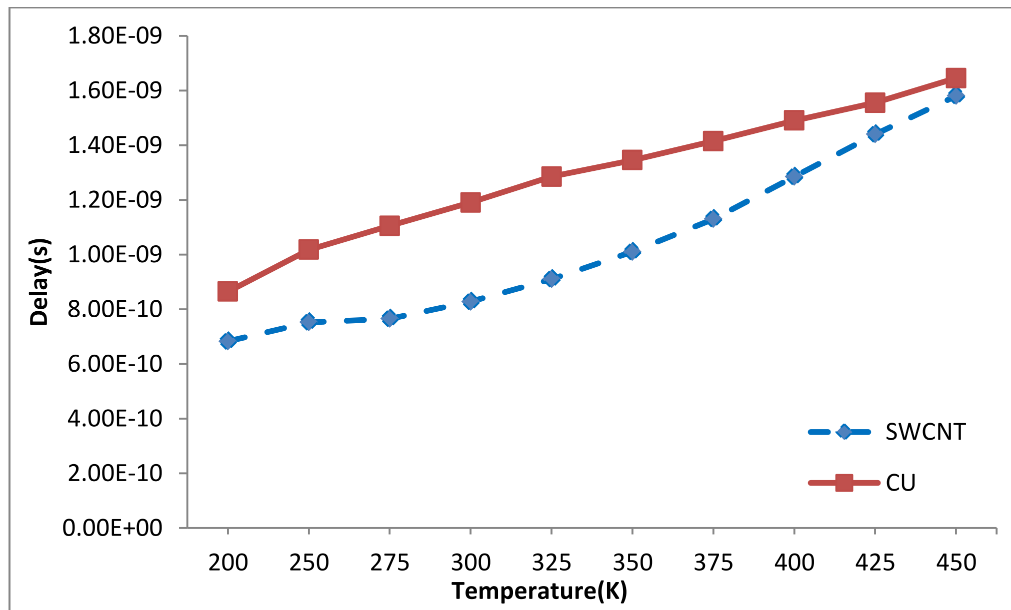

Figure 5.4 Delay Comparison of CNT bundle and copper at 32nm technology over Temperature range (200K-450K) at L=1000μm

Table 5.3 shows values of average and normalized delay for copper and CNT at 32nm and 22nm technology for global length of interconnect at 1000μm. Figure 5.4 and Figure 5.5 compares the delay of copper and CNT interconnect at 32nm (0.125 GHz frequency) and 22nm (0.3 GHz frequency) technology respectively, concluding that copper has more delay and thus CNT is a better choice than copper for high speed interconnect applications.

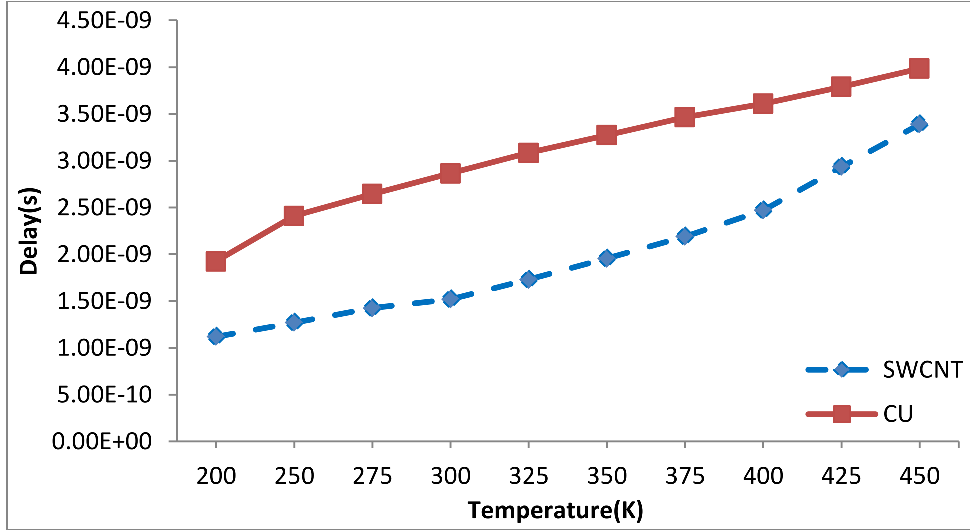

Figure 5.5 Delay Comparison of CNT bundle and copper at 22nm technology over Temperature range (200K-450K) at L=1000μm

Figure 5.6 shows the results for normalized delay for analyzing temperature dependent performance of CNT and copper. Since, delay of CNT is far less than that of copper, hence depicting CNT as better substitute for copper at nano-scaled technologies.

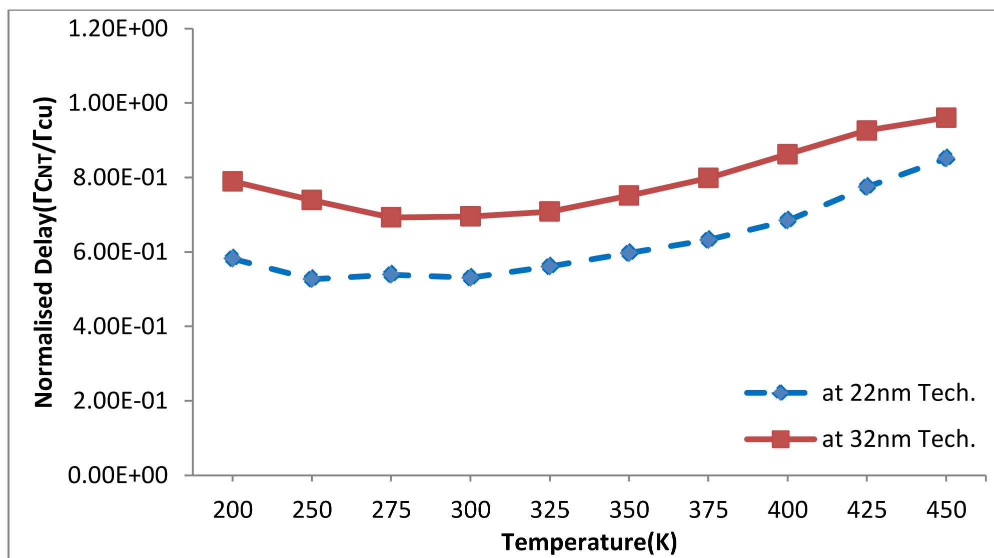

Figure 5.6 Normalized Delay over Temperature range (200K-450K) at L=1000μm

Table 5.4 Delay Comparison of copper and CNT over Temperature range (200K-450K) for L=500µm

Temperature (K)	Delay of Copper (ns)		Delay of CNT (ns)		Normalized Delay	
	32nm Tech.	22nm Tech.	32nm Tech.	22nm Tech.	32nm Tech.	22nm Tech
200	6.11×10^{-10}	1.19×10^{-9}	5.28×10^{-10}	8.56×10^{-10}	0.864	0.721
250	6.95×10^{-10}	1.43×10^{-9}	5.44×10^{-10}	9.21×10^{-10}	0.782	0.691
275	7.35×10^{-10}	1.49×10^{-9}	5.62×10^{-10}	9.91×10^{-10}	0.764	0.666
300	7.70×10^{-10}	1.65×10^{-9}	5.90×10^{-10}	1.07×10^{-9}	0.766	0.647
325	8.00×10^{-10}	1.77×10^{-9}	6.23×10^{-10}	1.14×10^{-9}	0.778	0.643
350	8.45×10^{-10}	1.81×10^{-9}	6.70×10^{-10}	1.23×10^{-9}	0.793	0.678
375	8.65×10^{-10}	1.96×10^{-9}	7.20×10^{-10}	1.35×10^{-9}	0.832	0.687
400	9.14×10^{-10}	2.04×10^{-9}	7.90×10^{-10}	1.48×10^{-9}	0.864	0.723
425	9.39×10^{-10}	2.13×10^{-9}	8.60×10^{-10}	1.61×10^{-9}	0.916	0.755
450	9.84×10^{-10}	2.22×10^{-9}	9.24×10^{-10}	1.86×10^{-9}	0.939	0.839

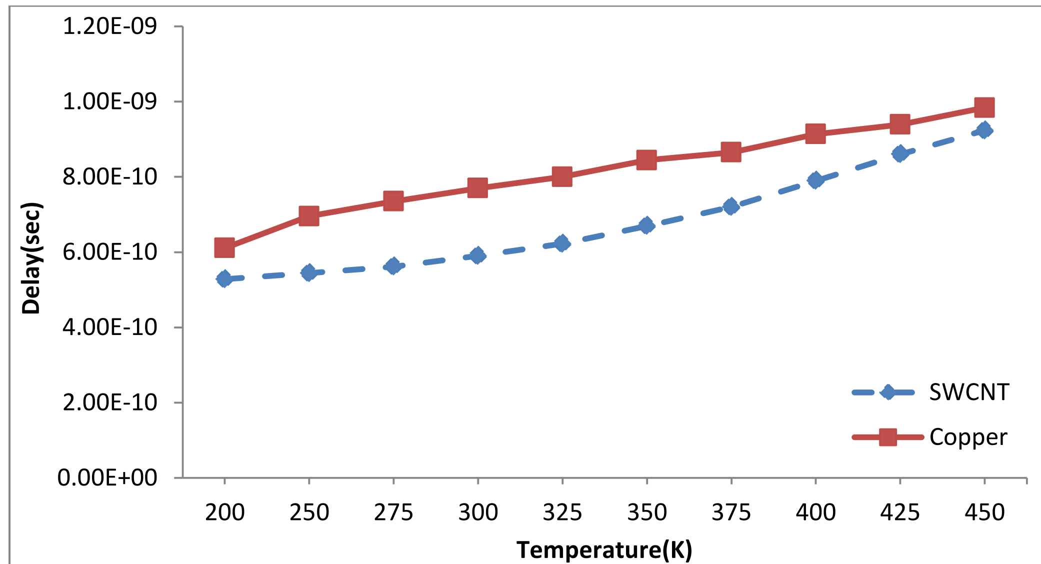

Figure 5.7 Delay Comparison of CNT bundle and copper at 32nm technology over Temperature range (250K-450K) at L=500µm

Table 5.4 shows values of average and normalized delay for copper and CNT at 32nm and 22nm technology for global length of interconnect at 500µm. Figure 5.7 and Figure 5.8 shows comparison of delay of CNT and copper at 32nm (at 0.2 GHz frequency) and 22nm (at 0.5 GHz frequency) technology for Length=500µm. CNT has less delay and thus, performs

better than copper at both technologies. CNT can be better alternative to copper to be used in VLSI circuits.

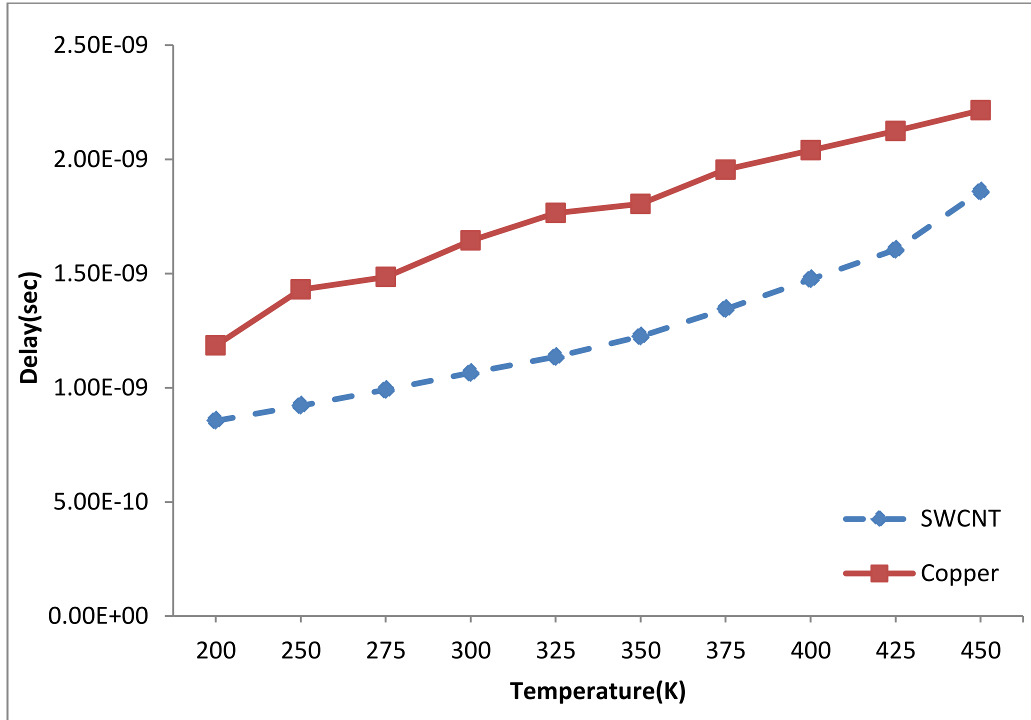

Figure 5.8 Delay Comparison of CNT bundle and copper at 22nm technology over Temperature range (250K-450K) at L=500μm

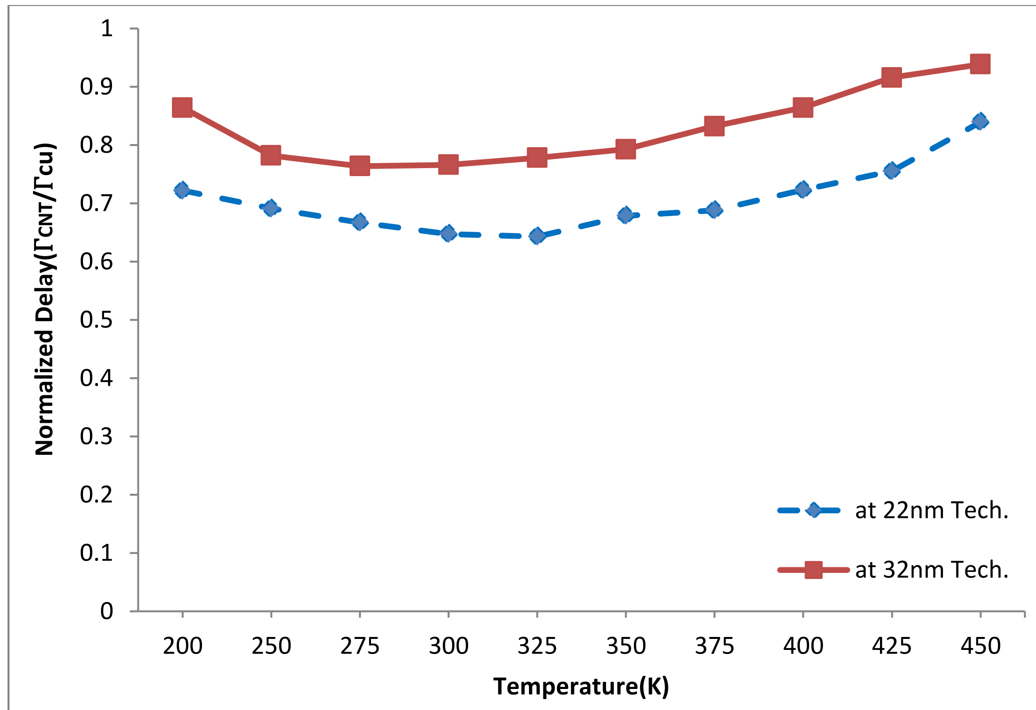

Figure 5.9 Normalized Delay over Temperature range (200K-450K) at L=500μm

Normalized delay is determined by dividing temperature dependent delay performance of CNT bundle with that of temperature dependent delay performance of copper. Since delay of copper is more than that of CNT due to shorter mean free path and more resistance, hence normalized factor will be less than unity. Figure 5.9 shows normalized delay at both technologies. Normalized delay at 1000μm is compared to normalized delay at 500μm and it is seen that CNT performs much better than copper especially at global lengths (1000μm) than at semi-global lengths (500μm).

Table 5.5 Delay analysis with Length variation of interconnects at 32nm technology over Temperature range (250K-450K)

Temperature (K)	**Average Delay of Copper (ns)**			**Average Delay of CNT (ns)**		
	L=600μm	**800μm**	**1000μm**	**600μm**	**800μm**	**1000μm**
250	7.65×10^{-10}	8.98×10^{-10}	1.02×10^{-9}	6.05×10^{-10}	6.59×10^{-10}	7.52×10^{-10}
300	8.65×10^{-10}	1.02×10^{-9}	1.19×10^{-9}	6.36×10^{-10}	7.40×10^{-10}	8.28×10^{-10}
350	9.59×10^{-10}	1.17×10^{-9}	1.35×10^{-9}	7.36×10^{-10}	8.66×10^{-10}	1.01×10^{-9}
400	1.06×10^{-9}	1.29×10^{-9}	1.49×10^{-9}	8.71×10^{-10}	1.05×10^{-9}	1.29×10^{-9}
450	1.16×10^{-9}	1.41×10^{-9}	1.65×10^{-9}	1.05×10^{-9}	1.35×10^{-9}	1.62×10^{-9}

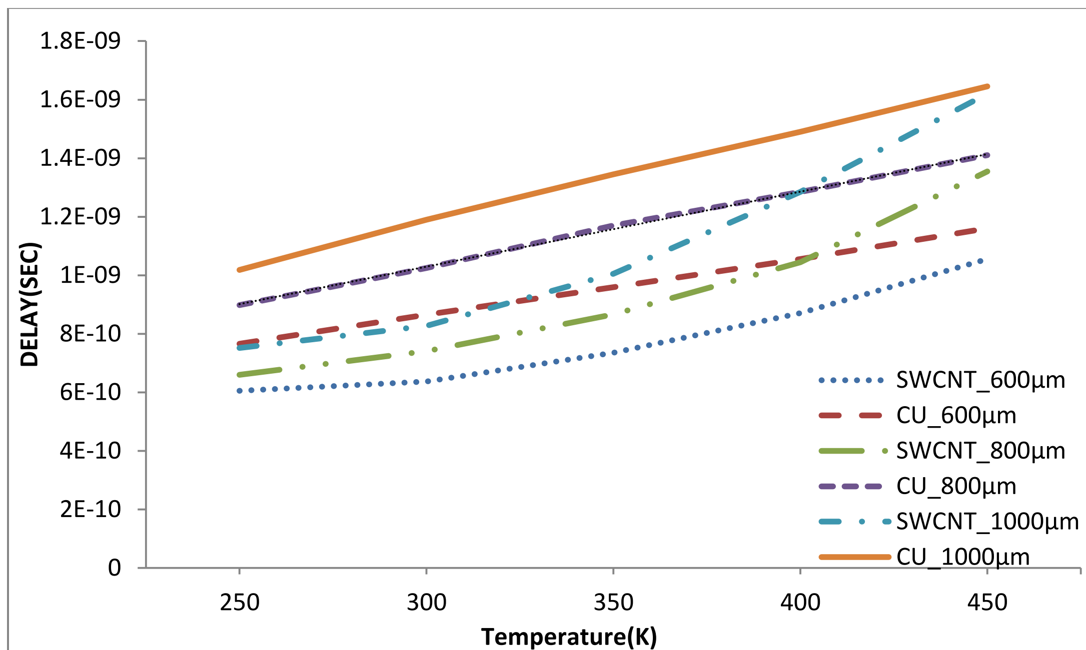

Figure 5.10 Delay Comparison of CNT and copper with length variation of interconnects at 32nm technology over Temperature range (250K-450K)

Table 5.6 Delay analysis with Length variation of interconnects at 22nm technology over Temperature range (250K-450K)

Temperature (K)	Average Delay of Copper (ns)			Average Delay of CNT (ns)		
	L=600μm	800μm	1000μm	600μm	800μm	1000μm
250	1.49×10^{-9}	1.85×10^{-9}	2.41×10^{-9}	1.01×10^{-9}	1.19×10^{-9}	1.23×10^{-9}
300	1.74×10^{-9}	2.24×10^{-9}	2.87×10^{-9}	1.16×10^{-9}	1.36×10^{-9}	1.52×10^{-9}
350	1.92×10^{-9}	2.58×10^{-9}	3.28×10^{-9}	1.33×10^{-9}	1.68×10^{-9}	1.96×10^{-9}
400	2.34×10^{-9}	2.91×10^{-9}	3.61×10^{-9}	1.70×10^{-9}	2.12×10^{-9}	2.50×10^{-9}
450	2.58×10^{-9}	3.22×10^{-9}	3.99×10^{-9}	2.19×10^{-9}	2.74×10^{-9}	3.41×10^{-9}

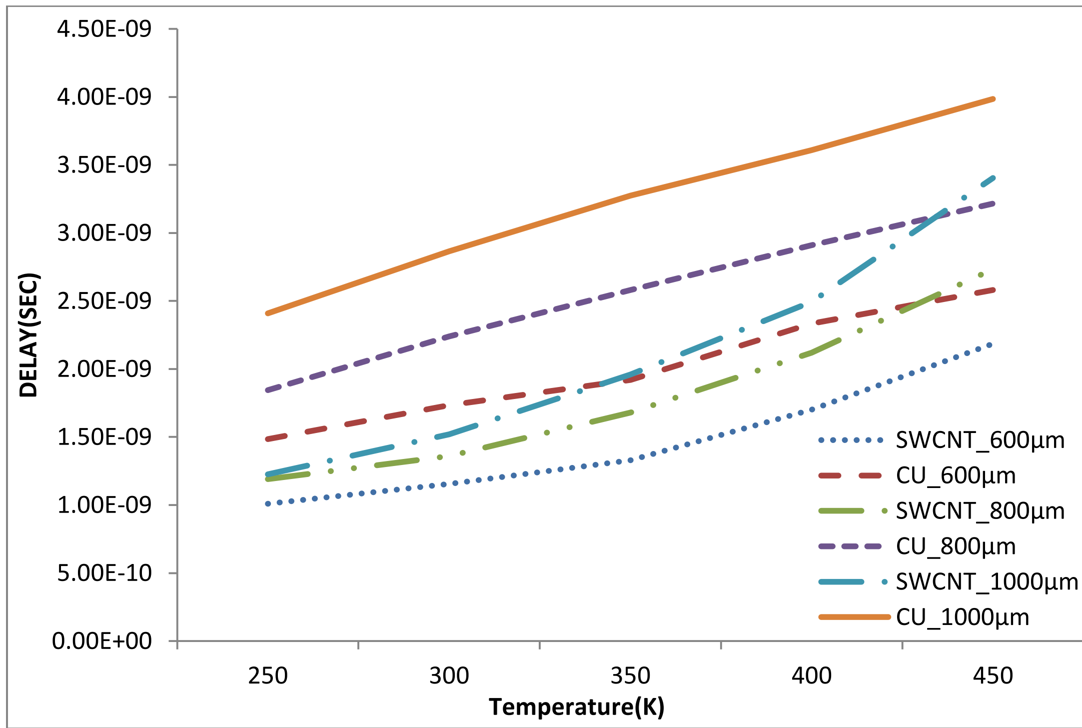

Figure 5.11 Delay Comparison of CNT and copper with length variation of interconnects at 22nm technology over Temperature range (250K-450K)

Table 5.5 and Table 5.6 shows delay analysis of copper and CNT at 32nm and 22nm technology with varied length of interconnects from 600μm to 1000μm. Figure 5.10 and Figure 5.11 takes length variation of interconnects into account at 32nm and 22nm technology respectively. Different lengths of copper and CNT are taken, their delay analysis is done and then compared. It can be clearly observed that for same lengths, say 800um, copper shows more delay than CNT at entire temperature range.

Table 5.7 Delay analysis with Diameter variation of interconnects at 32nm technology over Temperature range (250K-450K)

Temperature (K)	Average Delay of Copper(ns)	Average delay of SWCNT (ns)					
		d=1 nm	d=1.2 nm	d=1.4 nm	d=1.6 nm	d=1.8 nm	d=2 nm
250	1.02×10^{-9}	6.6×10^{-10}	6.7×10^{-10}	6.9×10^{-10}	7.1×10^{-10}	7.5×10^{-10}	7.5×10^{-10}
300	1.19×10^{-9}	7.1×10^{-10}	7.3×10^{-10}	7.6×10^{-10}	7.8×10^{-10}	8.3×10^{-10}	8.5×10^{-10}
350	1.35×10^{-9}	8.3×10^{-10}	8.4×10^{-10}	8.9×10^{-10}	9.4×10^{-10}	9.9×10^{-10}	1.0×10^{-9}
400	1.49×10^{-9}	9.6E-10	1.0×10^{-9}	1.1×10^{-9}	1.1×10^{-9}	1.2×10^{-9}	1.3×10^{-9}
450	1.65×10^{-9}	1.1×10^{-9}	1.2×10^{-9}	1.4×10^{-9}	1.5×10^{-9}	1.6×10^{-9}	1.7×10^{-9}

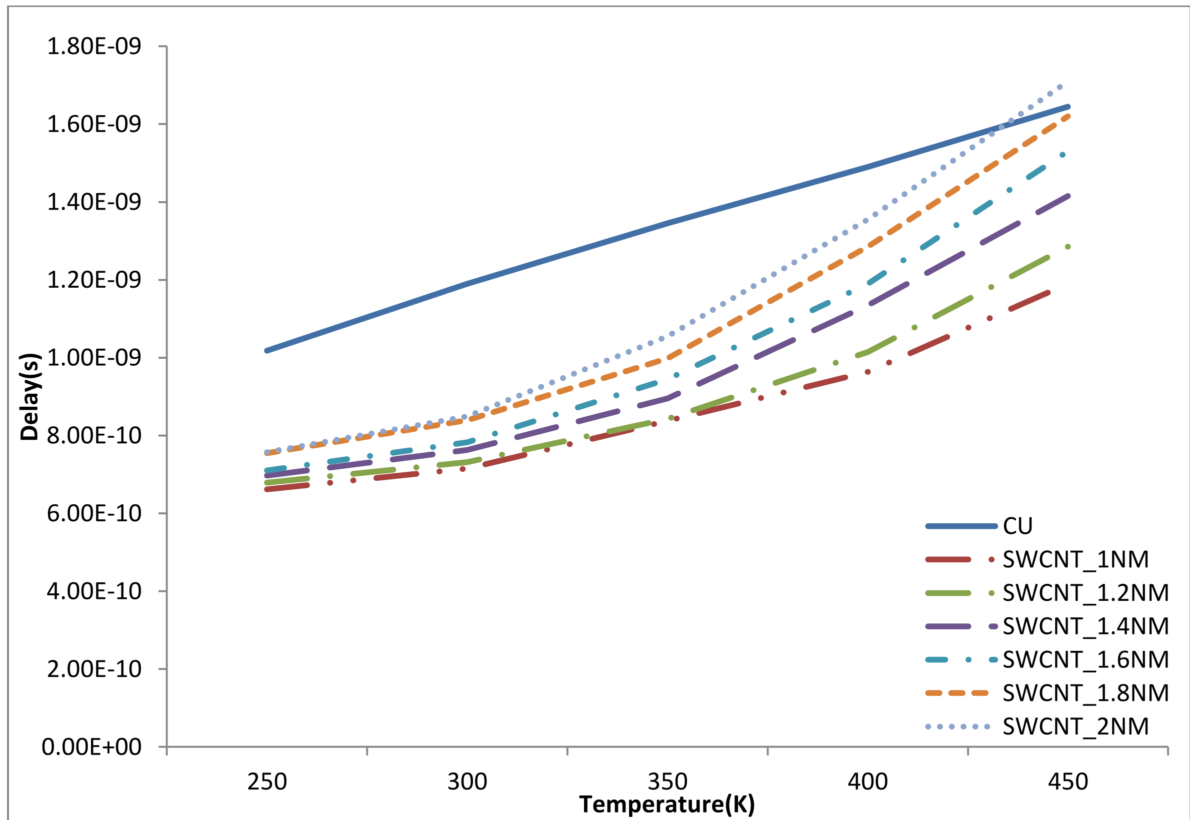

Figure 5.12 Delay Comparison of CNT and copper at 32nm technology with diameter variation at L=1000μm over Temperature range(250K-450K)

Table 5.7 and Table 5.8 shows delay analysis of copper and CNT at 32nm and 22nm technology with varied diameter of interconnects from 1nm to 2nm.

Table 5.8 Delay analysis with Diameter variation of interconnects at 22nm technology over Temperature range (250K-450K)

Temperature (K)	Average Delay of Copper(ns)	Average delay of SWCNT (ns)					
		d= 1nm	d=1.2 nm	d=1.4 nm	d=1.6 nm	d=1.8 nm	d=2 nm
250	2.41×10^{-9}	1.03×10^{-9}	1.13×10^{-9}	1.18×10^{-9}	1.24×10^{-9}	1.27×10^{-9}	1.35×10^{-9}
300	2.87×10^{-9}	1.21×10^{-9}	1.29×10^{-9}	1.36×10^{-9}	1.46×10^{-9}	1.50×10^{-9}	1.57×10^{-9}
350	3.28×10^{-9}	1.41×10^{-9}	1.49×10^{-9}	1.67×10^{-9}	1.84×10^{-9}	1.98×10^{-9}	2.01×10^{-9}
400	3.61×10^{-9}	1.72×10^{-9}	1.91×10^{-9}	2.10×10^{-9}	2.27×10^{-9}	2.48×10^{-9}	2.59×10^{-9}
450	3.99×10^{-9}	2.19×10^{-9}	2.42×10^{-9}	2.73×10^{-9}	3.10×10^{-9}	3.42×10^{-9}	3.57×10^{-9}

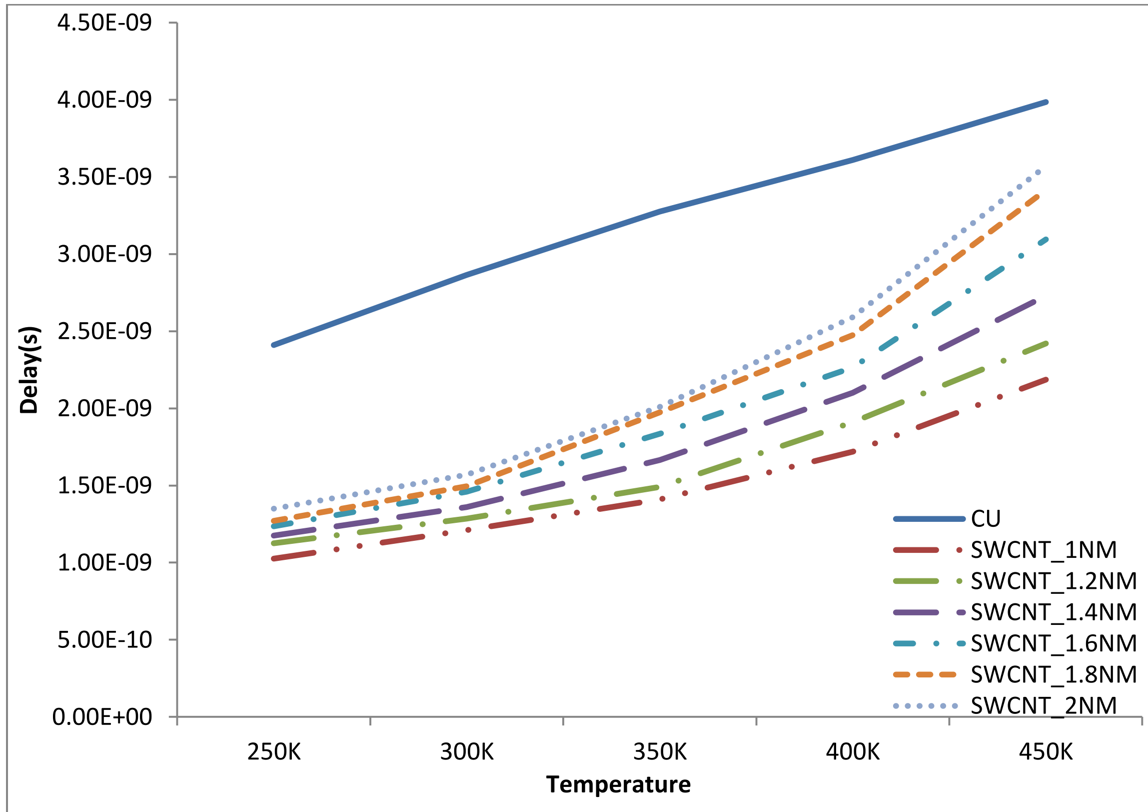

Figure 5.13 Delay Comparison of CNT and copper at 22nm technology with diameter variation at L=1000um over Temperature range(250K-450K)

Figure 5.12 and Figure 5.13 takes diameter variation of CNT interconnect into consideration at 32nm and 22nm technology respectively.

The length of interconnects is assumed to be constant at 1000um; their delay comparison is then done. With the increase in diameter of CNT from 1nm-2nm, delay of CNT increases with rise in temperature due to less number of parallel CNTs placed in bundle, thereby increasing resistance. However, still the delay of copper is always more than all diameter cases as shown in figures below. Hence, CNT proves to be a better candidate for interconnect usage. As clearly depicted in results, SWCNT has less delay than copper for all lengths and diameters and provides better solution as interconnect in circuits over wide temperature range from 250K-450K.

CHAPTER 6

CONCLUSION AND FUTURE SCOPE

6.1 CONCLUSION

In this report, CNT as a possible future VLSI interconnect is presented. Due to certain problems that exist with copper at highly scaled technologies, SWCNT bundle interconnects provides an alternative solution and have the potential to replace and gives better results than copper. Isolated CNT has a disadvantage of high resistance; so always CNT bundle is preferred. The bundle of parallel CNTs allows large reduction in resistance; thus making better interconnect than isolated counterparts. Several parameters related like length and diameter of interconnect, repeater insertion techniques and using optimum number and size of repeaters is also covered. Propagation delay increases due to increase in interconnect RLC parameters with length and diameter of CNT. So, proper selection of device parameters needs to be done depending upon application requirement. Increasing number of repeaters i.e. dividing long interconnects into small segments and increasing the size of driver transistor decreases delay but then area factor is also considered. SWCNT bundle can be used as a future interconnect material in high speed VLSI circuits and have novel applications in every day to day life from computers to medical instruments, from cars to solar cells to batteries to planes and rockets.

Thermal effects are also studied in this report. High speed VLSI circuits have to operate over wide temperature range. Thermal issues are the main source of IC damage and needs to be taken care especially at nano-scale technologies. Different kinds of scattering responsible for reducing mean free path and increasing resistance of CNT are studied. The report also includes the equations and the dependence of the parameters of copper and metallic SWCNT interconnects without and with temperature that change due to rise in temperature above room conditions. Delay analysis is done using SPICE simulation. Length and diameter variation of interconnects with temperature and its delay relation with delay is also studied. However CNT always show better result by having less delay than copper and can easily

outperform copper at 32nm and below for global lengths in VLSI circuits. Analytical results presents that the value of resistance of copper is always more than CNT at entire temperature range from 250K to 450K. Hence, simulation results demonstrate that the propagation timing delay offered by copper is more than SWCNT bundle at both 32nm and 22nm technology. Also the results of CNT as compared to copper for 22nm technology are better than at 32nm technology. Last but not the least, SWCNT bundle interconnect can easily replace copper at advanced nano-scaled technology nodes.

6.2 FUTURE SCOPE

Due to problems like surface roughness, grain boundary scattering and electromigration in copper, it cannot be used as interconnect at highly scaled future technologies. So, lots of work is carried out in finding a suitable solution that can easily replace copper. SWCNT provides best solution provided all CNTs in bundle are metallic. SWCNT has been studied in this report and it is analysed that tube diameter, length and temperature plays an important role in determining delay. It is concluded that SWCNT performs better than copper and can be used as interconnect at semi-global and global lengths in high speed VLSI applications at 32nm and 22nm technology nodes and further study can also be done for technology below 22nm.

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1. Gurleen Dhillon, Karamjit Singh, "Temperature Dependent Performance Analysis of Single-Wall Carbon Nanotubes as VLSI Interconnect", *Journal of Electronic Materials Springer(JEMS)*, Springer-New York, communicated in May 2014, under review.
2. Gurleen Dhillon, Karamjit Singh, "Evaluation and comparison of Single-Wall Carbon nanotubes and Copper as VLSI interconnects" , *International Journal of Innovative Research in Electrical, Electronics, Instrumentation and Control Engineering (IJIREEICE)*, vol. 2, Issue5, pp.1459-1464, May 2014.
3. Gurleen Dhillon, Karamjit Singh, "Diameter and Length Dependent Performance Analysis of Single-Wall Carbon Nano-tubes as VLSI Interconnect", *International Conference on Electronics, Communication and Information Technology (ICECIT*), October 2013.

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