PERFORMANCE ANALYSIS OF OPTICAL BASED VLSI INTERCONNECTS

Dissertation submitted in partial fulfillment of the requirements
for the award of the degree of

Master of Engineering

In

Electronics and Communication Engineering

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July, 2014

CERTIFICATE

I hereby declare that the work which is being presented in the dissertation entitled, **"Performance Analysis of Optical based VLSI Interconnects"** in partial fulfillment of the requirement for the award of degree of Master of Technology (Electronics and Communication Engineering) at the department of Electronics and Communication Engineering, Thapar University, Patiala, is an authentic record of my own work carried out under the supervision of Dr. Mayank Kumar Rai, Assistant Professor, ECED.

The matter presented in this dissertation has not been submitted in any other University/Institute for the award of any other degree.

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It is certified that the above statement made by the student is correct to the best of my knowledge and belief.

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ACKNOWLEDGEMENTS

I take this opportunity to express my profound sense of gratitude and respect to all those who helped me through the duration of this dissertation. I acknowledge with gratitude and humility my indebtedness to **Dr. Mayank Kumar Rai, Assistant Professor,** Department of Electronics and Communication Engineering, Thapar University, Patiala, under whose guidance I had the privilege to complete this dissertation. I wish to express my deep gratitude towards him for providing individual guidance and support throughout the dissertation work.

I convey my sincere thanks to **Head of the Department, Dr. Sanjay Sharma** as well as **PG Coordinator, Dr. Kulbir Singh, Associate Professor, ECED**, entire faculty and staff of Electronics and Communication Engineering Department for their encouragement and cooperation.

My greatest thanks are to all who wished me success especially my family. Above all I render my gratitude to the Almighty who bestowed ability and strength in me to complete this work.

Savvy Jain

ABSTRACT

For more than 30 years, the performance of silicon integrated circuits has improved at an astonishing rate. The number of functions per chip has grown exponentially, dramatically bringing down the cost per function. The conventional copper interconnects are not able to fulfil different design requirements. Copper based interconnects are facing many challenges. Because of dispersion, reflections and ringing, attenuation and its variation with frequency, the high-speed signals are distorted. The performance of parallel links in conventional devices is also limited by the cross talk due to coupling from neighbouring signals. Optical Interconnects present a promising option for replacing the existing copper Interconnects. For global and semi-global wire, optical interconnects provide a better option as compared to both carbon nanotubes and copper in terms of latency, power dissipation and bandwidth density. The report includes the comparison of optical interconnects with the copper in terms of energy efficiency and latency at various sizes and technology nodes.

In this dissertation, the performance of high speed optical and electrical interconnects in terms of power vs. bandwidth have been analyzed. Results reveal that beyond a critical length, power optimized optical interconnects dissipates less power compared to high speed electrical signaling schemes. Beyond the 32nm technology node with its commensurate bandwidth, optical interconnect becomes favourable for the distances less than 10cm for inter-chip communications. We also examine two competing transmitters, the vertical cavity surface emitting laser (VCSEL) and the quantum well modulator (QWM), for optical links. The vertical cavity surface emitting laser (VCSEL) is used in the modelling of the transmitter circuit for the carrying out the SPICE simulations for calculating the delay and power dissipation in transmitter circuit.

The transimpedance types of receivers are considered here due to their high bandwidth, low noise and ease of biasing. Various transimpedance amplifiers are implemented and then, the optimum differential cascode transimpedance amplifier is used. Similarly, voltage amplifier and decision circuit are chosen. The receiver circuit is seen to dissipate more power as compared to the transmitter circuit. The optical waveguide is relatively very small so, the power dissipation in the optical waveguide is neglected. The delay in the waveguide is constant for a constant length and varies with the change in length only and has no effect of the technology node used.

In this dissertation, delay and power dissipation results are simulated for optical and copper interconnects at various technology nodes. Simulation is done using SPICE simulation tool at global interconnect level. Optical interconnects give better delay performance as compared to conventional copper interconnects at each technology node. Power dissipation of optical and copper interconnects increases with small technology nodes because of higher clock frequency and leakage current. The power dissipation in optical interconnects is more than copper interconnect at lower frequency levels but as we keep on increasing the frequency levels, the power dissipation in the optical interconnects keeps on decreasing as compared to copper interconnects, resulting more efficient operation in terms of power. Based on the comparisons made, various areas of improvement of optical fibers are concluded.

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ABBREVIATIONS

MOS	Metal Oxide Semiconductor
MOSFET	Metal Oxide Semiconductor Field Effect Transistor
ICs	Integrated circuits
OIs	Optical interconnects
CIs	Copper interconnects
CMOS	Complementary metal oxide semiconductor
PMOS	P channel metal oxide semiconductor
NMOS	N channel metal oxide semiconductor
PD	Photo detector
MSM	Metal semiconductor metal
TIA	Transimpedance amplifier
MQW	Modulator quantum well
VCSEL	Vertical cavity surface emitting laser
SOI	Silicon on insulator
CR	Contrast ratio
IL	Insertion loss
BR	Bit rate
WDM	Wave division multiplexing
VLSI	Very large scale integration
MZM	Mach–Zehnder modulator
CNT	Carbon nanotube
EMI	Electromagnetic interference
EMC	Electromagnetic compatibility

CHAPTER 1

INTRODUCTION

1.1 Introduction

A VLSI interconnect is a thin film of conducting material that provides electrical connection between two or more nodes of the circuit/system formed in the silicon chip. In the short distance interconnect applications (<100m), the interconnect hierarchy is typically divided into the following categories in the order of progressively smaller length spans: cabinet level (1-100m), backplane level between boards (10cm-1m), and chip to chip on a board (<10cm) and on-chip (<2cm) communication [1].The performance of silicon integrated circuits has improved at an amazing rate over the last 30 years. The number of functions per chip has grown exponentially, thus bringing down the cost per function. But for the first time the persistent scaling theory is threatened by fundamental limits including excessive power dissipation, signal latency and insufficient communication bandwidth. These obstacles are due to the physical limitation of Cu-based electrical wires like dispersion, reflections and ringing, attenuation and its variation with frequency which can distort high speed signals. There is cross talk due to coupling from neighbouring traces in parallel links. The variation in the delay between different signal traces causes the signal skew. Copper interconnects use strip lines on a printed wiring board (PWB). The problems mentioned above have created a situation in which the performance of the system is degraded by the interconnect capacity and this situation is called interconnection bottleneck. The two most important alternates are optical and carbon nanotube (CNT) based interconnects. There are three types of interconnects: local, intermediate and global.

- Local interconnects consist of very thin lines, connecting gates and transistors inside a functional block. They generally span only a few gates and occupy first and sometimes second metal layers.
- Intermediate interconnects are wider and longer than local interconnects in order to provide lower resistance; intermediate wiring provides clock and signal distribution within a functional block with typical lengths upto 3 to 4 nm.
- Global interconnects provide clock and signal distribution between the functional blocks and deliver power to all functions. Global interconnect occupies the top one or two layers, and they are longer than 4 mm- as long as half the chip

perimeter. It is critical that low- resistivity global interconnects be used as the bias voltage decreases and the total current consumption of the chip increases [2].

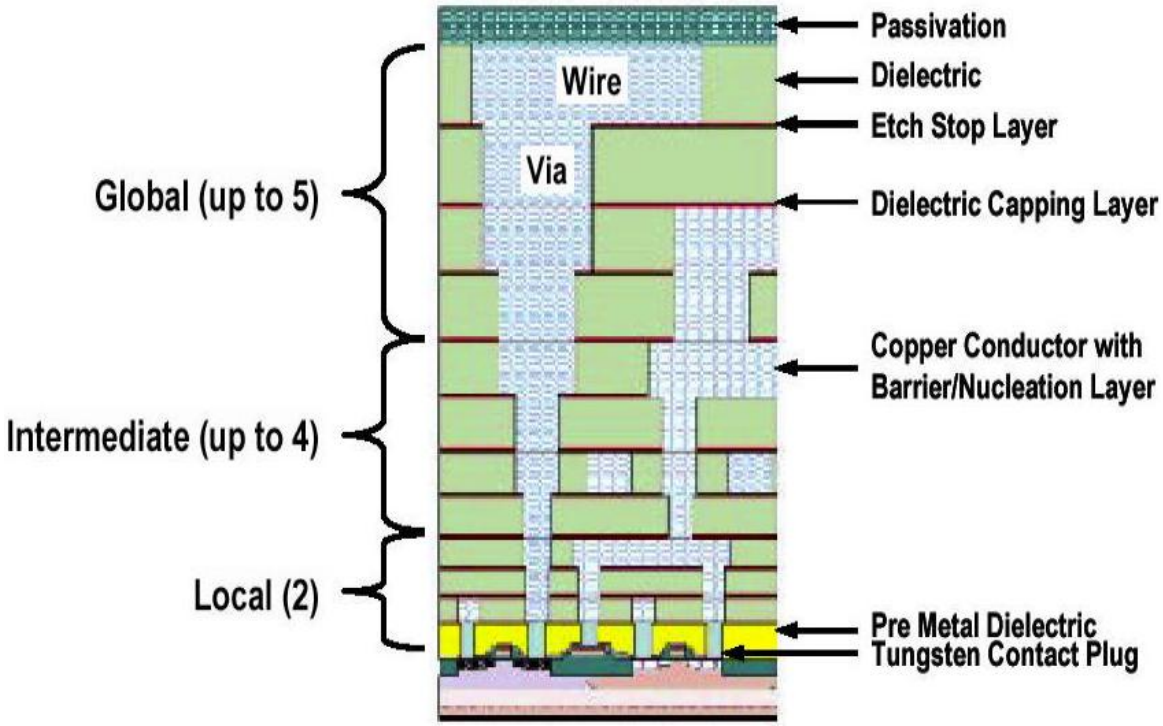

Figure 1.1 Schematic showing the hierarchy of metal levels for distribution of interconnects in modern ICs [3].

1.2. Statement of problems

Following objectives have been carried out in this dissertation report:

- To study the design and development of equivalent model for optical based VLSI Interconnects.
- Study the performance of optical interconnects in terms of delay, dynamic power dissipation and latency.
- Compare the performance of optical interconnects with copper interconnects.
- Comparison will be carried out in 22 nm technology nodes with PTM model.

1.3. Organization of report

The report is divided into 6 chapters keeping the performance comparison between optical and copper interconnects in terms of power and delay at various technology nodes. All aspects of copper interconnects and optical interconnects are discussed in the following chapters. Literature survey of about the topic is also given. Simulation results are discussed to compare both interconnects at various technology

nodes using different parameters. The conclusion is made from the simulation results for delay and power dissipation.

Chapter 2 gives literature survey related to the topics. In order to start the thesis, the first step is to study the relevant work that have already been published by other researchers. Research papers related to the work are studied and with the help of literature review, it becomes easier to carry out the work. A review of various aspects of copper interconnects is presented. It is shown in the papers, that how the conventional copper interconnects is not able to fulfil the requirements of modern IC designs at very high speeds. It is shown that optical interconnect is a potential candidate to tackle the challenges of modern ICs. Various requirements for the implementation of optical interconnects are also shown.

Chapter 3 describes the conventional copper interconnects. Various aspects of copper interconnects are shown. It is shown how they are not able to fulfil the requirements of modern ICs in term of various criteria. The negative aspects are wire resistance, causing delay and dispersion, and high capacitance, causing large power consumption at large voltage swings. They face challenges like reflections and ringing, attenuation and its variation with frequency. The attenuation of high frequency signals results in a need to use high-power line-drivers and thus causing thermal management issues. Electromagnetic interference (EMI) causes noise and design constraints due to the need to fulfil electromagnetic compatibility (EMC) specifications. Moreover, the performance of parallel links is limited by the cross talk due to coupling from neighbouring traces and the signal skew caused by variations in the delay between different signal traces. Then its basic CMOS circuit is shown. Model of global interconnect is shown. Various equations are given for calculating its R, L and C parameters. It is shown how repeaters are inserted in long interconnects to reduce the delay. Delay and power analysis is done.

Chapter 4 describes the optical interconnects. It is shown how they can tackle the various challenges imposed by conventional copper interconnects. Optical interconnects are described as potential alternative to the conventional copper interconnects at global interconnect level. Basic optical data path at 1mm and 1 cm length is shown. Optical interconnect based systems require a means of transforming the electrical signal to the optical domain (modulator), a super buffer to derive the modulator, a waveguide to route the optical signal, and a photo detector to convert the optical signal back into an electrical signal and then transimpedance amplifier to convert current into voltage. Transmitter, waveguide and optical receivers are described in detail. The optimization of the modulator

to extend its application to higher bandwidth and shorter distance interconnects is done. We examine two competing transmitter technologies for optical links, the vertical cavity surface emitting laser (VCSEL) and the quantum well modulator (QWM). VCSELs simplify packaging by allowing the optical power to be generated on-chip through hybrid bonding and also can provide a larger contrast ratio than modulators. The disadvantage stems from a poor reliability, especially in the high temperature environment of a modern integrated circuit. Modulator based links, especially using the quantum well modulators (QWM), on the other hand, can be more reliable, can be integrated monolithically in silicon, and do not dissipate large power, at least in the transmitter. However, their low contrast ratio, in particular, at the scaled CMOS supply voltages renders higher power dissipation at the receiver-end. The Delay and power dissipation analysis of each part of the optical interconnect system is done.

Chapter 5 gives results and discussion. Interconnect load can be represented by R, L and C parameters. These parameters are determined from the physical geometries of interconnects which are given for various technology nodes. R, L and C parameters of interconnect are calculated at various technology nodes for different numbers of repeaters using physical parameters of interconnect. Then delay simulation is done for optical and copper interconnects at different frequencies for various technology nodes. It is shown optical interconnects give better performance than copper interconnects in terms of delay. Delay of optical interconnects decreases with future technology nodes, whereas delay of copper interconnects increases. Delay of both interconnects decreases with frequency. Power dissipation simulation is also done for optical and copper interconnects at different technology nodes at global interconnect level. In the contrast to delay, power dissipation of optical interconnects increases with future technology nodes. Power dissipation of conventional electrical interconnects (copper interconnects) also increases with future technology nodes. As the technology is scaled down, power dissipation increases for both type of interconnects because of higher clock frequency and leakage current.

Chapter 6 gives conclusion and future work. The performance characteristics of future CMOS compatible optoelectronics devices are predicted. Based on this prediction, electrical and optical on-chip interconnects are compared for various design criteria at different technology nodes. The performance comparison between optical and copper interconnects is done in terms of delay and power dissipation. For performance comparison delay and power dissipation are simulated for both type of interconnects at

various technology nodes. SPICE simulation tool is used for delay and power dissipation simulation. Delay and Power dissipation are simulated at 90nm, 65nm, 32nm and 22nm technology nodes. For minimization of delay in copper interconnects repeaters are inserted. Delay and power dissipation are simulated for each individual part of the transmitter and receiver in an optical interconnect system. It is shown optical interconnects give better results than copper interconnects in terms of delay. Scope of future work related to this topic is also shown.

CHAPTER 2

LITERATURE SURVEY

2.1. Introduction

The researchers proposed that Optical interconnects are emerging as the promising technology for high bit rate data transfer. Optical interconnects shows advantage over both CNT and Cu for longer lengths around 10 mm because a large fraction of the delay occurs in end devices. For 1-mm long wires, optics becomes advantageous over CNT only at smaller technology nodes. This is because of scaling, CNT and Cu latency increases, whereas optical delay reduces due to an improvement in transistor performance. Length of optical interconnects is not a major parameter of performance of optical interconnects in terms of delay and power dissipation.

2.2. Performance analysis of Optical and Copper Interconnect

K. H. Koo et al. [4] proposed that the on-chip interconnect bottleneck with conventional copper and delay optimized repeater scheme provides an ample reason to investigate new interconnect circuit architectures. The comparison of delay and energy expenditure was done for different interconnect circuit schemes and different future technologies such as Cu, carbon nanotube and optical. The capacitive driven low-swing interconnect (CDLSI) has the capability to affect a significant energy saving and latency reduction. An accurate analytical and optimized model was developed for CDLSI wire scheme. It was found that CDLSI circuit scheme can outperform the conventional interconnects in latency and energy per bit for less bandwidth requirement, while these advantages mortify for higher bandwidth requirements.

Osman Kibar et al. [5] calculated the design optimization of digital free-space optoelectronic interconnections with particular purpose to minimize the power dissipation of the overall link and maximize the interconnect density. An approach to minimize the total power dissipation of an interconnect link at a specified bit rate is discussed. The impact on the link performance of two competing transmitter technologies, namely the multiple quantum-well (MQW) modulators and vertical cavity surface emitting lasers (VCSEL's) and their associated driver-receiver circuits together with complementary metal oxide semiconductor (CMOS) and bipolar transmitter driver circuits, and p-n junction photo detectors with multistage transimpedance receiver circuits are examined.

Operating bit rates and on-chip power dissipation are the main performance parameters discussed in the paper. The transmitter driver circuit is an important component in an optical link design, and it dissipates nearly the same amount of power as that of the transmitter circuit itself. VCSEL is more efficient at low bit rate while the power dissipation at high bit rate is comparable in VCSEL and MQW modulator. The bipolar technology supports a much higher operating bandwidth than CMOS technology in transmitter driver circuit implementation, but they dissipate nearly twice the electrical power.

Anas A. Hamoui and and Nicholas C. Rumin [6] proposed an analytical model for determining the supply current, delay and power of a submicron CMOS inverter. They proposed a modified version of the nth power law MOSFET model to relate the terminal voltages to the drain current in submicron transistors. This analysis included a three-step approach to calculate the time and output voltage when a short-circuit transistor changes its mode of operation. They predicted the delay, peak supply current, and power dissipation within a few percent of HSPICE or ELDO simulations depending on accurate physically based MOSFET models, while presenting about two orders of magnitude gain in CPU time based on a MATLAB implementation.

Christoforos Kachris and Ioannis Tomkos [7] proposed that the exponential increase of Internet traffic because of cloud computing and other rising web applications has created the requirement for more powerful data centres. These warehouse scale data centres comprises of thousands of racks interconnected with commodity switches and consume huge amount of energy. A number of optical interconnects for future data centre networks have lately appeared that provide low latency, high throughput and reduced power consumption. The paper discusses the need to shift the data centre networks to the optical domain to reduce the power consumption and meet the bandwidth requirements. This paper also represents a few indicative optical interconnects for high performance data centres that have appeared recently in the research literature. The work represents a comparison and qualitative categorization of these schemes based on their core features such as performance, connectivity and scalability.

Shogo Ura and Kenji Kintaka [8] proposed the basic concept and key structures of free-space wave add/drop multiplexers/demultiplexers and discussed for wide-band WDM optical interconnect system. The number of transistors is increased to improve LSI performance, but causes greater power dissipation. Even though three-dimensional

packaging is an efficient way to integrate CPU and memory chips, it becomes difficult to apply the same to multiple CPU chips due to their higher power dissipation. LSI chips and an optoelectronic interposer including VCSEL and PD 2D arrays are surface-mounted on a package substrate or circuit board integrating optical thin waveguides.

Hoyeol Cho et al. [9] proposed in the future, it will become more challenging to increase on-chip computational capability using board-level copper interconnects due to severe increase in high- frequency, noise due to crosstalk, skin-effect and dielectric loss, impedance mismatch, and package reflections. The complex signal processing at the interconnect endpoints is required to overcome these effects, which leads to larger power and area requirement. Optical interconnects provides a strong substitute, substantially at a lower power. A more practical power comparison with respect to the applicable parameters such as bandwidth, interconnect length and bit error rate (BER) is done by taking the necessary complexity in both types of interconnect systems. In optical interconnects detector and modulator capacitance, coupling efficiency, responsivity and modulator type are the parameters while, in the case of electrical system, the critical parameters consist of receiver sensitivity/offset and impedance mismatch.

Arun Palaniappan and Samuel Palermo [10] proposed that increasing input/output bandwidth demands can be dealt with the help of high-bandwidth interchip optical interconnect architectures. Several optical interconnect architectures are compared on the basis of power efficiency in 90-nm and 45-nm CMOS technologies. There are several architectures under consideration namely- a near term architecture consisting of discrete vertical cavity surface-emitting lasers (VCSELs) with p-i-n photodetectors (PDs) and three long term integrated photonic architectures that use waveguide metal–semiconductor–metal PDs and either electro absorption modulator (EAM), Mach–Zehnder modulator (MZM) ,or a ring resonator modulator (RRM) sources. A best possible current density methodology with normalized transistor parameters extracted from circuit simulations is applied to mutually optimize driver and receiver circuitry to minimize the total link power dissipation. The results of analysis show that the VCSEL-based link is restricted by VCSEL bandwidth and maximum power levels, instead of circuit bandwidth, and achieves a maximum bandwidth of 24 Gb/s in both the 90-nm and 45-nm nodes. The data rates can be scaled beyond 30 Gb/s at power efficiency levels near 0.5 mW/Gb/s in the 45-nm node using both RRM and the EAM integrated photonic technologies and are mainly limited by coupling and device insertion losses. The MZM

provides robust operation because of its wide optical bandwidth, but to become usable at high-density applications, significant improvements in power efficiency is needed.

Yun-Parn Lee and Yulei Zhang [11] proposed that even though large research has been done in many different approaches for devising optoelectronic interconnects, further detailed analysis of the performance parameters such as power, delay, and area of different optical technologies is yet to be done. New approaches for the production of VLSI interconnects are provided by optoelectronics, but previous works have made excessively simplified assumptions for optoelectronic interconnects. The three-dimensional free-space optoelectronic interconnect network has the finest speed area product performance compared with optical microelectromechanical systems (MEMS) interconnects and fiber-optical interconnects. The optoelectronic interconnect gives higher data rates and less power per bit compared with the electronic interconnects, but a larger area and volume will be needed due to the bipolar encoding scheme on the source plane and the detector plane.

Guoqing Chen et al. [12] proposed that with scaling of CMOS technology, it is becoming ever more difficult for conventional copper interconnect to provide different design requirements. The possible replacement for electrical interconnect is considered to be on-chip optical interconnect. Predictions of the performance of CMOS compatible optical devices are made based on current state-of art optical technologies. The electrical and optical interconnects are compared for delay uncertainty, power, latency, and bandwidth density based on above predictions.

Pawan Kapur and Krishna C. Saraswat [13] made comparison between electrical wires driven by repeaters and optical interconnects from both delay and power point of view. They involved properly modelling the power and delay of each component in an optical signaling system as well as repeated wires. The shorter wires favor an electrical operation on lower power grounds while for long wires, it is favourable to switch to optical interconnects for global signaling, on both power and delay account. They examined the change in the delay-power curves for both electrical and optical links with technology scaling.

Pawan Kapur and Krishna C. Saraswat [14] calculated the power dissipation in a global clock based on optical interconnects and compared it with metal wires. The receiver is the key power dissipation source for optical interconnects. They identified the important

parameters affecting its power and quantified the power trends with these parameters. With logically high optical power accessible, optical interconnect can reduce power despite of higher bandwidth requirements or higher clock frequency. They also found that optical interconnect based global clock dissipates less power compared to metal based interconnects as conventional metal interconnects based clock distribution will suffer from both timing uncertainty and power dissipation problems in the future.

Mahesh Kumar and Karamjit Singh Sandha [15] gave the performance comparison between copper and optical interconnects in terms of delay at global level. The conventional copper interconnects are not able to realize different design requirements, as the device dimensions shrink on the chip with the scaling down of technology. The optical interconnects can be presented as a substitute for copper interconnects. In this paper, the simulation results for delay of copper and optical interconnects are shown using SPICE simulation at different technology nodes at global interconnect length. The results of this paper show that, for global interconnect length, optical interconnects give better result as compared to conventional copper interconnect.

Labros Bisdounis et al. [16] introduced a novel precise analytical model for the estimation of the short-circuit power dissipation and the delay in a CMOS inverter. The correct expressions of the output response to an input ramp are derived by the thorough analysis of the inverter operation. New improved analytical formulae for the calculation of the short-circuit power and dissipation propagation delay are formed on the basis of their analysis. The effects of the short-circuit current while switching, and the gate-to-drain coupling capacitance are considered while formulating the Analytical expressions for all inverter operation regions and input waveform slopes. The real output voltage waveform to a ramp waveform for the model are plotted using the effective output transition time of the inverter to be applicable in an inverter chain.

Shaloo Rakheja and Vachan Kumar [17] studied two alternative on-chip interconnect technology options: the plasmonic interconnects and optical interconnects. According to the 2016 technology node, the plasmonic interconnects can be 3 times faster than minimum sized CMOS interconnects. But, they can only be used as short local interconnects as their propagation length is limited to few microns. Plasmonic switches are needed for the implementation of plasmonic interconnects at the GSI (GigaScale Integration) level as the energy and circuit overhead related with signal conversion will be unaffordable without plasmonic switches. Whereas, optical interconnects are restricted

to be used only at the global level because of the elementary limitations on their size. The bandwidth density of optical interconnects is limited inspite of quite less interconnect delay because of the fundamental limitations on the minimum pitch.

Eilert Berglind et al. [18] compared between dissipated power and signal-to-noise ratios (SNR's) in electrical interconnect and optical interconnect. The electrical interconnection requires much less signal powers in the absence of amplification to logic voltage levels. Under the constraint of equal output voltage, the total power dissipation and SNR's result are comparable if the amplification in the receiver is included.

2.3. Increasing Bandwidth Density of Optical Interconnect

B. G. Lee et al. [19] considered future challenges to bandwidth scaling within computing systems, including the current unsustainable raise in the number of fibers per system. This paper discusses the potentials technologies for the HPC like Flip-Chip Packaged Parallel Optical Transceivers, Multicore Graded-Index Fiber Transceivers, Optical Links Employing Planar Polymer Waveguides, and Dense WDM Exploiting Silicon Photonic Transceivers.

Satoshi Ide [20] proposed optical interconnect technologies to realize a next-generation server systems. New blade server architecture with bus-extensions by means of optical connections and its requirements for interconnects - high-density and high-speed over 25 Gb/s is proposed. The blade server is an aggregate of CPU blades connected via a mid-plane, and the performance depends on the data transmission capability of the mid-plane. In this structure, the Driver/TIA ICs and 850nm VCSEL/PD arrays are flip-chip mounted on a FPC.

Yuanyuan Yang and Jianchao Wang [21] proposed that optical communication wavelength division multiplexing (WDM) technique, can meet growing demands of bandwidth from the upcoming bandwidth demanding computing/communication applications. Optical interconnects will certainly play an important role in interconnects processors in parallel and distributed computing systems. The cost-effective designs of WDM optical interconnect for current and future generation parallel and distributed computing and communication systems are considered.WDM optical interconnects are categorized into two different connection models based on their target applications: the fiber -link-based model and the wavelength-based model. Most of existing WDM optical interconnects belong to the second category. A minimum cost design for WDM optical

interconnects under wavelength-based model using sparse crossbar switches instead of full crossbar switches in addition with wavelength converters is presented. The applications which use the fiber-link-based model, network cost can be significantly reduced using the model. The idea used in the design for the fiber-link-based model to WDM optical interconnects is generalized under the wavelength based model, and another new design that can trade off switch cost with wavelength converter cost in this type of WDM optical interconnect is obtained.

Naida Fehratovic and Slavisa Aleksic [22] compared with electronic backplane and optical point-to point options with optically switched interconnects using the three realizations that were analyzed regarding power consumption and scalability. The results showed that higher power efficiency is provided by optically switched interconnects as, optically switched interconnects consume less power than the two other options considered. AWG-based optically switched interconnects show the most terrible scalability when in-band crosstalk is taken into account. On the contrary, very large switches are possible if the in-band crosstalk is eliminated. So, MEMS-based interconnects are the most power efficient and scalable resolution but, they suffer from large switching times.

2.4. Optimization of Optical Interconnect Circuit

N. *C.* LI et al. [23] described that the super buffer is a set of tapered inverters, and the size of each inverter is larger than the preceding one by a constant factor, and each inverter is modelled by a capacitor and a conductor The value of the constant factor is chosen usually between three and four to minimize the overall propagation delay of the super buffer and is determined with the help of parameters of a minimum size transistor for a given CMOS technology. The first inverter is of minimum size, and the last inverter drives the modulator. In high-density CMOS circuits, severe mismatch between off-chip loads and on-chip logic devices occurs. In Jaeger's model, each stage of the buffer is represented by one conductor and one capacitor, but in this paper, one conductor and two capacitors are used.

Daniel A. Van Blerkom et al. [24] proposed that optical transimpedance receivers which are implemented in CMOS VLSI technologies are modelled and optimized for free space optoelectronic interconnections. Sensitivity, bandwidth, power dissipation, and circuit area are realised for receivers using three different submicron CMOS processes. A

comparison with the circuit noise limited optical power presents that, for the digital computing applications, the receiver sensitivity is restricted by the gain-bandwidth product of the receiver amplifiers and the essential noise margin of logic circuits.

H.B. Bakoglu and James D. Meindl [25] proposed that the propagation delay of interconnection lines is an important factor in determining the performance of VLSI circuits because the RC time delay of these lines increase quickly as chip size is increased and cross-sectional interconnection dimensions are scaled. In this paper, a model for interconnect time delay is obtained which includes the effects of changing transistor, interconnect, and chip dimensions. The delays of aluminium, WSi2, and polysilicon lines are compared, and accordingly, propagation delays in future VLSI circuits are proposed. Properly scaled multilevel conductors, cascaded drivers, repeaters, and cascaded driver/repeater combinations are investigated as possible methods for reducing propagation delay. The model gives best possible cross-sectional interconnection dimensions and driver/repeater configurations which can lower the propagation delays by a factor of more than an order of magnitude in MOSFET.

Min Tang et al. [26] proposed a new method of global interconnect optimization for the high performance integrated circuits. They considered the effects of interconnect width and spacing on a variety of performance parameters like delay, power dissipation and chip area. There is a trade-off between delay and power dissipation of global interconnects with repeater insertion. The minimum delay-power product is used to calculate the optimum line width which is defined as a figure of merit (FOM). To optimize the global interconnects, the delay-power-area product is introduced as another FOM, if the silicon area and wire ability of chip are considered. Optimizations of global interconnect size in different scenarios are applied for different International Technology Roadmap for Semiconductor technology nodes.

Ashok V. Krishnamoorthy et al. [27] proposed that optical links are successful over electrical links when the aggregated bandwidth–distance product exceeds ~100Gb/s-m since optical link's energy per bit per unit distance is lower. Optical links will be considered for a distance of 1m and below if link power falls below 1 pJ/bit/m. Optical links can be provided directly to a switching/routing chip to improve the switched energy/bit significantly. A nearly experimental switched CMOS vertical cavity surface emitting laser (VCSEL) system operating at Gigabit Ethernet line rates can achieve a switched interconnect energy of less than 19 pJ/bit for a fully non-blocking network with

16 ports and a combined capacity of 20 Gb/s/port. When operating at a line rate of 1.25Gb/s, the CMOS-VCSEL switch achieves an optical bandwidth density of 37 Gb/s/mm^2 and is capable of scaling to much higher peak bandwidth densities with 5–10pJ/switched bit. A silicon photonic system design which will lower link energies to 300 fJ/bit is reviewed, while providing multiterabits/ s/mm^2 band width densities. This system will eventually provide switched optical interconnect at less than a picojoule per switched bit and computer/router system energies of tens of picojoule per bit.

Sandeep Saini et al. [28] proposed that the signal level affected by the parasitic are restored using the VLSI interconnect buffers. But buffers have a certain switching time that increases overall signal delay. Furthermore, the transitions occurring in interconnects also contribute to crosstalk delay. Thus, the total delay in interconnects is because of the collective effect of both buffer and crosstalk delay. The replacement of buffers with Schmitt trigger is proposed for the reason of signal restoration. Signal can rise early due to lower threshold voltage of Schmitt trigger and also, the noise glitches are reduced due to the large noise margin of Schmitt trigger as well. The simulation results shows that using Schmitt trigger approach gives 20% delay reduction as compared to 10.4% as in case of buffers.

B. Dhoedt et al. [29] proposed that the interconnect limitations will decide performance of future generation data processing systems instead of the IC performance. The future increase in CMOS IC complexity and density is the main reason for the expected I/O bottleneck, in terms of chip size, number of I/O pads and clock frequency. The problems naturally linked with closely packed electrical interconnections (such as cross-talk, signal distortion, EMI) will give rise to bandwidth limitations, which will result in a mismatch between interconnect performance and silicon processing capabilities. A two-dimensional optical interconnect has been proposed, alleviating the chip level input/output bottleneck. Two optical arrangements, for inter-MCM(*microoptical* module) and intra-MCM interconnect respectively, were discussed and first results on optical components were presented, as well as performance characteristics of first generation opto-electronic components.

Guoqing Chen et al. [30] proposed that interconnect are becoming the main hinderance in integrated circuit design. It will become ever more difficult for conventional copper interconnect to satisfy the design requirements of delay, power, bandwidth, and noise, if CMOS technology is scaled down. On-chip optical interconnects have been considered as

a probable replacement for electrical interconnect since the past two decades. Predictions of the performance of CMOS compatible optical devices are made on the basis of present state-of-art optical technologies. Optical and electrical interconnects are being compared for a variety of design criteria based on these predictions. The optical interconnect becomes advantageous over electrical interconnect beyond the critical dimensions of approximately one tenth of the chip edge length at the 22 nm technology node.

Charles Thangaraj et al. [31] proposed that nanometer CMOS technologies have necessitated a better interconnection technology, as long global interconnects have been shown to be a design bottleneck. Optical interconnect technology is a prospective alternate to traditional electrical interconnects and has immense potential to improve interconnect delay, jitter, clock skew, and have better signal integrity. The keys to successful adjustment of on-chip optical interconnects are simplicity of integrating optical components into standard CMOS manufacturing and the manufacturing cost. A truly CMOS compatible optical clock distribution system is presented and enabled the successful acceptance of on-chip optical interconnects. The proposed clock recovery components and optical clock distribution system were implemented on silicon as a test vehicle in a mature 0.35 micro meter CMOS process for practicability analysis. The experiments on the test chip established the feasibility of the proposed approach and the overall system functionality, despite many aspects of the test circuit designs can be improved further. No fundamental challenges were observed in successfully implementing the design presented in advanced nanometre CMOS technologies that required greater than 10 GHz clock rates.

Thijs Spuesens et al. [32] proposed that with the increasing demand for bandwidth, optical interconnects are coming closer to the chip. Integration with CMOS is possible using optical interconnects on silicon-on-insulator (SOI) and the mature processing can be used for photonic integrated circuits. III-V active optical components on SOI can be included using a heterogeneous integration process and for that, compact sources and detectors are required, but the integration density is limited by the need of different epitaxial structures which is required for efficient working. An epitaxial structure containing both the layers for a laser and for a detector is used, thus ensuring very compact integration of sources and detectors.

Mikhail Haurylau et al. [33] proposed that electrical wires can be outperformed by intrachip optical interconnects and provide a solution to the communication bottleneck in high-performance integrated circuits. The requirements that silicon-based ICs must satisfy to successfully outperform copper electrical interconnects (IEs) are explored by using the International Technology Roadmap for Semiconductors (ITRS) as a reference. The requirements for individual optical interconnects components are identified by study of parameters such as bandwidth density, delay, and power consumption.

Sung Min Park [34] proposed that the amplifiers effectively isolate the large input parasitic capacitance and therefore, realize considerable bandwidth improvement by exploiting regulated cascode (RGC) configuration for the input stage. For 0.5pF photodiode capacitance, a 950 MHz bandwidth is shown by l.25-Gb/s RGC TIA and the difference of only 93MHz is present even for 1pF photodiode capacitance. A bandwidth of 2.2GHz is shown by 2.5-Gb/s RGC TIA fabricated in a 0.6um CMOS technology for 0.5pF photodiode capacitance, hence confirming the RGC mechanism. A differential RGC TIA is also realized in a 0.25pm CMOS technology. Optical measurements made show 1.25-Gb/s operation for 1pF photodiode capacitance.

Atul K. Nishad and Rohit Sharma [35] proposed an analytical time domain model for top contact and side contact multilayer graphene nanoribbon (MLGNR) interconnects. The physical aspects regarding the transient behaviour of these MLGNRs is given in the proposed models. The proposed models were compared with existing data as well as exhaustive simulation and show superb accuracy. They identified limiting factors that need to be taken into account for the design of optimal top contact MLGNRs that surpass the performance of copper and compared it with side contact MLGNR interconnects. Finally, they compared the performance of their optimum top contact MLGNRs with optical interconnects.

Drew Guckenberger et al. [36] demonstrated DC-coupled transimpedance amplifier (TIA) architecture for optical receiver front-ends with low- power requirements. 12.5 Gb/s performance is achieved for TIAs implemented in 0.25um CMOS and 47GHz SiGe BiCMOS technologies while drawing approximately, 1mA from 1.5V and 1.8V supplies. Data coding requirements for the system can be decreased by DC- coupling of the interface circuits to the photodetection device. A voltage gain stage with resistive negative feedback is used in conventional transimpedance amplifier (TIA) designs. This

configuration results in a trade-off between input impedance and gain, which sets the bandwidth.

Guoqing Chen and Eby G. Friedman [37] proposed that interconnects have a significant role in deep sub-micrometer VLSI technologies. Several design criteria are considered in interconnect design, like power, delay and bandwidth. The minimum power in an RC interconnect can be achieved using a repeater insertion methodology at the same time as fulfilling delay and bandwidth constraints. The number and size of the repeaters in a design space is determined by these constraints. The minimum power occurs at the boundary of the design space. Closed form solutions for the minimum power requirement are developed using the delay constraints, with the average error of 7% as compared with SPICE simulations. The minimum-sized repeaters can be used to achieve the minimum power dissipation with existing bandwidth constraints. The analysis of the effects of inductance on the bandwidth, power and delay of an RLC interconnect with repeaters is also done. Under a delay or bandwidth constraint, the minimum interconnect power decreases as compared to a RC interconnect by including inductance.

Fernando Paixao Cortes et al. [38] focused on the analysis of numerous analog circuits, including their functionality, while using different designing techniques. Initially, the two key design parameters: slope factor n and early voltage VA, were derived from simulations. The designing and analysis of three different analog circuits was shown. The two design methodologies implemented on an analog amplifier design are compared. The transistors are in saturation in the first approach while the second one is based on the g_m/I_d characteristic which allows a single synthesis methodology in all regions of operation of the transistor. Then the analysis of the analog modules for comparison and continuous filtering is done.

Hoi-Jun Yoo and Sung Min Park [39] realized a transimpedance amplifier (TIA) for Gigabit Ethernet applications in a 0.6 μm digital CMOS technology. The regulated cascode (RGC) configuration is exploited as the input stage by the amplifier, therefore achieves a large efficient input transconductance as that of Si Bipolar or GaAs MESFET. The input parasitic capacitance which includes photodiode capacitance is isolated from the bandwidth determination by the RGC input configuration, which is better than common-gate TIA. From a single 5-V supply, the chip core dissipates 85 mW power.

C.L. Schow et al. [40] reported a transimpedance amplifier fabrication in a 0.13mm CMOS process which is functional at bit rates up to 25 Gbit/s and having a power consumption of 0.36mW/Gbit/s. A transimpedance gain of 42 dBΩ is provided by the amplifier at a 15 GHz bandwidth and show a bit error-ratio of less than 10^{-12} for peak-to-peak input currents of 225 and 425mA at 20 and 25 Gbit/s respectively. The TIA is a DC-coupled, modified common-gate (CG) design that was fabricated in the IBM CMOS8RF-LM technology, which is a standard 0.13mm process with eight metal layers. The sensitivity of the TIA was evaluated by measuring the bit-error-ratio as a function of the input optical power.

Giovanni Anelli et al. [41] simulated and measured performance of a transimpedance amplifier designed in a quarter micron CMOS process. The amplifier can be included in any submicron CMOS process as it contains only NMOS and PMOS devices. The utilization of a transistor in the feedback path in place of a resistor is the main feature of this design. The optimization of circuit is done to read signals coming from silicon strip detectors having few pF input capacitance. An output pulse fall time of 3ns and an Equivalent Noise Charge (ENC) of around 350 electrons rms is calculated for an input capacitance of 4pF, an input charge of 4fC and a transresistance of 135kΩ. An improvement in the performance of the chip is seen when measurements are done at 130K. An integrated circuit containing 32 channels has been designed. The chip's radiation tolerance is improved by using special techniques to lay it.

Jing Xue et al. [42] proposed that a fundamental change in intra-chip and inter-chip interconnect technologies is demanded by the communications based nature of future high performance computing devices. Optical interconnects are a promising long term solution. A lot of investigation is required for on-chip optical interconnect networking issues in spite of significant progress made in optical signaling in recent years. The conventional packet-switching architectures are insufficient to realize the full potential of optical interconnects which are used for conventional electrical signaling. They proposed and studied the free-space optics design of a fully distributed interconnect architecture. The architecture makes use of a set of newly-developed or developing devices, circuits, and optics technologies. The interconnect offers scalable bandwidth and an ultra-low transmission latency, and provide new opportunity for coherency substrate designs and optimization.

Timir Datta and Pamela Abshire [43] made observations relating to the efficiency of this technique in both weak and strong inversion. The present analytical and simulated results quantified these observations. The low cost in CMOS fabrication and the simplicity of operation made the use of CMOS current mirrors interesting to circuit designers. But, the device mismatch is possible CMOS current mirror due to process variations. For mismatch compensation, floating gate transistors are used in recent years. The floating gates compensation works well in correcting mismatch for subthreshold operation but, new mismatch effects are seen in above threshold operation for same compensation.

Milaim Zabeli et al. [44] studied the impact of physical parameters which describe the MOSFET transistors structure on the threshold voltage value. The role of substrate (the body effect) on the threshold voltage is also analysed. The MOSFET threshold voltage value will have an impact on the dynamic and static mode of device. The impact of each single physical parameter on the total value of threshold voltage can be seen using the results obtained. These parameters will have considerable and small impact on the threshold voltage. So the values of MOSFET physical parameters can be adjusted to reach the accepted threshold voltage.

Ahmed Emira et al. [45] proposed effect of three design transistor parameters (DC current, width and length) on the current mirror performance. An expression is derived for each specification valid for any inversion level based on only one-equation for all-region MOS model. The experimental results of a current mirror fabricated in 0.5µm AMI CMOS process are in fine accordance with the theoretical ones. The analysis of the performance of simple current mirror is done using the one-equation model.

2.5. Conclusion

After the detailed study of the research papers on the various aspects, it is found that extensive research work has been done on optical interconnects at 180nm, 90nm and 65nm technology nodes but lots of work is needed to be done at lower technology nodes i.e. 32nm, 22nm and below. There has been a constant research going on the methods of increasing the bandwidth density of the optical interconnects by wave division multiplexing and other techniques. The total delay in interconnects is because of the collective effect of both buffer and crosstalk delay. The replacement of buffers with Schmitt trigger is proposed for the reason of signal restoration. The number and size of the repeaters in a design space is determined.

CHAPTER 3

COPPER INTERCONNECTS

3.1. Introduction

Enhancements in integrated circuits (IC) density and performance have fuelled semiconductor industry and the resultant information revolution for over 40 years. The improvements in density (Moore's Law) and performance has been achieved through evolutionary and revolutionary advances in the front end of the chip manufacturing line, where the circuit elements are fabricated, and the back end, where these elements are appropriately wired within the IC. Chip interconnections or interconnects, serve as global wiring, connecting circuit elements and distributing power. Copper interconnects are used in interconnection of semiconductor integrated circuits mainly microprocessor using copper. Chips using copper interconnects have smaller metal components and use less energy to pass electricity through them as compared to aluminium. This help in developing high performance processor [46].Copper interconnects fabricated by a dual damascene process offer advantages of performance, cost, reliability over existing aluminium wiring process. Performance is gained because the resistivity of copper is approximately 40% lower than that of aluminium, so copper wires exhibit approximately 40% lower RC delay than aluminium wires of the same cross section. By combining the copper interconnect with a dielectric material with a low permittivity, the interconnect RC delay can decrease upto 50% of that for Al/SiO2. Moreover, the dual damascene approach, compared with single damascene, provides lower via resistance reducing the number of interfaces in the vias. The interconnect RC delay can also be reduced by increasing the thickness T of the metal layer, i.e., by increasing the aspect ratio AR, or by increasing the pitch P of the line. However, when the aspect ratio is increased by increasing T, the capacitance C_L is also increased, and high aspect ratios are hard to fill uniformly; therefore, industry roadmaps predict local wiring AR <1.7 and global wiring AR < 2.2, [46]. Cost reduction comes from eliminating some process steps and simplifying other process steps in the dual-damascene process. Reliability is improved because the electrochemical deposited copper, when compared with aluminium, exhibit far less electromigration and far less stress migration. Other advantages of using copper include that copper has twice the thermal conductivity of aluminium and copper has ten to 100 times more resistance to electro migration failures as compared aluminium. Electro

migration causes transport of the conductor material as a result of high current densities, which can eventually lead to a void in the conductor [47]. The use of copper results in power dissipation reduction of 30% at a specific frequency. By using copper rather than aluminium as an interconnect material, interconnect routing can be simplified, reducing the number of interconnect levels and resulting in fewer process steps. This is cost saving and give higher performance.

3.2. Modeling of Global interconnect

The global interconnect cross section is shown in Figure 3.1. For a given process technology and a given layer, the interconnect thickness T, the height of the metal layer from the substrate H, the width W and spacing between the signal and ground line S are the commonly used variables in the optimization of global interconnect [48]. Only delay and the bandwidth effects are included in the FOM. Other performance parameters such as power dissipation and area are not taken into account. Consequently, the optimization results can't ensure overall the optimum system performance. The interconnect width and spacing are optimized under two scenarios, 1) spacing is kept at its minimum value and 2) spacing is kept the same as line width, for various International Technology Roadmap for Semiconductors (ITRS) technology nodes.

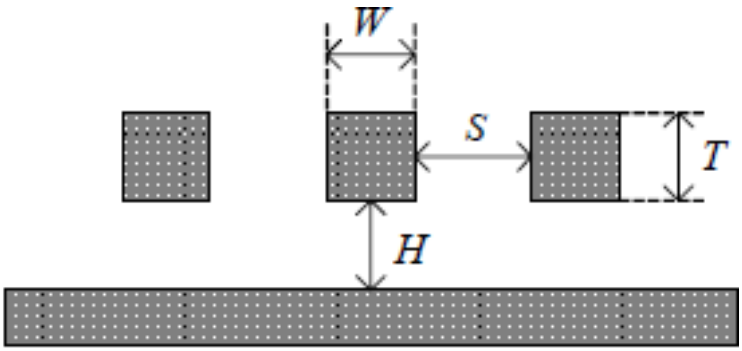

Figure 3.1 Cross section of global interconnects [26].

Here, *W* is the interconnect width, *S* is the spacing between the neighbour interconnects, *T* is the interconnect thickness and *H* is the dielectric height.

Coupling lines above one metal ground (for top global layer)

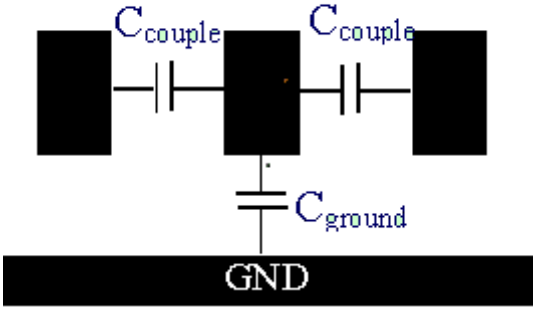

Figure 3.2 Schematic showing the inter-metal and the inter-level components of capacitance.

C_{ground} : Area and fringe flux to the underlying plane

C_{couple} : Coupling Capacitance

Power dissipation depends on charging and discharging of its capacitance. At a given technology node, the interconnect power is heavily dependent on its total capacitance.

Formulas used for the analysis are [49]:

Resistance (R):

$$R = \frac{\rho . l}{w . t} \tag{3.1}$$

For Cu:
Resistivity, ρ=2.2μohm

Inductance (L):

$$L = \frac{\mu_0 . l}{2\pi}\left[ln\left(\frac{2l}{w+t}\right) + \frac{1}{2} + \frac{0.22(w+t)}{l}\right] \tag{3.2}$$

μ_0 =4π×10^{-7} $H\ m$

Capacitance (C):

Total capacitance of the wire ($\mathbf{C_{total}}$) =

$$C_t = C_g + 2C_c \tag{3.3}$$

C_g: Area and fringe flux to the underlying plane

$$\mathbf{C_g} = \varepsilon\left[\frac{w}{h} + 2.04\left(\frac{s}{s+0.54h}\right)^{1.77} . \left(\frac{t}{t+4.53h}\right)^{0.07}\right] \tag{3.4}$$

C_c: coupling capacitance

$$C_c = \varepsilon \left[1.41 \frac{t}{s} e^{\frac{-4s}{s+8.01h}} + 2.37 \left(\frac{w}{w+0.31s} \right)^{0.28} . \left(\frac{h}{h+8.96s} \right)^{0.7} \right] \qquad (3.5),$$

l= Length of the interconnect

ρ = Resistivity

t = Thickness of interconnect

w = Width of interconnect

h= Height of metal layer from the substrate

s = Spacing between the signal and ground line

3.3. Cmos Inverter as Buffer

In copper interconnects, repeater or buffer is basically implemented as CMOS inverter [25]. A CMOS inverter is used to derive interconnect load. PMOS is assumed as thrice as NMOS in CMOS model.

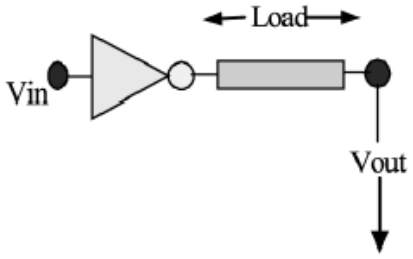

Figure 3.3 CMOS buffer driving an interconnect load [30].

A simple MOSFET model can be considered for circuit analysis, using *n*th power law for short channel devices. A comprehensive analytical scheme can be used to analyse the delay of a CMOS inverter [50]. The current through both the transistors and gate to drain coupling capacitance are taken into account. Interconnect load can be represented by R, L and C parameters. Its RC/RLC lumped model is shown in figure 3.3.

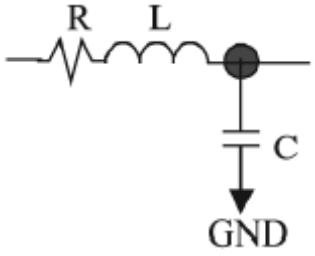

Figure 3.4 RLC lumped model representations of an interconnect line [25].

3.4. Repeater Insertion

For driving long interconnects [51], a single buffer is not a good solution, as they present a very large resistive-capacitive (RC) load at the terminals of the gate(s) connected to it. Instead, a number of buffers are inserted at regular intervals of distance in interconnect, which are termed as repeaters. The insertion of repeaters is used to minimize the interconnect response time by reducing the effect of resistance and capacitance. Repeaters are compatible for driving high resistive capacitive loads. The increase in the load in VLSI circuits due to large fanouts and the long interconnects requires effective driver circuits that can charge/discharge capacitances with sufficient speed, therefore, helping in delay minimization.

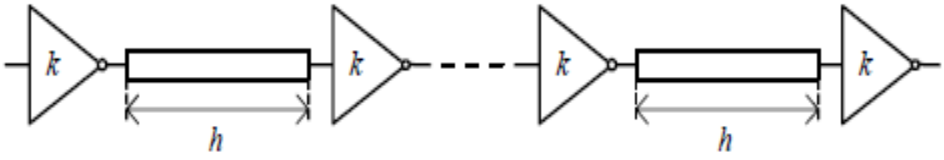

Figure 3.5 Repeaters insertions in a long global interconnect [26].

An electrical interconnect with repeaters can also be represented with R, L and C parameters as shown in figure 3.6.

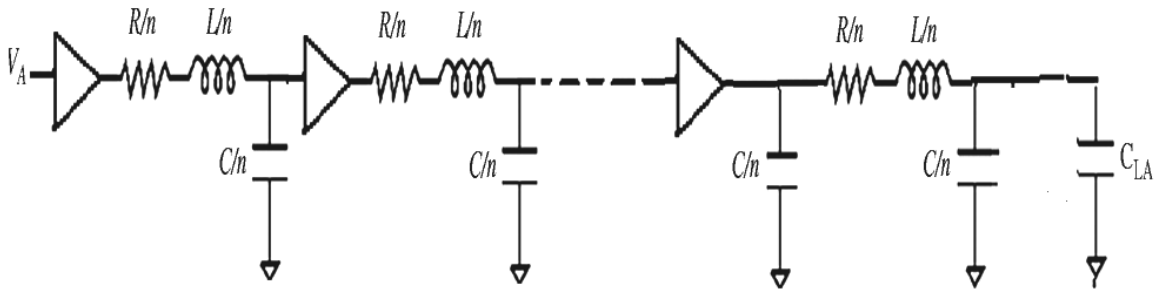

Figure 3.6 Copper interconnects with R, L and C parameters [10].

The delay per unit length after optimization is given by [26]

$$\left(\frac{\tau}{h}\right)_{opt} = 2\sqrt{r_s c_0 \frac{\rho}{T}}\left(1+\sqrt{\frac{1}{2}\left(1+\frac{c_p}{c_0}\right)}\right)\sqrt{\frac{c}{w}} \propto \sqrt{\frac{c(w,s)}{w}} \qquad (3.6)$$

The input capacitance is c_0, the output parasitic capacitance is c_ρ and the output resistance is r_s.

The power dissipation per unit length for a global interconnect is given by [26]

$$\frac{P_{total}}{h_{opt}} \propto c(W, S_{min}) \qquad (3.7)$$

If R, L and C are the values for one repeater, then for n number of repeaters it will be $\frac{R}{n}$, $\frac{L}{n}$ and $\frac{C}{n}$.

3.5. Future Materials for Interconnects

The increasing copper resistivity due to surface and grain boundary scattering results in increasing resistance-capacitance delay, and it has become a near-term challenge for copper interconnect. The current density through the copper interconnects also increases as the feature size scales down, which aggravates the electro-migration (EM) reliability of the copper interconnect. Copper can be replaced with new materials like metal silicides, carbon nanotube and graphene nano-ribbon and other interconnect scheme like optical interconnect and wireless interconnect [52].

- **Optical interconnects**- Optical interconnect is used in communication by optical waveguides. Optical wires can handle high bandwidth; from 10 Gbit/s up to 100 Gbit/s. Optical interconnects have low cross talk, minor frequency dependent loss and high band width. Optical interconnects aren't used commercially much since optical interconnects technology is incompatible with manufacturing processes and assembly methods that are currently being used in the semiconductor industry [53].

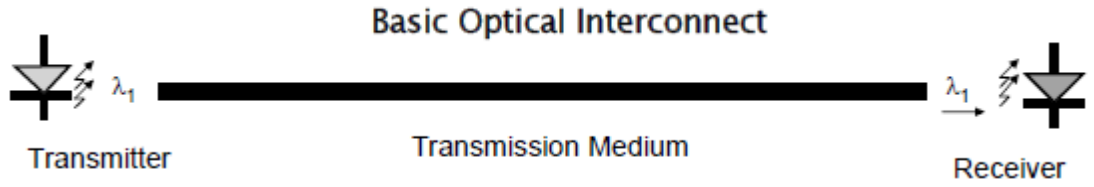

Figure 3.7 Optical fiber interconnect fundamental [54].

- **Carbon Nanotube interconnects-** Carbon nanotubes are the allotropes of carbon consisting of cylindrical nanostructure. Nanotubes are constructed with length-to-diameter ratio of upto 132,000,000:1. They are having amazing thermal conductivity and mechanical and electrical properties. Nanotubes are the member of the fullerene family. Nanotubes are characterized as single-walled nanotubes (SWNTs) and multi-walled nanotubes (MWNTs). On the basis of chirality, CNT are classified as armchair, zigzag and chiral [55].

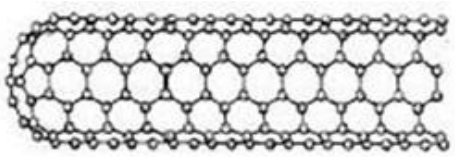

Figure 3.8 (a) Armchair [53]

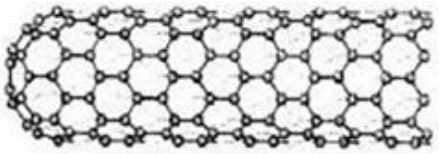

Figure 3.8 (b) Zigzag [53]

- **Graphene nanoribbon interconnects-** Graphene nanoribbon interconnects are strips of graphene with ultra-thin width (<50 nm).The electronic states of GNRs are mostly dependent on the edge structures. Zigzag edges offer the edge localized state with non-bonding molecular orbital near the Fermi energy. Graphene nanoribbons with controlled edge orientation are fabricated by scanning tunnelling microscope (STM) lithography. Zigzag nanoribbons are semiconducting and have spin polarized edges. The gap size is inversely proportional to the ribbon width. Graphene nanoribbons and their oxidized counterparts called graphene oxide nanoribbons have been used as nano-fillers to improve the mechanical properties of polymeric nanocomposites [56].

3.6. Replacement of interconnect materials

Aluminium is replaced by copper interconnects due to less power consumption and smaller chip size possible due to copper. Due to advancement in nanotechnology and increased bandwidth copper interconnect are proving to be slow. Therefore, they are being replaced by optical interconnects, carbon nanotubes interconnects and graphene nanoribbon interconnects.

Optical interconnects and carbon nanotubes interconnects are used to some extent but graphene nanoribbon interconnects are under experimental development.

3.7. Conclusion

Copper interconnects are used in interconnection of semiconductor integrated circuits mainly microprocessor using copper. Chips using copper interconnects have smaller metal components and use less energy to pass electricity through them as compared to aluminium. A number of buffers are inserted at regular intervals of distance in interconnect, which are termed as repeaters for driving long interconnects. The R, L and C values are calculated for the copper interconnect at various technology nodes using the formulae. Due to the advancement in the technology, the copper interconnects are proving to be slow so, novel materials like optical interconnects, carbon nanotubes interconnects are been tested in place of copper interconnects.

CHAPTER 4

OPTICAL INTERCONNECTS

4.1. Introduction

Different classes of digital systems impose specific requirements on the communication medium. These requirements pertain to the communication length scale and the figure of merit of relevance (bandwidth or latency). The choice of the communication medium is heavily dependent on these factors. For example, long-haul systems ubiquitously use optical fibers because of low attenuation at high bandwidths. Systems at shorter length scales have traditionally used copper (Cu) interconnects for both latency and bandwidth sensitive applications. However, as the computational bandwidth of the modern integrated circuits (ICs) increases dramatically according to the Moore's law, Cu traces at short distances are struggling to keep up at least in bandwidth sensitive applications, rendering communication bandwidth a bottleneck.

This presents a fertile ground for optical medium of communication to penetrate the short distance world. Optical interconnects with low signal attenuation and crosstalk could potentially be very useful in short distance, bandwidth sensitive applications. Already many different backplane optical media have been demonstrated and/or their prospect discussed including polymer waveguides [57], fiber image guides (FIGs) [58] [59], fiber ribbons [60], and free space optical interconnects (FSOI) using lens and mirror system.

The optical link consists of an off-chip laser, a quantum-well modulator at the transmitter (converts CMOS gate output to optical signal), a waveguide comprising of a silicon core (refractive index ~3.5), a SiO2 cladding as the transmission medium, and a transimpedance amplifier (TIA) followed by gain stages at the receiver. The total delay of an optical wire is the sum of the transmitter, waveguide, and receiver delays.

An on-chip optical link contains (a) A off chip Laser source which is coupled to the modulators; (b) Optical modulator that is used to manipulate a property of light often of an optical beam such as a laser beam; (c) an optical waveguide that can be implemented as a silicon strip waveguide or a rib waveguide for a 2-D confinement; (d) photo-detector which generates current proportional to the incoming light intensity and (e) a transimpedance amplifier followed by gain stages [17].

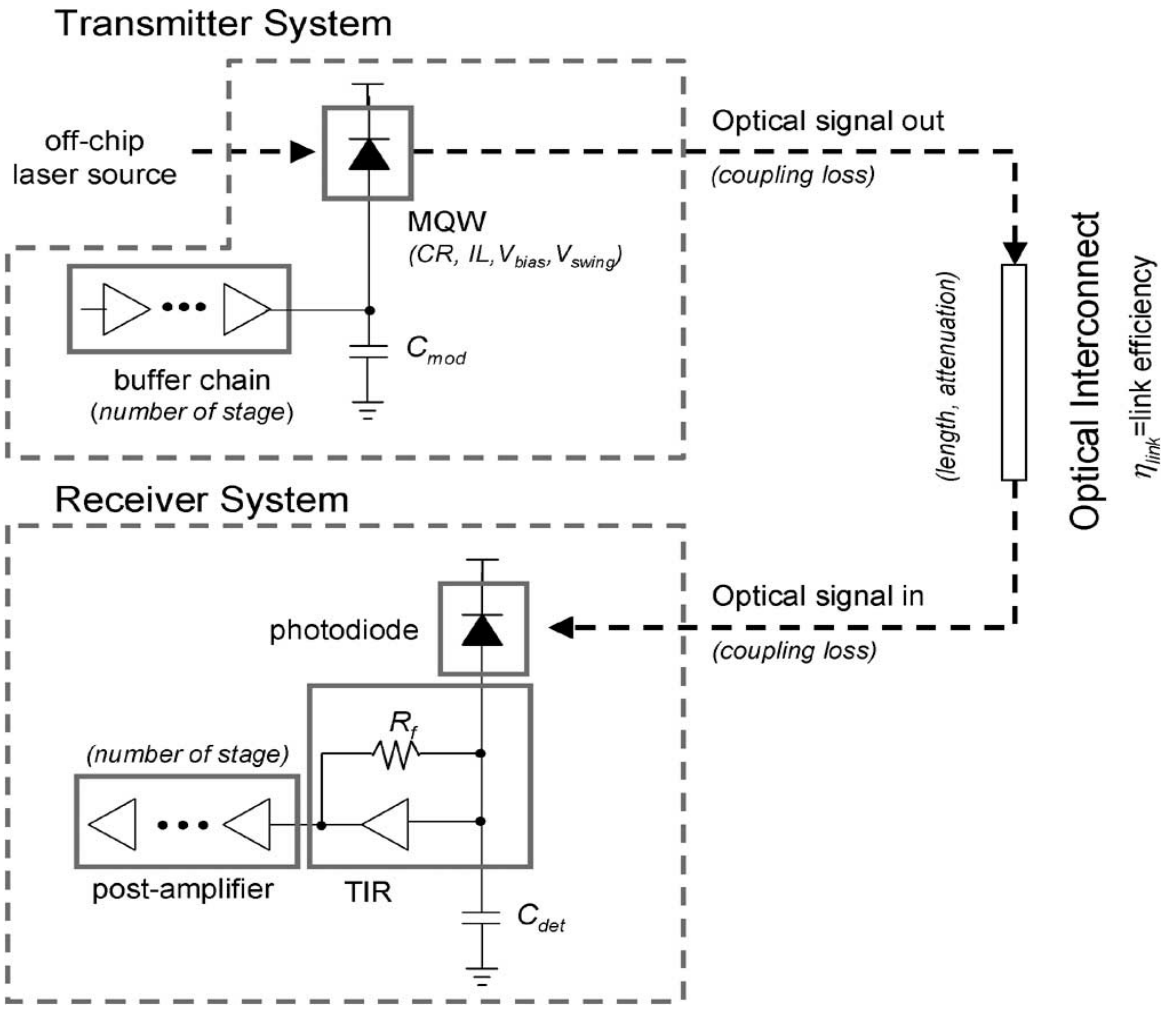

Figure 4.1 Schematic of quantum-well modulator-based optical interconnect [4].

The delay of an optical link t_{opt} is given as

$$\boldsymbol{t_{opt} = t_{tx} + t_{wg} + t_{rx}} \quad (4.1),$$

where t_{tx} is the delay of the transmitter is, t_{wg} is the delay of the waveguide and t_{rx} is the receiver delay.

The link is characterized by five sets of parameters: the characteristics of the CMOS (or bipolar) technology used, the transmitter characteristics, the optical system efficiency, the system fan-out, and the receiver characteristics [5].

4.2. Problem in existing interconnect material

As copper is a better conductor than aluminium, chip size became smaller and power consumption reduced. Copper can withstand more current density than aluminium. The degrading performance of on-chip Cu wires threatens to greatly delay the continued integrated circuits (IC) improvement all along Moore's law. All wire metrics, including latency, power dissipation, bandwidth density, and reliability, for local and global wires

deteriorate with scaling. The high-speed signals can be distorted due to dispersion, reflections and ringing, as well as attenuation and its variation with frequency [4].
Due to an order of size mismatch between nanoelectronic components and wavelength of light, the use of optical interconnects is restricted to global interconnect level.

The optical latency is independent of ΦBW, since a higher ΦBW is achieved just by adding more wavelengths, which does not impact the latency of each wavelength. In contrast, both CNT and Cu latency increases with ΦBW, as a smaller wire pitch increases resistance and the resulting number of repeater stages. The CNT and Cu power density nonlinearly increases with ΦBW, following the dependence of total wire capacitance while power density linearly rises with ΦBW for an optical wire [4]. The power dissipation in the electrical schemes has strong switching activity dependence while the optical link is independent of switching activity.

4.3. Optical interconnects

The term optical interconnect is assumed to deal with data transmission inside an electronic device or system using light. It can be compared with optical communication which refers to optical data transmission between distant and independent systems. Optical interconnection refers to the data transmission in which the data signal is transmitted as a modulation of optical carrier wave (light) through an optically transparent media such as optical fibre, planar optical waveguide or air. Nearly all optical data links actually function at the near-infrared wavelength range between 800 nm and 1600 nm. . Optical communications through fibre has been the technology of choice for high-speed long-distance data links. The optical links have emerged into shorter distance applications as the capacity requirements have increased, such as fibre-to-the-home and even into fibre-optic interconnects between boards and cabinets inside electronic equipment which is referred as optical interconnects.

Optical interconnect are free from any capacitive loading effects. They do not suffer from crosstalk. The speed of propagation of a signal is determined by the speed of light and the refractive index of the optical transmission medium only. They do not suffer from electromigration- induced failure. Optical chip-to-chip interconnections can be anchored directly to the interior of a chip rather than to a pin on its perimeter. Chip-to-chip optical interconnections operate at much higher speeds allowing the multiplexing of a large number of I/O signals. They can carry a large amount of information and can also have very short pulses(less than 1 picosecond). They provide the possibility of imaging interconnects which means 10000 connections with one lens. Both of these, the fibers and

imaging enable very dense interconnect. Optical interconnects provide the opportunity of No pick–up of electrical noise while transmission. Optical isolation of different voltage levels is possible [61].

There are 3 types of configuration of optical interconnect:

- Thin-Film Waveguides

  Nanometallic or plasmonic metal waveguides have been considered for on-chip waveguiding in both single conductor and two-conductor waveguides. Such waveguides can be very small, possibly even smaller than dielectric waveguides. Such very small waveguides could concentrate light to very small device volumes.

- Optical Fibers

  Fibers are used to take the information from each chip, to connect even a small bit of the information from multiple chips to the world outside the board. WDM is used on these external fibers.

- Free-Space or Holographic

  Free-space optics can also be attached within a chip, though it has received relatively less attention in the research literature. A free-space approach is certainly an interesting option for delivering clock signals synchronously over an entire chip [62].

4.4. Need of Optical Interconnects

The rapid growth of the VLSI technology is mainly due to the constant reduction of the VLSI devices. Feature size is minimum transistor size. With the rapid developments in VLSI technology, designs and CAD techniques, the central processor cycle times are reaching the vicinity of 1 ns and communication switches are being designed to transmit the data which have frequency greater than 1 GHz .The ever increasing quest for high speed applications is placing higher demands on interconnect performance and highlights the previously negligible effects of interconnects such as ringing, signal delay, distortion, reflection and cross talk [63].

The global interconnect delay grows as a cubic power of the scaling factor [64]. It is predicted that interconnects will be responsible for nearly 70 to 80% of the signal delay in high-speed Systems. These interconnect effects can cause logic glitches if not considered during the design stage that renders a fabricated digital circuit unoperational, or could distort an analog signal in a way that it fails to meet specifications. As extra iterations in the design cycle are costly, precise prediction of these effects is a required in

high-speed designs. It becomes extremely important for designers to simulate the entire design along with interconnect sub circuits as efficiently as possible while retaining the accuracy of simulation.

When technology continues to scale into deep sub-micron regions, there is a corresponding increase in chip size and device speed. Whereas transistor scaling provides simultaneous improvements in both density and performance, interconnect scaling improves interconnect density but generally at the cost of degraded interconnect delay as illustrated in Figure 4. Results of theoretical modelling indicate that below 1µm minimum feature size, interconnect delay because of parasitic capacitance which includes both fringe and inter-wire coupling capacitance, will have a strong impact on circuit performance [64]. As a result, effects of interconnects, which previously have been regarded as trivial, are becoming more prominent. These effects include bus delays, clock skews, coupling signal noise, and power/ ground noise. To address these problems, active research has resulted in the following technological trends [65].

- Increasing the aspect ratio
- Increasing the number of metal layers
- Reducing dielectric constant
- Reducing resistivity of metal line

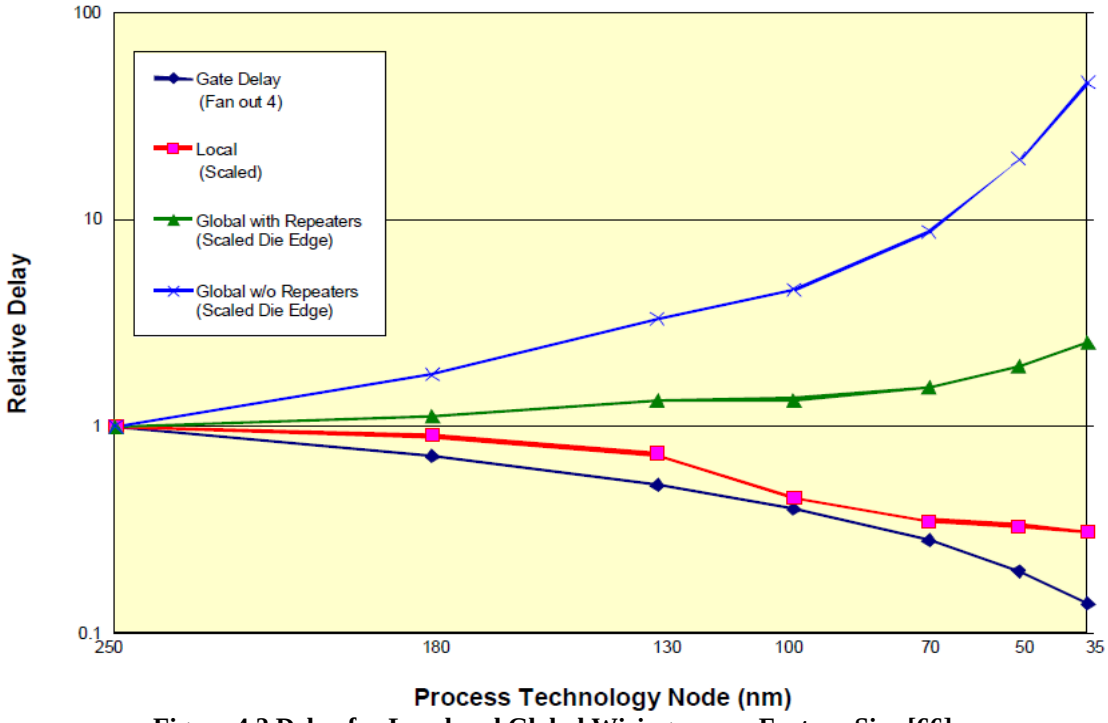

Figure 4.2 Delay for Local and Global Wiring versus Feature Size [66].

4.5. Working Operation

Optical interconnect are compatible with a CMOS technology at 1.5 μm wavelength light source with a silicon modulator and a SiGe or Ge photo-detector. Optical devices are not readily scalable like electrical devices due to the light wavelength constraint. The integration ability and performance of optical devices are expected to further improve by structural optimization and technology inventions. A transmitter consists of a driver circuit and an electro-optical modulator. The design of a fast and cost efficient CMOS compatible electro-optical modulator is one of the most difficult tasks in realizing on-chip optical interconnects. A comprehensive closed-form model is used to determine a proper trade-off among all physical parameters of a MOS modulator to optimize the performance of a modulator. The modulator is driven by a series of tapered inverters. For a definite operating wavelength of 1.5μm, low refractive index strip polymer waveguides are supposed with a core cross section of 1.5 μm×1.5 μm. The refractive index of core and cladding are 1.6 and 1.1 respectively. The mode effective index is determined as 1.48. The receiver has two components: a photo-detector and an amplifier. Si-Ge based photo-detectors [67], low-loss input couplers and optical amplifiers [30], are providing the possibility of an on-chip optical communication system.

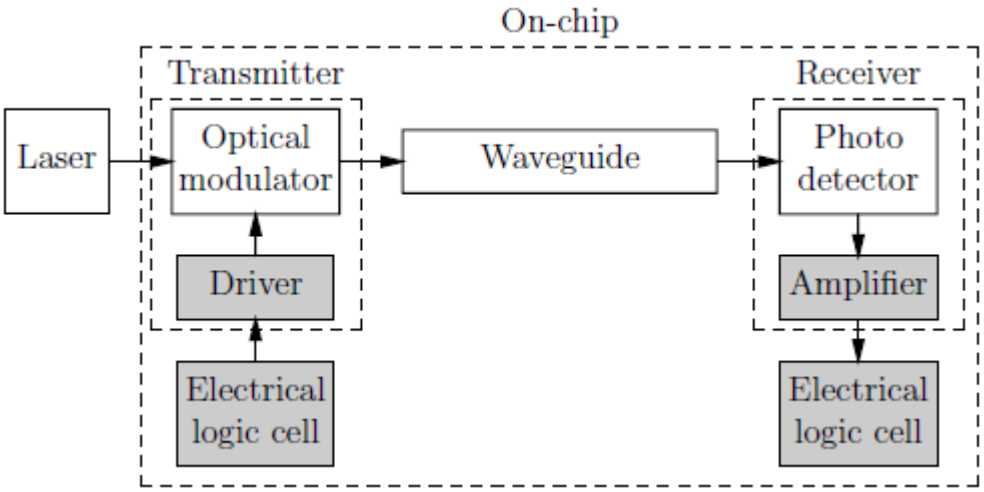

Figure 4.3 On-chip optical interconnect data path [12].

The spatial-bandwidth for the optical interconnects is higher than their electrical interconnect using Wave Division Multiplexing (WDM). Several architectures have been projected for on-chip optically connected multi-processor systems. On the basis of these systems, architects have found modest performance improvement against their electrical counterparts. Though, the majority of performance evaluations ignore the technological

challenges that will arise out of integration, such as controlling the thermal sensitivity of optical devices. For example, while a ring-resonator based modulator requires only ~100μW data-modulation power, the thermal heater required for these devices to operate reliably requires 10mW for 40-degree C temperature compensation, thereby rendering any comparison that doesn't account for thermal control power incorrect. Different choices of technologies can be made when robust operation is considered, and may challenge the conventional expectations about dense optical integration [68].

The electrical power is evaluated for optical interconnect and the power dissipated by the optical and electrical interconnect is compared. The power consumed by the transmitter dominates the power of the receiver in optical interconnect. Both the electrical and optical interconnect power consumption increases due to higher clock frequencies and larger leakage current. The ability to transmit data through a unit width can be evaluated using bandwidth density. The clock rate is the maximum bit rates for a single interconnect. Single wavelength optical interconnects are not advantageous if the high bandwidth density is desired. The bandwidth of optical interconnects, however, can be significantly improved by introducing wavelength division multiplexing (WDM). The bandwidth density of different interconnects is compared. For optical interconnect with WDM, the channel number in a waveguide is assumed to be one at the 90 nm technology node, and to increase by four for each new technology node [69].

4.6. Classification of Optical Interconnects

Interconnects are classified using the international packaging level hierarchy (Tummala & Rymaszevski 1989), which is based on the type of interconnected components and their typical interconnection distances as follows:

1. Chip level (intra-chip): 0-10 mm
2. Multi-chip-module level (intra-MCM or chip-to-chip): 1-100 mm
3. Board level (MCM-to-MCM or chip-to-chip): 10-300 mm
4. Backplane level (board-to-board): 0.1-1 m
5. Cabinet level (rack-to-rack): 0.3-5 m
6. System level (cabinet-to-cabinet): 1-100 m.

4.7. Transmitter

A transmitter consists of an electro-optical modulator and a driver circuit [70]. CMOS circuits are examined for driving both MQW modulators and VCSEL's. From a system designer perspective, using VCSEL's as transmitters is advantageous in terms of simplifying the system optics because the required optical energy can be generated on-chip rather than using an external laser source. On the other hand, multiple quantum well (MQW) modulators have an advantage over active light emitters in terms of signal and clock distribution [71].In these systems, the clock can be distributed optically to eliminate the clock skew and jitter problem, which exists in all large-scale systems. The input digital electrical signal is first fed into the transmitter driver circuit, converted to an optical signal by the transmitter, and then routed to the detector by the optical system. Bipolar transistors are studied to drive VCSEL's for high bandwidth applications.

4.7.1. MQW Modulators with CMOS Driver Circuits

The circuit schematic of a MQW modulator driven by a CMOS superbuffer circuit is shown in figure 4.2. The superbuffer is a set of cascaded inverters, and the size of each inverter is larger than the previous one by a constant factor of β [23]. The first inverter is a minimum size inverter, and the last inverter drives the modulator. The optical power in a modulator-based system is generated by an external light source, and the electrical power dissipation of the light source is thus not included in the total on-chip power dissipation [5].

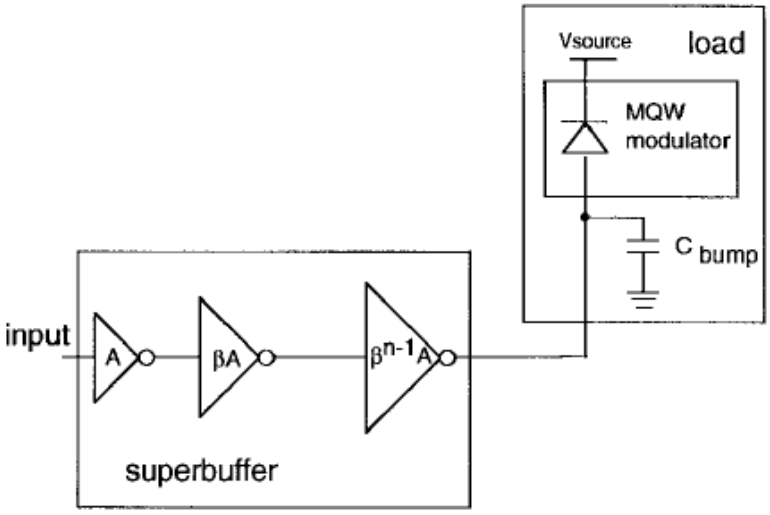

Figure 4.4 CMOS superbuffer driving the MQW modulator [5].

The total power dissipation in superbuffer is given as

$$P_{ab} = C_{total}.V_{dd}^2.\frac{BR}{2} \quad (4.2),$$

where C_{total} is the total capacitance of the superbuffer (i.e. of inverters) and BR is the bit rate with units of bits/second, and the transient on-current is neglected. The total capacitance is the sum of input and output capacitance of all the inverters and is in the form of

$$C_{total} = \left(C_{load} - C_{in,min}\right) + \sum_{k=0}^{n-1}\left(C_{in,min} + C_{out,min}\right).\beta^k \quad (4.3),$$

where $C_{in,min}$ and $C_{out,min}$ are the input and output capacitance of a minimum size inverter for a given CMOS technology, and is the load capacitance of the superbuffer and includes the modulator capacitance and any parasitic capacitance as seen by the last inverter of superbuffer.

The modulator performance is characterized by its contrast ratio (CR) and insertion loss (IL) at its optimal bias voltage with a voltage swing. The maximum voltage swing is determined by the voltage supply of the driver circuit. The power dissipation in the modulator due to absorbed light power is

$$P_{diss,MQW} = \frac{F.P_{opt,rec}}{\eta_{link}}.\frac{q}{h\vartheta}.\left(\frac{V_{bias}.\left(1 + IL - \frac{1-IL}{CR}\right) - V_{dd}.IL}{(1-IL).(1-\frac{1}{CR})}\right) \quad (4.4),$$

where $P_{opt,rec}$ is the average optical power required at the receiver input, F is the system fan-out, and η_{link} is the optical system efficiency. The total power dissipation of the transmitter is the sum of the power dissipated in the modulator due to optical absorption and the switching power of the superbuffer.

4.7.2. VCSEL with Cmos Driver Circuit

The output stage of the CMOS VCSEL driver circuit consists of two NMOS transistors (N_A and N_B) providing the threshold and the modulation currents, respectively, and a superbuffer are driving the gate of N_A. The total electrical power dissipated in the driver and VCSEL can be separated into two parts: the power dissipation of the

superbuffer and the power dissipation of the VCSEL and the two transistors due to their current flow [5].

The total laser current is the sum of the threshold current and the average modulation current. The modulation current is assumed to have a 50% duty cycle. The source voltage is the sum of the threshold voltage of the VCSEL, the voltage drop across its series resistance when the modulation current flows and the minimum source-drain voltage required ensuring that the transistor is in its saturation region.

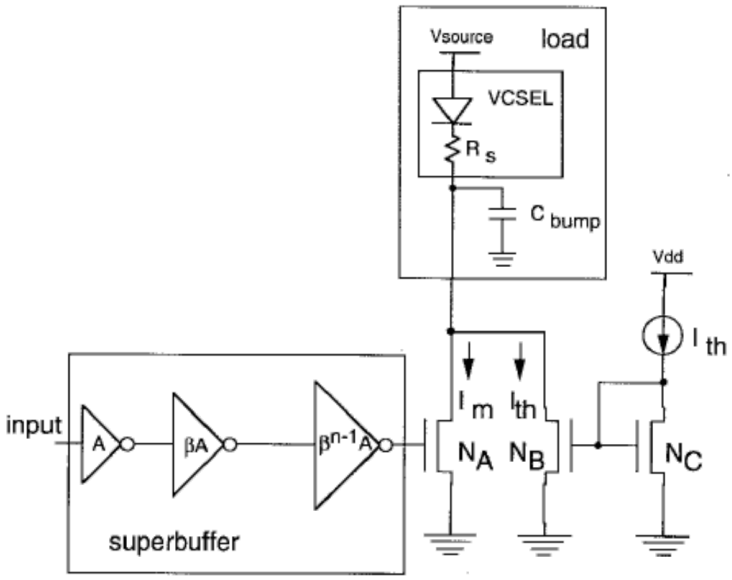

Figure 4.5 Output driving stage of a CMOS driver connected to the VCSEL [5].

The total electrical power consumed in the VCSEL and the output stage is

$$P_{CMOS,VCSEL} = I_{total}.V_{source} \quad (4.5),$$

$$= \left[I_{th} + \frac{I_m}{2}\right].[V_{th} + R_s.I_m + (V_{dd} - V_{th})] \quad (4.6),$$

For a given laser slope efficiency (η_{LI}) , the average output optical power is

$$P_{opt,transmitter} = \frac{I_m.\eta_{LI}}{2} \quad (4.7),$$

where the spontaneously emitted power at threshold is neglected.

4.7.3. VCSEL with a Bipolar Driver

The output driving stage implemented using bipolar transistors is shown in figure 4.5. Because of the parameter variations in bipolar technology, a differential configuration is imperative [72], [73]. The sum of the emitter currents of transistors Q_B and Q_A is fixed by joining a current source to the transistor. The partitioning of the fixed current between Q_B and Q_A is dependent on the differential voltage supplied to the bases of these two transistors. The currents in these transistors are designed such that when the threshold current (I_{th}) flows through Q_A, the current through Q_A is equal to $I_{th} + I_m$, and vice versa. The total current in the output driving stage is thus ($2I_{th} + I_m$).

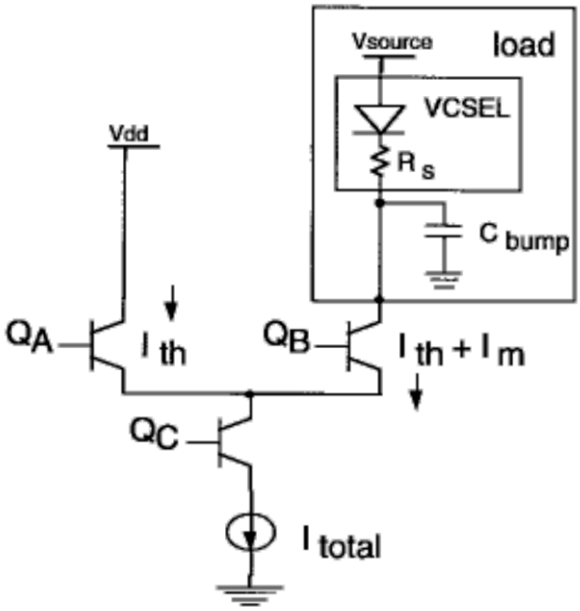

Figure 4.6 Output driving stage of a bipolar driver connected to the VCSEL [5].

The power supply voltage for the bipolar driver circuit is the sum of the threshold voltage, the voltage drop across its series resistance, and the collector-emitter voltage (V_{ce}) across both Q_B and Q_C. For a high frequency operation, both Q_B and Q_A are generally biased in their active regions. V_{ce} is typically 1 V or higher when a BJT is in its active region. The total dissipated power is

$$P_{bipolar,VCSEL} = [2I_{th} + I_m] \cdot [V_{th} + R_s \cdot I_m + 2V_{ce}] \quad (4.8),$$

which is about twice as that in a CMOS driver.

4.8. Waveguides

Wavelength of the optical signal and optical material limit the performance of waveguide [3]. Although a novel waveguide like photonic crystal waveguide decreases the waveguide pitch but gives optical losses. There are two types of the waveguide

material for the operating wavelength of the signal. A silicon-on-insulator (SOI) structure is used for the applications requiring dense and short waveguide arrays because of its smaller waveguide pitch. Low loss polymers are used for longer links as they give smaller losses and optimized propagation delay [74] [75]. Area required by polymer waveguide for fabrication is larger than the area required by SOI waveguides but polymer waveguides are fabricated on an additional layer, so they do not reduce the on-chip silicon resources. Polymer waveguides have low refractive index. They have effective index of 1.4 [74].

The delay through the optical waveguide can be expressed as

$$t_{wg} = \eta_{eff} \frac{L}{c} \tag{4.9},$$

where η_{eff} is the effective refractive index of the mode in the waveguide medium, *c* is the speed of light in the vacuum and *L* is the waveguide length.

The high dielectric contrast confinement shrinks the wavelength of the light to dimensions of $\frac{\lambda}{n}$ .Smaller sized devices are preferred because they provide faster optoelectronic transduction, higher local fields to drive non-linear interactions and higher levels of integration which gives new functionality at lower costs [17]. The variation in waveguide dimensions results in skews at different branches.

4.9. Receivers

The receivers considered are of the transimpedance type due to their high bandwidth, low noise, and ease of biasing. The operational model of a transimpedance receiver can be broken into four components: the detector, the transimpedance amplifier, the voltage amplifier, and the decision circuit. The detector produces the photo-current based on an optical signal. The transimpedance amplifier converts the photocurrent from the detector to an analog voltage. This voltage is then amplified by the voltage amplifier to match the input requirements of the decision circuit. The decision circuit provides a digital voltage output to the following computational logic circuits [5].

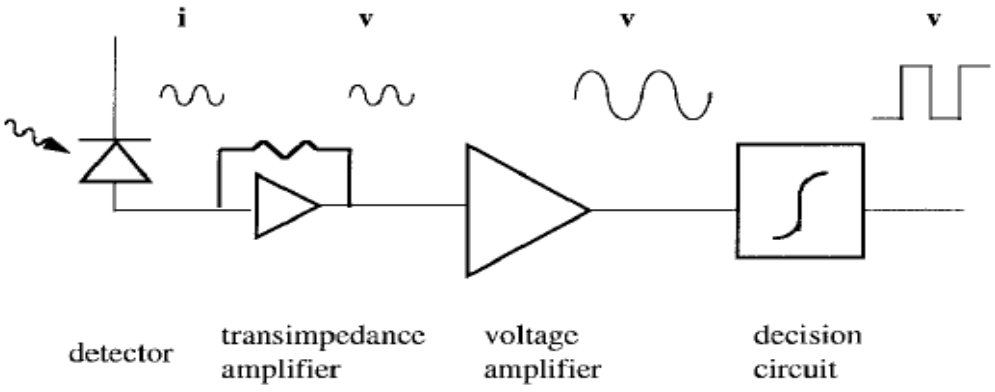

Figure 4.7 Block diagram of a receiver circuit [5].

4.9.1. Photodetectors

There are many different types of photo detectors such as the photodiodes with a p-n or a p-i-n structure, M-S-M photo detectors, avalanche photo detectors and photo multipliers. The M-S-M photo detector has the fastest response and good quantum efficiency. The response time of the M-S-M photo detector is dependent on the carrier transit time and the RC charging time of the detector capacitance. Thus the response time is given as [69]:

$$T_r = (\tau_{tr}^2 + \tau_{RC}^2)^{\frac{1}{2}} \quad (4.10),$$

$$\tau_{tr} = \frac{x}{v} \quad (4.11),$$

$$\tau_{RC} = 2.2RC \quad (4.12),$$

where *v* is the carrier drift velocity and x is the drift distance covered by the carriers. τ_{tr} is the time needed for the photo generated carriers to drift to the electrical contact, and τ_{RC} is the RC response time of the detector. The delay of the M-S-M photo detector can be expressed as [69]

$$T_D = 0.315T_r \quad (4.13),$$

The limiting factor in the delay of photo detectors is in the carrier transit time [70]. The response time of the photo detector decreases as the electrode is made smaller in area. However, there is an optimum area at which the response time of the detector is minimum [69].

4.9.2. Transimpedence Amplifier

The cascode and common source amplifier have same gain, but the cascode will have a lower input capacitance. The downside of the cascode configuration is that it requires a higher supply voltage to maintain the same gain as the common source topology, and there will be a small noise contribution from the common gate transistor.

For the reasons described above, a cascode gain stage was chosen for the TIA. The schematic for the input transimpedance stage of the amplifier is shown in Figure 4.8. A source follower was added to isolate the load resistance RD from the feedback resistor RFB as well as the capacitance of the next stage. The TIA has been designed to be pseudo differential. The TIA is not truly differential because the photodiode is single ended and is only connected to one side of the differential structure. The purpose of using a pseudo differential structure is to improve the common mode rejection of the device. The intended application of this TIA is to be integrated on the same substrate as other transceiver components. By making the structure differential the input referred noise current is increased by a factor of √2. However, since there is significant cross-talk expected, the increase in common mode rejection will outweigh this penalty.

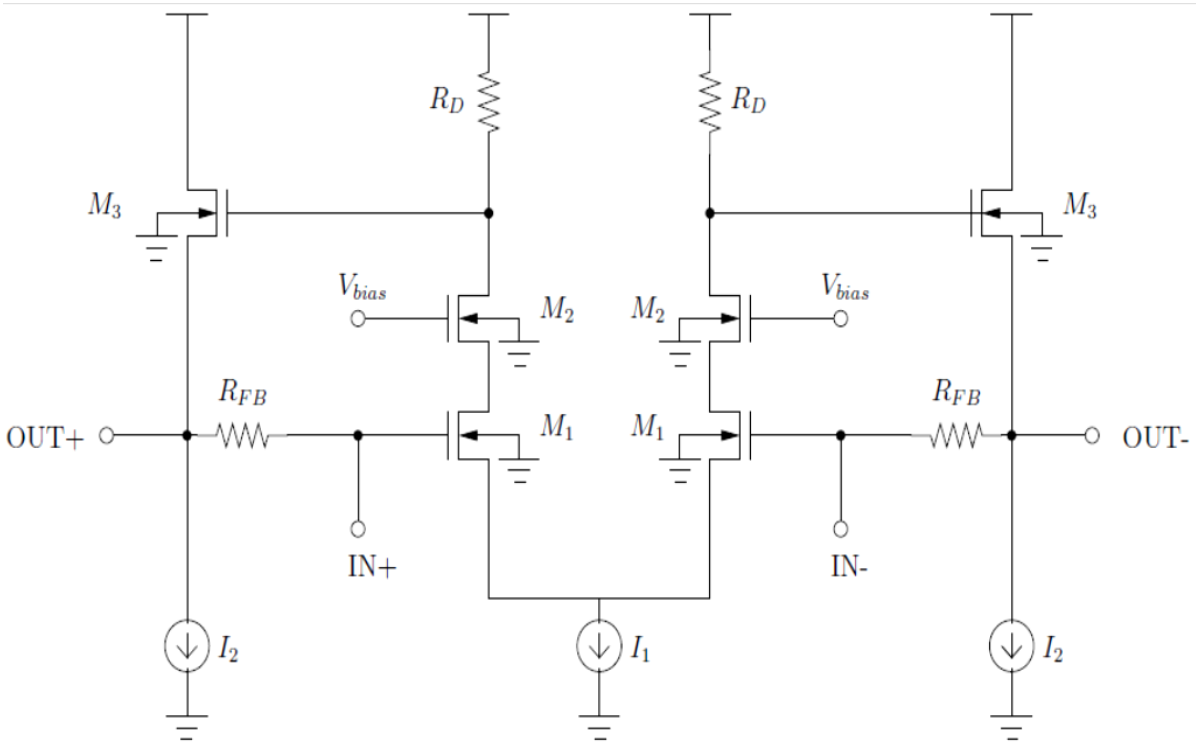

Figure 4.8 Differential Cascode TIA [76].

4.9.3. Voltage Amplifier

The important performance specifications for the amplifier are a high gain, large bandwidth, low noise, and low input capacitance. Two topologies were considered for this design, a common source configuration and a cascode configuration. These two configurations are shown in Figure 4.9. The common source transistor has a resistive load for broadband amplification. The cascode configuration also has a common source transistor at the input. The common source transistor is cascaded with a common gate transistor and a resistive load. One of the issues to consider when comparing the two topologies is the effect of the Miller capacitance. The gate to drain capacitance, known as the Miller capacitance, is connected between the input and output. The gate to drain capacitance is formed as a result of the overlap between the gate and the drain caused by lateral diffusion of the drain under the gate. For short gate length devices, this overlap capacitance is significant compared to other parasitic capacitances and is important to consider.

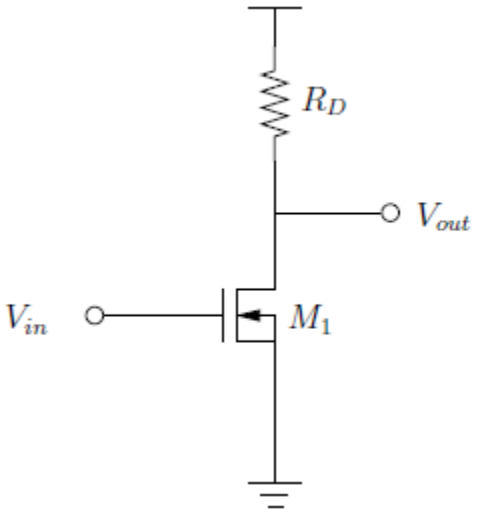

Figure 4.9(a) Common Source Amplifier [76].

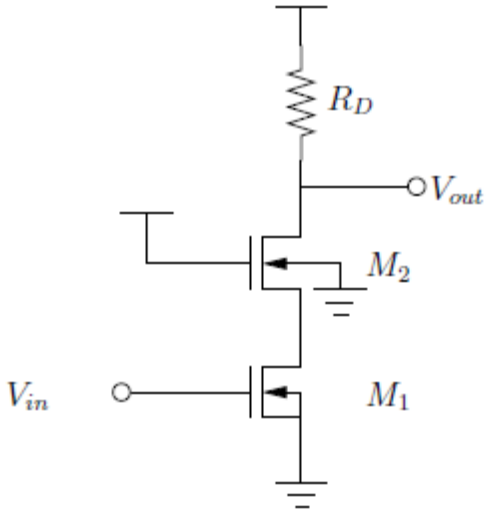

Figure 4.9(b) Cascode Amplifier [76].

4.9.4. Decision Circuit

We use a simple but effective CMOS two-stage op-amp configuration to implement the adder. The structure of this op-amp is shown in Figure 4.8. This structure is appropriate for use in high-speed optical signal receivers due to their low noise, stability, and high bandwidth. In this design, we use PMOS as input transistors to reduce the noise; we also adopt a nulling resistance compensation approach to satisfy the stability requirement in the closed-loop application. Furthermore, the phase margin (PM)

is made insensitive to process and environment variations by using M9, M10, and M11 transistors to implement the nulling resistor. The most important design specification of this op-amp is the gain–bandwidth product (GBW). Since the op-amp is used in the closed-loop adder and the bandwidth of present-day photodetectors is normally larger than 10 GHz, we set the GBW specifications to be larger than 10 GHz in this design. Small signal analysis provides the GBW expression shown below [11]:

$$GBW = \frac{g_{m1}}{C_c} \quad (4.14),$$

where g_{m1} is the transconductance of transistor M1 and C_C is the Miller compensation capacitance. The phase margin of this op-amp is given by

$$PM = 90° - arctan\left(\frac{g_{m1}}{g_{m3}}\frac{C_L}{C_C}\right) + arctan\left[\frac{g_{m1}}{g_{m3}}\left(\frac{(W/L)_3}{(W/L)_{11}}\frac{\sqrt{(W/L)_9}}{\sqrt{(W/L)_{10}}} - 1\right)\right] \quad (4.15),$$

where g_{m3} is the transconductance of transistor M3, C_L is the load capacitance, and $(W/L)_i$ is the size ratio of transistor M_i.

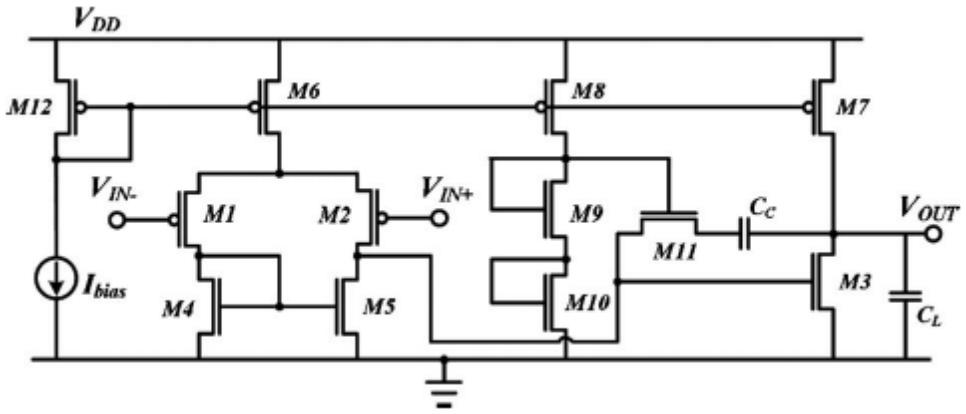

Figure 4.10 Structure of the CMOS two-stage op-amp with nulling resistance compensation [11].

4.10. Conclusion

The optical interconnects are replacing the copper interconnects at the global level as the technology is scaling down. Optical interconnection refers to the data transmission in which data signals are transmitted as a modulation of light through an optically transparent media such as optical fibre, waveguide or air. Optical interconnects are free from any capacitive loading effects. They do not suffer from crosstalk. The spatial-bandwidth for the optical interconnects is higher than their electrical interconnect using Wave Division Multiplexing (WDM). Several architectures have been projected for on-chip optically connected multi-processor systems. A transmitter consists of an electro-optical modulator and a driver circuit. CMOS circuits are examined for driving both

MQW modulators and VCSEL's. The VCSEL's as transmitters is advantageous in terms of simplifying the system optics because the required optical energy can be generated on-chip rather than using an external laser source. On the other hand, multiple quantum well (MQW) modulators have an advantage over active light emitters in terms of signal and clock distribution. Various transmitter and receiver components are tested and the optimum components are implemented in the circuit for carrying out the SPICE simulations to calculate the delay and power dissipation of the optical interconnect.

CHAPTER 5

RESULTS AND DISCUSSION

5.1. R, L AND C PARAMETERS OF COPPER INTERCONNECTS

R, L and C parameters are used to represent interconnect load. R, L and C parameters are determined from the physical geometries of interconnects. For a given process technology and a given layer, the interconnect thickness T, the height of the metal layer from the substrate H, the width W and spacing between the signal and ground line S are the commonly used variables in the optimization of global interconnect. The interconnect width and spacing are optimized under two scenarios, 1) spacing kept at its minimum value and 2) spacing kept the same as line width, for various International Technology Roadmap for Semiconductors (ITRS) technology nodes. Width and space are kept same. Various parameters w, s, t, h and dielectric constant k are shown below in table 5.1 for various technology nodes.

Table 5.1: **Technology and equivalent circuit model parameters for top layer metal for different technology node Based on the ITRS**

Technology Nodes	Width (μm)	Space (μm)	Dielectri Constant(k)	Thickness (μm)	Height (μm)	Length (μm)
90nm	0.50	0.50	2.8	1.20	0.30	10000
65nm	0.45	0.45	2.2	1.20	0.20	10000
32nm	0.048	0.048	2.25	0.144	0.1104	10000
22nm	0.032	0.032	2.05	0.096	0.0768	10000

R, L and C parameters using Shyh- Chyi Wong's TSM model are calculated using the values given in Table 5.1. Parameters are calculated for different technology nodes for different numbers of repeaters as shown in tables below. Values of R, L and C parameters are calculated for technology nodes 90nm, 65nm, 32nm and 22nm.

Table 5.2: R, L and C parameters for different technology node at 10mm

Technology Nodes	R(ohm)	L(nH)	C(fF)	C_{ground}(fF)
90nm	366.666	19.745	2596.72	829.32
65nm	407.407	19.805	2284.75	820.31
32nm	31828.703	24.107	2178.31	202.27
22nm	71614.583	24.918	1983.25	176.61

5.2 Delay

Delay of the optical and copper interconnects increases as the frequency decreases. The delay of driving the modulator can be minimized by using an exponentially sized buffer chain. For reasonable aspect ratios, this delay is close to the 0-D delay formula. There exists a possibility of delay reduction at small widths (large aspect ratio). However, this comes at the price of loss in optical energy. The delay per unit length of global Cu wires with optimized repeaters, is shown. The delay-optimized repeaters approximately double the capacitance of the wire, hence the power dissipation. Delay uncertainty is caused by geometric process variations and environmental changes. Variations in the environment include power/ground noise, temperature fluctuations, and crosstalk coupling. Delay due to environmental changes is not considered here. The delay uncertainty of the optical interconnect is expected to be lower in future technology nodes. The delay uncertainty of the conventional copper interconnect, in contrast, is expected to slowly increase in future technology nodes due to the larger number of inserted repeaters. The optimal number and size of repeaters along an RLC interconnect can be determined to achieve the minimum delay. Delay of the waveguide is taken as the propagation delay of the signal through it which is same for all technology nodes. The delay of each individual part of the transmitter and receiver of optical interconnects is simulated using SPICE simulation. Delay of copper and optical interconnects is simulated at different technology nodes for different frequencies.

Delay of optical and copper interconnects is shown at 25 MHz frequency in table 5.3.

Table 5.3: Delay (ps) in a 1 cm optical data path as compared with the copper interconnects delay at 100 MHz

Technology Node	90 nm	65 nm	32 nm	22 nm
Transmitter	304.89	273.42	218.43	202.16
Receiver	398.06	369.53	297.61	273.68
Waveguide	49	49	49	49
Total optical	751.95	691.95	565.04	524.84
Copper	1770	1560	1256	1413

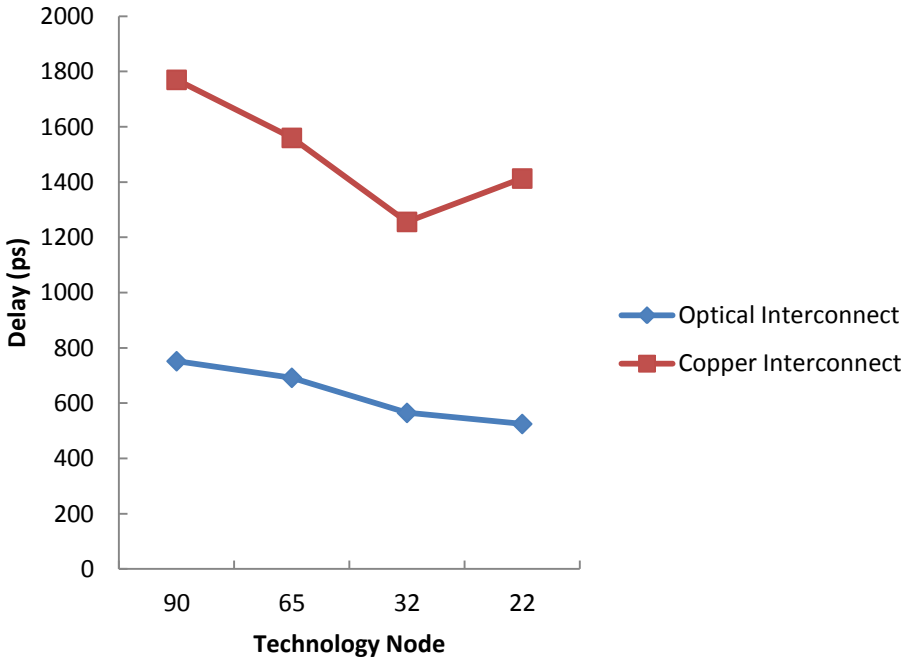

Figure 5.1 Comparison between Optical interconnects and Copper interconnects in terms of delay

Performance of optical interconnects and copper interconnects with respect to delay for different technology nodes at 50 MHz is shown in table 5.4.

Table 5.4: Delay (ps) in a 1 cm optical data path as compared with the copper interconnects delay at 50 MHz

Technology Node	90 nm	65 nm	32 nm	22 nm
Transmitter	342.74	319.29	238.15	225.62
Receiver	478.92	446.15	331.28	311.96
Waveguide	49	49	49	49
Total optical	870.66	814.44	618.43	586.58
Copper	1790	1640	1273	1190

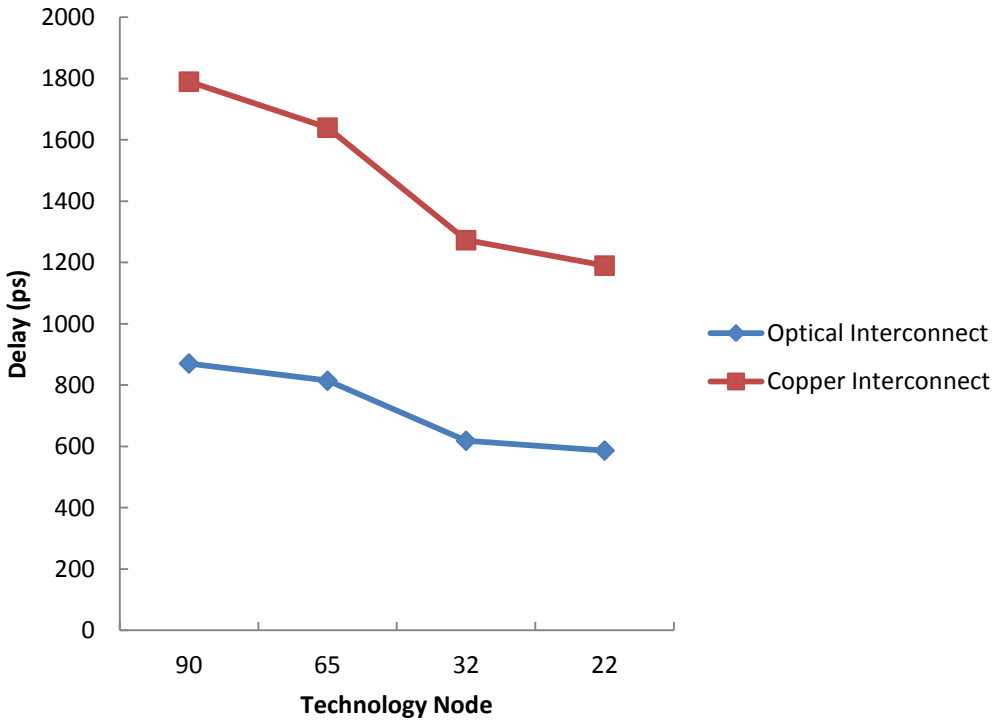

Figure 5.2 Comparison between Optical interconnects and Copper interconnects in terms of delay

Performance of optical interconnects and copper interconnects with respect to delay for different technology nodes at 25 MHz is shown in table 5.5.

Table 5.5: Delay (ps) in a 1 cm optical data path as compared with the copper interconnects delay at 25 MHz

Technology Node	90 nm	65 nm	32 nm	22 nm
Transmitter	363.39	339.04	281.08	259.26
Receiver	461.74	428.01	354.84	326.37
Waveguide	49	49	49	49
Total optical	874.13	816.05	684.92	634.63
Copper	1813	1680	882.93	864.3

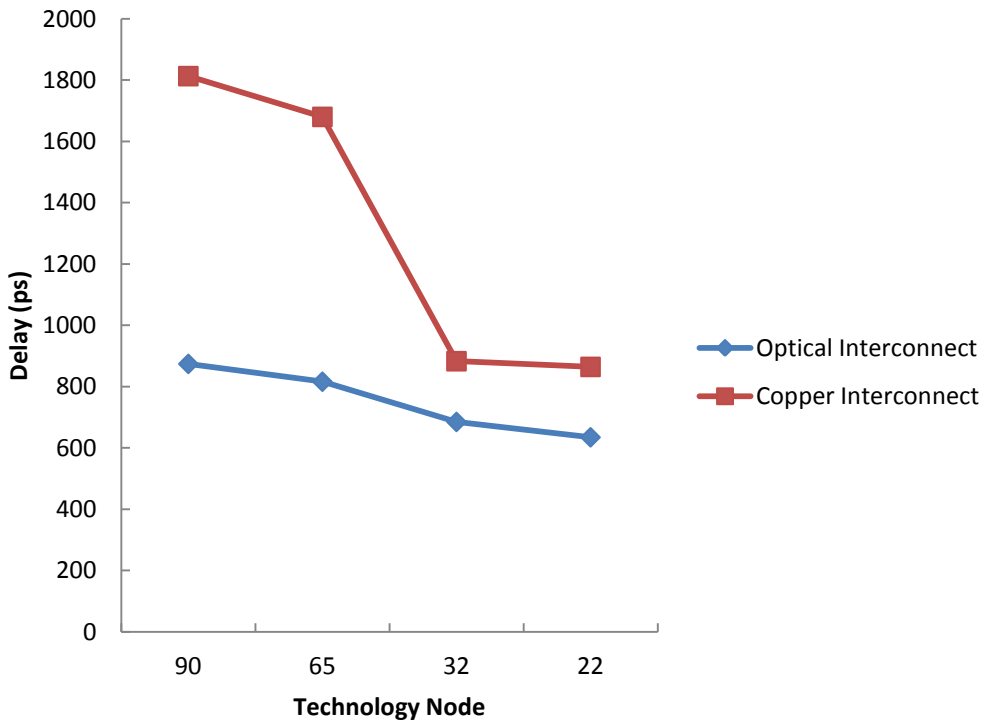

Figure 5.3 Comparison between Optical interconnects and Copper interconnects in terms of delay

The delay increases as the frequency decrease. Optimum results are obtained at 100MHz. Results show that optical interconnects give better results as compared to copper interconnects in terms of delay . Delay of optical interconnects and copper interconnects decreases with future technology nodes.

5.3 Power Dissipation

For electrical interconnects, the power should be evaluated under specific design requirements, such as delay and bandwidth. A minimum sized wire without repeaters consumes minimum power, however, this configuration is not practical for global interconnect due to the significant delay and low bandwidth of the line. The power dissipation due to these repeated wires is dictated by both the wire and the repeater capacitances. Due to small length optical power loss in the waveguide is negligible. Hence, only electrical power is evaluated for the optical interconnects. The power consumed by the transmitter dominates the power of the receiver. The two components of transmitter power: the dynamic power of the buffer chain and the static power in the absorbing state of the modulator can both be shown to be a very small fraction of the receiver power at low IOPs (high receiver sensitivity).The receiver power is dominated by static power dissipation. It is directly proportional to the transistor size, which is dictated by the speed and the signal reliability constraints (BER), and on number of gain stages, which is deduced from power supply voltage swing requirement. Both the electrical and optical interconnect power increases with future technology nodes due to higher clock frequencies and greater leakage current. Simulation is done for the power dissipation for both type of interconnects at various technology nodes for different frequencies. Power dissipation for both optical and electrical interconnects at 100 MHz is shown in table 5.6.

Table 5.6: Power dissipation (mw) in 1cm optical data path as compared with copper interconnects at 100 MHz

Technology Node	90 nm	65 nm	32 nm	22 nm
Transmitter	0.102	0.106	0.113	0.166
Receiver	0.114	0.421	0.731	1.44
Total optical	0.216	0.527	0.844	1.606
Copper	0.065	0.087	0.176	0.254

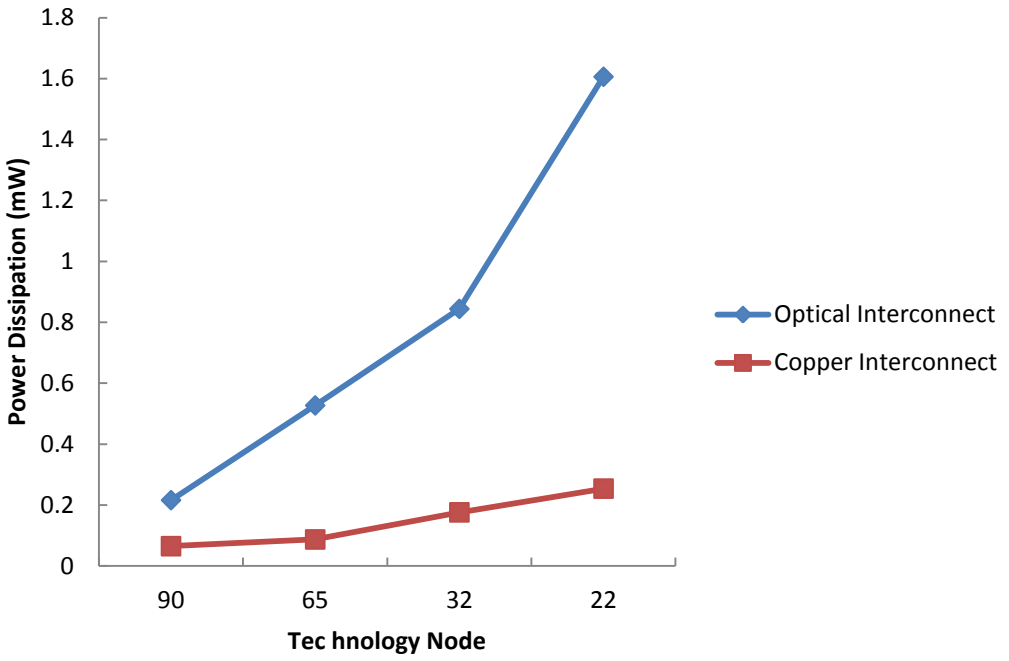

Figure 5.4 Comparison between Optical interconnects and Copper interconnects in terms of power dissipation

Performance of optical interconnects and copper interconnects with respect to power dissipation for different technology nodes at 50MHz is shown in table 5.7.

Table 5.7: Power dissipation (mw) in 1cm optical data path as compared with copper interconnects at 50 MHz

Technology Node	90 nm	65 nm	32 nm	22 nm
Transmitter	0.098	0.103	0.106	0.16
Receiver	0.144	0.457	0.723	1.42
Total optical	0.242	0.56	0.829	1.58
Copper	0.044	0.065	0.09	0.10

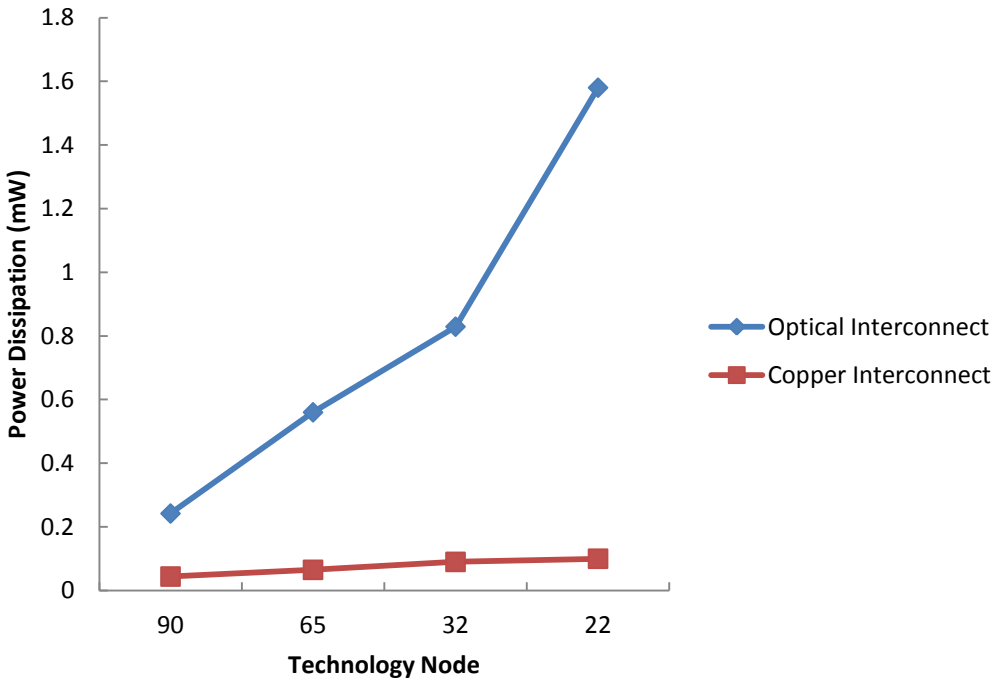

Figure 5.5 Comparison between Optical interconnects and Copper interconnects in terms of power dissipation

Performance of optical interconnects and copper interconnects with respect to power dissipation for different technology nodes at 25 MHz is shown in table 5.8.

Table 5.8: Power dissipation (mw) in 1cm optical data path as compared with copper interconnects at 25 MHz

Technology Node	90 nm	65 nm	32 nm	22 nm
Transmitter	0.097	0.1	0.102	.161
Receiver	0.142	0.445	0.719	1.43
Total optical	0.239	0.545	0.821	1.591
Copper	0.043	0.063	0.08	0.11

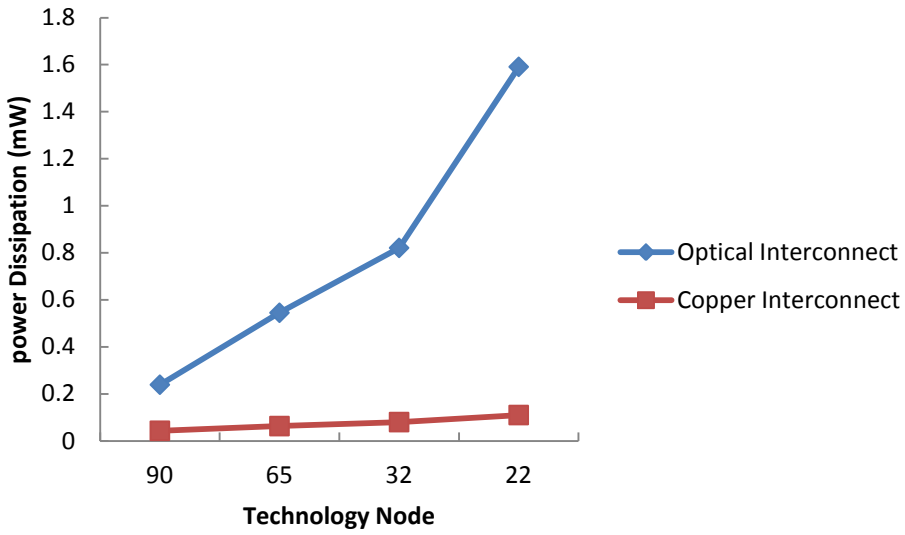

Figure 5.6 Comparison between Optical interconnects and Copper interconnects in terms of power dissipation

Power dissipation of both type of interconnects increases with future technology nodes because of higher clock frequency and leakage current. Power dissipation of optical and copper interconnects decreases as the frequency decreases. The power dissipation in optical interconnects is more than copper interconnect at lower frequency levels but as we keep on increasing the frequency levels, the power dissipation in the optical interconnects keeps on decreasing as compared to copper interconnects resulting more efficient operation in terms of power also.

CHAPTER 6

CONCLUSION AND FUTURE SCOPE

6.1. Conclusion

In this dissertation, comparisons between Cu and optical interconnects for off-chip communications have been analyzed. For off-chip applications, we compared high speed optical and electrical interconnects using relevant metrics, such as power and delay. It has been seen that beyond a critical length, power optimized optical interconnects show low delay compared to high-speed electrical signaling schemes. Beyond the 32nm technology node, with its commensurate bandwidth requirement, optical interconnects becomes favourable for distances as little as 10cm. These distances correspond to inter-chip communication on a board. In addition, we examined two competing optical transmitter technologies for off-chip link: the vertical cavity surface emitting laser (VCSEL) and the quantum well modulator (QWM), for optical links. VCSEL-based links are power favourable compared to QWM-based links at higher bandwidth (>20Gb/s) and larger distance. However, from the practical standpoint, it is instructive to note that currently VCSELs are difficult to drive beyond 15-20 Gbps and are likely to suffer from reliability problems in harsh CMOS chip environment with elevated temperatures. The QWM is better for lower detector and modulator capacitances. Furthermore, we quantify the design constraints on the modulator under which it is superior to VCSEL technology as a function of bandwidth, link length, and transmitter and detector capacitances. We found that QWM are more power-efficient compared to VCSELs, as lower capacitances for both the modulator and the photo-detector would be required.

Finally, we examined the impact of technology node scaling on the modulator design optimization. We observed that the modulator design metrics are relatively insensitive to the transistor performance and the power dissipation has two opposite trends depending on the bit rate and the device capacitances. Lower bit rate and smaller device capacitances decrease the power dissipation with technology scaling while, the power dissipation increases at higher bit rates and larger capacitances.

For performance comparison, delay and power dissipation are simulated for both type of interconnects at various technology nodes. SPICE simulation tool is used for delay and power dissipation simulation. Delay and Power dissipation are simulated at 90nm, 65nm, 32nm and 22nm technology nodes. For minimization of delay in copper

interconnects repeaters are inserted. Comparing the delay between the optical and copper interconnect for varying frequencies and fixed interconnect length 1cm (at global interconnect level) shows that optical interconnects give better performance than copper interconnects. Delay of optical interconnects decreases with future technology nodes whereas delay of conventional copper interconnects increases. Delay of both type of interconnects increases as the frequency decreases. The power dissipation in optical interconnects is more than copper interconnect at lower frequency levels but as we keep on increasing the frequency levels, the power dissipation in the optical interconnects keeps on decreasing as compared to copper interconnects resulting more efficient operation in terms of power also.

6.2. Future Scope

This work can continue in many different directions. Noise immunity, crosstalk and variation effects must be considered in designing the circuitry. New novel device and advanced circuit technologies enhance the performance while reducing power. The system's impact of these devices should be investigated. For off-chip electrical links, a comparison between uni-directional signaling and bi-directional signaling would be useful. On the other hand, optical links have various novel options whose performances need to be evaluated in system's context. The innovations include non-TIA (transimpedance amplifier) based receiver designs including integrating current and sampling receivers, as well as novel device structures, such as monolithically integrated modulator, metal semiconductor metal (MSM) photo-detectors, and optoelectronic switch which has a built- in gain. These solutions will inevitably speed the insertion of optical interconnect for shorter distance applications. Very little work has been done at 14nm technology. As a future recommendation, a cavity tuning method with the specifically handled processing would be very useful for improving the performance of end-device (modulator/detector) for optical links.

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