Design of Low Power and High Fault Coverage Test Pattern Generator for BIST

Thesis Report submitted towards the partial fulfilment of the requirements
for the award of the degree of

Master of Technology (VLSI design & CAD)

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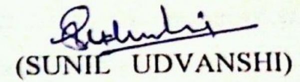
July 2011

DECLARATION

I hereby declare that the Thesis report entitled "**Design of Low Power And High Fault Coverage Test Pattern Generator For BIST (Built-In Self Test)**, is an authentic record of my own work carried out as the requirements for the award of degree of Master of Technology in VLSI Design & CAD at Thapar University, Patiala under the guidance of **Ms. Harpreet Vohra** (Assistant Professor), Department of Electronics and Communication Engineering, during July'10 to June'11.



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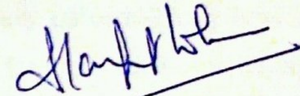

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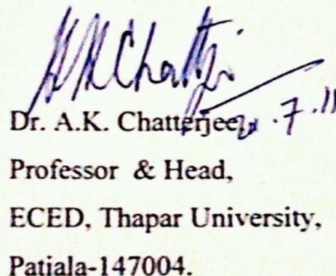

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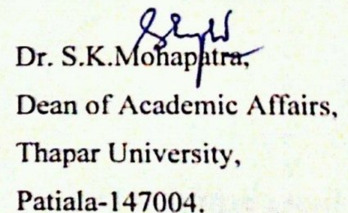

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SUNIL UDVANSHI

ABSTRACT

Low Power consumption has become increasingly important in hand-held communication systems and battery operated equipment, such as laptop computers, audio and video-based multimedia products, and cellular phones. For this new class of battery-powered devices, the energy consumption is a critical design issue since it determines the lifetime of the batteries. Thereby, the reduction of the energy consumption is becoming one of the most growing topics of interest in the electronics industry and one of the most challenging areas of research in this domain.

In the same time, modern design and package technologies make external testing more and more difficult, and built-in self test (BIST) has emerged as a promising solution to the VLSI testing problem. BIST is a design for testability methodology aimed at detecting faulty components in a system by incorporating test logic on-chip. BIST is well known for its numerous advantages such as improved testability, at-speed test of modules, no need for automatic test equipment, and support during system maintenance. Moreover, with the emergence of core-based "system-on-a-chip" designs, BIST represents one of the most favourable testing methods since it allows preserving the intellectual property of the design.

A new low power test pattern generator using a linear feedback shift register (LFSR), called LP-TPG, is presented to reduce the average and peak power of a circuit during test. The correlation between the test patterns generated by LP-TPG is more than conventional LFSR. LP-TPG inserts intermediate patterns between the random patterns. The goal of having intermediate patterns is to reduce the transitional activities of primary inputs which eventually reduces the switching activities inside the circuit under test, and hence, power consumption. The random nature of the test patterns is kept intact. The area overhead of the additional components to the LFSR is negligible compared to the large circuit sizes. The experimental results are shown for ISCAS85 benchmarks, confirming up to 63% and 27% reduction in average and peak power, respectively.

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ABBREVIATIONS

BIST	Built in self test
BILBO	Built in logic block observer (register)
LFSR	Linear feedback shift register
MISR	Multiple input signature register
ORA	Output response analyser (Generic)
PRPG	Pseudo random pattern generator
SISR	Single input signature register
SRSG	Shift register sequence generator also a single output PRPG
TGP	Test pattern generator (Generic)
DFT	Design-for-testability
SRPG	Shift register pattern generator
WSA	Weighted switching activity
SA	Switching activity
SOC	System on chip
ATPG	Automatic test pattern generation
CUT	Circuit under test
PIs	Primary inputs
POs	Primary outputs

CHAPTER 1 Introduction

1.1 Motivation for Low power testing

Power dissipation has become a major design objective in many application areas, such as wireless communications and high performance computing, thus leading to the production of numerous low-power designs. At the same time, power dissipation is also becoming a critical parameter during manufacturing test, as the design can consume much more power during test than during functional mode of operation. As test throughput and manufacturing yield are often affected by test power, dedicated test methodologies have emerged over the past decade.

In this chapter, we discuss issues arising from excessive power consumption during test application as well as provide structural and algorithmic solutions that can be used to alleviate the low-power test problems. We first review some basic elements of power modelling and related terminologies. After discussing test power issues, promising low-power test techniques to deal with nanometre system-on-chip (SOC) designs are presented. These techniques can be broadly classified into those that apply during scan testing and those that apply during built-in self-test (BIST). A few of them are also applicable to test compression circuits or memory designs.

In the literature, techniques that reduce power consumption during test application are generally referred to as power-conscious testing, power-aware testing, power-constrained testing, or low-power testing. These terms will be interchanged for use throughout the chapter whenever fit with the advance in semiconductor manufacturing technology, a very-large-scale integration (VLSI) device can now contain tens to hundreds of millions of transistors. Test currently ranks among the

most important issues in the development process of an integrated circuit. The issues that centre on test are manufacturing yield, product quality, and test cost. To address these test issues, design-for-testability (DFT) techniques have become widely used in industry since the 1990s. Traditionally, these techniques are mainly employed to improve the circuit's fault coverage, test application time, and test development efforts. The recent advances in low-power design techniques and deep-submicron manufacturing technologies, however, have spurred the rapid growth of electronic products into consumer markets using laptop computers, cellular phones, audio and video-based multimedia products, energy-efficient desktop computers, etc. These new products make power management a critical issue that needs to be considered not only during circuit design but also during test development. The main motivation for considering power consumption during test is that generally, a circuit consumes much more power in test mode than in normal mode [3].

It was shown that test power can be more than twice the power consumed in normal functional mode. There are several reasons that could explain this increase in test power. 1st, modern automatic test pattern generation (ATPG) tools tend to generate test patterns with a high toggle rate in order to reduce pattern count and thus test application time. Thus, the node switching activity of the device in test mode is often several times higher than that in normal mode. 2nd, parallel testing (e.g., testing a few memories in parallel) is often used to reduce test application time, particularly for system-on-chip (SOC) devices. This parallelism inevitably increases power dissipation during test. 3rd, the DFT circuitry inserted in the circuit to alleviate test issues is often idle during normal operation but may be intensively used in test mode. This surplus of active elements during test again induces an increase of power dissipation.

Finally, this elevated test power can come from the lack of correlation between consecutive test patterns, while the correlation between successive functional input vectors applied to a given circuit during normal operation is generally very high.

For instance, in a speech signal processing circuit, the input vectors behave in a predictable manner, with the least significant bits more likely to change than the most significant bits. Similarly, in high-speed circuits that process digital audio and video signals, the inputs to most of those modules change relatively slowly over time. The low power designers often take advantage of this fact when they determine the thermal and electrical limits of the circuit and system packaging requirements. In contrast, there is no definite correlation between successive test patterns generated by an ATPG

tool during scan testing or produced by a pseudorandom pattern-generator (PRPG) during logic BIST. As power dissipation in CMOS circuits is Proportional to switching activity, this excessive switching activity during test can cause catastrophic problems, such as instant circuit damage, test-induced yield loss due to noise phenomena, reduced reliability, product cost increase, or reduced autonomy for battery-operated devices.

In order to reduce this increased power consumption during test application, the industry generally resorts to ad hoc solutions. These solutions include:

♦ Over-sizing power and ground rails to allow higher current densities in the circuit under test. This allows additional power to be supplied to the circuit to satisfy the increase in switching activity that occurs during test. However, this solution raises several problems. By increasing the power available for the circuit, the amount of energy (heat) that needs to be dissipated is also increased, which in turn leads to additional problems related to the thermal constraints of the circuit. It is possible to avoid these problems by using packages with higher thermal capabilities or by using higher performance cooling systems. However, the impact on the final product cost may prevent the use of these solutions. Another problem is that this solution affects the entire design and may require an early estimation of the power consumption during test. As test data is generally not available in the early stages of the design process, this solution may not be satisfactory in all cases.

♦ Testing with a reduced operating frequency. This solution does not require additional hardware, but it increases the test application time and may lead to a loss of defect coverage as timing-related faults may escape detection. In effect, this solution reduces power consumption at the expense of longer test time, and does not reduce the total energy consumed during test.

♦ Partitioning of the circuit under test with appropriate test planning. This solution, although effective from a power reduction point of view, increases test time because it reduces test concurrency. Moreover, it generally requires circuit design modifications, thus impacting final product cost and circuit performance. Considering the problems associated with these *ad hoc* approaches and the need to provide an adequate remedy to the problems, numerous solutions have been proposed in recent years to cope with test power problems during test. These solutions can be classified based on whether they apply during scan testing or whether they apply during logic

BIST. A few of them can also be used with memory designs or can be used in conjunction with test compression.

1.2 Project objectives

Test Pattern generation has long been carried out by using conventional Linear Feedback Shift Registers (LFSR's). LFSR's are a series of flip-flop's connected in series with feedback taps defined by the generator polynomial. The seed value is loaded into the outputs of the flip-flops. The only input required to generate a random sequence is an external clock where each clock pulse can produce a unique pattern at the output of the flip-flops.

This random sequence at the output of the flip-flops can be used as a test pattern. The number of inputs required by the circuit under test must match with the number of flip-flop outputs of the LFSR. This test pattern is run on the circuit under test for desired fault coverage.

The power consumed by the chip under test is a measure of the switching activity of the logic inside the chip which depends largely on the randomness of the applied input stimulus. Reduced correlation between the successive vectors of the applied stimulus into the circuit under test can result in much higher power consumption by the device than the budgeted power. A new low power pattern generation technique need is to be implemented using a modified conventional Linear Feedback Shift Register.

Conventional as well as low power test patterns generators are run on ISCAS 85 benchmark circuits. The power consumption of the circuit is measured using industry standard Xilinx tool called X-Power and it is demonstrated that the new low power approach results in significant reduction in power consumption of the circuit under test compared with that of using the conventional pattern for the same fault coverage.

1.3 Thesis outline

Chapter 2 gives the introduction of BIST. The concept of BIST architecture and its components is explained along with the explanation of LFSR, a circuit very commonly used to generate random test patterns. The correlation of the LFSR, its characteristic polynomial and matrix theory is described.

Chapter 3 gives a description of a pattern generated using a conventional LFSR. It explains in detail the idea behind the low power pattern generation in particular the low power technique designed using two levels of logic between the outputs of the LFSR and the actual outputs coming out of the second level of logic. Standard tools such as Verilog HDL, Xilinx, and Mentor's Modelsim are used for design description, synthesis, simulation and power consumption estimation. A brief background of the commonly used industry standard benchmark circuits is also provided.

Chapter 4 includes the methodology used to determine the power consumption by the c432 benchmark circuit using the conventional pattern. It explains the methodology used for computing power consumption by the ISCAS-85 benchmark circuit c432 (27-channel interrupt controller) using the low power pattern. A comparison of the circuit power consumption is discussed between the two techniques.

Chapter 5 finally concludes and some recommendations on future work as given the report.

CHAPTER

2 Literature Survey on BIST

Introduction

Built-in self test is a design technique in which parts of a circuit are used to test the circuit itself. Built in self test is the capability of the circuit (chip board or system) to test itself. BIST represents a merger of concept of built in test and self test and hence come to be synonymous with these terms.

BIST technique can be classified into two categories, namely online BIST which includes concurrent and non concurrent techniques, and offline BIST which includes functional and structural approaches.

In ONLINE BIST [1], testing occurs during normal function operating condition; i.e. the circuit under test (CUT) is not placed into a test mode where normal functional operation is locked out. Concurrent-on-line BIST is a form of testing that occurs simultaneously with normal function operation. This form of testing is usually accomplished using coding techniques or duplication and comparison. In non-concurrent on-line BIST, testing is carried out while a system is in an idle state. This is often accomplished by executing diagnostic software routine or diagnostic firm where routines. The test process can be interrupted any time so that normal operation can be resuming.

OFFLINE BIST[1] deals with testing a system when it is not carrying out its normal functions. Systems, boots and chips can be tested in this mode. This form of testing is also applicable at the manufacturing field, depot and operational levels. Often off-line testing is carried out using on chip or on board test pattern generator (TPGS) and output response analyser (ORAS) or micro diagnostic routine. Offline testing does

not detect errors in real time that is when they first occur, as it possible with many online concurrent BIST techniques.

Functional offline BIST deals with execution of a test based on a functional description of CUT and often employs a functional or high level, fault level. Normally such a tests is implemented as diagnostic software or firmware.

Structural offline BIST deals with the execution of a test base on the structure of the CUT. An explicit structural fault model may be use fault coverage is based on detecting structure faults. Usually tests are generated and responses are compresses using some form of an LFSR.

Two common TPG circuit exists. A pseudo random pattern generator(PRPG) is a multi output device normally implemented using an LFSR , while a shift register pattern generator(SRPG) is a single output autonomous LFSR for simplicity the reader can consider a PRPG to represent a parallel random pattern generator , and a SRPG to be a serial random pattern generator. Two common ORA circuits also exist. One is multiple input signature register (MISR) the other is single input signature register (SISR).both are implemented an LFSR [1].

2.1 BIST Implementations

Figure 2.1(a) shows typical BIST hardware in more detail. Note that the wires from PIs to the Input MUX and the wires from circuit outputs P to primary outputs (POs) cannot be tested by BIST. These wires, instead, require another testing method, such as an external ATE or JTAG Boundary Scan hardware. Figure 2.1(a) also shows how a comparator compares the signature produced by the data compacter with a reference signature stored in a ROM during BIST. The comparator and ROM hardware can frequently be implemented with a single logic gate with 32 or fewer inputs. This is acceptable only when the comparison can occur at extremely low rates of circuit operation, since this logic gate is exceedingly slow.

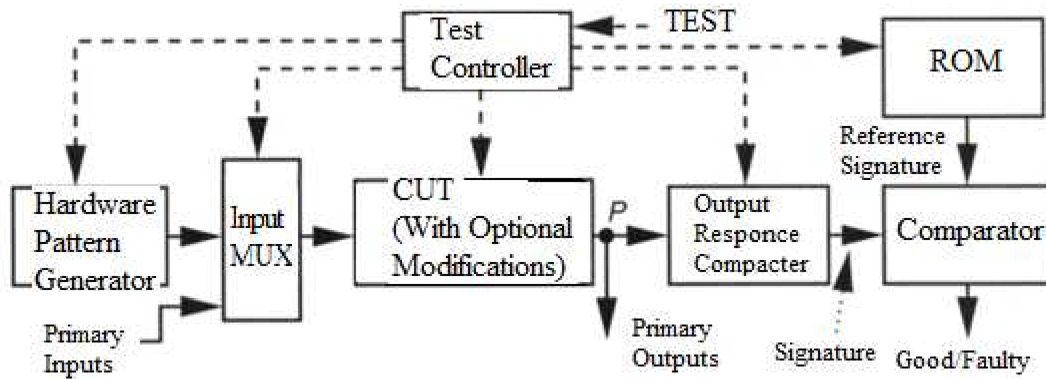

Figure 2.1(a): BIST process .

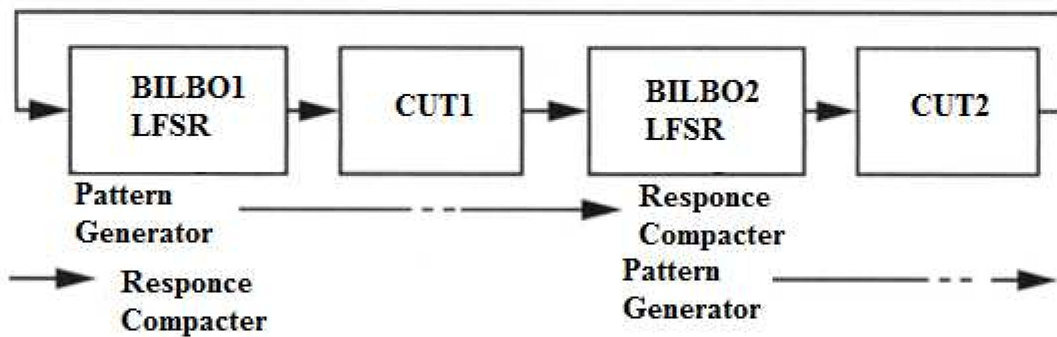

Figure 2.1(b): Multi-purpose registers in a BIST implementation .

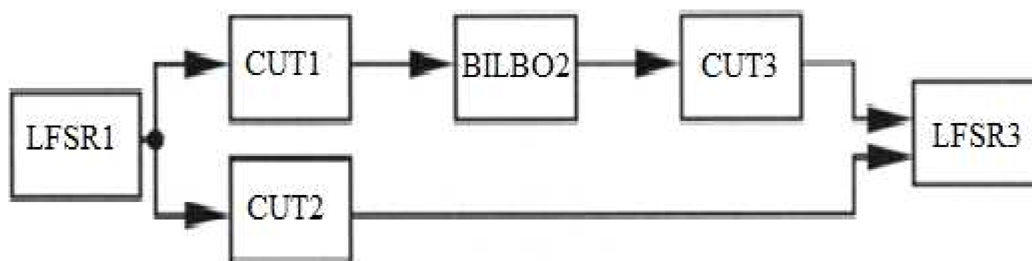

Figure 2.1(c): Complex BIST implementation .

Figure 2.1(b) shows a BIST implementation using built-in logic block observers (BILBOs). A BILBO is a bank of D flip-flops in the CUT that has test hardware added to make it behave in one of four modes:

• As ordinary D flip-flops.

• As a linear feedback shift register (LFSR) hardware pattern generator.

• As an LFSR configured to compact a circuit response.

• As a scan chain.

BILBO1 is configured as an LFSR pattern generator to test CUT1 in the circuit, while BILBO2 is configured as a response compacter to compact the responses of CUT1. During this process, the behaviour of CUT2 is ignored. BILBO2 is configured as an LFSR pattern generator to test CUT2 in the circuit, while BILBO1 is configured as a response compacter to compact the responses of CUT2. During this second process, the behaviour of CUT1 is ignored. For the normal system function, both BILBO1 and BILBO2 are configured to behave as simple D flip-flops.

Figure 2.1(c) shows a more complicated BIST system. Here, LFSR1 is used to simultaneously generate patterns to test CUT1 and CUT2. BILBO2 is configured as a response compacter for CUT1, while LFSR3 is configured as a response compacter for CUT2. In this mode, inputs to CUT3 must be held steady so that the outputs of CUT3 remain stable. In the second test mode, BILBO2 is configured as a pattern generator for CUT3, while LFSR3 is configured as a response compacter for CUT3. The outputs of CUT1 are ignored, and LFSR1 must be set so that the outputs of CUT2 are held steady during this second mode. Finally, Figure 2.1(d) shows a bus-oriented BIST implementation. The self-test control broadcasts test-patterns to each of the CUTs over their common bus. The self-test control then awaits bus transactions from each CUT that indicate the CUT's response to the stimulus pattern broadcast over the bus. This allows for a certain amount of concurrency during self-test. In this mechanism, pattern generation for all of the CUTs can happen in parallel, but response compaction is serialized over the bus. The strategy for overall test control is the most difficult part of BIST design. Care must be taken so that the BIST circuitry, as well as the circuit-under-test, can be tested for stuck-at faults. The BIST circuitry that must operate correctly for BIST to work is referred to as the hard-core. Either the hard-core must be minimized, or it must be made testable.

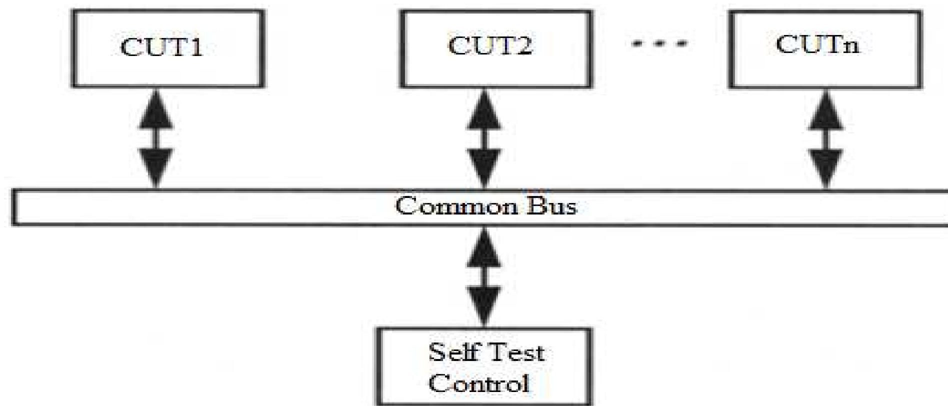

Figure 2.1(d): Bus-based BIST implementation.

2.2 Power Consumption Analysis of Digital System

With the application and development of large-scale integrated circuit and system, Built-in Self-test technology has become the main stream design for testability. It can provide higher fault coverage and relatively shorter testing time. So in recent years, more and more researches are done on BIST, the power consumption problems during BIST test attract more attention. Because more power consumption can bring a series of problems, it can reduce the finished products rate and reliability of chips, therefore influencing the performance of circuits and making them loss efficacy. Now power consumption testing technology has become the hot research subject of academic and industrial community, it presents some academic research methods to deal with power consumption problem in testing [2].

It Includes:

1. Circuit division technology. Circuit Under test is divided into several structuralized sub-circuit. Every sub-circuit can be tested by different BIST part continuously.

2. Reducing the switching activity of circuit under test. The change of CUT (circuit under test)'s input end can be decreased through designing test pattern generator carefully, thereby reducing power consumption.

3. Filtrating unused testing vector. For circuit under test, the addition of every testing vector can produce certain power consumption, but not all of testing vector makes contribution to testing fault coverage rate.

Three parameters are important for evaluating the power properties of BIST architecture:

1. The consumed energy directly corresponds to the switching activity generated in the circuit during test application, and has impact on the battery lifetime during remote testing.
2. The average power consumption is given by the ratio between the energy and the test time. This parameter is even more important than the energy as hot spots and reliability problems may be caused by constantly high power consumption.
3. The peak power consumption corresponds to the highest switching activity generated in the CUT during one clock cycle. The peak power determines the thermal and electrical limits of components and the system packaging requirements.

Power consumption of CMOS large-scale integrated circuit is affected by three main factors [15,7].

1. Static power consumption.
2. Dynamic power consumption.
3. Mains voltage;

In CMOS circuit, power consumption E_i is the function of the node's signal switching times and load capacitance, as:

$$E_i = \frac{1}{2} s_i \cdot f_i \cdot c_o \cdot v_{dd}^2 \quad (1)$$

In which S_i is the overturn times, F_i is the fan-out, c_o is the unit output load capacitance, V_{DD} is main voltage. The sum of all nodes E_i in circuit is the total power consumption E during this period of time. Because mains voltage V_{DD} and unit output load capacitance C_o are constant, dynamic power consumption E_i of node is only proportional to the ($s_i \cdot F_i$), which can be used to measure big or small of node power consumption.

The defined it as the WSA of the node, it can estimate the power consumption. For two continuous input testing vectors $TP_k(v_{k-1}, v_k)$, the WSA_k of circuit is [16]:

$$WSA_k = \sum_i s(i,k) \cdot F_i \quad (2)$$

In which i includes the number of all nodes in circuit, S (i, k) is the overturn times of node i excited by vector TP_K .

Considering the whole testing vector set TP = ($v_1, v_2 \ldots . v_n$), the total WSA of circuit is

$$\mathrm{WSA} = \sum_k \sum_i s(i,k).F_i \quad (3)$$

In this formula, k = 2, 3.......... n.

From formula (2) and (3), we can know that power consumption can be reduced by decreasing the overturn times S(i, k) of CUT's input end.

2.3 BIST Pattern Generation

The following hardware pattern generation approaches have been used [1].

1. **ROM**.- One method is to store a good test-pattern set (from an ATPG program) in a ROM on the chip, but this is prohibitively expensive in chip area, and will not be discussed further.

2. **LFSR**.- Another method is to use a linear feedback shift register (LFSR) to generate pseudo-random tests. This frequently requires a sequence of 1 million or more tests to obtain high fault coverage, but the method uses very little hardware and is currently the Preferred BIST pattern generation method.

3. **Binary Counters-**. A binary counter can generate an exhaustive test sequence, but this can use too much test time if the number of inputs is huge. For example, with 64 inputs and the test-pattern generator clocked at 100 MHz, this takes 51,240,955.8 hours of test time to generate all patterns, which is impractical. Therefore, this type of pattern generator must be partitioned. Also, the binary counter requires more hardware than the typical LFSR pattern generator.

4. **Modified Counters**. Modified counters have also been successful as test-pattern generators, but they also require long test sequences.

5. **LFSR and ROM**. One of the most effective approaches is to use an LFSR as the primary test mode, and then generate test-patterns with an ATPG program for the faults that are missed by the LFSR sequence. These few additional test-patterns can either be stored in a small ROM on the chip for a second test epoch, they can be

embedded in the output of the LFSR, or they can be embedded in a scan chain in order to augment the stuck-fault coverage to 100%.

6. **Cellular Automaton**. In this approach, each pattern generator cell has a few logic gates, a flip-flop, and connections only to neighbouring gates. The cell is replicated to produce the cellular automaton.

2.4 BIST Pattern Generation using LFSR

Linear Feedback Shift Register is a circuit consisting of flip-flops connected in series with each other. The output of one flip-flop is connected to the input of the next flip flop and so on. The feedback polynomial which is also known as the characteristic polynomial is used to determine the feedback taps which in turn determines the length of the random pattern generation [13].

An example below in Figure 2.2 is used to illustrate a correlation between the LFSR, its characteristic polynomial and matrix theory. In the circuit the feedback taps are shown to be from the output of the 4th and 1st register.

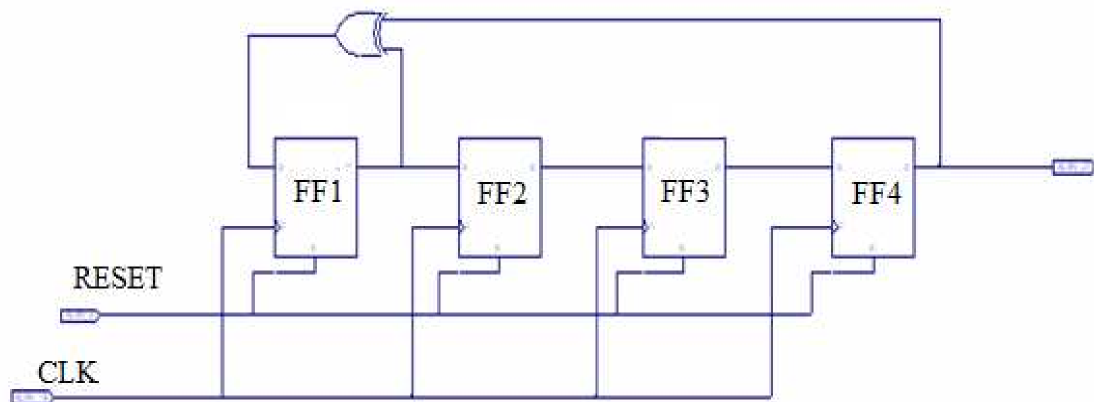

Figure 2.2 4 bit LFSR [13]

These taps are indicative of the generator polynomial. According to this polynomial the present and the next state of these registers are shown in table 2.1 (R1, R2, R3, R4 and R1=R1⊕R4, R2 = R1, R3 = R2 and R4 = R3).

Table 2.1 Present/Next State

Present State	Next State
R1	R1 ex-or R4
R2	R1
R3	R2
R4	R3

Using the matrix theory the companion matrix required for relating the present to the next state is depicted in Figure 2.3 below. The actual sequence of the LFSR is represented as BT, BT^2, BT^3 , where B is the seed vector. The determinant of the T matrix is called the characteristic polynomial and the generator polynomial is the inverse of the characteristic polynomial.

$$\begin{pmatrix} 1\ 0\ 0\ 1 \\ 1\ 0\ 0\ 0 \\ 0\ 1\ 0\ 0 \\ 0\ 0\ 1\ 0 \end{pmatrix}$$

Figure 2.3 Companion Matrix [13]

Det (T) = [xI – T] {Characteristic Polynomial} Where I is the identity matrix

Generator Polynomial = Inverse of the Characteristic Polynomial

As an example the characteristic polynomial for the above circuit is = $X^4 + X^3 + 1$ and the generator polynomial is represented as $X^4 + X + 1$.

Normally the feedback taps are selected such that entire sequence is generated including all zero's and one's. The generation of all zero's pattern requires an additional NOR gate whose inputs are the outputs of all flip- flops in the LFSR. The output of the NOR gate is fed into the input of the first flip-flop in the circuit as shown in Figure 2.4.

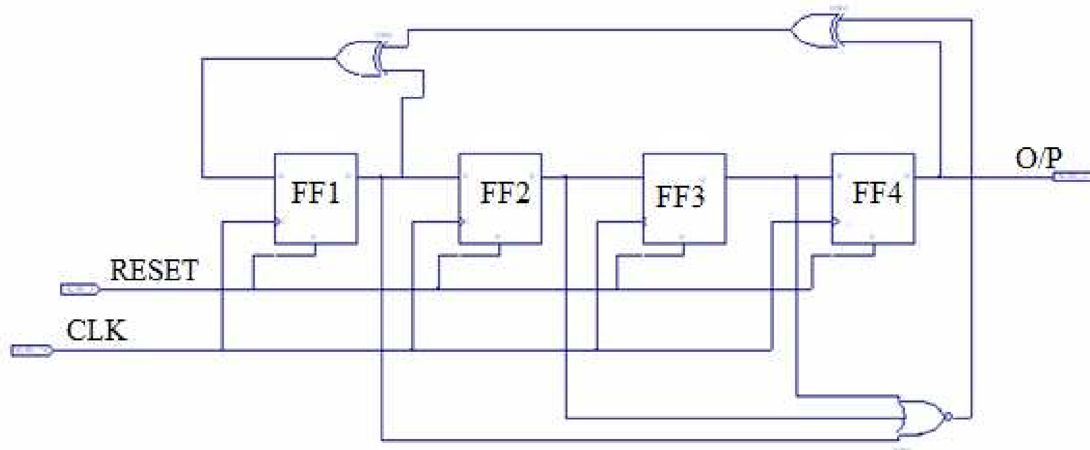

Figure 2.4 Maximal Lengths LFSR [13]

The outputs of the LFSR are initially loaded with a combination of 1's and 0's normally referred to as the seed vector. Proper selection of the generator polynomial is important in order to ensure the generation of the entire sequence. Common Clock signal is applied to the entire chain of flip-flops which essentially enables the propagation of the logic values present at the inputs to the flip-flop outputs. These random outputs are used as the input stimulus for circuit to be tested.

Normally this random pattern can be propagated through a known good circuit and the output of the circuit is captured using a MISR (Multi- Input Shift Register). The MISR output also known as the good signature is then used to compare with the signature obtained for other similar circuits [13].

One of the drawbacks of generating a pattern using the above approach is the reduced correlation between the bits (output bits of the LFSR) of the successive vectors. This can attribute to one of the key differences between the vectors used for functional verification of the IC in the system environment compared to the vectors used in the manufacturing test environment.

In a functional operation environment, the input stimulus is generated by the component(s) of the system interfacing with the device under test and therefore can have better correlation between the successive vectors.

Additionally the number of vectors generated in a functional test environment can be much lower than the number of vectors generated by the LFSR. This increase in the number of test vectors combined with reduced correlation between the bits can result in

significant increase in the switching activity of the circuit under test and therefore increased power consumption of the device in the Manufacturing Test environment.
The increased power consumption by the device in the manufacturing test environment therefore can in most cases exceed the maximum power consumption specification of the IC resulting in un-repairable device failures begins with a pattern generated using a conventional LFSR causing significant loss of yield.

2.5 Low Power Test Pattern Generation Techniques:

2.5.1 Low Power Test Pattern Generator [Dual Speed LFSR (DSLFSR)]

Figure 2.5(a) shows DS-LFSR testing excited generator which is a n input CUT. In order to reduce change frequency of circuit input end and raise the correlation between adjoining testing vector. Test Pattern Generation is divided into two LFSR, one is a slow LFSR, the other is a normal-speed LFSR. When testing model generation, slow LFSR is controlled by SCLK, but in normal working condition, it's controlled by CLK; usually, slow clock frequency is the $\frac{1}{d}$ of normal clock frequency. Like this, more switching input end in circuit-under-test can connect with slow LFSR, thus decreasing internal node switching of the circuit-under-test to lower power consumption [18].

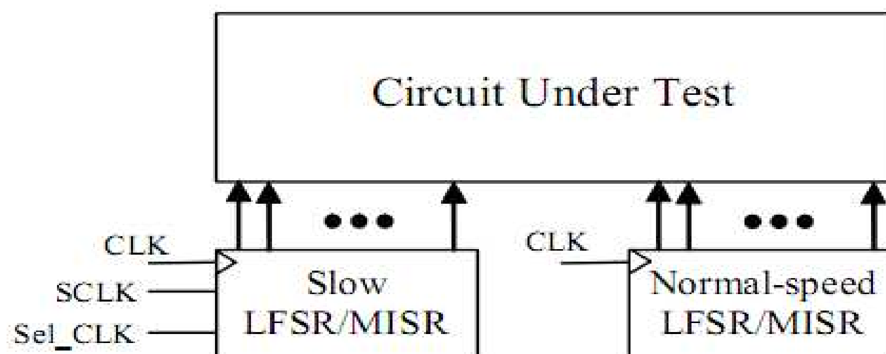

Figure 2.5 (a) Low Power Consumption BIST Test Realization of DS-LFSR [18]

2.5.2 Low Transition Random Test Pattern Generator (LT-RTPG)

Figure 2.5(b) is the general structural drawing of LFSR and CUT, which imposes testing vector on scanning chain series[2]. It's on the basis of r steps ML-LFSR, and additional k input end "AND" gate and a T trigger. As figure 2.5 (c) shown, the input end of AND gate connects with Q or Q end of LFSR, the output end links with the input end of T trigger. Because the output of T trigger drives the input of scanning chain, the probability which scanning unit receives signal is 1/2. Only when the input end of T trigger is 1, its output can change, so if state switching probability of two adjoining scanning units is $1/2^k$, it can reduce the testing power consumption during scanning [14].

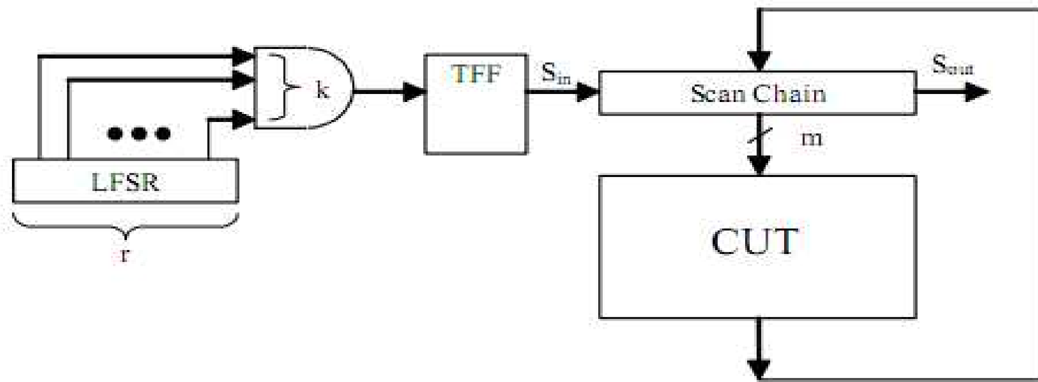

Fig 2.5(b) BIST Structure of LT-RTPG and Test-per-scan [14]

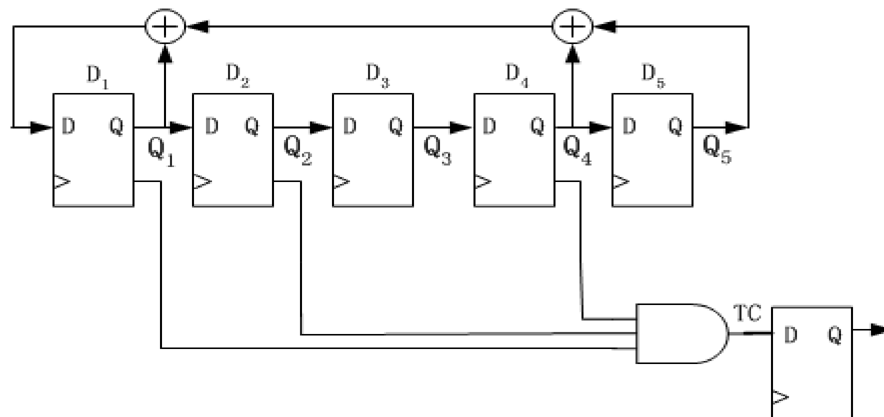

Fig 2.5 (c) LT-RTPG Schematic diagram [14]

2.6 Low Power Consumption BIST Testing Method of Gated Clock

In current integrate circuit (IC), clock signal is connected to the circuits through an clock tree, which is formed with clock buffers. The clock tree provides enough drive and control the clock offset within a determinate range. Because of the changes of clock signal during system operation, power consumption is increased due to the clock tree. It means that reduction of redundant switching of clock tree will lower the power consumption. On the other hand, the switching activity of circuit under test (CUT) during test application can be as high as 200% of that in normal mode, because that the functional input vectors applied to the circuit during normal mode have significant correlations while pseudorandom test patterns have not. It leads to a prominent increase of power consumption [9,19].

There are three sources of producing power consumption in scanning test, one is logical power consumption produced by the switching of logical gate in circuit; another is the scanning power consumption caused by scanning path in its operation process; the last one is clock power consumption used up by clock tree when the clock is changing. So power consumption in scanning testing is the sum of above three.

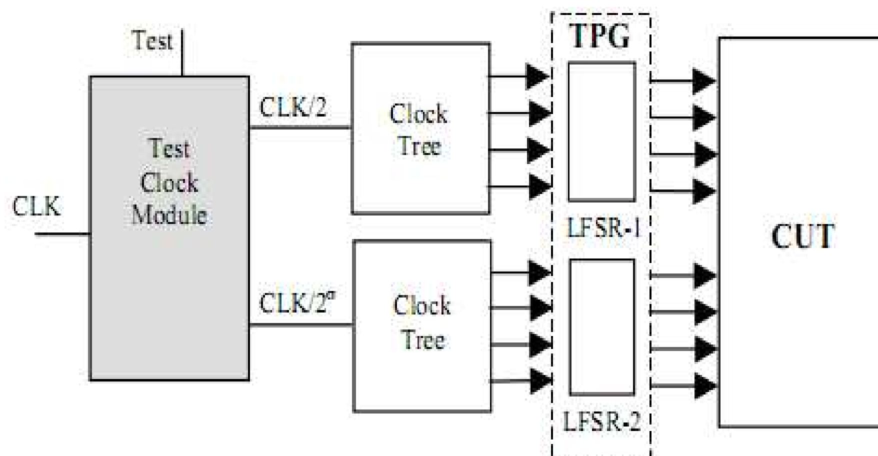

Figure2.6 (a) TPG Structure of Low Power Consumption BIST2 [9]

As figure 2.6 (a), in a clock period of scanning operation, the half D trigger of the whole testing generator is activated by a clock, and in the next clock period the another clock activates the rest part. The frequency of these two clocks is the half of

system clock and synchronizes with system clock CLK but exists deviation in period, shown in figure 2.6 (b).

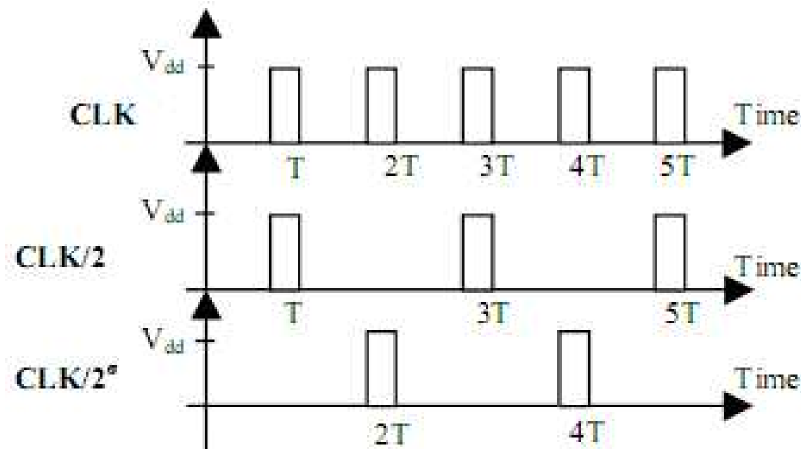

Figure2.6 (b) Sequence of Phase-shift Clock [9]

2.7 Scan-Based BIST Scheme for Low Power Testing

Scan-based BIST integrates scan design and built-in self-test methodologies [4,20,21]. Using scan, the memory elements are connected into a shift register and thus their values can be controlled or observed during the test mode by shifting the desired values into the register or shifting out the content of the register. BIST is a technique that makes the circuit test itself without using automatic test equipment. It includes on-chip test pattern generator (TPG) [for e.g., Linear Feedback Shift Register (LFSR)] and response analyzer [for e.g., Multiple Input Signature Register (MISR)]. The LFSR is commonly used as a TPG in low overhead BIST schemes. The correlation between consecutive random patterns generated by an LFSR is low but a significant correlation exists between consecutive patterns at the primary inputs (PJs) during the normal operation of circuit. For DFT, the situation is even worse. Here, during test mode, it breaks all the secondary input (SI) and secondary output (SO) to apply any desired value at state FFs i.e. breaks a sequential circuit into a combinational block and state elements (scan elements/D FFs). This destroys the correlation that typically exists between successive states of FSM leading to even lesser correlation. Due to all these, the switching activity in a circuit can be significantly higher during BIST than that

during its normal operation, which can cause very destructive consequences like excessive heat dissipation, electro-migration and simultaneous switching noise, i.e. power / ground noise. Hence, excessive switching leads to the failure of some good chips only because they are tested, leading to unnecessary loss of yield. Thus, reducing the heat dissipated during test application is becoming a very important objective these days, particularly for the large VLSI systems [4].

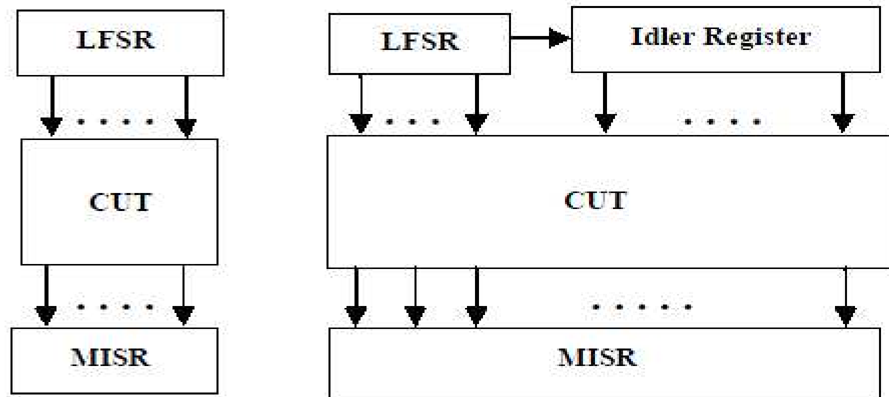

Figure 2.7 (a) Test-per-clock BIST architecture [4]

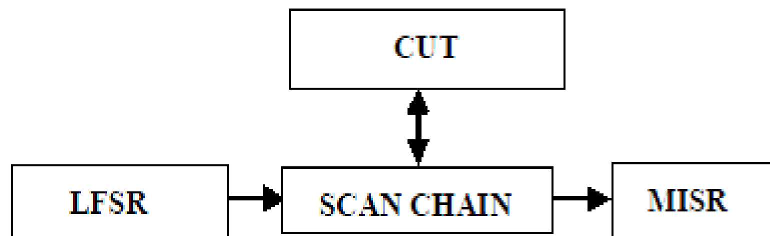

Figure 2.7 (b) Test-per-scan BIST Architecture [4]

Scan based built-in self test (BIST) architectures can be divided into two classes test-per-clock and test-per-scan, based on how the test vectors are applied.

In test-per-clock architecture (Fig.a), a test vector is applied to the primary inputs every clock cycle and response is captured every clock cycle. In test-per-scan BIST architecture (Fig.b), a test vector is applied to the circuit under test (CUT), via scan chain, every m+1 clock cycles, where m is the number of flip-flops in the scan

chain. The response to a test vector applied to CUT is captured into the scan chain and shifted out during next m clock cycles, and loaded into a response analyzer. At the same time a new test vector is scanned into the scan chain. BIST is a technique that makes the circuit test itself without using automatic test equipment. It incorporates on chip test pattern generator (TPG) [typically a linear feedback shift register (LFSR)] and response analyzer [typically a multiple input signature register (MISR)]. LFSR is commonly used as TPG in low overhead BIST. The correlation between consecutive patterns generated by LFSR is low but a significant correlation exists between consecutive vectors at the inputs during normal operation of circuit. Hence, switching activity (SA) in a circuit can be significantly higher during BIST than that during its normal operation.

Excessive switching activity during test can cause serious failures, such as accelerated electro migration and switching noise, lowering reliability of the circuit. It has been shown that switching activity during test mode can be reduced (at the cost of reduced fault coverage) by using a low transition random test pattern generator (LT-RTPG). It has been shown that using different functional cycle lengths during scan operation can improve the test quality as well as increase the number of test vectors applied at-speed, at the cost of minor increase in complexity of the BIST controller.

It is observed that combining test-per-clock and test-per-scan schemes and, using two functional cycle lengths during scan and LT-RTPG as TPG, can take optimal advantage of the three schemes and reach the desired FC earlier with reduced switching activity compared to conventional LFSR-BIST.

2.8 Circuit Partitioning for low power testing

Another approach involves partitioning the original circuit into two structural sub-circuits so two different BIST sessions can be used to successively test each sub-circuit. In order to minimize the area overhead of the resulting BIST scheme, however, the number of connections between the sub-circuits of the partition, called the *cut size*, has to be minimal. The basic scheme of partitioning a circuit into two sub-circuits is shown in Figure3.7. In Figure 2.8 (a), a logic circuit is partitioned into two sub-circuits *C*1 and *C*2. Many such partitions exist for large VLSI circuits. Figure 2.8 (b) depicts how multiplexers are inserted between the two sub-circuits. By controlling the

multiplexers, all inputs and outputs of each sub-circuit can be accessed using primary inputs and primary outputs. For example, to test sub-circuit *C*1, the multiplexers can be controlled as shown in Figure 2.8(c). The demultiplexers (DMUX) on the sets *B* and *C* of input signals are added to avoid switching activity in *C*2 during the test of *C*1. This technique tries to find an optimal partitioning solution, which is a *NP*-complete problem, by using a simple *graph partitioning* algorithm. Traditional partitioning algorithms compute a partition of a graph by directly operating on the original graph. This approach is often too slow and can lead to poor quality partitions in terms of cut size which is representative of the area overhead of the BIST scheme. The multilevel partitioning algorithm follows a completely different approach. The algorithm successively decreases the size of the graph (or the hyper graph) by collapsing vertices and edges, partitions the smallest graph, and then uncoarsens it to construct a partition for the original graph. At each level of the uncoarsening phase, an iterative refinement algorithm is used to improve the partition [6].

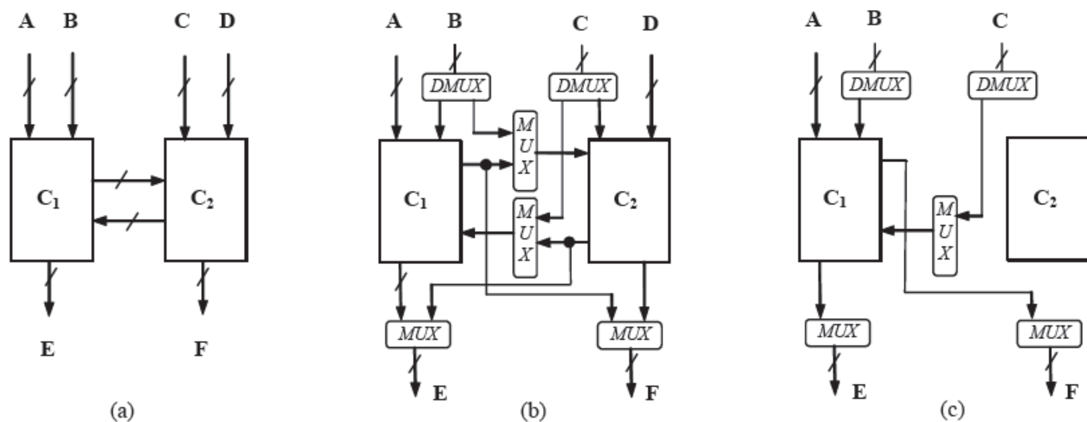

Figure 2.8 Circuit partitioning for low-power testing [6]

By partitioning the circuit into two sub-circuits and testing the sub-circuits in successive test sessions, average and peak power consumption are minimized. In addition, this approach reduces the total energy consumed during BIST operation because the test length required for the two sub-circuits is usually shorter than that of the original circuit. This is due to the fact that circuit partitioning increases the controllability and observability of the internal nodes in the CUT. The area overhead with this approach is low. Drawbacks are a slight penalty on circuit performance and a

non-negligible impact on routing. The proposed strategy can be applied to scan-based BIST or parallel BIST by adapting the test pattern generation structure.

2.9 Vector Filtering BIST

BIST techniques based on vector filtering to reduce power consumption have also been proposed in [5]. It is based on the observation that as self test progresses, the detection capability of the pseudo-random test vectors generated by an LFSR decreases very quickly. Therefore, many of the pseudorandom test vectors do not detect new faults despite consuming a significant amount of energy. For example, only 159 patterns among the 2524 required to reach 99.9% fault coverage actually detect faults in the benchmark circuit c5315 . In addition, the length of the sub-sequence of consecutive non-detecting test vectors is often long. For example, the longest sub-sequence of consecutive non-detecting vectors in the pseudo-random test sequence generated for the benchmark circuit s1488 [to reach 100% fault coverage contains 509 vectors, while the complete test sequence is of length 2931. Consequently, the main goal of these techniques is to filter test vectors that do not detect additional faults, thus preventing the CUT from being excited by these undesired vectors. For this purpose, a decoder can be used during BIST pattern generation to store the first and last vectors of each sub-sequence of consecutive non-detecting vectors to be filtered. The output of this decoder provides the logic value 1 after detection of each of these vectors. Then, the vector filtering structure has to allow or prevent application of these test vectors to the circuit inputs. A toggle D flip-flop (Figure 2.9 (a)) is used to control the transmission of stimuli from the LFSR to the CUT. The transmission is activated or inhibited by means of a transmission gate network.

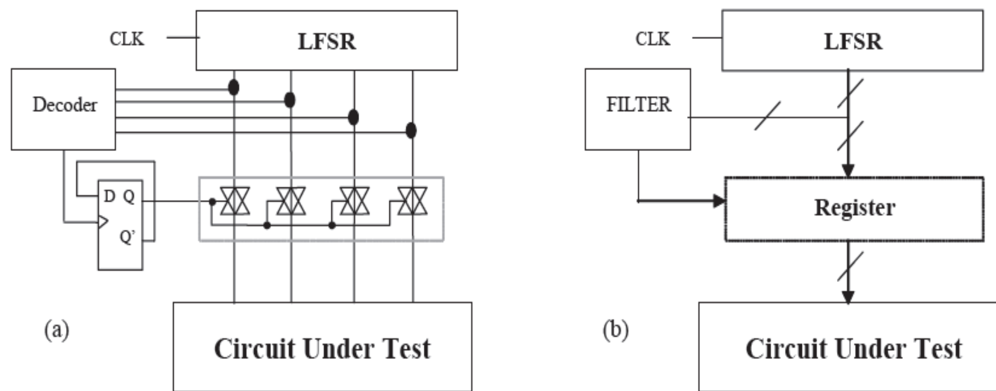

Figure 2.9 Two vector filtering BIST structures [5]

Rather than just filtering the sub-sequences of non-detecting vectors, it is also possible to filter all vectors that do not detect any faults. Using this approach, a register made of latches is used to control the transmission of test vectors from the LFSR to the CUT. A filter module is used to provide the needed control signals to the register (see Figure 2.9 b).

The main advantage of all these techniques is that they allow significant reduction of energy and average power consumption during testing. The drawbacks are the negative impact on circuit performance and the area overhead which may be high in some cases.

CHAPTER

3

Design and Implementation of proposed low Power test pattern generator

Here we present a new test pattern generator for low power BIST. The proposed technique increases the correlation between test patterns. The original patterns are generated by an LFSR and our proposed technique generates and inserts intermediate patterns between each pair patterns to reduce the primary inputs (PIs) activities which eventually reduce the switching activities inside the circuit under test, and hence power consumption. Adding intermediate test patterns does not prolong the overall test length for target fault coverage, and hence the test application time is still the same. We embed our proposed technique into an LFSR to create our LPTPG. We will show that both the average and peak powers are significantly reduced in LP-TPG compared to a conventional LFSR [8].

3.1 Idea behind Low Power Test Pattern Generation

One way to improve the correlation between the bits of the successive vectors is to avoid frequent transitioning of the logic levels (1→0 or 0 → 1) of the primary inputs.

The new approach entails inserting 3 intermediate vectors between every two successive vectors. The total number of signal transitions between these 5 vectors is equal to the total number of signal transitions between the 2 successive vectors generated using the conventional approach. This reduction of signal transition activity in the primary inputs reduces the switching activity inside the design under test and therefore results in reduced power Consumption by the device under test [17].

The additional circuitry used to accomplish the generation of the 3 intermediate vectors is minimal at best consisting of few logic gates. The pattern generation controller

which is designed using Verilog code can be very easily modified for the required number of LFSR outputs. The number of outputs required is driven by the number of test inputs required for circuit under test. The technique of inserting 3 intermediate vectors is achieved by modifying the conventional LFSR circuit with two additional levels of logic between the conventional flip-flop outputs and the low power outputs as shown in Figure 3.1. The first level of hierarchy from the top down includes logic circuit design for propagating either the present or the next state of the flip-flops to the second level of hierarchy. The second level of hierarchy is a multiplexer function that provides for selecting between the two states (present or next) to be propagated to the outputs as low power output.

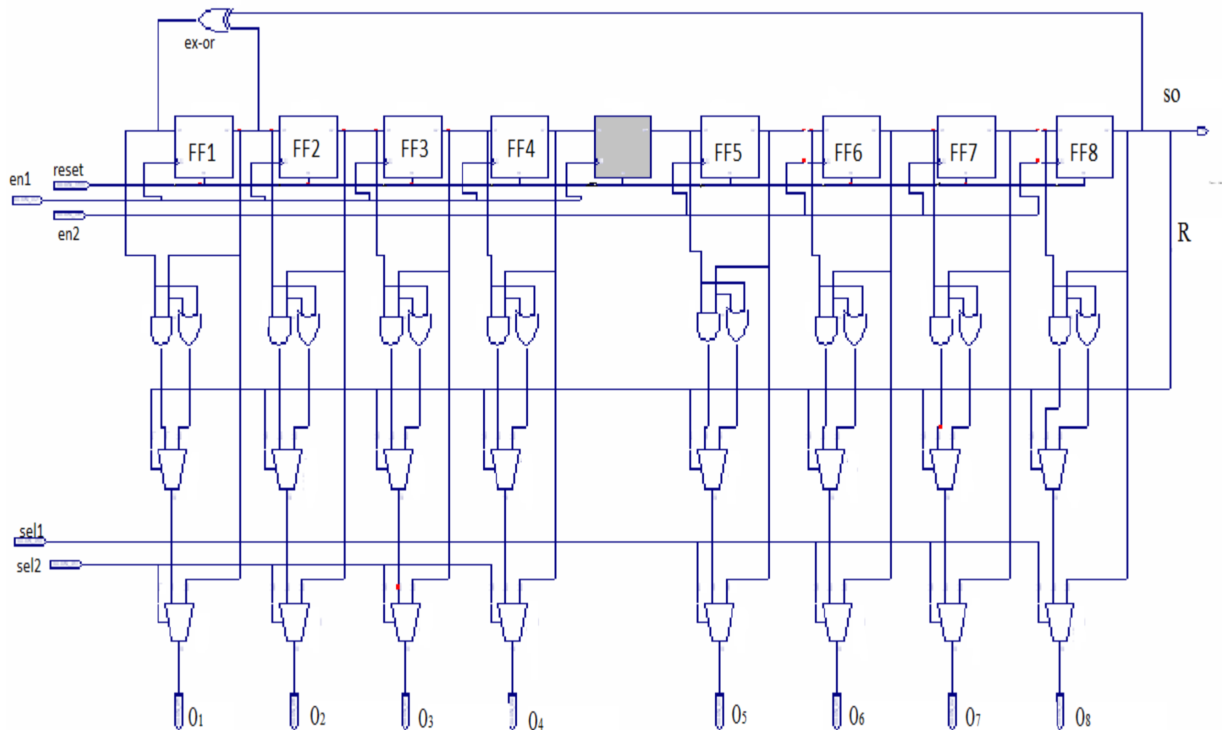

Fig. 3.1 8-bit LP-LFSR [8]

In the simulation environment, the outputs of the flip-flops are loaded with the seed vector. The feedback taps are selected pertinent to the characteristic polynomial $x^8 + x + 1$. Only 2 inputs pins, namely test enable and clock are required to activate the generation of the pattern as well as simulation of the design circuit. It is also noteworthy here that the intermediate vectors in addition to aiding in reducing the

number of transitions can also empirically assist in detecting faults just as good as the conventional LFSR patterns.

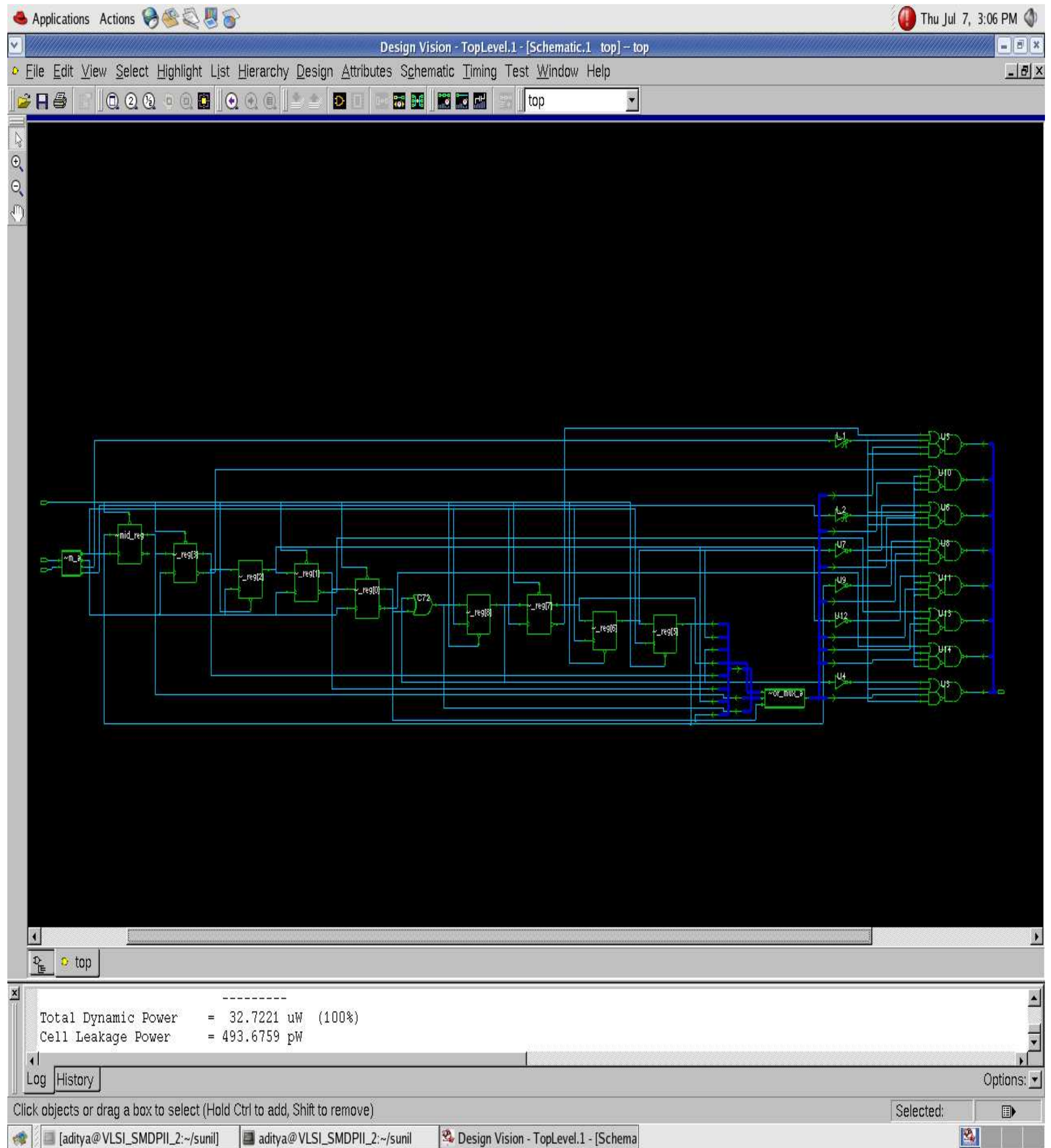

Fig. 3.2 Schematic of LP-LFSR

Fig. 3.3 Schematic of LP-LFSR FSM

Fig. 3.4 Schematic of LFSR, AND-OR, MUX

Table 3.1 output of the LP-LFSR for R=1

No. Of clk	pattern	en1	en2	Sel1	Sel2	LP-LFSR
1	T1	1	0	1	1	1010 1011
2	Ta	0	0	1	0	1010 1111(R=1)
3	Tb	0	1	1	1	1010 0101
4	Tc	0	0	0	1	1111 0101(R=1)
5	T2	1	0	1	1	0101 0101

3.2 Description of the technique to produce low power pattern for BIST

The following is a description of a low power test pattern generation technique as depicted in the 9-bit LFSR based schematic in Figure 3.1 Verilog code is used in assigning the initial output states (0100 1011) of the 9-bit LFSR. The feedback taps are designed for maximal length LFSR generating all zeros and all one's as well [8].

The first step is to generate T1, the first vector by enabling (clocking) the first 4-bits of the LFSR and disabling (not clocking) the last 4 bits. This Shifts the first 4 bits to the right by one bit. The feedback bits of the LFSR are the outputs of the 8th and the first flip-flop. The output of the 8th flip-flop is 1 and the output of the first flip-flop is 0. The exclusive-or of the 8th-flip-flop (logic 1 in this case) and the first flip-flop (logic 0 in this case) is input (1 EXOR 0) = 1 into the first D flip-flop. The new pattern in the first four bits of the LFSR is 1010. Note that the shaded register is clocked along with the first 4 bits of the LFSR. So the input of the shaded flip-flop is the output of the 4th flip-flop which in this case is 0.

Also note that prior to the first clock, the input of the shaded register was the seed value of the 4th flip-flop at the output of the 4th flip-flop which in this case is 0. So after the first clock this value of 0 will now appear at the output of the shaded flip-flop. In other words the value of the 4th output is stored in this shaded register and is used in the next few steps.

The first 4 shifted bits of the LFSR and the last 4 un-shifted bits (i.e. the seed value) are propagated as T1 (1010 1011) to the final outputs.

3.3 Steps involve generating the 3 intermediate patterns from T1 .

These patterns are defined as Ta, Tb and Tc.

Ta is generated by maintaining (disabling the clock to the first 4 bits) the first four bits of the LFSR outputs (as is from T1) as the final first four low power outputs 1010. Note that the clock to the last four bits of the LFSR is also disabled. The last four bits however are the outputs from first flip-flop and 101 for the 2nd, 3rd and 4th flip-flop respectively. The next the injector circuits the injector circuit compares the next value (@ the input of the D-flip-flop) with the current value (@ the output of the D-flip-flop).

According to T1, the outputs (current values) of the last 4 bits of the LFSR are 1011. The next values are the values at the inputs of the D-flip-flops which in this case are 0101. Compare the current values (1011) bit by bit with the next values (0101). If the values bit by bit are not the same then use the random generator feedback R (in this case is logic 1) as the bit value as shown in the schematic above. If however both values bit by bit are the same then propagate that bit value to output as opposed to the R bit. This bit by bit comparison gives us the last four bits of Ta to be 1111. Therefore Ta = 1010 1111.

Next step is to generate Tb. Shift the last 4 flip-flops to the right one bit but do not shift the first 4 flip-flops to the right. The clock to the first 4 bits plus the shaded flip-flop is disabled. The clock to the last 4 bits is enabled.

Propagate the outputs of the flip-flops of the entire LFSR as opposed to the outputs of the injection circuit to the outputs (low power). The injection circuits are disabled. As in Ta, maintain the first four LFSR outputs (1010) as the low power outputs. Again from Ta, the inputs of the last four D flip-flops from the previous step (generating Ta) are 0101. Also note that the output of the shaded register is 0 from the previous step (generating Ta). Therefore the input of the 5th flip-flop is a 0. The outputs of the last 4 flip-flops are 0101 resulting in Tb = 1010 0101.

The 3rd intermediate vector Tc is generated via disabling the clock to the entire LFSR. Propagate the first 4 outputs from the injection circuit as the first 4 low power

outputs and maintain the last 4 low power outputs the same as Tb. Generating injection circuit outputs for Tc is conceptually the same as explained above in generating Ta. Current values (@ the outputs of the flip-flops) of the first four flip-flops are compared with the next values (@ the inputs of the flip-flops) of the flip-flops.

The feedback from the 8th flip-flop is 1 (please see generating Tb). Therefore the logical feed forward value of R is 1. The feedback value from the first flip-flop is also 1 as per the current values above. The exclusive or of two ones is a 0. Therefore the input to the first flip-flop is a 0 which is also the next state of the first flip-flop. Hence the next values are 0 for the values are 0101.

The first four outputs from the injection circuit are 1111. The last 4 outputs are the same as Tb which are 0101 resulting in the 3rd and final intermediate vector Tc = 1111 0101.

Generating T2 is quite similar to generating T1. As in Tc the outputs of the last four LFSR flops are 0101. The outputs of the first 4 flip-flops of the LFSR are the current values which are 1010. Therefore the seed vector for generating T2 is 1010 0101.

Shift the first four bits of the LFSR plus the shaded flip-flop. Do not clock the last four flip-flops. Propagate the outputs of the entire LFSR to the final low power outputs.

The output of the 8th flip-flop from the previous step (generating Tc) is a 1 and the output of the first flip-flop from the previous step (generating Tc) is also a 1. The exclusive or of the output of the 8th flip-flop and the first flip-flop is 0.

Therefore the input to the first flip-flop will be a 0. The inputs to the 2nd, 3rd, 4th and the shaded flip-flops are 1010. These are also the current values from the previous step (generating Tc).Shifting the first four flip-flops of the LFSR to the right by one bit results in 0101 as the outputs of the first four flip-flops. Therefore T2 generated is 0101 0101. This concept of low power pattern generation is extended to 36-bits required for the design circuit.

CHAPTER

4 Results and discussion

4.1 Simulation using standard LFSR pattern

The standard 36-bit pattern is generated using the LFSR configuration as shown in figure 4.1 below. The schematic in the case of conventional pattern generation consists of 36 flip-flops connected in series. The design is modified as indicated in figure 4.1.1 below with feedback taps to generate a maximal length pattern generator including all 0’s and 1’s.The number of vectors expected in this case are 236. The outputs of the 36-bit LFSR are used as the inputs to the c432 ISCAS-85 interrupt controller design circuit. A common clock is supplied to all flip-flops. A seed value is assigned to the output of each flip-flop. Each clock pulse thereafter shifts the logic value present at the input of the flip-flop to its output.

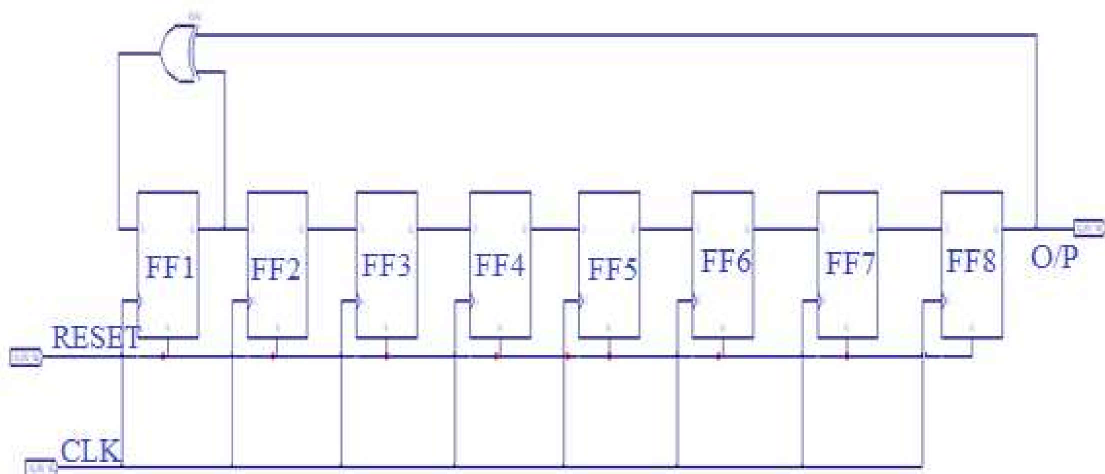

Figure 4.1 8-bit LFSR [1]

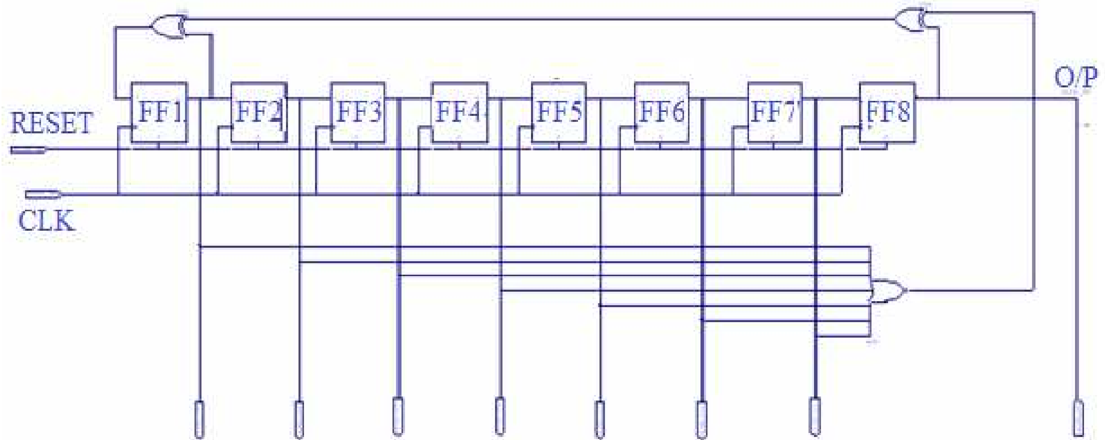

Figure 4.2 Maximal 8-bit LFSR [1]

4.2 Simulation Using LP-LFSR

LP-LFSR pattern is generated as shown in Figure 4.2 below. The simulation report confirms the number of signal transitions between the bits of the successive vectors to be the same for both patterns namely, conventional and LP-LFSR.

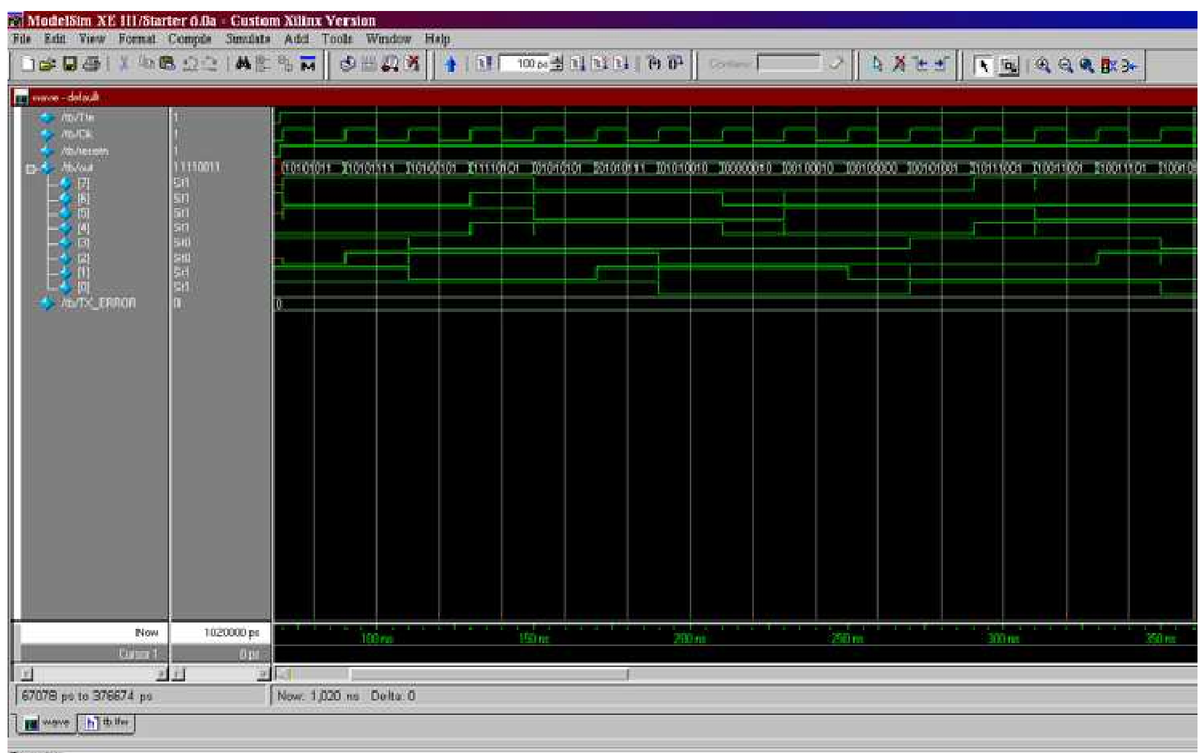

Figure 4.3 LP-LFSR Pattern Simulations

4.3 Power consumption using standard conventional pattern

The methodology used to estimate the power consumption is similar to the one used for the low power pattern generator. As shown in figure 4.3 the design circuit is simulated in the Xilinx ISE development environment using Mentor Graphics ModelSim. The number of test vectors is restricted in order to contain the Verilog Core Dump file to a manageable size for power consumption analysis.

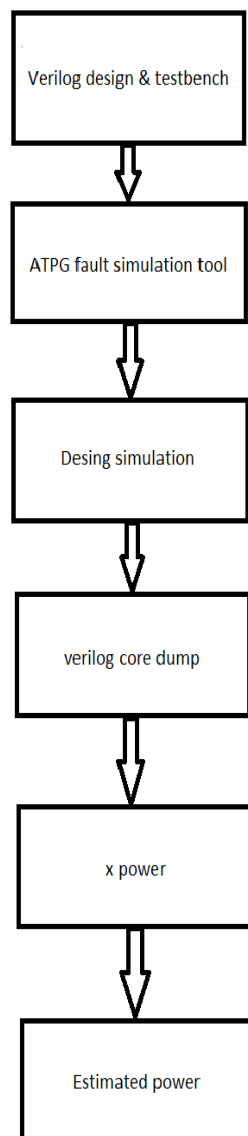

Fig 4.4 Power Estimation Flow

The VCD file contains the switching activity of the design circuit for the number of test vectors. The number of test vectors is obtained from a Fault simulation tool called TetraMax from Synopsys. This tool takes the VCD file as the input file along with the c432 interrupt controller design file and produces the number of test vectors required for the desired fault coverage.

Another way of generating specific number of vectors is by using the clock period and simulation time. For instance if the clock period is 60ns and the simulation time is 60us. The number of vectors produced will be 60us/60ns = 1000.

Using the standard pattern, the ATPG tool generates 330 vectors for 98% fault coverage which translates to approximately 16mw power consumption by the c432 circuit.

4.4 Power consumption using low power pattern

The key to achieving Low power consumption in System-On-Chip devices is by reducing the switching activity in the device under test. The low power technique described in chapter 3 improves the correlation between the signals of the successive vectors (i.e. input stimulus to the circuit under test) resulting in reduced transitions of the primary inputs hence reducing switching activity inside the circuit under test [10].

The methodology used in estimating the power consumption of the device under test includes the generation of the 36-bit low power pattern, synthesizing the c432 circuit using generic libraries, running the 36-bit pattern on the c432 circuit and computing the power consumption using a power estimation EDA tool.

Circuit Simulation is implemented using Mentor's ModelSim tool in the Xilinx ISE development environment. It is important to restrict the simulation time (i.e. number of test vectors) to a few microseconds in order to contain the VCD file to a manageable size for the purpose of evaluating the switching activity. Xilinx XPower tool is used to read in the VCD file for power consumption estimation. TetraMax was used to determine the number of test vectors required for the desired fault coverage.

Power consumed by the c432 circuit is observed to be 10mw using 370 vectors for 98% fault coverage.

4.5 Power Consumption Comparison (Standard LFSR vs LP-LFSR)

Two test benches are designed using Verilog. The first test bench uses a conventional test pattern generator and the second test bench uses a low power pattern generator. Both test benches are used to simulate a common design circuit which in this case is an industry standard 27-channel interrupt controller benchmark circuit.

Both test benches are designed to use the same pre-defined clock period as well as identical simulation time. This ensures the same number of test vectors generated by both test benches. The numbers of gates used by the interrupt controller are 250 as indicated by the synthesis reports from the Xilinx development environment. Logic gates used by the conventional test bench are 60 and the numbers of gates used by the low power test bench are 135.

TetraMax ATPG and Fault simulation tool is used to estimate the number of test vectors required for 98% fault coverage of the interrupt controller. The tool generated 330 vectors for the conventional test bench and 370 vectors for the low power test bench. Both test benches produced almost the same number of test vectors for the desired fault coverage thus demonstrating about the same test time used in both cases.

The two VCD files (for conventional and low power pattern) containing the interrupt controller's switching activity were used for power consumption estimation by Xilinx xpower power analysis tool. Xpower calculates the average power consumed by the circuit for each test vector applied by observing the logic value at each internal and external node of the circuit. The transition in the logic value at each node ($1 \rightarrow 0$ or $0 \rightarrow 1$) results in the dynamic power consumption by the gate of the Xilinx Spartan 2 device. Total power consumed by the circuit is the sum of the power consumption by the circuit for each test vector.

The reported power consumption estimates as indicated above demonstrates approximately 60% lower power consumption by the interrupt controller using the low power test bench as compared with the conventional pattern. This result demonstrates lower number of logic transitions at the internal and external nodes of the test circuit. The difference in the power consumption of the test logic between the two approaches (65 gates versus 135 gates is negligible). Similarly analysis is done for other benchmark circuits also.

Table 4.1 Power Consumption Comparison

LFSR	FAULT COVERAGE	NO. OF TEST VECTORS	NO. OF GATS IN TEST CUT	NO. OF GATS IN TEST CONTROLLER	POWER CONSUMPTION
CONVENTIONAL LFSR	98%	330	250	65	16mw
LP-LFSR	98%	370	250	130	10mw

The configurable logic blocks and input/output blocks used in most field programmable gate arrays such as the Spartan 2 device are typically not optimized for lowest power consumption compared with some options of the gate array and Standard cell products. Therefore it is possible to achieve even lower power consumption by the circuit in an ASIC implementation compared with an FPGA.

Here some experimental results are shown in tables 4.2 for ISCAS benchmark circuits.

TABLE 4.2 ISCAS Benchmarks Specifications

CIRCUIT	PI	PO	FC%
C432	36	7	98
C499	41	32	98
C880	60	26	97

Tool used

1. **Tetramax** and **Design Vision** OF SYNOPSIS CAD TOOLS to calculate the fault coverage.
2. **Modelsim** for wave form generation.
3. **ATALANTA** for test pattern generation and fault simulation.
4. **Xillinx** for power calculation.

CHAPTER

5 Conclusion

A Technique to generate low power PRPG is implemented and applied on an industry standard benchmark circuit for power consumption estimation. The comparison of power consumption by the circuit demonstrates 60% lower power consumed by the circuit when using low power pattern as the input stimulus compared with the input stimulus generated by the conventional LFSR based PRPG.

This thesis report presented a new low-power LFSR to reduce the average and peak power of a circuit during the test mode. By increasing the correlation between the test pattern, the switching activity in the circuit under test and eventually the power consumption is reduced. Additional intermediate test patterns inserted between the original random patterns reduces the Pis activity, average and peak power, but do not affect on fault coverage. The experimental results indicate up to 63% and 27% reduction in average and peak power, respectively, while it achieves the same fault coverage. LP-TPG also reduces the instantaneous power violation compared to conventional LFSR.

RECOMMENDATIONS FOR FUTURE WORK

SOC designs are making a rapid shift from mostly digital to mixed signal including millions of user defined logic gates and dozens of IP (Core as well as I/O based). IC Verification and Test strategy needs to include advanced controllers and pattern generators for testing digital as well as analog components of the chip. Pattern generation inside the chip is well known to cause increase in the power consumption of

the IC during the manufacturing test. New design and test techniques need to be investigated to keep this increase in the power consumption by the chip as minimum as possible.

The availability of advanced manufacturing process rules in the design/verification libraries and tool flow methodologies is mandating the IC front-end designers to verify the manufacturability of the chip much in advance in the design process . Therefore development of the new SOC DFT techniques needs to be compliant with the advanced DFM rules.

Appendix

Benchmark Design Circuits:

Several Industry standard benchmark circuits such as ISCAS-85, ISCAS-89, etc can be used to test new design, test and manufacturing approaches and technologies. Following is a brief description of one of the ISCAS-85 circuits used for the purpose of testing the new low power pattern generation scheme described above.

For example c432 is a 27-channel interrupt controller whose circuit details are as follows: The input channels are grouped into three 9-bit buses (we call them A, B and C), where the bit position within each bus determines the interrupt request priority. A forth 9-bit input bus (called E) enables and disables interrupt requests within the respective bit positions. Figure A1 below shows the c432 circuit. Figures A3 to A7 below show the logic of the underlying modules.

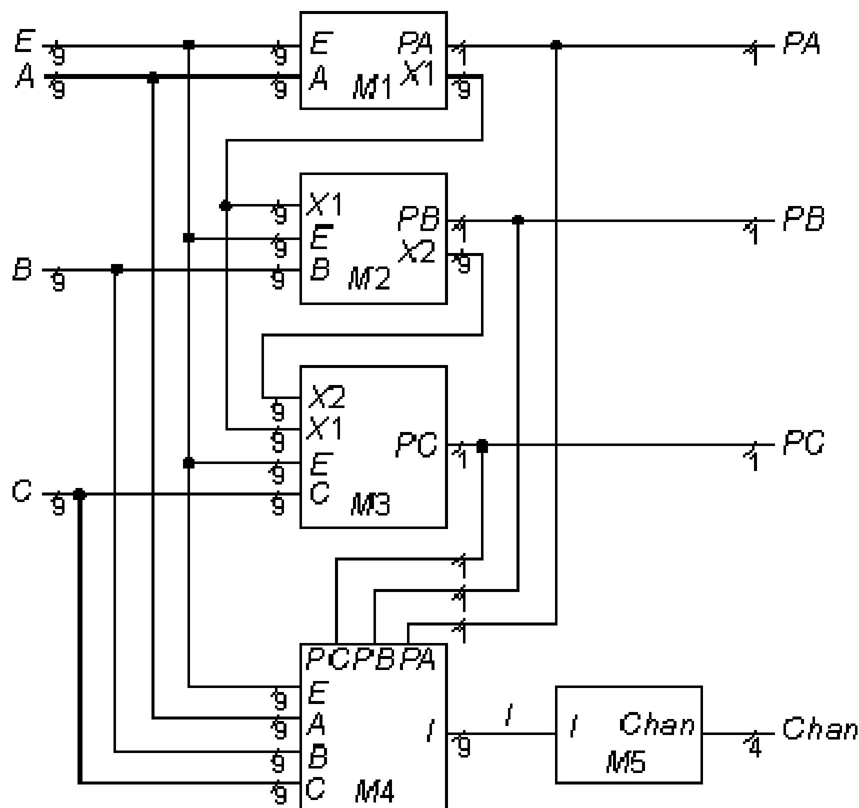

Fig A1: ISCAS-85 C432 27-channel interrupt controller

The interrupt controller has three interrupt request buses A, B and C, each having nine bits or channels, and one channel-enable bus E. The following priority rules apply: A[i] > B[j] > C[k], for any i, j, k; i.e., bus A has the highest priority and bus C the lowest. Within each bus, a channel with a higher index has priority over one with a lower index; for example, A[i] > A[j], if i > j. If E[i] = 0, then the A[i], B[i], and C[i] inputs are disregarded.

The seven outputs PA, PB, PC and Chan [3:0] specify which channels have acknowledged interrupt requests. Only the channel of highest priority in the requesting bus of highest priority is acknowledged. One exception is that if two or more interrupts produce requests on the channel that is acknowledged, each bus is acknowledged. For example, if A[4], A[2], B[6] and C[4] have requests pending, A[4] and C[4] are acknowledged. Figure 3.4.7 is a 9-line-to-4-line priority encoder.

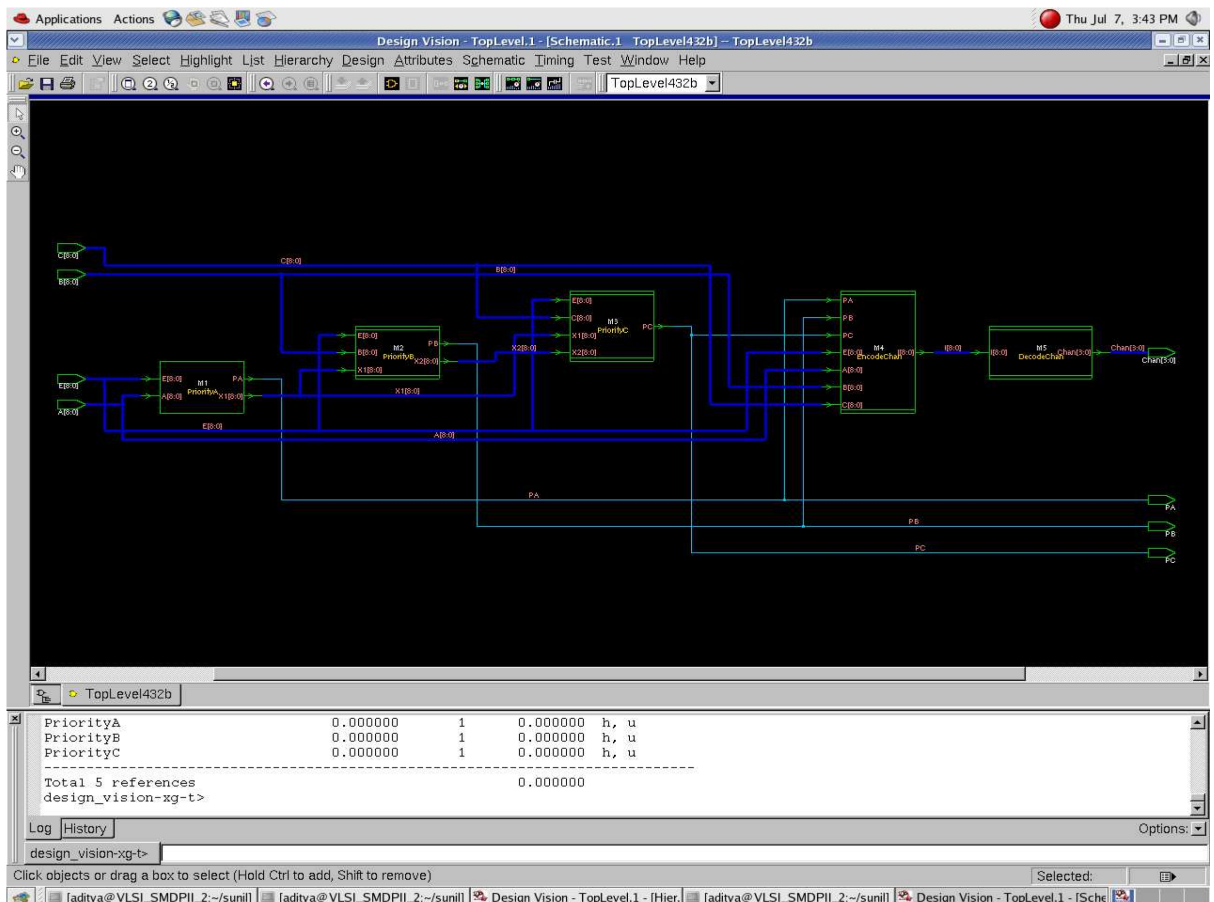

Fig A2: schematic of C432 27-channel interrupt controller

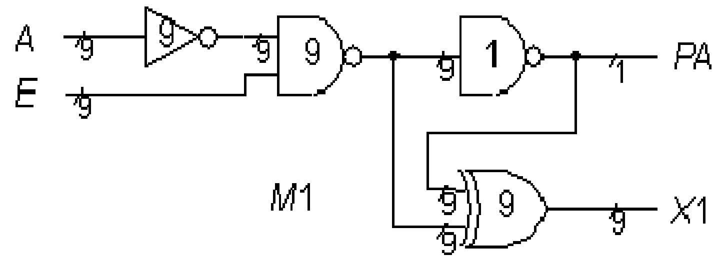

Fig A3: ISCAS-85 c432 M1

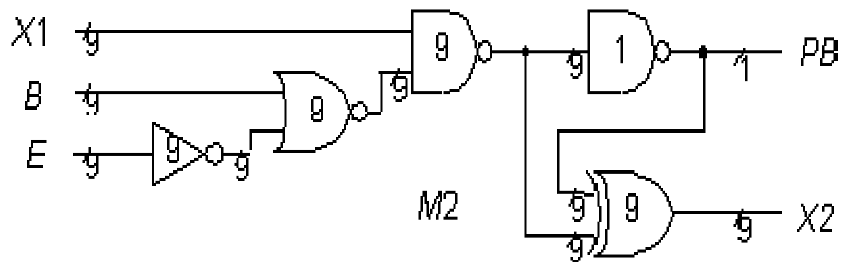

Fig A4: ISCAS-85 c432 M2

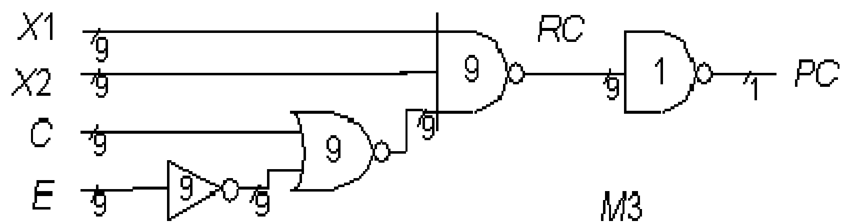

Fig A5: ISCAS-85 c432 M3

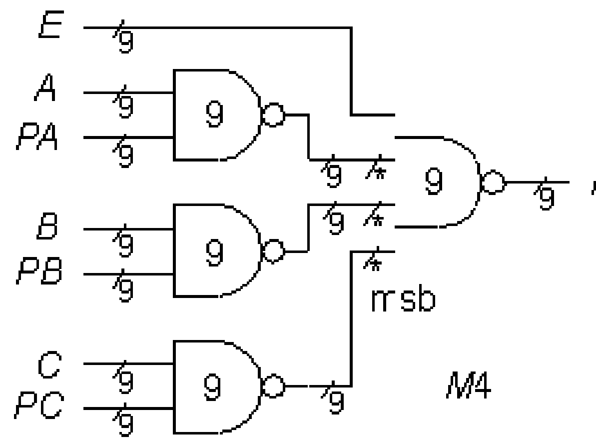

Fig A6: ISCAS-85 c432 M4

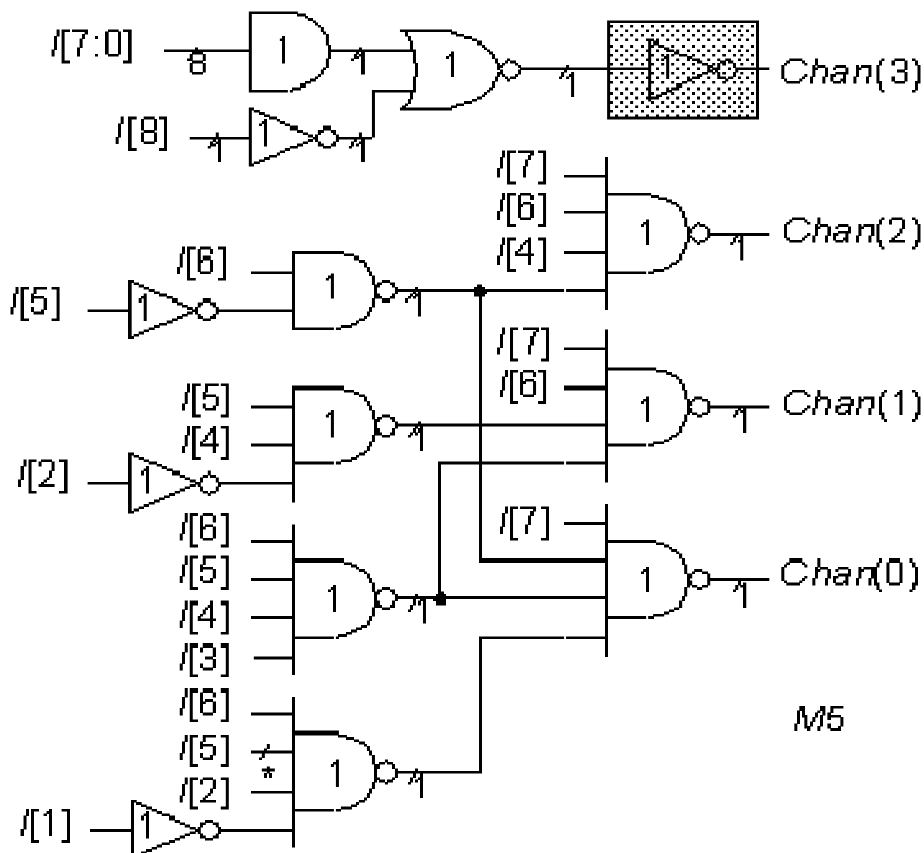

Fig A7: ISCAS-85 c432

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