DEVELOPMENT OF QA CELL FOR PDK VALIDATION AND ITS AUTOMATION

A Thesis submitted in partial fulfillment of the requirement for the Award of the Degree of

MASTER OF TECHNOLOGY

VLSI Design

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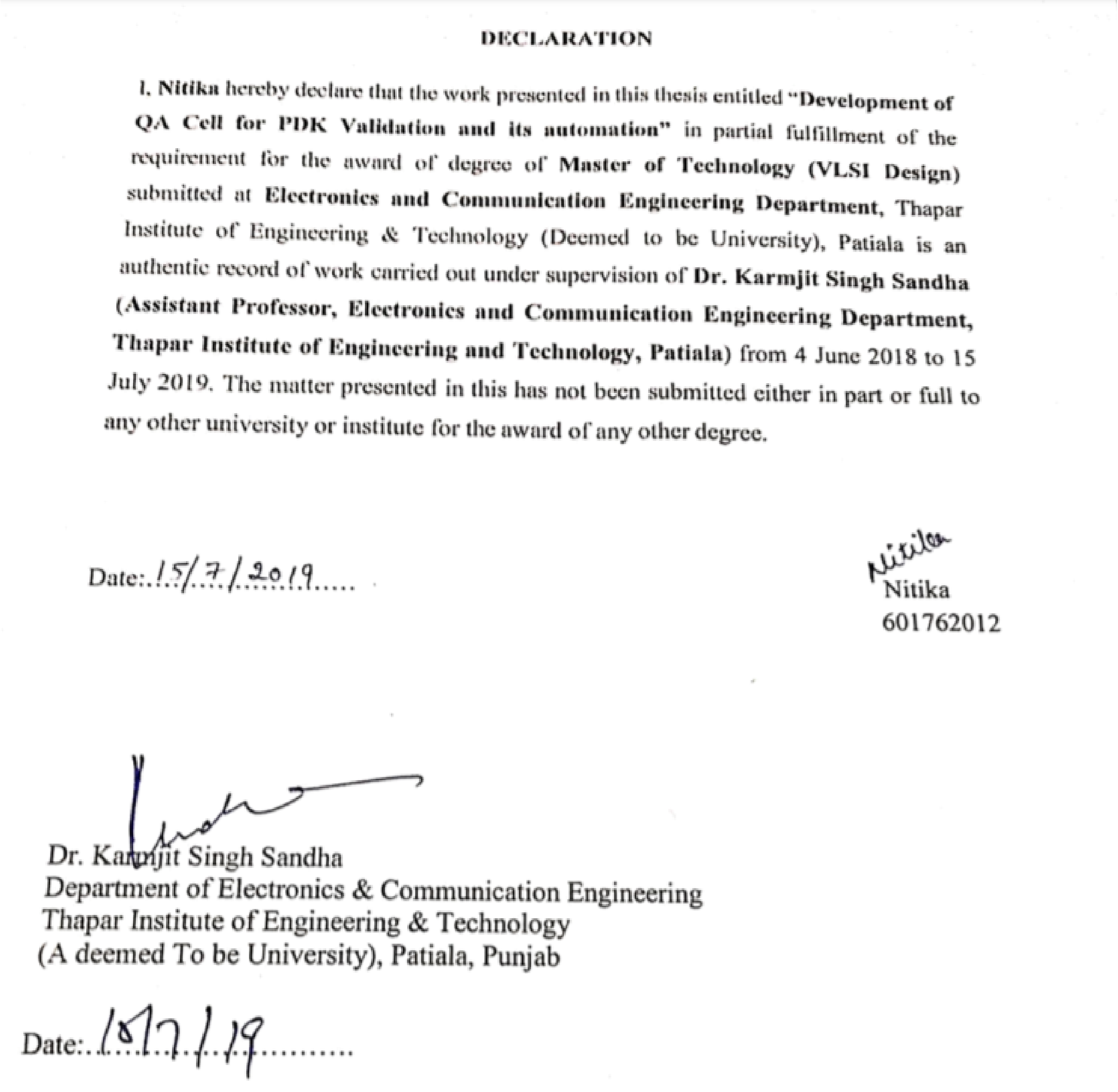

DECLARATION

I, **Nitika** hereby declare that the work presented in this thesis entitled **"Development of QA Cell for PDK Validation and its automation"** in partial fulfillment of the requirement for the award of degree of **Master of Technology (VLSI Design)** submitted at **Electronics and Communication Engineering Department**, Thapar Institute of Engineering & Technology (Deemed to be University), Patiala is an authentic record of work carried out under supervision of **Dr. Karmjit Singh Sandha (Assistant Professor, Electronics and Communication Engineering Department, Thapar Institute of Engineering and Technology, Patiala)** from 4 June 2018 to 15 July 2019. The matter presented in this has not been submitted either in part or full to any other university or institute for the award of any other degree.

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TO WHOMSOEVER IT MAY CONCERN

This is to certify that **NITIKA** has undergone internship in our **Technology & Design Platform** Group from 4th June 2018 to 20th May 2019. She has successfully completed her project on: **Development of QA cell for PDK Validation and Automation using Cadence SKILL.**

During her internship period, she was found to be sincere and professional in her conduct.

We wish her all the best in her future endeavours.

for **STMicroelectronics Pvt. Ltd.**

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The study has helped me to enhance my knowledge and give exposure to different domains related to my topic.

Nitika

ABSTRACT

Process Design Kit is that part of VLSI industry which deals with the process technology, i.e. masking procedures of different layers present or used particularly in that technology. Design kit means, an environment or a platform that is created for the users who uses these PDK's for developing their own designs. So, these design kits do not have any particular functionality. Rather the users which are designers of various fields use these PDK to test their design's functionality. Also this is important because this is the last step before the chip goes for manufacturing. Hence, it should be error free before it is being given for fabrication, else the chip will fail due to which the industries have to face huge loses. Hence PDK's are extremely important for the industry point of view. Now, designing of these PDK's are also done in frontend as well as in backend. In frontend the models are made and then these models are simulated using different simulators and finally they are cross checked and if discrepancies are found then they are fixed and again procedure repeats until all the discrepancies are resolved. Similarly, in backend, layouts are made for the various devices along with their test cases for the different DRC rules. These rules are validated and checked and if discrepancies are found then they are fixed and same procedure repeat itself. There are many other parameters which are to be taken care of like the LVS, DFM etc. PCell Validation also plays a significant role in PDK validation because PDK provides all tools and device libraries. Every device is simulated in order to check its working and also all the CDF parameters are verified. All the rules specified in DRC deck and in format of SVRF file. By getting basic knowledge of keywords helps in better understanding of verification process.

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LIST OF ABBREVIATIONS

ASIC	Application Specific Integrated Circuit
CAD	Computer Aided Design
PCell	Parametrized Cell
SVRF	Standard Verification Rule Format
PDK	Process Design Kit
CMP	Chemical Mechanical Polishing
DFM	Design For Manufacturability
DK	Design Kit
CMOS	Complementary Metal Oxide Semiconductor
EDA	Electronic Design Automation
LVS	Layout V/S Schematic
GDSII	Graphic Database System II
DRC	Design Rule Check
NVM	Non Volatile Memory
DRM	Design Rule Manual
QA	Quality Assurance

CHAPTER 1

INTRODUCTION

1.1 INTRODUCTION

With the Increase in demand for High Performance, Low Power and Low Area among microelectronic devices lead the fabrication process to go beyond ultra-deep sub-micron (UDSM) technologies such as 45nm, 32nm and so on. Similarly, design complexity is also increasing and foundries need to find a way to ensure the designers that the design would have better yield according to industrial requirement. To accomplish this target, designers have to provide solution at some standard level [1-4]. For standardization the first step was defining design rules for particular technology and then validating of these rules. Design rules defines the minimum requirement for manufacturing a particular process of a given foundry. The foundries use pre-characterized device models and the manufacturing constraints for fabless design success which are present in the Process Design Kit.

1.2 WHAT IS PROCESS DESIGN KIT?

Process Design Kit (PDK) is used in the semiconductor industry which contains files to model a fabrication process to design an integrated circuit. All the technology variations are specified in PDK and it is created by foundry [5]. The designers use this PDK for circuit designing. With increase in design complexity accuracy of PDK is of great importance for first time silicon success. The combination of all the pre-characterized device models and all the design constraints are very helpful for the designers and also PDK can be modified according to customer requirements. It will help in providing design solution in less time in order to meet market requirement. PDK has various categories to provide support to designers. Whenever any technology is released PDK plays significant role by validating all the flows like Back End flow, Front End flow and Digital flow.

In Backend Flow, there is complete DRC flow that will include Deck Development of PDK for Design rule checking[6-8]. In Frontend Flow we have to check the simulation of all the device models i.e. to check whether they are aligned with all simulators like Spectre, AMS and all the functionalities are reflected to designers who are using that particular PDK.

Figure 1.1 PDK Application

1.3 PDK COMPONENT

PDK is integration of many components listed below.

- DRC deck
- LVS Deck
- PEX deck
- Models for simulation.
- PDK Device library.
- EDA tools plugin files.
- Automation infrastructure for designers.

1.4 PDK FLOW

The important role played by PDK in Full Custom design flow is shown below:

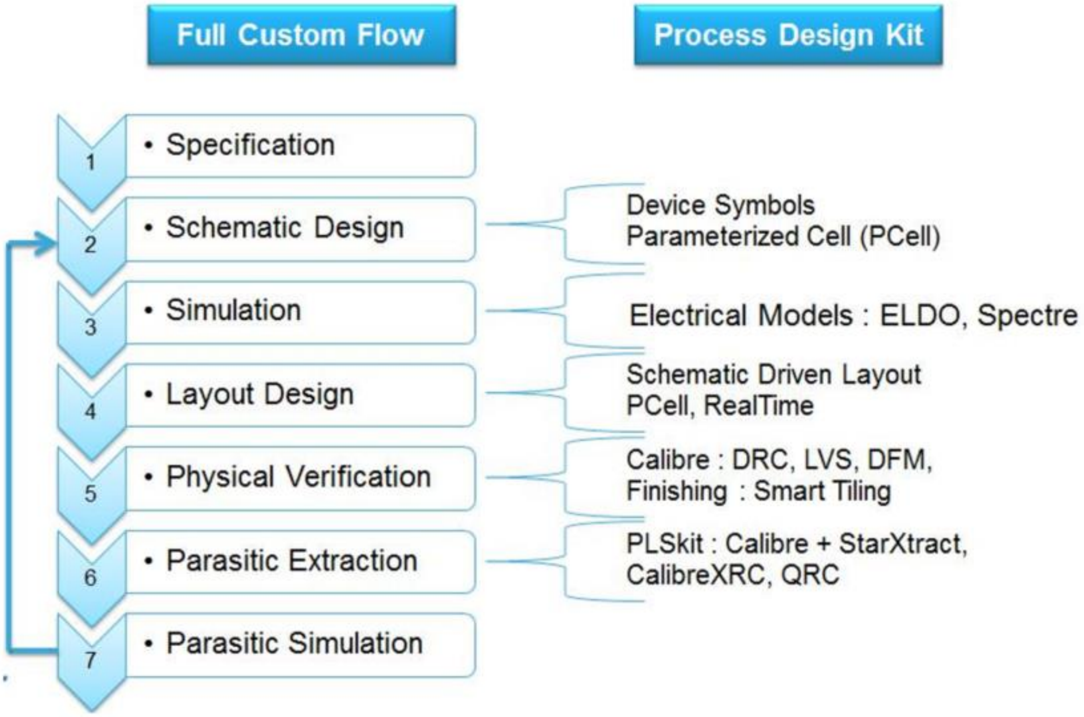


Figure 1.2 PDK Flow

As seen from the full custom Design Flow, PDK is required for each step i.e. From Schematic Entry to Tape out.

To start with schematic entry PDK contains Device symbols so that it is easy for the designer to draw the schematic and use all the parameters defined for particular model. PDK should work properly like if designer wants to annotate some operating points for simulation purpose. Next step is simulation design PDK offers various electrical models that can be used for simulation and to obtain various characteristics of the design for various options. Coming to the layout part PDK offers various

Parametrized Cell which plays a very important role while creating layout. PDK provides various layers depending upon the technology on which designer is working. Next step includes physical verification which is the most important step in the flow for which Design Rule Check (DRC) and Layout-Vs-Schematic (LVS) tools are required. These tools require set of instructions known as verification Decks which is contained in the PDK. Last step is of parasitic extraction for which PDK offers different tools which can be used to extract various R, L, C parasitic present in the layout which can be used as input for any static timing analyzer for calculating various delays[9]. Therefore, the quality of PDK, features, tool, support and capabilities decides the time to market and yield of the chip. The PDK quality also decide the first time silicon success for any chip which in turn can save lot of money for the industry.

1.5 PDK GROUP ACTIVITIES

There are various activities which are carried out in our group. Following are activities that take place in PDK Department

1.5.1 Front-End validation

In this step ,Front end validation takes place. It includes validation of all the tools , device libraries and technology libraries working. All the specified tools in the environment setup must be compatible to the PDK version. Like for validating all the devices there is top cell creation concept which includes all the blocks like MOSFET block, capacitor block, resistor block, diode bock, RF devices block and many more according to categories provided by foundry[10-12]. These blocks are combined together and simulated using different simulation tools which support that PDK and there netlisting is done to ensure that all the model name are interpreted correctly and various flow like LPE, LVS Flow and QRC Flow. By doing Post layout netlisting simulation is carried out and again all the warnings are checked.

1.5.2 Back-End Validation

In this step all the back end validation tasks are carried out. Back end tasks include DRC, Smart Tiling, LVS Deck verification. For DRC Deck validation different test cases are created and verified whether they are aligned with SVRF file. Because designer use all the devices for layout designing there should not be any problem. All the validation tasks are very important.

1.5.3 PCell Development and Validation

A parametrized cell or PCell is a programmable design entity. Whenever designer is creating layout there is need of multiple instance for default values and for modified values of single cell. So PCell is used to create multiple instances where designer can vary several parameters for single PCell for example with different width, different number of fingers etc.

PCell is a powerful tool in design methodology combined with Relative Object Design (ROD). Using the concept of ROD one can define technology independent cells that are customizable to any application. Basically, ROD is a set of high level SKILL functions for defining complex layout objects and persistent spatial relationships between them.

To increase the productivity of design Parameterized Cells are developed. To optimize this gain PCell validation plays important role from designing point of view. Exhaustive PCell validation is done to check reliability .

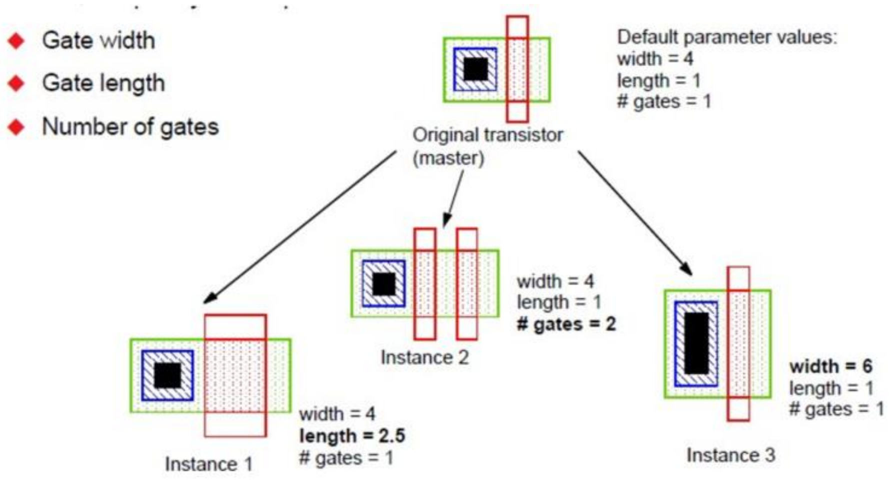


Figure 1.3 PCell Instances [13]

1.5.4 SignOff and Support to Various Flows

In the automated design of integrated circuits, signoff (also written as sign- off) checks are the collective name given to a series of verification steps that must pass before the design can be taped out. This implies an iterative process involving incremental fixes across the board in one or more check type and retesting the design. There are two types of sign-offs are there, namely Front-end sign-off and Back-end sign-off. After back-end sign-off the chip will go to fabrication.

Support System in PDK:-

An Online Ticketing System has been incorporated with PDK Greater Noida Group for Internal and External Use. There are several Issues related to as follows:

- Physical Verification Issues.
- Layout Related Issues in Reference to DRC/LVS Rules.
- Environment Launch Related Issues
- SOC Support(Mostly Used in Calibre DESIGNrev)
- Calibre Related Issues with respect to Design Kits.

1.5.5 Full Custom Design Flow

The back-end design of the ASIC Flow can be divided into ASIC-style flow and full- custom flow. In all there are 4 different types ,with each type having different possibilities for automation. Full custom layout which is driven by area limitations, such type of layout is made of repeated complex structures like adders, multipliers, decoders, sense amplifiers etc. They have tight control over area and signal noise. Such type of layout is called as ”Datapath layout”.

Full-custom layout which needs high performance or analog circuitry design, such types of layout are useful for high speed requirement circuits such as PLL, digital to analog converters or analog to digital converters (DACs/ADCs),ESD circuits, RF speed requirements, such type of layout are called as ”analog layout”

Full-custom layout that requires greater attention to area and performance than the full digital (ASIC) flow, but has less stringent requirements for speed and less need for control over device-level layout than Datapath or analog layout: This type of layout is called ”custom digital layout.” Full-custom layout for cell development: Cells are the basic building blocks that are part of the components that share common rules, functionality and performance. Each of the above mentioned design style should be used in accordance with the requirement of chip under development, the tradeoffs between the style focuses on area and power.

1.5.6 Layout Finishing

Layout finishing is performed as the last step, once the GDS is DRC clean, except for density violations. Smart Tiling is an automated process to avoid Design for Manufacturing (DFM) rules.it is used to fill layout shapes at the System on Chip (SoC) level of the design.

Metal fills or dummies are used to reduce planarity issues and Critical Dimension (CD) uniformity issues on the chip, that can occur during Chemical Mechanical Polishing (CMP) process of IC fabrication. They also provide mechanical support to the IC

Smart tiling is performed on the layout Smart Tiling fills the layout with the extra dummies or fillers so as to reduce density violations.

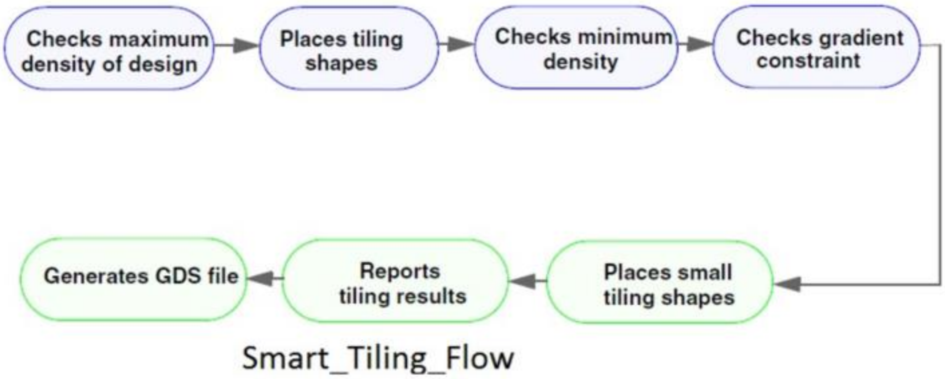


Figure 1.4 Smart Tiling Flow

CHAPTER 2

LITERATURE SURVEY

System and Framework for QA of Process Design Kits [3]

- M. C. Scott, M. O. Peralta, J. D. Carothers

The quality of electronic design automation (EDA) tools and integration of libraries plays important role in designing. If any error is found at any stage that can cause critical fault. And designer is not aware about these as they blindly on the design kit provided with all libraries and tools. As the technology is shrinking with increase in complexity it is very important that there should be no library errors or any issue with design tool. In this paper they have implemented systematic means for qualification of design kit at various stages. They have introduced a tool called "RegMan" i.e. regression manager for validation of verification tools. This tool is used to run regression sets for simulations to validate various device models and their libraries. This is generalized for any design kit and for any set of design rules for physical verification. This tool helps to analyze extraction tool accuracy. It validates the set of rules provided to the tool for particular process. The extracted netlist from LPE is also validated in order to check further errors. This aggressive testing at every step help to measure the accuracy of design kit and its libraries. Usually for the testing of PDK validation engineers run different flows manually but this tool can enhance the validation process and provides systematic framework.

An Approach for A Comprehensive QA methodology for the PDKs[4]

- Sridhar Joshi, Ravi Perumal, Kamesh Gadepally, Mark Young

This paper discuss about process of achieving high quality PDK. It is well known that the "time to market" concern has redefined the designers' approach, leaving very little margin for error. First Time Silicon is the mantra of all the organizations. Designers do not start from scratch for a particular PDK instead they have some standard IPs to include in design cycle. First time silicon success has now become a crucial necessity. In this paper author has introduced different testing structures that includes three sub sections, unit testing structure, division of rules and then creation of different test cases third one is Post Mortem that creates test case for every error reported and validate PDK accordingly. Unit testing structure includes creation of unit test cases for each rule in PDK an ensure that if any rule is changed it will not affect the entire PDK validation. Prioritizing each category will create balance between test structures. All the testcases should be modular so that they can be modified according to situation demands. Validation team run all the test cases that covers almost all the possible scenarios and create special test case for new bug. The author has suggested balanced approach to quality Assurance for Process Design Kit. It suggests to find pattern of error from starting and estimating those patterns to avoid further occurrences. In this way a modular and portable approach is used to reduce turnaround time (TAT).

A Complete Process Design Kit Verification Flow and Platform for 28nm Technology and Beyond[5]

- Yanfeng Li , Miao Li , Waisum Wong

In this paper verification flow and platform to qualify the advanced PDKs is demonstrated which address layout dependent effects. It is successfully implemented on 28nm technology. All the test structures verify layout dependent components. Earlier Quality Assurance of PDK focus on individual components and carried out by various groups like device modelling team handle SPICE model QA. To check layout dependent effect running SPICE simulation is not enough and new methodologies for verification need to be developed. It was observed that number of issues are increasing due to inaccuracy in LPE decks and required to be verified extensively. During execution layout is generated by Skill code and different parameters are passed to generate test layouts. Then this generated layouts are then passed to layout extraction and SPICE simulation tool. The results are collected by automatic data analysis mechanism to ensure of circuit/device scales physically on varying layout parameters. This paper presents a new PDK verification flow with focus on layout-dependent model verification and LPE verification. The flow was successfully applied to SMIC 28nm process.

A robust and automated methodology for LVS quality assurance[6]

- Ahmed Mohy, Mohamed Abul Makarem

This paper highlights the importance of Layout Versus Schematic (LVS) check and its rule file. Layout Versus Schematic (LVS) is important step in layout verification and writing of LVS Rule file is considered a difficult in order to provide verification tool proper understanding of layout. However achieving hundred percent accuracy is not possible in first attempt so QA techniques are required on LVS rule file. The author has suggested a new approach which is based on individually checking LVS rule file that extracts single device and then its ability to extract netlist and whole circuit. There are other single device checks like truth table check and circuit level check. In this check mask levels are added or removed from the test cases to ensure the absence and presence of prohibited/mandatory layers for each device. Using multiple instantiations of each device by creating test cases for pin swapping ability and series/parallel reduction with different topologies. In circuit level testing devices are picked up randomly and simulated. This will create a scenario to check working after LVS run and comparing netlist generated from the network for different devices connected in different configuration. This algorithm was implemented for different technologies. This technique helps to provide error free LVS rule deck in short time period and save the designers from hidden errors.

Development of parameterized cell using Cadence Virtuoso[7,8]

- Vadim Borisov

In this paper significance of CAD system Cadence Virtuoso in designing is described. The concept of parameterized cell of the transistor is discussed in it. This parameterized cells helps in reducing design time. There are two ways to for parameterized cell creation one is writing a SKILL code and second is to create graphically using menu Pcell. This parameterized creation helps in unification of all transistors. Because if any designer try to create transistors layer by layer then there are chances of inequalities in dimensions. Using parameterized cells we can create any number of instances by changing certain parameters. A parameterized cell is a programmable/graphical cell that allows you to customize instances in layout designing. Whenever changes are applied to master they are reflected in instances. Designer can changes width, length , number of fingers in transistors using Pcell. In case of Menu Pcell there are various options are present like the Virtuoso parameterized cell reference point commands. Developers should implement all the parameters that can be used to create multiple instances and reduce database.

STMicroelectronics. Design Rule Manual, 2017[9]

DRM is a document provided by foundry which contains all the information about the technology like layer details, metal stacking, DRC rules, etc. Design Rule Manual contains the rule description including its values according to the technology used. Test cases should be built with all possible conditions. For example, the distance or the space rules, must be checked for cases like single point touch, multi point touch, any angle, overlap condition. QA Cell are created for different types of rules in DRM. For example, rules related to FEOL layers, Rules related to BEOL Layers, Robust design rules like density rules, Latch up rules, Antenna rules. Rules related to voltage management.

The importance of layout density control in semiconductor manufacturing[10]

- Vivek Singh

On increasing demands of industry for high performance IC products. As die size is decreasing then within die variations are increasing. Process designer needs to take care of all these variations and try to detect the defects as early as possible. Density design rules plays a very important role in chip fabrication and those rules should be validated properly. The complexity of density rules is also increasing like in DRM there are maximum density rules and minimum density rules. The percentage of density of particular layer is defined and validation engineer have to create all the possible test cases for those rules. If these rules are violated there are chances of chip failure. For example in Chemical-Mechanical Polishing process if density requirements were not met properly then there are chances of removal of those less density layers that can affect the functionality of complete chip. Designers have developed a new concept of smart tiling where dummy layers are added to meet density percentage specifications in order to avoid density violations. Dummy layers are some extra layers which are added but they does not create any impact on functionality of the device. Adding dummy layers reduces within die variations and it improves uniformity in chip fabrication.

CHAPTER 3

RESEARCH GAPS

The main objective of QA Cell development is to validate the DRC Deck i.e. to check whether the rules that are coded in SVRF file are completely aligned with the rules defined in Design Rule Manual.

Validation of DRC deck has significance in designing integrated circuits. When designers are working on some circuit, they rely on the PDK provided and that should be of high quality[13]. This task emphasis on detecting defects before they get into final manufacturing and addresses three problems:

I. How to verify DRC decks in order to ensure that complex design rule description is specified correctly and also its accurate evaluation ?
II. How to ensure design rule consistency and to avoid potential conflicts between different design rules?
III. How to check the functionality of devices present in Process Design Kit library?

3.1 OBJECTIVES

1. To automate the flow of QA Cell development for generic design rules.
2. To exhaustively check all the possible test cases so that there are minimal chances of chip failure.
3. To cover all the complex rules i.e. Robust Design Rules(Antenna Rules, Density Rules, Latch-up Rules) that will ensure chip reliability.
4. To automate the flow of creation of density rules.
5. To study the development of PCell and its validation which are provided by PDK department to designers.
6. To understand how the SVRF file is coded and implementation of basic keywords used in DRC deck.

CHAPTER 4

VALIDATION OF PDK

4.1 FORMAL QUALITY ASSURANCE (FQA)

Formal quality assurance is any systematic process used to check whether the product or service being developed is meeting specified requirements. A formal quality assurance system of the product increases the chance of first time success of the products which in turn increases the customer confidence and company's credibility. By improving work processes and efficiency, and enable a company to better compete with others. It emphasizes on catching the defects before they get into the final chip/product.

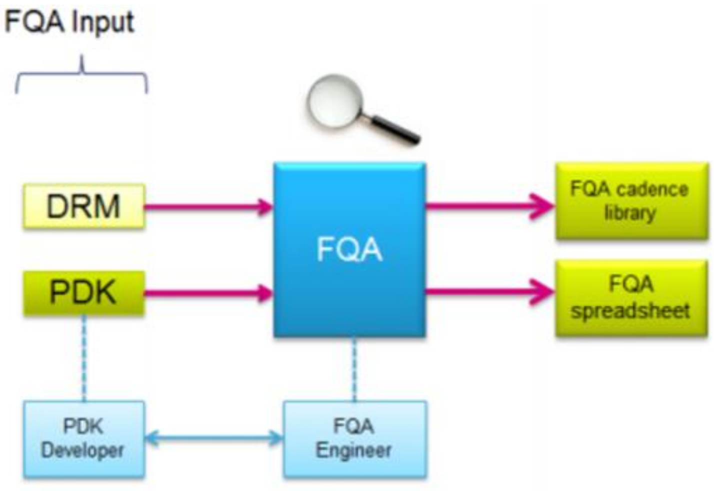


Figure 4.1 FQA Flow chart

4.1.1 Quality Assurance Cell

Quality Assurance Cells are made with respect to the Design rules specified in the DRM. Quality is ensured by developing the test cases for the rules which are mentioned in design rule manual of the specified technology for various possible cases[14]. To minimize the risk and release higher quality PDK, FQA team create QA cells for each design rule mentioned in the DRM.

QA Cell are created for different types of rules in DRM. For example, rules related to FEOL layers, Rules related to BEOL Layers, Robust design rules like density rules, Latch up rules, Antenna rules. Rules related to voltage management.

These test cases are layout structures drawn with different possibilities that a layout engineer may come across, that manifest both violating (fail) and legal (pass) configurations. The developed DRC code is then run on these layout test cases and the error should be flagged in on the bad test case and not on Good test case. If any errors which are highlighted on Good Test case, developer needs to rewrite its code again or there might be some problem in QA Cell.

4.2 PHYSICAL VERIFICATION COMPONENTS

Physical verification is performed after physical Design Flow. It is one of the important step before sending the final GDS to foundry for chip fabrication.it includes testing of the layout for various rules in accordance to foundry. It consists of

1.DRC

2.LVS

3.Parasitic extraction

4.2.1 Design Rule Check (DRC)

Design Rule Check (DRC) is the part of EDA tool in which DRC deck is written and it checks whether the layout satisfies the rules recommended by the Foundry for fault free production of the chips and to increase the reliability of chip. One can understand that layout is the drawing version of the photo mask which is used in the manufacturing process. Layout cannot be perfectly reproduced on wafer as the technology is shrinking day by day due to the limitations of hardware tools. So the foundry people comes with the specific set of rules these rules are known as Design rules. Every foundry set various constraints in converting layout to final fabricated product. These rules are different for different technologies and depends on the size of the wafer. Complexity of these rules is increasing with the shrinkage of technology node[15]. These rules are documented in Design Rule Manual (DRM). The set of rules for a particular process is referred to as a runset, rule deck, or just a deck. DRC is a very computationally complex task it may take time to check DRC according to the design complexity and tool functionality. Design rule checking is considered as a major step before sending the GDS to the fabrication lab. It also involves LVS check, ERC (Electric rule check), Antenna check and density checks. To achieve a high yield is the main objective of design rule checking (DRC) along with the reliable working of the design. If any design rule is violated, then that can cause manufacturing defect. To order to improve die yields, DRC has evolved from simple measurement and Boolean checks, to more complex rules that insert new features, modify existing features and check the entire design for process limitations such as layer density, antenna violations while the design rule checks whether the design can be manufactured properly or not ,they do not validate the functionality of the Design.

4.2.2 Layout versus Schematic (LVS)

This check is used to verify whether the drawn layout is in correspondence with the schematic. Basically it compares the netlist generated from schematic with the one generated from layout. In LVS number of pins, instances, net connections present in layout are compared with schematic.

It involves three steps:

- Extraction: In this step, recognition of devices takes place based on the layer which are used to draw it. There is particular mechanism to detect the type of devices

- Reduction: In this step, it combines the components which are extracted in series and parallel form and generates a netlist similarly in the schematic.
- Comparison: In this comparison is done between layout netlist and schematic netlist, if they match LVS check is passed.

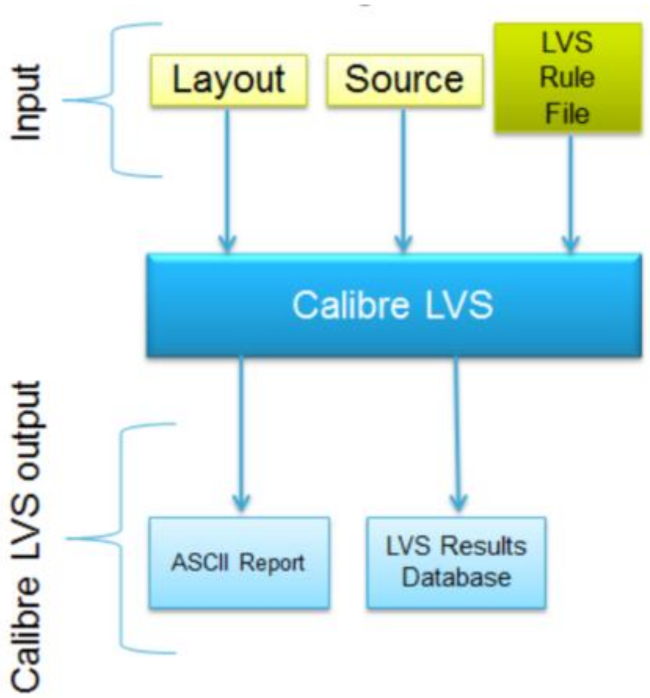


Figure 4.2 LVS check Flow

4.2.3. Parasitic extraction

Parasitic extraction is used to calculate effects of parasitic in the required wiring interconnects and designing devices. The parasitic components include parasitic resistances, parasitic capacitances and parasitic inductances[16]. The purpose behind the extraction is to create the analog model of circuit which is accurate in order to get detailed simulations including analog and digital circuit responses. The digital response provide database for timing analysis ,power analysis and simulation time. The analog response will give information about the effect of parasitic elements in the functionality of the circuit.

4.3 INFORMATION REQUIRED FOR CREATION OF TESTCASES:

4.3.1 Design Rule Manual(DRM): DRM is a document provided by foundry which contains all the information about the technology like layer details, metal stacking, DRC rules, etc. Design Rule Manual contains the rule description including its values according to the technology used. Test cases should be built with all possible conditions. For example, the distance or the space rules, must be checked for cases like single point touch, multi point touch, any angle, overlap condition.

4.3.2 Design rule labels and Geometry Terminology

Definitions & Shape

A shape in layer A is an object in layer A with a non-null area. It is used in opposition to an edge, a text or a property in the stream file under check (GDSII or OASIS).

(a) Inner/Outer vertex

Considering the angle in between the 2 adjacent edges of a vertex, and measuring it outside of the shape this vertex is belonging to, a vertex is considered an inner vertex when this angle is smaller than 180 degree and an outer vertex when this angle is greater than 180 degree.

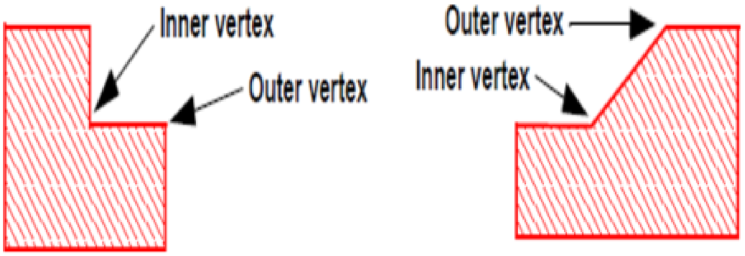


Figure 4.3 Inner/Outer Vertex [9]

(b) Acute/Obtuse Angle

An acute angle is an angle smaller than the orthogonal angle, therefore creating a singularity in terms of width or space. These angles are typically prohibited in a design. An Obtuse angle is an angle larger than the orthogonal angle, therefore not creating a singularity in terms of width or space. These are typically the only non-orthogonal angles allowed in a design on physical shapes.

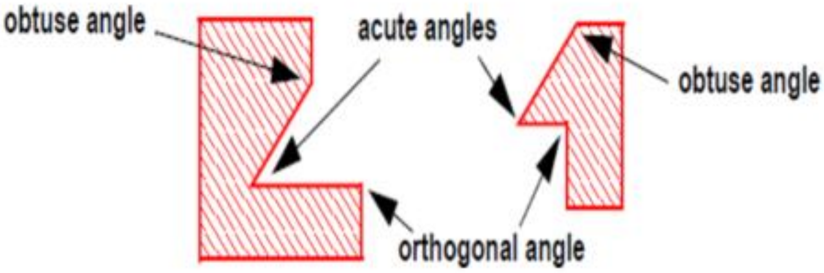


Figure 4.4 Acute/Obtuse Angle [9]

(c) Width & Length

For a rectangle, the width is the smallest dimension of the shape, i;e. the smallest edge length of the edges forming the rectangle. Therefore, the length is the other one, i.e. the longest one.

(d) Maximum Width

For any shape, the width notion is complex. The criterion width < a is con- sidered fulfilled as soon as the shape disappears in a downsizing operation with the value of a/2.

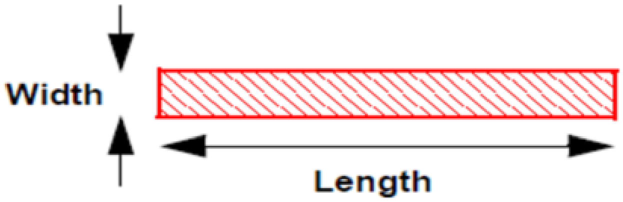


Figure 4.5 Width/Length [9]

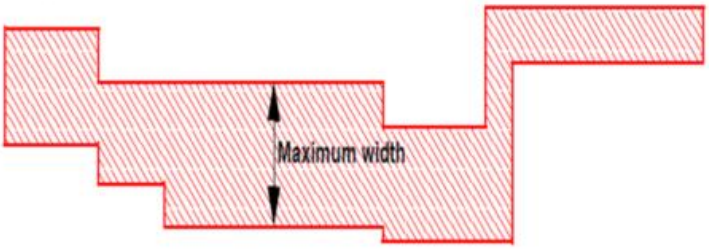


Figure 4.6 Maximum Width [9]

(e) Gate length/width

The Gate length of a transistor is the length of the channel from the device prospective. It is therefore the distance in between internal Poly edges, measured over Active. The Gate width of a transistor is the width of the channel from the device prospective. It is therefore the distance in between internal Active edges, measured over Poly.

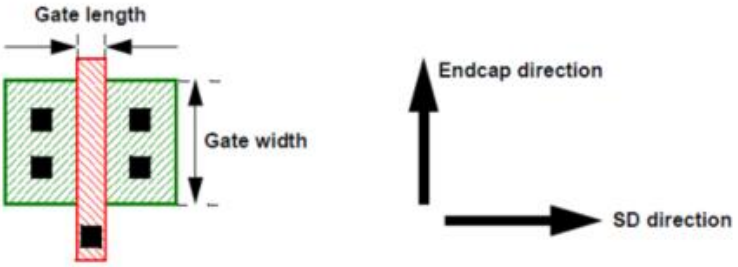


Figure 4.7 Gate Length/Width [9]

Dimensional Unitary Operations

1. Width: Distance between internal boundaries of a shape in the same layer

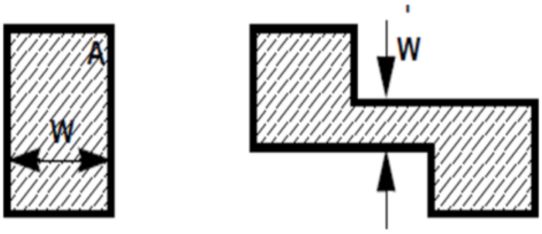


Figure 4.8 Width of Polygon [9]

2. Area**:** Geometrical area of a shape of layer

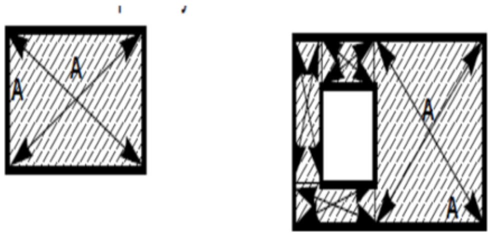


Figure 4.9 Area of Polygon [9]

3. Space**:** Distance between external boundaries of shapes. Applies also to edges from the same shape, unless specified. As Shown in Below Figure:

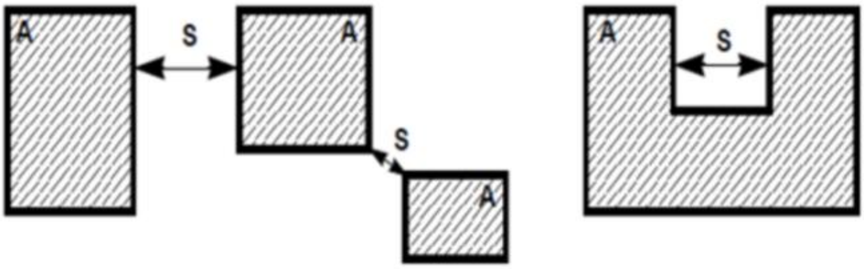


Figure 4.10 Space of Polygon [9]

Dimensional Binary Operations

(a) A Distance to B

Distance between external boundaries of two shapes of different layers (A and B). A intersection with B is still authorized, unless specified

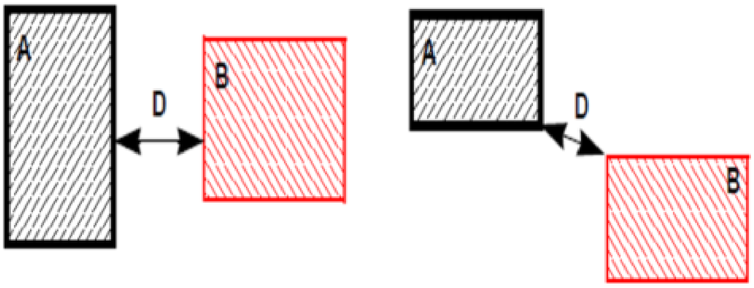


Figure 4.11 A Distance to B [9]

(b) A Overlap of B

Distance between the internal boundary of A and the internal boundary of B, as long as there is no other A nor B edge in between the measured edge pair.

    1. A and B must not necessarily interact with each other, still.
    2. A overlaps B if A .and. B is having a non-null area.

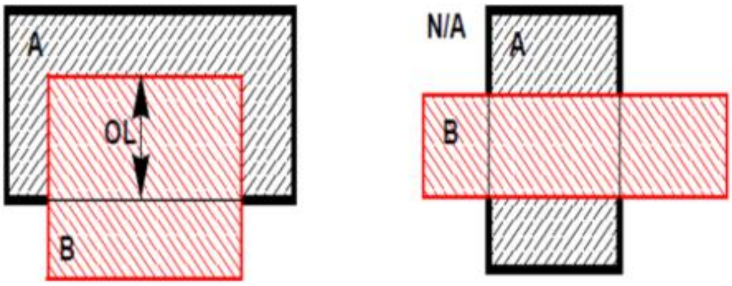


Figure 4.12 A overlap of B [9]

(c) A Extension on B

Distance between internal boundary of A and external boundary of B. B extending outside A is still authorized.

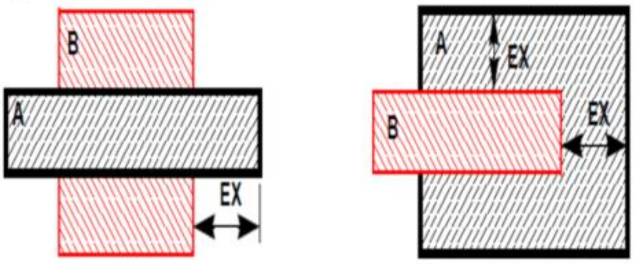


Figure 4.13 A Extension on B [9]

(d) A Enclosure of B

Distance between internal boundary of A and external boundary of B, with the additional requirement that B must be completely included in A. B not covered by A still authorized, unless specified B enclosure by A

Distance between the internal boundary of A and the external boundary of B. B must be completely included in A. (B Enclosure by A = A Enclosure by B)

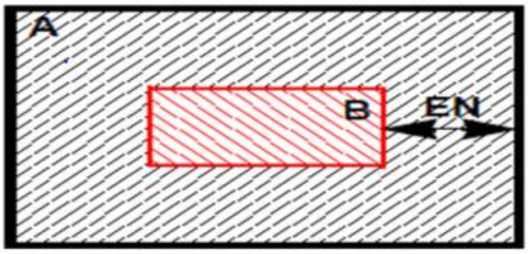


Figure 4.14 A Enclosure B [9]

Non-Dimensional Binary Operations

(e) A Interact B

A interacts with B, if they have an edge or an area in common (i.e. if they overlap, or if they touch along an edge). A .interact. B returns A if A interacts B.

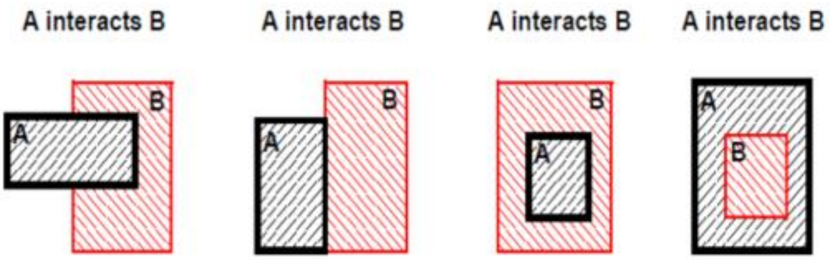


Figure 4.15 A Interact B [9]

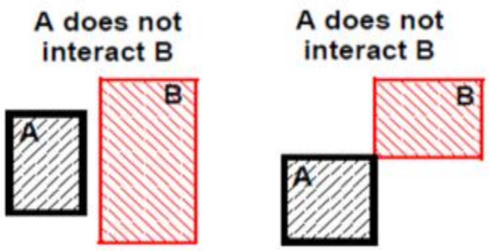


Figure 4.16 A does not Interact B [9]

(f) A Intersect B

A intersects B, if the Boolean operation A .and. B does return a shape with area > 0. A .intersect. B returns A if A intersects B.

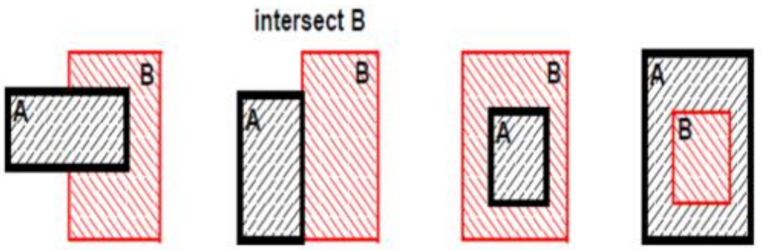


Figure 4.17 A Intersect B [9]

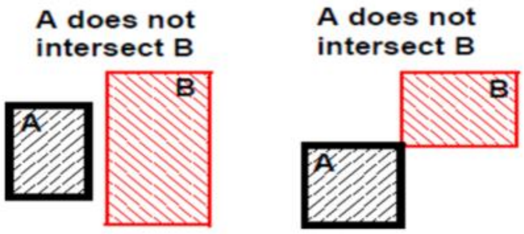


Figure 4.18 A does not Intersect B [9]

(g) A Cut B

A cuts B if A shares parts but not all of its area with B, i.e. if A overlaps B and A overlaps .not. B A .cut. B returns A if A cuts B.

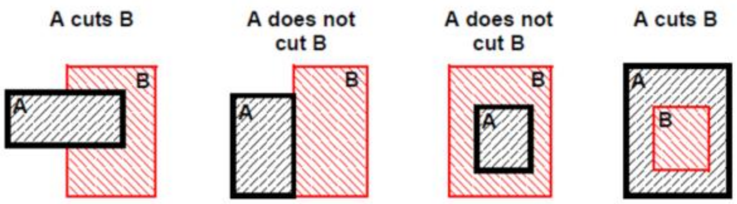


Figure 4.19 A Cut B [9]

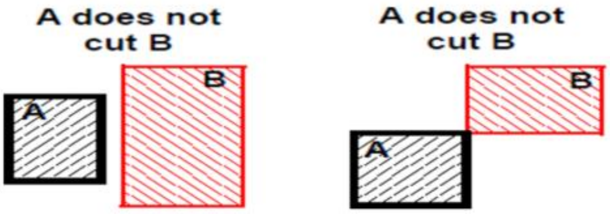


Figure 4.20 A does not Cut B [9]

(h) A Straddle B

A straddles B if A is crossing over B with A extending on B on both sides and B extending on A on both sides as well.

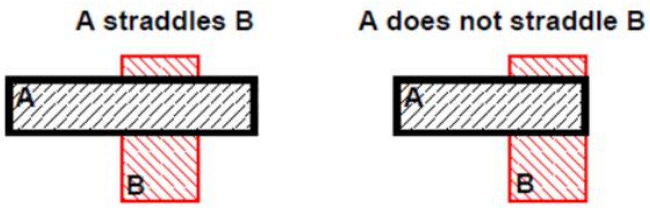


Figure 4.21 A Straddle B [9]

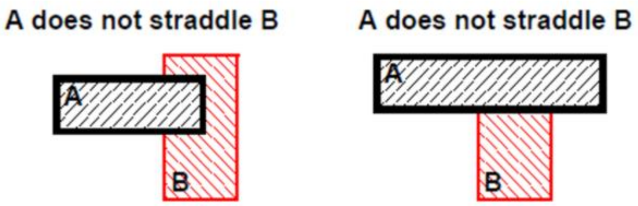


Figure 4.22 A does not Straddle B [9]

4.3.3 Layout Design Rules

Layout Design Rules are divided into various categories.

(a) General Data Design Rules

General Data Design Rules concerns all the layers present in layer map file of DRC DECK. All the standard layout design should be of 0.005 micron for all the levels. Off-Grid design data is not allowed. Only vertical and horizontal geometries are allowed. Any angle different from 0 and 90 degrees are forbidden except where 45 degree or other angles are explicitly allowed.

(b) Process Identification Marker Design Rules

The product designs must contain markers to identify the baseline process and the metallization choice. This is required for the automated tape out procedure.

(c) Die Size Restrictions Design Rules

Physical surface area size is referred as Die size on the wafer. It is the pitch of the scribe street (distance between the median lines of two adjacent scribe streets).The three most important contributing factors to die size are the process technology used, the circuit size in microns and the design of the device itself.

Processing of a semiconductor wafer is divided into different regimes or groups of steps. These regimes are commonly referred to as Front-End Process or front-end-of-the-line (FEOL), middle-of-the-line (MOL) and Back- End Process or back-end-of-the-line (BEOL).

Front-End Process Design Rules

The front-end process is the first part of IC fabrication where the individual devices (capacitors, resistors, transistors, etc.) are patterned in the semiconductor. FE process covers almost all the layers (but not including) the deposition of metal interconnects layers.

FE contains all processes of CMOS fabrication needed to form fully isolated CMOS elements:

1. Selecting the type of wafer to be used.
2. Chemical-mechanical planarization and cleaning of the wafer.
3. Shallow trench isolation (STI)
4. Well formation
5. Source and drain module formation
6. Gate module formation

Typical Front-End Process contains the following layers:

(a) Gate Oxide and Diffusion (OD)

(b) NWELL Design Rules (NW)

(c) Deep NWELL Design Rules(DNW)

The purpose of this layer is to get PW isolated from substrate: DNW provides vertical isolation; an NW guard ring provides lateral isolation. The complete electrical isolation is achieved by DNW with NW guard ring. The DNW should also be drawn under NW for better latch-up immunity.

(d) VTHN Design Rules(HVT NMOS)

The purpose of the VTHN layer is to allow the additional implants necessary for HVT NMOS transistors.

(e) VTHP Design Rules(HVT PMOS)

The purpose of the VTHP layer is to allow the additional implants necessary for HVT PMOS transistors.

(f) Thick Oxide Device OD-XX Design Rules

The purpose of this layer is to get thick gate oxide MOS transistors.

Gate oxide and implants

Front-end surface engineering is followed patterning of the gate, by growth of the gate dielectric (traditionally silicon dioxide), patterning of the drain and source regions, and subsequent implantation or diffusion of dopants to obtain the desired electrical properties[15]. In Dynamic Random Access Memory (DRAM) devices, storage capacitors are also fabricated at this time typically stacked above the access transistor.

g) NPLUS Design Rules(NP)

h) PPLUS Design Rules(PP)

i) POLY Design Rules(PO)

j) Resist Protection Oxide Design Rules(RPO): Inside the feature of this layer, there is no silicidation of the silicon (substrate mono silicon or any deposited amorphous or poly crystalline silicon). Outside this feature, all sources, drains and poly are silicided. Due to the doping of the PO by the source/drain implants, the designer must avoid forming N+/P+ diodes in the unsilicided PO or OD features.

Back-End Process Design Rules

The back-end process is the second part of IC fabrication where the individual devices (capacitor, resistors, transistors, etc.) are interconnected with wiring on the wafer, the metallization layer.

Common metals are Copper interconnect and Aluminum interconnect. BE generally begins when the first layer of metal is deposited on the wafer[16]. BEOL includes contacts, insulating layers (dielectrics), metal levels, and bonding sites for chip-to-package connections.

After the last Front end step isolation of transistors (without any wires) on wafer is done. In BE part of fabrication stage interconnect wires, contacts (pads), vias and dielectric structures are formed. With the advancement of technology number of metal layers is also increasing up to 10 layers.

The top-most layers of a chip have thickest and most widely dissevered metal layers, which make the wires on those layers, most minuscule RC time delay and have the least resistance so they are utilized for clock distribution and power distribution. The bottom-most metal layers of the chip, most proximate to the transistors, have thin, narrow, tightly-packed wires, used only for local interconnect. Integrating layers can potentially ameliorate performance, but integrating layers additionally reduces yield and increases cost of manufacturing.

Chips with a single metal layer typically utilize the polysilicon layer to "jump across" when one signal needs to cross another signal.

Steps of the BE:

1. Silicidation of the polysilicon region and source/drain region.
2. Adding a dielectric (first, lower layer is Pre-Metal dielectric, PMD to isolate metal from silicon and polysilicon), CMP processing it
3. Make holes in PMD, create contacts in them.
4. Addition of metal layer 1
5. Addition of a second dielectric (this time it is Intra-Metal dielectric)
6. Connect lower metal with higher metal by making vias through dielectric. Vias filled by Metal CVD process.
7. Repeat steps 4-6 for all the metal layers.
8. Finally addition of passivation layer to protect the microchip Typical Back-End Process contains the following layers:

    a) Contact Design Rules(CO)

    b) Metal Design Rules

    c) Via Design Rules

(f) Far-Back-End Process Design Rules

Far-Back-End is a sub-regime of BEOL. A semiconductor device having protected far back end process structures includes a substrate, a front end of the line (FEOL) stack formed on the sub- strate, a BEOL stack formed over the FEOL stack.

An encapsulation boundary is conformally formed over the BEOL stack covering horizontal surfaces and sidewalls of extended openings which ex- tend into at least the BEOL stack to a stop position to protect at least a portion of the BEOL stack.

Typical Far-Back-End Process contains the following layers:

a) Encapsulation Opening - Copper Bondpad (CB) Design Rules

- CB defines an opening in the glass encapsulation to provide access to the top copper metal, i.e. CB is a via between Mtop and AP.

b) Aluminum Cap (AP) Design Rules

- AP defines the Aluminum cap

c) Nitride Passivation (CB2) Design Rules

- CB2 defines an opening in final nitride passivation

Device Specific Design Rules

(a) Resistors:

Resistors can be built in the following flavors:

- Either PO or OD, according to the layer in which they are fabricated.
- Either N+ or P+, as to the doping type.
- Either unsilicided or silicided, relying in the presence or not of the silicidation protection layer RPO.

As for the dimensions, the drawn width is defined by the PO/OD width. The drawn length is defined as:

- The distance between the CO for silicided resistors
- The length of the resulting shape of the intersection of the RPO layer and the PO/OD for unsilicided resistors.
- For spice accuracy:

1. Do not dog-bone the resistor at the transition from head to body.
2. Input PO/OD resistor among dense pattern.
3. Draw MKR;RH line-on-line with NP or PP that covers resistor.

RES.W.1 : Width of unsilicided OD or PO;RESISTOR 0.2

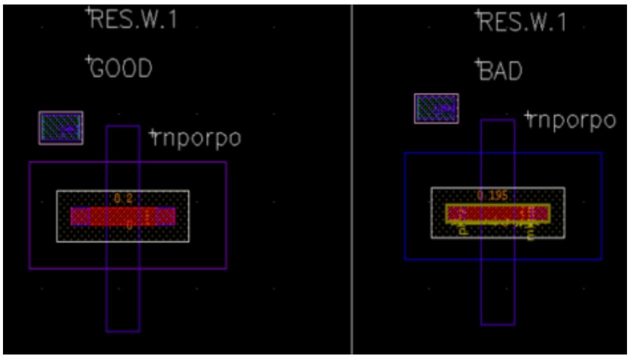


Figure 4.23 QA Cell for Resistor

4.3.4 Robust Design Rules

(a) Understanding the importance of layout Density control and Development of Density Rule QA cells.

Density requirements have to be strictly followed in order to avoid any destruction of chip during the CMP (Chemical Mechanical planarization) process which is done in order to make chips planar[17]. It has been observed that the polishing rate is proportional to the pressure that the polishing pad exerts at the point of contact between the pad and the topographically uneven film being polished. This non uniformity can be the reason for local defocusing in further lithography steps, which in turn results in flawed patterning due to the reduced process margins. The possible method to overcome this cascading chain of failures and variations is to minimize the variation in layout density with the addition of dummy layers in relatively “open” areas.

These density rules are checked either locally i.e. local to specific part of the chip or globally on the whole chip. For that purpose stepping distance is used which is half the window size. if we use smaller stepping size then the margin for error is extremely low and it also avoids problem during IP placement.

The density rules are defined in the DRM for density check For example

OD.DEN.1.1: Maximum physical OD density over local 150 µm x 150 µm areas, stepping 75µm = 80 %

Calculations:

Total chip area = 150*150 = 22500µm^2

Total Area occupied by the OD layer in 150*150 window = 150*150*80% = 18000 µm^2

satisfies according to rule defined.

Bad test case if Area of OD layer > 18000 µm^2

Area for Bad case 18000+0.25 (Area of any extra layer) = 18000.25µm^2 Percentage = 18000.25/22500 = 80.0111% (Violation BAD Case)

After this area calculation development of QA Cell for bad and good test cases takes place.

So in case of maximum density rules in good cases area is maintained according to the percentage specified but in bad test case area is set at the value more than that of the value specified in rule. If the DRC deck is aligned properly then it will highlight in bad test case.

(b) Understanding the importance of Latch-up effects on the Chip fabrication.

A latch-up is a type of short circuit which can happen in an integrated circuit (IC). More specifically it is the unintentional creation of a low-impedance path between the power supply rails of a MOSFET circuit, triggering a parasitic structure which disrupts proper functioning of the part, sometimes it can lead to destruction of transistor due to over current[18].

To prevent the latch-up effect the distance between well tie and vdd/ground must be maintained properly otherwise it will create short circuit path.

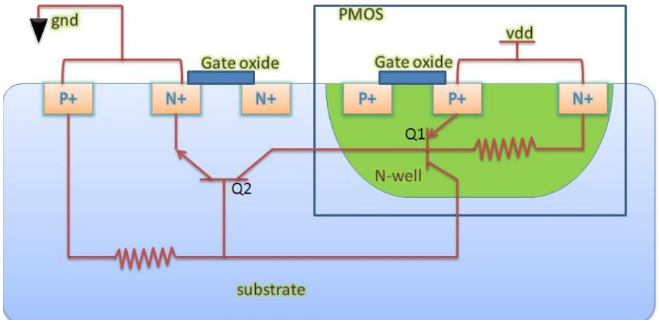


Figure 4.24 Latch-up problem in MOSFET [18]

Following are the ways to prevent latch-up problem.

1. Reduction in beta of any of parasitic device i.e. npn or pnp transistor. To achieve this increasing space between the devices would be best but that will increase the width of the lateral device. Also increase in space reduces packing density.
2. Another way to avoid is to increase substrate and well doping to reduce resistance of well or substrate. Using retrograde doped well resistance will reduce.
3. Providing alternative collectors of minority carriers can also be a good solution to this latch-up problem. Use of guard rings around the device avoid latch-up.

In fabrication process foundry specifies certain rules for latch-up. For example :

LUP.D.1: Maximum distance from any point inside SD_SourceDrain area not covered by (OD25) to nearest OD of a well tie within the same NW or PW is 30.00 [A]

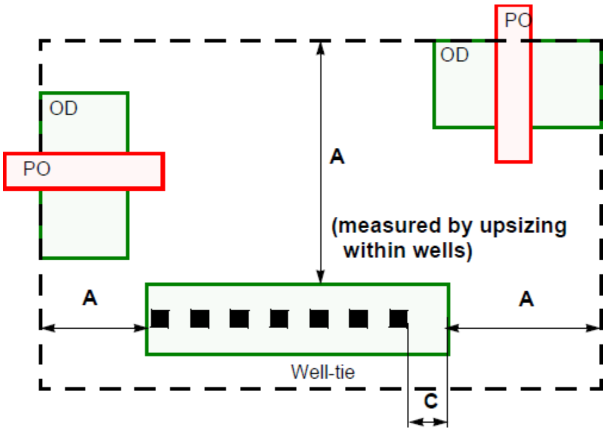


Figure 4.25 Latch-up rule defined in DRM [19]

(c) High Voltage Management Design Rules

The Voltage property is determined in two ways:

1. Layout Information **:** The voltage property is assessed through the recognition of the sources of HV Management. Recognized Sources are:

- Source/Drain of MOS Transistor
- Terminals of unsalicided PO resistor

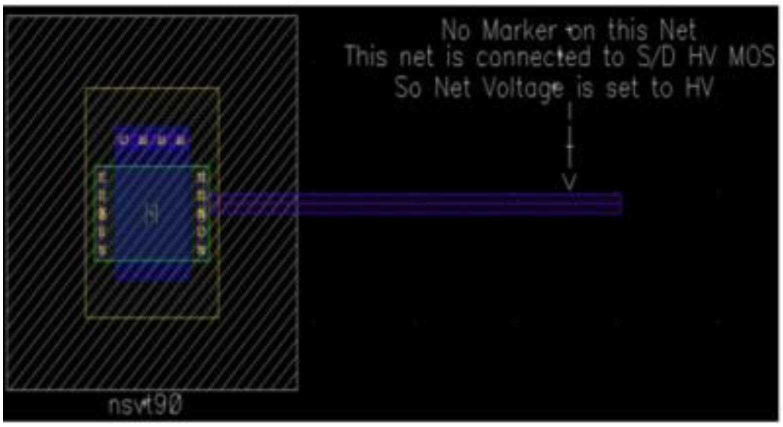

No Marker on this Net
This net is connected to S/D HV MOS
So Net Voltage is set to HV

Figure 4.26 Voltage Management: When net is connected to S/D of MOS

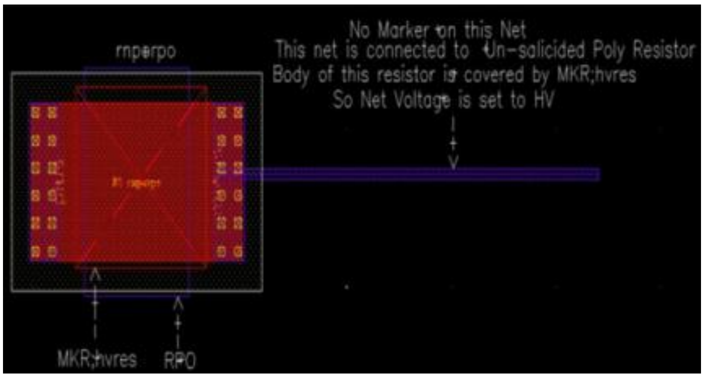


Figure 4.27 Terminals of unsalicided PO resistor

2. Voltage Marker Information

The designer has the possibility to correct the voltage information determined in the LAYOUT by using dedicated markers. If the net is connected to a layer marked with a voltage marker, then the net inherits this voltage property[19]. The Voltage property is propagated to the entire net through any interconnecting layer (OD, PO, PO1 and metals). The Voltage property is propagated to the entire net (also outside the GOHV regions) through any interconnecting layer (OD, PO, PO1 and metals)

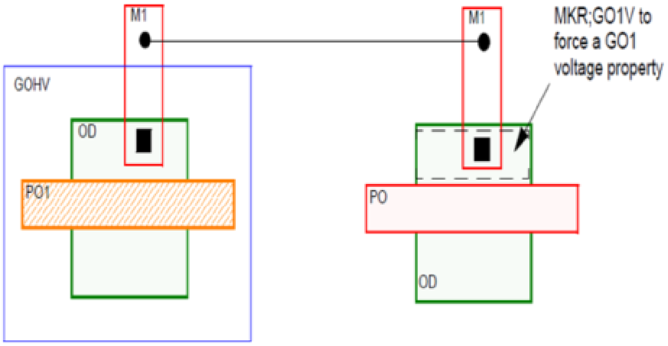


Figure 4.28 Voltage Management Mechanism [9]

Concept of Aggressor and Victim

Any time on a net, are present devices belonging to different voltage domain, we can identify at least one Aggressor and at least one Victim; an aggressor is always the device or the marker with highest voltage class present on the net; victims are devices with lower voltage class on the same net.

If designer consider this configuration as “SAFE”, then designer needs

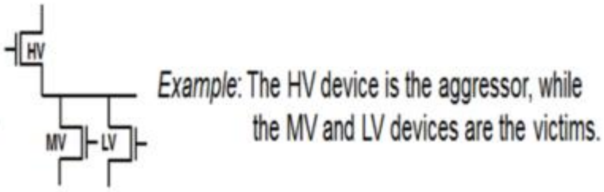


Figure 4.29 Concept of Aggressor and Victim

(d) Antenna rules

In fabrication process during plasma etching the large amount of charge is induced. If a large interconnect poly or conducting material is connected to Gate terminal then this Gate will act as Antenna and large amount of charge will induce[20]. The amount of charge because of extra carriers becomes very difficult for gate to handle and it can damage thin oxide layer.

So , Antenna effect results in degradation of oxide layer and breakdown of Gate oxide. In order to avoid antenna effect reduce large interconnect area to gate of MOSFET and there are several other ways for the same. Following are the ways to prevent Antenna effects:

1. Insertion of jumpers: A Jumper is a forced layer change of one metal on another metal layer and then back to same layer. Jumper breaks long metal layer into small segments so that the wire connected to the gate is short and not much capable to collect charge. Jumper insertion is fully controlled by routing tool and its disadvantage is it can cause congestion problems.

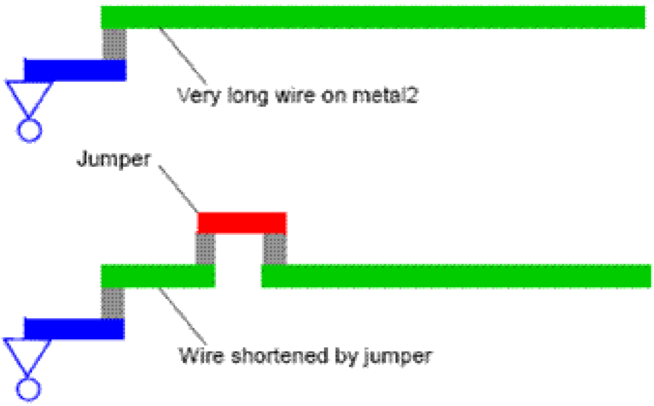


Figure 4.30 Insertion of Jumpers

2. Insertion of diode near input gate pin provides discharge path to the substrate to avoid the accumulation of charges near gate. But diode insertion will increase cell area and speed will decrease as increase in input load.

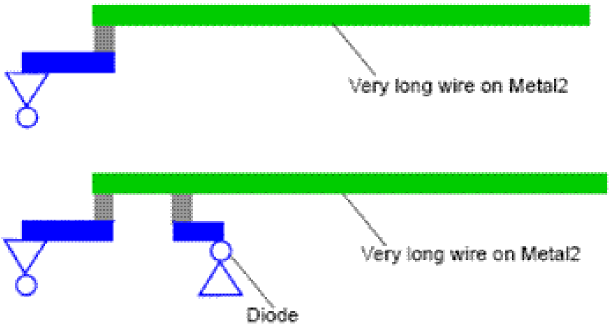


Figure 4.31 Diode Insertion

3. Another way to avoid Antenna effect is change the order of routing layers by connecting gate to the highest metal layer.

ANTENNA RATIO: The antenna ratio is used to predict whether the damage will occur or not. It is the ratio by which the tunneling currents get multiplied. Fabrication of conductor layers is done starting from lowest layer to highest conducting layer[21]. The layer which are directly connected to gate oxide are conducting layers and can form antenna. Probability of gate damage is proportional to the antenna size.

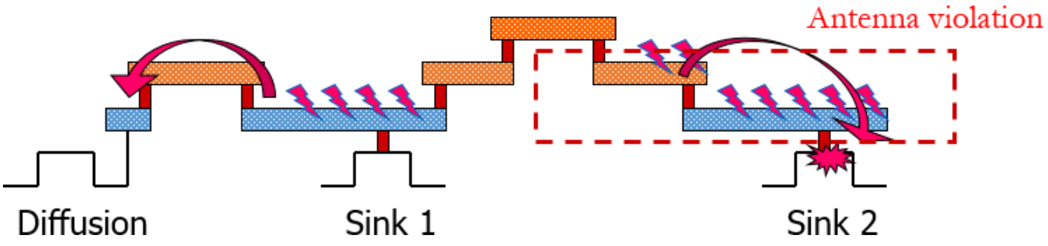


Figure 4.32 Antenna violation

Magnitude of effect is proportional to Antenna Ratio

Antenna Ratio = Exposed Conductor Area/Gate Oxide Area

4.3.5 Purposed Methodology

Design Rule Checking run-set implementation is a part of PDK validation team. As complexity of design rules is increasing , it is very important to check alignment of DRC Deck with DRM. So to check its alignment we need to create all the possible test cases that designer can come across during circuit designing. If DRC deck is properly coded then the chances of error in layout would be minimal. For validation team creates Quality Assurance cells where there are two type of test cases are defined , Good test case and Bad test case. Under good test cases the values that are mentioned in DRM are used and in bad test cases vales are less than the actual values with difference of minimum grid size. For example, in distance rule value mentioned is 2.0 then for good case distance between two layers is maintained 2.0 and for bad test case distance between two layers is 2.0 – grid size . Errors will highlight in bad test cases and will not highlight in good test case. If validation team found any misalignment like error is highlighted in good cases then it will report problem to Deck developer to make the desired changes. After completion of creating test cases all the cells are passed through regression testing to check overall percentage of rules that have been covered[22]. To provide good quality PDK to customer its good coverage should lie between 95-100 percent and bad coverage must be nearly zero. This percentage is used to measure the quality of PDK.

DRM Rule example:

NWELL DESIGN RULES:

NW.S.1	Space		B	0.340

Step-1: To check the above rule, specified layers are picked from layer palette of virtuoso and drawn accordingly to the rule statement. Labels are put for the better understanding and user readability.
There are two types of test cases one is good test case and other is bad test case.
Also, creating QA cell has some defined naming conventions for the ease of the QA engineer.
Top cell name is based on layer for which rules are defined to make it easy to understand where QA cells are present for particular rule. For example if rule is defined for NW layer top cell is named based on DRM i.e. DRC_NW. NW.S.1 is a space rule in which first we will select NW drawing layer from the layer palette and draw the test case.

Step-2: The DRC deck developed by the PDK developer is then run on this gds file with the help of Calibre nmDRC tool by Mentor Graphics. There are some Customization settings for the DRC. User can switch on/off depending on the requirements for the particular test case requirement. Once the customization settings are done, user can run the DRC to highlight the errors in the test cases drawn Block level or chip level settings are also available. They also help in reducing the simulation time by unchecking the box which are not needed. After running the DRC, errors present in the layout are highlighted.

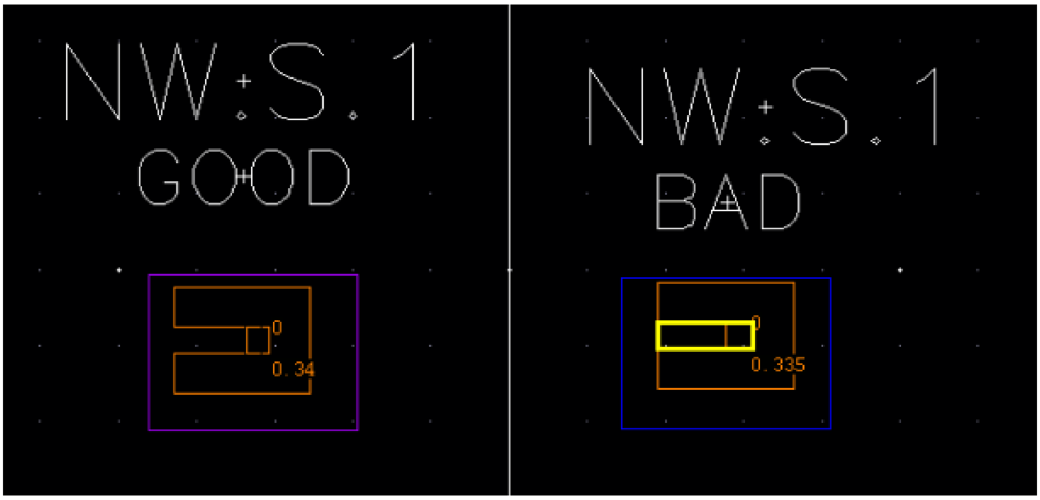


Figure 4.33 Snapshot of QA cell highlighting error in Bad test case

In DRM there are various categories for design rules like generic design rules include distance, enclosure, space, width, overlap, extension rules, robust design rules include latch-up design rules, antenna design rules and density design rules.

Design Rules specify certain geometrical constraints i.e. dimensional inequalities to the designer for the layout so that the patterns on processed wafer will preserve the topology and all the geometrical values of the design with highest probability[23]. All the connected regions will stay connected and all length and width of transistor remain same. The implementation process includes data handling , mask making and wafer fabrication should produce final patterns maintaining all constraints and electrical properties.

Generic design rules:

The layout design rules are used as guidelines for construction of various masks needed in fabrication of integrated circuits. The most important parameter which is used in designing is minimum line width. This parameter indicates the mask dimensions of semiconductor material. Minimum line width is the minimum MASK dimension which can be accurately transferred to the fabrication material.

Development of layout is the most critical in IC design because of involvement of many costly tools and also huge amount of human resources. Due to device shrinking technology development has become difficult. These problems can become a cause of yield drop.

Yield dropout happens due to certain defects mentioned below:

1. Random Defects: During processing some dust particle may lands on the wafer also due to impurities in silicon itself[24]. These defects can cause a shorts or open connections at metal layers. On shrinkage of feature sizes , there is no decrease in random defects which makes advanced integrated circuits more susceptible to this type of defect.

2. Systematic Defects**:** In deep submicron process technologies systematic defects are prominent contributor in yield loss**.** Systematic defects caused due to limitation of lithographical processes that increased the variation in desired patterns. There is another aspect of process related problem that is planarity issues which make layer density requirements necessary because areas with a low density of a particular layer can cause sagging of upper layer, resulting in uneven planarity across the chip.

3. Parametric Defects: Parametric defects become more critical in deep submicron technology. Parametric defects occur due to improper modeling of parasitic present in interconnects. On comparing the results manufactured devices does not match with the expected results from simulations and does not meet design specifications.

DESIGN FOR MANUFACTURABILITY:

To ensure quality, reliability and time to market there is a process known as Design for Manufacturability. In order to improve yield, set of guidelines are used for polygons and shapes are defined under Design for manufacturability. For fixed amount of space available for layout there are multiple ways to enhance yield.

Following are some DFM guidelines that can be taken care during layout designing:

- For minimum area for physical layers
  Under this configuration first identify rectangle which are small in dimension of a given layer (example shape at the minimum area size like diffusion). Now try to draw area value more than the minimum value when free space is available because with this action process window can

allow minimum area shapes but if number of shapes is more then there are chances of missing implant. For example in case of PWell and NWell Straps.

- Enclosure of contact by poly silicon

  Under this configuration first of all identify minimum enclosure of contacts by diffusion. Then try to extend enclosure of contact when possible because of overlay contact can fall on the border of diffusion area generating junction leakage.

Example for this scenario is shown below:

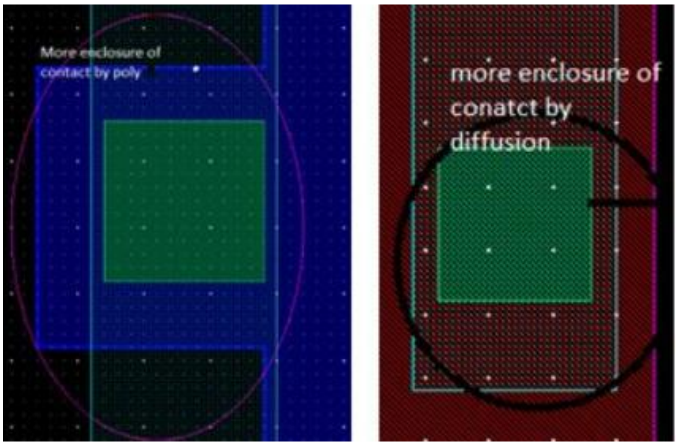


Figure 4.34 Enclosure of Contact by poly silicon

- Extension of Metal on Via/contact at Line End

Under this configuration identify via transition and then try to extend the overlap of metal lines otherwise process window issue could lead to open vias. For better transition extending metal overlap is good solution.

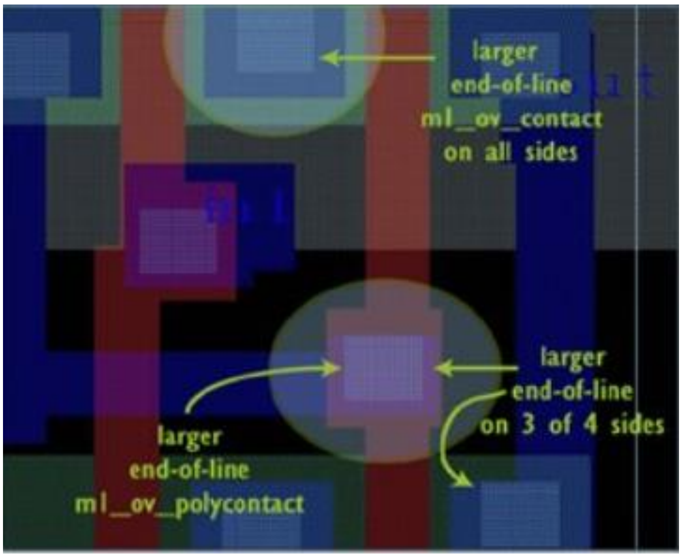


Figure 4.35 Extension of Metal on Via/contact at Line End

- Extension of Gate on Diffusion

For this configuration , identify poly gate at minimum distance from diffusion layer and try to extend when it is not close to other structure. Otherwise during silicon implementation it could lead problem of leakage current between source and drain of the transistor.

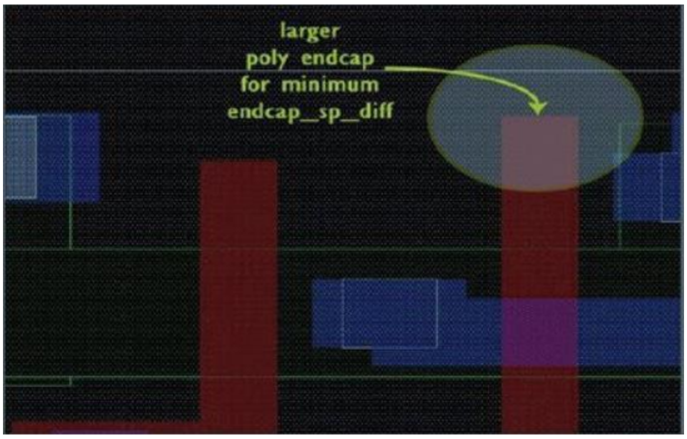


Figure 4.36 Extension of gate on Diffusion

- Redundancy of Contact/Via

In this configuration, identify single contact for critical transistor in cell. And then try to increase number of contacts along with extension of poly and metal without creating impact on critical area**.** In case of single contact sensitivity for defect would increase and chances of open contacts. With insertion of new contacts chances for open contacts reduces and reduce electro migration effects.

- Spacing between two metals

In this configuration identify minimum spacing wires and increase the minimum spacing values. If long wires are present at minimum spacing there is probability of shorts.

CHAPTER 5

PCELL DEVELOPMENT

5.1 WHAT IS PCELL ?

A parametrized cell or PCell is a programmable design entity. Whenever designer is creating layout there is need of multiple instance for default values and for modified values of single cell. So PCell is used to create multiple instances where designer can vary several parameters for single PCell for example with different width, different number of fingers etc. This type of devices saves a lot of time and efforts of layout designers. It improves productivity of designer and also make design more accurate. The PCell developer creates is called master[24]. A master is the SKILL Language code used to define the structure of the cell and its parameters. After compiling the master it is stored in database in the form of SKILL procedure. So whenever designer edit some parameter it appears in the cell instance on compiling the master. In this way PCell remain unchanged only instances vary.

PCells provide the following advantages:

- It speed up entering the layout data by eliminating the need to create layout for same device with different variations.
- It saves huge amount of disk space by creating a library of cells for similar parts which are attached to same source.
- It improves accuracy by eliminating dimensional errors that can occur while creating multiple versions of same cell.
- It eliminate the efforts required to explore different hierarchal levels to change a small detail of the design.
- It makes the complex Design creation easy and maintenance of library becomes easy.
- It is tightly integrated with cadence virtuoso environment and have better porting process
- Integration with block and chip design using SKILL programs is efficient.

5.2 IMPORTANCE OF PCELL IN PDK

PCell plays a very important in PDK because whenever a new technology is released every time there are some new PCell devices are added according to requirement of the circuit design and its validation is also crucial because designer will use this device and it should not have any error like all the parameters must be completely aligned with other ,callbacks should be defined properly and work properly for example if we change any parameter like width then the complete gate area will also change automatically through callback. It is very important part during PDK validation.

The diagram shown below describes how multiple instances of PCell are used.

PCell Example

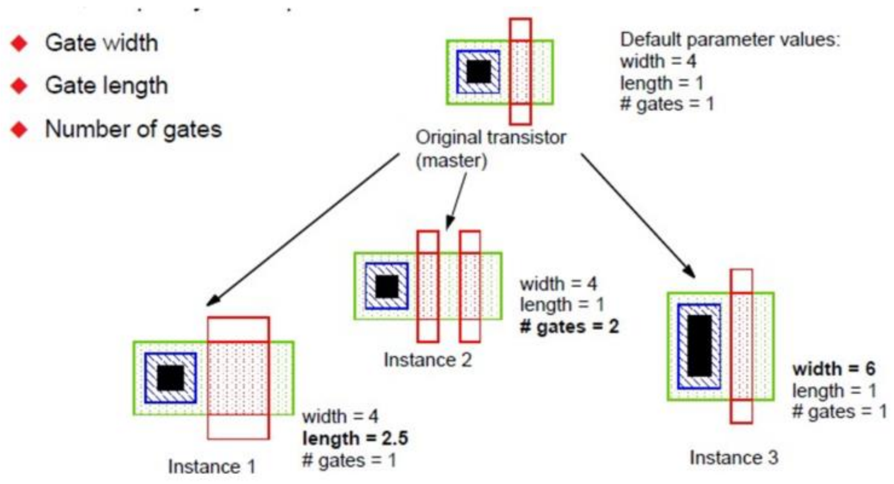


Figure 5.1 PCell Example

5.3 DEVELOPMENT OF PCELL

PCell is a powerful tool in design methodology combined with Relative Object Design (ROD). Using the concept of ROD one can define technology independent cells that are customizable to any application. Basically, ROD is a set of high level SKILL functions for defining complex layout objects and persistent spatial relationships between them.

With ROD , one can create from simple rectangle to complex shapes such as guard rings, buses and transistors. It associates a signal with shape and align ROD objects with each other. Designers can access information stored in ROD objects through all levels of hierarchy. It assigns unique names to different shapes and to get particular coordinates of that shape one can get easily with the help of ROD functions.

5.4 PCELL VALIDATION

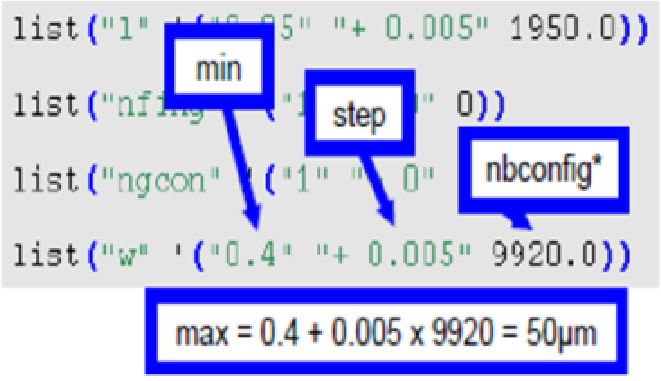
To increase the productivity of design Parameterized Cells are developed. To optimize this gain PCell validation plays important role from designing point of view. Exhaustive PCell validation is done to check reliability .

PCell generates different instances for various configuration of parameters. In order to check these configurations , different values for parameters are passed. So, all the possible configurations are instantiated on topcell for validation of PCell.

To generate automatically the Validation topcell from 3 Configuration files:-

- Topcell.cdf (Contains the List of CDF (Component Description Format) Parameters)
- Topcell.func8h.il (Call Backs)
- Topcell.il file (PCell Code-Library Details, Description of PCell and its Layer Information)

On the example of “w”, from the minimum value of 0.4um it will reach the maximum value of 50um by step of 0.005um.



```
list("1"       5" "+ 0.005" 1950.0))
list("nf             " 0))
list("ngcon"   ("1" "   0"
list("w" '("0.4" "+ 0.005" 9920.0))
```

Figure 5.2 CDF Parameter

In the case of an ideal Complete Validation of a PCell, all Configurations should be instantiated on the topcell. For a transistor with only two parameters. “width”(w) and “length”(l), their ranges are the following:

0.4um<=w<=50um

0.25um<=l<=10um

In order to get all possible Configuration the variation step of those parameters is set to the grid resolution (0.005um), which allows to calculate the number of configuration for each parameter.

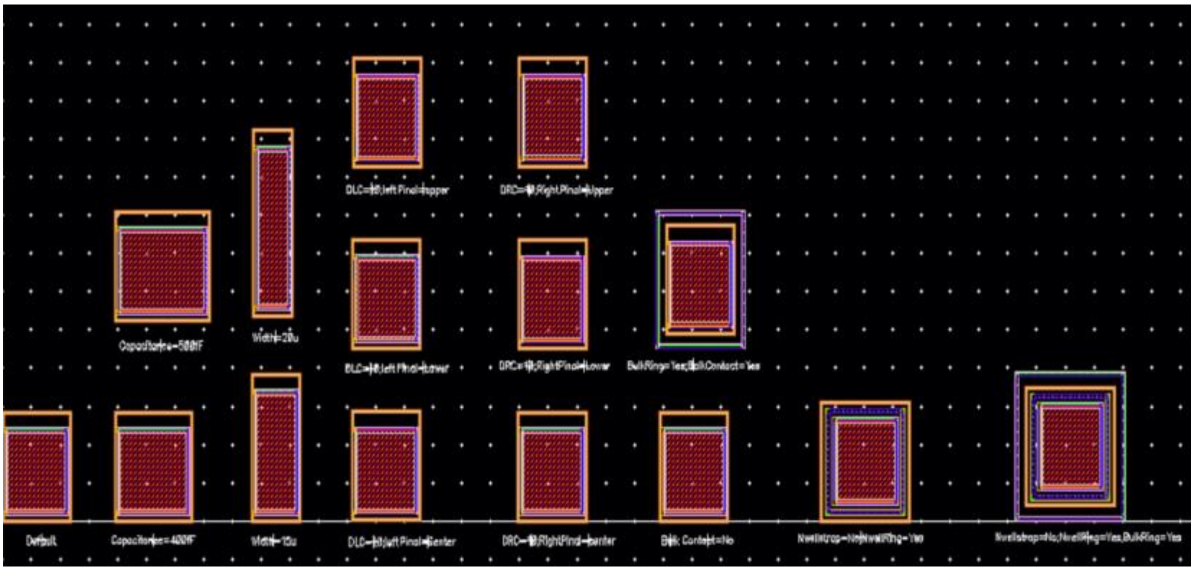


Figure 5.3 PCell Validation on CDF Parameter

CHAPTER 6

DRC DECK CODING (SVRF)

6.1 INTRODUCTION TO SVRF

SVRF stands for Standard Verification Rule Format. It is developed by Mentor Graphics. The information provided in the SVRF file(s) specifies almost everything needed for physical verification, including :

1. DRC rules.
2. LVS connectivity and device recognition rules.
3. I/O file specifications.
4. User-specified job options.

But some information related to the following topics is not provided in the SVRF:

1. Run type- flat or hierarchical.
2. Use of multiple processors and/or networked computers.
3. LVS job type- layout netlist extraction, netlist compare or both.
4. Name of extracted layout netlist file (LVS).
5. Hierarchical cell list file name (LVS).

Standard Verification Rule Format (SVRF) is a rule file which is used in calibre Verification applications. These rule files consist of design rule (DRC) checks; electrical rule (ERC) checks; layout versus schematic (LVS) and connectivity checks; parasitic extraction (PEX) applications. SVRF is completely aligned with DRM provided by the foundry. In DRM there are different types of rules defined for BEOL and FEOL[25-27]. Also rules are divided into two classifications i.e. Boolean functions and dimensional checks. Boolean checks include AND,OR,NOT,XOR and Dimensional checks include INT,EXT,ENC.

6.2 DESCRIPTION OF BOOLEAN FUNCTIONS

1. AND: For AND operation there are two types of cases possible i.e. performing AND on single layer or performing AND on two different layers.

Syntax for single layer:
AND Layer1 (constraint)
Syntax for two layers:
AND Layer2 Layer3 ([NOT] CONNECTED)

Description: It constructs the intersection regions of polygons on the input layer(s) and outputs the intersections as polygons.

Example 1: Rule 2 {

@ Rule 2 : AND L1

AND L1

}

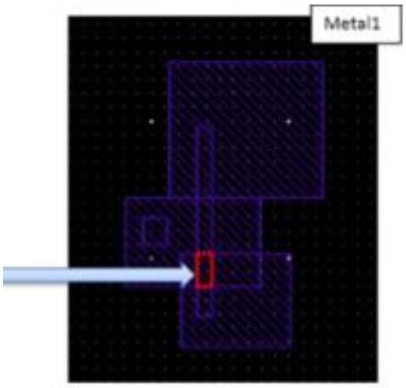


Figure 6.1 Error highlighting for Rule 2

Example 2: Rule 3 {

@ Rule 3 : AND L1 L2

AND L1 L2

}

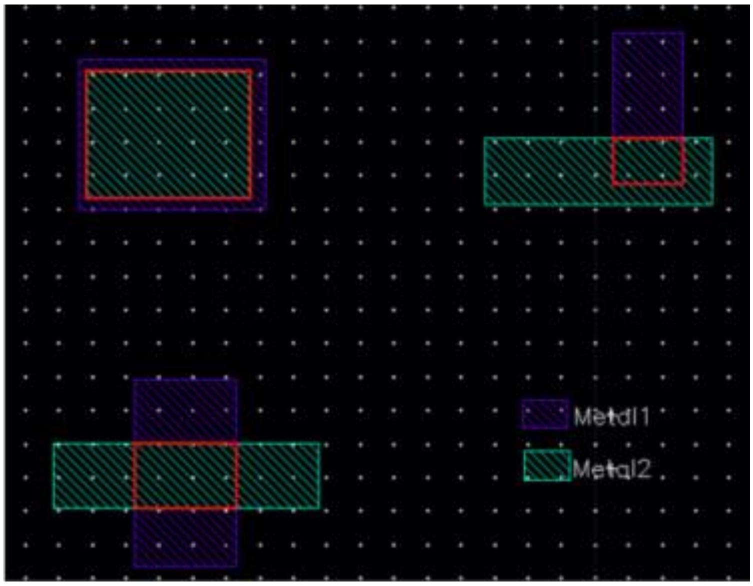


Figure 6.2 Error highlighting for Rule 3

The above code will highlight intersection region of polygons on Layer L1.

2. OR**:** In case of OR operation there is two possible ways to write rules in deck ,one is for single layer and other is for two or more layers.

Syntax:

OR layer1

OR layer2 layer3 [layerN]

Description: This merges all polygons on the input layers into one layer. The one-layer operation is equivalent to the AND layer1 > = 1 operation.

A two-layer operation generates output equivalent to the polygon data on layer3 if layer2 is empty and vice versa. More than two layers are permitted.

Example 3 **:**

Rule 5{

@ Rule 5 : OR operation of L1 and L2

OR L1 L2

}

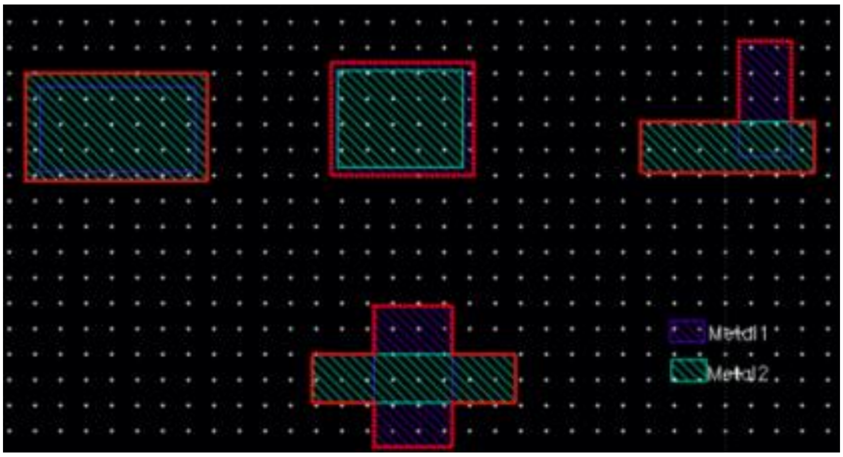


Figure 6.3 Error highlighting for Rule 5

NOT layer1 layer2

Description Selects all layer1 polygon areas not common to layer2 polygons. If layer2 is empty, the NOT operation generates output equivalent to the polygon data on layer1.The NOT operation is node-preserving for connectivity extraction. Connectivity is generally passed from layer1 to the output layer.

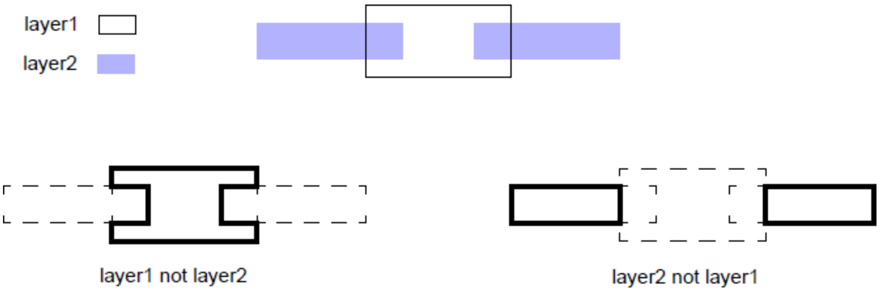


Figure 6.4 NOT operation

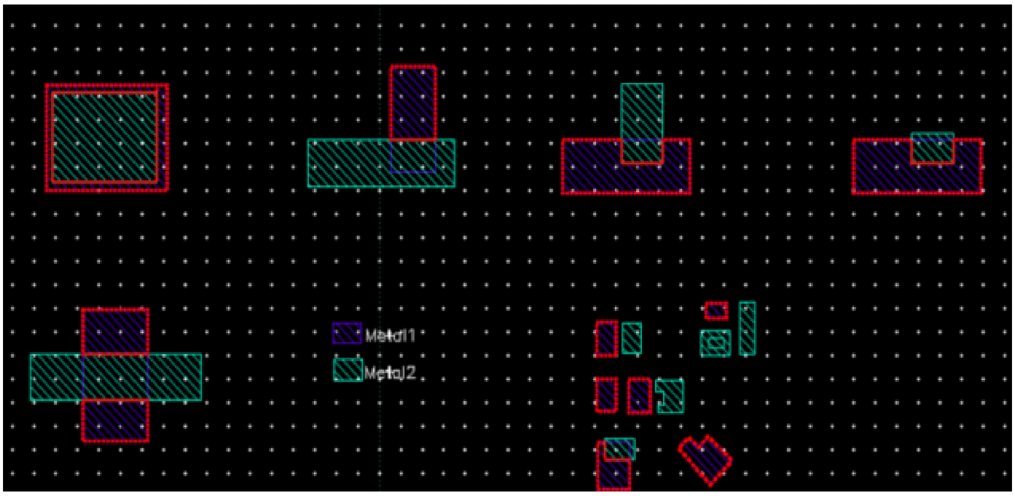


Figure 6.5 Error highlighting for NOT case

3. XOR Syntax:

XOR Layer1

XOR Layer2 Layer3

Parameters:

Layer1 : Original layer

Layer2 : Original layer or layer set or a derived polygon layer

Layer3 : original layer or layer set or a derived polygon layer

Description:

This keyword is used to select all polygon areas that common to exactly one polygon. The one-layer operation is equivalent to the AND layer1 = = 1 operation. The two-layer operation generates output equivalent to the polygon data on layer3 if layer2 is empty. If layer3 is empty, the two-layer operation generates output equivalent to the polygon data on layer2.

Example 4:

Figure 6.6 XOR operation

RULE 7 {

@Rule 7: XOR L1 L2

XOR L1 L2

}

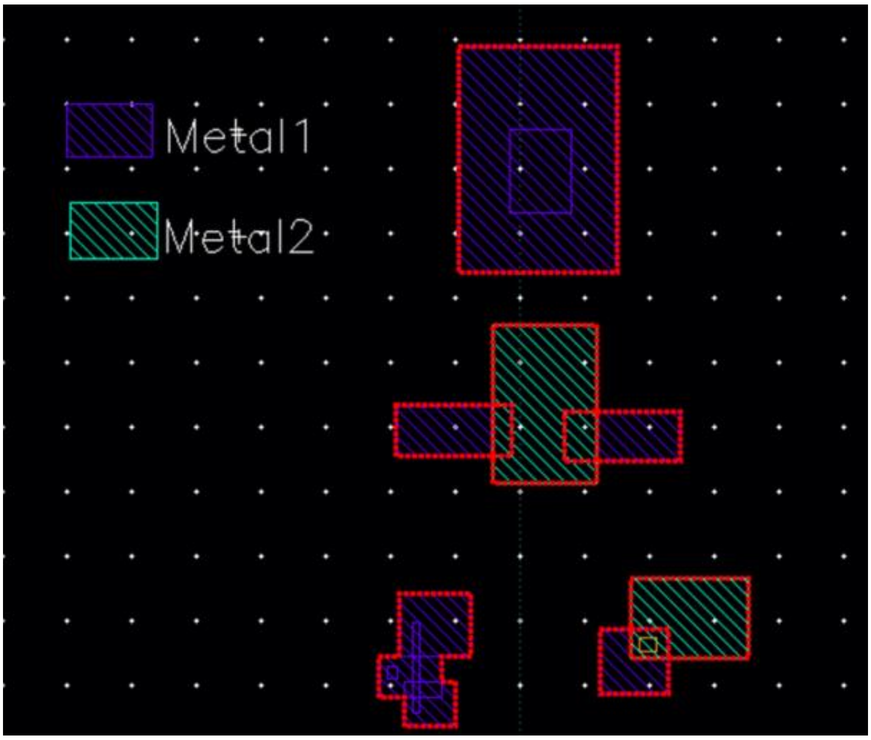


Figure 6.7 Error highlighting for Rule 7

6.3 DESCRIPTION OF DIMENSIONAL CHECKS

1. INT(internal):

Width and overlap is checked using INT command

Syntax**:**

INT Layer1 constraint

Parameters:

Layer1 : original layer

Layer2 : original layer or layer set or a derived polygon layer.

Layer3 : original layer or layer set or a derived polygon layer

Description:

For the single-layer syntax, measures the separations between interior-facing sides of edges from the same polygon on layer1.

Two-layer syntax, measures the separations between the interior-facing sides of layer1 edges and the interior-facing sides of layer2 edges.

Example 5:

```
Rule8{
@Rule8 : Width of L1
INT L1 < 1.0
}
Rule9{
@Rule9 : Overlap of L1 and L2 ;Value : 0.5
INT L1 L2 < 0.5
```

}

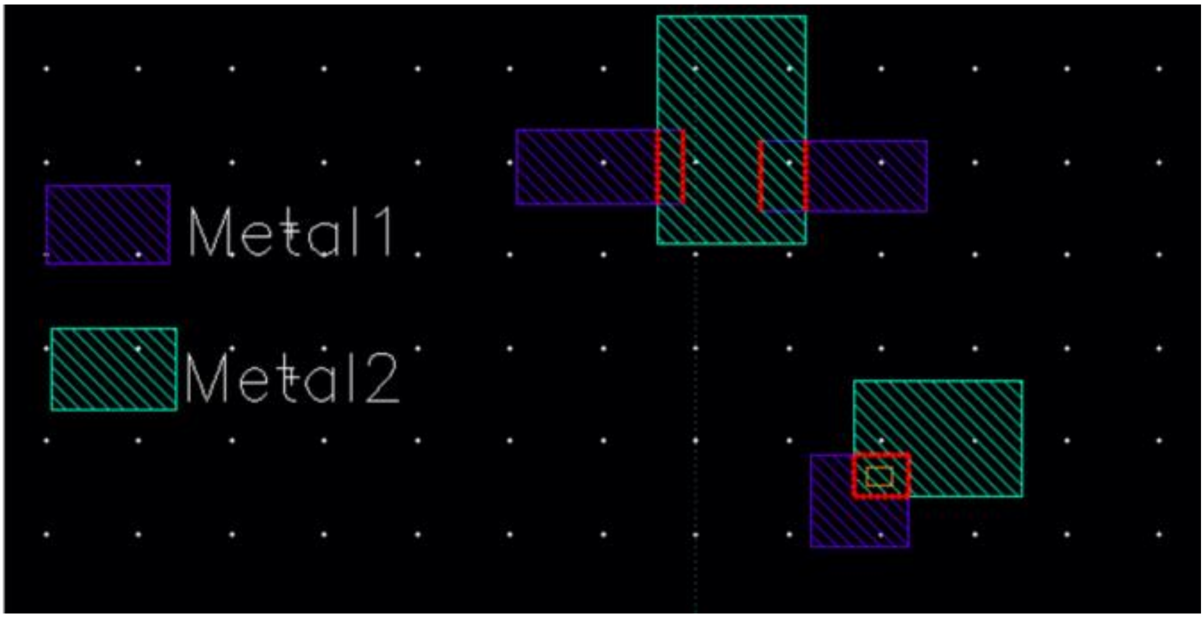


Figure 6.8 Error highlighting for Rule 9

2. ENC

Syntax:

ENC layer1 layer2 constraint

Description:

Measures the separation between exterior-facing sides of layer1 and interior- facing sides of layer2 edges.

Example 6:

Rule10{

@Rule10 : Enclosure of L1 and L2 ;Value : 0.5

ENC L1 L2 < 0.5

}

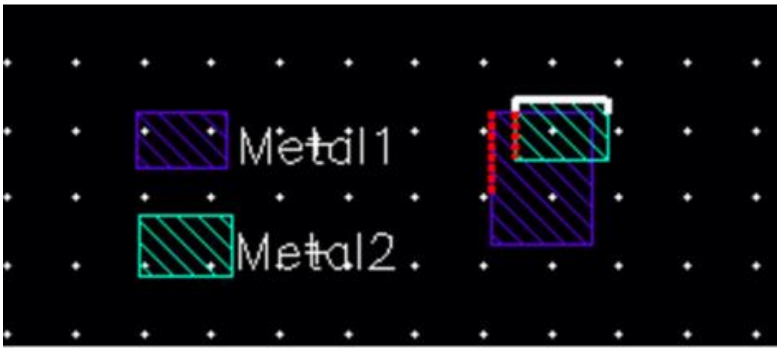


Figure 6.9 Error highlighting for Rule 10

CHAPTER 7

RESULTS AND DISCUSSION

7.1 AUTOMATION OF GENERIC DESIGN RULES

For the automation of QA Cell development SKILL language is used. Manual creation of QA Cell makes process cumbersome because we have to draw keeping in mind all the constraints defined in the DRM. Sometimes manual test cases may cause critical error because the distance measured can be wrong Even on adding property to marker layers it makes the process repetitive to add same property again and again. Also when we want to repeat the same rule with different layers it consumes time. To fasten the QA Cell development we use the cadence SKILL routine.

As we all know automation is the key objective of all industrial practices. Everyone prefer to automate the process using SKILL scripts.

SKILL is a High level Language which is used to customize and extend virtuoso design environment. It is a programming language that helps to procedurally invoke any operation that you can perform interactively through graphical interface. It supports C-like syntax and allows to develop new applications and to quickly customize existing CAD applications. It can be immediately executed in Cadence environment.

SKILL is ideal for rapid prototyping. One can partly validate the steps of the algorithm before incorporating them in a bigger program. It is useful when repetitive jobs to be performed. SKILL also controls notoriously error-prone system programming tasks like list management and complex exception handling. It is powerful tracing and debugging.

7.1.1 Automated flow of QA Cell development

Following are the output snapshot of QA Cell of Distance rules generated by SKILL routine.

1. Rule name is NW.D.4

Procedure passed:

```
fqaDistance( cv "NW" "OD" 0.080 "NW.D.4" ?layerX "y4" ?Yref 10.0) ; input by user
```

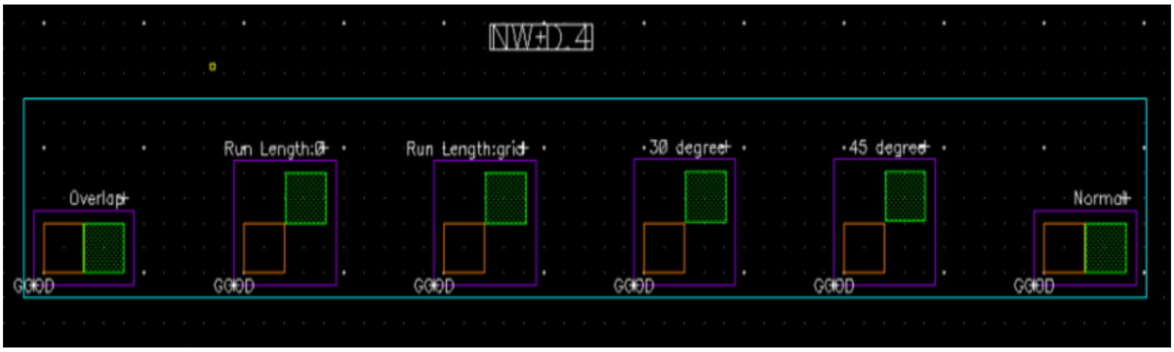


Figure 7.1 Good test case QA Cell generated for Distance rules.

The above figure shows all the possible good cases for Distance rule that include different runlength case, overlap case ,normal distance case with actual value of the distance i.e. 0.080

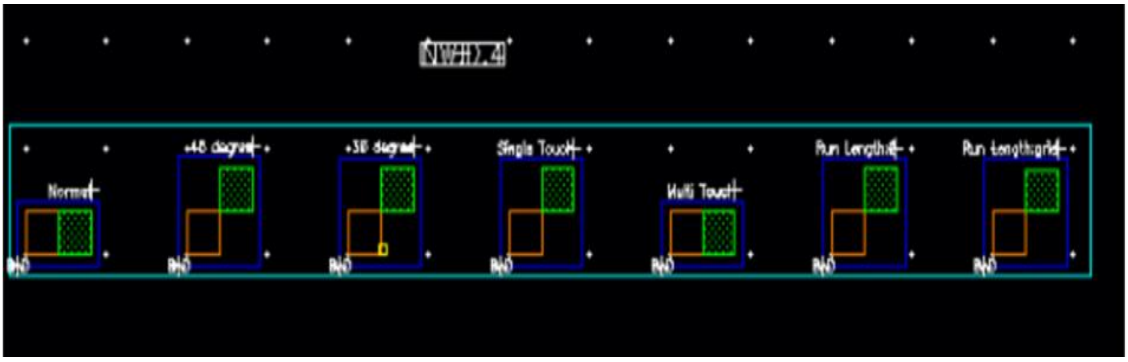


Figure 7.2 Bad test case QA Cell generated for Distance rules

The above figure shows all the possible bad cases for Distance rule that include different runlength case, multipoint touch case , single point touch case ,normal distance case with value less than actual value of the distance i.e. 0.080 – 0.005 =0.075.

2. Rule Name: PP.EN.3

Procedure passed:

fqaEnclosure(cv "PO" "PP" 0.020 "PP.EN.3" ?layerX "y4" ?Yref 10.0) ; input by user

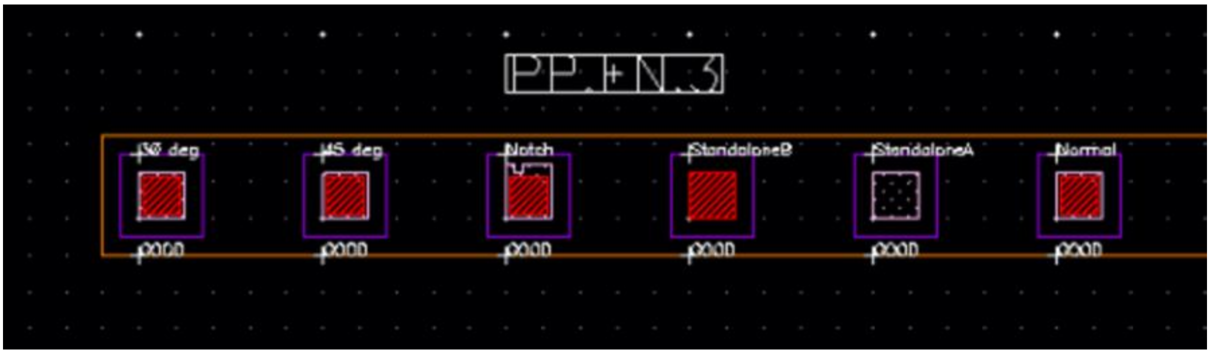


Figure 7.3 Good test case QA Cell generated for Enclosure rules

The above figure shows all the possible good cases for Enclosure rule that include different angle case, notch case ,normal enclosure case with actual value of the enclosure between PP and PO i.e. 0.020.

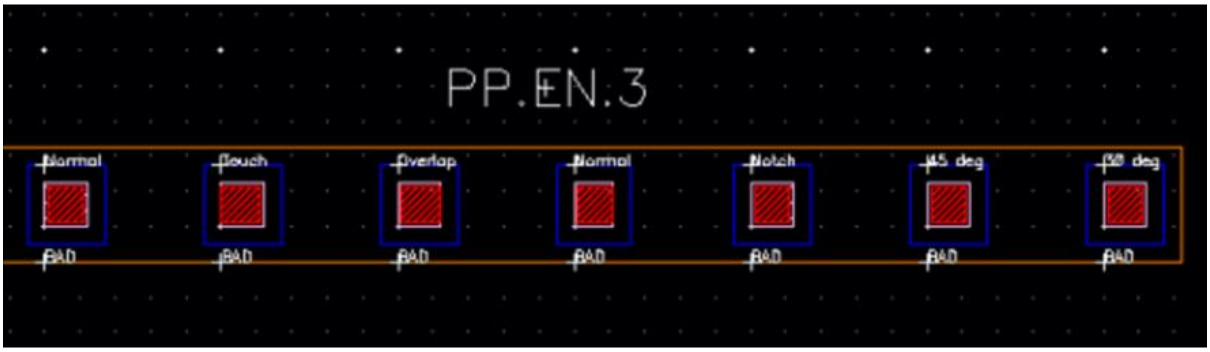


Figure 7.4 Bad test case QA Cell generated for Enclosure rules

The above figure shows all the possible bad cases for Enclosure rule that include different angle case, notch case ,touch case, normal enclosure case with value less than actual value of the enclosure between PP and PO i.e. 0.020 – 0.005 = 0.015.

3. Rule Name: NT_NHV.EX.1

Procedure passed:

fqaExtension(cv list("PO1" "drawing") list("OD" "drawing") 0.35 "NT_NHV.EX.1")

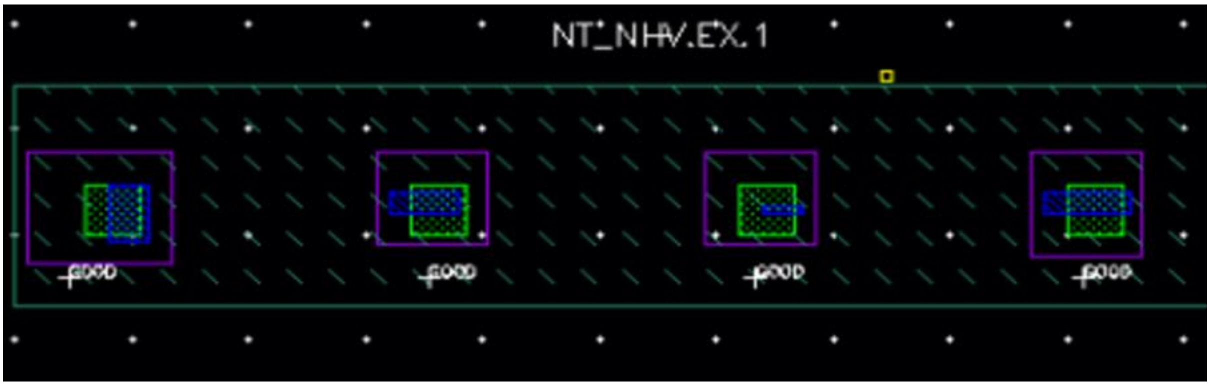


Figure 7.5 Good test case QA Cell generated for Extension rules

The above figure shows all the possible good cases for Extension rule that include touch case, overlap case ,normal extension case with actual value of the extension of PO1 on OD i.e. 0.35

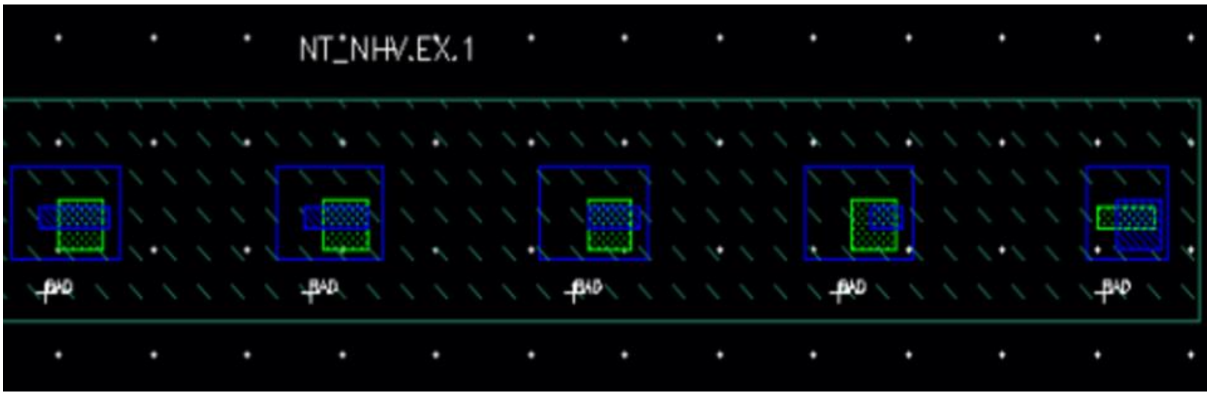


Figure 7.6 Bad test case QA Cell generated for Extension rules

The above figure shows all the possible good cases for Extension rule that include touch case, overlap case ,normal extension case with value of the extension of PO1 on OD i.e. 0.35 – 0.005 = 0.345

4. Rule Name: NW.S.1

Procedure passed:

fqaSpace(cv "NW"   0.340 "NW.S.1") ; input by user with required arguments

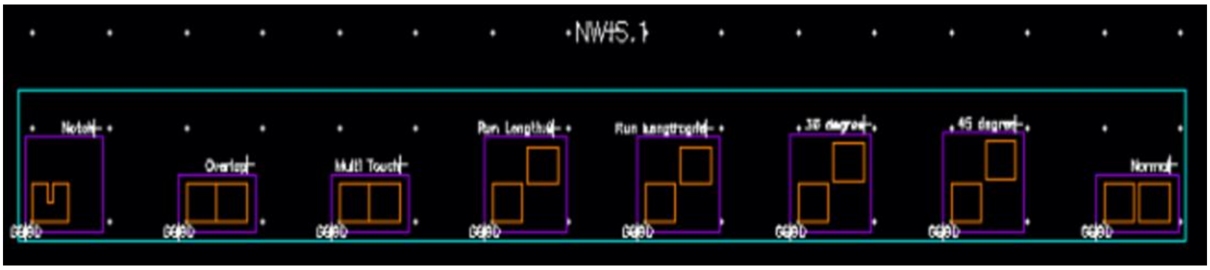


Figure 7.7 Good test case QA Cell generated for Space rules

The above figure shows all the possible good cases for space rule that include different run-length case, overlap case, multipoint touch case, notch case, normal space case with actual value of the space i.e. 0.340

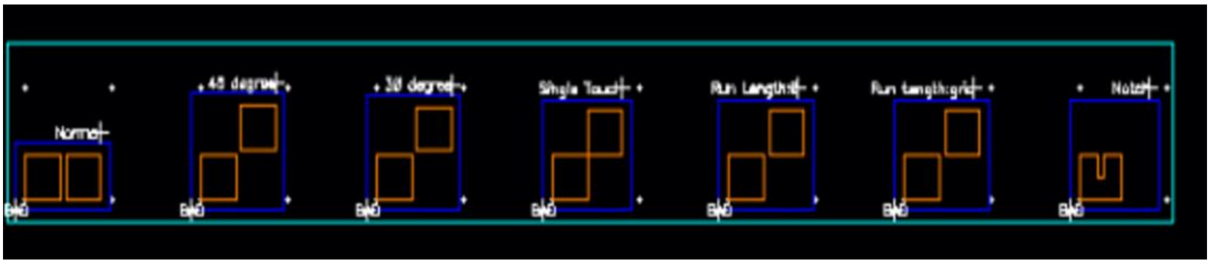


Figure 7.8 Bad test case QA Cell generated for Space rules

The above figure shows all the possible good cases for space rule that include different run-length case, single point touch case, notch case, normal space case with value less than actual value of the space i.e. 0.340 -0.005 = 0.335

5. Rule Name: RPOHV.OL.1

Procedure passed:

fqaOverlap(cv "RPO" "PO1" 0.3 "RPOHV.OL.1" ?layerX "NW" ?Yref 10.0)

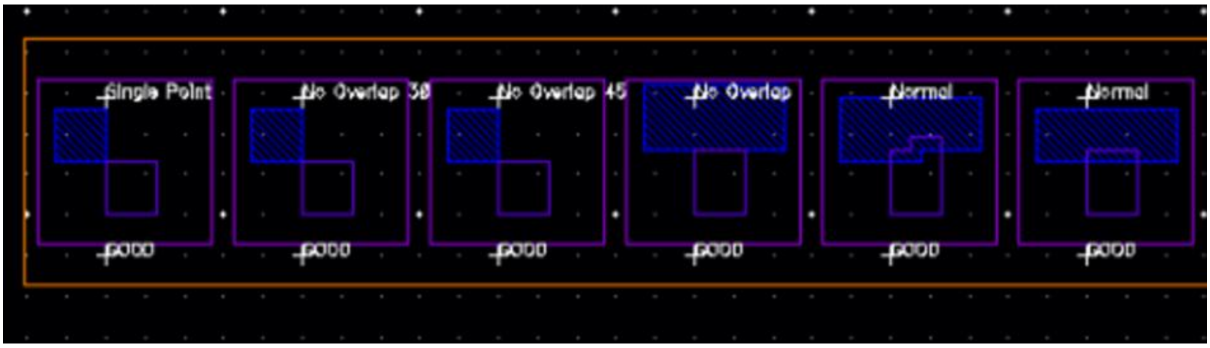


Figure 7.9 Good test case QA Cell generated for Overlap rules

The above figure shows various good test cases where no overlap case, single point touch case and normal cases for overlap are developed with value equal to 0.3.

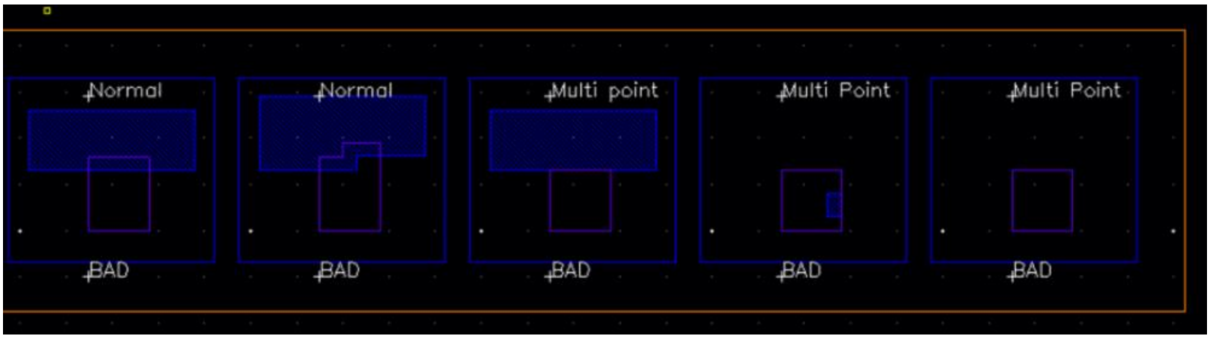


Figure 7.10 Bad test case QA Cell generated for Overlap rules

The above figure shows various bad test cases where no overlap case, multi point touch case and normal cases for overlap are developed with value equal to 0.3 – 0.005 = 0.295 .

6. Rule name: M1.W.1

Procedure passed:

fqaWidth(cv "M1" 0.34 "M1.W.1" ?Yref 20.0) ; user input with yaxis reference

Figure 7.11 Good test case QA Cell generated for Width rules

The figure shown above shows test cases developed for width rule using SKILL procedure with value of width equal to 0.34

Figure 7.12 Bad test case QA Cell generated for Width rules.

The figure shown above shows test cases developed for width rule using SKILL procedure with two different values of width equal to 0.34 – 0.005 = 0.335 and 0.34 + 0.005 = 0.345.

QA Cells for Robust design Rules:

1. Density Rules:

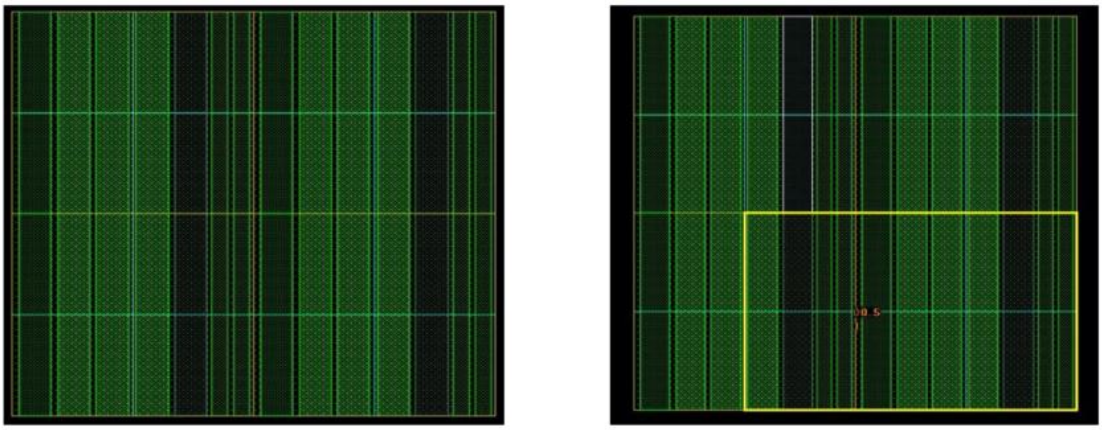


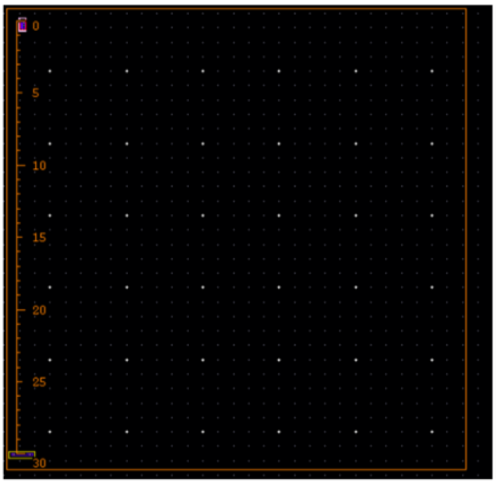
Figure 7.13 Good and Bad case for OD.DEN.1.1

Good test case checks the density of OD layer is maintained as 80 %

Bad test case checks that density rule is violated as its percentage is greater than 80.011% and highlighting after running Calibre nmDRC .

2. Latch-up Rule:

After creating test cases for latch up Rule for maximum distance scenario. Following are the snapshot of the test cases.



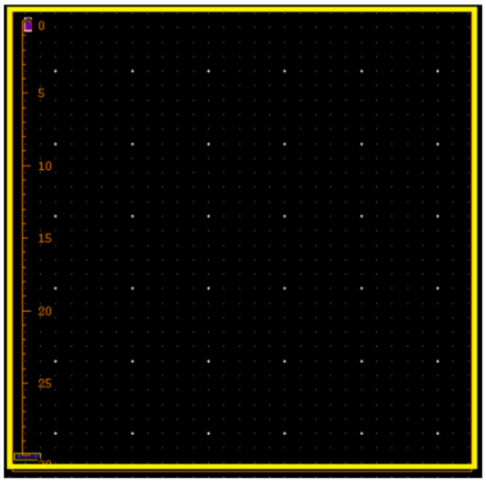


Figure 7.14 Good test case for LUP.D.1 Figure 7.15 Bad test case for LUP.D.1

Good test case for latch-up is to check that maximum distance from any point in Source/Drain to the well tie should be 30.00.

Bad test case for latch-up is highlighting when distance is greater than 30.00 i.e. 30.005 showing that DRC is violated.

3. Voltage Management rules

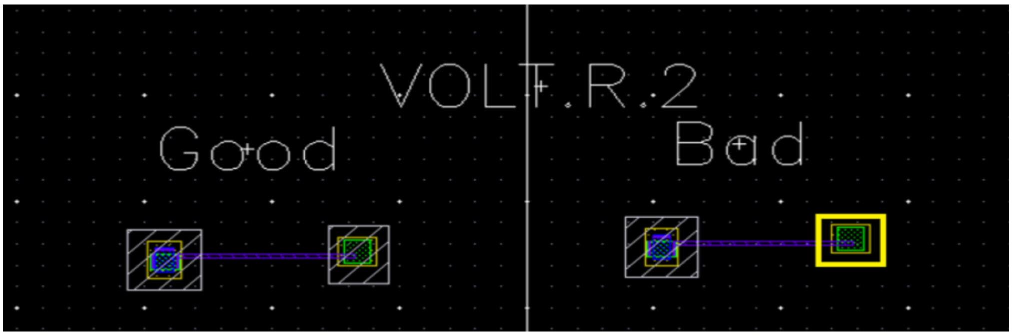


Figure 7.16 Good and Bad test case for voltage management rule.

Good test case for voltage management rule where OD layer is covered by voltage marker providing voltage information.

Bad test case for voltage management rule without voltage marker on OD layer highlights error after running Calibre nmDRC showing violation of voltage rule.

4. Antenna Rules

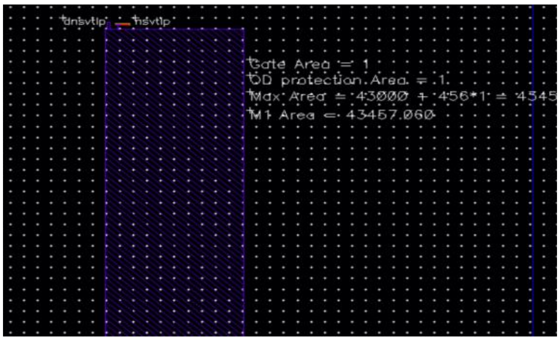
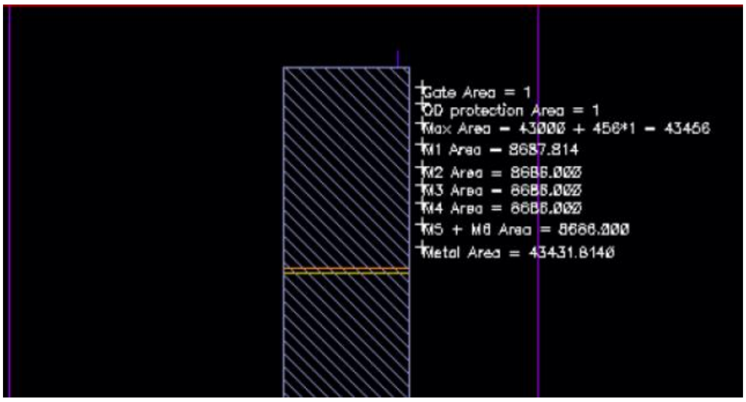


Figure 7.17 good case for Antenna Rule

For the rule present in DRM, Antenna ratio is calculated and test cases are generated according to the values calculated.



```
Gate Area = 1
OD protection Area = 1
Max Area = 43000 + 456*1 = 43456
M1 Area = 8687.814
M2 Area = 8686.000
M3 Area = 8686.000
M4 Area = 8686.000
M5 + M6 Area = 8686.000
Metal Area = 43431.8140
```

Figure 7.18 Bad case for Antenna rule

7.2 DEVELOPMENT OF PARAMETERIZED CELL

As discussed in chapter 5, PCell is developed using ROD Objects. PCell is developed for MOS Transistor. Design rules are specified for MOS transistor and according to the rules defined PCell is developed.

Following are the various sections used to define PCell and its parameters

Section 1: this section includes pcDefinePCell() , this procedure is used to provide the details about the library name , cell name and view name of the PCell. Also it contains the list of configuration parameters

```
pcDefinePCell(
list(ddGetObj("nitika") "mos1" "layout")
(
(w 0.5)
(l 0.16)
(polyLayer "poly")
(diffLayer "active")
(contLayer "contact")
(metalLayer "metal1")
(drainName "D")
(gateName "G")
(sourceName "S")
)
```

Section 2: This section includes body of PCell. Here all the shapes that are required for development are defined.

Example:

```
let((poly1 active1 cont1 cont2 polyWidth contWidth activeWidth contLength conAct_over
conPoly_over polyExtend metalContEnclose pinEndOffset)
tfId = techGetTechFile(pcCellView)
contWidth= techGetSpacingRule(tfId "minWidth" "contact")
polyExtend = techGetSpacingRule(tfId "minSpacing" list("poly" "active"))
```

```
diffContEnclose = techGetOrderedSpacingRule(tfId "minSpacing" diffLayer contLayer)
metalContEnclose = 0.05
sdWidth = contWidth + polyContSep + polyExtend
pinEndOffset = -(polyExtend + diffContEnclose - metalContEnclose)
rodAlign(?alignObj poly1 ?alignHandle "centerCenter" ?refObj active1 )
*/
transObj = rodCreatePath(
      ?layer list(polyLayer "drawing")
      ?endType    "variable"
         ?width w
      ?pts list(0.0:0.0 0.0:w+(2*polyExtend))
      ?beginExt polyExtend
      ?endExt  polyExtend
?encSubPath
list(list(?layer diffLayer
       ?enclosure 0.0
          ?beginOffset -polyExtend
       ?endOffset -polyExtend
          )
```

In the above code procedure is defined for poly layer , similarly other procedure are defined for other layers like NPLUS layer , Active layer , Metal layer etc.

Output snapshot of the PCell developed for MOS Transistor and its symbol generated to use in different cell views.

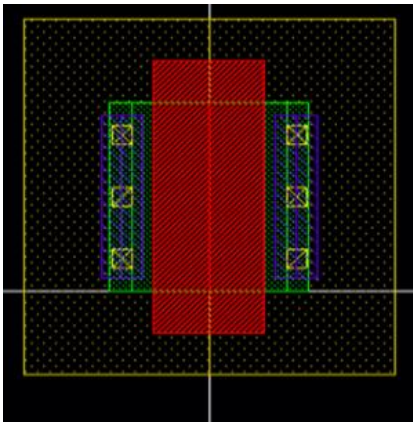


Figure7.19 Layout View of MOS transistor PCell

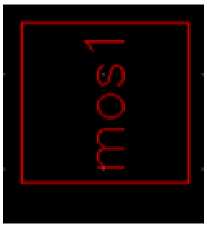
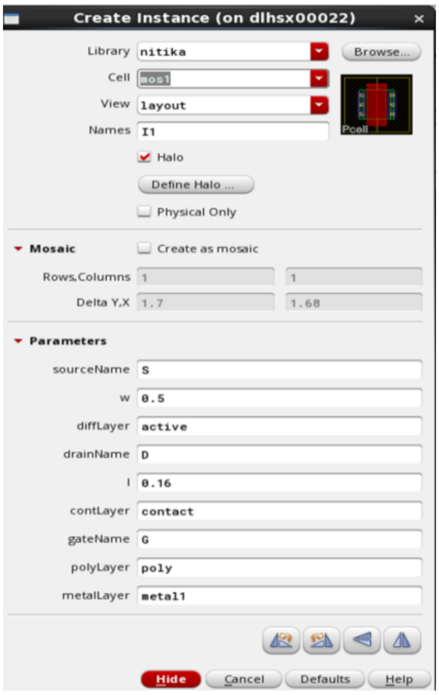


Figure 7.20 Symbol View of PCell for MOS transistor

Figure 7.21 is a snapshot of create instance window that appears while instantiating PCell. It has a section of parameters where we can change value of parameters and create different instances.



Library nitika
Cell mos1
View layout
Names I1
☑ Halo
☐ Physical Only

Mosaic ☐ Create as mosaic
Rows,Columns 1 1
Delta Y,X 1.7 1.68

Parameters
sourceName S
w 0.5
diffLayer active
drainName D
l 0.16
contLayer contact
gateName G
polyLayer poly
metalLayer metal1

Figure 7.21 Create instance window to change parameters

7.3 DISCUSSION

From the above results it is observed that automation of QA Cell using SKILL language helps to fasten this validation process. This automatic QA cell are more accurate as compared to QA Cell generated manually, there is probability of errors like value of distance created is wrong according to the rule which may increase efforts to debug this problem. Also development of PCell gives a small idea about their significance in PDK. The robust design rule testing also plays very important role in PDK validation because they are complex rules and should be completely aligned with DRC deck. PCells also improve the layout problems which designer face while designing circuits because designer can create multiple instances by changing parameter values for one device and do circuit testing easily.

CHAPTER 8

CONCLUSION AND FUTURE SCOPE

As the node technology is decreasing day by day i.e. Beyond Moore’s law, the DRC rules are becoming more complex. Rules in the DRM are increasing at the exponential rate. Hence good quality of PDK is essential for any Designer to ensure first time silicon success. At the same time, in this cut throat competitive environment, time to market is the most essential thing for the growth of any company. PDK validation helps us to find errors before they can derail the chip and help to avoid huge loss for the company before releasing the design kit it has to be fully validated with respect to DRC and LVS. Thus, QA Cell development is of high importance to the semiconductor industry. This validation can take huge time for lower process technology node as the Rules are very complex, so there’s need for automation of the QA flow.

My work deal with the development, validation of FQA cell & Automation of QA Cell and to make it robust and all. This project is useful as it provides a good framework on how to do the Formal Quality Assurance (FQA) for the various design Kits. The QA cells can be taken as reference by the developer to develop more stringent DRC deck which in turn can increases the first time silicon success rate. These QA cells can be useful when layout engineer face any DRC or LVS issue. Also , there is one internal ST company tool named CORAIL which is used for covalidation. In place of running ARTE tool which will give result after taking 2-3 hours about the status of QA cell covered .CORAIL will run on particular top cell and it check its alignment with eDRM. It will provide the report simultaneously without waiting for the ARTE Report. This practice will further improve validation process by reducing testing time.

By using the automation, the process of validation can be made faster and the validation time required can be reduced to less than half the original time required. Thus the automation of the QA Flow can drastically reduce turnaround time (TAT).

In future PCell validation process could be automated to exhaustively check all the CDF parameters and functionality of callbacks. All the callbacks should work properly and must be validated properly. Automated flow to validate DRC Deck is required in order to reduce validation time and also work on different PDK in parallel. Apart from DRC deck validation there are various other decks that need to be verified. Automatic validation of those decks is also goal to be achieved.

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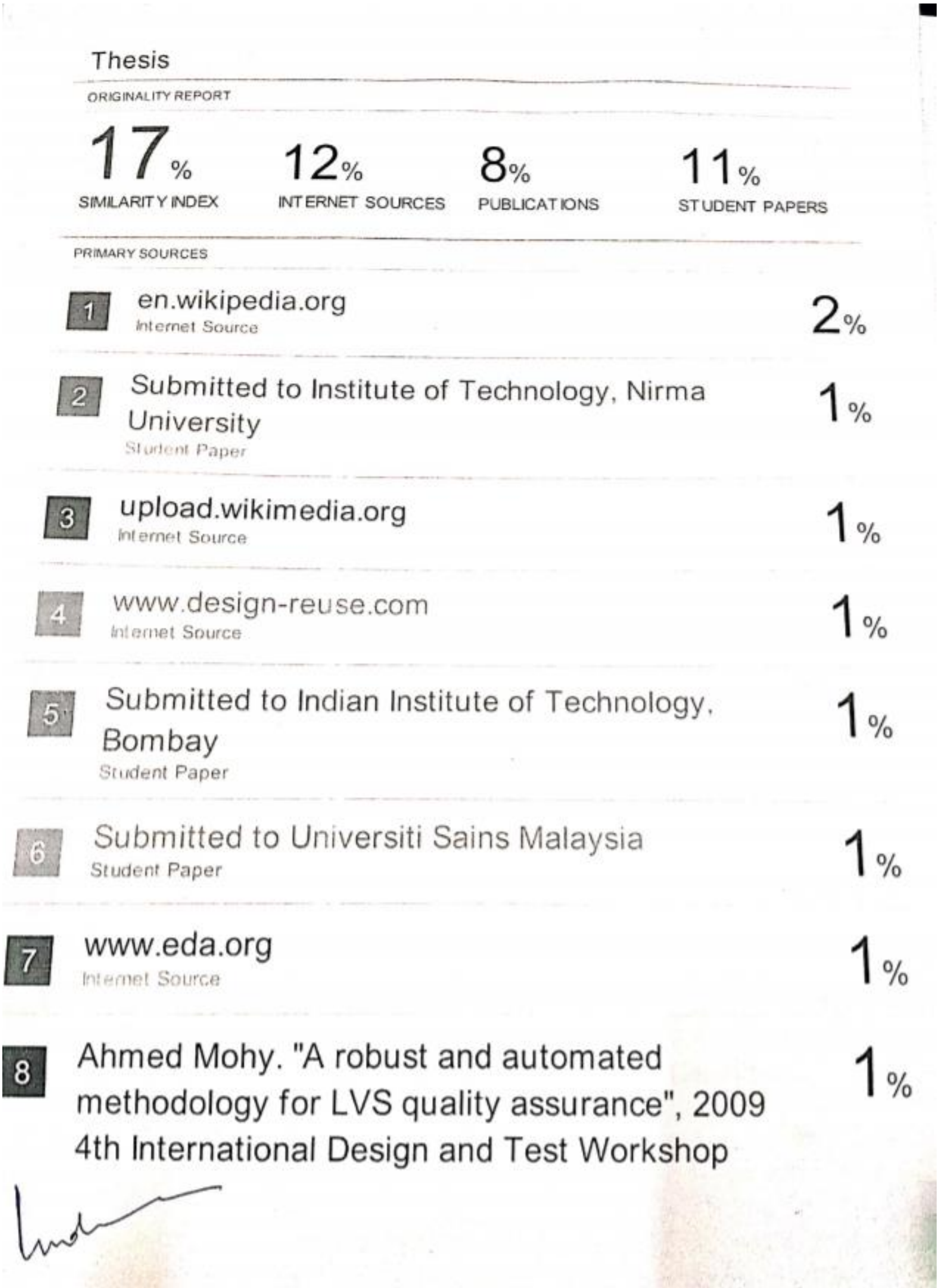

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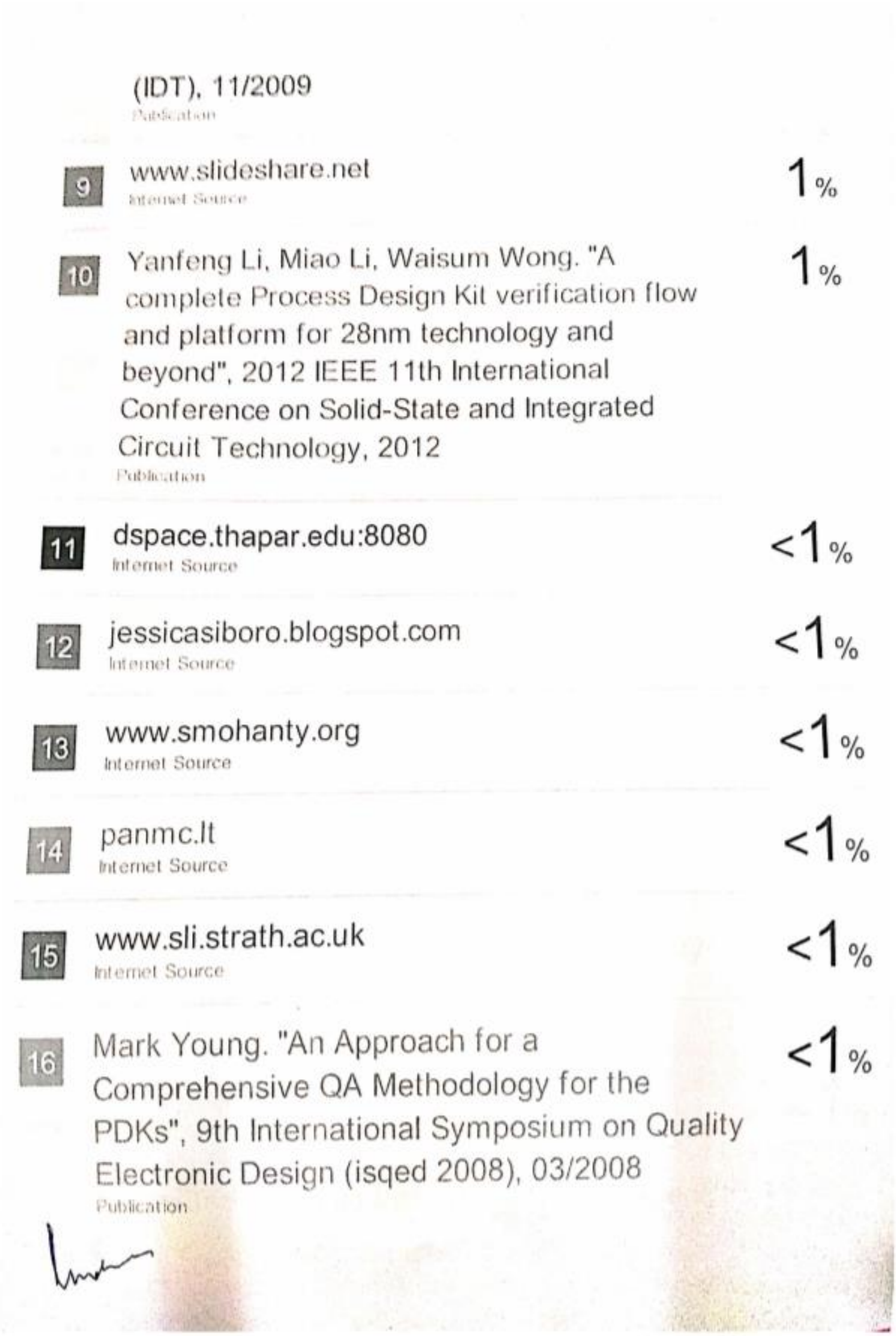

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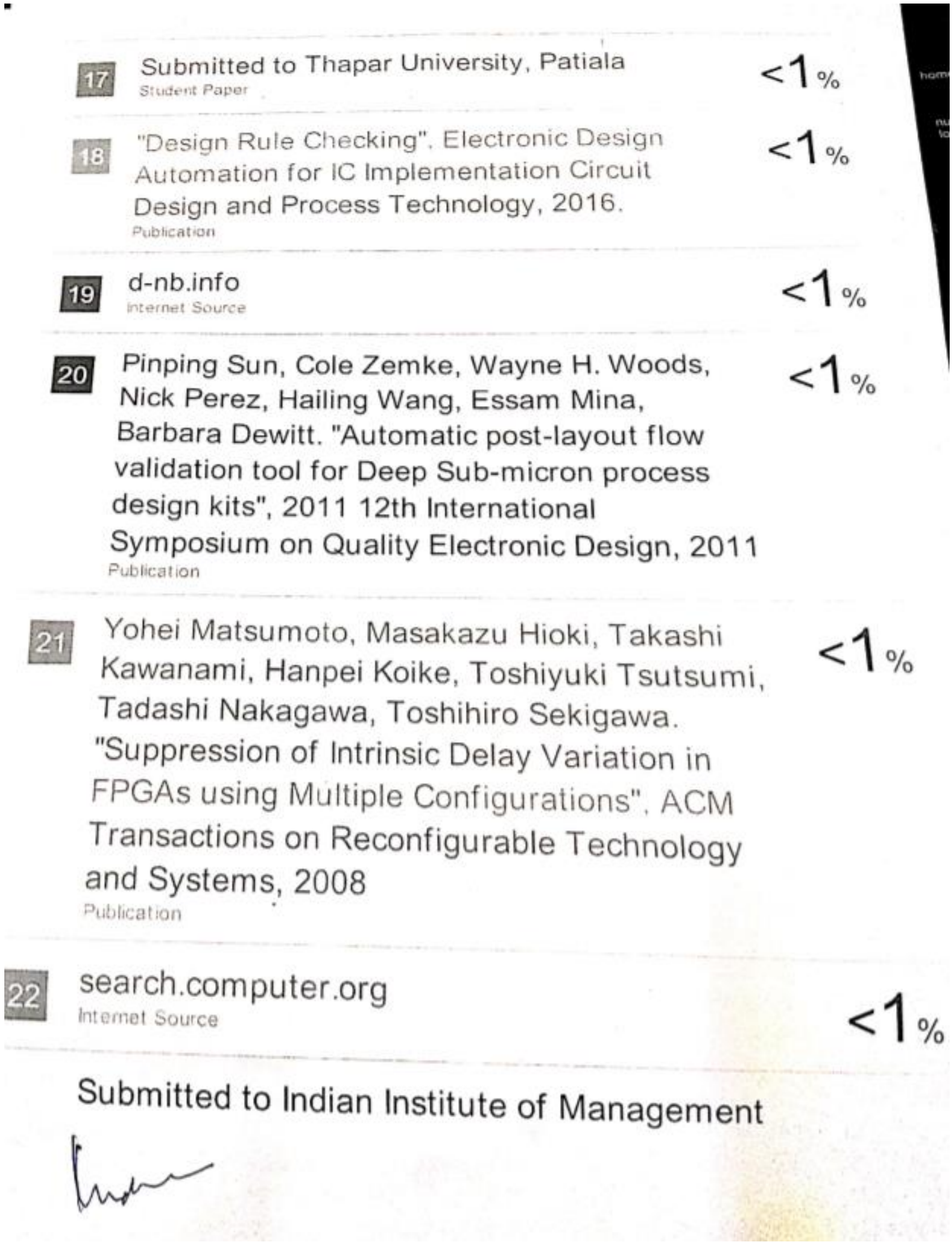

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