"STUDY THE PERFORMANCE ANALYSIS OF CARBON NANOTUBE BUNDLE INTERCONNECTS"

A dissertation Submitted towards the partial fulfillment of requirement for the award of degree of

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In
VLSI Design & CAD

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DECLARATION

I hereby declare that the work which is being presented in the dissertation entitled, **"Study the Performance Analysis of Carbon Nanotube Bundle Interconnects"** in partial fulfillment of the requirement for the award of degree of Master of Technology in VLSI Design & CAD submitted in Electronics and Communication Engineering Department of Thapar University, Patiala, is an authentic record of my own work carried out under the supervision of Mr. Mayank Kumar Rai, Assistant Professor, ECED and refers other researcher's work which are duly listed in the reference section.

The matter presented in this dissertation has not been submitted in any other University/Institute for the award of degree.

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It is certified that the above statement made by the student is correct to the best of my knowledge and belief.

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ABSTRACT

Interconnect delay is a major factor determining the performance of VLSI circuits. As technology scaled down, interconnects delay dominates the gate delay. CNTs are susceptible to electro migration problems that plague the copper interconnect. Due to high thermal conductivity and large current carrying capacity CNTs are preferred over copper as VLSI future interconnects.

In this dissertation, performance of CNT as a VLSI interconnect has been studied and results are compared with existing copper interconnects at 32nm technology node. The effects of various parameters such as interconnect length, number of repeater and size of driver transistor on propagation delay and on crosstalk noise have been analysed.

The normalized crosstalk noise is evaluated for carbon nanotube interconnects using SPICE simulation. SPICE simulation result reveals that normalized crosstalk noise increases with increase in length of interconnect and decreases with number of repeaters. The study reveals that bundle of CNT interconnect model gives better result as compared to copper in deep submicron technology for semi global and global length of interconnects.

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LIST OF SYMBOLS

V_{DD}	Positive supply voltage
I_D	Drain current
h	Planck's Constant
d	Tube diameter
L_O	Mean free path of electron
y	ILD Thickness
x	Separation between centres of two neighbouring tubes
K_p	PMOS process trans-conductance parameter
K_n	NMOS process trans-conductance parameter
W	Channel width
L	Channel length
μ_n	Mobility of electrons
μ_p	Mobility of holes
C_{OX}	Oxide capacitance
Io	Bias current
V_T	Threshold voltage
V_{GS}	Gate to source voltage
V_{DS}	Drain to source voltage
λ	Channel length modulation parameter

ABBREVIATIONS

VLSI	Very Large Scale Integration
CNT	Carbon Nanotube
IC	Integrated Circuit
ITRS	International Technology Road map for semiconductors
RLC	Resistance, Inductance and Capacitance
SWCNT	Single Wall Carbon Nanotube
MWCNT	Multi Wall Carbon Nanotube
SPICE	Simulation Program with Integrated Circuit Emphasis
MOSFET	Metal Oxide Semiconductor Field Effect Transistor
CMOS	Complementary Metal Oxide Semiconductor
NMOS	N-channel Metal Oxide Semiconductor
PMOS	P-channel Metal Oxide Semiconductor
MFP	Mean Free Path
EDA	Electronic Design Automation

CHAPTER

1 INTRODUCTION TO VLSI INTERCONNECT

Interconnects are basically the wires use to connect the components on a VLSI chip or to make the chips in VLSI circuit and connect these chips on a multiple module by using wires are referred to as interconnect. A VLSI interconnect makes from a thin film of conducting material that provides electrical connection between two or more nodes of the circuit formed in the silicon chip. Interconnect used for controlling the performance parameters of the circuit such as power, speed and noise.

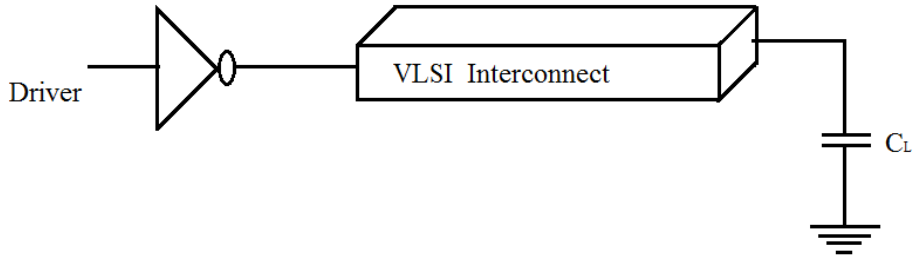

Figure 1.1 VLSI Interconnect

In deep submicron technology, a VLSI interconnect plays an important role in the performance of the circuit. Because in deep submicron technology node, associated impedance parasitics such as inductance and capacitance need to be considered. These parasitics introduce delay in a propagating signals through VLSI interconnects. As feature size of ICs will continue to diminish enforces an enhance in impurity concentration and scaling down of supply and threshold voltage to sustain the electric fields in the device. The interconnect dimensions must also reduced with the scaling of the supply voltage to take benefit of feature size scaling. As the chip size growth increase due to increase in complexity and functionality and due to scaling the capacitance and resistance of interconnect wires quickly increases. With the advancement in technology node, the feature size of ICs has been shrinking to improve the propagation delay, power consumption, silicon area and cost characteristics. The effect of technology scaling in VLSI interconnect is in the form of increased density.

This increased density results in the increasing of the coupling effect. Interconnect plays a very important role in the performance of a high-speed chip and also used to connect the different macro cells within a very large-scale integrated (VLSI) chip.

1.1 Aluminium Interconnect

Aluminium was the most commonly used material or wire until 180nm technology node. Aluminium was selected due to its good conductivity. Another useful property of aluminium is that it forms good ohmic contact with silicon. Basically, aluminium was used for global and semi global interconnects where low resistivity required. The effect of technology scaling in VLSI interconnect is in the form of increased current density. This increased density results in the increasing of the coupling effect. The disadvantage with aluminium is that at high current densities considerable electro migration takes place that means lower life time. Another material as VLSI interconnect with technology scaling is copper, which is used to solve the problem of electro migration. The choice of aluminium due to following advantages**:**

1. Good conductivity
2. Good ohmic contact with silicon.
3. Adherence on silicon dioxide and silicon.
4. Easy to purifies.

1.2 Copper Interconnect

In comparison with aluminium, copper can withstand about five times more current density for IC-applications. Copper has higher conductivity which is several times more resistant to electro migration than aluminium. Copper has a high melting point (1,357 K) than aluminium (933 K). This provides more thermal stability to copper. Due to the advantages that it offers copper became the preferred interconnect material, especially for submicron and deep submicron high density, high performance chips [1]. With decrease in cross-section copper interconnect resistivity increases due to surface roughness and grain boundary scattering, causing increase in propagation delay, power dissipation and electro migration. The existing interconnects material problems are electro migration and grain boundary scattering. A grain boundary is interface between two grains in a polycrystalline material. Due to grain boundary scattering, resistivity of copper interconnect increases which results in increasing the propagation delay. Electro migration is caused by the gradual movement of the ions in a conductor due to the transfer of energy between the conducting electrons and diffusing metal atoms. Electro

migration degrades the performance by reducing the reliability of circuit and also concluding the loss of connections or failure of an integrated circuit(IC). To alleviate this problem, for interconnects of future generation chips alternative solutions are under consideration. The most appropriate alternative for copper interconnects turns out to be Carbon Nanotube (CNT) [2]. With continuous reduction of feature size there has been a parallel increase in die size. The result is more and more increase in length of some of the on chip interconnects as technology scaling continues. Based on their length interconnects are categorized as local, semi-global and global.

1.3 Types of Interconnects

1.Local (short) interconnects

2.Semi-global (intermediate length) interconnects

3.Global (long) interconnects

1. Local (short) interconnects: - As the name indicates local interconnects used for localized region of a chip to provide electrical path between different nodes.

2. Semi-global (intermediate length) interconnects:-The semi-global are positioned between the local and global type interconnects and having the intermediate lengths between these interconnects.

3. Global (long) interconnects:-The global interconnects as the name suggests, provide electrical paths over considerable length of the chip. Its die size is long.

As device density increased with technology scaling, interconnect current density increased. This increased density results in the increasing of the coupling effect. Another potential material as VLSI interconnect in deep submicron is carbon nanotube (CNT) [1].

1.4 What are Carbon Nanotubes?

Carbon-Nanotubes (CNTs) are allotropes of carbon. These are extremely thin hollow cylinders made of carbon atoms. Carbon nanotubes are basically the wires make from pure carbon with diameters in the range of nanometer and lengths of many microns. CNTs are made by using the graphene sheet and rolled this sheet in a form of cylinder with a proper chirality and diameter of these cylinders in the order of nanometer.

1.4.1 Classification of Carbon Nanotubes

On the basis of Conductivity, chirality and layers, CNT can be classify in mainly three categories.

- **Based on Conductivity:**
  - Metallic
  - Semiconducting
- **Based on Chirality:**
  - Zigzag
  - Armchair
  - Chiral.
- **Based on layers:**
  - Single-walled Carbon nanotube (SWCNT)
  - Multi-walled Carbon nanotube (MWCNT)

Carbon nanotubes (CNTs) are recently discovered materials considered as an another potential material in deep submicron technology for future nano electronic applications, such as transistors, antennas, filters and VLSI interconnects [3]. A single walled carbon nanotube (SWCNT) may be thought of as a single atomic layer thick sheet of graphite (called graphene) rolled into a seamless cylinder. Multi -walled carbon nanotubes (MWCNT) consist of several concentric nanotube shells. There are some CNTs which consist of a multiple of concentric SWCNT like graphene tubes. These are termed MWCNT. Out of these two types, the SWCNTs are preferable for use as interconnect. A single tube of SWCNT is not a good choice for use as interconnect due to its large resistance. Alternatively, a parallel connection of a large number of SWCNTs can be used and each nanotube has four conducting channels in parallel. Such SWCNTs-bundles have proven to be of lower resistance than Cu-interconnects at advanced VLSI technology nodes [4].

Table1.1 Properties of CNTs compared to copper [3].

Property	CNT	Cu
Maximum current density[A/am^2]	~10^{10}	~10^6
Thermal Conductivity [W/mK]	~6000	~400
Mean free path [nm]	~1000	~40

1.5 Scaling of Device and Interconnect Lines

The area occupied by a MOS transistor can be made smaller by shortning its channel width and length. Based on constant field scaling table is suggested (ideal scaling) [15].

Table 1.2 Scaling of Interconnects.

Device/Circuit parameter	Scaling factor
Dimensions w, L	1/S
Voltage	1/S
Field	1
Gate delay	1
Line resistance	S
Line capacitance	1/S

1.6 Role of Repeater

Both capacitance and resistance increase linearly with length of the interconnect; therefore propagation delay increases as the square of the interconnection length when the resistance of the interconnection is comparable to or larger than the on-resistance of the driver. The uses of repeaters reduce the delay by dividing the interconnection into smaller subsections. Repeater insertion is a technique use to reduce the time delay associated with long wire lines in VLSI chips. This technique involves the division of long wire interconnect into smaller segments/sections and inserting a repeater between each new pair of short wire. It can also be done by inserting a buffer at the beginning and at the end of the interconnect line to improve the delay and slew rate of the signal. The propagation delay of interconnects is a major factor determining the performance of VLSI circuits, because the RC time constant of interconnects increases very rapidly as chip and interconnect dimensions are scaled aggressively. As the chip dimension increases and the minimum feature size decreases, the propagation delay rises rapidly.
To reduce interconnect time delay, properly-scaled multilevel conductors, repeaters, cascaded drivers, and cascaded drivers as repeaters are presented [5].

1.7 Types of Repeaters

According to Bakoglu and Mendl, the propagation delay of interconnect with k minimum sized inverters is given as

$$T = k(2.3\frac{R_0}{h}\left(\frac{C_{int}}{k} + hC_0\right) + \frac{R_{int}}{k}\left(\frac{C_{int}}{k} + 2.3hC_0\right))$$

If the delay of the segments connected by the repeaters is made equal to that of a repeater then shortest total delay can be achieved [5].

No. of repeaters is given by- $$k = \sqrt{\frac{R_{int}C_{int}}{2.3\ R_0C_0}}$$

For long-distance interconnections, C_{int} is on the order of picofarads and C_o is on the order of femtofarads, and R_{int} and R_{tr}, have values around kilohms; therefore, RoCint >>RintCo, and the delay expression can be further simplified to $T=2.3R_oC_{int}$.

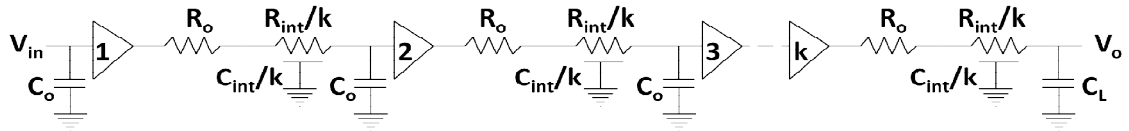

Figure 1.2 Minimum Size Repeaters [5].

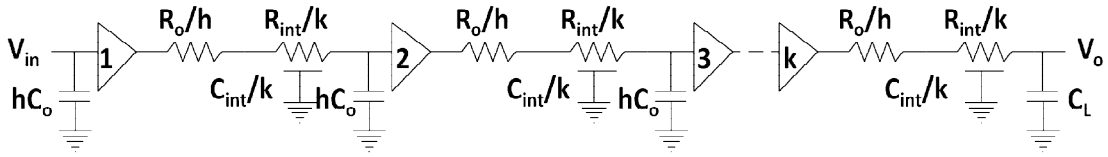

Figure 1.3 Optimal Repeaters [5].

To drive the large capacitive loads cascaded drivers are good option as repeaters are good option to dive the large RC loads. To improve the driver circuit through cascaded drivers that increase in size until the last device was large enough to drive the line and/or by using a chain of drivers instead of single minimum-size driver. When structure is driven by a minimum-size transistor then to optimize the total propagation delay and also to lower the input capacitance of the structure, the first stage of the optimal-size repeaters must be a cascaded driver as shown in figure 1.4 [5].

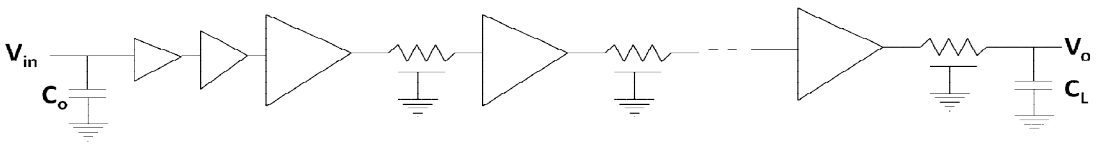

Figure 1.4 Optimal Repeaters with a cascaded stage first [5].

1.8 Interconnect Model

1.8.1 The Lumped RC Model

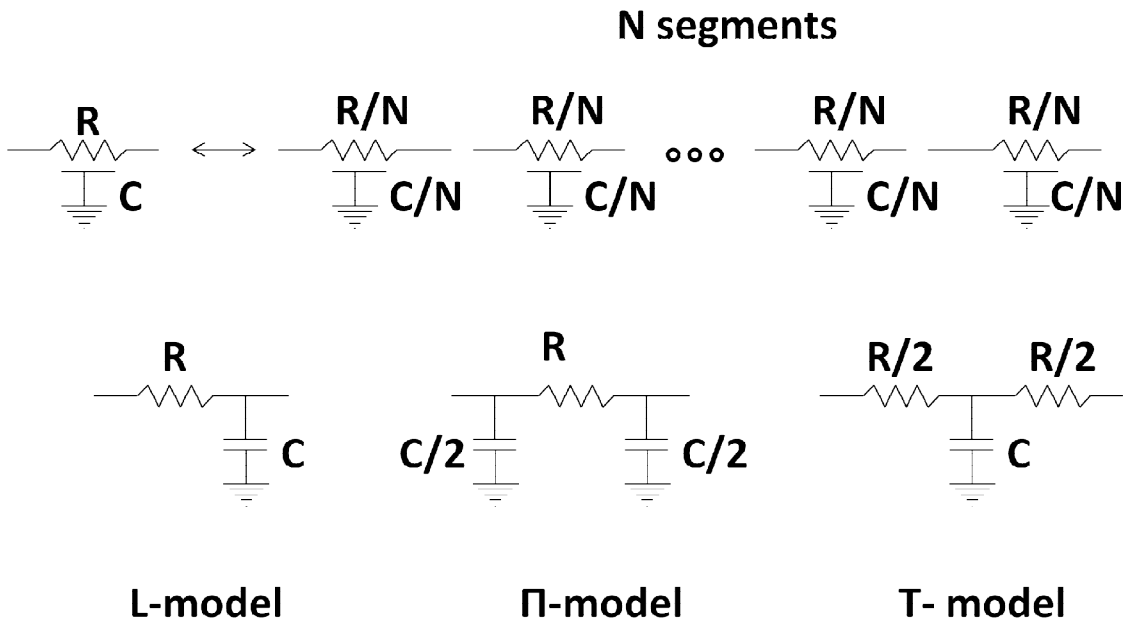

Figure 1.5 Different configuration of RC interconnect models

Figure 1.5 shows the different configurations of RC interconnect models. These are L-model, T-model and Π-model. To make the distributed configuration, RC model is divided into N-segments. Khang and Muddu proposed a pi model for distributed RLC interconnect to estimate the driving output admittance at the output of a CMOS gate [16].

1.8.2 Distributed RLC model

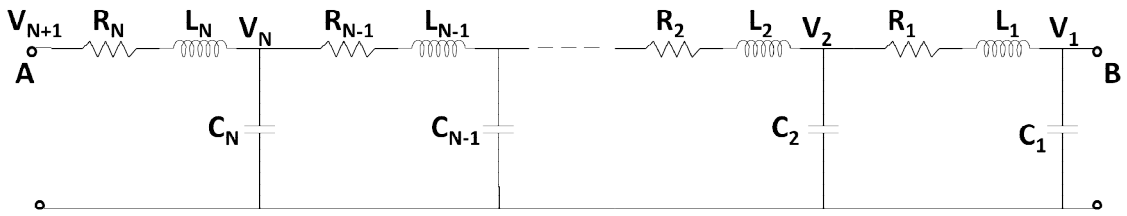

Figure 1.6 Distributed RLC model with N-segments [16].

The distributed RLC line can be approximated by a lumped multi-stage RLC ladder network and individual element is given by-

$$R_N = \frac{R}{N}, \quad L_N = \frac{L}{N}, \; C_N = \frac{C}{N}$$

CHAPTER 2

LITERATURE REVIEW

Introduction:

Interconnects are basically the wires use to connect the components on a VLSI chip or to make the chips in VLSI circuit and connect these chips on a multiple module by using wires (interconnect). A VLSI interconnect makes from a thin film of conducting material that provides electrical connection between two or more nodes of the circuit formed in the silicon chip. Interconnect used for controlling the performance parameters of the circuit such as power, speed and noise.

2.1 Interconnect Delay Models

Bakoglu and Meindl [5] developed a model for interconnection time delay that include the effects of scaling transistor, interconnection and chip dimensions. The delays of aluminium, WSi2 and poly silicon lines were compared. With the technology scaled chip dimension increases which decrease the minimum feature size, R_{int} becomes important and delay rises quickly. So, the major challenges were to minimize the capacitances and resistances to reduce the delay. Therefore, two techniques to shortening the delay were investigated. The first was to reduce the interconnection resistance by using only aluminum lines for long-distance communication and by forming multilayers of interconnections with thicker and wider lines in the upper levels. The second was to improve the driver circuit through cascaded drivers that increase in size until the last device was large enough to drive the line and/or by using repeaters that divide the interconnections into smaller subsections.

Mayank Kumar Rai and Sarkar [2] compare the resistance of copper interconnect with CNT interconnect. As the process technology scales down in order to provide sufficient current and to minimize the electro migration, the conductor height-to-width aspect ratio of traditional copper interconnect continues to increase. Since the CNTs can reliably

handle three orders of magnitude larger current densities than copper conductor, CNTs-based interconnects potentially provide larger benefits in area.

Naeemi et al. [9] compare the study of copper interconnect with CNT interconnect. As interconnect feature sizes shrink, due to surface and grain boundary scatterings, resistivity of copper increases and surface roughness also increases. Furthermore, wires, especially power and ground lines are becoming more and more susceptible to electro migration because of quick increases in current densities. In contrast, carbon nanotubes exhibit ballistic flow of electrons with electron mean free paths of several microns, and are capable of conducting very large current densities. Carbon nanotubes are therefore proposed as potential candidates for power and signal interconnection.

Sarkar et al. [1] study of different Propagation delay model and power dissipation in CNT interconnect for 32nm and 22nm technology nodes.

(a) For 32nm technology node: As the tube diameter is increased the capacitance dominates till a critical diameter is reached. Beyond this critical diameter resistance takes over. Briefly, for good performance, the optimum tube diameter should be selected if possible (32nm). Otherwise tube diameter should be restricted (22 nm).

(b) For 22nm technology node: As diameter is increased delay gradually rise indicate dominance of CNT resistance over its capacitance.

(c) Power dissipation decreases as increase in tube diameter due to the dominance of the capacitance.

Kadir and Hasan, [10] proposed that each new semiconductor technology node brings smaller transistors and wires. Although this makes transistors faster, wires get slower. In nano-scale regime, the standard copper (Cu) interconnect will become a major hurdle for FPGA interconnect due to their high resistivity and electro migration. study the performance comparison of CNT and Cu interconnect for target FPGA. The parameters (R, L, C) of interconnect were extracted, using the Carbon Nanotubes Interconnect Analyzer (CNIA) and BPTM tools, with interconnect geometry. The segment length (between two CLB tile) for 32nm technology node considered is 17.7um.

Mayank Kumar Rai and sarkar [4] reported the effect of tube diameter on delay and power dissipation on CNT bundle interconnect performance and also reveal that the effect of resistance in deep submicron region for both CNT and Copper. It was concluded that resistance of Cu interconnect increases with decrease in technology due to electron

migration and grain boundary effect, where as in CNT resistance increases marginally with lower technology.

Saraswat et al. [11] proposed that for local Cu and CNT interconnects, the driver resistance dominates the wire resistance, hence the delay is determined by the driver resistance and the wire capacitance. CNT delay is consistently lower. Both interconnects exhibit optimum aspect ratio (AR) minimizing delay (reflecting wire capacitance minimum). The maximum electro migration limit for Cu limits it's AR to ~ 1.5, preventing it from achieving optimum AR for delay minimization. CNTs do not have this limit (Jmax~109 A/cm2). Thus, CNT delay is not only intrinsically superior but its better reliability results in a design optimization, which gives it an additional delay advantage over Cu. For CNTs and Cu, latency increases with technology scaling due to a higher resistance.

El-Moursy and Friedman **[12]:** In this paper, authors discussed the concept of interconnect tapering to minimize the transient power dissipation and proposed an optimum tapered structure for RLC interconnect. The reduction in line resistance (with increasing wire width) decreases the signal attenuation along the line, improving the signal transition time. The same criterion can be used to reduce the power dissipated by a load driven by a tapered interconnect line. Results show that wire tapering can reduce the power dissipated by a circuit up to 72% as compared to uniform wire sizing.

Srivastava et al. [13] proposed that CNT interconnects can provide 30%–40% improvement in the delay of millimetre long global interconnects. Dense CNT bundle global interconnects are shown to offer a 4 times reduction in power dissipation while achieving the same delay as optimally buffered Cu interconnects at the 22 nm node. This power saving increases to 8 times at the 14 nm node.

Li and Banerjee [14] proposed that due to the presence of large kinetic inductance in each CNT, the skin effect in CNT bundles is significantly reduced compared to that in conventional conductors. Particularly, MWCNTs could offer significant advantages in high-frequency applications, since they exhibit much reduced skin effect in comparison to SWCNTs and are also known to offer comparable circuit performance with that of SWCNTs due to low dc resistivity. This preferable high-frequency property of CNTs is then explored in the design and analysis of high-performance on-chip inductors. It has been demonstrated that the *Q* factor of CNT-based inductors could be as high as 3.3 times

compared to those based on Cu without using any magnetic materials or any optimization techniques.

2.2 Interconnect Crosstalk Models

Rossi et al. [6] proposed a novel RLC equivalent model for CNT bus architecture made of parallel single-walled nanotubes and a single multi-walled nanotube. The proposed bus architecture is made of dual-walled nanotubes arranged in parallel. The effects of crosstalk on performance are evaluated by simulaton. Author reported a significant reduction up to 59% for the crosstalk-induced delay and up to 81% for the crosstalk-induced peak voltage. Thus, shows improvement in the circuit performance with the proposed CNT bus architecture.

Das and Rahamam [8] developed an equivalent circuit of the existing model of CNT to perform the crosstalk analysis for SWCNT bundle and MWCNT bundles based VLSI interconnects. The impact of crosstalk on gate oxide reliability in terms of failure-in-time (FIT) rate is calculated and comparisons are made with copper based interconnect. The results show that the CNT based interconnects are more suitable in VLSI circuits as far as the gate oxide reliability is concerned.

The conventional PDP criteria, is used to calculate appropriate number of repeaters in long interconnects, reduces the propagation delay and crosstalk in coupled interconnects at the cost of increase in the power dissipation. ***Kaushik et al.*** [20] proposed a novel concept of Power-Delay-Crosstalk Product (PDCP) to calculate the efficient number of repeaters in interconnects so that minimum power-delay product could be achieved in the interconnect. Author compared the performance of the PDCP criteria with the conventional PDP criteria in terms of optimum number of repeaters, power dissipation, propagation delay and crosstalk for a wide range of coupling combinations. Results show that PDCP criteria is best suited to find optimum number of repeaters.

CHAPTER

3

SWCNT AS VLSI INTERCONNECT

Introduction

The analysis of copper and one dimensional CNT bundle as interconnects for VLSI circuit is done in the chapter. Model is developed to calculate equivalent circuit parameters for a CNT bundle and copper based on interconnect geometry. This delay analysis is done using Tanner EDA tools in which simulation is done with the equivalent circuit SPICE files. An isolated SWCNT is prefer in compare to MWCNT interconnect. The separation between the nanotube and the ground is y and the diameter of the SWCNT is d. If a 1-D system has N conducting channels in parallel then its resistance is h/Ne^2T. Where h is Planks constant, e is electron charge and T is electron transmission coefficient. Due to spin and sub lattice degeneracy of electrons there are 4 parallel conducting channel in SWCNT (N=4). Thus assuming perfect contacts (T=1), the resistance of an SWCNT is $h/4e^2$. With the values of the physical constants substituted the resistance assumes the fairly large value of 6.45 KΩ. In this resistance (R_f) is equally divided between the contacts at the two ends of the nanotube.

If the tube length (L) is larger than mean free path then enhancement of scattering gives rise to an addition in the resistance increases with increase in CNT length. A SWCNTs-bundle interconnect provides this advantage at the semi-global and global levels of length. The metallic CNTs are attractive interconnect materials because of their high thermal and mechanical stability, thermal conductivity as high as 5800W/mK, ability to carry current in excess of 10^{14}A/m2 current density even at temperatures higher than 200°C and Fermi velocity comparable with that of a metal. It is very difficult to make a good contact with a CNT. CNT resistances in the range 7 KΩ - 100 KΩ have been reported [2].

An isolated CNT is not preferred to use as a interconnect due to its high resistance. To understand the electronic properties of the graphene sheet helps to understand the electronic properties of carbon nanotubes. Graphene is a zero-gap semiconductor; for most directions in the graphene sheet, there is a band gap, and electrons are not free to flow along those directions unless they are given extra energy. However, electrons flow easily along directions when graphene is metallic. This property is not obvious in bulk graphite, since there is always a conducting metallic path which can connect any two points, and hence graphite conducts electricity. To make the nanotube graphene is rolled up and a special direction is selected along the axis of the nanotube. Sometimes this is a metallic direction, and sometimes it is semiconducting, so some nanotubes are metals, and others are semiconductors. Since both metals and semiconductors can be made from the same all carbon system, nanotubes are ideal candidates for molecular electronics technologies.

3.1 Equivalent Circuit Parameters of Copper Interconnect

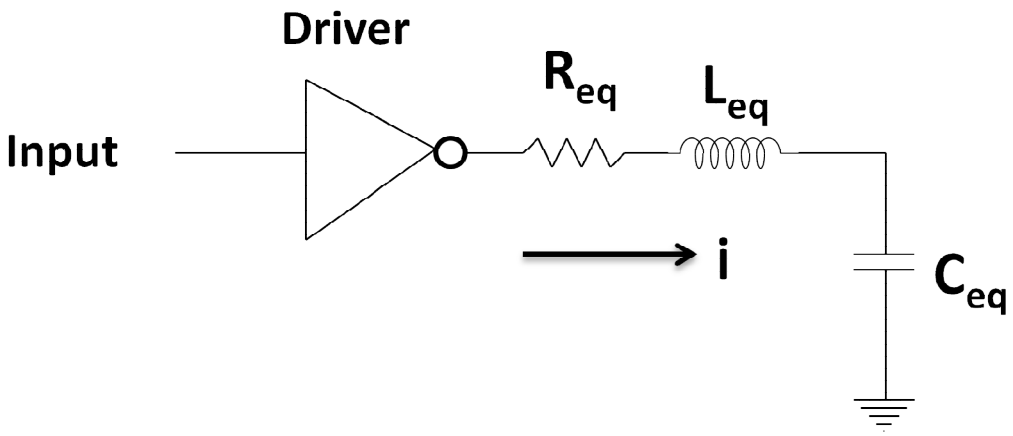

Figure 3.1 Equivalent Circuit model of copper interconnect

According to the model, the thickness of the interconnect is t, the width of interconnect is w, and h is the height of the interconnect above the ground.

3.1.1 Equivalent Resistance

Based on this model, the resistance of a copper interconnect of length L is given by:

$$R = \frac{\rho l}{wt}$$

Where ρ is the resistivity of copper.

3.1.2 Equivalent Capacitance

The total effective capacitance of the copper interconnect is given by

$$C_g = \epsilon\left[\frac{w}{h} + \left\{2.22\left(\frac{s}{s + .7h}\right)^{3.19}\right\} + \left\{1.17\left(\frac{s}{s + 1.51h}\right)^{0.76}\left(\frac{t}{t + 4.53h}\right)^{0.12}\right\}\right]$$

Where ε is the dielectric permittivity; and ε_r is the relative dielectric permittivity of copper.

$$\varepsilon = \varepsilon_r \times 8.86 \times 10^{-12}$$

Thickness t is determined by t = 3 × W (width of interconnect)

3.1.3 Equivalent Inductance

Inductance associated with copper interconnect is given by the following expression:

$$L_s = \frac{\mu_0 l}{2\pi}\left[\ln\left(\frac{2l}{w + t}\right) + \frac{1}{2} + \frac{.22(w + t)}{l}\right]$$

Where μ_o is the permeability and given as $\mu_o = 4\pi \times 10\text{-}7$

3.2 Equivalent Circuit Parameters of CNT Interconnect

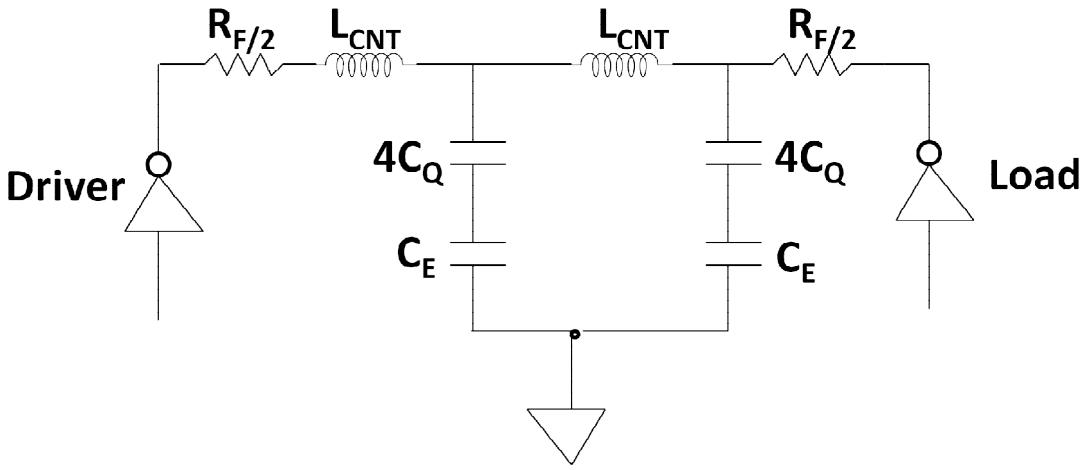

Figure 3.2 - Equivalent RLC circuit for an isolated SWCNT [2].

3.2.1 Resistance of Isolated SWCNT

The resistance of equivalent circuit for length of interconnect (L) is less than mean free of electron (λ_{CNT}) is [2].

$$R_f = \frac{h}{4e^2}$$

If the length of CNT is greater that mean free path of electron then resistance is given as [1, 2].

$$R_{CNT} = \frac{h}{4e^2}\frac{L}{L0}$$

The resistance of a CNT has three components: the fundamental resistance R_f, the scattering resistance R_{CNT} and the contact resistance at the two ends of the tube [1, 9].

3.2.2 Capacitance of Isolated SWCNT

CNT has two capacitances of different origins. One is electrostatic capacitance and the other quantum capacitance. The electrostatic capacitance (C_E) is due to charge stored by the CNT- ground plane system and is given by -

$$C_E = \frac{2\pi\epsilon}{\ln [y/d]}$$

This is per unit length of Nano Tube. The quantum capacitance (C_q) accounts for the quantum electrostatic energy stored in the nanotube when it carries current [1,2]. It is given as

$$C_q = \frac{2e^2}{hv_f}$$

where v_f is the Fermi velocity. As CNTs have four conducting channels, total effective quantum capacitance resulting from four parallel channels is $4C_q$. When current flows both C_E and $4C_q$ carry same charge. Thus the two capacitances appear in series in the isolated SWCNT equivalent circuit

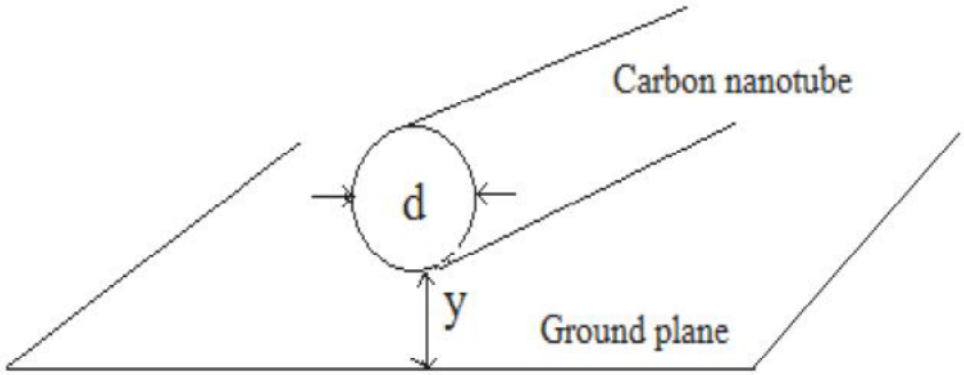

Figure 3.3 - Carbon nanotube, of diameter ‘d’ and distance ‘y’ below ground [2].

3.2.3 Inductance of an Isolated SWCNT

For a SWCNT, there are two types of inductances termed magnetic inductance and kinetic inductance. Magnetic inductance (L_M) is due to the total magnetic energy resulting from the current flowing in the wire. The kinetic inductance (L_k) arises from

kinetic energy stored in each conducting channel of the CNT. The four parallel conducting channels in a CNT results in an effective kinetic inductance of $L_k/4$ [1,2]. The expressions for L_M and L_k are –

$$L_k = \frac{\mu}{2\pi} \ln (y/d)$$

$$L_M = \frac{h}{(v_f)2e^2}$$

3.3 Equivalent Circuit Parameters for a Bundle of SWCNTs

The expressions to calculate the number of CNTs in the bundle are shown in following equations where n_H is the number of "rows" in the interconnect bundle, nw is the number of "columns" n_{CNT} is the total number of CNTs and denotes the largest integer less than or equal to '*y*'.

Number of rows in interconnect bundle is given by

$$n_W = \left\lfloor \frac{w-d}{s} \right\rfloor$$

Number of columns in interconnect bundle is given by

$$n_H = \left\lfloor \frac{h-d}{(\sqrt{\frac{3}{2}})s} \right\rfloor + 1$$

Therefore number of CNT used in the interconnect bundle is given by the following equation [2]. If number of rows nH in the CNT bundle is even, the number of CNT used is given by

$$n_{CNT} = n_W n_H - \frac{n_H}{2}$$

If number of rows n_H in the CNT bundle is odd, the number of CNT used is given by

$$n_{CNT} = n_W n_H - \frac{n_H - 1}{2}$$

3.3.1 Resistance of CNT Bundle

In order to calculate the effective resistance of a CNT bundle, it is assumed that all CNTs packed into the interconnect structure are metallic and conducting. The CNT-bundle

resistance is then given by following Equation, where Risolated is the resistance of an isolated CNT and n_{CNT} is the total number of CNTs forming the bundle [1,2].

$$R_{CNT}(bundle) = \frac{h}{4e^2}\frac{L}{L_0}/n_{CNT}$$

3.3.2 Capacitance of CNT Bundle

CNT bundle is given by-

$$C(bundle) = \frac{C_E^{bundle} . C_q^{bundle}}{C_E^{bundle} + C_q^{bundle}}$$

where

$$C_E^{bundle} = 2C_{En} + \frac{n_W - 2}{2} C_{Ef} + \frac{3(n_H - 2)}{5} C_{En}$$

Where C_{En} and C_{Ef} are the intrinsic plate capacitances calculated for an isolated CNT over a ground plane. C_{En} is calculated assuming the ground plane to be at a distance equal to the separation distance 's' from the adjacent interconnect [1,2].

$$C_{En} = \frac{2\pi\epsilon}{\ln\left(\frac{s}{d}\right)}$$

C_{Ef} is calculated assuming the ground plane to be at a distance equal to the separation distance 's+w' from the "far" adjacent interconnect.

$$C_{Ef} = \frac{2\pi\epsilon}{\ln\left(\frac{s+w}{d}\right)}$$

Quantum capacitance of the bundle is given by the following expression:

$$C_Q^{bundle} = C_Q^{CNT} . n_{CNT}$$

3.3.3 Inductance of CNT Bundle

The inductance of a CNT bundle is given by the parallel combination of the inductances corresponding to each CNT forming the bundle where LCNT is the (magnetic) inductance of an isolated SWCNT. The inductance of CNT bundle is given by [1, 2]:

$$L(bundle) = \frac{L_M + L_K}{4n_{CNT}}$$

3.4 Impedance Analysis

The Figure 3.4 - 3.8 show the effect of the interconnect length on impedance parameter for CNT and Copper interconnect. The impedance parameters of CNT bundle and copper are calculated from the models available in [4, 25]. As the length of interconnect increases, all impedance parameters of the carbon nanotube increases.

Table 3.1 Comparison of CNT bundle and copper resistance at different length of interconnect.

	Resistance (ohm)	
Length of Interconnect (μm)	CNT	Cu
100	83.56	509.25
400	334.24	2037.04
700	584.92	3564.814
1000	835.601	5092.59

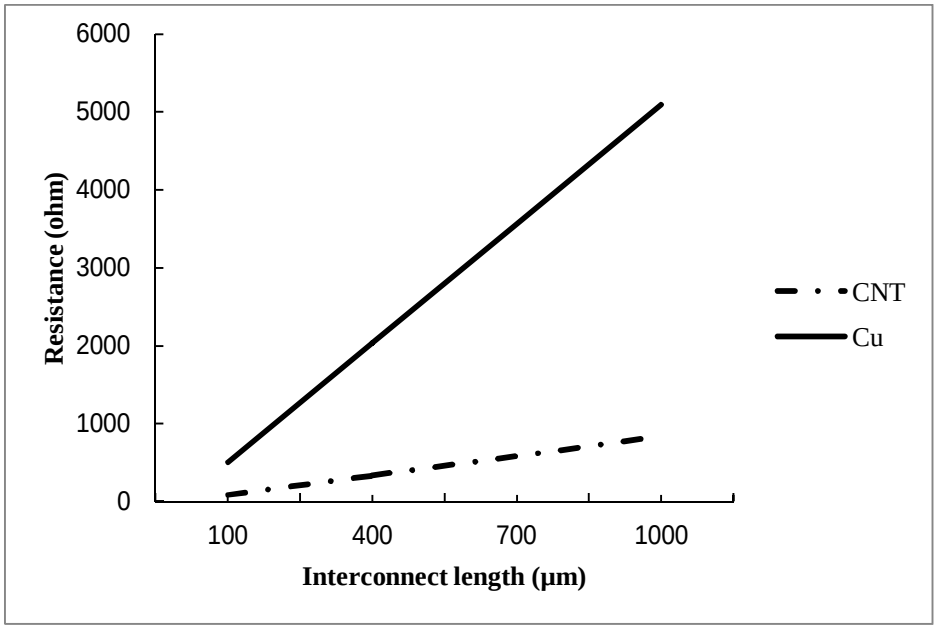

Figure 3.4 Resistance versus Interconnect length for CNT and copper.

The Figure 3.4 draw the comparison of resistance of CNT bundle and copper with variation in the length of the interconnect. As interconnect length increases, resistances of CNT bundle and copper increases and resistances of carbon nanotube is much lower than copper. Therefore, propagation delay is also low in carbon nanotube in compare to copper interconnect due to dominance of resistance in delay.

Table 3.2 CNT bundle inductance at different length of interconnect.

Length of Interconnect (μm)	Inductance (fH)
100	12.18
400	48.75
700	85.318
1000	121.88

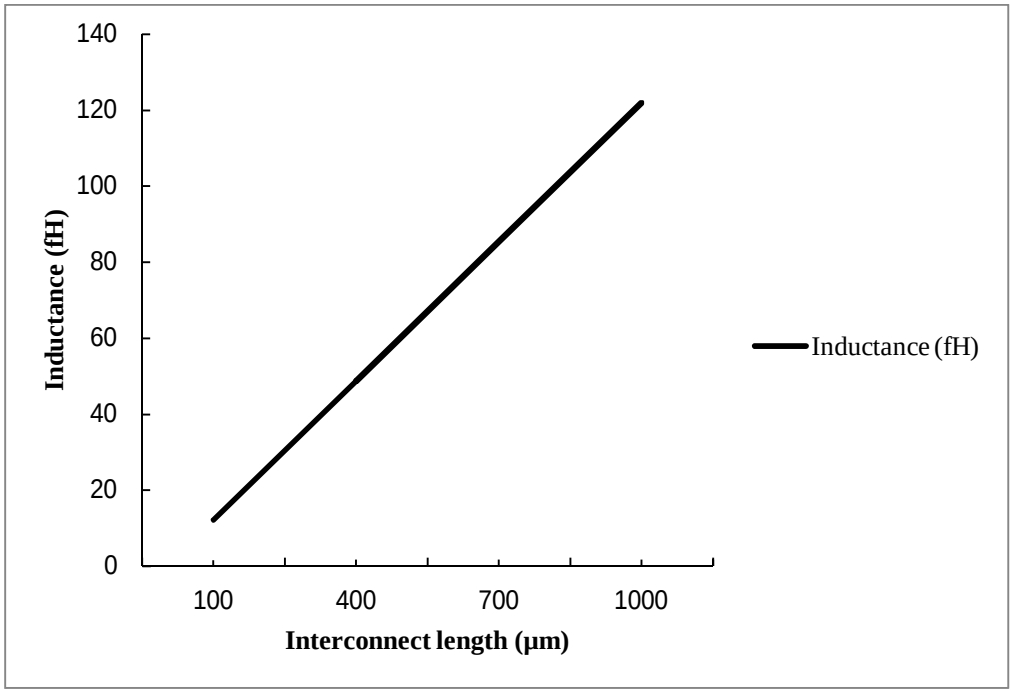

Figure 3.5 Inductance versus Interconnect length for CNT bundle.

The Figure 3.5 shows the variation of inductance with interconnect length for CNT bundle interconnects. As the length of interconnect increases, inductance increases rapidly.

Table 3.3 CNT bundle capacitance at different length of interconnect.

Length of Interconnect (μm)	Capacitance (pF)
100	0.385
400	1.53
700	2.69
1000	3.85

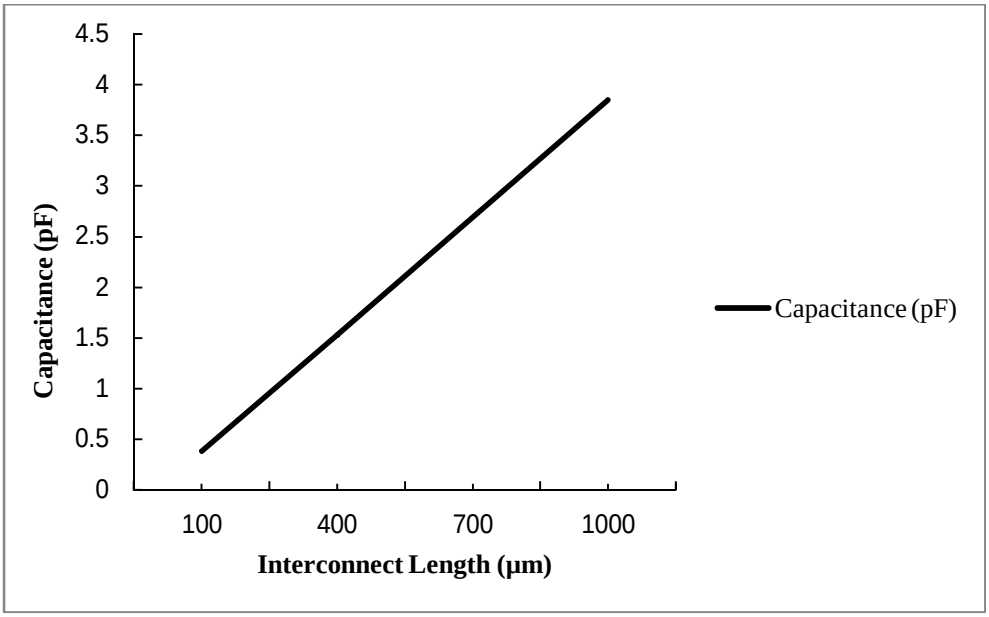

Figure 3.6 Capacitance versus Interconnect length for CNT bundle.

The Figure 3.6 shows the variation of capacitance with interconnect length for CNT bundle interconnects. As the length of interconnect increases, capacitance increases rapidly. Therefore, power dissipation is also high in carbon nanotube as compared to copper interconnect.

Table 3.4 Copper inductance at different length of interconnect.

Length of Interconnect (µm)	Inductance (pH)
100	148.98
400	706.79
700	1315.24
1000	1950.24

The Figure 3.7 shows the effect of interconnect length on inductance for copper based interconnect. As the length of interconnect increases, inductance increases exponentially and is much large than CNT bundle interconnect.

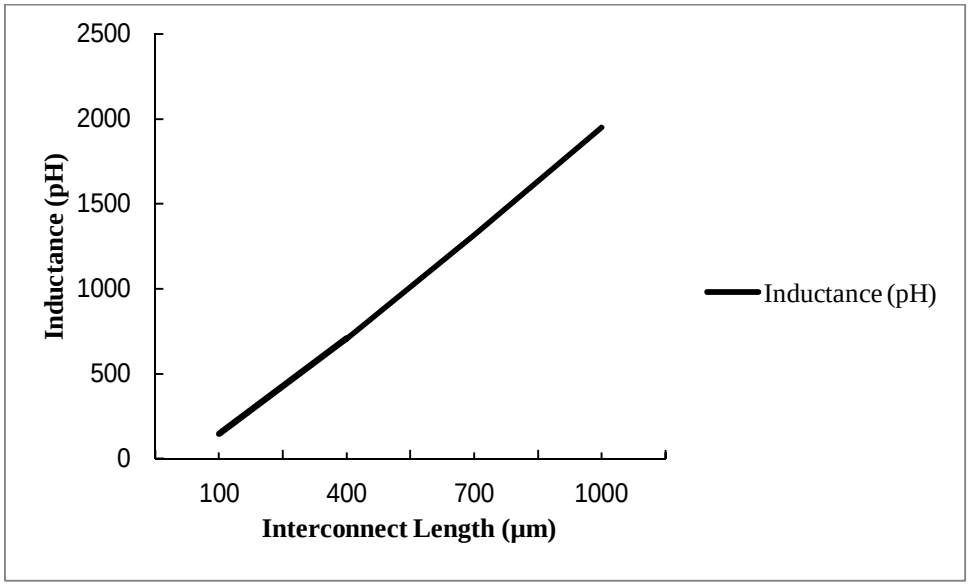

Figure 3.7 Inductance versus Interconnect length for copper.

Table 3.5 Copper capacitance at different length of interconnect.

Length of Interconnect (µm)	Capacitance (fF)
100	1.69
400	6.79
700	11.874
1000	16.96

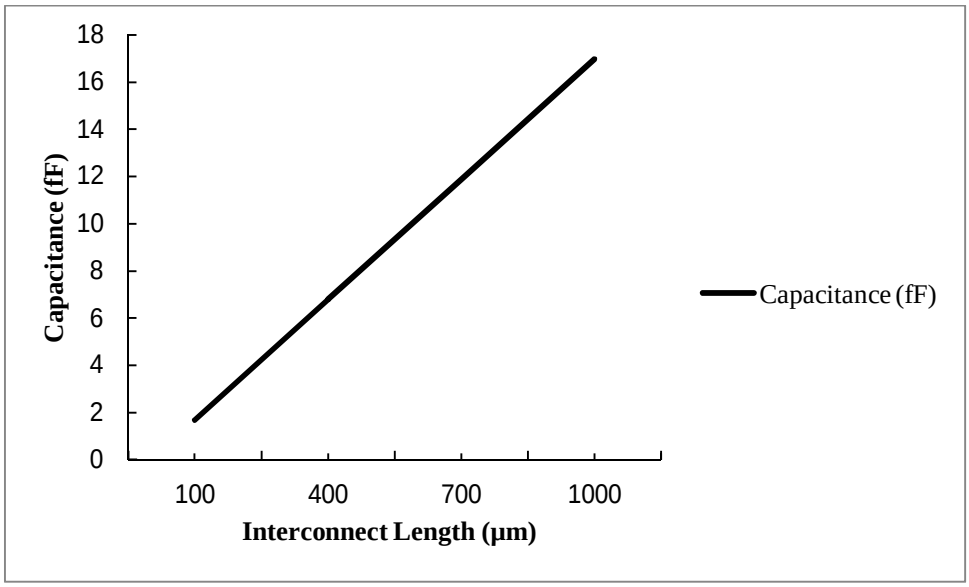

Figure 3.8 Capacitance versus Interconnect length for copper.

The Figure 3.8 shows the effect of interconnect length on capacitance for copper based interconnect. As the length of interconnect increases, inductance increases exponentially

and is much lower than CNT bundle interconnect. Therefore, power dissipation is also low in copper interconnect as compared to CNT bundle interconnect.

Table 3.6 Nor. resistance, inductance and capacitance for CNT bundle at different interconnect length.

Length of Interconnect (μm)	Nor. Resistance	Nor. Inductance	Nor. Capacitance
100	1	1	1
400	1.154	1.358	7.498
700	2.019	2.377	13.18
1000	2.885	3.395	18.868

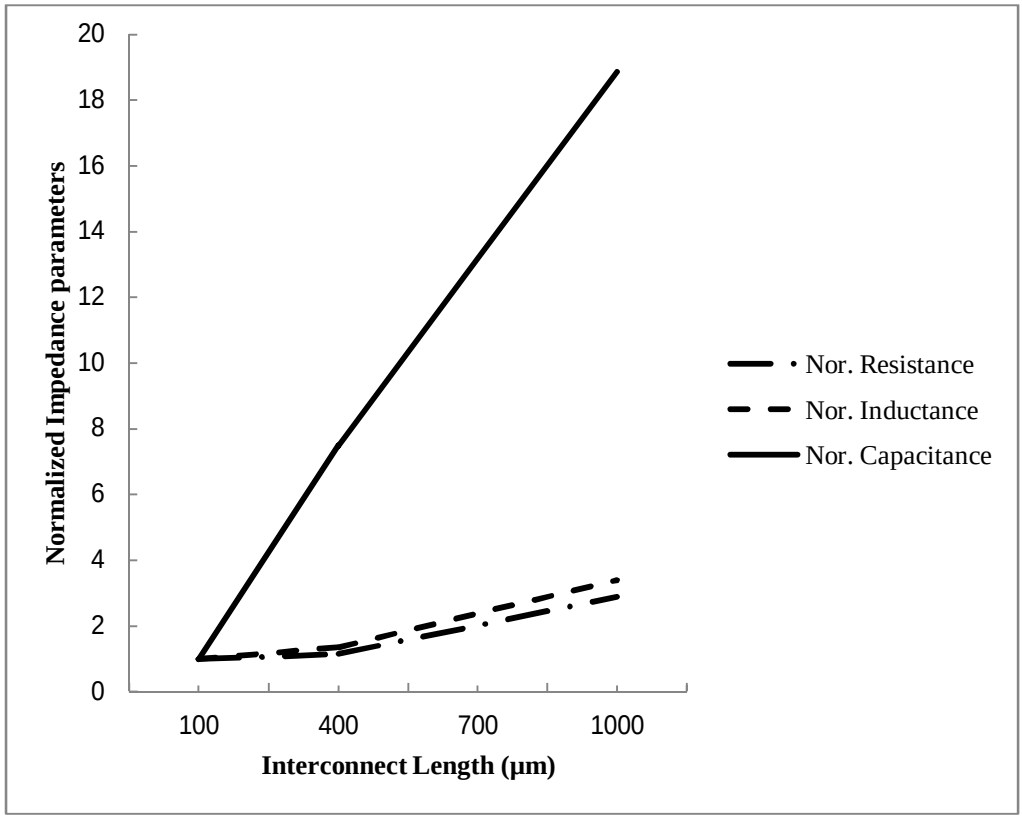

Figure 3.9 Normalized impedance parameter versus Interconnect length for CNT

The Figure 3.9 and 3.10 show the effect of the interconnect length on normalized impedance parameter for CNT and Copper interconnect. Impedance parameters are normalized by its respective value of 100 micrometer length of interconnect parameters. Normalized capacitance and inductance are linearly increased with length of CNT bundle and copper based interconnect. It is observed that copper based VLSI interconnects has less capacitance in comparison to CNT bundle. Therefore, power dissipation in copper is lower than CNT bundle interconnects.

Table 3.7 Normalized resistance. inductance and capacitance for copper at different interconnect length.

Length of Interconnect (µm)	Nor. Resistance	Nor. Inductance	Nor. Capacitance
100	1	1	1
400	1.185	4.34	3.004
700	2.074	8.077	5.25
1000	2.96	11.977	7.504

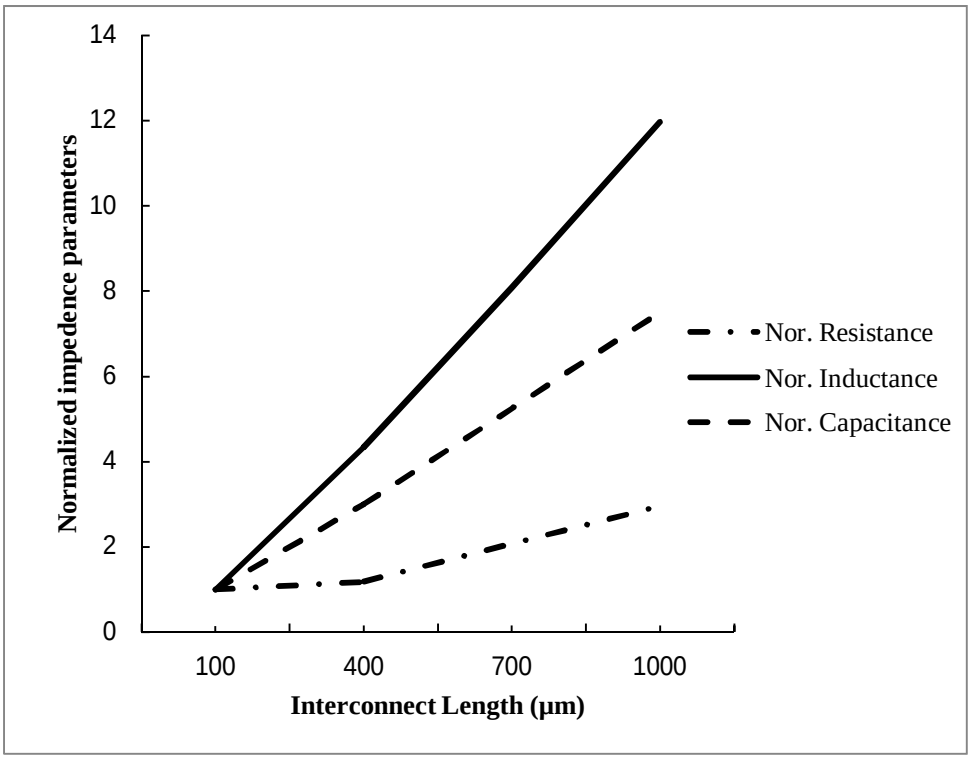

Figure 3.10 Normalized impedance parameter versus Interconnect length for Copper

CHAPTER 4

DELAY ANALYSIS

Introduction

On the basis of parasitic explained with equations in previous chapter the equivalent resistance, capacitance and inductance of copper and CNT bundle is determined. With variation in length and width of interconnect, variation in resistance, capacitance and inductance of global, semi global and local interconnect is observed with the help of graph.

4.1 Parameters used for calculation

Table 4.1: ITRS 2005 based parameters for calculation at 32 nm technology [17].

Parameters	CNT	Cu
Vdd	0.9	0.9
Width(w) of global interconnect	48nm	48nm
Aspect ratio (global)	3	3
Thickness(H) of global interconnect	144nm	144nm
Width(w) of local and semiglobal interconnect	32nm	32nm
Aspect ratio (local)	2	2
Diameter	1nm	1nm
Length (L)	1000um	1000um
ILD thickness	110.4nm	110.4nm
Seperation(s) between adjacent bundle of global interconnect	48nm	48nm
Seperation(s) between adjacent bundle of local interconnect	32nm	32nm
ε (relative)	2.25	2.25

Table 4.2: Value of resistance, inductance and capacitance for CNT and Cu at 32nm technology for 1000μm length.

Parameter	CNT (bundle)	Cu
Resistance	835.601Ω	5092.59Ω
Inductance	121.88fH	1950.24pH
Capacitance	3.85pF	16.96fF

4.2 Delay Analysis:

CNT and Copper delay is determined by using the above parasitic. The above resistance, inductance and capacitances are used for calculation of delay for different models of interconnect. By performing transient analysis by Tanner EDA tool at 32nm technology at 0.1GHz frequency, delay is determined for bundled CNT and Cu interconnect.

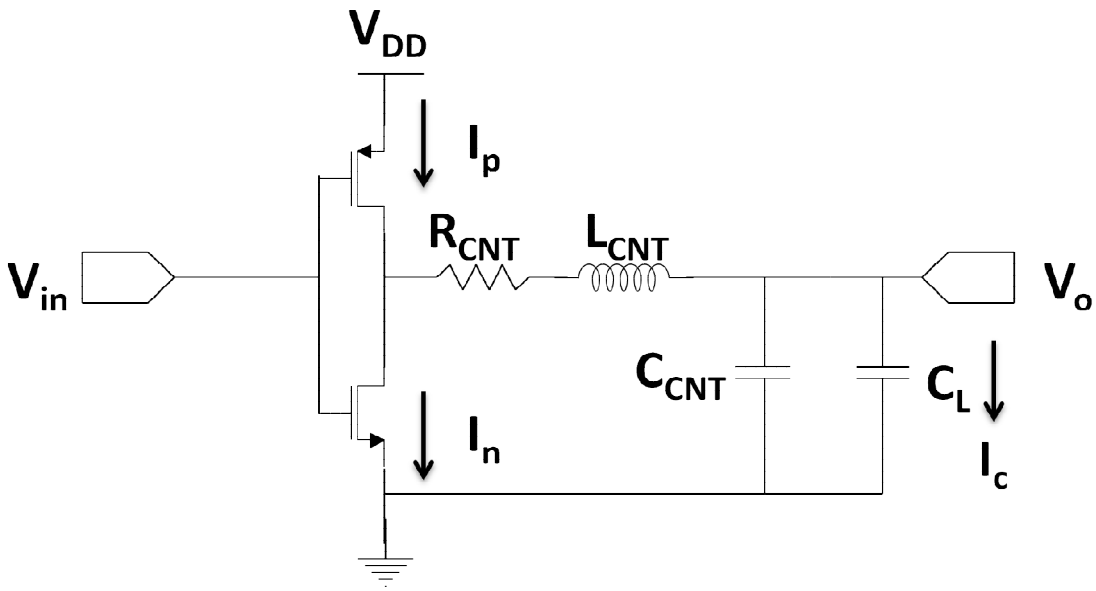

Figure 4.1 An equivalent model of CMOS gate driving L segment RLC circuit of interconnect.

4.3 Comparison of CNT with Copper Interconnect:

4.3.1 Optimal Repeater:

In optimal repeater, when the resistance of the interconnection is equal or larger than the on-resistance of the driver, propagation delay increases as the square of the interconnection length because both capacitance and resistance increase linearly with length. As the number of repeaters increase, the coupling associated with each smaller segment decrease because of increasing number of segments, therefore crosstalk is reduced [20].

Table 4.3 Comparison of delay of CNT with Cu at different no. of repeater.

No. of repeater	Delay (ns)	
	CNT	Cu
6	1.495	2.24
8	1.26	1.97
10	1.17	1.81
12	1.085	1.675

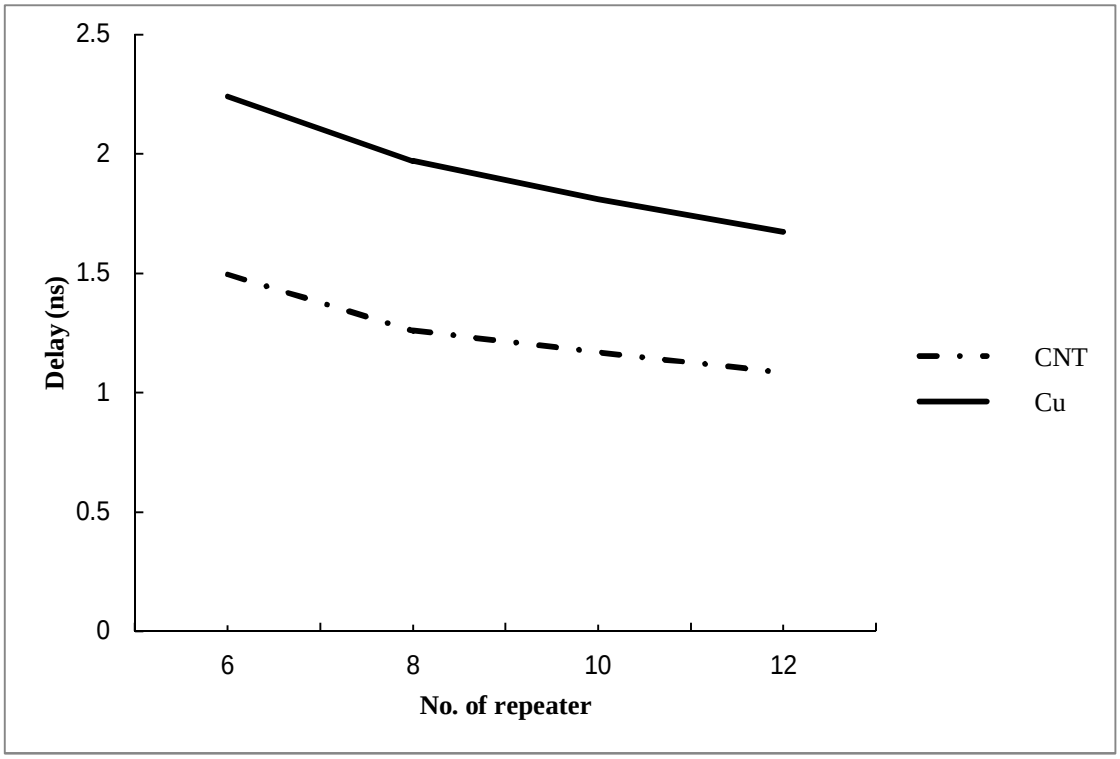

Figure 4.2 Delay versus no. of repeater of CNT and Cu

Figure 4.2 reveals delay as a function of repeaters. This graph shows that interconnect delay decreases with increase in number of repeater. As number of repeaters increase, long wire interconnects is divided into small segments which results in reduction of impedance parameter and finally reduces the delay of interconnects. This graph compares the delay of copper with CNT interconnect and shows, delay in copper interconnect is less than CNT bundle based interconnect due to less resistance.

Table 4.4: Cu delay for different no. of repeater at different size of driver transistor

Size of driver transistor	Delay (ns)		
	rep 6	rep 8	rep 10
15	3.29	2.96	2.79
20	2.845	2.42	2.19
25	2.47	2.165	2.05
30	2.325	2.09	1.895
35	2.28	2.015	1.85
40	2.24	1.97	1.81

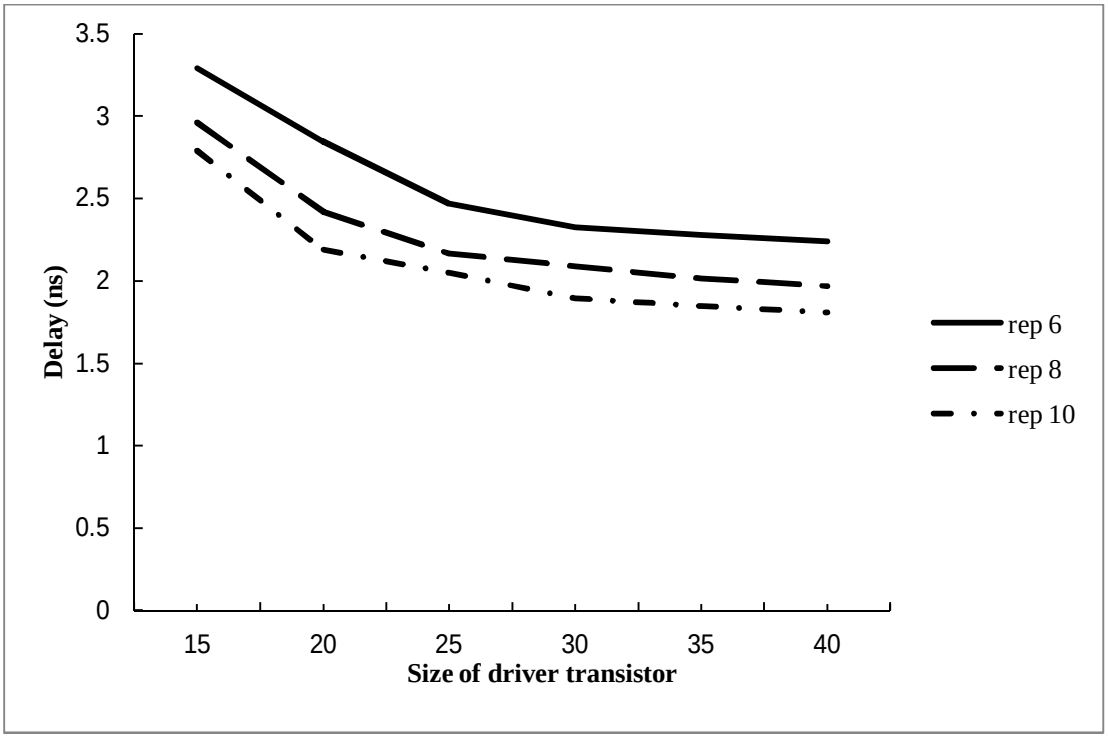

Figure 4.3 Size of driver transistor versus delay at different no. of repeater for Cu.

Figure 4.3 reveals the delay as a function of size of driver transistor at different number of repeaters for Cu interconnect. As the size of driver transistor is increased, the resistance reduces and the capacitance increases and if in this case, number of repeaters increase, RLC segment of interconnect decreases, therefore when size of driver transistor is increased as well as number of repeaters, the delay reduces rapidly.

Table 4.5: CNT delay for different no. of repeaters at the different size of driver transistor

Size of driver transistor	Delay (ns)			
	rep 4	rep 6	rep 8	rep 10
15	-	3.415	3.08	2.815
20	3.4	2.765	2.415	2.22
25	2.765	2.23	1.99	1.83
30	2.3	1.815	1.595	1.34
35	2.04	1.66	1.42	1.295
40	1.85	1.495	1.26	1.17

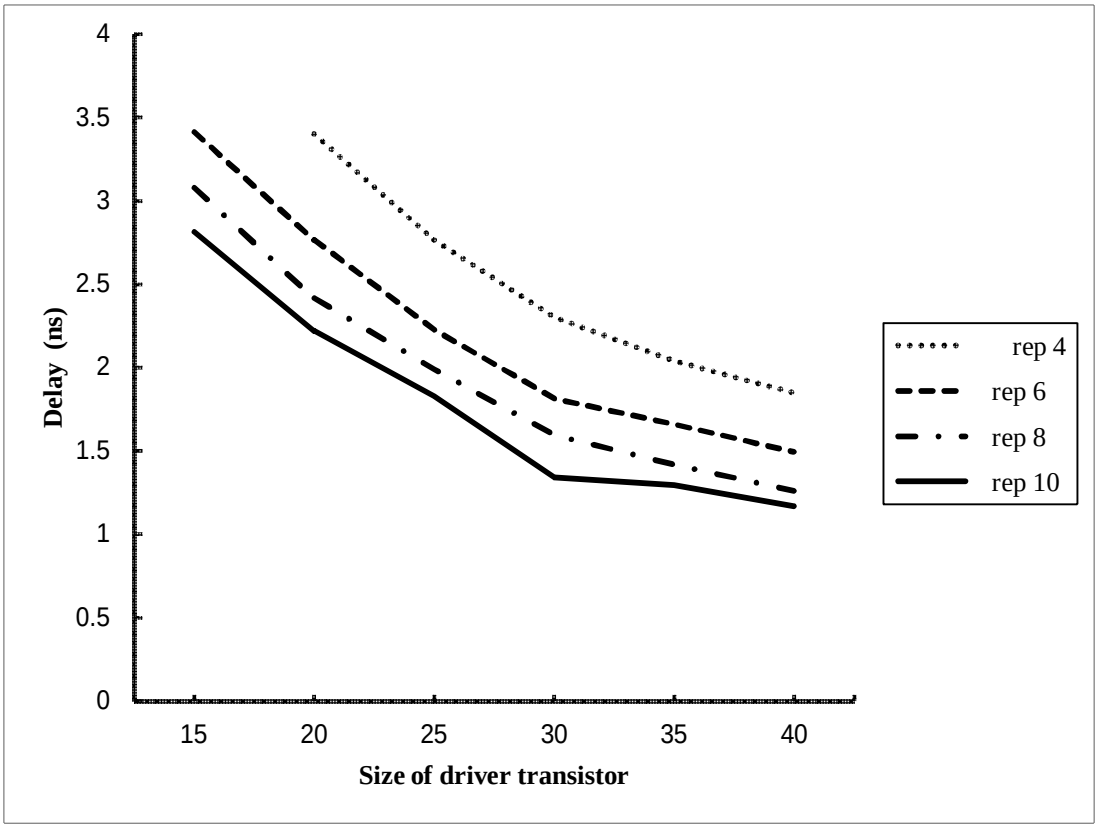

Figure 4.4 Size of driver transistor versus delay at different no. of repeater for CNT.

In the Figure 4.4, it shows the delay versus size of driver transistor at different no. of repeaters for CNT Interconnect. As the size of driver transistor is increased, the resistance reduces and the capacitance increases and if in this case, number of repeaters increase, RLC segment of interconnect decreases, therefore when size of driver transistor is increased as well as number of repeaters, the delay reduces rapidly.

Table 4.6: Comparison of CNT and Cu delay at different no. of repeater for different size of driver transistor.

Size of driver transistor	for 6 repeater		for 8 repeater	
	Delay(ns)		Delay(ns)	
	Cu	CNT	Cu	CNT
15	3.29	3.215	2.96	2.88
20	2.845	2.765	2.42	2.415
25	2.47	2.23	2.165	1.99
30	2.325	1.815	2.09	1.595
35	2.28	1.66	2.015	1.42
40	2.24	1.495	1.97	1.26

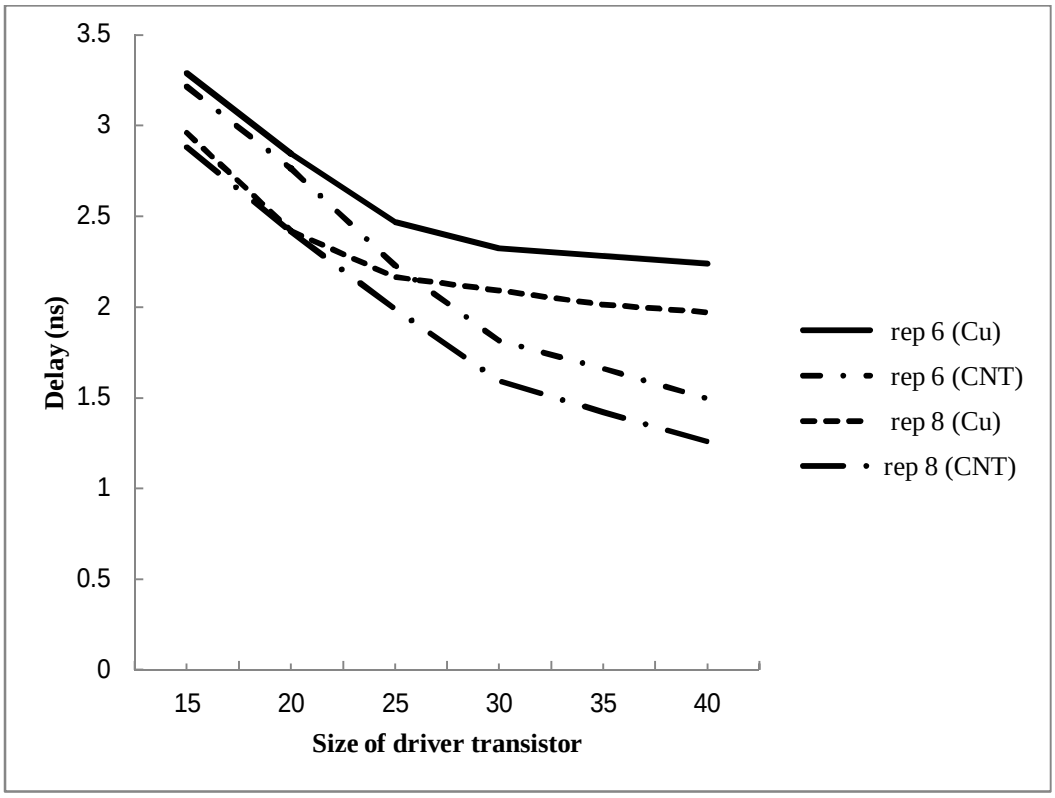

Figure 4.5 Size of driver transistor versus delay for different repeater for CNT and Cu.

In the Figure 4.5 the graph shows the delay as a function of driver transistor size for different number of repeaters for Cu and CNT interconnect. As we increase the size of driver transistor with number of repeater the delay is reduced quickly for CNT interconnect in comparison to copper interconnect due to less resistance in case of CNT bundle interconnect as compared to copper interconnect.

Table 4.7 Delay for cascade repeater for CNT.

Cascade with repeater for CNT	
Size of driver transistor	Delay (ns)
15	3.235
20	2.92
25	2.675
30	2.48

Figure 4.6 Size of driver transistor versus delay for cascade with repeater.

In Figure 4.6 the graph shows the delay versus size of driver transistor for cascade with repeater of CNT interconnect. Because in this technique, a chain of drivers is used instead of single minimum-size driver and as cascaded drivers are increase in size until the last device is large enough to drive the line, therefore propagation delay is optimized.

CHAPTER

5

CROSSTALK ANALYSIS FOR MODELS OF VLSI INTERCONNECT

Introduction

In capacitive coupled interconnect, the line which is responsible for introducing the crosstalk is referred as aggressor line and which line is affected by crosstalk is referred as victim line [8]. Propagating signal on aggressor affects the propagating signal on victim due to capacitive and inductive coupling between adjacent interconnects. This is commonly referred to as crosstalk. Crosstalk induces two types of fault: glitch fault and delay fault. Glitch fault is the unwanted output which occurs on the victim line, results a noise pulse is generated, and the other fault is induced on the aggressor line when aggressor and victim have simulation transitions [19, 23]. The CNT-based interconnect is more suitable in VLSI circuits as far as the gate oxide reliability is concerned. The crosstalk-induced overshoot/undershoots expressed as percentage of supply voltage remain almost same with the scaling of technology nodes, and increases approximately linearly with the length of the Cu-based interconnects whereas in the case of CNT-based interconnects the overshoot/undershoots remain almost invariant with the scaling and interconnect length. Due to the large capacitance to ground and small resistance of SWCNT bundle, it has least overshoot/undershoots among three types of interconnects and hence has very small impact on the gate oxide reliability. On the gate oxide reliability MWCNT-based interconnect has lower impact than copper wire but MWCNT is not as good as SWCNT-bundle-based interconnect. It has also been shown that a parallel connection of large number of SWCNT is better than a single tube of SWCNT. Therefore, we can conclude that the impact on gate oxide reliability is not critically influenced with the increase in length of CNT-based interconnect. As technology node is scaled down, both SWCNT- and MWCNT-based interconnect has less impact on the gate oxide reliability. As far as the gate oxide reliability is concerned, sparsely packed SWCNT-bundle based interconnect is most suitable in comparison to MWCNT or Cu-based interconnects [8].

5.1 Crosstalk Analysis

The circuits considered for analysis as reported in [18] comprise a CMOS inverter driving a capacitive coupled distributed RLC model of interconnects. A load capacitance of 10fF terminates the capacitive coupled interconnects and a 0.1 GHz pulse of 1ns rise time provides input to the CMOS inverter. The performance of this set up is studied by SPICE simulation in 32nm technology node. The comparison of the impedance parameter of copper interconnect are also determined [25].

5.2 Simulation Results

The Figure 5.1 shows the variation of normalized crosstalk noise as a function of interconnect length for both copper and CNT bundle. This crosstalk noise is caused due to the capacitive coupling on the victim line. As interconnect length increases normalized crosstalk noise for capacitive coupled interconnects increases exponentially in case of copper due to higher values of impedance parameters as compared to CNT bundle while fewer changes occur in case of CNT bundle.

Here crosstalk overshoot is normalized by input voltage and referred as normalized crosstalk. Crosstalk generates overshoot and undershoots on the victim net. Overshoots and undershoots are the positive and negative peaks on the victim line respectively. These aberrations degrade the interconnect performance and faults arise in the VLSI chip. The coupling capacitance is taken same for both CNT bundle and copper based interconnect for calculating the crosstalk noise.

Table 5.1 Comparison of CNT and Cu normalized crosstalk noise for different interconnect length.

Length of Interconnect (μm)	Normalized Crosstalk noise (mV)	
	CNT	Cu
100	4.04	15.06
400	4.46	23.31
700	5.15	112.27
1000	5.47	144.56

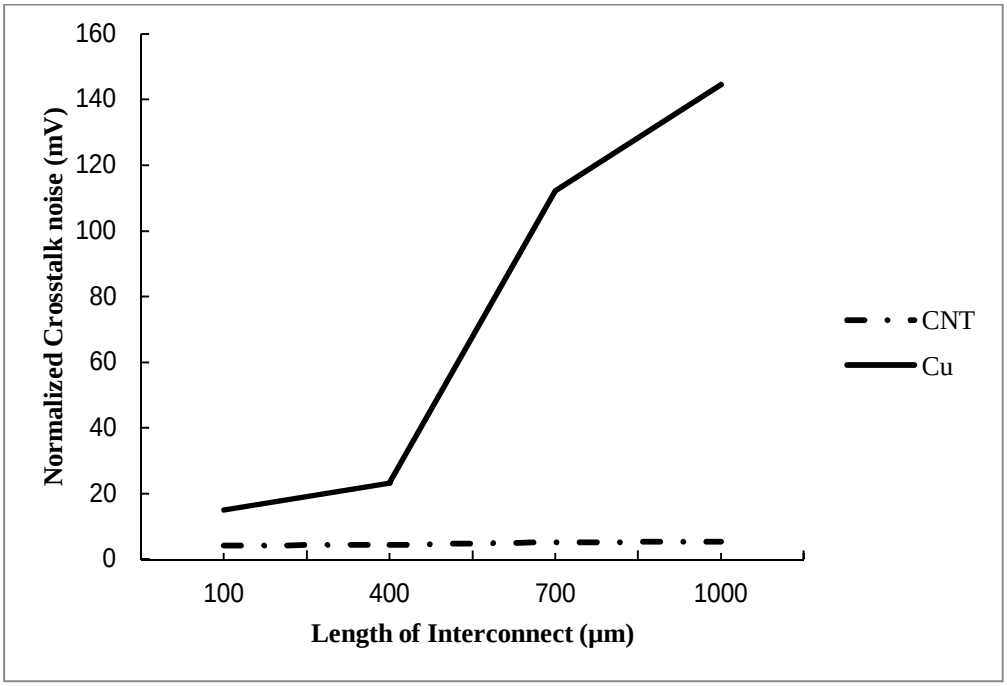

Figure 5.1 Normalized crosstalk noise versus Interconnect length.

Table 5.2 Comparison of CNT and Cu normalized crosstalk noise at different no. of repeater.

No. of Repeater	Normalized Crosstalk noise (mV)	
	CNT	Cu
2	7.48	74.38
4	5.5	52.94
6	5.7	64
8	5.757	100
10	5.38	120

The Figure 5.2 shows the variation of normalized crosstalk noise as a function of number of repeaters for CNT bundle and compared it with copper interconnect. Interconnect length of 1mm is used to calculate the normalized crosstalk noise drawn in the Figure 5.2 and optimum number of repeaters are used. It is observed that as the number of repeater increases the crosstalk noise is much less in CNT based interconnects as compare to copper based interconnects as shown in Figure 5.2. As the number of repeaters increase, crosstalk is reduced due to increasing number of segment which forces to decrease the coupling associated with each smaller segment [20].

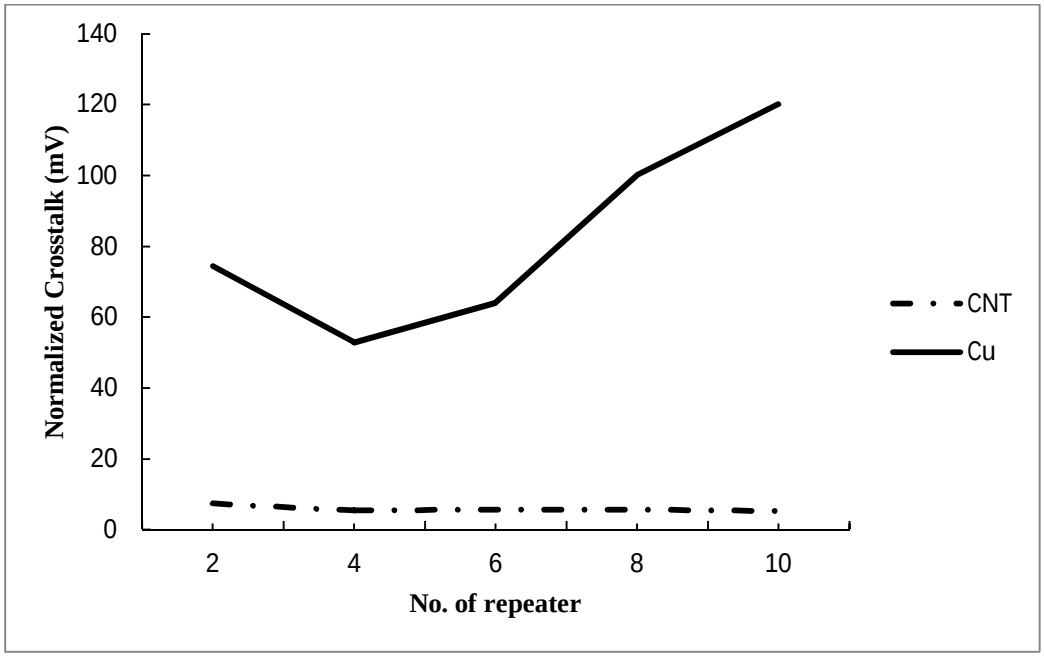

Figure 5.2 Normalized crosstalk noise versus no. of repeater.

Table 5.3 Comparison of CNT and Cu crosstalk induced delay at aggressor output for different lengths of interconnect.

Length of Interconnect (μm)	Crosstalk induced delay (ns) at aggressor output	
	CNT	Cu
100	.035	.015
400	.13	.06
700	.325	.03
1000	.49	.05

The Figure 5.3 shows the variation of crosstalk induced delay at aggressor output as a function of interconnect length for both copper and CNT bundle. This type of noise is cause when aggressor and victim have simulation transitions. As interconnect length increases crosstalk induced delay for capacitive coupled interconnects increases exponentially in case of CNT bundle due to higher values of capacitance as compared to copper while fewer changes occur in case of copper. These aberrations degrade the interconnect performance and faults arise in the VLSI chip. The coupling capacitance is taken same for both CNT bundle and copper based interconnect for calculating the crosstalk noise.

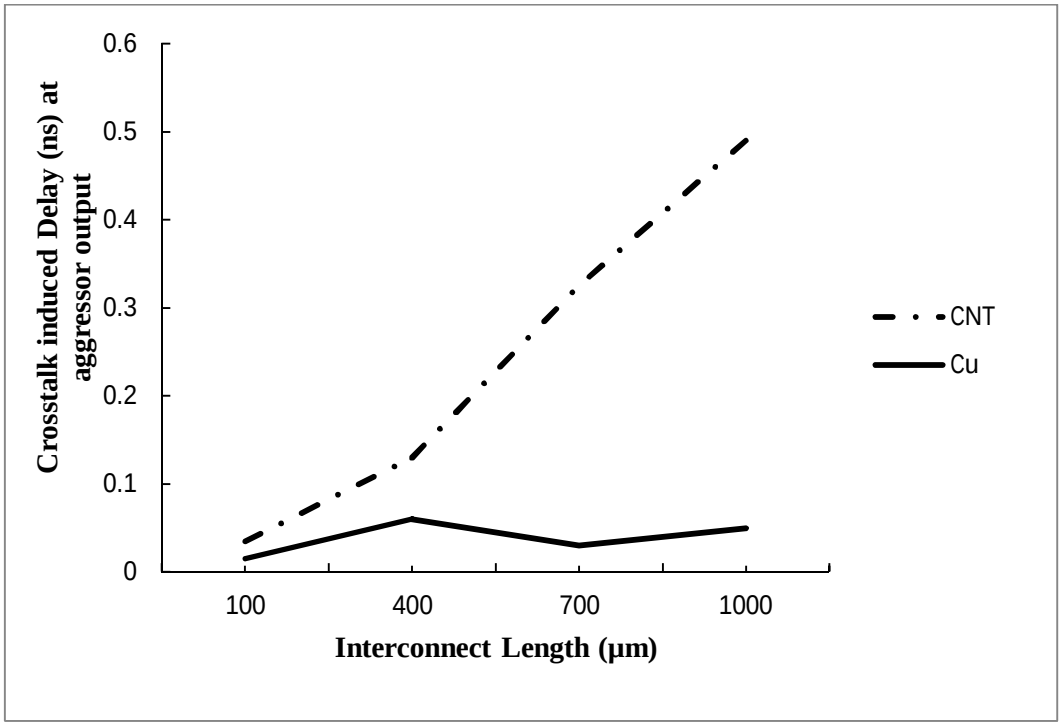

Figure 5.3 Crosstalk induced delay at aggressor output versus interconnect length.

Table 5.4 Comparison of CNT and Cu crosstalk induced power dissipation at aggressor output for different interconnect length.

Length of Interconnect (µm)	Crosstalk induced power (mW) at aggressor output	
	CNT	Cu
100	.088	.0706
400	.208	.0722
700	.303	.0752
1000	.403	.0786

The Figure 5.4 shows the variation of crosstalk induced power dissipation at aggressor output as a function of interconnect length for both copper and CNT bundle. As interconnect length increases crosstalk induced power dissipation for capacitive coupled interconnects increases exponentially in case of CNT bundle due to higher values of capacitance as compared to copper while fewer changes occur in case of copper. These aberrations degrade the interconnect performance and faults arise in the VLSI chip. The coupling capacitance is taken same for both CNT bundle and copper based interconnect for calculating the crosstalk noise.

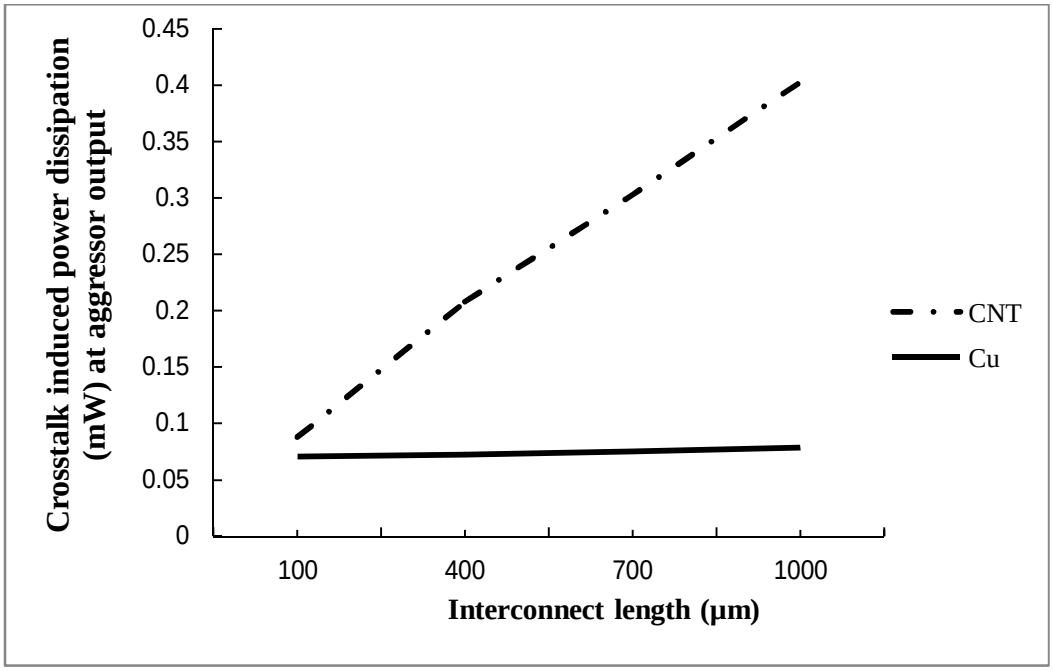

Figure 5.4 Crosstalk induced power dissipation at aggressor output versus interconnect length.

Table 5.5 Normalized delay and normalized power dissipation with variation in interconnect length in CNT based Interconnect.

Length of Interconnect (µm)	Normalized Delay	Normalized Power Dissipation
100	2.33	1.246
400	2.16	2.88
700	10.83	4.029
1000	9.8	5.127

The Figure 5.5 shows the normalized delay and normalized power dissipation with variation in interconnect length. Delay and power dissipation of CNT are normalized by its respective values of copper interconnects. As interconnect length increases, normalized delay and power dissipation also increases with it, due to increase in normalized impedance parameters.

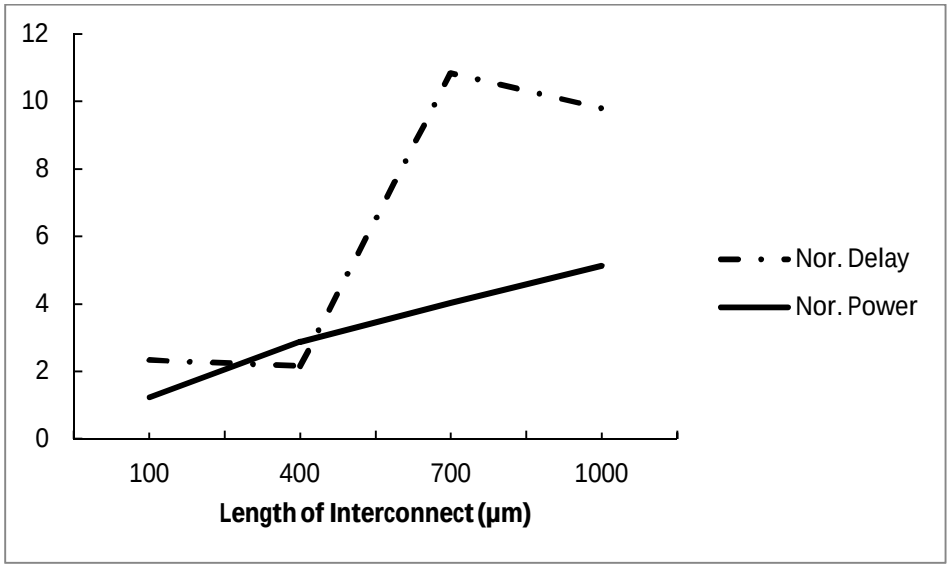

Figure 5.5 Normalized delay and power dissipation versus interconnect length.

Table 5.6 Comparison of CNT normalized crosstalk noise for three different cases at different no. of repeater.

No. of repeater	Normalized Crosstalk noise (mV)		
	Case 1	Case 2	Case 3
2	6.58	6.48	8.34
4	6.47	5.86	7.28
6	6.02	5.67	7.02
8	5.15	5.47	7.15
10	5.51	5.28	7.33
12	5.58	5.08	6.67
14	4.94	5.13	6.97

Case 1: w'= 0.5w, s'= s + 0.5w Case 2: w'= w, s'= s

Case 3: w'= 1.5w, s'= s - 0.5w

W is the width of interconnect and s is the separation between two interconnects.

The Figure 5.6 shows the variation of normalized crosstalk noise for three different cases at different no. of repeater for CNT bundle interconnect. Case 2 is good among these three cases. Interconnect length of 1mm is used to calculate the normalized crosstalk noise drawn in the Figure 5.6 and optimum number of repeaters are used. This type of noise occurs on the victim line.

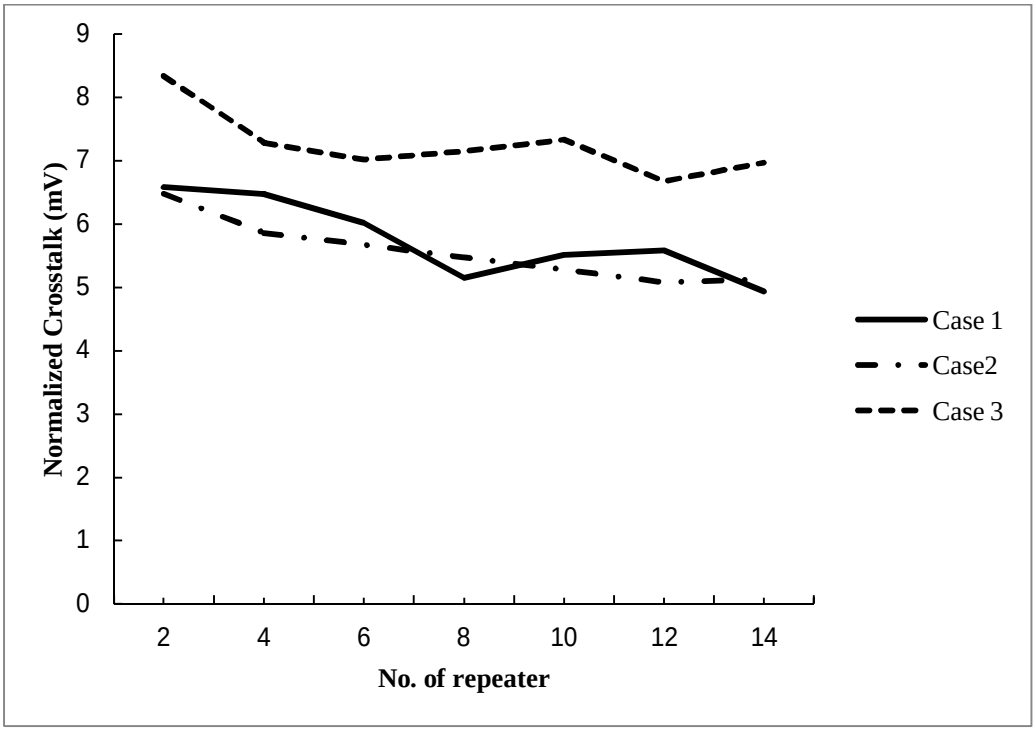

Figure 5.6 Normalized crosstalk noise versus different no. of repeater for three different cases in CNT.

Table 5.7 Comparison of crosstalk induced delay for three different cases for CNT at different no. of repeater.

No. of repeater	Delay (ns)		
	Case 1	Case 2	Case 3
2	2.015	1.865	2.94
4	0.85	0.97	1.525
6	0.5	0.635	1.06
8	0.65	0.485	0.825
10	0.25	0.395	0.535
12	0.185	0.27	0.45
14	0.18	0.23	0.35

The Figure 5.7 shows the variation of crosstalk induced delay for three different cases at different no. of repeater for CNT bundle interconnect. Interconnect length of 1mm is used to calculate the crosstalk induced delay drawn in the Figure 6.7 and optimum number of repeaters are used. This type of noise is occurred on the aggressor line. Propagation delay is reduced due to division of long interconnect wire into small segments with increase in the number of repeater.

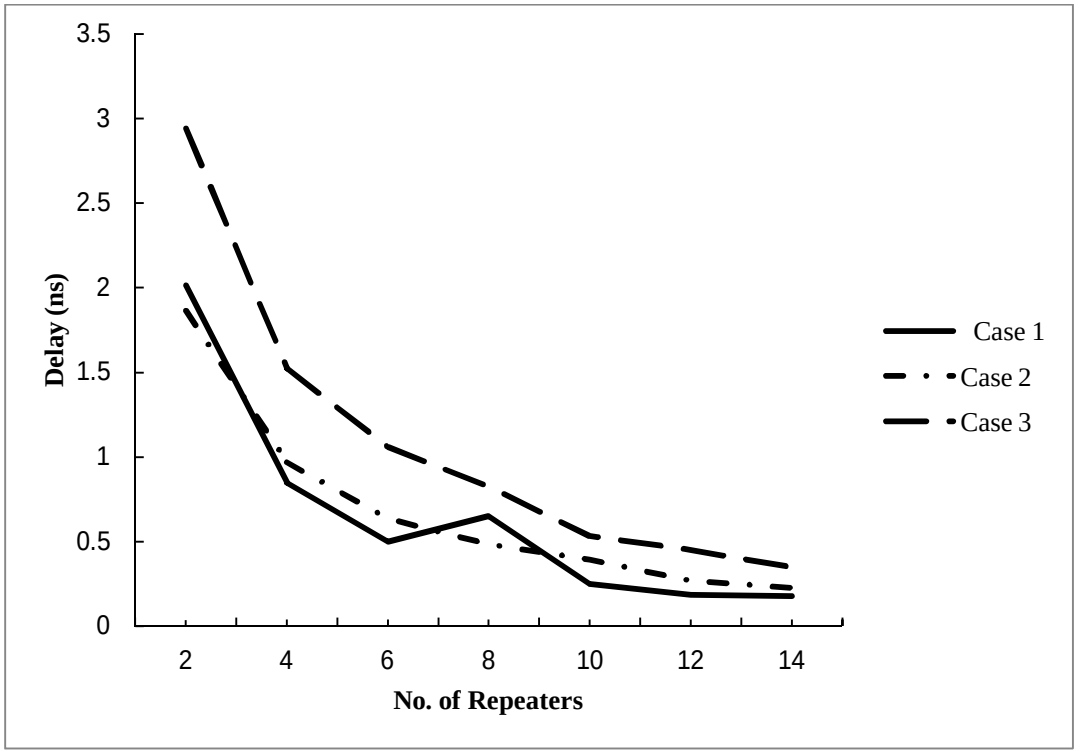

Figure 5.7 Crosstalk induced delay versus different no. of repeater for three different cases in CNT.

Table 5.8 Comparison of crosstalk induced power dissipation for three different cases for CNT at different no. of repeater.

No. of repeater	Power dissipation (mW)		
	Case 1	Case 2	Case 3
2	0.188	0.347	0.602
4	0.206	0.362	0.622
6	0.217	0.384	0.629
8	0.176	0.403	0.647
10	0.243	0.408	0.693
12	0.287	0.459	0.713
14	0.269	0.478	0.722

The Figure 5.8 shows the variation of crosstalk induced power dissipation for three different cases at different no. of repeater for CNT bundle interconnect. Interconnect length of 1mm is used to calculate the power dissipation drawn in the Figure 6.8 and optimum number of repeaters are used. Power dissipation slightly increases with number of repeater.

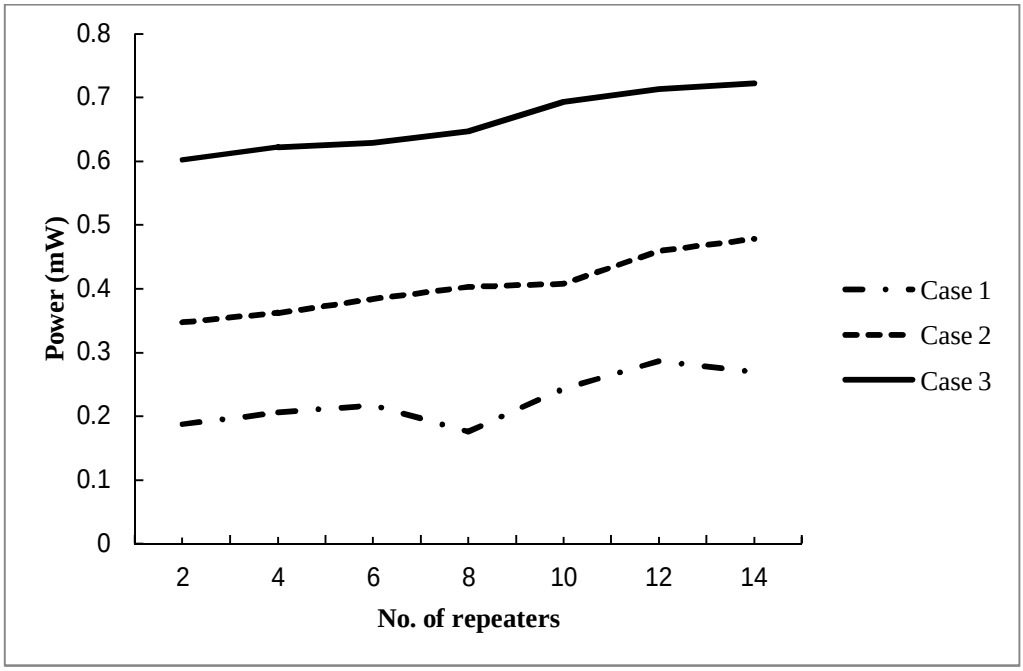

Figure 5.8 Crosstalk induced power dissipation versus different no. of repeater for three different cases in CNT.

Table 5.9 Comparison of CNT normalized crosstalk noise for 9 segment RLC and 7 segment RLC at different size of driver transistor.

Size of driver transistor	Normalized Crosstalk (mV)	
	9 segment RLC	7 segment RLC
20	4.08	4.52
30	3.52	4.52
40	3.16	3.81
50	2.76	3.57
60	2.4	3.31

The figure 5.9 shows the variation of normalized crosstalk noise for 9 segment and 7 segment RLC model at different size of driver transistor for CNT bundle interconnect. This figure shows that 7 segment RLC has crosstalk noise lower than 9 segment RLC. In 9 and 7 segments RLC, only one CMOS inverter is used without repeater but RLC value is normalized by 9 and 7 means divided into 9 and 7 sections. As the number of repeaters increase, crosstalk is reduced to increasing number of segment which forces it to decrease the coupling associated with each smaller segment.

Figure 5.9 Normalized crosstalk noise for 9 segment RLC and 7 segment RLC versus different size of driver transistor in CNT.

CHAPTER

6

CONCLUSION

An over view of the exploratory research on CNT as possible VLSI interconnect is presented in my dissertation. The problem of continuing with copper interconnects in highly scaled technologies of future are briefly discussed. The works carried out in finding an alternative solution indicates that the CNT based interconnects have the potential to replace copper in future and bundle of CNTs gives better performance in terms of delay and power delay product (PDP) with respect to copper. The study also reveals that propagation delay decreases with increase in number of repeater. This occurs due to division of long interconnect wire into small segment. Propagation delay is also reduce with increase in the size of driver transistor due to decrease in resistance of interconnect. An investigation on the normalized crosstalk noise with variation in interconnect length and number of repeater in CNT interconnect is presented. Simulation results demonstrate that the crosstalk induced voltage peaks increases linearly with increase in lengths of interconnects due to dominance of impedance parameters and more voltage peaks are observed in copper as compared to CNT bundle. Results also reveal that crosstalk induced positive peaks abruptly change with number of repeater in copper and less change in CNT based interconnect.

LIST OF PUBLICATION

Anuj Kumar Sharma, Mayank Kumar Rai,"Crosstalk Analysis in Capacitive Coupled Carbon Nanotube Bundle Interconnects", *Proc. International conference on Information Technology, Electronics and Communication*, pp. 37-40, July 2013.

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APPENDIX

A.1 PTM level 54 model

.model nmos nmos level = 54

+version = 4.0	binunit = 1	paramchk= 1	mobmod = 0
+capmod = 2	igcmod = 1	igbmod = 1	geomod = 1
+diomod = 1	rdsmod = 0	rbodymod= 1	rgatemod= 1
+permod = 1	acnqsmod= 0	trnqsmod= 0	+tnom = 27
toxe = 6.5e-010	toxp = 4e-010	toxm = 6.5e-010	+dtox = 2.5e-010
epsrox = 3.9	wint = 5e-009	lint = 1.35e-009	+ll = 0 wl = 0
lln = 1	wln = 1	+lw = 0	ww = 0
lwn = 1	wwn = 1	+lwl = 0	wwl = 0
xpart = 0	toxref = 6.5e-010	xl = -9e-9	+dlcig = 1.35e-009
+vth0 = 0.3692	k1 = 0.2 k2 = 0	k3 = 0	+k3b = 0
w0 = 2.5e-006	dvt0 = 1	dvt1 = 2	+dvt2 = 0
dvt0w = 0	dvt1w = 0	dvt2w = 0	+dsub = 0.078
minv = 0.05	voffl = 0	dvtp0 = 1e-011	+dvtp1 = 0.1
lpe0 = 0	lpeb = 0	xj = 7.2e-009	+ngate = 1e+023
ndep = 1.2e+019	nsd = 2e+020	phin = 0	+cdsc = 0
cdscb = 0	cdscd = 0	cit = 0	+voff = -0.13
nfactor = 2.3	eta0 = 0.0045	etab = 0	+vfb = -1.058
u0 = 0.0181	ua = -5e-010	ub = 1.7e-018	+uc = 0
vsat = 200000	a0 = 1	ags = 0	+a1 = 0
a2 = 1	b0 = 0	b1 = 0	+keta = 0.04
dwg = 0	dwb = 0	pclm = 0.06	+pdiblc1 = 0.001
pdiblc2 = 0.001	pdiblcb = -0.005	drout = 0.5	+pvag = 1e-020
delta = 0.01	pscbe1 = 2.0e+009	pscbe2 = 1e-007	+fprout = 0.2
pdits = 0.01	pditsd = 0.23	pditsl = 2300000	+rsh = 5
rdsw = 60	rsw = 30	rdw = 30	+rdswmin = 0
rdwmin = 0	rswmin = 0	prwg = 0	+prwb = 0
wr = 1	alpha0 = 0.074	alpha1 = 0.005	+beta0 = 30
agidl = 0.0002	bgidl = 2.1e+009	cgidl = 0.0002	+egidl = 0.8
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aigbinv = 0.014	bigbinv = 0.004	cigbinv = 0.004	+eigbinv = 1.1
nigbinv = 3	aigc = 0.0213	bigc = 0.0025889	+cigc = 0.002
aigsd = 0.0213	bigsd = 0.0025889	cigsd = 0.002	+nigc = 1
poxedge = 1	pigcd = 1	ntox = 1	+xrcrg1 = 12
xrcrg2 = 5	+cgso = 7e-011	cgdo = 7e-011	cgbo = 0
cgdl = 7.5e-013	+cgsl = 7.5e-013	clc = 1e-007	cle = 0.6
cf = 1.1e-010	+ckappas = 0.6	ckappad = 0.6	vfbcv = -1
acde = 195	+moin = 15	noff = 1	voffcv = 0
+kt1 = -0.154	kt1l = 0	kt2 = 0.022	ute = -1.1
+ua1 = 1e-009	ub1 = -1e-018	uc1 = -5.6e-011	prt = 0
+at = 33000	+fnoimod = 1	tnoimod = 0	noia = 6.25e+041
noib = 3.125e+026	+noic = 8.75e+009	em = 41000000	af = 1
ef = 1	+kf = 0	tnoia = 1.5	tnoib = 3.5
ntnoi = 1	+jss = 1.2e-006	jsws = 2.4e-013	jswgs = 2.4e-013
njs = 1	+ijthsfwd= 0.1	ijthsrev= 0.1	bvs = 10
xjbvs = 1	+jsd = 1.2e-006	jswd = 2.4e-013	jswgd = 2.4e-013

xjbvd = 1	+pbs = 1	cjs = 0.0018	mjs = 0.5
pbsws = 1	+cjsws = 1.2e-010	mjsws = 0.33	cjswgs = 2.1e-010
cjd = 0.0018	+cjswd = 1.2e-010	mjswd = 0.33	pbswgd = 1
cjswgd = 2.1e-010	+mjswgd = 0.33	tpb = 0	tcj = 0
tpbsw = 0	+tcjsw = 0	tpbswg = 0	tcjswg = 0
xtis = 3	+dmcg = 0	dmci = 0	dmdg = 0
dmcgt = 0	+dwj = 0	xgw = 0	xgl = 0
+rshg = 0.4	gbmin = 1e-010	rbpb = 5	rbpd = 15
+rbps = 15	rbdb = 15	rbsb = 15	ngcon = 1

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+capmod = 2	igcmod = 1	igbmod = 1	geomod = 1
+diomod = 1	rdsmod = 0	rbodymod= 1	rgatemod= 1
+permod = 1	acnqsmod= 0	trnqsmod= 0	+tnom = 27
toxe = 6.7e-010	toxp = 4e-010	toxm = 6.7e-010	+dtox = 2.7e-010
epsrox = 3.9	wint = 5e-009	lint = 1.35e-009	+ll = 0
wl = 0	lln = 1	wln = 1	+lw = 0
ww = 0	lwn = 1	wwn = 1	+lwl = 0
wwl = 0	xpart = 0	toxref = 6.7e-010	xl = -9e-9
+dlcig = 1.35e-009	+vth0 = -0.25399	k1 = 0.2	k2 = -0.01
k3 = 0	+k3b = 0	w0 = 2.5e-006	dvt0 = 1
dvt1 = 2	+dvt2 = -0.032	dvt0w = 0	dvt1w = 0
dvt2w = 0	+dsub = 0.1	minv = 0.05	voffl = 0
dvtp0 = 1e-011	+dvtp1 = 0.05	lpe0 = 0	lpeb = 0
xj = 7.2e-009	+ngate = 1e+023	ndep = 4.4e+018	nsd = 2e+020
phin = 0	+cdsc = 0	cdscb = 0	cdscd = 0
cit = 0	+voff = -0.13	nfactor = 2.3	eta0 = 0.0037
etab = 0	+vfb = -1.058	u0 = 0.0023	ua = -5e-010
ub = 1.6e-018	+uc = 0	vsat = 78000	a0 = 1
ags = 1e-020	+a1 = 0	a2 = 1	b0 = 0
b1 = 0	+keta = -0.047	dwg = 0	dwb = 0
pclm = 0.1	+pdiblc1 = 0.001	pdiblc2 = 0.001	pdiblcb = 3.4e-008
drout = 0.6	+pvag = 1e-020	delta = 0.01	pscbe1 = 2e+009
pscbe2 = 9.58e-007	+fprout = 0.2	pdits = 0.08	pditsd = 0.23
pditsl = 2300000	+rsh = 5	rdsw = 60	rsw = 30
rdw = 30	+rdswmin = 0	rdwmin = 0	rswmin = 0
prwg = 096	+prwb = 0	wr = 1	alpha0 = 0.074
alpha1 = 0.005	+beta0 = 30	agidl = 0.0002	bgidl = 2.1e+009
cgidl = 0.0002	+egidl = 0.8	aigbacc = 0.012	bigbacc = 0.0028
cigbacc = 0.002	+nigbacc = 1	aigbinv = 0.014	bigbinv = 0.004
cigbinv = 0.004	+eigbinv = 1.1	nigbinv = 3	aigc = 0.012731
bigc = 0.00115	+cigc = 0.0008	aigsd = 0.012731	bigsd = 0.00115
cigsd = 0.0008	+nigc = 1	poxedge = 1	pigcd = 1
ntox = 1	+xrcrg1 = 12	xrcrg2 = 5	+cgso = 7e-011
cgdo = 7e-011	cgbo = 0	cgdl = 3e-011	+cgsl = 3e-011
clc = 1e-007	cle = 0.6	cf = 1.1e-010	+ckappas = 0.6
ckappad = 0.6	vfbcv = -1	acde = 1	+moin = 15
noff = 1	voffcv = 0	+kt1 = -0.14	kt1l = 0
kt2 = 0.022	ute = -1.1	+ua1 = 1e-009	ub1 = -1e-018

uc1 = -5.6e-011	prt = 0	+at = 33000	+fnoimod = 1
tnoimod = 0	noia = 6.25e+041	noib = 3.125e+026	+noic = 8.75e+009
em = 41000000	af = 1	ef = 1	+kf = 0
tnoia = 1.5	tnoib = 3.5	ntnoi = 1	+jss = 2e-007
jsws = 4e-013	jswgs = 4e-013	njs = 1	+ijthsfwd= 0.1
ijthsrev= 0.1	bvs = 10	xjbvs = 1	+jsd = 2e-007
jswd = 4e-013	jswgd = 4e-013	xjbvd = 1	+pbs = 1
cjs = 0.0015	mjs = 0.5	pbsws = 1	+cjsws = 9.4e-011
mjsws = 0.33	cjswgs = 2e-010	cjd = 0.0015	+cjswd = 9.4e-011
mjswd = 0.33	pbswgd = 1	cjswgd = 2e-010	+mjswgd = 0.33
tpb = 0	tcj = 0	tpbsw = 0	+tcjsw = 0
tpbswg = 0	tcjswg = 0	xtis = 3	+dmcg = 0
dmdg = 0	dmcgt = 0	xgw = 0	+xgl = 0
+rshg = 0.1	gbmin = 1e-012	rbpb = 50	rbpd = 50
+rbps = 50	rbdb = 50	rbsb = 50	ngcon = 1