STUDY OF POWER GATING TECHNIQUE FOR LOW POWER FLIP-FLOPS

Dissertation submitted in the partial fulfillment of requirement for the award of degree of

Master of Technology

In

VLSI Design

Submitted by

Ankit Rao

Roll No. 601161026

Under the guidance of

Dr. Alpana Agarwal

Associate Professor

ELECTRONICS AND COMMUNICATION ENGINEERING DEPARTMENT

THAPAR UNIVERSITY

(Established under the section 3 of UGC Act, 1956)

PATIALA – 147004 (PUNJAB)

JULY 2013

DECLARATION

I hereby declare that the work which is being presented in the dissertation entitled **"Study of power gating technique for low power flip-flops"** is an authentic record of my own work carried out as requirement for the award of Master of Technology in VLSI Design at Thapar University, Patiala under the guidance of **Dr. Alpana Agarwal**, Associate Professor, Electronics and Communication Engineering Department (ECED) during 2011-2013.

The matter presented in this dissertation has not been submitted in any other university/institute for the award of degree.

Ankit

Date: 10-7-2013

Ankit Rao
601161026

It is certified that the above statement is correct to the best of my knowledge and belief.

(Alpana Agarwal)
Associate Professor
ECED, Thapar University

Date: 10-7-2013

Countersigned by:

Head
ECED, Thapar University
Patiala-147004

Dean of Academic Affairs
Thapar University, Patiala

Acknowledgement

First of all, I would like to express my gratitude to **Dr. Alpana Agarwal, Associate Professor**, Electronics and Communication Engineering Department, Thapar University, Patiala for her patient guidance and support throughout my work. I am truly very fortunate to have the opportunity to work with her. I found her guidance to be extremely valuable.

I am also thankful to **Dr. Rajesh Khanna, Professor and Head of the Department**, Electronics and Communication Engineering Department, entire faculty and staff of Electronics and Communication Engineering Department for their encouragement and execution of this dissertation work.

Next I would like to thank Mr. Anil Singh and all my friends who devoted their valuable time and helped me in all possible ways towards successful completion of this work.

Finally and above everyone else, I pay my heartiest thank you and lifelong grace to my parents for their love, care, constant support and encouragement.

I am also thankful to God who bestowed upon his grace and always with me.

Date : 10/07/2013 Ankit Rao
Place : Patiala Roll no. 601161026

Abstract

Flip-flops are common building blocks and are frequently used in digital VLSI circuits. These are used as starting, ending and intermediate part in delay paths which decides the maximum speed of the systems. They consumes large amount of power because these are operated at system operating frequency. Thus a careful design of low power flip flop with optimum speed is necessary which is becoming challenge with technology scaling.

In order to achieve flip-flops power gated technique is used for both single-edge triggered and double-edge triggered flip-flops. Different circuit topologies of flip-flops are used to increase the speed. Static and dynamic flip-flops are studied in order to study optimum tradeoff between power and propagation delay.

Different flip-flop designs are simulated in UMC 0.18 µm CMOS process under different supply voltages in Cadence Analog Design and simulation Environment.

TABLE OF CONTENTS

Chapter1

Chapter 2

Chapter 3

Chapter 4

Chapter 5

List of Figures

List of tables

Abbreviations

CMOS	Complementary Metal Oxide Semiconductor
DET	Dual Edge Triggered
D FF	Delay Flip Flop
DRC	Design Rule Check
FF	Flip Flop
HSDMHLFF	High Speed Dual edge Modified Hybrid Latch Flip Flop
HSMHLFF	High Speed Modified Hybrid Latch Flip Flop
LVS	Layout versus Schematic
MTCMOS	Multi Threshold Complementary Metal Oxide Semiconductor
NMOS	N-channel Metal Oxide Semiconductor
PMOS	P-channel Metal Oxide Semiconductor
SET	Single Edge Triggered
TSPC	True Single Phase Clock
RCX	Resistance and Capacitance Extraction

Chapter1 Introduction

Flip-flops and latches are the elements which are frequently used in digital VLSI (very large integrated circuits) designing. In synchronous systems these are the starting and ending part of the signal delay paths, which decide the maximum speed of the systems. They consume a large amount of power because they are clocked at system operating frequency. Thus careful design of the latch circuit is important for low power VLSI systems. The clock power dominates the total power dissipation. A large portion of the clock power is used to derive sequential elements such as flop-flops and latches. Reducing the clock power dissipation of flip-flop and latches is thus an important technique for total power conservation.

The energy dissipation of a flip-flop can be divided into two components. First component is clock energy and second is data energy. The first component is the energy dissipation when flip-flop id clocked while the data of the flip-flop is unchanged. The second component is additional energy required to write a different data value into the flip-flop. In a typical flip-flop the two components are comparable. In most of the systems data rate of a flip-flop is typically much lower than its clock rate. This means that identical data values are being loaded with very high probability. Thus the power saving technique for the flip-flop mostly concentrates on the clock energy reduction.

1.1 **Sequential circuits**

A sequential circuit defines its output as a function of both its current inputs and its previous inputs. Therefore, the output depends on past inputs. To remember previous inputs, sequential circuits must have storage element. This storage element is a flip-flop. The state of this flip-flop is a function of the previous inputs to the circuit. Therefore, pending output depends on both the current inputs and the current state of the circuit. In the same way that combinational circuits are generalizations of gates, sequential circuits are generalizations of flip-flops.

1.2 **Clock**

The fact that a sequential circuit uses past inputs to determine present outputs indicates they are event ordering. Some sequential circuits are asynchronous, which means they become active the moment any input value changes. Synchronous sequential circuits use clocks to order events. A clock is a signal that emits a series of pulse with a precise pulse width and a precise interval between consecutive pulses. This interval is called the clock cycle time. Clock speed is generally measured in megahertz (MHz), or millions of pulses per second. A clock is used by a sequential circuit to decide when to update the state of the circuit (when do “present” inputs become “past” inputs). This means that inputs to the circuit can only affect the storage element at given, discrete instances of time. Most sequential circuits are edge-triggered (as opposed to being level-triggered).This means they are allowed to change their states on either the rising or falling edge of the clock signal.

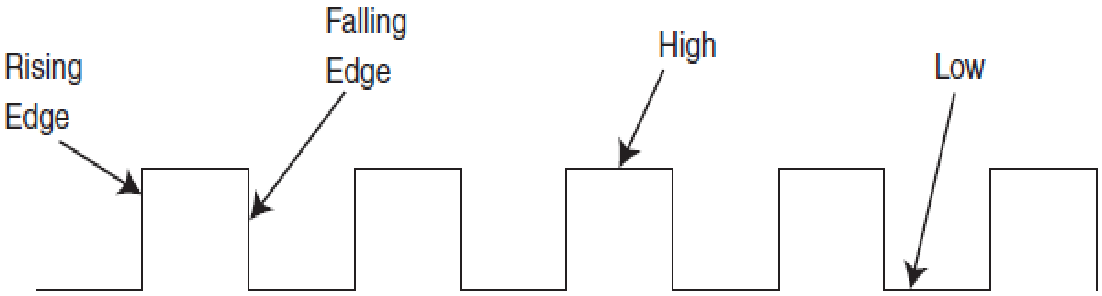


Fig. 1.2 Clock Signal [4]

1.3 **Flip-flop**

In electronics, a flip-flop or latch is a circuit that has two stable states and can be used to store state information. The circuit can be made to change state by signals applied to one or more control inputs and will have one or two outputs. It is the basic storage element in sequential circuits. Flip-flops and latches are a fundamental building block of digital electronics systems used in computers, communications, and many other types of systems.

Flip-flops and latches are used as data storage elements. Such data storage can be used for storage of state, and such a circuit is described as sequential logic. When used in a finite-state machine, the output and next state depend not only on its current input, but also on its current state (and hence, previous inputs). It can also be used for counting of pulses, and for synchronizing variably-timed input signals to some reference timing signal. Flip-flops can be either simple (transparent or opaque) or clocked (synchronous or edge-triggered); the simple ones are commonly called latches and these are level triggered. The word latch is mainly used for storage elements, while clocked devices are described as flip-flops.

1.3.1 **Flip-flop types**

Flip-flops can be divided into common types: the SR ("set-reset"), D ("data" or "delay"), T ("toggle"), and JK types are the common ones. The behaviour of a particular type can be described by what is termed the characteristic equation, which derives the "next" (i.e., after the next clock pulse) output, Q_{next}, in terms of the input signal(s) and/or the current output, Q.

1.3.2 **Gated latches and conditional transparency**

Latches are designed to be transparent, that is, input signal changes cause immediate changes in the output. When several transparent latches follow each other, using the same clock signal, signals can propagate through all of them at once. Alternately, additional logic can be added to a simple transparent latch to make it non-transparent or opaque when another input (an enable input) is not asserted. By following a transparent-high latch with a transparent-low latch, master slave flip-flop is implemented.

1.3.2.1 **Gated D latch**

This latch exploits the fact that, in the two active input combinations (01 and 10) of a gated SR latch, R is the complement of S. The input NAND stage converts the two D input states (0 and 1) to these two input combinations for the next SR latch by inverting the data input signal. The low state of the enable signal produces the inactive "11" combination. Thus a gated D-latch may be considered as a one-input synchronous SR latch. This configuration prevents from applying the restricted combination to the inputs. It is also known as transparent latch, data latch, or simply gated latch. It has a data input and an enable signal (sometimes named clock, or control). The word transparent comes from the fact that, when the enable input is on, the signal propagates directly through the circuit, from the input D to the output Q.

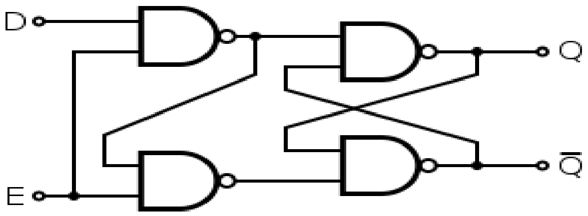


Fig. 1.3 (a) D-type transparent latch based on SR NAND latch [4]

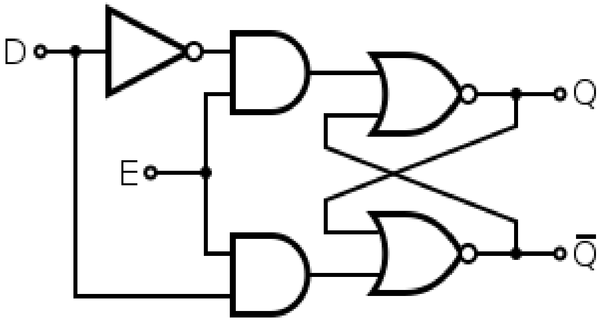


Fig. 1.3 (b) A gated D latch based on SR NOR latch [4]

Transparent latches are typically used as I/O ports or in asynchronous systems, or in synchronous two-phase systems (synchronous systems that use a two-phase clock), where two latches operating on different clock phases prevent data transparency as in a master–slave flip-flop.

1.3.3 **D flip-flop**

D flip-flop is widely used device. It is also known as a data or delay flip-flop. D flip-flop captures the value of D-input at a definite portion of the clock cycle (such as the rising edge of the clock). That captured value becomes the Q output. At other times, the output Q does not change. The D flip-flop can be viewed as a memory cell, a zero-order hold, or a delay line.

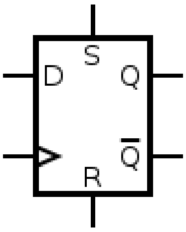


Fig. 1.3(c) D flip-flop symbol [4]

Table 1 Truth table

Clock	**D**	**Q_{next}**
Rising edge	0	0
Rising edge	1	1
Non-Rising	X	Q

Most of the D flip-flops in ICs have the compatibility to force to the set or reset state(which ignores the d an clock input).The illegal condition S=R=1 is resolved in d flip-flop. The advantage of the D flip-flop over the D-type "transparent latch" is that the signal on the D input pin is captured the moment the flip-flop is clocked, and subsequent changes on the D input will be ignored until the next clock event. An exception is that some flip-flops have a "reset" signal input, which will reset Q (to zero), and may be either asynchronous or synchronous with the clock.

1.3.3.1 **Classical positive-edge-triggered D flip-flop**

It consists of two stages implemented by SR NAND latches. The input stage (the two latches on the left) processes the clock and data signals to ensure correct input signals for the output stage (the single latch on the right).

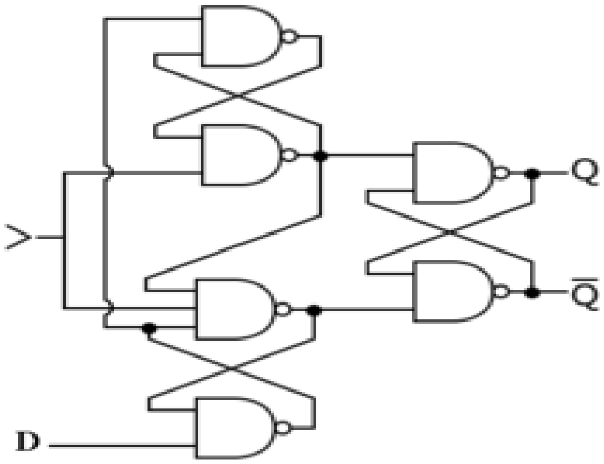


Fig. 1.3(d) Positive-edge-triggered D flip-flop [4]

If the clock is low, both the output signals of the input stage are high regardless of the data input; the output latch is unaffected and it stores the previous state. When the clock signal changes from low to high, only one of the output voltages (depending on the data signal) goes low and sets/resets the output latch: if D = 0, the lower output becomes low; if D = 1, the upper output becomes low. If the clock signal continues staying high, the outputs keep their states regardless of the data input and force the output latch to stay in the corresponding state as the input logical zero remains active while the clock is high. Hence the role of the output latch is to store the data only while the clock is low. The circuit is closely related to the gated D latch as both the circuits convert the two D input states (0 and 1) to two input combinations (01 and 10) for the output SR latch by inverting the data input signal (both the circuits split the single D signal in two complementary S and R signals). The difference is that in the gated D latch simple NAND logical gates are used while in the positive-edge-triggered D flip-flop SR NAND latches are used for this purpose. The role of these latches is to "lock" the active output producing low voltage (a logical zero); thus the positive-edge-triggered D flip-flop can be thought of as a gated D latch with latched input gates.

1.3.3.2 **Master–slave pulse-triggered D flip-flop**

A master–slave D flip-flop is created by connecting two gated D latches in series, and inverting the enable input to one of them. It is called master–slave because the second latch in the series only changes in response to a change in the first (master) latch.

The term pulse-triggered means that data is entered on the rising edge of the clock pulse, but the output does not reflect the change until the falling edge of the clock pulse.

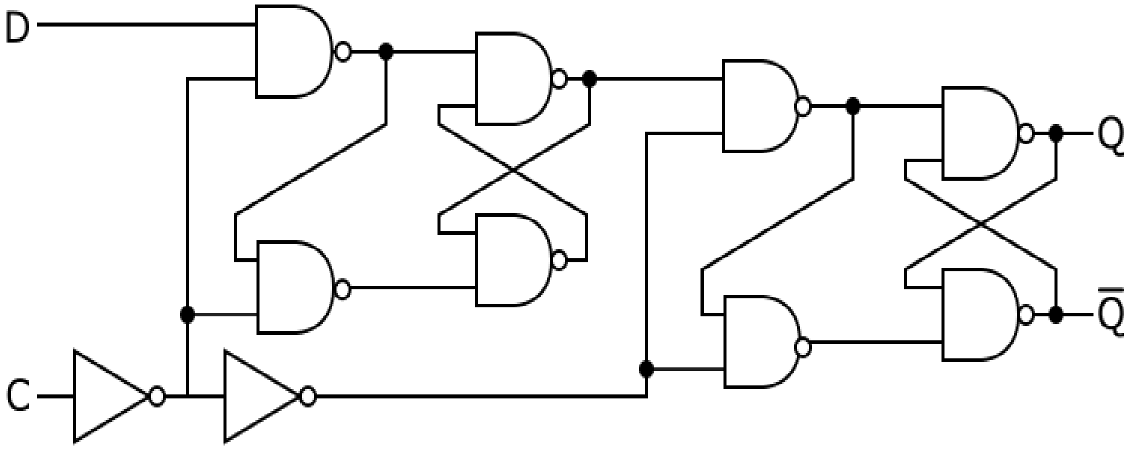


Fig. 1.3(e) Implementation of a master–slave D flip-flop triggered on the positive edge of the clock [4]

A master–slave D flip-flop in Fig. 1.3(e) responds on the negative edge of the enable input (usually a clock).For a positive-edge triggered master–slave D flip-flop, when the clock signal is low (logical 0) the "enable" seen by the first or "master" D latch (the inverted clock signal) is high (logical 1). This allows the "master" latch to store the input value when the clock signal transitions from low to high. As the clock signal goes high (0 to 1) the inverted "enable" of the first latch goes low (1 to 0) and the value seen at the input to the master latch is "locked". Nearly simultaneously, the twice inverted "enable" of the second or "slave" D latch transitions from low to high (0 to 1) with the clock signal. This allows the signal captured at the rising edge of the clock by the now "locked" master latch to pass through the "slave" latch. When the clock signal returns to low (1 to 0), the output of the "slave" latch is "locked", and the value seen at the last rising edge of the clock is held while the "master" latch begins to accept new values in preparation for the next rising clock edge. By removing the leftmost inverter in the circuit at side, a D-type flip flop that strobes on the falling edge of a clock signal can be obtained.

1.3.3.3 **Edge-triggered dynamic D storage element**

An efficient functional alternative to a D flip-flop can be made with dynamic circuits as long as it is clocked often enough; while not a true flip-flop, it is still called a flip-flop for its functional role. While the master–slave D element is triggered on the edge of a clock, its components are each triggered by clock levels. The "edge-triggered D flip-flop", as it is called even though it is not a true flip-flop, does not have the master–slave properties.

Edge-triggered D flip-flops are often implemented in integrated high-speed operations using dynamic logic. This means that the digital output is stored on parasitic device capacitance while the device is not transitioning. This design of dynamic flip flops also enables simple resetting since the reset operation can be performed by simply discharging one or more internal nodes. A common dynamic flip-flop variety is the true single-phase clock (TSPC) type which performs the flip-flop operation with little power and at high speeds. However, dynamic flip-flops will typically not work at static or low clock speeds: given enough time, leakage paths may discharge the parasitic capacitance enough to cause the flip-flop to enter invalid states.

1.4 **Metastability**

Flip-flops are prone to a problem called metastability, which can happen when two inputs, such as data and clock or clock and reset, are changing at about the same time, such that the resulting state would depend on the order of the input events. When the order is not clear, within appropriate timing constraints, the result is that the output may behave unpredictably, taking many times longer than normal to settle to one state or the other, or even oscillating several times before settling. Theoretically, the time to settle down is not bounded. In a computer system, this metastability can cause corruption of data or a program crash, if the state is not stable before another circuit uses its value; in particular, if two different logical paths use the output of a flip-flop, one path can interpret it as a 0 and the other as a 1 when it has not resolved to stable state, putting the machine into an inconsistent state.

1.5 **Timing considerations**

Setup time is the minimum amount of time the data signal should be held steady **before** the clock event so that the data are reliably sampled by the clock. This applies to synchronous circuits such as the flip-flop.

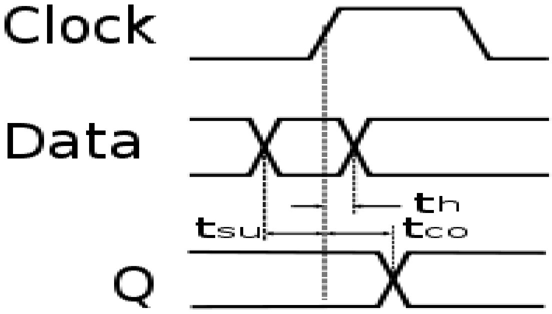


Fig. 1.5 Setup and hold time [4]

Hold time is the minimum amount of time the data signal should be held steady **after** the clock event so that the data are reliably sampled. Setup time must be greater than clock flank which is greater than hold time.

The metastability in flip-flops can be avoided by ensuring that the data and control inputs are held valid and constant for specified periods before and after the clock pulse, called the setup time (t_{su}) and the hold time (t_h) respectively. These times are specified in the data sheet for the device, and are typically between a few nanoseconds and a few hundred picoseconds for modern devices. Unfortunately, it is not always possible to meet the setup and hold criteria, because the flip-flop may be connected to a real-time signal that could change at any time, outside the control of the designer.

In this case, the best the designer can do is to reduce the probability of error to a certain level, depending on the required reliability of the circuit. One technique for suppressing metastability is to connect two or more flip-flops in a chain, so that the output of each one feeds the data input of the next, and all devices share a common clock. With this method, the probability of a metastable event can be reduced to a negligible value, but never to zero. The probability of metastability gets closer and closer to zero as the number of flip-flops connected in series is increased.

So-called metastable-hardened flip-flops are available, which work by reducing the setup and hold times as much as possible, but even these cannot eliminate the problem entirely. This is because metastability is more than simply a matter of circuit design. When the transitions in the clock and the data are close together in time, the flip-flop is forced to decide which event happened first. However fast we make the device, there is always the possibility that the input events will be so close together that it cannot detect which one happened first. It is therefore logically impossible to build a perfectly metastable-proof flip-flop.

1.6 **Propagation delay**

Another important timing value for a flip-flop (F/F) is the clock-to-output delay (common symbol in data sheets: t_{CO}) or propagation delay (t_P), which is the time the flip-flop takes to change its output after the clock edge. The time for a high-to-low transition (t_{PHL}) is sometimes different from the time for a low-to-high transition (t_{PLH}).

When cascading F/Fs which share the same clock (as in a shift register), it is important to ensure that the t_{CO} of a preceding F/F is longer than the hold time (t_h) of the following flip-flop, so data present at the input of the succeeding F/F is properly "shifted in" following the active edge of the clock. This relationship between t_{CO} and t_h is normally guaranteed if the F/Fs are physically identical. Furthermore, for correct operation, it is easy to verify that the clock period has to be greater than the sum $t_{su} + t_h$.

Organization of dissertation is as follows: chapter 1 discuss the brief introduction of flip flops, chapter 2 shows the previous work done on the flip flops and there comparison, chapter 3 shows the simulation and results of different static and dynamic single edge triggered and dual edge triggered flip flops, chapter 4 represents the layout and post layout simulations of low power flip flops and chapter 5 brings out the conclusion and future scope of the work done and references.

Chapter 2 Literature Review

In this we will discuss work done on flip-flop and the techniques used for low power low, voltage and high speed flip designs. As the demand for portable battery operated computing devices with longer battery life, low cost and high speed increases, there is a constant need of new circuit designs to fulfill these requirements. Since digital VLSI integrated circuits are considered to be a combination of interconnected logic gates and flip-flops (FFs), choosing appropriate flip-flop topology is of fundamental importance. Moreover these systems use clock signals to sample and store the input data through FFs synchronously. Since clock signal is needed for the synchronization of large number of digital components, the clock load increases substantially. The clock network alone dissipates 30-70% of the total system power dissipation; hence reduction in power dissipation due to clock load has been a major area of emphasis for digital system designers and also the problems of power generation and power distribution. Another problem faced by VLSI designers is how to improve the speed of the system. The methods used for power (static power and dynamic power) reduction and to increase speed include reduction of supply voltage, improvement in setup, hold time and also the reduction of clock frequency. The review of previous work on flip-flop is given below.

2.1 Novel high speed and low power single and double edge-triggered flip-flop [3]

The circuit is applied in two cases, single edge triggered, and double edge triggered. One which works at single edge is called High Speed Modified Hybrid Latch Flip-Flop (HSMHLFF), and another one which works at double edge is called High Speed Double edge triggered Modified Hybrid Latch Flip-Flop (HSDMHLFF). In these flip-flops, path between clock and output becomes shorter than the previous one. This leads to lower delay and power dissipation. HSMHILFF and HSDMHLFF use 180nm bulk CMOS technology. Compared to the earliest work, the new circuits show better speed and power consumption.

2.1.1 Single-edge triggered flip-flop

In this flip-flop, the dynamic part (MN4, MN3, and the clock path) was changed. The basic idea was got from LSDFF, The low-swing clock double edge-triggered flip-flop that has been developed to reduce the dynamic power consumption compared to a conventional flip-flop. At the rising edge of the CLK, MN3 and MN4 are both turned on for the short duration of tp1to sample data. In HSMHLFF, the path between CLK and Q is shorter than MHLFF, so speed and power consumption is better. Like other flip-flops, a back-to-back-inverter type driver at the output node is used for robust operation.

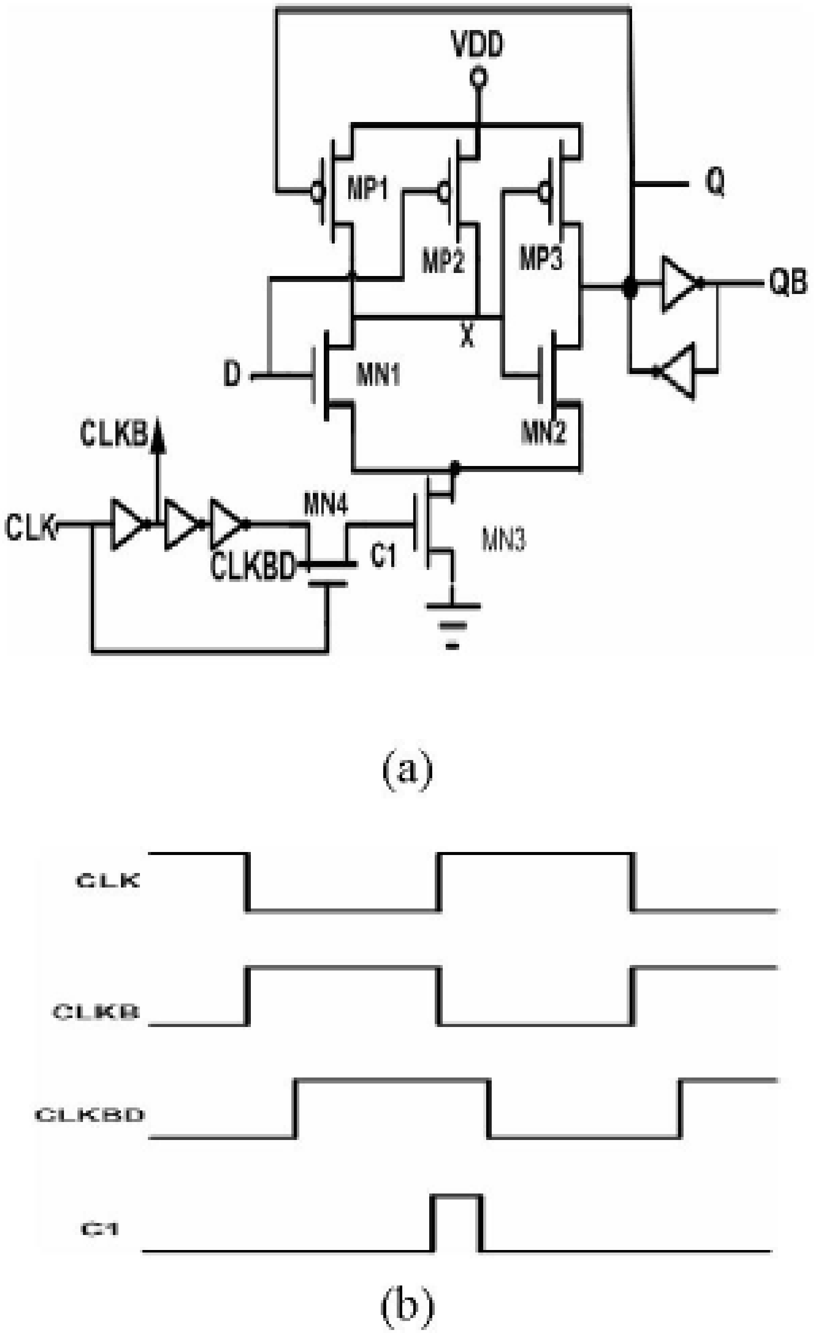
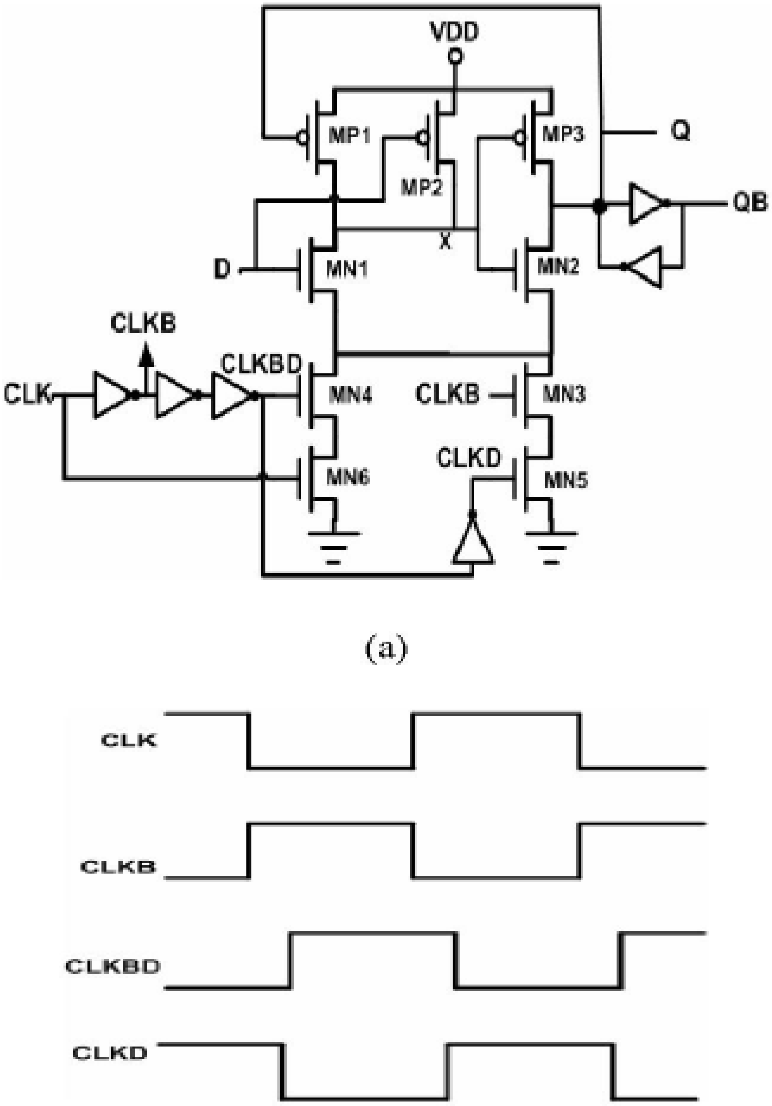


Fig. 2.1 (a) Circuit diagram of HSMHLFF, (b) Timing diagram [3]

2.1.2 **Double-edge triggered flip-flop**

The circuit diagram and timing behavior of this structure are shown in Fig. 2.1.2 (a), b) respectively. It works similar to HSMULFF, but the input of the flip-flop is transferred to the output at the rising and falling edges of the clock. At the rising edge of the CLK, transistor MN4 and MN6 are both turned on for the short duration of tp1 to sample data, while at the falling edge of the CLK, MN3 and MN5 are turned on to sample data during tp2. Also in HSDMHLFF, the path between CLK and Q is shorter than DMHLFF, so speed and power consumption is better.



(a)

(b)

Fig. 2.1.2 (a) Circuit diagram of HSDMHLFF (b) Timing diagram [3]

2.1.3 **Comparison between two structures of single-edge Triggered (SET)**

Table 2.1(a) shows the propagation delay between clock to output (CLK-Q), data to output (D-Q). It also shows the power delay product (P.D.) and the amount of improvement achieved when we compare with HSMHLFF and MHLFF.

Table 2.1(a) Power and propagation delay [3]

Flip-Flop (FF)	Clk-Q (ps)	D-Q(ps)	Power (µW)	P*D (fj)
MHLFF	582	173	83	14.4
HSMHLFF	463	154	79	12.1
Improvement	20%	11%	5%	16%

2.1.4 **Comparison between two structures of double edge MHLFF**

Table 2.1(b) compares the propagation delay, delay between data applied in input and the output obtained and the power delay product of the HSDMHLFF [3] and the previous DMHLFF. Improvement with double edge MHLFF flip-flop is obtained.

Table 2.1(b) Power and propagation delay [3]

Flip-Flop(FF)	Clk-Q (ps)	D-Q(ps)	Power (µW)	P*D (fj)
DMHLFF	466	156	151	23.6
HSDMHLFF	401	148	139	20.6
Improvement	16%	5%	8%	13%

2.1.5 **Static power consumption of flip-flops**

Table 2.1(c) shows the static power of SETFF [3] is less as compared to previous MHLFF but this increases in case of HSDMHLFF [3].

Table 2.1(c) Static power [3]

Flip flop(FF)	Static power (µW)
MHLFF	35
HSMHLLF	33
DMHLFF	35
HSDMHLFF	39

2.2 A novel CMOS double-edge triggered flip-flop for low-power applications [15]

This flip-flop is a low-power double-edge triggered flip-flop. It uses a single latch, a low-swing clock, and low-Vt transistors for the clocked Transistors. Therefore, fewer transistors are used and lower power consumption is achieved.

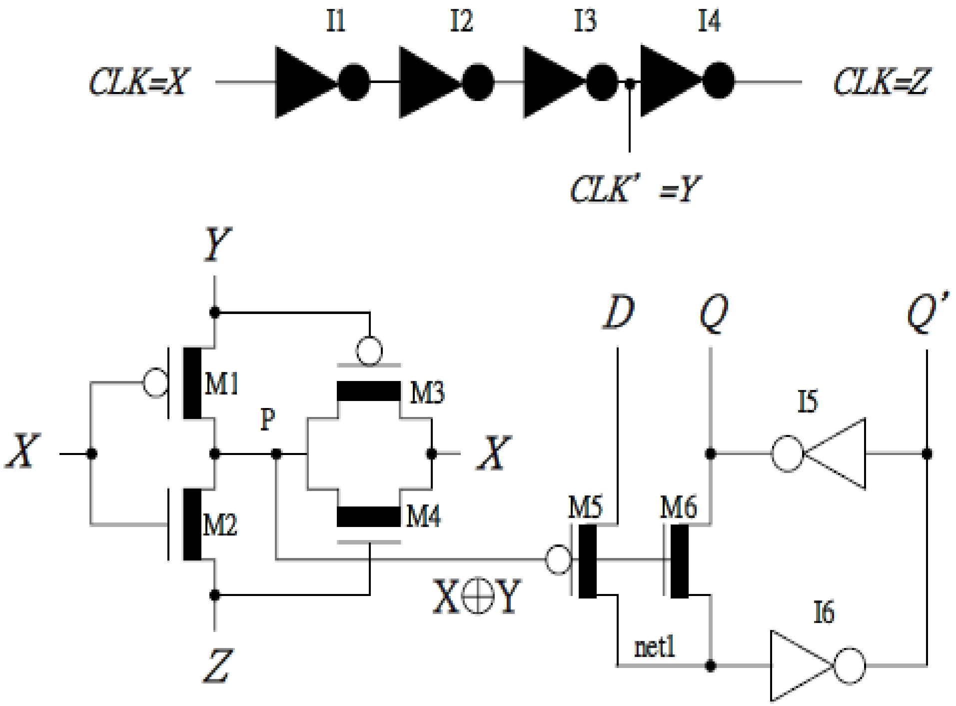


Fig. 2.2 (a) Single latch double edge triggered flip-flop [15]

In it power consumption has been reduced by at least 28% and the power-delay product is also reduced by at least 50%.The dynamic power consumption in a circuit is given by

$$P= f^* C^*Vdd^2 \qquad [3]$$

From equation, we know that the best way to decrease power consumption is to reduce supply voltage. But the schematic of the DET in Fig. 2.2(a) encounters bottleneck when the supply voltage decreases to 1.5V. Data transfer to Q through M5. When D is logic 0, net1 is not a perfect zero but at a threshold voltage Vth of M5. It causes I6 very slow when the supply voltage is 1.5V. In order to increase the speed, we first increase the PMOS's size of I6, but the effect of voltage is larger than that of size. The size becomes tremendous large, thus M5 is hard to transfer data to I6 because of large capacitance. Besides, the period of CLK must be increased to ensure the correct function. The method of increasing size is not only decreases speed but wastes power. Thus, we decrease Vth of M5. In addition, we also reduce the swing of CLK to decrease power consumption. To prevent performance degradation, low-Vt transistors are used for clocked transistors without significant leakage current problems.

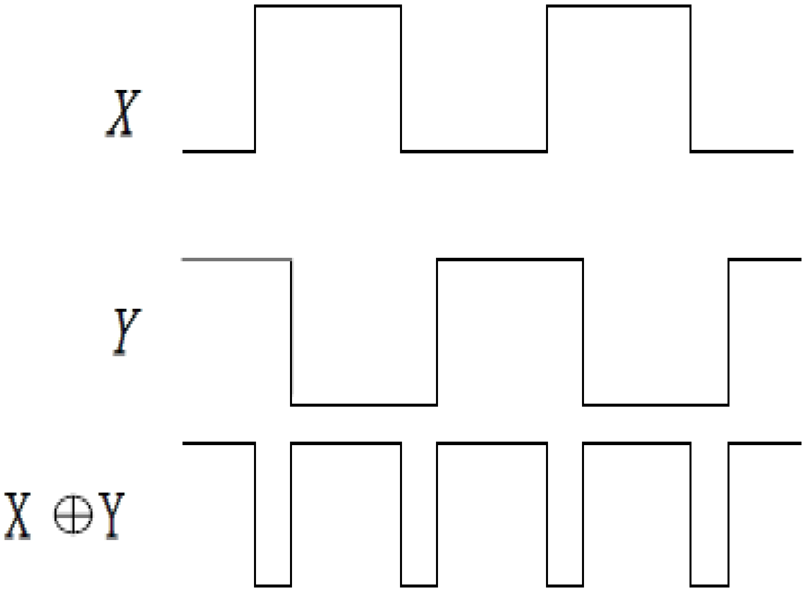


Fig. 2.2 (b) Clock timings [15]

Node P =X xor Y = CLK xor CLK'.

There is a short period of time after each clock signal transition where node P is low or high. During this short period of time the XOR gate outputs logic "0" or "1"thereby turning on or off M5 and M6.Then the signal D transmits the output to Q. The back-to-back inverters I5 and I6 will hold the data and the further of the input signal. D will not affect the output Q.

2.3 **A low power high density double edge triggered flip flop for low voltage systems [11]**

Figure 2.3(c) shows static master slave double edge triggered flip-flop. Comparisons were made with other state of the art double edge triggered flip-flop designs. Flip-flops were investigated using standard parameters, optimization techniques and extensive simulation procedures. Power results of Fig. 2.3(c) flip-flop has improvement of 20% and 58.63% in terms of total power dissipation when compared with DETFF of Fig. 2.3(a) (dual edge triggered flip-flop) and DETFF in Fig. 2.3(b) respectively.

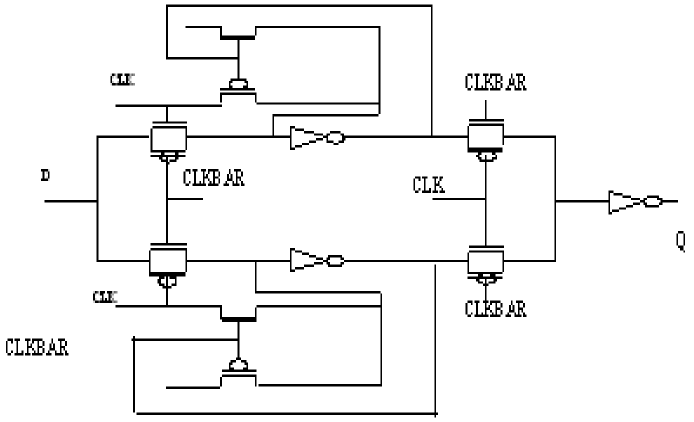


Fig. 2.3 (a) Hossain’s DETFF [11]

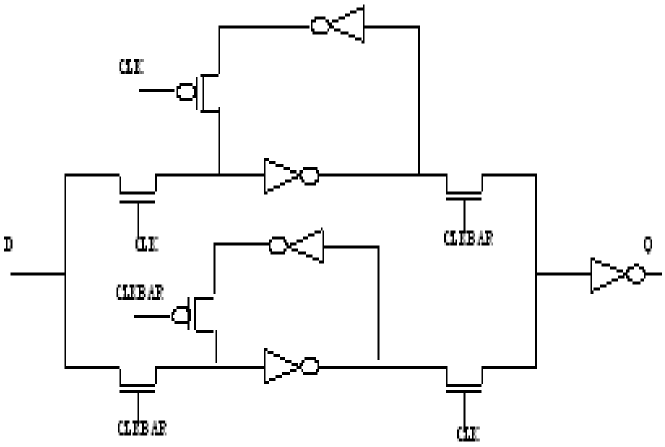


Fig. 2.3 (b) Pedram’s DETFF [11]

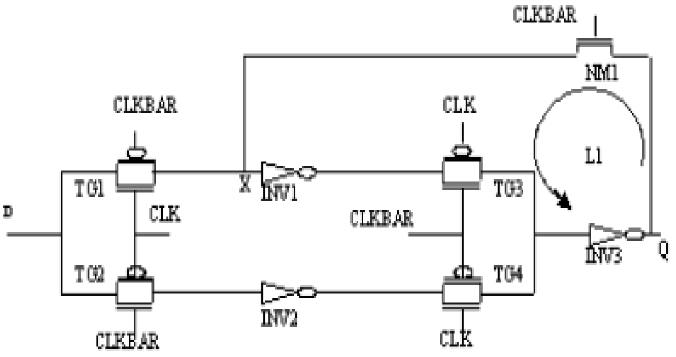


Fig. 2.3 (c) Tiwari’s DETFF [11]

The flip-flop also shows appreciable results with 21% and 55.7% percent improvement in terms of power delay product as compared to DETFF in Fig. 2.3(a) and DETFF in Fig 2.3(b) respectively. More over the Fig. 2.3(c) design has an improvement of 39.9% and 27.27% in terms of total transistor width over DETFF 2.3(a) and DETFF 2.3(b) respectively, which makes the flip-flop suitable for low power, high density applications.

The structure is based on master slave configuration. It has two data paths, the upper data path consisting of TG1, INV1 and TG2; the lower data path consisting of TG3, INV2 and TG4. The input data is connected to TG1 and TG3 and the output is taken from INV3 whose input is in turn connected with TG2 and TG4. A feedback transistor NM1 (NMOS) is employed as a switch such that its one end is connected with output ‘Q’ and other to an intermediate node ‘X’ in upper data path. The transmission gates (TG) in both the data path are clocked such that upper data path works as negative edge triggered flip flop and lower data path works as positive edge triggered flip-flop. The novelty of the design lies in the feedback strategy used to make the flip-flop static using a single pass transistor as a switch through loop L1. When the clock is grounded, the logic level at the output is maintained by the regenerative action of the loop L1 which has two inverters INV1 and INV3 in the forward path and a switch NM1 in the feedback path. The main advantages of this flip-flop are reduced transistor count, increased performance and low power consumption.

2.4 **Low-power double edge-triggered flip-flop circuit design [14]**

This DET flip-flop uses only 12 transistors in addition to the clock driver, and hence requires a small area.

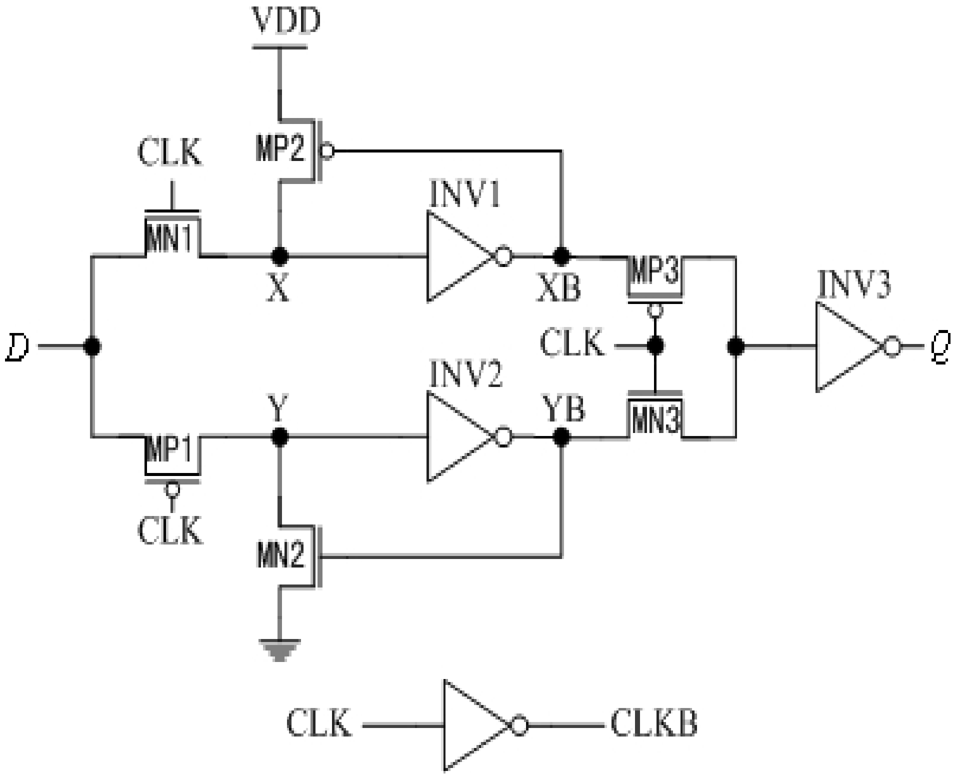


Fig. 2.4 DET flip-flop [14]

Several HSPICE simulations with different input sequences show that the DET flip-flop reduces power consumption up to 85%, as Compared to conventional DET flip-flops. The DET flip-flop is illustrated in Fig. 2.4. This design can be thought of as a parallel connection of two latches, one transparent when the clock is high and the other transparent when the clock is low, with a multiplexor selecting the output of the latch that is in hold state. In the upper data path, transistor MP2 provides feedback to pull up storage node X substantially to VDD when signal node XB is low. Pull-up transistor MP2 ensures that, although a clock signal applied to the gate of MN1 does not reach the voltage VDD, the storage node X can still reach VDD. In the lower data path, transistor MN2 provides feedback to pull down node Y to a lower voltage when the signal node YB is high. The inclusion of pull-down transistor MN2 ensures that, although the clock signal applied to the gate of MP1 does not reach the voltage GND, the storage node Y can still reach GND. When the clock is in the "high" state, for the upper data path, the input signal D is quickly conducted into the node XB. If the input signal D is "high", node X goes to the logic high with help from the pull-up transistor MP2. Node X remains high as long as input signal D is at the high level. Meanwhile, for the lower data path, the previously hold data is quickly pass to the output node Q with help from the transistor MN3. On the contrary, when input signal D falls while the clock is in the "low" state, for the lower data path, the input signal D is quickly conducted into the node YB and node Y goes to the logic low with help from the pull-down transistor MN2. Node Y remains low as long as input signal D is at the low level. Meanwhile, for the upper data path, the previously hold data is quickly pass to the output node Q with help from the transistor MP3.

2.5 **Low power latch design in near sub-threshold region to improve reliability for soft error [10]**

This latch consists of IBPN shown in Fig. 2.5(a) and AFSC shown in Fig. 2.5(b) circuits. AFSC means alternative feedback stacked CMOS and IBPN means independent bias NMOS and PMOS.

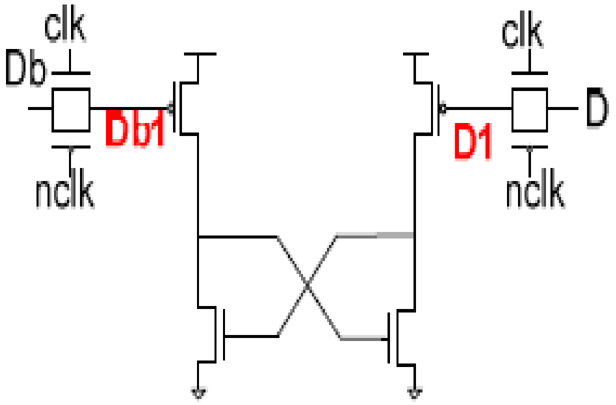


Fig. 2.5(a) IBPN [10]

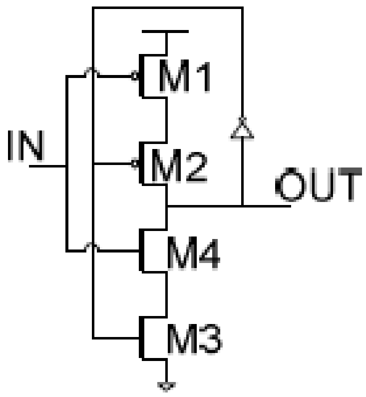


Fig. 2.5(b) AFSC [10]

Integrating the circuit components forms the latch circuit which is shown in Fig. 2.5(c). The latch Achieves low power with a less penalty in delay and area. In Fig 2.5(c), M21-M24 and I1 is an AFSC circuit to isolate The “OUT’’ node from Transient Faults. M9-M12 is a normal Clocked inverter which is required to initiate AFSC-3 to a correct state. Simulation results show that D1 and DB1 nodes were having the least Qcrit in the whole circuit. Hence the circuit was optimized to improve the critical charge for these nodes. Suppose Db1 is stored with logic 0, then M2 and M3 are switched on. If any TF occurs on node Db1 which changes its value to logic 1 then AFSC-2 and AFSC-1 will block the TF. This protects the node OUT from changing. The OUT node is kept at correct logic value by node D1. The same scenario can be explained if TF occurs at node D1 and OUT will be isolated from D1 by AFSC-3. The OUT node will change its State in static mode when both D1 and Db1 have a TF Simultaneously which is very rear to occur.

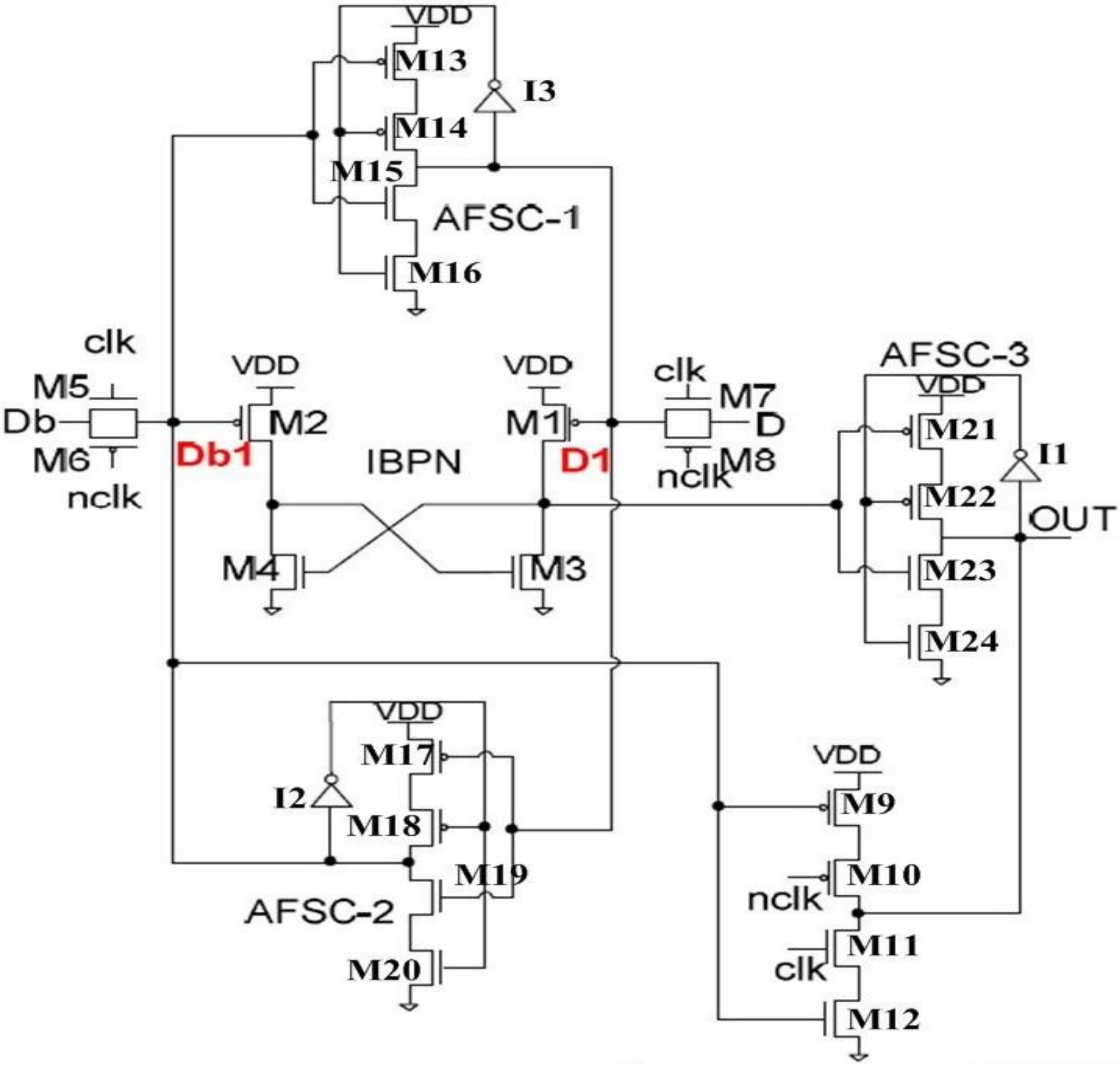


Fig. 2.5(c) DET latch circuit [10]

Also, if any TF Occurs on data switch M5, M6, M7 and M8 it will be suppressed by input signals since these switches are connected to external input signals. It is a new hardened latch for ultra deep submicron technology. The circuit is designed, analyzed and simulated using predictive models at 45nm technology with 0.5V of power supply. The flip-flop circuit [10] is immune to soft error and is intended to use in low power applications. The new circuit is compared with previous 3 hardened latches. Simulation results show that the new circuit is able to prevent transient faults 15 times better than the previous hardened latches with delay improvement but at the cost of power and area.

2.6 **A novel dual edge triggered near-threshold state retentive latch design [9]**

The flip-flop [9] is also a dual edge triggered circuit which is triggered by an external pulse. The circuit topology for pulse generating circuit is shown in Fig. 2.6(a). CLK is a regular clock signal and CLKB is a delayed CLK signal. The delay difference between CLK and CLKB signal determines the width of the pulse. The pulse is generated using two transmission gates. The TG1 is enabled by CLKB and the positive edge of CLK is converted into a pulse. The TG2 is enabled by inverted CLKB and the negative edge of CLK is converted into pulse. Consequently both positive and negative edge of the CLK is converted into pulse.

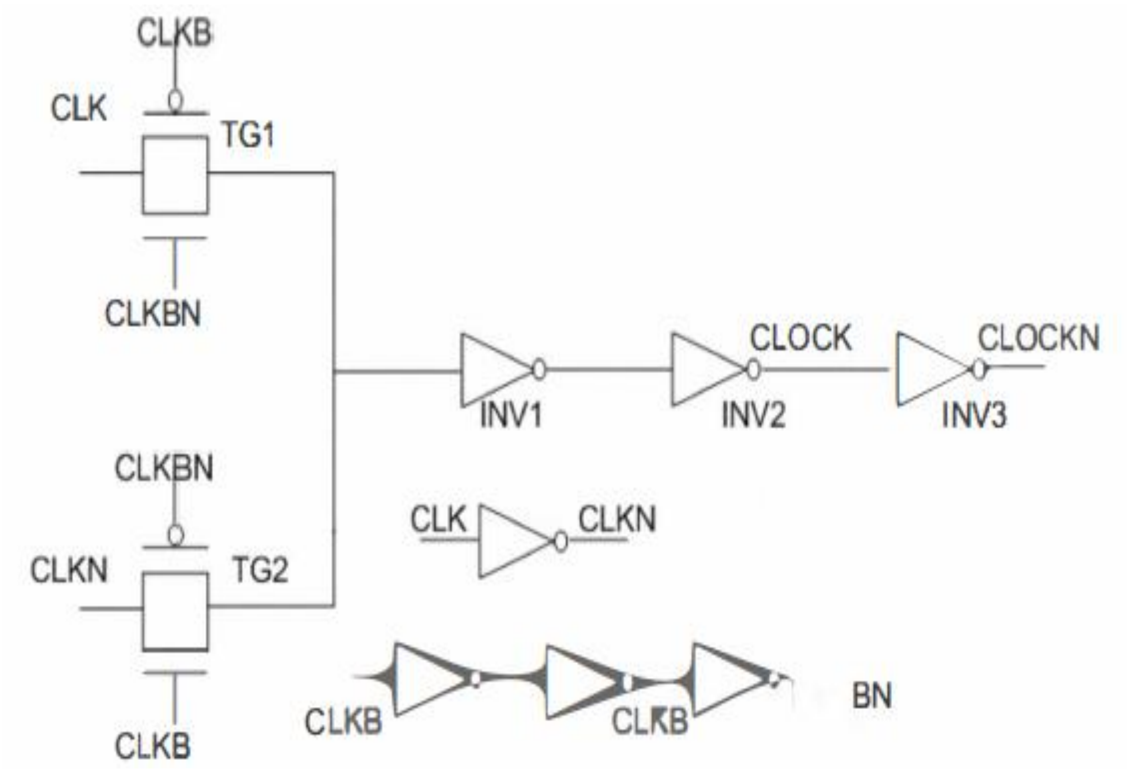


Fig. 2.6(a) pulse generating circuit [9]

Figure 2.6(b) shows the circuit diagram of the designed FF. In the transparent mode (CLOCK=l) TG1 and TG2 allows the data to be latched. M1-M4 and M5-M8 allows the output node QB and Q to bias to the correct state. Inverters INV1 and INV2 and M9-Ml0 and M1l-M12 transistors stores the correct data during static mode. All these operations are done when Sleep signal is low which is called as functional or the active mode of operation. When Sleep is high the circuit enters retention or sleep mode, which is used to save power by switching-off some part of the transistors in the circuit while retaining the logic state using transistors which are not affected by 'Sleep' signal.

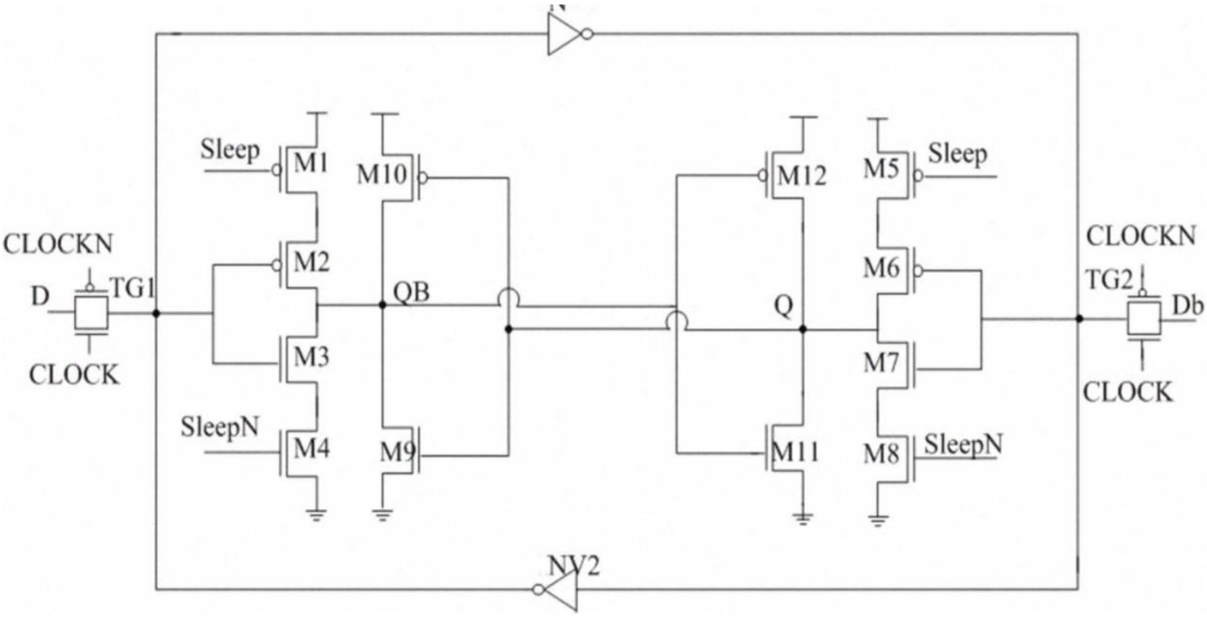


Fig. 2.6(b) Dual-edge triggered FF. [9]

When Sleep is high M1, M4, M5, M8 transistors switch-off and hence M6-M7 and M2-M3 transistors are cut-off from power supply. Hence the power dissipated by these transistors is reduced. But M9, M10, M1l and M12 transistors retain the data since these are not dependent on 'Sleep' signal. When the sleep signal goes low again, circuit state and normal functioning of the flip-flop is retained. The circuit uses the idea of power gating during the sleep or idle mode thereby avoiding leakage but still retaining its state.

It uses a dual edge triggered pulse which is a pulse trigger at both the rising and falling edges of the clock. The circuit used low Vth Devices only and hence can operate at Vdd as low as 0.5 V. The circuit was simulated using HSPICE at 45nm technology which results in reduced power delay product.

2.7 **Comparison**

The study of previous work tells the techniques used for reduction of power consumption and propagation delay. Speed is increased by reducing the clock frequency and by reducing the setup and hold time for the data. Power includes the static power and the dynamic power consumption. Static power consumption is in standby mode due to leakage current and the dynamic power consumption is due to the charging and discharging of the capacitances which comes into existence as the technology scales down. Method used for the reduction of the dynamic power employs the reduction of the power supply. But reducing power supply increases the delay and leakage current when the supply is reduced near, equal to or below the threshold voltage. So reduction in power consumption can be achieved by suitable tradeoff between the supply voltage and the delay and leakage current. Static power is reduced by power gating method. Multi threshold circuit can also be used to reduce the leakage current and then power.

The digital circuits are synchronous circuits and the make use of clock for their operation in order to reduce the complexity. Clock in VLSI digital circuits design consumes lot of power in clock network and clock buffer. This power is reduced by reducing the clock frequency. So the single edge triggered flop-flops are replaced by dual edge triggered flip-flops which makes less use of clock cycles to produce the same throughput as produced by single edge triggered flip-flop. Thus reduces the power consumed by the clock. Comparison of flip-flops is given in table 2.7.

Table 2.7 Comparison of flip-flops from literature.

Parameters	**[8]**	**[7]**	**[13]**	**[1]**	**[15]**	**[3]**	**[14]**	**[11]**	**[9]**
Year	1994	1998	2001	2002	2004	2006	2008	2010	2011
Technology (µm)	0.18	0.18	0.18	0.18	0.18	0.18	0.18	0.18	0.045
Power (µW)	877	1690	66.3	90.9	47.8	139	58.42	699	0.0911
Supply Voltage(V)	1.8	1.8	1.5	1.5	1.5	1.8	1.8	1.8	0.5
PDP(fj)	360	640	50.5	39	19.6	20.6	-	283.09	0.0220
Low clock swing Voltage(v)	-	-	-	-	1	-	-	-	-
Transistor count	-	-	-	-	-	-	12	15	20

3.1 INRODUCTION

This chapter includes the simulation result of different flip-flops which are studied at 180 nm technology. It also includes the method used for reduction of reduction of power, transmission gate and types of flip-flops. Rest of the chapter is organized as follows: section 3.2 contain rising edge master slave flip-flop, section 3.3 contains TSPC based rising edge flip-flop, section 3.4 discuss about pulse static dual edge triggered flip-flop, section 3.5 contains dual edge master slave flip-flop and section 3.6 discuss about dual edge triggered TSPC based flip flop.

3.1.1 **Transmission gate**

The figure 3.1.1 shows transmission gate. Improvements in performance of static and dynamic circuit are obtained when switches are implemented with CMOS transmission gates.

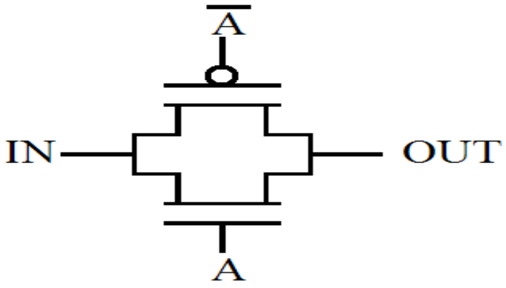


Fig. 3.1.1 Transmission gate

The transmission gate utilizes a pair of complementary transistors connected in parallel. It acts as an excellent switch, providing bidirectional current flow and it exhibits an on-resistance that remains almost constant for wide ranges of input voltage. It also prevents threshold loss and passes complete ‘0’or ‘1’

3.1.2 **Power gating**

Scaling the supply voltage and device threshold voltages (*V*t) to a level which just maintains acceptable performance is an effective approach for low-power operation. This method achieves low active power, but comes at a cost of increased standby power resulting from increased device leakage from the use of low-threshold devices. Multi-threshold CMOS (MTCMOS) has been described as a method of reducing standby leakage current in the circuit by using a high-threshold MOS device to decouple the logic from the supply or ground during long idle periods, or sleep states.

During active operation of the MTCMOS circuit, the power-interrupt switch is turned on by the SLEEP’ (or SLEEP) signal, and current dissipated by the logic is drawn through the interrupt switch, which causes a reduction in drive voltage seen by the logic, reducing logic performance. To compensate for the reduction in logic performance, larger power-supply voltages can be used at the expense of increased active power. For similar performance, larger device widths for the power interrupt switch can be used to minimize performance impact at the expense of increased area and power for entering and exiting sleep mode. Adjustment of device implants to allow moderately high-threshold values is another technique that can be used to increase performance at the expense of increased device leakage during idle mode.

3.1.3 **Static and dynamic flip flops**

Flip-flops are categorized as dynamic and static. Static sequential circuits rely on cross coupled inverter, which is a bistable element to memorize the values. These store value for long time and it remains there as long as the supply voltage is applied to the circuit.

Dynamic sequential circuits make use of parasitic capacitance as a temporary storage of data. The stored charge is used to represent the signal. Presence of charge makes the logic‘1’while absence makes logic ‘0’. Charge leakage is the always present in dynamic circuits so to store the data for the longer time a periodic refresh of the value is necessary.

All the simulations are carried out for 180 nm technology with following data

Frequency	250 MHZ
Load capacitance	21fF
Rise time	0 .1 ns
Fall time	0.1 ns
Input period	10 ns
Sleep period	32 ns

3.2 Rising edge mater slave flip flop [5]

Figure 3.2(a) shows positive edge triggered master slave flip-flop [5]. On the low phase of clock master stage is transparent and on the high phase slave is transparent. When the clock is low T1 is on and T2 is off, and the D input is sampled onto node Qm. During this period T3 is off and T4 is on. The cross coupled inverters (CMOS inverter 5 and 6) hold the state of slave latch. When the clock goes high, the master stage stops sampling the input and goes to hold state. T1 is off and T2 is on, and the cross coupled inverters CMOS inverter 2 and 3 hold the state of Qm.T3 is on and T4 is off, and Qm is copied to the output. Width of PMOS and NMOS in inverter is 1.4µm and 0.27µm. and Transmission gate are 0.67µm and 0.27µm respectively. Setup time is 290ps and hold time is 0. Power and propagation delay are calculated by using following formulae.

$P = \frac{Vdd}{T}\int_0^T idt$, where

P is dynamic power dissipation

T is time period

Vdd is supply voltage.

Propagation delay is given by $\tau p = (\tau hl + \tau lh)\frac{1}{2}$

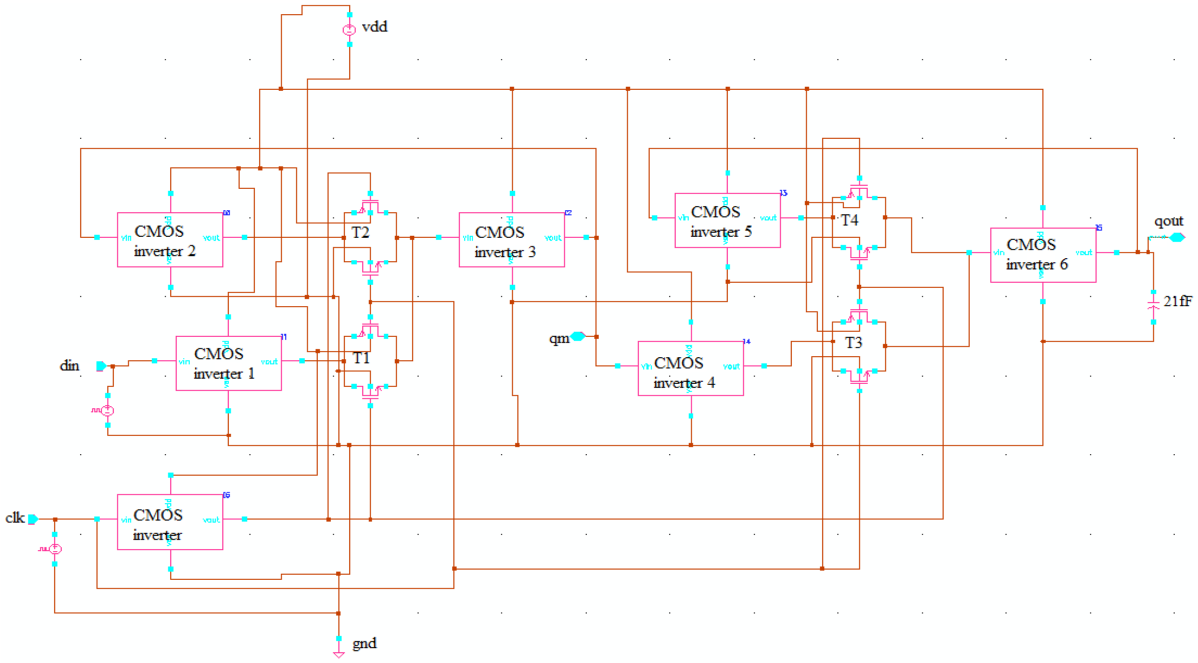


Fig. 3.2(a) Rising edge master slave flip flop.

Figure 3.2(b) shows the simulation results of rising edge master slave flip-flop and the table 3.2 shows the power dissipation and propagation delay of rising edge master slave flip-flop at different supply voltages. Propagation delay and power is inversely proportional. Supply voltage reduces from 1.8V to 0.9V which gives reduction in power from 738 µW to 171 µW. To further reduce the power of this flip-flop the power gating technique can be applied and has been discussed in next section.

Fig. 3.2(b) Simulation of rising edge triggered master slave flip-flop.

Table 3.2 Propagation delay and power dissipation.

Supply voltage (V)	Propagation delay (ns)	Power dissipation (µW)
1.8	5.24	738
1.4	5.27	420
0.9	5.58	171

3.2.1 Master slave flip-flop with power gating

Figure 3.2.1(a) shows the proposed circuit diagram of positive edge master slave flip-flop with power gating. In it the working of the flip flop is controlled by sleep signal. Device is active when sleep signal is low and when sleep becomes high the device sleeps to save power. Rest of working is same as of circuit in Fig. 3.2.

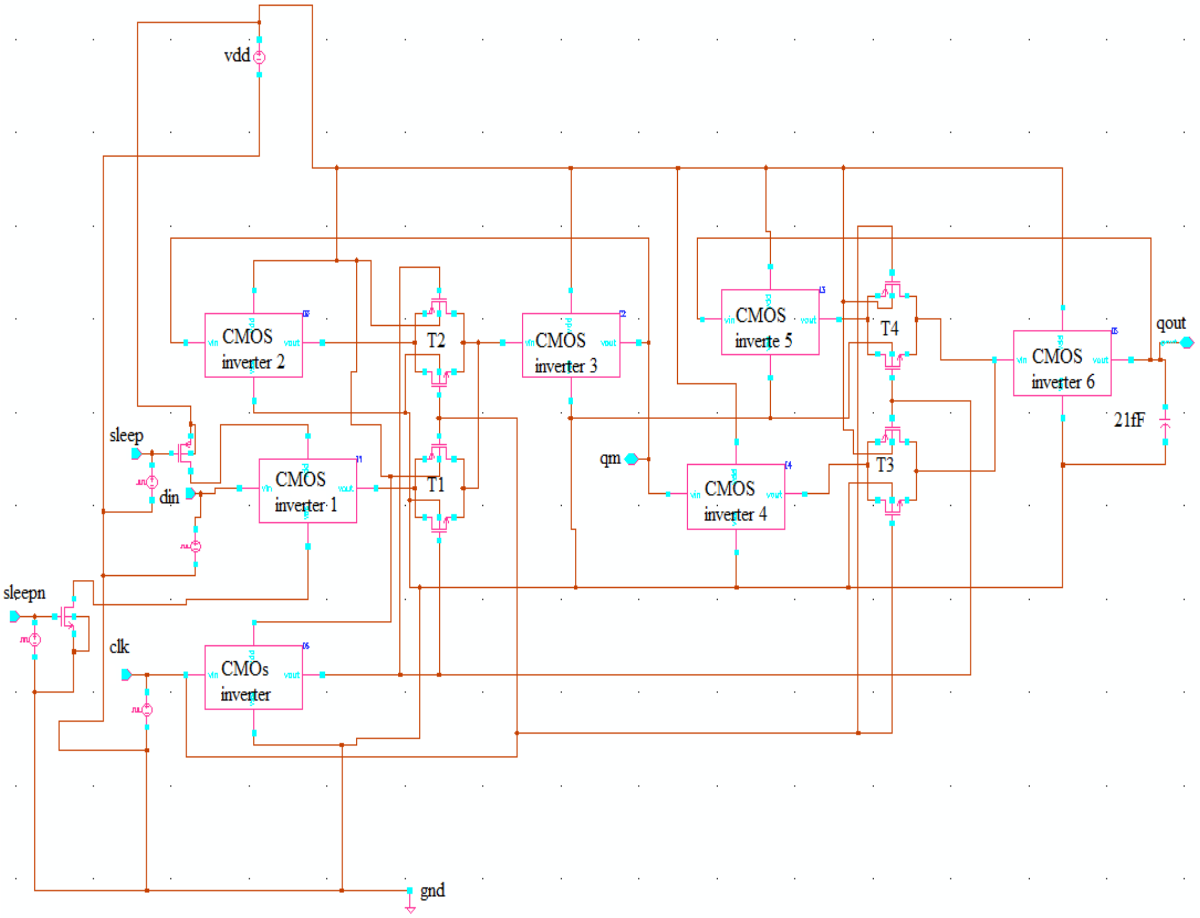


Fig. 3.2.1(a) Low power rising edge master slave flip flop.

Figure 3.2.1(b) shows the simulation results of positive edge triggered master slave flip flop. The simulation result clearly shows that when sleep is low only that time data is sampled by the input inverter and when sleep goes high sampling of input data is stopped and value is stored by CMOS inverter 6, inverter 5, inverter 3 and inverter 2 for sufficient time. Sleep signal acts as a control signal and it can be adjusted according to the need when the data is to be sampled by device.

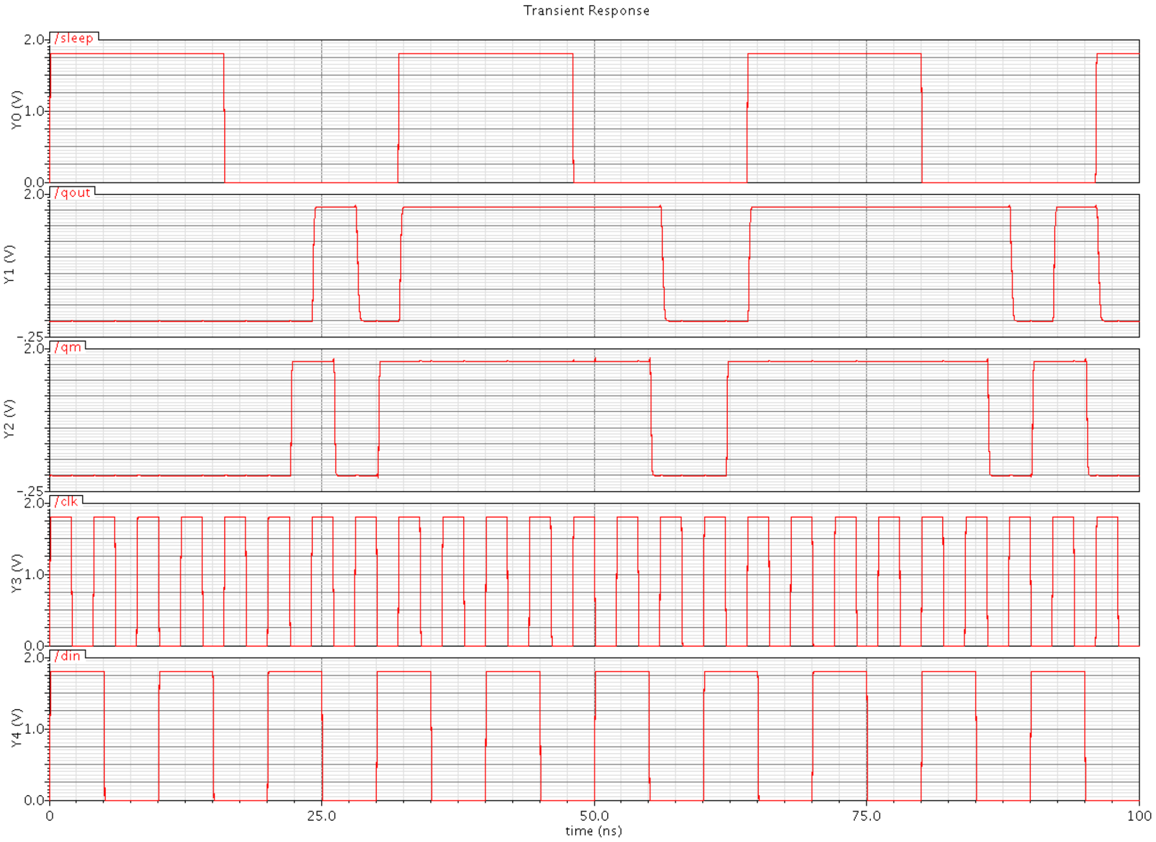


Fig. 3.2.1 (b) Simulation of low power rising master slave flip-flop.

Table 3.2.1 shows the power dissipation and propagation delay of rising edge master slave flip-flop at different supply voltages with power gating effect. Power is reduced in proposed flip-flop by 360 µW, 201.6 µW and 82.8 µW at 1.8V, 1.4V and 0.9V supply voltages respectively at cost of propagation delay.

Table 3.2.1 Power and delay of single edge triggered flip flop.

Supply voltage (V)	Propagation delay of proposed FF (ns)	Power dissipation of proposed FF (µW)
1.8	9.12	378
1.4	9.277	218.4
0.9	9.5835	88.2

3.3 TSPC rising edge flip flop [12]

Figure 3.3(a) shows the circuit diagram of rising edge dual edge triggered D flip-flop [12] which is based on true single phase clock (TSPC) principle. This circuit contains four stages with 11 transistors. At low clock signal the first stage act as a transparent latch to receive the input signal while the output node of the second stage is being precharged. During this cycle the third and fourth stages simply keeps the previous output state. When the clock signal switches from low to high the first stage stops to be transparent and the second stage starts evaluation. At that time the third stage becomes transparent and transmits the sampled value to the output. The final inverter stage is used to obtain non inverted output. The width of PMOS and NMOS transistors are 1.27µm and 0.45µm respectively. Figure 3.2(b) shows the simulation results of TSPC based rising edge flip-flop.

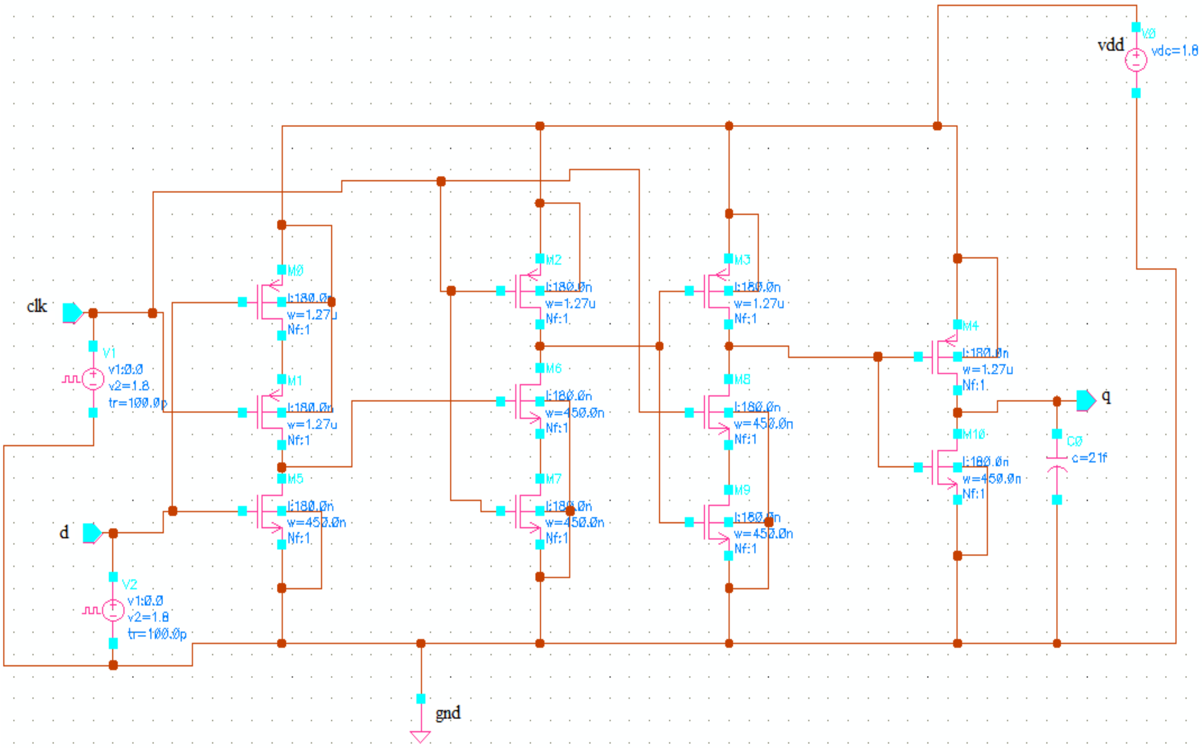


Fig. 3.3 (a) TSPC rising edge flip flop.

TSPC based flip flops have more advantages. It makes use of single clock throughout the circuit. Since there is no use of inverted clock so clock skew problem is not present. Signal swing is fully obtained at each internal node and different families can be easily used with TSPC.

Fig. 3.3 (b) Simulation of TSPC rising edge flip-flop.

Table 3.3 shows the delay and power dissipation of single edge triggered flip-flop. Power reduces from 373.77 µW to 89.55 µW with decrease in supply voltage from 1.8V to 0.9V. For further reduction of the power of TSPC flip-flop power gating technique can be applied and is discussed in next section.

Table 3.3 TSPC propagation delay and power dissipation.

Supply voltage (V)	Propagation delay (ns)	Power dissipation (µW)
1.8	5.1	373.77
1.4	5.2121	221.9
0.9	5.2837	89.55

3.3.1 **Positive edge TSPC flip-flop with low power**

Figure 3.3.1 (a) shows the proposed TSPC positive edge flip-flop with power gating which controls the output of flip-flop. Low value of sleep signal makes the system active and high value makes the flip-flop to sleep.

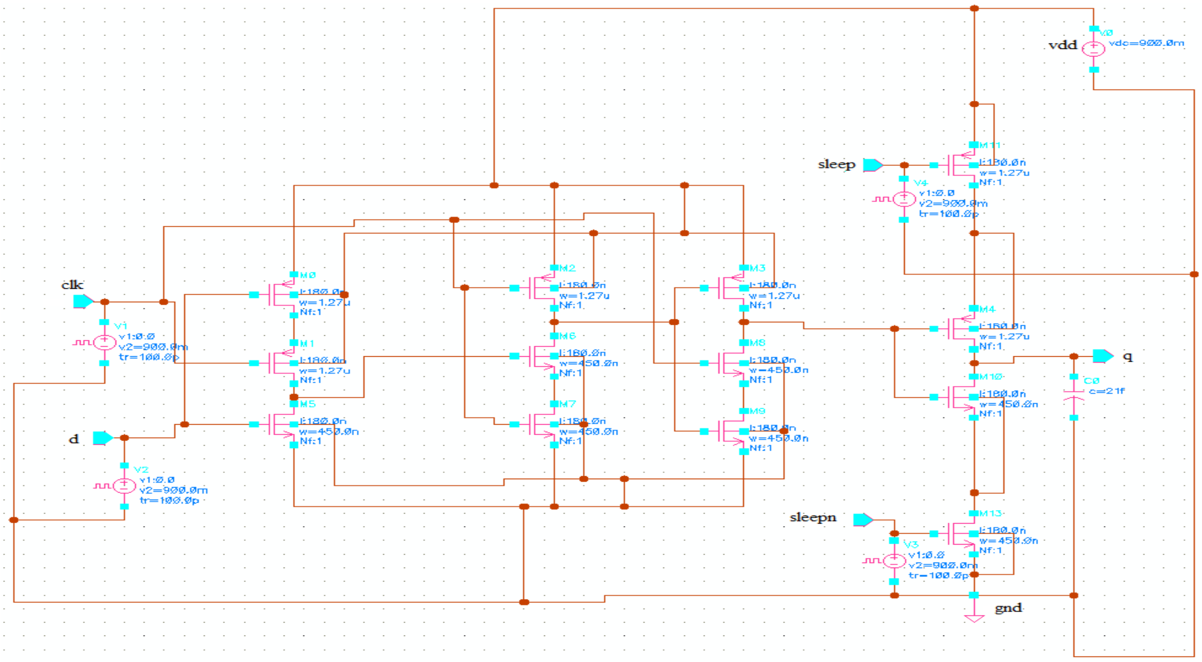


Fig. 3.3.1(a) Low power TSPC rising edge flip-flop.

Figure 3.3.1(b) shows the simulation results of rising edge TSPC based D flip flop with power gating effect.

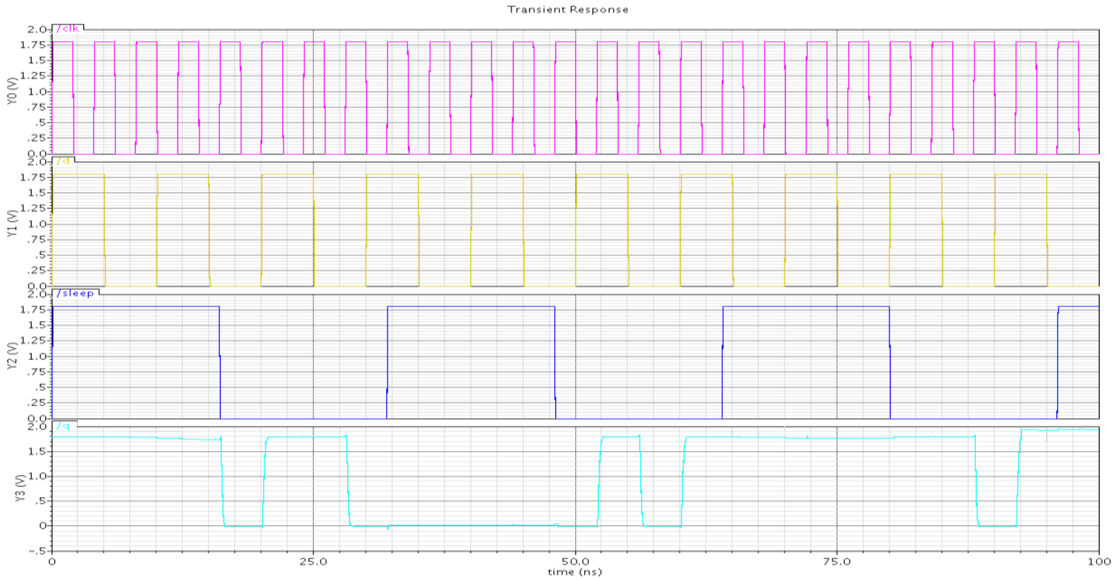


Fig. 3.3.1(b) Simulation of low power TSPC rising edge flip-flop.

Table 3.3.1 shows the dynamic power dissipation and propagation delay of proposed rising edge triggered TSPC based flip-flop. Proposed flip-flop consumes less power at cost of delay by amount 101.09 µW, 61.22 µW and 25.125 µW at supply voltages 1.8V, 1.4V and 0.9V respectively.

Table 3.3.1 Low power TSPC delay and power.

Supply voltage (V)	Propagation delay of proposed FF (ns)	Power dissipation of proposed FF (µW)
1.8	7.2105	272.68
1.4	7.2905	160.68
0.9	7.669	64.125

3.4 **Pulse static dual edge triggered flip-flop with V_{sb} effect**

The pulse static dual edge triggered flip-flop [9] and V_{sb} effect technique has been used.

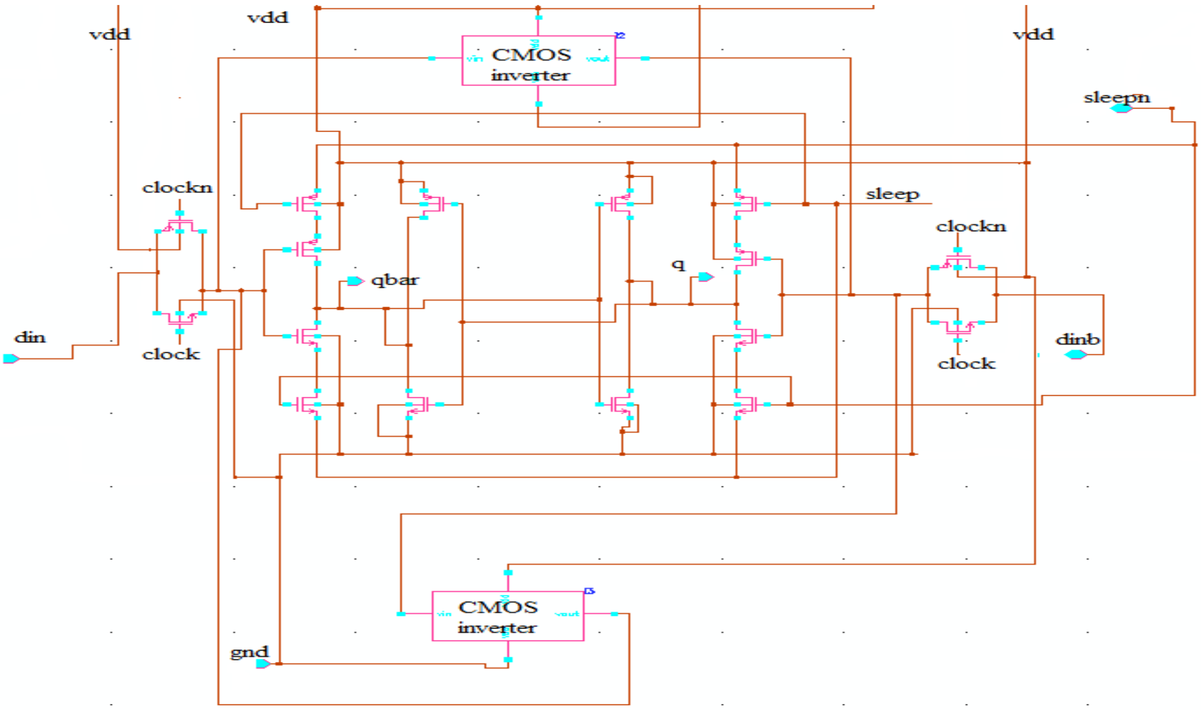


Fig. 3.4(a) Pulse static dual edge triggered flip-flop.

The proposed flip-flop is shown in Fig. 3.4(a). This flip-flop contains 20 transistors. When clockn is low and clock is high input is sampled and inverted input is obtained at the final output. Back to back inverters are used to hold the state. CMOS inverter holds the logic level true at the output of the each transmission gate by providing feedback from opposite side as shown in Fig. 3.4(a). Formula Sizes of transistors are given ahead.

Width of the output stage inverter of flip-flop and 3 inverter chains used in clock circuitry are found by using logical effort method. Formulae and calculation for this is shown next.

F = GHB where

F is path effort,

$\mathrm{B} = \frac{\text{capacitance on path} + \text{capacitance off path}}{\text{capacitance on path}}$ is the branching effort,

$\mathrm{H} = \frac{\mathrm{Cin}}{\mathrm{Cout}}$ is electrical effort,

G is logical effort which is 1 in case of inverter,

Sizes of inverter chain are found by starting from end inverter by using following formulae.

gh = $(F)^{1\backslash N}$ where N is number of stages

Cin = g Cout / $(F)^{1\backslash N}$ input cap for output inverter.

In this flip flop F=6.11, Cin =3.44*$(10)^{-15}$ (for minimum transistor sizes), Cout = 21* $(10)^{-15}$.

Then the widths of last stage inverter in flip-flop for NMOS and PMOS are Wn= 0.64 µm and Wp= 1.59 µm respectively. Similarly sizes of 3 stage inverter chain with N= 3 and F= 0.54 are found. For last stage Wn=0.89, Wp=2.23,for middle stage Wn= 0.72 µm, Wp= 1.81 µm and for first stage Wn= 0.58 µm, Wp= 1.47µm. The sizes of back to back inver are kept minimum Wn= 0.27µm, Wp= 1.4µm. Transmission gate acting as a switch have sizes Wp=0.675 µm, Wn=0.27 µm. Setup time is 100ps and hold time is 0.

Figure 3.4(b) shows the symbol of proposed pulse static dual edge triggered flip-flop with V_{sb} effect.

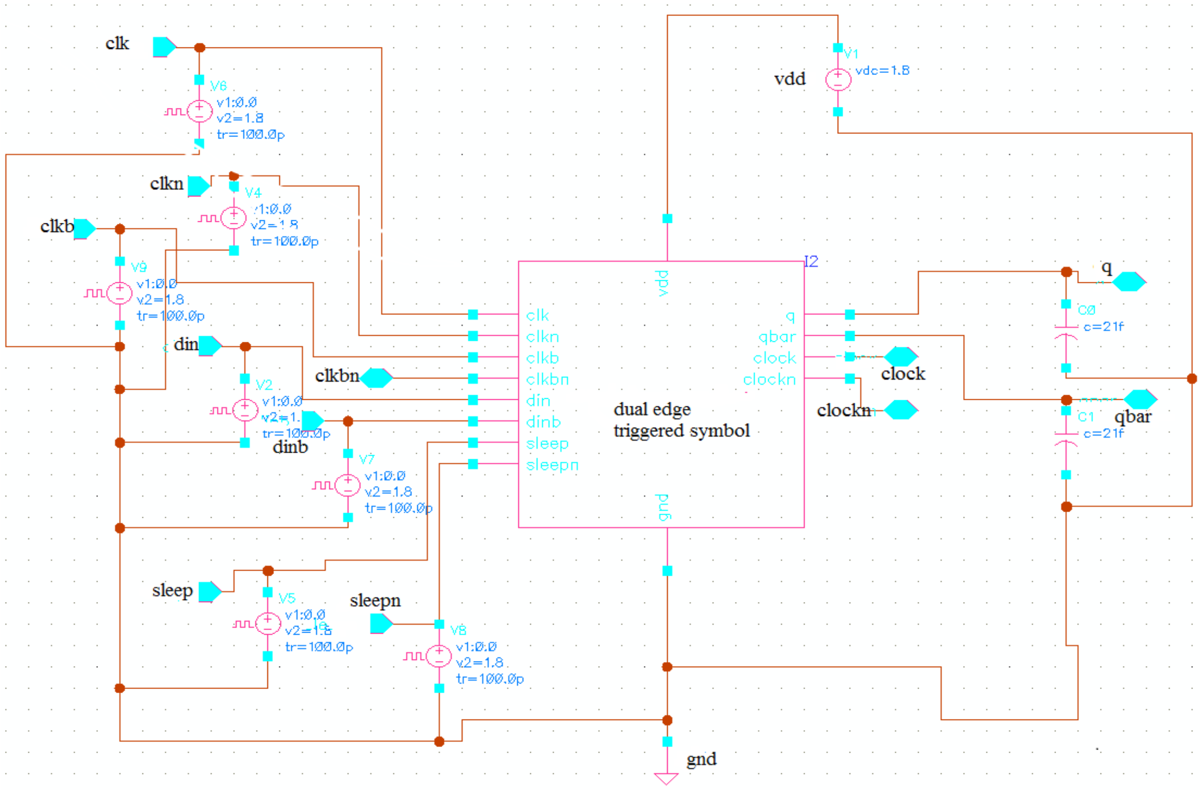


Fig. 3.4(b) Symbol.

Figure 3.4(b) shows simulation results of proposed flip-flop with 20 transistors.

Fig. 3.4(c) Simulation of pulse static dual edge triggered flip-flop.

Table 3.4 shows power and the propagation delay results of proposed pulse static flip-flop under back gating effect and pulse static dual edge triggered flip-flop [9] for different supply voltages. Results are taken for 180 nm technology. Power reduces from 2.205mW to 0.486mW for pulse static flip-flop [9] and for proposed flip-flop from 2.02mW to 0.427mW at supply voltages 1.8V and 0.9V respectively. Proposed flip-flop power reduced by an amount of 0.185mW and 0.059mW for 1.8V and 0.9V supply voltages.

Table 3.4 Power and delay of pulse static flip-flop.

	DETFF [9]		Proposed FF with V_{sb} effect	
Supply voltage	Propagation delay	Power dissipation	Propagation delay	Power dissipation
(V)	clk-q (ns)	(mW)	clk-q (ns)	(mW)
1.8	6.21	2.205	6.21	2.02
0.9	7.315	0.486	7.315	0.427

3.4.1 **Pulse static dual edge triggered flip-flop with reduced transistors**

Figure 3.4.1 shows the proposed pulse static D flip-flop with 18 transistors in count along

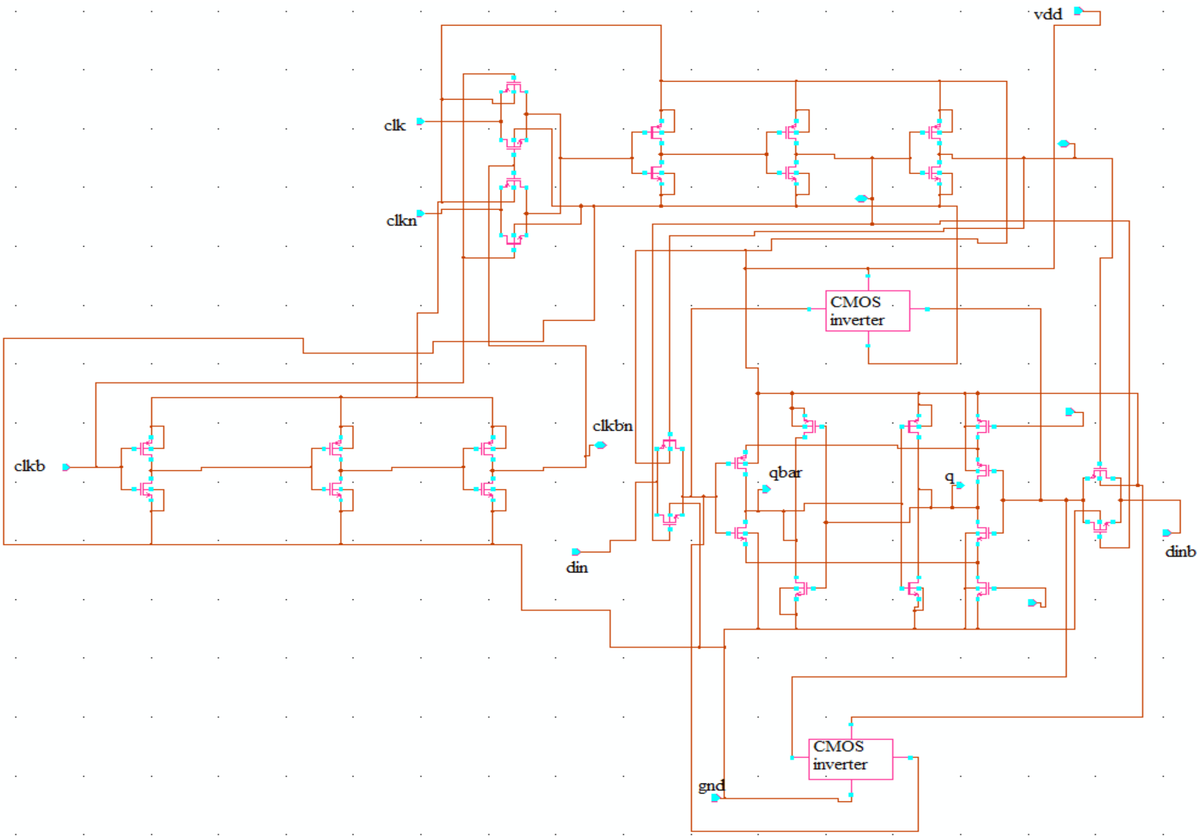


Fig. 3.4.1 Low power pulse static dual edge triggered flip-flop.

with clock circuitry. This circuit is run first without and after that with back gate effect. Results are tabulated in Tale 3.4.1.

Table 3.4.1 shows propagation delay and power dissipation of proposed pulse static dual edge triggered flip-flop. Propagation delay of the proposed pulse static dual edge triggered flip-flop does not change with V_{sb} effect.

Table 3.4.1(a) Power and delay without and with V_{sb} effect.

Supply voltage	Proposed FF without V_{sb} effect and 18 transistors		Proposed FF with V_{sb} effect and 18 transistors	
	Propagation delay	Power dissipation	Propagation delay	Power dissipation
(V)	clk-q (ns)	(mW)	clk-q (ns)	(mW)
1.8	6.496	1.9	6.496	1.6
0.9	7.5	0.405	7.5	0.349

The power of proposed flip-flop without V_{sb} effect is 1.9mW and 0.405mW for supply voltages 1.8V and 0.9V respectively. After applying V_{sb} effect the power of proposed flip-flop at supply voltages 1.8V and 0.9V are 1.6mW and 0.349mW respectively. Improvement of power reduction in proposed pulse static dual-edge triggered flip-flop with back gating effect is 0.3mW and 0.056mW at supply voltages 1.8V and 0.9V respectively as compared to without V_{sb} effect. This reduction in power is achieved without cost of propagation delay.

3.5 Mater slave dual edge triggered flip-flop with low power

Master slave dual edge triggered flip-flop circuit has been taken from Tiwari's flip-flop [11] and power gating technique has been applied. Figure 3.5(a) shows the proposed master slave dual edge triggered flip-flop with power gating. Working of proposed flip-flop is similar to Twari's flip-flop [11] at active sleep signal. Sizes of inverter are found by logical effort method and these are same for lower and upper path of flip flop. In this flip-flop the value of Cin= 1.73fF, Cout= 21fF, F= 12.11, N= 2, $F^{1\backslash N}$ = 3.48. Sizes of last stage inverter are Wn= 1.2 µm, Wp=2.8 µm and first stage inverter are Wn=.32 µm, Wp=.8 µm . The sizes of sleep transistor are Wp= 1.4 µm, Wn= 0.27µm. Pass transistor is kept minimum, Wn= 0.27 µm and Wp= 0.67 µm.

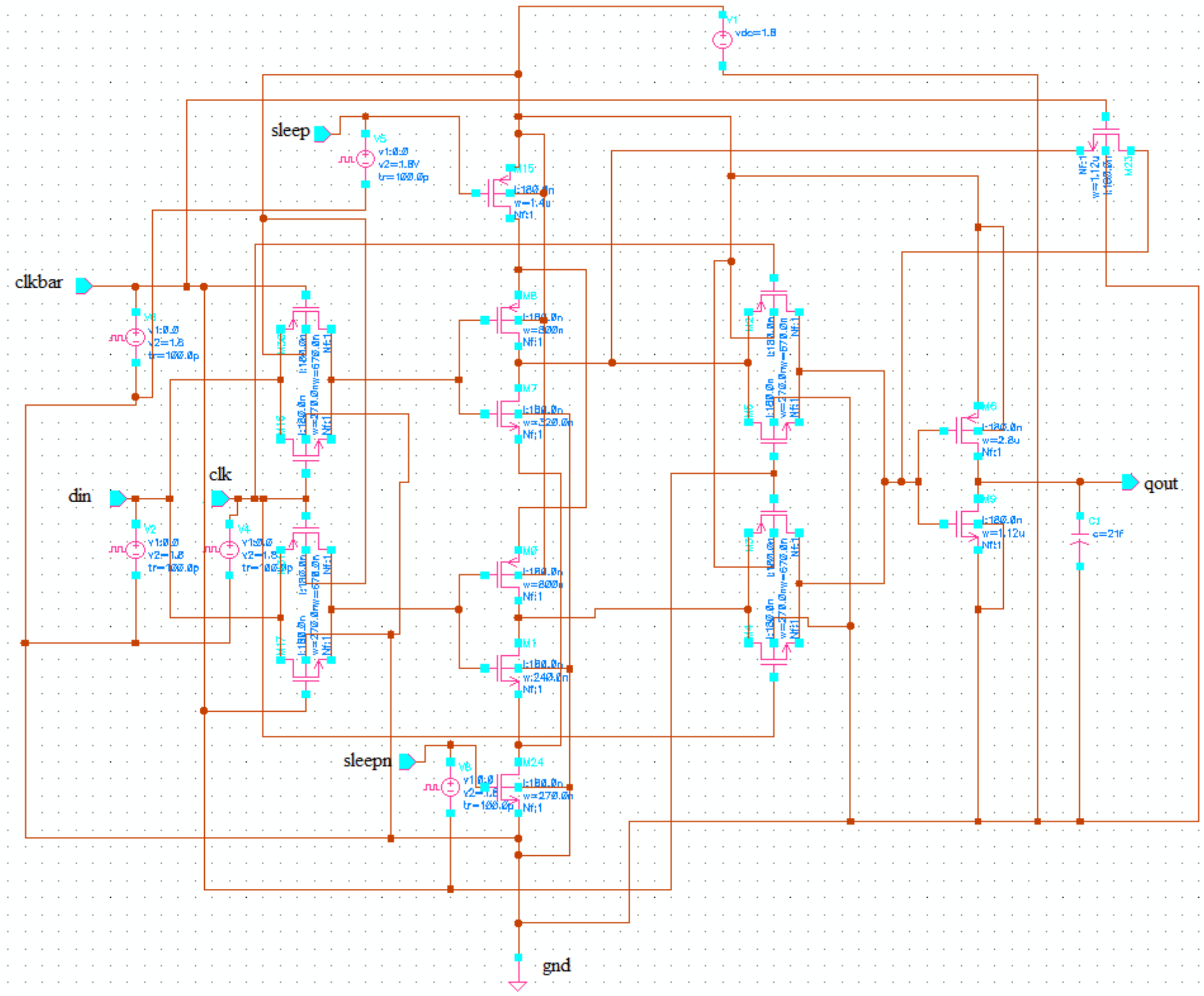


Fig. 3.5(a) Low power mater slave dual edge triggered flip-flop.

Circuit of proposed flip-flop in Fig 3.5(a) works at low value of sleep signal. This flip flop has two paths upper path and lower path which works alternately. When clock signal is high input is read by upper path transmission gate and output comes from lower path transmission gate at output and when clock signal is low input is read by lower path transmission gate an output comes from the upper path output transmission gate which gives the value stored in previous clock pulse.

Figure 3.5(b) shows the simulation results of proposed dual edge triggered master slave flip-flop. Device is active when sleep signal is low and results, power dissipation and propagation delay, are shown in Table 3.5(a) for different supply voltages.

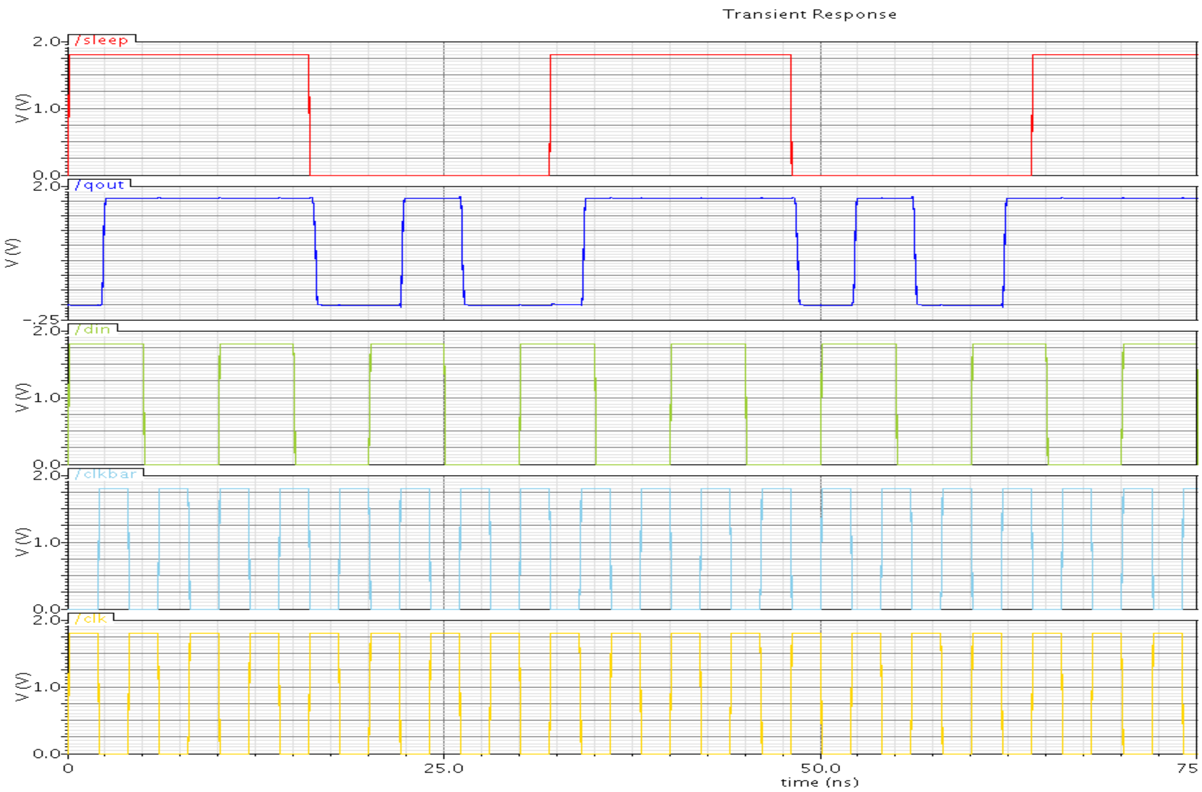


Fig. 3.5(b) Simulation of low power dual edge triggered master slave flip-flop.

Table 3.5(a) shows the power of proposed dual-edge master slave flip-flop reduces from 4.62 µW to 79.5 µW as the supply voltage decreases from 1.8V to 1V with certain cost of propagation delay.

Table 3.5(a) Power and delay of dual edge triggered master slave flip flop.

Supply voltage (V)	Proposed master slave dual edge triggered flip-flop	
	Propagation delay (ns)	Power dissipation (µW)
1.8	5.17	462.15
1.6	5.19	295.9
1.4	5.242	189
1.2	5.3235	125
1	5.4965	79.5

Table 3.5(b) shows the power comparison of the proposed master slave dual edge triggered flip-flop with power gating with other low power flip-flop in the literature. The power dissipation of proposed flip-flop is much less than all master slave flip-flop in

literature. Proposed flip-flop power is 236.5 µw, 228.1 µw, 214 µw, 166 µw and 116.5 less than Tiwari’s flip-flop at supply voltages 1.8V, 1.6V, 1.4V, 1.2V and 1V respectively.

Table 3.5(b) Comparison of flip-flop’s power.

Supply voltage (V)	Pedram's FF [7] Power dissipation (µW)	Hossain's FF [8] Power dissipation (µw)	Tiwari's FF[11] Power dissipation (µW)	Proposed FF Power dissipation (µw)
1.8	1690	877	699	462.15
1.6	1230	670	542	295.9
1.4	836	493	403	189
1.2	532	Failed	291	125
1	297	Failed	196	79.5

3.6 TSPC dual edge triggered flip flop

Figure 3.6(a) shows a novel dual edge triggered TSPC D flip-flop. This flip-flop contains 24 transistors including upper portion and lower portions with four stages in each. In upper part input is given to PMOS which makes it active when clock is low and output is seen when the clock goes high. So, upper part is active low rising edge portion. Due to this upper portion of flip-flop samples input data during rising edge of clock.

The lower portion is active when clock is high because input is given to NMOS and output is seen when clock goes low. This makes lower portion active high and falling edge which samples the data when clock goes low. In this way the flip flop samples data at both the edges of clock.

The sizes of this flip-flop are also found by logical effort method for upper and lower paths. For this Cin= 5.14fF, Cout= 21 fF, F=8.16, N=4, $F^{1\backslash N} = 1.69$ and the sizes of last stage are Wn=2.31µm, Wp= 5.79 µm, third stage sizes are Wn= 1.38µm, Wp= 3.44µm, second stage sizes are Wn= 0.86µm, Wp= 2.5µm, and fir stage sizes are Wn=0.55µm, Wp= 1.38µm.

The upper portion which consists of four stages contains two static PMOS (SP) and two static NMOS (SN) stages which makes it positive edge triggered. The lower portion also contains four stages, first two stages are static NMOS (SN) and rest two is static PMOS (SP) stages making it negative edge triggered.

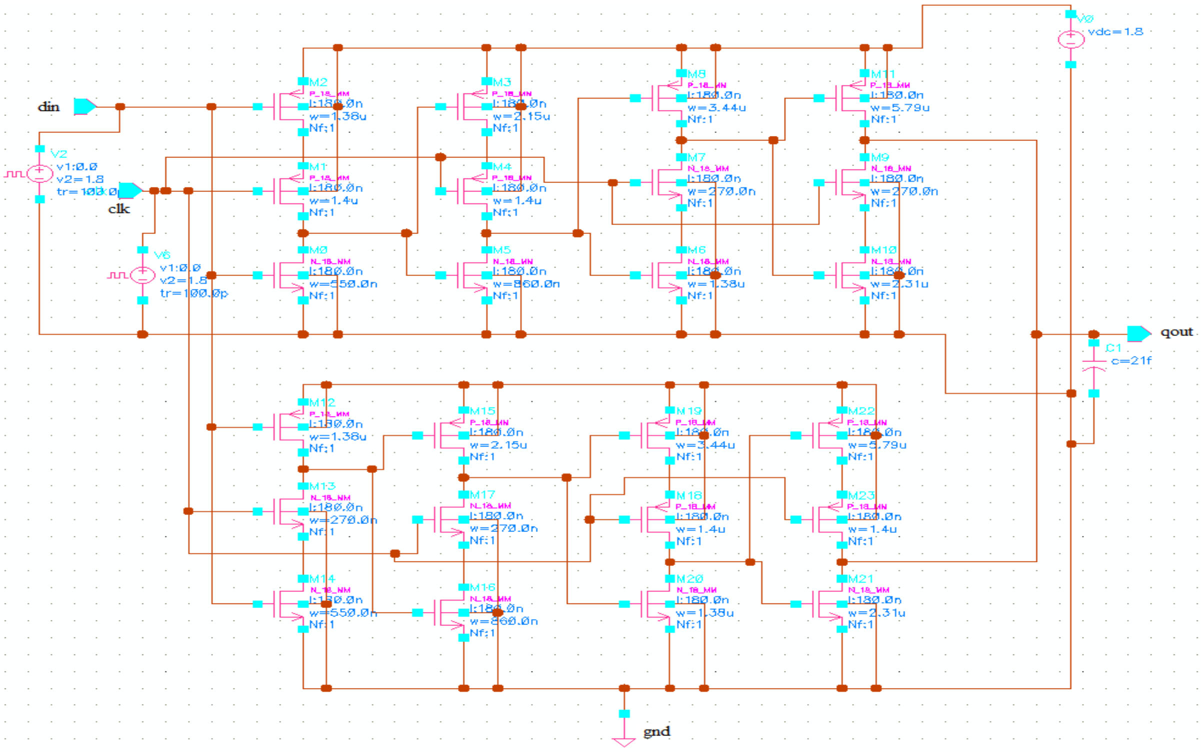


Fig. 3.6(a) TSPC dual edge triggered flip-flop.

Figure 3.6(b) shows the simulation results of proposed dual edge triggered TSPC based flip-flop.

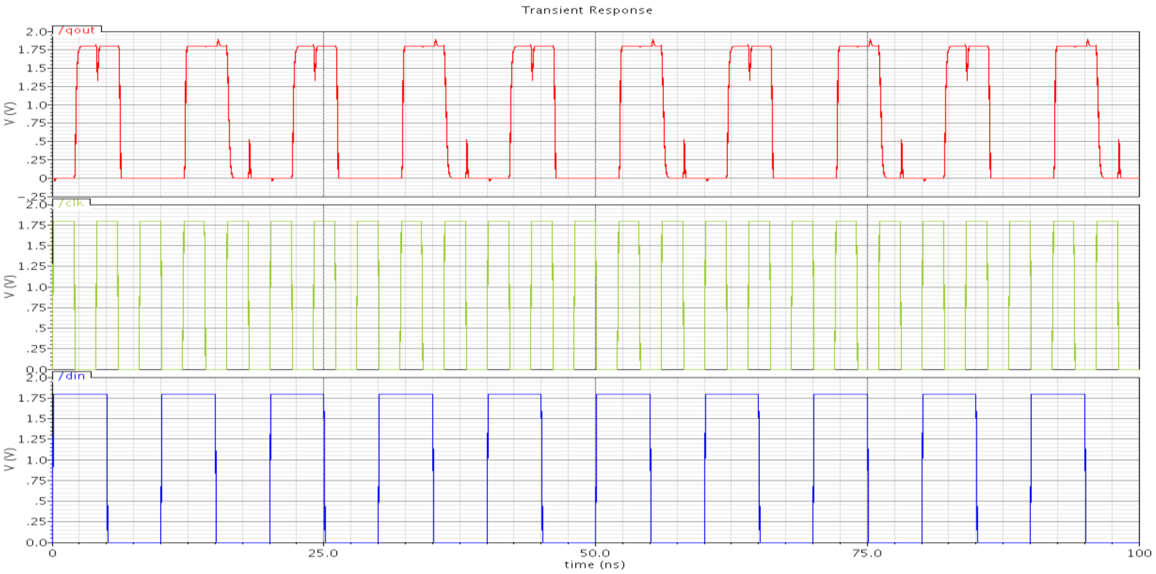


Fig. 3.6(b) Simulation of TSPC dual edge triggered flip flop.

Table 3.6 shows power and delay optimization of proposed dual edge triggered TSPC flip-flop at different voltages. At high supply voltages power is in mW but with decrease in supply voltages power reduces to micro watt. Power reduces from 1.46mW to 324 µW as supply voltage reduces from 1.8V to 0.9V. The power dissipation is much less with hardly increasing in propagation delay.

Table 3.6 Power and delay of proposed novel TSPC dual edge triggered flip-flop.

Supply voltage (V)	Propagation delay (ns)	Power dissipation (mW)
1.8	4.1853	1.46
1.6	4.216	1.136
1.4	4.247	0.854
1.2	4.31265	0.612
1	4.43615	0.41
0.9	4.55905	0.324

Chapter4 Layout and post layout simulations

4.1 INTRODUCTION

This chapter describes the layout design of dual edge triggered flip-flops. The physical layout design has been made in standard UMC 0.18µm CMOS technology. Cadence Virtuoso layout editor tool is used for the layout design and DRC, LVS and RCX have been performed by using Cadence Assura. Design Rule Check (DRC) is performed in order to verify that layout full fill all electrical and geometric rules provided by foundry and finally, LVS (Layout VS Schematic) is performed on the layout design to provide equivalence between the layout and schematic. The basic design rules are summarized below:

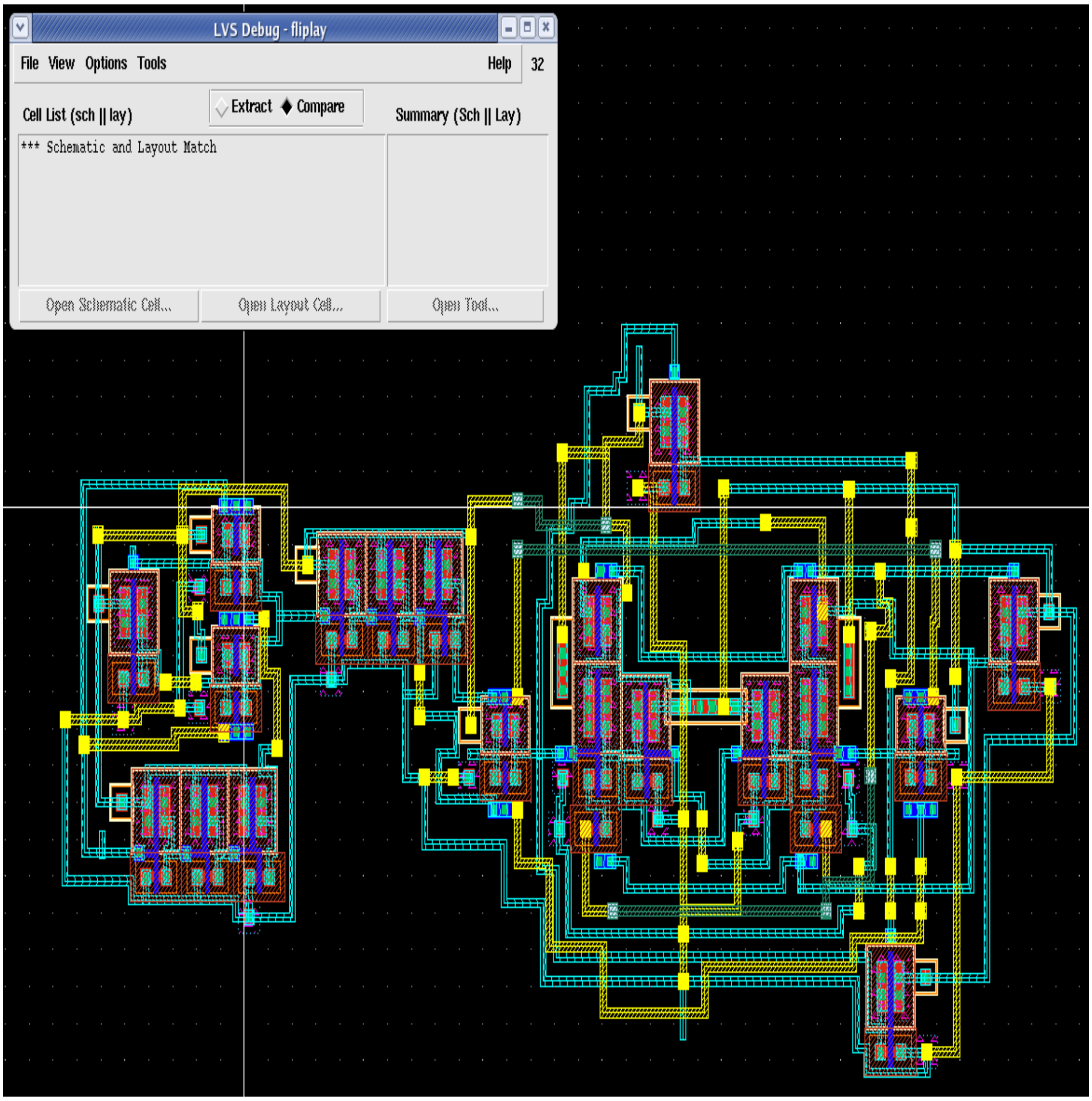
Metal 1 to metal 1 spacing	0.24 µm
Metal 2 to metal 2 Spacing	0.28 µm
Minimum contact size	0.24 µm*0.24 µm
Poly to poly spacing	0.24 µm
Poly to metal spacing	0.28/0.00 µm
Contact overlap to p+ diffusion	0.1 µm
Metal 1 width	0.24 µm
Metal 2 width	0 .28 µm
Metal 3 width	0.28 µm
Poly extension beyond active	0.22 µm
Minimum contact spacing	0.26 µm
N well overlap p+ diffusion	0.43 µm
Diffusion contact to poly spacing	0.15 µm
Minimum p+ implant overlap p+ diffusion	0.22 µm
Poly width	0.18 µm
Minimum poly extension on to field region	0.22 µm
Poly contact to diffusion edge spacing	0.18 µm
Minimum poly overlap contact	0.1 µm
Minimum metal area	0.1764 µm*µm
Minimum metal2 width	0.28 µm
Metal1 and metal2 overlap over via	0.08 µm
Minimum equal potential N-well spacing	0 µm or >=0.9 µm

Minimum non equal potential 1.8 V N well spacing 2µm

Rest of the the chapter discuss about the layout, RCX extrction and post layout simulations of pulse triggered dual edge flip flop in section 4.2 and of masterslave dual edge triggered flip flop in section 4.3.

4.2 **Layout of pulse static dual edge triggered flip-flop**

Figure 4.2(a) shows the layout of proposed pulse static dual edge flip-flop with V_{sb} effect (20 transistors). In this layout blue color shows the metal 1, yellow color shows metal 2, yellow box shows contact of metal 1 and metal 2. Violet color shows poly.



```
*** Schematic and Layout Match
```

Fig. 4.2(a) Layout of pulse static dual edge triggered flip-flop.

Layout and schematic are successfully matched. After matching layout versus schematic RCX extraction of the layout is done. This includes the resistance and capacitances in the post layout simulations. Figure 4.2(b) shows RCX extraction of pulse static dual edge triggered flip-flop with back gating effect.

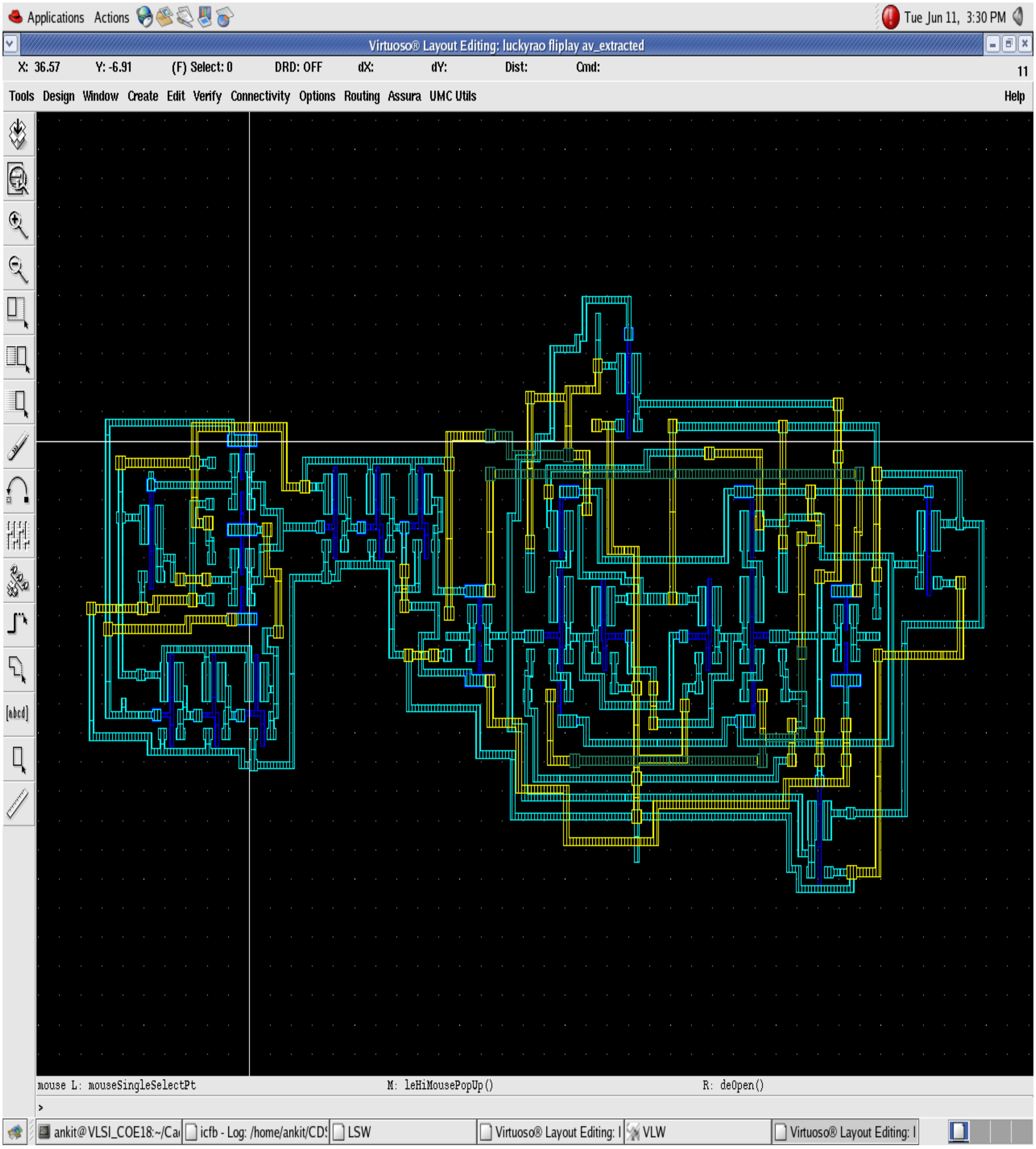


Fig. 4.2(b) RCX extraction of pulse static flip-flop.

After running RCX successfully again the simulation of schematic is done. This time simulation is carried out with extracted view. Results after simulation are depicted in Fig. 4.2(c). Simulation results of proposed flip-flop after extraction are slight different but these changes cause great change in power dissipation and propagation delay.

Fig. 4.2(c) Simulation of pulse static flip-flop after extraction.

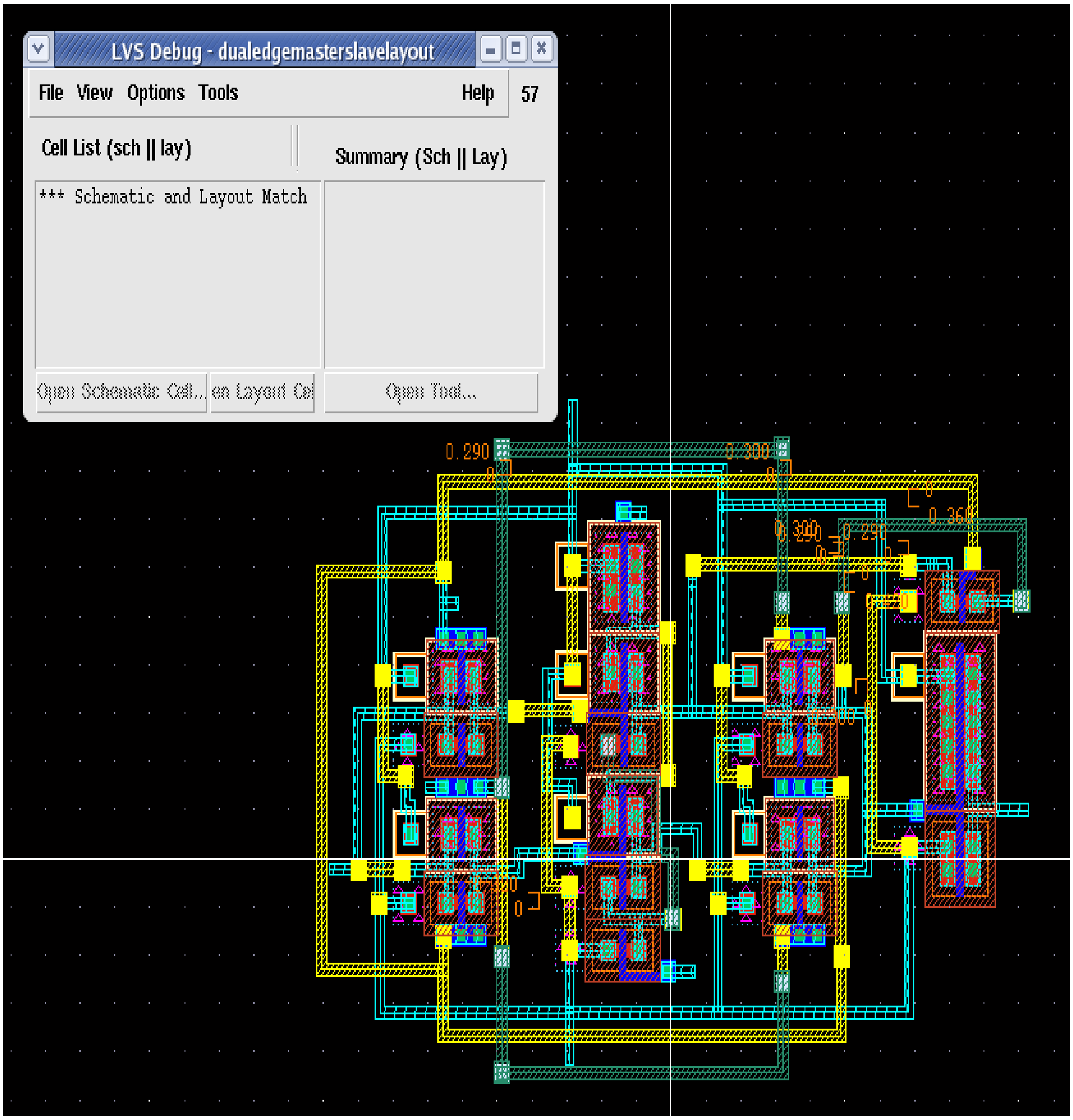
Table 4.2 shows the power and delay estimation of proposed pulse static dual edge triggered flip-flop after extraction. Difference in power is 0.58 mW and in propagation delay is 0.88 ns on comparing before and after extraction result at 1.8V supply voltage. Difference in power is 0.08825 mW and in delay is 1.234 ns at 0.9V supply voltage.

Table 4.2 Power and delay after extraction of pulse static flip-flop.

Supply voltage	Propagation delay (clk-q) of proposed pulse static flip-flop		Power dissipation of proposed pulse static flip-flop	
	pre layout	post layout	pre layout	post layout
(V)	(ns)	(ns)	(mW)	(mW)
1.8	6.21	7.09	2.02	2.6
0.9	7.315	8.549	0.427	0.51525

4.3 **Layout of dual edge triggered master slave flip flop**

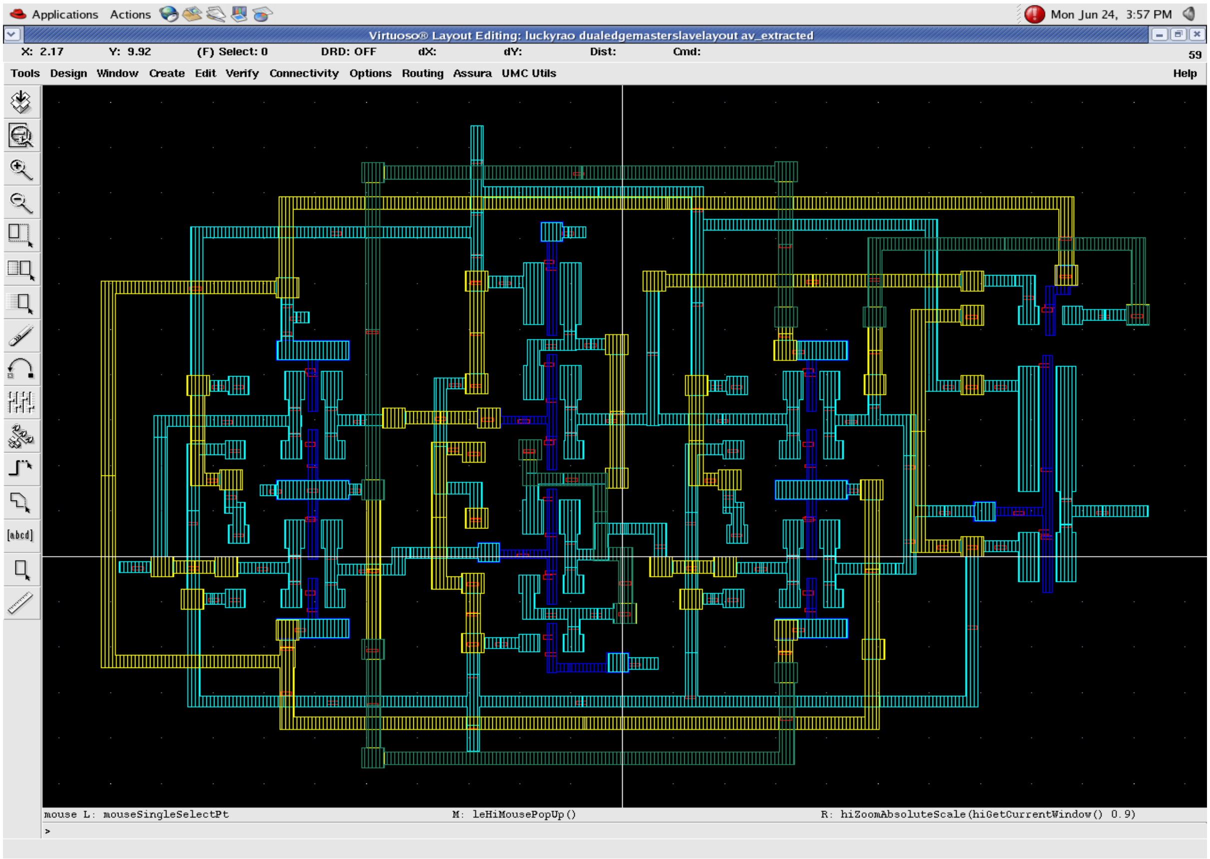
Figure 4.3(a) shows the layout of proposed dual edge triggered master slave flip-flop with power gating.



*** Schematic and Layout Match

Fig. 4.3(a) Layout of dual edge triggered master salve flip-flop.

The layout and schematic are matched successfully after that RCX extraction is done which is shown in Fig. 4.3 (b). Simulation results are shown in Fig. 4.3(b).



```
mouse L: mouseSingleSelectPt          M: leHiMousePopUp()          R: hiZoomAbsoluteScale(hiGetCurrentWindow() 0.9)
>
```

Fig. 4.3(b) RCX extraction of dual edge master slave flip-flop.

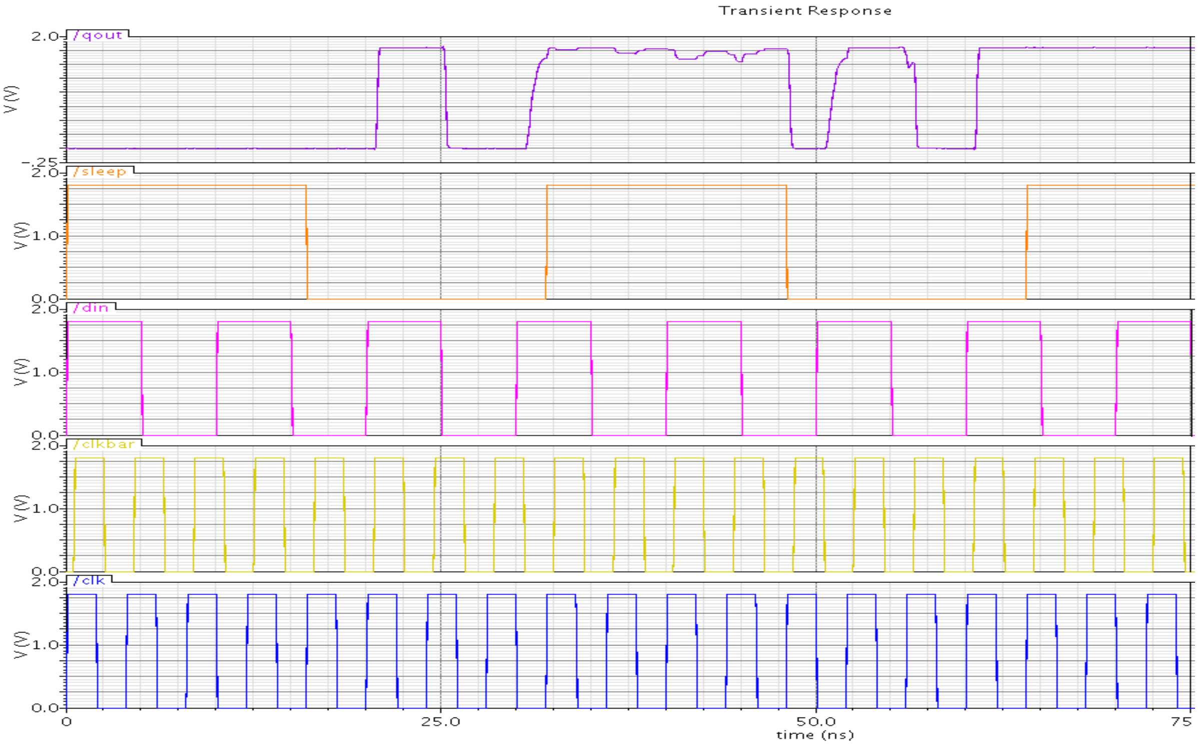


Fig. 4.3(c) Simulation of dual edge master slave flip-flop after extraction.

Table 4.3 shows the power and propagation delay values for proposed dual edge triggered master salve flip-flop after extraction.

Table 4.3 Power and delay of dual edge master slave flip-flop after extraction.

Supply voltage (V)	Propagation delay (ns)		Power dissipation (µW)	
	pre layout	post layout	pre layout	post layout
1.8	5.17	5.99	462.15	951.3
1.6	5.19	6.038	295.9	544
1.4	5.242	6.1135	189	297.4
1.2	5.3235	6.2825	125	140.4
1	5.4965	6.634	79.5	67.62

The differences in power dissipation for pre layout and post layout simulations are 489.15 µW, 248.1 µW, 108.4 µW, 15.4 µW at supply voltages 1.8V, 1.6V, 1.4V and 1.2V respectively. At 1V power is very less for post layout simulation results in comparison to pre layout results. Propagation delay of proposed flip-flop increased after post layout from 5.99 ns to 6.634 ns as supply voltage reduces from 1.8 V to 1V.

Chapter 5 Conclusion and future scope

In the present work the power gating technique and V_{sb} effect technique has been applied to single and dual edge triggered master salve flip-flops, single and dual edge triggered TSPC based flip-flops and pulse static dual edge triggered flip-flops with or without back gate effect. Simulations are carried out at 180 nanometer technology. Power gating method has proved very effective in reducing power at a cost of certain delay.

Table 5 shows the power and propagation delay of proposed flip-flops as they appeared in the work for 1.8V supply voltage. Less power is achieved at cost of delay. The number of transistors used in the flip-flop is shown in Table 5. Master slave dual edge triggered flip-flop with power gating has better results than other proposed flip-flops in the work. Power dissipation of proposed master slave dual edge triggered flip-flop is 462.15 μW at a cost of 5.17 ns propagation delay. A novel dual edge TSPC flip-flop has better results at low supply voltages.

Table 5 Power and delay of proposed flip-flops at supply voltage 1.8V

Proposed flip-flop structure with power gating technique	Propagation delay (nW)	Power dissipation (μW)	Number of transistors
Rising edge triggered master slave flip-flop	9.12	378	24
Positive edge triggered TSPC based flip-flop	7.2105	272.125	13
Pulse static dual edge flip-flop with V_{sb} effect	6.21	2020	20
Pulse static dual edge triggered flip-flop without V_{sb} effect	6.496	1900	18
Pulse static dual edge triggered flip-flop with V_{sb} effect	6.496	1600	18
Dual edge triggered master slave flip-flop	5.17	462.15	17
Dual edge triggered TSPC flip-flop	4.1853	1460	24

Power can be further reduced by using adiabatic logic which utilizes pulse as a supply voltage instead of constant supply. Dynamic families can also be integrated at ease with TSPC flip flops in order to improve the speed of device. Pipelining can also be used in flip-flops which also enhance the speed of circuit.

References

[1] C. Kim and S.-M. Kang, "A low-swing clock double-edge triggered flip-flop," *IEEE J. Solid-State Circuits,* vol. 37, pp.648-652, May 2002.

[2] Chiou, L.-Y, and Luo, S.-C., "Energy-efficient dual-edge-triggered level converting flip-flops with symmetry in setup times and insensitivity to output parasitic," *IEEETrans. on VLSI,* vol-l7, no.11, pp. l659-1663, Nov. 2009.

[3] Fatemeh Aezinia, Sara Najafzadeh, and Ali Afzali-Kusha,"Novel high speed and low power single and double edge-triggered flip-flops", *IEEE International Asia Pacific Conference on Circuit and Systems,* December 2006.

[4] http://en.wikipedia.org/wiki/Flip-flop_(electronics).

[5] Jan M. Rabaye,Anantha Chandrakasan and Borivojie Nikolic, "Digital integrated circuits", Charles G. Sodini, second impression, 2008.

[6] Karimiyan, H.; Sayedi, S.M.; Saidi, H., "Low-power dual-edge triggered state-retention scan flip-flop ", *IET,* pp. 410 – 419, 2010.

[7] M. Pedram, Q. Wu, and X. Wu, "A new design of double edge-triggered flip-flops" in Proc. *Asia and South Pacific Design automation conference (ASPDAC),* pp. 417-421, 1998.

[8] R. Hossain, L. D. Wronski, and A. Albicki, "Low power design using double edge triggered flip-flops", *IEEE Trans. on VLSI Systems,* vol.2, no. 2, pp.261-265, June 1994.

[9] Sandeep Sriram, Arun Ramnath Ramani, Haiqing Nan,Hojoon Lee, Ken Choi, " A novel dual edge triggered near-threshold state retentive latch design",*IEEE 54^{t}International Midwest Symposium on Circuits and Systems*, August 2011.

[10] Sandeep Sriram, Haiqing Nan, Ken Choi, "Low power latch design in near sub-threshold to improve reliability for soft error", *IEEE International Symposium on Quality Electronic Design*, March 2011.

[11] Satish Chandra Tiwari, Kunwar Singh and Maneesha Gupta, "A low power high density double edge triggered flip-flop for low voltage systems ", *IEEE International conference on Advances in Recent Technology in Communication and Computing,* October 2010.

[12] Sung Mo Kang and Yusuf Leblebici, "CMOS digital integrated circuit", Tata McGraw-hill. 21st reprint 2008.

[13] T.A. Johnson, I.S. Kourtev, "A single latch, high speed double-edge triggered flip-flop,"*IEEE International Conference on Electronics, Circuits and Systems*, vol.1 pp. 189-192, 2001.

[14] Yu Chien-Cheng, “Low-power double edge-triggered flip-flop circuit design”, *IEEE International Conference on Innovative Computing and Information Control*, June2008.

[15] Yu-Yin Sung and Robert C. Chang, “A novel CMOS double-edge triggered flip-flop for low-power applications”, *IEEE International Symposium on Circuits and systems,* vol-2, May 2004.