RADIATION HARDENED FLIP FLOP DESIGN

A Thesis submitted in fulfillment of the requirement for the Award of the Degree of

MASTER OF TECHNOLOGY

In VLSI Design

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TO WHOMSOEVER IT MAY CONCERN

This is to certify that **Arushi** has undergone internship in our **Technology & Design Platform** Group from **June 11, 2018 to June 05, 2019**. She has successfully completed her project on: **Radiation Hardened Flip Flop Design.**

During her internship period, she was found to be sincere and professional in her conduct.

We wish her all the best in her future endeavours.

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Parminder Singh WALIA
Group Manager - HR

DECLARATION

I, Arushi hereby declare that the work presented in this thesis **"Radiation Hardened Flip Flop Design"** in the fulfillment of the degree of Master of Technology (VLSI DESIGN) submitted at Electronics and Communication Engineering Department, Thapar Institute of Engineering and Technology (Deemed to be University), Patiala has been carried out under the supervision of Ms. Madhu Kushwaha (Lecturer, Electronics and Communication Engineering Department, TIET, Patiala) from August 2018 to July 2019. The matter presented in this is authentic and have not been submitted to any university for the award of any degree.

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ABSTRACT

Device scaling has become an important part of very large scale integration (VLSI) design that can result in faster and denser integration of devices. Increased speed of data transfer, ability to achieve multiple tasks simultaneously and better performance are some of the main advantages of scaling. Subthreshold leakage, dynamic power dissipation and short channel effects are some of the reasons predicted as the disadvantages of transistor scaling.

Density of memory elements also keeps on increasing which leads to increased susceptibility of the device nodes toward the radiation. Thus, increasing susceptibility of the device nodes is an add on drawback to scaling of technology node. Earlier, radiation had a prominent effect on integrated ICs in aerospace applications only but due to continuous scaling, it has become a serious hazard at ground level also.

In digital electronics, flip flop is the basic sequential circuit which is used to store the state information. Under the influence of radiation, performance of CMOS flip flop circuits get disturbed. Power dissipation, robustness and propagation delay are some of the parameters which are considered while designing a RADHARD flip flop.

This thesis work contains the analysis of radiation induced soft errors on 90nm technology node CMOS circuits. It targets to design low power flip flop along with sufficient immunity towards the radiation.

Several state-of-the-art designs like DICE, TMR and Single Phase Clocked Design have been implemented. Virtuoso (Cadence) tool has been used to design the structures of flip flops with 1.2V as the supply voltage. An algorithm has been proposed to find out the MOSFETs in cut off region and to remove redundant nodes. It checks the output state of flip flop to observe the effect of radiation strike on it. This algorithm is well implemented on the RADHARD structures along with the proposed design. Analysis has been done on these RADHARD structures on the basis of delay, power and critical charge.

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CHAPTER 1

INTRODUCTION

1.1 BACKGROUND

Radiation is an emission of energy from space or via a medium of material in the form of radio waves, microwaves, X-rays, gamma rays, ultraviolet rays. The word ‘radiation’ is derived from an event of radiating waves from a source (possibly travelling in all directions). These radiations can be ionizing or non-ionizing in nature based on their related energies.

Radioactive materials are a typical source of ionizing radiation responsible for emitting alpha, beta and gamma particles. Two other sources whose radiations enter the atmosphere of earth are sun and space. The particles from space have very high energies but are less frequent in nature.

In case of non ionizing radiation, energy of particle is very small to generate charged ions passing through a medium. The particles in non-ionizing radiation have a potential to cause thermal ionization if enough heat is transmitted so that temperature is raised to ionize energies.

The energy emitted through radiation is encountered on a regular basis, but in such low quantity that its effects are not taken care off. In highly radiation prone environments such as in space, the energized particles that are neglected in daily life have a significant impact on the performance of electronics.

1.2 OVERVIEW OF RADIATION ON SEMICONDUCTOR DEVICES

Radiation can cause damage in electronic circuits that lead to their improper functioning. The semiconductor materials used in electronics are damaged by virtue of which the lifetime of the devices is reduced to a great extent. For instance, solar panels in spacecrafts, after continuous exposure towards radiation become less promising in efficiency.

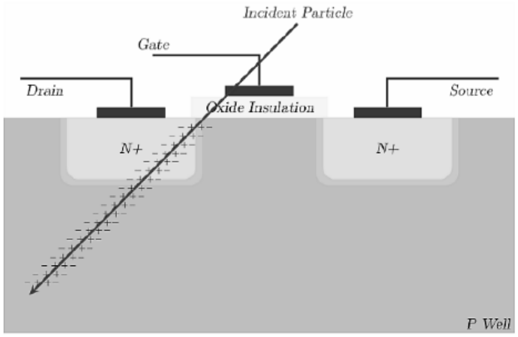

Figure 1.1: Radiation strike on MOSFET [1]

Onset of radiation causes energy transfer from the ionizing particle to the material per unit distance. It is called as the radiation action to material. If energy is deposited in higher concentrations, it can cause severe damage to microelectronics. The radiation had been a vast area of research for the effect of radiation on MOSFET for about two decades.

When an ionizing radiation strikes on MOSFET (Figure 1.1) electron-hole pairs are generated disturbing the device performance. Thus, in order to reduce the impact of radiation on semiconductor devices, radiation hardening is required which is discussed in detail in section 1.3.

1.2.1 Sources of Radiation

The sources of radiation which can create a problem in building reliable circuits at aerospace are Solar flares, Cosmic ray particles, trapped radiation and proton belt. Cosmic rays undergo collisions with earth's atmosphere which result in generation of secondary particles at ground level as well. Figure 1.2 shows the presence of different particles with different energy levels at different altitudes.

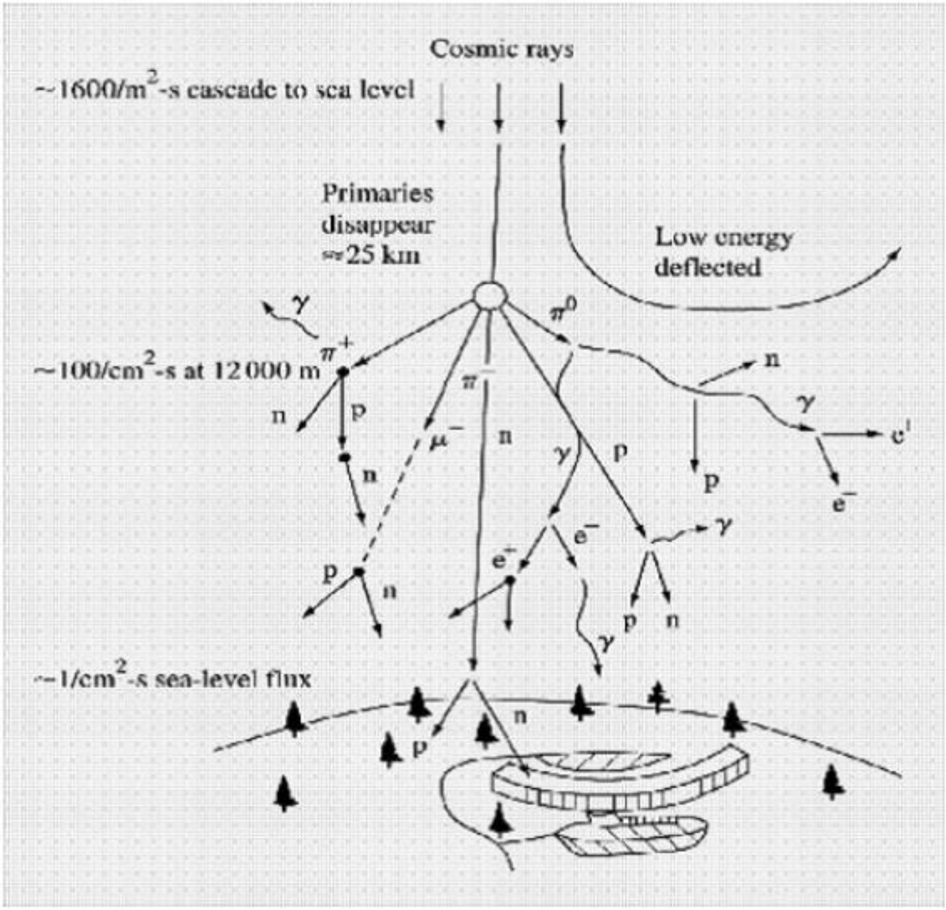

Figure 1.2: View of cosmic rays showing cascade of particles [1]

The radiation contributors in semiconductor devices are

1. Radioactive material present in the packaging material

Uranium and thorium, radioactive impurities in packaging material emit energy through alpha particles while decaying through lower energy states [2]. They have kinetic energy from 4 to 9 MeV. There are many radioactive isotopes, however, Uranium and Thorium have the highest activity among the other naturally occurring materials. Alpha particles emitted from these isotopes are the major sources of SEs.

2. Highly energized cosmic ray particles

Neutrons (>1 MeV) emitting from cosmic radiations can cause soft errors in semiconductor devices via semiconductor ions produced by neutron reaction with silicon nuclei at terrestrial level [2].

3. Low energy neutrons

Cosmic neutrons interact with the isotope boron-10 (commonly used as p-type dopant for junction formation in IC package) which results in the secondary radiation being the significant source of ionizing particles in electronic devices. This interaction releases Li nucleus with energy 1MeV, alpha particle of 1.4 MeV energy and gamma photon with around 400KeV energy. Figure 1.3 shows the interaction of cosmic ray neutron and boron.

1.2.2 Single Event Effect mechanism

1.2.2.1 Collision with high energy particle

Collision of highly energized particle leads to charge generation in the semiconductor devices. This is possible due to two of the reasons mentioned below.

a) Direct ionization:

It leads to electron hole pair generation due to a heavy ion hit. An ion is considered to be heavy if its atomic number is greater than or equal to two. The ion releases electron hole pairs as it travels in semiconductor device and loses energy in the same process. The energy lost per unit length is called Linear Energy Transfer (LET) and the length of the particle travelled by particle is called Range.

b) Indirect ionization:

It is the result of the nuclear reaction between a struck particle and an energetic particle, resulting in ionization by secondary particles. The energetic particle, here, refers to the protons or neutrons which can produce significant upset rates by undergoing elastic collisions with a target nucleus [1].

1.2.2.2 Charge Generation and Collection

Charged carriers which are generated due to high energy particle strike move according to electric field (applied or built-in) and doping of the substrate. Charge generated at the reverse bias junction leads to major charge generation and collection due to drift process. The high electric field present at the reverse bias junction is the reason of free charge carriers formed which results in the transient current pulse formed at the contact. Drift time period is affected by the saturation velocity of charge carriers. Therefore, it is very small. In case of silicon, saturation velocity is 1x107 cm/sec [1]. The three main steps for charge collection and transportation is shown in Figure 1.3.

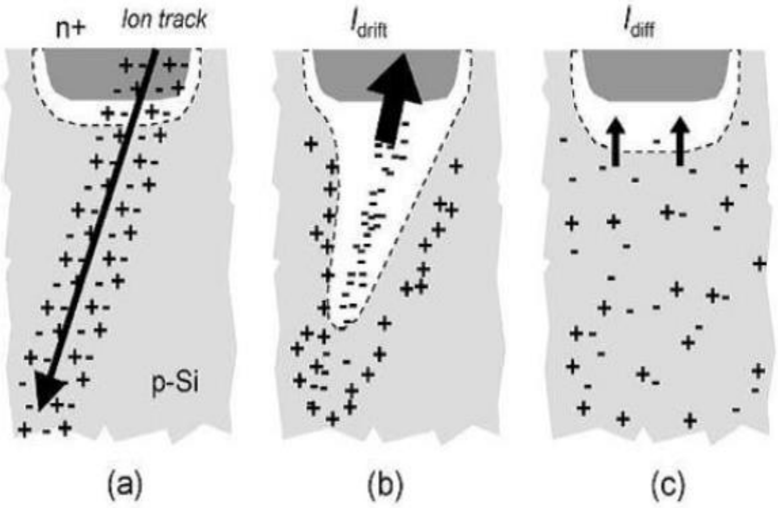

Figure 1.3: Mechanism of charge collection and flow [3]

The drift process causes disturbance of junction electrostatic potential which leads to Field Funneling Collection process. In this process, the high field is extended in the shape of funnel due to the connection of deposited charge with depletion region. As a result, charges that are present outside the depletion region are also pushed towards the depletion junction contacts due to which more charge is being accumulated resulting in voltage level flip at the node. This process is further followed by diffusion. It is a slow process and takes more time as compared to the drift process.

The consequences of these steps lead to transient pulse generation at the device terminal. The time span for the initial spike in the current pulse is short lived. The rising transient in this pulse is due to the Drift process. The shape of the current pulse is expressed using I = dQ/dt (where I is current, Q is the charge and t is the time). The behavior of the current pulse is shown in Figure 1.4. This double exponential current pulse has a rise time of about tens of picoseconds and fall time of hundreds of picoseconds. It can be modeled using the equation 1.1

$$I_{\mathrm{p}} = I_{\mathrm{o}}(e^{\text{-t}/\mathrm{T_f}} - e^{\text{-t}/\mathrm{T_r}})$$

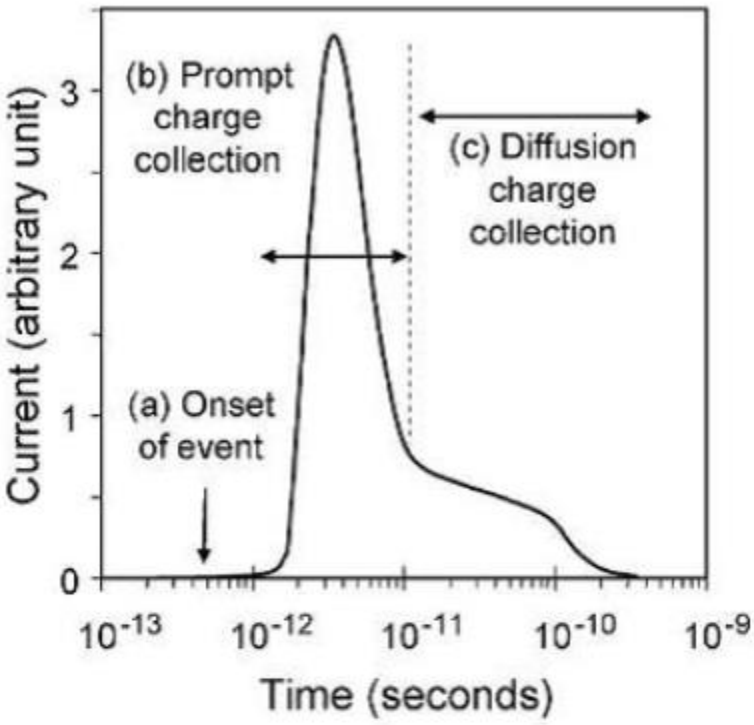

Figure 1.4: Double Exponential Current Pulse [3]

In equation 1.1, Ip is the transient current pulse, Io is the peak current, Tr is the rise time of the current pulse, Tf is the delay time for the current pulse. Critical charge at the particular node can be calculated using the equation 1.2

$$Q_{\mathrm{CRIT}} = \int_0^{\mathrm{T_{PERIOD}}} I(t)dt \tag{1.2}$$

1.3 ISSUES RELATED TO RADIATION STRIKES

SEE are the disturbances caused in an electronic device due to radiation strike (single particle) which can take any form. Single event phenomenon is classified into three forms as shown in Figure 1.2.

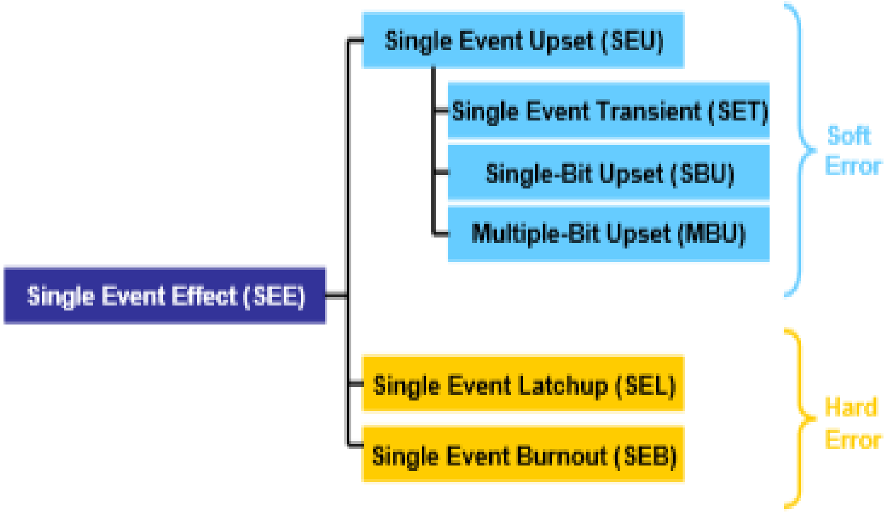

Figure 1.5: Classification of Single Event Effects [2]

1.3.1 Soft Errors

SEU arises in microelectronic circuits when charged particles lose energy by ionizing the medium (semiconductor)leaving behind electron-hole pairs. SET is a voltage disturbance produced when a cosmic particle falls on the combinational logic circuit which can propagate through the logic.

SBU refers to flipping of one bit of data due to single radiation particle. MBU is a soft error in which a single ion hits more than one bits causing simultaneously occurring errors.

1.3.2 Hard Errors

SEL is a hard error that causes loss in device functionality because of single event induced state current. It can result to permanent device damage due to high operating current above the specification of device. SEB can cause device destruction due to a high current state in a power transistor. It includes burnout of power MOSFETs, gate rupture etc.

This piece of work concentrates only on soft errors as hard errors are permanent in nature and thus, beyond our interests.

1.4 SINGLE EVENT UPSET (SEU)

Onset of radiation on a device causes soft errors (SEU) in the form of glitches which generate charge accumulation at the node of the semiconductor device. This accumulation is due to hitting of the charged particles at a particular node. These charged particles are the particles which are generated due to cosmic rays, some are the results of activities going on in the space and some are the results of the decaying of radioactive material present in the packaging of the semiconductor devices like Thorium and Uranium.

As the size of devices shrinks, nodal capacitance values of transistors and the value of operating voltage of circuits decrease in a very fair amount becoming more prone to radiation. Every node in a circuit accumulates a specific charge. Once this accumulated charge increases from the value of critical charge, which is the maximum limit of charge below which the data is safe, the saved data on that node is flipped under the effect of the charge strike. If Qcritical is the critical charge of the node and Qaccumulation is the charge accumulated, then,

Qaccumulation > Qcritical (data at the node flipped)
Qaccumulation < Qcritical (data at the node is safe)
Here, critical charge can be given as,

$$Q_{critical} = C_{nodal} * V_{supply} \quad (1.1)$$

Where,
Qcritical = Critical charge
Cnodal = Nodal capacitance
Vsupply = Supply voltage

As the data stored at a particular node is corrupted due to radiation strike, radiation hardening is developed to enhance the device performance.

1.5 NEED OF RADIATION HARDENING

Radiation hardening is a process of making electronic circuits capable of resisting damages or malfunctions due to ionizing radiation. A single charged particle has the ability to knock out thousand of electrons causing signal spikes. Thus, in case of digital designs, results can be inaccurate. It is a serious issue in spacecrafts, satellites, military aircrafts etc. In order to achieve proper functioning of these systems manufacturers of integrated circuits adopt various methods of radiation hardening discussed in section 1.3. Such systems are called as rad(iation)-hardened, rad-hard or hardened systems.

1.5.1 Applications of Radiation Hardened devices

Research on radiation hardening has increased on a rapid rate over the past few years. The research is strongly influenced by the demand of radiation hardened devices for various applications. These applications include

1. Medical: The electronics designed for medical industry are invented along with the aim of

low power consumption maintaining the standard of reliability. For example, a fault affecting the device performance involved in surgery can cause threat to patient’s life. Therefore, great effort is made to design a reliable product.

2. Aerospace and Defense: Aerospace and Defense is depended heavily on systems such as communication satellites. An interruption in service of these systems can cause failure of the mission or national security.

3. Automotives: The electronic devices and systems are equipped with automated features like airbags in cars. Due to technology scaling, such systems are prone to radiation strike.

1.5.2 Merits of radiation hardening

Although, the tasks associated with hardening by design are broadcast and diverse, they include the combination of following.

1. Single Event Upset (SEU)- tolerant electronics: These electronics play a vital role for designing of radiation immune and efficient memory devices, logic and arithmetic elements.

2. High performance processors: These processors are used for higher throughput (million of instructions per second) and processing efficiency.

3. Low temperature electronics: These electronics have been developed for longer planetary operations in night or shadowed conditions.

1.6 WAYS TO ACHIEVE RADIATION HARDENING

Radiation hardness can be achieved via two ways. It can be obtained by suitably modifying the fabrication process (“Radiation Hardening by Process” - RHBP) or by designing electronic circuits to achieve tolerance to radiation (“Radiation Hardening by Design” - RHBD). However, RHBP is a much complex and costly method to achieve radiation immunity. RHBD can be classified as follows:

1.6.1 RHBD at system level

At system level, radiation hardness may be achieved in the form of software algorithms that are capable of extracting correct data from redundant information. At this level, it is compulsory to design redundant electronic systems.

1.6.2 RHBD at architectural level

At architectural level, Error Correcting Code (ECC) circuitry is added to increase the correcting capability of electronic devices. Furthermore, placement strategies can be adopted to lessen the radiation effects.

1.6.3 RHBD at circuit level

At circuit level, structures are designed using several design techniques. These techniques are adopted to lessen the effect of radiation on the circuit like redundancy.

1.6.4 RHBD at layout level

During the design of the layout, several solutions are adopted to eliminate the damaging radiation effects: physical separation, guard rings, etc.

1.7 RADIATION HARDENING IN SEQUENTIAL CIRCUITS (FLIP FLOPS)

SEU is defined as the flipping of the data bit due to the radiation strike. The rate at which SEUs occur is defined as SER (Soft error rate), measured as FIT (Failures in time), representing failures per million device operation hours. Traditionally, SER was focused mainly on SRAM and DRAM but literatures investigated that the effect of soft errors on logic components became equally important. Later on, logic elements like flip flop and latches (hold event signals and buffer data before going in or out of the chip) are taken into consideration. Latching of transient error induced due to radiation by these sequential elements became the foremost reason for the development of their radiation hardening. Thus, the largest contributors of soft errors were found out to be memory elements within the sequential logic [1]. This increases the need to suppress the effect of soft errors in sequential elements. Therefore, researchers are more inclined towards proposing new hardening approaches for flip flop and latches.

Basic flip flop circuits which are part of this piece of work are Dual interlocked cell, Triple Modular Redundancy and Single phase clocked design. The functioning of these flip flops are based on D flip flop, basic memory cell. These designs use design techniques to reduce the vulnerability towards the radiation. Feedback, redundancy and the use of voter circuit are some of the ways which can be used to design robust flip flop designs. The utilization of C-element is also incorporated to combat effect of radiation at the output and recover the correct data.

Flip flops, important components in the sequential circuits, are becoming more prone to soft errors. Therefore, flip flop hardening has become an essential requirement.

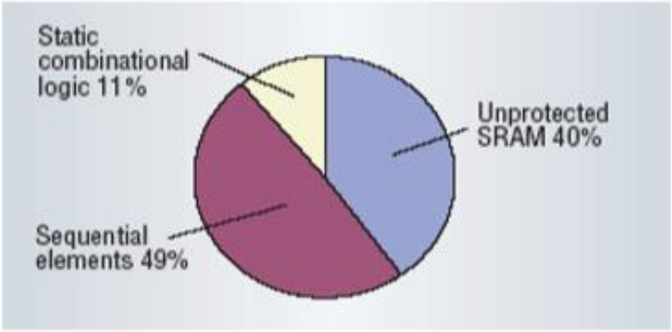

Figure 1.6: Contributors to the overall SER for the design manufactured using state-of-the-art technology [2].

1.7.1. DICE (Dual Interlocked cell)

The D flip flops which are designed on the basis of DICE latch are capable of restoring the original state, when a radiation strikes on a particular node. Data in DICE is stored as a pair of complementary values on A, B, C, D as shown in Figure 1.4.

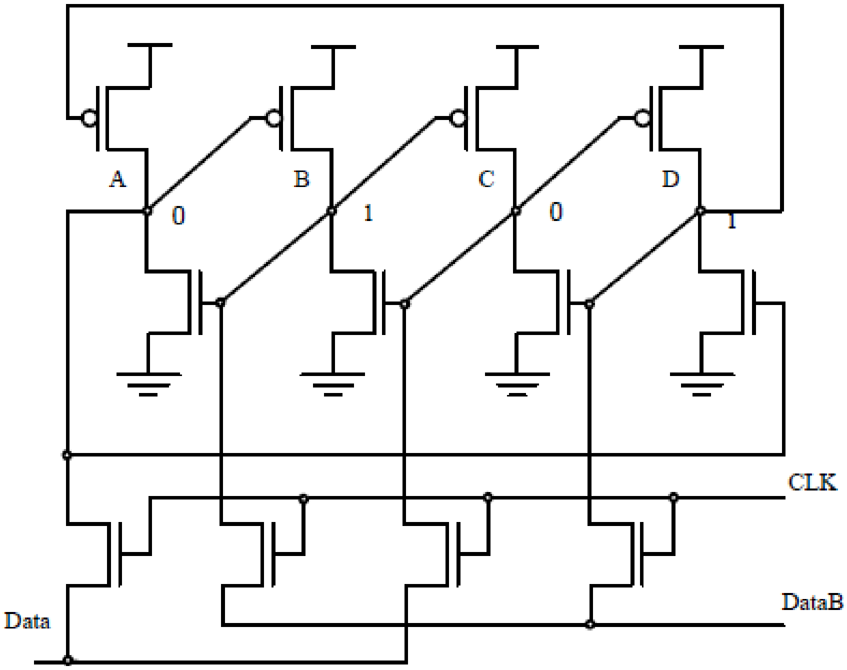

Figure 1.7: DICE storage cell [4]

Its working is explained as follows. When CLK is kept at VDD and D is also at VDD, then, A=0 B=VDD C= 0 and D= VDD. Suppose, the radiation strikes at any node then due to redundancy data can be restored as shown in the following example.

Suppose, event occurs at the node B by virtue of which value stored at the node B changes from VDD to 0. Now, P0 turns on and N2 will be in OFF state, as the N0 transistor was already in ON state, there will be a direct path from P0 and N0 from VDD to GND, hence node A will remain at 0 potential. If A is at GND value then N1 is in off state and therefore, P3 is ON, P1 is already in on state. Thus, B will be recharged up to VDD value and the value of B is restored.

1.7.2 SPCD (Single Phased Clocked Design)

A single phase clocked structure is introduced which shows robustness against SEUs. This flip flop contains an input stage having a clock (single phase) to the storing unit using positive edge of the clock. The storage unit has DICE. The two nodes in the storage unit with same logic are passed from a C-element to the output node. This C-element helps to mask the SET pulse to propagate to the output. This flip flop is used in SOCs and microprocessors.

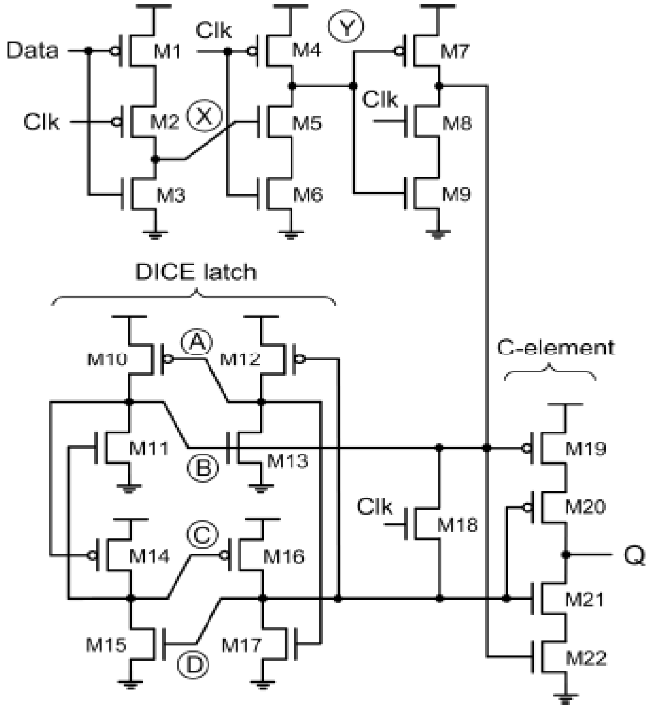

Figure 1.8: SPCD-DICE flip flop [5]

The operation of this design can be explained as follows. When CLK is at logic 0, node Y is at logic 1 and node X is pre-charged at complement of data. Also, M7 and M8 are in off mode. Writing of data is done in two ways being CLK at logic high. When CLK is at logic 1 and data is also at logic 1, node Y comes at logic 1 and node X is at logic 0. It turns on the transistor M18 and pulls down B. Node D pulls down due to the low impedance path which passes through M18. Values of node A and C are changed from logic 0 to logic 1. Output node is at logic 1 same as the input data as node B and D are both at logic 0. Otherwise, if the data is at logic 0 and CLK is at logic 1, node X will be at logic 1 and logic Y will be pulled down to 0. Thus, node is at logic 1 by M18 and M16 transistors updating A and C nodes. M18 and M7 are kept large enough to overpower M17. Also, M15 and M13 are made smaller. It was found that the SPCD has less power consumption as compared to DICE flip flop.

1.7.3 TMR (Triple Modular Redundancy)

A new radiation hardened scheme is investigated for harsh radiation environments. In this type of circuit, main system is replicated three times and the output is forced to be passed from a majority voter. The voter plays a pivotal role that the erroneous value cannot be propagated to the output of the system. It ensures that the system is operated correctly even in the presence of a radiation event. However, replicating the system three times increases the delay and power dissipation as well.

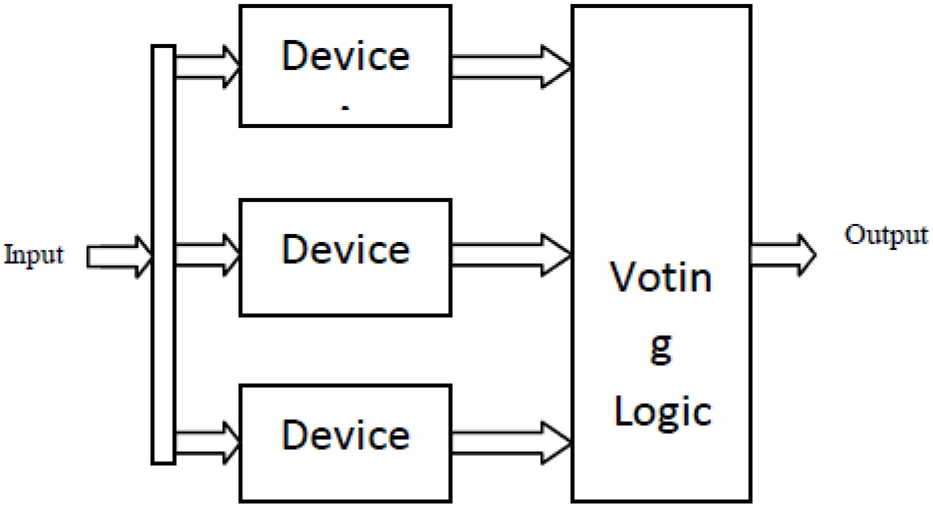

Figure 1.9: Block diagram of TMR [6]

1.7 OBJECTIVE OF THESIS

M.Haghi designed a DICE latch in order to recover the correct value following the DICE, TMR and SPCD structures. Moving towards nanometer technologies, these structures goes on becoming more and more affected by the radiation strike. Thus, there is a great need to find the sensitive nodes in a circuit and the effect of radiation on them to find the circuit's immunity. The objective of the thesis is as follows:

1. Analysis of double exponential current pulse to be modeled as a radiation strike on the node of the circuit.

2. Propose an algorithm to find the sensitive nodes in a circuit, effect of radiation on them and critical charge.

3. Performance analysis of DICE (Dual interlocked cell), TMR (Triple Modular Redundancy), SPCD (Single phased clocked design) structures in terms of power, delay and critical charge using the proposed algorithm.

4. Propose an efficient circuit in terms of power and critical charge and its performance comparison with the existing structures.

1.8 OUTLINE OF THESIS

Chapter 1 gives the introduction to radiation induced soft errors, need to study radiation hardening, various approaches investigated to combat the effect of radiation, need to design radiation hardened flip flop designs, motivation of thesis along with its outline.

Chapter 2 includes an overview of literature survey which contains all the researches done till now associated with radiation hardening in chronological order starting from 2003. It contains design approaches implemented at circuit level to make the designs robust.

Chapter 3 includes the analysis and modeling of double exponential current pulse for radiation strike. An algorithm has been proposed to detect the MOSFETs in cutoff region and to remove redundant nodes. It checks the output state of flip flop to observe the effect of radiation strike on it.

Chapter 4 gives the implementations and simulations of the basic RADHARD structures. All these designs are implemented on 90nm CMOS technology. All these designs are made using an assumption that a single particle strike can lead to collection of charge on single node of the circuit.

Chapter 5 gives the proposed designs and a comparative study among the implemented structures and the proposed designs on the basis of power, delay and critical charge.

Chapter 6 gives the conclusion of the work implemented and studied and the future work associated with the same.

CHAPTER 2

LITERATURE SURVEY

Earlier, radiation hardening used to be prominent on space and nuclear applications only. Continuous increase in packaging densities have led researchers to innovate as many robust designs as possible. In-depth research has been done on the factors responsible for SEUs, ways to combat them, techniques for designing radiation immune circuits. Sequential logic elements, being the largest contributors of SEs are extensively discussed since 1990 and are the most trending topic in the field of radiation hardening. This section deals with the brief overview over the background and robust designs discussed till now in chronological manner.

In 1978, T.C. May *et al.*, found that the ionization caused due to cosmic rays is a cause of bit errors in satellites. Susceptibility to errors caused due to cosmic rays results in a small charge to represent the data bit. Small amount of energy deposition causes discharge of storage node which results in a bit error. MOS semiconductor memories which are used to store small amount of charge for the bit information can be sensitive to error by discharge from cosmic rays. Ionization caused by cosmic rays in an individual memory cell results in the error for the entire memory systems using large number of memory systems. Bit error can be reduced that can maximize the storage of data and minimization of the volume can be done [7]

In 1978, J.C. Pickel *et al.*, studied the sources of radiation which can create a problem in building a reliable circuit at aerospace are Solar flares, Cosmic ray particles, trapped radiation and proton belt. The authors extended the analytical methods so that the soft error rates due to the cosmic rays can be predicted in the memory devices. The results were found that the memory cells sensitivity is related to the density of MOS technology, determining the node capacitance value. The result found is that bit errors in the memory devices are due to cosmic ray generated charge. RAM cell was found to be hard to cosmic rays due to large capacitance values and large voltage change requirement for the flipping of data [8].

In 1979, C. S. Guenzer *et al.,* studied the single event upset caused due to neutrons and protons. The solutions which they suggested here is to design less sensitive circuitries. Memory redundancy would likely to eliminate the problems caused due to Single event upset. Continuous reduction in speed power product can be directly correlated to the critical charge, therefore high performance devices are proved to be sensitive to the upset caused to the radiation strike. Single event upset whether from any source is a serious problem which is needed to be dealt in the generations to come of performance devices [9]

In 1979, T.C. May *et al.,* studied another factor responsible for the Single Event Upset in the memory devices. 16K RAMS were irradiated by the impact of neutrons. It is mad possible that the upset can be made reset again and the normal operation is continued again. The authors found that the dynamic RAMs are sensitive to upsets generated due to highly energized neutrons. Sensitivity decreases with decrease in the energy of neutrons but not to some extent. The dynamic RAMs which are tested were found to be more sensitive to protons as compared to neutrons as the energy related to these protons are in the range till hundreds of MeV. They also found that the semiconductor devices are becoming more prone to the upset caused due to the alpha upset problem [10].

In 1981, C.M. Hsieh *et al.,* studied the phenomenon of charge collection in silicon devices. Penetration of an alpha particle distorts the junction field in a semiconductor device drastically. The field extends to the bulk silicon and funnels the carriers into the junction. The field regains its normal position after a very few nanoseconds. Left out carriers are transported by the process of diffusion. The drift process causes disturbance of junction electrostatic potential which leads to Field Funneling Collection process.The funneling effect was well observed in the computer calculations. This effect was found to have very great impact on highly dense devices. They also concluded that the drift component plays an important role for the soft error rate [11].

In 1990, S.Whitaker *et al.,* a design was proposed for space station which hardens the CMOS circuits from Single Event Upset. A RAM was presented to signify the method. Design techniques without serious performance degradation have been presented. It has been observed that the RAM cell consists of feedback from the non corrupted node of stored data to recover the data loss. Thus, value is restored even after a particle strike. A basic D flip flop was also designed from RAM circuitry. Both the designs were developed to represent SEU immunity. D flip flop was used to implement the RAM cell. After the chip fabrication, the shift register designed will be sent to be tested for SEU immunity and results will then be submitted [12].

In 1995, P.E. Dodd *et al.,* studied the charge collection and SEU characteristics of SRAM which indicated that the computations of the charge collected should be taken into consideration. They discussed the need of model predictions of the linear energy transfer that can cause upset. The conclusion which came as the output is that the device simulation alone cannot predict the critical charge. For the soft error rate calculations, the critical charge and the depth of junction are needed. Critical charge and the linear energy transfer can be computed using mixed mode simulations. Therefore, the need of three dimensional simulations have been arised and thus, an insight has been presented which is used for the realization of the SEU hardened designs [13].

In 1996, P.E. Dodd *et al.,* investigated the impact of technology trends on SEU hardness of CMOS SRAMs. The author not only explored the upset mechanisms for various strike locations but also investigated their dependence on gate length scaling. An application based on 0.5um technology of CMOS radiation hardened design was presented. The authors concluded with the result that the mechanism of charge collection starts late reducing the effectiveness of the feedback resistors. They discussed the need of new hardening techniques needed in the CMOS technologies [14].

In 2000, M.P. Baze *et al.,* a new technique for SEU prevention has been investigated and demonstrated experimentally. The technique used isolated well transistors to prevent them from the transients in the combinational logic to propagate to the output. This technique hardens the transient errors for control as well as dynamic logic. This technique can be scaled such that it has it future perspectives in vulnerable submicron processes [15].

In 2001, S. Hareland *et al.,* observed that the node charge of circuit latches has resulted in an increasing SER for the logic components. They examined the SRAM technology and the charge collection physics whose results indicated that the SER is reducing on per bit basis in the future technologies. This has implications for the future based designs. As a result, due to the technology scaling, emerging trends from one generation to another that allows SER estimates to be made [16].

In 2002, Robert Baumann, examined the effect of radiation on electronic circuits in terrestrial environments with latest scaling trends for sequential logic and memory and future issues for product robustness. Figure 2.1 shows that system SER kept on increasing with the technology node except for 0.18um where BPSG is reduced resulting in lowering of SER baseline. BPSG (Borophosphosilicate) has been disrupted to reduce the soft errors induced by 10B activation due to radiation. Three mechanisms are found to be responsible for the errors at the terrestrial levels i.e. highly energized neutrons, alpha particles from the radioactive impurities. It is concluded that the failure rate for the sequential logic is very high even if there is saturation after the 0.13um technology [17].

In 2003, P.E. Dodd *et al.,* investigated the physical mechanisms which are responsible for SEE in microelectronics. The effect of trends in technology on single event susceptibility is explored. Non destructive Single Event Effects are the result of charge deposited by direct ionization due to heavy ions and indirect ionization caused due to protons and neutrons. The authors concluded with a remark that the circuit level techniques came out to be effective in nature. Increased area and more number of transistors are some of the disadvantages of the circuit level techniques. Also, passive feedback elements are held responsible for reduction in circuit performance and degradation in IC manufacturability. Due to the devices being evolved to smaller dimensions, new challenges will be encountered for device level modeling. Simulation tools are required to be more validated and predictive in nature. Single event upsets at the ground level will be in continuous nature for microelectronics [18]

In 2005, S. Mitra *et al*., found that the advanced technologies like 90nm, 65nm and further are much more frequently affected by radiation strikes as compared to previous occurrences. They derived that soft errors associated with digital systems have gained much significant attention. The need to evaluate the effect of soft errors in flip flops, latches, combinational logic etc is incorporated along with effective mechanism to curb their effect. A comparative study of circuit level hardening techniques was done with other hardening methods with respect to areas protected, performance overhead, undetected errors and applicability. They concluded that soft errors occurring in digital designs are getting worse with higher levels of integration. Novel radiation hardening techniques are not only required in SRAM cells but also in combinational logic and sequential elements [19].

In 2006, J.E. Knudsen *et al*., described radiation hardened by design flip flop with high single event effect immunity. Circuit size and power are reduced i.e. a temporal latch and a master slave are used in 0.13um technology. SEE immunity has been tested using heavy ion testing and power results are described. Power measurements in this investigation show that the combined temporal dice flip flop shows a 13% energy savings. Layout is improved such that the top and bottom circuits are separated so that the NMOS circuits are separated which increases the threshold LET of the design. [20].

In 2007, T.H. Chen *et al.,* discussed a RHBD register file on 130nm node. DICE is undergone heavy testing. It is observed that no errors are observed at any voltage showing that the DICE is capable of removing diffused charge from the ionizing particles. It means that operating voltages are viable for ultra low power RHBD integrated circuits [21].

In 2007, O.A. Amusan *et al.,* studied the directional dependence of the radiation strike on the semiconductor device. Heavy ion testing of RHBD of 90nm DICE cell is observed. The conventional techniques to attain radiation hardening by design overlook these type of dependence which results in underestimation of error rates in deep submicron technologies. Using 3D simulation techniques, the results show that the charge collection and charge sharing process has a strong dependence on the angle strike [22].

In 2009, M.Haghi *et al.,* discussed a new RADHARD structure called DICE. Two basic concepts used here are feedback and redundancy. The D flip flops which are designed on the basis of DICE latch are capable of restoring the original state, when a radiation strikes on a particular node. Data in DICE is stored as a pair of complementary values on A, B, C, D. The usage of symmetric structure makes it easy and feasible. They concluded with the result that for the smaller technologies, nodal separation is possible within the nodal separation [23].

In 2010, S.M. Jahinuzzaman *et al.***,** a single phase clocked structure is introduced which shows robustness against SEUs. This flip flop contains an input stage having a clock (single phase) to the storing unit using positive edge of the clock. The storage unit has DICE. The two nodes in the storage unit with same logic are passed from a C-element to the output node. This C-element helps to mask the SET pulse to propagate to the output. This flip flop is used in SOCs and microprocessors [24].

In 2011, O. Runao *et al.,* investigated that redundancy is a popular technique to increase the reliability of the circuits. Triple Modular Redundancy is frequently used but in case of high area. They concluded with the benefit of applying an optimization process reducing a computation time to achieve the optimal solution as compared to the default case of choosing an arbitrary initial partition. A real example has been presented that goes well with the realistic circuits [25].

In 2013, K.C. Wu Due discussed that due to current technology scaling trends such as shrinking feature sizes and decreasing supply voltages, circuit reliability is becoming more susceptible to radiation-induced transient faults (soft errors). Soft errors, which have been a great concern in memories, are now a main factor in reliability degradation of logic circuits as well. A systematic and integrated methodology for circuit robustness to soft errors has been presented. The proposed soft error rate (SER) reduction framework, based on redundancy, aims at eliminating those gates with large contribution to the overall SER. This approach is very well applicable to sequential circuits [26].

In 2013, Mahesh T. Kolte *et al.,* found an alternative way to have a fault less system. Triple Modular Redundancy is used for making a fault tolerant system. This model not only detects the faulty processor but also detects the fault but also repair the faulty bits in the processor. The authors concluded with the result that the TMR administrator will come to know which of the processor has failed and is being diverted from regular program [27].

In 2014, J.F. Lin *et al.,* presented an ultra low power flip flop design with master slave logic on 90nm technology node. In this design, logic reduction scheme is used at different process corners. The key idea which was used by the authors here is the use of discharge path between the master and slave latches which shortens the transition time to enhance power in a system. The proposed design was determined to have better results in every performance which proves the efficiency of the design [28].

In 2016, K. Prasad *et al.*, investigated a new radiation hardened scheme in for harsh radiation environments. In this type of circuit, main system is replicated three times and the output is forced to be passed from a majority voter. The voter plays a pivotal role that the erroneous value cannot be propagated to the output of the system. It ensures that the system is operated correctly even in the presence of a radiation event. However, replicating the system three times increases the delay and power dissipation as well [29].

A lot of research has been done in the field of radiation hardening till now. It started from the study of sources of radiation in the space applications. Later on, the radiation keeps on leaving its impact at the ground level becoming prominent in terrestrial applications, shrinking of the technology node being the ultimate reason. The charge deposited by the radiation, then, became an important phenomenon to study further in the discipline of circuit level radiation hardening approaches. Therefore, there is a great need to calculate the critical charge and the sensitive nodes in a circuit which is done in the next chapter along with the modeling of double exponential current pulse. So, the proposed algorithm is implemented on the radiation hardened structures and the proposed algorithm with the calculation of delay, power dissipation and the critical charge.

CHAPTER 3

DEVELOPMENT OF ALGORITHM FOR RADIATION HARDENED STRUCTURES

3.1 OVERVIEW

In this chapter, initial studies required for study and experiments of radiation hardening is done. To study radiation hardening on Flip-Flops (FFs), various configurations of flip flops were made in 90nm technology. The configurations varied on the basis of presence and absence of set and reset pins. The basic approach to combat the issue is by first detecting the vulnerable points in any circuit. Thus evaluation of various flip flop designs to find the susceptible nodes and their vulnerability with the help of scripting Language (ECL) simulations was done.

3.2 ALGORITHM TO CHECK RADIATION EFFECT

There is an algorithm which used for analyzing the effect of radiation on the devices.

1. Initially the flip flop circuits are designed using cadence virtuoso tool. The netlist of the design is extracted.

2. The algorithm finds the MOSFETS in cut off region by comparing each ones gate to source voltage to the threshold voltage. If Vgs < Vth, off MOSFETS are detected and redundant nodes are identified.

3. A double exponential current pulse is modeled using exponential function at the susceptible node of the circuit and the simulations are being done.

4. Finally, the output of flip flop is observed and if data at the output is flipped then the area under the area under the current pulse is integrated upto the time period of pulse using the integral function and that is equal to the critical charge of that output node. If the data at the output does not flip, the higher peak current is used to find out the critical charge value.

3.3 MODELING AND STUDYING THE EFFECT OF RADIATION ON DIFFERENT MEMORY ELEMENTS (FLIP FLOPS)

In order to understand the radiation effect on the semiconductor device different models of flip fops were made in the 90 nm CMOS technology. The main task is to identify the sensitive nodes or the vulnerable points in the modeled circuits and this task is done with the help of scripting language (ECL). After the simulation the vulnerable nodes are found out.

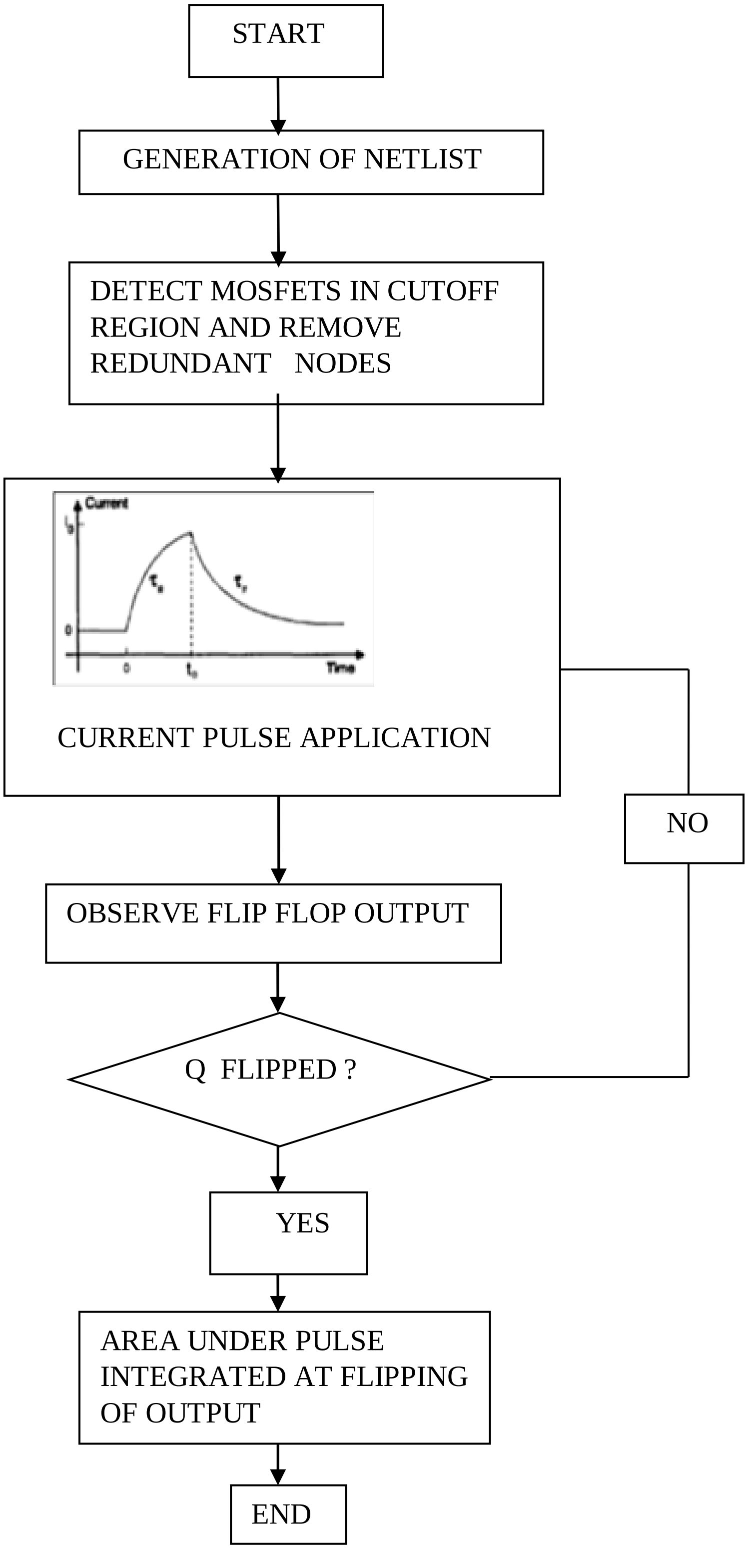

Figure 3.1: Algorithm to check radiation effect

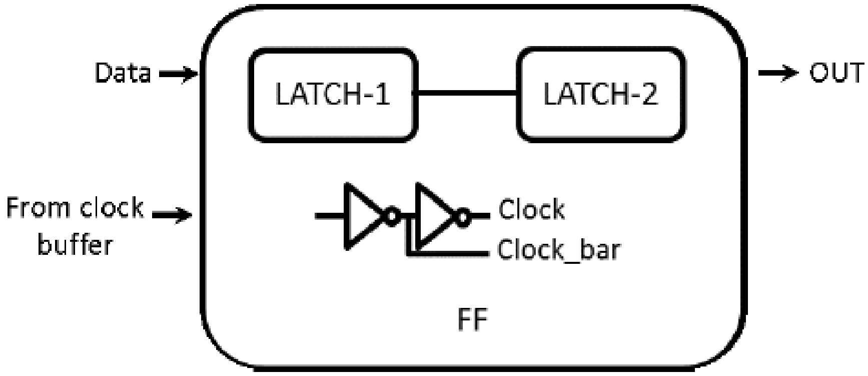

Figure 3.2: Circuit of Flip Flop under consideration

Node 0 represents the inverted clock Node
Nodes 1,Node 3 represents Internal Nodes of 1st and 2nd latch respectively,
Node 2 represents the Node which Connects 1st and 2nd latch
Data represents the input node and OUT represents the final output of the flip flop design.
Analysis is done by observing different values of critical charge at the nodes 0,1,2 and 3 during charging and discharging condition of that particular node. A comparative Table 2.1 is given to understand the relative critical charge value of the nodes of five different types of configurations designed for various radiation hardening applications.

Table 3.1: Comparison of QCRITICAL values at FF internal nodes

Node	**FF1**		**FF2**		**FF3**		**FF4**		**FF5**	
	C	**D**	**C**	**D**	**C**	**D**	**C**	**D**	**C**	**D**
0	-0.7	0.4	-0.8	0.3	-0.8	0.4	-1	0.5	-1	0.4
1	-0.5	0.3	-0.6	0.4	-0.6	0.3	-0.8	0.4	-0.6	0.3
2	-0.8	0.5	-0.7	0.4	-0.5	0.2	-0.7	0.6	-0.8	0.6
3	-0.4	0.3	-0.3	0.2	-0.3	0.2	-0.4	0.3	-0.3	0.2

`

Here, C means charging and D means discharging and respective values are in pico coulombs

3.2.1 Fall time variation

The fall time of the current pulse is being varied for analyzing its effect on the accumulation of charge on a node. Different values of Fall Times taken are 100pS, 500pS and 1000pS. The observation is that the alteration in the data surely starts late but it attains the faulty level before the outputs flipped which are with lesser fall-times. Only a negligible amount of difference was found and hence the effect of fall time was not considered for further analysis. The result of analysis is represented in the figure belo

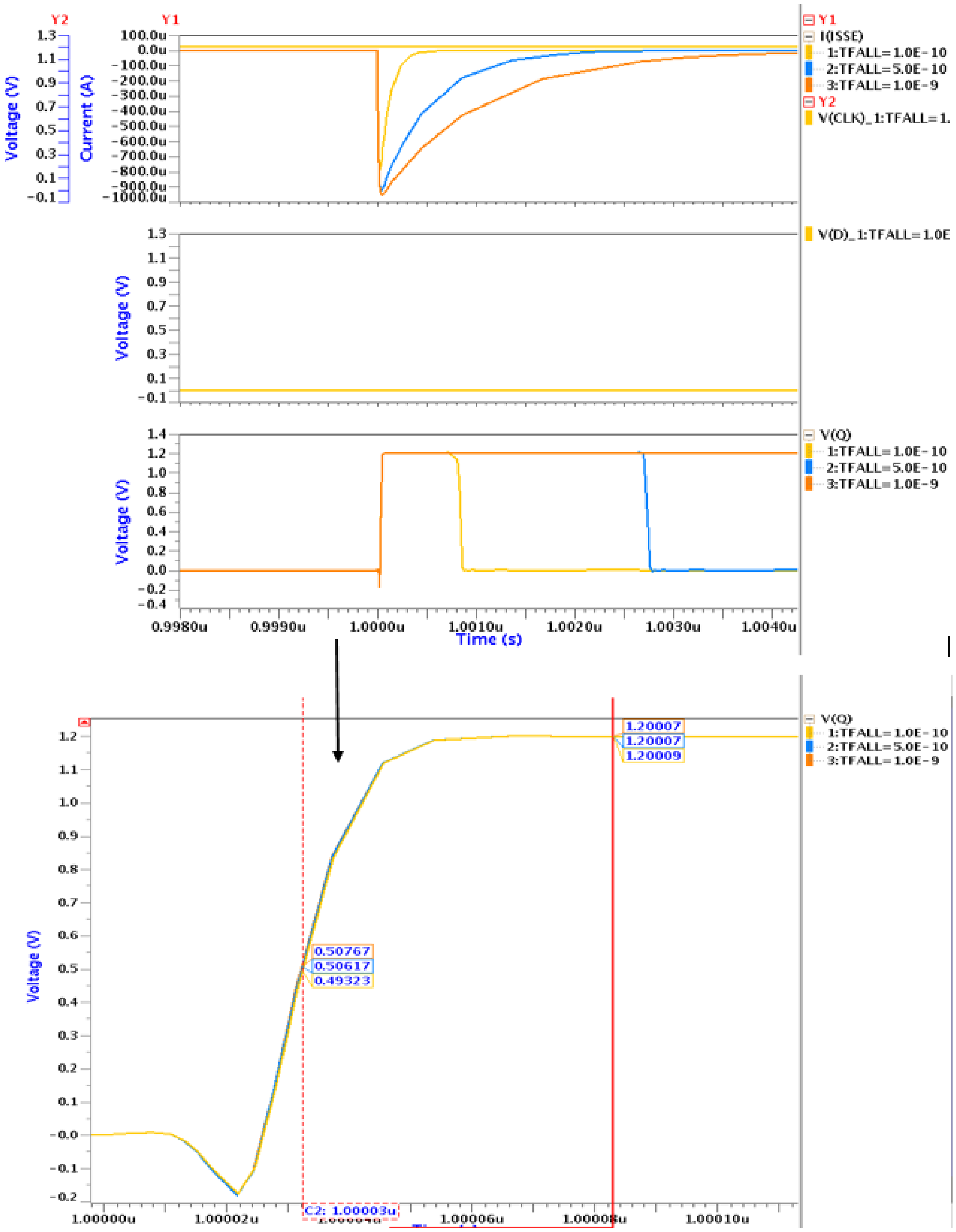

Figure 3.3: Variation due to variation in fall time

Simulation with varying value of the fall time is done on a particular node of Flip-Flop, increasing peak current. The data provided during this simulation are, clock is 1, Data is 0 and the output attained is 0.

3.4 ANALYSIS OF STACKED CONFIGURATION

Stacked configuration refers to the arrangement of transistors in an array. This configuration is used here as it increases the node capacitance.

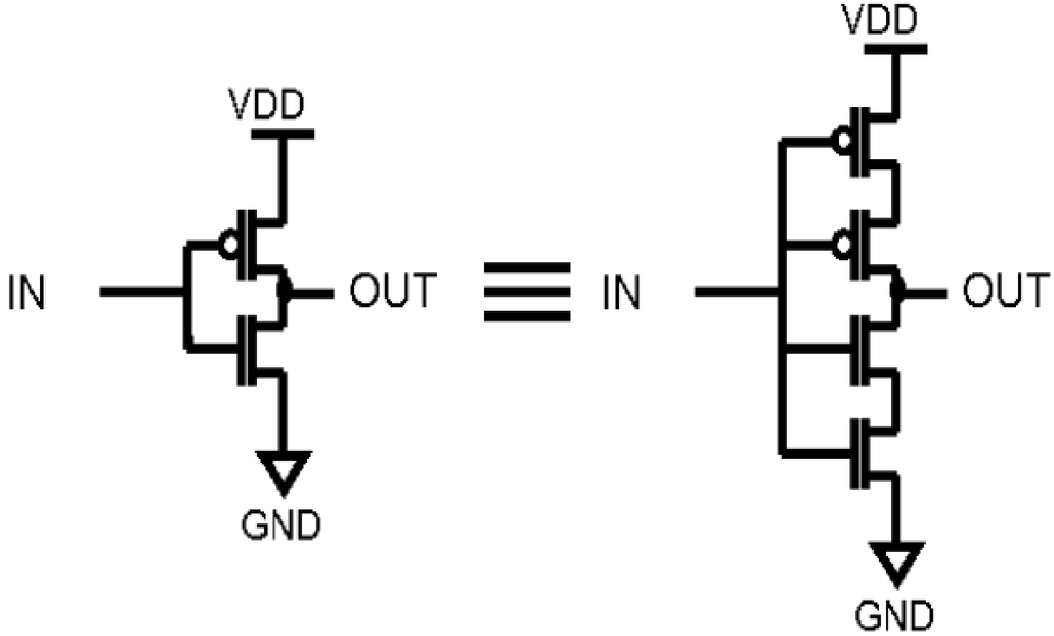

Figure 3.4: Regular inverter versus the stacked inverter

Figure 3.4 shows the use of stacked inverter configuration rather than the regular inverter which consists of 2 NMOS and PMOS transistors. This configuration leads to a more robust design but it is done with the trade off with area. It leads to increase in the value of resistance of the circuit because of which the stored value of the output node takes more energy as well as more time to flip the data while charging and discharging of the node capacitance. The circuit gets enough time for the exponential pulse to lose its energy and eventually it dies. Therefore, it does not allow the faulty value to propagate to the output node of the device. Also, it leads to greater delay because of the increased value of capacitance and resistance at the output. However, the process of stacking is preferred as it shows positive results in terms of increased critical charge value.

For peak current of 0.5mA, critical charge in case of flip flop with regular inverter is calculated as 0.02pC and for stacked inverter, it is 0.23pC.

3.5 CONCLUSION

The conclusion attained after the experiment performed on the circuits are as follows:

1) PMOS is more robust as compared to NMOS.

2) Variation of fall time did not show any significant effect on the output. Therefore, it is not considered an important parameter to be analyzed further.

3) Increasing the value of resistance and capacitance at a node leads to the increase in robustness for radiation induced errors.

4) After modeling the double exponential current pulse, the rise time is 10ps and fall time is 460ps.

After the modeling of double exponential current pulse, different RADHARD structures are implemented and current pulse is injected to find the circuit behavior and its robustness.

CHAPTER 4

RADIATION HARDENED STRUCTURES

4.1 OVERVIEW

Radiation hardened structures are designed by implementing redundant structures which adds extra delay between input and the output of the flip flop. Single event transient pulse cannot travel to the output if the delay is not large enough, SEU will not occur. Also, redundancy increases the design resistance. By increase in resistance, the time to charge or discharge the node also increases due to which the double exponential current pulse dies and the erroneous value does not propagate to the output. This chapter discusses some radiation hardened structures implemented in 90nm technology node.

4.2 DICE

4.2.1 Implementation

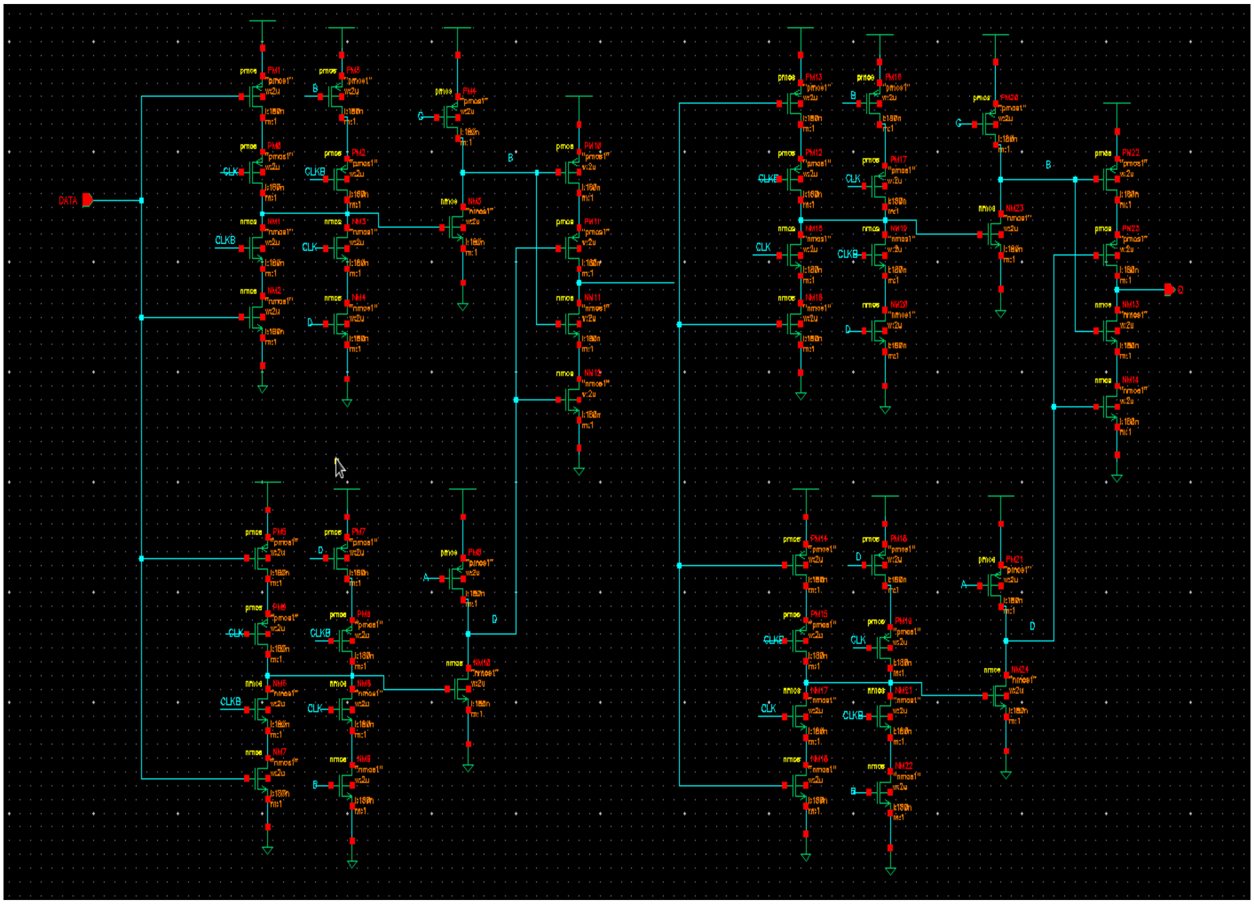

Figure 4.1: DICE circuit diagram

In this circuit, DICE circuit is implemented using transistor stacking having A, B, C and D be their internal nodes.

4.2.2 Input and Output waveforms

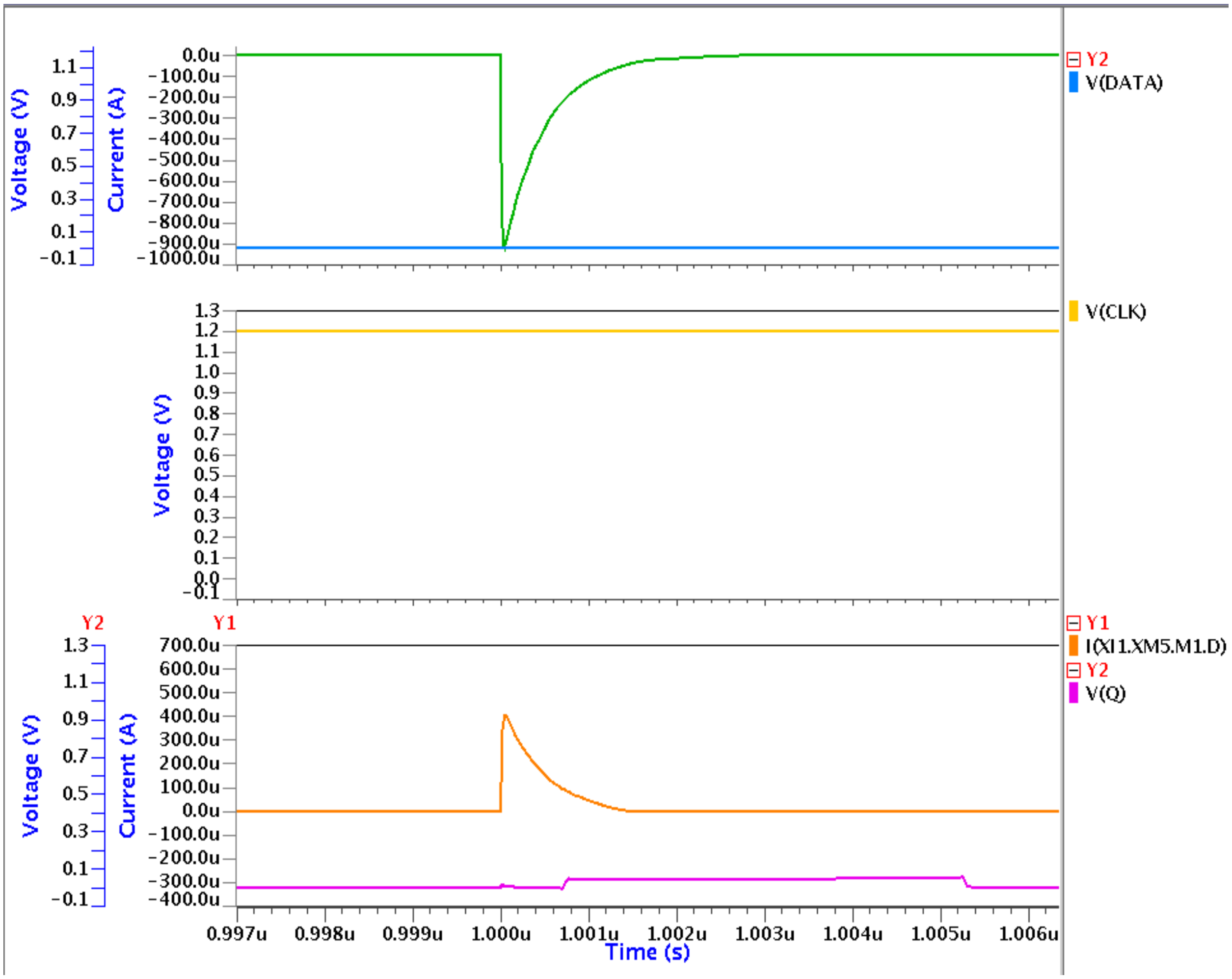

Figure 4.2: Simulation results of DICE

Here is a basic flip flop design using DICE concept and the effect of radiation was observed on it. Clock pulse (CLK) is high and the data is low, the output is observed to be low. When the current pulse is modeled as the radiation effect with peak current 1mA and applied on node M of the PMOS transistor as represented in the waveform. It shows that the DICE structure shows robustness against radiation. Using this structure, radiation can be prevented to propagate to output to some extent but also adds to the propagation delay. There is also a tradeoff for power consumption. Therefore, DICE exhibits radiation resistant property but compromise between delay and power id done.

4.3 TMR (TRIPLE MODULAR REDUNDANCY)

It is one of the old techniques to overcome the effect of radiation that uses three identical structures arranged in parallel. Same data is given at three inputs following by the voter circuit. If an error occurs at any of the nodes due to radiation strike then it can be easily detected at the output as the error occurred is corrected by the voter schematic. The circuit is called so as it will reflect the output which it will receive in majority at the input i.e. the most common value out of three outputs is considered as the correct output. The issue faced with TMR is that it exhibits more area and power as compared to the basic circuit.

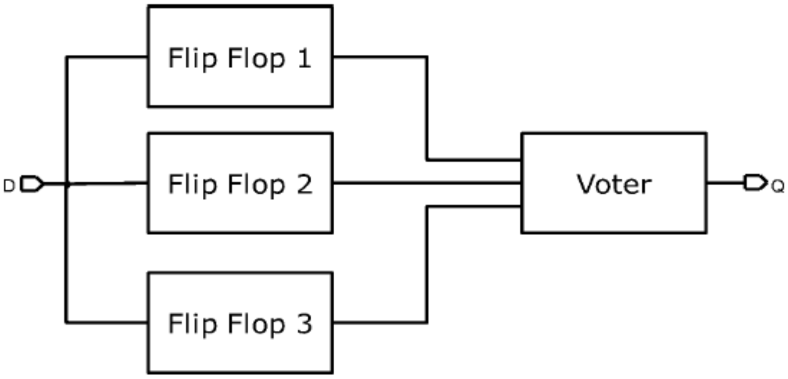

Figure 4.3: TMR structure

The voter schematic (Figure 4.4) is represented by the equation OUT= A*B + B*C + C*A. If there are no input failures, the output of three circuits are identical. But due to circuit failures, the output of one of the three circuits may be different due to the radiation strike which is prevented by the usage of voter circuit.

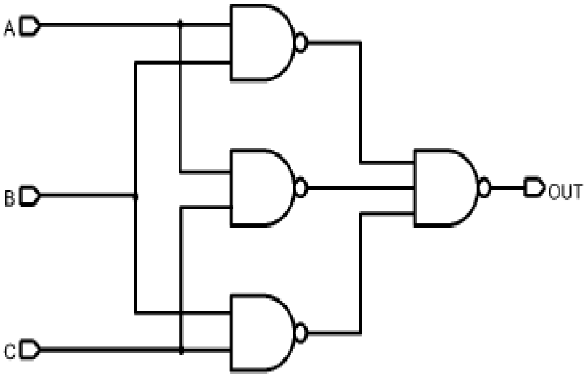

Figure 4.4: Voter Schematic

4.3.1 Implementation of TMR

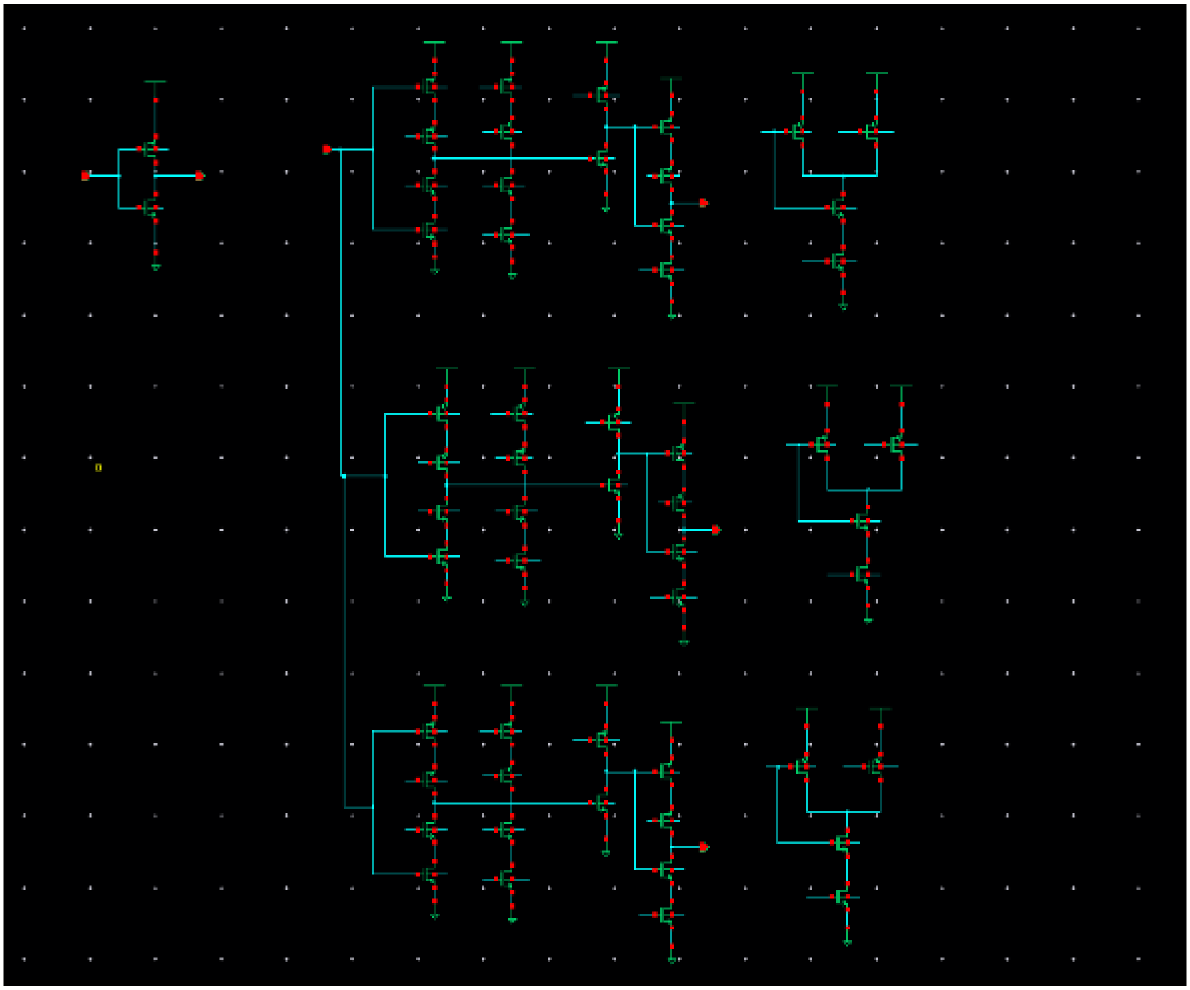

Figure 4.5: TMR circuit diagram

4.3.2 Inputs and Outputs of TMR

In Figure 4.6, D and Q represents the input and output of the circuit and Q1, Q2 and Q3 represent the outputs of flip flop 1,2 and 3 respectively. As explained in voter circuit, if there is any non matching input to voter, then the value of the output is retained. An assumption is also made that radiation strike will occur only on a single node of the circuit. The probability of effect of radiation of multiple nodes is very less. As it can be seen from the output of EZ wave that if there is any fault in Q3,the correct value is carried by Q1 and Q2 nodes. The output value is unaffected by the error faced by the node Q3 i.e. it is retained. Here, ISSE represents the double exponential current pulse with peak current 10mA.

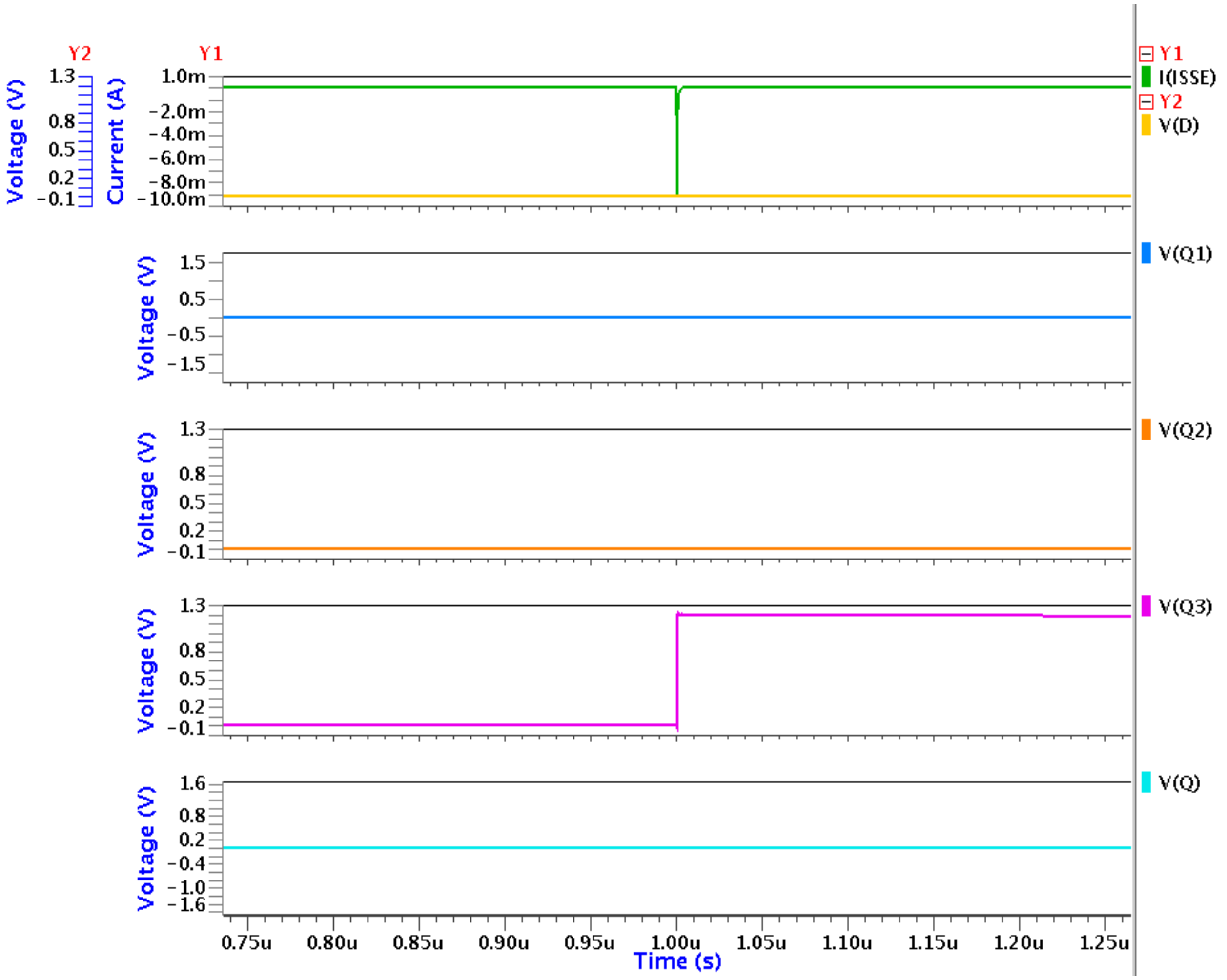

Figure 4.6: Simulation results of TMR

4.4 SPCD (Single Phase Clocked Design)

In flip flop design, only one transistor is clocked by clock pulse which is called True Single Phase Clocked Design. It offers less power consumption and higher speeds. These type of designs enable less sensitivity towards radiation. They work on the principle of pre-charging of internal nodes. The structure which is implemented here has DICE as the storing unit. The two nodes in the storing unit with the same logic are passed from the C-element to the output node.

4.4.1 C-element

C element is a structure which was proposed by Intel. The structure (Figure 4.7) and working is given below. In this circuit, output is generated only when both the inputs are same, but if the inputs are not same output attains the previous value only. Thus, this element is used to rectify the soft errors in flip flop design.

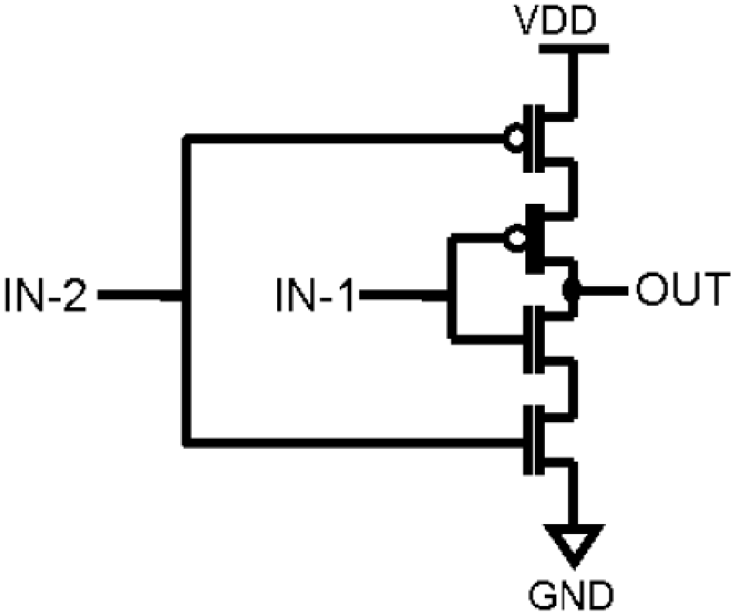

Figure 4.7: C-element

Hence, using this design any error in the input can be restored at the output of the device. If any of the nodes in a circuit gets affected by the radiation strike and the data stored at that node changes, then the C element will detect the difference and in place of getting uncertain output it will restore the previous output value only. Its truth table is shown in Table 4.1.

Table 4.1: Truth table of C-element

IN1	IN2	OUT
1	1	0
0	0	1
0	1	Previous value attained
1	0	Previous value attained

4.4.2 Implementation of SPCD

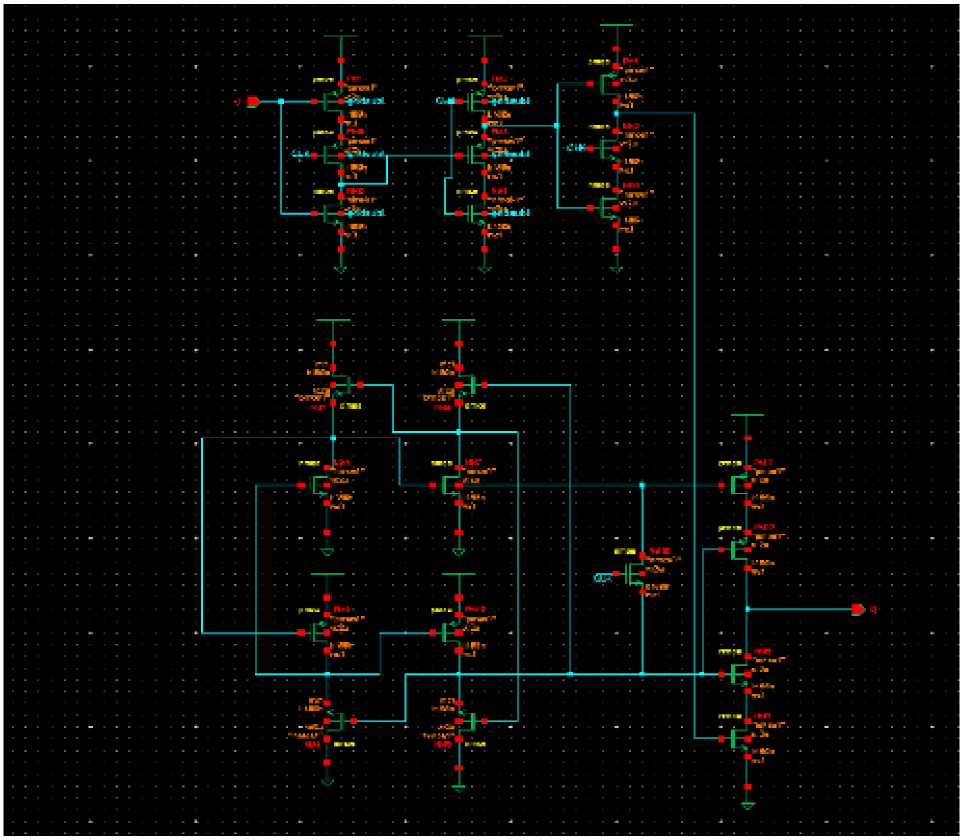

Figure 4.8: SPCD DICE structure

4.4.3 Inputs and Outputs of SPCD

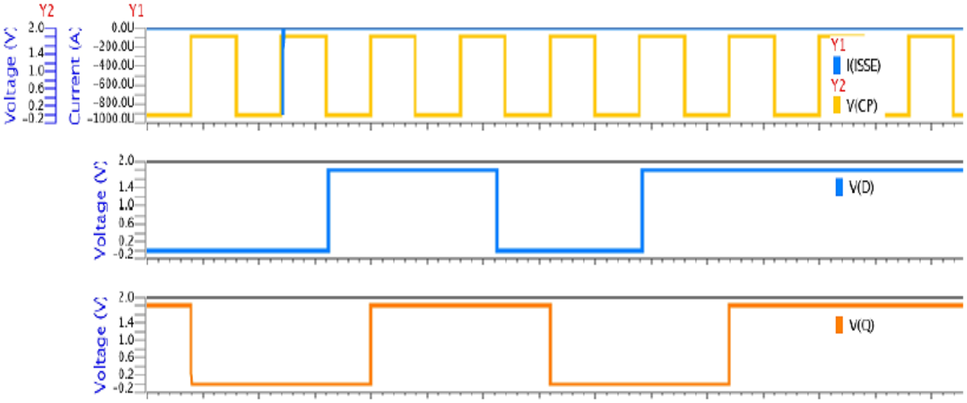

Figure 4.9: Simulation results of SPCD DICE

4.5 PROPOSED DESIGN

The proposed circuit is designed using 90nm CMOS technology. It is alternative design to dual phased clock structure with less cost in terms of power. This design uses the properties like stacking of transistors, DICE concept. Hence for the radiation hardening, same quality of design results in the robustness in single phase structure.

The design which is proposed is represented in the Figure 4.10. It uses the following techniques:

1) Master and Slave flip flops are designed using DICE scheme.
2) Only a single phase of clock is used for both master and slave flops.
3) Stacking of transistor is done in both the master and slave designs.
4) There exists cross coupling between master and slave blocks.
5) Variation of clock slope is done

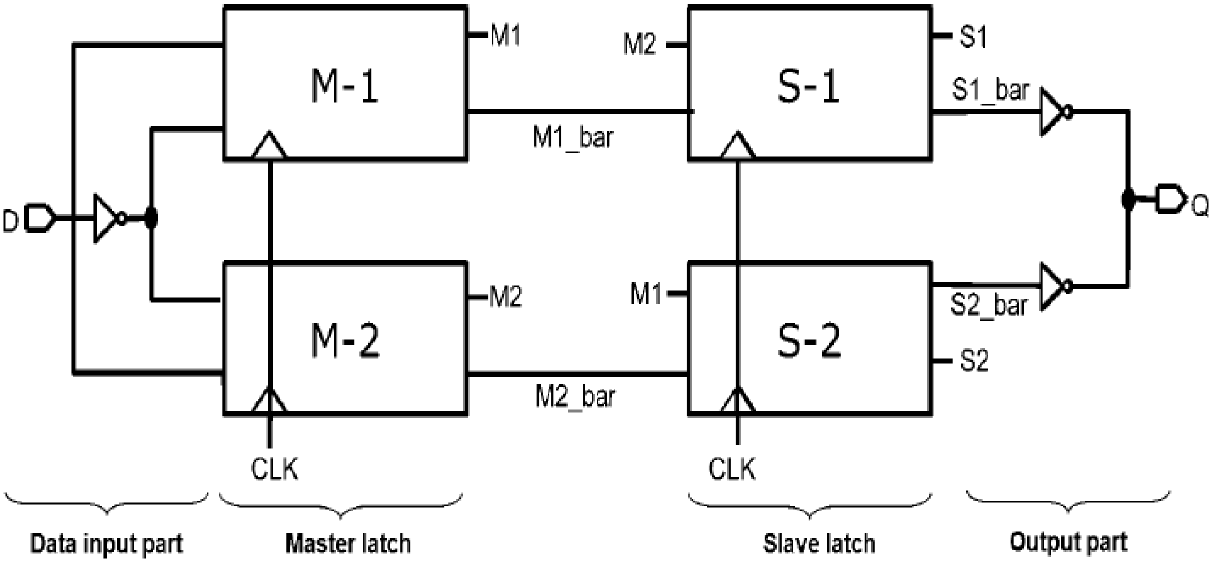

Figure 4.10: Proposed design

In the normal master slave configuration flip flops, the master and slave works on different phase of the clock. But here in the proposed structure SPCD designs, only single phase of clock is sufficient for the working of master and slave flip flops. Hence, this can reduce in the probability of getting an error in the form of glitches in clock. DICE configuration is used to design both master and slave and also cross coupling is done between master and slave stages of the design. This provides effectiveness of redundancy in the circuit which is required for robustness. Thus, the robustness increases for the proposed structure. The output of slave stage is opposite to that of at output.

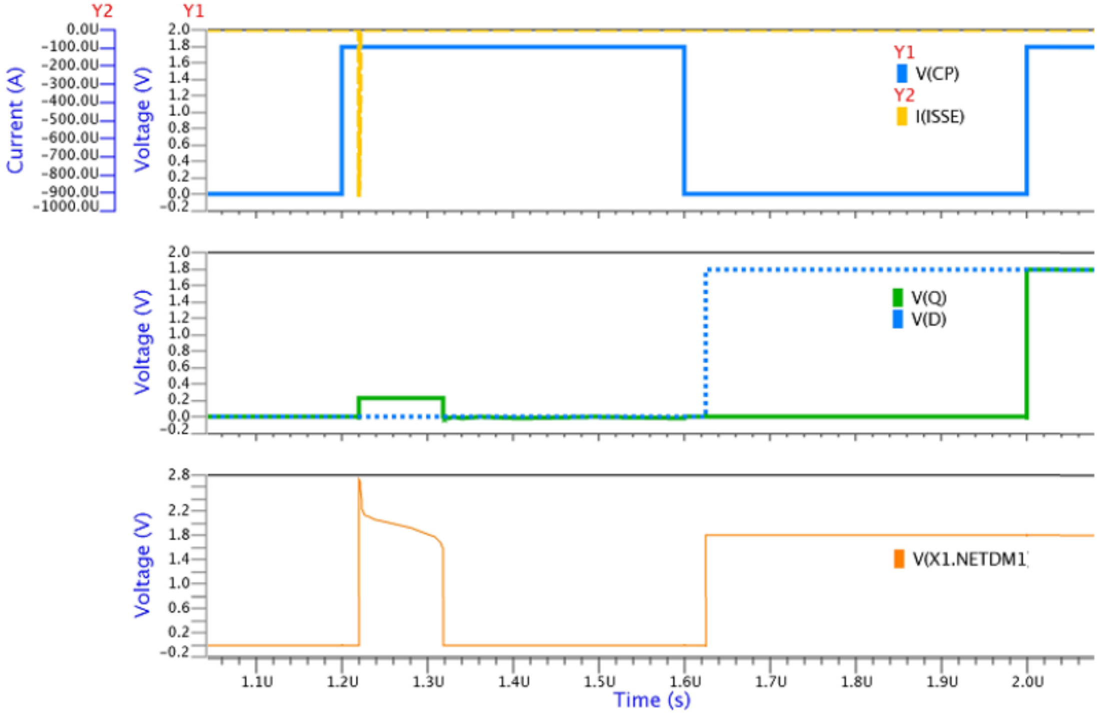

Figure 4.11: Simulation results of proposed design

CHAPTER 5

RESULTS AND ANALYSIS

5.1 OVERVIEW

This section has the comparative analysis results of various radiation hardened structures discussed in this piece of work. These structures are implemented at 1.2V on typical scenario. Normalized values are being used to plot the graphs. The parameters like propagation delay, power dissipation and critical charge are calculated using the model file and the input initialization of the design are set of inputs for the script.

5.2 RESULTS

Various functions were applied in the script in order to perform the analysis. Calculations are done for different clock slope values (20 ps, 200 ps, and 2 ns). The results are shown below

5.2.1 Propagation delay

The value of the propagation delay was calculated using the functions like TPDUU and TPDUD in ELDO. The function TPDUD calculates the value of fall time delay and function TPDUU calculates the rise time delay value. Following are the results obtained in nano seconds.

a) Rising data

Table 5.1: Simulation results of rise time delay at different clock slopes

FLIP-FLOP/ CLOCK SLOPE	20ps	200ps	2ns
DICE	3.45	3.65	3.01
TMR	4.67	4.98	4.99
SPCD	3.22	3.29	3.72
PROPOSED	3.55	3.77	3.99

b) Falling data

Table 5.2: Simulation results of fall time delay at different clock slopes

FLIP-FLOP/ CLOCK SLOPE	20ps	200ps	2ns
DICE	3.90	3.93	3.11
TMR	4.72	4.78	4.87
SPCD	3.48	3.71	3.74
PROPOSED	3.80	3.85	3.90

5.2.2 Power dissipation

Different flip flops were taken under consideration and their power dissipation are calculated in nano watts.

Table 5.3: Simulation results of power dissipation at different clock slopes

FLIP-FLOP/ CLOCK SLOPE	20ps	200ps	2ns
DICE	5.75	5.63	5.44
TMR	6.89	6.68	6.01
SPCD	4.70	4.49	4.45
PROPOSED	5.71	5.81	5.46

5.2.3 Critical charge

Comparison of critical charge is represented as follows.

Table 5.4: Simulation results of critical charge

FLIP-FLOP	CRITICAL CHARGE (pC)
DICE	9
TMR	11
SPCD	13
PROPOSED	12

Thus, the proposed algorithm is well implemented on the RADHARD structures along with the proposed design.

CHAPTER 6

CONCLUSION AND FUTURE SCOPE

This work contains the radiation hardened structures implemented on 90nm technology. Proposed design and the state of the art designs are thoroughly studied and compared. DICE structure and stacking of transistors are used in order to implement these designs. Proposed design with better power and critical charge are discussed. The proposed algorithm is well implemented on the start-of-the-art designs and the proposed design.

The future work can be further carried on with the help of device modeling. It helps in analyzing the effect of radiation ion strike on the MOSFET by considering the effect on various parameters of the device along with the radiation particle. Study can be further using multiple particle strike effect of the devices.

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