DESIGN OF AREA AND POWER EFFICIENT N-BIT DIGITAL BINARY COMPARATOR

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MASTER OF TECHNOLOGY

In

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DECLARATION

I, Piyush Tyagi hereby declare that the work presented in this thesis entitled "**DESIGN OF AREA AND POWER EFFICIENT N-BIT DIGITAL BINARY COMPARATOR**" in partial fulfilment of the requirement for the award of degree of Master of Technology in VLSI Design submitted at Electronics and Communication Engineering department, Thapar Institute of Engineering & Technology (Deemed to be University), Patiala is an authentic record of work carried out under supervision of **Dr. Rishikesh Pandey**, Assistant Professor, ECED, Thapar Institute of Engineering & Technology from January 2017 to July 2018. The matter presented in this has not been submitted either in part or full to any other university or institute for the award of any other degree.

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It is certified that the above statement made by the candidate is correct to the best of my knowledge and belief.

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ABSTRACT

The design techniques aimed for the optimizations of the area, power and speed parameters of the digital circuits are used as the integral part in design process of any modern digital electronic device. To achieve the high speed and low power operation, an extensive research of such techniques is required. Proposed N-bit digital comparator designed with minimal number of transistors, can operate with high operating speed while dissipating limited power in any digital building block. With the advantages offered by it, it has presented itself as a promising substitute over other conventional comparator design approaches.

In the proposed circuit Novel EX-OR-NOR logic cells are used for the power and area optimizations. The circuit intended for comparison of 64-bit operands has full input-output swing of 1.8V, maximum operating frequency of 1.75 GHz, worst case power dissipation of 1.03 mw/ GHz and requires total number of transistors as 1384 for its operation. The proposed circuit architecture have been designed and simulated in Cadence Virtuoso Design Environment using Gpdk 180 nm CMOS technology. The comparison of the proposed N-bit digital comparator with other comparator structures available in literature shows that the suggested comparator design can be used in the jitter measurements, built in self-test circuits, load-store queue buffers, etc.

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CD	Constant-delay
BCL	Bitwise Competition Logic
MSB	Most Significant Bit
LSB	Least Significant Bit

CHAPTER 1

INTRODUCTION

1.1 INTRODUCTION

At the present time there is a great requirement for low power, high speed and area efficient competitive system designs aiming portable devices because of its emerging prominence at marketplace for example portable wireless communication devices, portable devices for medical application, notebooks, laptops and many other computing devices. As a result of the popularity of these devices and its future aspects, this area is evolving as the main field of focus for most of the electronic design companies. Limited battery life of the portable system further imposes the strict demands on the power consumption along with high throughput and required chip density by the various sections of the circuit's architecture. Power dissipation, area, operating speed of the circuit is determined by the logic style used in structuring the circuit. Appropriate choice of the logic style is mandatory because characteristics of the circuit varies with variations in the logic style used for designing which further effects the efficiency of the design. Comparator is the fundamental design element which is incorporated in various digital systems. Comparator serves as the basic combinational circuit which is used to determine the relative magnitude of operands taken for comparison. The result of the comparison with respect to first operand can be stated in three forms depicting “greater than”, “lesser than” or “equal to” the other operand taken for comparison. Comparison is the basic arithmetic function which is carried out in various computational based applications such as graphics and image/signal processing [1,2], sorting process required for multiprocessing and parallel computing [3], test circuit applications [4,5] and evaluation based task carried out by the various components of general purpose processor [6-8]. The widespread use of comparator based design in high-end system trigger off need for the limited power consumption and the performance optimizations of the circuit. Various architecture for the comparator based design are proposed in the recent years which mainly consists dynamic logic based gates structures [9-13], the flat adder circuitry [14-16], hierarchical prefix-tree based structures [17], mux-based topology [18], priority-based encoding mechanism [19], ripple based structures [20-24]. In this chapter the conventional design techniques are discussed. The motivation behind the research is also mentioned followed by the organisation of thesis.

1.1.1 Different design techniques of comparators

For the purpose of increasing the portability of the electronic design, optimizations are carried out which majorly focus on area consumption, power dissipation, functional complexity and operating speed of the comparator architecture. Some of the major design topology used to develop the comparator architecture in recent years are discussed as follows:

1.1.1.1 Adder based comparator structure

In this technique, primitive way for implementing comparator design using parallel adder was taken into consideration. In this design output signal resulting into “a” greater than “b” is determined by the Manchester chain and “a” equal to “b” as the output result is determined by dynamic NOR gate. Then “a” equal to “b” and “a” greater than “b” both results combined to give third output as “a” less than “b”. Manchester Comparator is the dynamic structure [13]. Dynamic logic is advantageous when compared to the static CMOS logic in terms of low power dissipation, reduced parasitic node capacitances and less switching activities caused due to false transitions, but it suffers from limitation like low noise margin, low-speed and requirement of the node capacitance refreshment for dynamic storage of the charge. The comparator structure which incorporates adder structures uses unnecessary arithmetic function causing complicated physical implementation. These structures are area intensive and typically have slow response.

1.1.1.2 Hierarchical prefix tree based comparator structure

This approach uses tree-based design to ease the comparison process. Comparator based on this approach aims for static logic design. To reduce the delay of the design, constant-delay (CD) logic is entirely realized in timing-critical stages without losing the energy consumption. Usage of CD logic in the design results into speed improvement over the dynamic domino logic with equivalent robustness and clock-timing requirements. The most distinct characteristics of the CD logic that delay of the design remains unaffected by the logical expression. CD logic inherits the Timing Block for the creation of the adjustable window to reduce the static power dissipation and the Logical Block for reduction of the Glitches as well as for making the cascading CD Logic feasible [17]. Due to the presence of cascaded logic and comparison levels, these design are prohibited for the comparison of large bit operands.

1.1.1.3 Mux based comparator structure

The limitation encountered in the prefix tree structure’s area and power consumption was improved by incorporating mux based topology in place of comparator cells together with generate-propagate logic cells at the first level instead of using adder cells previously [13]. In this design [18] the implementation of AND gate, OR gate and Multiplexer Network is developed by NMOS logic. In this approach complementary pass transistor is used for the reduction in the data skew problem. Using this technique, for the large bit operands comparison, prefix-tree requires more levels but it suffers from the high power consumption problem as every cell existing in the structure being active, irrespective of input operand's width. Moreover the structure [18] achieves "less-than" or "greater-than" comparisons and not equality.

1.1.1.4 Priority encoder based comparator structure

Priority encoder based comparator structure accomplishes the comparison between the provided operands using priority-encoding algorithm and the dynamic circuit technique [19]. Structure of this type suffer from the heavily loaded parasitic components on the present clock signal which further limits the jitter margin and clock speed.

1.1.1.5 Ripple based comparator structure

This approach reduces the switching activity in the comparator architecture with the usage of compute-on-demand topology. The comparison operation is performed on each bit of both the operands at a time while rippling from most significant bit to the least significant bit. The comparison outcome obtained from each bit comparison activates the comparison of the next subsequent bits of the operands [20-24]. Though this approach switching activity can be reduced but the design suffers from limited operating frequency.

1.1.1.6 Bitwise competition logic based comparator structure

To reduce the delay faced by comparator architecture based on bitwise ripple design, an improved architecture was presented in [25], which is based on the algorithm that does not involve any arithmetic computations for comparison. In this approach, the larger among the two operands taken for comparison is decided with the help of Bitwise Competition Logic (BCL) by spotting the location of first logic one bit referenced from the most significant bit of the result obtained after pre-encoding of input operands. The digital comparators based on this approach [25] use pre-encoder followed by the BCL structure. Encoding of each bit of two input operands is performed by the pre-encoder structure before applying it to the BCL structure. Further, for the prevention of the logic failure of the BCL structure through removal of the possibility of having both input operands as one at the same bit position. BCL structure is designed in such a manner that detects the earlier first "logic 1" from MSB among two input operands. The result from the BCL structure further given into the multiplexer for the determination of final comparison result [25]. Due to high power consumption and limited operating frequency restrict the usage of BCL based comparator structures.

1.1.2 Motivation

In the portable electronic equipment market, designs are aimed for having low power consumption, high operating speed and minimum area intensive structures. Optimum logic style of the design affects the size, speed, power dissipation and wire complexity of a circuit. Previous comparator architectures have serval drawbacks, in which majorly include high power consumption, custom structures that are unsuitable for the continued technology scaling, irregular VLSI structures causing long time to market, multicycle computation and limited operating speed. Usage of digital comparator architecture as the key design element in various digital building blocks leads to great requirement of the optimization of the design. For the enhancement of the operating speed and reduction of switching activities in the circuit, prefix tree [17] and ripple based design [20]-[24] approach is employed in proposed comparator architecture. Usage of combinational logic in the designing of the proposed architecture further enhances performance by the elimination of the heavy loaded clock signal [25]. The drawback of the previous structure such as short time to market and continued technology are eliminated by the usage of reconfigurable arithmetic algorithm for the designing of the proposed comparator structure. Proposed comparator circuit eliminates the possibility of irregular comparator structure by leveraging single-gate-level logic at every stage irrespective of bit length of operands taken for comparison.

1.1.3 Organisation of thesis

The organization of thesis is as follows:

Chapter 1 introduces to various comparator techniques used for comparison and motivation behind new comparator structure.

Chapter 2 presents the brief description of the research that has been reported in the literature in the field of the digital comparator designs.

The proposed N-Bit digital comparator circuit using Novel EX-OR-NOR cell in Chapter 3.

Chapter 4 addresses the simulation results of the proposed circuit. The results have been compared with the similar circuits available in the literature.

Chapter 5 concludes the report while also mentioning the future possibilities to carry forward the research in this domain.

CHAPTER 2

LITERATURE SURVEY

This chapter discusses the research work which has been carried out on the comparator architecture cell reported by the various authors in recent years. A concise review based on the study of the papers is as follows

Suzuki *et al.* [1] introduced diode-partitioned domino circuit based tag comparator architecture intended for 64-bit microprocessors. The diode circuit consisting in the proposed domino block helps in boosting up the gate voltage of NMOS diode. Diode-partitioned domino circuit enables the smaller keeper in gates with high fan-in and also facilitates in the reduction of parasitic capacitances. It has been discussed that the presented domino circuit based tag comparator provides improvement in the operating speed as compared to conventional complex domino circuit based tag comparators.

Guangjie *et al.* [13] presented digital comparator design based on the Manchester chain structure for realizing the comparison results. Authors discussed about the suitability of the design for further achievement of the parallel or pipelined operation in view of the fact that clock signal was used as the controlling signal for the Manchester comparator architecture. Dynamic design approach had been used for prevention of switching activity caused by the false transition in the circuit. Additionally, due to insertion of dynamic latches and other optimization the harmful noise present on the input signal have been isolated.

Comparator architecture based on the hierarchical prefix tree structure is proposed in [17]. For handling both floating point operands and the two’s complement operands author have used serval cascaded logic gates structure at each level. The structure reported by author supports not only the comparison of 32 or 64 bit floating point operands but also the comparison involving their complements. Suggested structure by the author aimed for improvement in the operating speed as well as occupied area when compared with other comparator architecture used in application specific and other general purpose processor.

Cheng *et al.* [18] has modified the prefix tree structure for achieving the further improvement in the area and power consumption of the design. Comparator structure specified by the author is based on the conditional sum adder scheme and the principle of 1’s complement. Reported structure by the author have the limited propagation delay and transistor count as compared to other conventional comparator design. The author specified the possibility of additional reduction in power dissipation and the data skew problem in the proposed architecture through the replacement of static CMOS logic gates with the Complementary Pass-transistor logic in the low voltage applications. Author also suggested the improvement in terms of data throughput with help of pipelined structures.

Wang *et al.* [26] has presented 64-bit comparator based on dynamic CMOS logic consisting of noninverting modified all-N-transistor block. In the design author has inserted two feedback MOS transistor for accelerating the pull-up charging and pull-down discharging mechanism of the comparator unit. The author has achieved the pipelined operation in the design without using latches through triggering the adjacent layer of comparator unit using two out-of-phase clocks. A comparison between presented comparator structure by the author and the other comparators design have also been reported, in which it is observed that all-N-transistor block based comparator structure offers better speed performance.

The high Fan-in dynamic CMOS comparator design consisting of low transistor count is reported in [27]. The comparator includes evaluation block consisting of two series transistors causing reduction in the pull down delay.

Serval comparators that depend on low-power design techniques and pipelining approach are discussed in [28]. These designs are intended for improvement in the power consumption and operating speed of the circuit.

Huang *et al.* [19] proposed comparator architecture based on the priority-encoding algorithm. The author has used the magnitude decision module which merges logic function with priority encoding function. The complete realization of magnitude decision module further completed in multiple output domino logic. The use of fewer transistor in the presented comparator architecture results in enhancement of the operating speed, compactness and power efficiency of the comparator design. Additionally, author also have realized latch-based two stage pipelined structure in the circuit for the further enhancement in the operating speed, which is achieved by partioning the logic function into two parts and executing each part in delay-balanced manner.

Larn *et al.* [29] introduced CMOS comparator architecture intended for high Fan-in applications. The design proposed by the authors performs the comparison operation in two hierarchical stages consisting of high Fan-in comparators in first stage and dynamic multiplexer structure in the second stage of the design. The modified structure of priority encoder is also presented which receives inputs from the first stage consisting of comparator blocks. It is discussed that reported architecture achieved the limited delay when compared with the other multi-stage 64-bit comparator structures.

Frustaci *et al.* [30] presented binary comparator design utilizing a fast low-power single clock cycle for the comparison. The reported architecture incorporates two-phase domino clocking [31] for performing comparison operation in single cycle and aims for reducing power consumption by eliminating dynamic switching activities at the internal node of the design. Authors has also used parallel-prefix architecture for improving operating speed of the design. A comparison between the suggested architecture and the conventional design are also reported in which it is observed that the architecture achieves equal operating speed and lower energy dissipation than the compared comparator architecture.

Perri *et al.* [32] suggested comparator architecture which combines the two-phase domino clocking structure with the tree structure. Optimized adder module of the tree structure is constructed for computation of carry signal, which is the critical signal in the design presented. The proposed structure uses simpler logic Equations for the reduction in the computational steps with the intention of reducing the hardware complexity by using lesser number of input and output signals in each step.

Comparator architecture based on the reduction of switching activity is described in [23]. The structure presented by the author is based on the compute-on-demand design principle. The architecture uses asynchronous logic to achieve fast comparisons by checking just a few bits. It has been discussed that the circuit operates faster as compared to the equivalent synchronous design.

Lam *et al.* [24] presented the comparison algorithm based on parallel MSB exploratory method instead of priority encoding for the determination of most significant unequal bit. The architecture reported by the author achieves improved performance over conventional designs through the usage of fast dynamic NOR gates instead of NAND gates with high Fan-in.

Kim *et al.* [25] proposed the comparator architecture based on the bitwise competition logic. The presented structure by the author compares the two operands through examining the first “logic 1” from the MSB instead of using complex arithmetic computations for comparison. The described comparator architecture consists of pre-encoder, bitwise competition logic and the selection logic. Bitwise competition based comparator architecture offers advantages in terms of operating speed and the physical area occupied by the design.

Chuang *et al.* [33] introduced binary comparator structure based on the Constant-Delay (CD) logic. In the circuit, author has used single cycle tree based comparison scheme accompanied by CD logic for the comparable achievement of additional operating speed and energy consumption over the same design implemented using only static logic. CD logic presented in the architecture consists of PMOS transistors in the critical path of NMOS transistor network for conditionally making output transition to “logic 1” and pull-down NMOS logic for predischarges the output to “logic 0”. Reported comparator design consists of two stage, where first stage comprises of tree structure purposely aimed for attaining power efficiency and second stage takes advantage of CD logic for achieving high design performance without losing the overall power efficiency.

Scalable digital Comparator architecture based on parallel prefix tree approach is reported in [34]. Author has achieved the limited power dissipation in comparator circuit through the elimination of the unnecessary logic transitions that occur in circuit while performing computations. The comparator architecture consists of hierarchical stages which involves repeated logic cells with maximum Fan-in of five and minimum Fan-in of four. Described comparator structure includes interconnection of locally available logic cells that further avoid needs for large cell drivers. A comparison between the proposed scalable digital comparator architecture and conventional comparator design has also been reported in which it is observed that parallel-prefix tree based comparator design approach offers improvements in power efficiency and operating speed in addition with the regular reconfigurable VLSI topology.

Boppana *et al.* [35] suggested low power and area efficient 64-bit digital comparator implemented using radix-4 tree structure. The described comparator architecture based on the multiple threshold voltage scheme consisting of MOS transistors with low thresh hold voltage in the critical path design and MOS transistors with regular threshold voltage at other areas of design. Author implemented 64 XOR-XNOR blocks in the proposed comparator architecture. The introduced design have advantages in terms of low power and area consumption as compared to other conventional design.

Comparator architecture based on reducing the dynamic activity and area consumption is introduced in [36]. The proposed architecture is based on the parallel prefix tree architecture and utilizes EX-OR-NOR gates as pre-encoder in the design. The introduced architecture consists of locally-arranged gate structure intended for reducing the parasitic capacitance in the circuitry. It has been discussed that reported comparator architecture offers improvements in the efficiency of the area and power consumption.

CHAPTER 3

PROPOSED N-BIT DIGITAL BINARY COMPARATOR ARCHITECTURE

In this chapter N-Bit digital binary comparator is proposed. Section 3.1 discusses the introduction to the comparator design methodology along with the proposed algorithm used for implementation of the N-bit digital binary comparator. The design principle of proposed N-bit digital binary comparator is presented in Section 3.2. Section 3.3 presents the proposed circuit description whereas Section 3.4 address the evaluations of area, power and operating speed.

3.1 DESIGN METHODOLOGY

The working principle of comparator architecture design is depicted in Figure 3.1(a), where the operands A and B have unequal MSB bits. On confronting the first unequal bits comparator ignores the comparison of bits present at the rest of the bit positions because the first unequal bit encountered is well sufficient to decide the outcome of the comparison between the two operands. According to this approach, only two outcomes are required to achieve the result as compared to the traditional method to find out all three comparison outcomes as depicted in Figure 3.1(b). Comparator design intended for comparing N-Bit operands, starts comparison from MSB bit, (N-1)th bit, and it proceeds towards comparison of (N-2)th bit, if and only if the MSB bits of the two operands are equal [5].

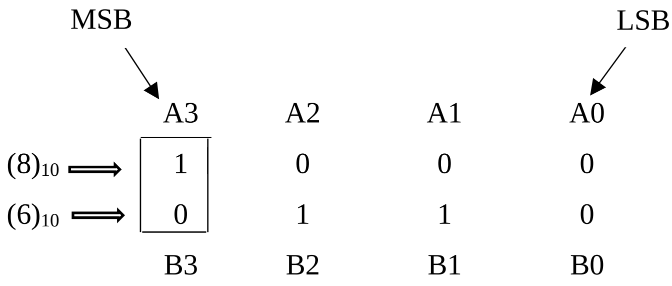

Figure 3.1(a) Comparison principle of the binary operands

Result			
A>B	1	0	0
A<B	0	1	0
A=B	0	0	1

Result			
A>B	1	0	0
A<B	0	0	1
A=B	0	1	0

Figure 3.1(b) Modification of the comparator design from traditional 3-bit output to encoded 2-bit output

As shown in Figure 3.2, the comparison process continues to compare the bit pair obtained from the operand until it gets an unequal pair of bits on its way towards the LSB bit position. The equal pair (E) and unequal pair (X) are realized as

$$X = A\,(XOR)B \tag{3.1}$$

$$E = A(XNOR)B = \overline{X} \tag{3.2}$$

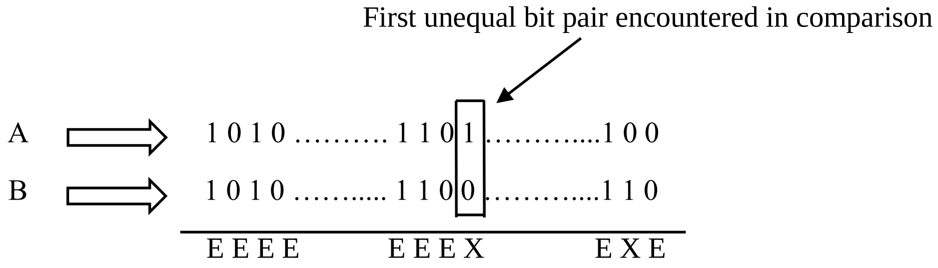

Figure 3.2 Comparison of N-bit operands

The comparison between two N-bit binary operands results into total of 2^{2N} comparison pairs. Out of these 2^{2N} comparison pairs the total number of comparison pairs that would result into "equal" comparison result would be 2^N. Therefore, the total number of comparison pairs resulting into "greater than" or "less than" comparison result can be obtained using total comparison pairs present and comparison pairs resulting "equal" output as shown in Table 3.1

TABLE 3.1 Total number of possibility exists for N-bit operands

Results of comparison	Total Number of results
Equal comparisons	2^N
Greater or less than comparisons	$\frac{2^{2N} - 2^{N}}{2}$

The flow chart of proposed algorithm used for the implementation of N-bit digital binary comparator is shown in Figure 3.3. The symbol notations and definition used for proposed algorithm and circuit are listed in Table 3.2. The two N-bit input operands A and B are taken for comparison and are checked if the operands are equal or not by performing bitwise comparison. If the result of comparison comes out as "equal" then the comparator drives the output logic AEB to logic one. If the comparison result of the operands does not come out to be equal then the pre-encoder (performs the encoding of unequal bits of the operands) output bits are checked from MSB to LSB for the corresponding output logic 1 (for example k^{th} bit is logic 1, where k varies from N-1 to 0). Comparator drives the AGB output logic to one or ALB output logic to one based on the results of pre-encoder. The suggested algorithm helps in reducing the insignificant switching activities that occur during comparison operation which further limits the dynamic power consumption of the comparator architecture. The total number of the active transistor as compared to the total transistors are also gets reduce due to implementation of the proposed algorithm.

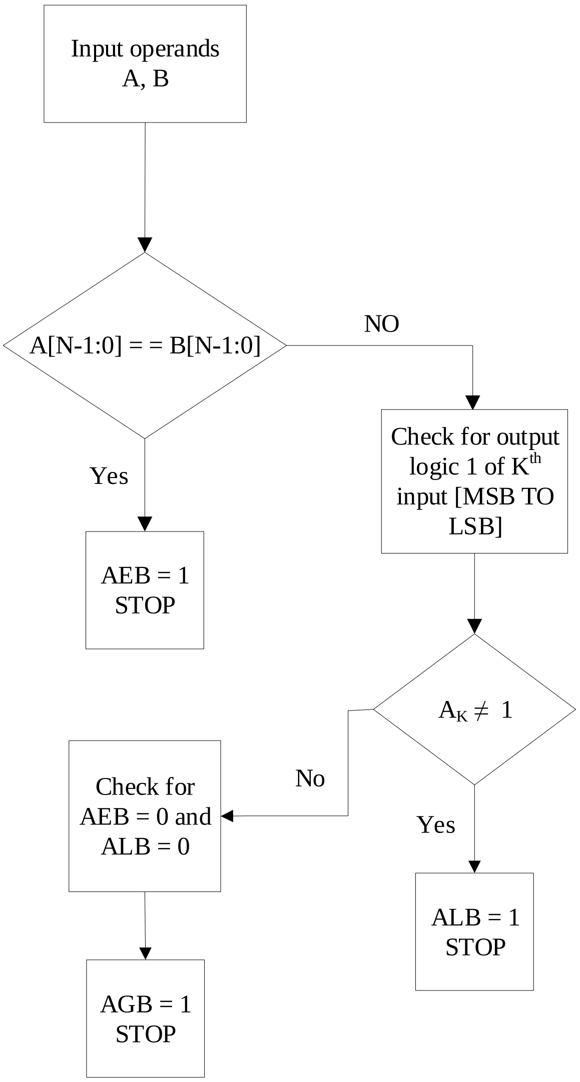

Figure 3.3 Flow chart of proposed N-bit digital binary comparator

Table 3.2 Symbol notation and definition

Symbol	**Definition**
N	Operand Bitwidth
A	First input operand
B	Second input operand
Π	Bitwise AND
Σ	Bitwise OR
COMP	Complement function
AGB	A is greater than B (in terms of magnitude)
ALB	A is lesser than B (in terms of magnitude)
AEB	A is equal to B (in terms of magnitude)
E	Representation of equal bitwise comparison
X	Representation of unequal bitwise comparison

The proposed comparator architecture based on the basic design principal that involves bitwise comparison. For example for two 4-bit operands, $A(A_3A_2A_1A_0)$ and $B(B_3B_2B_1B_0)$ using below mentioned Equations. “A greater than B”, “A less than B” and “A equal to B” are denoted by “AGB”, “ALB” and “AEB” respectively.

For 4-bit comparison

$$\mathrm{AGB} = \mathrm{A_3\overline{B_3} + R_3A_2\overline{B_2} + R_3R_2A_1\overline{B_1} + R_3R_2R_1A_0\overline{B_0}} \tag{3.3}$$

$$\mathrm{AEB} = \mathrm{R_3R_2R_1R_0} \tag{3.4}$$

$$\mathrm{A\overline{B} = A * S} \tag{3.5}$$

$$\mathrm{AGB} = \mathrm{A_3S_3 + R_3A_2S_2 + R_3R_2A_1S_1 + R_3R_2R_1A_0S_0} \tag{3.6}$$

Where $\mathrm{R = (AB) + (\overline{A} * \ \overline{B})}$

$\mathrm{S= (\overline{A}B) + (A\overline{B})}$

For N-bit comparison the Equations (3.3), (3.4) and (3.5) are generalised in Equations (3.7), (3.8) and (3.9), respectively.

$$\begin{aligned}\mathrm{AGB} = {} & \mathrm{A_{N-1}\overline{B_{N-1}} + R_{N-1}A_{N-2}\overline{B_{N-2}} + R_{N-1}R_{N-2}A_{N-3}\overline{B_{N-3}}} \\ & + \ldots\ldots + \mathrm{R_4(A_3\overline{B_3} + R_3A_2\overline{B_2} + R_3R_2A_1\overline{B_1}} \\ & \mathrm{+ R_3R_2R_1A_0\overline{B_0})}\end{aligned} \tag{3.7}$$

$$\mathrm{AEB} = \mathrm{R_{N-1}R_{N-2}R_{N-3}R_{N-4}} \ldots\ldots\ldots\ldots\ldots \mathrm{R_3R_2R_1R_0} \tag{3.8}$$

$$\begin{aligned}\mathrm{AGB} = {} & \mathrm{A_{N-1}S_{N-1} + R_{N-1}A_{N-2}S_{N-2} + R_{N-1}R_{N-2}A_{N-3}S_{N-3}} \\ & + \ldots\ldots\ldots\ldots + \mathrm{R_{N-1}R_{N-2}R_{N-3}} \ldots\ldots.. \mathrm{R_5R_4(A_3S_3} \\ & \mathrm{+ R_3A_2S_2 + R_3R_2A_1S_1 + R_3R_2R_1A_0S_0)}\end{aligned} \tag{3.9}$$

3.2 CIRCUIT DESCRIPTION

The circuit description of N-bit digital comparator is presented in this section. For performing comparison between two N-bit binary operands the proposed comparator structure is divided into two separate modules named as comparison evaluation module and final module. These modules serve as the high level and low level architecture of the proposed comparator. The comparison evaluation module incorporates parallel prefix tree structures that is intended for performing bitwise comparison of two N-bit operands A and B depicted by A_{N-1}, $A_{N-2}, \ldots\ldots\ldots, A_0$ and $B_{N-1}B_{N-2} \ldots\ldots.B_O$. The triggering of comparison logic's computation only happens if all the bits of greater significance are equal during the asynchronous bitwise comparison performed by the comparison evaluation module from MSB to the LSB of the operand. On coming across the most significant unequal bits of the operands, termination operation on the subsequent bitwise comparison takes place which results into reduction of the delay and power consumption of the circuit. The output from the comparison evaluation module would serve as the input to the final module. The final module establishes the final comparison on the basis of results obtained from the comparison evaluation module. The complete process of comparison is divided into five Sets. All the Sets in the design are placed in four hierarchal prefixing order according to their functionality therefore, output of each Set in this approach serves as the input to the other Set with an exclusion of Set 1 whose outputs act as the input to Sets 2 and 3.

In Set 1, bitwise comparison of two N-bit operands is carried out by the novel EX-OR-NOR cell. The proposed structure for EX-OR-NOR cell is shown in Figure 3.4, which is based on the pass transistor logic and the CMOS logic.

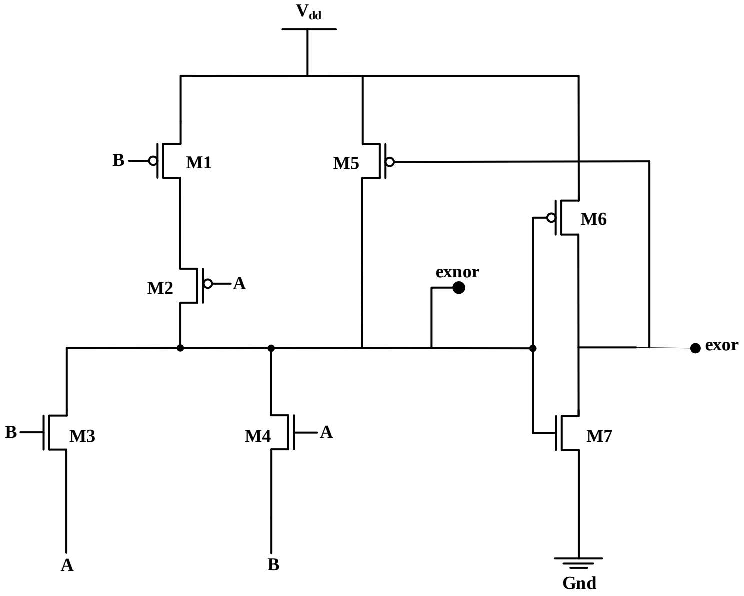

Figure 3.4 Novel EX-OR-NOR

The proposed structure of EX-OR-NOR logic cell consists of 7 transistor generating EX-OR and EX-NOR outputs as compared to conventional 8 transistors model [35]. The proposed structure is used in Set 1 aims towards enhancement in terms of area, power and speed performance of the comparator architecture. Optimal design of these 7 transistors consisting of 4 PMOS and 3 NMOS transistors named as M1-M7 is carried out to avoid the universal drive constraint faced by the pass transistor logic. The novel structure consists of the PMOS transistor in the feedback topology to maintain the logic level on the EXNOR output pin and the CMOS logic to boost up the output for achieving the full voltage swing on the EXOR output pin. Set 1 will be used as the part of pre-encoder in the proposed circuit implementation and the outputs from the Novel logic cells present in this Set is responsible for providing the termination and comparison bits intended for Set 2 and Set 3 structures. These cells conduct as follows (where k is in the range of 0 ≤ k ≤ N-1)

$$\mathrm{SET\ 1:\ T_K = A_K \odot B_K} \tag{3.10}$$

$$\mathrm{SET\ 1:\ D_K = A_K \oplus B_K} \tag{3.11}$$

Where, T_k and D_K indicate the equal and unequal bit pair resulting from the bitwise operation on the each bit pair of the operands A and B.

Set 2 comprises of cells, which operates on the Termination bits (T_k) obtained from Set 1 as input. The logic cells present in Set 2 combines the termination bits obtained from the nibble-partitions (partition intended for the comparison of every 4 bits of the operands starting from the MSB) present in Set 1 and the output obtained from the preceding logic cells present in the same level of Set 2 by using AND-logic. Logic cells present in Set 2 control the comparison activity performed by Set 3 because the outputs evaluated by Set 2 control the triggering of the next subsequent partition present in Set 3. Comparison request from the Set 2 originates if and only if all the results obtained from the bitwise comparison performed by preceding cells in Set 1 are “equal” otherwise initiation of termination bits takes place. For 0 ≤ m ≤ (N/4) – 1 and 0 ≤ L ≤ m, Set 2 operation is depicted mathematically as follows

$$\mathrm{SET\ 2:\ C_{2,m}} = \prod\left(\left(\prod_{\mathrm{K=4m}}^{\mathrm{4m+3}}(\mathrm{A_K \odot B_K})\right)\mathrm{E_L}\right) \tag{3.12}$$

Where, $\mathrm{C_{2,m}}$ and $\mathrm{E_L}$ represents AND type logic cells and equal flag in Set 2.

Set 3 includes cells which combine the output obtained from Set 1 as shown in Figure 3.5. In each partition of this Set the number of inputs of the cells increase, ascending from left to right for each cell in their respective partition and end with the maximum Fan-in of six. The combination of Set 1 and Set 3 architectures form the pre-encoder structure. Termination bits from the proposed EX-OR-NOR gates of Set 1 and output bits obtained from the logic cells of Set 2 allow the termination of the subsequent bitwise comparison activity of the logic cells present in Set 3 accordingly as result of coming across the first most significant unequal bits of the referred operands taken for comparison. The output achieved from Set 3 have at most one bit as logic zero indicating presence of unequal bits otherwise remaining bits maintained at logic one. Computation of cells present in each partition of Set 3 can be depicted as follows

$$\mathrm{C_{m,1} = COMP}\left(\prod_{\mathrm{m=0}}^{\left(\frac{\mathrm{N}}{4}-1\right)} \mathrm{E_m A_{4m+3} D_{4m+3}}\right) \tag{3.13}$$

$$\mathrm{C_{m,2}} = \mathrm{COMP}\left(\prod_{\mathrm{m}=0}^{\left(\frac{\mathrm{N}}{4}-1\right)} \mathrm{E_m A_{4m+2} D_{4m+2} T_{4m+3}}\right) \tag{3.14}$$

$$\mathrm{C_{m,3}} = \mathrm{COMP}\left(\prod_{\mathrm{m}=0}^{\left(\frac{\mathrm{N}}{4}-1\right)} \mathrm{E_m A_{4m+1} D_{4m+1} T_{4m+3}\, T_{4m+2}}\right) \tag{3.15}$$

$$\mathrm{C_{m,4}} = \mathrm{COMP}\left(\prod_{\mathrm{m}=0}^{\left(\frac{\mathrm{N}}{4}-1\right)} \mathrm{E_m A_{4m} D_{4m} T_{4m+3}\, T_{4m+2} T_{4m+1}}\right) \tag{3.16}$$

where $C_{m,1}$, $C_{m,2}$, $C_{m,3}$ and $C_{m,4}$ represent outputs of NAND type logic cells for mth partition of set 3

Set 4 contains NAND type of logic cells which receives the input from Set 3. The results from this Set will be in such a way that the output will contain at most one bit as logic 1 in case of dissimilar bits, while remaining bits remain at logic zero. There will be total $\log_4(N)$ cells present in Set 4 that combines the output acquired from each partition of Set 3. The complete operation can be represented as

$$\text{Set 4} : \mathrm{G_m} = \mathrm{COMP}\left(\prod_{\mathrm{m}=0}^{\left(\frac{\mathrm{N}}{4}-1\right)} \mathrm{C_{m,1}} \mathrm{C}_{m,2} \mathrm{C_{m,3} C_{m,4}}\right) \tag{3.17}$$

where, $\mathrm{G_m}$ represents output from each the logic cell in Set 3 and Set 4.

Set 5 contains NOR logic cells for reaching to the final conclusion of the parallel binary comparator. Cells in this Set obtain their inputs from Set 4 and Set 2. NOR gate structure first lead to result indicating the first operand lesser than second operand, which is represented by ALB. The final output is then realised with the help of NOR operation between ALB and AEB. The computation performed in Set 5 is represented as follows

$$\text{Set 5} : \ \mathrm{ALB} = \mathrm{COMP}\left(\sum \mathrm{G}_{\left(\frac{\mathrm{N}}{4}\right)-1} \ldots.\mathrm{G_0}\ \ \mathrm{AEB}\right) \tag{3.18}$$

$$\text{Set 5} : \ \ \mathrm{AGB} = \mathrm{COMP}\left(\sum (\mathrm{ALB})\, (\mathrm{AEB})\right) \tag{3.19}$$

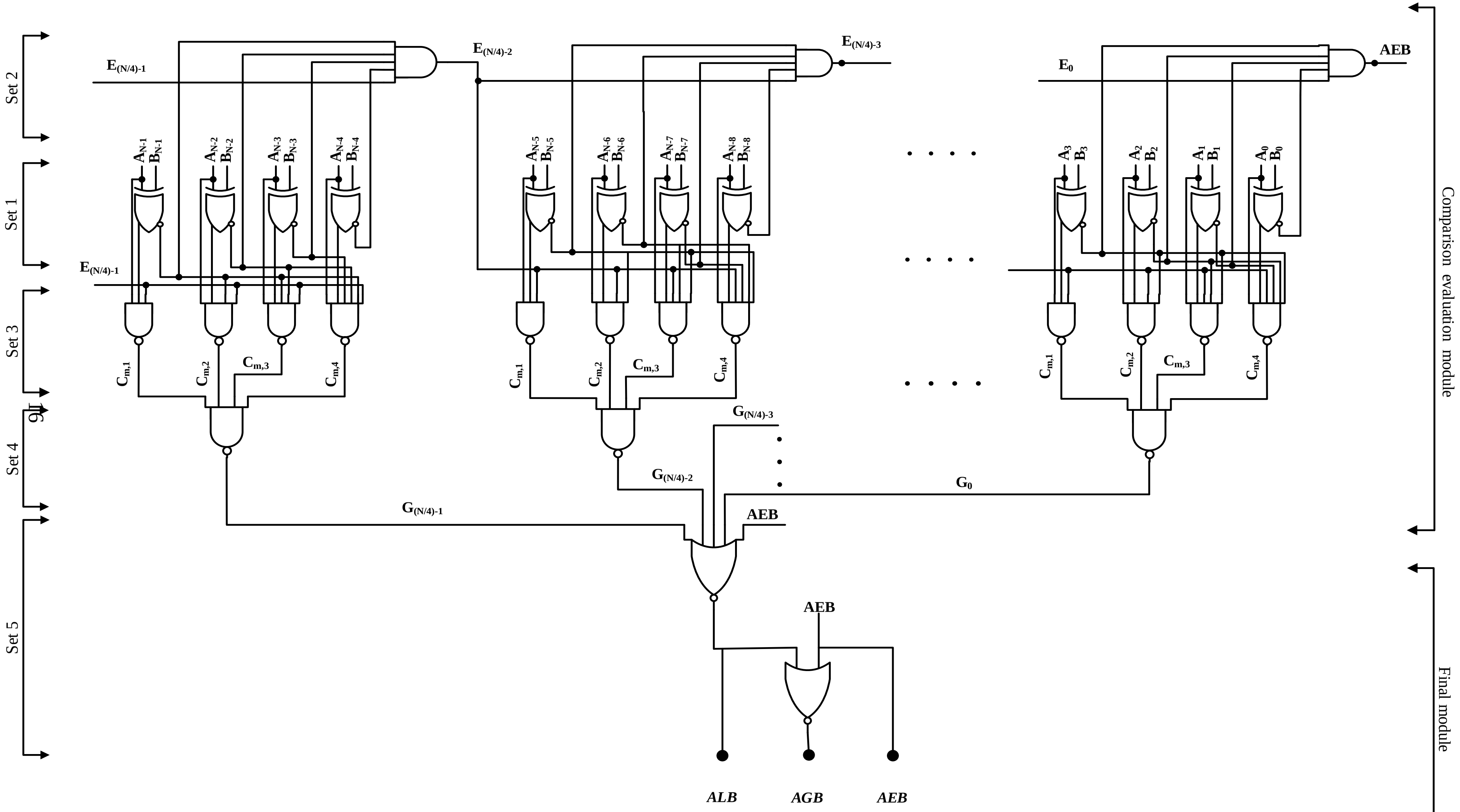

Figure 3.5 Proposed N-bit parallel binary comparator.

3.3 CIRCUIT ARCHITECTURAL OVERVIEW

To explain the process of proposed methodology two input operands as A=10101010 and B=10011001 are chosen for 8-bit comparison and the pictorial view of the process is illustrated in Figure 3.6. All the operations are divided into five Sets. Set 1, includes bitwise comparison of input operands for the examination of equal and unequal bit pairs, respectively. In this example, the operands taken for the comparison have bit pairs A7=1 & B7=1 and A6=0 & B6=0 as equal bit pairs while the third bit pair A5=1 & B5=0 as the most significant unequal bit pair.

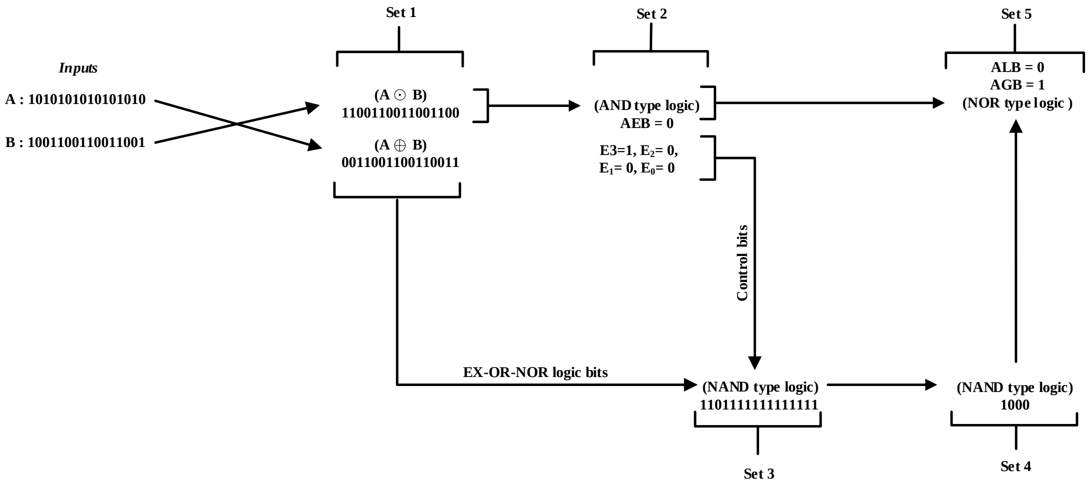

Figure 3.6 4-bit comparison using proposed N-bit digital binary comparator

Parallel execution of Set 2 and Set 3 take place simultaneously, as the logic cells present in Set 2 examines the presence of equal bit pairs in the respective operands and results into AEB = 0 due to the bitwise logical AND operation. Set 3 keeps check on the corresponding unequal bit pairs of the operands and results into 11011111 as the output bit stream with atmost one zero that depicts the presence of most significant unequal bit pair in the operands.

Set 4 comprises of NAND type of logic cells that combines each nibble into one bit, obtained from the Set 3 referenced from MSB as 1101 and 1111. The resultant pattern of bits obtained from Set 4 consists of at most one logic one bit depicted as “10”.

Finally, Set 5 comprises of NOR type logic cells that acquires the input bit pattern from Set 4 and Set 2 for the attainment of final decision. In this example, operand A is greater than B so comparator architecture drives the AGB= “1” and ALB= “0” while keeping AEB= “0”.

3.4 POWER, SPEED AND AREA EVALUATIONS

The analysis of power requirement, area (in terms of number of transistors), operating speed and number of logic levels requirement of the proposed structure of N-bit digital comparator based on the CMOS logic gates is presented in this section.

3.4.1 Area analysis

Area analysis of the proposed comparator architecture is done by estimating the total number of cells required in the different Sets and then the logic cell count translated into total number of transistors used in the designing of N-bit comparator architecture. Based on Equations (3.10)-(3.16), the total number of logic cells required by the comparison evaluation module (C_{CEM}) and the final module is illustrated by following Equation:

$$C_{CEM} = (N\ X\ (\ SET\ 1\ CELL)) + (\ N/4\ \ X\ (SET\ 2\ CELL)) + (N\ \ X\ (SET\ 3\ CELL)) + (\ N/4\ X\ (SET\ 4\ CELLS)) \tag{3.20}$$

$$C_{FM} = (2\ X\ (SET\ 5\ CELL)) \tag{3.21}$$

According to various bitwidths, the total number of cells and levels required in each Set is depicted in Table 3.3. The number of transistors per cell calculated using number of cells given in Table 3.3 for different bitwidths are listed in Table 3.4. An approximate linear growth is observed in the result illustrating comparator size as a function of bitwidths.

TABLE 3.3 Total number of logic cells present at each Set for various comparator bitwidths

Comparator Bitwidth	Set 1		Set 2		Set 3		Set 4	
	Cells	Levels	Cells	Levels	Cells	Levels	Cells	Levels
16-b	16	1	3	1	16	1	4	1
32-b	32	1	7	1	32	1	8	1
64-b	64	1	15	1	64	1	16	1
128-b	128	1	31	1	128	1	32	1
256-b	256	1	63	1	256	1	64	1

TABLE 3.4 Total number of transistors for different comparator bitwidths

Comparator Bitwidth	**Transistor Counts**				
	Set 1	**Set 2**	**Set 3**	**Set 4**	**Total**
16-b	16 x 7	3 x 12	16 x 12	4 x 8	372
32-b	32 x 7	7 x 12	32 x 12	8 x 8	756
64-b	64 x 7	15 x 12	64 x 12	16 x 8	1524
128-b	128 x 7	31 x 12	128 x 12	32 x 8	3060
256-b	256 x 7	63 x 12	256 x 12	64 x 8	6132
512-b	512 x 7	127 x 12	512 x 12	128 x 8	12276

3.4.2 Operating speed

The critical path delay of the proposed design is examined by taking into account the behaviour of the circuit on application of the critical N-Bit inputs. Critical delay is the summation of all the cells delay that come across in the critical path. The critical delay originated from the logic cells present in the Set 1 under Comparison Resolution Module to the logic cell present in the Set 5 under final Module. The total encountered delay in the critical path would become the applicable minimum time period of the input which further decides the maximum operating frequency of the design. Total critical path delay of the comparison evaluation module can be described through the mathematical representation, illustrated as below

$$D_{CEM} = D_{SET\ 1} + D_{SET\ 2} + D_{SET\ 3} + D_{SET\ 4} \tag{3.22}$$

Where D_{CEM} represents the total critical path delay in the comparison evaluation module.

All terms mentioned in equation 3.22 possess the single delay cell except the second term on R.H.S, resulting in

$$D_{CEM} = D_U + (N/4)\, D_U + D_U + D_U \tag{3.23}$$

where D_U represents the single activated cell delay in the respective Set.

The delay D_{FM} due to final module is illustrated as follows:

$$D_{FM} = 2\, D_U \tag{3.24}$$

The total delay of the proposed N-Bit digital comparator evaluated from input to the output is given by

$$D_T = D_{CEM} + D_{FM} \tag{3.25}$$

Using Equations (3.23) and (3.24), we get

$$D_T = 5D_U + (N/4)D_U \tag{3.26}$$

From Equation (3.26), it is evident that proposed N-Bit digital binary comparator has minimum delay than the similar comparator structures reported in the literature.

3.4.3 Power Requirements

In the most of the digital circuits, power dissipation arises due to dynamic switching activity in the design. As a result, minimizing the switching activities is the vital key for reduction of overall average power dissipation of the modern low power designs. In the proposed design, the switching activities are reduced using termination of the subsequent bitwise comparison process of the logic cell.

No power saving provided by the logic cells contained in Set 1, since the operands simultaneously initiates all the logic cells present in this level. As shown in Table 3.4, the total number of transistors present in Set 1 of the design constitutes 30% of the total transistors for 16-bit comparison.

Logic cell present in Set 2 undergoes through the selective activation except the most significant partition which remains always active. The subsequent partition of Set 2 is activated only if the bitwise comparison results of all the bits of greater significance are equal. Hence, if the bitwise comparison results of the operands in most significant partition of Set 1 came out to be equal then only the comparison request is sent to the next subsequent partition present in this Set, else no gate activity will occur in this Set. As Set 2 encompasses smallest number of logic gates necessary for reaching on the final comparison outcome, it accounts only 9.6% for 16-bit comparison of total switching activity in worst case scenario.

Set 3 integrates the comparison outcomes of all the preceding partition in this level and the intermediate results are further used for the activation or deactivation of the cell at specific bitwise positions. Therefore, only one cell in Set 3 undergoes through the switching activity, resulting into significant reduction in the power dissipation. Table 3.4 shows that Set 3 accounts for 51.6% of total transistors for 16-bit comparisons however, as only one logic cell in present in Set 3 will be active, Set 3 accounts only 3.2% of total transistor switching activities. Although this present share decreases as the comparison bitwidths increases further.

The single active logic cell from Set 3 further triggers subsequent logic cell present in the Set 4. Thus only one cell in Set 4 will be active, which leads to additional reduction in power dissipation. Set 4 accounts for 8.6% of total transistor for comparator structure comparing 16-bit operands and thus accounts for only 2.1% of total transistor switching activity. However, this share will decrease as the comparison bitwidths increases further.

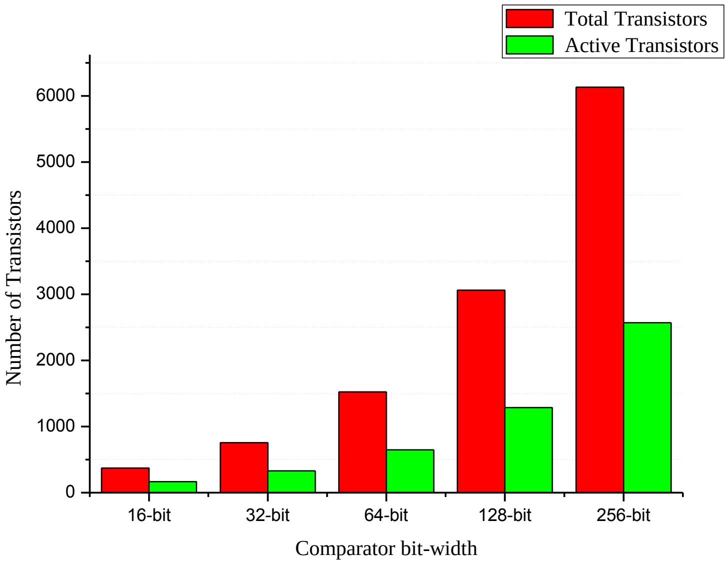

Figure 3.7 Number of active transistors for various comparators bitwidths

Worst case cell activities of the proposed comparator occur when the operands entitled with values $A = 0000 \ldots .01$ and $B = 0000 \ldots .00$ (or vice versa). The graphical plot between number of transistors and their corresponding comparison bitwidths is depicted in Figure 3.7. The red and green coloured bars show that total number of transistors and total number of active transistors, respectively. For each comparison bitwidths, total number of transistors used in the design is shown by the first bar and the total number of active transistors required for achieving the comparison outcomes is represented by the second bar. It has been noticed that the less than half of the transistors are active for each comparator bitwidths thus initiating significant reduction in power consumption. Therefore, the proposed design is competitive with other low power digital comparator structures in conjunction with scalability and operating speed achieved.

CHAPTER 4

SIMULATION RESULTS

The proposed N-bit digital comparator has been designed and simulated using Cadence virtuoso design environment with 0.18 μm- gpdk digital CMOS technology. For the realisation of the worst case delay for the proposed design we have applied the input operands that would activate the maximum number of cells in each Sets, which also includes the least significant cells (referring to condition where all the input bits of the operands are equal, except the least significant bits). On behalf of achieving the optimization with respect to the operating speed of the design, the minimum channel length is used for both NMOS and PMOS is 0.18 μm.

The proposed N-bit digital comparator uses minimum number of transistors for wide bitwidths comparison and Figure 4.1 shows the plot depicting the comparison in terms of number of transistors used in the proposed design with the other comparator architectures reported in the literature [23, 25, 29, 32, 34, 36, 37].

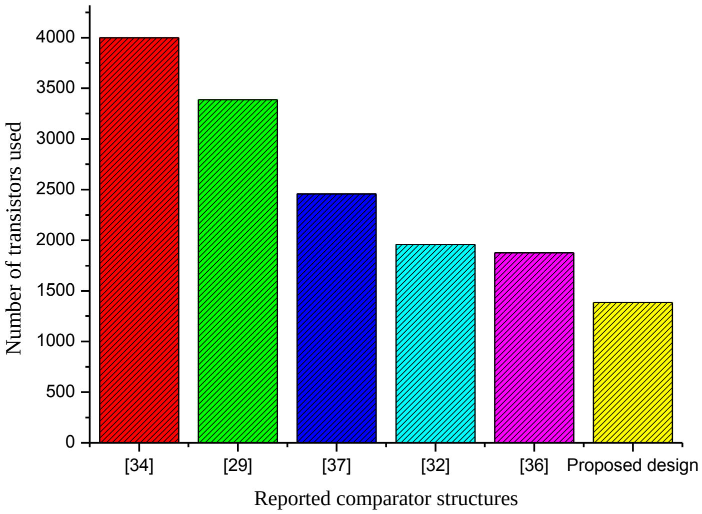

Figure 4.1 Transistors used for 64-bit comparator structures available in literature

The DC transient characteristics for the various comparator bitwidths on application of worst case operands (listed in Table 4.1) are shown in Figures 4.2, 4.3, 4.4, 4.5 and 4.6. The DC transient characteristics consist of waveforms depicting the maximum delay occurred in the input to output flow. From the Figures it is evident that the maximum delays for 4-bit, 8-bit, 16-bit, 32-bit and 64-bit comparator circuits are 0.2957 ns, 0.3184 ns, 0.376 ns, 0.476 ns and 0.573 ns, respectively. The waveforms obtained at the output ports AGB, ALB and AEB with full voltage swing of 1.8 V corresponds to the application of worst case input operands.

Table 4.1 Worst case operands for different comparator bitwidths

Comparator bitwidths	Worst case operand
4-bit	A = 0000 & B = 0000 A = 0001 & B = 0000 A = 0000 & B = 0001 A = 0001 & B = 0001
8-bit	A = 00000000 & B = 00000000 A = 00000001 & B = 00000000 A = 00000000 & B = 00000001 A = 00000001 & B = 00000001
16-bit	A = 0000….0000 & B = 0000….0000 A = 0000….0001 & B = 0000….0000 A = 0000….0000 & B = 0000….0001 A = 0000….0001 & B = 0000….0001
32-bit	A = 0000….0000 & B = 0000….0000 A = 0000….0001 & B = 0000….0000 A = 0000….0000 & B = 0000….0001 A = 0000….0001 & B = 0000….0001
64-bit	A = 0000….0000 & B = 0000….0000 A = 0000….0001 & B = 0000….0000 A = 0000….0000 & B = 0000….0001 A = 0000….0001 & B = 0000….0001

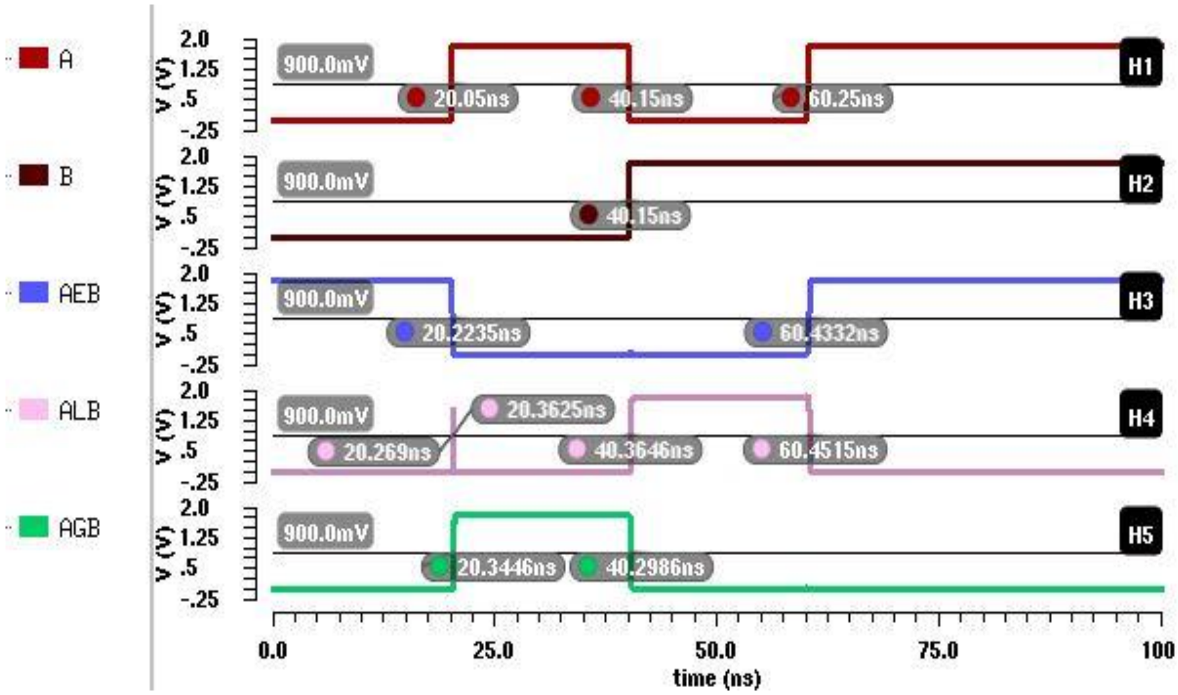

Figure 4.2 DC transient characteristics of proposed 4 bit digital comparator

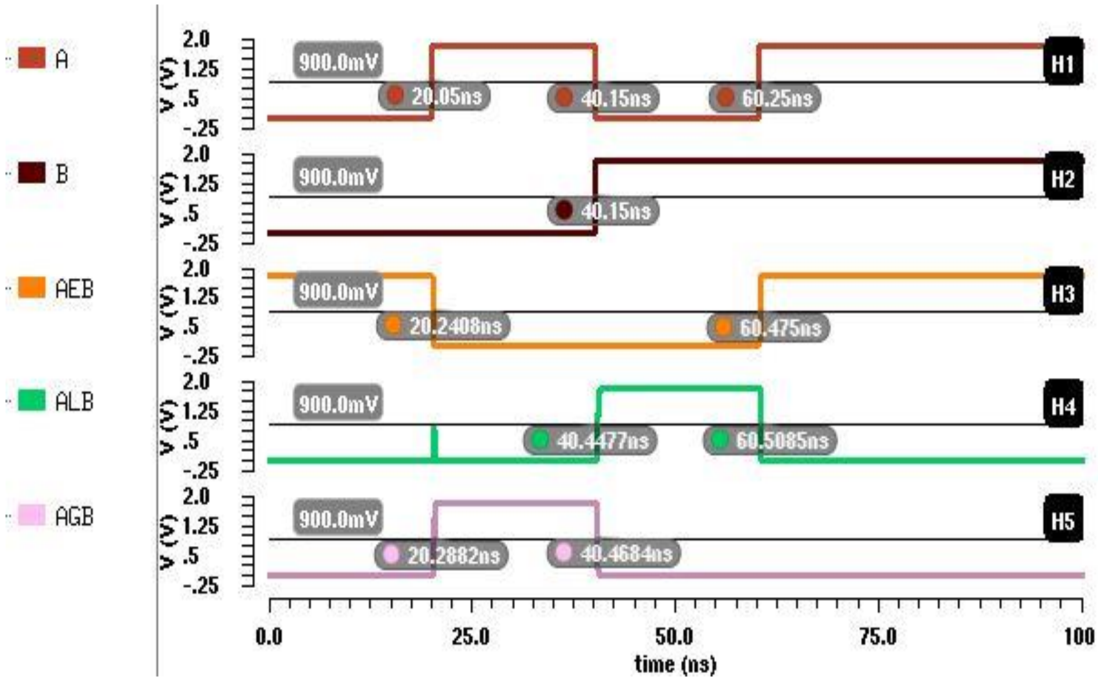

Figure 4.3 DC transient characteristics of the proposed 8 bit digital comparator

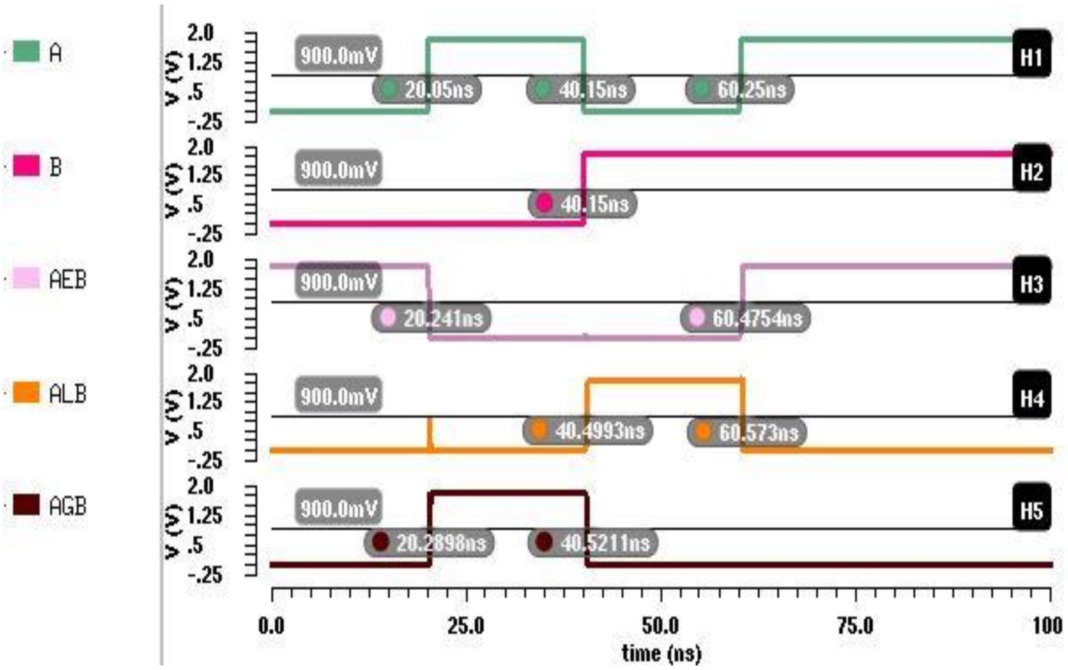

Figure 4.4 DC transient characteristics of proposed 16 bit digital comparator

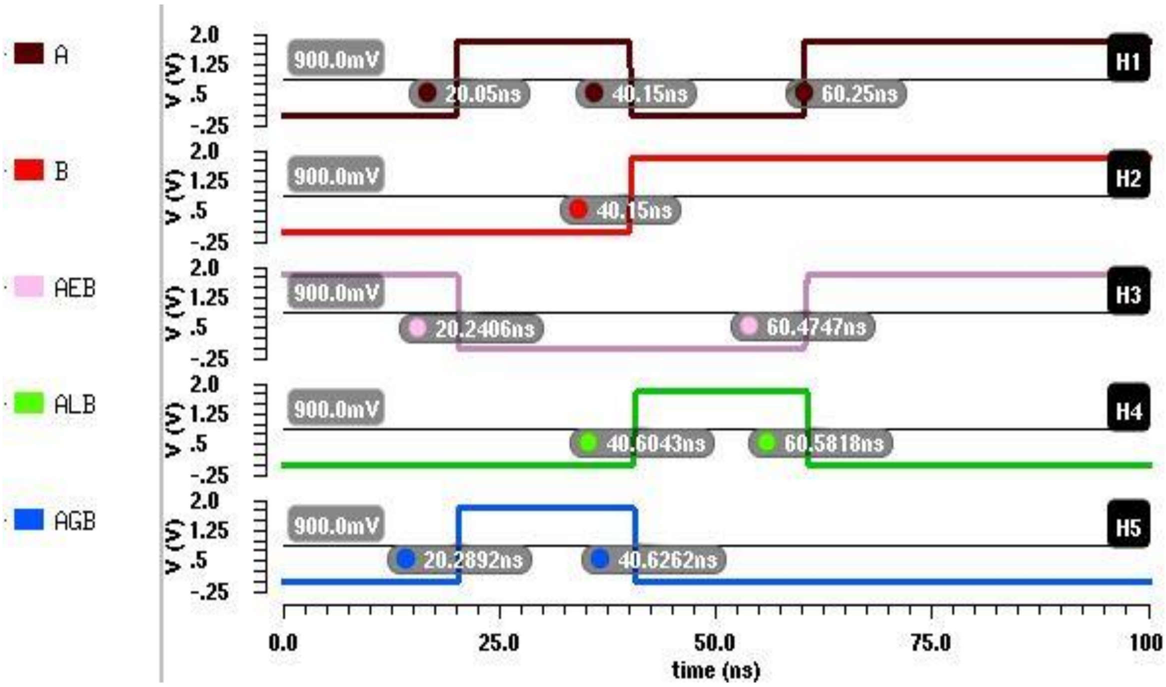

Figure 4.5 DC transient characteristics of proposed 32 bit digital comparator

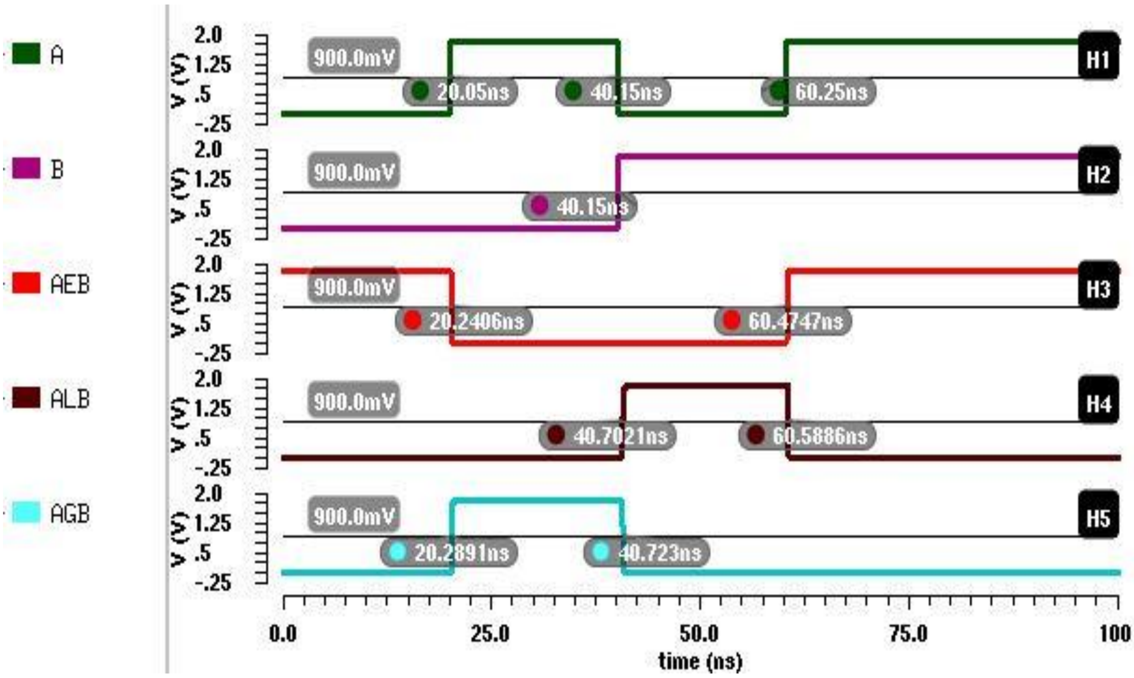

Figure 4.6 DC transient characteristics of proposed 32 bit digital comparator

Figure 4.7 depicts the maximum delay encountered in input to output flow versus the respective input operands bitwidths for the proposed comparator circuit. The results obtained from the simulation closely relate with the analytical model that was presented in Table 3.4, illustrating the increase in the gate levels according to ((N/4) + 5)

According to Figure 4.7, the proposed comparator design have maximum 0.57 ns of input-output delay in the worst case scenario. Therefore, the proposed design can have the maximum operating speed of 1.75 GHz which makes the proposed design as fastest comparator among the existing similar comparator structures.

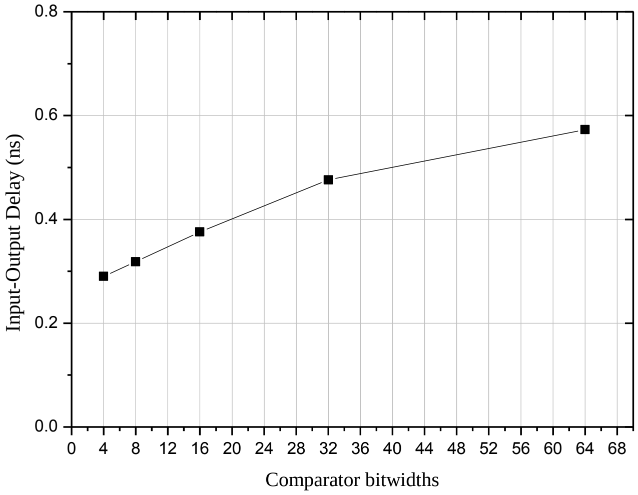

Figure 4.7 Maximum input-output delay versus input bitwidths for the proposed comparator

Figure 4.8 shows the maximum power dissipation versus number of bits required for evaluation by the proposed 64-bit comparator operating at 1 GHz to reach the desired result. For instance, in the course of comparison between the two operands having values 1111...11 and 0111…11, only one bit is required to declare the result of comparison. As estimated, the power dissipated by the proposed structure is always lower than that of the reported structures [34, 36]. As observed even for the wider bit operands, limited amount of leakage power dissipation (in nanowatt) will be experienced in the design.

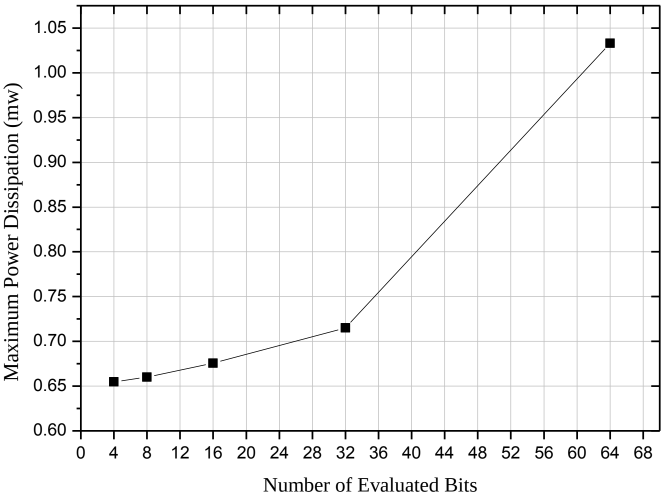

Figure 4.8 Maximum power dissipation in design versus number of evaluated bits for reaching to the comparison result of 64-bits inputs at 1GHz

Various state-of-the-art implementations of the digital comparator architecture [23, 25, 29, 32, 34, 36, 37] whose structures are based on the recent reported topologies which are aimed for the power saving along with achieving high speed operation are compared with the proposed comparator architecture and listed in Table 4.2. From the table, it can be seen that the proposed comparator structure has low power dissipation and high operating speed. The circuit also offers an additional advantage of minimum area in terms of number of transistors. The all three advantages of the proposed structure make it suitable for the applications that require minimum transistor count, power efficient architecture along with evaluation of low average number of operand bits carried out for reaching the final decision.

Table 4.2 Simulation and reported results for various 64-bit comparator design

Comparator Type	**Technology/ Power supply**	**Transistor Count/Comparator Bitwidth**	**Power Dissipation**	**Delay(ns)**	**Remarks**
Proposed (static type)	0.18 μm /1.8 V	1384/64-b	1.03 mW at 1GHz (64-b)	0.57 (64-b)	1) Optimized structure in terms operating speed, power dissipation and area
Hafeez *et al.* [34](static type)	0.15 μm/1.5V	4000/64-b	7.76 mW at 1 GHz (64-b)	0.86 (64-b)	1) High transistor count 2) limited power efficiency
Hensley *et al.* [23] (static type)	0.18 μm /1.8 V	624/24-b	5.23 mW at 100 MHz (24-b) 0.735 μW/MHz	4.16 (24-b)	1) Very slow
Perri *et al.* [32] (static type)	0.35 μm/3.3 V	1960/64-b	24 μW/MHz (64-b)	1.73 (64-b)	1) Supports only “greater than” or “less than” operation 2) high transistor count
Lam *et al.* [29]	0.35 μm/3.3 V	3386/64-b	14.2 mW at 200 MHz 42 μW/MHz	2.82 (64-b)	1) heavy clock loading along with substantial number of gated transistor 2) limited power efficiency
Kim *et al.* [25]	0.18 μm/1.8 V	964/32-b	2.53 mW at 200 MHz 12.65 μW/MHz	1.12 (32-b)	1) heavy loading of dynamic clock with gated number of transistors 2) limited operating speed
Chua *et al.* [36]	0.18 μm/1.8 V	1875/64-b	3.8 mW	0.88 (64-b)	1) Area extensive design for wide operands 2) restricted power proficiency and operating speed
Cadence [37]	0.35 μm/3.3 V	2456/64-b	17.54 mW at 200 MHz 34 μW/MHz	1.93 (64-b)	1) excessive power dissipation in tree structure 2) Area extensive design with limited power efficiency.

CHAPTER 5

CONCLUSION AND FUTURE SCOPE

An area efficient N-bit digital comparator structure with high operating speed and minimal power dissipation is presented in this work. The proposed comparator structure consists of two separate modules. The first module is the comparison evaluation module and the second module is final module. Independent from the input operands bitwidths, stages present in comparison evaluation module involve regular structure of repeated logic cells used for implementing parallel prefix structure. The final module validates the final comparison on the basis of results obtained from the comparison evaluation module. Presence of regularity in the proposed architecture further facilitates the characteristic determination of any arbitrary sized comparator.

The proposed comparator structure comprises of parallel prefix tree structure responsible for parallel bitwise comparison starting from MSB to LSB bits of the input operands. Simulation results with standard CMOS transistor cells for the proposed 64-bit comparator architecture show the maximum operating speed of 1.75 GHz. Further, simulation results confirm the power efficiency of the proposed comparator structure, with limited worst case power dissipation of 1.03 mw/GHz achieved through 1384 of total number of transistors. For attaining further optimization in terms of power dissipation in the design, future work expected to include additional circuit optimizations by adapting dynamic implementations for the comparison evaluation module together with high speed one detection logic circuit intended for final module. Operation of two modules consisting in the design could be performed by using pipelining approach, to efficiently increase the comparison throughput at the expenditures of area and the power consumption.

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