Design and Control of Grid Connected Photovoltaic System

A Thesis submitted in fulfillment of the requirements for the award of the degree of

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Submitted By

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CERTIFICATE

I hereby certify that the work which is being presented in the Thesis entitled, ***"Design and Control of Grid Connected Photovoltaic System"*** in fulfillment of the requirement for the award of the Degree of ***Doctor of Philosophy*** submitted in the ***Electrical & Instrumentation Engineering Department*** of the **Thapar Institute of Engineering & Technology** is an authentic record of my own work carried out under the supervision of **Dr. Sanjay K. Jain** and **Dr. Krishna Kumar Gupta** and refer other researcher's work, which are duly listed in the reference section.

The matter presented in this Thesis has not been submitted for the award of any other degree of this or any other University.

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.....dedicated to

My parents

My sisters ***Ohm & Rashmi***

Brother ***Nakshatra Singh***

Abstract

Renewable Energy Systems (RESs) are poised to address the concerns arising due to excessive usage of depleting fossil fuels and global warming. Among various renewable resources namely wind, solar, fuel cells, and hydro; solar energy is being harnessed prominently because it is freely available, does not involve moving parts, and can be placed near the load centers. However, the *Photovoltaic (PV)* source is characterized by intermittent output and wide operating range and therefore requires power converters or *Power Conditioning Unit (PCU)* for grid interconnection. From the viewpoint of easy maintenance and cost-effectiveness, the grid-tied structure can be advantageous for the *PV* system as they do not use batteries for energy storage.

Different configurations of *PCUs* have been investigated for various *RESs*. The two-stage structure is generally used with *PV* systems having low and fluctuating output voltage. Such structure is usually operated utilizing a DC-DC converter to regulate the *PV* output voltage and maximize the output power, whereas the inversion process is achieved through an inverter. Traditionally, two-level *Voltage Source Inverter (VSI)* and *Current Source Inverter (CSI)* are widely used for grid integration. The *VSI* is a buck converter and requires an additional DC-DC boost converter to boost its DC-link voltage; while *CSI* is a boost converter and requires a DC-DC buck converter for buck operations.

The impedance source inverters, which characterize single-stage power converters, provide voltage boost ability within the inversion stage. This group of *PCUs* is poised to be a viable option in comparison to the two-stage arrangement for low and fluctuating voltage sources. The *Z-Source Inverter (ZSI)* is a single-stage topology proposed to overcome the shortcomings of *VSI* and *CSI*. However, *ZSI* provides a boost in single-stage but is not a preferable candidate for *PV* as it takes discontinuous current from the source. The *Quasi-Z-Source (QZS)* inverter, a modified form of *ZSI*, is suitable for *PV* systems because it draws continuous current from the source and has a low component rating.

The *QZS* inverter has attracted considerable attention in *PV* power generation applications because of single-stage power conversion, no dead time between switches of same bridge leg, the ability to handle wide DC voltage, and drawing continuous current. During the boost mode, the DC-link voltage of the *QZS* inverter pulsates between zero and maximum value. A strategy is proposed to indirectly control the *Peak DC-Link Voltage (PDV)* of the *QZS* inverter fed grid-tied *PV* system by sensing the voltages of *QZS* network capacitors. Consequently, a two-stage like control structure is discussed where the *Shoot-Through (ST)* duty ratio is used to regulate the DC-link voltage and AC-current is controlled to control active and reactive power injection into the grid. For the purpose, the AC- and DC-sides are modeled separately and the crossover frequency of the AC-side control loop is kept high to avoid intruding with the DC-side. A *Third-Order-Integral-Lead (TOIL)* controller is realized to regulate *PDV* and minimize the *Non-Minimum Phase (NMP)* characteristic effect of *ST* duty-ratio to *PDV* transfer function. A damped-*Second-Order-Generalized-Integrator (SOGI)* offering high power frequency gain is used to control the AC-side current and attain *Zero Steady-State Error (ZSSE)*. The performance of the proposed *TOIL* and damped-*SOGI* controllers is compared with other designed linear and *Sliding Mode Controller (SMC)*.

Grid integration of *PV* systems although leads to efficient utilization of generated power, the efficiency of the grid integration system depends essentially on the performance of the power conditioner and the capability of the adopted control strategies in achieving high performance. The topologies employed in interconnecting the *PV* system to the grid can be classified into single-stage or two-stage and two-level or *Multi-Level Inverters (MLIs)*. The *MLIs* are characterized by high power quality at the AC-side, reducing the filter size significantly, operating at higher voltage levels, and reducing switching losses. The *Three-Phase (*3-Φ*) Neutral-Point-Clamped (NPC)-QZS* inverter is set to become a potential candidate for renewable energy applications because it yields a continuous input current and voltage boost. A dynamic model has been developed to design the control strategy accurately of the 3-Φ *NPC-QZS* inverter. The proposed method includes the control of grid-tied current and the *PDV*. The control of grid-tied current is achieved through a damped-*SOGI*. The *PDV* is estimated indirectly from the voltages of *QZS* network capacitors and is regulated by an *Integral-Double-Lead (IDL)* controller. Two modified modulation techniques based on *Phase-Opposite Disposition (POD)* and *In-Phase Disposition (IPD)* are proposed to yield *ST* by injecting 3rd harmonics for *Maximum Constant*

Boost Control (MCBC). A comparison is drawn between the performance of the proposed controller and *SMC* on the DC-side.

Transformerless grid-tied inverters have been widely accepted in *RESs* applications owing to higher efficiency, relatively inexpensive, and compact design. The fundamental buck characteristic of the output voltage is the bottleneck. It requires a DC-DC boost converter, which causes an expensive performance for single-stage energy conversion. A novel single-stage transformerless *Switched Capacitor (SC)*-based inverter topology is presented to boost the input voltage value and limit the start-up and charging current problem through the *QZS* network between *PV* and *SC* inverter. Likewise, the insertion of the *QZS* network provides additional control freedom in terms of the *ST* duty ratio to regulate the DC-link voltage. Due to this hybridization, the size of inductors in the *QZS* network is reduced. Furthermore, to inject the AC-current to the grid, a damped-*SOGI* controller is utilized, which can control both the active and reactive power.

Large-scale solar *PV* systems encounter unpredictable *Partial Shaded Condition (PSC)*. The *PSC*, causing multiple peaks in the *Power–Voltage (P–V)* characteristics, potentially downgrades the performance of the *PV* system. However, it is recommended that the *PV* system should be operated at *Global Maximum Power Point (GMPP)* to extract maximum power and efficient utilization. The *Flying Squirrel Search Optimization (FSSO)*, a search and optimization algorithm, has been implemented in a real-time manner to track the *GMPP* for different *PSCs*. For an effective adoption with a much-reduced convergence time, the original *FSSO* is modified to update the squirrel position without the presence of the predator. An investigation of the proposed scheme is carried out employing a *QZS* converter. The proposed method yields higher tracking efficiency, non-oscillatory steady-state response, and lower transients. The performance of the developed *FSSO* algorithm under different shading conditions is compared with *Perturb and Observe (P&O)*, *Particle Swarm Optimization (PSO)*, and *Grey Wolf Optimization (GWO)* based algorithms to track the *GMPP*.

Keywords: AC-side controller, DC-side controller, Maximum power point tracking algorithm, Neutral-point-clamped, Quasi-Z-source inverter, Switched capacitor.

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Abbreviations

1-Φ	Single-Phase
2S2P	Two-Series & Two-Parallel
3-Φ	Three-Phase
4S	Four-Series
I–V	Current–Voltage
P–V	Power–Voltage
3L	Three-Level
5L	Five-Level
ACO	Ant Colony Optimization
ANN	Artificial Neural Network
BW	Bandwidth
BZSI	Bidirectional Z-Source Inverter
CCM	Continuous Conduction Mode
CHB	Cascaded H-Bridge
CMV	Common-Mode Voltage
CSI	Current Source Inverter
DCM	Discontinuous Conduction Mode
DE	Differential Evolution
DG	Distributed Generations
DSO	Digital Storage Oscilloscope
EBQZS	Extended Boost Quasi-Z-Source
EMI	Electromagnetic Interference
ESR	Equivalent Series Resistance
EZSI	Embedded Z-Source Inverter
FC	Flying Capacitor
FFT	Fast Fourier Transform
FS	Flying Squirrel

FSSO	Flying Squirrel Search Optimization
GM	Gain Margin
GMPP	Global Maximum Power Point
GW	Gigawatts
GWO	Grey Wolf Optimization
HC	Hill Climbing
HF	High Frequency
HIL	Hardware-In-The-Loop
IDL	Integral-Double-Lead
IGBT	Insulated-Gate Bipolar Transistor
IMP	Internal Model Principle
INC	Incremental Conductance
IPD	In-Phase Disposition
IRENA	International Renewable Energy Agency
ISI	Impedance Source Inverter
IZSI	Improved Z-Source Inverter
LCCT	Inductor-Capacitor-Capacitor-Transformer
LDST	Lower DC-Link Shoot-Through
LI	Lagrange Interpolation
LMPP	Local Maximum Power Point
MCBC	Maximum Constant Boost Control
MLI	Multi-Level Inverter
MPP	Maximum Power Point
MPPT	Maximum Power Point Tracking
NMP	Non-Minimum Phase
NOS	Near Optimum Solution
NPC	Neutral-Point-Clamped
NST	Non-Shoot-Through
OS	Optimum Solution

P	Proportional
P&O	Perturb and Observe
PAM	Pulse Amplitude Modulation
PCU	Power Conditioning Unit
PDV	Peak DC-Link Voltage
PI	Proportional-Integral
PID	Proportional-Integral-Derivative
PM	Phase Margin
POD	Phase-Opposite Disposition
PSC	Partial Shaded Condition
PSO	Particle Swarm Optimization
PV	Photovoltaic
PWM	Pulse Width Modulation
QZS	Quasi-Z-Source
RES	Renewable Energy System
RHPZ	Right-Half-Plane Zero
RMS	Root Mean Square
RS	Random Solution
RTS	Real-Time Simulation
SC	Switched Capacitor
SL	Switched Inductor
SMC	Sliding Mode Controller
SOGI	Second-Order-Generalized-Integrator
SP	Shading Pattern
ST	Shoot-Through
STATCOM	Static Synchronous Compensator
STC	Standard Test Condition
SVM	Space Vector Modulation
SZSI	Series Z-Source Inverter

THD	Total Harmonic Distortion
TL	Tapped Inductor
TOIL	Third-Order-Integral-Lead
UDST	Upper DC-Link Shoot-Through
UPF	Unity Power Factor
VSI	Voltage Source Inverter
WC	Weather Condition
ZSI	Z-Source Inverter
ZSSE	Zero Steady-State Error

Notations

Symbols

B_z	Boost factor
C	Capacitance of *QZS* network capacitor (F)
C_D	Drag coefficient
C_L	Lift coefficient
C_P	Terminal capacitance at *PV* output (F)
F_D	Drag force (N)
F_L	Lift force (N)
G	Actual irradiation (W/m^2)
$G_{dc0}^{pk}(s)$	DC gain of $G_{dc}^{pk}(s)$
$G_{dc}^{pk}(s)$	*ST* duty ratio to *PDV* transfer function
$G_{ac}(s)$	Transfer function for AC-side of the inverter
G_c	Gliding constant
$G_{ff}(s)$	Feed-forward compensator transfer function
G_n	Nominal irradiation (W/m^2)
$G_{vd}(s)$	*ST* duty ratio to *PV* voltage transfer function
I_M	Peak value of inverter current (A)
I_d	Diode current (A)
I_{phn}	Photo-current of *PV* module at the nominal condition (A)
I_{ph}	Photo-current of *PV* module at actual condition (A)
I_{rs}	Diode reverse saturation current (A)
I_{scn}	Short-circuit current at nominal condition (A)
I_{sc}	Short-circuit current at actual condition (A)
$K_{SOGI}^{Damp}(s)$	Damped-*SOGI* transfer function
$K_{ac}^{\alpha\beta}(s)$	$\alpha\beta$ component of AC-side controller transfer function

$K_{\mathrm{dc}}^{\mathrm{pk}}(s)$	*PDV* controller transfer function
K_{I}	Short-circuit current temperature coefficient (%/K)
K_{SP}, K_{SI}	Constants of damped-*SOGI* controller
K_{V}	Open-circuit voltage temperature coefficient (%/K)
$K_{\mathrm{ac}}(s)$	The AC-side controller transfer function
L	Inductance of *QZS* network inductor (H)
L_{f}	Inductance of AC-side filter inductor (H)
M	Modulation index
NT_{FS}	Number of normal tree *FSs*
N_{fs}	Number of *FSs*
N_{par}	Number of parallel connected *PV* modules
N_{ser}	Number of series connected *PV* modules
N_{se}	Number of series connected cells
$PM_{\mathrm{dc}}^{\mathrm{pk}}$	Phase margin for *PDV* control loop
P_{s}^{*}	Reference real power injection to grid (kW)
$P_{\mathrm{PV}}^{\mathrm{mx}}$	Maximum output power from *PV* source (kW)
P_{PV}	*PV* power output (kW)
P_{s}	Real power injection to grid (kW)
Q_{s}^{*}	Reference reactive power injection to grid (kVAr)
Q_{s}	Reactive power injection to grid (kVAr)
R	Load resistance (Ω)
RNT_{FS}	Randomly selected normal tree *FSs*
$R_{\mathrm{PV}}^{\mathrm{mx}}$	Resistance at *MPP* (Ω)
R_{C}	*ESR* of *QZS* network capacitors (Ω)
R_{L}	Winding resistance of *QZS* network inductors (Ω)
R_{PV}	*PV* resistance (Ω)
R_{f}	Winding resistance of AC-side filter inductor (Ω)
R_{se}	Series resistance of *PV* module (Ω)
R_{sh}	Shunt resistance of *PV* module (Ω)

S	Body surface area of *FS* (cm^2)
S_C	Seasonal constant
S_{min}	Minimum value of seasonal constant
T	Actual temperature (K)
$T_{dc}^{pk}(s)$	Closed loop transfer function for DC-side
$T_{ac}(s)$	Closed loop transfer function for AC-side
T_{nst}	*NST* time interval (s)
T_n	Nominal temperature (K)
T_{st}	*ST* time interval (s)
T_s	Switching time interval (s)
V	Velocity of *FS* (m/s)
V_{dc}^{av}	Average *PDV* (V)
V_{PV}^{mx}	Voltage corresponding to *MPP* of *PV* source (V)
V_{dc}^{pk}	Steady-state *PDV* (V)
V_{dc}^{*}	Reference DC-link voltage (V)
V_M	Peak AC-side terminal voltage of the inverter (V)
V_{ocn}	Open-circuit voltage at nominal condition (V)
V_{oc}	Open-circuit voltage at actual condition (V)
V_t	Thermal voltage at temperature T (V)
a	Parameter of *GWO* algorithm
$c_{1,max}$	Maximum cognitive rate
$c_{1,min}$	Minimum cognitive rate
c_1	Cognitive rate
$c_{2,max}$	Maximum social rate
$c_{2,min}$	Minimum social rate
c_2	Social rate
d_{st}^{at}	Duty ratio corresponding to acorn tree *FS* position
d_{st}^{ht}	Duty ratio corresponding to hickory tree *FS* position
d_{st}^{mn}	Minimum value of duty ratio

$d_{\mathrm{st}}^{\mathrm{mx}}$	Maximum value of duty ratio
$d_{\mathrm{st}}^{\mathrm{nt}}$	Duty ratio corresponding to normal tree *FS* position
d_{nst}, D_{nst}	Instantaneous and steady-state *NST* duty ratio
d_{st}, D_{st}	Instantaneous and steady-state *ST* duty ratio
f_{s}	Switching frequency (Hz)
g_{d}	Gliding distance (m)
h	Constant of $K_{\mathrm{dc}}^{\mathrm{pk}}(s)$
h_{g}	Height loss after gliding (m)
$i_{\alpha\beta}^{*}$	$\alpha\beta$ reference component of inverter current (A)
i_{Labc}	abc component of load current (A)
i_{L}, I_{L}	Instantaneous and steady-state *QZS* network inductor current (A)
i_{PV}, I_{PV}	Instantaneous and steady-state *PV* current (A)
i_{SCA}	Current through *SC* (A)
$i_{\alpha\beta}$	$\alpha\beta$ component of inverter current (A)
i_{abc}	abc component of inverter current (A)
i_{dc}, I_{dc}	Instantaneous and steady-state DC-link current (A)
i_{gabc}	abc component of grid current (A)
k	Iteration number
k_{b}	Boltzmann constant (J/K)
k_{m}	Maximum iteration number
$l_{\mathrm{dc}}^{\mathrm{pk}}(s)$	Loop gain for *PDV* control loop
$l_{\mathrm{ac}}(s)$	Loop gain for inverter current control loop
m_{abc}^{*}	abc component of third harmonic injected modulating signal
$m_{\alpha\beta}$	$\alpha\beta$ component of modulating signal
m_{abc}	abc component of modulating signal
q	Electric charge (C)
r_{i}	Ripple factor of inductor current
r_{v}	Ripple factor of capacitor voltage
s	Lévy step length

s_{f}	Scaling factor
$t_{\mathrm{d}}^{\mathrm{ac}}$	Time-delay in inverter current control loop (s)
$t_{\mathrm{d}}^{\mathrm{dc}}$	Time-delay in *PDV* control loop (s)
$v_{\mathrm{dc}}^{\mathrm{pk}}$	Instantaneous *PDV* (V)
$v_{\mathrm{C}}^{\mathrm{sum}}$	Sum of voltages of *QZS* network capacitors (V)
v_{CM}	Common mode voltage (V)
$v_{\mathrm{C}}, V_{\mathrm{C}}$	Instantaneous and steady-state *QZS* network capacitor voltage (V)
$v_{\mathrm{L,abc}}$	abc component of load voltage (V)
$v_{\mathrm{PV}}, V_{\mathrm{PV}}$	Instantaneous and steady-state *PV* output voltage (V)
v_{SCA}	Voltage across *SC* (V)
v_{dc}	Instantaneous DC-link voltage (V)
$v_{\mathrm{g}\alpha\beta}$	$\alpha\beta$ component of grid voltage (V)
v_{gabc}	abc component of grid voltage (V)
v_{n}	Neutral point voltage of AC system (V)
$v_{\mathrm{t}\alpha\beta}$	$\alpha\beta$ component of the terminal voltages of the inverter (V)
v_{tabc}	abc component of the terminal voltages of the inverter (V)
v_{tab}	Inverter line voltage (V)
v_{tan}	Inverter phase voltage (V)
v_{tao}	Inverter pole voltage (V)
w	Inertia weight
w_{max}	Maximum inertia weight
w_{min}	Minimum inertia weight

Greek Symbols

β	Lévy index
η	Efficiency of the converter
γ_1, γ_2	Sliding coefficient
κ	Lévy step coefficient
$\omega_{\mathrm{ac}}^{\mathrm{HF}}$	High frequency pole of $K_{\mathrm{ac}}(s)$ (rad/s)

$\omega_{\mathrm{dc}}^{\mathrm{HF}}$	High frequency pole of $K_{\mathrm{dc}}^{\mathrm{pk}}(s)$ (rad/s)
$\omega_{\mathrm{ac}}^{\mathrm{cut}}$	Cut-off frequency of damped-*SOGI* controller (rad/s)
$\omega_{\mathrm{ac}}^{\mathrm{gc}}$	Gain crossover frequency of inverter current control loop (rad/s)
$\omega_{\mathrm{dc}}^{\mathrm{gc}}$	Gain crossover frequency of *PDV* control loop (rad/s)
$\omega_{\mathrm{dc}}^{\mathrm{lag}}$	Zero frequency of lag compensator (rad/s)
$\omega_{\mathrm{dc0}}^{\mathrm{pk}}$	Resonance frequency of $G_{\mathrm{dc}}^{\mathrm{pk}}(s)$ (rad/s)
$\omega_{\mathrm{pdc}}^{\mathrm{pk}}$	Pole frequency of lead controller (rad/s)
$\omega_{\mathrm{zdc}}^{\mathrm{pk}}$	Zero frequency of lead controller (rad/s)
ω_{RHPZ}	*RHPZ* frequency of $G_{\mathrm{dc}}^{\mathrm{pk}}(s)$ (rad/s)
ω_{g}	Angular grid frequency (rad/s)
$\phi_{\mathrm{mdc}}^{\mathrm{pk}}$	Maximum phase boost of $K_{\mathrm{dc}}^{\mathrm{pk}}(s)$ at $\omega_{\mathrm{dc}}^{\mathrm{gc}}$
$\phi_{G_{\mathrm{dc}}^{\mathrm{pk}}}$	Phase angle of $G_{\mathrm{dc}}^{\mathrm{pk}}(s)$ at $\omega_{\mathrm{dc}}^{\mathrm{gc}}$
ρ	Air density ($\mathrm{kg/m^3}$)
ξ	Diode ideality constant
ζ	Ratio of N_{ser} and N_{par}

Chapter–1

Introduction

1.1 GENERAL

The electric power has mostly been generated through large scale projects using conventional resources such as thermal, hydroelectric, and nuclear. The implementation of such power plants has resulted in socioeconomic effects and concern for the environment. Even the *Clean Air Act* is enforced to regulate the pollution emitting from fossil fuel-based plants [1]. These concerns are detrimental in expanding the power generation through conventional arrangements.

The power generation through renewable energy resources mitigates the concern to the environment and climate change, which are arising with conventional power generation. Renewable power generation is also serving other goals such as sustainability, access to affordable electricity, and reliability. The present share of renewable energy is although 27.3% worldwide, there is increasing trend of its utilization, which is exhibited in Fig 1.1 [2]. Among various renewable sources, wind and solar energy resources are being harnessed mostly because of their abundant availability and emission-free conversion. In addition, solar energy is characterized by advantages, namely more predictable output, modular space requirement, less maintenance, and noise-free operation. Nevertheless, the power generated from solar *PV* is intermittent and largely depends on environmental conditions.

Energy extraction from *PV* systems involves the usage of *PCU* for grid integration. The battery-free grid-tied structure is preferred because of easy maintenance and cost-effectiveness. It requires efficient power transmission and high reliability of *PCUs* to convert the varying DC *PV* output voltage to AC power of appropriate voltage and frequency suited for grid integration. Due to the low and variable *PV* output voltage, a two-stage *PCU* configuration is commonly utilized in *PV* systems. The DC-DC boost converter is employed to control the output voltage of the *PV* source, and a *VSI* is used to complete the inversion process.

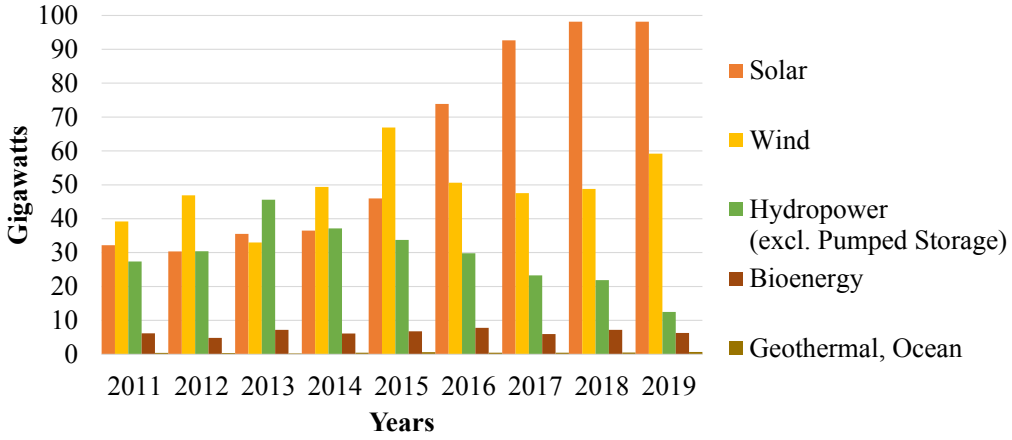

Fig. 1.1: Annual additions of renewable energy capacity.

The impedance source converters reflect a separate class of existing *PCUs* and are referred to as a single-stage power converter class. These *Impedance Source Inverters (ISIs)* incorporate the boosting ability with the inversion process. This *PCU* class is viewed as a unique and competitive solution to the two-stage structure essential for energy sources with small and varying voltage, like the *PV* system. Consequently, such *ISIs* were used in various applications, such as distributed generation and electric vehicles.

This class of *PCUs*, i.e., *ISIs* has undergone a rapid advancement over the past few decades to substitute the traditional two-stage structure since the first introduction of the 3-Φ *ZSI*. Accordingly, several qualitative research studies have been developed to enrich the functioning of *ZSI* from various viewpoints, like overall voltage boost, input current continuity, the voltage across active/passive elements, and conversion efficiency.

Although several topologies of *ISIs* were investigated, the operating principle is similar to that of conventional *ZSI*. Fundamentally they utilize a switching state in addition to eight states (six active and two zero states) that are used with 3-Φ *VSI*. This additional state, termed as *Shoot-Through* (*ST*) state, is responsible for accommodating the boosting mechanism of the converter within the inversion capability. In *ST* state, the H-bridge serves as a short-circuit by concurrently gating ON at least one-phase leg switches. On the contrary, in the *Non-Shoot-Through* (*NST*) state (traditional active and zero states), the H-bridge is emulated as a current source. Additionally, this *ST* state is allowable owing to the use of the impedance network and it should be placed within any of the zero states with a view not to impact the active states and, thereby, the AC voltage output.

Between several structural modifications in *ISI* topologies, the *Quasi-Z-Source* (*QZS*) inverter is the widely employed topology for renewable energy applications. Thus, the research work is carried out to investigate the performance of grid-tied *PV* systems based on *QZS* inverter.

1.1.1 Typical arrangement of grid-tied *PV* system

The key elements of the grid-tied *PV* system, presented in Fig. 1.2, are *PV* array, inverter, and filter. These are briefed hereunder:

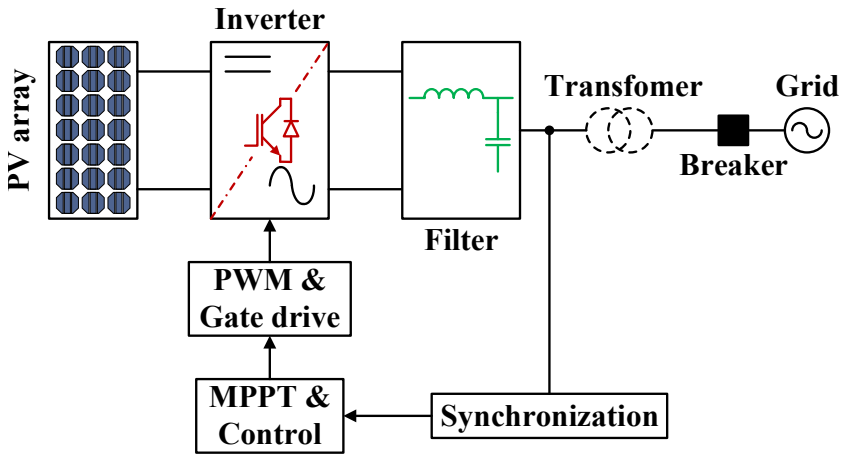

Fig. 1.2: Typical arrangement of single-stage *PV* system.

- ***PV* array**

  The *PV* array is an interconnected arrangement of *PV* modules or panels working as a single electricity-producing unit, whereas a large number of *PV* cells are connected in series to form a *PV* module [3].

- **Inverter**

  To transform the DC voltage produced by the *PV* array to AC voltage, inverters are used. The inverter is generally connected to the utility grid through a transformer. The inverter is usually controlled using carrier-based or space-vector-based *Pulse Width Modulation (PWM)* technique [4]. The transformerless inverter topologies have also been implemented for grid-tied applications.

- **Filter**

  Modulation of inverter generates switched voltage waveform along with 50 Hz fundamental signal. To separate the 50 Hz signal, a filter is required between inverter output and grid.

1.1.2 Advancement of *PV* inverters technology

Kjaer et al. [5] presented a comprehensive overview of the inverter technology for the *PV* system. This section summarizes the classification based on the configuration of *PV* panels and the power converters, which is illustrated in Fig. 1.3. They can be classified as a centralized structure, single-string structure, multi-string structure, AC module, and AC cell technology.

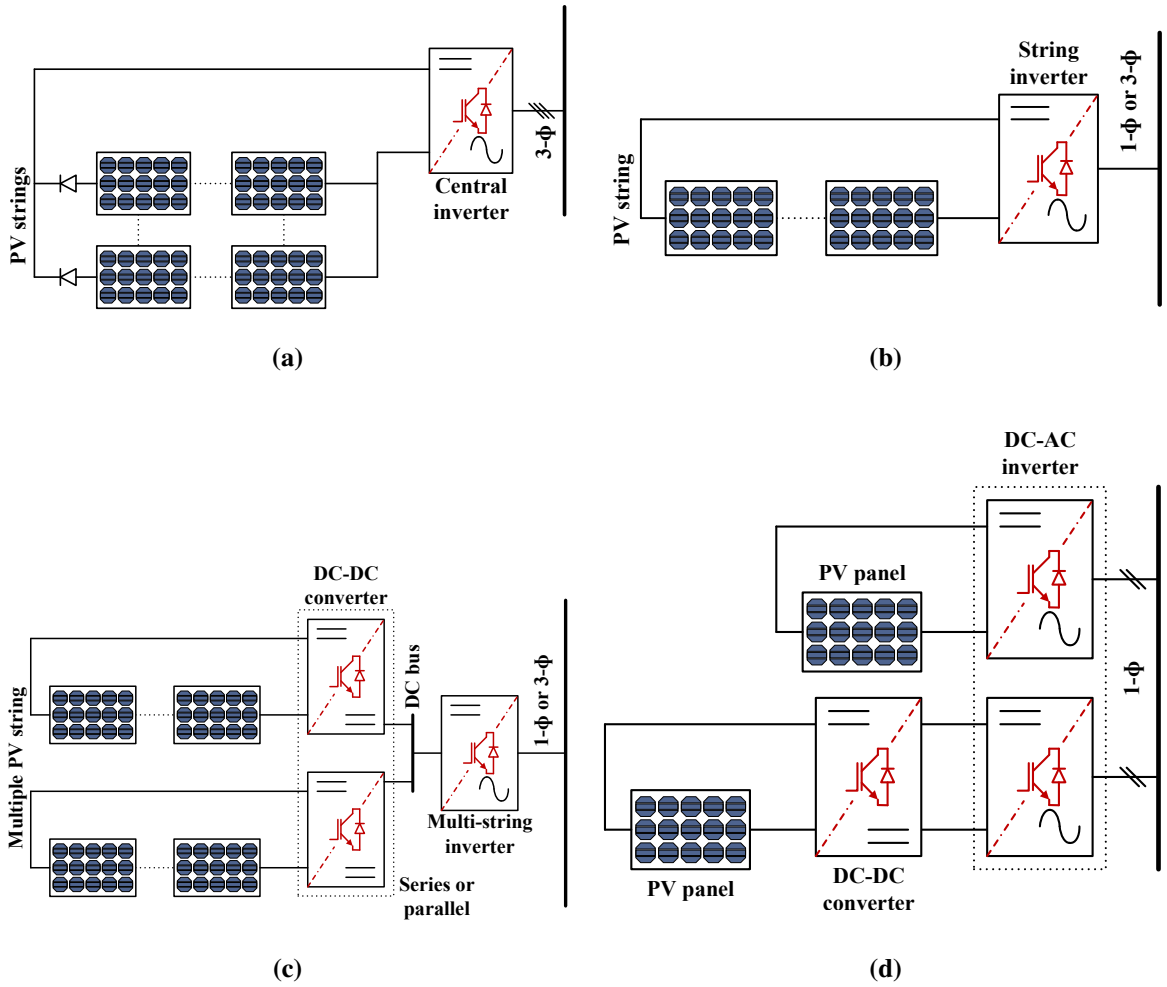

Fig. 1.3: *PV* power system classification based on the configuration of *PV* panels and power converters. **(a)** Past centralized technology. **(b)** Present string technology. **(c)** Present and future multi-string technology. **(d)** Present and future AC-module and AC cell technologies.

- **Centralized structure**

  Past developments were focusing on a centralized concept, as shown in Fig. 1.3(a). In such structure a large number of solar modules are connected to the grid by an inverter. The salient features of this system are as:

- The *PV* modules were grouped to form several strings. Each string had enough voltage to avoid further boosting.
- To obtain high power levels, strings were combined in parallel using blocking diodes.
- Typically, grid connections were made by line commutated thyristors, which increased the current harmonics and therefore yielded inferior power quality.

As the large DC voltage is resulting due to the series connection of *PV* modules, the primary issue of the centralized structure is the requirement of a large voltage DC cable between the inverter and *PV* modules. Besides, the centralized structure could not cope with *PSC*, which resulted in power loss.

- **Single-string structure and AC modules**

  The present technology constitutes the string inverters and the AC module, as shown in Fig. 1.3(b). In a string inverter, a single string of *PV* modules is integrated into the inverter, while the AC module consists of one module and one inverter as one electric device. Compared to the centralized structure, it provides better performance in the following aspects:

  - Overall efficient operation and price reduction due to mass production.
  - Due to a modular structure, there is a possibility of a simple up-scaling of the unit.
  - It is built with self-commuted *Insulated-Gate Bipolar Transistor (IGBT)*-based DC-AC converters, resulting in lower *Total Harmonic Distortion (THD)* and higher power quality.

- **Multi-string structure, AC modules, and AC cells**

  As shown in Fig. 1.3(c) and Fig. 1.3(d), these structures are a blend of the past and present technology. Multiple strings with a dedicated DC-DC converter are tied to a single DC-AC inverter (multi-string), or a large *PV* cell is integrated into a DC-AC inverter (AC module). In contrast to past technology, each string can be independently controlled. There is inherent flexibility to incorporate emerging innovations into established structures when compared to current technology.

1.1.3 Classification of inverter topology

The *PV* system grid interface inverter topologies are categorized based on the following: i) power conversion topology, ii) transformer and transformerless arrangement, and iii) power conditioning unit. They are briefed herewith:

- **Power conversion topology**

  The Fig. 1.4(a) presents a single-stage inverter topology. The inverter is made to control *Maximum Power Point Tracking (MPPT)*, inverter current, and voltage boost, etc. It requires that inverter for such single-stage conversion be designed so that it can sustain the peak power of twice the nominal power [6]. A two-stage topology is demonstrated in Fig. 1.4(b). In this topology, the *MPPT* is achieved by the DC-DC converter while inverter current control is performed by the DC-AC converter. In multi-string technology [5], shown in Fig. 1.4(c), DC optimizers are DC-DC buck-boost converters that can communicate to each other, equalize every panel output current in a series string, provide *MPPT*, are connected to common DC-link and grid interfacing is employed by a DC-AC inverter.

- **Transformer and transformerless arrangement**

  The transformer can be employed in two different forms during low *PV* voltage. The first strategy is to use a high-frequency DC-DC converter before the inverter, termed as an isolated DC-DC converter, as shown in Fig. 1.5(a). Another alternative is to utilize a line frequency transformer, as depicted in Fig. 1.5(b) at the inverter output. Employing a line frequency transformer does not cause DC current injection, increases system size and weight, and reduces efficiency. The use of *High Frequency (HF)* transformers reduces size and weight, becomes modular, and causes higher efficiency but does not prevent DC current injection. Consequently, when the *PV* voltage is sufficiently high, the transformer is viewed as an additional element. Accordingly, transformerless inverters, as illustrated in Fig. 1.5(c), were implemented to reduce the size, weight, and price, but they suffer from leakage current flowing between *PV* array and grid.

- **Power conditioning unit**

  The *PCU*, popularly referred to as inverter or converter, is the interface for connecting *PV* systems to the grid. The grid interface or converter technology suited for *PV* systems

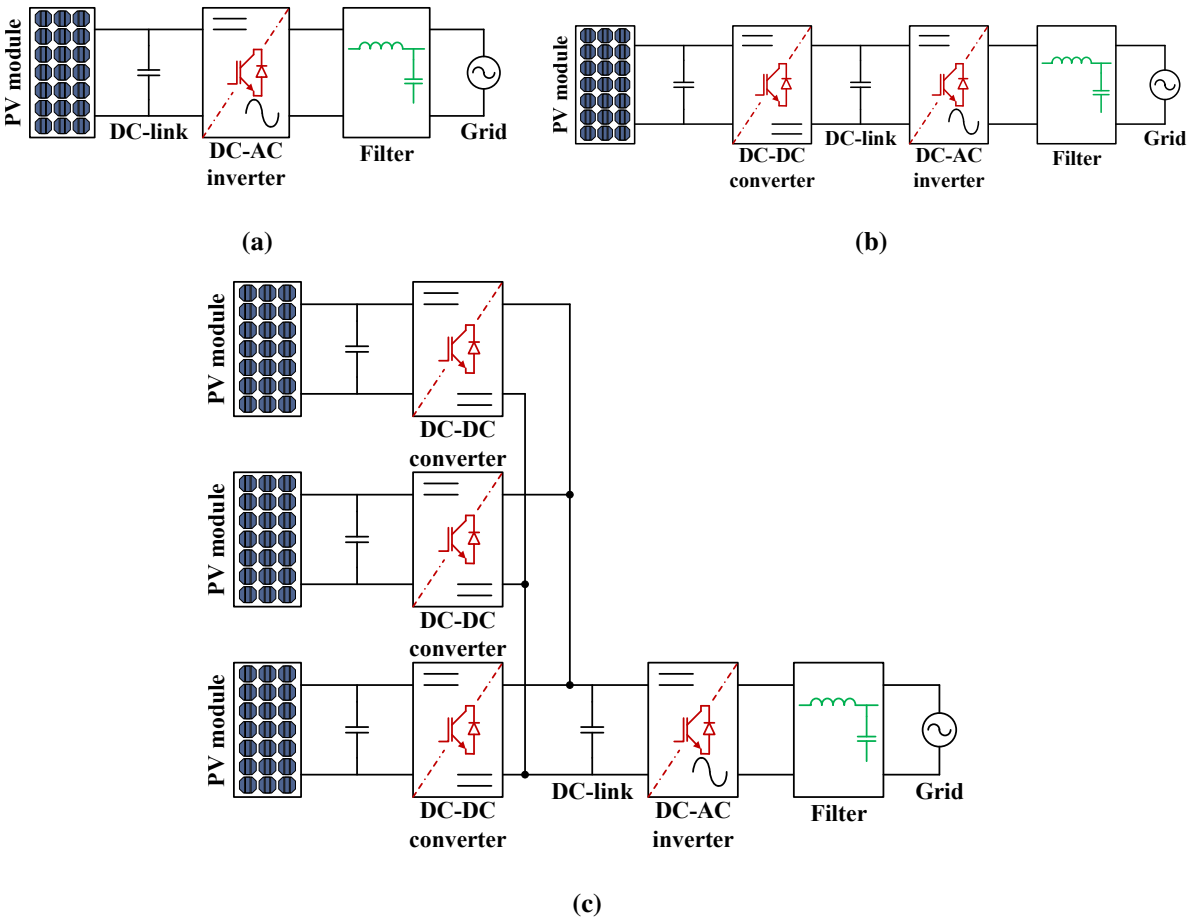

Fig. 1.4: *PV* grid interface topologies. **(a)** Single-stage power processing. **(b)** Two-stage power processing. **(c)** Two-stage power processing with common DC-link.

is presented in Fig. 1.6. The widely explored converter configurations are *VSI*, *CSI*, and *ZSI*. The selection of *PCU* is crucial as it may reduce the power stages and decrease the cost of the overall system. A review of the structure of the power electronic interface is provided in [7, 8]. As shown in Fig. 1.6(a), *VSI* is widely used for the grid-connected *PV* system. It utilizes a simple control scheme and well established *PWM* techniques [9]. It has four-quadrant capability, buck characteristic, and requires high input DC voltage for its proper functioning [5, 10]. Moreover, the switching devices of the same leg should not be gated-ON simultaneously. The DC-DC boost converter is used to boost the input voltage.

Another inverter topology used for interfacing the *PV* system to the grid is *CSI*, as shown in Fig. 1.6(b). It is preferred for high power, high-voltage direct current applications. The presence of an inductor on the DC side causes low current ripples at the interface of the *PV* array and inverter. The *CSI* is a boost converter, where the AC output voltage is greater than the DC input voltage that feeds the inductor. For wide voltage application,

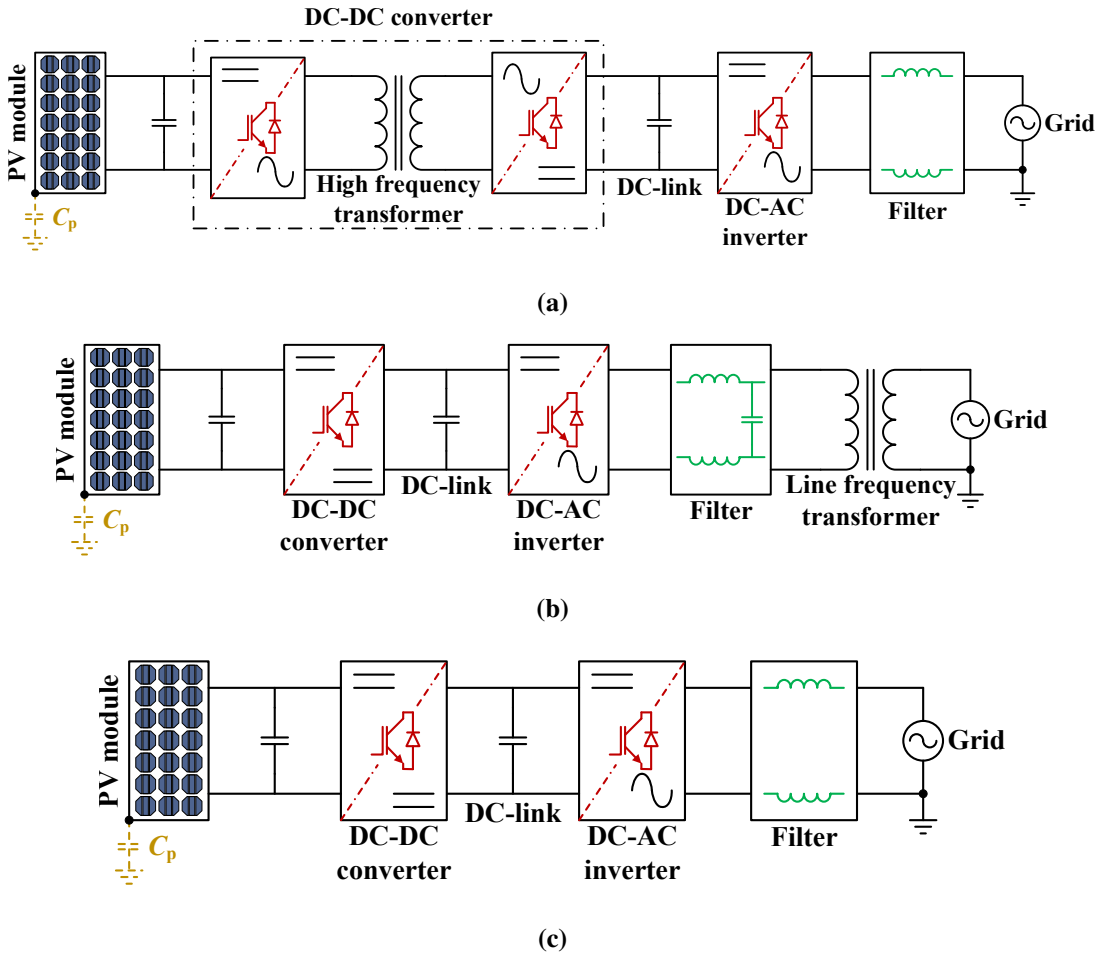

Fig. 1.5: Grid-tied *PV* system. **(a)** With *HF* transformer. **(b)** With line frequency transformer. **(c)** With transformerless configuration.

an extra DC-DC buck converter is required. Further, overlap time is needed between the upper and lower devices of the same leg, causing output waveform distortion and increasing filtering requirements. It requires an additional series diode with high speed and high-performance *IGBT* [11].

The *VSI* and *CSI* are either buck or boost converter and not be the buck/boost converter simultaneously. To overcome this, an impedance network, as shown in Fig. 1.6(c), is used between the DC input source and inverter bridge [12]. The *ZSI* provides single-stage buck/boost power conversion and avoids the use of a bulky transformer [13].

The *ZSI* requires a filter circuit at the input side as the input current is discontinuous. To overcome this issue, a *QZS* inverter topology, as shown in Fig. 1.6(d), has been proposed [14]. It has a lower component rating, reduced switching ripples to the *PV*

panels, less *Electromagnetic Interference (EMI)* problem, and reduced source stress in comparison to traditional *ZSI* [15].

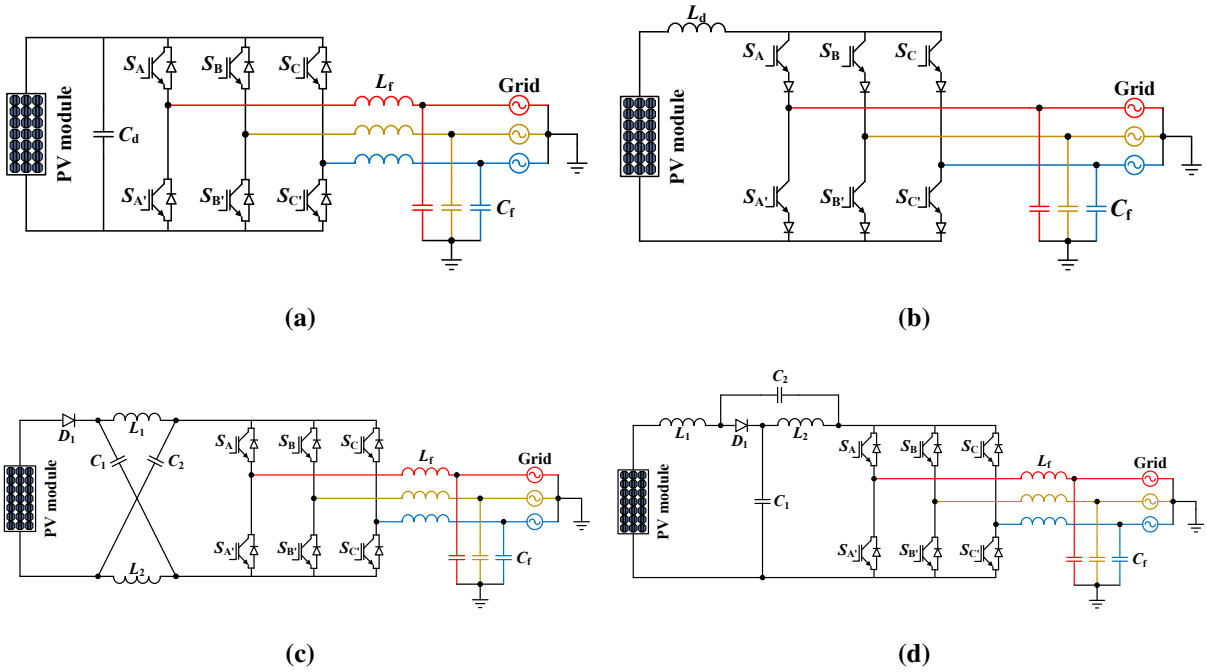

Fig. 1.6: *PV* grid interface topologies. **(a)** *VSI*. **(b)** *CSI*. **(c)** *ZSI*. **(d)** *QZS* inverter.

1.2 STATE-OF-THE-ART

In 1965, William McMurray invented the class of H-bridge converter, which benefited from the viable force-commutated semiconductor devices (thyristors) [16]. This H-bridge converter acts as a buck converter for DC-AC power conversion, commonly termed as *VSI*. Kenneth P. Phillips presented *CSI* topology, another most popular converter structure based on the current source concept [17]. The *CSI* was created using the duality principle [18] and provides a boost operation for DC-AC power conversion. When a wide variation in input voltage is found, such as *PV* application, a DC-DC boost converter is required for *VSI*, whereas in the case of *CSI*, a DC-DC buck converter is needed.

In 2003, Fang Z. Peng introduced a Z-source network between the DC source and inverter bridge to mitigate the drawbacks of *VSI* and *CSI* [12]. The impedance network comprises two inductors, two capacitors, and one diode. This impedance network is responsible for bucking or boosting the voltage of the circuit. The circuit integrates the boost and inversion in the single-stage. The *ZSI* inverter has six active states and two zero states called *Non-Shoot-Through*

(NST) states, and an additional zero state termed as *ST* state where switches of the same leg can be gated-ON simultaneously. Traditional *PWM* techniques were modified to add this unique feature of the *ST* state [12, 19–21].

The basic *ZSI*, due to several shortcomings, has resulted in poor performance, like unidirectional power flow, light-load operation, high inrush current, discontinuous input current, the large voltage across network capacitors, and isolated inverter and DC source. *Bidirectional Z-Source Inverter (BZSI)* [22] was derived by modifying the input diode with a bidirectional switch that could operate in the regenerative state and prevent completely unwanted modes when functioning at small inductance and low load power factor [23]. The *Improved Z-Source Inverter (IZSI)* [24] and the *Series Z-Source Inverter (SZSI)* [25] are capable of reducing the voltage of the network capacitor and can restrict the inrush current during starting. Four *QZS* inverters, investigated by Anderson and Peng [26], can provide a low network capacitor voltage, a constant input current, and a common DC-link between the source and the inverter resulting in low *EMI*. To minimize the source current ripples and guarantee consistent unidirectional processing, the *Embedded Z-Source Inverter (EZSI)* was derived by integrating two isolated DC-sources in series with network inductors [27, 28]. The voltage-fed *QZS* inverter with continuous input current is used prominently for renewable energy applications [29–49].

The *QZS* inverter was investigated for the 3-Φ *PV* power applications for standalone [29, 30] and grid-tied operation [30–33]. Owing to the transformerless topology, *Common-Mode Voltage (CMV)* is established in the *QZS* inverter causing leakage current to flow between the *PV* and the grid. Additional active and passive elements and modified *PWM* techniques were utilized to eliminate *CMV* [33, 34].

The *QZS* inverter was explored for the *Single-Phase (*1-Φ*) PV* power applications [35–41] under low passive elements and control [35, 36] and *PWM* technique [37]. The modeling of system was presented considering the 2ω ripples [38–41], its minimization using passive network components [38, 39], and *PWM* methods [40, 41].

The basic *QZS* inverter was modified by integrating a battery to reduce *PV* power fluctuation [42–49]. This configuration was investigated for *MPPT* [42], *PWM* techniques [43, 44], limit 2ω ripples [45], and controller design in grid-connected and islanded mode [46, 47]. The energy stored *QZS* inverter configuration for *PV* system [48, 49] solved the power

restriction of topology presented in [43–46], which is caused by a wide range of discontinuous conduction modes during the discharge of the battery.

Baker and Bannister [50] applied the *MLI* principle to reduce *THD*, switching losses, the voltage stress on the switching devices, and improves the electromagnetic capability. Due to the above benefits, *MLIs* were employed for renewable energy applications [51–54]. The most widely used *MLI* structures namely *NPC*, *Flying Capacitor (FC)*, and *Cascaded H-Bridge (CHB)* work in buck mode for DC-AC power conversion [55]. Impedance source network was utilized between DC-source and *MLI* structure to provide single-stage buck/boost ability [56–80]. The *MLI* topologies [56–66] suffer from the major drawback of discontinuous input current during boost operation. The *QZS MLI* family draws constant input current and has same boosting ability as multilevel *ZSI* [67]. *QZS* cascaded *MLI* was explored for *PWM* techniques [68, 69], grid integration of 1-Φ [70–72], and 3-Φ [73] system. *NPC-QZS* inverter was studied for *PWM* techniques [74–77], and T-type *QZS* inverter investigated for neutral point capacitor voltage balance [78, 79] and *CMV* reduction [79, 80].

The extended voltage gain topologies are classified into *Switched Inductor (SL)* topology [81–85], *Tapped Inductor (TL)* topology [86], cascaded topology [87], transformer-based topology [88–96]. The *SL* structures acquire large boost capability by replacing one or two inductors of the traditional impedance network, which results in size reduction, large power density, and better dependency among voltage gain and modulation index. Two terminal *TL* cells were utilized to replace the two inductors of the basic impedance network topology. Thus, the output voltage range can be widely expanded by changing the turn ratio of *TL* and employing a lower *ST* duty ratio than the basic *ISI*, which results in a larger modulation index and, consequently, improved output waveform. To increase the voltage boost capacity, including the modulation index, magnetically coupled inductors, and transformers were employed in the impedance network. It reduces the number of passive components in the network, increases the power density, and decrease costs.

Various methods have been explored to regulate the pulsed DC-link voltage of ISIs that are direct DC-link voltage control [97, 98], indirect DC-link voltage control [79, 99–102], and capacitor voltage control [30, 49, 103–109]. Direct control utilizes special measurement circuits. The indirect DC-link voltage control was estimated through capacitor voltage and ST duty ratio, input and capacitor voltage; and capacitor voltage control was regulated to its reference value.

Some other DC-link voltage control methods utilize the average peak DC-link voltage [110], the active power current component [111], and one cycle control [112].

Integrated with a properly selected converter, the *MPPT* strategy should guarantee that maximum power is extracted from the *PV* system for varying ambient temperature and solar insolation under diverse environmental situations. The classical *MPPT* algorithms [113–122] are capable of operating under uniform insolation but fail to detect *GMPP* due to *Partial Shaded Condition* (*PSC*). There are methods such as *PV* array reconfiguration [123], complex converter circuit topology [124], and the use of improved techniques of *MPPT* [125] to limit the degradation of *PV* power generation owing to *PSC*. Among these, the most enticing possibilities are using the modified *MPPT* technique, which does not involve physical modifications to an established system [126]. Intelligent techniques such as fuzzy logic [127], *Artificial Neural Network (ANN)* [128], swarm intelligence methods [129–136], two-stage methods [137–149] were explored for the extraction of maximum power from the solar *PV* system.

1.3 RESEARCH OBJECTIVES

The research work entitled “Design and Control of Grid Connected Photovoltaic System” is carried out with the following objectives:

- To design a control scheme for single stage converter for grid connected *PV* system.
- To design a control scheme for multilevel converter based grid connected *PV* system capable of injecting a sinusoidal current.
- To develop an *MPPT* algorithm capable of operating at different irradiation level.

1.4 THESIS ORGANIZATION

The thesis is organized into seven chapters. It summarizes the specific contributions directed in achieving the above objectives and presents the results obtained during this research. The brief description of these chapters is outlined as follows:

- **Chapter 1: Introduction**

  This chapter presents a brief introduction of the participation of the solar *PV* system on the total power generation, the general structure of the grid-tied *PV* system, and different

inverter topologies that are utilized for *PV* applications. The state-of-the-art in the field of research is addressed. This chapter also enlists the objectives of the present study and outlines the organization of the thesis.

- **Chapter 2: Literature Review**

  The vital part of this chapter provides a brief literature review on various operational and control aspects of the 3-Φ *QZS* inverter. The literature review is divided into five categories namely *QZS* inverter for *PV* application, multilevel *QZS* inverter topology for the solar *PV* system, improvement in *ISI* topologies, *PDV* control strategies, and *MPPT* techniques with *PSC*. The chapter ends with a summary of research gaps and identified research objectives. The later part of this chapter describes the authors' contributions to the identified research objectives.

- **Chapter 3: *QZS* Inverter Based Three-phase Grid-tied *PV* System**

  This chapter deals with the analysis of the *QZS* inverter based 3-Φ grid-tied *PV* system. Sinusoidal inverter current reference is regulated through damped-*SOGI* controller and DC-link voltage control is performed by *TOIL* compensator via its indirect estimation. The performance of the proposed controller is compared with the other linear and robust controllers. The effect of parameter variation and time-delay in the control loop is investigated. Finally, experimental results are presented to verify theoretical and simulation findings.

- **Chapter 4: Three-level *NPC-QZS* Inverter Based Three-phase Grid-tied *PV* System**

  This chapter presents the investigation on the performance of the 3-Φ grid-tied three-level *NPC-QZS* inverter for *PV* application. Inverter current is controlled in stationary reference frame via damped-*SOGI* controller and the *IDL* compensator is implemented for DC-link voltage control. A qualitative study of the two modified level-shifted modulation schemes is addressed. A performance comparison is given between the *IDL* compensator and the robust *SMC* controller. Further, theoretical and simulation are validated experimentally.

- **Chapter 5: *QZS-SC* Inverter Based Three-phase Grid-tied *PV* System**

  This chapter presents the performance of grid-tied 3-Φ multilevel *QZS-SC* inverter for *PV* applications. An *SC* inverter structure is cascaded to the *QZS* network to improve

the voltage gain range. The carrier level shifted modulation technique is explored for the gating signal generation. Grid-tied operation is achieved via inverter current control using the damped-*SOGI* controller and DC-link control is performed through *Proportional-Integral-Derivative (PID)* compensator. Finally, to confirm theoretical and simulation observations, a *Hardware-In-The-Loop (HIL) Real-Time Simulation (RTS)* study is presented.

- **Chapter 6: Flying Squirrel Search Optimization Algorithm for *MPPT* under *PSC***

  This chapter presents the implementation of an *MPPT* based *FSSO* algorithm under a partial shaded solar *PV* system. The duty ratio to array voltage transfer function is derived to analyze the stability of the system. Experiments are performed for the two *PV* array configurations and a comparison with other state-of-the-art *MPPT* techniques such as *P&O*, *PSO*, and *GWO* is presented to show the novelty of the *FSSO* algorithm.

- **Chapter 7: Conclusions and Scope for Future Work**

  This chapter presents a summary of the main conclusions of the studies presented in previous chapters. It also enlists the direction for further research.

Chapter–2

Literature Review

2.1 GENERAL

In recent years, the concerns emanating from environmental problems related to fossil fuel usage, increasing fuel costs, and energy security have accelerated the deployment of *PV* systems for electric power generation. To date, *PV* systems with single- and double-digit megawatt capability have been tied to the grid predominantly at the stage of sub-transmission voltage. At the distribution stage, such small rating systems do not affect the current power grid, which has a predominant share of power generated by conventional resources. *PV* systems comprise primarily of roof-top structures with a capacity of several kilowatts. However, with an increasing interest in solar energy and national policies to pursue clean energy, it is anticipated that large-scale *PV* plants would rise exponentially.

A reliable and cost-effective *PV* inverter technology is crucial for the smooth functioning of the large-scale grid-tied *PV* system. The factors such as the vast potential of solar energy and the motivation for clean energy resulted in various design solutions for the *PV* inverter in the areas of *PCU*. The *VSI* has so far been commonly used to interface the grid with the *PV* systems. Although *VSI* is an attractive and promising topology, some inherent disadvantages increase the complexity and cost of a *PV* system architecture. The techno-economic considerations suggest that the power electronic interface for grid-tied *PV* systems should be cost effective, high in efficiency and life span. Thus, researchers have proposed a single-stage buck/boost *QZS* inverter configuration, which improves the transient response and lifespan compared to the *VSI*. To enlist

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The contents of this chapter are partly published in:

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* "A review on modulation techniques of Z-source network," *2016 7th India International Conference on Power Electronics (IICPE)*, Patiala, 2016, pp. 1-6, doi: 10.1109/IICPE.2016.8079344.

the contributions of various researchers, a brief literature review is carried out on numerous aspects of *QZS* inverter-based grid-tied *PV* systems.

The Section 2.2 outlines the review on the performance analysis of grid-tied *QZS* inverter for *PV* system applications. A study on *MLI* topologies based on *ISI* is summarized in Section 2.3. To overcome the limitations and improve the boost characteristics of the traditional *ISI* topologies, various topological structures have been reviewed in Section 2.4. As the DC-link voltage is pulsating in nature, numerous methods used to measure and control the *PDV* are reviewed in Section 2.5. Finally, a literature review of various *MPPT* techniques is presented in Section 2.6. The Section 2.7 highlights the authors contributions to the identified research objectives.

2.2 *QZS* INVERTER TOPOLOGY

A *VSI* has buck characteristics and it needs high DC input voltage for a stable operation, which is realized through an extra DC-DC boost converter for a transformerless configuration. *VSI* usage is advantageous due to ease of control. The control schemes and *PWM* techniques for *VSI* are well established compared to the relatively new *QZS* inverter topology.

QZS topology derived from the *ZSI* offers several advantages over *ZSI*, such as continuous input current, low voltage stress across the network capacitor, and reduced *EMI* caused by common DC-link between input and output [26]. The *PWM* techniques derived for *ZSI* [12, 19–21] are applicable for the *QZS* inverter by adding *ST* duration, during which upper and lower devices of the same leg can be gated-ON simultaneously. A *QZS* inverter is a preferred topology to integrate *RES* such as *PV* to AC power grid as it provides single-stage power transfer with buck/boost inversion feature and can work even with a wide fluctuation in input voltage.

QZS inverter for *PV* power generation system was first presented in [29], which also discusses the passive component selection and uses *MCBC* for the *ST* generation for standalone operation. The constant capacitor voltage control [30] is implemented through a two-stage control. The dynamic behavior of the *QZS* inverter was studied with small-signal analysis for both standalone and grid-connected mode. Appropriate reference capacitor voltage was selected to yield minimum switching stress and avoid high gain instability. The model predictive control algorithm for grid-tied *QZS* inverter [31] extract maximum power from the *PV* array. Active and reactive power injected into the grid was regulated to compensate the reactive power required by local loads. Lashab et al. [32] reported a dual-input *QZS* inverter, where one *PV* array was tied

to the *QZS* network input and the other in parallel to the *QZS* network capacitor. The suggested solution offers higher conversion efficiency and better extraction of power from the *PV* arrays with the same passive elements of the conventional *QZS* inverter. Owing to transformerless configuration, the *QZS* inverter experiences a common mode current, and thus forms a leakage current path between the *PV* source and the grid. Noroozi and Zolghadri [33] demonstrated that connecting an inductor to the negative terminal of the *QZS* network and applying the odd *PWM* method caused the *CMV* to be nearly constant. Thus, the leakage current flowing through the stray capacitance of *PV* panels was reduced. Two additional active switches on the grid-side were employed to dissociate the grid and inverter, and a *PWM* method was introduced to eliminate the *CMV*. Noroozi et al. [34] reported a modified *Space Vector Modulation (SVM)* to reduce the leakage current by suppressing low-frequency harmonics from *CMV*. The reduction of high-frequency harmonics from leakage current was achieved by combining the proposed *SVM* with a high-frequency inductive-capacitive filter.

The research article on standalone 1-Φ *QZS* inverter [35] discussed operation modes caused by small inductance. The resonance at high frequency due to reduced *QZS* impedance was suppressed by active damping control. The *Proportional (P)* controller was added for damping. Singh et al. [36] investigated hysteresis current controlled active power filter at the DC-side to achieve low *QZS* network capacitance values. A hybrid *PWM* technique for *QZS* inverter for grid-tied *PV* was presented by combining *PWM* and *Pulse Amplitude Modulation (PAM)* [37]. The performance of a 1-Φ grid-connected *QZS* inverter was investigated [38] through the 2ω ripple model of *QZS* inverter-based *PV* system with and without *PV* terminal capacitance. Ge et al. [39] described the minimization of impedance network elements and buffered 2ω ripple power in *QZS* capacitors. A damping control for the 2ω inductor current ripple was discussed and control scheme designed to eliminate 2ω power in inductors of the *QZS* network and DC source. The 1-Φ *PV* system based on the *QZS* inverter was used for buffering the 2ω component through a capacitance reduction control strategy [40]. The reduction of capacitance causes increased voltage stress across the switching device and power loss. Liang et al. [41] suggested a pulse-width amplitude modulation technique by combining *PAM* into sinusoidal *PWM* to decrease the *QZS* network impedance values owing to the allowed 2ω ripple in DC-link voltage and to increase the efficiency. The original *QZS* inverter was modified by integrating an energy storage battery at the *PV* terminal to make the system work in grid-tied and standalone mode.

A battery-assisted *QZS* inverter [42–46] was investigated for a *PV* system. An adaptive neuro-fuzzy interface system was developed for the *QZS* inverter-based *PV* system [42] to extract maximum power. The *ST* duty ratio and modulation index were regulated to control injected power and maintain voltage, frequency, and current. A modified *SVM* technique [43] employed second-order *LC*-filter decoupled control of active and reactive power. It helped the *PV* panel store extra energy or supply inadequate energy and reduces *PV* power fluctuation.

The *SVM* for the *QZS* inverter divides the total *ST* time interval into six equal parts per control cycle [44], which yields six switching moments, a low ripple in inductor current, and high inverter efficiency. The controller equipped with a harmonic compensator [46] controls the battery current in grid-tied mode and regulates the voltage in islanded mode during unbalanced and non-linear loading conditions. Liang et al. [45] addressed the 2ω ripple model for the energy stored *QZS* inverter considering the asymmetric *QZS* network and the design of passive elements was formulated depending on the investigated impedance design methodology. Liang et al. [47] modified the battery-assisted *QZS* inverter [42–46] to suit its working both day and night. The *Proportional-Integral (PI)* controller regulated *ST* states during the day for *MPPT* and at night to control *PDV*. To maintain the AC output voltage, the *SOGI* controller was utilized.

The *QZS* inverter topology with energy storage for *PV* system [48, 49] overcomes the power limitation of topologies [43–46], which arise due to a wide range of discontinuous conduction mode during battery discharge. The control techniques [48] were investigated for regulating the inverter output power, *MPPT*, and manage battery power. In contrast, article [49] demonstrated the control method to maintain constant peak DC-link voltage as the conventional methods does not ensure this due to the battery's voltage clamp.

2.3 MULTILEVEL *ISI* TOPOLOGY

The *MLIs*, first introduced in 1975 [50], have drawn significant attention for high power and medium voltage applications. The basic concept of a multilevel converter is to obtain high power operation using a series of power semiconductor devices with several low voltage DC sources and synthesizing a stair-case voltage waveform. By increasing the number of levels, the stair-case output voltage for *VSI* or output current for *CSI* can be achieved. This results in closer to sinusoidal waveform with reduced *THD* at a decreased switching frequency, improved electromagnetic capability, lesser switching losses, and transformerless configuration

at distribution voltage level. For their advantageous characteristics, *MLIs* have been accepted in renewable energy applications [51, 52]. Operation of *MLI* at low switching frequency results in a lower switching loss and high power transfer capacity [53].

Most popular multilevel structures namely *NPC*, *FC*, and *CHB* utilize *VSI* operating in voltage buck mode [55]. The *NPC Three-Level (3L)* converter is a fundamental multilevel converter. An extra DC-DC boost converter is required for interfacing the renewable energy with lower voltage to the grid in the transformerless configuration.

As the dead time between the devices is omitted, an accurate output waveform quality and lesser *CMV* can be achieved by inserting a Z-source network between the DC input and traditional *MLI*. The first Z-source network for the multilevel structure [56] utilized two Z-source networks between two isolated DC sources and conventional *NPC* circuitry to get the single-stage buck-boost capability. Two impedance networks can be short-circuited sequentially for voltage boosting. A single Z-source network was used to decrease passive component count, system cost and balancing the inductive voltage boost [57]. It utilized *POD* carrier-based *PWM* with triple offset and time advance/delay and require two DC-sources.

Through continuous *PWM* and discontinuous *PWM* techniques [58], it was observed that continuous modified reference *PWM* is the preferred solution for *3L* Z-source *NPC* inverter. Comparison between *POD* and modified *IPD* techniques and *3L ZSI* with reduced element count was presented in [59]. A five-level Z-source *NPC* inverter [60] used *IPD* modulation technique to insert *ST* states.

A modified *SVM* for *3L* Z-source *NPC* inverter utilizes six commutating devices [61]. A generalized *SVM* was investigated for *CHB 3L ZSI* [62] that produces a high-quality waveform at a low switching frequency. *PWM* technique for dual H-bridge *3L ZSI* was developed to provide balance voltage boosting with reduced common-mode switching [63]. The *PWM* was modified to enable dual *ZSI* work under semiconductor failure and to achieve zero common-mode switching. Input diode was replaced by *IGBT* with an anti-parallel diode for a bidirectional power flow. A *3L* modified Z-source *NPC* inverter was used for *RES* with closed-loop control in the islanded mode [64].

By introducing an *HF* transformer and two additional capacitors, the Z-source *NPC* inverter with a single impedance network was supplied from a single DC source [65]. Moreover, an input

voltage gain higher than the traditional Z-source network was achieved with transformer turns ratio different from 1:1. Mo et al. [66] proposed a transformer-based Z-source *NPC* inverter to achieve a high gain while maintaining a high modulation index. The topologies [56–66] have one common drawback: a discontinuous input current during the boost conversion mode could negatively influence the input voltage source.

As the *QZS* inverter draws continuous input current from the source and provides the same boosting capability as *ZSI*, it can be a viable *PV* inverter option [67]. Zhou et al. [68] discussed a 1-Φ grid-connected *PV* module integrated converter based on cascaded *QZS* inverter that utilized Gallium Nitride enhancement-mode field-effect transistor and an electrolytic capacitor. The triangular carrier was replaced with the sawtooth carrier. A module optimized design was derived based on the AC equivalent circuit and power loss analytical model. By analyzing the phase-shifted *PAM* and phase-shifted sine wave *PWM* [69], it was observed that the switching action is reduced in *QZS* cascaded *MLI* for phase-shifted *PAM*. A controller was developed to provide grid-tied current injection at *Unity Power Factor (UPF)*, independent *MPPT* for each *PV* panel, and DC-link voltage balance for seven-level *QZS* cascaded *MLI* based 1-Φ grid-connected *PV* system [70]. Controller parameters were designed to ensure system stability and fast response, and a multilevel *SVM* technique was provided to get a step-like waveform. Article [71] discussed the modeling, *QZS* network parameter selection, and efficiency calculation for 1-Φ seven-level *QZS* cascaded *MLI*. A distributed *MPPT* was incorporated to achieve *PDV* balance. Operating principle and controller design for the energy stored seven-level *QZS* cascaded *MLI* for the *PV* system was developed to overcome the intermittent and stochastic fluctuation of solar power injected into the grid [72]. The detailed dynamic model [73] was developed for 3-Φ seven-level *QZS* cascaded *MLI* based *PV* system.

A steady-state analysis of the topology with carrier-based modulation technique was proposed for a 1-Φ *3L NPC-QZS* inverter [74]. Analytic expressions were also presented for the *Continuous Conduction Mode (CCM)* and *Discontinuous Conduction Mode (DCM)*. A *3L QZS* inverter configuration resulted in reduced voltage across the capacitor [75]. A level-shifted carrier-based *PWM* technique was presented for *3L NPC-QZS* inverter where *NST* states were provided using the traditional *IPD* scheme. In contrast, *ST* states were inserted by another carrier with double frequency [76]. Shults et al. [77] examined the *SVM* for a *3L NPC-QZS* inverter, providing low switching, balanced capacitor voltage, and no distortion in the output

voltage. Roncero-Clemente et al. [78] demonstrated a carrier level-shifted *PWM* technique for a T-type *QZS* inverter to generate constant width *ST* states throughout the fundamental period and mitigate neutral point capacitor imbalance by using the *PI* controller. Qin et al. [79] proposed a *PWM* technique for *3L QZS* T-type inverter to simultaneously achieve voltage boosting, *CMV* reduction, and neutral point voltage balance. A coordinated control strategy in standalone mode was presented between neutral point voltage and voltage boosting, limiting the *CMV* magnitude to one-sixth of the DC-link voltage. Neutral-point voltage imbalance was successfully reduced. In standalone mode, an *SVM* technique was suggested for a *3L* T-type *QZS* inverter to decrease *CMV*s magnitude and slew rate [80]. By properly selecting the *ST* states, *CMV* was limited to one-sixth of DC-link voltage with required voltage boosting. The neutral point voltage oscillates slightly in normal operating situations.

2.4 IMPROVED BOOST *ISI* TOPOLOGIES

The research on *ISI* has been a subject of intensive investigation since it first was proposed in 2002 [12]. New Z-source topologies are being evolved to cater three major factors: (i) a decrease in Z-source network component count and rating; (ii) improvement of voltage gain range; and (iii) application-oriented optimization and advancement. The elementary two-level *ZSI* has various disadvantages: reduced efficiency, unidirectional power flow, light load operation, high inrush current during start-up, a discontinuous input current, higher Z-network capacitor voltage, and isolated source and inverter DC-link.

Rabkowski [22] replaced the input diode of the Z-source network with a bidirectional switch. The proposed *BZSI* completely avoids undesirable operation modes of *ZSI* when it is working under a low load power factor or small inductance [23]. *IZSI* [24] and *SZSI* [25] were introduced to reduce the huge inrush current and lower capacitor voltage stress. In the case of *IZSI*, the inverter bridge and the input diode position were changed, and the connections were also reversed, while the *SZSI* was obtained by placing the Z-source network between the input and the inverter bridge. Anderson and Peng [26] presented a *QZS* topology with a lower component rating, joint earthing of the input source and the DC-link to reduce the common-mode noise in the system, and the continuous input current to lower the source stress. Two isolated DC sources connected in series with the inductors were introduced as *EZSI* to make the source current waveform continuous [27, 28]. All the above circuit modifications improve the basic *ZSI*,

although there is no effect on voltage gain. The *QZS* inverter appears to be the most improvised *ZSI* topology as it results continuous current, lower component rating, common DC-link between source and inverter bridge, and reduced leakage current.

One inductor of the Z-source network in *QZS* inverter topology was replaced by an *SL* cell to achieve a higher boosting ability [82]. Two *SL QZS* inverter topologies were presented by replacing both the inductor with the *SL* cell [83]. Ho et al. [84] suggested an active-*SC*/*SL QZS* inverter topology to provide a high voltage boost, low voltage stress across switching devices. Still, they do not share the common ground between the input voltage source and the inverter bridge. Ahmed et al. [85] applied *SC* in conjunction with a three-winding switched-coupled-inductor to *QZS* inverter to improve the boost ability with a smaller component count and lower turn ratio. In the case of *SL QZS* inverter topologies, additional inductors are in series during *NST* state and parallel during *ST* state.

A *TL* and two diodes were used to replace one inductor for improving the boost inversion capability of the traditional *QZS* inverter [86]. Gajanayake et al. [87] proposed an *Extended Boost Quasi-Z-Source (EBQZS)* inverter to increase the voltage gain of *QZS* inverter without increasing the number of active switches and grouped as capacitor assisted and diode assisted *EBQZS* inverter. These *EBQZS* inverter topologies have certain disadvantages, such as a small boost effect, intricate passive element design, complex structure, and large size.

Magnetically coupled inductors and transformers were used to improve the voltage boost capability besides the modulation index. Furthermore, these topologies utilize less passive components, improves the power density, and lowers the cost [11]. Qian et al. [88] used two inductors built together on one core (transformer) and one capacitor to form a trans-*QZS* inverter that provides a common DC-link between DC source and inverter bridge. The inverter output voltage and *ST* duty ratio can be manipulated using transformer turn ratio greater than 1. Nguyen et al. [150] proposed an improved version of the trans-*QZS* inverter using one transformer, two capacitors, and one inductor that achieves continuous input current, lower current stress on transformer winding and suppresses surge current during start-up. *Inductor-Capacitor-Capacitor-Transformer (LCCT) ZSI* uses a DC current blocking capacitor in series with transformer and prevent the transformer core from saturation [91, 92]. TZ*SI* was presented by replacing the two inductors in the Z-source network of the *QZS* inverter with two transformers to achieve very high voltage gain [93]. By reconfiguring the connections of

T*ZSI*, Σ*ZSI* was developed, which achieve smaller size compared to T*ZSI* as voltage boost was improved by reducing the transformer turns ratio [151]. Discontinuous input current Γ-*ZSI* [89] and continuous input current asymmetrical Γ-*ZSI* [90] were proposed, whose voltage gain can be improved by lowering the transformer turn ratio. A coupled transformer with three windings was used to realize the Y-source inverter [94–96]. Despite the potential benefits of transformer-based topologies like high modulation index at high gain, improved waveform quality, better use of DC-link voltage, lower voltage stress across switching devices, they have some drawbacks: high instantaneous *ST* and magnetizing currents, requirement of high magnetic coupling transformers, and low leakage impedance [152].

2.5 *PDV* CONTROL

Owing to *ST* zero states, the DC-link voltage of *ISIs* is a pulsating waveform, which is difficult to measure. The various methods for controlling *PDV* are classified into three main categories: (i) direct DC-link voltage control; (ii) indirect DC-link voltage control; and (iii) capacitor voltage control.

The DC-link voltage was measured directly using a scaling and sensing circuit [97] or a sampling circuit [98] to achieve direct control of *PDV*. The direct methods require a specially designed external sensing circuit.

Depending on the relationship between the DC-link voltage, capacitor voltage, and *ST* duty ratio, the capacitor voltage of impedance source network was indirectly used to regulate the *PDV* [99, 100]. Dual-loop regulation was used where the *P* regulator carried out the internal inductor current loop, and the *PI* regulator carried out the outer voltage loop. Input and capacitor voltage was measured, and therefore *PDV* was estimated to control it at reference value [79, 101, 102]. Single loop voltage control was performed utilizing a *PI* compensator [79]. The simulations and experimental validation was performed after replacing the inverter bridge with a switch and designed a single and double-loop compensator [101]. Regulators were developed based on direct digital control in dual-loop mode, where the *PI* controller performed the inner inductor current control to increase the stability margin, and outer voltage regulation was performed by the *PI* regulator [102]. These indirect control methods of *PDV* results in poor performance due to the non-linear *PDV* and capacitor voltage ratio.

Li et al. [30] implemented constant capacitor voltage control through two-stage control, where appropriate capacitor voltage reference was selected according to *PWM* techniques. Constant *PDV* was achieved using the outer capacitor voltage and the inner battery current loop [49]. A varying capacitor voltage reference method was used to keep the DC-link voltage constant [153]. Gajanayake et al. [103] investigated a double-loop control strategy. The *PI* compensator achieved outer capacitor voltage regulation and inner inductor current control was realized by employing the *P* controller. The capacitor voltage was regulated by controlling the *ST* duty ratio [104, 105]. The *PID* compensator was employed to regulate the *ST* duty ratio [104] whereas, the parameter of the *PI* compensator was regulated by neural networks for wide-range control [105]. The non-linear control techniques [106–109] were utilized to regulate the capacitor voltage through model predictive control [106, 107] and *SMC* [108, 109]. The *ZSSE* was achieved and the average value of *PDV* was used to calculate its reference value [110]. A *PI* compensator was employed to regulate the *PDV* towards target voltage by adjusting the current component of active power [111]. One cycle control technique to control the DC-link voltage had been proposed for *QZS* inverter where the diode voltage selected as a switched variable [112]. In the capacitor voltage control, the voltage stress across devices is unapparent and the *PDV* increases during step-increase in the input voltage and thereby causes the distortion in AC-voltage.

2.6 *MPPT* ALGORITHMS

Implemented with an appropriately selected converter, an *MPPT* scheme must ensure that the maximum power is extracted from the *PV* system under different environmental conditions, caused by changes in the ambient temperature and solar insolation. The process of *MPPT* gets complicated due to non-linear *Current–Voltage (I–V)* characteristics and largely varying *P–V* curve with variations in solar insolation and temperature. Some popular classical *MPPT* techniques include *Hill Climbing (HC)* [113] and *P&O* [114–116]. The *HC* and *P&O* methods cause oscillations around *Maximum Power Point (MPP)* due to continuously changing perturbation in both directions, thereby resulting in power loss [117]. The *Incremental Conductance (INC)* [118] method, although reduces these oscillations, but does not completely eliminate them.

The *MPPT* methods [119–122] are effective under uniform solar insolation and temperature, when there is only one *MPP* in the *P–V* curve. These methods, however, are

not suited for large *PV* installations comprising several series- and/or parallel-connected *PV* modules. The degraded performance of even a single module affects the performance of the complete *PV* installation. At times, a part of the *PV* array receives nonuniform sunlight due to moving clouds or shadows of the neighboring objects, leading to *PSC*. The *PSC* leads to reduced power output, and the quantum of reduction depends on the system configuration and the *Shading Pattern (SP)*. *PSC* results in multiple peaks in the *P–V* curve, and the conventional *MPPT* methods are not able to distinguish between the local and global peaks.

There are methodologies to limit the drop in power generation owing to *PSC*, which mainly include: *PV* array reconfiguration [123], complex converter circuit topologies [124], and improved techniques of *MPPT* [125]. Among these options, the use of an improved *MPPT* algorithm is the most attractive possibility, which does not require physical changes to an already existing system.

As a result, numerous *MPPT* techniques have been investigated to search *GMPP* under *PSC* [126]. These methods were based on fuzzy logic [127], *ANN* [128], and the swarm intelligence and their modifications, such as *PSO* [129–132], firefly algorithm [133], artificial bee colony algorithm [134], *GWO* algorithm [135], and bat algorithm [136], etc. Due to the simplicity of design and implementation, *PSO* and its variants have been explored extensively for *GMPP* tracking in *PV* systems. A *PSO* based centralized *MPPT* controller [129] was proposed for a multi-module *PV* system having multiple converters. The direct duty cycle control method [130] utilized the *PSO* based *MPPT* algorithm to regulate the duty cycle of the *PWM* signal and to eliminate *PI* control loops. There are twin drawbacks of using conventional *PSO* for *MPPT*: large convergence time due to low-velocity particles and divergence due to high-velocity updated particles. To overcome these difficulties [131, 132], the traditional *PSO* was modified by linearly decreasing the inertia weight and the cognitive parameter while linearly increasing the social parameter [131], while the swarm size was decreased when solution approached the *GMPP* [132].

Two-stage methods were formulated employing traditional approaches [137–139] and soft-computing techniques [140, 141] to find the true *GMPP* under *PSC*. The basic principle in these methods is first to move the operating point near to the *GMPP* and then the actual position of the *GMPP* is to be discovered. The algorithm [138] utilized a linear function to estimate the position of *GMPP* and the *INC* method to find the true *GMPP*. A scanning method [139] was

employed to estimate *GMPP*, while the true *GMPP* was attained using a fitted quadratic function. The *ANN* was used to approximate the *GMPP* and then the *P&O* to achieve the true *GMPP* [140]. Differential flatness control was explored to find the *GMPP* under *PSC* and then fuzzy logic control was employed to track the exact *GMPP* [141]. For the implementation, these two-stage methods require prior information and additional sensors to realize *MPPT* [142].

For improving the search speed with less steady-state oscillations, *MPPT* methods [143–149] utilized bionic swarm algorithms. Deterministic *PSO* updated the velocity deterministically without using random numbers and used *INC* to search in the local mode [143]. However, due to the removal of randomization, the key benefit of an evolutionary algorithm was lost, and it may not find the *GMPP* in all instances. The *P&O*, in conjunction with *PSO*, was used to search first *Local Maximum Power Point (LMPP)* then the *GMPP*, respectively [144]. Due to this, the search space for *PSO* was significantly reduced in the initial iterations. *Differential Evolution (DE)* was combined with *PSO* to add diversification [145]. The *PSO* was utilized in odd iterations, while *DE* was employed in even iterations. The method [146] used *Lagrange Interpolation (LI)* to search near the *MPP* region and *PSO* to obtain the true *GMPP*. The velocity term of *PSO* was updated using Lévy flight, resulting in reduced convergence time and decreased tracking and steady-state oscillations [147]. In the *P&O* integrated *Ant Colony Optimization (ACO)*, the *ACO* was utilized for the global search and *P&O* for the local search. The method [149] combined *P&O* with *GWO* for improving the convergence time. The *GWO* was used in the early phases, while the *P&O* algorithm was employed at the final stage.

The *PSO* is characterized by increased settling time as its main limitation, although it ensures global convergence. This is because the velocity and position of the best particle are also getting updated to explore the solution space. Further, the hybrid methods [143–149] improve convergence time and steady-state performance but suffer from higher complexity and randomness.

2.7 IDENTIFIED RESEARCH AREAS

After a comprehensive review of the *QZS* inverter, the following areas have been identified for further investigations in this research work:

- It is evident that in the *ISI* topologies, the *PDV* is pulsating due to the insertion of *ST* states. Several *PDV* regulation schemes have been reported in the literature. The previously

proposed control methods suffer from limitations such as poor performance, increased cost owing to specially designed circuits, and the voltage across the elements is also unapparent. Therefore, a new control strategy is needed to control the *PDV* at the reference value while eliminating these drawbacks.

- It is identified that the *3L NPC* inverter provides an improved performance in comparison to the two-level counterparts in terms of reduction in semiconductor voltage stress, decrease in switching frequency, lower $\mathrm{d}v/\mathrm{d}t$, and better harmonic performance. However, the *3L NPC* inverter can perform only buck function. By integrating the *QZS* to traditional *NPC* inverter topology, a single-stage buck/boost *3L NPC-QZS* inverter was investigated. But, according to the best knowledge of the author, no work has been reported on a 3-Φ grid-tied *NPC-QZS* inverter for *PV* applications.

- New *ISI* topologies are still being established due to three primary motivations: reducing the component count and rating of the impedance source network, improvement in voltage boost range, and application-oriented optimization and enhancement. There is enough scope for research on inverter topology that can enhance the low *PV* voltage to the required level, with a reduced size of the passive components for grid-tied application.

- As reported in the literature, the traditional *MPPT* techniques fail to detect the *MPP* in *PSC*. To overcome the limitation of conventional *MPPT* algorithms, various evolutionary methods have been presented. New *MPPT* algorithms are still being explored to improve previously investigated *MPPT* techniques and achieve performance indices such as higher tracking efficiency, non-oscillatory steady-state response, and lower transients. Consequently, research work can be performed to conceptualize on *MPPT* algorithm to locate the *GMPP* in the event of *PSC*.

2.8 RESEARCH CONTRIBUTIONS

The investigations have been carried out in the identified research areas to achieve the research objectives. The specific contributions to accomplish those research objectives are presented herewith and these different contributions are interpreted with simple schematics in Fig. 2.1.

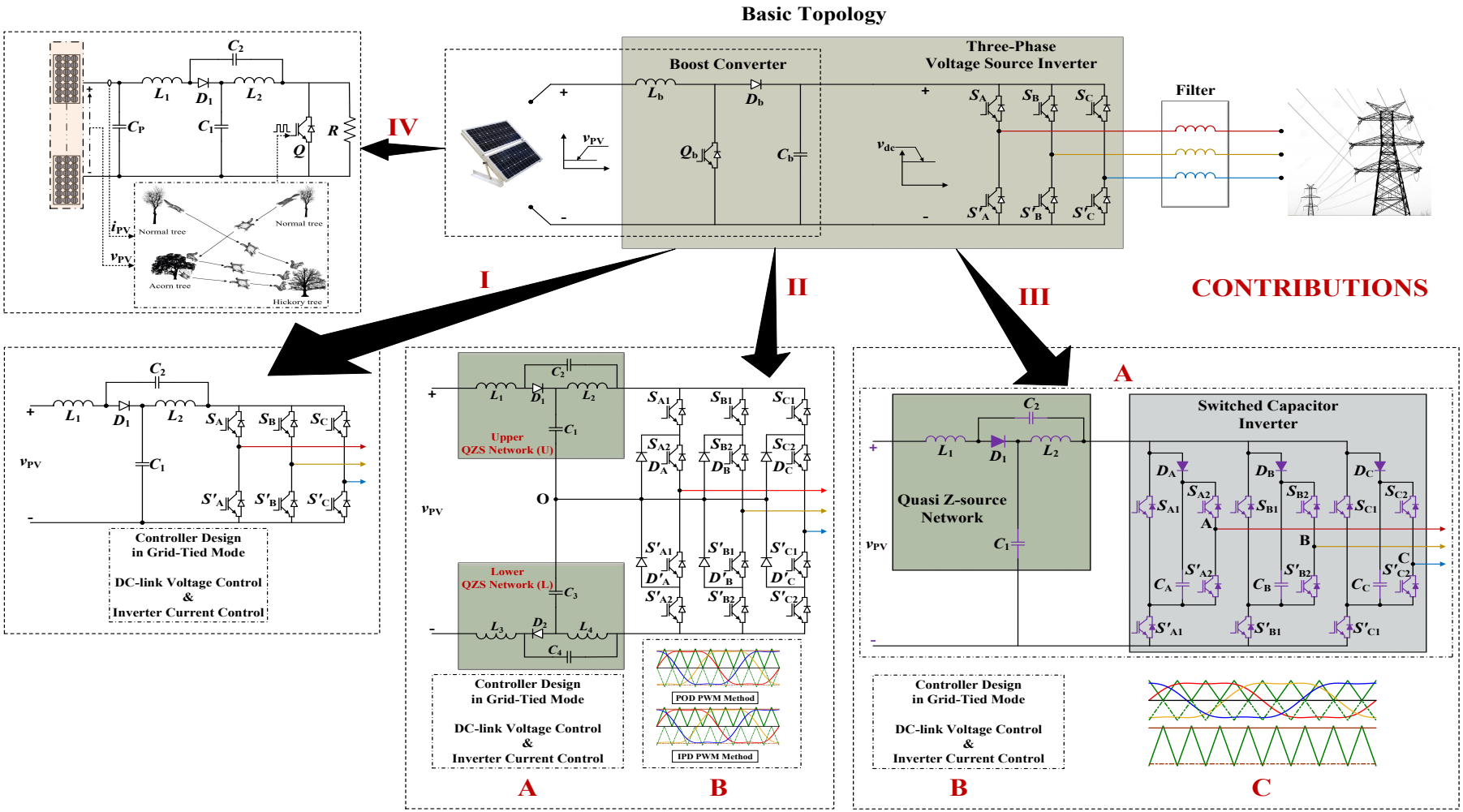

Fig. 2.1: An illustrative schematic of contributions to Thesis

1. ***QZS* inverter based three-phase grid-tied *PV* system**

- The investigated approach to indirectly determine and regulate the *PDV* via voltage across *QZS* network capacitors overcomes the disadvantages of capacitor voltage control and direct control techniques. In this context, the *ST* duty ratio to *PDV* transfer function is derived.
- A performance analysis was also accomplished, taking into account the time delays in the AC- and DC-side control loops. With time delays in control loops, a degraded transient response and extended settling time were detected.
- The efficacy of the suggested regulators is compared with linear and robust controllers. Response of *TOIL* and *PID* is underdamped while response of *SMC* is highly damped. In the steady-state, *TOIL* and *PID* achieves *ZSSE*, however *SMC* has a non-*ZSSE* characteristic behavior. The transient behavior of *TOIL* and *PID* is almost the same but switching ripple in *ST* duty ratio are more in *PID* control. For the AC-side, damped-*SOGI* tracks sinusoidal command effectively while *PI* controller results in magnitude attenuation/ phase delay.
- It is also concluded that the proposed controller is sufficiently reliable to tolerate ±25% of the change in *LC* component values.

2. **Three-level *NPC-QZS* inverter based three-phase grid-tied *PV* system**

- For AC- and DC-sides, different regulators are formulated based on the frequency response technique. Damped-*SOGI* and *IDL* regulators are employed as AC- and DC-side controllers, respectively. The DC-side controller is programmed to regulate the *PDV* by utilizing the *ST* duty ratio to *PDV* transfer function.
- With the addition of a pole, the regulators are adjusted to decrease the corresponding gains at high frequencies and provide a filtering effect on the harmonic content of transmitted signals.
- To mitigate the impact of *Right-Half-Plane Zero (RHPZ)* of *ST* duty ratio to *PDV* transfer function, the gain crossover frequency of DC-side is chosen to be lower than the folding frequency presented by it.
- Due to the pulsed behavior of *PDV*, it has been evaluated and controlled indirectly through *QZS* network capacitors voltage.

- Based on the *POD* and *IPD* techniques, the *PWM* strategies are altered to achieve *ST* utilizing the third harmonic injected *MCBC*. The *POD* method is noticed to be superior concerning reduced *CMV* and zero average neutral point current.
- The performance of *IDL*-damped-*SOGI* compensator is compared with the *SMC*-damped-*SOGI* controller. It is observed that the *IDL*-damped-*SOGI* configuration is efficient and results in *ZSSE* and lower transients during the change in *Weather Conditions (WCs)*.

3. ***QZS-SC* inverter based three-phase grid-tied *PV* system**

- The *QZS* network provides an additional boost stage between the *PV* and *SC* inverter, in addition to flexibility in control through the *ST* duty ratio, and limits start-up and charging current.
- For the same working parameters, the *SC* inverter configuration reduces the size of the inductor of the *QZS* network.
- A two-stage control structure is employed, in which the DC-link voltage is controlled at the reference value using the *ST* duty ratio, and a damped-*SOGI* controller regulates the inverter current.
- In order to produce the gating pulses to control semiconductor switches, a new *PWM* technique has been investigated.
- For the *QZS-SC* inverter topology, the design procedures and voltage/current stresses of switches are also discussed.

4. **Flying squirrel search optimization algorithm for *MPPT* under *PSC***

- The new *MPPT* algorithm, based on the *FSSO* technique, which is used without the presence of a predator, leads to faster convergence towards *GMPP*.
- It is observed that for all instances, *FSSO* always detects *GMPP*. Therefore, its tracking efficiency is maximum in comparison to *P&O*, *PSO*, and *GWO*.
- Though the technique is implemented using a *QZS* converter, the method is universal and can be easily generalized to other converter configurations.
- The realization is performed on the *PV* system with various series- and/or parallel-configuration of *PV* arrays; the technique can be viewed as system independent.

Chapter–3

QZS Inverter Based Three-phase Grid-tied PV System

3.1 GENERAL

Grid-tied *PV* systems are receiving much attention due to simplicity and low operating and maintenance cost. However, these systems require a power converter interface to generate suitable power. The *VSI* that has been traditionally used for the purpose suffers from the disadvantages:

- Due to the intermittent and stochastic nature of the *PV* source arising due to the partial shading or change in weather conditions, the DC-link voltage fluctuates and thus requires the over-sized inverter or the DC-DC boost converter [6].
- Dead-time is required between the upper and lower device of each phase leg.

Among various topologies that have been proposed to cope with the problems mentioned above, *QZS* inverter appeared to be advantageous for *PV* system due to voltage boost and inversion in single-stage, no dead-time requirement between switches of a bridge leg, capable of handling wide input DC voltage variation, and drawing constant current from the source.

Due to the above advantages, *QZS* inverter has been investigated for the grid-tied *PV* system applications. For inverter operation, *PDV* ought to be consistent, which otherwise is pulsating for the *QZS* inverter. The AC-side current needs to be controlled for grid-tied system to regulate real and reactive power.

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* "TOIL and damped-SOGI control of quasi-Z-source inverter based grid-connected renewable-system," in *Control Engineering Practice*, vol. 90, pp. 267-284, 2019.
doi: https://doi.org/10.1016/j.conengprac.2019.07.004.
* "A novel strategy for indirect control of peak DC-link voltage of grid-connected qZS inverter fed through renewable energy sources," in *Electrical Engineering*, vol. 102, pp. 611-625, 2020.
doi: https://doi.org/10.1007/s00202-019-00897-4.

Various researchers contributed the efforts to control *PDV* through controlling the battery current [49], measurement of capacitor voltage [104], its direct measurement [97], and capacitor voltage control [103]. The capacitor voltage was controlled to produce *ST* states [30]. The equivalent DC-link voltage was derived by sensing the voltage of one capacitor and *ST* time [100]. The input and capacitor voltages were measured to estimate the *PDV* [101, 102]. The *ZSSE* was achieved without an inner inductor current loop and the DC-link voltage reference was calculated with the help of its average value [110]. The DC-link voltage was controlled [111] by changing the current component of active power. These methods characterize the following drawbacks:

1. The voltage stress across devices is unapparent in capacitor voltage control, thereby restricting the *ST* duty ratio. Further, the *PDV* increases and AC-output voltage is distorted for step input increase.

2. In the direct control of *PDV*, additional circuitry is required to measure the DC-link voltage.

There are various strategies for regulating AC-side current. The *PI* controller can track the DC signal but cannot track sinusoidal current with *ZSSE* and have poor disturbance rejection capability [154]. The deadbeat current controller generates a tracking error and stability problem [155]. Although the hysteresis current controller provides *ZSSE*, the switching frequency depends on load parameters and AC voltage [156]. A damped-*SOGI* achieves high gain at a particular frequency. It characterizes the higher convergence rate, improved steady-state performance, and good disturbance rejection capacity and thus suited for grid application [157].

The motivation for this chapter is to realize the AC-side current controller enabling *ZSSE* and DC-side *PDV* controller capable of addressing the drawbacks of the capacitor voltage and direct control methods as highlighted above.

A strategy is proposed in this chapter to indirectly control the *PDV* of *QZS* inverter fed grid-connected *PV* system by sensing the voltages of *QZS* network capacitors. For this purpose, the mathematical model is developed for *QZS* inverter based 3-Φ grid-tied *PV* system, which is depicted in Fig. 3.1. The AC- and DC-sides are modeled separately and the crossover frequency of the AC-side control loop is kept high to avoid intruding with the DC-side. A *TOIL* controller is realized to regulate *PDV* and minimize the *NMP* characteristic effect of *ST* duty ratio to *PDV* transfer function. A damped-*SOGI* offering high power frequency gain

is used to control the inverter current and attain *ZSSE*. The impact of time-delay in control is also analyzed. The performance of the proposed *TOIL* and damped-*SOGI* controllers is compared with other designed linear and sliding mode controllers. The system is investigated using MATLAB/Simulink and validated through *HIL RTS* in OPAL-RT and experimentation on a practical setup in the laboratory.

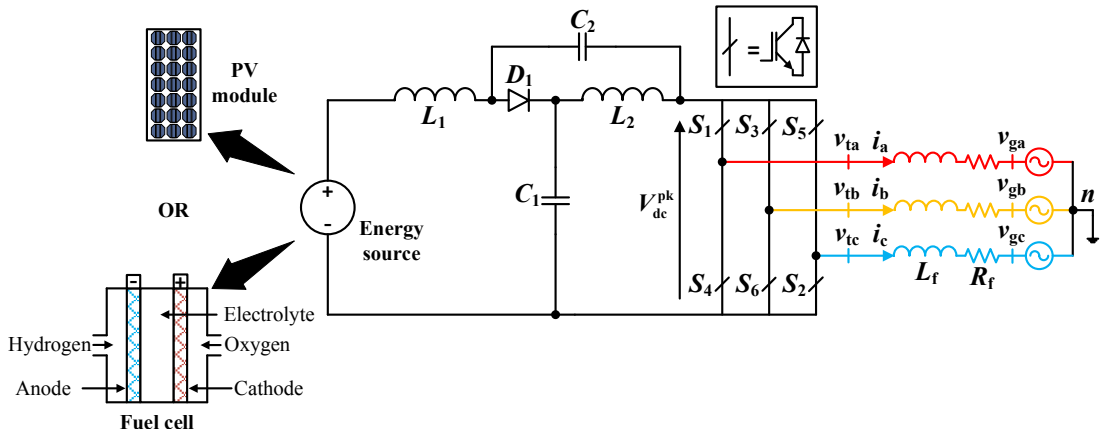


Fig. 3.1: Schematic of grid-tied 3-Φ *QZS* inverter for *RES*.

3.2 MODELING OF *QZS* NETWORK

For single-stage control strategy, AC- and DC-sides are decoupled. The H-bridge inverter is represented as a single switch S and parallel current source i_{dc} [158]. The mathematical model of the DC-side of *QZS* inverter, as shown in Fig. 3.1, is developed using large-and small-signal analysis under the following assumptions:

- The passive elements of *QZS* network are assumed to be equal, $L_1 = L_2 = L$ and $C_1 = C_2 = C$.
- The *QZS* inverter is operating in *CCM*.
- Lossy inductors and capacitors of *QZS* network encompass winding resistance R_L and *Equivalent Series Resistance (ESR)* R_C, respectively.
- The diode D_1 and switch S are assumed to be ideal.

The two operating modes are recognized in the *QZS* inverter operation, which are represented through two distinctive equivalents in Fig. 3.2. In *ST* state, as shown in Fig. 3.2(a), load side is decoupled from the source by non-conducting diode D_1 and conducting switch S.

Therefore, no energy is exchanged from the source to load and electrostatic energy stored in $C_1,\ C_2$ is transferred to the magnetic energy of $L_1,\ L_2$. Duration of *ST* interval is defined as T_{st}.

In *NST* state, as shown in Fig. 3.2(b), diode D_1 conducts while switch *S* does not conduct. Therefore, the energy source charges the capacitors and powers the load. Inductors additionally discharge their energy to the load, thus boost the DC-link voltage v_{dc}. Duration of *NST* interval is characterized as T_{nst}.

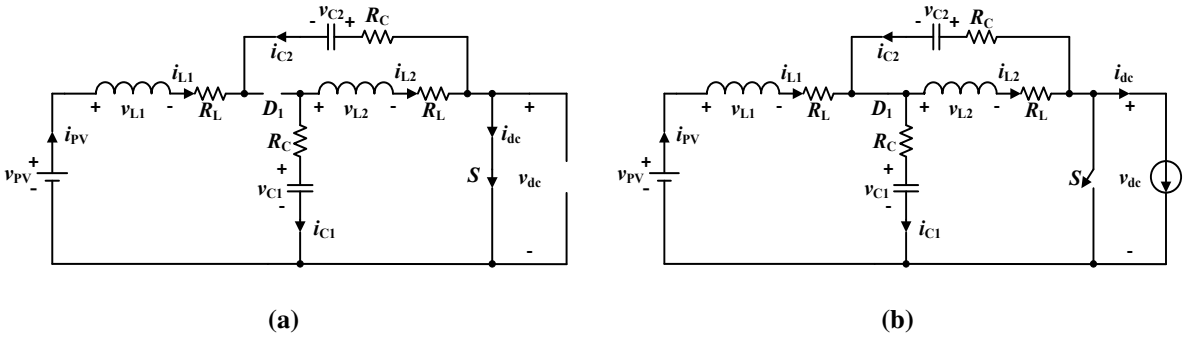


Fig. 3.2: Equivalent circuit of *QZS* inverter. **(a)** *ST* state. **(b)** *NST* state.

For the system, the state vector $\boldsymbol{x}$ and input vector $\boldsymbol{u}$ are expressed as:

$$\boldsymbol{x} = \begin{bmatrix} i_{\text{L1}} & i_{\text{L2}} & v_{\text{C1}} & v_{\text{C2}} \end{bmatrix}^{\text{T}} \qquad \boldsymbol{u} = \begin{bmatrix} v_{\text{PV}} & i_{\text{dc}} \end{bmatrix}^{\text{T}} \tag{3.1}$$

The state space form $\dot{\boldsymbol{x}} = \boldsymbol{A_0 x} + \boldsymbol{B_0 u}$, where $(\dot{})$ represents d/dt, of differential equations in *ST* mode is written as:

$$\frac{d}{dt}\begin{bmatrix} i_{\text{L1}} \\ i_{\text{L2}} \\ v_{\text{C1}} \\ v_{\text{C2}} \end{bmatrix} = \begin{bmatrix} -\frac{(R_{\text{L}}+R_{\text{C}})}{L} & 0 & 0 & \frac{1}{L} \\ 0 & -\frac{(R_{\text{L}}+R_{\text{C}})}{L} & \frac{1}{L} & 0 \\ 0 & -\frac{1}{C} & 0 & 0 \\ -\frac{1}{C} & 0 & 0 & 0 \end{bmatrix}\begin{bmatrix} i_{\text{L1}} \\ i_{\text{L2}} \\ v_{\text{C1}} \\ v_{\text{C2}} \end{bmatrix} + \begin{bmatrix} \frac{1}{L} & 0 \\ 0 & 0 \\ 0 & 0 \\ 0 & 0 \end{bmatrix}\begin{bmatrix} v_{\text{PV}} \\ i_{\text{dc}} \end{bmatrix} \tag{3.2}$$

Similarly, the state space form $\dot{\boldsymbol{x}} = \boldsymbol{A_1 x} + \boldsymbol{B_1 u}$ of differential equations in *NST* state is written as:

$$\frac{d}{dt}\begin{bmatrix} i_{\text{L1}} \\ i_{\text{L2}} \\ v_{\text{C1}} \\ v_{\text{C2}} \end{bmatrix} = \begin{bmatrix} -\frac{(R_{\text{L}}+R_{\text{C}})}{L} & 0 & -\frac{1}{L} & 0 \\ 0 & -\frac{(R_{\text{L}}+R_{\text{C}})}{L} & 0 & -\frac{1}{L} \\ \frac{1}{C} & 0 & 0 & 0 \\ 0 & \frac{1}{C} & 0 & 0 \end{bmatrix}\begin{bmatrix} i_{\text{L1}} \\ i_{\text{L2}} \\ v_{\text{C1}} \\ v_{\text{C2}} \end{bmatrix} + \begin{bmatrix} \frac{1}{L} & \frac{R_{\text{C}}}{L} \\ 0 & \frac{R_{\text{C}}}{L} \\ 0 & -\frac{1}{C} \\ 0 & -\frac{1}{C} \end{bmatrix}\begin{bmatrix} v_{\text{PV}} \\ i_{\text{dc}} \end{bmatrix} \tag{3.3}$$

The (3.2) and (3.3) are combined through the state space averaging over one switching period T_s to yield resulting dynamic state equations as:

$$\dot{\boldsymbol{x}} = \boldsymbol{Ax} + \boldsymbol{Bu} \qquad \text{and} \qquad \boldsymbol{y} = \boldsymbol{Cx} + \boldsymbol{Eu} \tag{3.4}$$

where $\boldsymbol{A} = d_{st}\boldsymbol{A_0} + d_{nst}\boldsymbol{A_1}$, $\boldsymbol{B} = d_{st}\boldsymbol{B_0} + d_{nst}\boldsymbol{B_1}$, and $\boldsymbol{y}$ is output vector. Characterizing the system output vector to be same as state vector, i.e. $\boldsymbol{y} = \boldsymbol{x}$, suggests $\boldsymbol{C} = \boldsymbol{I}$ (identity matrix) and $\boldsymbol{E} = \boldsymbol{0}$ (null matrix).

The duty ratio of switch S, defined as *ST* duty ratio, is $d_{st} = T_{st}/T_s$, while the duty ratio of D_1 described as the *NST* duty ratio, is $d_{nst} = T_{nst}/T_s = (1 - d_{st})$. The input voltage v_{PV}, disturbance input i_{dc}, and *ST* duty ratio d_{st}, are perturbed as $v_{PV} = V_{PV} + \tilde{v}_{PV}$, $i_{dc} = I_{dc} + \tilde{i}_{dc}$, and $d_{st} = D_{st} + \tilde{d}_{st}$ which yield perturbation in state variables, i.e., $\boldsymbol{x} = \boldsymbol{X} + \tilde{\boldsymbol{x}}$. After ignoring the product of higher order terms, the resulting small-signal state equations are expressed as:

$$\frac{d\tilde{\boldsymbol{x}}}{dt} = (D_{st}\boldsymbol{A_0} + D_{nst}\boldsymbol{A_1})\tilde{\boldsymbol{x}} + (D_{st}\boldsymbol{B_0} + D_{nst}\boldsymbol{B_1})\tilde{\boldsymbol{u}} + \{(\boldsymbol{A_0} - \boldsymbol{A_1})\boldsymbol{X} + (\boldsymbol{B_0} - \boldsymbol{B_1})\boldsymbol{U}\}\tilde{d}_{st} \tag{3.5}$$

where "~" denote perturbed quantities.

The steady-state values of capacitor voltage and inductor current can be acquired by equating first derivative of state variable in (3.4) to zero as:

$$\boldsymbol{X} = \begin{bmatrix} I_{L1} \\ I_{L2} \\ V_{C1} \\ V_{C2} \end{bmatrix} = \begin{bmatrix} 0 & B_z D_{nst} \\ 0 & B_z D_{nst} \\ B_z D_{nst} & -B_z^2 D_{nst}(R_L + 2R_C D_{st}) \\ B_z D_{st} & -B_z^2 D_{nst}(R_L + 2R_C D_{st}) \end{bmatrix} \begin{bmatrix} V_{PV} \\ I_{dc} \end{bmatrix} \tag{3.6}$$

where *NST* duty ratio D_{nst} and the boost factor B_z are defined as:

$$D_{nst} = 1 - D_{st} \qquad \text{and} \qquad B_z = \frac{1}{(1 - 2D_{st})}. \tag{3.7}$$

By referring Fig. 3.2, DC-link voltages in the *ST* and *NST* states are expressed as:

$$\begin{cases} v_{dc} = 0 \\ v_{dc} = v_{C1} + v_{C2} + R_C(i_{L1} + i_{L2} - 2i_{dc}) \end{cases} \tag{3.8}$$

In steady-state condition, the average and peak DC-link voltage V_{dc}^{av} and V_{dc}^{pk}, can be determined from (3.6) and (3.8) as:

$$\begin{bmatrix} V_{dc}^{av} \\ V_{dc}^{pk} \end{bmatrix} = \begin{bmatrix} B_z D_{nst} & -2B_z^2 D_{nst}(R_L D_{nst} + R_C D_{st}) \\ B_z & -2B_z^2(R_L D_{nst} + R_C D_{st}) \end{bmatrix} \begin{bmatrix} V_{PV} \\ I_{dc} \end{bmatrix} \tag{3.9}$$

The V_{dc}^{pk} is the equivalent DC-link voltage of the inverter. With the consideration of modulation index M, peak AC-side terminal voltage of *QZS* inverter is obtained as [12]:

$$V_M = \frac{1}{2} M V_{dc}^{pk} \tag{3.10}$$

3.3 CONTROLLER DESIGN

The principal control scheme of grid-connected *PV* system based on *QZS* inverter is shown in Fig. 3.3. The procedure to design the *QZS* network parameters is described in appendix A. Correspondingly, the design values are summarized in Table 3.1. As AC-side dynamics are faster compared with the DC-side dynamics [99], gain crossover frequency at AC-side is selected higher than DC-side. The damped-*SOGI* controller is proposed for tracking AC-side sinusoidal reference current with *ZSSE*, while the *TOIL* controller is proposed for indirect estimation and control of *PDV*.

Table 3.1. Summary of designed 3-Φ *QZS* inverter parameters

Parameter	**Values**
QZS network inductances (L_1 and L_2)	2 mH
Winding resistance of L_1, L_2 (R_{L1} and R_{L2})	0.1 Ω
QZS network capacitances (C_1 and C_2)	1000 μF
ESR of C_1, C_2 (R_{C1} and R_{C2})	0.01 Ω
AC-side filter inductance (L_f)	3 mH
Winding resistance of L_f (R_f)	0.1 Ω
Grid *RMS* voltage (phase-neutral)	120 V
Angular grid frequency (ω_g)	2π (50 Hz)
Switching frequency (f_s)	10 kHz

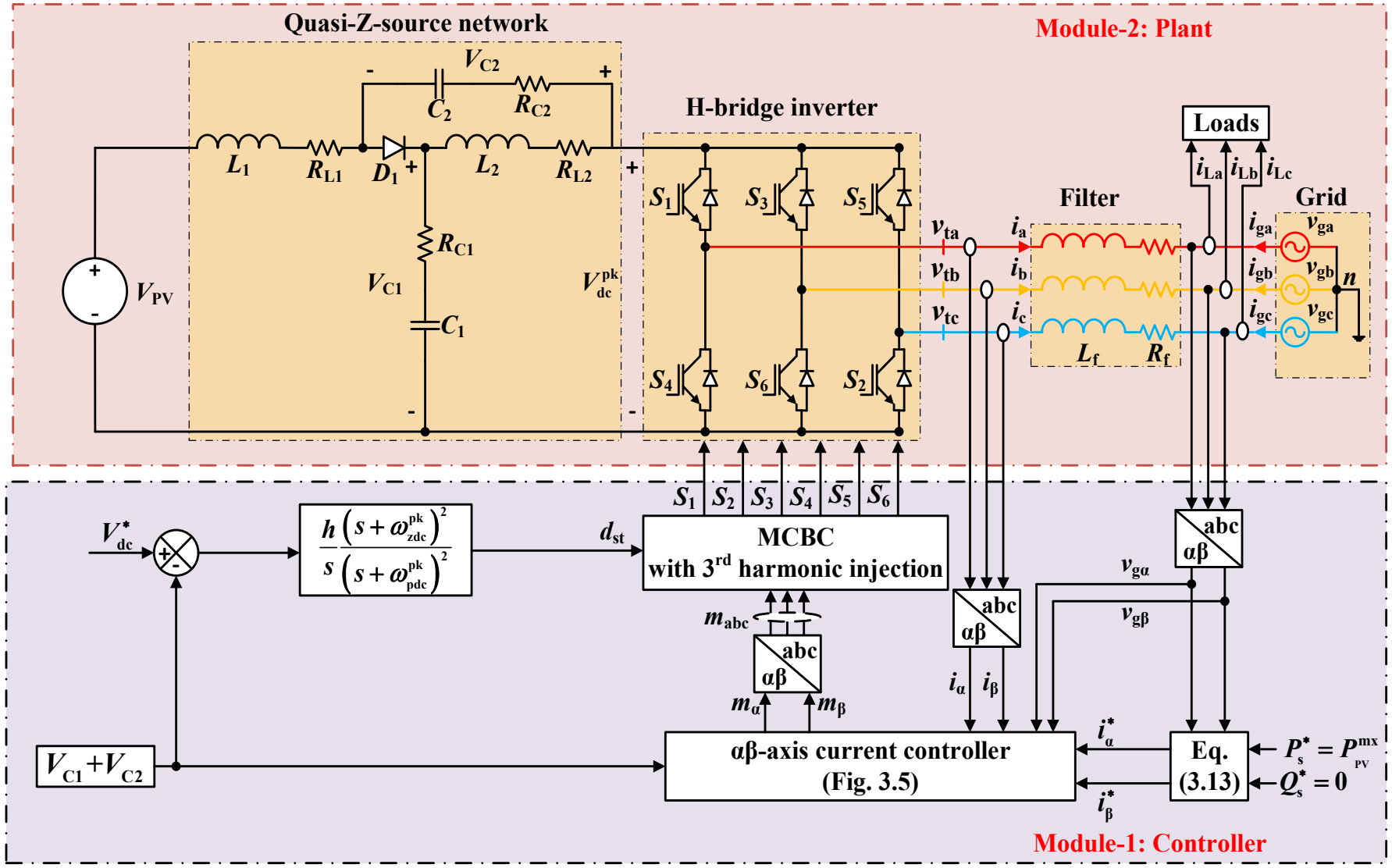


Fig. 3.3: The control strategy for *QZS* inverter based grid-tied *PV* system.

3.3.1 Design of damped-*SOGI* controller for AC-side

Applying Kirchoff's voltage law to all phases of Fig. 3.1, as:

$$L_{\mathrm{f}}\frac{\mathrm{d}i_{\mathrm{abc}}}{\mathrm{d}t} = v_{\mathrm{tabc}} - v_{\mathrm{gabc}} - R_{\mathrm{f}}i_{\mathrm{abc}} \tag{3.11}$$

The inductance is inherently present in the transmission line and that is why L-filter (L_{f}) is considered.

The state equation (3.11) is transformed in the $\alpha\beta$ domain as control in $\alpha\beta$-frame does not require synchronization mechanism as needed in dq-frame [159]. By using (3.10), the transformed equations are written as:

$$\begin{cases} L_{\mathrm{f}}\dfrac{\mathrm{d}i_{\alpha}}{\mathrm{d}t} = \dfrac{1}{2}m_{\alpha}V_{\mathrm{dc}}^{\mathrm{pk}} - v_{\mathrm{g}\alpha} - R_{\mathrm{f}}i_{\alpha} \\ L_{\mathrm{f}}\dfrac{\mathrm{d}i_{\beta}}{\mathrm{d}t} = \dfrac{1}{2}m_{\beta}V_{\mathrm{dc}}^{\mathrm{pk}} - v_{\mathrm{g}\beta} - R_{\mathrm{f}}i_{\beta} \end{cases} \tag{3.12}$$

where m_{α}, $v_{\mathrm{g}\alpha}$, and i_{α} are α-axis components and m_{β}, $v_{\mathrm{g}\beta}$, and i_{β} are β-axis components of modulation index, grid voltage, and inverter current, respectively.

The AC-side current is regulated at the predetermined reference value by adjusting real power reference P_{s}^{*} to the *MPP* and reactive power reference Q_{s}^{*} to zero to achieve *UPF* operation. Thus, for the known grid side voltage v_{gabc}; P_{s}^{*} and Q_{s}^{*}; i_{α}^{*} and i_{β}^{*} are calculated from the instantaneous power theory [160] as:

$$\begin{bmatrix} i_{\alpha}^{*} \\ i_{\beta}^{*} \end{bmatrix} = \frac{2}{3}\frac{1}{v_{\mathrm{g}\alpha}^{2} + v_{\mathrm{g}\beta}^{2}} \begin{bmatrix} v_{\mathrm{g}\alpha} & v_{\mathrm{g}\beta} \\ v_{\mathrm{g}\beta} & -v_{\mathrm{g}\alpha} \end{bmatrix} \begin{bmatrix} P_{\mathrm{s}}^{*} \\ Q_{\mathrm{s}}^{*} \end{bmatrix} \tag{3.13}$$

In the $\alpha\beta$-frame, i_{α}^{*} and i_{β}^{*} are periodic quantities. The tracking of the periodic signal is accomplished through the *Internal Model Principle (IMP)*. The *IMP* suggests that it is adequate to incorporate the model of the disturbance inside the controller to guarantee command tracking with *ZSSE*. The more direct application of the *IMP* is *SOGI*, which accomplishes infinite gain at the resonance frequency. The practical *SOGI* is expressed as:

$$K_{\mathrm{SOGI}}^{\mathrm{Damp}}(s) = K_{\mathrm{ac}}(s) = K_{\mathrm{SP}} + \frac{2K_{\mathrm{SI}}\omega_{\mathrm{ac}}^{\mathrm{cut}}s}{s^{2} + 2\omega_{\mathrm{ac}}^{\mathrm{cut}}s + \omega_{\mathrm{g}}^{2}} \tag{3.14}$$

where $\omega_{\mathrm{ac}}^{\mathrm{cut}}$ is the cut-off frequency ($\omega_{\mathrm{ac}}^{\mathrm{cut}} \ll \omega_{\mathrm{g}}$), ω_{g} is angular grid frequency, and K_{SP}, K_{SI} are the constants of the damped-*SOGI* controller.

The *Bandwidth (BW)* of the closed loop control system should be sufficiently smaller than the inverter switching frequency [159]. Therefore, the target gain crossover frequency $\omega_{\text{ac}}^{\text{gc}}$ of 2π(1 kHz) is selected for the converter switching frequency of 10 kHz, a *Phase Margin (PM)* of 60°, and $\omega_{\text{ac}}^{\text{cut}}$ as 2π(10 Hz).

Transfer function for the AC-side of the inverter is obtained using (3.12), as:

$$G_{\text{ac}}(s) = \frac{1}{L_{\text{f}}s + R_{\text{f}}} \tag{3.15}$$

Using (3.14) and (3.15), the loop gain for the current control can be defined as:

$$l_{\text{ac}}(s) = K_{\text{ac}}(s)G_{\text{ac}}(s) \tag{3.16}$$

The gains K_{SP} and K_{SI} of (3.14) are calculated at the desired $\omega_{\text{ac}}^{\text{gc}}$ as:

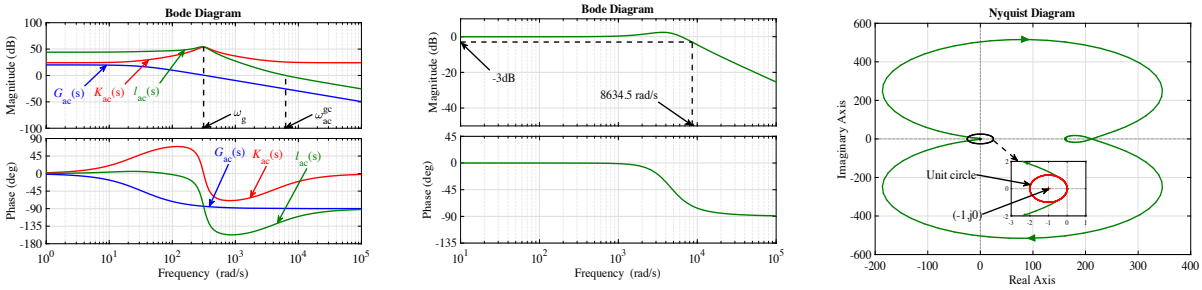
$$l_{\text{ac}}(j\omega)\big|_{\omega=\omega_{\text{ac}}^{\text{gc}}} = K_{\text{ac}}(j\omega)G_{\text{ac}}(j\omega)\big|_{\omega=\omega_{\text{ac}}^{\text{gc}}} = 1e^{-j(120^\circ)} \tag{3.17}$$

This results in $K_{\text{SP}} = 16.084$ and $K_{\text{SI}} = 474.086$. With all the parameters known for the compensator, the final compensator $K_{\text{ac}}(s)$ is given as (3.18). The corresponding frequency response of the damped-*SOGI* controller gain $K_{\text{SOGI}}^{\text{Damp}}(s)$ is shown in Fig. 3.4(a), which suggests a high gain at the grid frequency 2π(50 Hz).

$$K_{\text{ac}}(s) = K_{\text{ac}}^{\alpha\beta}(s) = 16.084 + \frac{59640.796s}{s^2 + 125.664s + 314.16^2} \tag{3.18}$$

The loop gain $l_{\text{ac}}(s)$ for compensator (3.18), shown in Fig. 3.4(a), suggests a *PM* of 60° at $\omega_{\text{ac}}^{\text{gc}}$. The corresponding closed-loop frequency response is shown in Fig. 3.4(b), which suggests that there is no attenuation/phase shift for the frequency well beyond the $\omega_{\text{ac}}^{\text{gc}}$. Thus, the response correlates with the design requirement. The system will operate stably as Nyquist plot for $l_{\text{ac}}(s)$, shown in Fig. 3.4(c), does not encircle the critical point $(-1, j0)$ and there is no pole in the right-half-plane of the $l_{\text{ac}}(s)$ [161].

The current controller output is divided by $(V_{\text{C1}} + V_{\text{C2}})/2$ (or $V_{\text{dc}}^{\text{pk}}/2$) to obtain the modulating signal and to compensate for the converter voltage gain. A feed-forward compensation $G_{\text{ff}}(s) = 1/(5 \times 10^{-6}s + 1)$ is utilized to avoid start-up transient, to decouple dynamics of the converter system from the grid, and to enhance the disturbance rejection capability. Using compensator (3.18) for both α-and β-axis current control, the schematic of the AC-side current control loop is shown in Fig. 3.5.



(a) **(b)** **(c)**

Fig. 3.4: Frequency response of the grid-tied current control. **(a)** Open-loop Bode plot of $G_{ac}(s)$, $K_{ac}(s)$, and $l_{ac}(s)$. **(b)** Closed-loop Bode plot. **(c)** Nyquist plot of $l_{ac}(s)$.

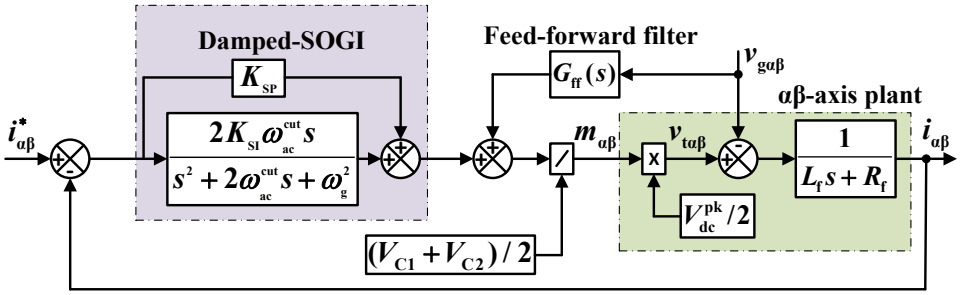


Fig. 3.5: Block diagram of the current control loop in $\alpha\beta$-frame.

3.3.2 Design of *TOIL* for DC-side

The *TOIL* controller is proposed on DC-side for indirectly estimating and regulating the *PDV*. The DC-link voltage v_{dc} is zero in the *ST* state. It attains the peak value equal to V_{dc}^{pk} as in (3.9) during the *NST* state. As v_{dc} is a pulsed signal, it is troublesome to measure and control. The indirect control of *PDV* is achieved by detecting the voltages across the *QZS* network capacitors. For the purpose, the *ST* duty ratio to *PDV* transfer function $G_{dc}^{pk}(s)$ is determined. From (3.8), v_{dc}^{pk} is expressed as:

$$v_{dc}^{pk} = v_{C1} + v_{C2} + R_C(i_{L1} + i_{L2} - 2i_{dc}) \tag{3.19}$$

The perturbation and linearization is applied to v_{dc}^{pk}. After neglecting the higher order terms and taking Laplace transformation, it results as:

$$\tilde{v}_{dc}^{pk}(s) = \tilde{v}_{C1}(s) + \tilde{v}_{C2}(s) + R_C(\tilde{i}_{L1}(s) + \tilde{i}_{L2}(s) - 2\tilde{i}_{dc}(s)) \tag{3.20}$$

$G_{dc}^{pk}(s)$ is obtained by taking Laplace transform of (3.5) and using (3.20) and expressed as:

$$G_{dc}^{pk}(s) = \frac{\tilde{v}_{dc}^{pk}(s)}{\tilde{d}_{st}(s)} = \frac{n_1 s + n_2}{LCs^2 + C(R_L + R_C)s + (D_{nst} - D_{st})^2} \tag{3.21}$$

where the values of the coefficients n_1 and n_2 are:

$$n_1 = 2R_C C(V_{C1} + V_{C2} - R_C I_{dc}) + 2L(I_{dc} - I_{L1} - I_{L2})$$
$$n_2 = 2(D_{nst} - D_{st})(V_{C1} + V_{C2} - R_C I_{dc}) + 2(R_L + 2R_C D_{st})(I_{dc} - I_{L1} - I_{L2})$$

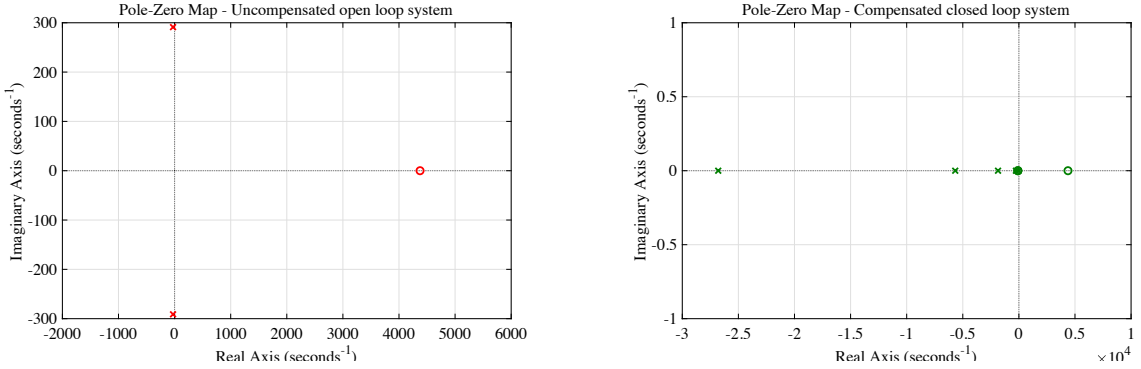
It can be observed that (3.21) is a proper transfer function characterized by *RHPZ*, also known as *NMP* system. It is difficult to design feedback controller with sufficient *PM* for such *NMP* system [162].

In the proposed *PDV* control, voltages across the capacitors C_1 and C_2 are measured and fed-back for comparing with reference voltage V_{dc}^{*} because the voltages across capacitors C_1 and C_2 are not pulsed and the sum of their voltages v_C^{sum} is always equal to *PDV*. The design requirement of decoupled AC- and DC-side control suggests that the crossover frequency of DC-side control loop should be lower than both the crossover frequency of AC-side control loop and folding frequency introduced by *RHPZ* to minimize the effect of *NMP* behavior [163]. To satisfy these conditions, the crossover frequency of *PDV* control loop ω_{dc}^{gc} is selected to be $1/5^{th}$ of ω_{ac}^{gc}, i.e. $\omega_{dc}^{gc} = 2\pi(200\text{ Hz})$, and a *PM* target is set at $PM_{dc}^{pk} = 60°$.

The loop gain $l_{dc}^{pk}(s)$ of *PDV* control loop is defined as:

$$l_{dc}^{pk}(s) = K_{dc}^{pk}(s) G_{dc}^{pk}(s) \tag{3.22}$$

The Pole-Zero plot of $G_{dc}^{pk}(s)$, as shown in Fig. 3.6(a), presents *RHPZ*. Correspondingly, the magnitude and phase Bode plots of $G_{dc}^{pk}(s)$ are shown in Fig. 3.7(a). It suggests that $G_{dc}^{pk}(s)$ has a gain crossover frequency 41443 rad/s, phase crossover frequency 571 rad/s, *PM* −83.9°, and *Gain Margin (GM)* −57.5 dB, thereby indicating an unstable system.



(a) **(b)**

Fig. 3.6: Pole-Zero map of *PDV* control system. **(a)** Uncompensated open-loop. **(b)** Compensated closed-loop.

The DC value of uncompensated loop gain G_{dc0}^{pk}, system resonance frequency ω_{dc0}^{pk}, and location of *RHPZ* ω_{RHPZ} are obtained as:

$$\begin{aligned} G_{dc0}^{pk} &= 66.475 \text{ dB} \\ \omega_{dc0}^{pk} &= \frac{D_{nst} - D_{st}}{\sqrt{LC}} = 2\pi(46.546 \text{ Hz}) \\ \omega_{RHPZ} &= 2\pi(696.359 \text{ Hz}) \end{aligned}$$

At $\omega = \omega_{dc}^{gc}$, $G_{dc}^{pk}(s)$ demonstrates a phase angle $\phi_{G_{dc}^{pk}}$ of $-193.375°$, suggesting that a lead type of compensator is recommended in the vicinity of ω_{dc}^{gc}. The high phase boost can be provided by the *TOIL* controller [164]. The *TOIL* controller has a pole at the origin and two Pole-Zero pairs. The pole at the origin achieves a large gain at low frequencies and introduces $-90°$ phase lag at all frequencies. This phase lag can be alleviated by means of lead part of the controller. The *TOIL* compensator $K_{dc}^{pk}(s)$ is defined as:

$$K_{dc}^{pk}(s) = \frac{h}{s}\frac{(s+\omega_{zdc}^{pk})^2}{(s+\omega_{pdc}^{pk})^2} = \frac{h}{q^2 s}\frac{\left(1+\frac{s}{\omega_{zdc}^{pk}}\right)^2}{\left(1+\frac{s}{\omega_{pdc}^{pk}}\right)^2} \tag{3.23}$$

where $q = \omega_{pdc}^{pk}/\omega_{zdc}^{pk}$. The maximum phase boost ϕ_{mdc}^{pk} is generated at ω_{dc}^{gc} by $K_{dc}^{pk}(s)$. The ω_{dc}^{gc} and ϕ_{mdc}^{pk} are expressed as:

$$\omega_{dc}^{gc} = \sqrt{\omega_{zdc}^{pk}\omega_{pdc}^{pk}} = \sqrt{q}\omega_{zdc}^{pk} = \frac{\omega_{pdc}^{pk}}{\sqrt{q}} \tag{3.24}$$

$$\phi_{mdc}^{pk} = 2\arctan\left(\frac{q-1}{2\sqrt{q}}\right) \tag{3.25}$$

Using (3.22), the value of ϕ_{mdc}^{pk} at ω_{dc}^{gc} can be found for the desired *PM* PM_{dc}^{pk} as:

$$\phi_{mdc}^{pk} = PM_{dc}^{pk} - \phi_{G_{dc}^{pk}} - \frac{\pi}{2} \tag{3.26}$$

The constant h of $K_{dc}^{pk}(s)$ is obtained by imposing unity loop gain at ω_{dc}^{gc} and expressed as:

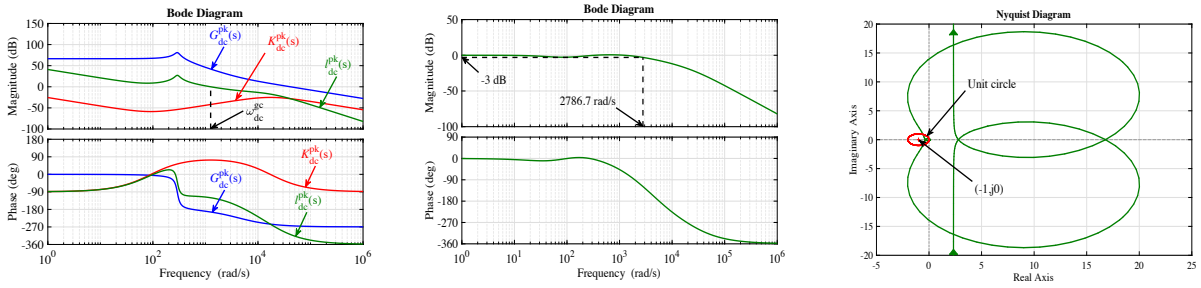
$$h = \frac{q\omega_{dc}^{gc}}{|G_{dc}^{pk}(j\omega_{dc}^{gc})|} \tag{3.27}$$

With the help of (3.24), (3.25), (3.26), and (3.27), the value of ω_{zdc}^{pk}, ω_{pdc}^{pk}, and h are obtained as $2\pi(14.538 \text{ Hz})$, $2\pi(2751.422 \text{ Hz})$, and 1896.107, respectively. Thus, the resulting transfer function of the compensator for *PDV* control can be written as:

$$K_{\text{dc}}^{\text{pk}}(s) = \frac{1896.107(s + 91.345)^2}{s(s + 17287.694)^2} \tag{3.28}$$

By using the compensator (3.28), the loop gain $l_{\text{dc}}^{\text{pk}}(s)$ of the *PDV* control loop is shown in Fig. 3.7(a). It suggests that $l_{\text{dc}}^{\text{pk}}(s)$ has a gain crossover frequency of 1257.2 rad/s, phase crossover frequency 5674.7 rad/s, *PM* 60°, and *GM* 10.5 dB.

With the designed TOIL controller (3.28), the closed-loop frequency response of *PDV* control is shown in Fig. 3.7(b). The Nyquist plot of $l_{\text{dc}}^{\text{pk}}(s)$, shown in Fig. 3.7(c), does not encircle $(-1, j0)$ and has no right-half-plane pole that implies the system is stable. All the poles of the closed-loop system are in the left-half-plane as shown in Fig. 3.6(b), thereby suggesting a stable system.



(a) **(b)** **(c)**

Fig. 3.7: Frequency response of the *PDV* control. **(a)** Open-loop Bode plot of $G_{\text{dc}}^{\text{pk}}(s)$, $K_{\text{dc}}^{\text{pk}}(s)$, and $l_{\text{dc}}^{\text{pk}}(s)$. **(b)** Closed-loop Bode plot. **(c)** Nyquist plot of $l_{\text{dc}}^{\text{pk}}(s)$.

Theorem 1. *The closed loop transfer functions for the AC- and DC-side are obtained by using* (3.16) *and* (3.22)*, respectively, as:*

$$T_{\text{ac}}(s) = \frac{l_{\text{ac}}(s)}{1 + l_{\text{ac}}(s)}$$

$$T_{\text{dc}}^{\text{pk}}(s) = \frac{l_{\text{dc}}^{\text{pk}}(s)}{1 + l_{\text{dc}}^{\text{pk}}(s)}$$

The closed loop transfer functions $T_{\text{ac}}(s)$ and $T_{\text{dc}}^{\text{pk}}(s)$ will be stable if PM and GM of loop gains $l_{\text{ac}}(s)$ and $l_{\text{dc}}^{\text{pk}}(s)$ are positive [165].

Proof. The frequency response for the loop gain of the AC- and DC-side, i.e. $l_{\text{ac}}(s)$ and $l_{\text{dc}}^{\text{pk}}(s)$ as shown in Figs. 3.4(a) and 3.7(a) suggests positive *PM* and *GM* which justifies the stability criteria.

□

3.3.3 Design of *SMC* for DC-side

The *SMC* is well known robust controller, to accomodate parameter variation and external disturbances. *SMC* can not be applied directly to power converter application due to limited switching frequency [52]. For the system entering into sliding mode for required dynamic and steady-state performance hitting, existence, and stability condition should be satisfied. Using (3.2) and (3.3), the state space model in the standard form for DC-side of *QZS* inverter is given as:

$$\dot{\boldsymbol{x}} = \boldsymbol{A}_{\mathbf{s}} + \mathbf{B}_{\mathbf{s}} u \tag{3.29}$$

where

$$\boldsymbol{A}_{\mathbf{s}} = \begin{bmatrix} \frac{1}{L}\{-v_{\mathrm{C1}} - (R_{\mathrm{L}} + R_{\mathrm{C}})i_{\mathrm{L1}} + R_{\mathrm{C}} i_{\mathrm{dc}} + v_{\mathrm{PV}}\} \\ \frac{1}{L}\{-v_{\mathrm{C2}} - (R_{\mathrm{L}} + R_{\mathrm{C}})i_{\mathrm{L2}} + R_{\mathrm{C}} i_{\mathrm{dc}}\} \\ \frac{1}{C}(i_{\mathrm{L1}} - i_{\mathrm{dc}}) \\ \frac{1}{C}(i_{\mathrm{L2}} - i_{\mathrm{dc}}) \end{bmatrix} \qquad \boldsymbol{B}_{\mathbf{s}} = \begin{bmatrix} \frac{1}{L}(v_{\mathrm{C1}} + v_{\mathrm{C2}} - R_{\mathrm{C}} i_{\mathrm{dc}}) \\ \frac{1}{L}(v_{\mathrm{C1}} + v_{\mathrm{C2}} - R_{\mathrm{C}} i_{\mathrm{dc}}) \\ \frac{1}{C}(i_{\mathrm{dc}} - i_{\mathrm{L1}} - i_{\mathrm{L2}}) \\ \frac{1}{C}(i_{\mathrm{dc}} - i_{\mathrm{L1}} - i_{\mathrm{L2}}) \end{bmatrix}$$

The hitting condition can be satisfied by appropriate choice of switching function. The control law u that adopt switching function is described as:

$$u = \frac{1}{2}\big(1 + sign(S)\big) \tag{3.30}$$

The state variables i_{L1} and v_{C1} are chosen to control *PDV* of the *QZS* inverter. Therefore, sliding coefficient matrix is defined as:

$$\boldsymbol{J} = \begin{bmatrix} \gamma_1 & 0 & \gamma_2 & 0 \end{bmatrix} \tag{3.31}$$

Thus, the sliding surface S of the controller is obtained as the linear combination of state variables and adding an integral term to regulate *PDV* to reference [166] as:

$$S = \gamma_1 x_1 + \gamma_2 x_3 + \int_0^t (v_{\mathrm{C}}^{\mathrm{sum}} - V_{\mathrm{dc}}^{*})dt = \boldsymbol{J}\boldsymbol{x} + \int_0^t (v_{\mathrm{C}}^{\mathrm{sum}} - V_{\mathrm{dc}}^{*})dt \tag{3.32}$$

After hitting the sliding surface, the state trajectory should be confined to the sliding surface and approach towards its equilibrium point. To ensure this existence condition, the sliding function must satisfy:

$$\lim_{S \to 0} S \cdot \dot{S} < 0 \tag{3.33}$$

This can be expressed as:

$$\lim_{S\to 0^+}\frac{dS}{dt} = \lim_{S\to 0^+}\left[\frac{\gamma_1}{L}\{v_{C2} - (R_L + R_C)i_{L1} + v_{PV}\} - \frac{\gamma_2}{C}i_{L2} + (v_C^{sum} - V_{dc}^*)\right] < 0 \tag{3.34}$$

$$\lim_{S\to 0^-}\frac{dS}{dt} = \lim_{S\to 0^-}\left[\frac{\gamma_1}{L}\{-v_{C1} - (R_L + R_C)i_{L1} + R_C i_{dc} + v_{PV}\} + \frac{\gamma_2}{C}(i_{L1} - i_{dc}) + (v_C^{sum} - V_{dc}^*)\right] > 0 \tag{3.35}$$

The values of sliding coefficients γ_1 and γ_2 are obtained from (3.34) and (3.35). The analysis of the *SMC* system on the sliding surface is often carried out through the equivalent control input u_{eq}. When on the sliding surface, the sliding function satisfies:

$$S = \boldsymbol{J}\boldsymbol{x} + \int_0^t (v_C^{sum} - V_{dc}^*)dt = 0 \tag{3.36}$$

$$\dot{S} = \boldsymbol{J}\boldsymbol{x} + (v_C^{sum} - V_{dc}^*) = 0 \tag{3.37}$$

Thus, the u_{eq} is given from (3.37) as:

$$\begin{aligned} u_{eq} &= -[\boldsymbol{J}\boldsymbol{B_s}]^{-1}[\boldsymbol{J}\boldsymbol{A_s} + (v_C^{sum} - V_{dc}^*)] \\ &= \frac{\frac{\gamma_1}{L}\{v_{C1} + (R_L + R_C)i_{L1} - R_C i_{dc} - v_{PV}\} + \frac{\gamma_2}{C}(i_{dc} - i_{L1}) + (V_{dc}^* - v_C^{sum})}{\frac{\gamma_1}{L}(v_{C1} + v_{C2} - R_C i_{dc}) + \frac{\gamma_2}{C}(i_{dc} - i_{L1} - i_{L2})} \end{aligned} \tag{3.38}$$

The equivalent control input u_{eq} is used as output of the controller, i.e., *ST* duty ratio d_{st} and it is limited to 0.4 [108]. The closed loop system on the sliding surface is obtained by substituting u_{eq} in-place of u in (3.29). The stability condition is reached when closed loop system transfer function has all poles in the left-half-plane [166].

3.4 EIGENVALUE AND TIME-DELAY ANALYSIS

The negative unity feedback, i.e. $H(s) = 1$, linear system with time-delay t_d in control input $U(s)$ with $R(s)$ and $Y(s)$ as reference input and output, respectively, is shown in Fig. 3.8. Its dynamics equations can be given by:

$$\begin{aligned} \dot{\boldsymbol{x}} &= \boldsymbol{A}\boldsymbol{x} + \boldsymbol{B}u(t - t_d) \\ \boldsymbol{y} &= \boldsymbol{C}\boldsymbol{x} \end{aligned} \tag{3.39}$$

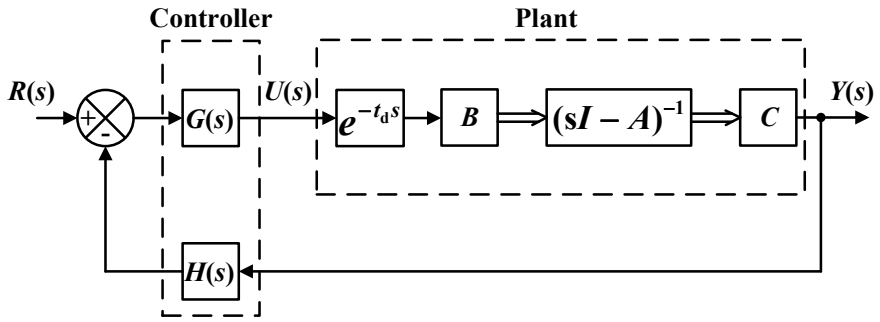


Fig. 3.8: General closed loop system with time-delay in control.

The plant transfer function $G_{\mathrm{P}}(s)$ is expressed as:

$$G_{\mathrm{P}}(s) = \boldsymbol{C}(s\boldsymbol{I} - \boldsymbol{A})^{-1}\boldsymbol{B}e^{-st_{\mathrm{d}}} \tag{3.40}$$

Let the loop gain $l(s)$ and closed loop transfer function $T(s)$ are expressed as:

$$\begin{aligned} l(s) &= G_{\mathrm{P}}(s)G(s) \\ &= G(s)\boldsymbol{C}(s\boldsymbol{I} - \boldsymbol{A})^{-1}\boldsymbol{B}e^{-st_{\mathrm{d}}} \end{aligned} \tag{3.41}$$

$$T(s) = \frac{l(s)}{1 + l(s)} \tag{3.42}$$

The roots of characteristic equation $\big(1 + l(s)\big)$ are the eigenvalues of the system. This characteristic equation has a infinite number of roots because $l(s)$ expressed by (3.41) is transcendental equation. Transcendental characteristic equation is transformed into algebraic equation using Padé rational function $e^{-st_{\mathrm{d}}} \approx \frac{1-\frac{st_{\mathrm{d}}}{2}}{1+\frac{st_{\mathrm{d}}}{2}}$ [164]. The (3.41) can be simplified as:

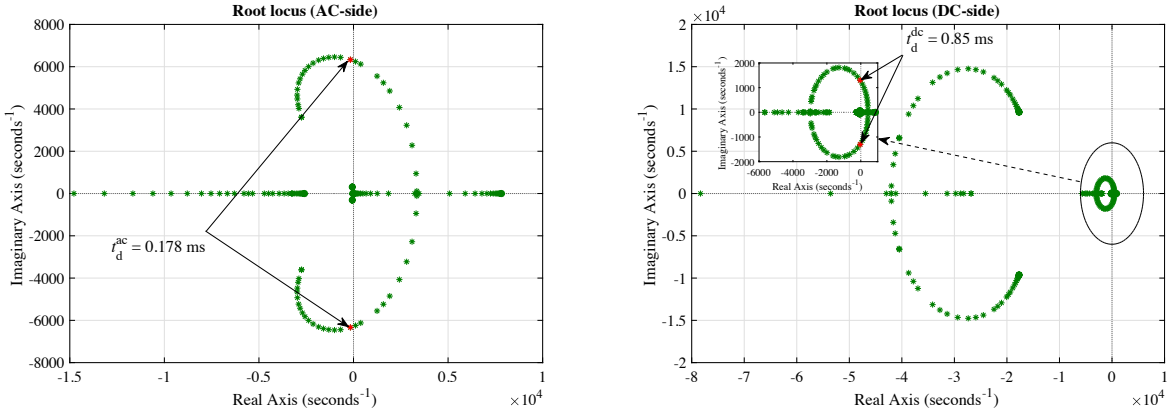
$$l(s) = G(s)\boldsymbol{C}(s\boldsymbol{I} - \boldsymbol{A})^{-1}\boldsymbol{B}\frac{1 - \frac{st_{\mathrm{d}}}{2}}{1 + \frac{st_{\mathrm{d}}}{2}} \tag{3.43}$$

For time-delay t_{d}, characteristic equation of the control system can be modified as:

$$1 + l(s) = 1 + t_{\mathrm{d}}\frac{P(s)}{Z(s)} \tag{3.44}$$

where $P(s)$ and $Z(s)$ are polynomial in s. This transformation is useful as it allows plotting the roots of the characteristic equation for the variation in time-delay $t_{\mathrm{d}} \in [0, \infty)$.

The eigenvalue spectrum for the AC- and DC-sides in presence of time-delay are shown in Figs. 3.9(a) and 3.9(b), respectively. It is noted that the system reaches at the verge of stability when AC- and DC-sides time-delay reaches 0.178 ms and 0.85 ms, respectively. The large time-delay in control implies a low decay of transients resulting from reduced *GM* and *PM*.



(a) **(b)**

Fig. 3.9: Eigenvalue spectrum with time-delay. **(a)** AC-side current control loop. **(b)** DC-side *PDV* control loop.

Theorem 2. *Loop gains for the AC- and DC-sides are obtained by using* (3.16) *and* (3.22)*, respectively, considering the time-delay in control as:*

$$l_{ac}(s) = K_{ac}(s)G_{ac}(s)\frac{1-\frac{st_d^{ac}}{2}}{1+\frac{st_d^{ac}}{2}} \tag{3.45}$$

$$l_{dc}^{pk}(s) = K_{dc}^{pk}(s)G_{dc}^{pk}(s)\frac{1-\frac{st_d^{dc}}{2}}{1+\frac{st_d^{dc}}{2}} \tag{3.46}$$

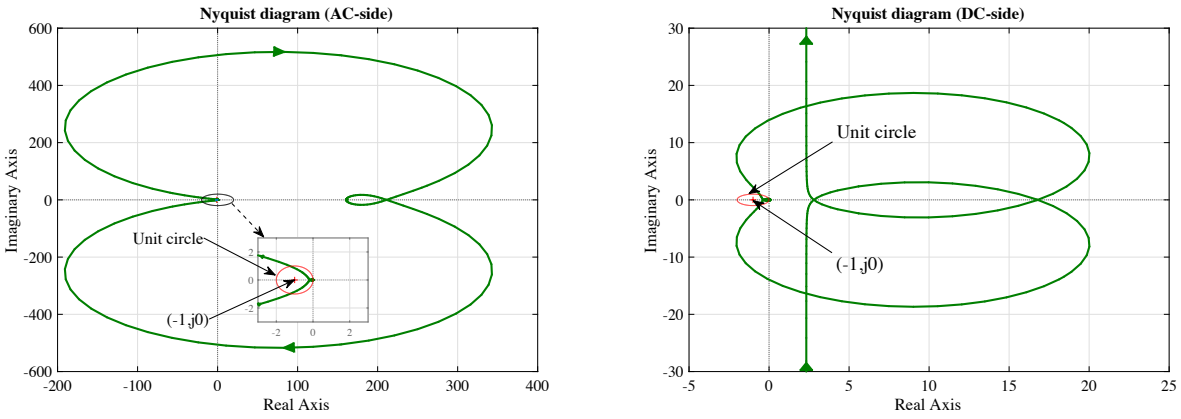
where t_d^{ac} and t_d^{dc} are delay in control for AC- and DC-side, respectively.

A system will be stable if the number of open-loop transfer function poles in the right-half-plane, is equal to the number of times that the Nyquist diagram for this function makes anti-clockwise encirclement at point $(-1, j0)$ [161].

Proof. The time-delays t_d^{ac} and t_d^{dc} are taken as 0.05 ms corresponding to $T_s/2$ [102]. The loop gains for the AC- and DC-sides expressed by (3.45) and (3.46) do not have right-half-plane pole. The corresponding Nyquist diagram, shown in Fig. 3.10, does not encircle the critical point $(-1, j0)$ for both the AC- and DC-side control. Therefore, according to **Theorem 2** both the subsystems will work stably for taken time-delays. □

3.5 SIMULATION RESULTS

In this section, 3-Φ grid connected *QZS* inverter system is simulated in MATLAB/Simulink and results of the proposed scheme with *TOIL* and damped-*SOGI* controller are validated



(a) **(b)**

Fig. 3.10: Nyquist plot with time-delay. **(a)** $t_{\mathrm{d}}^{\mathrm{ac}} = 0.05$ ms in AC-side current control. **(b)** $t_{\mathrm{d}}^{\mathrm{dc}} = 0.05$ ms in DC-side *PDV* control.

with the design parameters listed in Table 3.1. The performance of proposed scheme with *TOIL*-damped-*SOGI* controllers is also compared with different linear and robust *SMC* namely; *PID*-*PI* and *SMC*-damped-*SOGI*. The performance of the proposed controller is investigated for accounting time-delay in control loops and for change in *LC* values of the *QZS* network.

Six series and two parallel connected Havells *PV* modules are used as energy source. The technical specification of these modules is summarized in Table 3.2 [167]. Fig. 3.11 presents the typical $I - V$ and $P - V$ characteristics of *PV* array for two different *WCs*, *WC*1 and *WC*2. The *WCs*, the corresponding voltage at maximum power $V_{\mathrm{PV}}^{\mathrm{mx}}$, and maximum *PV* output power $P_{\mathrm{PV}}^{\mathrm{mx}}$, as obtained from Fig. 3.11, are described as follows:

*WC*1 : 1000 W/m^2 and 25 °C, $V_{\mathrm{PV}}^{\mathrm{mx}} = 186.12$ V, $P_{\mathrm{PV}}^{\mathrm{mx}} = 3000$ W.
*WC*2 : 250 W/m^2 and 50 °C, $V_{\mathrm{PV}}^{\mathrm{mx}} = 168.18$ V, $P_{\mathrm{PV}}^{\mathrm{mx}} = 662.034$ W.

For modulating the *QZS* inverter, *MCBC* with the 3$^{\mathrm{rd}}$ harmonic injection is used. The *PDV* is regulated at $V_{\mathrm{dc}}^{*} = 450$ V.

3.5.1 Change in weather condition

The *PV* voltage is changed from 186.12 V to 168.18 V at $t = 1$ s due to change in weather condition from *WC*1 to *WC*2. This demands a change in *ST* duty ratio with required boost, as shown in Fig. 3.12(a). This causes overshoot and undershoot in the DC-link voltage. There

Table 3.2. Technical specification of an adjusted model of Havells *PV* module

Parameter	**Values**
Electrical properties	
Maximum power	250 W
MPP voltage	31.02 V
MPP current	8.06 A
Open circuit voltage	36.99 V
Short circuit current	8.62 A
Module efficiency (%)	15.37
Number of cells	$6 * 10$
Series resistance	0.0405 Ω
Parallel resistance	701.289 Ω
Temperature coefficients	
Nominal power/temperature coefficient	−0.40 %/°C
Open circuit voltage/temperature coefficient	−0.30 %/°C
Short circuit current/temperature coefficient	0.05 %/°C

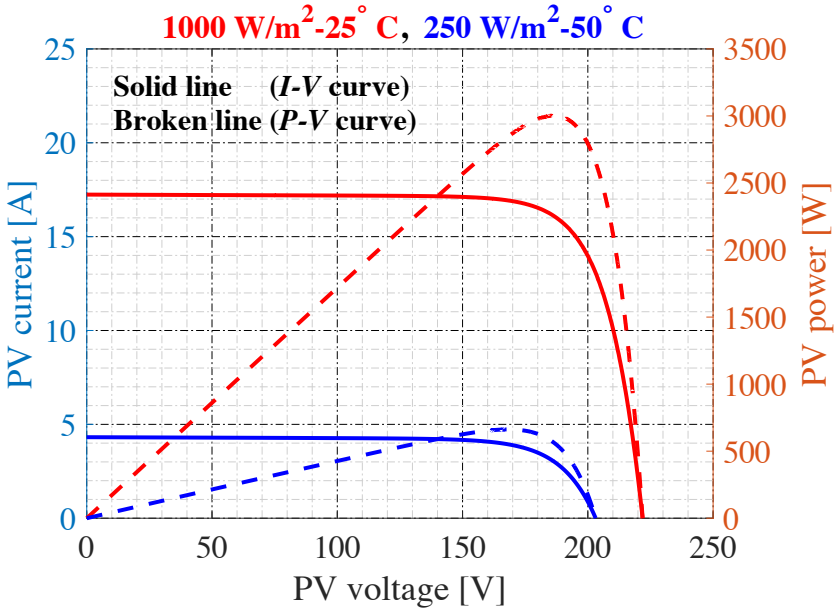


Fig. 3.11: *I–V* and *P–V* characteristics for different *WCs* (ENVIRO PVM6-250).

is momentary undershoot in modulating signal m_{abc} as shown Fig. 3.12(b), because of its dependency on *ST* duty ratio d_{st} in single stage *QZS* inverter. Due to a step change in input voltage, the voltages across *QZS* network capacitors v_{C1} and v_{C2} experience transients and

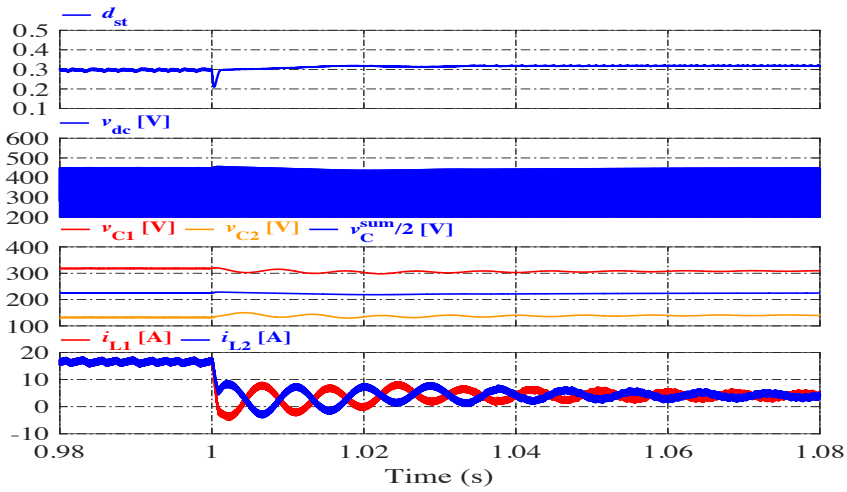
their steady-state values are changed from 318.06 V and 131.94 V to 309.11 V and 140.92 V, respectively. However, the sum $v_{\mathrm{C}}^{\mathrm{sum}} = v_{\mathrm{C1}} + v_{\mathrm{C2}}$ settles to a steady-state reference value V_{dc}^{*} after overshoot and undershoot. Fig. 3.12(a) shows transients in *QZS* network inductors current L_1 and L_2, i.e., i_{L1} and i_{L2}.

Fig. 3.12(b) depicts the transients in the *QZS* inverter phase voltage v_{tan} and line voltage v_{tab}. Fig. 3.12(b) shows that grid voltage and inverter current are in-phase, thereby suggesting *UPF* operation. The Fig. 3.12(c) show that real power P_{s} and reactive power Q_{s} change rapidly as input supply changes. Small ripples in P_{s} and Q_{s} are due to pulse-width modulation switching harmonics. A notch is observed in P_{s} and Q_{s} at $t = 1$ s because they are not perfectly decoupled. For perfect decoupling, i_α and i_β should closely follow i_α^* and i_β^* instantaneously as shown in Fig. 3.12(c). Inverter exhibits effective performance as a very small duration transients are resulted and new steady-state conditions are achieved quickly. This suggests the effective realization of closed-loop control strategy through DC- and AC-side controllers.

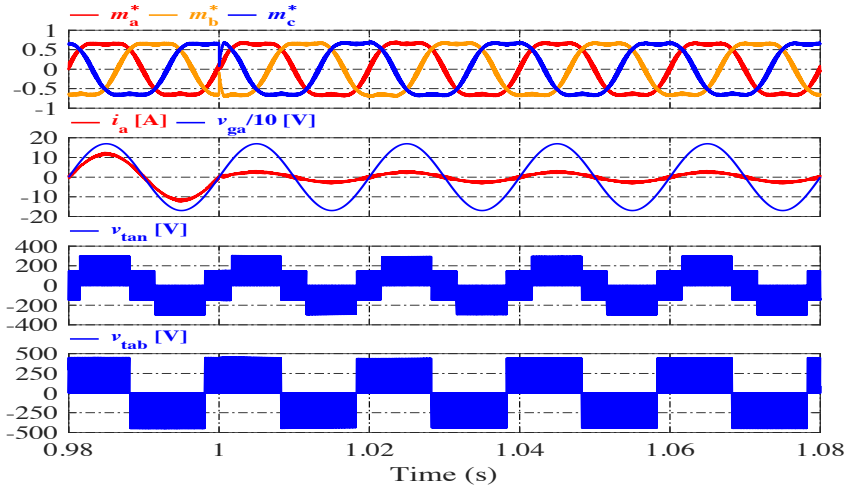
3.5.2 Step change in load

Fig. 3.13(a) shows the system performance at weather condition *WC*1, for applying linear load of real power (P_{L}) = 4 kW, and reactive power (Q_{L}) = 0.8 kVAr. Before the application of linear load, the i_{a} was in-phase with v_{ga}, and i_{ga} was 180° out-of-phase with v_{ga}. This 180° out-of-phase is due to the opposite reference direction of i_{a} and i_{ga}. When the linear load is switched at $t = 0.3$ s, the inverter current i_{a} remains in-phase with v_{ga}, thereby maintaining *UPF* operation. The demand of the linear load is met by the *PV* source and the grid. As the *PV* system is supplying 3 kW in *WC*1, the rest of real and reactive power demand of the load (1 kW, 0.8 kVAr) is supplied by the grid. Due the reactive power flow, i_{ga} leads v_{ga} and same is reflected in Fig. 3.13(a).

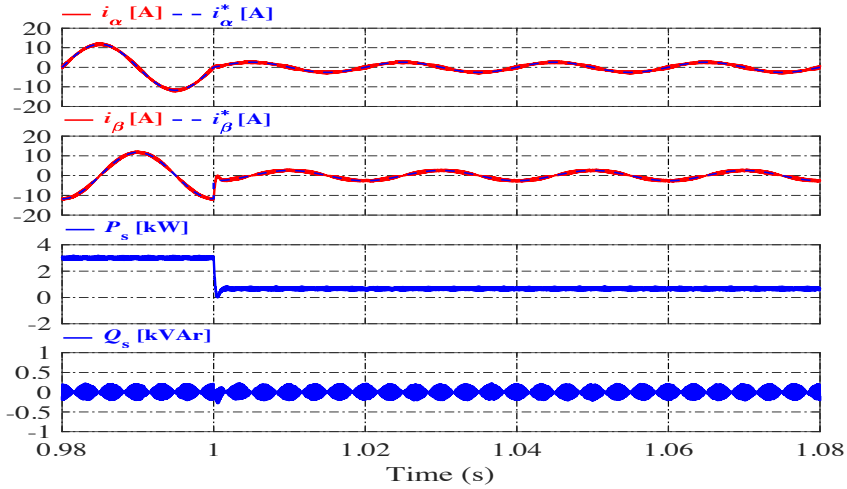
Fig. 3.13(b) shows performance for applying highly nonlinear load. At $t = 1$ s, a 3-Φ six-pulse bridge rectifier feeding a *RL*-load ($R = 20\ \Omega$ and $L = 1$ mH) is connected to the system, which is operating with above mentioned linear load. It can be observed that although the rectifier input currents are highly distorted with *THD* of 24.29%, as shown in Fig. 3.14(b), the proposed control strategy forces the inverter current to be sinusoidal at *UPF*. Fig. 3.14(a) shows that the *THD* of the inverter current is 3.65%, which is within the restriction imposed by IEEE standards [168].



(a)



(b)



(c)

Fig. 3.12: Simulation results for change in weather condition. **(a)** d_{st}; v_{dc}; v_{C1}, v_{C2}, and v_C^{sum}; and i_{L1} and i_{L2}. **(b)** m_{abc}^*; i_a and v_{ga}; v_{tan}; and v_{tab}. **(c)** i_α and i_α^*; i_β and i_β^*; P_s, and Q_s.

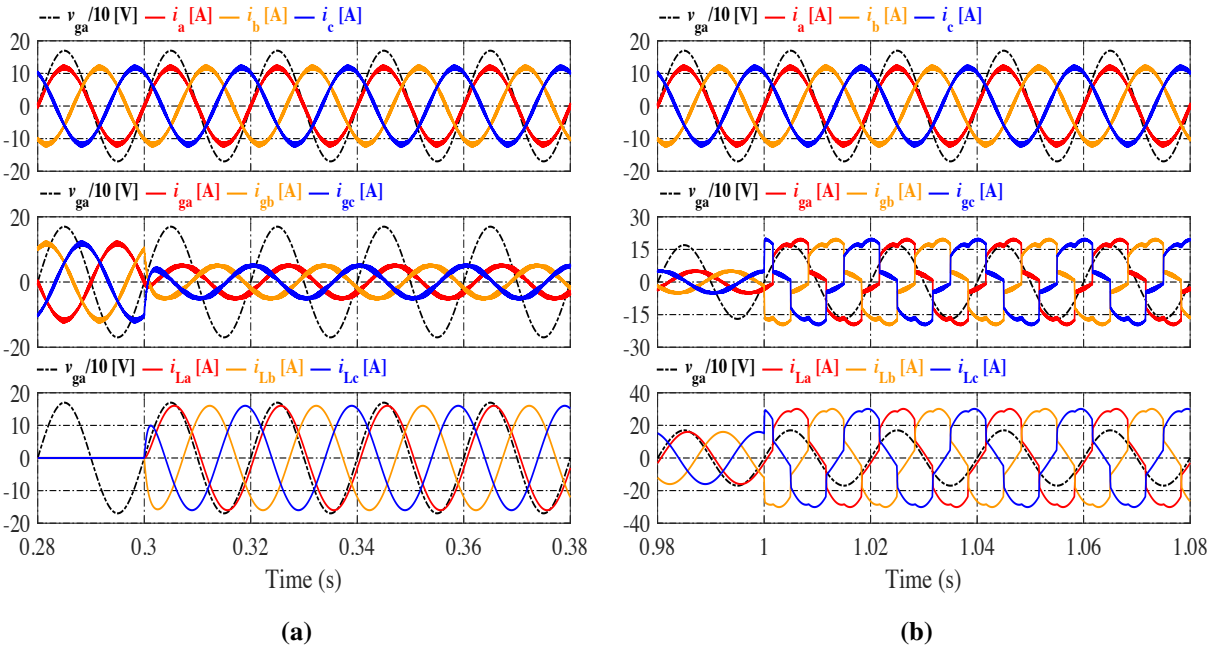


Fig. 3.13: Simulated grid voltage v_{ga}; inverter current i_{abc}; grid current i_{gabc}; and load current i_{Labc} under grid-side dynamics. **(a)** Linear load. **(b)** Non-linear load.

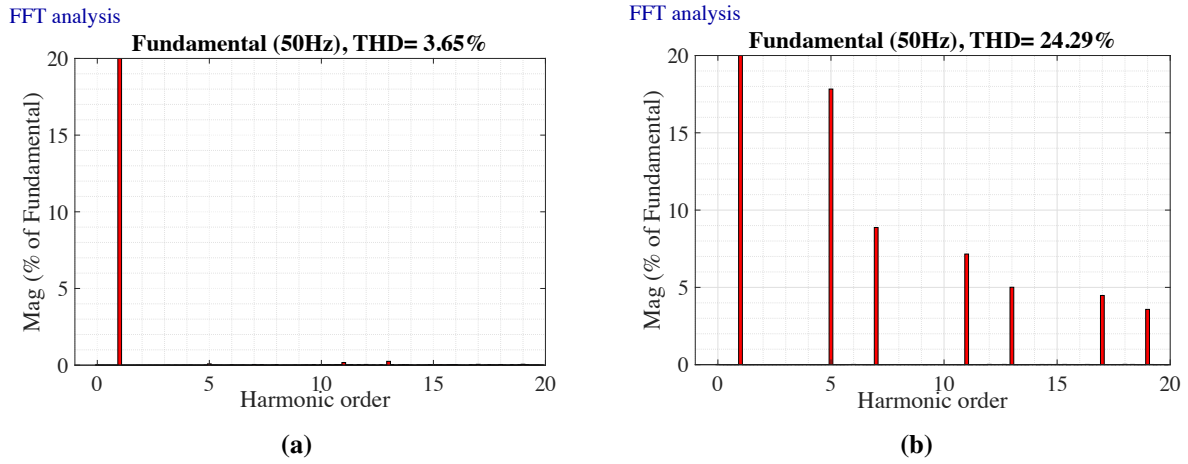


Fig. 3.14: *FFT* analysis. **(a)** Inverter current i_a. **(b)** Load current i_{La}.

3.5.3 Time-delay impact on the system

A time-delay of 0.05 ms is considered in the control loops of *TOIL* and damped-*SOGI* controllers and the system performance is analyzed. The comparison is made with a system having *TOIL* and damped-*SOGI* controllers without time-delay. The corresponding start-up transients are presented in Fig. 3.15. The response of the voltages v_{C1}, v_{C2}, and their sum v_C^{sum} results in

degraded transient response and longer settling time with time-delay in control loops. This is because time-delay is introducing additional phase delay which results in reduced *GM* and *PM*.

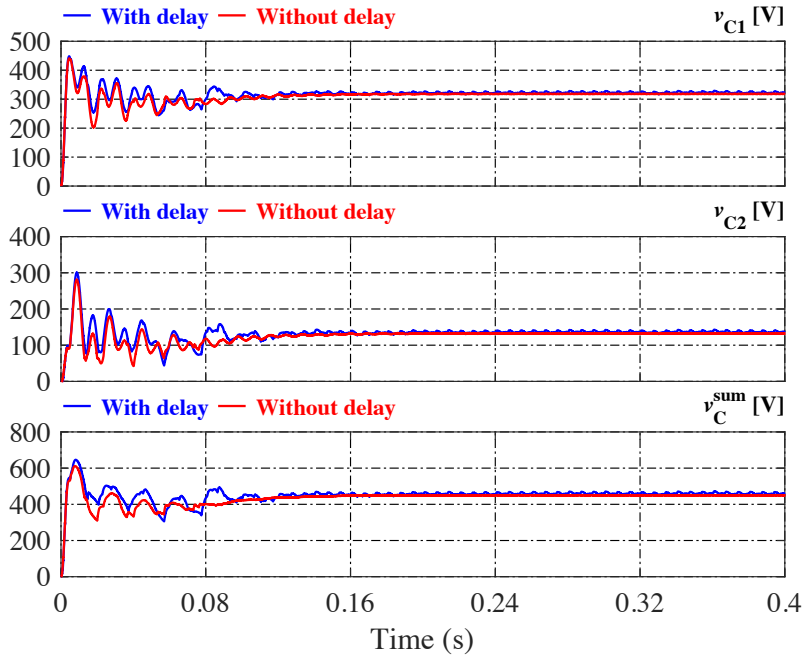


Fig. 3.15: Start up transients in v_{C1}, v_{C2}, and v_C^{sum} with and without time-delay.

3.5.4 Comparison with other controllers

The performance of the proposed scheme having *TOIL* on DC-side and damped-*SOGI* on AC-side, referred as *TOIL*-damped-*SOGI* combination, is compared with the following, considering that the disturbance is initiated from the input side due to change in weather condition from *WC*1 to *WC*2.

- *PID* on DC-side and *PI* on AC-side (*PID-PI* combination).
- *SMC* on DC-side and damped-*SOGI* on AC-side (*SMC*-damped-*SOGI* combination).

Performance with *PID-PI* controllers

The parameters of the *PID* controller are selected such that the crossover frequency is same as that of the *TOIL* controller. It results into *PID* compensator of the form:

$$K_{vd}^{PID}(s) = 0.075\frac{(s + 132.966)}{(s + 11876.241)}\left(1 + \frac{100}{s}\right) \tag{3.47}$$

The crossover frequency of the *PI* controller on AC-side is kept same as that of the damped-*SOGI*, which results into form:

$$K_{\text{ac}}^{\text{PI}}(s) = K_{\text{ac}}^{\alpha\beta(PI)}(s) = 18.85 + \frac{628.31}{s} \tag{3.48}$$

Fig. 3.16 shows a comparison of the *TOIL* and *PID* controllers for the DC-side. As shown in Fig. 3.16, *PID* controller achieves steady-state quickly as compared to the *TOIL* controller. In Fig. 3.16, large switching ripples can be observed in the waveform of *ST* duty ratio for the *PID* controller. These conditions occur due to the fact that, extra pole in *TOIL* yields a sluggish response while providing a filtering action in *ST* duty ratio. As d_{st} and m_{abc} are interdependent, these switching ripples cause distortions in the AC-side. By comparing Figs. 3.14(a) and 3.17(c), it is observed that the *THD* of the inverter current is increased to 3.86% while using *PID-PI* combination from 3.65% resulted while using *TOIL*-damped-*SOGI* combination.

The real power delivered from the *PV* source to grid, shown in Fig. 3.17(b), is reduced due to introduced phase lag between the grid voltage and inverter current as shown in Fig. 3.17(a). Due to this phase lag, a small amount of reactive power is required as shown in Fig. 3.17(b) and therefore *UPF* operation can not be achieved.

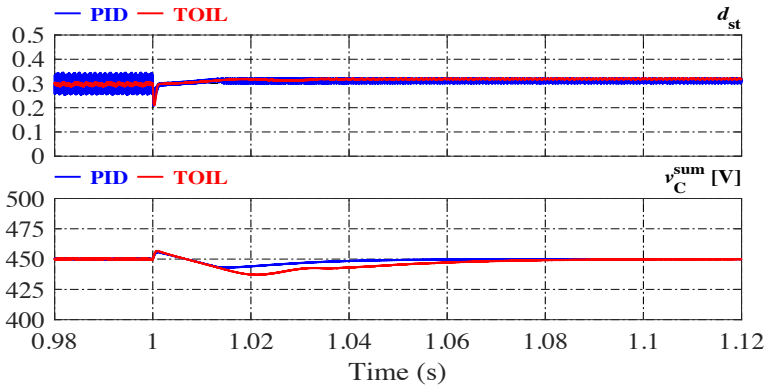
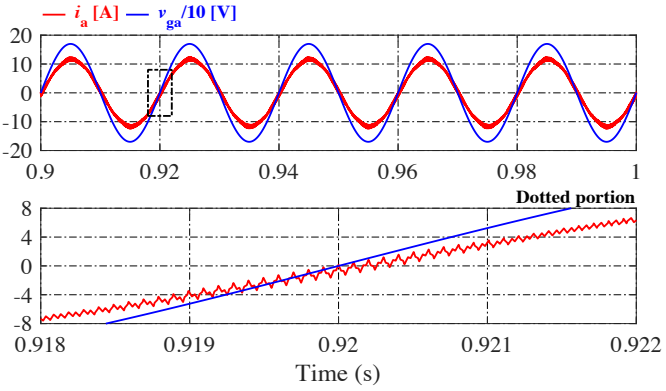


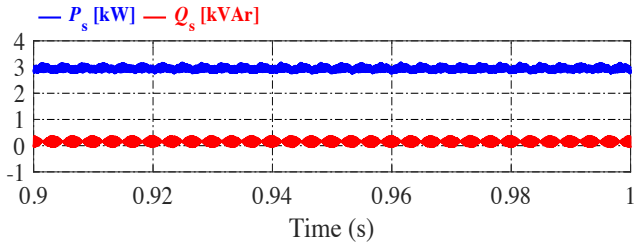
Fig. 3.16: Comparative performance of *PID* and *TOIL* controllers using d_{st} and $v_{\text{C}}^{\text{sum}}$.

Performance with *SMC*-damped-*SOGI* controllers

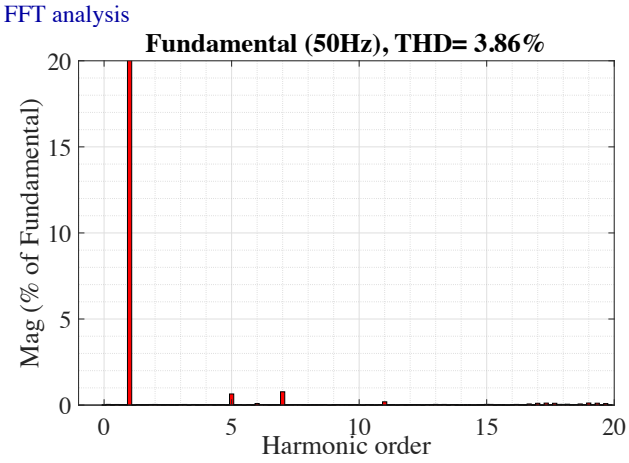
The *PV* voltage is changed from 186.12 V to 168.18 V at $t = 1$ s and performance characteristics are presented in Fig. 3.18. The Fig. 3.18(a) shows the voltages v_{C1} and v_{C2}. As evident from Fig. 3.18(b), the $v_{\text{C}}^{\text{sum}}$ with *SMC* experience sustained oscillations during steady-state and a large overshoot at the initiation of a transient. Whereas, the proposed *TOIL* controller is capable to track



(a)



(b)



(c)

Fig. 3.17: Performance of *PI* controller on AC-side. **(a)** v_{ga} and i_a with zoomed view. **(b)** P_s and Q_s. **(c)** *FFT* of i_a

V_{dc}^* without oscillations and with low overshoot. These oscillations with *SMC* at steady-state cause non-*ZSSE*. Therefore, it is justified to suggest that the response of *TOIL* is that of an underdamped system while *SMC* responds like that of a highly damped system. As *ST* duty ratio and modulating signal are interdependent, oscillations observed in d_{st} will be reflected on the AC-side. Thus, P_s and Q_s show sustained ripple in the steady-state illustrated in Fig. 3.18(c). Due to reflection of DC-side ripples into AC-side, the *THD* increased to 3.74% as presented in Fig. 3.18(d).

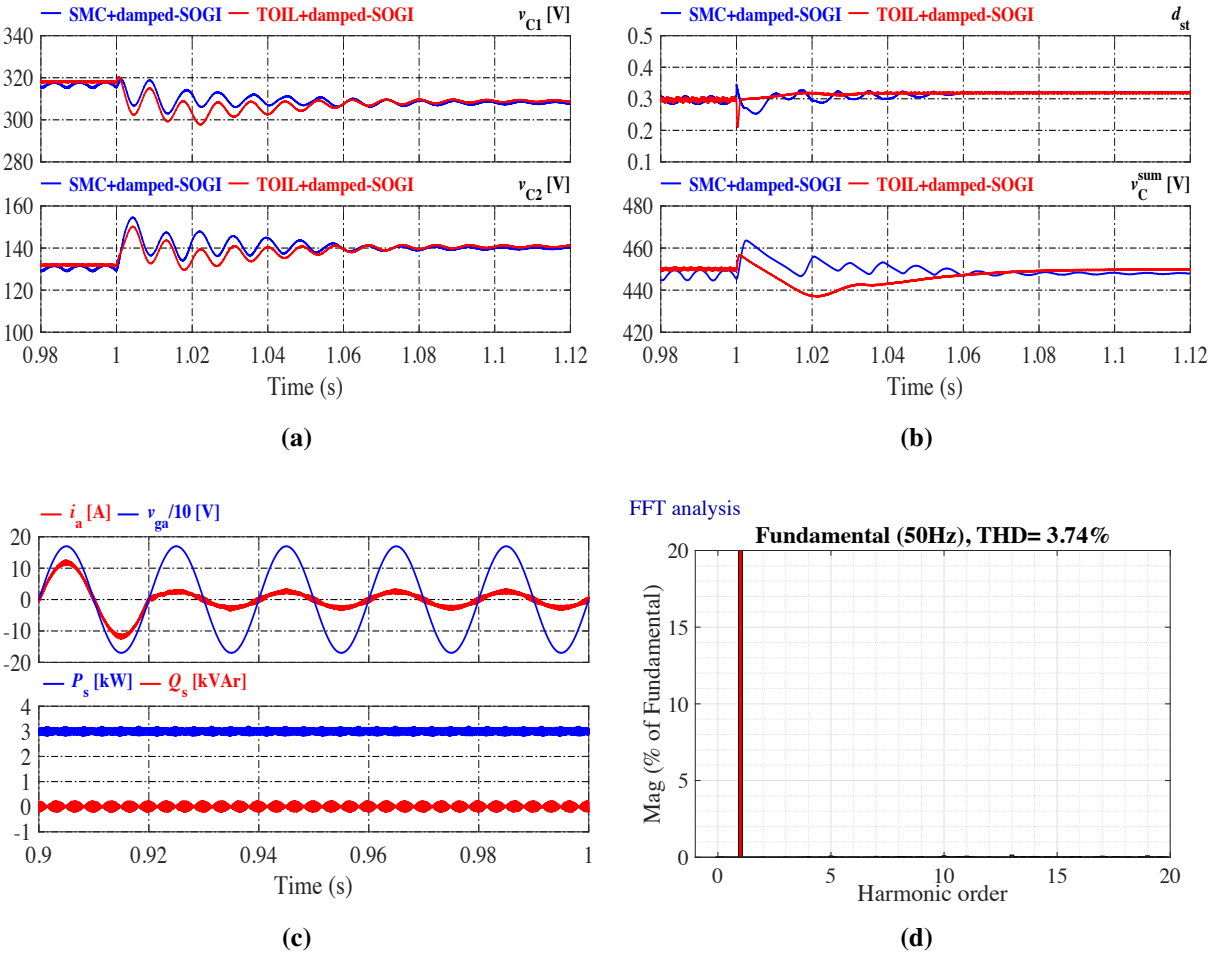


Fig. 3.18: Comparative performance of *TOIL* controller and *SMC*. **(a)** v_{C1} and v_{C2}. **(b)** d_{st} and v_C^{sum}. **(c)** i_a; v_{ga}; P_s; and Q_s. **(d)** *FFT* of i_a.

3.5.5 Change in *QZS* network parameters

Analysis is carried out for change in *LC* component values of the *QZS* network by ±25% from design values. The corresponding change in lossy inductor resistance and *ESR* of capacitor is not affecting system performance significantly and thus they have been kept unchanged. The simulations are performed and results are presented in Fig. 3.19 for cases described as:

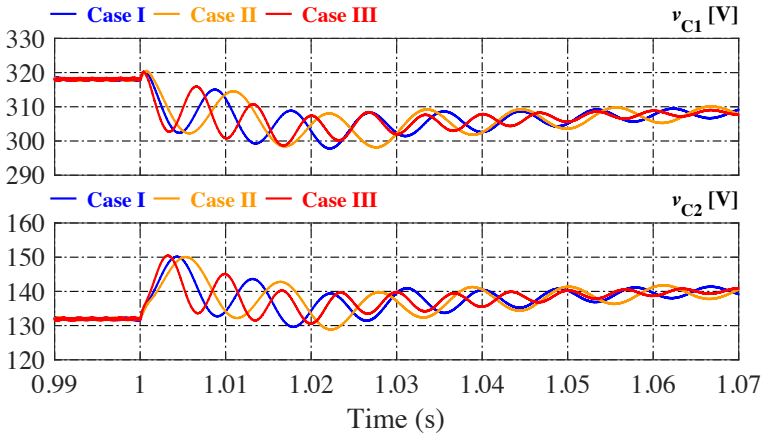
Case I: $L_1 = L_2 = 2$ mH, $C_1 = C_2 = 1000$ μF.

Case II: $L_1 = L_2 = 2.5$ mH, $C_1 = C_2 = 1250$ μF (+25% of selected *LC* values).

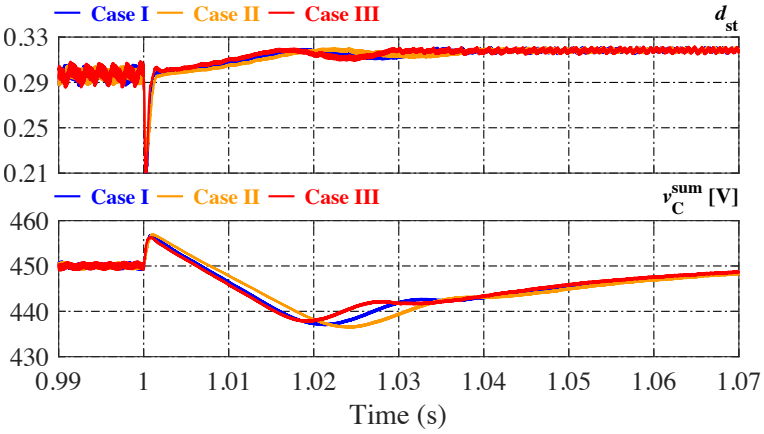
Case III: $L_1 = L_2 = 1.5$ mH, $C_1 = C_2 = 750$ μF (−25% of selected *LC* values).

Fig. 3.19 shows that the transient period is governed by the *LC* time constant. With lower *LC* values, resettling time decreases. The lower capacitance results in an underdamped response. Further, lower inductance causes high ripples in the inductor current as shown in Fig. 3.19(c).

These ripples make controlling difficult and also cause increased losses. Transients are observed in v_{C1} and v_{C2} as shown in Fig. 3.19(a), but the sum v_C^{sum}, shown in Fig. 3.19(b), is largely unaffected due to change in LC values.



(a)



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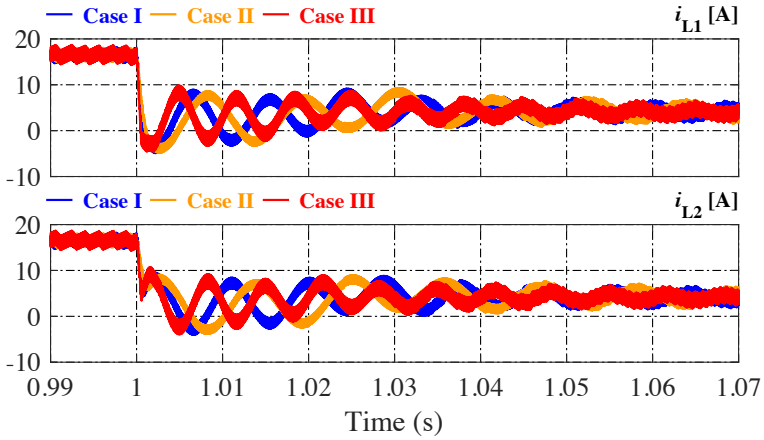


(c)

Fig. 3.19: Simulation results for different LC values of *QZS* network. **(a)** v_{C1} and v_{C2}. **(b)** d_{st} and v_C^{sum}. **(c)** i_{L1} and i_{L2}.

3.6 REAL-TIME VALIDATION USING OPAL-RT

The system under investigation, as shown in Fig. 3.3 is validated using *HIL RTS*, which is a crucial and reliable arrangement to validate complex real-time embedded systems before final hardware implementation [169].

The OPAL-RT, a *RTS* platform has been used for validation in the lab and the same is shown in Fig. 3.20. The controllers and plant are embedded in separate OPAL-RTs (OP4510) module. The *TOIL* controller for *PDV* regulation and damped-*SOGI* controller for inverter current control are embedded in Module-1, while the plant describing *PV* system, *QZS* inverter, and grid, is embedded in Module-2. The gating signals for the inverter bridge are fed from Module-1 to Module-2 and system measurements are fed back from Module-2 to Module-1 in real-time manner. These two modules are connected through the hardware inputs and outputs whereas the communicating signals are monitored through oscilloscopes. For real-time verification, the change in *WC* is initiated. It is evident from the Fig. 3.21 that the nature and values of capacitor voltages (v_{C1}, v_{C2}), their sum v_C^{sum}, grid voltage (v_{ga}), and inverter current (i_a) are same as obtained with the simulation performed in the MATLAB/Simulink environment (Fig. 3.12). This similarity between real-time results and MATLAB/Simulink results validates the hypothesis and controller design.

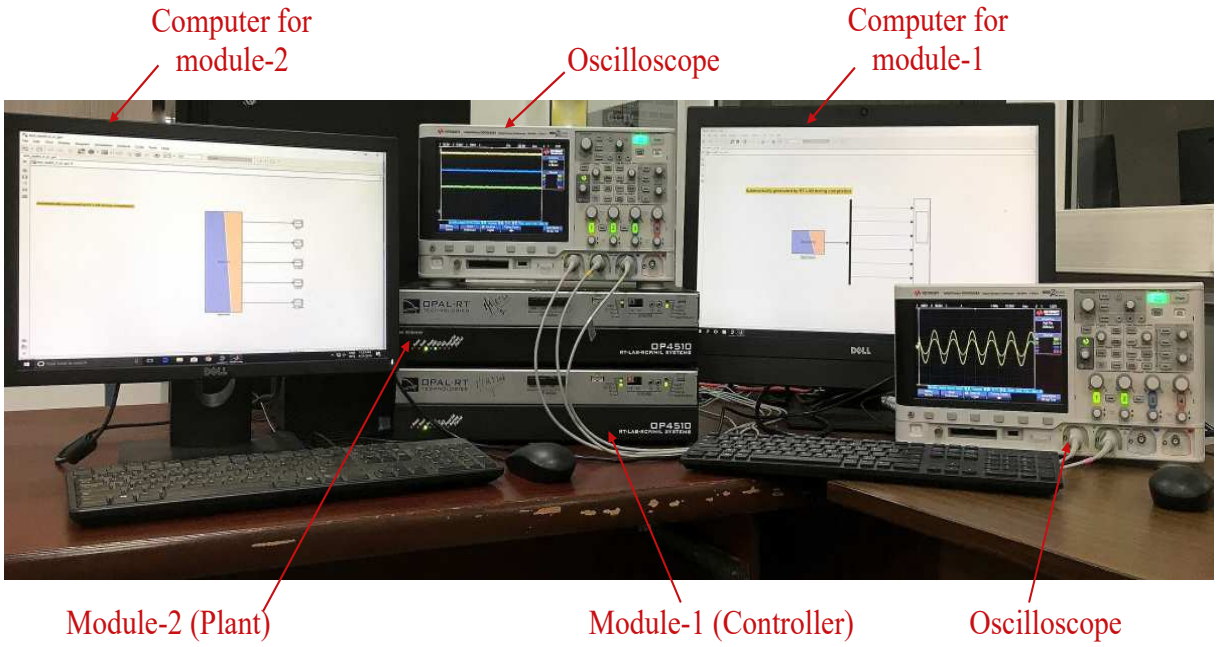
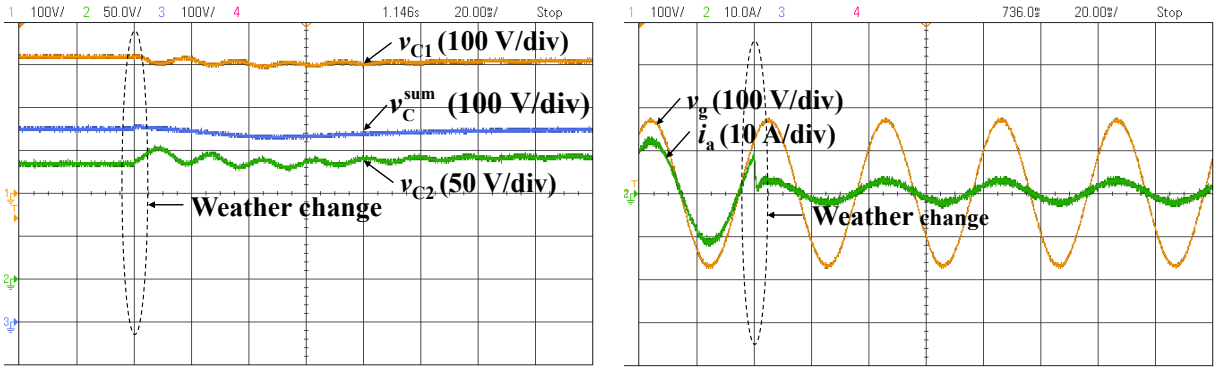


Fig. 3.20: The experimental setup for *HIL RTS* in the OPAL-RT platform.



(a) **(b)**

Fig. 3.21: *HIL RTS* results for transient initiated due to change in *WC*. **(a)** v_{C1}, v_{C2}, and v_C^{sum}. **(b)** v_g and i_a.

3.7 LABORATORY SETUP AND EXPERIMENTAL RESULTS

An experimental rig is implemented in the laboratory to evaluate the performance of the realized control scheme. It is integrated with the utility employing the 3-Φ autotransformer. A photograph of the experimental rig is depicted in Fig. 3.22. The layout comprises *QZS* network, H-bridge inverter, programmable DC-power supply (KEYSIGHT make, model: N8952A), and interfacing inductors. For the control purpose, the IC7840 based voltage sensing circuit, HE055T01 hall-effect current sensors, and control unit OP4510 are employed. The presented controllers are implemented on a host computer. It is transferred to OPAL-RT through RT-LAB software. The values of *QZS* network parameters, output filter inductor, grid voltage, and reference DC-link voltage are taken same in both MATLAB/Simulink and *HIL RTS* study. For recording transient conditions, two four-channel *Digital Storage Oscilloscopes (DSOs)* (KEYSIGHT make, model: DSOX2024A) are employed. Two experiments are conducted in the laboratory; first for transients due to input side dynamics and second for grid side transients arising due to application of linear/non-linear load.

3.7.1 With input-side dynamics

Fig. 3.23 presents the dynamic characteristics of the proposed system when exposed to input supply transient from (186.12 V, 3 kW) to (168.18 V, 662.034 W), resulted due to change in *WC* from *WC*1 to *WC*2. Fig. 3.23(a) represent v_{C1} and v_{C2} waveforms regulating v_{dc} at V_{dc}^*. As depicted in Fig. 3.23(b), the DC-link voltage is a high-frequency pulsed waveform with

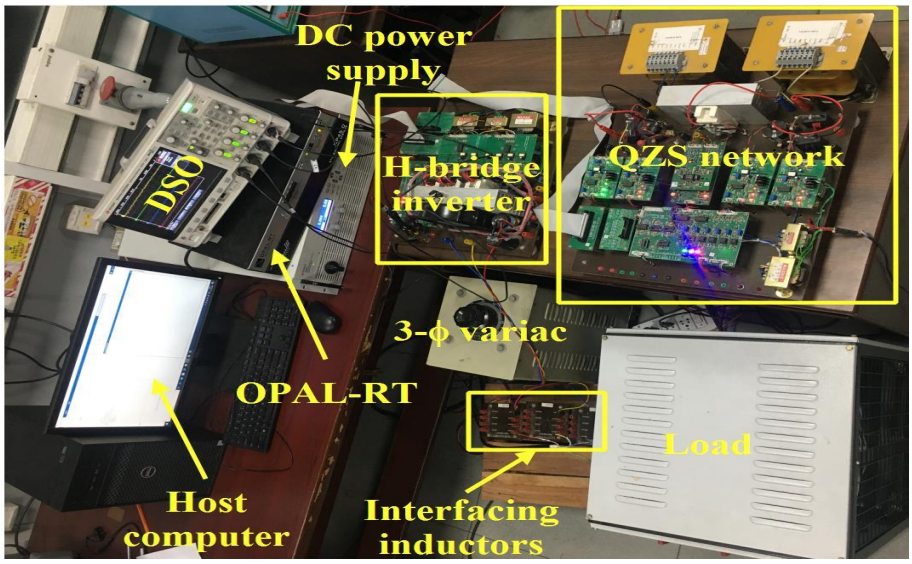


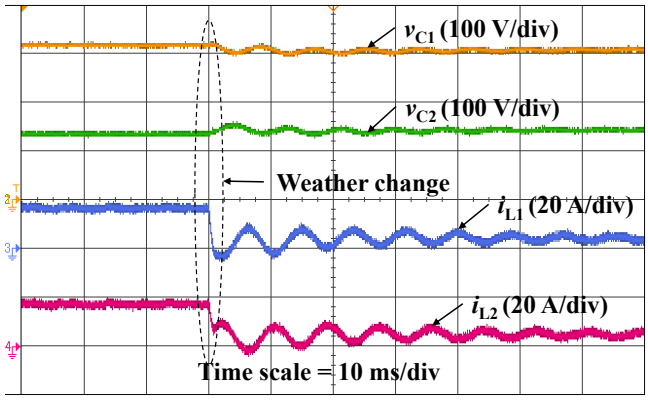
Fig. 3.22: Experimental rig of 3-Φ *QZS* inverter.

a peak value of 450 V and its estimated value $v_{\mathrm{C}}^{\mathrm{sum}}$ is well regulated at reference value. The phase voltage v_{tan} and line voltage v_{tab} of the *QZS* inverter comprises five and three levels, respectively, as illustrated in Fig. 3.23(b). The Fig. 3.23(c) indicates that the inverter current i_{a} is well synchronized with the grid voltage v_{ga}. The step change in weather conditions from *WC*1 to *WC*2, causes a decrease in *QZS* network inductor current i_{L1} and i_{L2}, followed by the fall in inverter current i_{abc}, as shown in Figs. 3.23(a) and 3.23(c), respectively.

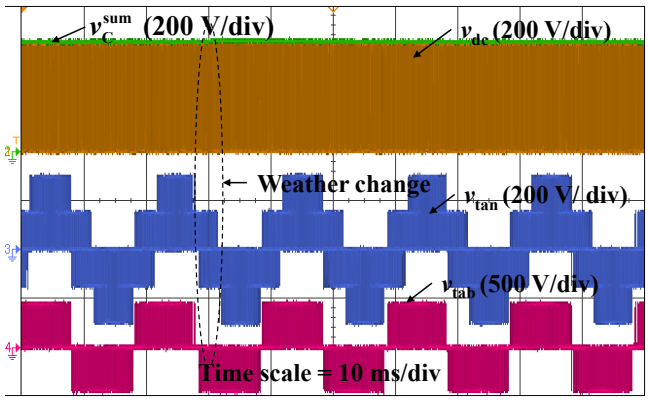
3.7.2 With grid-side dynamics

The experimental results of the proposed system for the sudden application of linear and non-linear loads are presented in Fig. 3.24 through grid phase voltage v_{ga}, inverter current i_{a}, grid current i_{ga}, and load current i_{La}. The DC-power supply is configured to provide 3 kW to the system at a specified input voltage of 186.12 V.

Before the integration of loads, the total power from the source is transferred to the grid. For the sudden addition of a 4 kW, 3 kVAr linear load, as shown in Fig. 3.24(a), the real power of 3 kW is supplied by the source, whereas the remainder real power and 3 kVAr of reactive power are provided by the grid. Fig. 3.24(b) presents the waveforms when the 3-Φ diode bridge rectifier feeding a resistive load of 1 kW is added to the system. Under this situation, i_{La} is highly distorted and i_{a} is purely sinusoidal. The *PV* source meets the load demand of 1 kW and the remaining 2 kW of generated power is delivered into the grid.



(a)



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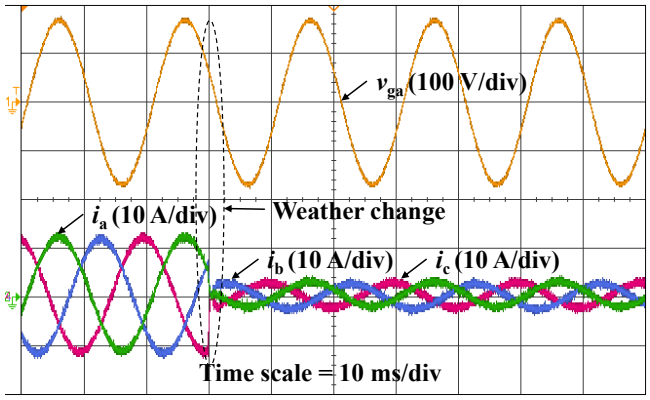
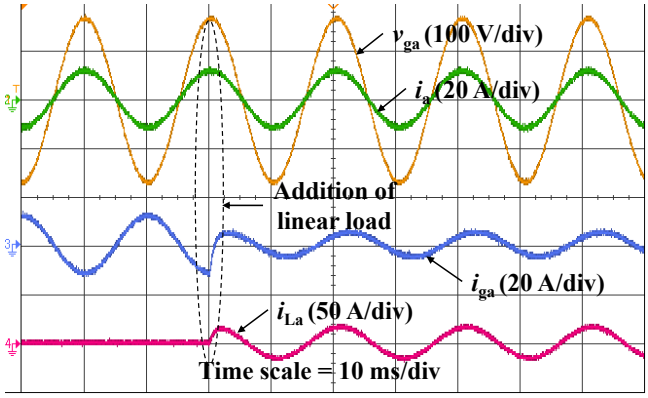


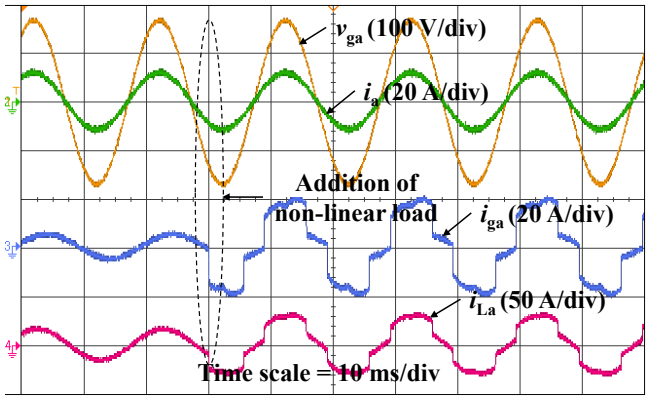
(c)

Fig. 3.23: Experimental results under input-side dynamics. **(a)** v_{C1}, v_{C2}, i_{L1}, and i_{L2}. **(b)** v_C^{sum}, v_{dc}, v_{tan}, and v_{tab}. **(c)** v_{ga} and i_{abc}.

The experimental findings are consistent with MATLAB and *RTS* results, as reported before. The experiment verifies that the proposed grid-connected *PV* system with *QZS* inverter would work for the input voltage varying in a wide range while maintaining a high-quality inverter current. The presented controllers also show excellent reference tracking and disturbance rejection ability.



(a)



(b)

Fig. 3.24: Experimental results under grid-side dynamics for v_{ga}, i_a, i_{ga}, and i_{La}. **(a)** Linear load. **(b)** Non-linear load.

3.8 CHAPTER SUMMARY

A single-stage control strategy to control the grid-tied *QZS* inverter has been investigated for *PV* system. Controllers are designed for AC- and DC-sides after developing a detailed dynamic model of the system. The DC-side controller is designed using *ST* duty ratio to *PDV* transfer function. The AC-side controller is realized to yield high gain at grid frequency and to track sinudoidal quantities with *ZSSE*. The performance was also evaluated considering the time-delay in AC- and DC-side control loops. The performance of the controllers is evaluated for the transients initiating from source due to change in *WCs* and load sides in MATLAB/Simulink environment and experimentally verified through *HIL RTS* in OPAL-RT and on practical test rig in the laboratory. The performance of the presented *TOIL*-damped-*SOGI* controller is also compared with other linear and robust controllers. The following conclusions are drawn from the study:

- The presented method indirectly estimates and controls *PDV* through the voltage across the *QZS* network capacitors. It is regulated to reference value using a *TOIL* controller.
- The damped-*SOGI* is realized to yield a high gain at grid frequency.
- The damped-*SOGI* and *TOIL* controllers for AC- and DC-sides, respectively, result in *ZSSE*. The design is effective to avoid interference between AC- and DC-side dynamics.
- A deteriorated transient response and prolonged settling time were observed with time-delay in control loops.
- The response with *TOIL* and *PID* controllers is underdamped while that with *SMC* is highly damped. At steady-state, *TOIL* and *PID* controllers yield *ZSSE* whereas *SMC* leads to non-*ZSSE* response.
- The transient response of *TOIL* and *PID* is approximately same but switching ripples in *ST* duty ratio are more with *PID* control.
- For the AC-side, damped-*SOGI* tracks the sinusoidal command effectively while *PI* controller results in magnitude attenuation/phase delay.
- It is also observed that the controller is robust enough to accommodate ±25% of the change in *LC* component values.

Chapter–4

Three-level NPC-QZS Inverter Based Three-phase Grid-tied PV System

4.1 GENERAL

The efficiency of grid-tied *PV* systems inevitably depends on the performance of the power conditioner and the ability of the implemented control strategies in achieving high performance. The power converter topologies for such system are classified into single-stage or two-stage and two-level or *Multi-Level Inverters* (*MLIs*). Having analyzed the performance of two-level *QZS* inverter based 3-Φ grid-tied *PV* system in Chapter-3, the investigation is extended to inverter operation as *MLI*, which are characterized with high power quality at the AC-side, reduced filter size, operation at high voltage levels, and reduced switching losses.

The *NPC-QZS* inverter is poised to be a potential candidate for renewable energy applications because it yields continuous input current and voltage boost. This hybrid topology possesses high quality staircase output voltage with low harmonic distortion, independent DC-link voltage control with special voltage step-up/down function in single-stage power conversion, and independent control of power distribution with high reliability.

The motivation of this chapter is to analyze the performance of the 3-Φ grid-tied *PV* system based on single-stage *NPC-QZS* inverter, as shown in Fig. 4.1. This chapter presents the design of controllers for DC-link voltage and AC-side current. The DC-link voltage controller is responsible for regulating the inverter's DC-link voltage to a reference value. The AC-side current controller works in coordination with DC-link voltage controller and injects a sinusoidal

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current, corresponds to the *Maximum Power Point* (*MPP*) at particular insolation level, into the grid and in-phase with the grid voltage. The control of inverter current is achieved through a damped-*SOGI* controller. The *PDV* is estimated indirectly from the voltages of *QZS* network capacitors and is regulated by an *IDL* controller. Two modified modulation techniques based on *POD* and *IPD* are proposed to yield *ST* by injecting third harmonics for *MCBC*. The performance of the proposed controller is compared with the designed sliding-mode controller. The controller design and system performance are validated through real-time simulation and experimentation on practical setup in laboratory.

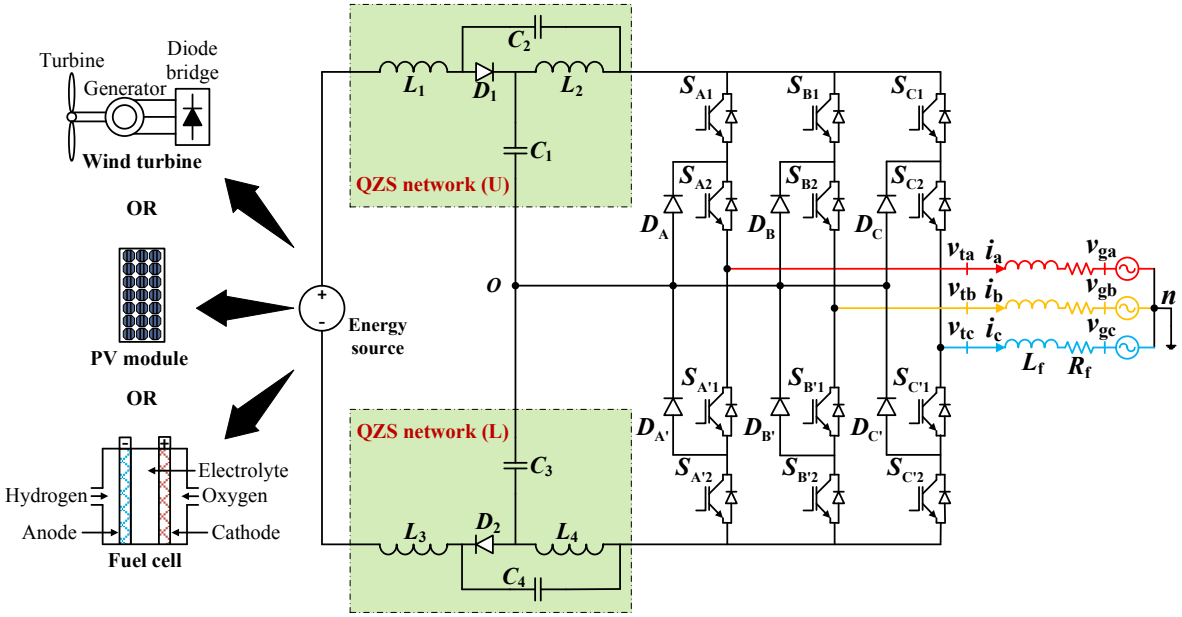


Fig. 4.1: Schematic of grid-tied 3-Φ *3L NPC-QZS* inverter for *RES*.

4.2 MODELING OF 3-Φ *3L NPC-QZS* NETWORK

The AC- and DC-side of *3L NPC-QZS* inverter are decoupled for developing a single-stage control strategy. The equivalent circuits distinctly representing the *ST* and *NST* states are shown in Fig. 4.2. These states are full DC-link *ST*, *Upper DC-Link Shoot-Through (UDST)*, *Lower DC-Link Shoot-Through (LDST)*, and *NST*. The inverter and external load are represented by switches S_U, S_L in parallel with the current sources $i_{dc(U)}$, $i_{dc(L)}$, respectively [170]. The small-signal modeling and analysis are carried out through the following assumptions:

- The inductances and capacitances of *QZS* inverter are equal to *L* and *C*, respectively.
- *CCM* operation of the inverter.

- Lossy capacitors and inductors encompass *ESR* and winding resistance R_C and R_L, respectively.
- The diodes D_1, D_2, and switches S_U, S_L are assumed to be ideal.

In full DC-link *ST* state, shown as Fig. 4.2(a), the load and source sides are decoupled by non-conducting diodes D_1, D_2 and conducting switches S_U and S_L. The energy stored in $C_1 \ldots C_4$ is transferred to $L_1 \ldots L_4$. In *UDST*, shown as Fig. 4.2(b), switch S_L and diode D_2 are non-conducting, while during *LDST*, shown as Fig. 4.2(c), switch S_U and diode D_1 are non-conducting [59].

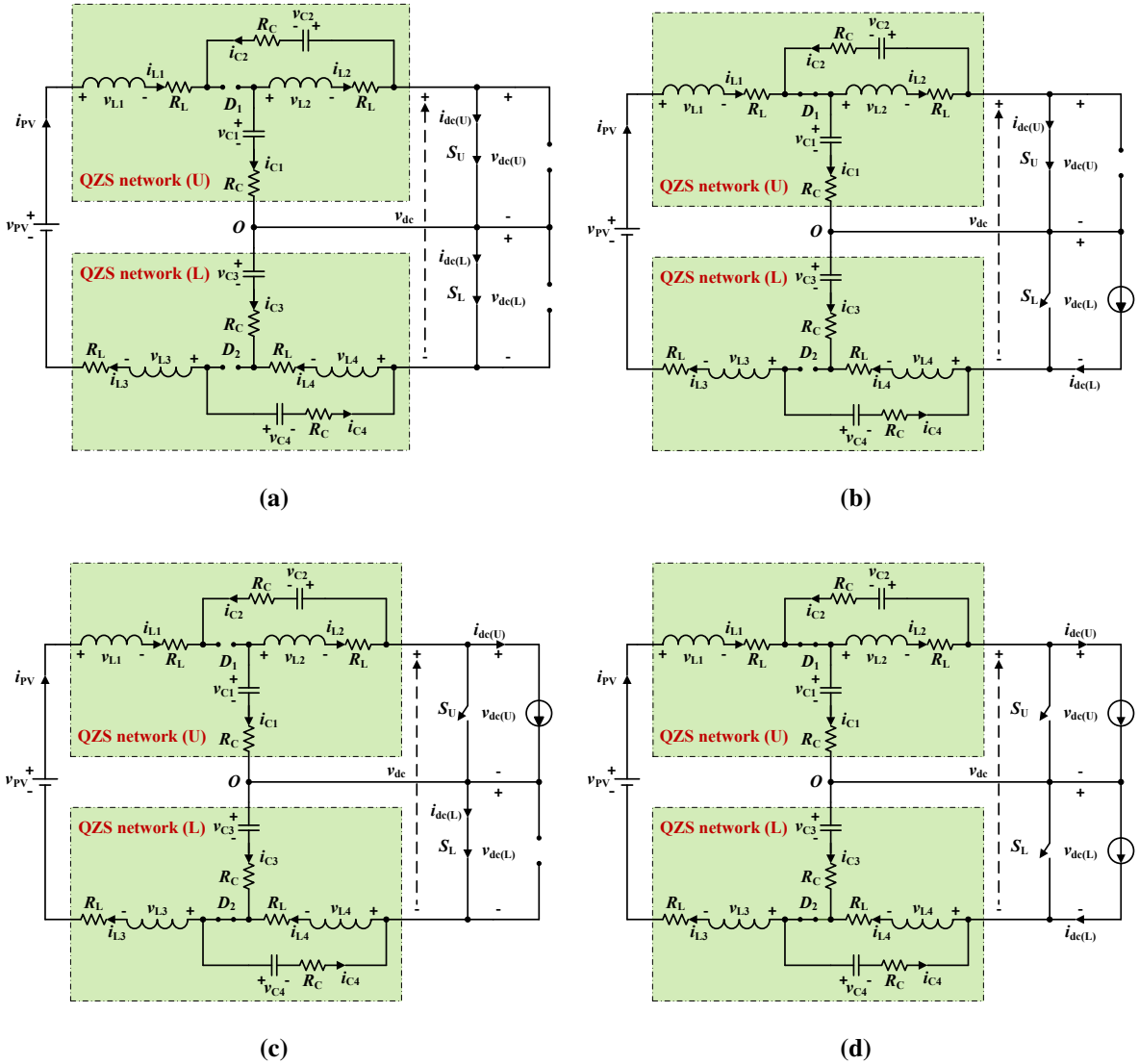


Fig. 4.2: Equivalent circuit of 3-Φ *3L NPC-QZS* inverter when in **(a)** Full DC-link *ST* state. **(b)** Upper DC-link *ST* state. **(c)** Lower DC-link *ST* state. **(d)** *NST* state.

In *NST* state, shown as Fig. 4.2(d), the source charges the capacitors and supplies the load as input diodes D_1, D_2 conduct and switches S_U, S_L do not conduct. Inductors additionally discharge through the load and therefore boosting the DC-link voltage v_{dc}. The duration of *ST* and *NST* intervals are specified as T_{st} and T_{nst}, respectively, which defines the switching period $T_s = T_{st} + T_{nst}$.

Due to symmetry:

$$\begin{aligned} i_{L1} &= i_{L3} \qquad i_{L2} = i_{L4} \\ v_{C1} &= v_{C3} \qquad v_{C2} = v_{C4} \\ i_{dc(U)} = i_{dc(L)} &= i_{dc} \qquad v_{dc(U)} = v_{dc(L)} \end{aligned} \tag{4.1}$$

With capacitor voltages v_{C1}, v_{C2}; inductor currents i_{L1}, i_{L2}; input voltage v_{PV}; and DC-link current i_{dc}; the state vector $\boldsymbol{x}$ and input vector $\boldsymbol{u}$ are formed as $\boldsymbol{x} = [\, i_{L1}\ i_{L2}\ v_{C1}\ v_{C2} \,]^\intercal$ and $\boldsymbol{u} = [\, v_{PV}\ i_{dc} \,]^\intercal$, respectively. The state-space equations in *ST* and *NST* mode are obtained as (4.2) and (4.3), respectively:

$$\boldsymbol{x} = \boldsymbol{A_0 x} + \boldsymbol{B_0 u} \tag{4.2}$$

$$\boldsymbol{x} = \boldsymbol{A_1 x} + \boldsymbol{B_1 u} \tag{4.3}$$

where

$$\boldsymbol{A_0} = \begin{bmatrix} -\frac{(R_L+R_C)}{L} & 0 & 0 & \frac{1}{L} \\ 0 & -\frac{(R_L+R_C)}{L} & \frac{1}{L} & 0 \\ 0 & -\frac{1}{C} & 0 & 0 \\ -\frac{1}{C} & 0 & 0 & 0 \end{bmatrix} \qquad \boldsymbol{B_0} = \begin{bmatrix} \frac{1}{2L} & 0 \\ 0 & 0 \\ 0 & 0 \\ 0 & 0 \end{bmatrix}$$

$$\boldsymbol{A_1} = \begin{bmatrix} -\frac{(R_L+R_C)}{L} & 0 & -\frac{1}{L} & 0 \\ 0 & -\frac{(R_L+R_C)}{L} & 0 & -\frac{1}{L} \\ \frac{1}{C} & 0 & 0 & 0 \\ 0 & \frac{1}{C} & 0 & 0 \end{bmatrix} \qquad \boldsymbol{B_1} = \begin{bmatrix} \frac{1}{2L} & \frac{R_C}{L} \\ 0 & \frac{R_C}{L} \\ 0 & -\frac{1}{C} \\ 0 & -\frac{1}{C} \end{bmatrix}$$

Above equations are combined using state-space averaging over T_s to yield (4.4) as:

$$\boldsymbol{x} = \boldsymbol{Ax} + \boldsymbol{Bu} \qquad \text{and} \qquad \boldsymbol{y} = \boldsymbol{Cx} + \boldsymbol{Eu} \tag{4.4}$$

where $\boldsymbol{A} = d_{st}\boldsymbol{A_0} + d_{nst}\boldsymbol{A_1}$, $\boldsymbol{B} = d_{st}\boldsymbol{B_0} + d_{nst}\boldsymbol{B_1}$. When the output vector $\boldsymbol{y}$ coincides with state vector $\boldsymbol{x}$, it yields $\boldsymbol{C} = \boldsymbol{I}$ and $\boldsymbol{E} = \boldsymbol{0}$.

The *ST* duty ratio, defined as $d_{\rm st} = T_{\rm st}/T_{\rm s}$, is the duty ratio of switches $S_{\rm U}$ and $S_{\rm L}$, while duty ratio of D_1, D_2, $d_{\rm nst} = T_{\rm nst}/T_{\rm s}$, is described as the *NST* duty ratio. The perturbation and linearization are applied to (4.4) to yield small-signal relations among the state variables. The input voltage $v_{\rm PV}$, disturbance input $i_{\rm dc}$, and *ST* duty ratio $d_{\rm st}$, are perturbed as $v_{\rm PV} = V_{\rm PV} + \tilde{v}_{\rm PV}$, $i_{\rm dc} = I_{\rm dc} + \tilde{i}_{\rm dc}$, and $d_{\rm st} = D_{\rm st} + \tilde{d}_{\rm st}$, where "~" denotes perturb quantities. After ignoring higher-order terms, the resulting equations are:

$$\frac{d\tilde{\boldsymbol{x}}}{dt} = (D_{\rm st}\boldsymbol{A_0} + D_{\rm nst}\boldsymbol{A_1})\tilde{\boldsymbol{x}} + (D_{\rm st}\boldsymbol{B_0} + D_{\rm nst}\boldsymbol{B_1})\tilde{\boldsymbol{u}} + \{(\boldsymbol{A_0} - \boldsymbol{A_1})\boldsymbol{X} + (\boldsymbol{B_0} - \boldsymbol{B_1})\boldsymbol{U}\}\tilde{d}_{\rm st} \quad (4.5)$$

With the consideration of lossy capacitors and inductors, the steady-state values of state-variables ($\boldsymbol{X}$) are obtained from (4.4) as:

$$\boldsymbol{X} = \begin{bmatrix} 0 & B_{\rm z}D_{\rm nst} \\ 0 & B_{\rm z}D_{\rm nst} \\ \frac{B_{\rm z}D_{\rm nst}}{2} & -B_{\rm z}^2 D_{\rm nst}(R_{\rm L} + 2R_{\rm C}D_{\rm st}) \\ \frac{B_{\rm z}D_{\rm st}}{2} & -B_{\rm z}^2 D_{\rm nst}(R_{\rm L} + 2R_{\rm C}D_{\rm st}) \end{bmatrix} \begin{bmatrix} V_{\rm PV} \\ I_{\rm dc} \end{bmatrix} \quad (4.6)$$

At steady-state, *NST* duty ratio $D_{\rm nst}$ and boost-factor $B_{\rm z}$ are defined as:

$$\begin{cases} D_{\rm nst} = 1 - D_{\rm st} \\ B_{\rm z} = \dfrac{1}{(1 - 2D_{\rm st})} \end{cases} \quad (4.7)$$

From Figs. 4.2(a) and 4.2(d) and using (4.1), the DC-link voltage $v_{\rm dc}$ in the *ST* is obtained as zero ($v_{\rm dc} = 0$), while in *NST*, it is expressed as:

$$v_{\rm dc} = 2[v_{\rm C1} + v_{\rm C2} + R_{\rm C}(i_{\rm L1} + i_{\rm L2} - 2i_{\rm dc})] \quad (4.8)$$

The average and peak DC-link voltages $V_{\rm dc}^{\rm av}$ and $V_{\rm dc}^{\rm pk}$ at steady-state are determined from (4.6) and (4.8) as:

$$\begin{bmatrix} V_{\rm dc}^{\rm av} \\ V_{\rm dc}^{\rm pk} \end{bmatrix} = \begin{bmatrix} B_{\rm z}D_{\rm nst} & -4B_{\rm z}^2 D_{\rm nst}(R_{\rm L}D_{\rm nst} + R_{\rm C}D_{\rm st}) \\ B_{\rm z} & -4B_{\rm z}^2(R_{\rm L}D_{\rm nst} + R_{\rm C}D_{\rm st}) \end{bmatrix} \begin{bmatrix} V_{\rm PV} \\ I_{\rm dc} \end{bmatrix} \quad (4.9)$$

The $V_{\rm dc}^{\rm pk}$ is the equivalent DC-link voltage. The peak AC-voltage $V_{\rm M}$ of the inverter is obtained using modulation index M, as [12]:

$$V_{\rm M} = \frac{1}{2}MV_{\rm dc}^{\rm pk} \quad (4.10)$$

4.3 CONTROLLER DESIGN

The control scheme for the system is shown in Fig. 4.3. Correspondingly, the design values of parameters are summarized in Table 4.1. The procedure to design the *QZS* network parameters is described in Appendix B. The overall control structure is implemented through a separate controller for AC-current and for *PDV*. The AC-side dynamics are faster compared to the DC-side dynamics [99], and thus higher *BW* is selected for AC-side control loop. The damped-*SOGI* controller at the AC-side is proposed to track the sinusoidal reference with *ZSSE*, while the *IDL* controller at DC-side is proposed for *PDV* regulation. The design of these controllers are described as follows:

Table 4.1. 3-Φ *3L NPC-QZS* inverter parameters

Parameter	**Value**
Reference *PDV* (V_{dc}^{*})	400 V
QZS network inductances ($L_1 \ldots L_4$)	1 mH
Winding resistance of $L_1 \ldots L_4$ ($R_{\mathrm{L1}} \ldots R_{\mathrm{L4}}$)	0.1 Ω
QZS network capacitances ($C_1 \ldots C_4$)	3000 μF
ESR of $C_1 \ldots C_4$ ($R_{\mathrm{C1}} \ldots R_{\mathrm{C4}}$)	0.01 Ω
AC-side filter inductance (L_{f})	3 mH
Winding resistance of L_{f} (R_{f})	0.1 Ω
Grid *RMS* voltage (phase-neutral)	100 V
Angular grid frequency (ω_{g})	2π(50 Hz)
Switching frequency (f_{s})	10 kHz

4.3.1 Design of damped-*SOGI* controller for AC-side

The AC-side voltage balance equations from Fig. 4.1, suggests:

$$L_{\mathrm{f}} \frac{\mathrm{d}i_{\mathrm{abc}}}{\mathrm{d}t} = v_{\mathrm{tabc}} - v_{\mathrm{gabc}} - R_{\mathrm{f}} i_{\mathrm{abc}} \tag{4.11}$$

where v_{tabc} is inverter AC-side voltage, v_{gabc} is grid voltage, and i_{abc} is AC-side current, R_{f} is filter resistance and L_{f} is filter inductance.

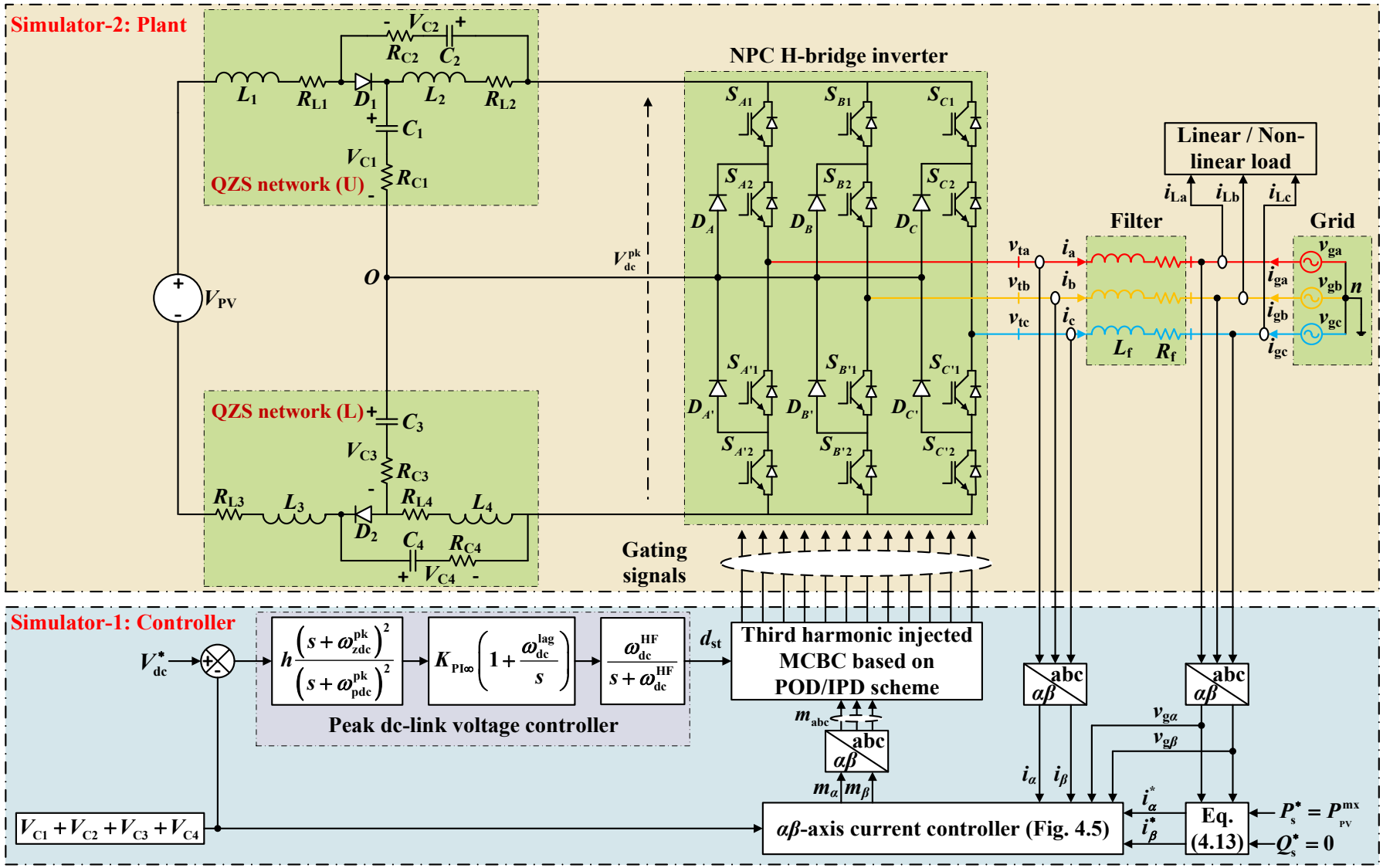


Fig. 4.3: Overall control strategy for 3-Φ *3L NPC-QZS* inverter based grid-tied *PV* system.

The state equation (4.11) is transformed in $\alpha\beta$ domain using the abc- to $\alpha\beta$ transformation and (4.10) as:

$$L_{\mathrm{f}}\frac{\mathrm{d}i_{\alpha\beta}}{\mathrm{d}t} = \frac{1}{2}m_{\alpha\beta}V_{\mathrm{dc}}^{\mathrm{pk}} - v_{\mathrm{g}\alpha\beta} - R_{\mathrm{f}}i_{\alpha\beta} \tag{4.12}$$

where $m_{\alpha\beta}$, $i_{\alpha\beta}$, and $v_{\mathrm{g}\alpha\beta}$ are $\alpha\beta$-axis components of modulating signal, AC-current, and grid voltage, respectively.

The system is operated in current control mode to realize *UPF* operation. For the purpose, the real power reference P_{s}^{*} is set to *MPP* and reactive power reference Q_{s}^{*} is set to zero. For the known grid voltage $v_{\mathrm{g}\alpha\beta}$, P_{s}^{*} and Q_{s}^{*}; $i_{\alpha\beta}^{*}$ is acquired using instantaneous power theory [160] as:

$$\begin{bmatrix} i_{\alpha}^{*} \\ i_{\beta}^{*} \end{bmatrix} = \frac{2}{3}\frac{1}{v_{\mathrm{g}\alpha}^{2} + v_{\mathrm{g}\beta}^{2}} \begin{bmatrix} v_{\mathrm{g}\alpha} & v_{\mathrm{g}\beta} \\ v_{\mathrm{g}\beta} & -v_{\mathrm{g}\alpha} \end{bmatrix} \begin{bmatrix} P_{\mathrm{s}}^{*} \\ Q_{\mathrm{s}}^{*} \end{bmatrix} \tag{4.13}$$

The *SOGI* integrates a sinusoidal input without introducing any phase-delay. A practical compensator $K_{\mathrm{SOGI}}^{\mathrm{Damp}}(s)$ is expressed as [157]:

$$K_{\mathrm{SOGI}}^{\mathrm{Damp}}(s) = K_{\mathrm{SP}} + \frac{2K_{\mathrm{SI}}\omega_{\mathrm{ac}}^{\mathrm{cut}}s}{s^{2} + 2\omega_{\mathrm{ac}}^{\mathrm{cut}}s + \omega_{\mathrm{g}}^{2}} \tag{4.14}$$

The K_{SP} determines the system dynamics. The *SOGI* attains infinite gain in a narrow band, whose width is decided by the integral gain K_{SI}, centered around angular grid frequency ω_{g}. The cut-off frequency $\omega_{\mathrm{ac}}^{\mathrm{cut}} \ll \omega_{\mathrm{g}}$. A *HF* pole $\omega_{\mathrm{ac}}^{\mathrm{HF}}$ is added to attenuate the gain of the $K_{\mathrm{SOGI}}^{\mathrm{Damp}}(s)$ at high frequencies and provide filtering action on the harmonic content of the sensed signal. The compensator is modified as:

$$K_{\mathrm{ac}}(s) = \underbrace{\left(K_{\mathrm{SP}} + \frac{2K_{\mathrm{SI}}\omega_{\mathrm{ac}}^{\mathrm{cut}}s}{s^{2} + 2\omega_{\mathrm{ac}}^{\mathrm{cut}}s + \omega_{\mathrm{g}}^{2}}\right)}_{\text{Damped}-SOGI} \underbrace{\left(\frac{\omega_{\mathrm{ac}}^{\mathrm{HF}}}{s + \omega_{\mathrm{ac}}^{\mathrm{HF}}}\right)}_{\text{HF pole}} \tag{4.15}$$

The target closed loop *BW* of 2π(1 kHz) is chosen corresponding to $1/10^{\mathrm{th}}$ of converter switching frequency. For closed loop control, a *BW* of -3 dB satisfying the inequality associated with ω^{BW} and gain crossover frequency ω^{gc} is written as:

$$\omega^{\mathrm{gc}} < \omega^{\mathrm{BW}} < 2\omega^{\mathrm{gc}} \tag{4.16}$$

The (4.16) can be approximated as $\omega^{\mathrm{BW}} \approx 1.5\omega^{\mathrm{gc}}$ [159]. Therefore, gain crossover frequency $\omega_{\mathrm{ac}}^{\mathrm{gc}}$ of 2π(666.67 Hz), PM of 60°, $\omega_{\mathrm{ac}}^{\mathrm{cut}}$ as 2π(10 Hz), and $\omega_{\mathrm{ac}}^{\mathrm{HF}} = 10\omega_{\mathrm{ac}}^{\mathrm{gc}}$ are selected accordingly.

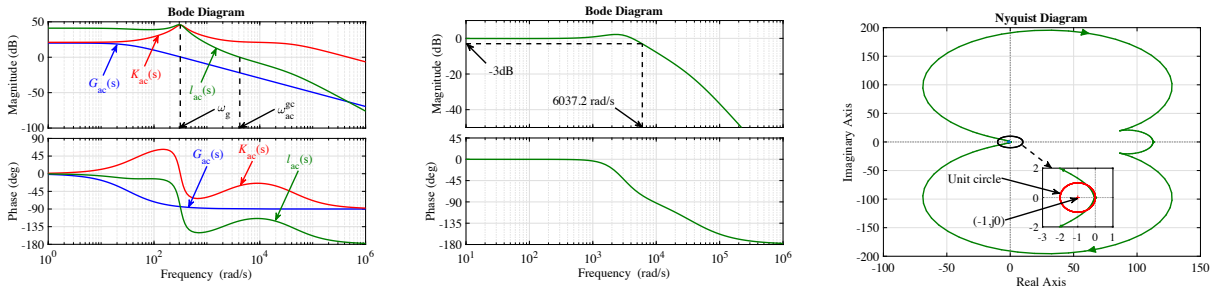
Using (4.12), transfer function is obtained as (4.17). Bode plot correspond to $G_{\mathrm{ac}}(s)$ is presented in Fig. 4.4(a).

$$G_{\mathrm{ac}}(s) = \frac{1}{L_{\mathrm{f}}s + R_{\mathrm{f}}} \tag{4.17}$$

The loop gain $l_{\mathrm{ac}}(s)$ for the current control is expressed as:

$$l_{\mathrm{ac}}(s) = K_{\mathrm{ac}}(s)G_{\mathrm{ac}}(s) \tag{4.18}$$

Unknown K_{SP} and K_{SI} are calculated at the desired $\omega_{\mathrm{ac}}^{\mathrm{gc}}$ as 11.254 and 174.506, respectively, using the procedure described in [164]. Having known the compensator parameters, the Bode plot of current controller $K_{\mathrm{ac}}(s)$ is shown in Fig. 4.4(a).



(a) **(b)** **(c)**

Fig. 4.4: Frequency response of the grid-tied current control. **(a)** Open-loop Bode plot of $G_{\mathrm{ac}}(s)$, $K_{\mathrm{ac}}(s)$, and $l_{\mathrm{ac}}(s)$. **(b)** Closed-loop Bode plot. **(c)** Nyquist plot of $l_{\mathrm{ac}}(s)$.

Bode plot of the loop gain $l_{\mathrm{ac}}(s)$ using the compensator $K_{\mathrm{ac}}(s)$, presented in Fig. 4.4(a), suggests PM of 60° at $\omega_{\mathrm{ac}}^{\mathrm{gc}}$. Correspondingly, the closed-loop frequency response, Fig. 4.4(b), yields a BW of 2π(960.848 Hz). The system will operate stably as Nyquist plot for $l_{\mathrm{ac}}(s)$, shown in Fig. 4.4(c), does not encircle the critical point $(-1, j0)$ and there is no pole in the right-half-plane of the $l_{\mathrm{ac}}(s)$ [161].

The controller output is divided by $(V_{\mathrm{C1}} + V_{\mathrm{C2}} + V_{\mathrm{C3}} + V_{\mathrm{C4}})/2$ to compensate for the converter voltage gain and to obtain modulating signal, while $V_{\mathrm{dc}}^{\mathrm{pk}}$ is equal to the sum of voltages resulting across *QZS* network capacitors. A grid voltage feed-forward compensation

$G_{\mathrm{ff}}(s) = 1/(5 \times 10^{-6}s + 1)$ is used to decouple converter and grid dynamics and to avoid start-up transient [171]. The $K_{\mathrm{ac}}(s)$ is used for both α- and β-axis current control as illustrated in Fig. 4.5.

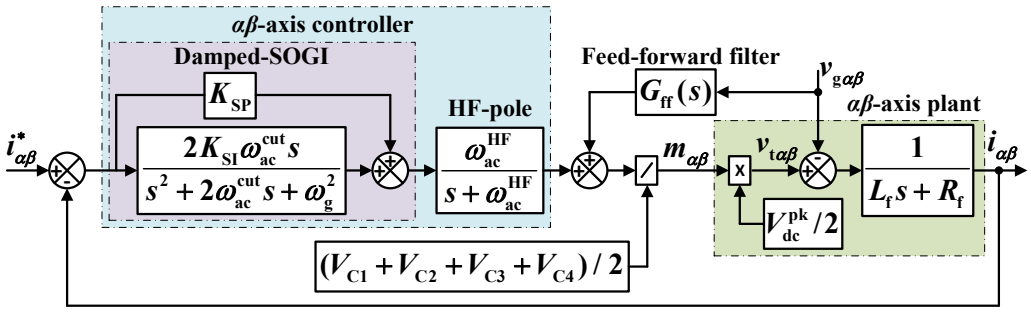


Fig. 4.5: Block diagram of current control loop in $\alpha\beta$-frame.

4.3.2 Design of *IDL* controller for DC-side

The control of *PDV* is realized by controlling *ST* duty ratio. Due to adoption of *ST* states, the v_{dc} as given by (4.8) is a pulsed waveform and it can not be utilized as feedback variable. Therefore, the *PDV* is estimated indirectly by measuring the voltages of capacitors of *QZS* network. To attain the above objective, the *ST* duty ratio to *PDV* transfer function $G_{\mathrm{dc}}^{\mathrm{pk}}(s)$ is determined.

From (4.8), the *PDV* $v_{\mathrm{dc}}^{\mathrm{pk}}$ is expressed as:

$$v_{\mathrm{dc}}^{\mathrm{pk}} = 2[v_{\mathrm{C1}} + v_{\mathrm{C2}} + R_{\mathrm{C}}(i_{\mathrm{L1}} + i_{\mathrm{L2}} - 2i_{\mathrm{dc}})] \tag{4.19}$$

After Laplace transform to perturbation and linearization to $v_{\mathrm{dc}}^{\mathrm{pk}}$, $\tilde{v}_{\mathrm{dc}}^{\mathrm{pk}}(s)$ is obtained. The $G_{\mathrm{dc}}^{\mathrm{pk}}(s)$ is expressed as ratio of $\tilde{v}_{\mathrm{dc}}^{\mathrm{pk}}(s)$ and $\tilde{d}_{\mathrm{st}}(s)$, resulted from the Laplace transform of (4.5) and $\tilde{v}_{\mathrm{dc}}^{\mathrm{pk}}(s)$, as:

$$G_{\mathrm{dc}}^{\mathrm{pk}}(s) = \frac{n_1 s + n_2}{LCs^2 + C(R_{\mathrm{L}} + R_{\mathrm{C}})s + (D_{\mathrm{nst}} - D_{\mathrm{st}})^2} \tag{4.20}$$

The coefficients n_1 and n_2 are expressed as:

$$n_1 = 4R_{\mathrm{C}}C(V_{\mathrm{C1}} + V_{\mathrm{C2}} - R_{\mathrm{C}}I_{\mathrm{dc}}) + 4L(I_{\mathrm{dc}} - I_{\mathrm{L1}} - I_{\mathrm{L2}})$$
$$n_2 = 4(D_{\mathrm{nst}} - D_{\mathrm{st}})(V_{\mathrm{C1}} + V_{\mathrm{C2}} - R_{\mathrm{C}}I_{\mathrm{dc}}) + 4(R_{\mathrm{L}} + 2R_{\mathrm{C}}D_{\mathrm{st}})(I_{\mathrm{dc}} - I_{\mathrm{L1}} - I_{\mathrm{L2}})$$

The (4.20) has *RHPZ*. The control of this system is challenging due to phase-lag introduced by *RHPZ*, which imposes constraint on the achievable *BW* and *GM*.

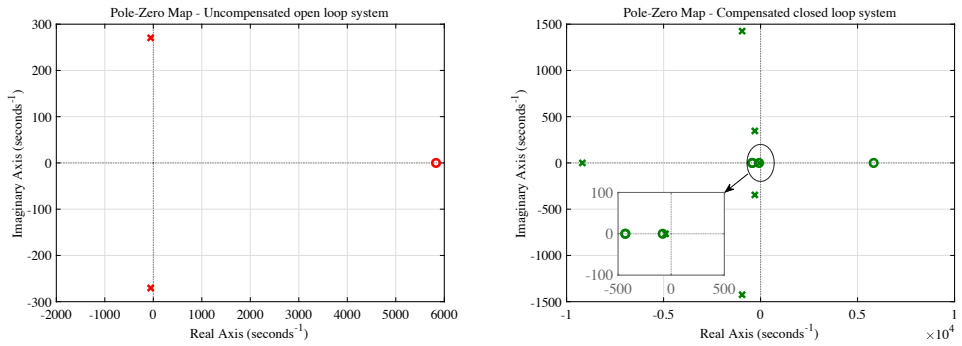
The voltages across the *QZS* network capacitors C_1, C_2, C_3, and C_4 are measured and are fed-back for comparing with reference voltage V_{dc}^{*}.

The requirements for a separate *PDV* controller suggest that its closed loop *BW* be lower than the AC-side *BW* while its crossover frequency $\omega_{\text{dc}}^{\text{gc}}$ be less than the folding frequency introduced by *RHPZ* [163]. Therefore, closed loop *BW* is selected as $1/5^{\text{th}}$ of AC-side closed loop *BW*, i.e., $2\pi(200\text{ Hz})$. Using $\omega^{\text{BW}} \approx 1.5\omega^{\text{gc}}$, $\omega_{\text{dc}}^{\text{gc}}$ is selected to be $2\pi(133.33\text{ Hz})$. The *PM* target is set at 60°.

The *PDV* control loop gain $l_{\text{dc}}^{\text{pk}}(s)$ is defined as:

$$l_{\text{dc}}^{\text{pk}}(s) = K_{\text{dc}}^{\text{pk}}(s)G_{\text{dc}}^{\text{pk}}(s) \tag{4.21}$$

where $K_{\text{dc}}^{\text{pk}}(s)$ is the controller transfer function for the *PDV* control. Pole-Zero plot of $G_{\text{dc}}^{\text{pk}}(s)$, shown as Fig. 4.6a, suggests *RHPZ*. The Bode plots of $G_{\text{dc}}^{\text{pk}}(s)$, shown in Fig. 4.7(a), suggests a gain crossover frequency of $2\pi(3397.3\text{ Hz})$, phase crossover frequency of $2\pi(134.895\text{ Hz})$, *PM* of −74.43°, and *GM* of −45.432 dB, and therefore an unstable system.



(a) **(b)**

Fig. 4.6: Pole-Zero map of *PDV* control system. **(a)** Uncompensated open-loop. **(b)** Compensated closed-loop.

At $\omega = \omega_{\text{dc}}^{\text{gc}}$, the $G_{\text{dc}}^{\text{pk}}(s)$ exhibits a phase of about −179.8°, and thus requires a lead compensator in the neighborhood of $\omega_{\text{dc}}^{\text{gc}}$. As phase boost of single-lead controller is low [164], a double-lead compensator $K_{\text{dc}}^{\text{lead}}(s)$ is used. It is defined as:

$$K_{\text{dc}}^{\text{lead}}(s) = h\frac{(s+\omega_{\text{zdc}}^{\text{pk}})^2}{(s+\omega_{\text{pdc}}^{\text{pk}})^2} = \frac{h}{q^2}\frac{\left(1+\frac{s}{\omega_{\text{zdc}}^{\text{pk}}}\right)^2}{\left(1+\frac{s}{\omega_{\text{pdc}}^{\text{pk}}}\right)^2} \tag{4.22}$$

where ω_{zdc}^{pk} and ω_{pdc}^{pk} are zero and pole frequency of $K_{dc}^{lead}(s)$, respectively, and $q = \omega_{pdc}^{pk}/\omega_{zdc}^{pk}$. The maximum phase boost $\phi_{mdc}^{pk} = 2\arctan\left(\frac{q-1}{2\sqrt{q}}\right)$ at ω_{dc}^{gc} generated by $K_{dc}^{lead}(s)$ Pole-Zero pair occurs at $\sqrt{\omega_{zdc}^{pk}\omega_{pdc}^{pk}}$. Using $K_{dc}^{pk}(s)$ as $K_{dc}^{lead}(s)$ in (4.21), the constant h is obtained by imposing unity loop gain at ω_{dc}^{gc},

$$l_{dc}^{pk}(j\omega)\big|_{\omega=\omega_{dc}^{gc}} = K_{dc}^{pk}(j\omega)G_{dc}^{pk}(j\omega)\big|_{\omega=\omega_{dc}^{gc}} = 1 \tag{4.23}$$

Adding an integral action in the compensator transfer function leads to *ZSSE*. Such lag compensation is given as:

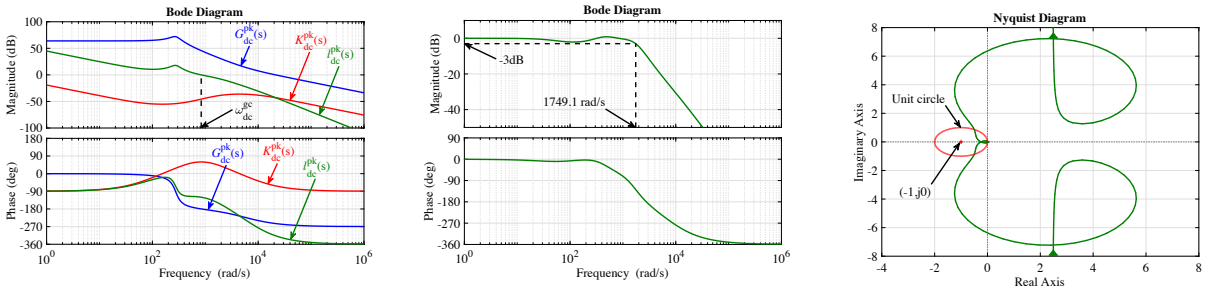
$$K_{dc}^{lag}(s) = K_{PI\infty}\left(1 + \frac{\omega_{dc}^{lag}}{s}\right) \tag{4.24}$$

The $K_{dc}^{lag}(s)$ is selected such that it should not affect either gain crossover frequency ω_{dc}^{gc} or desired *PM*. Therefore, the high-frequency gain $K_{PI\infty}$ is set to one, and the corner frequency ω_{dc}^{lag} is selected such that $\omega_{dc}^{lag} \ll \omega_{dc}^{gc}$. An acceptable value of ω_{dc}^{lag} is $\omega_{dc}^{lag} \leq \omega_{dc}^{gc}/10 = 2\pi(40/3 \text{ Hz})$, i.e., $2\pi(12.73 \text{ Hz})$.

A high frequency pole ω_{dc}^{HF} is introduced to lessen the gain of the $K_{dc}^{pk}(s)$ at high frequency and offer filtering to harmonic content of the sensed signal. At $\omega_{dc}^{HF} = 10\omega_{dc}^{gc}$, the complete transfer function of the controller $K_{dc}^{pk}(s)$ is expressed as:

$$K_{dc}^{pk}(s) = K_{dc}^{lead}(s)K_{dc}^{lag}(s)\frac{\omega_{dc}^{HF}}{s + \omega_{dc}^{HF}} \tag{4.25}$$

The Bode plots of designed $K_{dc}^{pk}(s)$ and $l_{dc}^{pk}(s)$ are shown in Fig. 4.7(a). The $l_{dc}^{pk}(s)$ has a gain crossover frequency of $2\pi(133.277 \text{ Hz})$, phase crossover frequency $2\pi(441.103 \text{ Hz})$, *PM*



(a) **(b)** **(c)**

Fig. 4.7: Frequency response of the *PDV* control. **(a)** Open loop Bode plot of $G_{dc}^{pk}(s)$, $K_{dc}^{pk}(s)$, and $l_{dc}^{pk}(s)$. **(b)** Closed loop Bode plot. **(c)** Nyquist plot of loop gain, $l_{dc}^{pk}(s)$.

60°, and *GM* 12.1 dB. The Fig. 4.7(b) suggests, a *BW* of 2π(278.372 Hz) to the corresponding closed-loop frequency response. The Nyquist plot of $l_{\mathrm{dc}}^{\mathrm{pk}}(s)$, shown in Fig. 4.7(c), does not encircle $(-1, j0)$ and has no right-half-plane pole that implies the system is stable [161]. All the poles of the closed-loop system are in the left-half-plane as shown in Fig. 4.6(b), thereby suggesting a stable system.

4.3.3 Design of *SMC* controller for DC-side

The *SMC* is a well-known robust state-of-the-art nonlinear controller that force the system states to track trajectories that lie on the sliding surface [172]. Three conditions namely hitting, existence, and stability to be fulfilled for the system entering into sliding mode.

The state space model for *SMC* using (4.2) and (4.3) is expressed as:

$$\dot{\boldsymbol{x}} = \boldsymbol{A_s} + \boldsymbol{B_s} u \tag{4.26}$$

where

$$\boldsymbol{A_s} = \begin{bmatrix} \frac{1}{L}\{-(R_{\mathrm{L}} + R_{\mathrm{C}})i_{\mathrm{L1}} - v_{\mathrm{C1}} + \frac{v_{\mathrm{PV}}}{2} + R_{\mathrm{C}} i_{\mathrm{dc}}\} \\ \frac{1}{L}\{-(R_{\mathrm{L}} + R_{\mathrm{C}})i_{\mathrm{L2}} - v_{\mathrm{C2}} + R_{\mathrm{C}} i_{\mathrm{dc}}\} \\ \frac{1}{C}(i_{\mathrm{L1}} - i_{\mathrm{dc}}) \\ \frac{1}{C}(i_{\mathrm{L2}} - i_{\mathrm{dc}}) \end{bmatrix} \qquad \boldsymbol{B_s} = \begin{bmatrix} \frac{1}{L}(v_{\mathrm{C1}} + v_{\mathrm{C2}} - R_{\mathrm{C}} i_{\mathrm{dc}}) \\ \frac{1}{L}(v_{\mathrm{C1}} + v_{\mathrm{C2}} - R_{\mathrm{C}} i_{\mathrm{dc}}) \\ \frac{1}{C}(i_{\mathrm{DC}} - i_{\mathrm{L1}} - i_{\mathrm{L2}}) \\ \frac{1}{C}(i_{\mathrm{DC}} - i_{\mathrm{L1}} - i_{\mathrm{L2}}) \end{bmatrix}$$

To satisfy hitting condition, the control law u adopting switching function is expressed as:

$$u = \frac{1}{2}\big(1 + sign(S)\big) \tag{4.27}$$

Although the *PDV* is the final control target that is estimated by the voltage across *QZS* network capacitors. As the stable motion on the sliding surface can not be reached with only one state variable, the number of state variables are increased to the extent minimum to avoid large number of tuning gains. Thus, a surface containing the state variables i_{L1} and v_{C1} are chosen to control *PDV*. Correspondingly, sliding coefficient matrix is expressed as:

$$\boldsymbol{J} = \begin{bmatrix} \gamma_1 & 0 & \gamma_2 & 0 \end{bmatrix} \tag{4.28}$$

To suppress steady-state error in both inductor current and capacitor voltage for fixed switching frequency operation, the sliding surface also requires an integral term of state-variables [166]. Thus, sliding surface S to regulate PDV to reference is expressed as:

$$\begin{aligned} S &= \gamma_1 x_1 + \gamma_2 x_3 + \int_0^t (v_{\mathrm{C}}^{\mathrm{sum}} - V_{\mathrm{dc}}^*)dt \\ &= \boldsymbol{J}\boldsymbol{x} + \int_0^t (v_{\mathrm{C}}^{\mathrm{sum}} - V_{\mathrm{dc}}^*)dt \end{aligned} \tag{4.29}$$

After hitting the surface S, existence condition must be ensured which suggests that the state trajectory should confine to the sliding surface and approach equilibrium. Therefore, the sliding function must satisfy:

$$\lim_{S\to 0} S \cdot \dot{S} < 0 \tag{4.30}$$

It suggests:

$$\begin{aligned} \lim_{S\to 0^+} \frac{dS}{dt} = \lim_{S\to 0^+} \Bigg[\frac{\gamma_1}{L} \Big\{ &- (R_{\mathrm{L}} + R_{\mathrm{C}}) i_{\mathrm{L1}} + v_{\mathrm{C2}} + \frac{v_{\mathrm{PV}}}{2} \Big\} \\ &- \frac{\gamma_2}{C} i_{\mathrm{L2}} + (v_{\mathrm{C}}^{\mathrm{sum}} - V_{\mathrm{dc}}^*) \Bigg] < 0 \end{aligned} \tag{4.31}$$

$$\begin{aligned} \lim_{S\to 0^-} \frac{dS}{dt} = \lim_{S\to 0^-} \Bigg[\frac{\gamma_1}{L} \Big\{ &- (R_{\mathrm{L}} + R_{\mathrm{C}}) i_{\mathrm{L1}} - v_{\mathrm{C1}} + \frac{v_{\mathrm{PV}}}{2} + R_{\mathrm{C}} i_{\mathrm{dc}} \Big\} \\ &+ \frac{\gamma_2}{C} (i_{\mathrm{L1}} - i_{\mathrm{dc}}) + (v_{\mathrm{C}}^{\mathrm{sum}} - V_{\mathrm{dc}}^*) \Bigg] > 0 \end{aligned} \tag{4.32}$$

The γ_1 and γ_2 are obtained from (4.31) and (4.32). When the sliding function satisfies (4.33) and (4.34) on sliding surface, the equivalent control input u_{eq} is obtained as (4.35).

$$S = \boldsymbol{J}\boldsymbol{x} + \int_0^t (v_{\mathrm{C}}^{\mathrm{sum}} - V_{\mathrm{dc}}^*)dt = 0 \tag{4.33}$$

$$\dot{S} = \boldsymbol{J}\boldsymbol{x} + (v_{\mathrm{C}}^{\mathrm{sum}} - V_{\mathrm{dc}}^*) = 0 \tag{4.34}$$

$$\begin{aligned} u_{\mathrm{eq}} &= -[\boldsymbol{J}\boldsymbol{B}_{\mathbf{s}}]^{-1} [\boldsymbol{J}\boldsymbol{A}_{\mathbf{s}} + (v_{\mathrm{C}}^{\mathrm{sum}} - V_{\mathrm{dc}}^*)] \\ &= \frac{\frac{\gamma_1}{L} \big\{ (R_{\mathrm{L}} + R_{\mathrm{C}}) i_{\mathrm{L1}} + v_{\mathrm{C1}} - \frac{v_{\mathrm{PV}}}{2} - R_{\mathrm{C}} i_{\mathrm{dc}} \big\} + \frac{\gamma_2}{C} (i_{\mathrm{dc}} - i_{\mathrm{L1}}) + (V_{\mathrm{dc}}^* - v_{\mathrm{C}}^{\mathrm{sum}})}{\frac{\gamma_1}{L} (v_{\mathrm{C1}} + v_{\mathrm{C2}} - R_{\mathrm{C}} i_{\mathrm{dc}}) + \frac{\gamma_2}{C} (i_{\mathrm{dc}} - i_{\mathrm{L1}} - i_{\mathrm{L2}})} \end{aligned} \tag{4.35}$$

The u_{eq} is taken as d_{st} and its value is limited to maximum 0.4 [108]. Corresponding to u_{eq}, the closed loop system is obtained from (4.26). The stability condition can be obtained by deriving system eigenvalues as a function of the coefficient γ_1, γ_2 that have negative real parts and an acceptable dynamic operation [173].

4.4 MODIFIED *MCBC* STRATEGY

The procedure for *PWM* gating signal generation using *POD* and *IPD* modulation yielding *ST* is summarized herewith. The AC-side current controller provides m_α and m_β and then modulating signal m_{abc} is generated through $\alpha\beta$-to abc transformation. The third harmonic injected signal alters m_{abc} as:

$$m_{\text{a}}^{*} = M\sin(\omega_{\text{g}}t) + \frac{1}{6}M\sin(3\omega_{\text{g}}t) \tag{4.36}$$

Similarly, m_{b}^{*} and m_{c}^{*} can be obtained. Using $M^2 = m_\alpha^2 + m_\beta^2$ [159], m_{abc}^{*} is obtained in terms of m_{abc} and $m_{\alpha\beta}$ as:

$$m_{\text{abc}}^{*} = \frac{3}{2}m_{\text{abc}} - \frac{2}{3}\frac{m_{\text{abc}}^3}{m_\alpha^2 + m_\beta^2} \tag{4.37}$$

4.4.1 Third harmonic injected *MCBC* based on *POD* scheme

The procedure for third harmonic injected *MCBC* based on *POD PWM* is shown in Fig. 4.8(a). Two opposite phase carriers V_{car}^{+} and V_{car}^{-} are used for comparing with reference m_{abc}^{*} and *ST* signals. Two straight lines $V_{\text{p}} = (1 - d_{\text{st}})$ and $V_{\text{n}} = -(1 - d_{\text{st}})$ are used for generating *ST* signals. The *ST* is realized when upper carrier V_{car}^{+} is greater than V_{p} or lower carrier V_{car}^{-} less than V_{n}. Therefore, inverter goes in full DC-link *ST* state, where all the power switches of inverter leg is turned on as shown in Fig. 4.8(b).

4.4.2 Third harmonic injected *MCBC* based on *IPD* scheme

In third harmonic injected *MCBC* based on *IPD PWM*, as shown in Fig. 4.8(c), two in-phase carriers V_{car}^{+} and V_{car}^{-} are used for comparing with reference m_{abc}^{*} and *ST* signals. Same as *POD PWM*, two straight lines $V_{\text{p}} = (1 - d_{\text{st}})$ and $V_{\text{n}} = -(1 - d_{\text{st}})$ are used for generating *ST* signals. In this *PWM* technique, full DC-link *ST* is not possible. So, in this method *UDST* can be achieved when upper carrier V_{car}^{+} is greater than V_{p} and *LDST* can be achieved when lower carrier V_{car}^{-} is less than V_{n} as shown in Fig. 4.8(d).

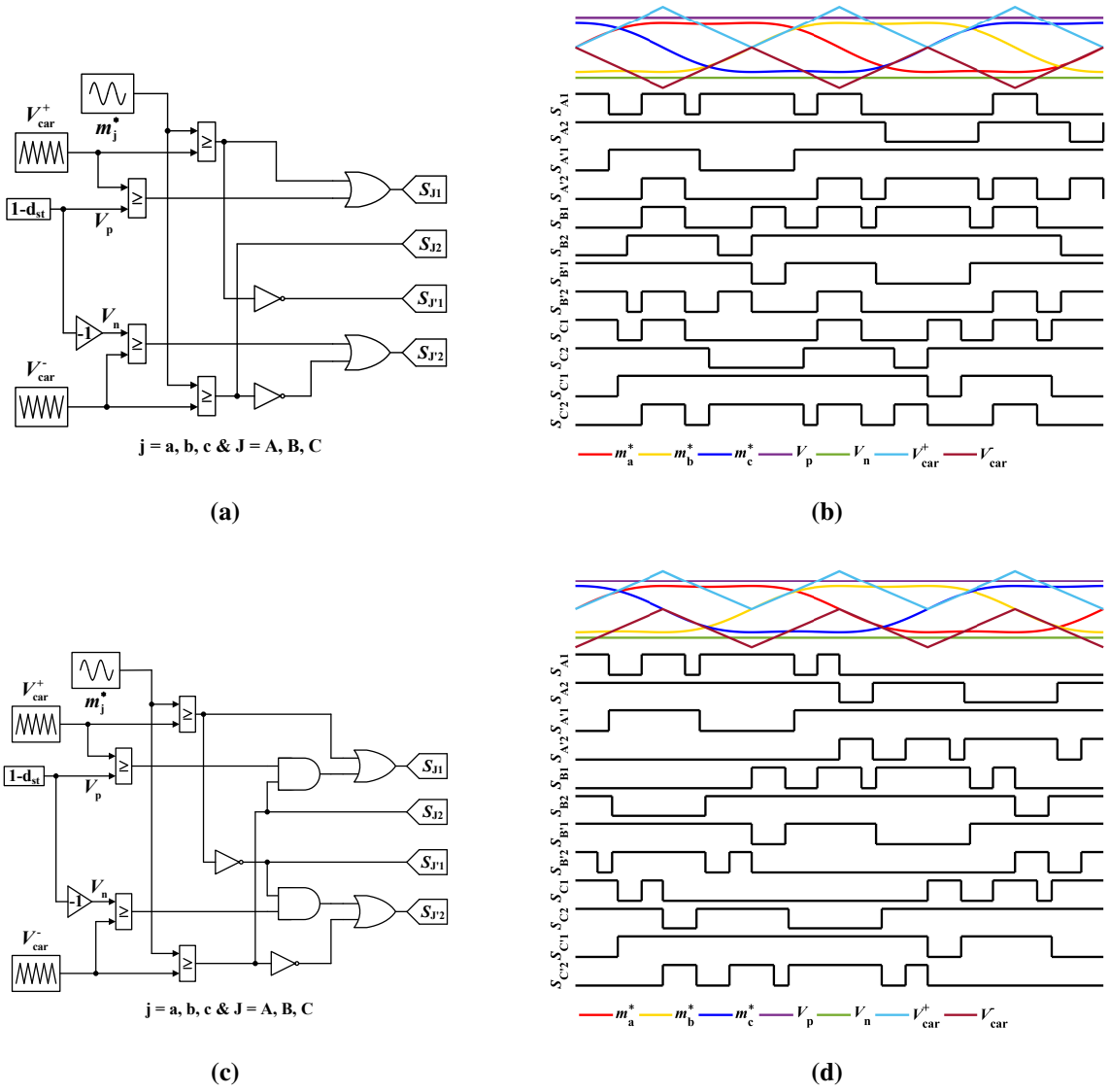


Fig. 4.8: Level-shifted 3rd harmonic injected *MCBC* modulation techniques. **(a)** Implementation of *POD* method. **(b)** *POD* method waveforms. **(c)** Implementation of *IPD* method. **(d)** *IPD* method waveforms.

4.5 SIMULATION RESULTS

The proposed *IDL*-damped-*SOGI* controller has been realized under MATLAB/Simulink. The controller design and performance are validated through *HIL RTS* in OPAL-RT. For the design parameters listed in Table 4.1, the performance is investigated for *MCBC* based on modified *POD* and *IPD* modulation for *3L NPC-QZS* inverter based *PV* system. To test the efficacy of the proposed control, the results are presented for the disturbances originated from the input side and step change in loads. Furthermore, the performance of the *IDL*-damped-*SOGI* controller is compared with *SMC*-damped-*SOGI* controller combination.

The technical specification of the used Havells *PV* modules is summarized in Table 4.2 [167]. The energy source is realized through three parallel connections of ten series-connected modules. The typical *I–V* and *P–V* characteristics of the *PV* source are shown in Fig. 4.9. The weather conditions at maximum *PV* output power $P_{\text{PV}}^{\text{mx}}$ and corresponding voltage $V_{\text{PV}}^{\text{mx}}$ are summarized from Fig. 4.9 as:

$WC1:$ 1000 W/m^2 and 25 °C, $V_{\text{PV}}^{\text{mx}} = 191.2$ V, $P_{\text{PV}}^{\text{mx}} = 3000$ W.
$WC2:$ 500 W/m^2 and 25 °C, $V_{\text{PV}}^{\text{mx}} = 184.16$ V, $P_{\text{PV}}^{\text{mx}} = 1420.3$ W.
$WC3:$ 250 W/m^2 and 50 °C, $V_{\text{PV}}^{\text{mx}} = 172.13$ V, $P_{\text{PV}}^{\text{mx}} = 646.40$ W.

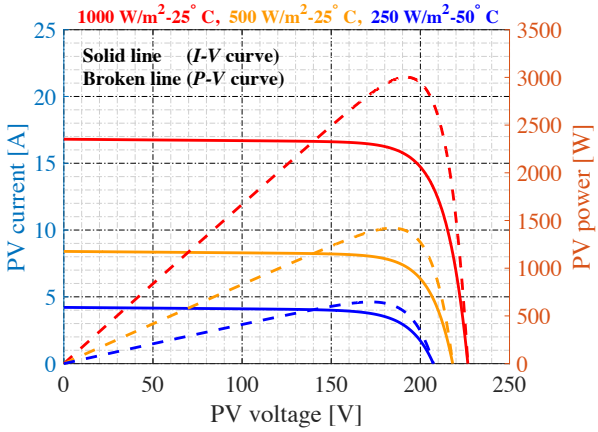


Fig. 4.9: *I–V* and *P–V* characteristics for different *WCs* (ENVIRO PVM6/PVC-100).

Table 4.2. Adjusted Havells solar panel specification

Parameter	**Values**
Electrical properties	
Maximum power	100 W
MPP voltage	19.12 V
MPP current	5.23 A
Open circuit voltage	22.68 V
Short circuit current	5.60 A
Module efficiency (%)	14.9
Number of cells	$4 * 9$
Series resistance	0.0094 Ω
Parallel resistance	281.47 Ω
Temperature coefficients	
Nominal power/temperature coefficient	−0.40 %/°C
Open circuit voltage/temperature coefficient	−0.30 %/°C
Short circuit current/temperature coefficient	0.05 %/°C

4.5.1 With input-side dynamics

WCs, *WC*1 and *WC*3 are considered for transient analysis due to significant change in both the associated irradiation and temperature. Correspondingly, V_{PV} is changed from 191.2 V to 172.13 V at $t = 1$ s. Correspondingly, the transient performance with *POD* and *IPD PWM* schemes are shown in Figs. 4.10 and 4.11, respectively. This change in input voltage causes a corresponding change in d_{st} with required boost, whereas there is overshoot and undershoot in v_{dc}. The voltage across *QZS* network capacitors v_{C1}, v_{C2}, v_{C3}, and v_{C4} experience transients, however, their sum $v_{\mathrm{C}}^{\mathrm{sum}}$, settle to a V_{dc}^{*}. The steady-state values are given in Table 4.3. The steady-state inductor currents of *QZS* network change from 16.48 A to 3.84 A for both *POD* and *IPD PWM* schemes.

Table 4.3. Steady-state values of *ST* duty ratios and capacitor voltages

Parameters	***POD* scheme**		***IPD* scheme**	
	***WC*1**	***WC*3**	***WC*1**	***WC*3**
D_{st}	0.2699	0.2893	0.2699	0.2893
V_{C1} [V]	148.30	143.00	148.40	143.30
V_{C2} [V]	52.37	56.97	52.41	57.05
V_{C3} [V]	147.30	143.00	147.20	142.80
V_{C4} [V]	52.03	56.96	51.99	56.88

The Figs. 4.10(b) and 4.11(b) suggest *UPF* operation. The real power P_{s}, reactive power Q_{s} change rapidly with the change in input condition. Small ripples in P_{s} and Q_{s} are due to *PWM* switching harmonics. A notch is observed in the response of P_{s}, Q_{s} at $t = 1$ s because cross-coupling exist in these powers. For perfect decoupling, the i_{α} and i_{β} should follow i_{α}^{*} and i_{β}^{*} on instantaneous basis. The inverter exhibits effective performance due to the realization of closed-loop control on DC- and AC-sides through proposed *IDL* and damped-*SOGI*, respectively. The system attains new steady-state conditions quickly with very small duration transients.

IDL-damped-*SOGI* with *MCBC* based on *POD* scheme

With the gating *PWM* signals generated through 3$^{\mathrm{rd}}$ harmonic injected *MCBC* based on *POD*, the DC-link voltage v_{dc} in steady-state, as shown in Fig. 4.10(a), changes between 0 and V_{dc}^{*}. A small duration transient is observed in all the voltages. The inverter operates in full DC-link *ST*. Pole voltage v_{tao}, as shown in Fig. 4.10(c), contains three levels 0 and $\pm V_{\mathrm{dc}}^{*}/2$. The phase voltage

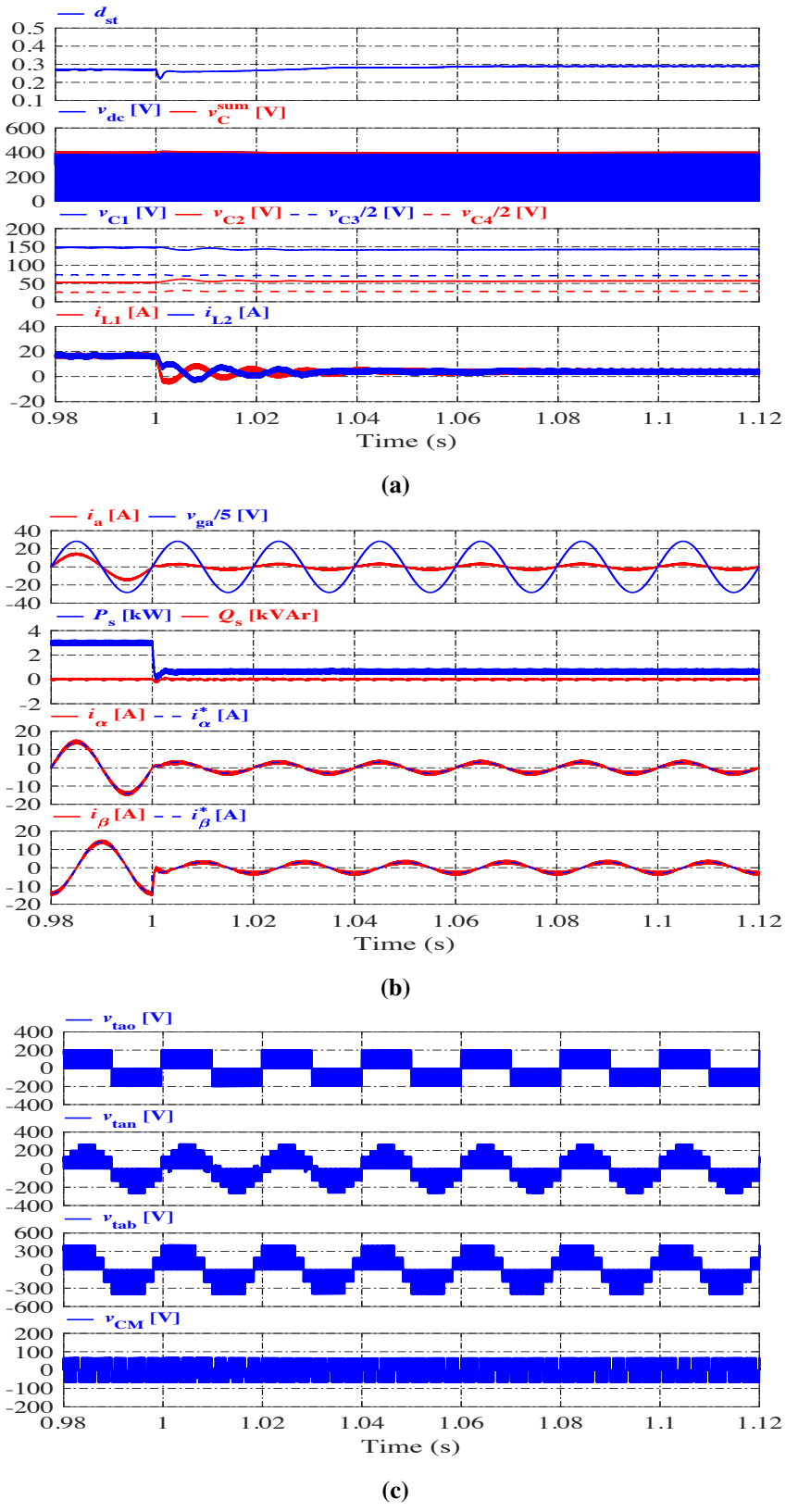
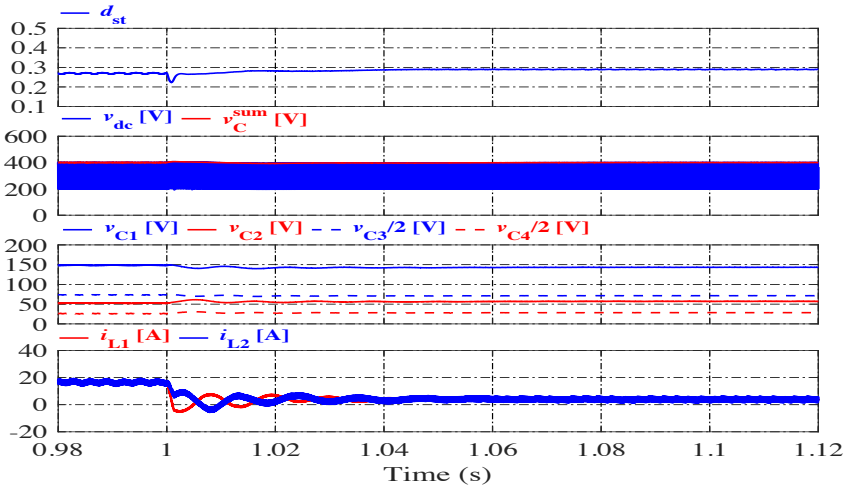
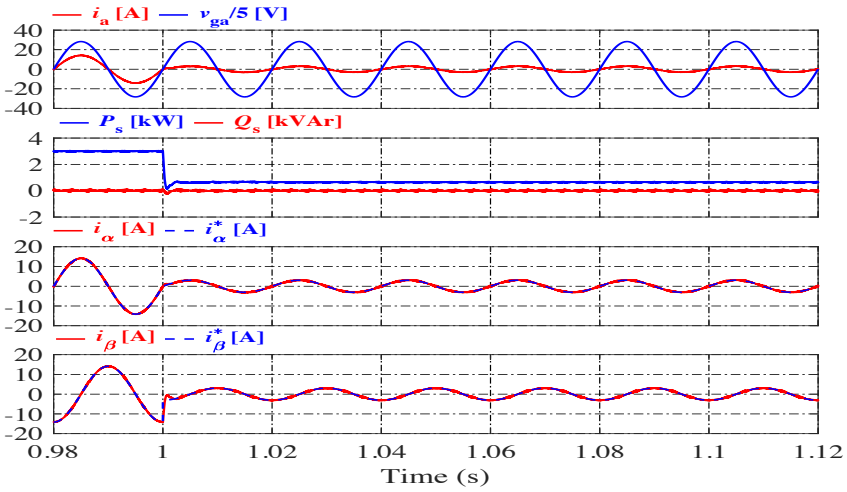


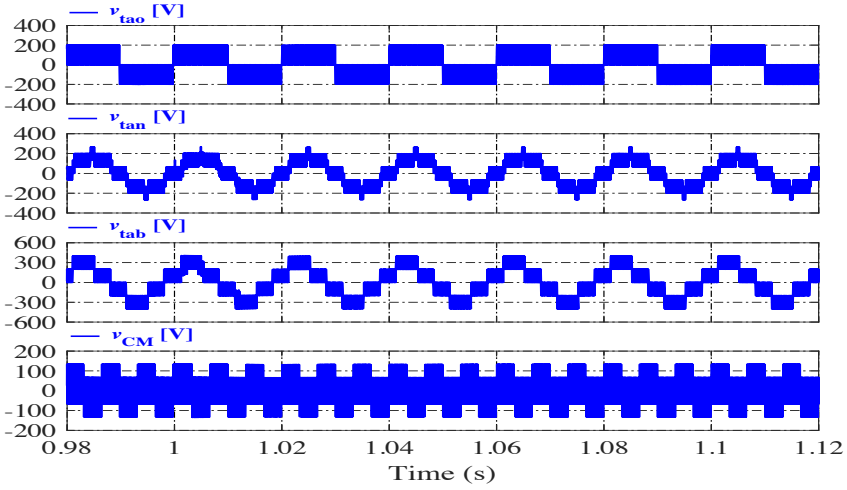
Fig. 4.10: Dynamic behavior for change in weather condition with *POD* scheme. **(a)** *ST* duty ratio; DC-link voltage, sum of capacitor voltages; capacitor voltages; and inductor currents. **(b)** Grid voltage, inverter current; real, reactive power; i_α, i_α^*; and i_β, i_β^*. **(c)** Pole voltage; phase voltage; line voltage; and *CMV*.



(a)



(b)



(c)

Fig. 4.11: Dynamic behavior for change in weather condition with *IPD* scheme. **(a)** *ST* duty ratio; DC-link voltage, sum of capacitor voltages; capacitor voltages; and inductor currents. **(b)** Grid voltage, inverter current; real, reactive power; i_α, i_α^*; and i_β, i_β^*. **(c)** Pole voltage; phase voltage; line voltage; and *CMV*.

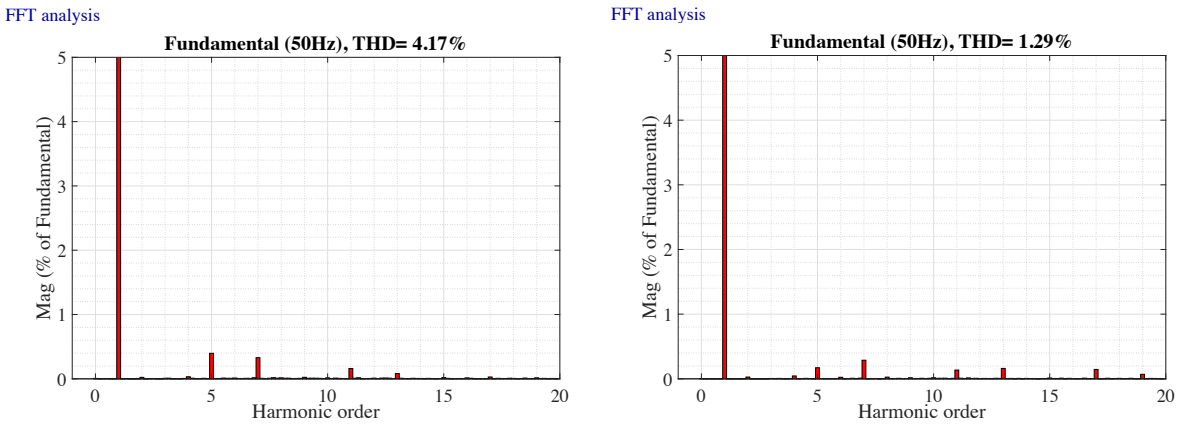
v_{tan} has seven levels 0, $\pm V_{\text{dc}}^*/3$, $\pm V_{\text{dc}}^*/2$, and $\pm 2V_{\text{dc}}^*/3$; the line-to-line voltage has five levels 0, $\pm V_{\text{dc}}^*/2$, and $\pm V_{\text{dc}}^*$. The average value of 3-Φ pole voltage [174], referred as *CMV* v_{CM}, is equal to $V_{\text{dc}}^*/6$. The *CMV* is an important performance criteria for *3L NPC-QZS* inverter because of absence of galvanic isolation. The high-frequency *CMV* induces a leakage current which can deteriorate the quality of line current [175].

The inverter current i_{a} contains dominant lower order harmonics (5^{th} and 7^{th}), as shown in Fig. 4.12(a) and is having a *THD* of 4.17%. The *THD* value satisfies IEEE standards due to the adoption of *3L* topology [168].

IDL-damped-*SOGI* with *MCBC* based on *IPD* scheme

Using the *PWM* signals obtained through 3^{rd} harmonic injected *MCBC* based on *IPD*, the inverter operates in *UDST* or *LDST*. The DC-link voltage, as shown in Fig. 4.11(a), changes between $V_{\text{dc}}^*/2$ and V_{dc}^*. As shown in Fig. 4.11(c), the pole voltage v_{tao} has three levels 0 and $\pm V_{\text{dc}}^*/2$; the phase voltage v_{tan} has nine levels 0, $\pm V_{\text{dc}}^*/6$, $\pm V_{\text{dc}}^*/3$, $\pm V_{\text{dc}}^*/2$, and $\pm 2V_{\text{dc}}^*/3$; the line-to-line voltage contains five levels 0, $\pm V_{\text{dc}}^*/2$, and $\pm V_{\text{dc}}^*$. The magnitude of *CMV* is equal to $V_{\text{dc}}^*/3$.

The inverter current i_{a} is close to sinusoidal. It characterizes with *THD* of 1.29%, which is much lower than the *THD* resulted with the *POD* as shown in Fig. 4.12(b). The waveform of i_{a} contains dominant lower order harmonics (5^{th} and 7^{th}) with relatively low magnitudes. Therefore, due to the small inverter current *THD*, ripples in real power P_{s}, reactive power Q_{s}, and $\alpha\beta$-axis current i_α and i_β are low as compared with *POD* scheme.



(a) **(b)**

Fig. 4.12: *FFT* spectrum of inverter current. **(a)** *POD* scheme. **(b)** *IPD* scheme.

4.5.2 Neutral-point voltage balancing

The DC-link neutral-point voltage balancing in *3L NPC-QZS* inverter is achieved by balancing v_{C1} and v_{C3} voltages [64]. Fig. 4.13 shows the variations of v_{C1} and v_{C3} over one period of the fundamental frequency for the *POD* and *IPD* schemes. For the *POD* scheme the v_{C1} and v_{C3} are alternatively increasing and decreasing and thus resulting in zero average neutral-point current, which is not possible for *IPD* scheme. Table 4.4 summarizes the performance comparison between *POD* and *IPD PWM* schemes. *CMV* with *POD* is 50% to its value with *IPD* scheme. This can be verified from Fig. 4.14, where the *IPD* and *POD* switching schemes are drawn for one switching cycle. The *THD* and input current ripples are less with *IPD* scheme.

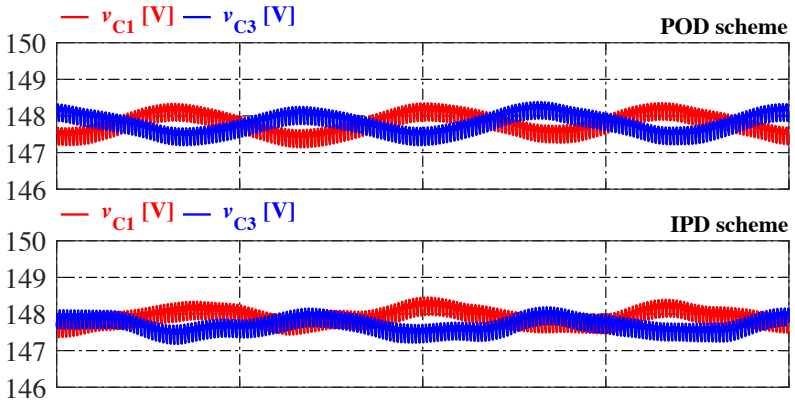


Fig. 4.13: Series capacitor voltages for *POD* and *IPD* scheme.

Table 4.4. Performance comparison of *POD* and *IPD PWM* scheme

Parameters	***POD* scheme**	***IPD* scheme**
CMV	$V^*_{dc}/6$	$V^*_{dc}/3$
Source current ripple (pk-pk)	23.63%	7.43%
THD	4.17%	1.29%
Average neutral-point current	Zero	Non-zero

4.5.3 With grid-side dynamics

Initially the system is operating at weather condition *WC*1. Correspondingly, i_a is in-phase with v_{ga}, while i_{ga} is 180° out-of-phase with v_{ga}. This is due to the opposite reference direction of i_a and i_{ga}. As shown in Fig. 4.15, a linear load of 4 kW and 0.8 lagging power-factor is switched-in suddenly at $t = 0.5$ s. The inverter current i_a remains in-phase with v_{ga}, thereby resulting in *UPF*

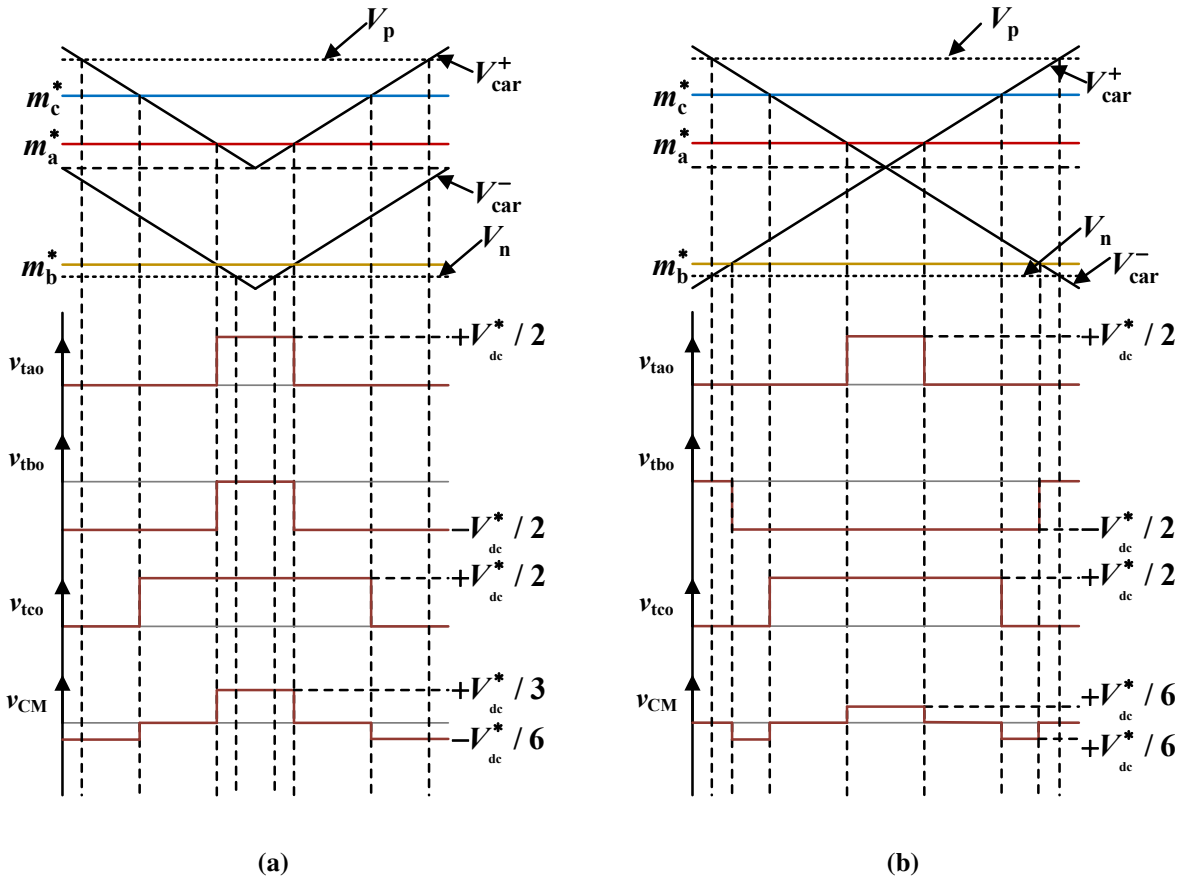


Fig. 4.14: Pole voltages v_{tabco} and common-mode voltage v_{CM} with different modulation techniques in one switching cycle. **(a)** *IPD* scheme. **(b)** *POD* scheme.

operation. It is observed that the *PV* system is supplying rated 3 kW, whereas the remaining load demand is supplied by the grid. Due to reactive power flow, i_{ga} leads v_{ga}.

Fig. 4.16 shows performance when 3-Φ six-pulse bridge rectifier feeding a load of 1 kW is applied suddenly at $t = 0.5$ s. It is observed from Fig. 4.16(b) that the rectifier input currents although are highly distorted with *THD* of 30.74%, the proposed controller drives the inverter output current to be sinusoidal at *UPF*.

4.5.4 Performance with *SMC*-damped-*SOGI* controller

The performance of the proposed *IDL*-damped-*SOGI* with *POD PWM* has been discussed previously. The performance of this controller is compared with the *SMC*-damped-*SOGI* controller. The design of *SMC* is explained in subsection 4.3.3. During the analysis, the

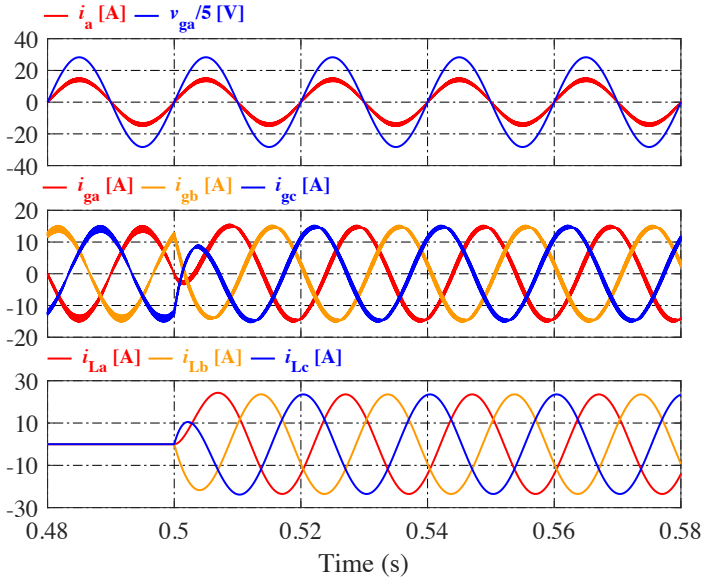
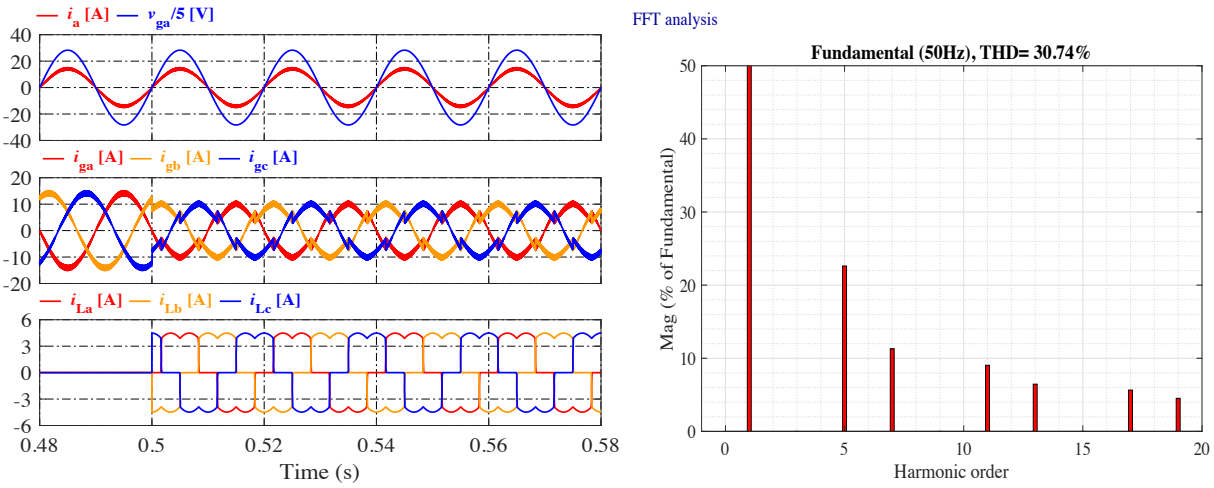


Fig. 4.15: Dynamic behavior under linear load: v_{ga} and i_{abc}; i_{gabc}; and i_{Labc}.



(a) **(b)**

Fig. 4.16: Dynamic behavior under non-linear load. **(a)** Grid voltage and inverter current; 3-Φ grid current; and 3-Φ load current. **(b)** *FFT* spectrum of load current.

disturbance is assumed to be initiated due to change in weather condition from the input side. The weather condition is changed from *WC*1 to *WC*3.

With the change from *WC*1 to *WC*3 arising due to the change in solar irradiation, V_{PV} is changed from 191.2 V to 172.13 V at t = 1 s and performance characteristics are presented in Fig. 4.17. Fig. 4.17(a) shows the voltages v_{C1} and v_{C2}. As evident from Fig. 4.17(b), the v_C^{sum} with *SMC* experience sustained oscillations during steady-state and a large overshoot at the initiation of a transient. Whereas, the proposed *IDL* controller is capable to track V_{dc}^* without

oscillations and with low overshoot. These oscillations with *SMC* at steady-state cause non-*ZSSE*. Therefore, it is justified to suggest that the response of *IDL* is that of an underdamped system while *SMC* responds like that of a highly damped system. As *ST* duty ratio and modulating signal are interdependent, oscillations observed in d_{st} will be reflected on the AC-side. Thus, P_s and Q_s show sustained ripple in the steady-state illustrated in Fig. 4.17(c). Due to reflection of DC-side ripples into AC-side, the *THD* increased to 4.42% as presented in Fig. 4.17(d).

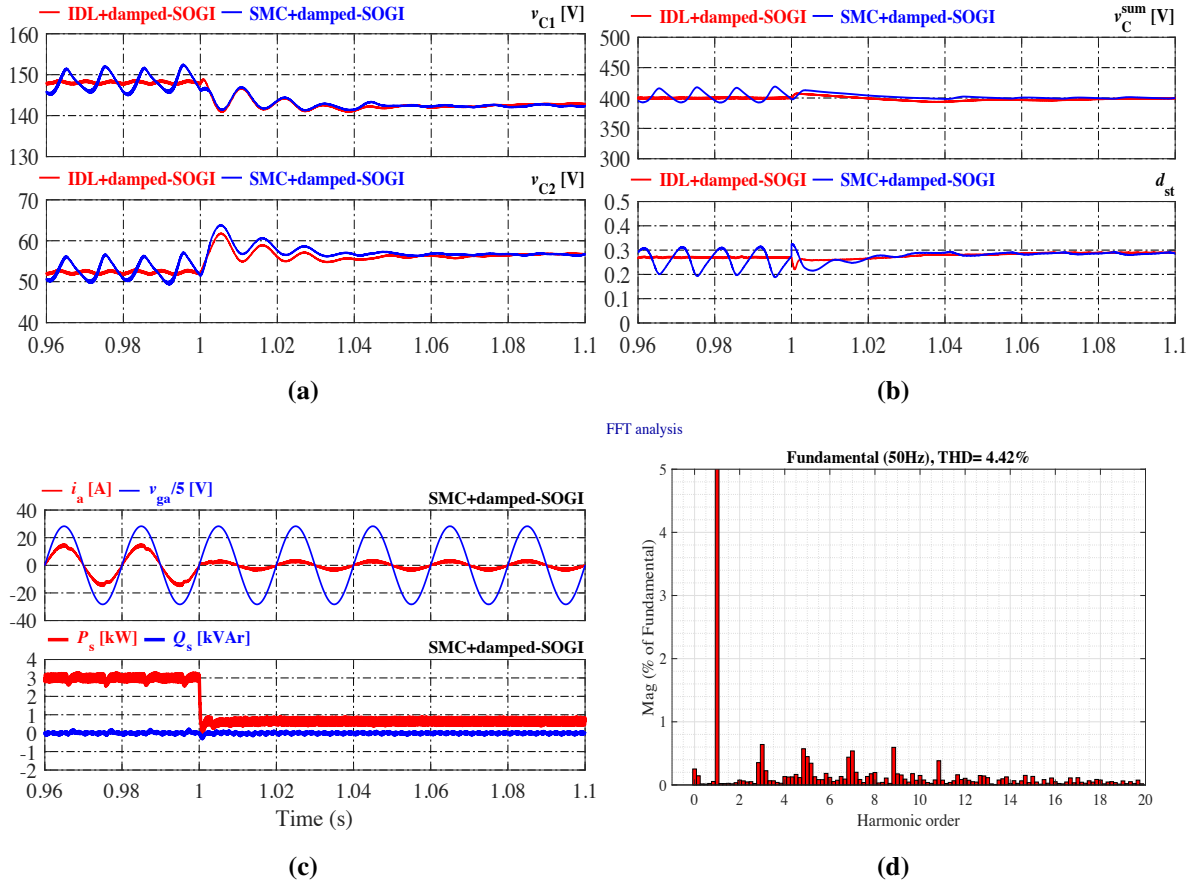


Fig. 4.17: Comparative performance of *IDL*-damped-*SOGI* and *SMC*-damped-*SOGI*. **(a)** Capacitor voltages v_{C1} and v_{C2}. **(b)** Estimated DC-link voltage v_C^{sum} and *ST* duty ratio d_{st}. **(c)** Grid voltage, inverter current; and real power, reactive power. **(d)** *FFT* spectrum of inverter current.

4.6 REAL-TIME VALIDATION USING OPAL-RT

The performance of the system shown in Fig. 4.3 is validated using *HIL RTS* in OPAL-RT OP4510 with Intel Xeon 4-core 3.5 GHz real-time processor, Xilinx Kintex 7 field-programmable gate array, and analog/digital channels. The equivalent *HIL* setup and validation arrangement of the proposed control schemes are shown in Figs. 4.18(a) and 4.18(b), respectively. *HIL* simulation

has the potential of parallel processing in real-time and providing results corresponding to hardware results [169, 176].

The controller stage and the power stage are two main components of the grid-tied *3L NPC-QZS* inverter based *PV* that are modeled in Simulator-1 and Simulator-2, respectively. The Simulator-1 has been embedded with the *IDL* controller, damped-*SOGI* controller, and a high-frequency *PWM* gating pattern generator. The power stage components namely energy source, *QZS* networks, *NPC* inverter arrangement, filter, and grid are embedded in Simulator-2. The *PWM* signals for the *3L NPC-QZS* inverter are supplied from Simulator-1 to Simulator-2. The system measurements from Simulator-2 are fed to Simulator-1 in real-time manner. These Simulators are connected through the DB37 connectors for digital and analog inputs and outputs. The *DSOs* are used to monitor communicating signals. As a sample case for real-time verification, *IPD* modulation scheme is taken and the change in weather condition is initiated. It is evident from Fig. 4.19 that the nature and values of capacitor voltages (v_{C1}, v_{C2}, v_{C3}, and v_{C4}), their sum v_C^{sum}, grid voltage (v_{ga}), and inverter current (i_a) are the same as resulted with the MATLAB/Simulink (Fig. 4.11), which validates the hypothesis and controller design.

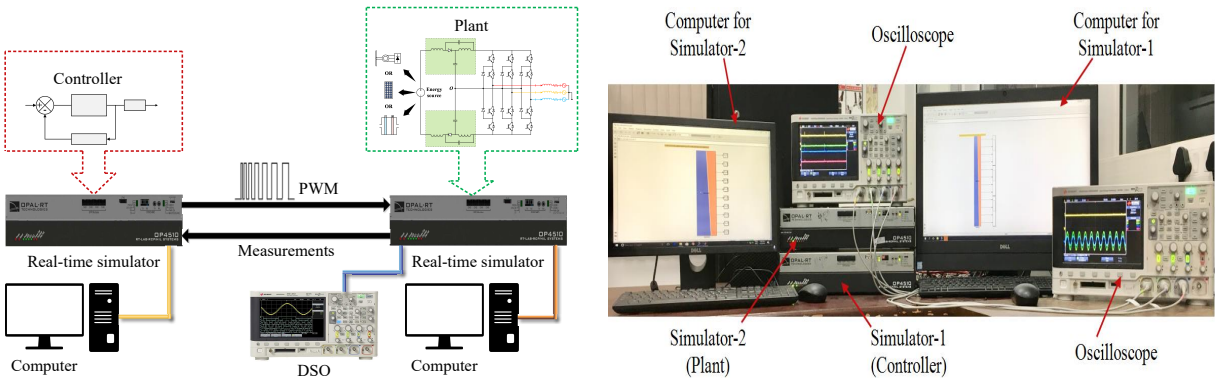
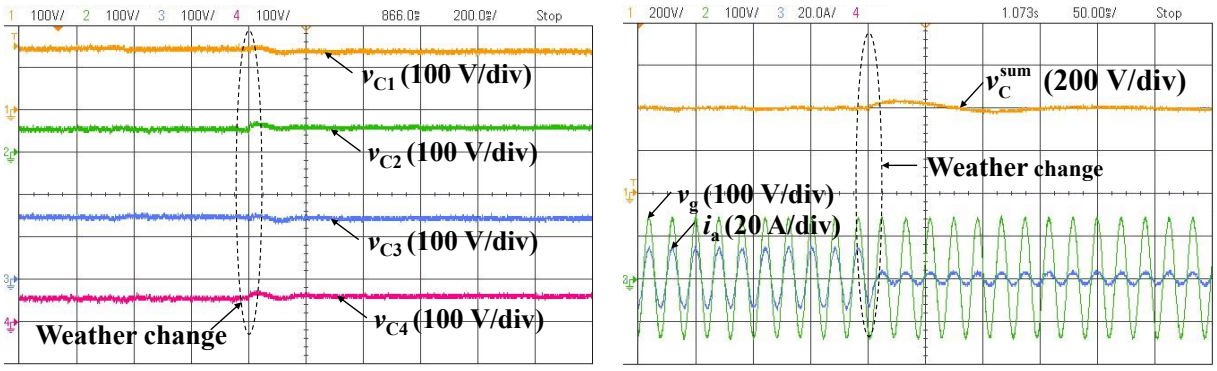


Fig. 4.18: *HIL RTS* setup in OPAL-RTs. **(a)** Equivalent of *HIL RTS* setup. **(b)** *HIL RTS* validation arrangement.

4.7 LABORATORY SETUP AND EXPERIMENTAL RESULTS

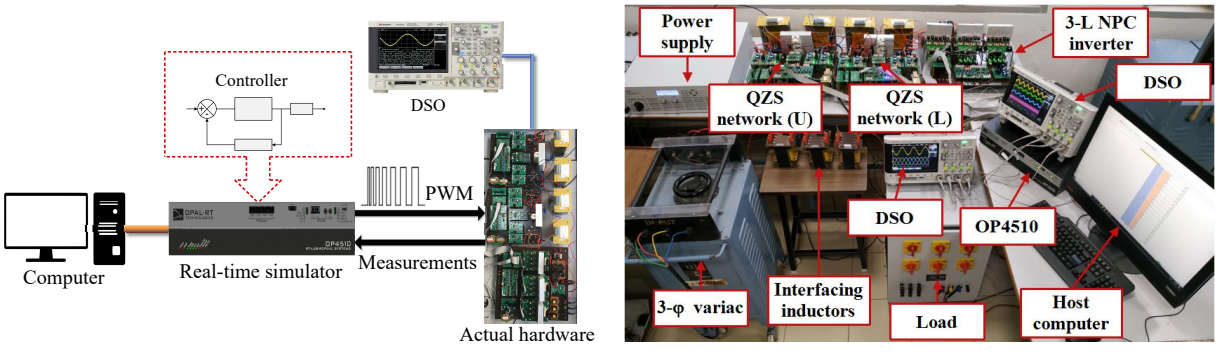
To validate the efficacy of the proposed control with modified *POD* and *IPD PWM* arrangements, an experimental system is developed in the laboratory. It is interfaced with the grid using 3-Φ variac. The equivalent *HIL* setup, which is realized using actual hardware, and a laboratory setup are shown in the Figs. 4.20(a) and 4.20(b), respectively. The system prototype consists



(a) **(b)**

Fig. 4.19: *HIL RTS* results of dynamic behavior for change in weather condition from *WC*1 to *WC*3. **(a)** v_{C1}, v_{C2}, v_{C3}, and v_{C4}. **(b)** v_C^{sum}, v_{ga}, and i_a.

of two *QZS* networks, *3L NPC* inverter, programmable DC-power supply (KEYSIGHT make, model:N8952A), and interfacing inductors. For the control purpose, the IC7840 based voltage sensing circuit, HE055T01 hall-Effect current sensors, and control unit OP4510 are used. The OP4510 configuration features are already detailed Section 4.6. The proposed controller with modified *POD* and *IPD PWM* techniques is programmed on a host computer in MATLAB/Simulink. It is exported to OPAL-RT using RT-LAB software. The values of *QZS* network and output filter parameters, grid and reference DC-link voltage are taken the same as reported in the MATLAB/Simulink and *HIL RTS* analysis. Two four-channel *DSO*s (KEYSIGHT make, model:DSOX2024A) are used to record dynamic conditions. Two experiments are performed in the laboratory, first when transients are initiated from the input side and another is performed for application of linear/non-linear load.



(a) **(b)**

Fig. 4.20: OPAL-RT and physical system *HIL* setup. **(a)** Equivalent of physical system *HIL* setup. **(b)** Physical system *HIL* validation arrangement.

4.7.1 With input-side dynamics

The Figs. 4.21 and 4.22 depict the dynamic behavior of the presented system when subjected to change in input supply from (191.2 V, 3 kW) to (172.13 V, 646.40 W).

Figs. 4.21(a) and 4.22(a) show v_{C1}, v_{C2}, v_{C3}, and v_{C4} waveforms controlling v_{dc} at 400 V. For both *POD* and *IPD PWM* schemes, the estimated *PDV* is well regulated at reference value of 400 V. As shown in Figs. 4.21(b) and 4.22(b), the DC-link voltage is a high-frequency pulsed waveform with peak value of 400 V. It is pulsating between 0 – 400 V with *POD* and between 200 – 400 V for *IPD*. The network inductor currents i_{L1} and i_{L2} are also shown in Figs. 4.21(b) and 4.22(b). The source current which is coinciding with the inductor current i_{L1} shows less ripple in *IPD* when comparing with the *POD PWM* scheme.

Figs. 4.21(c) and 4.22(c) show line-line voltage v_{tab}, pole voltage v_{tao}, phase voltage v_{tan}, and *CMV*, respectively. As depicted in Fig. 4.21(c) for the *POD* scheme, v_{tab}, v_{tao}, v_{tan} contains five, three, and seven voltage levels, respectively. Whereas, these voltages contain five, three, and nine voltage levels, respectively in case of *IPD* and is shown in Fig. 4.22(c). The *CMV*, as shown in Figs. 4.21(c) and 4.22(c), for the *POD* and *IPD* is $V^*_{dc}/6$ and $V^*_{dc}/3$, respectively.

The Figs. 4.21(d) and 4.22(d) suggest that the i_a is well synchronized with the v_g. However, the harmonic content in the inverter current is more for *POD* as compared to *IPD*.

4.7.2 With grid-side dynamics

The experimental performance of the presented system for the sudden application of linear and non-linear loads for *POD* scheme are depicted in Figs. 4.23(a) and 4.23(b), respectively through grid phase voltage v_{ga}, inverter current i_a, grid current i_{ga}, and load current i_{La}. The power supply is programmed to give 3 kW to the system at a fixed input voltage of 192.1 V.

Before the application of loads, total power from the source is fed into the grid. The performance with sudden application of a linear load of 4 kW, 3 kVAr is shown in Fig. 4.23(a). Under this condition, the real power of 3 kW is supplied by the source, while the remaining real power and 3 kVAr of reactive power is supplied by the grid. Fig. 4.23(b) shows the waveforms when the 3-Φ diode bridge rectifier feeding a resistive load of 1 kW is applied to the system.

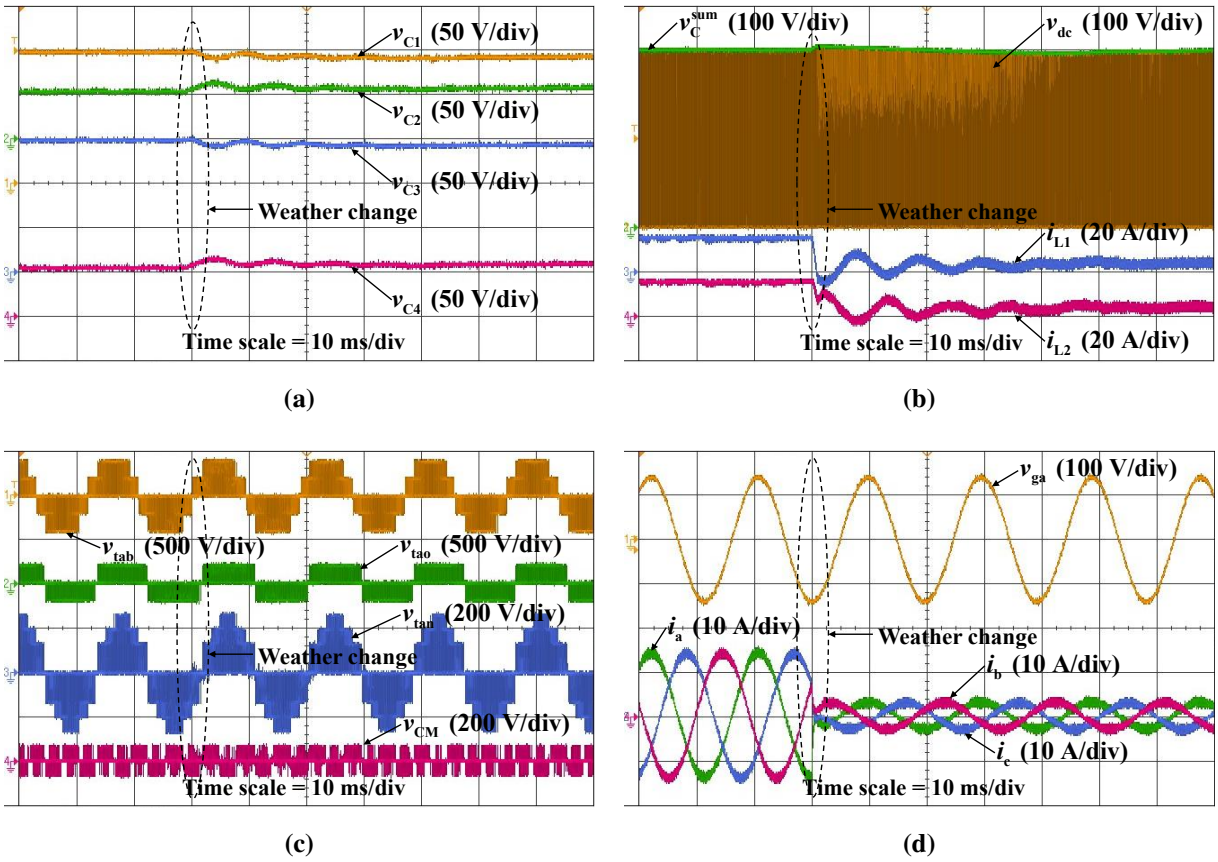


Fig. 4.21: Experimental results of *POD* scheme for input transient. **(a)** v_{C1}, v_{C2}, v_{C3}, and v_{C4}. **(b)** v_{dc}, v_C^{sum}, i_{L1}, and i_{L2}. **(c)** v_{tab}, v_{tao}, v_{tan}, and v_{CM}. **(d)** v_{ga} and i_{abc}.

Under this condition, i_{La} is highly distorted and i_a is purely sinusoidal. The load demand of 1 kW is met by the source and remaining 2 kW generated power is injected into the grid.

The experimental results are conforming with MATLAB and *RTS* results as obtained earlier. The experiment validates that the presented grid-tied *PV* with *3L NPC-QZS* inverter could operate for the input voltage varying in a wide range while maintaining high-quality inverter current. The designed controller also exhibits good reference tracking and disturbance rejection capability for both the transients initiated through the input-side or load-side.

4.8 COMPARISON OF *QZS* AND *NPC-QZS* INVERTERS

The performance of 3-Φ grid-tied *PV* system was analyzed employing *QZS* and *NPC-QZS* inverters in Chapter-3 and Chapter-4, respectively. The detailed guidelines for the design of these inverters are included in Appendix-A and Appendix-B.

A comparison is performed between *QZS* and *NPC-QZS* inverters for passive and active elements for the same input voltage, voltage and current ripples, and power rating. Correspondingly, for the input voltage of 100 V, P_{PV} = 3 kW, the factors $r_{i1}\%$ = $r_{i2}\%$ = $r_i\%$ = 20%, $r_{v1}\%$ = $r_{v2}\%$ = $r_v\%$ = 1%, grid voltage 100 Vrms, and switching frequency 10 kHz, the resulted parameters are summarized in Table 4.5.

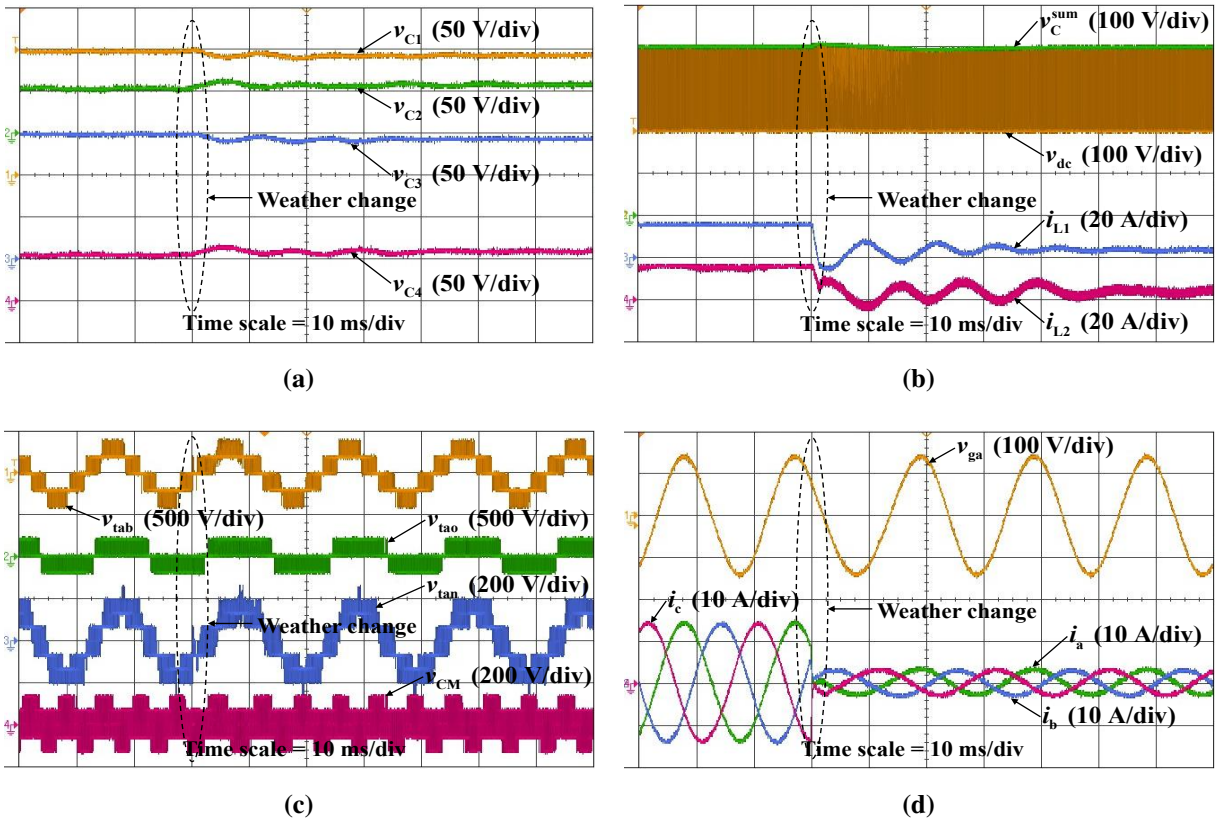


Fig. 4.22: Experimental results of *IPD* scheme for input transient. **(a)** v_{C1}, v_{C2}, v_{C3}, and v_{C4}. **(b)** v_{dc}, v_C^{sum}, i_{L1}, and i_{L2}. **(c)** v_{tab}, v_{tao}, v_{tan}, and v_{CM}. **(d)** v_{ga} and i_{abc}.

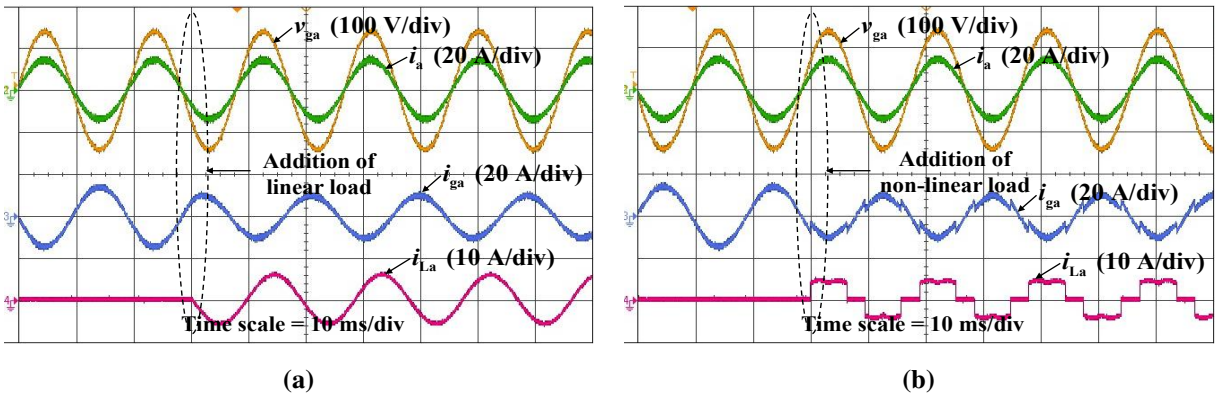


Fig. 4.23: Experimental results under application of load. **(a)** Linear load (v_{ga}, i_a, i_{ga}, and i_{La}). **(b)** Non-linear load (v_{ga}, i_a, i_{ga}, and i_{La}).

Table 4.5. Comparison of *QZS* and *NPC-QZS* inverter configurations, where χ = A, B, C

	QZS inverter	***NPC-QZS* inverter**
	Values of inductances and capacitances	
Inductance values	$L_1 = L_2 = 1.52$ mH	$L_1 = L_2 = L_3 = L_4 = 759\ \mu$H
Capacitance values	$C_1 = 455\ \mu$F $C_2 = 769\ \mu$F	$C_1 = C_3 = 911\ \mu$F $C_2 = C_4 = 1.54\ \mu$F
	Number of passive and active components	
No. of *QZS* network	1	2
No. of Inductors	2	4
No. of Capacitors	2	4
No. of Diodes	1	8
Power switches	6	12
No. of levels (Pole voltage)	2	3
Neutral point voltage balance	—	Through external circuit
Blocking voltage of switches	$V_{S_1 \ldots S_6} = V^*_{DC}$ $V_{D_1} = V^*_{DC}$	$V_{S_{\chi 1-\chi 2}} = V_{S_{\chi' 1-\chi' 2}} = V^*_{DC}/2$ $V_{D_\chi} = V_{D_{\chi'}} = V_{D_{1-2}} = V^*_{DC}/2$

In comparison, the *NPC* scheme requires four inductors of value about one-half of the inductance required in *QZS* scheme. Thus, the value of inductance for both the topologies will be equal. It is expected to reduce the loss significantly. The major advantage of *NPC-QZS* configuration is the number of output voltage levels, which will reduce the filtering requirement remarkably.

The voltage blocking of switches for *QZS* inverter is V^*_{DC}; and for *NPC-QZS* inverter is $V^*_{DC}/2$. Where, value of V^*_{DC} is taken same for both the inverter topologies. Stresses acting on the *NPC-QZS IGBTs* and diodes are therefore reduced, thus increasing the long-term reliability and the overall efficiency.

4.9 CHAPTER SUMMARY

The single-stage strategy to control AC-side current and *PDV* has been investigated for 3L *NPC-QZS* inverter-based grid-connected *PV* system. Mathematical model of the system is presented for both DC- and AC-sides and the controllers are designed utilizing the respective transfer functions. Damped-*SOGI* and *IDL* are used as controllers for AC- and DC-sides,

respectively. These controllers are modified by adding a pole to reduce the respective gains at high frequencies and to offer filtering action on the harmonic content of the sensed signal. To minimize the effect of *RHPZ* of DC-side transfer function, the gain crossover frequency of the *PDV* control loop is selected to be less than the folding frequency introduced by it. The *PWM* schemes are modified to yield *ST* using the 3rd harmonic injected *MCBC* on the basis of the *POD* and *IPD* methods. The performance of the *IDL*-damped-*SOGI* controller is compared with the *SMC*-damped-*SOGI* controller. The performance of the system is evaluated for change in *WCs* and loading. The system performance is validated through *RTS* and experimentation on a practical setup in the laboratory. The following conclusions are drawn from the study:

- Pulsating nature of *PDV* is accounted for by its indirect estimation and controlling through the voltage across *QZS* network capacitors.
- The *IDL*-damped-*SOGI* arrangement is found to be effective and resulting in *ZSSE* during steady state and lower transients during the change in *WCs*.
- With the considerations of lower *CMV* and zero average neutral point current, the *POD* scheme is found to be better.

Chapter–5

QZS-SC Inverter Based Three-phase Grid-tied PV System

5.1 GENERAL

In comparison to two-level counterpart, the *MLI* circuit topologies provide high power conversion efficiency, reduced filtering requirement, lower switching losses, fewer harmonics in the output voltage, decreased dv/dt, low-voltage stress on the switching devices, and good electromagnetic capability [177]. Fundamental *MLI* topologies are based on *NPC*, *FC*, and *CHB*. The performance of three-level *NPC-QZS* 3-Φ grid-tied *PV* system has been investigated in Chapter-4. The voltage gain for the above *MLI* topologies is limited to unity.

Switched Capacitor (*SC*) based *MLI* topologies have been investigated in the recent years [178–183] which are categorized as: single-stage and two-stage. In two-stage structures [178–180], an *SC* DC-DC converter is cascaded to an H-bridge. The *SC* DC-DC converter at the front-end provides a multilevel unipolar output voltage to the H-bridge inverter, which is greater than the input voltage. However, owing to increased voltage stress across the H-bridge, the single-stage *SC MLI* was proposed to give bipolar output voltage without using an H-bridge inverter, but the voltage gain was limited to two [181–183].

Despite the various literature on *SC* topologies, practical application has not been possible due to many critical issues. During start-up, an additional charging circuit is required to pre-charge the *SCs*. While in steady-state, *SCs* are charged through main source and are cause large current spikes [184]. To limit current spike, soft charging was realized using inductors [185]. The second stage of the *SC* cascaded *MLI* is the H-bridge inverter, in which switches

The contents of this chapter are partly published in:

∗ "A novel transformerless single-stage 3-phase grid-tied quasi-Z-source switched capacitors based multilevel inverter," (*Communicated in IEEE Transactions on Power Electronics*).

of the same leg should not be gated-ON simultaneously even by accident to avoid permanent damage to devices [24].

The motivation of this chapter is to realize a single-stage transformerless 3-Φ grid-tied *QZS-SC* inverter topology, as shown in Fig. 5.1, to generate *Five-Levels (5Ls)* in the line-to-line voltage with a single DC source while retaining the voltage boosting ability. The *SC* part is based on the structure discussed in [186]. The hybridization of *SC* with *QZS* is integrated to reduce the size of inductors in the *QZS* network. The proposed topology can have the advantages such as: (i) address the current spikes problem and improves reliability; (ii) the size of inductors in the *QZS* network is reduced; and (iii) using a *QZS* network provides additional control freedom in terms of *ST* state. Furthermore, a damped-*SOGI* controller is utilized to control both active and reactive power components of inverter current being injected into the grid. The theoretical design and simulation of proposed scheme is validated through *HIL RTS* results.

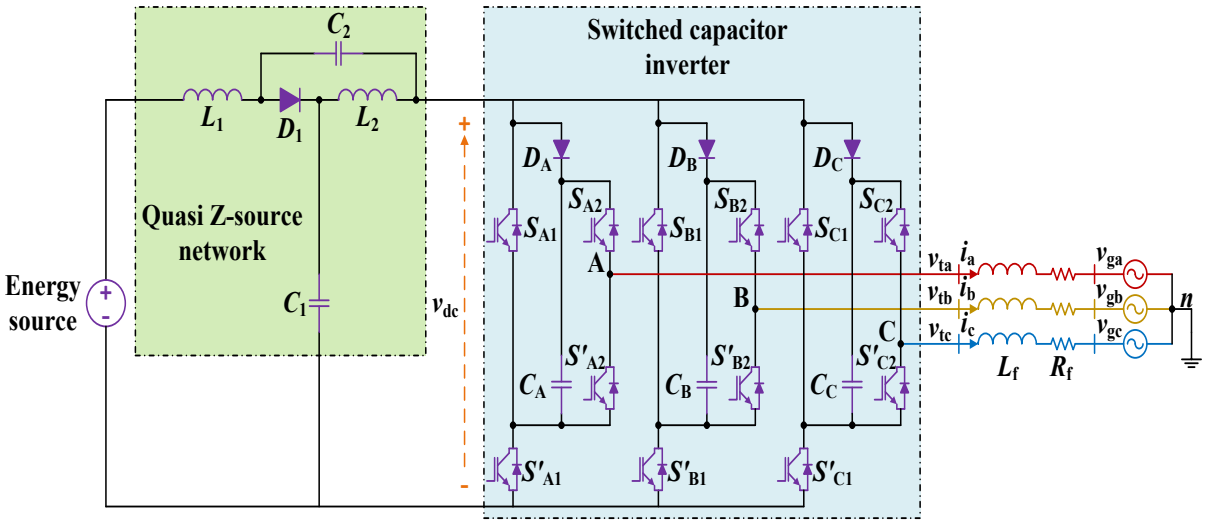


Fig. 5.1: 3-Φ *5L* grid-tied *QZS-SC* inverter topology.

5.2 OPERATING PRINCIPLE OF *QZS-SC* INVERTER

The schematic of the proposed *QZS-SC* inverter for 3-Φ grid-tied *PV* system is shown in Fig. 5.1. The structure consists of a *QZS* network (two inductors L_1, L_2, two capacitors C_1, C_2 and one diode D_1) cascaded with *SC* topology (one capacitor C_χ, one diode D_χ, and two sets of complementary switches ($S_{\chi 1}$, $S'_{\chi 1}$) and ($S_{\chi 2}$, $S'_{\chi 2}$) in a leg), where $\{\chi = \mathrm{A}, \mathrm{B}, \mathrm{C}\}$. The operation of *QZS-SC* inverter, which comprises mainly two components namely *QZS* network and *SC*

inverter, is detailed in the following subsections. The modeling of the *QZS* network, which has been discussed in the Section 3.2, is briefed herewith for easy reference.

5.2.1 *QZS* network operation

AC-side of the *QZS-SC* inverter is represented by current source i_{dc} in parallel with active switch S [102]. The small-signal modeling and analysis begin with the following assumptions: (i) inverter operate in *CCM*; (ii) $L_1 = L_2 = L$ and $C_1 = C_2 = C$; (iii) *QZS* network L and C have parasitic components R_L and R_C, respectively; and (iv) Switches are assumed to be ideal.

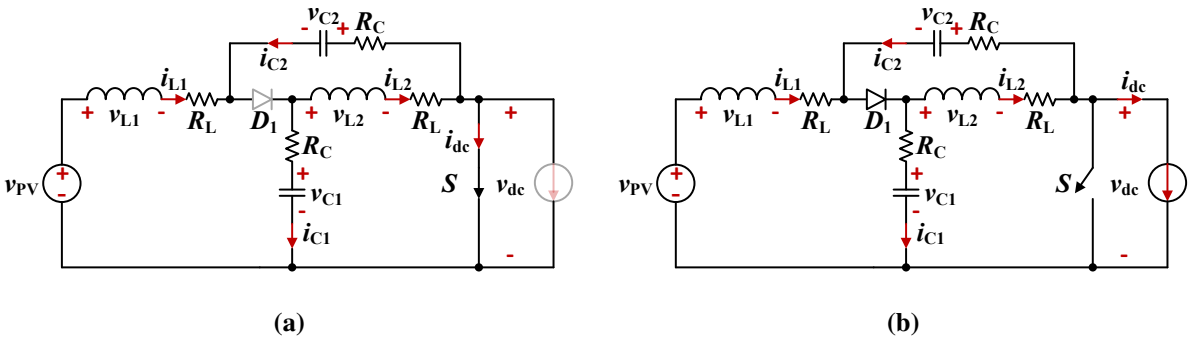


Fig. 5.2: Equivalent circuits of the *QZS* network. **(a)** *ST* state. **(b)** *NST* state.

When the inductor current is continuous, there are two operational states, as shown in Fig. 5.2. The *ST* state represented in Fig. 5.2(a) suggests S-ON, D_1-OFF; while *NST* state illustrated in Fig. 5.2(b) indicates S-OFF, D_1-ON. Accordingly, the average model will be:

$$\dot{\boldsymbol{x}} = \boldsymbol{A}\boldsymbol{x} + \boldsymbol{B}\boldsymbol{u} \tag{5.1}$$

where $\boldsymbol{A} = d_{st}\boldsymbol{A_0} + d_{nst}\boldsymbol{A_1}$, $\boldsymbol{B} = d_{st}\boldsymbol{B_0} + d_{nst}\boldsymbol{B_1}$, and $d_{nst} = 1 - d_{st}$ and d_{st} is the duty ratio of switch S. The state vector $\boldsymbol{x}$ and input vector $\boldsymbol{u}$ are formed as $\boldsymbol{x} = [\, i_{L1}\ i_{L2}\ v_{C1}\ v_{C2}\,]^\intercal$ and $\boldsymbol{u} = [\, v_{PV}\ i_{dc}\,]^\intercal$, respectively. i_{L1} and i_{L2} are *QZS* network inductor currents; v_{C1} and v_{C2} are *QZS* network capacitor voltages; v_{PV} is *PV* output voltage; and i_{dc} is the DC-link current. Matrices $\boldsymbol{A_0}$, $\boldsymbol{A_1}$, $\boldsymbol{B_0}$, and $\boldsymbol{B_1}$ are defined as:

$$\boldsymbol{A_0} = \begin{bmatrix} -\frac{(R_L+R_C)}{L} & 0 & 0 & \frac{1}{L} \\ 0 & -\frac{(R_L+R_C)}{L} & \frac{1}{L} & 0 \\ 0 & -\frac{1}{C} & 0 & 0 \\ -\frac{1}{C} & 0 & 0 & 0 \end{bmatrix} \qquad \boldsymbol{B_0} = \begin{bmatrix} \frac{1}{L} & 0 \\ 0 & 0 \\ 0 & 0 \\ 0 & 0 \end{bmatrix}$$

$$\boldsymbol{A_1} = \begin{bmatrix} -\frac{(R_L+R_C)}{L} & 0 & -\frac{1}{L} & 0 \\ 0 & -\frac{(R_L+R_C)}{L} & 0 & -\frac{1}{L} \\ \frac{1}{C} & 0 & 0 & 0 \\ 0 & \frac{1}{C} & 0 & 0 \end{bmatrix} \qquad \boldsymbol{B_1} = \begin{bmatrix} \frac{1}{L} & \frac{R_C}{L} \\ 0 & \frac{R_C}{L} \\ 0 & -\frac{1}{C} \\ 0 & -\frac{1}{C} \end{bmatrix}$$

The steady-state values of the state vectors are obtained by equating $\dot{\boldsymbol{x}} = 0$. Thus, steady-state values are expressed as $\boldsymbol{X} = -\boldsymbol{A^{-1}BU}$. During *ST* state, DC-link voltage $v_{dc} = 0$ while it's value in *NST* state is given as:

$$v_{dc}^{pk} = v_{C1} + v_{C2} + R_C(i_{L1} + i_{L2} - 2i_{dc}) \tag{5.2}$$

Thus, the peak DC-link voltage is specified as:

$$V_{dc}^{pk} = \frac{V_{PV}}{(1-2D_{st})} - \frac{2}{(1-2D_{st})^2}(R_C D_{st} + R_L D_{nst}) \tag{5.3}$$

The boosted DC-link voltage, given in (5.3), can be further improved by cascaded *SC* configuration inverter topology, whose operating is discussed in the following subsection.

5.2.2 *SC* inverter leg operation

The operation of the *SC-5L* inverter is explained with the help of a single leg, as shown in Figs. 5.3 and 5.4, where Fig. 5.3 depicts *NST* states and Fig. 5.4 represents *ST* states. The pole voltage is expressed as $v_{t\psi o}$, where $\psi = a, b, c$. In the *NST* state, *QZS* network diode D_1 is in conduction mode, while in the *ST* state, it will not conduct.

1. **Mode 1 [see Fig. 5.3(a)]:** In this mode, the pole voltage, $v_{t\psi o}$, equal to zero. This is resulted when the switches $S'_{\chi 1}$ and $S'_{\chi 2}$ are turned on, while switches $S_{\chi 1}$ and $S_{\chi 2}$ are non-conducting. The charging of capacitor C_χ occurs through the diode D_χ and switch $S'_{\chi 1}$.

2. **Mode 2 [see Fig. 5.3(b)]:** When switches $S'_{\chi 1}$ and $S_{\chi 2}$ are turned on, the pole voltage, $v_{t\psi o}$, is equal to capacitor voltage, i.e., v_{dc}, in this mode. The switches $S_{\chi 1}$ and $S'_{\chi 2}$ are non-conducting. The capacitor is simultaneously charging through path D_χ and $S'_{\chi 1}$.

3. **Mode 3 [see Fig. 5.3(c)]:** In this mode, switches $S_{\chi 1}$ and $S_{\chi 2}$ are conducting, thus the DC-link voltage v_{dc} and capacitor voltage $v_{\mathrm{SC}\chi}$ gets in series, therefore the pole voltage $v_{\mathrm{t}\psi\mathrm{o}}$ achieves the value $2v_{\mathrm{dc}}$. At the same time, diode D_{χ}, $S'_{\chi 1}$, and $S'_{\chi 2}$ are non-conducting.

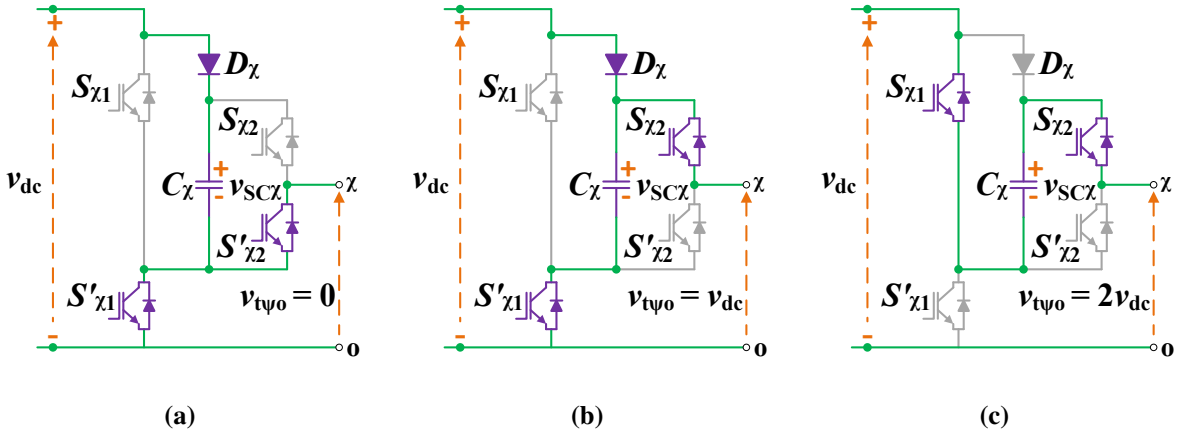


Fig. 5.3: Operating modes in the *NST* state. **(a)** Mode 1. **(b)** Mode 2. **(c)** Mode 3.

4. **Mode 4 [see Fig. 5.4(a)]:** In this mode, pole voltage $v_{\mathrm{t}\psi\mathrm{o}}$ is zero when switches $S'_{\chi 1}$ and $S'_{\chi 2}$ are conducting and *ST* state is achieved via $S_{\chi 1}$ and $S'_{\chi 1}$. At the same time, diode D_{χ} and $S_{\chi 2}$ are non-conducting.

5. **Mode 5 [see Fig. 5.4(b)]:** Simultaneous conduction of switches $S_{\chi 1}$, $S'_{\chi 1}$, and $S_{\chi 2}$ provides *ST* state and pole voltage, $v_{\mathrm{t}\psi\mathrm{o}}$, equal to v_{dc}. In this mode, diode D_{χ} and $S'_{\chi 2}$ are non-conducting.

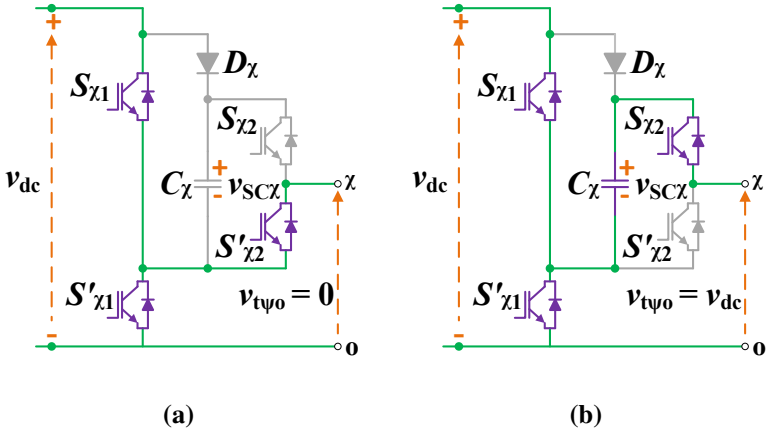


Fig. 5.4: Operating modes in the *ST* state. **(a)** Mode 4. **(b)** Mode 5.

The Table 5.1 summarizes switching states of the power semiconductor devices in a switching cycle.

Table 5.1. Switch status and inverter pole voltage $v_{t\psi o}$

State	Mode	Switch status						
		D_1	$S_{\chi 1}$	$S_{\chi 2}$	$S'_{\chi 1}$	$S'_{\chi 2}$	D_χ	$v_{t\psi o}$
NST states	**1**	On	Off	Off	On	On	On	$\mathbf{0}$
	2	On	Off	On	On	Off	On	v_{dc}
	3	On	On	On	Off	Off	Off	$2v_{dc}$
ST states	**4**	Off	On	Off	On	On	Off	$\mathbf{0}$
	5	Off	On	On	On	Off	Off	v_{dc}

(χ = A, B, C and ψ = a, b, c)

5.3 *PWM* SIGNAL GENERATION

The *PWM* gating signals are generated using multi-carrier modulation, as shown in Fig. 5.5 while utilizing *ST* signals. A multi-carrier level-shifted *PWM* method is used to drive the proposed topology in *NST* states. Two level-shifted triangular waves are used as a carrier. Carrier signal above zero reference is labeled as C_{r1} and below zero reference is labeled as C_{r2}. A comparison is made between the modulating and carrier signals. If $m_\psi \geq C_{r1}$, $S_{\chi 1}$ is turned on and it's complementary is given to $S'_{\chi 1}$. If $m_\psi \geq C_{r2}$, the gate signal is fed to $S_{\chi 2}$; otherwise, $S'_{\chi 2}$ is turned on.

To insert *ST* states, a triangular carrier C_{ST} having frequency same as level-shifted triangular carriers and two straight lines $V_p = (1 - d_{st})$ and $V_n = -(1 - d_{st})$ are used. When $C_{ST} \geq V_p$ or $C_{ST} \leq V_n$, then *ST* signals are generated. These *ST* signals are ORed with the signals for switches $S_{\chi 1}$ and $S'_{\chi 1}$.

5.4 CONTROL STRATEGY

The control structure of the presented grid-tied *QZS-SC* inverter is shown in Fig. 5.6. The system parameters are given in Table 5.2. The control strategy is explained through inverter current control and DC-link voltage control. The AC-side subsystem has faster dynamics than DC-side dynamics and thus the crossover frequency of the AC-side is selected higher [99]. The

damped-*SOGI* is used to track sinusoidal quantities, whereas the *PID* controller is used for DC-link voltage regulation.

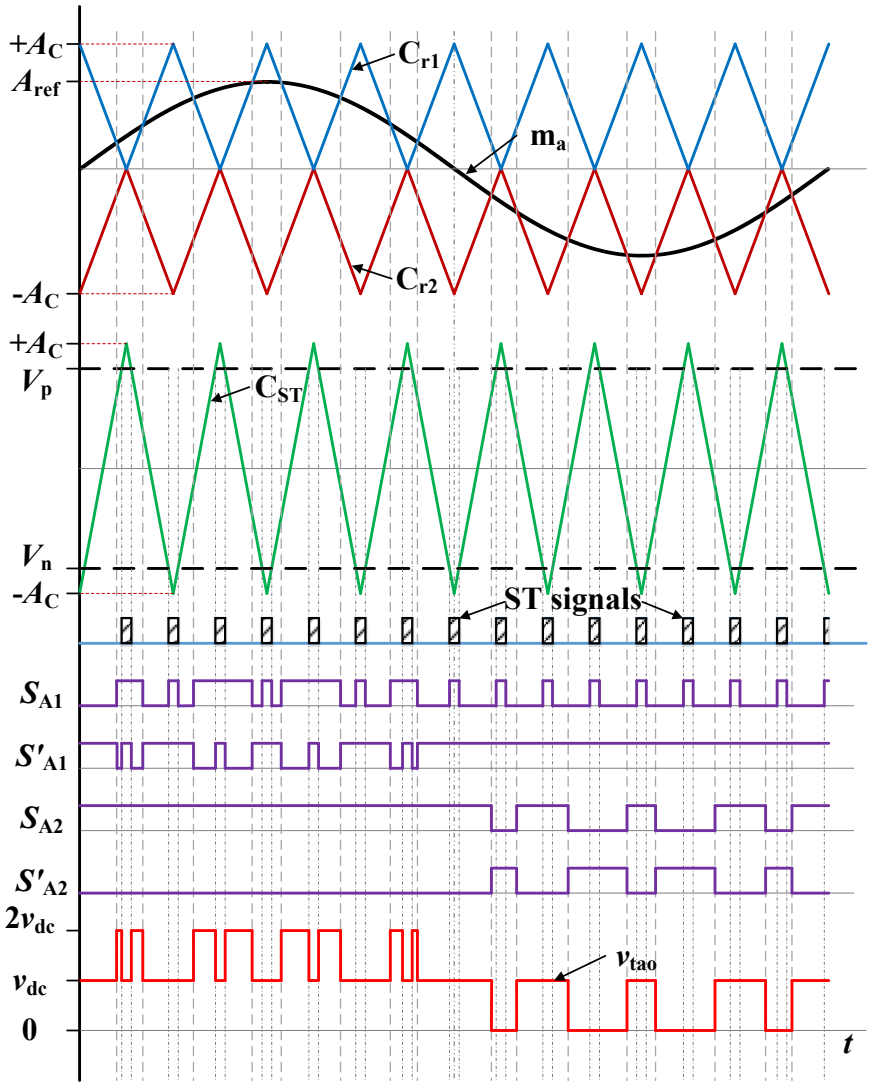


Fig. 5.5: Proposed *PWM* technique for *QZS-SC* inverter.

5.4.1 Design of damped-*SOGI* controller for AC-side

The dynamics of the system at the inverter-grid junction is described as:

$$v_{\text{tabc}} = L_{\text{f}} \frac{\text{d}i_{\text{abc}}}{\text{d}t} + R_{\text{f}} i_{\text{abc}} + v_{\text{gabc}} \tag{5.4}$$

where v_{tabc} output voltage vector of *QZS-SC* inverter, i_{abc} is the inverter current, v_{gabc} is the grid voltage, L_{f} is the filter inductance, and R_{f} is the winding resistance of the filter. Considering modulation index M, the peak terminal voltage of the inverter is given as:

$$V_{\mathrm{M}} = \frac{1}{2} M \left(2V_{\mathrm{dc}}^{\mathrm{pk}}\right) = MV_{\mathrm{dc}}^{\mathrm{pk}} \tag{5.5}$$

To reduce the number of equation from 3 to 2, (5.4) is transformed in $\alpha\beta$-domain using Clarke transformation as:

$$v_{\mathrm{t}\alpha\beta} = L_{\mathrm{f}} \frac{\mathrm{d}i_{\alpha\beta}}{\mathrm{d}t} + R_{\mathrm{f}} i_{\alpha\beta} + v_{\mathrm{g}\alpha\beta} \tag{5.6}$$

The inverter current is controlled by adjusting the real power reference P_{s}^{*} at *MPP* $P_{\mathrm{PV}}^{\mathrm{mx}}$ and reactive power reference Q_{s}^{*} is set to zero for *UPF* operation. Thus, for the known $v_{\mathrm{g}\alpha\beta}$, P_{s}^{*} and Q_{s}^{*}, the current reference $i_{\alpha\beta}^{*}$ is acquired as [187]:

$$\begin{bmatrix} i_{\alpha}^{*} \\ i_{\beta}^{*} \end{bmatrix} = \frac{2}{3} \frac{1}{v_{\mathrm{g}\alpha}^{2} + v_{\mathrm{g}\beta}^{2}} \begin{bmatrix} v_{\mathrm{g}\alpha} & v_{\mathrm{g}\beta} \\ v_{\mathrm{g}\beta} & -v_{\mathrm{g}\alpha} \end{bmatrix} \begin{bmatrix} P_{\mathrm{s}}^{*} \\ Q_{\mathrm{s}}^{*} \end{bmatrix} \tag{5.7}$$

Table 5.2. Grid-tied *QZS-SC* inverter parameters, where $\chi = \mathrm{A}, \mathrm{B}, \mathrm{C}$

Parameter	**Value**
PV array voltage	93.06 V
Power rating	3 kW
Reference *PDV* (V_{dc}^{*})	200 V
QZS network inductances (L_1, L_2)	500 μH
Winding resistance of *QZS* network inductors (R_{L})	0.1 Ω
QZS network capacitances (C_1, C_2)	2500 μF
ESR of *QZS* network capacitors (R_{C})	0.01 Ω
Capacitance of switched capacitor (C_{χ})	3000 μF
AC-side filter inductance (L_{f})	5 mH
Winding resistance of filter inductor (R_{f})	0.1 Ω
Grid *RMS* voltage (phase-neutral)	100 V
Angular grid frequency (ω_{g})	2π(50 Hz)
Switching frequency (f_{s})	10 kHz

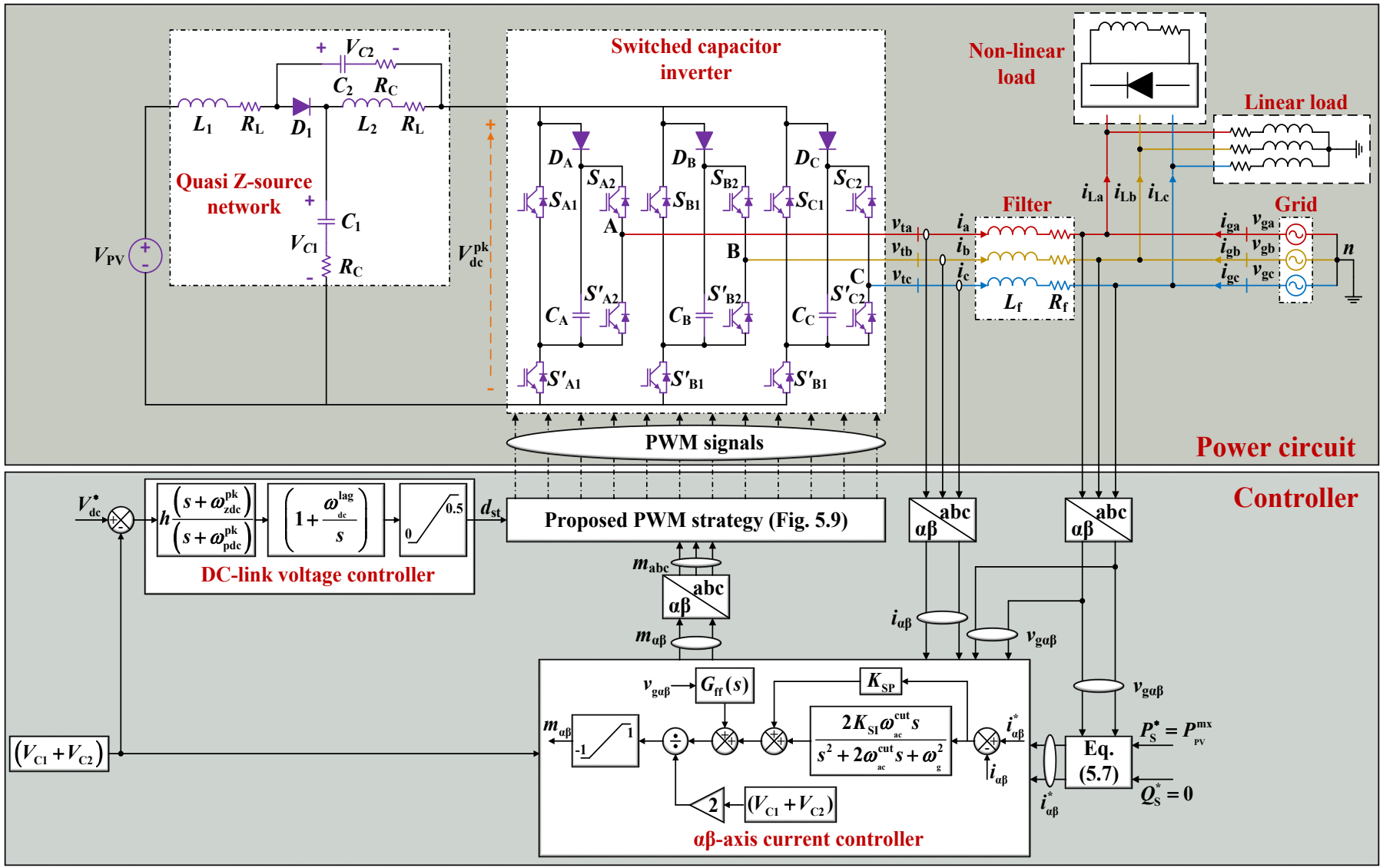


Fig. 5.6: System control strategy of 3-Φ *5L* grid-tied *QZS-SC* inverter.

The transfer function of the inverter current is defined as:

$$G_{\mathrm{ac}}(s) = \frac{1}{L_{\mathrm{f}}s + R_{\mathrm{f}}} \tag{5.8}$$

A damped-*SOGI* $K_{\mathrm{SOGI}}^{\mathrm{Damp}}(s)$ is employed to enforce the inverter current to track the desired reference [157]. The transfer function of the $K_{\mathrm{SOGI}}^{\mathrm{Damp}}(s)$ is given as:

$$K_{\mathrm{SOGI}}^{\mathrm{Damp}}(s) = K_{\mathrm{SP}} + \frac{2K_{\mathrm{SI}}\omega_{\mathrm{ac}}^{\mathrm{cut}}s}{s^2 + 2\omega_{\mathrm{ac}}^{\mathrm{cut}}s + \omega_{\mathrm{g}}^2} \tag{5.9}$$

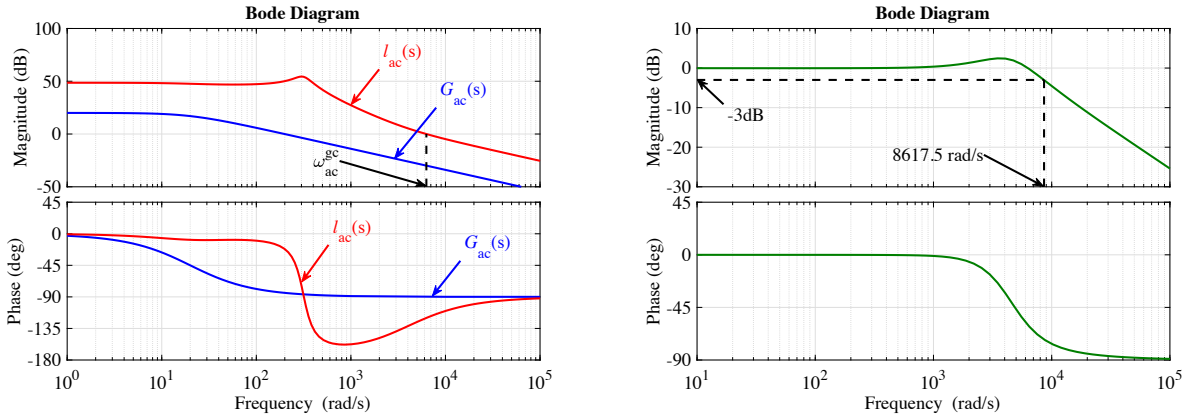
The K_{SP} and K_{SI} are the coefficients of damped-*SOGI* controller. The cut-off frequency $\omega_{\mathrm{ac}}^{\mathrm{cut}}$ is kept smaller than angular grid frequency ω_{g}, i.e., $\omega_{\mathrm{ac}}^{\mathrm{cut}} \ll \omega_{\mathrm{g}}$.

The loop gain of inverter current control $l_{\mathrm{ac}}(s)$ is provided as:

$$l_{\mathrm{ac}}(s) = G_{\mathrm{ac}}(s)K_{\mathrm{SOGI}}^{\mathrm{Damp}}(s) \tag{5.10}$$

The target crossover frequency $\omega_{\mathrm{ac}}^{\mathrm{gc}}$ of $2\pi(1\ \mathrm{kHz})$ is chosen corresponding to the $1/10^{\mathrm{th}}$ of the converter switching frequency and phase margin of 60°. Bode plots of the uncompensated and compensated loop gain are presented in Fig. 5.7(a). The Bode plot of $l_{\mathrm{ac}}(s)$ suggests phase margin of 60° at $\omega_{\mathrm{ac}}^{\mathrm{gc}}$ with $K_{\mathrm{SP}} = 26.84$, $K_{\mathrm{SI}} = 788.065$, and $\omega_{\mathrm{ac}}^{\mathrm{cut}} = 62.832$ rad/s. Fig. 5.7(b) shows −3 dB *BW* of 1371.5 rad/s for closed-loop current control.

The controller output is divided by two times of estimated DC-link voltage $2v_{\mathrm{C}}^{\mathrm{sum}} = 2(v_{\mathrm{C1}} + v_{\mathrm{C2}})$, to attain the modulating signal. A feed-forward controller $G_{\mathrm{ff}}(s) = 1/(5 \cdot 10^{-6}s + 1)$ is selected to avert the start-up transient and decouple the dynamics between inverter and the grid.



(a) **(b)**

Fig. 5.7: Bode plot of inverter current control. **(a)** Open-loop. **(b)** Closed-loop

5.4.2 Design of *PID* controller for DC-side

The DC-link voltage is controlled by regulating the *ST* duty ratio. Due to adoption of *ST* states, the DC-link voltage is a square waveform. The DC-link voltage is zero in *ST* state and its value is equal to sum of *QZS* network capacitors voltage during *NST* state. Therefore, the DC-link voltage is indirectly controlled using the sum of *QZS* network capacitors voltage. To attain the above objective, the *ST* duty ratio to DC-link voltage transfer function $G_{\mathrm{dc}}^{\mathrm{pk}}(s)$ is obtained as:

$$G_{\mathrm{dc}}^{\mathrm{pk}}(s) = \frac{\tilde{v}_{\mathrm{dc}}^{\mathrm{pk}}(s)}{\tilde{d}_{\mathrm{st}}(s)} = \frac{a_1 s + a_0}{LCs^2 + C\left(R_{\mathrm{L}} + R_{\mathrm{C}}\right)s + \left(D_{\mathrm{nst}} - D_{\mathrm{st}}\right)^2} \tag{5.11}$$

where

$$a_1 = 2CR_{\mathrm{C}}\left(V_{\mathrm{C1}} + V_{\mathrm{C2}} - R_{\mathrm{C}}I_{\mathrm{dc}}\right) + 2L\left(I_{\mathrm{dc}} - I_{\mathrm{L1}} - I_{\mathrm{L2}}\right)$$
$$a_0 = 2\left(D_{\mathrm{nst}} - D_{\mathrm{st}}\right)\left(V_{\mathrm{C1}} + V_{\mathrm{C2}} - R_{\mathrm{C}}I_{\mathrm{dc}}\right) + 2\left(R_{\mathrm{L}} + 2R_{\mathrm{C}}D_{\mathrm{st}}\right)\left(I_{\mathrm{dc}} - I_{\mathrm{L1}} - I_{\mathrm{L2}}\right)$$

The loop gain $l_{\mathrm{dc}}^{\mathrm{pk}}(s)$ for DC-link voltage control is given as:

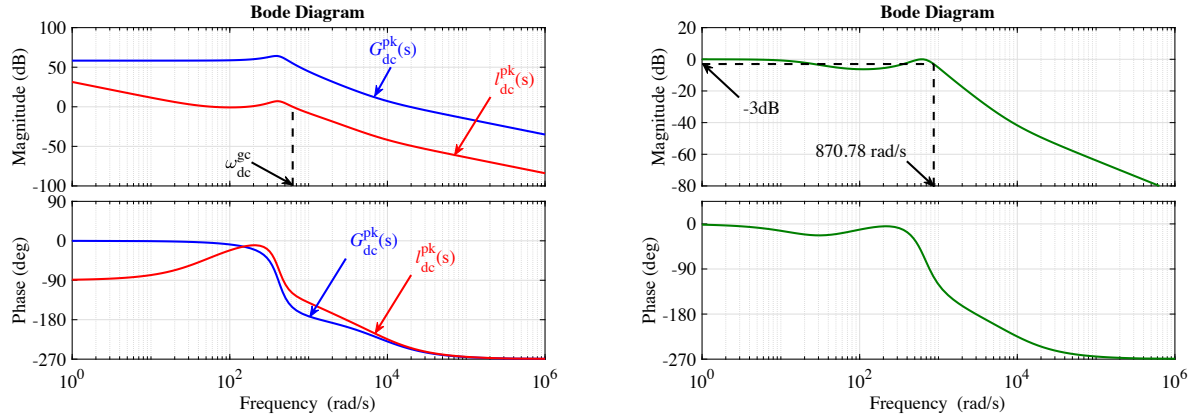
$$l_{\mathrm{dc}}^{\mathrm{pk}}(s) = G_{\mathrm{dc}}^{\mathrm{pk}}(s)K_{\mathrm{dc}}^{\mathrm{pk}}(s) \tag{5.12}$$

The Bode plot of the uncompensated loop gain is presented in Fig. 5.8(a) when unity gain compensator is used, $K_{\mathrm{dc}}^{\mathrm{pk}}(s) = 1$. The uncompensated loop gain has a *GM* −38.1 dB at phase-crossover frequency 3057.5 Hz and *PM* −66.38° at gain-crossover frequency 223.2 Hz. The negative values of *GM* and *PM* suggests an unstable system. A *PID* controller is used, whose transfer function is given as follows:

$$K_{\mathrm{dc}}^{\mathrm{pk}}(s) = h\frac{\left(s + \omega_{\mathrm{zdc}}^{\mathrm{pk}}\right)}{\left(s + \omega_{\mathrm{pdc}}^{\mathrm{pk}}\right)}\left(1 + \frac{\omega_{\mathrm{dc}}^{\mathrm{lag}}}{s}\right) \tag{5.13}$$

where h is the coefficient and $\omega_{\mathrm{zdc}}^{\mathrm{pk}}$, $\omega_{\mathrm{pdc}}^{\mathrm{pk}}$, and $\omega_{\mathrm{dc}}^{\mathrm{lag}}$ are the tuning parameters of the *PID* controller.

To avoid interaction between AC- and DC-side subsystems, the crossover frequency of the DC-side is selected less than the AC-side. Thus, the resulting loop gain has a *GM* 24.68 dB at phase-crossover frequency 474.98 Hz and *PM* 60° at gain-crossover frequency 100 Hz as depicted in Fig. 5.8(a). The positive values of *GM* and *PM* suggests a stable system. Also, the Fig. 5.8(b) shows −3 dB *BW* of 870.78 rad/s for closed-loop DC-link voltage control.



(a) **(b)**

Fig. 5.8: Bode plot of DC-link voltage control. **(a)** Open-loop. **(b)** Closed-loop

5.5 INVERTER DESIGN PROCEDURE

5.5.1 Passive components values for *QZS* network

The inductors and capacitors of the *QZS* network are chosen to limit *HF* ripple from the DC components. In an ideal case, equations in *ST* state for *QZS* network capacitor voltage and inductor current are given as:

$$\begin{cases} L_1 \dfrac{\Delta i_{L1}}{D_{st} T_s} = V_{PV} + V_{C2} \\ L_2 \dfrac{\Delta i_{L2}}{D_{st} T_s} = V_{C1} \\ C_1 \dfrac{\Delta v_{C1}}{D_{st} T_s} = I_{L2} \\ C_2 \dfrac{\Delta v_{C2}}{D_{st} T_s} = I_{L1} \end{cases} \tag{5.14}$$

where T_s is the switching interval. For *MCBC*, *ST* duty ratio D_{st} and modulation index M are related as [20]:

$$D_{st} = 1 - \frac{\sqrt{3}}{2} M \tag{5.15}$$

If the *HF* ripples ΔI_{L1}, ΔI_{L2}, ΔV_{C1}, and ΔV_{C2} are chosen (so that $\Delta I_{L1} \leq r_{i1}\% I_{L1}$, $\Delta I_{L2} \leq r_{i2}\% I_{L2}$, $\Delta V_{C1} \leq r_{v1}\% V_{C1}$, and $\Delta V_{C2} \leq r_{v2}\% V_{C2}$, respectively), and using (5.3), (5.5), (5.14), and (5.15), the inductances and capacitances of *QZS* network are calculated as:

$$\begin{cases} L_1 \geq \dfrac{\sqrt{3}}{4}\left(\dfrac{T_s V_M V_{PV}}{r_{i1}\%P_{PV}}\right)\left(\dfrac{\sqrt{3}V_M - 2V_{PV}}{\sqrt{3}V_M - V_{PV}}\right) \\ L_2 \geq \dfrac{\sqrt{3}}{4}\left(\dfrac{T_s V_M V_{PV}}{r_{i2}\%P_{PV}}\right)\left(\dfrac{\sqrt{3}V_M - 2V_{PV}}{\sqrt{3}V_M - V_{PV}}\right) \\ C_1 \geq \dfrac{2}{\sqrt{3}}\left(\dfrac{T_s P_{PV}}{r_{v1}\%V_M V_{PV}}\right)\left(\dfrac{\sqrt{3}V_M - 2V_{PV}}{\sqrt{3}V_M - V_{PV}}\right) \\ C_2 \geq \left(\dfrac{T_s P_{PV}}{r_{v2}\%V_{PV}}\right)\left(\dfrac{1}{\sqrt{3}V_M - V_{PV}}\right) \end{cases} \tag{5.16}$$

5.5.2 Switched capacitors values

The ideal *SC* is expected to retain a constant voltage. In actual circuit, the capacitor C_χ is determined based on the allowance of voltage ripple [188]. When C_χ is in parallel with source, the capacitor charges while in series connection, it discharges, as shown in Figs. 5.3 and 5.4. The *SC* is discharged when the pole voltage $v_{t\psi o}$ is equal to $2v_{dc}$.

As depicted in Fig. 5.5, v_{dc} and $2v_{dc}$ are alternately generated in the positive half cycle of the $v_{t\psi o}$. Thus, the average duty cycle D is given as [189]:

$$D = M \sin\left(\omega_g t\right) \tag{5.17}$$

where $M = A_{ref}/A_C$. The A_{ref} is the amplitude of control signal and A_C is the amplitude of the carrier signal. The average current flowing through C_χ during positive half cycle of $v_{t\psi o}$ is:

$$i = DI_M \sin\left(\omega_g t + \phi\right) \tag{5.18}$$

where I_M is the peak value of inverter current and ϕ is the power factor angle. Thus, the charge variation in C_χ is given as:

$$\Delta Q_{SC\chi} = \int_0^\pi DI_M \sin\left(\omega_g t + \phi\right) \tag{5.19}$$

For the ripple voltage of $\Delta V_{SC\chi}$, the C_χ is calculated as:

$$C_\chi \geq \frac{1}{\Delta V_{SC\chi}} \int_0^\pi MI_M \sin\left(\omega_g t\right) \sin\left(\omega_g t + \phi\right) dt \tag{5.20}$$

5.5.3 Semiconductor device ratings

From Figs. 5.2, 5.3, and 5.4, the voltage stress on the switches equals the DC-link voltage v_{dc}. Thus, we have:

$$V_{\mathrm{D1}} = V_{\mathrm{S}\chi_{1-2}} = V_{\mathrm{S}'\chi_{1-2}} = V_{\mathrm{D}\chi} = V_{\mathrm{dc}}^{\mathrm{pk}} \tag{5.21}$$

Peak current stress of the diode D_1 is twice the inductor current, i.e., $2I_{\mathrm{L}}$. While the peak current through $S_{\chi 1}$ and $S_{\chi 1}^{'}$ is given as [10]:

$$I_{\mathrm{S}\chi_1} = I_{\mathrm{S}'\chi_1} = \max\left[\frac{1}{3}\frac{P_{\mathrm{PV}}}{\cos\phi M V_{\mathrm{dc}}^{\mathrm{pk}}} + \frac{2}{3}\frac{P_{\mathrm{PV}}}{V_{\mathrm{PV}}}, \frac{2}{3}\frac{P_{\mathrm{PV}}}{\cos\phi M V_{\mathrm{dc}}^{\mathrm{pk}}}\right] \tag{5.22}$$

Peak current through switches $S_{\chi 2}$ and $S_{\chi 2}^{'}$ is equal to the maximum load current, i.e., I_{M}. While, peak current through D_χ is the sum of *SC* current and load current, as depicted in Fig. 5.3(b), as:

$$I_{\mathrm{D}\chi} = I_{\mathrm{M}} + \frac{V_{\mathrm{dc}}^{\mathrm{pk}} - V_{\mathrm{SC}\chi} - V_{\mathrm{D}\chi}}{R_{\mathrm{D}} + R_{\mathrm{SC}\chi} + R_{\mathrm{ON}}} \tag{5.23}$$

where $V_{\mathrm{SC}\chi}$ is the voltage across *SC*, $V_{\mathrm{D}\chi}$ is the forward voltage drop of the D_χ, $R_{\mathrm{SC}\chi}$ is the *ESR* of *SC*, and R_{D} and R_{ON} are the on-state resistance of D_χ and $S_{\chi 2}^{'}$, respectively.

5.6 SIMULATION RESULTS

The proposed grid-tied *QZS-SC* inverter topology and its control methodology has been realized in MATLAB/Simulink for the design parameter listed in Table 5.2. The Fig. 5.9 shows the implementation of the *PWM* technique using 3$^{\mathrm{rd}}$ harmonic injected modulating signal. The inverter current control provides $m_{\alpha\beta}$ and modulating signal m_{abc} is generated using inverse Clarke transform. The 3$^{\mathrm{rd}}$ harmonic injected control signal is then obtained in terms of $m_{\alpha\beta}$ and m_{abc} as [159]:

$$m_{\mathrm{abc}}^{*} = \frac{3}{2}m_{\mathrm{abc}} - \frac{2}{3}\frac{m_{\mathrm{abc}}^{3}}{m_{\alpha}^{2} + m_{\beta}^{2}} \tag{5.24}$$

The performance of the grid-tied *QZS-SC* inverter is evaluated for the following criteria: atmospheric conditions variation and reactive power compensation of the load connected at the grid. This section has been further divided for a clear overview as: (i) input-side transient and (ii) grid-side transient.

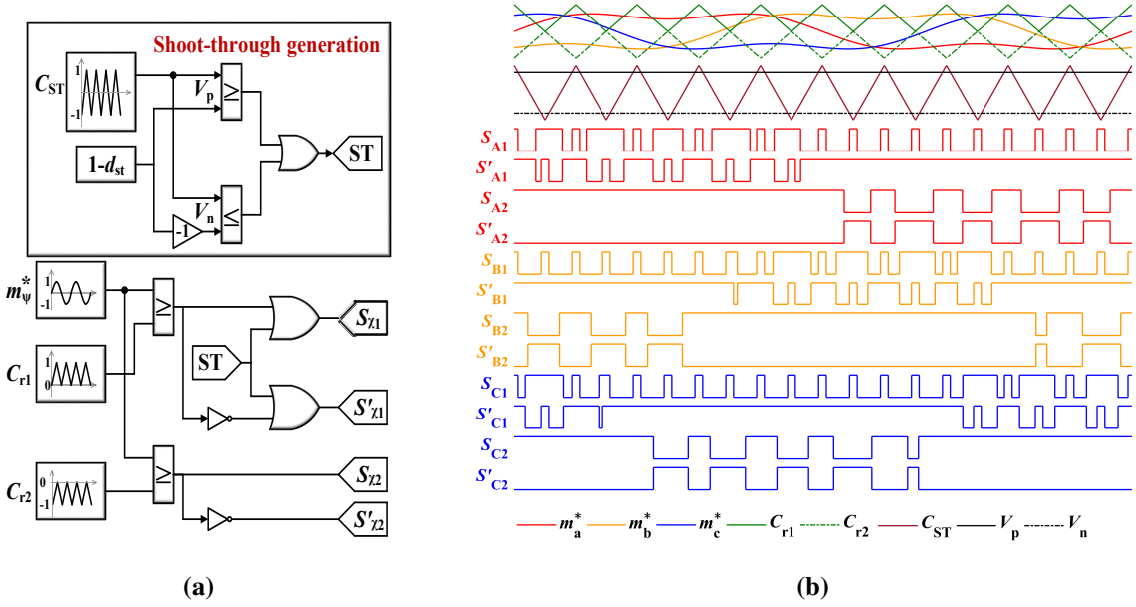


Fig. 5.9: *PWM* implementation. **(a)** Schematic diagram. **(b)** MATLAB waveforms.

5.6.1 With input-side dynamics

The energy source is realized through four parallel connection of five series-connected Havells *PV* modules, whose technical specification is given in Table 5.3. Maximum power $P_{\text{PV}}^{\text{mx}}$ and voltage $V_{\text{PV}}^{\text{mx}}$ at specific *WC* from Fig. 5.10 are outlined here as:

WC1 : 1000 W/m^2 and 25 °C, $V_{\text{PV}}^{\text{mx}} = 93.05$ V, $P_{\text{PV}}^{\text{mx}} = 3000$ W.

WC2 : 300 W/m^2 and 75 °C, $V_{\text{PV}}^{\text{mx}} = 85.19$ V, $P_{\text{PV}}^{\text{mx}} = 791.96$ W.

Initially, the system is working under *WC*1, where the *ST* duty ratio is 0.2816, as shown in Fig. 5.11(a). Correspondingly, the voltage across *QZS* network capacitors C_1 and C_2, as depicted in Fig. 5.11(a), are 146.5 V and 53.47 V, respectively. The DC-link voltage v_{dc} is regulated at V_{dc}^*, which is equal to sum of v_{C1} and v_{C2}, as presented in Fig. 5.11(b) and the voltage across *SC* v_{SCA} is given as V_{dc}^*. Fig. 5.11(c) suggests that the real power of 3 kW is supplied to the grid at *UPF* and the *RMS* value of inverter current is found to be 9.983 A. Fig. 5.11(d) illustrates the pole voltage v_{tao}, phase voltage v_{tan}, and line voltage v_{tab}. The v_{tao} has three levels 0, V_{dc}^*, and $2V_{\text{dc}}^*$; the v_{tan} has nine levels 0, $\pm V_{\text{dc}}^*/3$, $\pm 2V_{\text{dc}}^*/3$, $\pm V_{\text{dc}}^*$, and $\pm 4V_{\text{dc}}^*/3$; and the v_{tab} has five levels as 0, $\pm V_{\text{dc}}^*$, and $\pm 2V_{\text{dc}}^*$.

At $t = 0.5$ s, the system is suddenly subjected from *WC*1 to *WC*2. As the input voltage is decreased, the d_{st} is changed to 0.2985 for the needed boost. Accordingly, the v_{C1} and v_{C2}

is changed to 142.6 V and 57.39 V, respectively. The v_{dc} is persistently maintained at V^*_{dc} after small transient shown in Fig. 5.11(b), presenting the efficacy of control strategy. The steady-state inductor current i_{L1} and i_{L2} fall from 35.36 A to 9.647 A due to step variation from *WC*1 to *WC*2. The real power of 791.96 W is supplied to the grid at *UPF* and the *RMS* value of i_a is decreased to 2.623 A. Due to single stage control strategy, d_{st} and m_{abc} are interdependent. Thus, a transient is detected in m_{abc}. Small duration transients are observed in v_{SCA}, v_{tao}, v_{tan}, and v_{tab}. Fig. 5.12 presents *Fast Fourier Transform (FFT)* of the inverter current i_a and the *THD* is found to be 2.07 %, which is within IEEE-519 standards [168].

Table 5.3. Adjusted model of Havells *PV* module specification

Parameter	Values
Electrical properties	
Maximum power	150 W
MPP voltage	18.61 V
MPP current	8.06 A
Open circuit voltage	22.19 V
Short circuit current	8.62 A
Number of cells in series	$4 * 9$
Series resistance	0.0688 Ω
Parallel resistance	155.563 Ω
Temperature coefficients	
Nominal power/temperature coefficient	−0.40 %/°C
Open circuit voltage/temperature coefficient	−0.30 %/°C
Short circuit current/temperature coefficient	0.05 %/°C

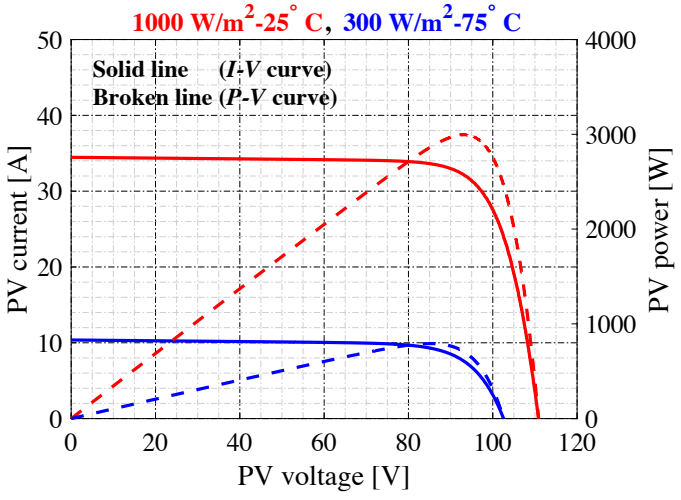


Fig. 5.10: *I–V* and *P–V* characteristics for different *WCs* (ENVIRO PVM6/PVC-150).

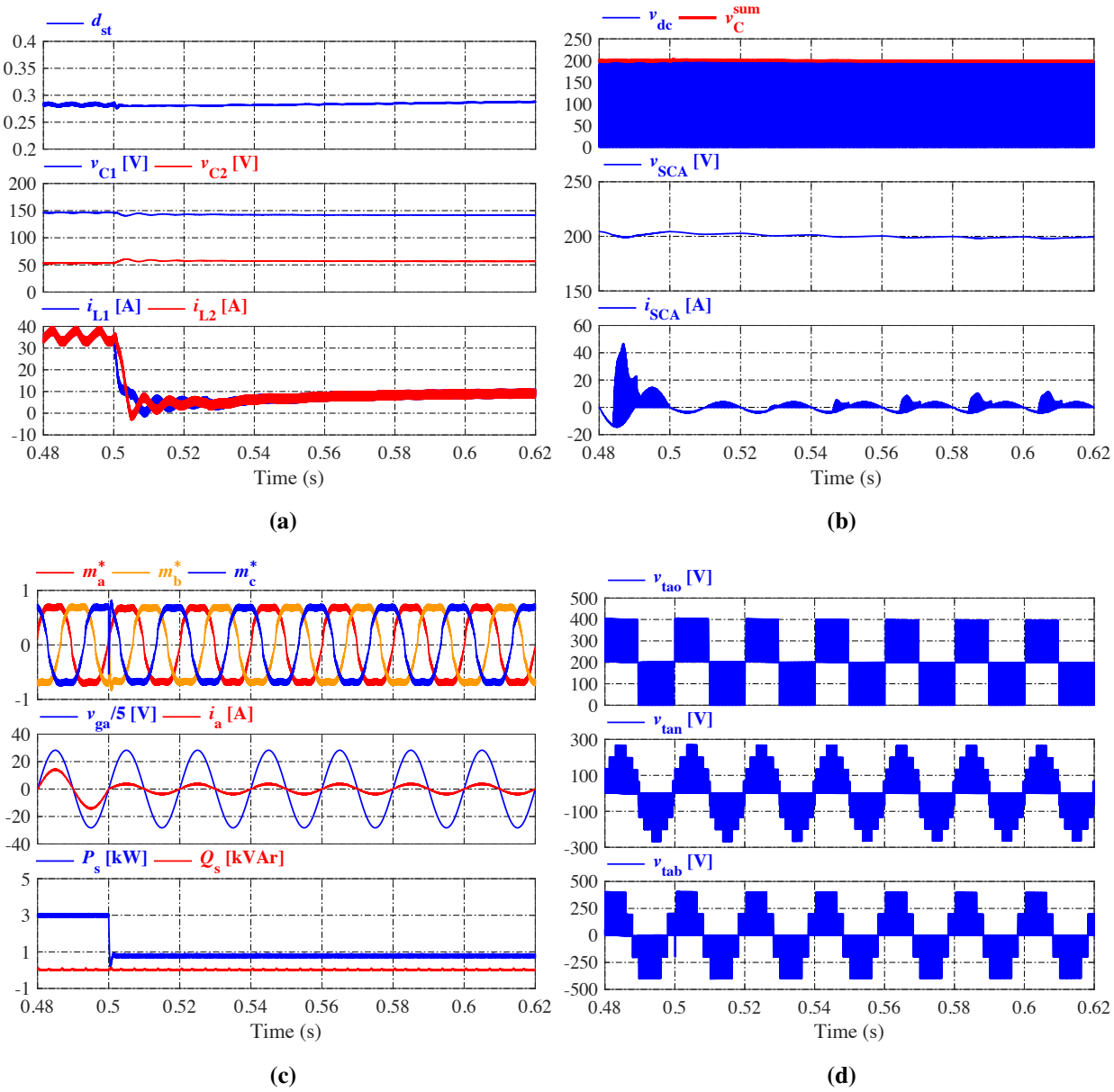


Fig. 5.11: Weather condition changes from *WC*1 to *WC*2. **(a)** d_{st}, v_{C1}, v_{C2}, i_{L1}, and i_{L2}. **(b)** v_{dc}, v_C^{sum}, v_{SCA}, and i_{SCA}. **(c)** m^*_{abc}, v_{ga}, i_a, P_s, and Q_s. **(d)** v_{tao}, v_{tan}, and v_{tab}.

5.6.2 With grid-side dynamics

The Fig. 5.13 presents the reactive power compensation for the local loads depicted in Fig. 5.6. The system is directed to change the operation from *UPF* to reactive power compensator at grid side by compensating the reactive power of the load by *QZS-SC* inverter. During this time, inverter will partially act as *Static Synchronous Compensator (STATCOM)*. Traditional reactive power compensation technique has been used in this chapter to show the effectiveness of the control strategy [190].

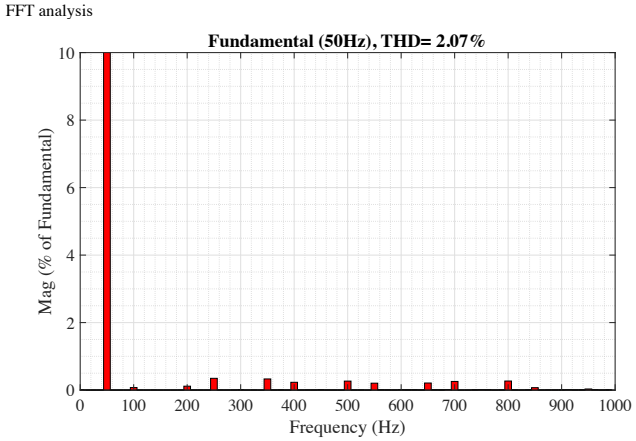


Fig. 5.12: *FFT* of i_a.

Initially, the system is working under *WC*1 at *UPF*, with a linear load of 1 kW and 500 VAr. Consequently, all the reactive power required by the load is supplied by the grid and the inverter current i_a is in-phase with the voltage. At $t = 1$ s, the inverter is directed to operate as traditional *STATCOM*. Therefore, the grid is operating at *UPF* and load reactive power requirement is fulfilled by the inverter. The *QZS-SC* inverter along with the *PV* power of 3 kW has compensated the reactive power demand of 500 VAr.

Now, $3-\Phi$ diode bridge rectifier is connected to the system at $t = 1.5$ s while the linear load is still connected to the system. It can be observed from Fig. 5.13(b) that the grid is still working on *UPF* while inverter is meeting the reactive power demand of load.

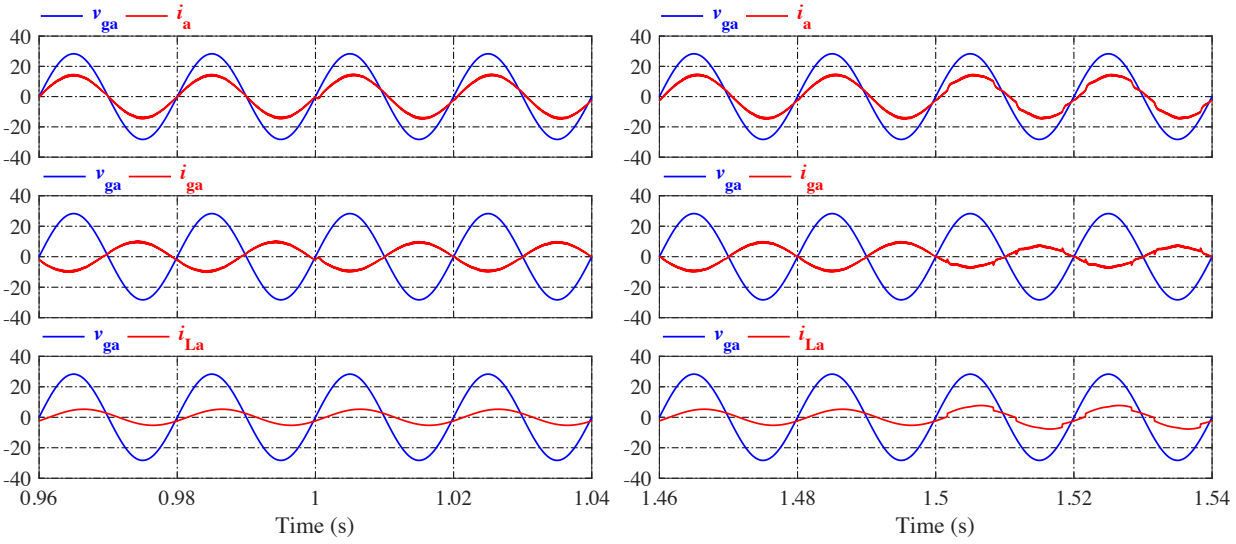


Fig. 5.13: Reactive power compensation by *QZS-SC* inverter. **(a)** Linear load (v_{ga}, i_a, i_{ga}, and i_{La}). **(b)** Non-linear load (v_{ga}, i_a, i_{ga}, and i_{La}).

5.7 REAL-TIME VALIDATION USING OPAL-RT

The system under investigation, as shown in Fig. 5.6 is validated using *HIL RTS* which is a crucial and reliable arrangement to validate complex real-time embedded systems before final hardware implementation [169]. The OPAL-RT, a *RTS* platform has been used for validation in the lab and the same is shown in Fig. 5.14. The controllers and plant are embedded in separate OPAL-RTs (OP4510) module. The *PID* controller for *PDV* regulation and damped-*SOGI* controller for inverter current control are embedded in Module-1, while the plant describing *PV* system, *QZS* network, *SC* inverter, and grid, is embedded in Module-2. The gating signals for the inverter bridge are fed from Module-1 to Module-2 and system measurements are fed back from Module-2 to Module-1 in real-time manner. These two modules are connected through the hardware inputs and outputs whereas the communicating signals are monitored through four-channel *DSOs* (KEYSIGHT make, model: DSOX2024A). The *RTS* was performed under two conditions as in the simulation: input-side dynamics and grid-side dynamics.

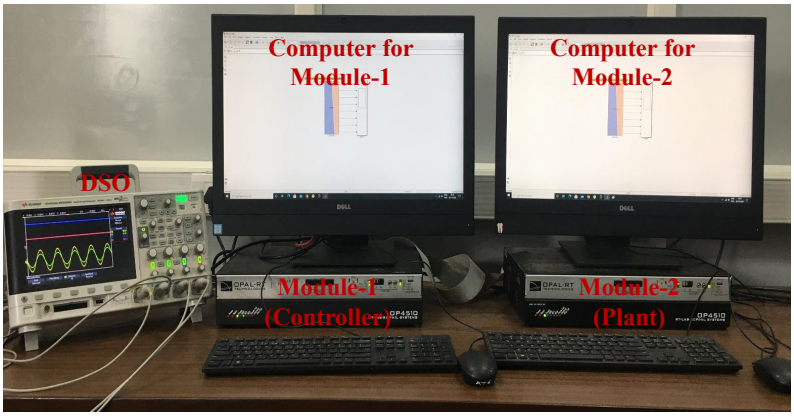
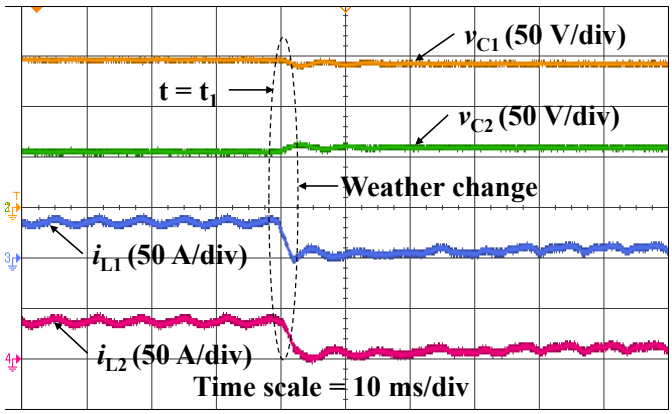


Fig. 5.14: The experimental setup for *HIL RTS* in the OPAL-RT platform.

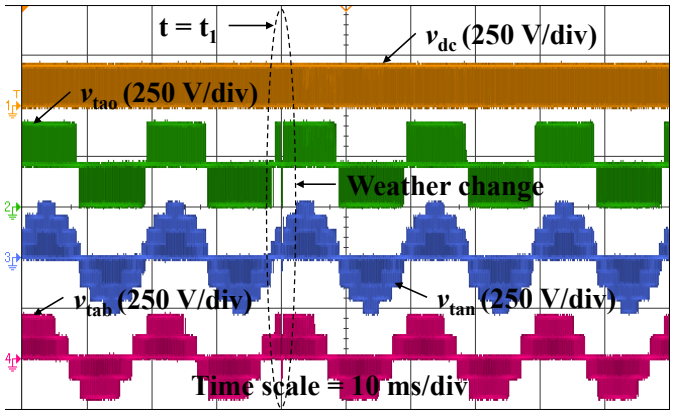
5.7.1 Performance under input-side dynamics

The Fig. 5.15 shows observed waveform with transient initiated from the input side. A step change is applied at $t = t_1$ by changing the operation form $WC1$ to $WC2$, which is followed by the fall in i_{L1} and i_{L2}, as shown in Fig. 5.15(a). At the instant t_1, transients are observed in the waveform of v_{C1} and v_{C2}. The v_{dc} is pulsating between 0 and 200 V and well regulated at the reference value showing the dynamic performance and effectiveness of the control. The pole voltage v_{tao} is showing three levels 0, 200 V, and 400 V, the phase voltage v_{tan} have 0, $\pm 200/3$ V, $\pm 400/3$ V, ± 200 V, and $\pm 800/3$ V, and line voltage v_{tab} have five levels 0, ± 200 V,

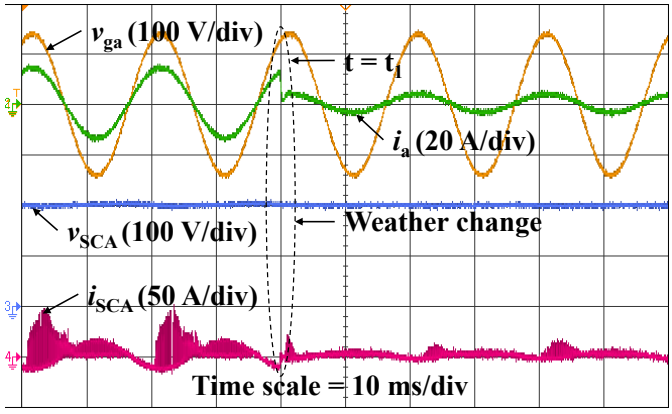
and ±400 V, as shown in Fig. 5.15(b). Fig. 5.15(c) suggest that the i_a is well synchronized with the v_{ga}. Voltage across the *SC* in the a-phase is fixed at a value of 200 V while current through *SC* depicts transients, as shown in Fig. 5.15(c).



(a)



(b)



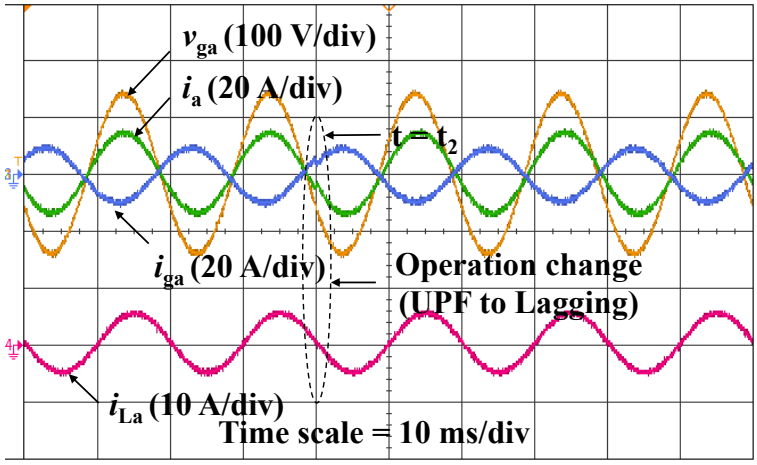
(c)

Fig. 5.15: *HIL RTS* results under input dynamics. **(a)** v_{C1}, v_{C2}, i_{L1}, and i_{L2}. **(b)** v_{dc}, v_{tao}, v_{tan}, and v_{tab}. **(c)** v_{ga}, i_a, v_{SCA}, and i_{SCA}.

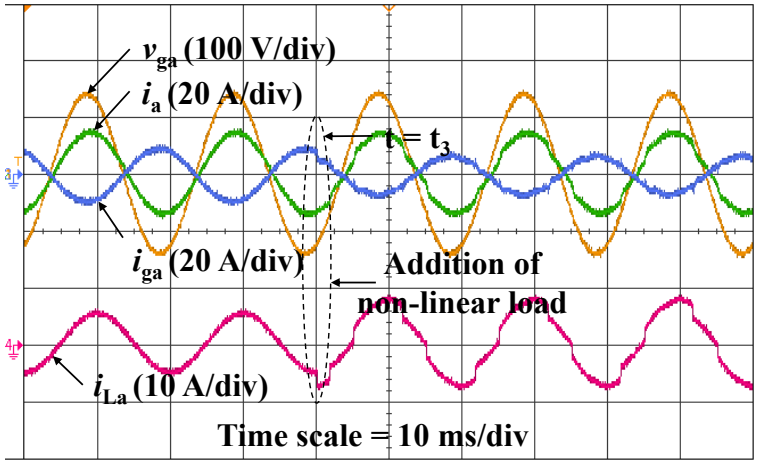
5.7.2 Performance under grid-side dynamics

The Fig. 5.16 demonstrates the reactive power compensation for the local loads presented in Fig. 5.6. Before time $t = t_2$, a linear load of 1 kW and 500 VAr is connected to the system and the Q_s^* is kept at zero. Therefore, all the reactive power is supplied by the grid and can be viewed as the i_{ga} is leading the v_{ga} and i_a is in-phase with v_{ga} verifying *UPF*, as shown in Fig. 5.16(a). At time instant $t = t_2$, system is commanded to work as reactive power compensator, consequently causing the i_{ga} in-phase with v_{ga} and i_a leads the v_{ga}.

At $t = t_3$, a 3-Φ bridge rectifier is connected to the system while linear load still connected to the system. From Fig. 5.16(b) it can be observed that the i_{ga} is still in phase with v_{ga} and reactive power is supplied by the *QZS-SC* inverter.



(a)



(b)

Fig. 5.16: *HIL RTS* results under grid dynamics (v_{ga}, i_a, i_{ga}, and i_{La}). **(a)** Linear load. **(b)** Non-linear load.

According to the *HIL RTS* findings, it can be concluded that they are in good agreement with the theoretical and simulation analysis; this consistency proves the legitimacy of the proposed inverter.

5.8 COMPARISON OF *QZS* INVERTER CONFIGURATIONS

The performance of 3-Φ grid-tied *PV* system was analyzed employing *QZS*, *NPC-QZS*, and *QZS-SC* inverters in Chapter-3, Chapter-4, and this Chapter-5, respectively. The detailed guidelines for the design of these inverters are included in Appendix-A, Appendix-B, and Section-5.5.

A comparison is performed between *QZS*, *NPC-QZS* and *QZS-SC* inverters for passive and active elements for the same input voltage, voltage and current ripples, and power rating. Correspondingly, for the input voltage of 100 V, P_{PV} = 3 kW, the factors $r_{\mathrm{i1}}\% = r_{\mathrm{i2}}\% = r_{\mathrm{i}}\% =$ 20%, $r_{\mathrm{v1}}\% = r_{\mathrm{v2}}\% = r_{\mathrm{v}}\% = 1\%$, grid voltage 100 Vrms, and switching frequency 10 kHz, the resulted parameters are summarized in Table 5.4. This table also has information of number of *QZS* network, operational aspect of external voltage balancing circuit.

As evident that two *QZS* networks are needed in *NPC-QZS* configuration whereas *QZS-SC* configuration utilizes only one *QZS* network. Thus, the number of inductors required in *SC* scheme is only two, at par with the two-level system. Further, the required inductance value in *SC* scheme is one-fifth of inductance needed in *QZS*. In comparison, the *NPC* scheme requires four inductors of value about 2.5 times the inductance required in *SC* scheme. The reduced number of inductors and that too of lower values are the biggest advantages of *3L SC* configuration. It is expected to reduce the loss significantly.

The *3L SC* configuration although requires five capacitors, but two capacitors pertains to *QZS* network and three capacitors pertains to three legs of 3-Φ configuration. The losses due to increase in capacitors and diodes, 4 in place of 2 is significantly low in comparison to reduction in losses in inductors and thus performance of *SC* shall be much better. Another major advantage of *SC* configuration is the inherent self voltage balancing, which otherwise require external circuit or special control scheme for *NPC* arrangement.

The voltage blocking of switches for *QZS* inverter is V^{*}_{DC}; for *NPC-QZS* inverter is $V^{*}_{\mathrm{DC}}/2$; and for *QZS-SC* inverter is $V^{*}_{\mathrm{DC}}/2$ except switch $S^{'}_{\chi 2}$. The reverse voltage across $S^{'}_{\chi 2}$ is V^{*}_{DC}. Where, value of V^{*}_{DC} is taken same for all the inverter topologies.

Table 5.4. Comparison of *QZS* inverter configurations, where χ = A, B, C

	***QZS* inverter**	***NPC-QZS* inverter**	***QZS-SC* inverter**
	Values of inductances and capacitances		
Inductances	$L_1 \geq \sqrt{3}\left(\frac{T_s V_M V_{PV}}{r_{i1}\%P_{PV}}\right)\left(\frac{\sqrt{3}V_M - V_{PV}}{2\sqrt{3}V_M - V_{PV}}\right)$ $L_2 \geq \sqrt{3}\left(\frac{T_s V_M V_{PV}}{r_{i2}\%P_{PV}}\right)\left(\frac{\sqrt{3}V_M - V_{PV}}{2\sqrt{3}V_M - V_{PV}}\right)$	$L_1 = L_3 \geq \frac{\sqrt{3}}{2}\left(\frac{T_s V_M V_{PV}}{r_{i1}\%P_{PV}}\right)\left(\frac{\sqrt{3}V_M - V_{PV}}{2\sqrt{3}V_M - V_{PV}}\right)$ $L_2 = L_4 \geq \frac{\sqrt{3}}{2}\left(\frac{T_s V_M V_{PV}}{r_{i2}\%P_{PV}}\right)\left(\frac{\sqrt{3}V_M - V_{PV}}{2\sqrt{3}V_M - V_{PV}}\right)$	$L_1 \geq \frac{\sqrt{3}}{4}\left(\frac{T_s V_M V_{PV}}{r_{i1}\%P_{PV}}\right)\left(\frac{\sqrt{3}V_M - 2V_{PV}}{\sqrt{3}V_M - V_{PV}}\right)$ $L_2 \geq \frac{\sqrt{3}}{4}\left(\frac{T_s V_M V_{PV}}{r_{i2}\%P_{PV}}\right)\left(\frac{\sqrt{3}V_M - 2V_{PV}}{\sqrt{3}V_M - V_{PV}}\right)$
Capacitance	$C_1 \geq \frac{1}{\sqrt{3}}\left(\frac{T_s P_{PV}}{r_{v1}\%V_M V_{PV}}\right)\left(\frac{\sqrt{3}V_M - V_{PV}}{2\sqrt{3}V_M - V_{PV}}\right)$ $C_2 \geq \left(\frac{T_s P_{PV}}{r_{v2}\%V_{PV}}\right)\left(\frac{1}{2\sqrt{3}V_M - V_{PV}}\right)$	$C_1 = C_3 \geq \frac{2}{\sqrt{3}}\left(\frac{T_s P_{PV}}{r_{v1}\%V_M V_{PV}}\right)\left(\frac{\sqrt{3}V_M - V_{PV}}{2\sqrt{3}V_M - V_{PV}}\right)$ $C_2 = C_4 \geq 2\left(\frac{T_s P_{PV}}{r_{v2}\%V_{PV}}\right)\left(\frac{1}{2\sqrt{3}V_M - V_{PV}}\right)$	$C_1 \geq \frac{2}{\sqrt{3}}\left(\frac{T_s P_{PV}}{r_{v1}\%V_M V_{PV}}\right)\left(\frac{\sqrt{3}V_M - 2V_{PV}}{\sqrt{3}V_M - V_{PV}}\right)$ $C_2 \geq \left(\frac{T_s P_{PV}}{r_{v2}\%V_{PV}}\right)\left(\frac{1}{\sqrt{3}V_M - V_{PV}}\right)$
Inductance values	$L_1 = L_2 = 1.52$ mH	$L_1 = L_2 = L_3 = L_4 = 759\ \mu$H	$L_1 = L_2 = 316\ \mu$H
Capacitance values	$C_1 = 455\ \mu$F $C_2 = 769\ \mu$F	$C_1 = C_3 = 911\ \mu$F $C_2 = C_4 = 1.54\ \mu$F	$C_1 = 760\ \mu$F $C_2 = 2.07$ mF
	Number of passive and active components		
No. of *QZS* network	1	2	1
No. of Inductors	2	4	2
No. of Capacitors	2	4	5
No. of Diodes	1	8	4
Power switches	6	12	12
No. of levels (Pole voltage)	2	3	3
Neutral point voltage balance	—	Through external circuit	Self balancing
Blocking voltage of switches	$V_{S_1 \ldots S_6} = V^*_{DC}$ $V_{D_1} = V^*_{DC}$	$V_{S_{\chi 1-\chi 2}} = V_{S_{\chi' 1-\chi' 2}} = V^*_{DC}/2$ $V_{D_\chi} = V_{D_{\chi'}} = V_{D_{1-2}} = V^*_{DC}/2$	$V_{S_{\chi 1-\chi 2}} = V_{S'_{\chi 1}} = V^*_{DC}/2$ & $V_{S'_{\chi 2}} = V^*_{DC}$ $V_{D_\chi} = V_{D_1} = V^*_{DC}/2$

5.9 CHAPTER SUMMARY

A novel single-stage topology based on *QZS-SC* grid-tied inverter for *PV* system has been presented in this chapter. The *QZS* network is used in the front end between *PV* and *SC* inverter and the resulted boosted output is fed to *SC* inverter. A two-stage like control structure is used, where DC-link voltage is regulated to reference value using *ST* duty ratio and damped-*SOGI* controller is used to control the inverter current. A multi-carrier level-shifted *PWM* integrating with *ST* states was proposed to synthesize the *5L* line-to-line staircase voltage waveform. The design guidelines and voltage/current stresses of switches were also presented for the proposed topology. To check the performance and operation of the proposed system, the simulation and *HIL RTS* results are performed in laboratory. The following conclusions are drawn:

- The *QZS* network between the *PV* and the *SC* inverter provides additional boost stage and limits the start-up and charging currents.
- The *QZS* network also provides additional control freedom in terms of *ST* duty ratio to regulate the DC-link voltage.
- The *SC* inverter structure reduces the inductor size of the *QZS* network for the same operating conditions.
- The system continues to inject current into the grid at *UPF* even after applying linear/non-linear load on the grid-side.
- The controller is also effective when transients are initiated from input side. The DC-link voltage is persistently maintained at the reference value and *ZSSE* is achieved.

Chapter–6

Flying Squirrel Search Optimization Algorithm for MPPT under PSC

6.1 GENERAL

The key concerns associated with a *PV* system are low conversion efficiency, high system cost, and non-linearity in the output power. The increased utilization and the technological developments in *PV* manufacturing and in power conversion systems helped in lowering the cost of *PV* modules in the last few decades. Still, the installation cost is high and the conversion efficiency is low, which ranges between 10% to 15%. Therefore, it must be ensured that the maximum power is extracted from the *PV* system under different environmental conditions, caused by changes in the ambient temperature and solar insolation. The basic requirements of any *MPPT* algorithm are: a) faster response with respect to change in environmental conditions; b) better accuracy; c) higher efficiency; and d) stable operation at *MPP*. The process of *MPPT* gets further complicated due to non-linear *I–V* characteristics and largely varying *P–V* curve with variations in solar insolation and temperature.

Large-scale solar *PV* systems encounter unpredictable *PSCs*, causing multiple peaks in the *P–V* characteristics, potentially downgrading the performance of the *PV* system. However, the *PV* system should be operated at *GMPP* for its efficient utilization. For the tracking of *GMPP*, a scheme based on *Flying Squirrel Search Optimization* (*FSSO*) is presented in this chapter. For an effective adoption with much reduced convergence time, the original *FSSO* is modified to update the squirrel position without the presence of predator. An experimental investigation of the

The contents of this chapter are partly published in:

* "A flying squirrel search optimization for MPPT under partial shaded photovoltaic system," *IEEE Journal of Emerging and Selected Topics in Power Electronics*.
doi: 10.1109/JESTPE.2020.3024719.

proposed scheme is carried out employing a *QZS* converter for the extraction of maximum power under *PSC*. The proposed scheme yields higher tracking efficiency, non-oscillatory steady-state response, and lower transients. Simulation and experimental investigations under various shading patterns indicate that the proposed strategy outperforms other popular *MPPT* strategies based on *P&O*, *PSO*, and *GWO*.

6.2 MATHEMATICAL MODELING OF SYSTEM

The schematic arrangement of the *PV* system coupled with *QZS* converter is shown in Fig. 6.1. The proposed *MPPT* control is implemented with OPAL-RT as the real-time controller. The analysis presented in this section is carried out with the following assumptions for *QZS* converter:

1. The semiconductor devices are ideal.
2. Passive elements are linear.
3. Inductors are operating in *CCM*.
4. The *QZS* network inductances and capacitances are equal to L and C, respectively. The *ESR* of capacitors and winding resistance of inductors are R_C and R_L, respectively.

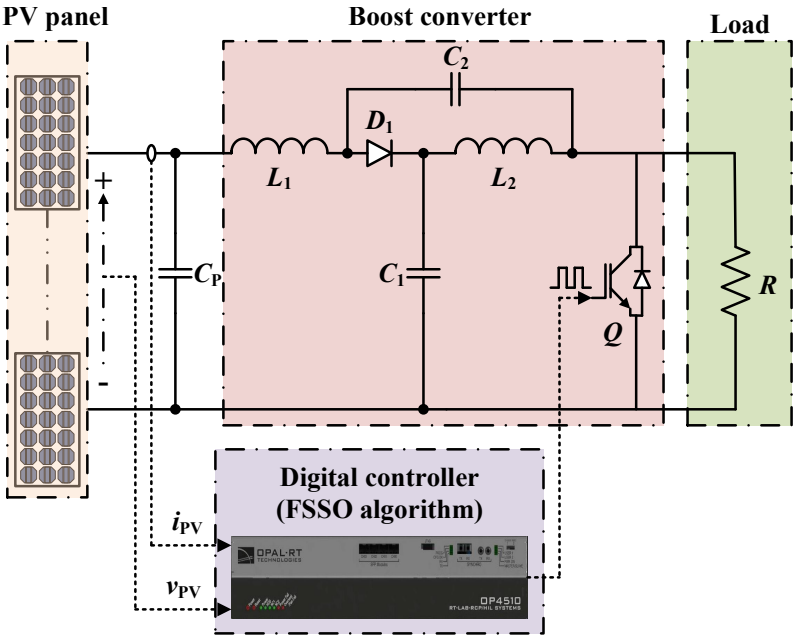


Fig. 6.1: Block diagram of the proposed solar *PV* test system.

6.2.1 *PV* module and array

The *PV* source, as shown in Fig. 6.2(a), is represented using the single diode model. It represents the precise output characteristics of various kinds of *PV* cells and modules [191]. This model comprises a current source I_{ph}, a diode, a shunt resistance R_{sh}, and a series resistance R_{se}. The gross module output current I_{PV} is given as:

$$I_{\mathrm{PV}} = I_{\mathrm{ph}} - I_{\mathrm{d}} - \frac{V_{\mathrm{PV}} + R_{\mathrm{se}} I_{\mathrm{PV}}}{R_{\mathrm{sh}}} \tag{6.1}$$

where I_{ph} is the current due to incidence of light at irradiation level G and I_{d} is the diode current, which are expressed as:

$$\begin{cases} I_{\mathrm{ph}} = \left[I_{\mathrm{phn}} + K_{\mathrm{I}} \left(T - T_{\mathrm{n}} \right) \right] \dfrac{G}{G_{\mathrm{n}}} \\ I_{\mathrm{d}} = I_{\mathrm{rs}} \left[\exp \left(\dfrac{V_{\mathrm{PV}} + R_{\mathrm{se}} I_{\mathrm{PV}}}{\xi V_{\mathrm{t}}} \right) - 1 \right] \end{cases} \tag{6.2}$$

The thermal voltage V_{t} at temperature T and diode reverse saturation current I_{rs} for N_{se} series-connected cells are:

$$\begin{cases} V_{\mathrm{t}} = N_{\mathrm{se}} k_{\mathrm{b}} T / q \\ I_{\mathrm{rs}} = \dfrac{I_{\mathrm{scn}} + K_{\mathrm{I}} (T - T_{\mathrm{n}})}{\exp \left(\frac{V_{\mathrm{ocn}} + K_{\mathrm{V}} (T - T_{\mathrm{n}})}{\xi V_{\mathrm{t}}} \right) - 1} \end{cases} \tag{6.3}$$

where V_{PV} be regarded as *PV* module output voltage; I_{phn} represents light generated current at the *Standard Test Condition (STC)*; k_{b}, q, and ξ are Boltzmann constant, electron charge, and diode ideality constant; T_{n}, G_{n}, I_{scn}, and V_{ocn} are temperature, irradiance, short-circuit current, and open-circuit voltage at *STC*; K_{I} and K_{V} are short-circuit current and open-circuit voltage temperature coefficients.

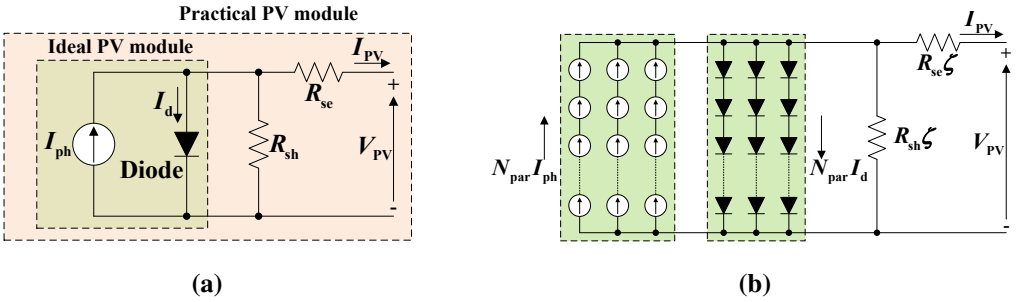


Fig. 6.2: Equivalent circuit of *PV*. **(a)** Single diode model of the *PV* module. **(b)** *PV* array composed of series and parallel combination of modules.

The *PV* modules are connected in series-parallel combinations, as represented in Figs. 6.3 and 6.4, to obtain higher voltage and current. With the equivalent as shown in Fig. 6.2(b), the output current from *PV* module I_{PV} must be updated as follows [192]:

$$I_{\mathrm{PV}} = I_{\mathrm{ph}} N_{\mathrm{par}} - I_{\mathrm{rs}} N_{\mathrm{par}} \left[\exp\left(\frac{V_{\mathrm{PV}} + R_{\mathrm{se}} I_{\mathrm{PV}} \zeta}{\xi V_{\mathrm{t}} N_{\mathrm{ser}}} \right) - 1 \right] - \frac{V_{\mathrm{PV}} + R_{\mathrm{se}} I_{\mathrm{PV}} \zeta}{R_{\mathrm{sh}} \zeta} \tag{6.4}$$

where $\zeta = N_{\mathrm{ser}}/N_{\mathrm{par}}$. N_{ser} and N_{par} are the number of series and parallel modules, respectively.

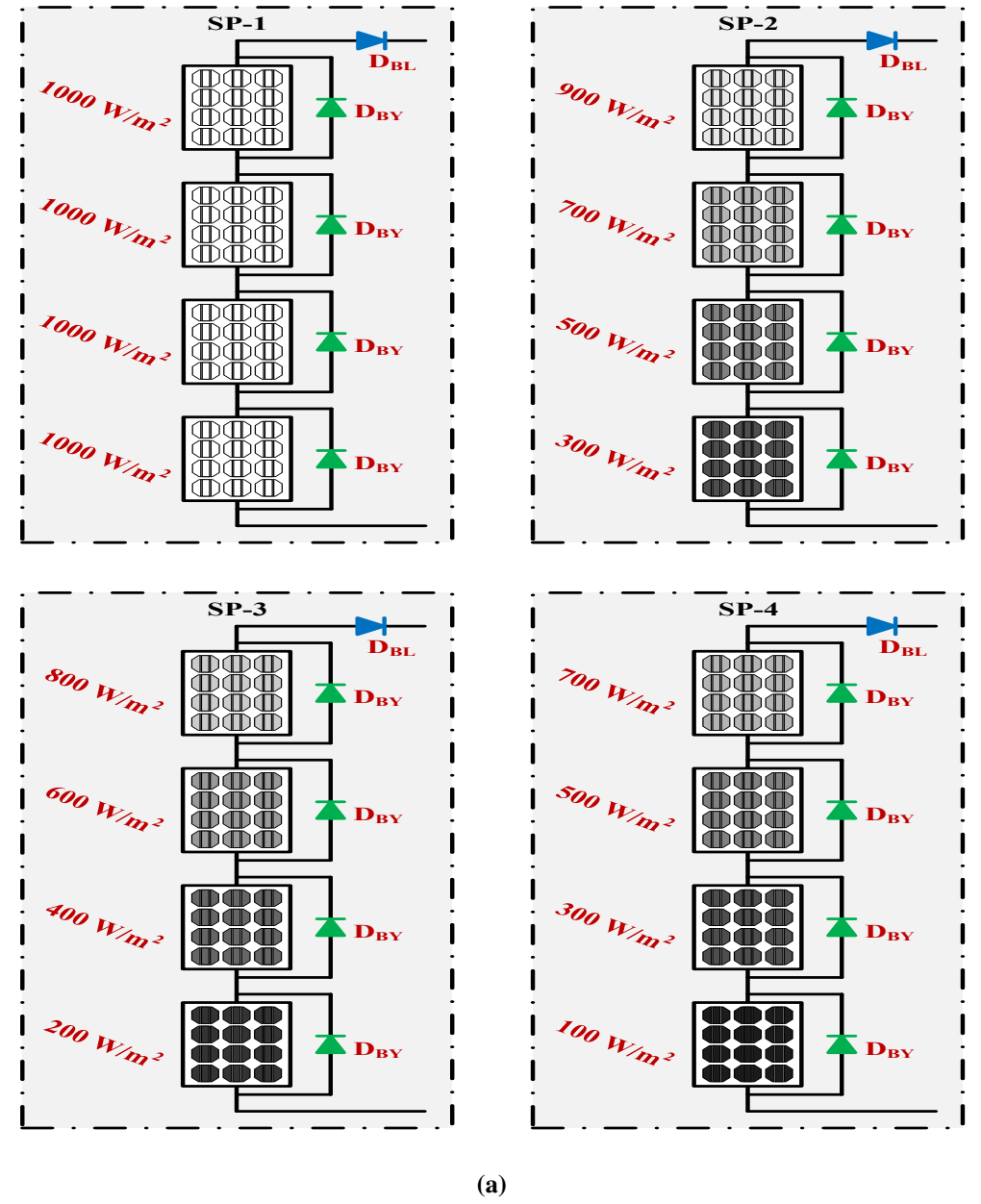
6.2.2 Array under *PSC*

In the proposed work, two different array configurations referred to as *Four-Series (*4*S)* and *Two-Series & Two-Parallel (*2*S*2*P)*, are formed by the interconnection of four *PV* modules and are shown in Fig. 6.3(a) and Fig. 6.4(a), respectively. With four different shading patterns (*SP*-1 to *SP*-4), the resulting *I–V* and *P–V* characteristics with 4*S* arrangement are shown in Figs. 6.3(b) and 6.3(c), while for shading patterns (*SP*-5 to *SP*-8), the characteristics with 2*S*2*P* configurations are shown in Figs. 6.4(b) and 6.4(c).

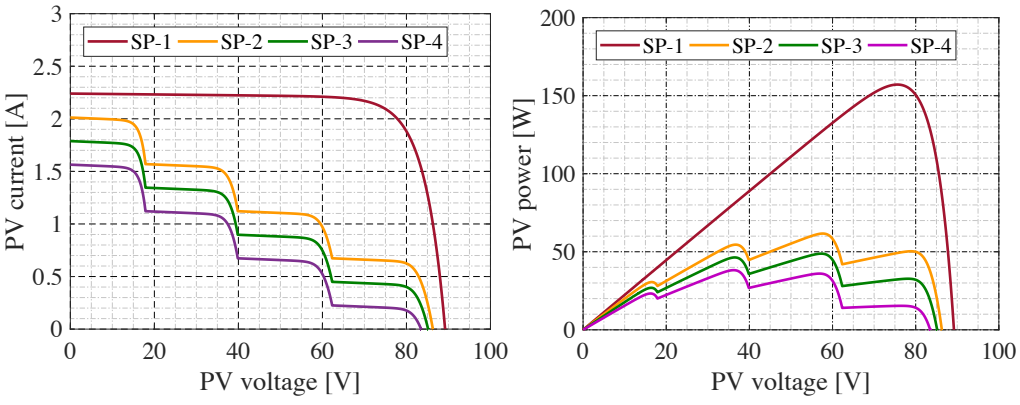
When the *PV* array is operating under uniform irradiation *SP*-1, the resulting *P–V* characteristic yields single *MPP* (i.e., *GMPP*). Whereas, during *PSCs*, multiple *LMPPs* are observed in the *P–V* curves. This is due to the presence of bypass diode ($\mathrm{D_{BY}}$) connected in parallel with each *PV* module. With parallel connections of PV modules, as in 2*S*2*P* configuration, the shaded string draws current from other strings in parallel, thereby resulting in a circulating current, which reduces the efficiency of the *PV* panel. The blocking diode ($\mathrm{D_{BL}}$) is therefore used with each series string, as shown in Fig. 6.4(a). Diode $\mathrm{D_{BL}}$ ensures that the current only flows out of the series array to the external circuit. It can be observed that the *GMPP* can occur in either the lower or higher voltage range, depending on the type of *SP*. This phenomenon makes it difficult to directly apply the conventional *MPPT* algorithms.

6.2.3 *QZS* converter

At *MPP*, the *PV* source is replaced by a voltage source (*MPP* voltage, $V_{\mathrm{PV}}^{\mathrm{mx}}$) in series with the internal resistance ($R_{\mathrm{PV}}^{\mathrm{mx}}$) whose value is equal to load resistance [115]. The *QZS* converter is

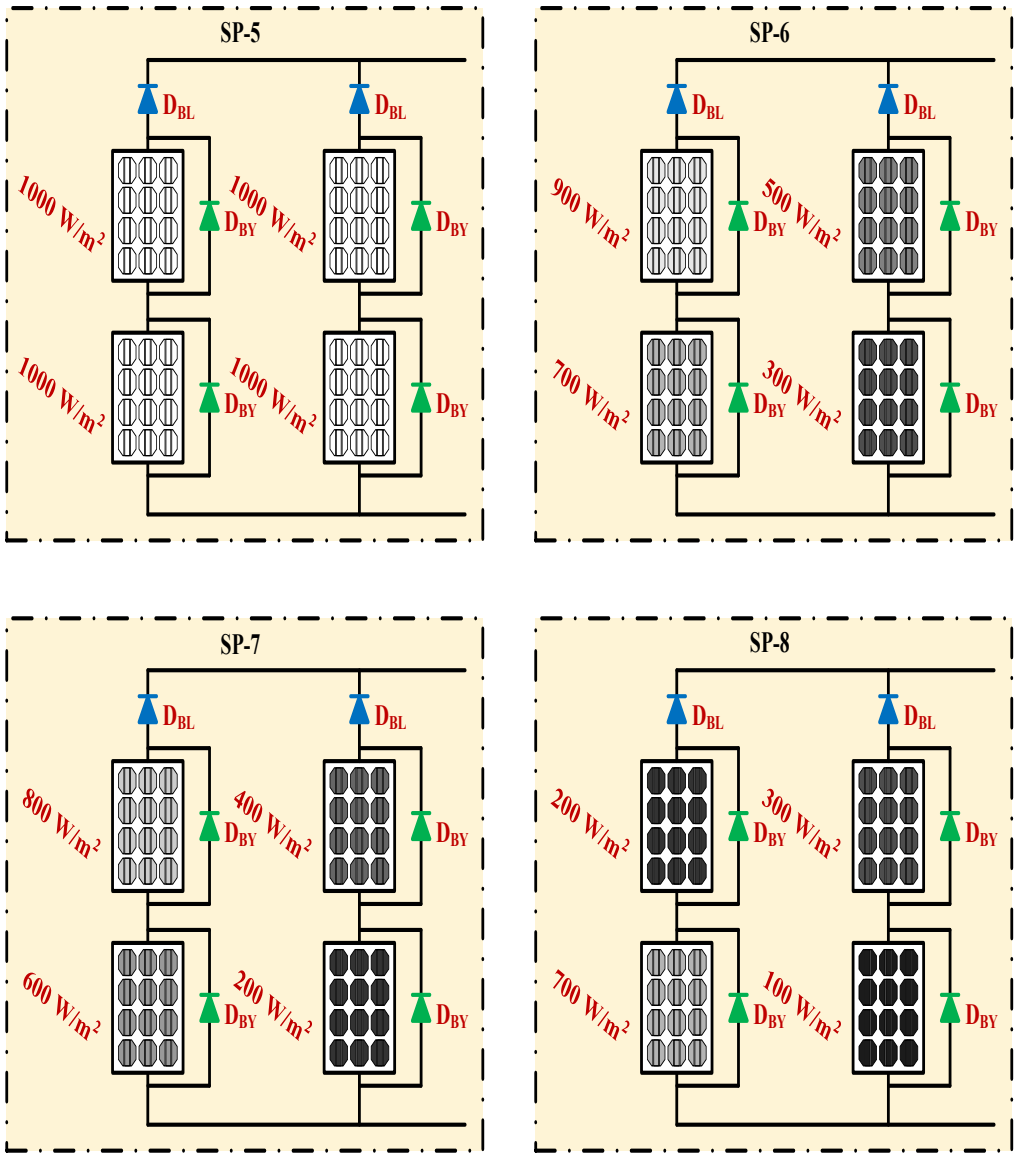


(a)

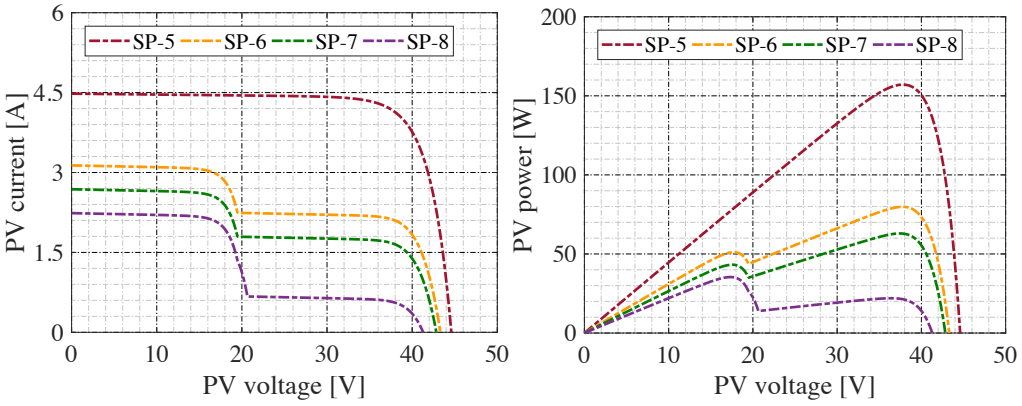


(b) **(c)**

Fig. 6.3: 4*S PV* configuration. **(a)** Different *SPs*. **(b)** *I–V* curves. **(c)** *P–V* curves.



(a)



(b) **(c)**

Fig. 6.4: 2*S*2*P PV* configuration. **(a)** Different *SPs*. **(b)** *I–V* curves. **(c)** *P–V* curves.

placed between the *PV* source and the load as shown in Fig. 6.1. Switching operation on the *QZS* converter provides a boosted DC output while controlling the operating point of the *PV* source. The converter, in *CCM* operation, can be modeled with the help of state-space averaging methodology. When the inductor current is continuous, there are two operational states as shown in Fig. 6.5, State-1: Q-ON, D_1-OFF; State-2: Q-OFF, D_1-ON and accordingly the average model will be:

$$\dot{\boldsymbol{x}} = \boldsymbol{A}\boldsymbol{x} + \boldsymbol{B}\boldsymbol{u} + \boldsymbol{E} \tag{6.5}$$

where $\boldsymbol{A} = d_{\text{st}}\boldsymbol{A_0} + d_{\text{nst}}\boldsymbol{A_1}$, $\boldsymbol{B} = d_{\text{st}}\boldsymbol{B_0} + d_{\text{nst}}\boldsymbol{B_1}$, and $d_{\text{nst}} = 1 - d_{\text{st}}$ and d_{st} is the duty ratio of the switch Q. The state vector $\boldsymbol{x}$ and input vector $\boldsymbol{u}$ are formed as $\boldsymbol{x} = [\, v_{\text{PV}}\ i_{\text{L1}}\ i_{\text{L2}}\ v_{\text{C1}}\ v_{\text{C2}}\,]^{\intercal}$ and $\boldsymbol{u} = [\, i_{\text{dc}}\,]$, respectively. Where, v_{PV} is *PV* output voltage; i_{L1} and i_{L2} are *QZS* network inductor currents; v_{C1} and v_{C2} are *QZS* network capacitor voltages; and i_{dc} is load current. Matrices $\boldsymbol{A_0}$, $\boldsymbol{A_1}$, $\boldsymbol{B_0}$, $\boldsymbol{B_1}$, and $\boldsymbol{E}$ are defined as:

$$\boldsymbol{A_0} = \begin{bmatrix} -\frac{1}{R_{\text{PV}}^{\text{mx}} C_{\text{P}}} & -\frac{1}{C_{\text{P}}} & 0 & 0 & 0 \\ \frac{1}{L} & -\frac{(R_{\text{L}}+R_{\text{C}})}{L} & 0 & 0 & \frac{1}{L} \\ 0 & 0 & -\frac{(R_{\text{L}}+R_{\text{C}})}{L} & \frac{1}{L} & 0 \\ 0 & 0 & -\frac{1}{C} & 0 & 0 \\ 0 & -\frac{1}{C} & 0 & 0 & 0 \end{bmatrix} \boldsymbol{A_1} = \begin{bmatrix} -\frac{1}{R_{\text{PV}}^{\text{mx}} C_{\text{P}}} & -\frac{1}{C_{\text{P}}} & 0 & 0 & 0 \\ \frac{1}{L} & -\frac{(R_{\text{L}}+R_{\text{C}})}{L} & 0 & -\frac{1}{L} & 0 \\ 0 & 0 & -\frac{(R_{\text{L}}+R_{\text{C}})}{L} & 0 & -\frac{1}{L} \\ 0 & \frac{1}{C} & 0 & 0 & 0 \\ 0 & 0 & \frac{1}{C} & 0 & 0 \end{bmatrix}$$

$$\boldsymbol{B_0} = \begin{bmatrix} 0 \\ 0 \\ 0 \\ 0 \\ 0 \end{bmatrix} \qquad \boldsymbol{B_1} = \begin{bmatrix} 0 \\ \frac{R_{\text{C}}}{L} \\ \frac{R_{\text{C}}}{L} \\ -\frac{1}{C} \\ -\frac{1}{C} \end{bmatrix} \qquad \boldsymbol{E} = \begin{bmatrix} \frac{V_{\text{PV}}^{\text{mx}}}{R_{\text{PV}}^{\text{mx}} C_{\text{P}}} \\ 0 \\ 0 \\ 0 \\ 0 \end{bmatrix}$$

The steady-state values of the state vectors are obtained by equating the first derivative of state vectors to zero, i.e., $\dot{\boldsymbol{X}} = 0$. Thus, steady-state values are given as $\boldsymbol{X_{ss}} = -\boldsymbol{A^{-1}BU} + \boldsymbol{E}$. In State-1, the load voltage v_{dc} is zero, while it's value is $\{V_{\text{C1}} + V_{\text{C2}} + R_{\text{C}}(I_{\text{L1}} + I_{\text{L2}} - 2I_{\text{dc}})\}$ in State-2. Thus, we can easily obtain the steady-state voltage gain of the converter as:

$$\frac{V_{\text{dc}}^{\text{av}}}{V_{\text{PV}}} = \frac{(D_{\text{nst}} - D_{\text{st}})R}{(D_{\text{nst}} - D_{\text{st}})^2 R + 2D_{\text{nst}}(R_{\text{L}} D_{\text{nst}} + R_{\text{C}} D_{\text{st}})} \tag{6.6}$$

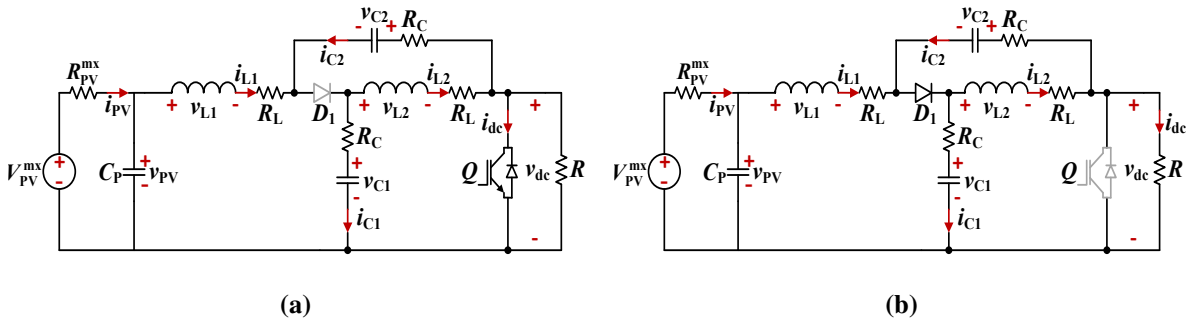


Fig. 6.5: Operation of *QZS* converter. **(a)** State-1. **(b)** State-2.

If $R_L, R_C \ll R$ then the load voltage and the *PV* voltage are related as:

$$\frac{V_{dc}^{av}}{V_{PV}} = \frac{1}{D_{nst} - D_{st}} \tag{6.7}$$

Using power balance, the relationship between *PV* current and load current is expressed as:

$$I_{PV} = \frac{I_{dc}(1 - D_{st})}{\eta(1 - 2D_{st})} \tag{6.8}$$

where η is the efficiency of the converter, V_{PV}, I_{PV} are the *PV* array voltage and current, respectively. The load resistance referred to the *PV* side is given as:

$$R_{PV} = \frac{\eta R(1 - 2D_{st})^2}{(1 - D_{st})^2} \tag{6.9}$$

i.e.,

$$\frac{V_{PV}}{I_{PV}} = \frac{\eta R(1 - 2D_{st})^2}{(1 - D_{st})^2} \tag{6.10}$$

Using (6.4) and (6.10) it is noted that, for given values of *PV* array parameters, weather conditions, the *PV* array voltage depends on the converter duty ratio (D_{st}). The power extracted from the *PV* is given as:

$$P_{PV} = V_{PV} I_{PV} \tag{6.11}$$

By substituting $I_{PV} = V_{PV}/R_{PV}$ and using (6.9), the (6.11) is modified as:

$$P_{PV} = \frac{V_{PV}^2(1 - D_{st})^2}{\eta R(1 - 2D_{st})^2} \tag{6.12}$$

As *PV* array power and voltage depend upon the duty ratio; therefore, the power tracking process can be achieved by controlling the converter duty ratio.

6.3 STABILITY ANALYSIS

The *PV* system using *MPPT* algorithm is constantly exposed to two dynamic conditions: one due to changing weather and the other due to perturbation caused by the *MPPT* algorithm. When the system operates under steady-state solar irradiance and temperature conditions, it is still subjected to continuous changes in the control parameter (duty ratio) at a selected perturbation size as in the case of *P&O* technique. To comment on the transient response and stability of the system, duty ratio to *PV* voltage transfer function $G_{\mathrm{vd}}(s)$ is calculated. In the direct duty cycle controlled PV system, converter operates as an open loop system [193].

Perturbation and linearization is applied to (6.5), neglecting the higher-order perturbation terms and transforming the equation in Laplace domain results as:

$$\begin{cases} C_{\mathrm{P}}\tilde{v}_{\mathrm{PV}}(s) = -\dfrac{\tilde{v}_{\mathrm{PV}}(s)}{R_{\mathrm{PV}}^{\mathrm{mx}}} - \tilde{i}_{\mathrm{L1}}(s) \\ L\tilde{i}_{\mathrm{L1}}(s) = \left(V_{\mathrm{C1}} + V_{\mathrm{C2}} - R_{\mathrm{C}}I_{\mathrm{dc}}\right)\tilde{d}_{\mathrm{st}}(s) + \tilde{v}_{\mathrm{PV}}(s) + R_{\mathrm{C}}D_{\mathrm{nst}}\tilde{i}_{\mathrm{dc}}(s) \\ \qquad\qquad - \left(R_{\mathrm{L}} + R_{\mathrm{C}}\right)\tilde{i}_{\mathrm{L1}}(s) - D_{\mathrm{nst}}\tilde{v}_{\mathrm{C1}}(s) + D_{\mathrm{st}}\tilde{v}_{\mathrm{C2}}(s) \\ L\tilde{i}_{\mathrm{L2}}(s) = \left(V_{\mathrm{C1}} + V_{\mathrm{C2}} - R_{\mathrm{C}}I_{\mathrm{dc}}\right)\tilde{d}_{\mathrm{st}}(s) + R_{\mathrm{C}}D_{\mathrm{nst}}\tilde{i}_{\mathrm{dc}}(s) \\ \qquad\qquad - \left(R_{\mathrm{L}} + R_{\mathrm{C}}\right)\tilde{i}_{\mathrm{L2}}(s) + D_{\mathrm{st}}\tilde{v}_{\mathrm{C1}}(s) - D_{\mathrm{nst}}\tilde{v}_{\mathrm{C2}}(s) \\ C\tilde{v}_{\mathrm{C1}}(s) = \left(I_{\mathrm{dc}} - I_{\mathrm{L1}} - I_{\mathrm{L2}}\right)\tilde{d}_{\mathrm{st}}(s) - D_{\mathrm{nst}}\tilde{i}_{\mathrm{dc}}(s) + D_{\mathrm{nst}}\tilde{i}_{\mathrm{L1}}(s) - D_{\mathrm{st}}\tilde{i}_{\mathrm{L2}}(s) \\ C\tilde{v}_{\mathrm{C2}}(s) = \left(I_{\mathrm{dc}} - I_{\mathrm{L1}} - I_{\mathrm{L2}}\right)\tilde{d}_{\mathrm{st}}(s) - D_{\mathrm{nst}}\tilde{i}_{\mathrm{dc}}(s) - D_{\mathrm{st}}\tilde{i}_{\mathrm{L1}}(s) + D_{\mathrm{nst}}\tilde{i}_{\mathrm{L2}}(s) \end{cases} \tag{6.13}$$

Using (6.13), the $G_{\mathrm{vd}}(s)$ is defined as:

$$G_{\mathrm{vd}}(s) = \frac{-\left(a_3 s^3 + a_2 s^2 + a_1 s + a_0\right)}{b_5 s^5 + b_4 s^4 + b_3 s^3 + b_2 s^2 + b_1 s + b_0} \tag{6.14}$$

where

$$\begin{aligned}
a_3 &= R_{\mathrm{PV}}^{\mathrm{mx}} C^2 L \left(V_{\mathrm{C1}} + V_{\mathrm{C2}} - R_{\mathrm{C}}I_{\mathrm{dc}}\right) \\
a_2 &= R_{\mathrm{PV}}^{\mathrm{mx}} C\left[C\left(R_{\mathrm{C}} + R_{\mathrm{L}}\right)\left(V_{\mathrm{C1}} + V_{\mathrm{C2}} - R_{\mathrm{C}}I_{\mathrm{dc}}\right) + L\left(D_{\mathrm{nst}} - D_{\mathrm{st}}\right)\left(I_{\mathrm{L1}} + I_{\mathrm{L2}} - I_{\mathrm{dc}}\right)\right] \\
a_1 &= R_{\mathrm{PV}}^{\mathrm{mx}} C\left[\left(R_{\mathrm{C}} + R_{\mathrm{L}}\right)\left(D_{\mathrm{nst}} - D_{\mathrm{st}}\right)\left(I_{\mathrm{L1}} + I_{\mathrm{L2}} - I_{\mathrm{dc}}\right) + \left(V_{\mathrm{C1}} + V_{\mathrm{C2}} - R_{\mathrm{C}}I_{\mathrm{dc}}\right)\right] \\
a_0 &= R_{\mathrm{PV}}^{\mathrm{mx}}\left(D_{\mathrm{nst}} - D_{\mathrm{st}}\right)\left(I_{\mathrm{L1}} + I_{\mathrm{L2}} - I_{\mathrm{dc}}\right) \\
b_5 &= C^2 L^2 C_{\mathrm{P}} R_{\mathrm{PV}}^{\mathrm{mx}} \\
b_4 &= C^2 L\left[L + 2R_{\mathrm{PV}}^{\mathrm{mx}} C_{\mathrm{P}}\left(R_{\mathrm{C}} + R_{\mathrm{L}}\right)\right] \\
b_3 &= C\left[CC_{\mathrm{P}}R_{\mathrm{PV}}^{\mathrm{mx}}\left(R_{\mathrm{L}} + R_{\mathrm{C}}\right)^2 + LCR_{\mathrm{PV}}^{\mathrm{mx}} + 2LC\left(R_{\mathrm{L}} + R_{\mathrm{C}}\right) + 2LC_{\mathrm{P}}R_{\mathrm{PV}}^{\mathrm{mx}}\left(D_{\mathrm{nst}}^2 + D_{\mathrm{st}}^2\right)\right]
\end{aligned}$$

$$b_2 = C\left[R_{\mathrm{PV}}^{\mathrm{mx}}\left\{C + C_{\mathrm{P}} + C_{\mathrm{P}}\left(D_{\mathrm{nst}} - D_{\mathrm{st}}\right)^2\right\}\left(R_{\mathrm{C}} + R_{\mathrm{L}}\right) + C\left(R_{\mathrm{L}} + R_{\mathrm{C}}\right)^2 + 2L\left(D_{\mathrm{nst}}^2 + D_{\mathrm{st}}^2\right)\right]$$

$$b_1 = C\left(R_{\mathrm{PV}}^{\mathrm{mx}} + 2R_{\mathrm{L}} + 2R_{\mathrm{C}}\right)\left(D_{\mathrm{nst}}^2 + D_{\mathrm{st}}^2\right) + R_{\mathrm{PV}}^{\mathrm{mx}} C_{\mathrm{P}}\left(D_{\mathrm{nst}} - D_{\mathrm{st}}\right)^2$$

$$b_0 = \left(D_{\mathrm{nst}} - D_{\mathrm{st}}\right)^2$$

The coefficients of the transfer function are determined by using the system parameter values from Tables 6.1 and 6.2 for shading pattern *SP*-5. The transfer function has one negative real pole at $s = -20.66$, two pairs of complex conjugate poles at $s = -393.89 \pm j1749.48$ and $s = 368.97 \pm j794.09$. It has one negative real zero at $s = -65.35$ and two complex zeros at $s = -360 \pm j1158.01$. The Pole-Zero map of the transfer function is illustrated in Fig. 6.6. The open loop system $G_{\mathrm{vd}}(s)$ will be stable as all the poles of the system transfer function are lying in negative left-half of s-plane.

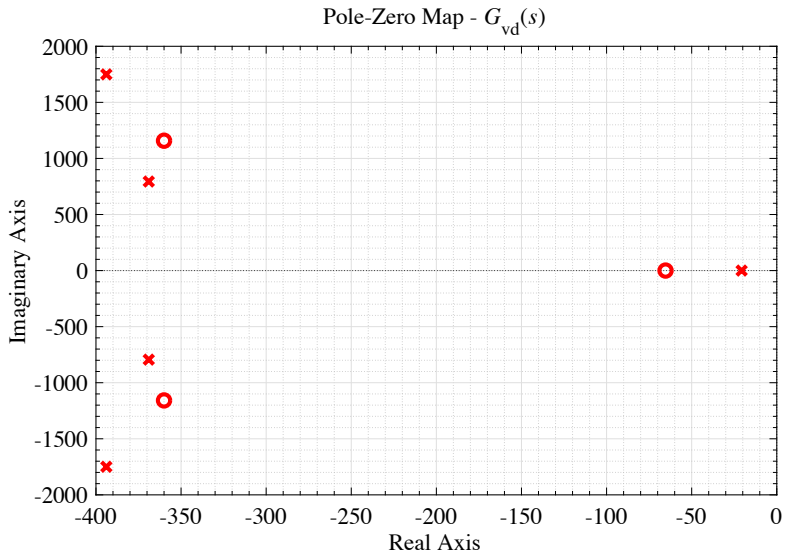


Fig. 6.6: Pole-Zero map of $G_{\mathrm{vd}}(s)$.

6.4 FUNDAMENTAL *FSSO* ALGORITHM

The *FSSO* algorithm imitates the dynamic foraging strategy of southern *Flying Squirrels (FSs)* and their gliding locomotion, as shown in Fig. 6.7. The potential solution vector and the corresponding fitness are referred to as the position of a *FS* and quality of food source, respectively. The position on the basis of fitness values is initially classified into three regions representing sets of *Optimum Solution (OS)* as hickory nut tree, *Near Optimum Solution (NOS)*

as acorn nut tree and *Random Solution (RS)* as normal tree. In the first step, the *NOS* is moved in the direction decided by global the best solution. In the second step, a part of *RSs* is directed to move towards *OS*. The remaining *RSs* are moved towards *NOS* in the third step. Such cooperation between *OS*, *NOS*, and *RS* is key to its convergence characteristics. The presented *MPPT* algorithm, not only exploit this feature of cooperation but positions are updated without the presence of predator.

6.5 *FSSO* ALGORITHM FOR *GMPP* TRACKING

For *MPPT*, the *PV* power output P_{PV} is taken as the objective (food source) and the duty ratio D_{st} of the *QZS* converter is the decision variable (position). The existing *FSSO* algorithm is suitably tailored by eliminating the presence of predator to reduce the convergence time to *GMPP*. The flowchart is shown in Fig. 6.8 and different stages and steps of *FSSO* algorithm to track *GMPP* are summarized as:

1. ***Initialization*:** Initially, N_{fs} flying squirrels are located at different positions, which are different values of duty ratio of the *QZS* converter. The position of *FSs* in the solution space is defined as:

$$d_{\mathrm{st}}^{\mathrm{i}} = d_{\mathrm{st}}^{\mathrm{mn}} + \frac{(i-1)[d_{\mathrm{st}}^{\mathrm{mx}} - d_{\mathrm{st}}^{\mathrm{mn}}]}{N_{\mathrm{fs}}}; i = 1, 2, \ldots, N_{\mathrm{fs}} \tag{6.15}$$

where $d_{\mathrm{st}}^{\mathrm{mn}}$ and $d_{\mathrm{st}}^{\mathrm{mx}}$ represent minimum and maximum values of converter duty ratio for the boost operation, which are taken as 10% and 90% of the permissible duty ratio.

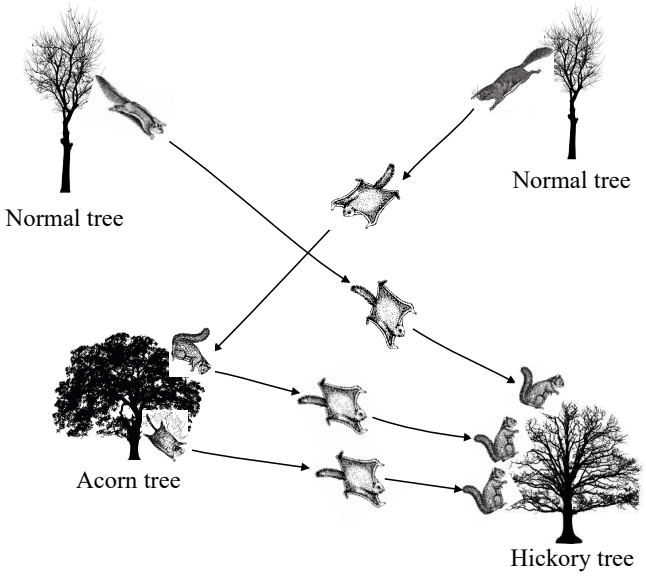


Fig. 6.7: Foraging behavior of *FSs*.

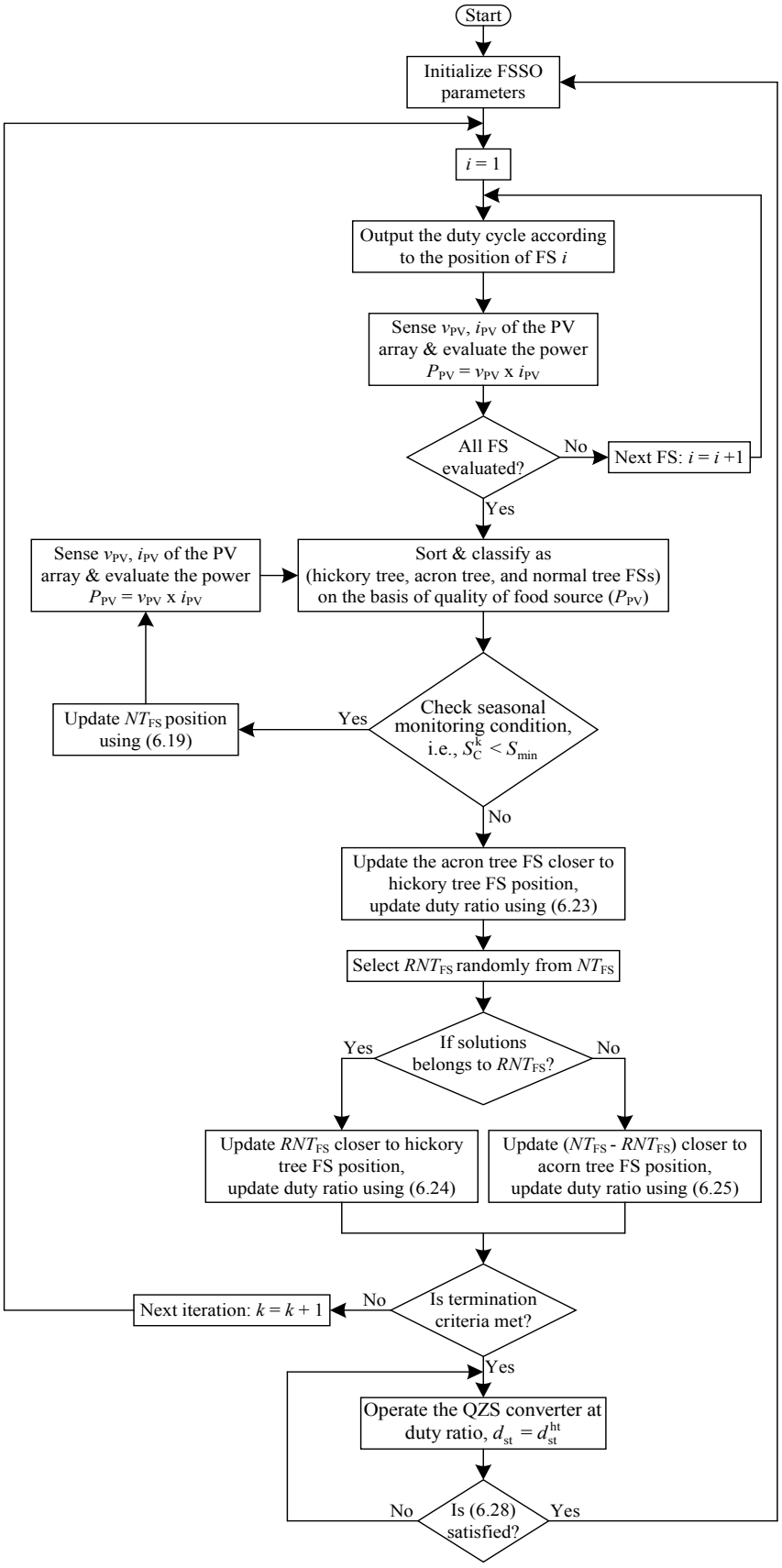


Fig. 6.8: Flowchart for the proposed *FSSO* algorithm.

The constraint limits on duty ratio are decided by (6.7) as:

$$0 < d_{\mathrm{st}}^{\mathrm{i}} < 0.5 \tag{6.16}$$

2. ***Fitness evaluation*:** In this step, the *QZS* converter is operated with each duty ratio (i.e., position of each *FS*) successively. For each duty ratio d_{st}, the instantaneous *PV* power output $P_{\mathrm{PV}}(d_{\mathrm{st}})$, is taken as quality of food source. This step is repeated for all duty cycles and the objective fitness function (f) for *MPPT* is defined as:

$$f(d_{\mathrm{st}}) = \max P_{\mathrm{PV}}(d_{\mathrm{st}}) \tag{6.17}$$

3. ***Declaration and sorting*:** Duty ratio with maximum *PV* power output is declared to be on the hickory tree. The next best position of *FS* is considered to be on acorn tree. The remaining *FSs* (NT_{FS}) are assumed to be positioned on the normal trees.

4. ***Position update*:** The duty cycle update is carried out after checking the seasonal monitoring condition. If ($S_{\mathrm{C}}^{\mathrm{k}} < S_{\min}$), the duty cycles are updated using **(a)**, otherwise duty cycles are updated using **(b)**. Thereafter, the fitness is evaluated.

a. ***Seasonal monitoring condition*:** Inclusion of seasonal monitoring condition prevents the algorithm from being trapped in *LMPP*. For a single dimensional search space, the seasonal constant (S_{C}) and its minimum value ($S_{\min}$) are computed as:

$$\begin{cases} S_{\mathrm{C}}^{\mathrm{k}} = \left| d_{\mathrm{st}}^{\mathrm{at,k}} - d_{\mathrm{st}}^{\mathrm{ht}} \right| \\ S_{\min} = \dfrac{10e^{-6}}{(365)^{k/(k_{\mathrm{m}}/2.5)}} \end{cases} \tag{6.18}$$

where $d_{\mathrm{st}}^{\mathrm{ht}}$ and $d_{\mathrm{st}}^{\mathrm{at}}$ represent squirrels position at hickory and acorn tree, respectively; k is the current iteration number and k_{m} is the maximum number of iterations allowed. The duty ratios (*FSs* on normal trees) NT_{FS} are relocated using Lévy distribution for better search space exploration [194].

$$d_{\mathrm{st}}^{\mathrm{nt,(k+1)}} = d_{\mathrm{st}}^{\mathrm{nt,k}} + s \tag{6.19}$$

where $d_{\mathrm{st}}^{\mathrm{nt}}$ represent squirrel position at normal tree and step length s using Lévy distribution is presented as:

$$s \approx \kappa \left(\frac{u}{|v|^{\frac{1}{\beta}}} \right) (d_{\mathrm{st}}^{\mathrm{ht}} - d_{\mathrm{st}}^{\mathrm{nt}}) \tag{6.20}$$

where the Lévy index β and step coefficient κ are taken as 1.5 and 1.25, respectively and u and v are determined from normal distribution curve as:

$$u \approx N(0, \sigma_{\mathrm{u}}^2) \quad \text{and} \quad v \approx N(0, \sigma_{\mathrm{v}}^2) \tag{6.21}$$

If Γ denotes the integral gamma function, then the variables σ_{u} and σ_{v} are defined as:

$$\sigma_{\mathrm{u}} = \left(\frac{\Gamma(1+\beta)\sin(\pi\beta/2)}{\Gamma\left(\frac{(1+\beta)}{2}\right)\beta(2)^{\left(\frac{\beta-1}{2}\right)}} \right)^{\frac{1}{\beta}} \text{ and } \sigma_{\mathrm{v}} = 1 \tag{6.22}$$

where $\Gamma(n) = (n-1)!$.

b. ***Routine update*:** The squirrel on the hickory tree remains in its position. The squirrel on the acorn tree moves toward the hickory tree. Some randomly selected squirrels RNT_{FS} from normal trees move toward hickory tree, while the remaining $(NT_{\mathrm{FS}} - RNT_{\mathrm{FS}})$ move toward acorn tree. The corresponding duty ratios are updated according to the following equations:

$$d_{\mathrm{st}}^{\mathrm{at,(k+1)}} = d_{\mathrm{st}}^{\mathrm{at,k}} + g_{\mathrm{d}} G_{\mathrm{c}} (d_{\mathrm{st}}^{\mathrm{ht,k}} - d_{\mathrm{st}}^{\mathrm{at,k}}) \tag{6.23}$$

$$d_{\mathrm{st}}^{\mathrm{nt,(k+1)}} = d_{\mathrm{st}}^{\mathrm{nt,k}} + g_{\mathrm{d}} G_{\mathrm{c}} (d_{\mathrm{st}}^{\mathrm{ht,k}} - d_{\mathrm{st}}^{\mathrm{nt,k}}) \tag{6.24}$$

$$d_{\mathrm{st}}^{\mathrm{nt,(k+1)}} = d_{\mathrm{st}}^{\mathrm{nt,k}} + g_{\mathrm{d}} G_{\mathrm{c}} (d_{\mathrm{st}}^{\mathrm{at,k}} - d_{\mathrm{st}}^{\mathrm{nt,k}}) \tag{6.25}$$

where G_{c} and g_{d} represent the gliding constant and gliding distance, respectively. The value of G_{c} is taken as 1.90 after rigorous simulations. The gliding distance g_{d} is expressed as:

$$\begin{cases} g_{\mathrm{d}} = \dfrac{h_{\mathrm{g}}}{s_{\mathrm{f}} \tan\theta} \\ \tan\theta = \dfrac{F_{\mathrm{D}}}{F_{\mathrm{L}}} \end{cases} \tag{6.26}$$

where θ is the glide angle, value of h_{g} height loss after gliding is taken as 8 m; the scaling factor s_{f} is selected as 18 to keep g_{d} between 0.5 and 1.11 to limit the perturbations in (6.23), (6.24), and (6.25). F_{D} and F_{L} are the drag and the lift forces, respectively, which are calculated as:

$$\begin{cases} F_{\mathrm{D}} = \dfrac{1}{2}\rho V^2 S C_{\mathrm{D}} \\ F_{\mathrm{L}} = \dfrac{1}{2}\rho V^2 S C_{\mathrm{L}} \end{cases} \tag{6.27}$$

where values of ρ air density, V velocity of squirrel, and S surface area of body are chosen as 1.204 kg/m^3, 5.25 m/s, and 154 cm^2, respectively. The drag coefficient C_{D} is taken as 0.6 and lift coefficient C_{L} is chosen randomly between 0.675 and 1.5 [195].

5. ***Convergence determination*:** If the change in position of all *FSs* become smaller than a threshold, or if the maximum number of iterations is reached, the optimization algorithm is terminated and output the duty cycle at which the *QZS* converter works while tracking the *GMPP*.

6. ***Re-initialization*:** The *MPPT* is time variant optimization where the fitness value often changes with the *WCs*. In such cases, the *FSs* positions (duty ratios) are reinitialized to search for the new *GMPP* again. In this article, the duty ratios are reinitialized after detecting the change in *SP* or insolation through the following constraint equation:

$$\frac{P_{\mathrm{PV}}^{\mathrm{k+1}} - P_{\mathrm{PV}}^{\mathrm{k}}}{P_{\mathrm{PV}}^{\mathrm{k+1}}} \geq \Delta P(\%) \tag{6.28}$$

6.6 SIMULATION RESULTS

To determine the effectiveness of the presented *MPPT* algorithm based on *FSSO*, its performance is compared with *MPPT* algorithms based on *P&O*, *PSO*, and *GWO*. The implementation of these *MPPT* algorithms is carried out in MATLAB 2017b on Intel core i7, 3.4-GHz, 8 GB RAM, and Windows 10 operating system. The block diagram for tracking *GMPP* under *PSC* is shown in Fig. 6.1. The parameters for modeling single diode representation of a *PV* module, introduced in subsection 6.2.1, are taken from MicroSun *PV* module data-sheet presented in Table 6.1 [196]. The *QZS* converter, working as a boost converter, is used between the *PV* source and load. The parameters for the designed converter are summarized in Table 6.2. The simulation studies for *GMPP* tracking have been conducted for *SPs* in the following two *PV* configurations:

- With series-connected 4*S* configuration, shown in Fig. 6.3(a), the investigation is carried out for shading patterns *SP*-2 and *SP*-3.

- With series-parallel 2*S*2*P* configuration, shown in Fig. 6.4(a), analysis is carried out for shading patterns *SP*-6 and *SP*-8.

The fixed step size for *P&O* method is taken as 10^{-2}. The parameters of *PSO* algorithm $w_{\max} = 1$, $w_{\min} = 0.1$, $c_{1,\max} = 2$, $c_{1,\min} = 1$, and $c_{2,\max} = 2$, $c_{2,\min} = 1$ are the upper and lower bounds of the w, c_1, and c_2, respectively. Where w is the inertia weight, c_1 is the cognitive rate, and c_2 is the social rate. The parameter a of the *GWO* algorithm linearly reduces from 2 to 0. Furthermore, to ensure the system attains steady-state before another *MPPT* cycle is initiated, the sampling interval for simulation and real-time tests is chosen as 0.01 s keeping the consideration of the available hardware OP-4510 from OPAL-RT Technologies processor as it is having a maximum switching frequency of 10 kHz.

Table 6.1. Adjusted model of MicroSun *PV* module specification

Parameter	Values
Electrical properties	
Maximum power	40 W
MPP voltage	18.1 V
MPP current	2.21 A
Open circuit voltage	22.32 V
Short circuit current	2.24 A
Number of cells in series	36
Series resistance	0.0001 Ω
Parallel resistance	601.424 Ω
Temperature coefficients	
Nominal power/temperature coefficient	−0.43 %/°C
Open circuit voltage/temperature coefficient	−0.36 %/°C
Short circuit current/temperature coefficient	0.06 %/°C

Table 6.2. Parameters of *QZS* converter

Parameters	Values
PV terminal capacitor, (C_{P})	470 μF
Inductors, (L_1, L_2)	1 mH
Winding resistance of *QZS* network inductors, R_{L}	0.68 Ω
Capacitors, (C_1, C_2)	680 μF
ESR of *QZS* network capacitors, R_{C}	0.04 Ω
Switching frequency, f_{s}	10 kHz

While tracking *GMPP*, the *PV* output power may have oscillations decided by the population size for *PSO*, *GWO*, and *FSSO*. For low population size, the algorithm may get

trapped in the local optima or convergence time may increase. On the contrary, large population size may lead to faster convergence, but with a simultaneous increase in the computation step and the duration of output power oscillations. Therefore, while deciding the population size, a balance is to be maintained. In this regard, the authors carried out simulations with various population sizes and population size of four was considered to be a balanced choice. The simulations by *P&O*, *PSO*, *GWO*, and *FSSO* algorithms are performed in a similar circuit and *WCs*.

6.6.1 4*S* configuration performance

The *MPPT* curves for 4*S* configuration under *SP*-2, shown in Fig. 6.3(c), are presented in Fig. 6.9. The *PV* voltage and current are also depicted in Fig. 6.9. *SP*-2 has three *LMPP* with *GMPP* of 61.665 W as shown in Fig. 6.3(c). *PSO* converge to the *GMPP* of 61.61 W, *GWO* converge to the *GMPP* of 61.65 W, and *FSSO* converge to the *GMPP* of 61.66 W. The convergence time taken by *PSO* and *GWO* based *MPPT* algorithms is 4.3 s and 2.6 s, respectively, while for *FSSO*, it is 1.8 s. The *P&O* algorithm tracks the *LMPP* of 29.71 W as it is unable to discriminate between *LMPP* and *GMPP*. Thus, in the case of *P&O*, the steady-state oscillation persists in the operating point, causing power loss and reduction in the efficiency. When *SP* changes to *SP*-3 at $t = 10$ s, the *MPPT* algorithms are reinitialized. The *SP*-3, as shown in Fig. 6.3(c), also has three *LMPP* with *GMPP* of 48.785 W. The *PSO* and *GWO MPPT* algorithms track the *GMPP* of 48.58 W and 48.63 W, respectively, whereas the *FSSO* tracks the *GMPP* of 48.65 W. The *P&O* could not reach *GMPP* and held back at *LMPP* of 26.2 W. The tracking time duration of *PSO* and *GWO* is 3.9 s and 1.8 s, respectively, while *FSSO* takes 1.3 s.

6.6.2 2*S*2*P* configuration performance

For simulation under 2*S*2*P* configuration, the *SP*-6 is made to exist for the first 10 s and the *SP*-8 appears for the next 10 s. The tracking curves are portrayed in Fig. 6.10. Shading patterns *SP*-6 and *SP*-8 each having one *LMPP* and *GMPP* of 79.81 W and 35.389 W, respectively, are shown in Fig. 6.4(c). The *PSO* based *MPPT* algorithm tracks *GMPP* of 79.71 W in 3.75 s. The *GWO* based *MPPT* method traces *GMPP* of 79.73 W in 2.4 s. The *FSSO* follows the *GMPP* of 79.75 W in 0.75 s, and *P&O* tracks the *LMPP* of 49.31 W as it tracks the peak which comes in contact first, i.e., it may be *GMPP* or *LMPP* resulting in oscillations around *MPP*. At $t = 10$ s,

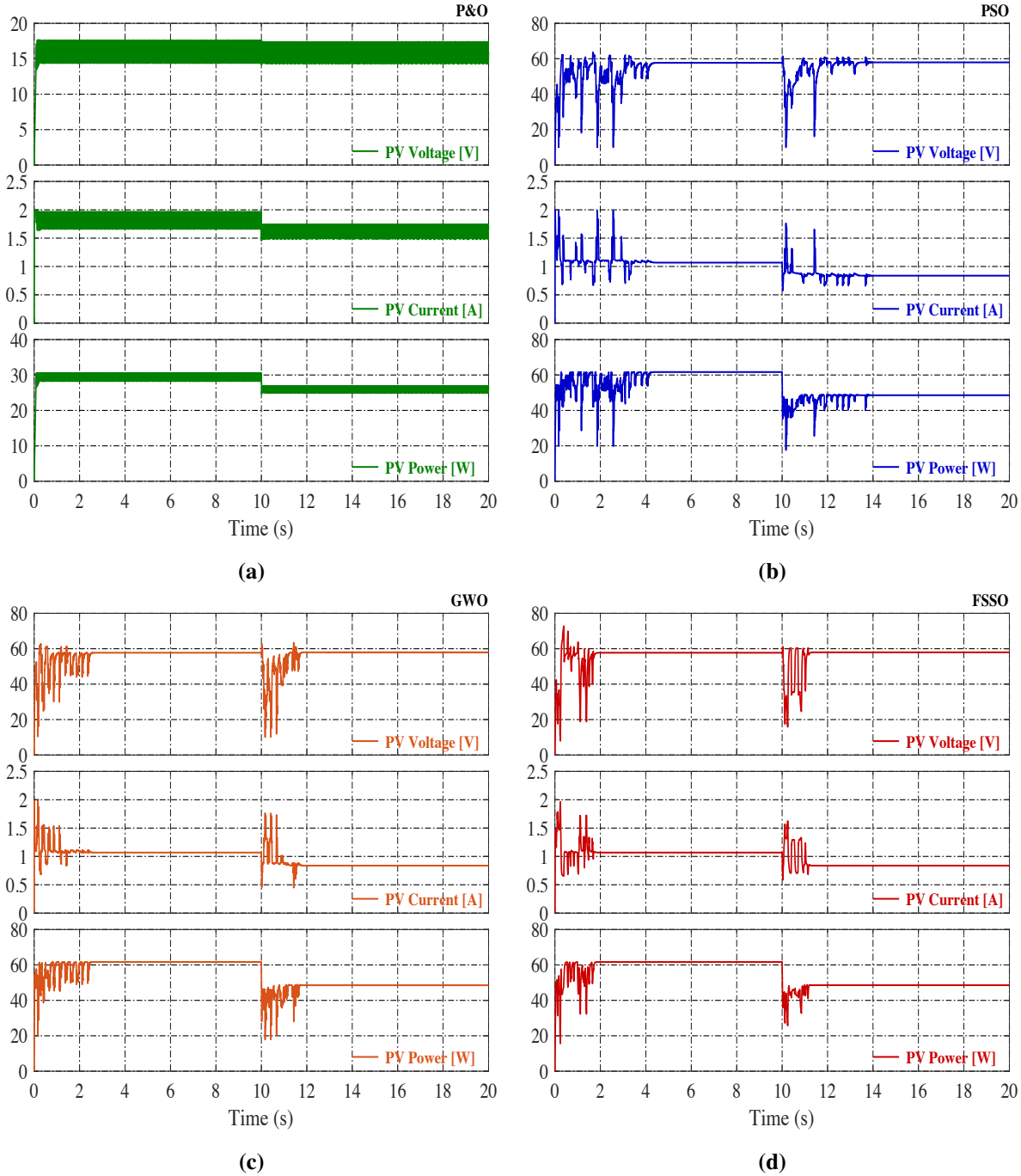


Fig. 6.9: Performance with 4*S* configuration. **(a)** *P&O*. **(b)** *PSO*. **(c)** *GWO*. **(d)** *FSSO*.

inhomogeneous insolation changes to *SP*-8. All the algorithms are reinitialized and the *PSO* locates the *GMPP* of 35.35 W in 4.25 s, the *GWO* finds the *GMPP* of 35.36 W in 2.3 s, the *FSSO* detects the *GMPP* of 35.37 W in 0.3 s, and *P&O* by chance locates the *GMPP* of 34.26 W with oscillations around *MPP* at steady-state. The *P&O* algorithm arrives at the global peak in *SP*-8, but it fails in the case of *SP*-6. It should be noted that the initial values of duty ratio and termination criteria are assumed to be same while comparing *PSO*, *GWO*, and *FSSO* algorithms so that the objectivity in comparison is preserved.

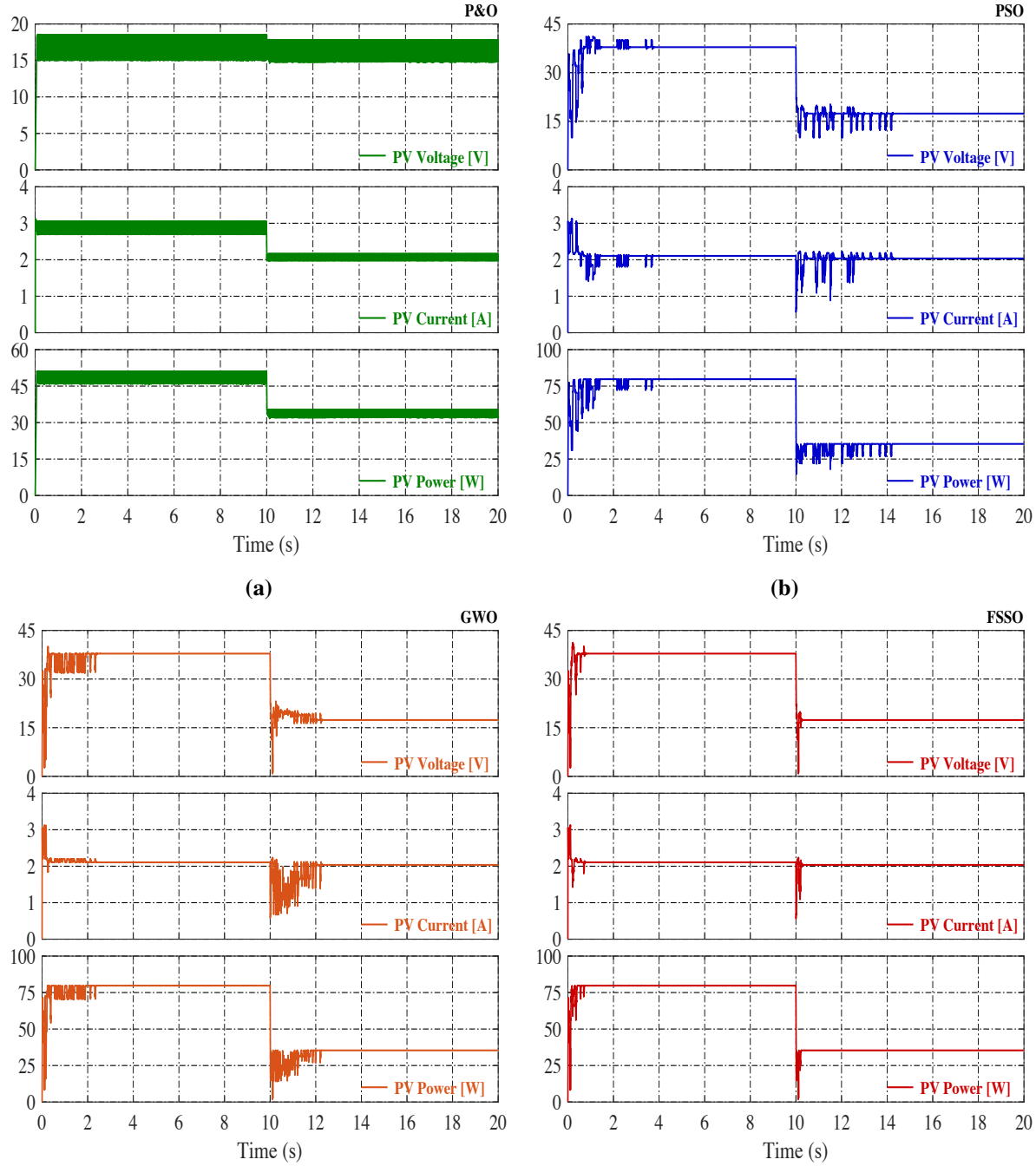


Fig. 6.10: Performance with 2*S*2*P* configuration. **(a)** *P&O*. **(b)** *PSO*. **(c)** *GWO*. **(d)** *FSSO*.

The tracking curves in Figs. 6.9 and 6.10 indicate that the *PSO* and *GWO* based methodology ensures global convergence, though the convergence time is higher. Thus, the power loss during tracking by *PSO* and *GWO* is very high. Furthermore, the perturbations in the *PV* power of the system during *PSO* and *GWO* based search lasts for more duration. In the *P&O* algorithm, the convergence time is low but it fails to recognize the *GMPP* and oscillations in *PV* output power persists during steady-state.

From simulation results shown in Figs. 6.9 and 6.10, it is concluded that the *FSSO* algorithm for *MPPT* can handle *PSC* effectively and it outshines the *P&O*, *PSO*, and *GWO* concerning faster convergence to *GMPP*, faster tracking speed, reduced steady-state oscillations, and higher tracking efficiency. The simulation results of Figs. 6.9 and 6.10 are summarized in Tables 6.3 and 6.4, respectively. The % tracking efficiency mentioned in Tables is calculated as the ratio of average power output from the *PV* system at the steady-state condition and maximum available power from the *PV* system under certain *SP*. From Tables 6.3 and 6.4, it is seen that the *FSSO* based *MPPT* outperforms the other three *MPPT* methods.

Table 6.3. Performance comparison of the proposed *MPPT* method for 4*S* configuration

Shading pattern	Tracking approach	Maximum power (W)	Voltage at *MPP* (V)	Current at *MPP* (A)	Tracking speed (s)	Maximum power from *P–V* curve (W)	Tracking efficiency (%)
SP-2	*P&O*	29.71	16.11	1.851	0.2	61.665	48.18
	PSO	61.61	57.74	1.067	4.3		99.91
	GWO	61.65	57.73	1.068	2.6		99.97
	FSSO	61.66	57.73	1.068	1.8		99.99
SP-3	*P&O*	26.2	15.9	1.653	0.22	48.785	53.71
	PSO	48.58	57.97	0.838	3.9		99.58
	GWO	48.63	57.96	0.839	1.8		99.68
	FSSO	48.65	57.99	0.839	1.3		99.72

Table 6.4. Performance comparison of the proposed *MPPT* method for 2*S*2*P* configuration

Shading pattern	Tracking approach	Average *PV* power (W)	Voltage at *MPP* (V)	Current at *MPP* (A)	Tracking time (s)	Maximum power from *P–V* curve (W)	Tracking efficiency (%)
SP-6	*P&O*	49.31	16.87	2.931	0.16	79.81	61.78
	PSO	79.71	37.85	2.106	3.75		99.88
	GWO	79.73	37.84	2.107	2.4		99.90
	FSSO	79.75	37.85	2.107	0.75		99.93
SP-8	*P&O*	34.26	16.35	2.099	0.2	35.389	96.81
	PSO	35.35	17.37	2.035	4.25		99.89
	GWO	35.36	17.36	2.037	2.3		99.92
	FSSO	35.37	17.37	2.036	0.3		99.95

6.6.3 Performance during load change

To guarantee the efficacy of the proposed *MPPT* algorithm, simulation is also carried out concerning load variation for shading pattern *SP*-6, as shown in Fig. 6.11. The *PV* system is initially operated with a resistive load of 40 Ω. At t = 5 s, the load is changed to 20 Ω, initiating a rapid fall in the PV power, thus the algorithm starts working. At t = 6.25 s, the algorithm finds the *GMPP* successfully. It can be concluded from the result that by varying the load does not inhibit the algorithm from finding the *GMPP*.

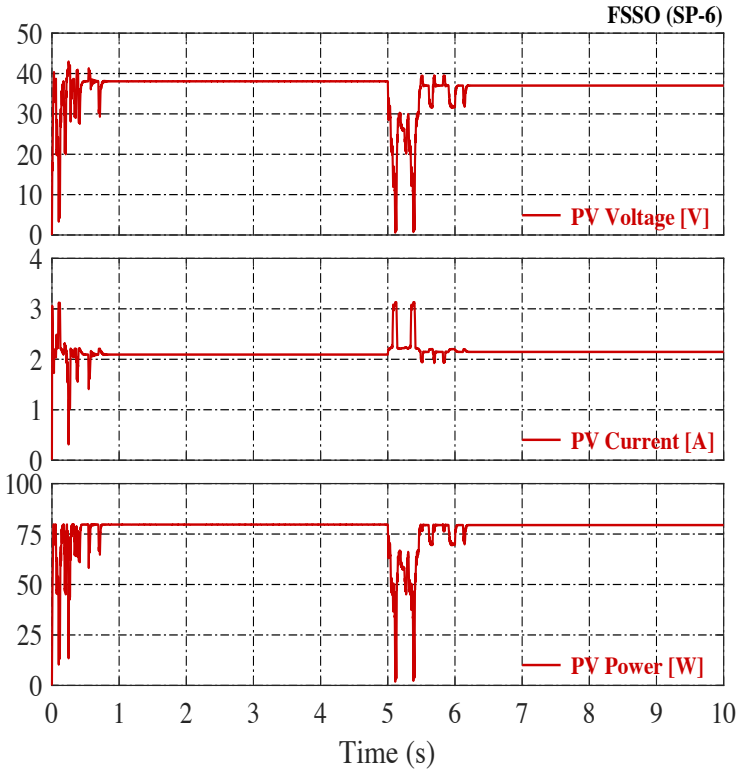


Fig. 6.11: Performance of *PV* system in load change for proposed algorithm.

6.6.4 Effect of change in inductance value

Simulations are also performed to see the effect of decreasing the inductance value of *QZS* network on the % tracking and system efficiency and results are summarized in Table 6.5. Where, % system efficiency is calculated as the ratio of power at the load and the average power from the *PV* system at steady-state. It is found that the % tracking efficiency does not alter as average power remain unaltered while % system efficiency decreases with decrease in inductance value due to high ripple component in the inductor current.

Table 6.5. Effect of change of *QZS* network inductance on % tracking and system efficiency

Shading pattern	Inductance *L* (mH)	Average *PV* power (W)	Load power (W)	System efficiency (%)	Shading pattern	Average *PV* power (W)	Load power (W)	System efficiency (%)
SP-2	1	61.66	59.66	96.76	*SP*-6	79.75	72.66	91.11
	0.9		59.64	96.72			72.65	91.10
	0.8		59.62	96.69			72.64	91.08
	0.7		59.59	96.64			72.63	91.07
	0.6		59.55	96.58			72.61	91.05
	0.5		59.50	96.50			72.59	91.02
SP-3	1	48.65	47.51	97.66	*SP*-8	35.37	28.55	80.72
	0.9		47.49	97.62			28.55	80.72
	0.8		47.47	97.58			28.54	80.69
	0.7		47.44	97.52			28.54	80.69
	0.6		47.41	97.46			28.53	80.66
	0.5		47.34	97.31			28.52	80.63

6.7 LABORATORY SETUP AND EXPERIMENTAL RESULTS

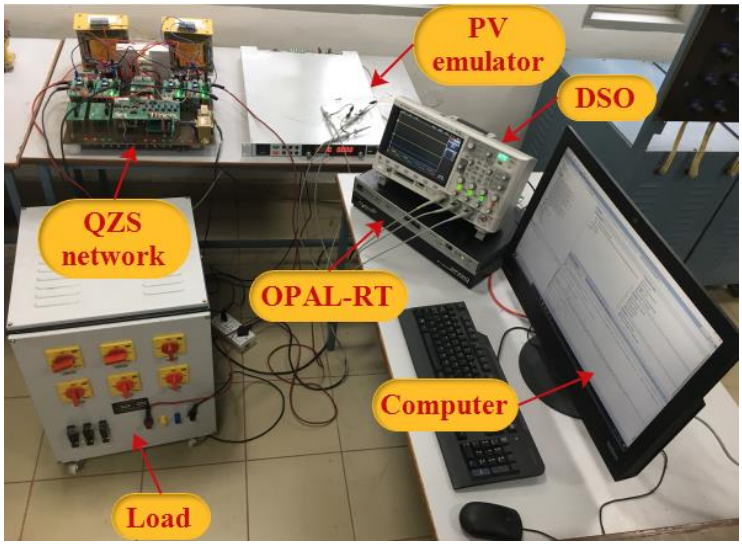


Fig. 6.12: Experimental test rig of proposed system.

The prototyping circuit is developed in the laboratory and the experimental rig is shown in Fig. 6.12. MAGNA-POWER programmable DC power supply (SL1000-6.0/415+HS) is used as a *PV* source to validate the proposed *FSSO* algorithm. Using the "Photovoltaic Power Profile Emulation" function, various *P–V* curves can be programmed to verify the *MPPT* capability of the proposed algorithm. The power from the *PV* simulator is supplied to the load (fixed resistance) by using a DC-DC boost converter (*QZS* converter). Parameters of the *QZS* converter are the same as described for the simulations. IC7840 based voltage sensing circuit is used to sense

v_{PV}. The i_{PV} is sensed using HE055T01 Hall-effect current sensor. Pertaining to a duty ratio, the multiplication of v_{PV} and i_{PV} is carried out by the digital controller to obtain the corresponding *PV* output power. The outputs of the sensors are given to the "analog-to-digital converter" of the "Digital Signal Processor" board. Digital controller OP-4510 from OPAL-RT Technologies comprising Kintex7 FPGA and working with Intel Xeon Quad-Core 3.5 GHz processor is used for executing the *MPPT* algorithm, which generates *PWM* pulses corresponding to each duty ratio (*FS* position) for the power switch of the *QZS* converter. Moreover, the signals (*PV* voltage, *PV* current, and *PV* power) are obtained from OPAL-RT and displayed on *DSO* DSOX2024A, 4-channel, 200 MHz from KEYSIGHT technologies.

6.7.1 4*S* configuration performance

For experimental verification, *PV* curves of *SP*-2 and *SP*-3 for 4*S* configuration are imported to the DC power supply. Each pattern is made to exist for 10 s sequentially. The *PV* voltage, current, and power waveforms, achieved by *P&O*, *PSO*, *GWO*, and *FSSO* algorithms, are shown in Fig. 6.13. The performance difference between all the algorithms is clearly visible from Fig. 6.13.

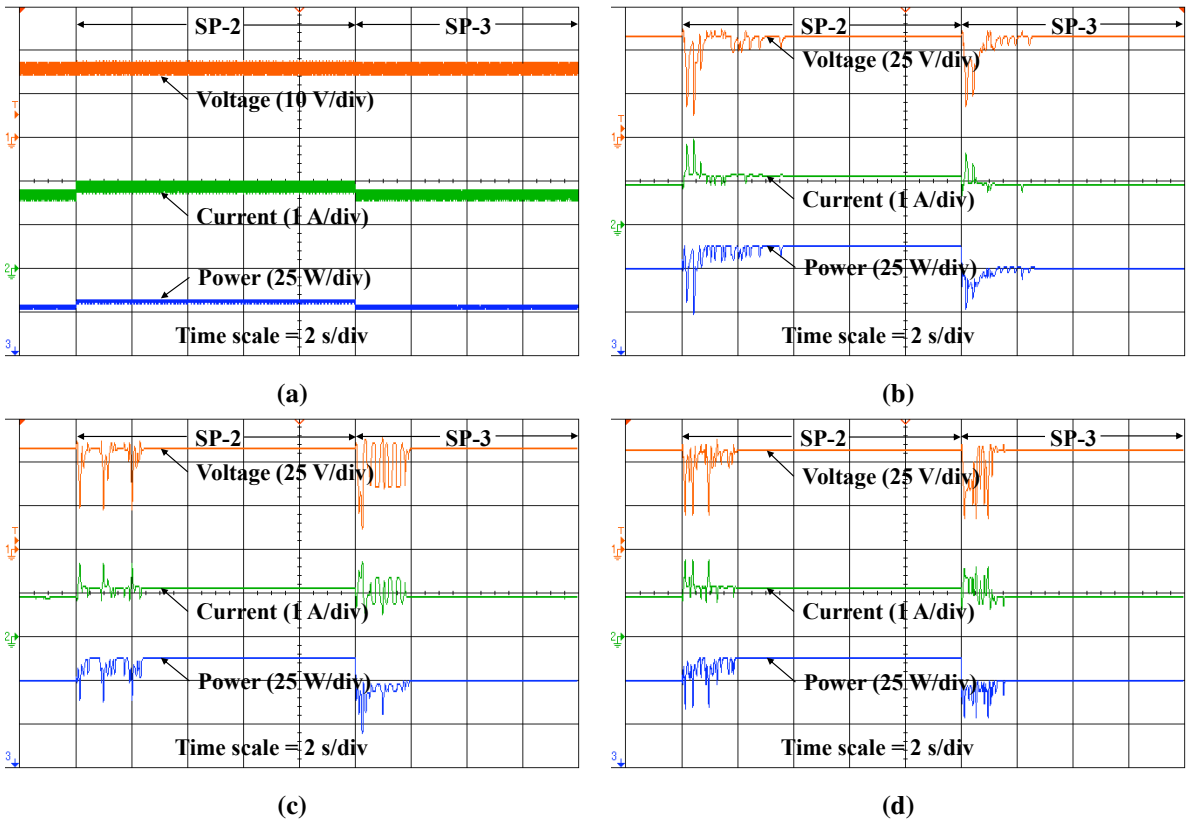


Fig. 6.13: Experimental results of 4*S* configuration for *P–V* curve tracking. **(a)** *P&O*. **(b)** *PSO*. **(c)** *GWO*. **(d)** *FSSO*.

The tracking curve shows that *FSSO*, *PSO*, and *GWO* based *MPPT* converge to the *GMPP* of 61.65 W, whereas *P&O* gets trapped to *LMPP* of 29.7 W resulting in oscillation in steady-state. During *SP*-2, *FSSO* converges quickly and takes almost 47.368% less time in comparison to *PSO* and 16.667% less time in comparison to *GWO*. The tracking time of *PSO*, *GWO*, and *FSSO* during experimentation for the *SP*-2 are 3.8 s, 2.4 s, and 2 s, respectively. When the shading pattern changes from *SP*-2 to *SP*-3, the *MPPT* algorithms are reinitialized. The *FSSO*, *PSO*, and *GWO* based *MPPT* reach *GMPP* of 48.55 W, whereas *P&O* gets trapped to *LMPP* of 26.2 W and is unable to discriminate between *LMPP* and *GMPP*. The tracking time of *FSSO* is 1.6 s, while for *PSO* and *GWO*, it is 2.2 s and 1.9 s, which are 27.273% and 15.789% less, respectively.

6.7.2 2*S*2*P* configuration performance

Now the DC power supply is programmed for the shading patterns *SP*-6 and *SP*-8 of 2*S*2*P* configuration and every pattern is allowed to occur successively for 10 s. Tracking curves for all the *MPPT* algorithms are shown in Fig. 6.14. The *PSO*, *GWO*, and *FSSO* converge to the *GMPP*

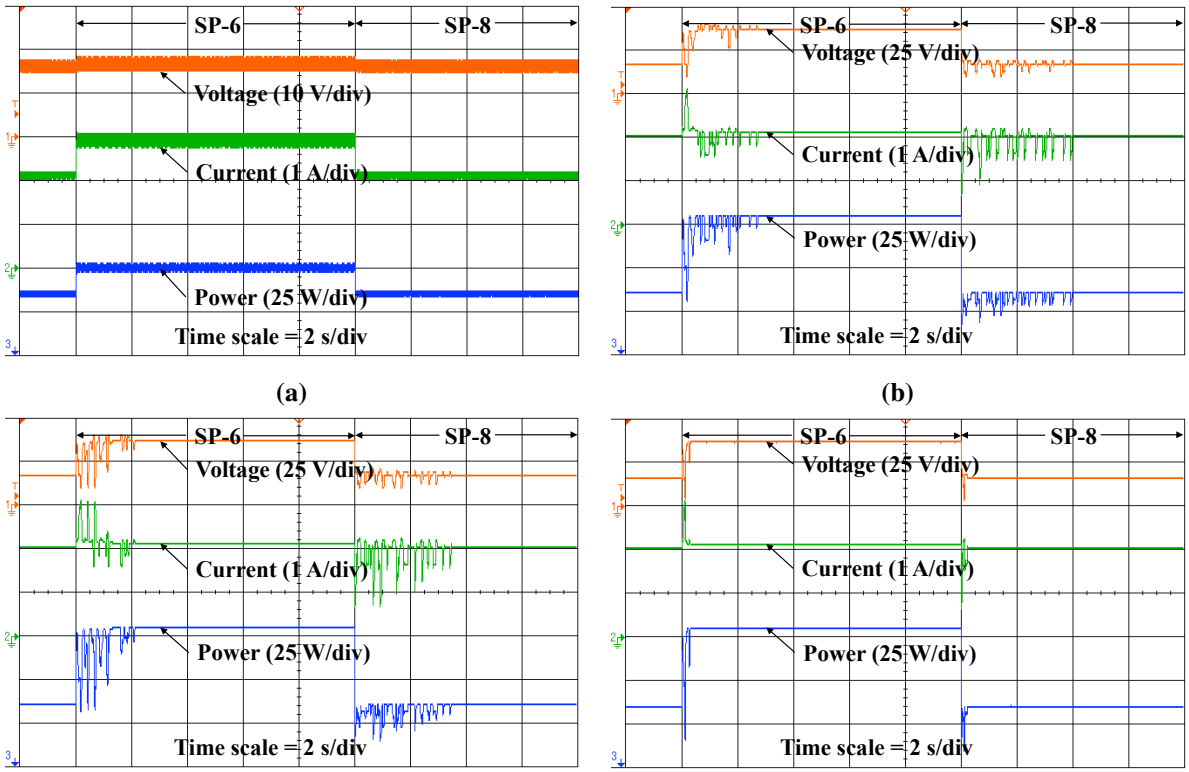


Fig. 6.14: Experimental results of 2*S*2*P* configuration for *P*–*V* curve tracking. **(a)** *P&O*. **(b)** *PSO*. **(c)** *GWO*. **(d)** *FSSO*.

of 79.70 W and *P&O* gets trapped in *LMPP* of 49.31 W causing oscillations in *PV* power at steady-state. *FSSO* converges very quickly and takes almost 88.679% and 86.047% less time duration in comparison to *PSO* and *GWO*, respectively. The tracking time of *PSO*, *GWO*, and *FSSO* during experimentation for *SP*-6 is 2.65 s, 2.15 s, and 0.3 s, respectively. After 10 s, when the shading pattern changes to *SP*-8, once again four algorithms search the *P–V* curve for the new *MPP*. The curves of the proposed *FSSO* based *MPPT*, *PSO* based *MPPT*, and *GWO* based *MPPT* methods converge to *GMPP* of 35.36 W and *P&O* incidentally settles to the *GMPP* 34.26 W while oscillations persist in the *PV* power output. The tracking times of *PSO*, *GWO*, and *FSSO* during experimentation for the partially shaded *PV* array are 4 s, 3.5 s, and 0.22 s, respectively. Thus, the performance of *FSSO* is 94.5% and 93.714% faster w.r.t. *PSO* and *GWO*, respectively.

From Figs. 6.13 and 6.14, it is concluded that the *FSSO* based *MPPT* algorithm outperforms *P&O*, *PSO*, and *GWO* based *MPPT* algorithms for the consideration of tracking efficiency, reduced steady-state oscillations, reduced tracking time, and faster convergence to *GMPP*.

6.7.3 Performance during load change

The experiment is also performed for the change in load under shading pattern *SP*-6 to check the effectiveness of the proposed algorithm and result is shown in Fig. 6.15. Initially, the system is operating with a resistive load of 40 Ω and its value is dropped to 20 Ω suddenly. Thus, power drops immediately and after 0.7 s *FSSO* finds the *GMPP* of 79.70 W. From the experiment, it can be inferred that change in load do not prevent the proposed *MPPT* to find the *GMPP*.

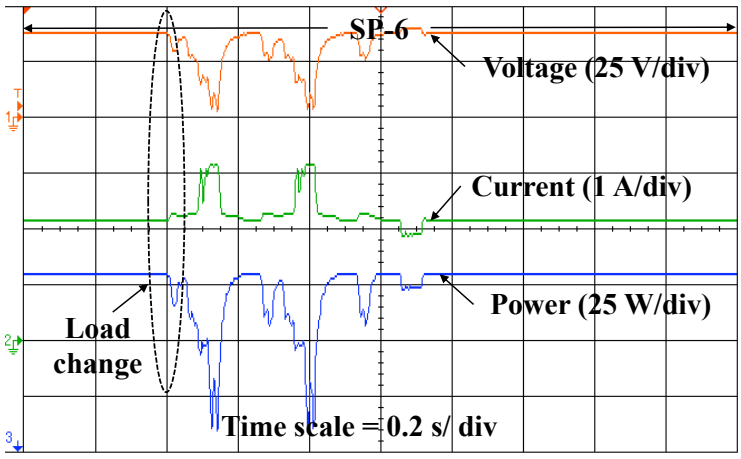


Fig. 6.15: Experimental results of the proposed *FSSO* algorithm under sudden load change.

6.8 CHAPTER SUMMARY

The chapter deals with the implementation of *FSSO* based algorithm for *GMPP* tracking of *PV* system under *PSC*. This algorithm has been adopted to exploit its unique advantage of communication between three classes of hickory tree, acorn tree, and normal tree flying squirrels and corresponding position update in the direction of optimum solution. The technique has been implemented on different *PV* systems having series- and/or parallel- arrangements of *PV* arrays and exposed to *PSC*. The implementation is carried out with *QZS* converter as the power electronic interface and results are validated experimentally and compared with other *MPPT* algorithms namely *P&O*, *PSO*, and *GWO*. The following conclusions are drawn from the investigation:

- The *FSSO* algorithm, which has been realized without the presence of predator, has a faster convergence.
- The presented *FSSO* algorithm always tracks the *GMPP*. The tracking efficiency, defined as the ratio of average power output at steady-state to the maximum available power, is highest for *FSSO* for all the cases under consideration.
- Although the method realization is carried out with *QZS* converter, the method is general and can be implemented with other converter configurations.
- The realization is carried out on *PV* system with different series- and/or parallel-configuration of *PV* arrays; thus, the method can be regarded as system independent.

Chapter–7

Conclusions and Scope for Future Work

7.1 MAIN CONCLUSIONS

The grid interconnection of *PV* system requires a *Power Conditioning Unit* (*PCU*) interface because of the intermittent and wide operating range of solar power. Among various converters, *QZS* inverter is a potential candidate for *PV* system due to no dead time requirement between the switches of the same leg and drawing continuous current from the *PV* source. In comparison to two-level inverters, the *Multi-Level Inverters* (*MLIs*) are advantageous due to the consideration of power quality, switching losses, and filtering requirements. The 3-Φ *NPC-QZS* inverter or *QZS-SC* inverter can be a potential candidate for *PV* applications because of voltage boost and continuous current. The voltage boost capability of *SC* may be helpful in reducing inductor size. Further, to exploit the solar potential, it is desired that the *PV* system is operated at *Global Maximum Power Point* (*GMPP*) during unpredictable partial shading, which causes multiple peaks and potentially downgrades the *PV* system performance.

The scope of work in such areas are identified after extensive literature review and contributions are made through the following studies in this thesis:

1. The control and performance analysis of grid-tied *QZS* inverter.
2. The control and performance analysis of grid-tied *3L NPC-QZS* inverter.
3. An operating principle and controller design of grid-tied *QZS-SC* inverter.
4. An *MPPT* technique based on *FSSO* optimization under *PSC* using the *QZS* converter.

The above studies including the implementation of control schemes are realized under MATLAB/Simulink and experimentally validated using *HIL RTSs* in OPAL-RT and experimentation on a practical setup in the laboratory. The main contributions of each of the above-mentioned study are summarized herewith:

The single-stage strategy to control grid-tied 3-Φ *PV* system based on *QZS* inverter has been investigated in *Chapter-3*. The dynamic models have been established for AC- and DC-sides independently. The *TOIL* and damped-*SOGI* controllers have been designed using frequency domain approach to yield *ZSSE* on DC-side and AC-side, respectively. The performance of the controllers is evaluated for the transients originating from source and grid sides. The performance was also evaluated considering the time-delay in AC- and DC-side control loops. The performance of the presented *TOIL*-damped-*SOGI* controller is also compared with other linear and robust controllers. The following conclusions are drawn from the study:

- The presented method indirectly estimates and controls *PDV* through the voltage across the *QZS* network capacitors. It is regulated to reference value using *TOIL* controller.
- The design of the controllers effectively avoid interference between AC- and DC-side dynamics and also yield *ZSSE*.
- A deteriorated transient response and prolonged settling time were observed with time-delay in control loops.
- The *TOIL* and *PID* controllers lead to underdamped response while *SMC* leads to a highly damped response. At steady-state, *TOIL* and *PID* controllers yield *ZSSE* whereas *SMC* has a non-*ZSSE* response characteristics.
- The transient response of *TOIL* and *PID* is approximately same but switching ripple in *ST* duty ratio are more in *PID* control.
- For the AC-side, damped-*SOGI* tracks sinusoidal command effectively while *PI* controller results in magnitude attenuation/ phase delay.
- The controller design is robust enough to accommodate ±25% of the change in *LC* component values.

Chapter-4 deals with the single-stage strategy to control AC-side current and *PDV* for *3L NPC-QZS* inverter-based 3-Φ grid-tied *PV* system. Mathematical model of the system is presented for both DC- and AC-side and *IDL* and damped-*SOGI* controllers are designed through frequency response approach. A pole is added in the transfer functions to reduce noise in the sensed signals. The effect of *RHPZ* is also minimized for DC-side control loop. The *PWM*

schemes are modified to yield *ST* using the 3rd harmonic injected *MCBC* on the basis of the *POD* and *IPD* methods. The performance of the *IDL*-damped-*SOGI* controller is compared with the *SMC*-damped-*SOGI* controller. The performance of the system is evaluated for change in *WCs* and loading. The following conclusions are drawn from the study:

- The control strategy is effective to regulate *PDV* to reference value and to inject inverter current at *UPF*.
- Pulsating nature of *PDV* is accounted for by its indirect estimation and controlling through the voltage across *QZS* network capacitors.
- The *IDL*-damped-*SOGI* arrangement is found to be effective and resulting in *ZSSE* during steady state and lower transients during the change in *WCs*.
- The controllers are effective to attain fast response, good stability, and *ZSSE*.
- With the considerations of lower *CMV* and zero average neutral point current, the *POD* scheme is found to be better in comparison to *IPD* scheme.

A novel single-stage topology based on *QZS-SC* grid-tied inverter for *PV* system has been presented in *Chapter-5*. The *QZS* network is used in the front end between *PV* and *SC* inverter and the resulted boosted output is fed to *SC* inverter. A two-stage like control structure is used, where DC-link voltage is regulated to reference value using *ST* duty ratio and damped-*SOGI* controller is used to control the inverter current. A multi-carrier level-shifted *PWM* was proposed to synthesize the *5L* line-to-line staircase voltage waveform. The following conclusions are drawn from the study:

- The proposed multi-carrier level-shifted *PWM* technique is effective to facilitate *ST*.
- The *QZS* network between the *PV* and the *SC* inverter provides additional voltage boost and limits the start-up and charging currents.
- The *QZS* network also provides additional control freedom through *ST* duty ratio to regulate the DC-link voltage.
- The *SC* inverter structure reduces the inductor size of the *QZS* network for the same operating conditions.

- The system continues to inject current into the grid at *UPF* even after applying linear/non-linear load on the grid-side.
- The controller is also effective when transients are initiated from input side. The DC-link voltage is persistently maintained at the reference value and *ZSSE* is achieved.
- The design guidelines for active and passive component selection and calculation of voltage/current stresses of switches for the proposed topology.

Chapter-6 deals with the implementation of *FSSO* based algorithm for *GMPP* tracking of *PV* system under *PSC*. This algorithm exploits the unique communication between classes of flying squirrels and correspondingly update the position in direction of optimum solution. The technique has been implemented on different *QZS* based *PV* system having series- and/or parallel- arrangement of *PV* arrays exposed to *PSC*. The results are validated experimentally and compared with other *MPPT* algorithms namely *P&O*, *PSO*, and *GWO*. The following conclusions are drawn from the investigation:

- The *FSSO* algorithm, which has been realized without the presence of predator, has a faster convergence.
- The presented *FSSO* algorithm always tracks the *GMPP* even during the *PSCs*, which is giving rise to multiple peaks. The tracking efficiency in all the test cases is shown to be higher than 99.7%.
- Although the method realization is carried out with *QZS* converter, the method is general and can be implemented with other converter configurations.
- The realization is carried out on *PV* system with different series- and/or parallel-configuration of *PV* arrays, the method can be regarded as system independent.

7.2 SCOPE FOR FUTURE WORK

The research work, an exploration exercise, is a continuous endeavor. The culmination of a research project opens up many more avenues for further research. After successful completion of the Doctoral research work on “Design and Control of Grid Connected Photovoltaic System”, the scope of further research is identified in the following related areas:

- In the thesis, the three-level *QZS* configuration based on both *NPC* and *SC* topologies have been investigated; the work can be extended to higher-level configurations employing *QZS* network.

- In the analysis, the *CMV* has been observed in three-level *NPC-QZS* topology. The *CMV* gives rise to leakage current. The investigation can be extended to accurately monitor and control it.

- The grid-tied configuration of *QZS* inverter has been analyzed for transients due to change in weather condition (input side) and change in load on the grid-side. The investigation can be extended to analyze the performance during fault and ride through capability in actual distribution system.

- The proposed *MPPT* algorithm effectively tracks *GMPP* during partial shading condition for different configurations of *PV* arrays; the investigation has been carried out with stand-alone DC load. There is a scope to investigate the algorithm performance with a grid-tied system.

List of Publications

JOURNAL PUBLICATIONS (SCI/SCIE)

1. Nagendra Singh and Sanjay K. Jain, "TOIL and damped-SOGI control of quasi-Z-source inverter based grid-connected renewable-system," ***Control Engineering Practice***, vol. 90, pp. 267-284, 2019. (Impact factor: 3.193) **[Chapter 3]**
   doi: https://doi.org/10.1016/j.conengprac.2019.07.004

2. Nagendra Singh and Sanjay K. Jain, "A novel strategy for indirect control of peak dc-link voltage of grid-connected qZS inverter fed through renewable energy sources," ***Electrical Engineering***, vol. 102, pp. 611-625, 2020. (Impact factor: 1.180) **[Chapter 3]**
   doi: https://doi.org/10.1007/s00202-019-00897-4

3. Nagendra Singh and Sanjay K. Jain, "Investigation of three-level NPC-qZS inverter-based grid-connected renewable energy system," ***IET Power Electronics***, vol. 13, pp. 1071-1085, 2020. (Impact factor: 2.839) **[Chapter 4]**
   doi: https://doi.org/10.1049/iet-pel.2019.0731

4. Nagendra Singh, Krishna Kumar Gupta, Sanjay K. Jain, Niraj Kumar Dewangan, and Pallavee Bhatnagar, "A flying squirrel search optimization for MPPT under partial shaded photovoltaic system," ***IEEE Journal of Emerging and Selected Topics in Power Electronics***. (Impact factor: 4.728) **[Chapter 6]**
   doi: 10.1109/JESTPE.2020.3024719

COMMUNICATED ARTICLE

1. Nagendra Singh, Krishna Kumar Gupta, and Sanjay K. Jain, "A novel transformerless single-stage 3-phase grid-tied quasi-Z-source switched capacitors based multilevel inverter," communicated in ***IEEE Transactions on Power Electronics***. (Impact factor: 6.373) **[Chapter 5]**

CONFERENCE PUBLICATIONS

1. Nagendra Singh and Sanjay K. Jain, “Single phase Z-source inverter for photovoltaic system,” *2016 7th India International Conference on Power Electronics (IICPE)*, Patiala, 2016, pp. 1-6. **[Chapter 2]**
   doi: 10.1109/IICPE.2016.8079340

2. Nagendra Singh and Sanjay K. Jain, “A review on modulation techniques of Z-source network,” *2016 7th India International Conference on Power Electronics (IICPE)*, Patiala, 2016, pp. 1-6. **[Chapter 2]**
   doi: 10.1109/IICPE.2016.8079344.

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Appendices

Appendix–A

Design Guidelines for LC Component Selection of QZS Network

LC parameters of *QZS* network are calculated by neglecting parasitic components (R_{L} and R_{C}) and using small ripple approximation. For specified current ripples Δi_{L1} and Δi_{L2}, the slopes of inductor currents i_{L1} and i_{L2} during the *ST* period $T_{\mathrm{st}} = D_{\mathrm{st}}T_{\mathrm{s}}$ are obtained from (3.2) as:

$$\frac{\mathrm{d}i_{\mathrm{L1}}}{\mathrm{d}t} = \frac{\Delta i_{\mathrm{L1}}}{\Delta t} = \frac{\Delta i_{\mathrm{L1}}}{D_{\mathrm{st}}T_{\mathrm{s}}} = \frac{V_{\mathrm{PV}} + V_{\mathrm{C2}}}{L_1} \tag{A.1}$$

$$\frac{\mathrm{d}i_{\mathrm{L2}}}{\mathrm{d}t} = \frac{\Delta i_{\mathrm{L2}}}{\Delta t} = \frac{\Delta i_{\mathrm{L2}}}{D_{\mathrm{st}}T_{\mathrm{s}}} = \frac{V_{\mathrm{C1}}}{L_2} \tag{A.2}$$

To maintain the continuous conduction operation of converter, the current ripples Δi_{L1} and Δi_{L2} should be smaller than the average input current I_{PV}, which can be defined as:

$$I_{\mathrm{L1}} = I_{\mathrm{L2}} = I_{\mathrm{PV}} = \frac{P_{\mathrm{PV}}}{V_{\mathrm{PV}}} \tag{A.3}$$

For *MCBC*, *ST* duty ratio D_{st} and modulation index M are related as [20]:

$$D_{\mathrm{st}} = 1 - \frac{\sqrt{3}}{2}M \tag{A.4}$$

Using (3.9), (3.10), and (A.4), the relation between V_{M}, D_{st}, and V_{PV} is written as:

$$V_{\mathrm{M}} = \frac{1}{\sqrt{3}}\frac{(1 - D_{\mathrm{st}})}{(1 - 2D_{\mathrm{st}})}V_{\mathrm{PV}} \tag{A.5}$$

With Δi_{L1} and Δi_{L2}, the ripple factors $r_{\mathrm{i1}}\%$ and $r_{\mathrm{i2}}\%$ are found from (3.6), (A.1), (A.2), (A.3), and (A.5) as:

$$r_{\mathrm{i1}}\% = \frac{\Delta i_{\mathrm{L1}}}{I_{\mathrm{L1}}} = \sqrt{3}\left(\frac{T_{\mathrm{s}}V_{\mathrm{M}}V_{\mathrm{PV}}}{L_1 P_{\mathrm{PV}}}\right)\left(\frac{\sqrt{3}V_{\mathrm{M}} - V_{\mathrm{PV}}}{2\sqrt{3}V_{\mathrm{M}} - V_{\mathrm{PV}}}\right) \tag{A.6}$$

$$r_{i2}\% = \frac{\Delta i_{L2}}{I_{L2}} = \sqrt{3}\left(\frac{T_s V_M V_{PV}}{L_2 P_{PV}}\right)\left(\frac{\sqrt{3}V_M - V_{PV}}{2\sqrt{3}V_M - V_{PV}}\right) \tag{A.7}$$

To maintain Δi_{L1} and Δi_{L2} within the specified limit, L_1 and L_2 are calculated from (A.6) and (A.7) as:

$$L_1 \geq \sqrt{3}\left(\frac{T_s V_M V_{PV}}{r_{i1}\% P_{PV}}\right)\left(\frac{\sqrt{3}V_M - V_{PV}}{2\sqrt{3}V_M - V_{PV}}\right) \tag{A.8}$$

$$L_2 \geq \sqrt{3}\left(\frac{T_s V_M V_{PV}}{r_{i2}\% P_{PV}}\right)\left(\frac{\sqrt{3}V_M - V_{PV}}{2\sqrt{3}V_M - V_{PV}}\right) \tag{A.9}$$

With specified capacitor voltage ripples Δv_{C1} and Δv_{C2}, slope of v_{C1} and v_{C2} during the *ST* period is obtained from (3.2) as:

$$\frac{dv_{C1}}{dt} = \frac{\Delta v_{C1}}{\Delta t} = \frac{\Delta v_{C1}}{D_{st} T_s} = \frac{I_{L2}}{C_1} \tag{A.10}$$

$$\frac{dv_{C2}}{dt} = \frac{\Delta v_{C2}}{\Delta t} = \frac{\Delta v_{C2}}{D_{st} T_s} = \frac{I_{L1}}{C_2} \tag{A.11}$$

For $I_{L1} = I_{L2}$, voltage ripple factors $r_{v1}\%$ and $r_{v2}\%$ are obtained using (3.6), (A.3) (A.5), (A.10), and (A.11) as:

$$r_{v1}\% = \frac{\Delta v_{C1}}{V_{C1}} = \frac{1}{\sqrt{3}}\left(\frac{T_s P_{PV}}{C_1 V_M V_{PV}}\right)\left(\frac{\sqrt{3}V_M - V_{PV}}{2\sqrt{3}V_M - V_{PV}}\right) \tag{A.12}$$

$$r_{v2}\% = \frac{\Delta v_{C2}}{V_{C2}} = \left(\frac{T_s P_{PV}}{C_2 V_{PV}}\right)\left(\frac{1}{2\sqrt{3}V_M - V_{PV}}\right) \tag{A.13}$$

Using (A.12) and (A.13), the capacitances C_1 and C_2 are calculated as:

$$C_1 \geq \frac{1}{\sqrt{3}}\left(\frac{T_s P_{PV}}{r_{v1}\% V_M V_{PV}}\right)\left(\frac{\sqrt{3}V_M - V_{PV}}{2\sqrt{3}V_M - V_{PV}}\right) \tag{A.14}$$

$$C_2 \geq \left(\frac{T_s P_{PV}}{r_{v2}\% V_{PV}}\right)\left(\frac{1}{2\sqrt{3}V_M - V_{PV}}\right) \tag{A.15}$$

For input voltage range of 100 V to 200 V and grid voltage (phase-neutral) as 120 V, the maximum required *ST* duty ratio of the *QZS* inverter can be determined using (A.5) as:

$$D_{st} = \frac{\sqrt{3}V_M - V_{PV}}{2\sqrt{3}V_M - V_{PV}} = 0.398$$

The *QZS* network parameters are determined from (A.8), (A.9), (A.14), and (A.15). Correspondingly, the *QZS* network parameters for the 3 kW system, inductor current ripple factors r_{i1}% and r_{i2}% as 20%, and capacitor voltage ripple factors r_{v1}% and r_{v2}% as 1%, are:

$$L_1 = L_2 \geq 1.95 \text{ mH}$$

$$C_1 \geq 406 \ \mu\text{F}$$

$$C_2 \geq 615 \ \mu\text{F}$$

Thus, L and C are selected as 2 mH and 1000 μF, respectively.

Appendix–B

Design Guidelines for LC Component Selection of 3L QZS Network

Calculation for inductor and capacitor of *QZS* network is carried out by neglecting parasitic component of *LC* and using small ripple approximation on network variables.

The value of inductor is calculated based on the predefined current ripple Δi_{L1}. The slope of indcutor current waveform during *ST* period $T_{\mathrm{st}} = D_{\mathrm{st}}T_{\mathrm{s}}$ is given from (4.2) as:

$$\frac{\mathrm{d}i_{\mathrm{L1}}}{\mathrm{d}t} = \frac{\Delta i_{\mathrm{L1}}}{\Delta t} = \frac{\Delta i_{\mathrm{L1}}}{D_{\mathrm{st}}T_{\mathrm{s}}} = \left(\frac{V_{\mathrm{PV}} + 2V_{\mathrm{C2}}}{2L}\right) \tag{B.1}$$

To maintain *CCM* operation of converter, the current ripple Δi_{L1} should be smaller than average *PV* current I_{PV}. Then I_{PV} is defined as:

$$I_{\mathrm{L1}} = I_{\mathrm{PV}} = \frac{P_{\mathrm{PV}}}{V_{\mathrm{PV}}} \tag{B.2}$$

During *CCM* with predefined current ripple, the ripple factor $r_{\mathrm{i}}\%$ is found from (4.6), (A.5), (B.1), and (B.2) as:

$$r_{\mathrm{i}}\% = \frac{\Delta i_{\mathrm{L1}}}{I_{\mathrm{L1}}} = \frac{\sqrt{3}}{2}\left(\frac{T_{\mathrm{s}}V_{\mathrm{M}}V_{\mathrm{PV}}}{LP_{\mathrm{PV}}}\right)\left(\frac{\sqrt{3}V_{\mathrm{M}} - V_{\mathrm{PV}}}{2\sqrt{3}V_{\mathrm{M}} - V_{\mathrm{PV}}}\right) \tag{B.3}$$

To maintain inductor current ripple within the specified limit, inductance is calculated from (B.3) as:

$$L \geq \frac{\sqrt{3}}{2}\left(\frac{T_{\mathrm{s}}V_{\mathrm{M}}V_{\mathrm{PV}}}{r_{\mathrm{i}}\%P_{\mathrm{PV}}}\right)\left(\frac{\sqrt{3}V_{\mathrm{M}} - V_{\mathrm{PV}}}{2\sqrt{3}V_{\mathrm{M}} - V_{\mathrm{PV}}}\right) \tag{B.4}$$

To find C_2 and C_4 with defined capacitor voltage ripple Δv_{C2}, slope of v_{C2} waveform during *ST* period is given from (4.2) as:

$$\frac{\mathrm{d}v_{\mathrm{C2}}}{\mathrm{d}t} = \frac{\Delta v_{\mathrm{C2}}}{\Delta t} = \frac{\Delta v_{\mathrm{C2}}}{D_{\mathrm{st}}T_{\mathrm{s}}} = \frac{I_{\mathrm{L1}}}{C_2} \tag{B.5}$$

Using (4.6), (A.5), (B.2), and (B.5), voltage ripple factor $r_{v2}\%$ is written as:

$$r_{v2}\% = \frac{\Delta v_{C2}}{V_{C2}} = 2\left(\frac{T_s P_{PV}}{C_2 V_{PV}}\right)\left(\frac{1}{2\sqrt{3}V_M - V_{PV}}\right) \tag{B.6}$$

Capacitance C_2 and C_4 are calculated from (B.6) as:

$$C_2 = C_4 \geq 2\left(\frac{T_s P_{PV}}{r_{v2}\% V_{PV}}\right)\left(\frac{1}{2\sqrt{3}V_M - V_{PV}}\right) \tag{B.7}$$

To find C_1 and C_3 with defined capacitor voltage ripple Δv_{C1}, slope of v_{C1} waveform during *ST* period is given from (4.2) as:

$$\frac{\mathrm{d}v_{C1}}{\mathrm{d}t} = \frac{\Delta v_{C1}}{\Delta t} = \frac{\Delta v_{C1}}{D_{st} T_s} = \frac{I_{L2}}{C_1} \tag{B.8}$$

Taking average inductor currents to be equal, i.e. $I_{L1} = I_{L2}$, voltage ripple factor $r_{v1}\%$ is written using (4.6), (A.5), (B.2), and (B.8) as:

$$r_{v1}\% = \frac{\Delta v_{C1}}{V_{C1}} = \frac{2}{\sqrt{3}}\left(\frac{T_s P_{PV}}{C_1 V_M V_{PV}}\right)\left(\frac{\sqrt{3}V_M - V_{PV}}{2\sqrt{3}V_M - V_{PV}}\right) \tag{B.9}$$

Finally, value of capacitances C_1 and C_3 is obtained from (B.9) as:

$$C_1 = C_3 \geq \frac{2}{\sqrt{3}}\left(\frac{T_s P_{PV}}{r_{v1}\% V_M V_{PV}}\right)\left(\frac{\sqrt{3}V_M - V_{PV}}{2\sqrt{3}V_M - V_{PV}}\right) \tag{B.10}$$

For input voltage range of 100 V to 200 V and grid voltage (phase-neutral) as 100 V, the maximum required *ST* duty ratio of the *QZS* inverter can be determined using (A.5) as:

$$D_{st} = 0.372$$

The *QZS* network parameters are determined from (B.4), (B.7), and (B.10). Correspondingly, the *QZS* network parameters for the 3 kW system, inductor current ripple factors $r_i\%$ as 20%, and capacitor voltage ripple factors $r_{v1}\%$ and $r_{v2}\%$ as 1%, are:

$$L_1 = L_2 = L_3 = L_4 \geq 759\ \mu\mathrm{H}$$

$$C_1 = C_3 \geq 911\ \mu\mathrm{F}$$

$$C_2 = C_4 \geq 1.54\ \mathrm{mF}$$

Thus, L and C are selected as 1 mH and 3000 μF, respectively.