Study of 3C-SiC Lateral Double Diffusion MOSFET For Current Enhancement Based On Fixed Oxide Charge Inside SiO_2 Layer.

A Thesis submitted in partial fulfillment of the requirements for the award of degree of

Master of Technology

in

VLSI Design & CAD

Submitted By

Meenal Bansal

Roll No: 600861028

Under the guidance of

Dr. A.K Chatterjee

Professor & Head, ECED

ELECTRONICS AND COMMUNICATION ENGINEERING DEPARTMENT

THAPAR UNIVERSITY

PATIALA-147004

JULY, 2010

CERTIFICATE

I hereby certify that the work which is being presented in the thesis entitled "**Study Of 3C-SiC Lateral Double Diffusion MOSFET For Current Enhancement Based On Fixed Oxide Charge Inside SiO_2 Layer**" in partial fulfillment of requirement for award of degree of **Master of Technology** in **VLSI Design & CAD** from **Thapar University**, is an authentic record of my own work carried under the supervision and guidance of **Dr. A.K.Chatterjee**, Professor and Head, Electronics & Communication Engineering department, Thapar University, Patiala.

The matter presented in this thesis has not been submitted in any other university or institute for the award of any other degree.

Meenal.

MEENAL BANSAL

Roll No: 600861028

It is certified that the above statement made by the candidate is correct to the best of my knowledge and belief.

Place: Patiala.

Date: 12.7.10.

Dr. A.K.CHATTERJEE

Supervisor

Professor & Head (ECED)

Thapar University

12.7.10.

Dr. A.K.CHATTERJEE

Professor & Head(ECED)

Thapar University

Patiala-147004

Counter signed by:

16.7.10

Dr.R.K.SHARMA

Dean of Academic Affairs

Thapar University

Patiala-147004

ACKNOWLEDGEMENT

First of all, I would like to express my gratitude to **Dr. A. K. Chatterjee,** Professor & Head, Electronics and Communication Engineering Department, Thapar University, Patiala for his patient guidance and support throughout the year. I am truly very fortunate to have the opportunity to work with him. I found his guidance to be extremely valuable.

I am also thankful to our PG Coordinator, **Mrs. Alpana Agrawal,** Assistant Professor, Electronics and Communication Engineering Department, entire faculty and staff of Electronics and Communication Engineering Department. I wish to thank all my friends who devoted their valuable time and helped me in all possible ways towards successful completion of this work. I thank all those who have contributed directly or indirectly in the completion of my thesis, especially Mr. Surjeet Singh, student of M.E, ECED who has helped in using the tool, MATLAB.

Lastly, I would like to thank my parents for their years of unyielding love and encourage.

Meenal .

Meenal Bansal

Roll No. 600861028

ABSTRACT

The fast growing market for semiconductor devices and the high costs for fabricating the devices give rise to ongoing miniaturization. Advances in process technology demands on the electrical and thermal characteristics of the devices leading to complex structures.

The entrance of SiC devices in the market has enormously improved energy efficiency in a wide range of industries, including lighting, electronics and telecommunications. It allows components to operate at substantially higher temperatures, voltages and power levels than silicon. This translates into smaller, lighter, simpler electrical systems. High avalanche breakdown field (1.0 – 3.0MV/cm), high thermal conductivity (5W/cm-^{o}C) and high electric field strength for SiC makes it alternative material for high voltage, high power devices.

For 3C-SiC Lateral Double Diffusion MOSFET, different parameters such as flat band voltage, bulk potential, mobility, body-effect term, transconductance etc. which depend on the doping concentration of the device are calculated and their variation with doping concentration is plotted. It was found that the electron mobility decreases with increase in doping concentration. However, it was noticed that the flat band voltage and bulk potential showed an increment with increase in the doping concentration.

The I-V characteristics of LDMOS is obtained excluding the effect of fixed oxide charge in SiO_2 layer. Furthermore, the effect of fixed oxide charge on flat band voltage is studied and a new approach to enhance the drain current is presented. The current in the device was found to increase due to reduction in flat band voltage, from 0.26A to 3A if fixed oxide charge is 6.76×10^{-8} Coulombs and doping concentration= $10^{15}cm^{-3}$ and from 0.035A to 0.044A if fixed oxide charge is 6.76×10^{-8} Coulombs and doping concentration = $10^{17}cm^{-3}$.

CONTENTS

List of Figures

List of Tables

Notation

Symbol	Description
C_{ox}	Oxide capacitance
E_c	Critical electric field
E_i	Intrinsic Fermi level
E_F	Fermi energy level at equilibrium
E_g	Energy band gap
E_v	Energy valence band
fcc	Face centered cubic
k	Boltzmann constant
p_{po}	Hole concentration in p-type substrate
n_{po}	Electron concentration in p-type substrate
N_B	Doping concentration
V_{SB}	Substrate bias voltage
V_{FB}	Flat band voltage
V_{DS}	Drain to source voltage
V_{GS}	Gate to source voltage
V_{Dsat}	Drain to source saturation voltage
V_B	Breakdown voltage
V_t	Threshold voltage
$R_{on,sp}$	Specific on resistance
N_{ox}	Oxide interface fixed charge density
N_{ref}	Reference doping concentration
μ	Mobility
ε_S	Permittivity of semiconductor

ε_o	Permittivity of free space
ψ_S	Surface potential
Ψ_B	Bulk potential
ϕ_m	Metal work potential
χ	Electron affinity of semiconductor
γ	Body effect term
Q_f	Fixed oxide charge
Q_{ot}	Oxide trapped charge
Q_{it}	Interface trapped charge
ϕ_{ms}	Work function difference between metal and semiconductor
β_o	Transconductance parameter
ϕ_F	Bulk Fermi potential
T	Temperature
q	Electronic charge
n_i	Intrinsic carrier concentration
α	Fitting parameter
δ	Fitting parameter

List of used Acronym

ACCUFET	Accumulation Channel MOSFET
CMOS	Complementary Metal-Oxide-Semiconductor
CVD	Chemical Vapor Deposition
DMOS	Double Diffused Metal-Oxide-Semiconductor
ECSCRM	European Conference on Silicon Carbide and Related Materials
IGBT	Insulated Gate Bipolar Transistor
ICSCRM	International Conference on Silicon Carbide and Related Materials
IMPATT	Impact Ionization Avalanche Transit Time
I-V	Current –Voltage
LDMOS	Lateral Double Diffused MOSFET
LPE	Liquid Phase Epitaxy
MIS	Metal-Insulator-Semiconductor
MOS	Metal-Oxide-Semiconductor
MOSFET	Metal-Oxide-Semiconductor-Field-Effect-Transistor
SiC	Silicon Carbide
VDMOS	Vertical Double Diffused MOSFET
VLSI	Very Large Scale Integration

CHAPTER-1
INTRODUCTION

Perhaps we have never thought about it, but Silicon devices have changed our life forever. When we look back in our recent evolution, only a few technological advances have been so decisive. The first big changes in people's lives and ideas began to occur only about 10,000 years ago. The Neolithic Revolution changed the way humans daily lived their nomadic lives creating a consistent food source, new materials and new tasks. 5000 years ago, the rise of the writing in the Middle East civilizations allows the efficient transmission of knowledge from one generation to the next. Science and philosophy spring from this simple achievement. Another simple advance will provoke the next revolution, the printing press. The process was developed independently in China and Europe. Before the invention of printing, multiple copies of a manuscript had to be made by hand, a laborious task that could take many years. Printing made it possible to produce more copies in a few weeks than formally could have been produced in a life time by hand. Invented by Gutenberg in 1450, the printing press made the mass publication and circulation of ideas and literature possible. Since then, the technological and scientific achievements have been countless. In the last decades of the last century arises the small but with great impact last breakthrough, the transistor. The transistor is on the basis of the last great change: THE GLOBAL DIGITAL REVOLUTION.

1.1 Motivation

As hundreds of thousands of interconnected tiny polyps make up a colossal coral colony, transistors are the base of computers and innumerable electronic devices. Computers are connected in a global network around the world. The information available is now almost infinite and immediate; the sources are innumerable and plural. Nothing will be the same, this is our revolution. There is nothing more abundant than transistors fabricated for men on earth. The most of these transistors are made of silicon, and are metal oxide semiconductor devices (MOSFETS) that is a sort of sandwich made up with Silicon, Silicon dioxide (SiO_2, generally known as gate dielectric or gate oxide) and a metal. The great success of the digital technology seems to indicate that silicon is the most suitable material for this issue. However, silicon is a mediocre material for electronics applications. There are a number of

potential semiconductors that improve the performances of Silicon. Hence, where lies the success of Silicon as the material of the digital revolution? There are two main technological and one economic reason for the overwhelming Silicon predominance:

i. The capability to grow large area wafers with controlled doping properties and very low residual defect density.
ii. Its insulator native oxide: SiO_2.
iii. Its abundance and low cost.

Silicon is an ordinary semiconductor, but SiO_2 is one of the best insulators that are known. It can be argued that the key element enabling the scaling of the Silicon based metal-oxide-semiconductor is the material properties associated with the dielectric employed. The use of amorphous, thermally grown SiO_2 offers several key advantages in microelectronic processing including a stable (thermodynamically and electrically), high quality Si-SiO_2 interface as well as superior electric isolation properties.

There is now considerable evidence of the need for a semiconductor technology which exceeds the limitations imposed by silicon across a wide spectrum of industrial applications. Examples range from in-engine sensors and controls for automotive and aerospace sectors to electronic system for power transmission and distribution. Wide band gap semiconductor, such as Silicon carbide (SiC), Gallium nitride (GaN) and diamond, offer the potential to overcome both the temperature and voltage blocking limitations of Si. They are expected to play critical roles in applications for well logging, aerospace, automotive and other industrial sectors. The gradual emergence of wide band gap semiconductor technology in these areas not only will greatly improve device and system performances, but will also reduce maintenance costs due to improved reliability.

On the other hand, SiC is proving to be the most attractive candidate, offering significant potential advantages at both high temperature and high voltage levels whilst benefiting from tractable material technology. Moreover, SiC is the only material that can be thermally oxidized to form a high quality native oxide (SiO_2), which enables the fabrication of MOS based devices. Although SiC offers substantial advantages over Si, it is still immature as a semiconductor material. Recently, new breakthroughs in the fields of material growth and of technological processes have

been proposed, which will boost the development of SiC microelectronic devices and its industrial production. Concretely, production of high quality material on large area wafers (4") is now possible. However, single crystal wafers of SiC have only been commercially available since around 1990 and a number of critical material and processing issues are still under active investigation. These investigation fields include activation of ion implanted impurities, formation of thermally stable contacts, reliable and controllable etching techniques, and especially high quality dielectric films suitable for MOS devices.

In recent years, the activity in silicon carbide (SiC) has considerably increased due to the need for electronic devices capable of operation at high power levels and high temperatures. With its very high thermal conductivity (~5.0 W/cm), high saturated electron drift velocity (~2.7× 10^7 cm/s) and high breakdown electric field strength (~3 MV/cm), SiC is a material of choice for high temperature, high voltage, high frequency and high power applications. There exist a number of power MOSFETs such as vertical MOSFET, U-MOSFETs, IGBTs and lateral diffusion MOSFET. There is a broad spectrum of applications for high-voltage lateral double diffused MOS(LDMOS) transistors in automotive and industrial electronics, computer peripheral appliance, telecommunication circuits, high end audio amplifiers and other markets with voltage requirements in the range of 20-150V and switching relatively large currents(2-10A).

In this thesis work, a method of improving the output current is being proposed by taking into account the effect of fixed oxide charge trapped in SiO_2 layer, on the flat band voltage.

1.2. Outline of the thesis

Chapter-1 introduces the reader to the world of silicon, gives the limitations imposed by silicon across a wide spectrum of applications and further suggests the new material, Silicon Carbide.

Chapter-2 starts with the physical and electrical properties of SiC, The chapter also surveys the SiC material growth, SiC technology, its polytypes (3C, 4H, 6H etc), properties and its applications.

Chapter-3 starts with explaining Lateral diffusion MOSFETs, its working, properties and applications.

Chapter-4 presents the device equation of LDMOSFET and variation of mobility, bulk potential and flat band voltage with respect to the doping concentration. It also presents the I-V characteristics of LDMOSFET without taking into account the effect of fixed oxide charge on the flat band voltage.

Chapter-5 presents the calculations of flat band voltage and VD_{sat}. It then presents the improvement in the drain current, I_{DS} by considering the effects of fixed oxide charge in the SiO_2 layer.

Chapter-6 includes conclusion and further improvement which is possible.

CHAPTER-2
SILICON CARBIDE – MATERIALS AND DEVICES

Silicon Carbide (SiC) is a wide band gap semiconductor with specific electrical properties such as a high breakdown electric field, a high thermal conductivity and a high inertness. Recently, new breakthroughs in the fields of material growth and of technological processes have been proposed [1], which will boost the development of SiC microelectronic devices and its industrial production. Concretely, production of high quality material on large area wafers is now possible, allowing the fabrication of reliable high temperature, high frequency or high current power electronic devices, improving the already optimized Silicon based structures. SiC devices possess a very wide range of industrial applications, such as spacecraft, aircraft, automobile, communication or energy distribution, among others. Therefore, SiC devices are expected to play a fundamental role, in normal life and in the cutting edge investigations, for high current/voltage management or harsh environments in the 21st century. An additional advantage of SiC is that among compound semiconductors, only SiC can be thermally oxidized to grow insulating, high quality SiO_2 layers. These insulating layers are of paramount importance in nearly all the SiC applications described below. The breakdown field in SiC is about 8 times higher than in silicon. This is important for high-voltage power switching transistors. For example, a device of given size in SiC will have a blocking voltage 8 times higher than the same device in silicon. More importantly, the on-resistance of the SiC device will be about 100 times lower than the silicon device [2].

2.1. Brief history of SiC

Silicon-based power devices have long dominated the power electronics and power systems applications. Devices such as bipolar, unipolar, controlled, uncontrolled, and MOS-gated made by Si are widely used by power electronics and power systems designers.

Silicon Carbide (SiC) was discovered in 1824 by the Swedish scientist Jons Jacob Berzelius, who received part of his education at Linkoping. SiC is also known as carborundum or moissanite, in natural form it is found in meteorites. At that time the properties of SiC were not understood. It was not until the invention of the electric

smelting furnace by E. H. & A. H. Cowles and its application to carbonaceous compounds by Acheson that the interest in SiC came into focus. The purpose of Acheson's invention was to produce a material substituting diamond and other abrasive materials for cutting and polishing purposes. The crystalline products Acheson found after the process were characterized by a great hardness, refractabiliy and infusibility. He called the product 'carborundum' and described it as silicide of carbon with the chemical formula SiC. The invention had a great impact and much material was produced using this process mainly for cutting and abrasive purposes. Shortly afterwards the electronic properties of SiC started to be investigated. The first Light Emitting Diode (LED) was made from SiC in 1907. In 1955, Lely[3] presented a new concept of growing high quality crystals. The research in SiC became more intensified after this and the first SiC conference was held in Boston 1958. The success and rapid increase of the Si technology made, however, that the interest in SiC dropped. Research during this time (mid '60 to '70) was mainly carried out in the former Soviet Union. In the West, some research in SiC was still maintained in this time. In the year 1978 a discovery of comparable dimension and importance as the Acheson process was presented by Tairov and Tsvetkov[4]. They discovered a way to produce substrates by a seeded sublimation growth. Due to this discovery the SiC technology gained new speed. The possibility to grow single crystal SiC on Si substrates which was invented by Matsunami et. al. in 1981 was an important milestone not so much technologically but more as a further 'temperature increase' in the SiC field. In 1987, Cree Research was founded which became the first and is, at present, the only company selling substrates of SiC. Limitations of the Si technology and the III/V technology have further increased the interest in SiC and at present the field is growing rapidly much owing to the recent commercial availability of substrates.

Nowadays, the commonly used method to grow SiC epitaxial layers is chemical vapor deposition (CVD) [5]. It provides good structural quality and excellent doping control, however it suffers from low growth rates of about 3-5 μm/hour, thus growth of very thick layers is time consuming and creates a need for long-term process control.

Due to the increased interest that SiC received, series of conferences was introduced, such as the International Conferences on Silicon Carbide and Related Material

(ICSCRM) and the European Conferences on Silicon Carbide and related Materials (ECSCRM). The rapid growth in SiC research is reflected in the number of contributions, which increased from 28 at the first ICSCRM conference held in Washington, D.C. in 1987 (by that time called as First International Conference on Amorphous and Crystalline Silicon Carbide and related Materials) to 430 at the latest one in Lyon, France 2003, making this conference the largest meeting of its kind worldwide.

The need for faster devices with high voltage and high switching frequency capability is growing, Silicon-based devices are not able to meet these requirements without costly cooling systems, so Wide band-gap based semiconductor devices such as silicon carbide and gallium nitride offer multiple advantages for power electronic designers. The superior physical properties of these semiconductors offer a lower intrinsic carrier concentration (10-35 orders of magnitude), a higher electric breakdown field (4-20 times), a higher thermal conductivity (3-13 times), a larger saturated electron drift velocity (2-2.5 times) which is suitable for faster devices with high voltage and high switching frequency.

2.2. Physical and electrical properties of SiC

SiC occurs in many different crystal structures, called polytypes [5]. Despite the fact that all SiC polytypes chemically consist of 50% carbon atoms covalently bonded with 50% silicon atoms, each SiC polytype has its own distinct set of electrical properties. While there are over 170 known polytypes of SiC, only a few are commonly grown in a reproducible form acceptable for use as an electronic semiconductor. The most common polytypes of SiC presently being developed for electronics are the cubic 3C-SiC, the hexagonal 4H-SiC and 6H-SiC, and the rhombohedral 15R-SiC. These polytypes are characterized by the stacking sequence of the biatom layers of the SiC structure.

Fig. 2.1 shows the layer structure of SiC (the [0001] direction) with the tetrahedrally bonded carbon atoms linked to three Si atoms within the bilayer and having a single bond linked to a Si atom in the layer below. If we consider the locations of the carbon atoms within a bilayer these form a hexagonal structure, labeled "A" in the Figure. The next bilayer then has the option of positioning its carbon atom in the "B" or the "C" lattice sites. It is this stacking sequence that determines the material polytype.

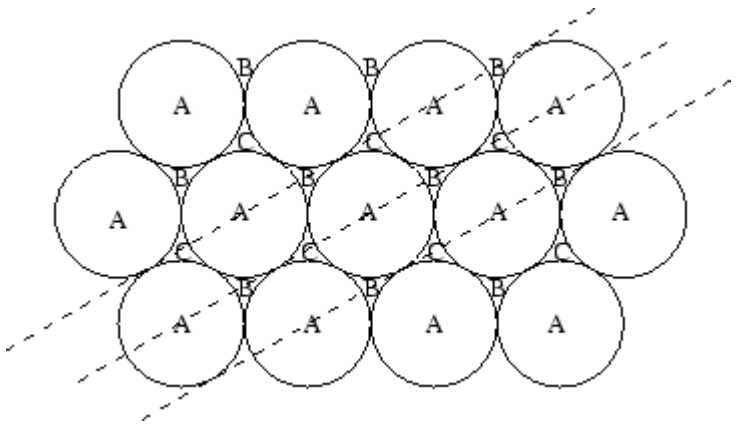


Fig: 2.1: site locations for C atoms in the [1100] plane. [6]

Silicon carbide is the only stable binary compound of silicon and carbon existing in a solid phase. It crystallizes in three bravais lattices [7]:

- Close packed cubic (zinc blende structure)
- Hexagonal (wurtzite structure)
- Rhombohedral

The ion (12%) – covalent (78%) bonding of Silicon ($1s^2 2s^2 2p^2 3s^2 3p^2$) and carbon ($1s^2 2s^2 2p^2$) atoms is tetrahedral with a binding energy of 5eV. In real space, each Bravais lattice corresponds to two interpenetrating sublattices of silicon and carbon atoms. The material exhibits the phenomenon of polytypism, which refers to one dimensional polymorphism, i.e. the existence of geometrically different stacking of the basic structural elements: the {111} Si-C bilayers of cubic structure or the equivalent {0001} layers of the hexagonal modification. In the zincblende structure, there are three alternating layer pairs of silicon and carbon, which are obtained by slicing the fcc structure perpendicular to its (111) axis. This is the only pure cubic SiC polytype, also known as β-SiC. Two alternating layers can be distinguished in the wurtzite structure, which represents the only pure hexagonal SiC polytype. All other polytypes are combination of these basic structures. Many other stacking arrangements can thus occur, yielding a wide range of ordered, long period, stacked hexagonal or orthorhombohedral structures, which are collectively known as α-SiC. The stacking sequence of the close-packed planes of covalently bonded Si-C elements can be described by the ramsdell notation, according to their positions in the lattice, as it is shown in Fig. 2.2.

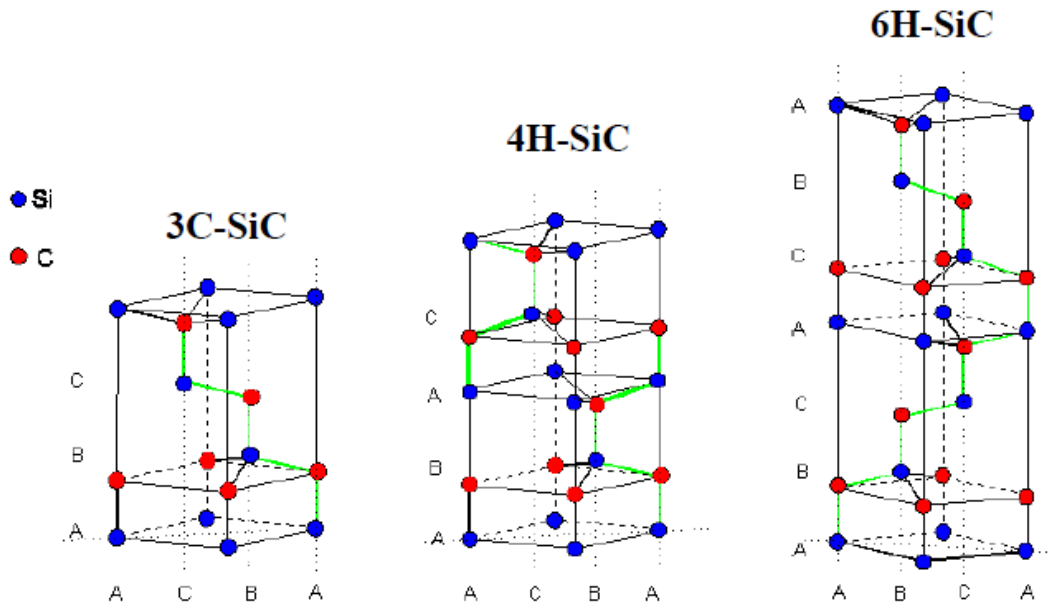


Fig 2.2. Stacking sequence of 3C-SiC, 4H-SiC and 6H-SiC[6]

The basic forms are indicated by 3C, 2H and R where the number gives the layer pairs of the succession period and C, H, and R, refer to cubic, hexagonal, and rhombohedral form. The reason for the occurrence of polytypism in SiC may be the small energy difference of about 2.4 meV per atom between the cubic and the hexagonal stacking [7]. SiC shows excellent mechanical and electronic properties which can, however, vary significantly between different SiC modifications, due to different arrangements of the silicon and carbon atoms in the unit cell between the SiC polytypes. Relevant material properties of Si and GaAs, GaN and of the 3C, 6H, and 4H polytype of SiC are shown in table 2.1. The various forms of SiC have the largest indirect energy gaps found in common semiconductor materials, ranging from 2.2eV for 3C-SiC to 3.33eV for 2H-SiC at room temperature. This indicates its potential for use in heterostructure electronic devices and high energy wavelength emission (e.g. blue light) and reception (e.g. UV light)[1]. Due to its wide bandgap a remarkable small intrinsic carrier concentration, n_i , of about 10^{-1} cm^{-3} for 3C-SiC and 10^{-10} cm^{-3} for 2H-SiC is found. For proper device operation, it should be negligible compared to the doping concentration. Electronic devices based on SiC are predicted to operate at temperatures up to 900 $^{\circ}$C ($n_i \sim 10^{15}$ cm^{-3}) without suffering from intrinsic conduction effects. Due to the exponential temperature dependence of failures rates, the reliability of those devices operating at lower temperatures will moreover be orders of magnitude higher than that obtained from Si devices.

Table: 2.1. Comparison of electronic properties of SiC with Si, GaAs and GaN[8]

	Si	GaAs	GaN	6H-SiC	4H-SiC	3C-SiC
Bandgap(Ev)	1.1	1.142	3.39	3	3.26	2.2
Breakdown field@10^{17} cm^{-3} (MV/cm)	0.6	0.6	3.3	3.2	3.0	1.5
Electron mobility at 10^{16} cm^{-3} (cm^2/V-s)	1100	6000	1000	370	800	750
Hole mobility at 10^{16} cm^{-3} (cm^2/V-s)	420	320	200	90	115	40
Saturation electron drift velocity(cm/s)	10^7	10^7	2.5×10^7	2×10^7	2×10^7	2×10^7
Intrinsic concentration n_i (cm^{-3})	1.5×10^{10}	1.9×10^{-10}	2.1×10^6	2.3×10^{-6}	8.2×10^{-9}	6.9
Thermal conductivity	1.5	0.55	1.3	4.9	4.9	5

The free carrier mobility in SiC is lower than that in Si which is attributed to the partial polar bonding of the Si and C atoms. The free carrier mobility is also related to the SiC polytype. 6H-SiC has, for example, the lowest electron mobility of the three SiC modifications compared in Table 2.1, due to the built in potential, 6H-SiC has an additional long period of the potential field of 15.12 Å, indicating the existence of small minibands whose band discontinuities control the scattering and transport properties. For 3C-SiC the width of the mini-Brillouin zones is sufficiently large (the period of the stacking arrangement is about 4.4 Å), and the transport properties are not greatly influenced by the miniband structure. Electron mobility and hole mobility are critically important device parameters, affecting the microwave performance, transconductance, output gain and on-resistance of MOSFET [9]. Although carrier mobility in SiC is relatively low at low electric fields, in high power high frequency applications, it is compensated by the high saturation electron drift velocity (v_{sat}) and high critical electric field (E_c).

2.3. SiC material growth

Many semiconductor materials can be melted and reproducibly recrystallized into large single-crystals with the aid of a seed crystal, such as in the Czochralski

method [15] employed in the manufacture of almost all silicon wafers, enabling reasonably large wafers to be mass-produced. However, because SiC sublimes instead of melting at reasonably attainable pressures, SiC cannot be grown by conventional melt-growth techniques. This prevented the realization of SiC crystals suitable for mass production until the late 1980's. Sublimate limits the size of the SiC crystals.

Thus, in contrast to most single-crystal semiconductor materials, SiC cannot be grown by crystal pulling or seeded solidification from elemental melts because of its thermodynamics. SiC crystals need to be grown using an elaborate furnace technique. The growth process of SiC material was suggested first by Acheson and major improvement to the process was developed by Lely in 1955. The modified-Lely method or seeded sublimation growth, developed by Tairov, et al. in 1978, is now used for commercial production of large-diameter SiC crystal. In the technique, SiC crystal is grown at temperatures of 2500-2700 K by the transport of subliming molecule species under partial vacuum conditions in the presence of an inert gas such as Ar, He. However, this bulk SiC cannot be used as an active layer in devices because of its low purity and poor electrical quality. At present, additional epitaxial growth on the bulk SiC is a necessary prerequisite for SiC-based device fabrication. Several methods for the epitaxial growth have been experimented, including chemical vapor deposition (CVD), sublimation epitaxy, and liquid phase epitaxy (LPE). Among them CVD method is used most widely because of relatively low cost, high throughput for mass production, and good film quality. The CVD epitaxial growth of SiC is performed by transport of gases containing silicon and carbon to the substrate surface in a reactor. Figure 2.3 shows the schematic drawing of hot-wall reactor which is a very common method for CVD epitaxial growth. The basic mechanism of CVD process is to transport precursor gases with a carrier gas into a chamber where the precursors decompose into atoms which diffuse down onto a substrate and produce an epitaxial film. The susceptor made of high purity graphite forms inner cell. The epitaxial growth of SiC has been achieved on many substrates including SiC, sapphire, AlN, TiC, and Si.

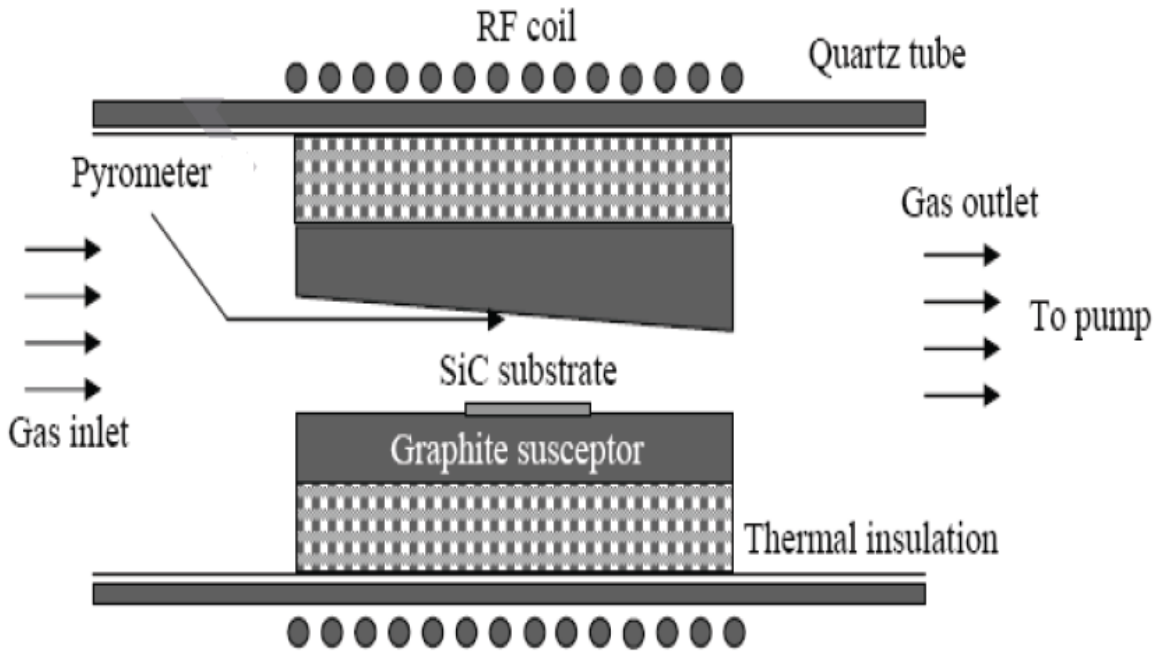


Fig 2.3: Schematic of horizontal hot-wall SiC CVD reactor[5]

2.4. SiC devices

In recent years, the activity in silicon carbide (SiC) has considerably increased due to the need for electronic devices capable of operation at high power levels and high temperatures. With its very high thermal conductivity (~5.0 W/cm), high saturated electron drift velocity (~2.7 × 10^7 cm/s) and high breakdown electric field strength (~3 MV/cm), SiC is a material of choice for high temperature, high voltage, high frequency and high power applications.

2.4.1. Power MOSFETs

A unique distinguishing feature of all semiconductor power devices is their high voltage blocking capability. Depending on the application, the breakdown voltage can range from 25 V for applications such as power supplies to over 6 KV for applications in power transmission and distribution. The ability to support high voltages is determined by the onset of avalanche breakdown, which occurs when the electric field within the device structure becomes strong. In power devices, high electric fields can occur both within the interior regions of the device where current transport takes place and at the edges of the devices. Proper design of devices requires careful attention to

field distributions both at the interior and at the edges to ensure high voltage blocking capability. Since the forward voltage drop during current conduction is larger for devices with higher breakdown voltage capability, it is important to obtain a device breakdown voltage as close as possible to the intrinsic capability of the semiconductor material for optimum device performance.

Power MOSFETs have a different structure than the lateral MOSFETs as with all power devices, their structure is vertical and not planar. In a planar structure, the current and breakdown voltage ratings are both functions of the channel dimensions (respectively width and length of the channel), resulting in inefficient use of the "silicon estate". With a vertical structure, the voltage rating of the transistor is a function of the doping and thickness of the N epitaxial layer, while the current rating is a function of the channel width. This makes possible for the transistor to sustain both high blocking voltage and high current within a compact piece of silicon.

SiC has been projected to have tremendous potential for high voltage solid state power devices with very high voltage and current ratings because of its high electric breakdown field of 1.5 – 4×10^6 V/cm and high thermal conductivity of 2.3 – 4 W/cmK, depending on the doping level[11].

$$V_B = \frac{E_c.W}{2} = \frac{\varepsilon_s.E_c^2}{2q.N_B} \quad \text{....(2.1)}$$

The high breakdown field allows the use of much higher doping and thinner layers for a given voltage than required in Si devices, resulting in specific on-resistances for SiC unipolar devices that can be $1/300^{th}$ that of the equivalent Si devices.

$$R_{on,sp} = \frac{V_B^2}{\mu_n.\varepsilon_s}\left(\frac{3}{2E_c}\right)^3 \quad \text{....(2.2)}$$

Power devices made with silicon carbide (SiC) are expected to show great performance advantages as compared to those made with other semiconductors. This is primarily because SiC has an order of magnitude higher breakdown electric field(2-4 × 10^6 V/cm)than conventional materials, and an electron mobility only ~20% lower than silicon.

2.4.2. Schottky Barrier Diode

Schottky barrier diodes offer unique advantages over conventional p–n rectifiers in terms of lower resistance, faster response, and negligible transient reverse current during switching. In addition, the reverse saturation current of Schottky diodes[12] is larger than that of p–n junction diodes. Therefore, a Schottky diode requires less forward bias voltage to achieve a given current than does a p–n junction diode. Schottky diodes based on silicon carbide (SiC) are of special importance owing to their capability of handling high voltages and high temperatures.

SiC possesses exceptional chemical and physical properties such as high thermal conductivity, a wide band gap, high breakdown field, high saturation velocity, and chemical stability. Therefore, metal-SiC Schottky contacts are suitable electrical devices for harsh environments such as high voltage rectifiers, UV radiation detectors, signal mixers, and high temperature gas sensors.

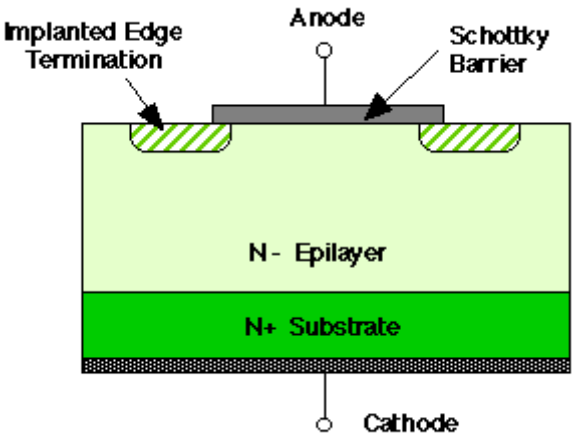


Fig 2.4: Cross section of an implant-edge-terminated Schottky barrier diode in SiC[12]

2.4.3. Vertical Power MOSFET

VDMOS transistors are common in silicon power device technology where the p-base and n+ source regions are formed by diffusion of impurities through a common mask opening. However, impurity diffusion is impractical in SiC because of the very low diffusion coefficients at any temperature. The Purdue group fabricated the first VDMOS transistors in SiC using ion implantation to introduce

dopants for the p-base and the n+ source. The implanted DMOSFET requires that separate masks be used to define the p-base and the n+ source. The construction is a vertical structure with a drift layer built on a highly conductive n+ layer. The n-drift region is designed to give the forward blocking capabilities (Figure 2.5). The forward blocking capability is achieved by the pn junction between p-base region and n-drift region [13].

In power MOSFET, the blocking voltage is supported across the drift layer, and thus the drift- region resistance is considered to be the minimum possible theoretical limit for the on-resistance of a MOSFET. For an ideal DIMOSFET, the resistances associated with the n+ source, the n-channel, the accumulation region and the n+ substrate are assumed to be negligible and the specific on-resistance of the power MOSFET is determined by the drift region only. This assumption is not accurate at lower breakdown voltages where the drift region resistance R_D is comparable to the other resistive components and these resistances should be included in calculating Ron-sp. However, at higher break- down voltages, R_D is significantly higher than other resistances and Ron-sp can be approximated by R_D. The details of the device structure are shown in Figure 2.5. During the device operation, a fixed potential to the p-base region is established by connecting it to the source metal by the break in the n+ source region.

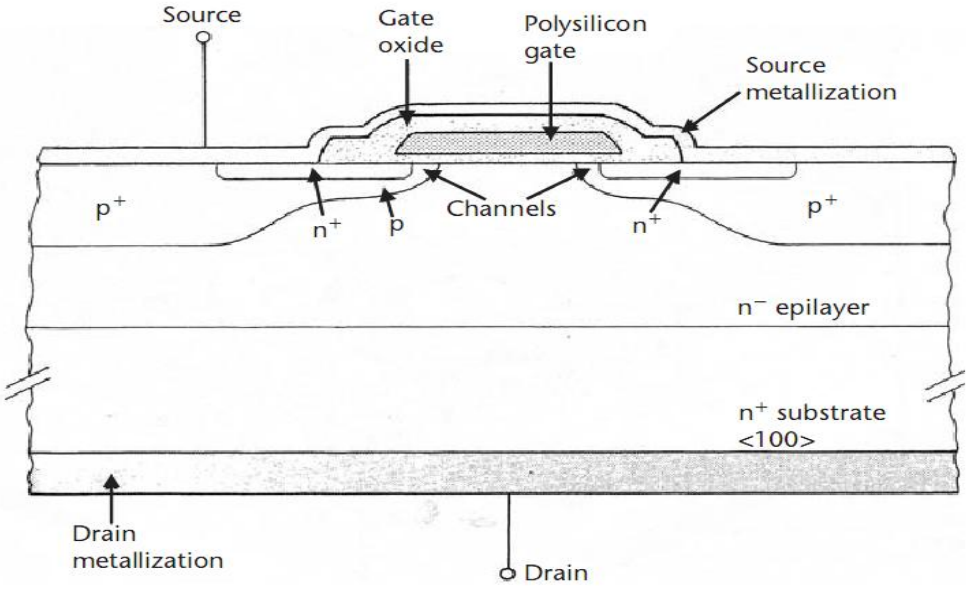


Fig 2.5: Schematic illustration of classical VDMOS transistor [13]

By short-circuiting the gate to the source and applying a positive bias to the drain, the p-base/n-drift region junction becomes reverse-biased and this junction supports the drain voltage by the extension of depletion layer on both sides.

However, due to the higher doping level of the p-base layer, the depletion layer extends primarily into the n-drift region. On applying the positive bias to the gate electrode, the conductive path between the n+ source region and the n-drift region is formed.

The application of positive drain voltage results in a current flow between drain and source through the n-drift region and conductive channel. The conductivity of the channel is modulated by the gate bias voltage and the current flow is determined by the resistance of various resistive components [14].

In a power MOSFET, the blocking voltage appears across the drift layer and so the drift- region resistance is considered to be the minimum possible theoretical value for the on- resistance of a MOSFET. For an ideal VDMOSFET, the resistances associated with the n+ source, the n-channel, the accumulation region and the n+ substrate are usually neglected and the specific on-resistance of the power MOSFET is determined by the drift region alone. SiC DIMOSFETs have been fabricated with the blocking voltage of 760V. To obtain the blocking voltage greater than 760 V for 6H-SiC depends on the drift region thickness, doping level, specific on-resistance and electric field strength.

2.4.4. ACCUFET

The principal difference between accumulation-channel lateral DMOSFET shown in Figure. 2.6 and the conventional inversion-layer structure is the presence of a thin n-channel region (accumulation-layer) below the gate oxide using a buried p-well region formed by ion-implantation. The thickness, length, and n-doping concentration of this accumulation-layer are carefully chosen so that it is completely depleted by the built-in potential of the p/n junction. This causes a potential barrier between the n+ source and the n-drift regions resulting in a normally-off device with the entire drain voltage supported by the n-drift region. Thus it can block high forward voltages at zero gate bias with low leakage currents. When a positive gate bias is applied, an accumulation channel of electrons at the SiO_2-SiC interface is created and hence a low resistance path for the electron current flow from the source to the drain is achieved.

This structure offers the possibility of moving the channel away from the oxide interface, thereby removing the consequence of the bad interface quality on the channel mobility. The structure also utilizes the buried p-well region as a shield to high SiC bulk electric field on the gate oxide.

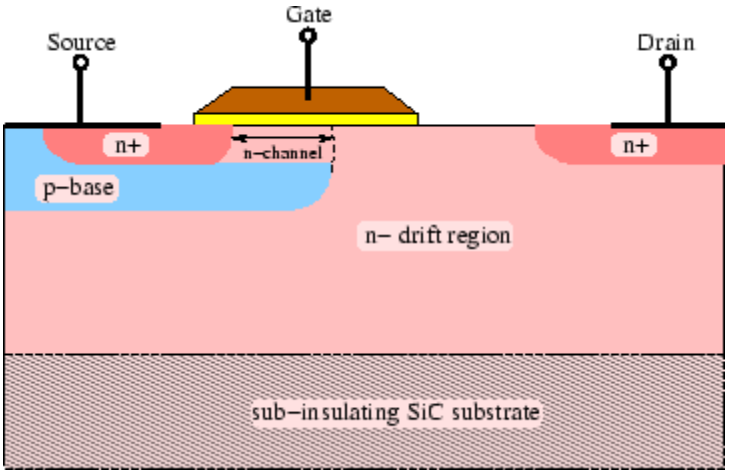


Fig 2.6: Cross section of an accumulation-channel lateral DMOSFET on SiC sub-insulating substrate [15].

2.4.5. Lateral Double Diffusion MOSFET

Before the advent of power devices of SiC, MOSFETs and thyristors had been fabricated as vertical structures with the substrate acting as an anode. In the off state, the voltage was blocked by a reverse-biased p/n junction. To achieve high blocking voltage, the drift region should be lightly doped and thick. For a given device thickness, there was a maximum possible blocking voltage regardless of doping. For SiC lateral MOSFETs with a 10 μm drift region, the maximum possible voltage is 1600V. To overcome the limitations of vertical-type MOSFETs, lateral- type MOSFET is used. The structure of lateral DMOSFET is as shown in Figure 2.7. It can be observed that the insulating substrate is of SiC. In the blocking state, the depletion layer spreads mainly into the lightly-doped drift region. Once the depletion region reaches the insulating substrate, it continues spreading toward the drain. Here, the maximum voltage is not limited by the thickness of the layer. As in the case of vertical devices, the drift region component of the total LDMOST specific on-resistance depends on its dimensions and doping concentration.

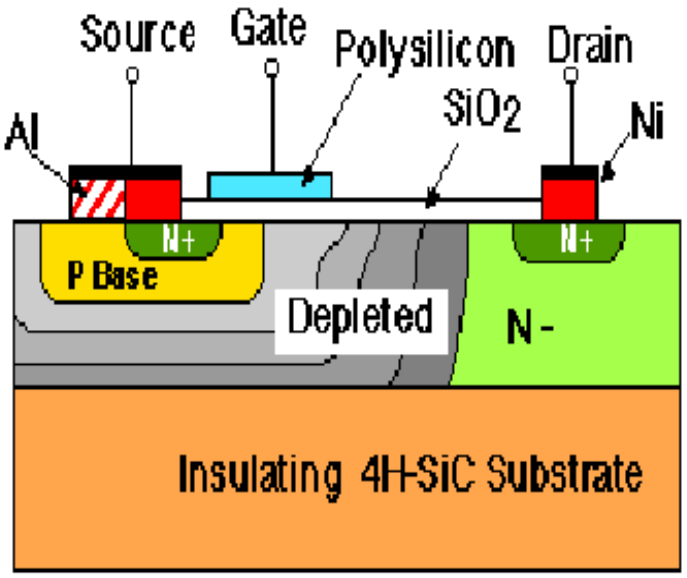


Fig 2.7: Cross section of Lateral Double Diffusion MOSFET [16]

2.4.6. SiC Impatt Diode

Silicon carbide is an ideal semiconductor for the fabrication of high-power microwave devices due to its high breakdown field. One device, in particular, that benefit from the high breakdown field of SiC is the IMPact ionization Avalanche Transit-Time (IMPATT) diode oscillator.

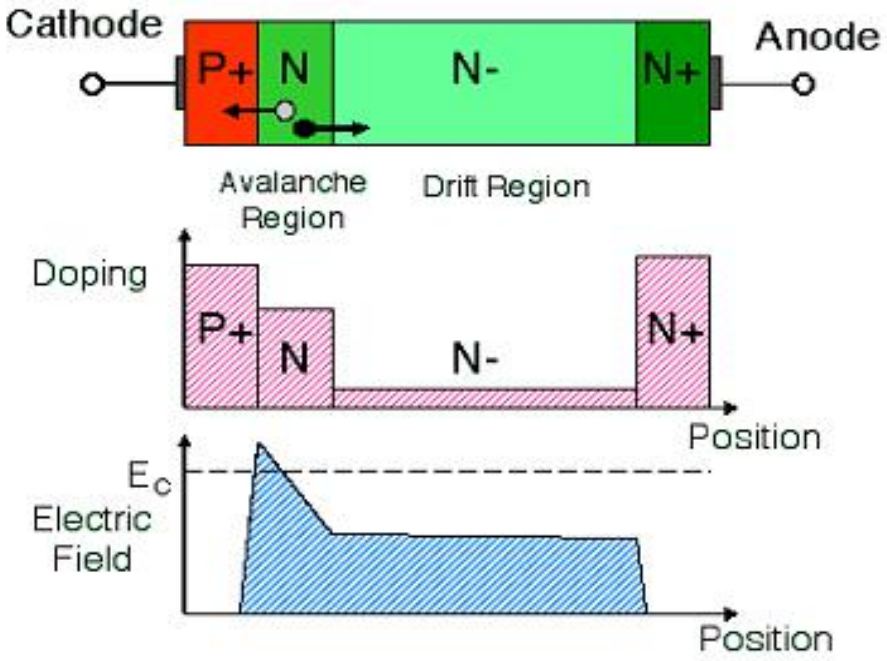


Fig 2.8: Cross section of a SiC IMPATT diode [17]

IMPATT diodes deliver the highest RF power of any semiconductor microwave oscillator, and are used to produce carrier signals for microwave transmission systems, particularly airborne and ground-based radar. Depending upon the design, IMPATT diodes can operate from few GHz to few hundred GHz. The power-frequency product (p f2) of an IMPATT diode scales as the square of the critical field for avalanche breakdown times the electron saturation drift velocity. Hole-electron pairs are created at the point of highest electric field (the "Avalanche Region"). Holes are swept into the cathode, but electrons drift toward the anode, inducing a displacement current in the external circuit as they drift.

Figure 2.8 shows the buildup of microwave oscillations in the diode current and voltage when the diode is embedded in a resonant cavity and biased at breakdown.

2.4.7. Charge Coupled Devices

Charge coupled devices (CCDs) are linear shift registers formed by a series of closely- spaced MOS plates on the surface of a semiconductor. Application of bias voltages to the MOS plates results in the creation of localized potential wells in the semiconductor under each plate. Charge packets can be confined in the potential wells and shifted along the surface under the influence of appropriate clocking waveforms applied to the gates. Silicon CCDs are widely used as image sensors, particularly in digital still cameras and hand-held video cameras. SiC is of interest as a specialized image sensor because its wide band gap makes it transparent to visible light, resulting in an ultraviolet (UV) sensor which is virtually blind to solar radiation. Such a sensor has applications in aerospace research, UV astronomy and in military systems. In this structure, the source and drain junctions and the buried n-type channel are formed by nitrogen ion implantation and the implants are activated by high temperature annealing. The gate oxide is thermally grown using the optimized conditions identified in MOS investigations. Then deposit a layer of polysilicon for the first-level gates and dope the poly with phosphorus. The polysilicon is patterned by reactive ion etching and oxidized to form a passivation layer. A second layer of polysilicon is then deposited and doped to form the second-level gates.

2.4.8. SiC Non-Volatile Memory Devices

6H silicon carbide is a single-crystal semi conducting material with a band gap of 3.0 eV. This wide band gap results in an extremely low value for the intrinsic carrier concentration in room temperature, about 16 orders of magnitude lower than silicon. Since thermal generation scales directly with the intrinsic carrier concentration, leakage currents in SiC are negligible [18].

2.4.9. Digital CMOS Integrated circuits in 6H-SiC

CMOS technology is attractive for digital logic because it offers low power consumption, full rail-to-rail output swing, and greater noise margins than NMOS circuits. CMOS also provides active current sources for linear applications. Development of CMOS technology in SiC is expected to provide low power, high temperature circuits as well as reliable control circuitry for smart power integrated circuits. Process utilized an implanted n-well and deposited oxides, but due to other processing problems the PMOSFETs exhibited a very high threshold voltage. Implanted p-well and thermally grown oxide is used to fabricate this device. The fabrication sequence is as follows:

1. P-wells are formed on n-type epilayers doped at $8x10^{15}cm^{-3}$ by boron implantation. Al and N are then implanted through polysilicon masks to form P+ and N+ source/drain regions, respectively.

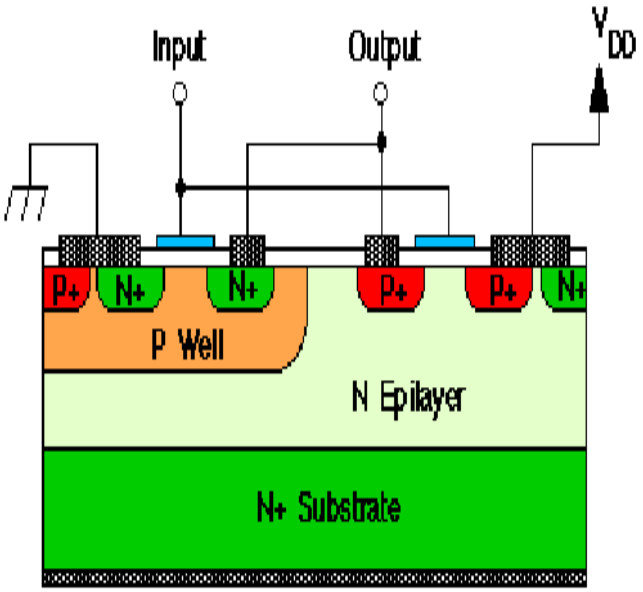


Fig 2.9: Cross section of a CMOS inverter in the implanted p-well process [3].

2. NMOSFETs are formed on p-wells while the PMOSFETs are formed on n-type epilayers. Implants are annealed at 160°C for 40 minutes in argon, followed by an 115°C, 2 hour wet oxidation to form a 40nm gate oxide layer.
3. Polysilicon is then deposited and patterned to form the gates. Al-Ni is used for p-type ohmic contacts and Ni for n-type contacts. A silicon oxynitride layer is deposited as an inter-metallic dielectric.
4. Vias are opened and interconnect metal is deposited and patterned.

2.5 SiC Technology and applications

SiC, as a new semiconductor, the first drawback to overcome towards to its development is the capability to grow large area wafers with controlled doping properties and very low residual defect density. By the end of the 70s, a first step has been done towards reaching this objective by means of the development of the modified Lely method, which allows growing boules of SiC larger than 1 inch diameter. This achievement waked up the interest of the microelectronic research community, and technological and device activities on this semiconductor started again. Since then, SiC has demonstrated its great potential as base material for high power, high temperature and high frequency devices over the past recent years. The physical background of this potential lies on its superior material properties (Table 2.2). The physical and electronic properties of SiC make it the foremost semiconductor material for short wavelength optoelectronics, high temperature, radiation resistance, and high power/high frequency electronic devices.

Among others properties its wide bandgap allows the operation of SiC electronic devices at extremely high temperatures without suffering from intrinsic conduction effects. For example, radiation hard high temperature silicon carbide electronics will play a key role in future missions to the hostile environments near the sun and on the surfaces of the inner planets. Long term operation of probes within Venus's scorching 450°C atmosphere will require the use of uncooled silicon carbide electronics. For spacecraft operating near the Sun, silicon carbide electronics would enable significant reductions in spacecraft shielding and heat dissipation hardware, so that more scientific instruments could be included in each vehicle. These achievements could be, of course, eventually used in the conventional aircraft or

automobile industry.

SiC can withstand a voltage gradient (or electric field) over eight times greater than Si or GaAs without undergoing avalanche breakdown. This high breakdown electric field enables the fabrication of very high-voltage, high power devices such as diodes, power transistors, power thyristors and surge suppressors, as well as high power microwave devices. Additionally, it allows the devices to be placed very close together, providing high device packaging density for integrated circuits. SiC is an excellent thermal conductor (SiC possess high thermal conductivity). Heat will flow more readily through SiC than other semiconductors materials. In fact, at room temperature, SiC has a higher thermal conductivity than any metal.

Applications of Silicon Carbide:

a) Spacecraft with high temperature, radiation hard SiC electronics will enable challenging missions in both the inner and outer solar system.
b) SiC is highly suitable for energy saving in public power distribution.
c) The high voltage power lines that currently destroy the beauty of the land killing the birds of the prey can be buried under ground.
d) SiC sensors and control on an automobile (electric or hybrid) engine will result in cleaner burning, more fuel efficient cars.

This property enables SiC devices to operate at extremely high power levels and still dissipate the large amounts of excess of heat generated. The high-saturated electron drift velocity explain why SiC devices can operate at high frequencies (RF and microwave) because of the high saturated electron drift velocity of SiC. Power semiconductor devices are a critical element of "smart" power electronics technology. Today, utilities generate on average 20% more electricity than is consumed at any given time. This excess power reserve is needed to ensure that electric service is reliably immune to everyday load changes and component failures that causes electrical glitches throughout the power grid. The incorporation of solid-state "smart" power electronics into the power grid should significantly reduce the power-reserve margin necessary for reliable operation, because these semiconductor circuits can detect and instantaneously compensate for local glitches. It has been estimated that a mere 5% reduction in power reserve margin would estimate the need for $50 billion worth of new power plants within the next 25 years. This same smart power technology would also enable as much as 50% larger power capacities to be carried

over existing power lines. Presently, these devices are all implemented in conventional silicon-based semiconductor technology. In short, SiC power devices could standoff higher voltages and respond faster using devices with lower parasitic resistances and physically sizes much smaller than silicon power devices. Faster switching speed not only increases power system conversion efficiency, but it also enables the use of smaller transformers and capacitors to greatly shrink the overall size and weight of the system. Furthermore, the high temperature capability of SiC greatly reduces cooling requirements that are also a substantial portion of the total size and cost of a power conversion and distribution system. SiC devices are therefore expected to drastically improve the distribution and efficient usage of electric power in the 21st century.

Table 2.2: Main advantages of SiC and related application fields.

	SiC vs Si advantage	Application
Electrical properties	High electric field Wide band gap High carrier Saturation velocity	Power devices HT electronics & sensors UV & radiation detectors High frequency(RF devices)
Mechanical properties	Young modulus Hardness	Mechanical sensors Surface coating
Chemical properties	Inertness Biocompatibility	Chemical sensors(gas,HT) Bio-sensors
Thermal properties	High thermal conductivity	Power devices

Apart from power devices, which is the main application field of SiC, biomedical sensors, UV and radiation detectors, MEMS, micro and nano-resonators, magnetic and temperature hall sensors and gas sensors are other applications in which SiC can play a major role to improve their current performances. Table 2.2 summarizes the main SiC advantages and the identified application fields where it can be applied.

CHAPTER-3
OVERVIEW OF LDMOSFET

3.1 Introduction

The 3C-SiC is a promising material for MOSFET devices because of high channel mobility due to lower density of interface states compared to 4H-SiC. Poor performance of 6H-SiC and 4H-SiC MOSFETs is related to the interface states located in the band gap close to the conduction band edge limiting the transport of electrons in the channel. Due to the smaller band gap of 3C-SiC, the interface states observed in 6H-SiC and 4H-SiC are located in the conduction band and have no effect on the transport properties of the channel. The 3C-SiC polytype has lower critical electric field value due to the lower band gap. It means that the drift region doping corresponding to a given blocking voltage will be lower compared to the hexagonal 4H-SiC and 6H-SiC polytypes. This also means that the specific junction capacitance will be lower in the 3C-SiC devices as compared to the 4H-SiC and 6H-SiC ones. This is an advantage from the point of view of high speed MOSFETs.[24]

The current highly energy information generation requires effective use of resources, control electric power and energy, so developing power electronics is an imperative work. Power MOSFET basically divides into lateral and vertical altogether two kinds of basic structure. The LDMOSFET structure is always built using a low doping density section near the drain end of the drift end of the drift region to increase breakdown ability, but causes a high turn-on resistance. In such a structure, the depletion region surrounding the p-well first depletes through the n-type epilayer to the insulating substrate, then moves laterally toward the drain. The lateral extent of the depletion is therefore not limited by the thickness of the epilayer.

3C-SiC lateral double-implanted metal-oxide semiconductor (LDMOS) field effect transistor is fabricated in a lightly doped n-epilayer on an insulating 4H-SiC substrate. The p-base region and the n^+ -source region are diffused through a common window defined by the edge of the polysilicon gate. The p-base region driven in deeper than the n^+ source. The difference in the lateral diffusion between the p-base and n^+ source regions defines the surface channel region. The channel length L is determined by the higher rate of diffusion of the p-dopant (e.g boron), compared to the n^+ dopant region(e.g phosphorous) of the source. The channel is

followed by a lightly doped drift region.

3.2 Device structure and operation

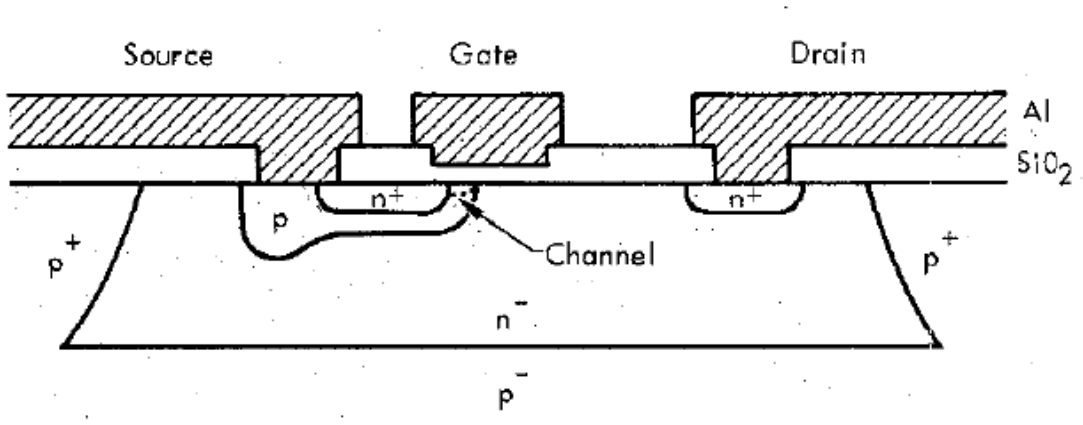


Fig 3.1: LDMOSFET structure [19]

The LDMOST is a MOS field effect device that attains short channel lengths by the difference in lateral diffusion of two impurity distributions. The starting material, in this case is a lightly doped n-type epitaxial layer on a lightly doped p-type substrate. A p-type isolation diffusion is performed to define an isolation island. A second p-type diffusion is performed to provide contact to the channel region of the transistor. A third p-type diffusion defines the bulk channel region but this time no oxide is grown. Now an n-type diffusion is performed through the same oxide window as the previous diffusion. In addition a second oxide window is opened for drain contact. Finally a gate window is etched, gate oxide regrown over the active channel region, contact holes etched, and metallization defined. The channel length is determined by the difference in lateral diffusion between the second p-type diffusion and the n-type impurity distribution.

Since the channel length of a MOSFET is inversely proportional to the transconductance and proportional to the on resistance, the structure shown in Figure 3.1 results in a device which has high transconductance and low on resistance. Therefore, this device has a high current carrying capability. High source to drain breakdown voltage is obtained because of the lightly doped epitaxial material so that the drain-channel depletion layer spreads mainly into the drain drift region as voltage is increased. Furthermore, the gate metal acts as a field plate to reduce surface fields and maintain high breakdown. This structure has been shown to have higher breakdown voltage that one in which the gate electrode extends to the drain contact diffusion.

The DMOS transistor is an n-channel MOSFET so that in normal operation the drain is at a positive potential with respect to the source. The threshold voltage V_t is defined as the gate to source voltage (V_{GS}) at the onset of current conduction. The electrons flow from the source through the surface channel and then through the bulk in the lightly doped epitaxial "drift region" to the drain contact. This drift region contributes an additional component to the on resistance. This additional resistance is much lower than that for a series MOSFET since current spreads into the n-type bulk.

3.3 MOS Physics

3.3.1 Ideal MIS Diode

The metal-insulator semiconductor (MIS) structure is shown in Figure 3.2, where d is the thickness of the insulator and V is the applied voltage on the metal field plate. The energy band diagram of an ideal MIS structure of p-type semiconductor for V=0 is shown in Figure 3.3.

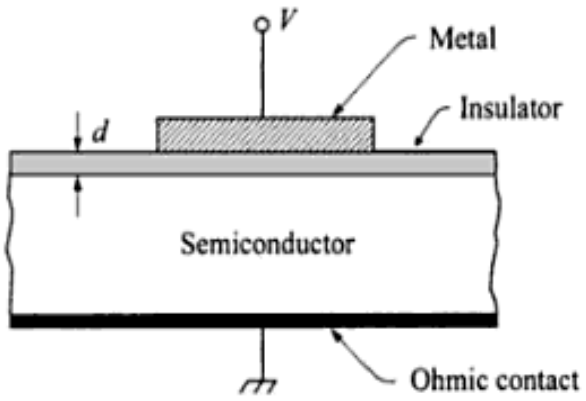


Fig 3.2: Metal-Insulator-Semiconductor diode

An ideal MIS diode is defined as follows.

(1) At zero applied bias energy difference between metal work function ϕ_m and the semiconductor is zero, or the work-function difference ϕ_{ms} is zero:

$$\phi_{ms} = \phi_m - (\chi + E_g/2q + \psi_B) \quad \text{for p-type} \qquad \ldots.(3.1)$$

$$\phi_{ms} = \phi_m - (\chi + E_g/2q - \psi_B) \quad \text{for n-type} \qquad \ldots.(3.2)$$

Where ϕ_m is the metal work function, χ the semiconductor electron affinity, E_g the bandgap energy, q is electronic charge, ψ_B the potential difference between the Fermi level E_F and the intrinsic Fermi level E_i. In other words, the band is flat (flat-band condition) when there is no applied voltage.

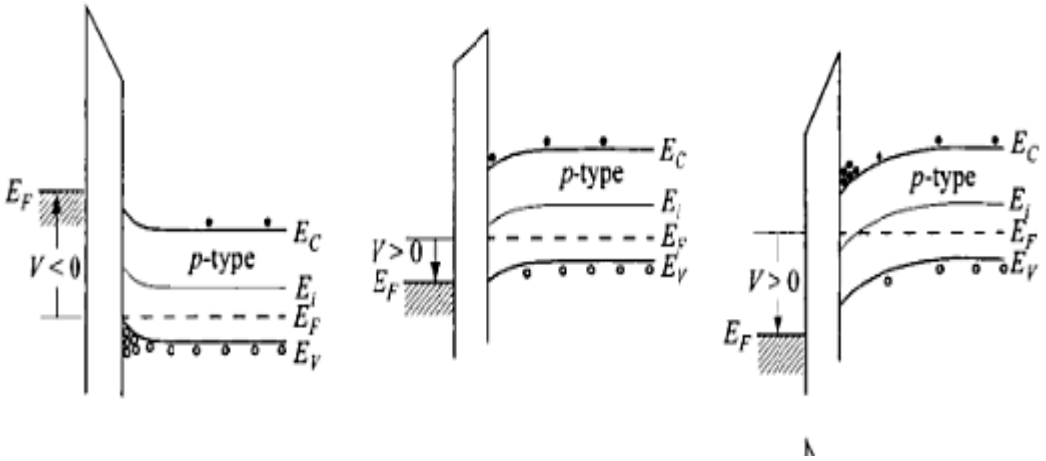
(2) The only that can exist in the structure under any biasing condition are those in the semiconductor and those with the equal but opposite sign on the metal surface adjacent to the insulator.

(3) There is no carrier transport through the insulator under dc biasing conditions or the resistivity of the insulator is infinity.

When the ideal MIS diode is biased with positive or negative voltages, basically three cases may exist at the semiconductor surface as shown in Figure 3.3.

The three cases are follows:

(a) Accumulation (b) Depletion (c) Inversion



(a) (b) (c)

Fig 3.3: Energy Band diagram (p-type) for an ideal MIS diode when V≠ 0 [26](a) accumulation, (b)depletion, (c) inversion

For the p-type semiconductor, when a negative voltage (V<0) is applied to the metal plate, the top of the valence band bend upward and is closer to the Fermi level Figure 3.3(a). For an ideal MIS diode, no current floes in the structure, so the Fermi level remains constant in the semiconductor. Since the carrier density depends exponentially on the energy difference (E_F-E_V), this band bending causes an accumulation of majority carriers (holes) near the semiconductor surface. This is the "accumulation" case. When a small positive voltage (V>0) is applied, the bands bend downward, and the majority carriers are depleted Figure 3.3(b). This is the "depletion" case. When a larger positive voltage is applied, the bands bend even more downward so that the intrinsic level E_i at the surface crosses over the Fermi level E_F. Figure 3.3(c). At this point the number of electrons (minority carriers) at the surface is larger than that of the holes, the surface is thus inverted, and this is

the “inversion” case.

3.3.2 Surface Space Charge Region

Surface space charge region to the intrinsic Fermi level E_i as shown. At the semiconductor surface $\psi = \psi_S$, and ψ_S is called the surface potential. The electron and hole concentration as a function of ψ are given by the following relations:

$$n_p = n_{p0} \exp(q\psi / kT) = n_{p0} \exp(\beta\psi) \quad \ldots\ldots(3.3)$$

$$p_p = p_{p0} \exp(-q\psi / kT) = p_{p0} \exp(-\beta\psi) \quad \ldots\ldots(3.4)$$

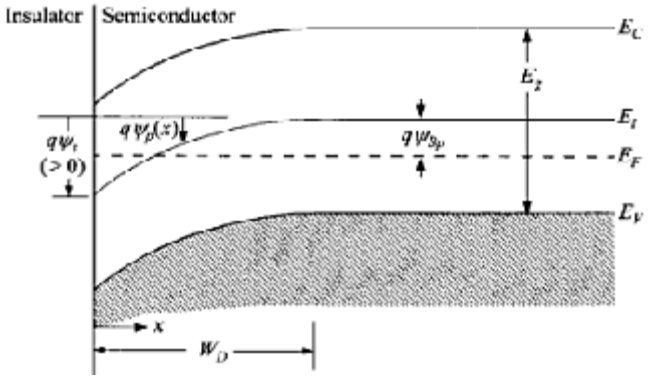


Fig 3.4: Energy-band diagram at the surface of p-type semiconductor. (a) Accumulation occurs at ψ_S <0. (b)Depletion occurs when $\psi_B > \psi_S >0$. (c) inversion occurs when $\psi_S > \psi_B$ [26].

Where ψ is positive when the band is bent downward n_{p0} and p_{p0} are the equilibrium densities of the electrons and holes, respectively, in the bulk of semiconductor, and β=q/kt. At the surface the densities are:

$$n_S = n_{p0} \exp(\beta\psi_S) \quad \ldots..(3.5)$$

$$p_S = p_{p0} \exp(-\beta\psi_S) \quad \ldots..(3.6)$$

It can be summarized as:

ψ_S <0 accumulation of holes (bands bend upward)

ψ_S =0 flat band condition

$\psi_B > \psi_S > 0$ depletion of holes (bands bend downward)

$\psi_S = \psi_B$ midgap with $n_S = p_S = n_i$ (intrinsic concentration)

$\psi_S > \psi_B$ inversion (electron enhancement, bands bend downwards)

Strong inversion begins at a surface potential,

$$\psi_{S_{(inv)}} = 2\psi_B = \frac{2kT}{q} ln\left(\frac{N_B}{n_i}\right) \quad \text{.....(3.7)}$$

3.4 Interface Trapped and Fixed Oxide Charges

3.4.1. Interface Trapped Charges: It has been shown that interface-trapped charges Q_{it} exists within the forbidden gap due to the interruption of the periodic lattice structure, at the surface of a crystal. Shockley and Pearson experimentally found the existence of Q_{it} in their conduction measurement. Measurements on clean surfaces in an ultra -high-vacuum system confirm that Q_{it} is very high of the order of 10^{12} atoms cm^{-2}.

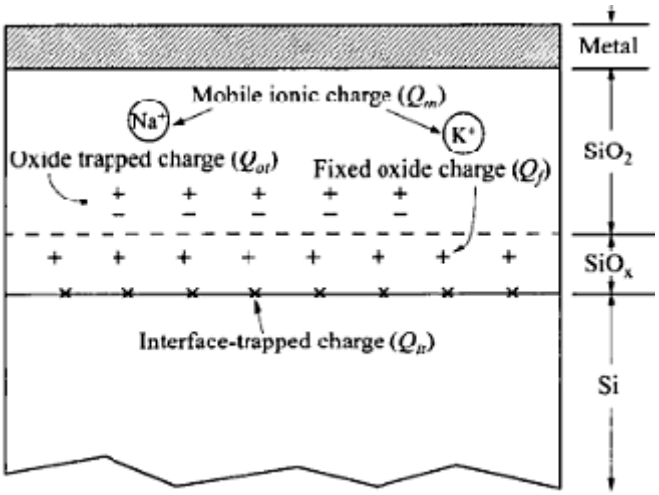


Fig 3.5: Terminology for charges associated with thermally oxidized silicon [20].

An interface trap is considered a donor if it can become neutral or positive by donating (giving up) an electron. An acceptor interface trap can become neutral or negative by accepting an electron. Figure 3.5 shows the distribution of these charges.

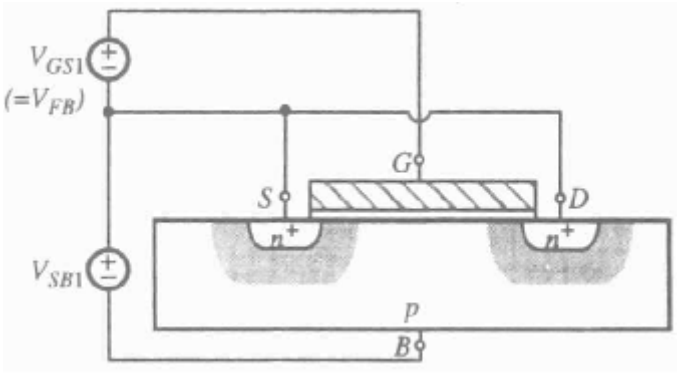
3.4.2. Fixed Oxide Charges: Oxide charges include the oxide fixed charge Q_f, the oxide trapped charge Q_{ot}, and the mobile ionic charges Q_m, as shown in Figure 3.5. The fixed oxide charges Q_f has the following properties: It is fixed and cannot be charged or discharged over a wide variation of ψ_s. Its density is not greatly affected by the oxide thickness or by the type of concentration of the impurities in the semiconductor; it is generally positive and depends on oxidation and annealing

condition [20].

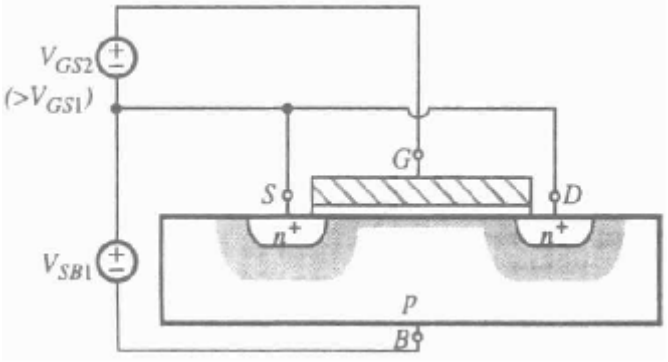
3.5. Flat Band Voltage

To illustrate the Flat Band voltage, a simple MOS transistor has been taken in this section. Let us consider a transistor connected to external voltage source as in Figure 3.6. The drain is short-circuited to the source, making V_{DS}=0. The external source-body bias V_{SB} is fixed at a positive value V_{SB1}, since the source is short-circuited to the drain, acts as the reverse bias for the pn junction. Let us consider the pn junction associated with the source. The shadow around the junction indicates the presence of the depletion region i.e., a region where most mobile charges have been removed, with holes in the body having moved away from the junction toward the negative terminal of the V_{SB} of the battery and electrons in the n^+ region having moved in the opposite direction towards the positive terminal of the battery. This means that, on the p side, immobile acceptor atoms are left with a net negative charge(they have been "uncovered"); also, on the n+ side, immobile donor atoms are left with a net positive charge. The total charges revealed on each side of the junction are equal in magnitude, preserving charge neutrality. Because the n+ region is much more heavily doped, only a very narrow strip need be uncovered on that side, to balance the charges on the much deeper strip on the p side. In the Figure, only the depletion region on the p side is shown, and it is indicated by the depletion region on the p side is shown, and it is indicated by the shadow around the n+ region.

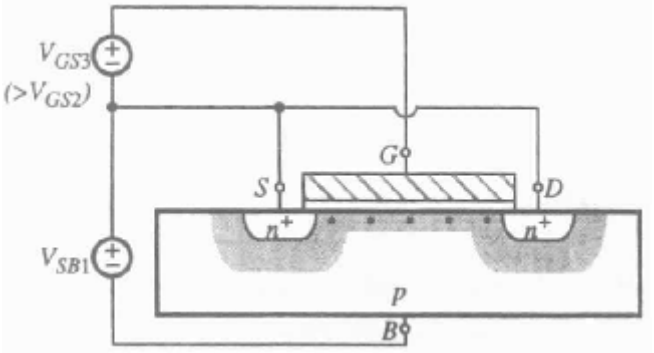
The depth of the depletion region is related to the charge density in it and the electrostatic potential across it, according to basic electrostatic laws. This depth is such that the resulting electrostatic potential drop across the region, along with the contact potentials at the contacts to the device, and the external bias V_{SB} algebraically add up to zero. A depletion region will exist even with V_{SB} = 0; the potential across it balances the contact potentials around the loop. If V_{SB} is increased, the depletion region will deepen accordingly to support the extra drop. It can be shown that since the n^+ region is much more heavily doped than the p region, practically all the potential drop across the depletion layer occurs on the p side.



(a) Flat band



(b) Depletion



(c) Inversion

Fig 3.6: MOS transistor with $V_{DS} = 0$ and successively increased values of V_{GS} [21].

On the drain side, another depletion region forms in the same way. Since the drain is short-circuited to the source, the drain-body junction sees the same reverse bias as the source-body junction, and thus both depletion regions have the same depth. If V_{GS} is sufficiently negative, positively charged holes can be attracted at the surface (the substrate interface to the oxide); this condition is known as accumulation. If the surface is accumulated, and subsequently V_{GS} is made less and less negative, the accumulation will become lighter and lighter, and at a certain value of V_{GS} it will disappear altogether, leaving the body neutral.

This is the *flat-band* condition, assumed in Figure. 3.6(a). The corresponding value of V_{GS} is called the *flat-band voltage* and is denoted by $V_{FB.}$ At the flat-band condition, each immobile negatively charged acceptor atom in the body outside the two depletion regions is, on average, covered by a mobile, positively charged hole, resulting in macroscopic neutrality.

If V_{GS} is now made more positive than its flat-band value, the charge on the gate will become more positive, too. This will tend to repel holes from the surface, resulting in a depletion region in the channel as shown in Figure. 3.6(b). This condition is called *depletion.*

If V_{GS} is raised still farther, more positive charges will be placed on the gate, which must be balanced by more negative charges in the channel; to uncover the extra negative charges, the depletion region in the channel must become deeper. Assume now that V_{GS} is increased to the point that the depletion region in the channel becomes almost as deep as that under the *n*+ regions. This means that the electrostatic potential at the surface (with respect to the body) is now almost the same as that on the *n*+ regions. Thus the surface becomes almost as attractive for electrons as the *n*+ regions. Electrons now enter from the *n*+ regions into the channel, next to the surface, despite the fact that the body is *p* type. The surface is now said to be *inverted,* and the electrons next to the surface what is known as an *inversion layer.* The larger the value of V_{GS} the more the electrons are attracted to the surface and the "heavier" the inversion [21].

The MOSFET Flat Band voltage is given by:

$$V_{FB} = \phi_{ms} - \frac{Q_f}{C_{ox}} - \frac{Q_{ot}}{C_{ox}} - \frac{Q_{it}}{C_{ox}} \quad \text{....(3.8)}$$

C_{ox} is the oxide capacitance given by the equation,

$$C_{ox} = \frac{\varepsilon_{ox}}{t_{ox}},\ \varepsilon_{ox} = \text{relative permittivity of } SiO_2 \quad \text{.....(3.9)}$$

Where Q_f is the oxide fixed charges, Q_{ot} is the oxide trap charge, and, Q_{it} is the interface trap charge[20].

3.6 Electron mobility models for 3C-SiC

In the 3C-SiC the samples are heteroepitaxially grown on either Si or 6H-SiC, because no 3C-SiC substrate exists. This results in large lattice mismatches (about 20% for Si substrates), and a corresponding high defect density. This coupled with the fact that

there is currently little drive to establish 3C-SiC commercially (unlike the 4H and 6H SiC), results in large differences in the quality of the material reported on. The mobility equation[25] is given as,

$$\mu = \frac{C\left(\frac{N}{N_{ref}}\right)^{\alpha-\delta} + \mu_{max}}{1+\left(\frac{N}{N_{ref}}\right)^{\alpha}} \quad \text{cm}^2/\text{Vs} \qquad \ldots.(3.10)$$

Where μ_{max}, C, $N_{ref,}$ α, δ are fitting parameters. The fit for the 3C-SiC mobility were found to be

$$\mu_{max} = 650\left(\frac{T}{300K}\right)^{-2.5} \text{ cm}^2/\text{Vs} \qquad \ldots.(3.11)$$

$$\text{C} = 330\left(\frac{T}{300K}\right)^{-1.5} \quad \text{cm}^2/\text{Vs} \qquad \ldots.(3.12)$$

$$N_{ref} = 3\times10^{16}\ \text{cm}^{-3} \qquad \ldots..(3.13)$$

$$\alpha = 0.8,\ \delta = 0.2 \qquad \ldots..(3.14)$$

3.7. Breakdown Voltages

3.7.1. Oxide Breakdown

This is destructive breakdown. It occurs when the electric field in the gate insulator exceeds a certain value [(about 7×10^6 V/cm) 0.07 V/A^o in silicon dioxide]. The result is a permanent short circuit through the insulator. Static charge, such as that gate by handling devices with bare hands, is known to cause oxide breakdown. For this reason, protective devices are used at those input terminals of an MOS integrated circuit that are connected to transistor gates.

3.7.2. Avalanche Breakdown

The junction formed by the substrate and drain or source region will conduct a large current if the reverse bias applied to them exceeds a certain value (because the field in the junction near the surface is influenced by the presence of the gate, the above value depends on the gate potential and can be different from the predicted common pn junction theory). When the device is on, carriers, moving fast in the channel can impact on silicon atoms and ionize them, producing electron-hole pairs; this is referred to as *impact ionization.* The newly generated pairs can gain enough energy to impact on silicon atoms and produce more electron-

hole pairs. This is called *avalanche effect* and is more pronounced in the pinch-off region near the drain where field can be high. Currents larger than those predicted by common device model will then flow, and the phenomenon is referred to as *channel breakdown*.

3.7.3. Punch-Through Breakdown

It occurs in devices with relatively short channels when the drain voltage is increased to the point that the depletion region surrounding the drain region extends through the channel to the source. The drain current then increases rapidly. Normally, punch-through does not result in permanent damage to the device [22].

CHAPTER-4
I-V CHARACTERISTICS OF LDMOS EXCLUDING FIXED OXIDE CHARGE IN SiO_2

4.1 Device equations

With reference to Figure 3.1, all the calculation is done for uniform doping profile in the drift region.

The current in the device is given by the relation [19]:-

$$I_{DS} = \beta_o \left\{ [V_{GS} - (V_{FB} + 2\phi_F)]V_{DS} - \frac{1}{2}V_{DS}^2 \ - \frac{2}{3}\gamma \left[(V_{DS} + \ V_{SB} + 2\phi_F)^{\frac{3}{2}} - (V_{SB} + 2\phi_F)^{\frac{3}{2}} \right] \right\} \quad \ldots.(4.1)$$

Where β_o = constant for a fixed value of doping (μmho/Vμm)

V_{GS} = Gate to source voltage = V_G (source has been grounded V_S = 0 volts)

V_{FB} = Flat band voltage (volts)

ϕ_F = Bulk potential (volts)

γ = Body effect term

V_{SB} = Source to p base voltage (volts)

V_{DS} = Drain to source voltage (volts)

C_{ox} = Oxide capacitance (F/cm^2)

Active channel length = 2μm, channel width = 100μm, oxide thickness = 0.1μm

In the saturation region, the drain current can be calculated by substituting the saturation drain voltage V_{Dsat} in equation (4.1).

$$V_{Dsat} = V_{GS} - (V_{FB} + 2\phi_F) + \frac{\gamma^2}{2}\left\{ 1 - \left[1 + 4\frac{(V_{GS} - V_{FB} + V_{SB})}{\gamma^2} \right]^{\frac{1}{2}} \right\} \quad \ldots.(4.2)$$

4.2. Calculations Based on Doping Concentration(N_B)

The values for different parameters mentioned above are for different values of doping are calculated:

4.2.1. Calculation of Mobility, μ (cm^2/Vs)

In the relation from equation (3.10):

$$\mu = \frac{C\left(\frac{N}{N_{ref}}\right)^{\alpha-\delta} + \mu_{max}}{1 + \left(\frac{N}{N_{ref}}\right)^{\alpha}} \ cm^2/Vs$$

Considering N_{ref} = 3 × 10^{16} cm^{-3}, μ_{max} = 650 cm^2/Vs, C = 330 cm^2/Vs, α = 0.2, and δ = 0.8, and substituting in equation 3.10, we obtain different values of mobility for different N_B.

4.2.2. Calculation of Bulk Potential, $2\phi_F$ (volts)

Since $\phi_F = \frac{KT}{q} \ln \frac{N_B}{n_i}$ …..(4.3)

Where k = 1.38× 10^{-23} J/K (Boltzmann's constant) and T is temperature

$\frac{KT}{q}$ = 0.026 at T=300 Kelvin

Using n_i = 6.9 (from Table 2.1) and substituting different values of N_B, we obtain the bulk potential.

4.2.3. Calculation of Transconductance parameter, β_o

$\beta_o = \frac{W\mu C_{ox}}{L}$ ….(4.4)

we consider the device dimensions $\frac{W}{L}$ and oxide thickness constant.

Active channel length = 2μm, channel width = 100μm, oxide thickness = 0.1μm

Since $C_{ox} = \frac{\epsilon_{ox}}{t_{ox}}$ ….(4.5)

Substituting t_{ox} = 0.1×10^{-4} cm, ϵ_{ox} = 3.9 ×8.85×10^{-14} F/cm in eq. (4.5), we obtain C_{ox} = 0.034 × 10^{-6} F

Now substituting the value of C_{ox}, $\frac{W}{L}$, and different values of mobility calculated in section 4.2.1 in the equation (4.4), we obtain the different transconductance parameters.

4.2.4. Calculation of Body effect term, γ

$\gamma = \frac{\sqrt{2.\varepsilon_{3c-sic}.q.N_B}}{C_{ox}}$ …..(4.6)

Substituting the values of parameters calculated above in equation (4.6), we obtain different values of γ for different N_B.

The calculated values are listed in the Table 4.1.

Table 4.1: Values of different parameter for different doping

N_B (cm^{-3})	μ (cm^2/Vs)	V_{FB}(volts)	$2\phi_F$ (volts)	β_o	γ
5×10^{14}	654	0.2088	1.65	1.131×10^{-3}	0.347
10^{15}	650	0.2268	1.69	1.124×10^{-3}	0.491
5×10^{15}	620	0.2683	1.77	1.072×10^{-3}	1.098
10^{16}	580	0.2863	1.81	1.005×10^{-3}	1.55
5×10^{16}	440	0.3278	1.89	0.759×10^{-3}	3.46
10^{17}	368	0.3458	1.93	0.635×10^{-3}	4.9
5×10^{17}	232	0.3873	2.01	0.4×10^{-3}	10.96
10^{18}	192	0.4053	2.05	0.331×10^{-3}	15.51

4.3 Plots showing the variation of device parameters with Doping concentration.

4.3.1 Mobility vs Doping Concentration

As per the values obtained above, it is clear that the mobility decreases with increase in impurity concentration. The Figure 4.1 demonstrates the values of mobility with respect to the doping concentration as listed in Table 4.1.

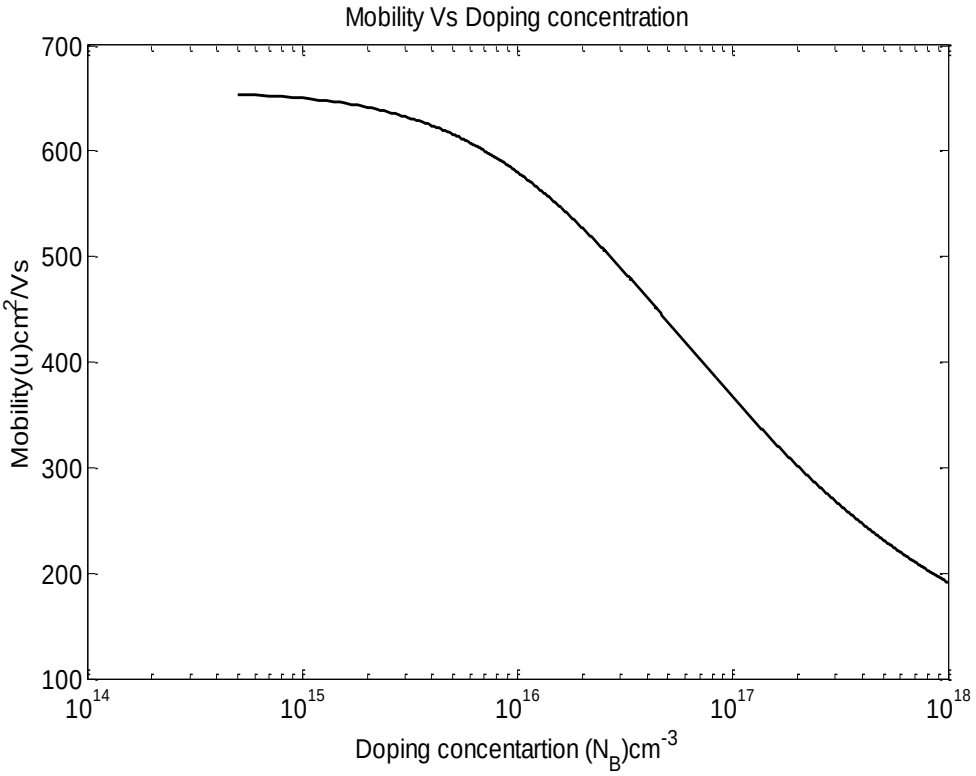


Fig 4.1: Mobility vs Doping concentration

4.3.2 Flat Band Voltage Vs Doping Concentration

Flat band voltage increases with increase in doping concentration. This is shown in Figure. 4.2.

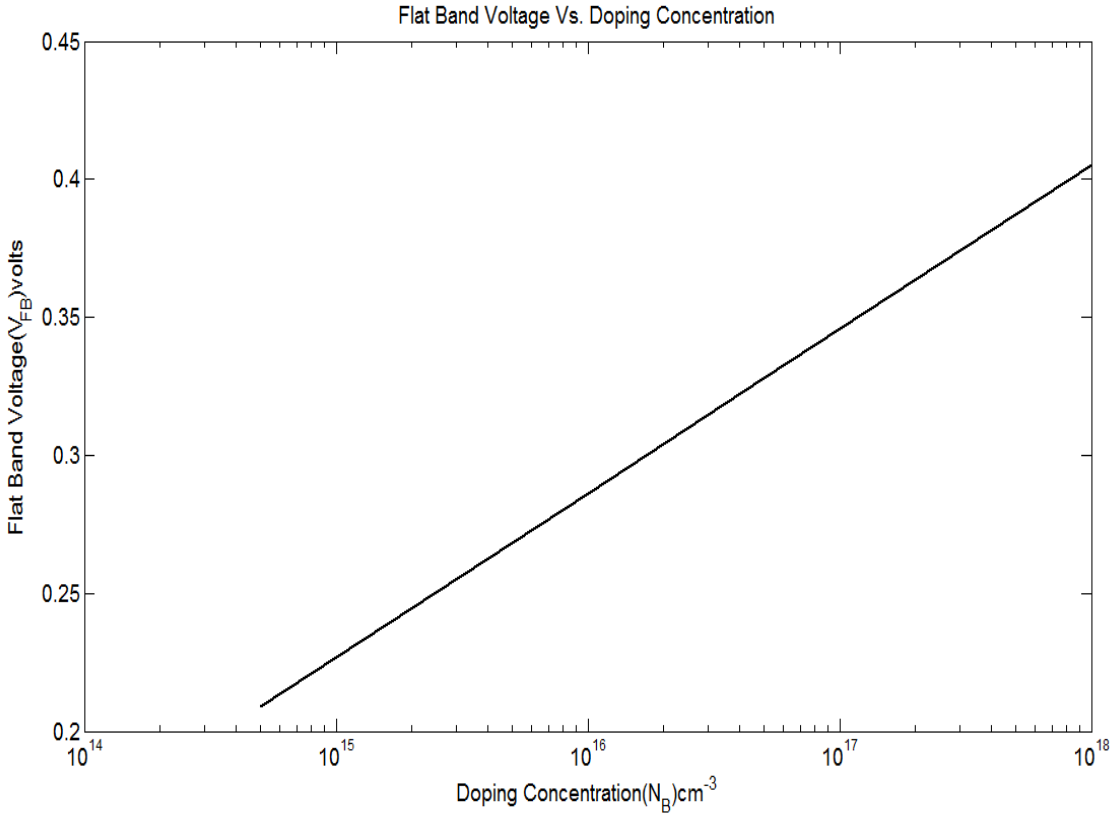


Fig 4.2: Flat Band Voltage vs Doping Concentration

4.3.3 Bulk Potential vs Doping Concentration

Bulk potential also increases with increase in Doping concentration. This is depicted in Figure. 4.3.

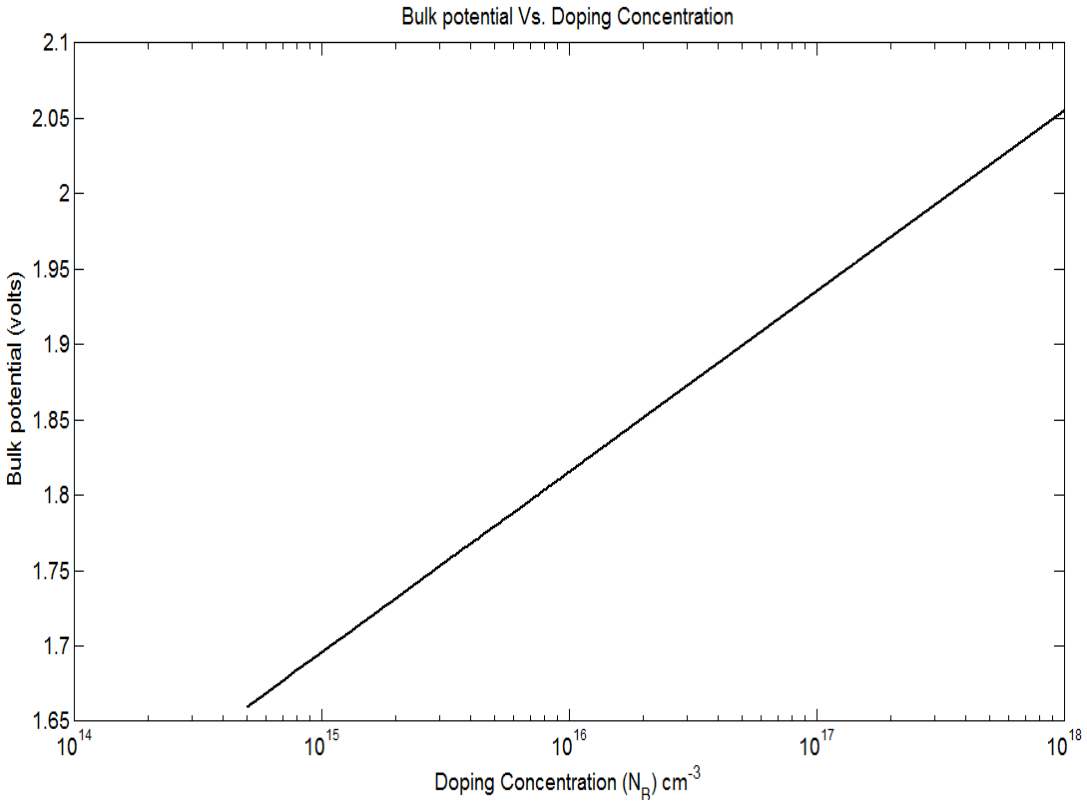


Fig 4.3: Bulk potential vs doping concentration

4.4. I-V Characteristics of LDMOS at different N_B and fixed V_{GS}

The current in LDMOS is calculated using values mentioned in Table 4.1 for different values of doping concentration (N_B) using equation (4.1) and (4.2). V_{GS} assumed is 25V. Figure. 4.4 shows the I-V characteristics of the device at different doping concentration and at fixed V_{GS} = 25V.

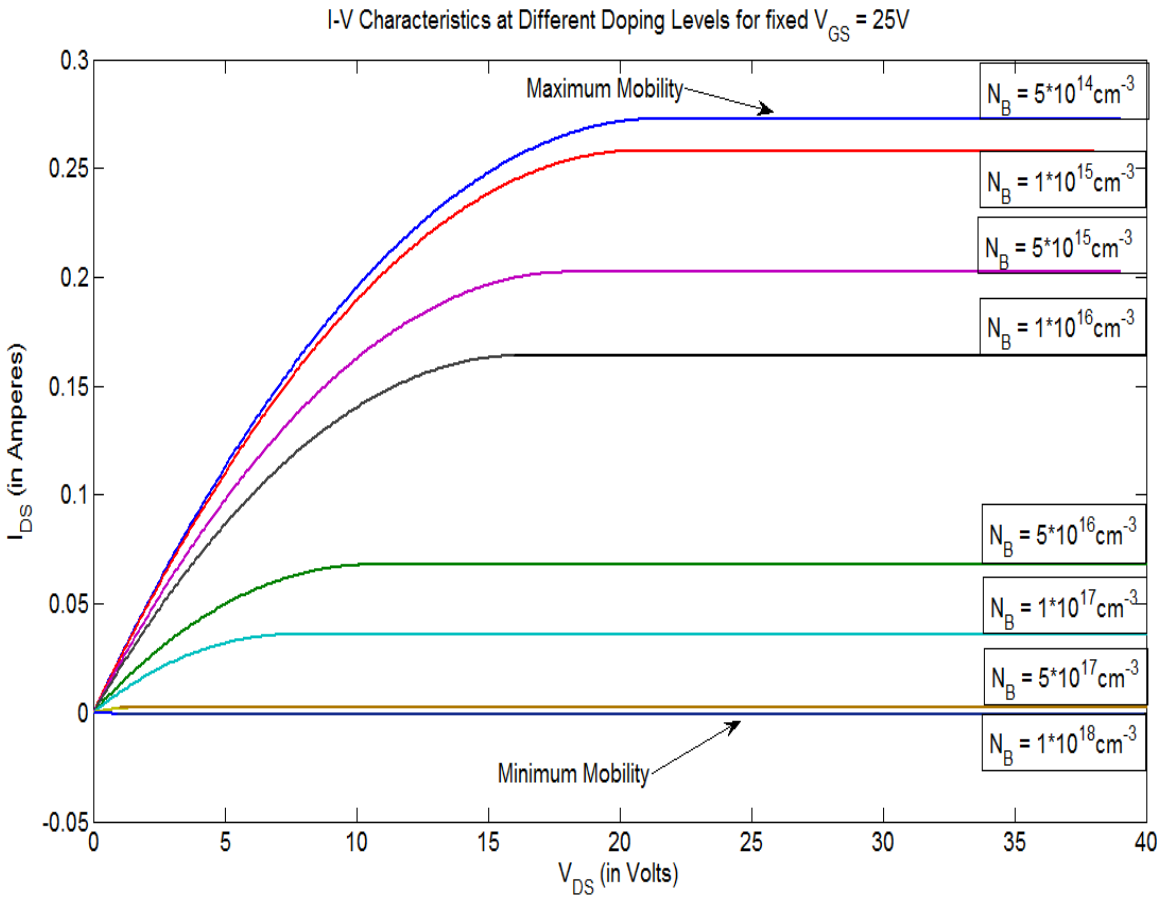


Fig 4.4: I-V characteristics at different doping levels for fixed V_{GS}=25V

From the Table 4.1, we find that when N_B increases, mobility decreases whereas the bulk potential, Flat band voltage and the body effect term increases. From the I-V characteristics shown above, it is evident that the effect of mobility decrement is dominant on the drain current I_{DS} that the effect of other parameters increment. As shown above the drain current I_{DS} is maximum at minimum impurity concentration since mobility is maximum there.

CHAPTER-5
CURRENT ENHANCEMENT BASED ON FIXED OXIDE CHARGE INSIDE SIO_2 LAYER.

5.1 Ways of improving current

From equation (4.1):

$$I_{DS} = \beta_o \left\{ [V_{GS} - (V_{FB} + 2\phi_F)]V_{DS} - \frac{1}{2}V_{DS}^2 \ - \frac{2}{3}\gamma \left[(V_{DS} + V_{SB} + 2\phi_F)^{\frac{3}{2}} - (V_{SB} + 2\phi_F)^{\frac{3}{2}} \right] \right\}$$

Drain current I_{DS} can be improved by:

- Increasing mobility, μ.
- Decreasing Bulk potential, $\phi_{F.}$
- Decreasing Flat band voltage, V_{FB}.
- Decreasing body effect term, γ.
- Decreasing transconductance parameter, β_o.

Since the device dimensions and oxide capacitance are considered constant, body effect term, γ, transconductance parameter, β_o cannot be altered. Also, mobility, bulk potential depend upon the doping concentration which is being varied. The drain current, I_{DS} can be improved if the flat band voltage is decreased. Flat band voltage can be decreased by taking into account the effect of fixed oxide charges present in the SiO_2 layer.

Since flat band voltage is given by:

$$V_{FB} = \phi_{ms} - \frac{Q_f}{C_{ox}} - \frac{Q_{ot}}{C_{ox}} - \frac{Q_{it}}{C_{ox}} \qquad \text{....(5.1)}$$

It can be reduced by considering Q_f. Fixed oxide charge density trapped in SiO_2 over 3C-SiC substrate is given by[23]:

Fixed charge density, N_{ox} for n-type 3C-SiC has been taken to be $4 - 9 \times 10^{11}$ cm^{-2}

Fixed oxide charge Q_f can be calculated as:

$$Q_f = q \times N_{ox}$$

With charge, $q = 1.69 \times 10^{-19}$ Coulombs

Table 5.1: fixed oxide charge as per N_{ox}

N_{ox} (cm^{-2})	Q_f (C/cm^2)
4×10^{11}	6.76×10^{-8}
5×10^{11}	8.45×10^{-8}
6×10^{11}	10.14×10^{-8}
7×10^{11}	11.83×10^{-8}
8×10^{11}	13.52×10^{-8}

5.2 Calculation of V_{FB} and V_{Dsat}

Using the values of fixed oxide charge, new set of flat band voltage, V_{FB} and the corresponding V_{Dsat} is calculated from equation (4.2) and (5.1). The calculated values are listed as under in Table 5.2.

Table 5.2: calculated values of V_{FB} and V_{Dsat} after considering the effect of fixed oxide charge.

$N_B = 10^{15}$ cm^{-3}, V_{FB} = 0.2268V			**$N_B = 10^{17}$ cm^{-3}, V_{FB} = 0.3458V**		
Q_f	**V_{FB} (new)**	**V_{Dsat} (volts)**	**Q_f**	**V_{FB} (new)**	**V_{Dsat} (volts)**
6.76×10^{-8}	-1.72	22.63	6.76×10^{-8}	-1.6	9.1
8.45×10^{-8}	-2.17	23.05	8.45×10^{-8}	-2.09	9.4
10.14×10^{-8}	-2.7	23.56	10.14×10^{-8}	-2.58	9.5
11.83×10^{-8}	-3.17	24	11.83×10^{-8}	-3.06	9.6
13.52×10^{-8}	-3.6	24.41	13.52×10^{-8}	-3.5	9.7

5.3. Related Graphs Showing the Current Enhancement

Using the values of V_{FB} and V_{Dsat} as listed in Table 5.2 , current I_{DS} is calculated from equation (4.1) and a graph is plotted showing I-V characteristics with improvement in current, for $N_B = 10^{15}$ cm^{-3} and 10^{17} cm^{-3} in each case. These are shown in Figures 5.1 and 5.2 respectively. The combined results are shown in Figure 5.3.

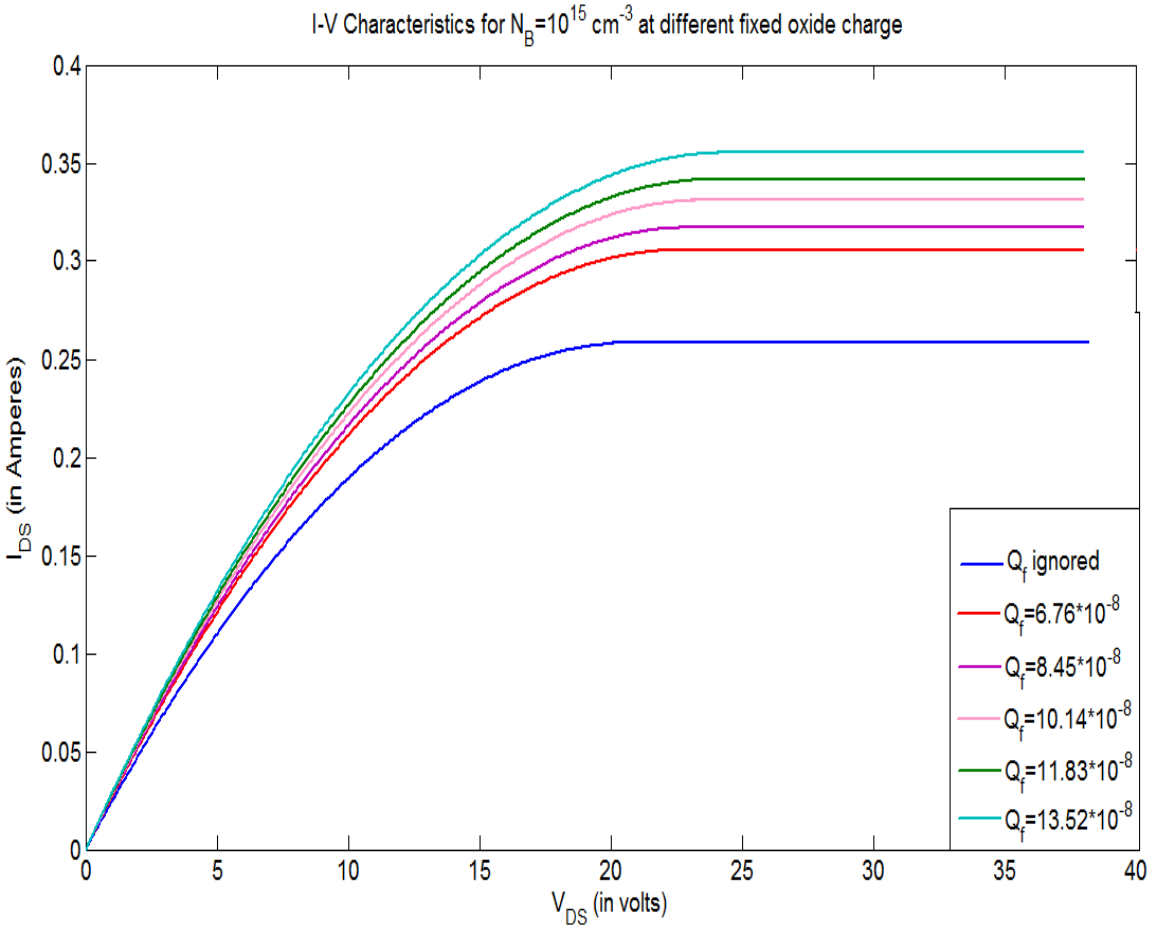


Fig 5.1: I-V Characteristics for $N_B=10^{15}cm^{-3}$ at different fixed oxide charge

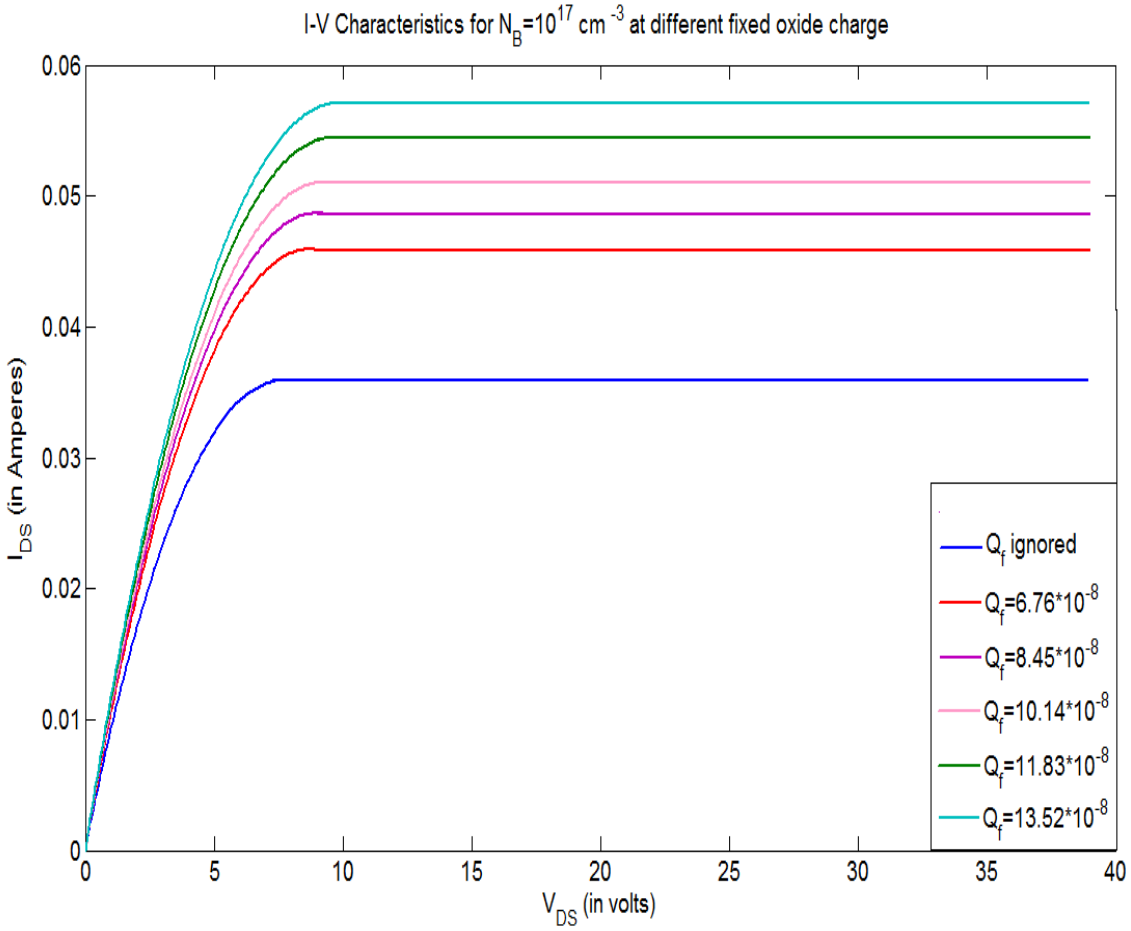


Fig 5.2: I-V Characteristics for $N_B=10^{17}cm^{-3}$ at different fixed oxide charge

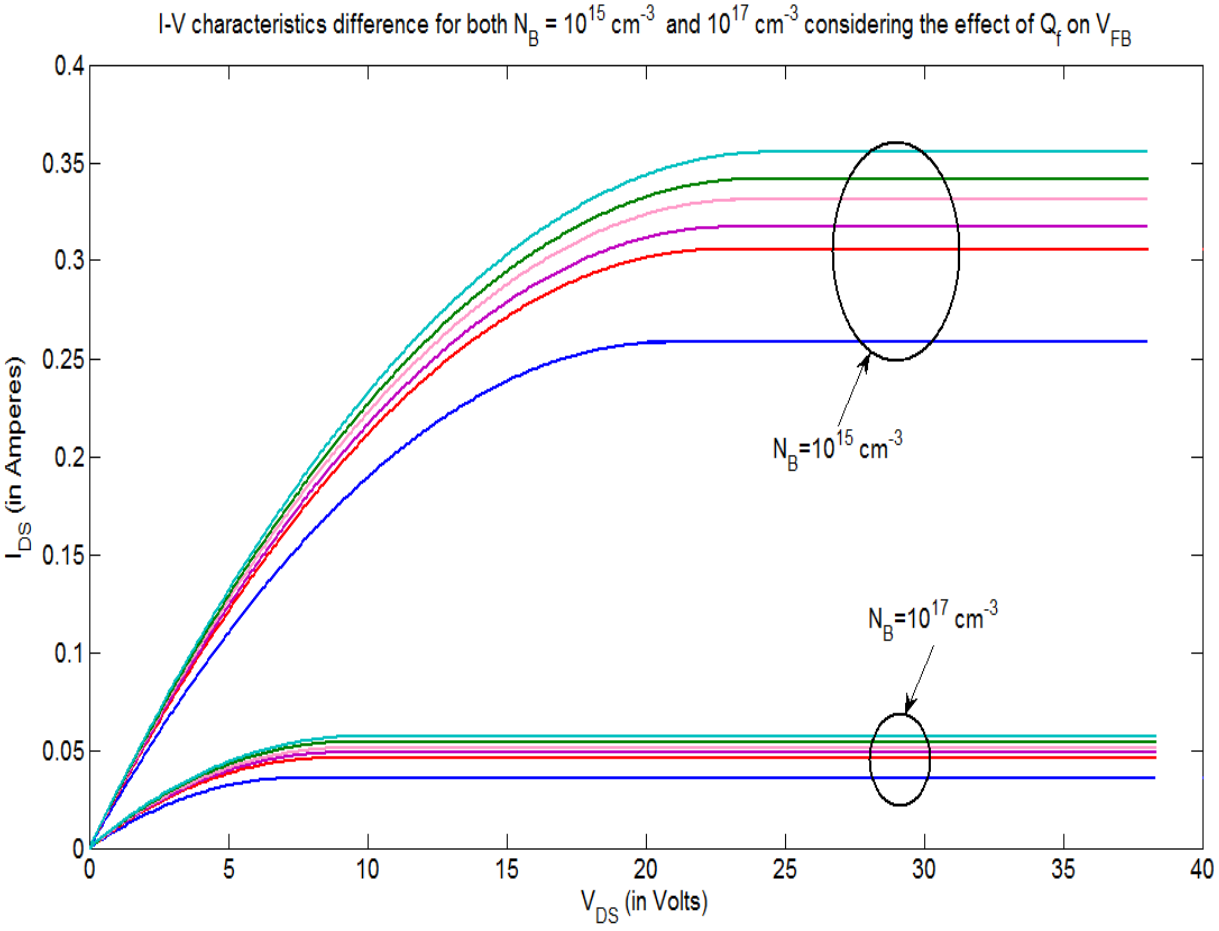


Fig 5.3: I-V Characteristics difference for both $N_B = 10^{15}$ and $N_B = 10^{17}$ cm^{-3} considering the effect of Q_f on V_{FB}

Using the results shown in Figures 5.1 to 5.3, the plots for the percentage increase in the drain current I_{DS} with respect to fixed oxide charge were obtained and are shown in Figures 5.4 and 5.5 respectively.

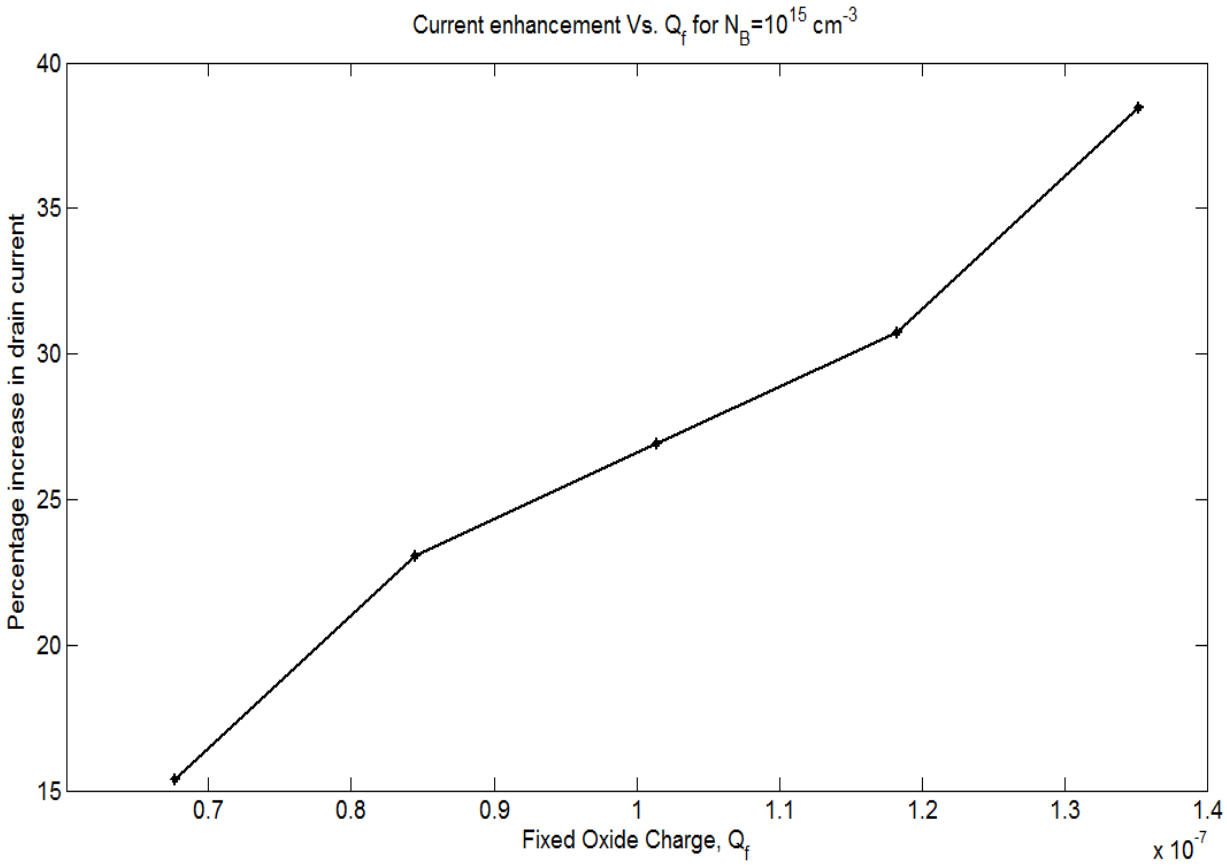


Fig 5.4: Percentage Current Enhancement vs Q_f for $N_B=10^{15}cm^{-3}$.

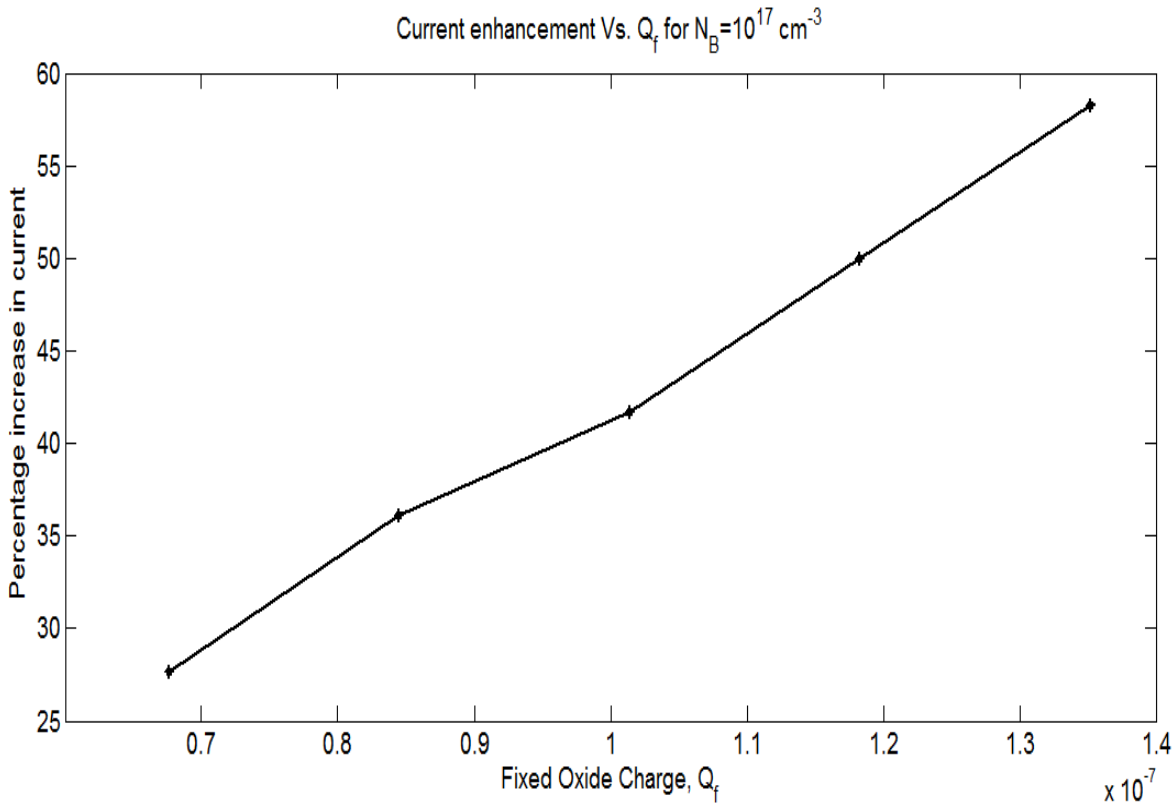


Fig 5.5: Percentage Current Enhancement vs Q_f for $N_B=10^{15}cm^{-3}$

CHAPTER-6

CONCLUSION AND FUTURE WORK

With power devices, we are concerned with their ability to work under high temperature, have high breakdown voltage, low on resistance and ability to switch larger currents. This thesis work provides a novel way to achieve larger currents through the device LDMOS by considering the effect of fixed oxide charge on the flat band voltage.

Analysis of I-V characteristics show that LDMOS can block high drain voltages without the need of thick epilayer. Under reverse bias, the depletion region surrounding the p-well first punches through the insulating SiC substrate, then continues moving laterally towards the drain. The lateral extent of the depletion region is therefore not limited by the epilayer thickness.

After calculating the values of device parameters, it was found that the electron mobility decreases with increase in doping concentration. However, it was noticed that the flat band voltage and bulk potential showed an increment with increase in the doping concentration.

Assuming V_{GS}=25V, I-V characteristics were obtained for N_B ranging from 5×10^{14} to 10^{18} cm^{-3}. It was observed that the drain current I_{DS} was maximum (0.27A) for minimum N_B (5×10^{14} cm^{-3}) and minimum (0.001A) for maximum N_B (10^{18} cm^{-3}).

From the drain current equation (4.1), ways of improving the drain current were presented in section 5.1 of chapter-5. There exists a trade off between mobility(μ) and bulk potential(ϕ_F) and Flat band voltage(V_{FB}) , since one increases and others decrease with increase in doping concentration.

The fixed oxide charge is calculated in section 5.1 of chapter-5 using the fixed oxide charge density given by[23]. Considering fixed oxide charges (Q_f) and ignoring oxide trapped (Q_{ot}) and interface trapped charges (Q_{it}), new flat band voltage was calculated using equation (5.1). Furthermore, the drain to source saturation voltage V_{Dsat} was calculated using equation (4.2) and listed in Table 5.2.

The newly obtained drain to source Saturation voltage V_{Dsat} was used to find the drain current I_{DS} from equation (4.1). Two values of doping concentration were selected which are $N_B = 10^{15}$ cm^{-3} and $N_B = 10^{17}$ cm^{-3} and I-V characteristics showing the current enhancement were obtained in sub-section 5.3.1 and 5.3.2 of chapter-5.

It was observed that the drain current I_{DS} showed improvement from 0.26A to 0.3A

for $N_B = 10^{15}cm^{-3}$ at fixed oxide charge = 6.76×10^{-8} C/cm^2 (by approximately 15%) and from 0.035A to 0.044A for $N_B = 10^{17}cm^{-3}$ at fixed oxide charge = 6.76×10^{-8} C/cm^2 (by approximately 26%).

For future work, the fixed oxide charges present in the oxide layer can be considered beneficial for obtaining larger current through LDMOS. This study provides the researchers an insight into the benefits of the presence of fixed oxide charges in the oxide layer through which larger drain current can be obtained.

REFERENCES

[1] B. J. Baliga, "The Future of Power Semiconductor Device Technology," *Proc.IEEE,* vol. 89, no. 6, pp. 822-832, 2001.

[2] http://www.ecn.purdue.edu/WBG/SiC, Data Bank, Introduction, Basic Studies, Device Research: From the Purdue's Wide band Gap Semiconductor Device Research in Electrical and Computer Dept., America.

[3] Munish Vashishath and Ashoke K. Chatterjee, "Recent trends in silicon carbide device research" Mj. Int. J. Sci. Tech. 2008, 2(03), 444-470.

[4] Y.M. Tairov and V.F. Tsvetkov, "Investigations of growth processes of ingots of silicon carbide single crystals," J. Cryst. Growth, 1978, 43, 209-212.

[5] Byeung Chul Kim, "Electrical characterisation of Schottky barrier diodes on heteroepitaxial 3C-SiC grown on Si substrates" MS Thesis, Purdue University,2008,pp 2-4

[6] Tesfaye Ayalew , "Numerical Simulation of SiC devices" Phd Dissertation, Institute of Microelectronics, TU, Vienna, Austria, 2007 ,pp.6-250.

[7] E.Arnold and D.Alok, "Effect of interface states on electron transport in 4H-SiC inversion layers" *IEEE Trans. Elect. Dev.* 48, 1870, (2001).

[8] R.Y Lakshman, "A Process for hydrogenation of silicon carbide crystals", MS. Thesis, 2001, Mississipi State University, USA

[9] M. Bhatnagar and B. Jayant Baliga, "Comparisons of 6H-SiC, 3C-SiC and Si for Power Devices," IEEE Trans. Electron Devices, Vol. 40, No. 3, March 1993

[10] S. M. Sze, "VLSI Technology," 2nd edition TMH, New Delhi.

[11] J. W. Palmour, R. Singh, R. Glass, O. Kordina, and C. H. Carter, Jr., "Power Semiconductor Devices and IC's," in Proceedings of the International Symposium on Power Semiconductor Devices and ICs, pp. 25-32, 1997.

[12] A. Itoh, T. Kimoto and H. Matsunami, “Excellent reverse blocking characteristics of high voltage 4H-SiC Schottky rectifiers with boron implanted edge termination”, IEEE Electron Device Lett., 1996, 17, 139-141.

[13] Stephen E. Saddow, Anant Agarwal, “Advances in Silicon Carbide Processing and Applications”

[14] Munish Vashishath and A. K. Chatterjee, “Theoretical analysis and design of double implanted MOSFET on 6H silicon carbide wafer for low power dissipation and large breakdown voltage”, Mj. Int. J. Sci. Tech. 2008, 2(02), 308-319.

[15] Tesfaye Ayalew, Jong-Mun Park, Andreas Gehring, Tibor Grasser and Siegfried Selberherr, “Silicon Carbide Accumulation-Mode Laterally Diffused MOSFET”, European Solid-State Device Research, 2003 33rd Conference on. ESSDERC’03, 581-584, 2003.

[16] J.Spits, M.R.Melloch, J.A.Cooper, Jr. And M.A.Capano,"High-Voltage (2.6kV) Lateral DMOSFETs in 4H-SiC," IEEE Electron Device Lett., 19,100(1998).

[17] L.Yuan, M.R.Melloch, J.A.Cooper and K.J.Webb, "Silicon Carbide IMPATT Oscillators for High-Power Microwave and Millimeter-Wave Generation”, IEEE Cornell Conference on Advanced Concepts in High Speed Semiconductor Devices and Circuits, Ithaca, NY,August7-9,2000.

[18] W.Xie, J.A.Cooper, M.R.Melloch, J.W.Palmour and C.H.Carter, Jr., "A Vertically Integrated Bipolar Storage Cell in 6H Silicon Carbide for Nonvolatile Memory Applications" IEEE Electron Device Lett., 15,212(1994).

[19] M. D. Pocha and R. W. Dutton, “A computer –Aided Design Model for High-Voltage Double Diffused DMOS Transistor,” IEEE Trans. Solid state circuits, Vol. Sc-11, No. 5, Oct. 1976.

[20] S. M. Sze, “Physics of Semiconductor Devices,” 2nd ed., Wiley-Interscience, New York.

[21] Yannis Tsividis, “Mixed Analog-Digital VLSI Devices and Technology”,World Scientific, Singapore, 1996.

[22] A. D. Sedra and K. C. Smith, “Microelectronics Circuits,” Oxford University Press Inc., New York, 2004

[23] Gary Lynn Harris, “Properties of Silicon Carbide”, INSPEC, Institution of Electrical Engineers, London, IET, 1995.

[24] Mietek Bakowski, Adolf Schöner, Per Ericsson, Helena Strömberg, Hiroyuki Nagasawa, and Masayuki Abe, “Development of 3C-SiC MOSFETs**”,** Journal of Telecommunication and information Technology,2/2007.

[25] Matthias Roschke, Frank Schwierz, “Electron Mobility Models for 4H, 6H, and 3C-SiC”, IEEE transactions on electron devices, 2001