`

DEVELOPMENT OF LOW TEMPERATURE OXIDATION PROCESS USING OZONE FOR VLSI

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requirements for the award of the degree of

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VLSI Design

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CERTIFICATE

I hereby declare that the work which is being presented in the dissertation entitled, **"DEVELOPMENT OF LOW TEMPERATURE OXIDATION PROCESS USING OZONE FOR VLSI"** in partial fulfillment of the requirement for the award of degree of Master of Technology (VLSI Design) at the Department of Electronics and Communication Engineering, Thapar University, Patiala, is an authentic record of my own work carried out under the supervision of Dr. Ajay Kakkar, Assistant Professor, ECED.

The matter presented in this dissertation has not been submitted in any other University/Institute for the award of any other degree.

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ABSTRACT

With decreasing size of MOS transistor the thickness of gate oxide (SiO_2) is reaching in regime where it is just 2-3 atomic layers thick. It is about 1 to 1.5 nm thick and due to thin oxide layers there is direct tunneling of charge carriers through gate oxide, and the transport of charge carriers through defects in gate oxide. The increasing leakage current through gate oxide is proving to be a showstopper to the scaling of MOS transistor, and saturating the

Moore's Law. For the applications, where the devices are need to be fabricated on plastic, glass or poly-crystalline silicon substrates a good quality of oxide is required to be grown at low temperatures. In this work, a low temperature, defect free oxide growth technique using ozone is presented. The effect of various ambient temperatures on growth of SiO_2, the effect of pre cleaning and passivation on quality of ozone grown oxide in terms of bulk defect density, Si-SiO_2 interface trap charge density and on oxide life time as been studied. In this thesis, we are designing a 8-Bit ring oscillator using FinFETs in which ring oscillators has been designed using ozone oxidized FinFETs and without ozone oxidized FinFETs.While comparing the results we found that the ring oscillator using ozone oxidized FinFETs shows significantly better results as compared to ring oscillator without ozone oxidized FinFETs and thus the application of ozone in VLSI has been described and justified. The design layout is prepared on the tool LASI and the application of ozone on the design is done through CADENCE tool and finally the simulation and results on MATLAB 7.0 is carried out. The technology used is 60 nm.

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ABBREVIATIONS

AR	Aspect Ratio
IC	Integrated Circuit
LSI	Large Scale Integration
CMOS	Complementary Metal Oxide Semiconductor
O_3	Ozone
VLSI	Very Large Scale Integration
FET	Field Effect Transistor
GSI	Giga-Scale Integration
GaAs	Gallium Arsenide
GHz	Giga Hertz
MOSFET	Metal Oxide Semiconductor Field Effect Transistor
MSI	Medium Scale Integration
TCOs	Transparent Conducting Oxides
RC	Resistance-Capacitance
RLC	Resistance-Inductance-Capacitance
SPICE	Simulation Program with Integrated Circuit Emphasis
InGaZnO	Indium Gallium Zinc Oxide
-OH	Hydroxyl Ions
-H	Hydrogen Ions
PVD	Physical Vapour Deposition
MuGFET	Multi-gate Field Effect Transistor

SADP	Self Aligned Double Patterning
BOX	Buried Oxide
MIGFET	Multigate Independent Gate Oxide
SONOS	Silicon-Oxide-Nitride-Oxide-Silicon
FDSOI	Fully Depleted Silicon On Insulator
LASI	Layout System for Individuals
CMP	Chemical Mechanical Polishing
PDSOI	Partially Depleted Silicon On Insulator
RF	Radio Frequency
LO	Local Oscillator
SRAM	Static Random Access Memory

CHAPTER

1

Introduction

This chapter includes various advantages and applications of ozone in VLSI. After studying various advantages of ozone, the detailed explanations of the various processes using ozone in VLSI has been discussed.

1.1. OXIDATION

Oxidation is a process in which oxygen is added to a compound. It is the loss of electrons during a reaction by a molecule, atom or ion. It occurs when the oxidation state of a molecule, atom or ion is increased [8]. An older meaning of oxidation was when oxygen was added to a compound. Example: Iron combines with oxygen to form iron oxide or rust [11]. The iron is said to have oxidized into rust.

1.2 WHAT IS OZONE?

Ozone is a commonly found constituent in the air. At the point when an atom of Oxygen (O_2), is bound by means of oxidation to a third oxygen atom, it gets to be ozone (O_3). It is an unstable somewhat blue water-dissolvable gas with an extremely trademark fragrance that is not difficult to perceive [3]. In low levels; it makes the air smell new/fresh and its colour makes the sky blue. It inactivates microorganisms and infections 3,125 times quicker and is a 50% stronger oxidizer than chlorine. It is made electronically or through ultraviolet light changes over particles of oxygen into atoms of ozone, referred as activated oxygen. Present day engineering makes ozone generators more cost effective [2]. Ozone is also presently used in the field of electronics and communication and helps in improving various the characteristics of the electronics in this modern era.

1.3 ADVANTAGES OF OZONE IN VLSI

Ozone has a solid oxidizing power and is regularly used in waste medication and drinking water

cleansing commercial enterprises. As of late, ozone has been presented in semiconductor wet cleaning techniques which pulls in and expands enthusiasm toward ozone, since the technology has proven highly promising for industrial application by meeting many aspects of the various needs[2]. The ozone-developed oxide was likewise found to show enhanced interface and electrical attributes over a traditionally dioxygen grown oxide.

1.4 VLSI (VERY LARGE SCALE INTEGRATION)

Very-large-scale integration is the process which consists of an integrated circuit using thousands of transistors. It began when complex semiconductor and communication technologies were being developed in early 1970s. The most commonly used VLSI device is the microprocessor. VLSI technology was introduced to enhance the limited set of functions of the ICs[29]. RAM, ROM, CPU and other glue logic were the main components used in the electronic circuits. All these components of ICs were integrated into a single chip because of VLSI. This method essentially

1) Reduces the size of the device.
2) Reduces the cost of the device.
3) Reduces the current consumption.
4) Increases the speed of operation.
5) Low Power.

To meet present day needs in the electronics era, millions and millions of transistors are staged in an IC chip which is about to function as per its best performance and efficiency which also meets the present day needs in the electronic era. Scalable devices are produced by researchers which work at several nanometers (nm) technology with the upcoming time[13]. The complexity, density or functionality of integration of ICs is described by using various terms such as LSI (large-scale integration, 10^4 transistors on a chip), VLSI (very large-scale integration, 10^6 transistors on a chip), ULSI (ultra-large-scale integration), and GSI (giga-scale integration). Circuits and technologies of wide ranges of size and complexity which simply mean ―large ICs are described by these above given terms.‖

1.5 USE OF OZONE FOR VLSI CARRIED OUT AT LOW TEMPERATURE OXIDATION PROCESS

Conventionally, molecular oxygen is used to grow the SiO_2 layer. In this process the silicon wafer is subjected to high temperature (900 °C – 1200 °C). Due to this high temperature, a lot of thermal stress exerts on the wafer which in return alters doping profile and causes the elevated thermal budget. However, this high temperature in conventional process of oxidation cannot be applied to the modern substrates such as plastics and glass. Therefore new oxidation method is required to be developed which is feasible at lower temperature and to reduce the thermal stress on the wafer and to reduce processing cost. Ozone is a tri-atomic allotrope of oxygen, which has symmetrical bent structure with an angle of $116^0 49'$, and equal oxygen-oxygen bond length of 0.128 nm [1]. It is characterized as a double bond with bond order of 1.7, because in this O-O bond length is shorter than that in H_2O_2 and O_2 [3]. The high reactivity of ozone [8] makes it is a proposed oxidant [12] and helps it to grow high quality SiO_2 film at low temperatures. It leads to overcome issues associated with thermal oxidation. A molecular oxygen and an atomic oxygen are generated because of decomposition of ozone layer as in chemical reaction. These are powerful oxidizing agent [8] which can even oxidize hydrogen passivated silicon whereas diatomic oxygen can never oxidize it at comparable temperatures [9]. SiO_2 (ozone-oxide) progresses in layer-by-layer fashion over an atomic flat silicon, and thus giving quality Si-SiO_2 .

1.6 OXIDATION OF SILICON

In ICs, silicon dioxide is used for several purposes, ranging from serving as a mask against dopant introduction into silicon to serving as the most critical component in the metal-oxide-semiconductor transistor. SiO_2 layers of precisely controlled thickness are produced during IC fabrication by reacting Si with either oxygen gas or water vapor at an elevated temperature [3]. In either case the oxidizing species diffuses through the existing oxide and reacts at the Si–SiO_2 interface to form more SiO_2.

Water vapor diffuses through SiO_2 faster than oxygen. Wet oxidation is performed by bubbling a carrier gas (Ar or N_2) through water in a heated flask or by burning O_2 and H_2 to form H_2O at the input to the tube. In a production framework, procedures, for example, wafer stacking, insertion into the heater, sloping of the heater temperature, and gas control are all mechanized [7]. The thickness of the oxide become relies on upon the heater temperature, the oxidation time, the ambient gas, and the Si surface orientation. Delegate dry and wet oxidation development curves are indicated in figure as given underneath. Wafers utilized as a part of IC creations are prevalently cut in the (100) plane on the grounds that the interface trap

thickness is low because of the low thickness of unsaturated bonds in this plane in respect to alternate planes. Additionally, the electron surface mobility is high i.e.102 [14].

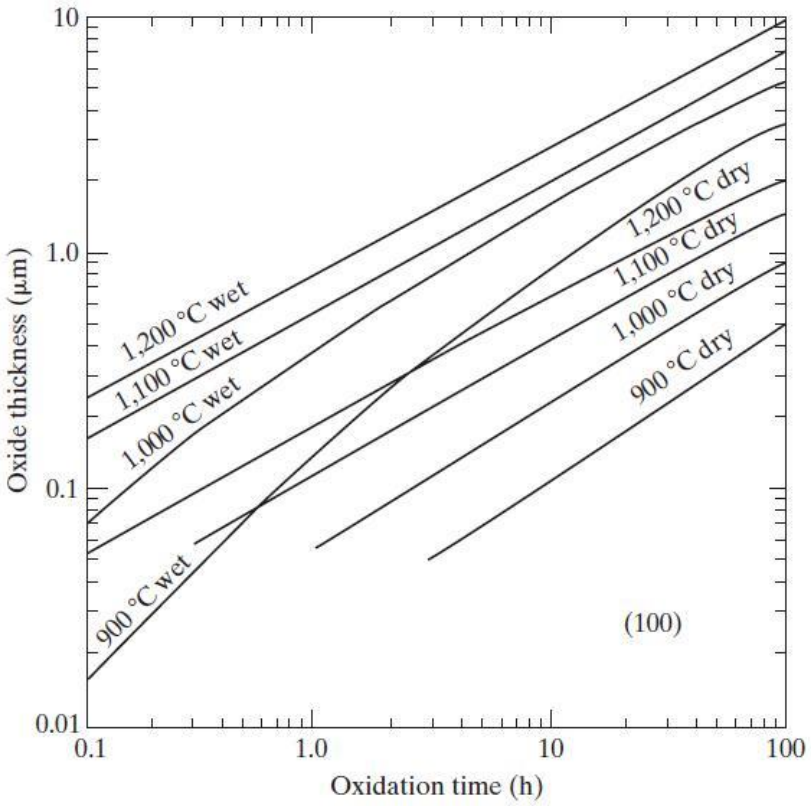

Figure 1.1 SiO2 thickness formed on (100) silicon surfaces as a function of time [4].

1.6.1 DRY OXIDATION

Dry oxidation or HCl dry oxidation is straight forward connected utilizing microprocessor controlled supplies. The desired insertion and withdrawal rates incline rates, gas streams, and temperatures are all programmable [11]. Care must be taken in in handling HCl, particularly with the fumes, in light of the fact that HCl erodes metal parts. Likewise amounts of traces of water vapor can radically influence the oxidation rate**.**

1.6.2 WET OXIDATION

Wet oxidation can be carried out traditionally by the pyrogenic procedure, which responds H_2 and O_2 to form water vapor. The microprocessor controls the H_2/O_2 mixture [11]. The pyrogenic procedure guarantees high-purity steam, provided high-purity gasses are utilized [6]. In the event that wet oxidation by the bubbler system is utilized, a carrier gas is typically flowed through a water bubbler kept up at 950 ^{o}C. This temperature relates to a vapor pressure of roughly 640 Torr.

1.7 MOTIVATION

The oxidation process of silicon is the heart of all the fabrication steps followed in creating a MOSFET and makes a MOSFET practical. At the same time with the progression in the IC innovation and lessening size of MOSFET's this critical SiO_2 is getting thinner and thinner. The thickness of SiO_2 at present needed is short of what 1 nm [1], which is only 3 monolayer of SiO_2 (1 monolayer ~ 0.3nm). For the performance assessment MOSFETs, the most essential factor is the current present in between of source and channel, which the transistor can drive. More current demonstrates that the transistor could be worked quicker and all the parasitic capacitances and resistances inside that transistor are having a lesser effect on the performance demanded from the transistor. From the basics of the MOSFET operation; we know there are two voltages accessible to control the operation of the MOSFET. Firstly, the gate voltage, connected between source terminal and substrate differentiated by a dielectric material to structure a parallel plate capacitor type arrangement, and the accumulation or inversion of charge carriers is induced in the substrate on its application [18]. The higher value of capacitance signifies more inversion of charge carriers in the semiconductor channel for the same applied voltage. And the second one is the voltage, which we apply between source and drain, which is accountable for driving the induced charges forward in the channel. Thus SiO_2 is the dielectric material, which made FET transistors to work in silicon technology [19]. Here some of the most significant properties of SiO_2 are as follows:

a. The high quality interface between Si and SiO_2.

b. Chemical and thermal stability at high temperature (~1000^{0}C).

c. Great quality of insulation.

d. The hard mask in different diffusion and doping process.

e. High breakdown fields of 13 MV/cm.

1.8 ADVANTAGES OF OXIDATION BY OZONE

The high reactivity of O_3 gives a faster oxidation rate, which allows the silicon oxidation to proceed at much lower temperatures. Second, the oxidation rate in O_3 was found to be independent of silicon's crystallographic orientation. Finally, the ozone grown oxide film yields a Si/SiO_2 interface of higher quality than a conventionally grown oxide film (800–900 °C). The enhancement in the SiO_2 quality and thickness uniformity and the reduction in the thermal budget are achieved because of the fact that ozone is more reactive oxidant than oxygen. It is also contemplated that during ozone generation, free radicals and other activated species may be formed which are more reactive oxidants than oxygen and these assist in oxidation of silicon.

1.8.1 FAST OXIDATION AT LOW TEMPERATURES

Originally, O_3 has been used as the more reactive oxidant to increase the oxidation rate and thus which lower the oxidation temperature [3]. By adding photo generated O_3 (UV/O_2 with 2.25 ppm O_3) to the O_2 gas at oxidation temperatures of 700–800 °C the oxide film was for the same oxidation time 50–100% thicker than in pure O_2 [5]. At higher ozone concentrations (BDO, O_3) and at lower temperatures (400–800 °C) this growth enhancement was even more pronounced [6] and was study the silicon oxide growth in O_2 and O_3 (5%)/O_2 (generated by a discharge ozonizer, BDO) found to increase with lower oxidation temperatures (e.g. at 400 °C the O_3/O_2 gas formed an oxide film which was 400% thicker than in pure O_2 [6]). Thus, at a temperature of 550 °C oxidation in O_3 gave a comparable growth rate to oxidation in pure O_2 at 850 °C [29]. Owing to high reactivity ozone, the growth rate of SiO_2 is independent of crystallographic orientation of silicon and to confirm the same behavior for the oxidant ozone, Kameda et al [ ] studied the oxidation of various silicon orientations by UV-excited ozone at temperatures of 20 and 400 °C. The authors found that the oxide film formed on Si {111} and Si {001} after UV– ozone exposure had the same thickness independent of the surface orientation. Similarly, the oxidation of poly-silicon by UV–ozone resulted in a homogeneous oxide film, which even at room temperature resulted in the formation of a high quality Si/SiO_2 interface with a low leakage current and a high breakdown voltage.

1.8.2 IMPROVED INTERFACE CHARACTERSTICS

Two kinds of transition layers have been identified at the $Si/SiO2$ interface, namely the compositional and the structural transition layers [14]. The compositional transition layer

corresponds to the formation of a sub stoichiometric oxide, SiO_x , where the Si atoms are not fully oxidized (thus species of Si^{1+}, Si^{2+} and Si^{3+} are present). This suboxide lowers the insulating qualities and the lifetime of the oxide and is usually limited to one-to-two atomic layers within the oxide. The structural transition layer, in contrast, is due to the volumetric expansion of the SiO_2 film relative to the silicon lattice, which implies a strained region, usually found on both sides of the interface (Si and SiO_2). On the Si side of the interface, this distortion is limited to only one or two layers, while on the oxide side this region has been found for thermally grown oxide to extend up to 1 nm thickness [15]. The structure of this transition region exhibits a distortion of the Si–O bond lengths and bond angles with respect to bulk SiO_2. Experimentally, the existence of a transition layer is inferred from changes in the XPS spectrum, HF etching rate, MEIS, and FTIR vibrational analysis. These techniques have been applied to elucidate the interface properties of the ozone grown oxide.

1.8.3 DIMINISHED INTERFACIAL TRANSITION LAYER

The first indication that ozone gives improved interface characteristics over a conventionally grown oxide was found by Awaji et al [4]. The authors applied difference x-ray reflectivity to study the silicon oxide growth in O_2 and O_3 (5%)/O_2 (generated by a discharge ozonizer, BDO - type) at temperatures between 800 °C and 1000 °C. They found an interfacial layer of ≈1 nm thickness, which exhibited a higher density than bulk SiO_2 [21]. The thickness of this interfacial layer, however, decreased with higher oxidation temperatures and also in the presence of the more reactive ozone oxidant. Subsequently, the ozone-grown oxide and its interface properties were studied in greater detail.

1.9 OUTCOME

This chapter includes various definition, parameters and types of oxidation. Brief introduction about various applications of ozone has been discussed.

1.10 OUTLINE OF DISSERTATION

This dissertation consists of seven chapters: **Chapter 1** consisting of the introduction part of ozone enriched oxidation. **Chapter 2** consists of the literature survey obtained by going through various research papers. The literature survey comprises of the work of various researchers in the field of ozone oxidation and different types of work of the researchers have been discussed in

Chapter 2. The device fabrication steps for characterization of ozone grown oxide are discussed in **Chapter 3**. This chapter will describe the fabrication steps right from wafer cutting to metallization to obtain MOS capacitors with oxide grown using ozone, the critical wafer cleaning and silicon surface passivation techniques are also described in this chapter. **Chapter 4** comprises of the selection of ring oscillator for design verification in which functioning and applications of the ring oscillator has been discussed. **Chapter 5** comprises of FinFET library characteristics in which fabrication steps of FinFET has been discussed and also working principle, applications and advantages of FinFET have been discussed**. Chapter 6** comprises of simulation and results in which various results obtained through simulation have been discussed and finally **Chapter 7** consisting of conclusion and future scope.

CHAPTER

2

Literature Review

This section involves the work done by the various researchers in the field of development of low temperature oxidation process using ozone for VLSI. The literature survey has been carried out by dividing this chapter into three subsections; a) Oxidation, b) Ozone Oxidation, and c) Ring Oscillator. Observations has also been drawn from the literature survey and stated at the end of this chapter. Finally, objectives have also been drawn from the observations.

2.1 OXIDATION

G.D. WILK *et al*. [12] developed a method for controllably and reproducibly growing self-limiting ultra-thin oxides with excellent electrical properties in the range ≈ 10-25 Å thick at temperatures ranging from 25 to 600 ^{0}C. The process resulted self-limiting in thickness, the growth front does not continually move into the substrate and this allows uniform formation of the ultrathin oxide at temperature below 600 ^{0}C. The low temperature oxide growth has been followed up in the ring oscillator design. The limitation being slight temperature dependence of the oxidation rate above 450 ^{0}C does cause an increase in thickness for longer exposure times.

Q. FANG *et al.* [32] reported an investigation of rapid oxidation of silicon using a 126 nm excimer lamp at low pressures. The experiment provided exciting evidence for the possibility of the application of 126nm UV radiation for producing room temperature oxidation of silicon. The ring oscillator has been designed investigating rapid oxidation of silicon at 60 nm technology. The

limitation being this work is partially supported by the Engineering and Physical Science Research Council.

K.J. YANG *et al*. [24] proposed that as oxide thickness is reduced below 2.5 nm in MOS devices, both series and shunt parasitic resistances become significant in capacitance– voltage (C-V) measurements. This technique can be integrated easily into a routine C-V measurement procedure and has been demonstrated to be suitable for obtaining accurate C-V characteristics of a MOS capacitor with 1.7 nm thick gate oxide.

W.K. HENSON *et al.* [43] demonstrated high-frequency capacitance–voltage (C–V) measurements have been made on ultrathin oxide metal–oxide–semiconductor (MOS) capacitors. The result being accurate oxide thickness measurements on ultrathin oxides have been performed using C-V measurements. The fundamental limitation of estimating the oxide thickness from C-V data is determined by the magnitude of series resistance and leakage current.

K.S. KRISCH *et al.* [25] proposed that as gate oxides become thinner, in conjunction with scaling of MOS technologies, a discrepancy arises between the gate oxide capacitance and the total gate capacitance, due to the increasing importance of the carrier distributions in the silicon and polysilicon electrodes. The result being the total gate capacitance is at least 10% smaller than the oxide capacitance for sub-10 nm oxides. The limitation being for the most accurate MOS device modeling, however, these physical effects should be explicitly included in simulation.

K. HIROSE *et al.* [26] described state-of-the-art photoelectron spectroscopy studies of SiO_2/Si interfaces that play fundamental role in metal-oxide semiconductor (MOS) field-effect transistors and showed comprehensive photoelectron spectra of SiO_2/Si interfaces, which were taken from SiO_2/Si samples of extremely high quality with atomically flat interfaces by the high resolution photoelectron spectroscopy technique with laboratory X-ray sources. The result being interface structures, which were characterized by, amounts of intermediate oxidation states were independent of surface orientation for the radical oxidation process, which is in contrast to the conventional thermal oxidation.

H. KOTANI *et al.* [17] proposed a low-temperature APCVD process using TEOS-0_3 chemistry has been investigated as interlayer dielectric applications for multilevel interconnections. The result provides novel step coverage with smooth flowing profiles, and excellent hole

and gap filling properties. Dense and stable films can be obtained under appropriate process conditions. The limitation being more work will be necessary to understand the deposition mechanisms.

Y. OKAWA *et al.* [45] described how thin film capacitance measurements below 2 nm are affected by anomalous ―Negative Capacitance Effect‖ induced by parasitic components that originate from the wafer chuck. The result being that the negative capacitance effect observed on the C-V measurements is induced by the stray capacitance and residual inductance mainly existing in the wafer prober and the ground and it returns an unexplainably large inductance in the system. The limitation being with higher biased conditions, the negative capacitance effect is still observed for the case of I-V method.

G. CERIOLA *et al.* [14] proposed an idea that X-ray reflectivity has been used to measure the thickness, density and the surface and interface roughness of $Si0_2$ and SiOF thin films prepared by plasma-enhanced chemical vapour deposition. The result being density of $Si0_2$ films can be increased by fluorine insertion i.e. the SiOF film density increases almost linearly by increasing the fluorine concentration. The limitation being this effect is also reversible, since the loss of fluorine occurring during thermal annealing of these films determines also a decreasing of density.

D.K. SCHRODER *et al.* [7] proposed an idea of oxide and interfaces trapped charges as well as oxide thickness. The most important aspect of device scaling was thinner oxide with each successive technology node. Thin oxides were an important aspect of device scaling and thus its quality depends on the low leakage current density. The limitation being thin oxides with their respective higher leakage currents, have a pronounced effect on many of the methods.

G.A. BROWN *et al.* [13] proposed the electrical measurements issues for alternative gate stack systems. The result being changes have arisen from the need of increasing MOS transistor drive current in the face of decreasing overall device dimensions. The limitation being it is difficult to increase MOS transistor drive current with overall decreasing device dimensions.

A. KAZOR et al. [1] proposed for the first time the low temperature oxidation of silicon with ozone generated by the barrier discharge method is reported. The result being at 550 ^{0}C, some 105 Å of SO, can be grown in only 30min which is a reaction enhancement rate of 750% over

conventional growth rates obtained using dry molecular oxygen at the same temperature. The limitation being more complete study of the controlling kinetics of this process has been underway.

T. SUGANO *et al.* [40] proposed low temperature oxidation of silicon by electric discharge in oxidizing atmosphere. Following several hours oxidation in a quartz tube at atmospheric pressure and 300 ^{0}C, results indicate that this method has been most effective to decrease the saturation current of silicon p-n junction. The limitation being the results has been found to be satisfied in the temp. of 300 ^{0}C which leads to the thermal instability of the device and thus exerts thermal stress on the device.

J. FOGGIATO *et al.* [21] proposed the use of chemical paper deposition for various insulator films in the fabrication of semiconductor devices. Film properties from different technologies have been compared, especially; the film properties required for application in integrated circuit making the limitation being new chemistries are being explored to provide more suitable films within the confines of currently available reactor.

C.J. SOFIELD *et al.* [4] proposed the oxidation of silicon and stated that silicon dominates the semiconductor industry for good reasons. One factor is the stable, easily formed, insulating oxide, which aids high performance and allows practical processing. The various features of Si SiO_2 interface have been shown which leads to the better VLSI devices. The limitation being several research works have yet been in progress in order to improve the VLSI gate dielectric.

2.1.1 OBSERVATION

a) The oxidation of silicon is an important/crucial step in fabricating a MOSFET and makes a MOSFET functional.

b) The oxidation of silicon usually comprising of using oxygen and water vapor and is referred to as dry and wet oxidation.

2.2 OZONE OXIDATION

R. N. TAUKER *et al.* [42] proposed the growth of SiO_2 using oxygen and water vapor is referred to as dry and wet oxidation, respectively. The result being due to the high reactivity of ozone it is a proposed oxidant to grow high quality SiO_2 film at low temperatures, and thus overcoming issues

associated with thermal oxidation. The limitation being that high temperature about (800 ^{0}C - 1200 ^{0}C), this conventional process of oxidation cannot be applied to the modern substrates such as plastics and glass.

P.N. HAI *et al.* [31] proposed that humid ozone-enriched ambient, created by bubbling (0_3+0_2) gas in H_2O or H_2O_2, enhanced the silicon oxide growth on the Si substrate at 250°C.. The result has been concluded that simple but effective WO3 growth method results in the relatively high SiO_2 growth rate of 1.4 Å/min at 250°C. The film thickness is also controllable without saturation. The limitation being that further optimization of the growth process at lower temperature for the better electrical properties of SiO_2 films is under way.

K. NAKAMURA et al. [23] proposed that hydrofluoric acid etching indicates that ultrathin silicon dioxide film made by high purity ozone on Si(100) between 300 and 700 ^{0}C has the same film density as that of thermally grown silicon dioxide for device use on Si (100) at 750 ^{0}C in a wet environment. The results indicate that ultrathin silicon dioxide film made by high purity ozone on Si (100) at between 300 and 700 ^{0}C has film density as dense as that of thermally grown silicon dioxide for device used on Si (100) at 750 ^{0}C at wet environment. The limitation being rate of film growth greater than 6Å becomes much lower as substrate temperature decreases down.

S.T. OYAMA *et al.* [35] propose various ozone properties and reaction i.e. chemical and catalytic properties of ozone. Various parameters have been discussed like structure and bonding in ozone, thermodynamic properties, spectral properties and photochemistry as well as reactions in stratosphere. The result being ozone is the three-atom allotrope of oxygen characterized by strong electrophilic and oxidizing properties. The limitation being that with catalysts, however, the reactivity of ozone can be harnessed at lower temperature but there is a need where selectivity can be controlled or controlled oxidation.

G.S. CHEM *et al.* [11] proposed the application of ozonated DI water (DI-O_3 water) in silicon wafer surface preparation, including removals of organic impurities, metallic contaminants and particles as well as photoresist stripping. The results indicated that ozone is a powerful oxidant and can provide economic benefits in wafer surface preparation. The limitation being that more efforts on ―β- testing‖ of the ozone processes should be taken under the collaboration between the equipment and the IC manufacturing industry to pilot the novel technology to fully accepted

commercial applications.

H. NONAKA *et al.* [19] reported 100 % ozone oxidation process has been applied for the first time to rapid low-temperature oxidation of silicon to fabricate device quality Si02 films. The result being the working pressure of the furnace was typically 900 Pa, which resulted in the growth of 4 nm Si02 film within 4 min at 400 ^{0}C. The limitation being ozone oxidation has been applied to further low temperature oxidation in order to perform oxidation process on various other substrates such as glass, plastics etc.

J.R. VIG *et al.* [20] reviewed the ultraviolet (UV)/ozone surface cleaning method. The UV/ozone cleaning procedure is an effective method of removing a variety of contaminants from surfaces. The result being it can produce clean surfaces at room temperature, either in a room atmosphere or in a controlled atmosphere. The limitation being prolonged exposure of oxide-forming metals to UV/ozone in room air can produce rapid corrosion.

H. OKABE *et al.* [18] proposed the various properties of ozone and the chemistry involved in ozone technology. The various process like photo dissociation is the Chappius Bands (4400 to 8500 Å), Huggins Bands (3000 to 3600 Å) and Hartley Bands (2000 to 3200 Å) have been proposed and the importance of the ozone in the atmosphere been discussed.

T. NAKANISHI *et al.* [39] reported improvement in MOS Reliability by Oxidation in Ozone. Using clean ozone in a new load-locked oxidation system thin gate oxides with improved charge to breakdown characteristics and low surface state densities. The result being using a new ozone oxidation technique, which provides excellent device performance and long term reliability. The limitation being due to ultrathin gate oxides, increase in leakage currents may occur in this proposed system.

L. WANG *et al.* [28] proposed that with low temperature and high concentration ozone oxidation, ultra-thin HfO_2 films were fabricated on silicon substrate. The results clearly showed the uniform composition and smooth transition from Si substrate to the HfO_2 film, and also the reduced charge trapping in the gate dielectric for ozone oxidized HfO_2.

H. KIM *et al*. [19] proposed the surface Treatment and Characterization of Indium–Tin-Oxide Thin Films Modified Using Cyclonic Atmospheric-Pressure Plasma investigated by static contact angle (CA) analysis as well as atomic force microscopy (AFM). As a result, it is believed that this

cyclonic atmospheric pressure plasma alters the ITO surface physicochemical features, which can in turn improve ITO films performance for various applications. The limitation being there is need to improve this technology so as to increase the efficiency of the device.

A.K. KULKARNI *et al.* [2] proposed the electrical, optical and structural characteristics of indium-tin-oxide thin films deposited on glass and polymer substrates. The results suggested that the low resistive ITO thin films are obtained in the films that are highly oriented in the (400) direction. The limitation being IZO have better characteristics properties than ITO.

K. NAKAMURA *et al.* [23] proposed zinc oxide bulk, thin films and nanostructures processing, properties and applications. ZnO been used for its wide range of applications like facial powder, ointments, sunscreens and as transparent conducting electrodes. The result being ZnO has numerous attractive characteristics for electronics and optoelectronics devices. The limitation being IZnO has more attractive characteristics than ZnO in electronics and thus need to be replaced.

K. ZANG *et al*. [24] proposed an analysis of the mechanical properties of transparent conducting oxide (TCO), indium tin oxide (ITO) and indium zinc oxide (IZO) thin films on the glass substrates. The results show that the presence of hydrogen in a gas mixture during film deposition could vary significantly the hardness and elastic modulus of the ITO films. and also IZO have higher elastic modulus and hardness in comparison to the ITO films deposited at same conditions. The limitation being amorphous oxide semiconductors such as ZnO, ZnTO, InGaO and InGaZn are used as it enhanced several characteristics.

Y.L. WANG *et al.* [46] proposed the characteristics of Room-Temperature-Deposited, Small Gate Dimension Indium Zinc Oxide TFTs in which indium zinc oxide channel thin film transistors TFTs with gate dimension of 1×200 μm were fabricated on glass substrates using radio frequency magnetron sputtering deposition at room temperature. The result being the IZO thin-film deposition and transistor fabrication were performed at room temperature, which makes this technology suitable for applications on organic flexible substrates. The limitation being organic TFTs have very low mobility and may have reliable concerns.

D.H. LEE *et al.* [9] proposed the effect of chloride precursors on the stability of solution-processed Indium Zinc Oxide Thin Film Transistors in which solution –processed indium zinc oxide (IZO)

films were prepared by spin-coating the films as an active layer in thin-film transistors (TFTs). These films were coated with nitrate and a mixture of acetate and chloride based precursors to allow the IZO films to contain indium and zinc components. The result being suitable amount of chlorine during annealing improved performance and stability. The limitation being a surplus of chlorine led to unfavorable results and high electrical losses.

C.G. CHOI *et al.* [6] proposed Solution-Processed Indium-Zinc Oxide Transparent Thin-Film Transistors in which TTFTs with an indium-zinc oxide IZO active layer by the solution processed deposition method were fabricated and their TFT characterization was examined. The result being highly transparent and amorphous IZO thin films were obtained by annealing at 500°C using this precursor solution.

2.2.1 OBSERVATION

a) With the use of ozone in oxidation process, a low temperature oxidation process has been proposed keeping in mind several chemical and electrical properties associated with ozone.

b) Use of ozone in VLSI enhances the quality of device by improving overall characteristics of the device.

2.3 RING OSCILLATOR USING FinFETs

Y.K. CHOI *et al*. [47] proposed Nanoscale CMOS Spacer FinFET for the Terabit Era which a spacer lithography process technology, which uses a sacrificial layer and spacer layer formed by chemical vapor deposition (CVD), has been developed. The result being it provides a doubling of feature density for a given lithography pitch, which increases current by a factor of two and also this spacer lithography technology yields better critical dimension uniformity than conventional optical or e-beam lithography and defines smaller features beyond the limit of current lithography technology. The limitation being short-channel behavior through this process yields better results but need to be improved.

J. SHEN *et al.* [22] proposed the 2D Analysis of Bottom Gate Misalignment and Process Tolerant for Sub-100nm Symmetric Double-Gate MOSFETs in which the effects of bottom gate misalignment in symmetric double-gate MOSFET's were examined. The result being higher off-current and subthreshold swing was observed due to punch through at the bottom interface with bottom-gate misalignment. The limitation being bottom gate misalignment degrades the

subthreshold swing and on-current of a SDG MOSFET, giving a smaller on-off current ratio in the I-V characteristics.

S. XIONG *et al.* [37] proposed Sensitivity of Double-Gate and FinFET Devices to Process Variations in which the manufacturability of 20-nm double-gate and FinFET devices in integrated circuits by projecting process tolerances was investigated. The result found that quantum effects have great impact on the performance of devices. As a result, the device electrical behavior is sensitive to small variations of body thickness. The effect dominates over the effects produced by other physical fluctuations.

H.R. KHAN *et al.* [15] proposed the Approaching Optimal Characteristics of 10-nm High Performance Devices: A Quantum Transport Simulation Study of Si FinFET in which a fully self-consistent quantum mechanical simulator based on the Contact Block Reduction (CBR) method to optimize a 10 nm FinFET device and meet the International Technology Roadmap for Semiconductors (ITRS) projections for double-gate high-performance logic technology devices was utilized. The result found that the device ON-current approaching the value projected by the ITRS could be obtained using a conventional unstrained Si channel and a SiO2 gate insulator.

D. HISAMOTO *et al*. [8] proposed FinFET—A Self-Aligned Double-Gate MOSFET Scalable to 20 nm and reported MOSFETs with gate length down to 17 nm. To suppress the short channel effect, a novel self-aligned double-gate MOSFET, FinFET has been proposed. The result being self-aligned double-gate effectively suppresses short channel effects, even with 17-nm gate length, Si Ge gate provides a proper threshold voltage for ultrathin body MOSFET, Gate is self-aligned to the S/D, which is raised to reduce the parasitic resistance. The structure uses a S/D first, gate last process flow that may be needed for future high- gate dielectric and metal gate. FinFET can be suitable integration of Si-ULSIs. Ring oscillator with FinFETs leads in the scalable device and the application of ozone in this results better.

M.K. Mandal *et al.* [29] proposed characteristics and applications of Ring Oscillator in which the structure and operating principle of ring oscillator have been described. The results being noise sources affect the phase and amplitude of ring oscillator, phase noise and timing jitter has been decreased with the increase in the power consumption of the oscillator circuit. The limitations being more work have to be done in order to design the ring oscillator of maximum efficiency and results.

A.D. Lourts *et al*. [3] proposed FinFET Based Ring Oscillator and reported that in future, as the size of channel length decrease, the necessity of low power based circuit will be increased. The results being FinFET consist of four modes developed using IG gate mode, since it's faster and improve the performance of the design. The limitation being in future the design can be developed using any of the other modes of FinFET operations like IG/LP mode where power plays an important role.

N. Collaert *et al*. [27] proposed a Functional 41-Stage Ring Oscillator Using Scaled FinFET devices with 25-nm gate lengths and 10-nm Fin widths applicable for the 45-nm CMOS Node and a functional FinFET ring oscillator with a physical gate length of 25 nm and a fin width of 10 nm, the smallest ever reported has been fabricated. The result being For the first time, functional ring oscillator circuits with these ultrasmall multigate devices have been demonstrated. Ring oscillator delay measurements show a stage delay of 60 ps at V_{dd}= 1.5V, consistent with the obtained driven currents. Excellent drive currents can be achieved by widening the fin above 30 nm. The measured delay time can be significantly improved by a dedicated layout.

2.3.1 OBSERVATION

a) The ring oscillator using FinFETs and the ring oscillator using ozone oxidized FinFETs has a lot of difference in performance and results.

b) With the use of ozone in ring oscillator design, the simulation results obtained such as C-V characteristics, temperature dependency yields better results.

2.4 GAPS IN STUDY, OBSERVATIONS AND OBJECTIVES

The following observations have been drawn from the literature survey and are stated below:

a) The ring oscillator designed with the view of using ozone and without ozone oxidized has different aspects as seen in the paper. Ring oscillator which is ozone oxidizes shows better simulation results than the ring oscillator without ozone oxidized but this technology is not yet implemented in full scale in electronics world due to various drawbacks faced by researchers.

b) Ozone has various advantages in the oxidation of silicon at low temperature but the main gap is that at low temperature we will not be able to get desired efficient results in order to achieve a

design of higher efficiency as etching of the device at higher temperature shows significant results as compared to the results at lower temperature.

c) With the use of ozone in the VLSI technology in the device level, it leads to the thinner of the oxide layer upto very few micrometers but the main gap is that it leads to the increasing leakage current and hence reduces the performance of the device.

d) Ozone has strong oxidizing properties but to get high quality Si/SiO2 interface and good growth rate at low temperatures (300°C) the substrate is UV irradiated to increase the decomposition rate of O_3. Ozone has a rich photochemistry and thus becomes a strong oxidizer in the presence of UV, so the gap in this is that UV must be enriched with ozone to get the desired results.

From the observations it is concluded that there is a need to develop a cryptographic model based upon the dynamic keys for data security. So, **objectives** have been derived from the observations obtained from literature survey. The **objectives** are given as:

1. In this project, we want to observe the impact of ozone based amorphous type oxidation on silicon substrates for application in the Thin Film Transistors and Fin Field Effect Transistors.
2. The performance will be tested by designing a complete system level circuit (ring oscillator) layout using Fin-Field Effect Transistors oxidized by ozone at low temperature and then its detailed analysis will be carried out.
3. We will compare the results of the ring oscillator using ozone and ring oscillator without using ozone and the detailed analysis about their results will be discussed.

CHAPTER

3

Device Fabrication

This chapter includes detailed explanation about the various fabrication steps employed in fabricating a silicon dice or silicon.

3.1 INTRODUCTION

As MOS (Metal oxide Semiconductor) capacitor is structurally very close to the MOS field effect transistor (MOSFET) with ease in fabrication, which makes it ideal to get electrical characteristics of gate oxide and its interface with silicon. Here the fabrication technique is discussed to get a simple MOS capacitor.

3.2 FABRICATION STEPS

The entire fabrication process is divided into the various steps and is given as; a) Wafer cutting and general cleaning, b) Removal of organic impurities, c) Removal of metallic impurities, d) Hydrogen passivation of silicon samples, e) UV-Ozone oxidation of front surface, f) Back side metal deposition and annealing to form ohmic contact, g) Front metal dots deposition and baking [31].

3.2.1 WAFER CUTTING AND GENERAL CLEANING

Doped Boron (2×10^{15} atoms/cm^3) and polished p-type Silicon (100) wafers of resistivity 2-10 Ω-cm are used as the main constituent in wafer cutting and general cleaning . The wafer was cleaved by a diamond cutter to obtain the substrate of size 1 cm x 1 cm approximately [9]. Then the series of cleansing steps are carried on the substrate to obtain a clean defect free surface of silicon. For wet cleaning the various electronic grade chemicals are used. All cleaning processes are done inside a 0% recirculation wet bench with laminar airflow from HEPA air filters maintaining class 100 environment [11]. For general cleaning of substrate it is sonicated in

acetone for 2 minutes and blow of nitrogen is given to dry it and thus big dust particles are removed for the surface.

3.2.2 REMOVAL OF ORGANIC IMPURITIES

Ozone is the second most powerful reducing agent after fluorine, and its reducing nature can further be increased by heat and UV light. In this work SAMCO UV-1 dry cleaning system is used which is fitted with silent discharge type ozone generator and an 110W low pressure mercury lamp with wavelengths mainly 253.7nm and 184.9nm [39]. Thus these qualities make this system perfect for removal of organic impurities from the surface of the sample. The sample is processed in UV-1 chamber for 30 minutes at 300^0 C with UV and ozone at flow rate of 0.5 litre/min [33]. Thus organic impurities are removed and a sacrificial SiO_2 layer is also grown which can be etched away by dilute aqueous solution of HF and strong rinse in DI water.

3.2.3 REMOVAL OF METALLIC IMPURITIES

For removal of metallic impurities standard RCA-2 cleaning is used in which 4:1:1 solution of H_2O:HCl:H_2O_2 at 70^0 C is used for 5 minutes [1]. Since H_2O_2 is an oxidizing agent the SiO_2 layer is also grown over silicon, which can be etched away and the surface is passivated with hydrogen by dilute aqueous solution of HF, moreover in this work the HF aqueous solution is replaced by Methanol-HF solution (discussed next) for better hydroxyl termination.

3.2.4 HYDROGEN AND HYDROXYL PASSIVATION OF SILICON

The SiO_2 over silicon from previous step can be etched and in same chemical reaction the underlying silicon can be passivated with hydrogen ions (-H) or the hydroxyl ions (-OH) by oxygen replacement reaction. These hydrogen ions and the hydroxyl ions have a similar effect on the bare silicon surface [7]. Both of them have a single dangling bond, which can neutralize the silicon dangling bonds on the surface of the wafer. Also, both of them will provide a repulsive effect on the oxygen adherence and which inhibits the native SiO_2 growth over silicon. A –H/-OH terminated silicon surface is a chemically passivated substrate upon which first we etch away the native oxide SiO_2, which in turn leave the surface atoms of silicon covalently bonded with hydrogen or hydroxyl. Since in all surfaces silicon atoms are totally coordinated, termination leads to improved stability in ambient environment unlike a ―clean surface‖ having unpassivated

surface atoms, and dangling bonds. It is very inert that it can be handled in clean ambient without any exceptional care for several minutes [33]. A comparative study has been done to compare the quality of oxide grown by ozone after this hydrogen and hydroxyl passivation. The hydrogen passivation of the silicon wafer is done by using H_2O-HF solution in the ratio of 49:1 and for achieving a good hydroxyl cover over the silicon surface a 1:9 mixture of HF: Methanol is used for 5 minutes and then rinsed in methanol.

3.2.5 UV-ZONE OXIDATION

Ozone has strong oxidizing properties [2] but to get high quality Si/SiO2 interface and good growth rate at low temperatures (300°C) the substrate is UV irradiated to increase the decomposition rate of O_3 [4]. Ozone has a rich photochemistry and thus becomes a strong oxidizer in the presence of UV. The bombardment of high-energy photons (greater than ~6eV) leads to structural distortion of Si-Si bonds, Si-OH groups and strained Si-O-Si bonds [11] at Si/SiO_2 interface but also provide a high growth rate [11]. Therefore, in this work the low pressure mercury lamp is used, which generates UV of peak wavelengths 253.7nm and 184.9nm corresponding to the energy of 4.887 eV and 6.7055 eV respectively. This wavelength range is optimum to get an excellent quality Si/SiO_2 interface at good growth rate. Ozone decomposition takes place due to broad absorption spectrum in UV, and visible region of the electromagnetic and the Chappuis band (440nm – 850 nm) [12]. In this case the photolysis of ozone takes place in the Hartley band via pathway with unity quantum yield [12]. The schematic view of process chamber is given in figure 2.1 in which with the flow rate of 0.5 liter/minute of oxygen at 300° C for 100 minutes.

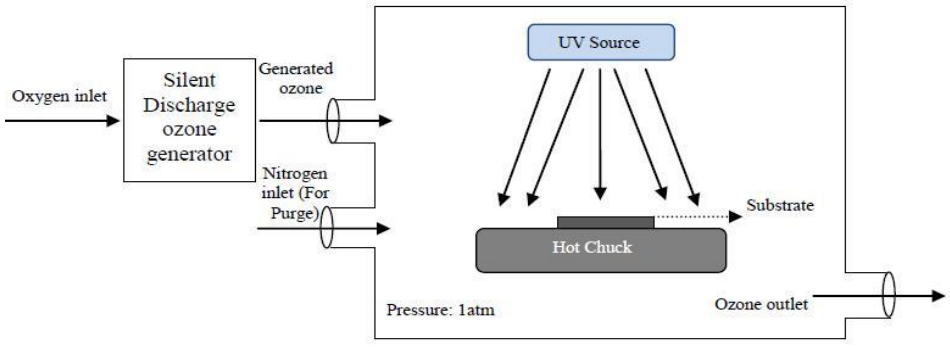

Figure 3.1 Schematic view of Ozone-oxidation chamber.

3.2.6 BACK SIDE METAL DEPOSITION AND ANNEALNG TO FORM OHMIC CONTACT

The most common methods of Physical Vapor Deposition (PVD) for metals are evaporation, e-evaporation and sputtering [13-14]. Out of these evaporation is a simple apparatus. Evaporation occurs when the material is heated more than its melting temperature in an evacuated chamber. The evaporated atoms travel with high speed in straight-line trajectories and get deposited on substrates placed in chamber. The rate of evaporation is controlled by the vapor pressure. After etching away possible oxide layer from back side, the aluminum metal in deposited using physical vapor deposition in high vacuum system (pressure ~ 10^{-5} mtorr) and then deposited metal is annealed at 450°C to 500° C in nitrogen ambient at flow rate of 1 lit/min for 15 minutes [39].

3.2.7 FRONT METAL DOTS DEPOSITION AND BAKING

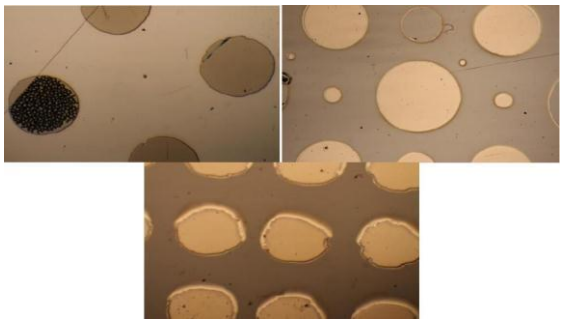

Figure 3.2 Front side metal dots under microscope[35].

At the front side of the sample the metal dots are deposited to from MOS capacitor structure. The metal dots are deposited using shadow mask with dots having diameter of 0.6 mm [18]. After all process steps structure we obtained is depicted below:

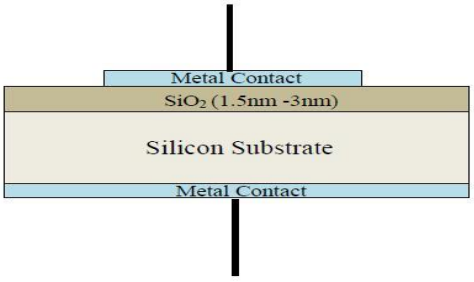

Figure 3.3 Final structure of MOS capacitor structure.

3.3 OUTCOME

The detailed fabrication process used in this work is described in this chapter. The cleaning, passivation technique, then oxidation and all metallization techniques are discussed in this chapter.

CHAPTER

4

Selection of Ring Oscillator for Design Verification

In this chapter, detailed study about the functioning and operation of ring oscillator has been discussed and thus has been checked for design verification.

4.1 INTRODUCTION

In a digital system oscillators are used for synchronizing computation, timing of the sampling in a data converter, carrier synthesis and LO in RF systems etc. A ring oscillator is defined as a device which is composed of an odd number of NOT gates whose output oscillates between two voltage levels, which represent true and false [44]. The NOT gates are attached in a chain; the output of the last inverter is fed into the first inverter. A circular chain which is composed of an even number of inverters can't be used as a ring oscillator; the last output in this case is same as input. However, the given configuration of inverter feedback can also be used as a storage element; it's the basic building block of static random access memory (SRAM) [46]. The stages of ring oscillator are often differential stages that are immune to external disturbances. This also renders non inverting stages available.

A ring oscillator can be made by mixing of the inverting and non-inverting stages, provided the total number of the inverting stages is odd. The period of the oscillator is equal to twice the sum of the individual delays of all stages in all the cases [41]. A real ring oscillator requires only power to function and above a certain threshold voltage, oscillations begin spontaneously. For increasing the frequency of oscillation, two methods are commonly used. First, the applied voltage is to be increased; this increases frequency of the oscillation as well as the current consumed. The maximum permissible voltage which is applied to the circuits limits the speed of a oscillator [11]. Secondly, by making the ring from a smaller number of inverters it results in a higher frequency of oscillation provided certain

power consumption is given. Ring oscillators are simplest type of oscillator which is used in electronic circuits. It can be designed both for fixed frequency and variable frequency operation. Ring oscillators generally consist of an odd number of inverters where the output of the oscillator oscillates between the two voltage levels such as high or low [16]. The inverters are connected in a chain and the output of the last inverter is fed back into the first. The ring oscillator can also be used for measuring the effects of voltage and temperature on a chip.

4.2 OPERATION OF RING OSCILLATOR

Ring oscillator is member of the class time delay oscillator. A time-delay oscillator consists of the following: an inverting amplifier with a delay element which is between the amplifier output and its input [32]. The amplifier must necessarily have a gain > 1.0 at the intended oscillation frequency. Considering the initial case where the amplifier input and output voltages are for the time being balanced at a stable point. Amplifier output can rise slightly even with small amount of noise. After passing through time-delay element, even this small output voltage change will be shown to the amplifier input. Amplifier has negative gain > 1, so the output will be changed opposite to the direction of input voltage [19]. It will be changed by an amount larger than the input value, for a gain > 1. This amplified and reversed signal moves from the output through the time-delay and back to input, where it is gets amplified as well as inverted again. The result of the sequential loop is square-wave signal at the amplifier output which has the period each of half of the square wave equal to time delay. As the square wave grows and until the amplifier output voltage reaches its limit, it will finally stabilize [32]. A deeper analysis will exhibit that the wave that grows from the initial noise may not be square as it grows, but the point here is that it will later become square as the amplifier reaches its output limit.

4.3 SCHEMATIC VIEW OF 31- STAGE RING OSCILLATOR

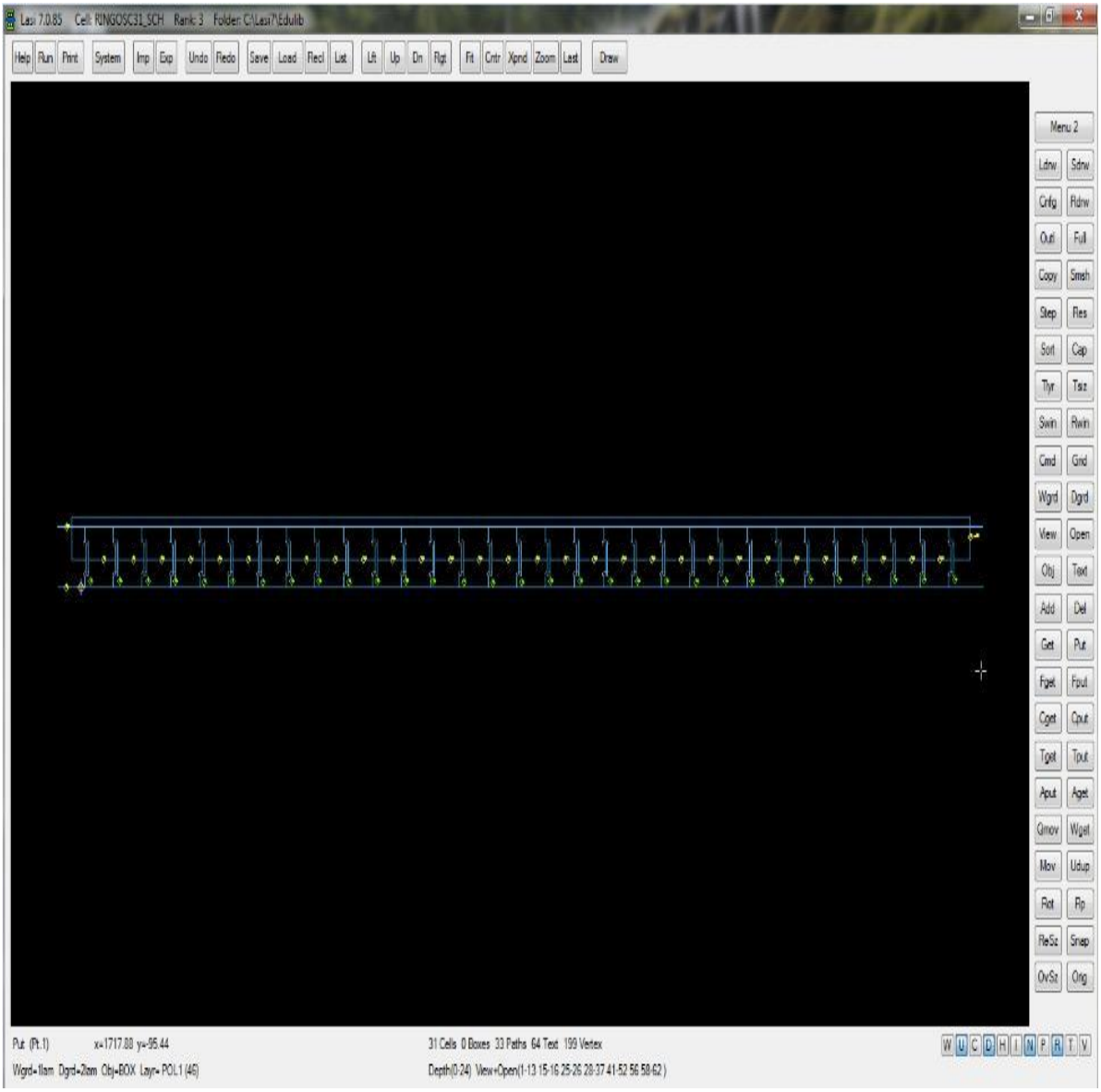

Figure 4.1 Schematic View of 31- Stage Ring Oscillator.

The above figure shows the schematic view of ring oscillator of thirty one stages and the zoom in figure of the above schematic is as follows:

4.3.1 ZOOM IN SCHEMATIC VIEW OF 31-STAGE RING OSCILLATOR

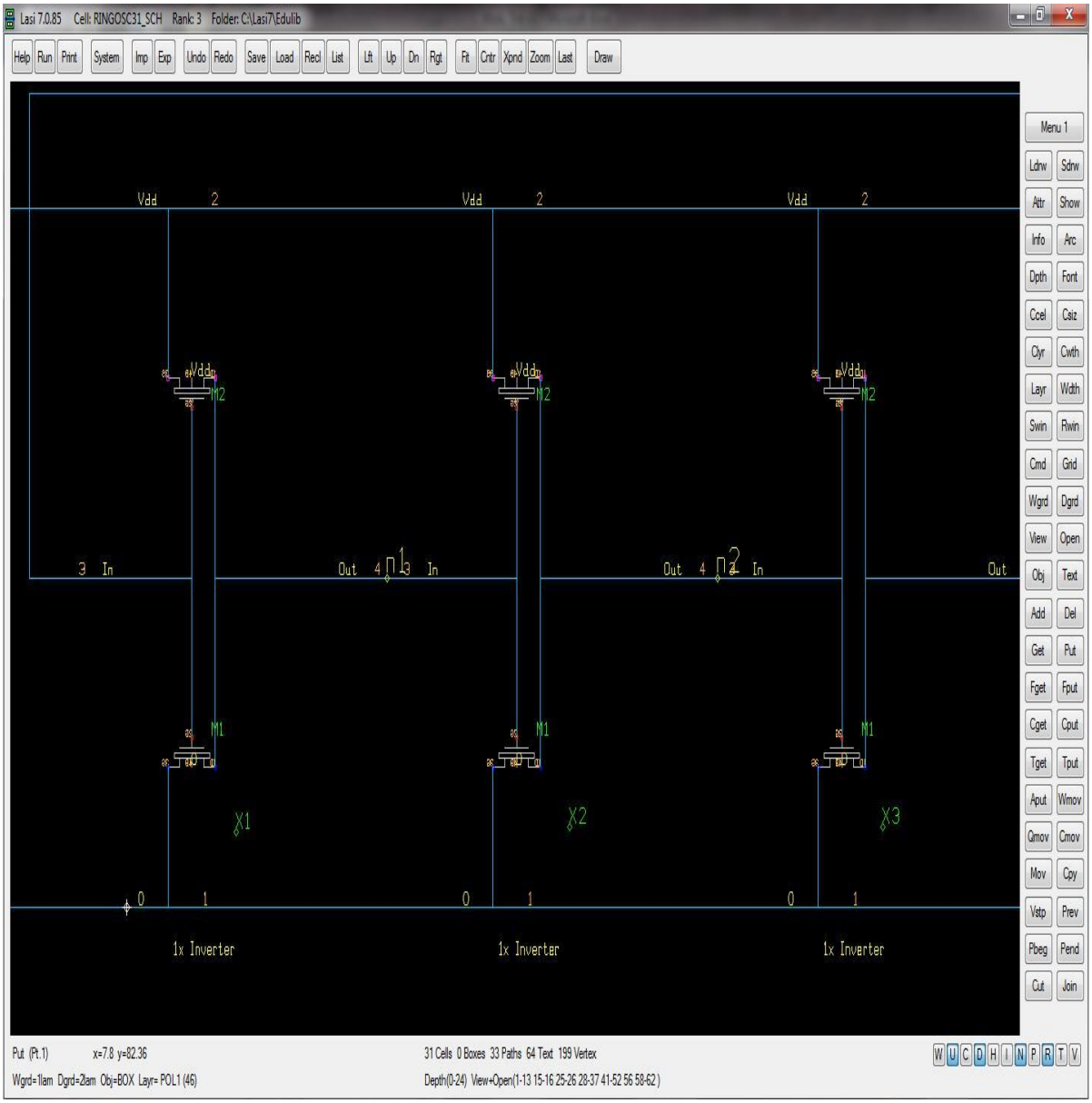

Figure 4.2 Zoom in schematic view of 31-stage ring oscillator.

It is a schematic view of 31-stage ring oscillator and the application of ozone will be defined by making use of ring oscillator with ozone oxidized FinFETs and with without ozone oxidize FinFETs and then performance verification by simulation should be carried out.

4.4 DESIGN OF FTNFET BASED 3-STAGE RING OSCILLATOR

FINFET is also known as Multi-gate FET (MuGFET). Multi-gate FET (MuGFET) is and emerging technology for sub-deep micron nodes and is also receiving consideration as a more scalable alternative to the bulk CMOS. The base of FINFET is Silicon-on-insulator (SOl), by etching the active silicon film on top of SOI fins are created in the insolation layer [14]. The gate oxide has been developed in both sidewalls of the silicon fin to form the double gate FINFET [32]. For Tri-Gate FinFET , on the top poly-silicon material will be deposited and etched to make a strip wrapped around the silicon fin defining the total MOS channel width. Using these benefits of FINFETs in mind, the ring oscillator has been developed using the 60 nm model file using the tool LASI.

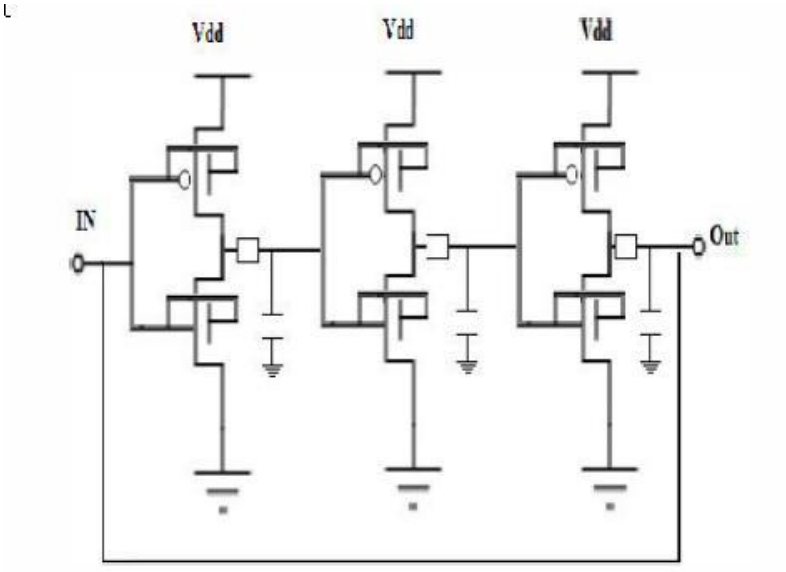

Figure 4.3 3-Stage FinFET based Ring oscillator.[38]

The fastest ring oscillator is a minimally loaded fan out of single inverter [16]. The figure given above shows the schematic diagram of FINFET based 3-stage ring oscillator, each inverter output is connected to the input as next inverter and finally the output of the 3rd inverter is feedback to the input of first inverter to form the oscillation output.

4.5 OUTCOME

In this chapter, the functioning and operation of ring oscillator has been discussed and keeping in mind these characteristics of the ring oscillator, we are designing a FinFET based ring oscillator oxidized with ozone and without ozone.

CHAPTER

5

Finfet Library Characterization

The design of a ring oscillator comprises of FINFETs and its various components, characterization and fabrication techniques are discussed in this chapter.

5.1 WHAT IS FINFET?

FinFET suppresses various short channel effects; in particular six different short-channel effects can be distinguished:

1) Drain-Induced Barrier Lowering And Punch through

2) Surface Scattering

3) Velocity Saturation

4) Impact Ionization

5) Hot Electrons

6) Sub-Threshold Swing.

It provides higher driving current. Using FinFETs allows scaling down to few nanometers which makes systems more compact. And allows improves speed thus making systems faster. As the requirement of low power device increases, it's essential to reduce power dissipation in the ring oscillator, since it produces more power in the circuit [3]. Low power design can be achieved by utilizing the alternative solutions instead of CMOS based design like Double Gate FETs or FinFETs. The main benefit of the FinFET is good control over leakage current and suppresses the short channel effects with the help of another gate which is placed opposite to the traditional gate and reduces the amount of power dissipation. FinFETs are a non planar double gate transistor built on single Silicon on Insulator (SOl) substrate. The important characteristic of the FinFET is that the conducting channel is enfolding by the thin silicon "fin", which creates the gate of the device [35].

5.2 FABRICATION STEPS OF MAKING FINS IN FINFET

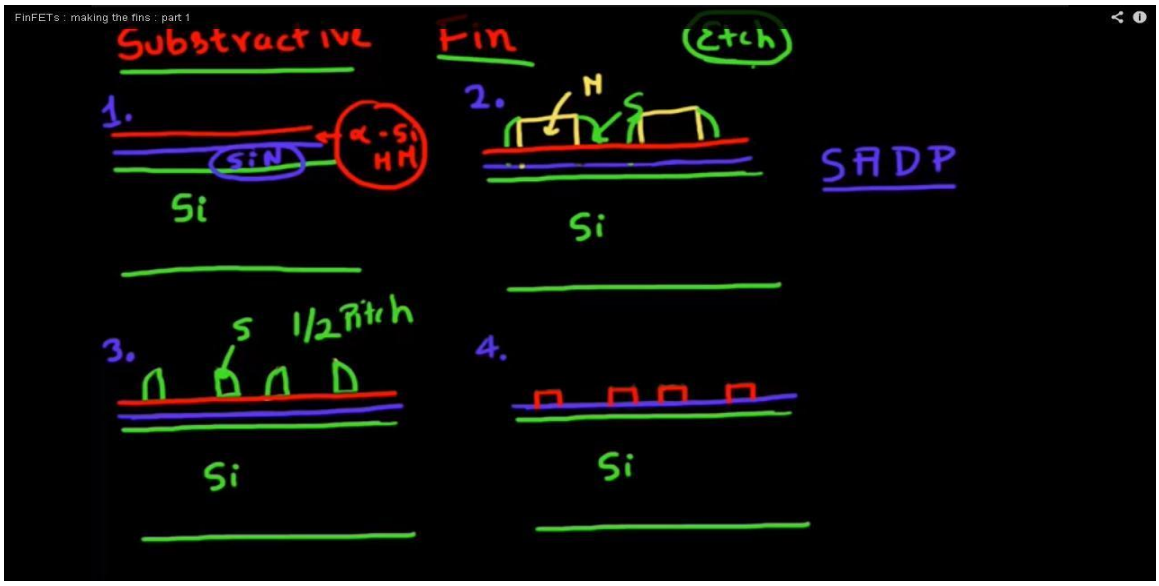

Figure 5.1 Fabrication steps of making fins in finfet [10].

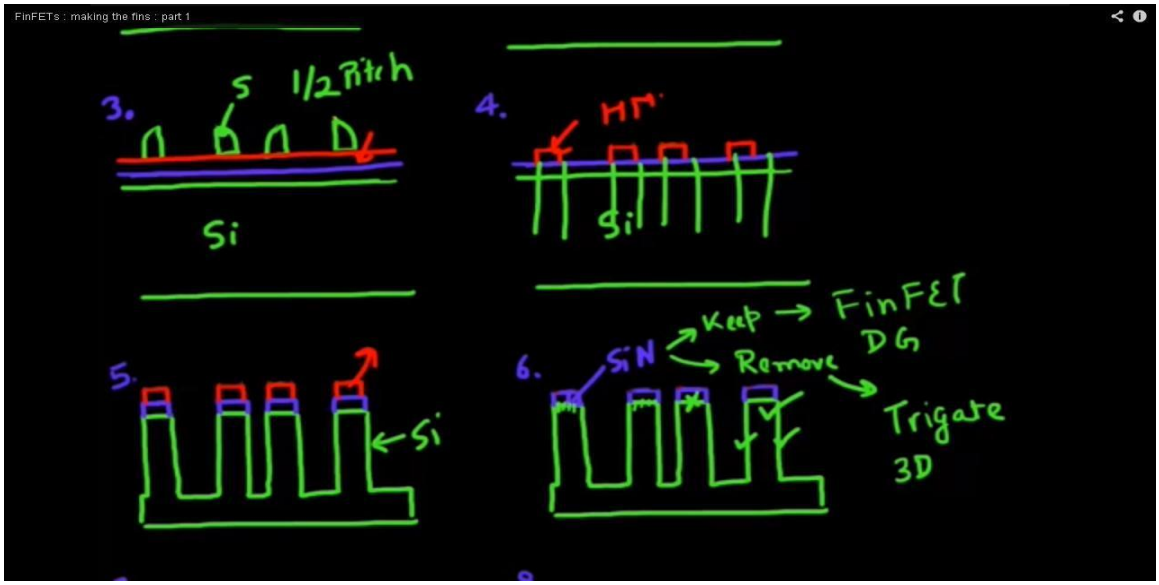

Figure 5.2 Fabrication steps of making fins in finfet [10].

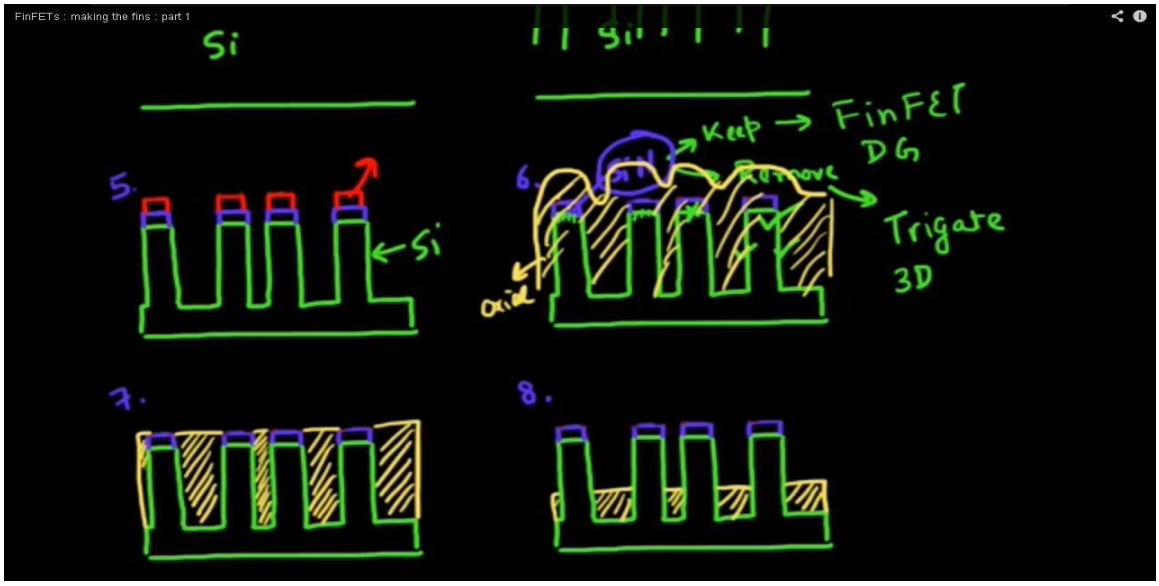

Figure 5.3 Fabrication steps of making fins in finfet [10].

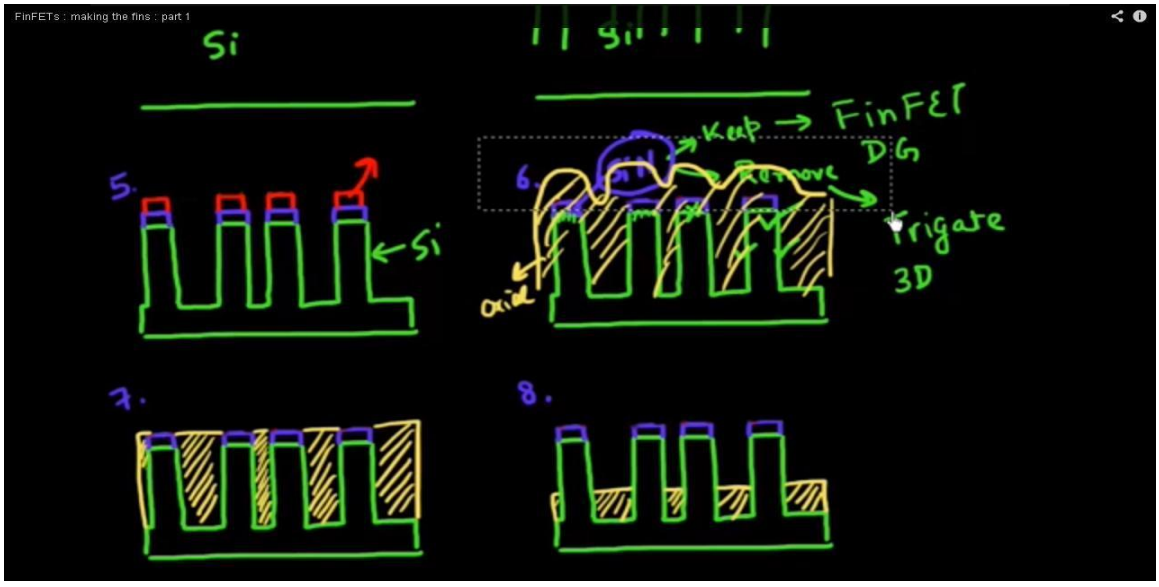

Figure 5.4 Fabrication steps of making fins in finfet [10].

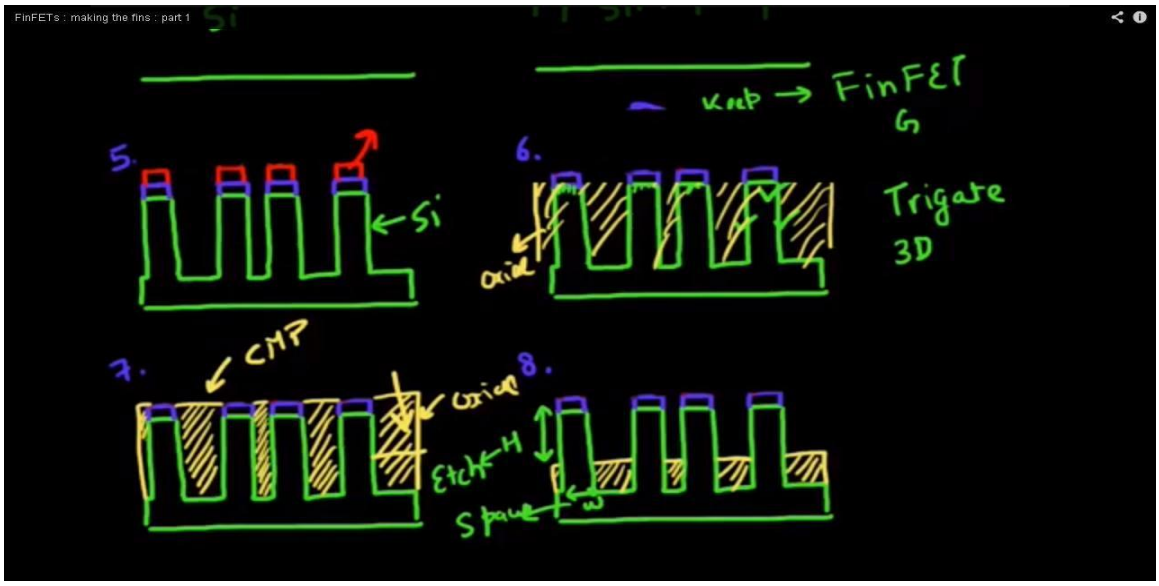

Figure 5.5 Fabrication steps of making fins in finfet [10].

5.2.1 FABRICATION STEPS OF FINFET

Starting with Si Substrate in this case & Nitride Capping Layer & Amorphous Si Hard Mask (HM) has been used as shown in figure (5.4). Double patterning/SADP(Self Aligned Double Patterning Approach Using has been used in order to define mandrels, spacers .Then mandrels are to be removed & spacers are left behind which are twice the density or ½ pitch & then those spacers are etched into the hard mask, then hard mask are left behind, which now can etch into Silicon. So using these hard masks it is etched into Si wafer & silicon fins will be formed as shown in figure (5.5). Width of FinFET device is defined at patterning steps (3^{rd} step). Width of FinFET is determined by spacers [15]. Next step is remove hard mask, now hard mask is never used, so hard mask is etched away. So Si Nitride caps on top are left behind. So at this point of time, one can decide whether one wants to keep this SiN on top surface for current conduction. Then it forms FinFET or double gate device. If this top surface SiN is removed, then top surfaces along with sidewalls for current conduction are used which leads to Trigate Device 3D Device Figure (5.6). Fill out the Trenches created where it is filled up with oxide. Oxide has to be conformal requirement on fins Figure (5.7) . Fill it up with oxide .Next Step to do is CMP. With CMP, try to planarise the top surfaces, planarise step of CMP are left behind.

In 6^{th} step the result of CMP has been seen [18]. Width of FinFET device is defined at patterning steps (3^{rd} step) and width of FinFET is determined by spacers Figure (5.8). Next Step

is to etch back oxide & that really reveals these fins [10]. Depending on how deep etching gas been done defines Height of Fin. Width of FinFET device is defined at patterning steps (3rd step) and width of FinFET is determined by spacers. Two critical dimensions need to keep track off.

5.3 DESIGN LAYOUT OF VLSI CIRCUIT (RING OSCILLATOR) USING FINFETs

The design layout of the ring oscillator using FinFETs is pictured below:

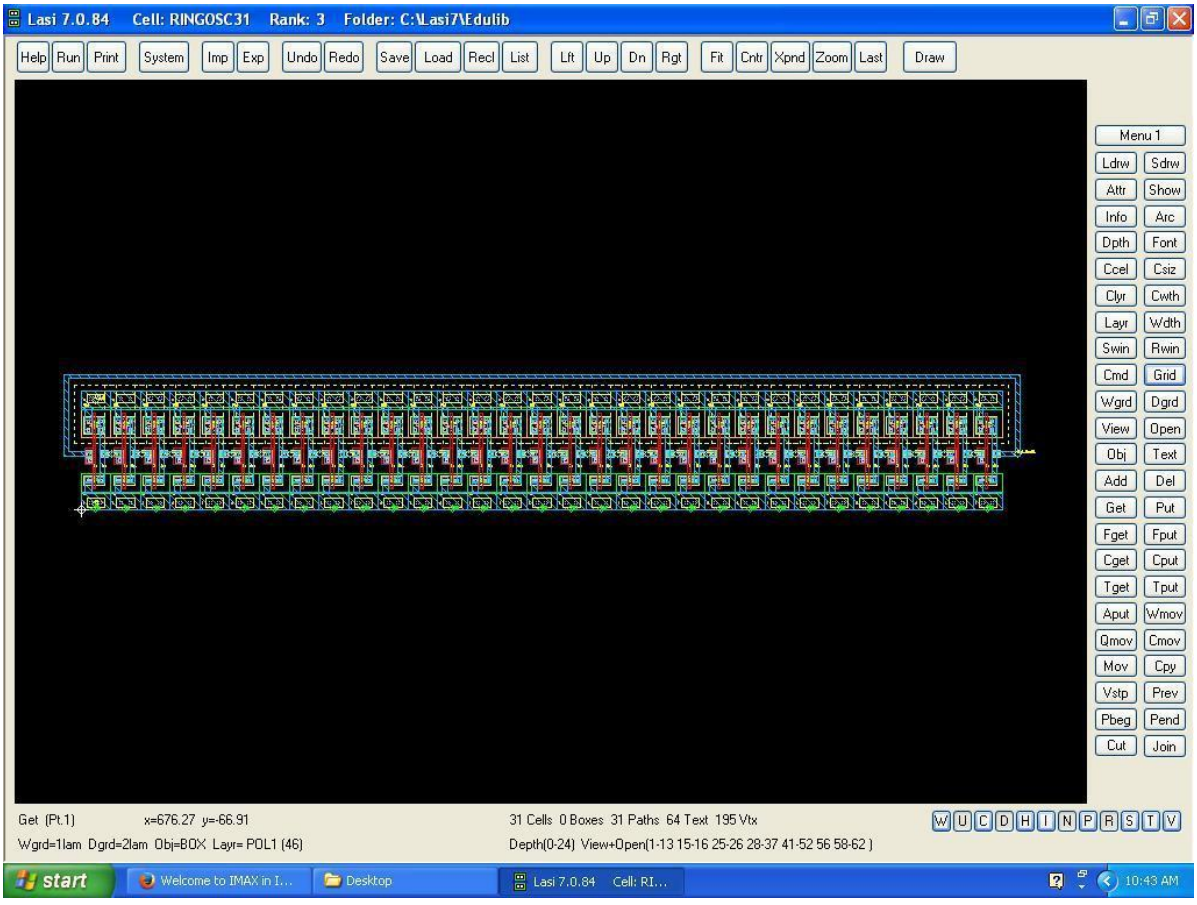

Figure 5.6 Design Layout of VLSI Circuit (Ring Oscillator) Using FinFETs.

The above shown figure is the design layout of 31-stage ring oscillator circuit. 31 CMOS inverters have been used in this design in order to get the desired results. The design has been made using the tool LASI and the technology used in 60 nm.

The zoom in figure for the ring oscillator using FinFETs is pictured below:

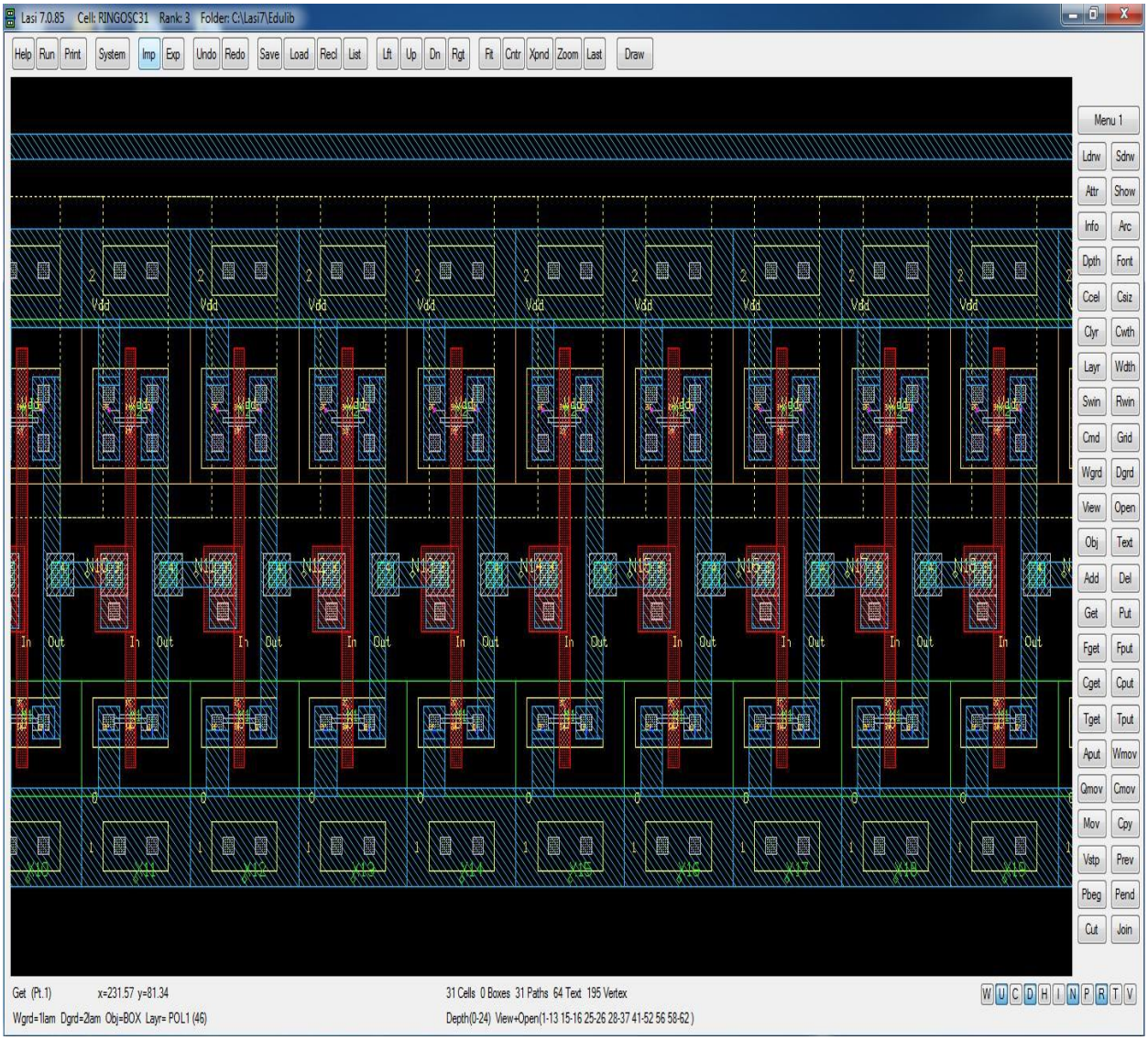

Figure 5.7 Zoom in figure for the 31-stage ring oscillator using FinFETs.

5.4 DESIGN LAYOUT OF VLSI CIRCUIT (RING OSCILLATOR) USING OZONE OXIDIZED FINFETs

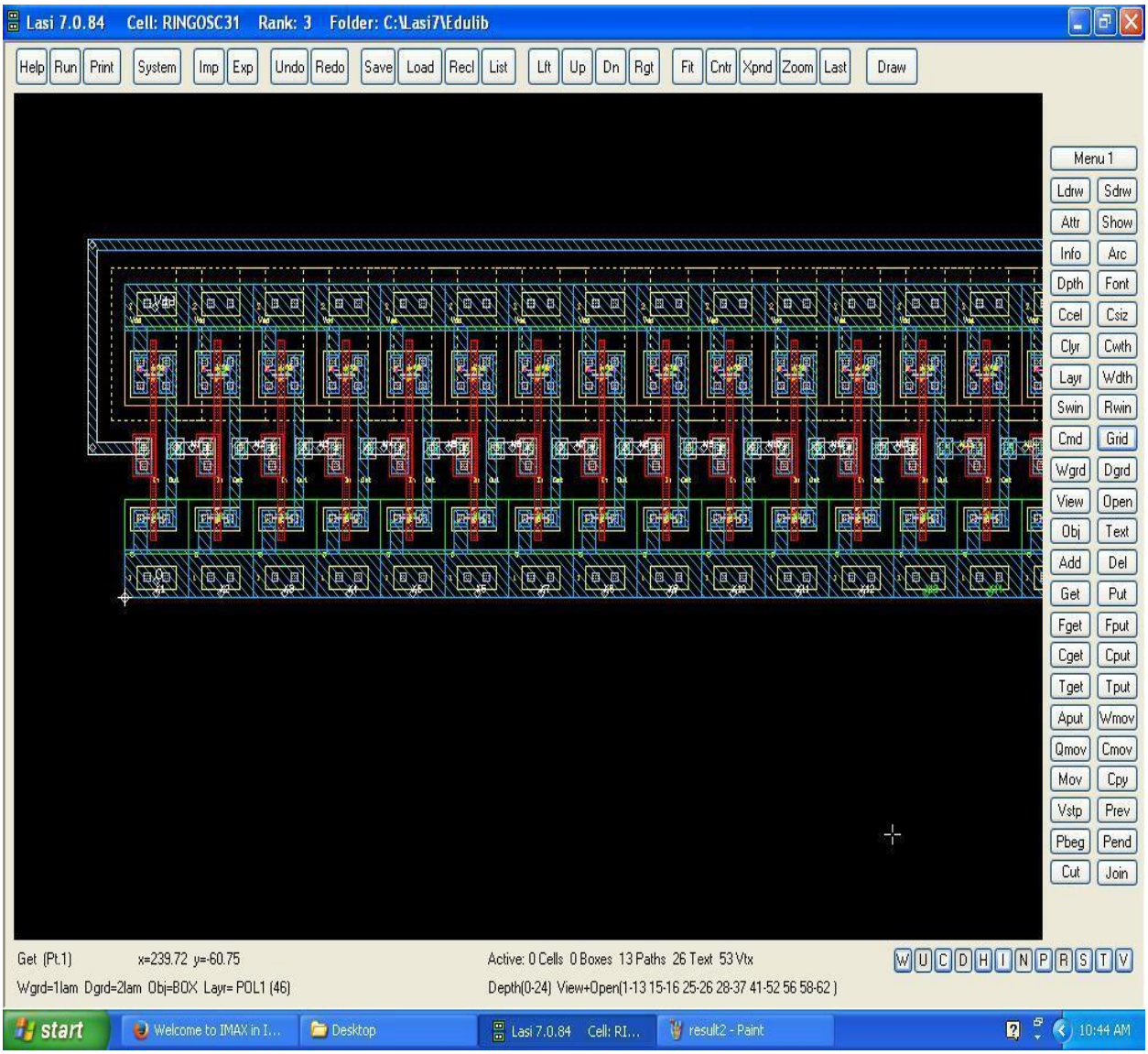

Figure 5.8 Design Layout of VLSI Circuit (Ring Oscillator) Using Ozone Oxidized FinFETs.

The above shown figure is the design layout of 31-stage ring oscillator circuit. 31 CMOS inverters have been used in this design in order to get the desired results. The design has been made using the tool LASI and the technology used in 60 nm. The white lining in the layout

indicates the application of ozone i.e. ring oscillator comprises of FinFETs and the FinFETs now are ozone oxidized in order to prove the application of ozone at the design level.

The zoom in figure of the design layout of the ring oscillator using ozone oxidized FinFETs is pictured below:

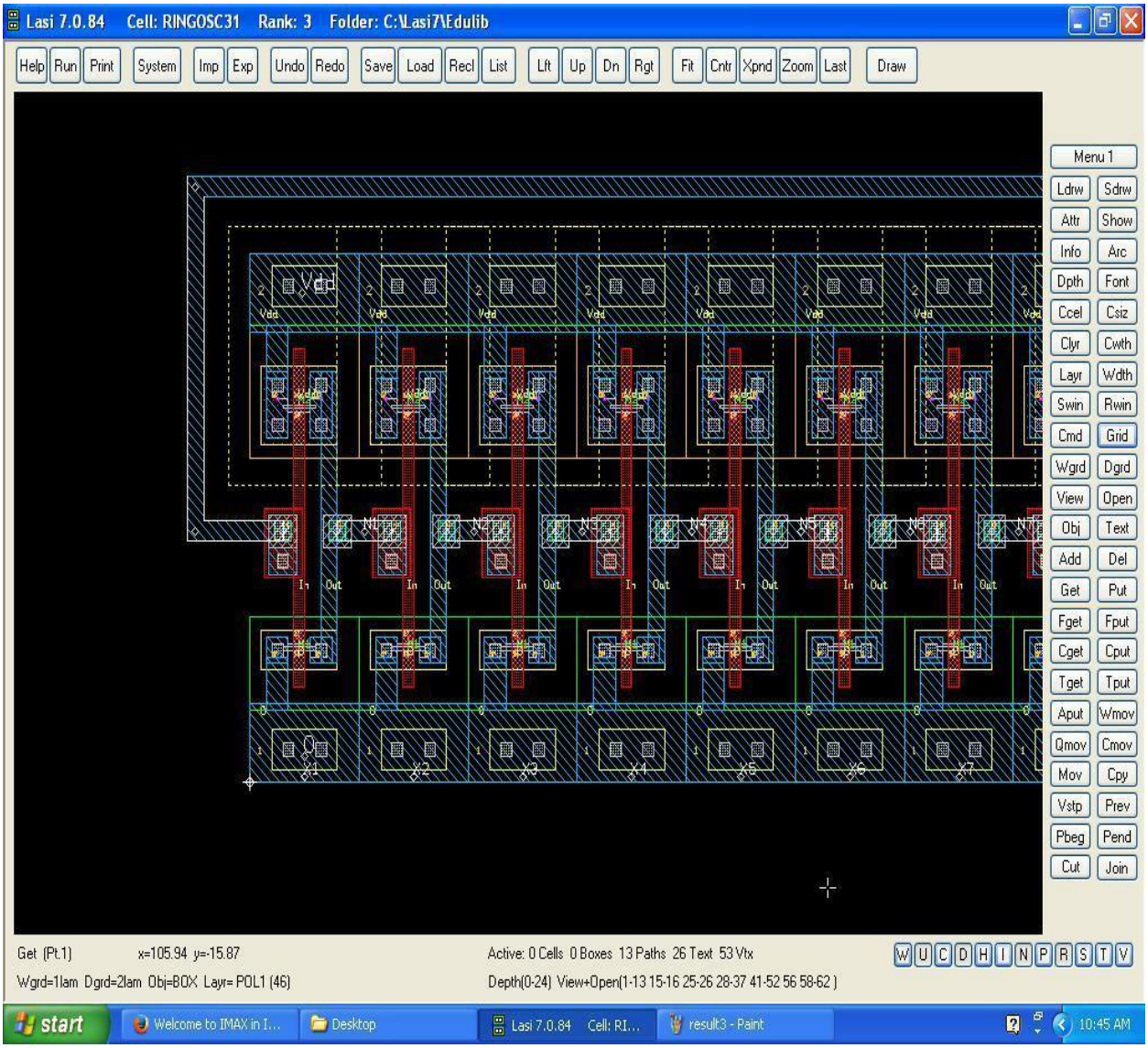

Figure 5.9 Zoom in figure of the design layout of the 31-stage ring oscillator using ozone oxidized FinFETs.

5.5 OUTCOME

In this chapter, the design layout of the 31-stage ring oscillator using ozone oxidized and without ozone oxidized FinFETs has been discussed keeping in mind the FinFET library

characteristics and thus results should be carried out by simulation.

CHAPTER 6

Results and Simulation

In this chapter device level comparison is done between the simulation results obtained by using ozone oxidation and without ozone oxidation.

6.1 INTRODUCTION

In this chapter the results of various experiments performed for the evaluation of the different parameters of low temperature ozone oxides are presented. The low temperature oxidation process using ozone is firstly evaluated through various processes and then the device level implementation of the low level oxidation process using ozone for VLSI is presented.

6.2 EFFECT OF PRE CLEANING AND PASSIVATION ON OXIDE QUALITY

To study the effect of pre cleaning and passivation on oxide and oxide interface. We have processed samples with fabrication steps discussed in chapter 3. And we have obtained MOS capacitors of five different device areas (table 6.1) on two differently processed silicon substrate. One substrate is passivated with hydrogen (-H) and other one is with hydroxyl (-OH) and the effect observed in different optical and electrical characteristics are as follows.

Table 1.1 Metal dot of different deposited

Area1	7.78e-3 Cm^2
Area2	4.62e-3 Cm^2
Area3	1.86e-3 Cm^2
Area4	3.317e-4 Cm^2
Area5	5.178e-5 Cm^2

6.2.1 EFFECT ON OPTICAL THICKNESS

The optical thicknesses of both the samples are measured using spectroscopic reflectometry using the Nanocalc - DUV system from Ocean Optics Inc. Germany. The measurements are done at different locations on the sample and the results obtained are as follows:

Table 1.2 Optical thickness obtained using spectroscopic reflectometry.

	Maximum Thickness Recorded	Minimum Thickness Recorded	Average Thickness Recorded
-OH Passivated	**1.35 nm**	**1.18 nm**	**1.21 nm**
-H Passivated	**1.89 nm**	**1.65 nm**	**1.80 nm**

6.2.2 EFFECT ON BULK DEFECTS

Gate current through oxide of thickness in this range is mainly depended on two phenomenon 1) Tunneling current 2) Charge hopping through bulk defects in SiO2 [35].The leakage currents density obtained for the devices of different area distributed across the wafer are as follows:

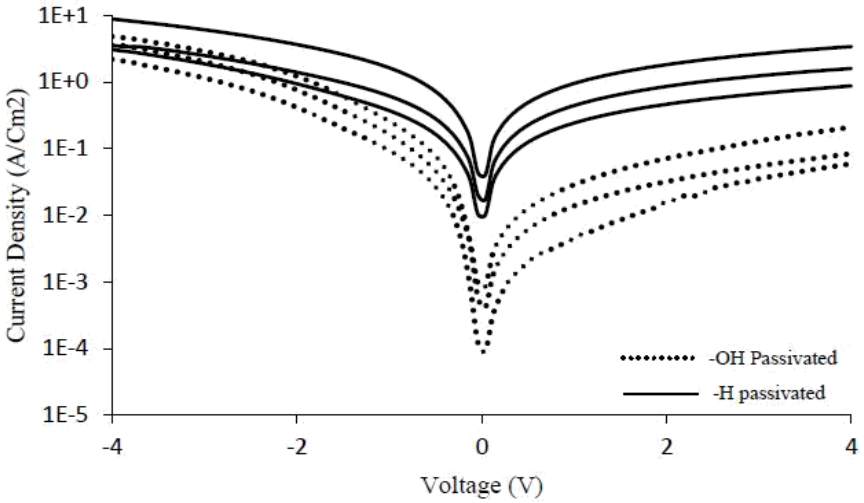

Figure 6.1 Gate leakage current density for different devices of area 7.78e-3 cm2distibuted across wafer.

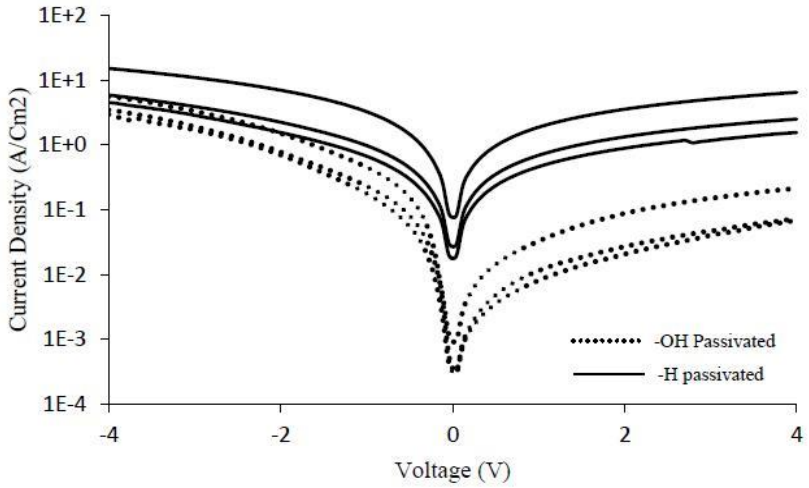

Figure 6.2 Gate leakage current density for different devices of area 4.62e-3 cm2distributed across wafer.

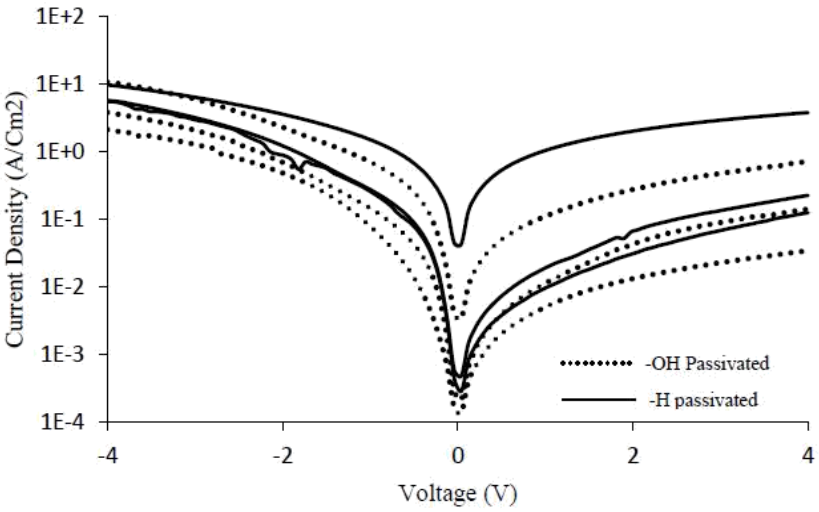

Figure 6.3 Gate leakage current density for different devices of area 1.86e-3 cm2 distributed across wafer.

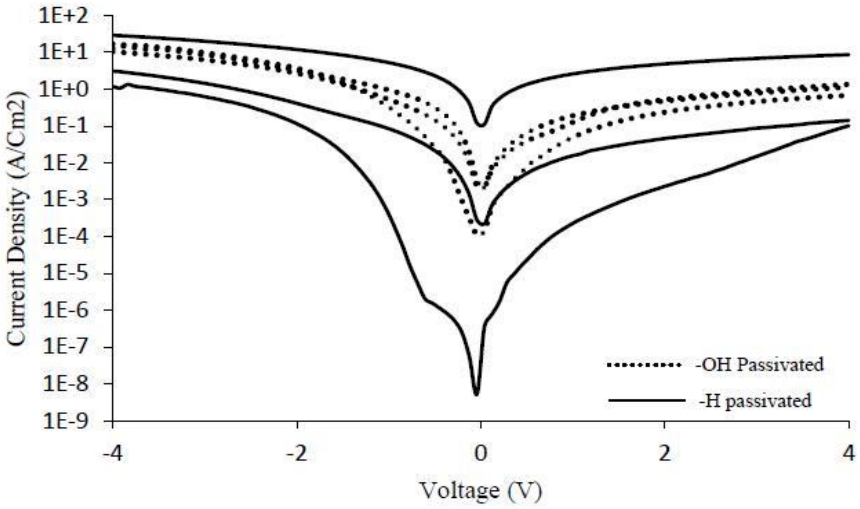

Figure 6.4 Gate leakage current density for different devices of area 3.317e-4 cm2distributed across wafer.

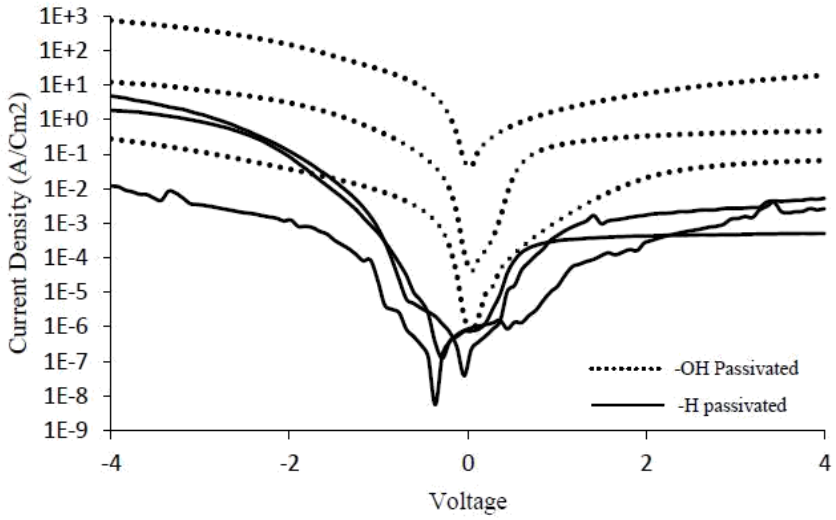

Figure 6.5 Gate leakage current density for different devices of area 5.178e-5 cm2distributed across wafer.

As described, we know that both –H and –OH covered silicon surface shows an initial repulsion to the O_3 molecule and thus initially cause a little inhibition in SiO_2 growth. But from the differences in the final optical thickness that we have measured, it can be concluded

that –OH ions provide more inhibition for SiO2 growth. The gate leakage is dependent on two factors:

1) Tunneling of charge carriers

2) Conduction through bulk defects.

The behaviors shown by leakage current density for small and large area devices shows that for large area devices the defect assisted leakage is prominent as compared to tunneling component of current in –H passivated devices even though the thickness is high as compared to –OH passivated but since defects are randomly distributed over area and thus the defect associated component is decreased with area and since tunneling is high in –OH passivated, for small areas the leakage current is high in –OH passivated.

6.2.3 EFFECT ON Si-SiO_2 INTERFACE

To get the effect of pre cleaning and passivation on Si-SiO_2, C-V and Gp/ω vs f characterization of samples are been done.

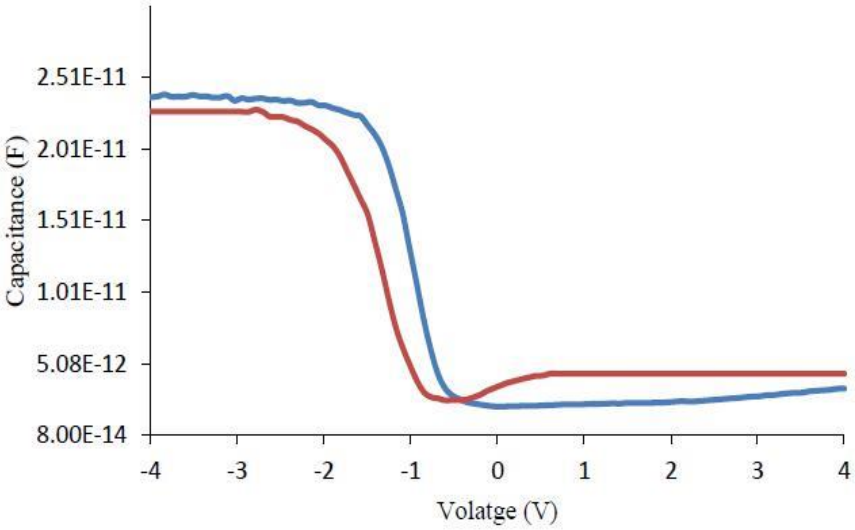

Figure 6.6 CV characteristics of different MOS devices with –OH passivated Si, tox= 1.2 nm.

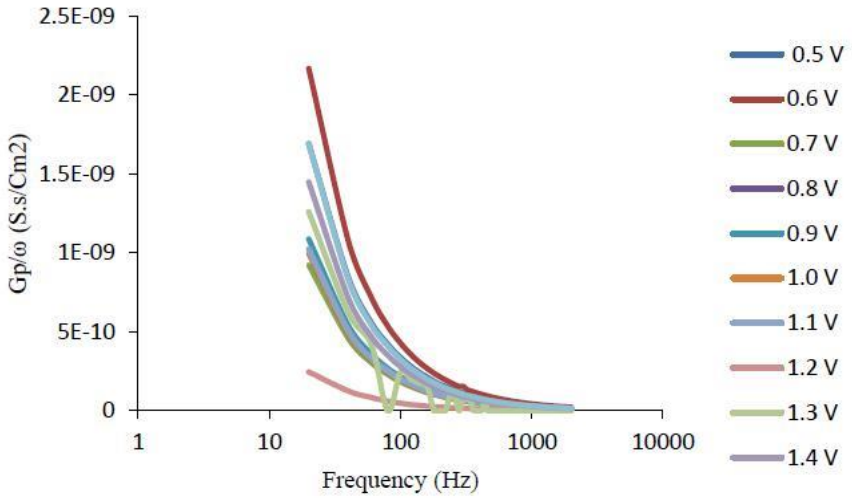

Figure 6.7 Gp/ω Vs f characteristics MOS capacitor with –OH passivated Si at different gate

voltages.

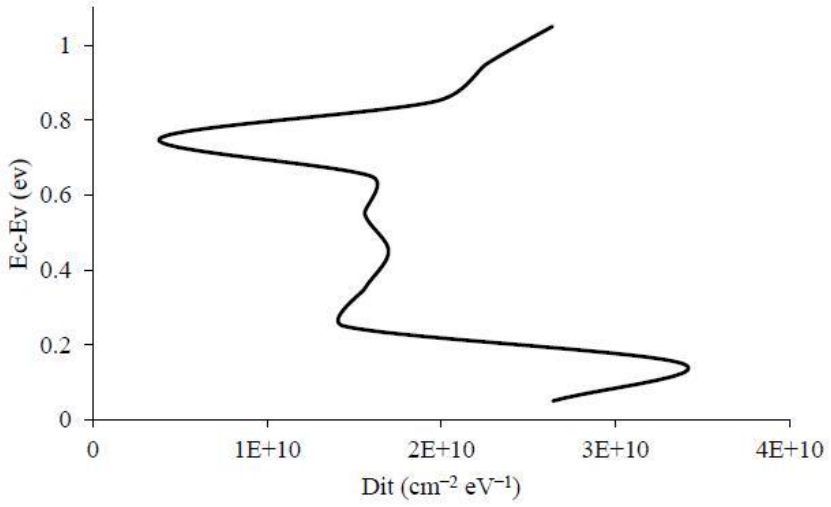

Figure 6.8 D_{it} Vs position within Si band gap for –OH passivated Si.

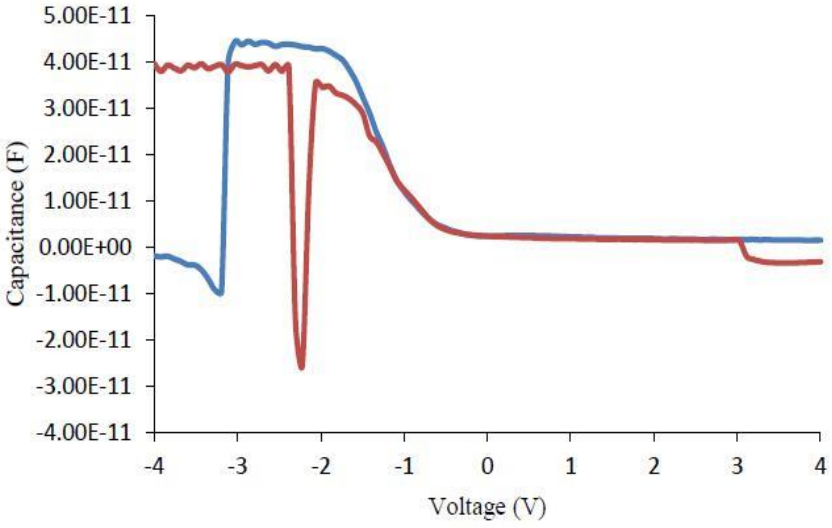

Figure 6.9 CV characteristics of different MOS devices with –H passivated Si, tox= 2nm.

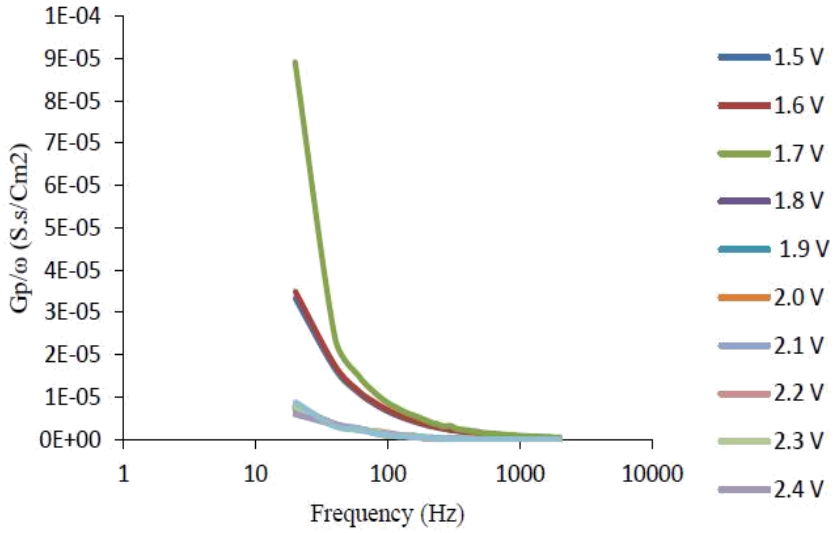

Figure 6.10 Gp/ω Vs f characteristics MOS capacitor with –H passivated Si at different gate voltages.

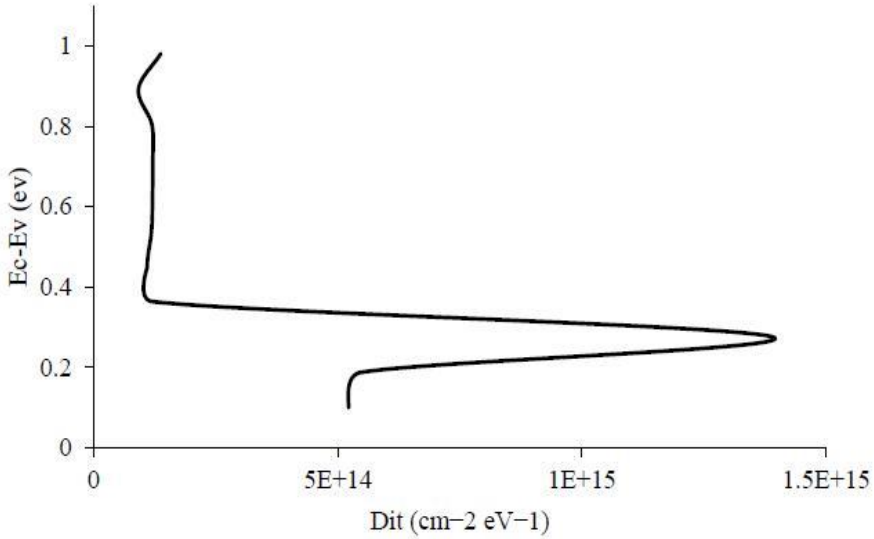

Figure 6.11 D_{it} Vs position within Si band gap for –H passivated Si.

The density of interface trapped extracted for both –H and –OH passivated samples, as there is huge difference in density of interface traps in both the samples. For –OH passivated samples the maximum D_{it} recorded is 3×10^{10} while in –H passivated samples it is going to 1.5×10^{15} which gives the difference five orders of difference.

6.3 EFFECT OF OXIDATION TEMPERATURE ON OXIDE QUALITY

To study the effect of temperature on oxide quality we have fabricated MOS capacitor with oxide grown at different temperatures. In this experiment we are growing oxide at four temperatures 50°C, 100°C, 200°C, and 300°C with ozone flow rate of 0.5 liter/minute to obtain MOS capacitors. The substrate is prepared by following the process steps described in chapter 3. And this study is done on –OH passivated surface because –OH passivation is enhancing the oxide quality in every aspect as compared to –H passivated substrate. The diameter of metal electrode is 0.6 mm. C-V and I-V characterization is done for evaluation of parameter such as leakage current, oxide thickness and mobile trap charges. The C-V characterization is done at 100 Khz frequency at room temperature.

6.3.1 C-V and I-V of MOS capacitors with oxide grown at 50°C

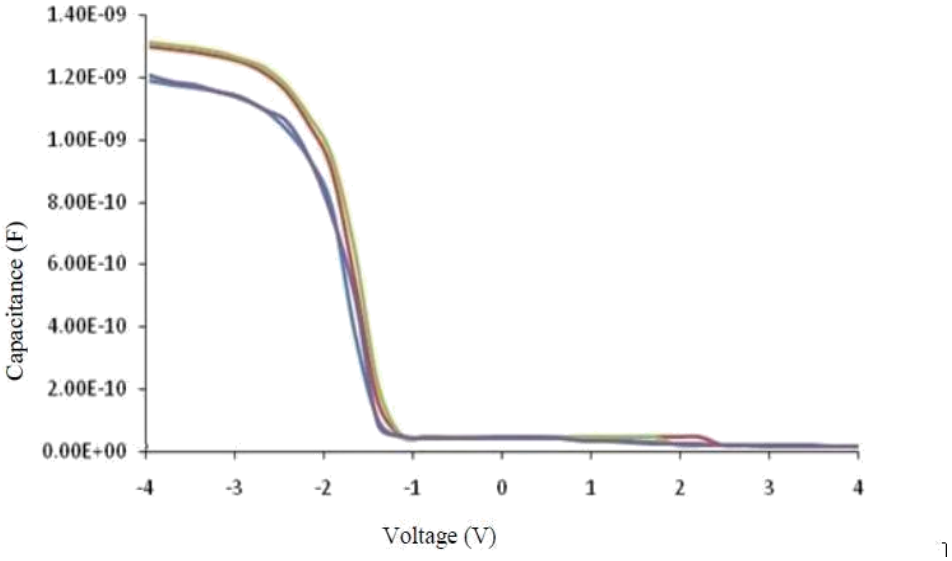

Figure 6.12 CV characteristics of different devices, tox= 2.5nm – 3nm.

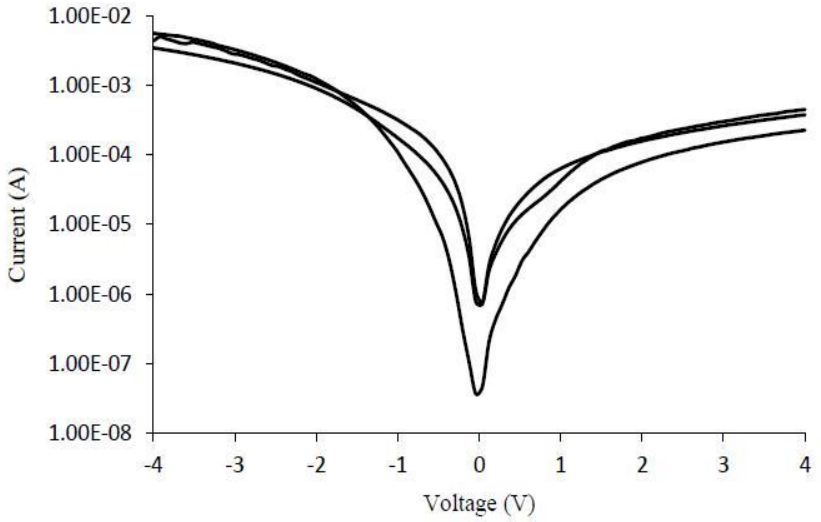

Figure 6.13 IV characteristics of different devices.

6.3.2 C-V and I-V of MOS capacitors with oxide grown at 100°C

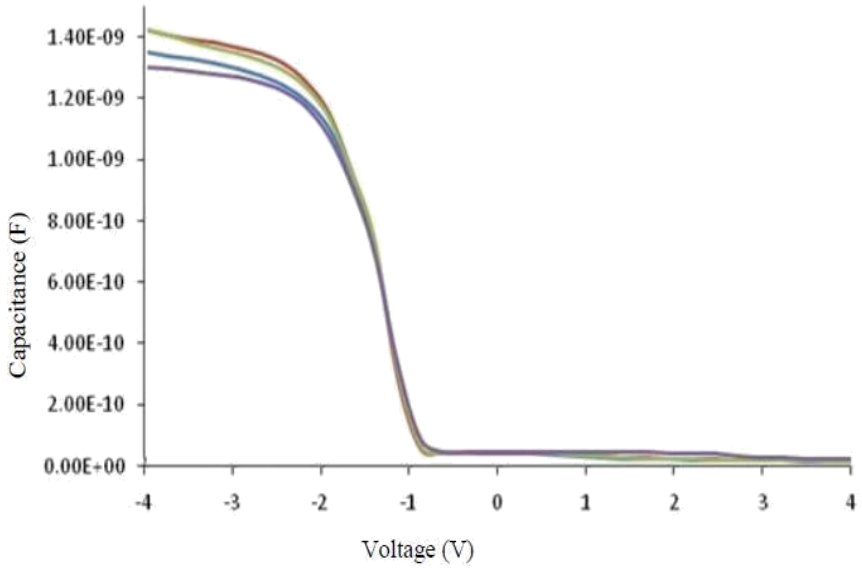

Figure 6.14 CV characteristics of different devices, tox= 2.5nm – 3nm.

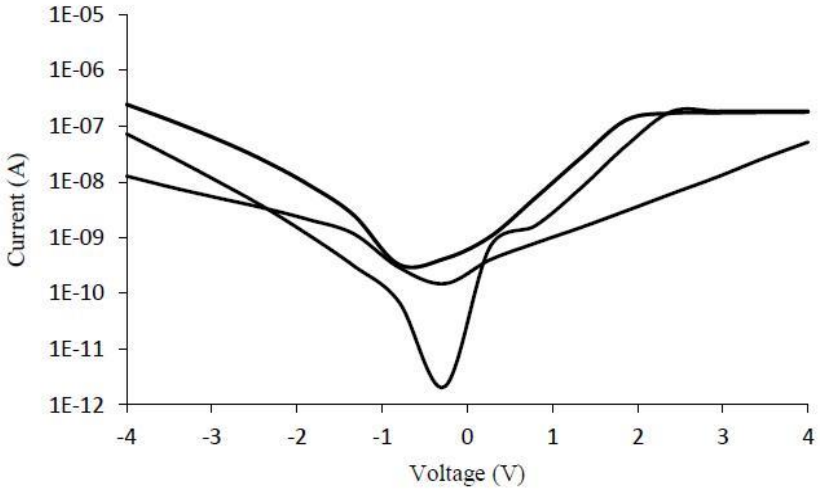

Figure 6.15 IV characteristics of different devices.

6.3.3 C-V and I-V of MOS capacitors with oxide grown at 200°C

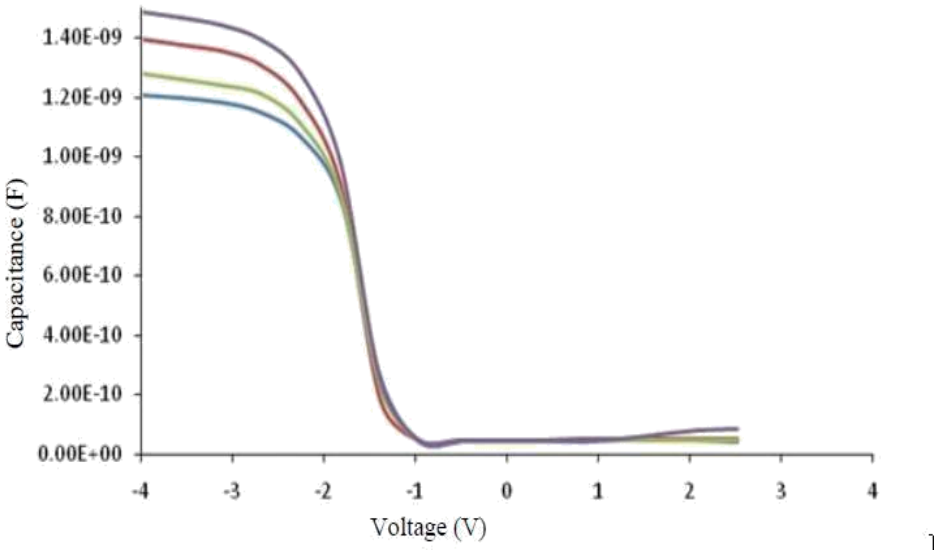

Figure 6.16 CV characteristics of different devices, tox= 2.5nm – 3nm.

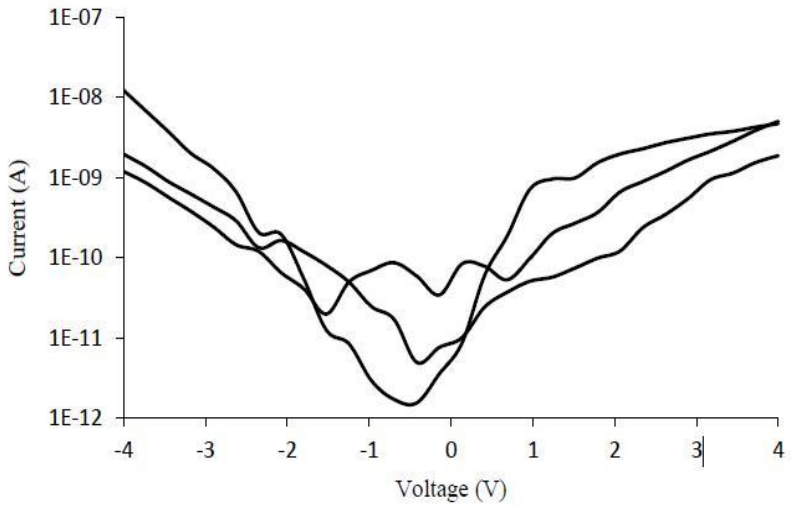

Figure 6.17 IV characteristics of different devices.

6.3.4 C-V and I-V of MOS capacitors with oxide grown at 300°C

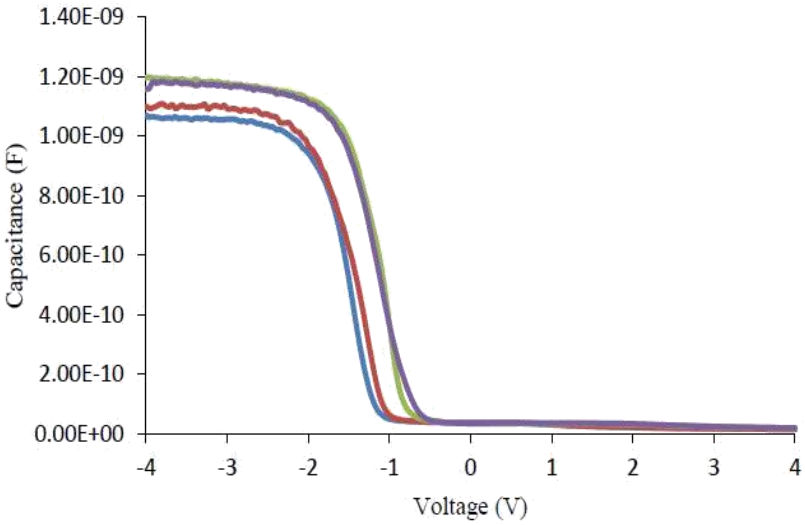

Figure 6.18 CV characteristics of different devices, tox= 2.5nm – 3nm.

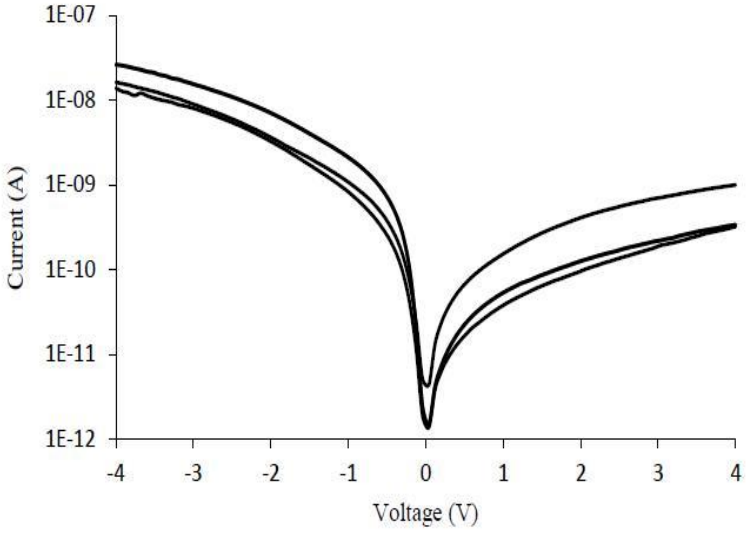

Figure 6.19 IV characteristics of different devices.

With increase in temperature, the drop in gate leakage current is observed even the thickness of SiO_2 is nearly same which suggests that this increase in gate leakage current

is due to increase in defect assisted leakage through SiO2 because for same oxide thickness the tunneling current component are equal. And the increase in inversion to accumulation

transition slope observed. Thus it is evident that with increase in oxidation temperature the quality of oxide is also enhancing.

6.4 RING OSCILLATOR CIRCUIT WAVEFORMS AND THEIR COMPARISON WITH OZONE OXIDIZED AND WITHOUT OZONE OXIDIZED FINFETs GATES

Simulation results have also been drawn using MATLAB 7.3. Following waveforms shows the results comparison between ozone oxidized and without ozone oxidized ring oscillator circuit and the application of ozone has been seen below.

6.4.1 VARIATION IN ENERGY BAND OF THE ELECTRONS AND ENERGY BAND OF THE HOLES WITH OZONE OXIDIZED AND WITHOUT OZONE OXIDIZED DEVICES AND THEIR COMPARISON

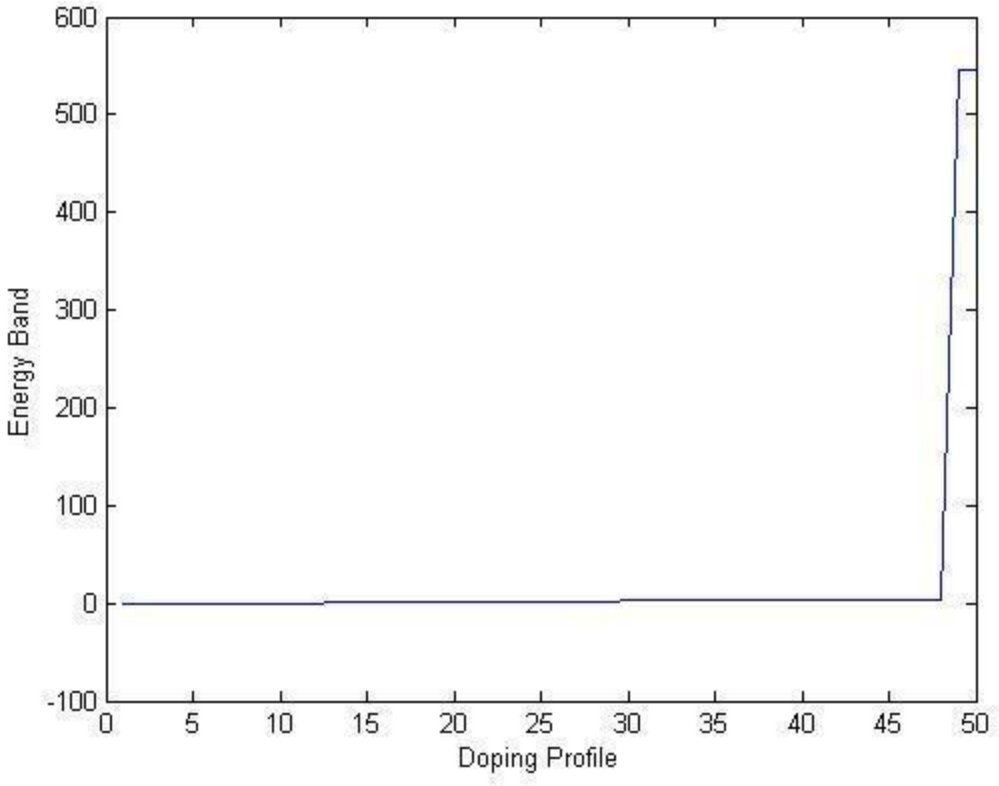

Figure 6.20 Energy band of the electrons in a CMOS transistor with a uniform doping profile.

This graph shows the energy band of the electrons in a CMOS transistor with a uniform doping profile.

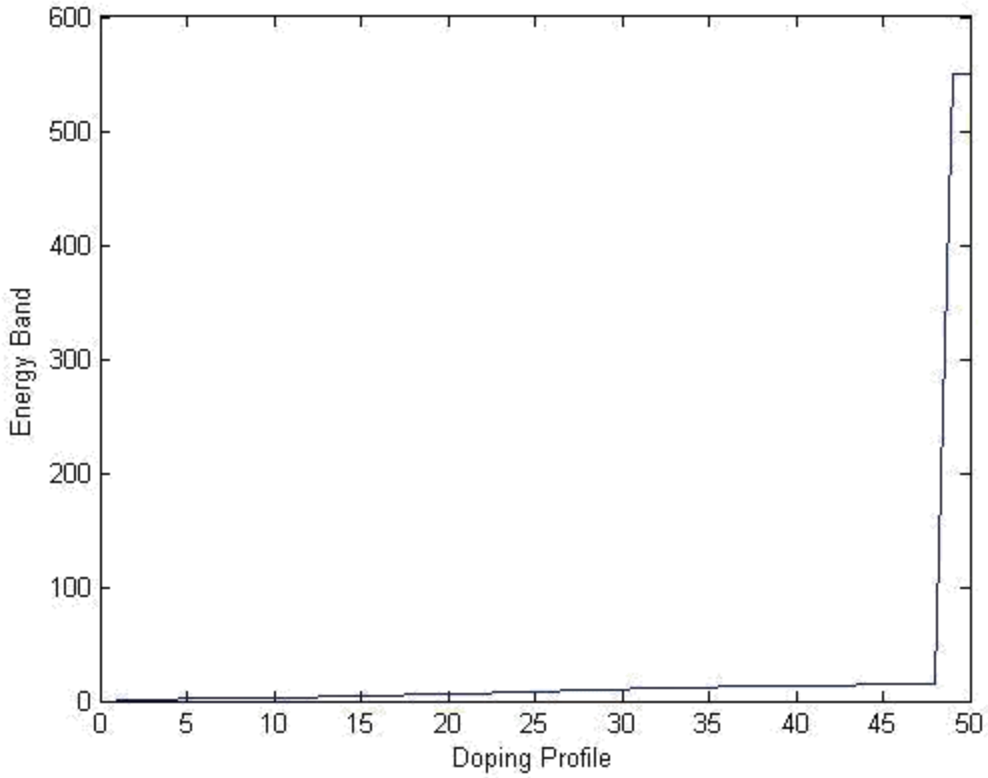

Figure 6.21 Energy band of the holes in a CMOS transistor with a uniform doping profile.

This graph shows the energy band of the holes in a CMOS transistor with a uniform doping profile.

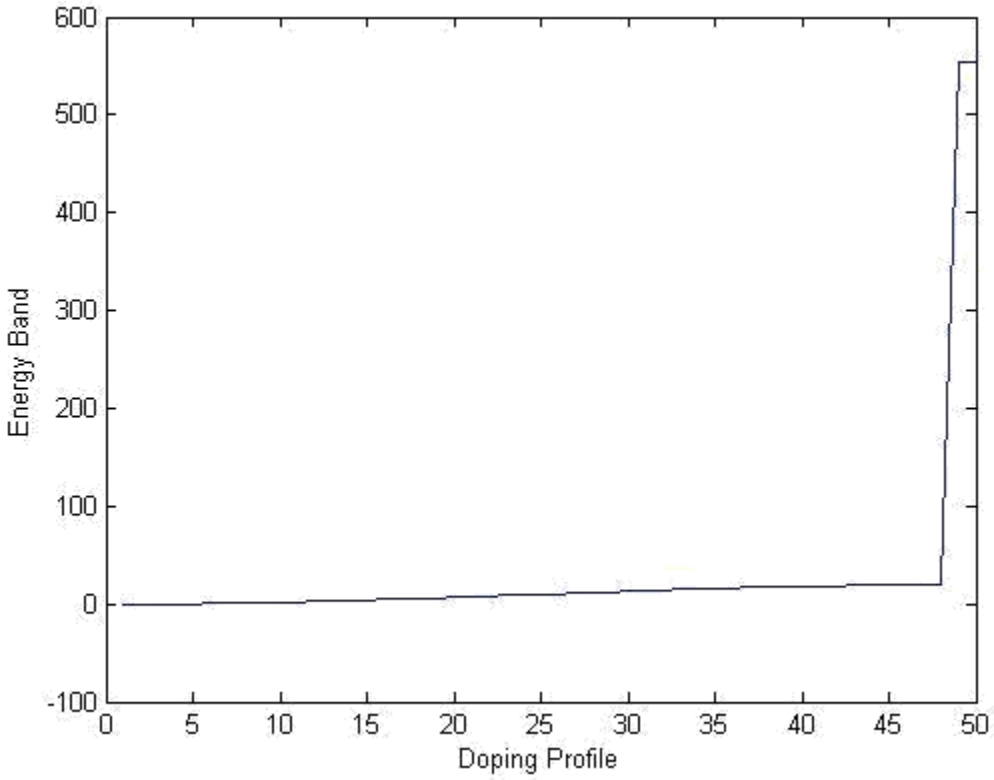

Figure 6.22 Energy band of the electrons in a CMOS transistor with a uniform doping profile and the gate oxidized with ozone.

This graph shows the energy band of the electrons in a CMOS transistor with a uniform doping profile and the gate oxidized with ozone. It is worthwhile to note the slight increase in the ramp from 0 to 48 mV in case of ozone oxidized CMOS while in case of non-ozone oxidized CMOS the curve is flat in that same region. This shows that the effect of ozone oxidization leads to higher dynamic performance characteristics for the device.

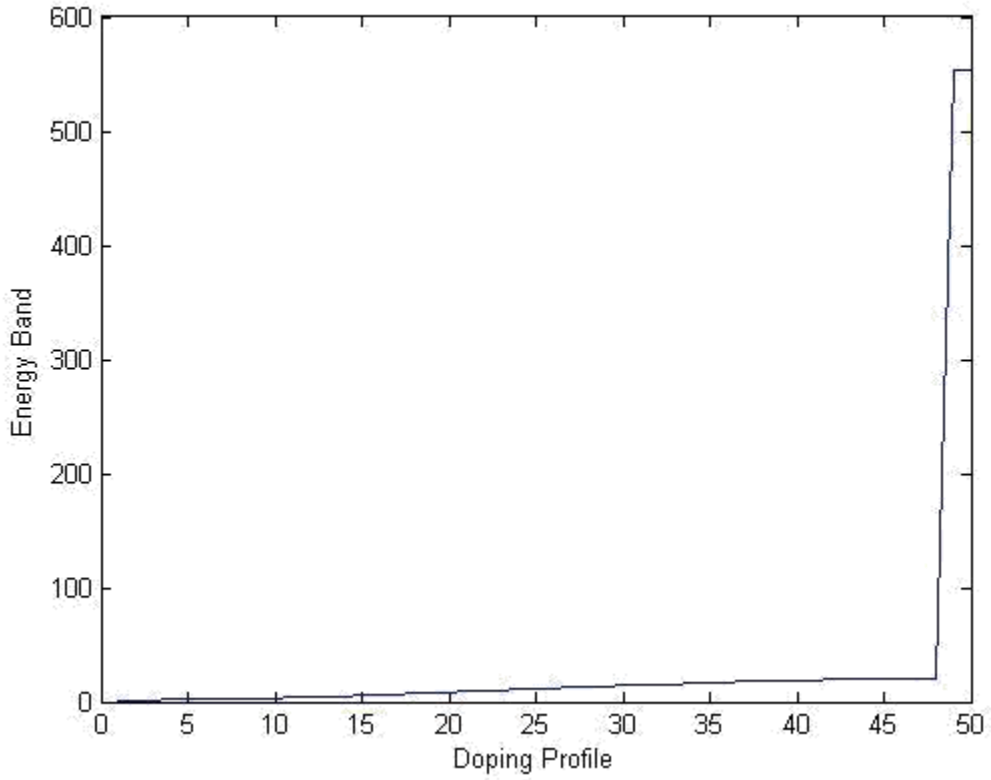

Figure 6.23 Energy band of the holes in a CMOS transistor with a uniform doping profile and the gate oxidized with ozone.

This graph shows the energy band of the holes in a CMOS transistor with a uniform doping profile and the gate oxidized with ozone. This is almost the same in case of non-ozone oxidized CMOS device.

6.4.2 VARIATION IN GATE POTENTIAL WITH OZONE OXIDIZED AND WITHOUT OZONE OXODIZED RING OSCILLATORS

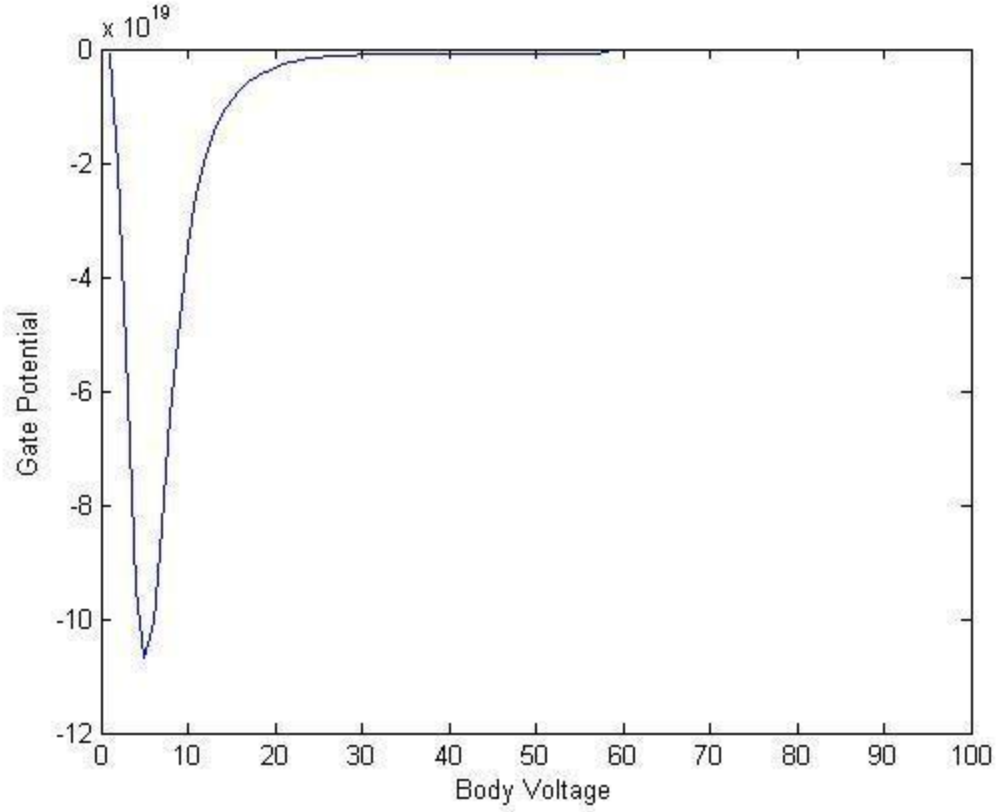

Figure 6.24 Variation of the gate potential without ozone oxidation in CMOS.

This graph shows the variation of the gate potential without ozone oxidation in CMOS. The gate potential without ozone oxidation has slightly less enhanced features as compared to ozone oxidized gates and thus it is elaborated in the next graph explanation.

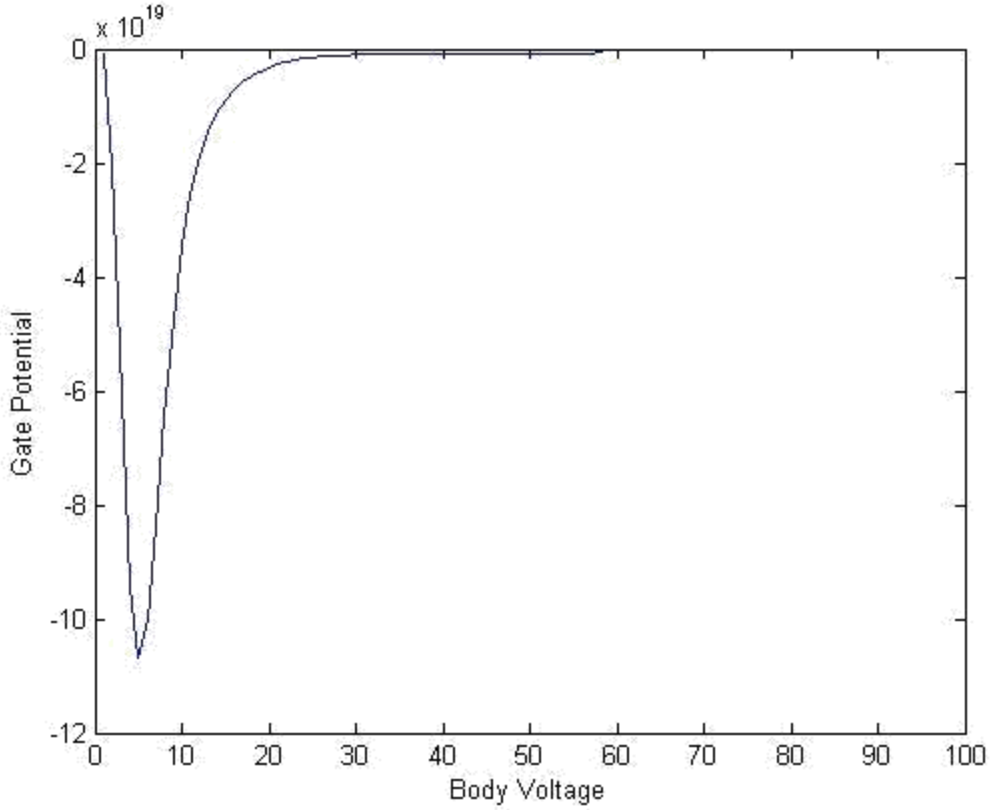

Figure 6.25 Gate potential with ozone oxidation in CMOS.

This is the gate potential with ozone oxidation in CMOS. Although both the curves are more or less the same, the gate potential in case of ozone affects the internal dynamics of conduction more than non-oxidized CMOS and thus enhance its application.

6.4.3 VARIATION OF Rho WITH BODY VOLTAGE

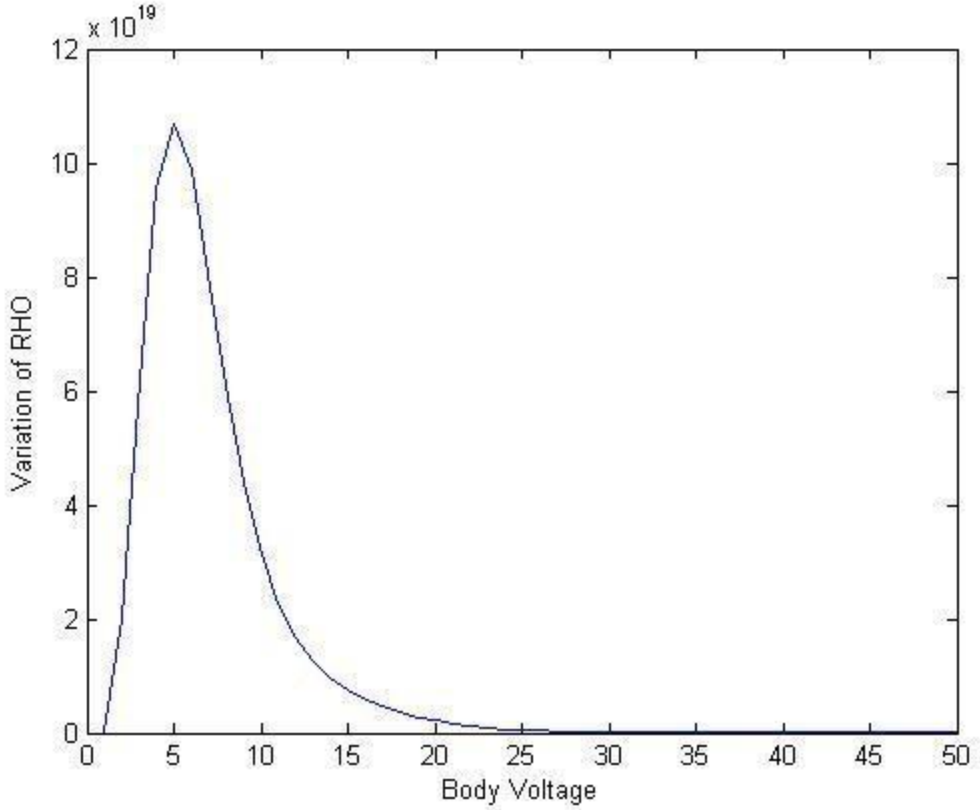

Figure 6.26 Variation of rho with body voltage without ozone oxidation in CMOS.

This is the variation of Rho with body voltage (in mV) in case of CMOS oxidized without ozone.

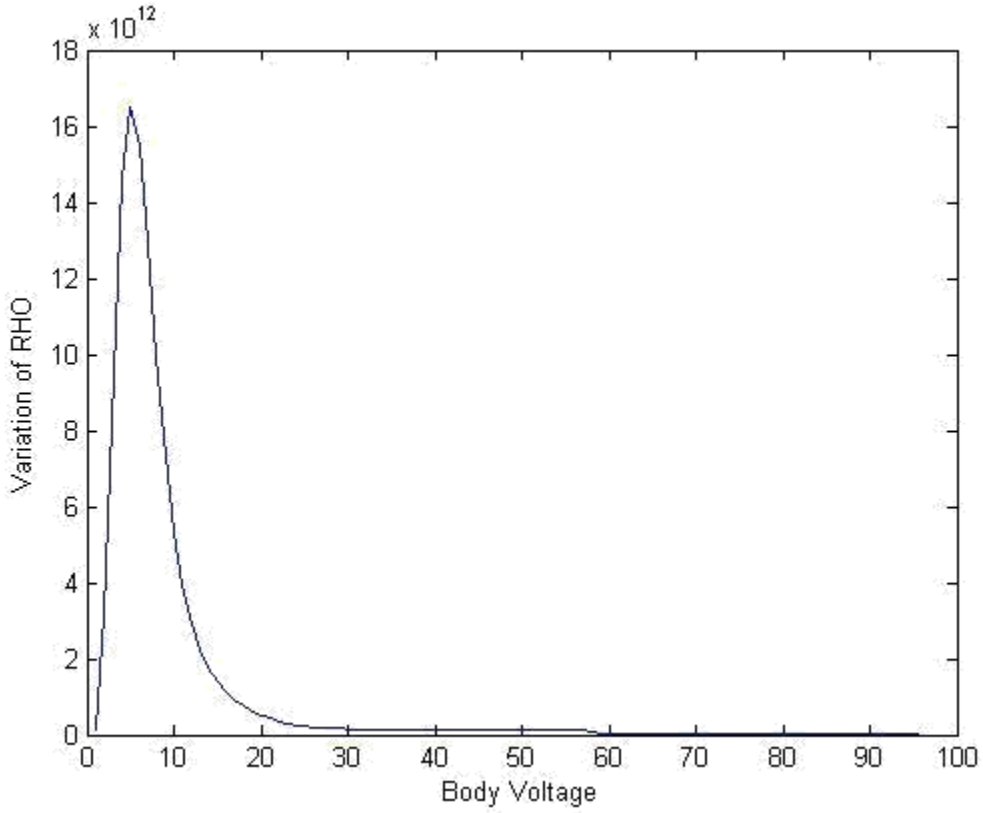

Figure 6.26 Variation of Rho with body voltage with ozone oxidation in CMOS.

This is the variation of rho with body voltage (in mV) in case of CMOS oxidized with ozone. Here we see a change in the Rho factor with the improved ozone characteristics. The resistivity of the material increases with the ozone oxidized gates.

6.4.4 VARIATION OF ΔV_0 WITH TEMPERATURE

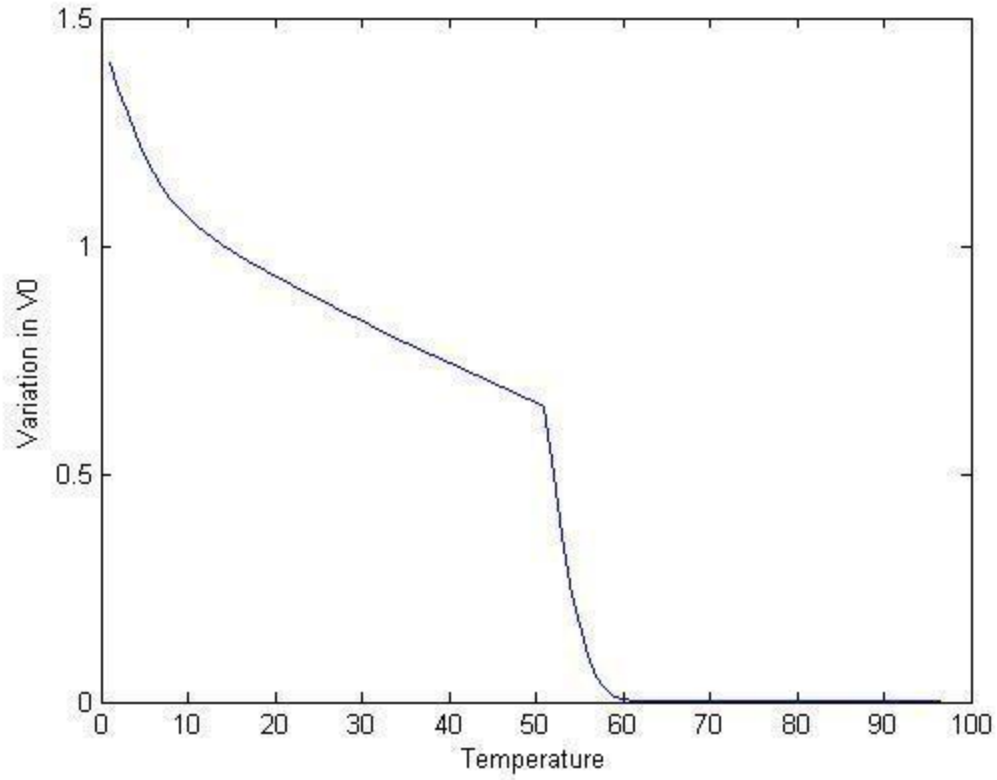

Figure 6.27 Variation of ΔV_0 in case of without ozone oxidized CMOS device.

Variation of ΔV_0 in case of without ozone oxidized ozone oxidized CMOS device. As with the increase in the temperature, the variation in the ΔV_0 reached to almost zero.

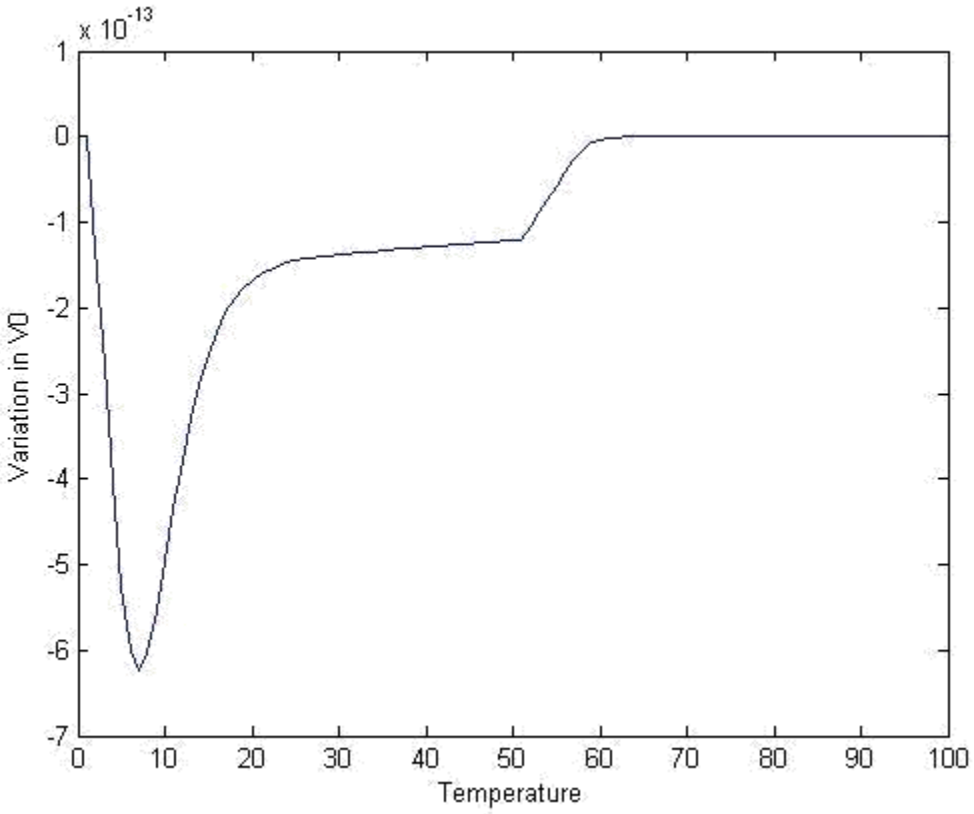

Figure 6.28 Variation of ΔV_0 in case of ozone oxidized CMOS device.

Variation of ΔV_0 in case of ozone oxidized CMOS device. This proves that the CMOS device can be fabricated at greater temperature bounds with higher performance compared to non-ozone oxidized CMOS devices.

6.5 OUTCOME

In this chapter, we have done optical characterization, current voltage characterization, capacitance voltage characterization for estimation of oxide quality of –H passivated and – OH passivated samples. And secondly, to study the effect of oxidation temperature on the quality of oxide on –OH passivated samples we have done I-V and C-V characterization of MOS devices with oxide grown at different temperatures and lastly various characterstics of oxidation through ozone and oxidation without ozone on ring oscillator design has been discussed and then the results of the various parameters have been compared.

CHAPTER

7

Conclusion and Future Scope

The main aim of using ozone in oxidation process is due to the fact that the use of ozone in VLSI leads to several advantages and leads to high quality oxide growth at low temperatures. With the use of the technology, several advancements has been made until now in the electronics era but it is not been used in large extend due to the some process implementation issues. So, the use of ozone in the VLSI leads to several advantages and advancement in the field of electronics but its implementation has not yet been in practice by the vendors all over the world due to some implementation errors seen by researchers as oxidation at room temperature has not yet fully in practice but will make a big difference in the electronic world if error probability may be reduced to some extent. This method of ozone oxidation can be successfully applied to other semiconductor and High-κ materials for semiconductor applications. Many researchers have shown the application of ozone oxidation of SiGe, GaAs and SiC and many High-κ materials, which can be studied and similar kind of passivation techniques can be developed for improvement in oxide quality.

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