Development of a Novel Single-Source Three-Phase Step-Up Multilevel Inverter Topology

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Submitted by

Manik Abrol
(Registration no.: 802042014)

under the guidance of

Dr. Krishna Kumar Gupta
Assistant Professor, EIED

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Electrical and Instrumentation Engineering Department
Thapar Institute of Engineering & Technology, Patiala
(Declared as Deemed-to-be-University u/s 3 of the UGC Act., 1956)
Post Bag No. 32, Patiala – 147004
Punjab

DECLARATION

I hereby certify that the work which is presented in dissertation entitled, "Development of a Novel Single-Source Three-Phase Step-Up Multilevel Inverter Topology", in partial fulfillment of the requirements for the award of the degree of **Master of Engineering in Power Systems**, submitted to Electrical & Instrumentation Engineering Department of Thapar Institute of Engineering & Technology (Deemed to be University) is as authentic record of my own work carried under the supervision of **Dr. Krishna Kumar Gupta**. It refers to work of other researchers which are duly listed in the reference section. The matter contained in this dissertation has not been submitted, neither in part nor in full to any other degree to any other university or institute except as reported in text and references.

Place:TIET, Patiala, Punjab (INDIA)

Dated : 25 August 2022

Manik Abrol

Roll No.: 802042014

It is certified that the above statement made by the student is correct to the best of my knowledge and belief.

Dr. Krishna Kumar Gupta
Assistant Professor, EIED

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MANIK ABROL

Roll No. 802042014

This work is dedicated to **SHAKTI**

CONTENTS

LIST OF FIGURES

Abbreviations and Acronyms

AC : alternating current

BCBB : bidirectional conducting & bidirectional blocking

BCUB : bidirectional conducting & unidirectional blocking

CHB : cascaded H-bridge

DC : direct current

DPST : double pole single throw

EV : electric vehicle

FACTS : flexible alternating current transmission system

FC : flying capacitor

FFT : fast fourier transform

LSPWM : level-shifted pulsewidth modulation

LV : low voltage

MI : modulation index

MLI : multilevel inverter(s)

MV : medium voltage

NPC : neutral point clamped

NPP : neutral point piloted

pf : power factor

POD : phase opposition disposition

PV : photovoltaic

PWM : pulsewidth modulation

rms : root mean square

SCMLI : switched-capacitor based multilevel inverter

SCU : switched-capacitor unit

SPST : single pole single throw

SPWM : sinusoidal pulsewidth modulation

SVM : space vector modulation

SW : switch

TCC : transistor clamped converter

THD : total harmonic distortion

UCS : universal control scheme

VSI : voltage source inverter

Abstract

DC to AC power conversion is required for numerous applications including electric drives, utilization of renewable energy sources and dc sources, flexible ac transmission systems (FACTS), etc. The use of Multilevel Inverters (MLI) have seen active development in these areas due to their various advantages such as reduced harmonics, voltage stress, etc. The classical topologies such as Cascaded H-bridge (CHB), Neutral-point clamped (NPC) and Flying Capacitor (FC) were the initial structures to be developed. But there are various issues which limited their use in some applications such as requirement of isolated DC sources and lack of voltage boosting capability among others. Switched Capacitor (SC) based topologies have the capability to boost the output voltage greater than input voltage, thus, giving a voltage gain greater than unity.

In this regard, this work proposes a novel SC based MLI (SCMLI) three-phase (3-ϕ) topology having a voltage boosting capability using a single DC input voltage source. The converter structure is able to provide voltage gain which is twice the applied input source voltage. Theoretical study and analysis are done to show the proper working of the proposed converter structure. The multicarrier based Level-Shifted Pulsewidth Modulation (LSPWM) strategy is used for the modulation of power semicondutor switches. The proposed MLI is able to provide bootsted line-to-line (l-l) pwm voltage output giving a five-level waveform. Further, soft charging of the switched capacitor strucutre is achieved by employing an inductor of a small value which is connected in series with input source. Finally, the simulations are performed and the obtained results are shown for a 100 KW inverter having an input voltage of 285V to validate the working of the topology. Here, LSPWM strategy using both Phase Opposition Disposition (POD-LSPWM) and Phase Disposition (PD-LSPWM) techniques is used for the modulation of power semicondutor switches during simulation. And comparison between these two modulation schemes is done and results are presented which show that PD type LSPWM scheme gives better results.

Chapter-1
INTRODUCTION

DC to AC power conversion is required for numerous applications. These applications include electric drives, utilization of renewable energy sources & dc sources such as batteries or fuel cells and flexible ac transmission systems (FACTS), etc. Power converters which perform this dc to ac power conversion are called Inverters [1]. Some of the applications are shown in Fig. 1.1.

1.1. BACKGROUND AND MOTIVATION

Around 1970's and also later decades started to experience the emergence of a new inverter philosophy called the multilevel inverter (MLI) [2]. This can be attributed to different reasons which are mentioned and explained below.

The demand and utilization of increased power levels by the industry, which then began to reach the Mega Watt (MW) and above ranges, spurred the growth for the development of new power semiconductor devices, converter topologies and control methods [3], [4].Also, coupling of this with the fact that capability of devices is limited for high power levels. And it is difficult to connect an individual semiconductor device directly to grids even with medium voltage levels (2.3, 3.3, 4.16, or 6.9 kV) [4]. Thus, to achieve this high voltage withstanding capability one solution is to

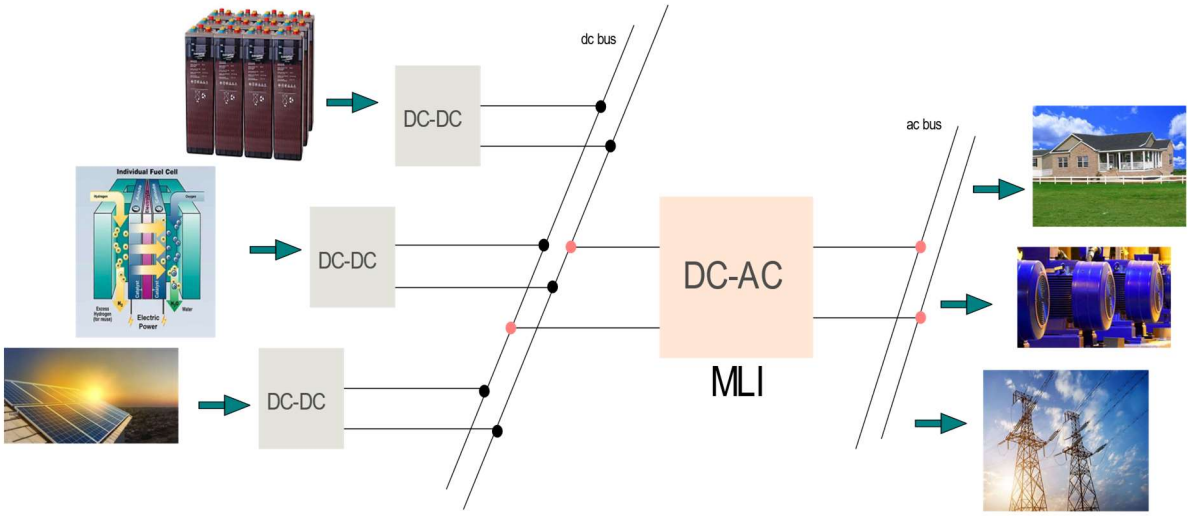

Fig. 1.1: Figure showing some of the typical applications of inverters

connect several devices in series having high voltage rating. But this is limited to low number of devices which are directly series connected [2].

Moreover, at higher power levels these devices have limited capabiltiy with regards to switching frequency which is several hundered of Hz to few KHz.

Thus, the outcome of all this was the emergence of different MLI topologies. These have been presented and explained in sections 1.2 and 1.3 with some classic and distinct topologies shown. And the basic concept of an MLI is explained in section 1.1.1.

1.1.1. THE CONCEPT OF MULTILEVEL INVERTERS (MLI)

The elementary concept of an MLI to achieve higher power is to use series connection of several dc voltage sources using power semiconductor devices to perform the power conversion by synthesizing a staircase voltage waveform of desired value. Capacitors, batteries, and renewable energy voltage sources can be used as the multiple input dc levels. These power semiconductor devices are used as switches which are in turn controlled so as to aggregate these multiple input dc levels to achieve high voltage at the output, while the rated voltage of the switches depend on the rating of the dc voltage sources to which they are connected. Thus, in general, the voltage stress on a power switch is much lower than the operating voltage.

Fig 1.2 shows the typical output voltage waveform of a multilevel inverter. The sinusoidal waveform is also shown in the same figure for comparison. We can note that the voltage waveform (blue colour) is a PWM stepped wave with two steps each above and below the reference axis (x-axis). Thus, this is a 5 level waveform including the zero level.

Ultimately, the conjunction of the basic MLI philosophy which gave staircase waveform, as shown in Fig. 1.2, with the other existing and subsequent inverter aspects, for instance, modulation and waveform quality requirements resulted in reaping of additional benefits.

For example, the general output requirement of dc to ac converters (inverters) is ac voltage of sinusoidal nature [5]. And this power conversion is achieved exclusively in switched mode form, i.e., semiconductor switches work in discrete form [6]. Hence, to achieve this pulse width modualtion (PWM) is used which reduces lower order harmonics by shifting them towards higher

side of the frequency spectrum. As a consequence, there lighter filters can be used depending upon the switching frequency and modulation strategy used. Moreover, use of more than one switching device to get different stairs of staircase waveform results in reduced switching frequency of individual switches [5].

As a consequence of all these things, Multilevel level Inverters have witnessed active development by researchers and industry.

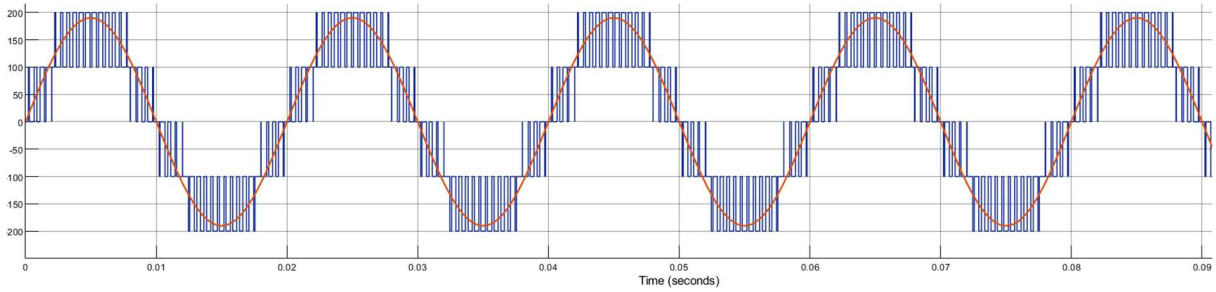

Fig. 1.2: Typical multilevel inverter output voltage waveform

1.2. LITERATURE REVIEW ON MULTILEVEL INVERTERS

This section presents a concise review on literature on multilevel inverters. Initially, the review begins with presentation of seminal work in this field with description of classical topologies. Later, the focus moves on to switched-capacitor based works.

In 1975, a patent describing the invention of a cascade inverter was published by Baker and Bannister [7], in a format that connects separately dc-sourced full-bridge cells in series to produce a staircase ac output voltage. This topology came to be known as the Cascaded H-bridge (CHB) inverter.

In another patent by Baker in 1980 [8], [9], through the manipulation of the cascade inverter, with diodes blocking the sources, the diode-clamped inverter was then derived. In contrast to the CHB inverter, this modified topology can produce multilevel waveforms from a single DC source, with additional diodes connected to the neutral point. This topology came to be known as the diode-clamped or neutral-point clamped (NPC) inverter. On the other hand in the same year, 1980, a research paper describing the implementation of NPC inverter using a PWM scheme was presented [10].

In the last decade of the 20th century, Meynard and Foch presented a new multilevel converter topology [11], having capacitors for clamping the ac output terminals of each phase-leg to half of the dc input voltage [12]–[14]. This topology is popularly called the flying capacitor (FC) topology. Other names which refer to the same topology are imbricated cell or multicell topology.

The three topologies, namely cascaded H-bridge (CHB), neutral-point clamped (NPC) and flying capacitor (FC) are considered as classical topologies which were the first to be initially developed into real industrial products [15]. These topologies are shown in Fig. 1.3, 1.4 and 1.5.

1.3. ISSUES WITH THE CLASSICAL TOPOLOGIES

Even though the presented classical topologies have come a long way since their inception, there are numerous issues which still plague them. Some of them are listed below:

1. They require multiple isolated dc sources for increasing their output levels. This results in cost increase in terms of transformers, rectifiers and filters [16].

2. Further, the output voltage of these converters is less than or equal to the input dc source voltage. This means they do not have voltage boosting capability.

3. Moreover, they have issues related to capacitor voltage balancing [16].

4. Also, the desire to increase the number of output voltage levels results in use of increased number of switch components, thus, requiring complex control.

From the above issues, it can be inferred that classical Voltage Source Inverter (VSI) topologies are inherently buck converters. This means that the output voltage is equal to or less than the supplied input voltage. Also, to achieve an increase, output voltage being greater than input voltage from a single input source, either a transformer be used or an auxiliary voltage source is required. This source can be in the form of an inductor which stores energy in the form of magnetic field, or it can be a capacitor which stores energy in the form of an electric field. And coupled with the fact that there is a desire as well as demand to achieve light and small sized ac power supply which should provide sinusoidal output of contant rms value even for large variation in line voltage or load [17]. It can be realised by consideration of utilizing a transformer or an inductor as an auxiliary voltage source that it would make the system bulky. This is because they would require large and heavy magnetic cores for high power [18].

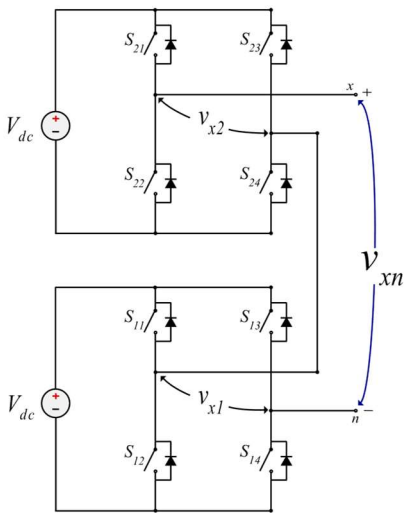

Fig. 1.3: single-phase leg of cascaded H-bridge (CHB) topology

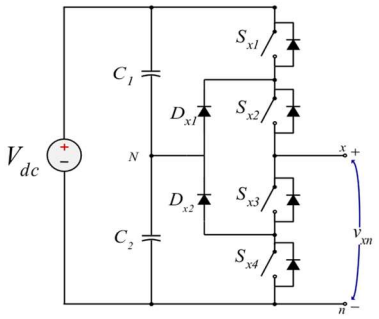

Fig. 1.4: single-phase leg of neutral point clamped (NPC) topology

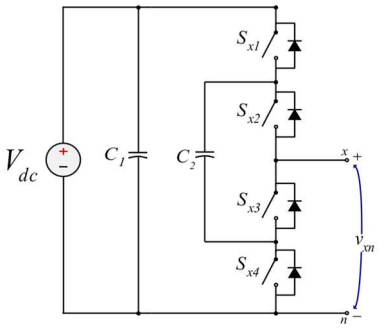

Fig. 1.5: single-phase leg of flying capacitor (FC) topology

Hence, the reduction in volume and weight can be achieved by novel magnetic core structures, core materials, converter topologies and control techniques [19]. As a consequence of all these things, capacitor is used an auxiliary voltage source. This results in the use of Switched-Capacitor based MLI (SCMLI).

Initially, the use of switched capacitor based principle was utilized and implemented in DC-DC converters. This was then soon followed by its use in DC-AC converters.

The above paragraph mentions the use of single source based topologies. There are a number of reasons which provide significance to their use. The application of topologies requiring use of multiple DC links necessitate that these sources are galvanically isolated from each other. Therefore, this in turn requires either separate multiple isolated DC sources be employed which are obtained from batteries, fuel cells, etc. or transformers and rectifiers be employed in case ac sources are used as input [20]. Moreover, controlled rectifiers would require their own associated gate drive units with auxiliary power supplies feeding them. All this makes the system bulky and increases its size as well as cost. Also, topologies utilizing asymmetric input sources excluding auxiliary capacitor sources would result in unequal ratings of voltage sources and switches [21]. Thus, increasing inventory control in terms of components. Moreover, use of multiple sources crops up the issue of unequal power sharing among the engaged sources [1], [21].As result of these

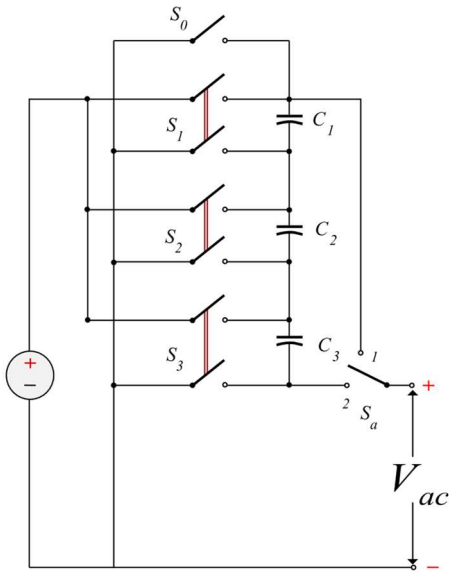

Fig. 1.6: General structure of SC converter as presented in [19]

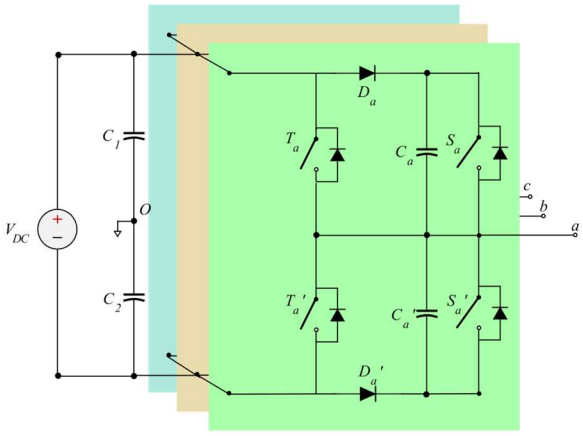

Fig. 1.7: three-phase topology as shown in [21]

concerns, there are various application scenarios where Single input DC voltage source is advantageous.

[22] was the initial paper which presented the use of switched capacitor principle in DC to AC power converters [17]. This work presented a general SC converter structure shown in Fig. 1.6. Although this structure shows only 3 capacitors it can be extended to n levels with n switches. These n switches, S_1 to S_n, are double pole single throw (DPST) type which are used to charge each capacitor sequentially from input dc voltage source while the switch S_a is single pole double throw which is used for polarity reversal and is thrown during ac waveform crossing a zero value. The switch S_0 is single pole single throw (SPST) which is used to generate negative peak value of output ac waveform.

[17] presented a SC based topology which is divided into two subcircuits, where each subcircuit contained equal number of basic SC cells which were formed from set containing a capacitor, two switches and two diodes. Further, it pointed out that earlier topologies and their implementation lacked regulation capabilities for changes in line load. Hence, it adopted strategy for improving voltage regulation in which the charging was divided into two phases – odd and even. Using this the ratio between the duration of odd and even phases was changed to adjust for the changes in load.

[18] proposed an SC topology based on Marx inverter structure with an H-bridge. It used less switching components than some of the earlier SC structures. Also, the H-bridge is used to generate the positive and negative polarity of the voltage waveform.

[23] presents two SC-based topology based on simple and basic switched-capacitor unit (SCU). This frontend SCU produces positive voltage levels while backend H-bridge topology helps to get both positive and negative output levels. The frontend can be built up from series connection of one or more SCU to get more voltage levels. Both first and second topologies take up CHB form with the difference between the two that second topology consists of an additonal switch and a diode giving it a capabiltiy to bypass an individual CHB cell.

[24] presents a single source based 3-phase topology consisting of a SC based frontend with half-bridge as output configuration in each leg. Each switched-capacitor is charged to a value equal to the input voltage source, V_{DC}. Further, the output pole voltage of values $\pm$ (0.5 V_{DC} & 1.5 V_{DC}) and giving a 7-level output line voltage. This topology is shown in Fig. 1.7.

1.4. RESEARCH GAPS AND OBJECTIVES OF STUDY

- The presented topologies in the literature have been developed mostly for single phase applications, even though their 3-phase Y-configuration may be done using same three single-phase structures [24].
- As a consequence of this number of devices employed increases considerably including the number of used capacitors.
- Moreover, most of these topologies would also require n number of isolated DC voltage sources for an n-phase configuration.
- Also, increased use of devices happens to use larger number of gate drivers and hence, increasing the volume and weight as well as gate driver losses.
- All of this results in increased cost and complexity.

Thus, the objective is to develop a topology which reduces the mentioned drawbacks. This would be an attractive proposition to study from an academic viewpoint and to explore new features

which emnate out from such an analysis. And ultimately, this would be developed for practical as well as industrial purposes.

1.5. METHODOLOGY

The review of the literature on multilevel inverters brought into light some of the issues concerning the use of classical topologies, which are listed in section 1.3. Among those listed in section 1.3, some of them were discussed such as limitations for the use of multiple isolated DC sources, lack of voltage boosting capability, etc. It was then identified that the use switched capacitor multilevel inverter topologies using single input DC source is able to resolve some of those issues. In this regard, section 1.4 further identifies the limitations in earlier SCMLI topologies being proposed. These limitations could be resolved by the use of single DC source, reduction in number of employed switching devices, reducing current spikes while charging of switched capacitors, and development for 3-phase operation of topology.

The consequence was the conception of a novel switched Capacitor mulitlevel inverter topology, which is described and its various apects are explained in Chapter-2. The main highlights of which are the use of single input DC voltage source, limiting the current spikes of switched capacitors during charging and presentation for the 3-phase operation of the topology.

The conception is followed by identification of the valid switching states which are necessary for the understanding and to develop the operation of the converter topology. The use of switched capacitor principle for voltage boosting requires proper identification of charging paths for charging of switched capacitors. These charging paths are shown with determination of equivalent charging circuit for analysis of charging current. The current spikes could be suppressed by delaying the charging of the capacitor. This is due to the fact that in general the switched capacitor topologies form an RC equivalent charging circuit. And the response of an RC circuit to a DC voltage source gives an initial current spike. Hence, an inductor of small value is used to change the response of the circuit which limits the sudden current spike.

The different modes of the topology are then developed. Ultimately, it is the modulation strategy which is used for switching the power semiconductor devices, thus, driving the converter to get output voltage. Hence, the modulation of the topology is done and the scheme used for the same

is shown in section-2.6. This scheme is implemented using universal control scheme which is also shown there.

Finally, the simulation of the proposed topology is done in MATLAB/SIMULINK environment to validate the working of the proposed converter structure. The model is run and various results were obtained. These results are shown and discussed in Chapter-3.

Further, there are various aspects which are identified in Chapter-4 which could be used to improve upon this work. The flow chart representing the work flow of the process followed in the research work is shown in Fig. 1.8

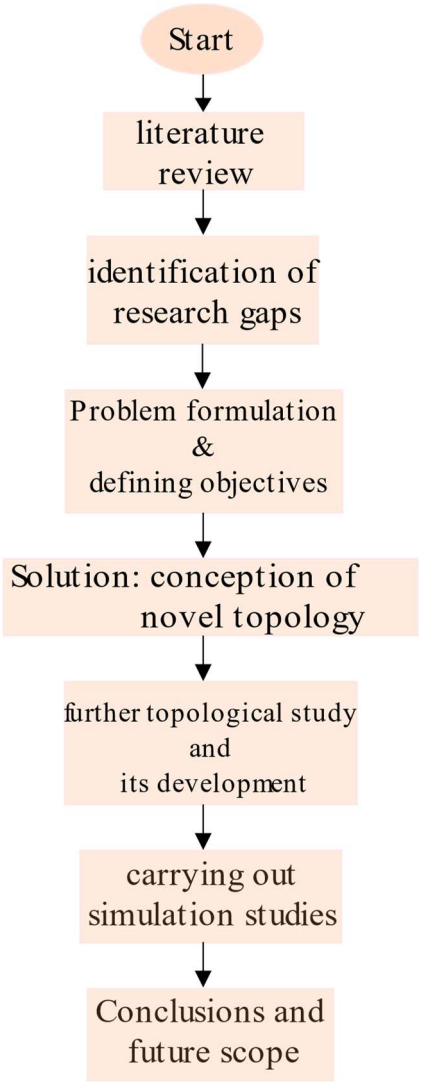

Fig. 1.8: flow chart representing the work flow followed in the research work

1.6. ORGANISATION OF THE REPORT

This section presents the details of the organisation of the report. Chapter-1 introduces the reader with the subject of the present report alongwith background and motivation of the work. It also presents the review of the literature on multilevel inverters. It further discusses the issues in the available literature and the research gaps that this work tries to address.The last section lists the materials and methods that are used and applied in the study, design and analysis of the presented work.

Chapter-2 presents the proposed topology and the analysis performed along with necessary explainations and descriptions for synthesis of different pole voltages, charging of switched capacitors and modualtion strategies wherever required.

Chapter-3 shows the simulation studies which are performed for the proposed topology. This also presents the obtained results from the simulation and the discussion of the results.These reults also contain the comparison between the two types of LSPWM schemes (POD and PD types) used during simulation of the converter structure.

Chapter-4 finally discusses the main conlusions of the overall work being done and analysed. Further, it details the numerous aspects of the MLI converters related to the work that has been done and which can be further studied and improved upon under the future scope section.

Chapter-2
PROPOSED TOPOLOGY

2.1. DESCRIPTION OF THE TOPOLOGY

The topology is shown in the Fig. 2.1. It comprises of 3-phase T-type topology consisting of 8 bidirectional conducting & unidirectional blocking (BCUB) and 3 bidirectional conducting & bidirectional blocking (BCBB) power semiconductor switches with 2 power diodes. The input is provided from a single dc voltage source, V_{DC} , which is in series with an inductor, L_i . Further, this input from dc-source is provided in a controlled fashion using S_{c1} & S_{c2} which are in turn connected to the common split switched-capacitor link divided into two parts using capacitors C_1 and C_2.The schematic diagram below in Fig. 2.2 shows an individual phase leg of the proposed topology with the different conventions taken for the value of voltage and current flow across the various devices and components.

2.2. VALID SWITCHING STATES

Now, the valid switching states of the converter topology are presented. These represent the primary working states which are useful for understanding the operation of the converter. Table 2.1 shows the valid switching states producing different output pole voltage values in an individual

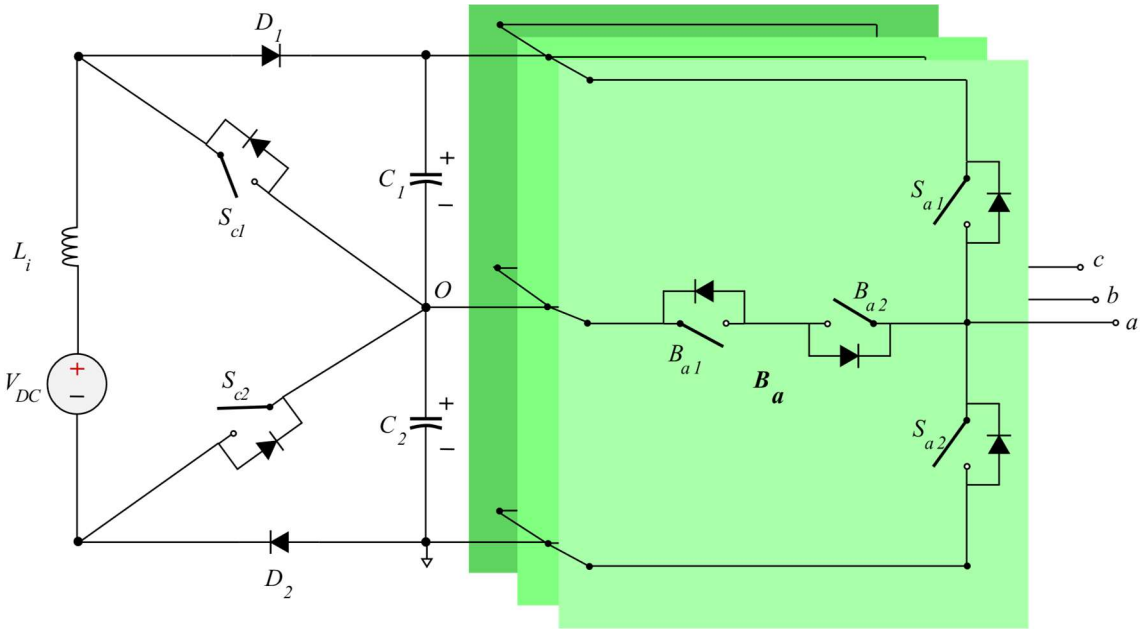

Fig. 2.1: Proposed T-type based SCMLI topology

phase-leg of T-type inverter.

2.3. CHARGING OF SWITCHED CAPACITORS

The switched capacitors are charged in a controlled fashion by complimentary switching aciton of S_{c1} and S_{c2} for capacitors C_1 and C_2, respectively. When Sc_1 is switched on, the current will flow through C1 allowing it to charge. This charging of C_1 is shown in Fig. 2.3. Alternatively, when Sc_2 is switched on current will flow through C_2 allowing it to charge.This charging of C_2 is shown in Fig. 2.4.

Table 2.1 : showing switching states of t-type inverter to produce corresponding ouptu pole voltages

State	Active Switches	Output pole voltage
[T2]	S_{x1}, B_{x1}	$2V_{DC}$
[T1]	B_x	V_{DC}
[T0]	S_{x2}, B_{x2}	0

where x = a, b or c, standing different phases

n = 1 or 2

S_{xn} = BCUB switches in a corresponding phase-leg

B_x = BCBB switches of a corresponding phase-leg

[X] = state names

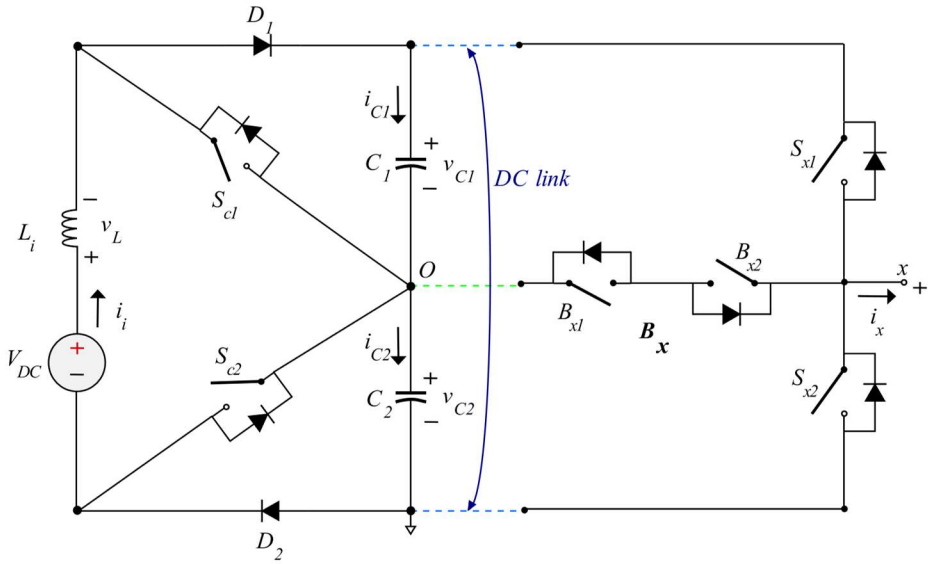

Fig. 2.2: Diagram showing different conventions used for analysis

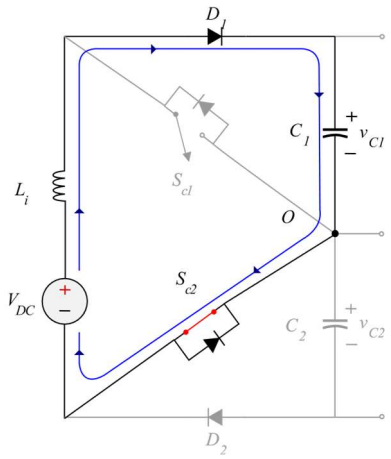

Fig. 2.3: Charging path of capacitor C1

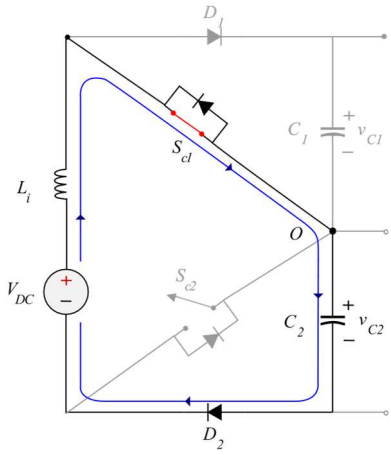

Fig. 2.4: Charging path of capacitor C_2

The charging loop in our case for both the capacitors consists of input dc source, an inductor, a switch and a diode. Thus, this will form an RLC circuit with a dc source and the choice of model that will be used for modelling the power semiconductor devices in the charging path. Theequivalent circuit is shown in Fig. 2.5. As a result, both the capacitors will approximately charge equal to the value of applied DC voltage. Thus,

$$v_{C1} = v_{C2} \approx V_{DC}$$

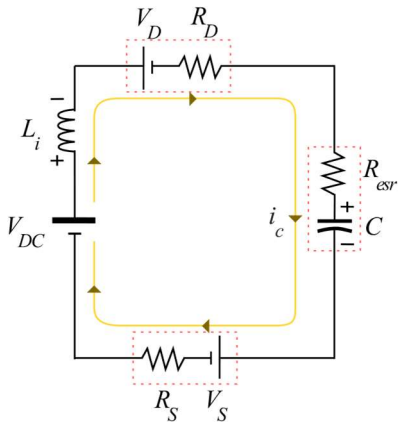

Fig. 2.5: equivalent circuit for charging of capacitor

In Fig. 2.5, the different variables used stand for:

V_{DC} = magnitude of input DC voltage source

V_D = voltage drop across diode

V_{SW} = voltage drop across semiconductor switch

L_i = input inductor

R_D = on-state resistance of diode

R_{SW} = on-state resistance of switch

R_{esr} = equivalent series resistance of capacitor

C = capacitor (C_1 or C_2)

2.4. DESCRIPTION OF SYNTHESIS OF POLE VOLTAGES

The operation of the converter circuit can be understood by considering an individual phase-leg, because all the other phase-legs are identical. The switching states which are shown in Table 3.1 are used to generate the desired pole voltages at the output terminals. Hence, the operation is primarily divided into three modes which are presented below:

Mode-0: $v_{xN} = 0$

This is mode is established in the state T0 when the switches S_{x2} & B_{x2} are turned ON which results in output pole voltage being zero w.r.t the shown neutral. This is shown in the Fig. 2.6.

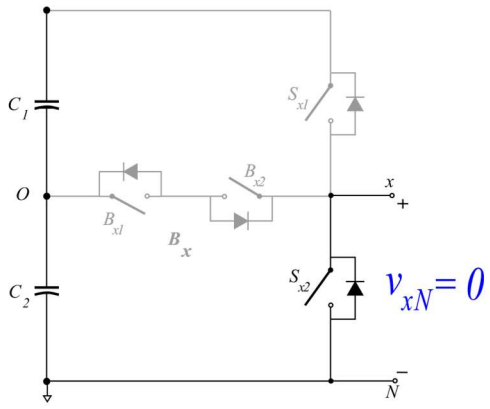

Fig. 2.6: Mode 0

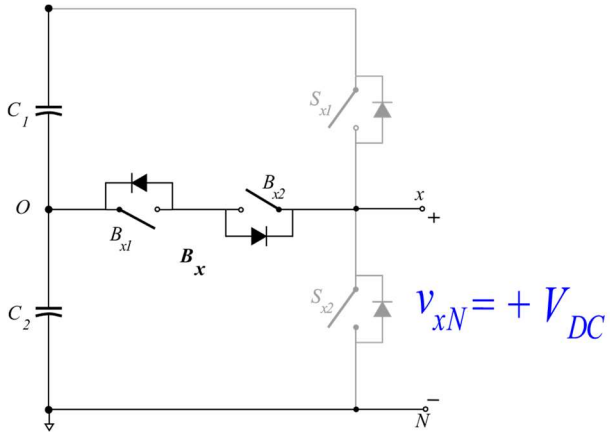

Fig. 2.7: Mode 1

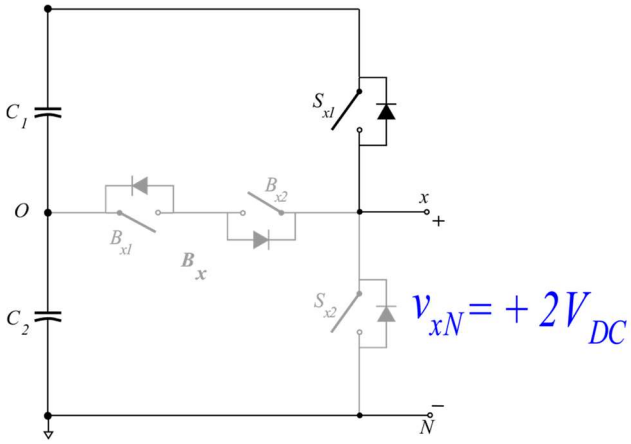

Fig. 2.8: Mode 2

Mode-1: $v_{xN} = +V_{DC}$

This is mode is established in the state T1 when the switches B_x (consisting of B_{x1} & B_{x2}) are turned ON which results in output pole voltage being $+V_{DC}$. This is shown in the Fig. 2.7.

Mode-2: $v_{xN} = +2V_{DC}$

This is mode is established in the state T2 when the switches S_{x1} & B_{x1} are turned ON. This results in output pole voltage being $+2V_{DC}$. This is shown in the Fig. 2.8.

Fig. 2.6-2.8 below show the diagrams having different operating modes for output pole voltage generation.

2.5. MATHEMATICAL FORMULATION OF POLE VOLTAGE FOR A PHASE

The semiconductor switch (SW) can be expressed in the form of a boolean function depending upon its present state, i.e., whether it is acitve (ON) or inactive (OFF). This function is defined as:

$$Switch,\ S = \begin{cases} 0\ , & when\ SW\ is\ inactive\ (OFF) \\ 1\ , & when\ SW\ is\ active\ (ON) \end{cases}$$

Therefore, the switching function for the output pole voltage expressed in terms of engaged switches can be written as :

$$v_{xN} = (2 \cdot S_{x1} + B_{x1} \cdot B_{x2}) \cdot V_{DC}$$

2.6. MODULATION

The converter transfers energy from a source in a controlled fashion using power semiconductor switches when they turned on and off at fast repetition rates [6]. The scheme as well as the process used to achieve these systematic transitions in a controlled and desired ways is called a modulation scheme [5]. Generally, those modulation schemes where width of the pulse is varied sinusoidally are used. Moreover, among these sinusoidal pulse width modulation schemes, level-shifted pulsewidth modulation(LS-PWM) scheme is being commonly used.

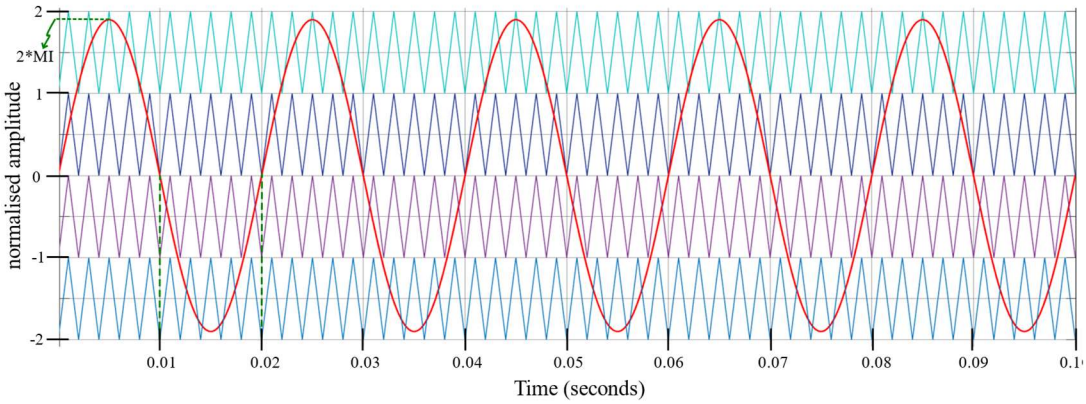

Fig. 2.9: Phase Dispostion (PD) LSPWM

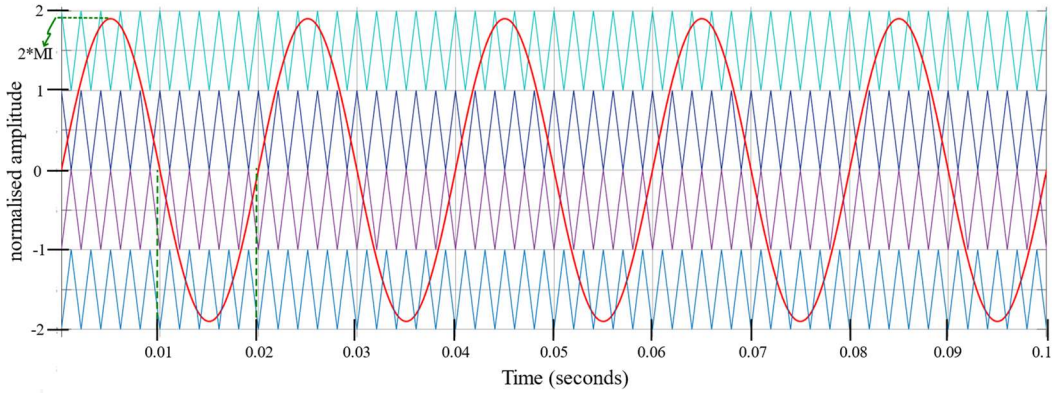

Fig. 2.10: Phase Opposition Disposition (POD) LSPWM

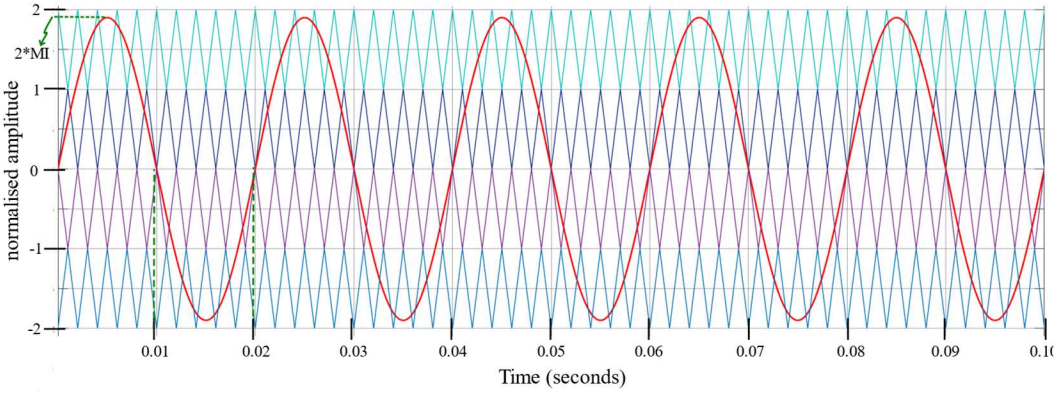

Fig. 2.11: Alternate Phase Opposition Disposition (APOD) LSPWM

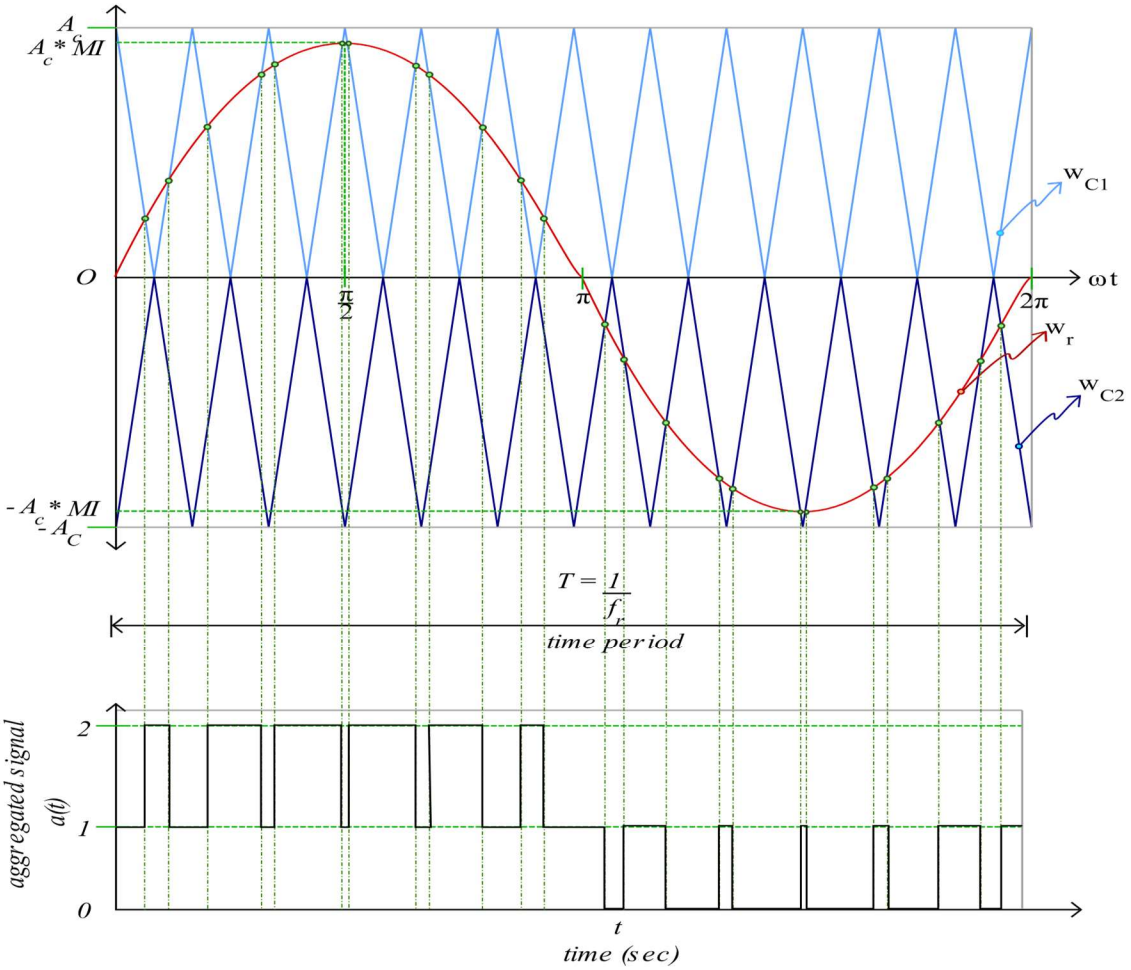

Fig. 2.12: The Phase Opposition Disposition LSPWM scheme and its aggregated signal, a(t)

In an LSPWM scheme, generally sine wave which is taken as a reference is compared with a triangular carrier wave. This has three types -- phase-dispostion (PD), phase opposition disposition (POD) and alternate phase opposition disposition (APOD). Diagrams in Fig. 2.9, 2.10 and 2.11 show three types of LSPWM schemes being employed for modulation of inverters.

Since for the modulation of the proposed topology, LSPWM scheme is being used, hence, it will be further explained in this work by taking Phase Opposition Disposition type as an example, which is shown in the Fig. 2.12. This desired scheme is implemented using Universal Control Scheme (UCS) [5], [25]. Here, two triangular carrier signals which are placed above and below the zero reference are compared with a sine reference wave. The amplitude and frequency of the

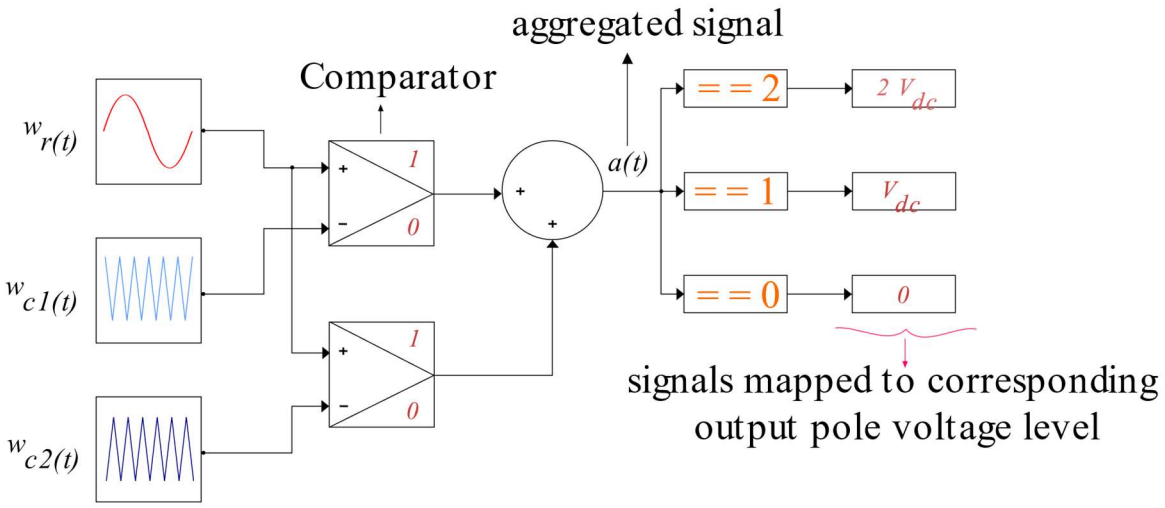

Fig. 2.13: Implementation of POD-LSPWM scheme for phase x

reference wave are taken to be A_r and f_r Hz , respectively. And the amplitude and frequency of carrier waves are taken to be A_c and f_c, respectively. Thus, the amplitude modulation index (MI) is defined as:

$$\text{MI} = \frac{A_r}{A_C}$$

The required comparison of reference wave with the carrier waves for achieving the desired switching of devices is explained in the following lines with the help of Fig. 2.13. When the sinusoidal reference signal is greater than or equal to each triangular carrier wave, the output of each comparator is '1' otherwise it will be '0'. The output of these comparator signals are added to yield an aggregated signal a(t), Fig. 2.12. This aggregated signal is again compared for different integral values which are then mapped to their corresponding output pole voltage values.

These digital output pole voltage values are ultimately used to provide the gate drive to the switch combination shown in Table 3.1. Note that the digital values '1' and '0' are binary logic values standing for turn-on and turn-off states of a switch respectively.

2.7. POTENTIAL APPLICATIONS

The low voltage power conversion has a line-to-line voltage of upto 690 V_{rms} (IEC) or 575 V_{rms} (ANSI) [26]. And in a general sense, the 2.3 to 6.6 kV is considered the medium voltage (MV) range and 1-50 MW is considered the high power range in the power converter industry.

Historically, the initial development of 3-level NPC topology utilizing diodes was for MV applications. This is due to the fact that it was necessary to have series connection of switches because of the limited voltage blocking capability of power semiconductor devices available. But this series connection of switches which increased conduction losses was overshadowed by the gain in voltage handling capability, which was in turn related to gain obtained in power handling capability. But this benefit is not suitable for low voltage applications where higher power is achieved by increasing the current levels. And conduction losses become a significant factor which limit the power range and should be kept as low as possible. Moreover, presently available power semiconductor technology have sufficient voltage ratings as well as switching speeds which could allow avoiding series connection of devices. Thus, the T-type topology is a better alternative for LV applications.

For MV applications, a single device does not have the sufficient voltage blocking capability to withstand full dc-link voltage. Hence, it is required to have series connection of two or more devices. This makes use of special active gate drive units necessary for transient and steady-state voltage balancing for power semiconductor devices [27], [28]. As a result, implementation effort is appreciably increased.

The use of T-type topology in MV applications deploying series connection of power devices for S_{x1} and S_{x2} is known as neutral point piloted (NPP) or transistor clamped converter (TCC) configuration shown in Fig. 2.14 [15], [29], [30]. Earlier, it was mentioned that the NPC topology was initially developed for MV applications because of use of series connection of switches. And coupled with the available switch combinations required in its valid states, employed for its different modulation strategies, it is natural to consider it for MV applications. And this topology has achieved already good market penetration.

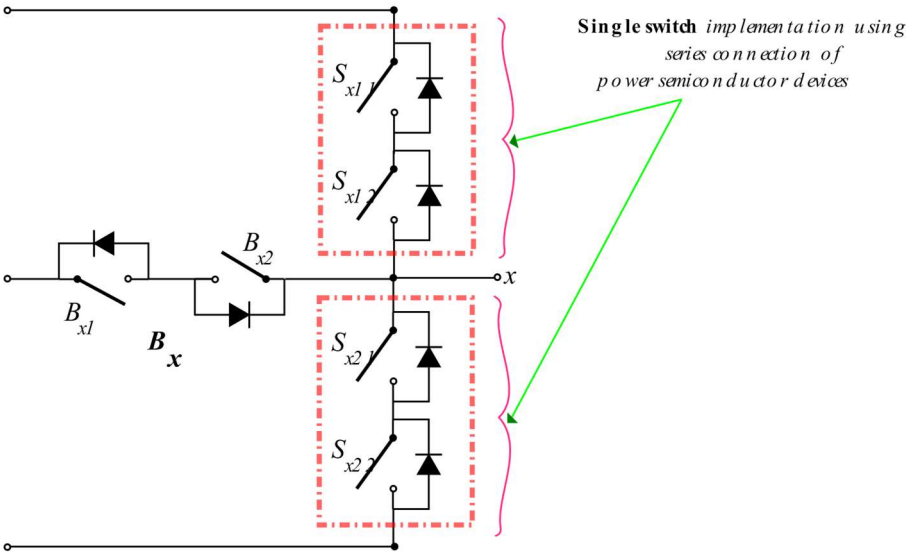

Fig. 2.14: Neutral Point Piloted (NPP) configuration

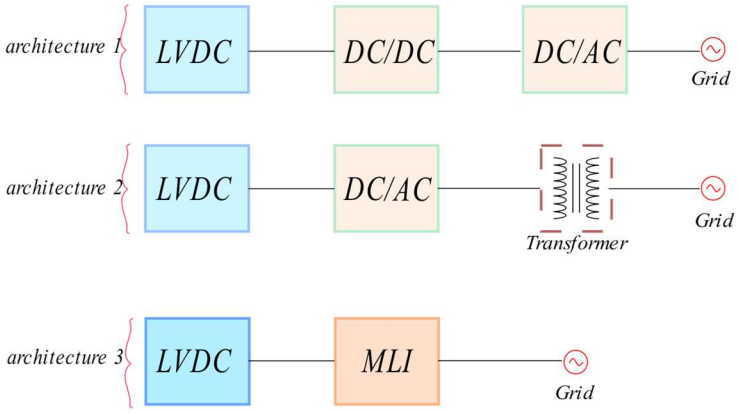

Fig. 2.15: architectures used by grid-connected power converters

But once the distribution of switching and conduction losses are taken into consideration, the NPP has an advantage even though the total losses are the same. This is because at higher modulation indexes, the outer switches, S_{x1} & S_{x4} of NPC(shown in Fig. 1.4), experience higher switching losses than inner ones. This results in a limitation in the capabiltiy with regards to components required in the implementation of NPC topology. Thus, the NPP configuration can also be used for MV application where higher current and frequency can be achieved for the same converter volume [29], [30].

The proposed topology could be used in LV as well as MV applications where voltage boosting from single-source DC voltage supply for a implementation in three-phase application is required. For instance, this could be in Photovoltaic (PV), fuel cell, electric vehicles (EV), and distributed energy sources (DES) applications where voltage boosting is generally required. Further, it could be useful for deployment in grid-connected converters where single stage conversion from the source can be achieved using transformerless operation due to its double voltage gain feature. Hence, reducing weight, volume and ultimately, cost of the system. Such an architecture comprising the mentioned situation is shown in Fig. 2.15.

Chapter-3
SIMULATION STUDIES

For the simulation of the proposed converter topology, MATLAB/SIMULINK environment is used and the reference parameters for the simulated block diagram model are shown in Table 3.1. The universal control scheme as presented in previous chapter is implemented for the modulation of the proposed converter circuit.

Table 3.1: Simulation Parameters

Parameter Name	Parameter Value
Input dc source voltage	285 V
Fundamental output frequency (f_r)	50 Hz
Carrier Frequency (f_c)	5.1 KHz
Capacitors ($C_1 = C_2$)	3000 μF
Load	R = 20 Ω & L= 30 mH
Modulation index (m)	1

The inverter is simulated for nominal power output of 100 kW and line-to-line voltage, Vrms=400V, under full load condition.

Further, the model is simulated and analysed for a balanced Y-connected load under two cases:

1. when we have a unity power factor (pf), thus, the load is purely resistive and

2. when we have typical power factor equal to 0.85

Moreover, the use of both Phase Dispostion (PD) as well as Phase Opposition Disposition(POD) LSPWM modulation scheme types are simulated to gain insight into variation of different aspects that will be observed. This is done to undertstand and establish various advantages obtained by using both the modulation scheme types. It is worth mentioning that APOD type LSPWM is not simulated because its use demands employing more than two carrier waves for its typical configuration formation as shown in Fig. 2.11 and present scenario requires only two carries.

Waveforms related to steady-state values of output phase voltages, line voltages and line currents are presented and analysed. Further, capacitor voltages and input source current are also analysed

for the above mentioned cases. These waveforms are shown for a duration of 0.1 seconds during steady-state operation when capacitors are precharged. Finally, the FFT results are also shown.

3.1. SIMULATION USING PODLSPWM GATE DRIVER

This section will show and analyse the simulation results obtained from the proposed topological structure when Phase Opposition Disposition LSPWM strategy is used for modulation of the converter model.

3.1.1. CASE 1 : unity power factor

The first case is when the inverter is operating with a purely resistive load giving a power factor of unity. Fig. 3.1 shows the phase voltage (line to neutral) of phase a, v_{an}, for a duration of 0.1 seconds under steady-state and below it is presented zoomed snapshot of it from t = 0.04 to t = 0.06 seconds. This time duration represents a complete cycle of time period equal to 20 milliseconds (ms), i.e., for a frequency of 50 Hz. We can observe that the phase voltage is a seven level wave. Phase voltage of other phases b and c have the same wave shape except for the fact that they are shifted by 120 degree.

Fig. 3.2 shows the line (line-to-line) voltage between phases a and b. Here, we can see in this figure that the line voltage is a multilevel wave of 5 levels. The upper waveform in the figure shows line voltage for a duration of 0.1 seconds while the lower waveform shows the zoomed snapshot of the same wave from t = 0.04 to t = 0.06 seconds.

Similarly, Fig. 3.3 shows the current response of the converter for the above mentioned duration of 0.1 seconds. The current response of all the phases a, b and c is shown in the figure, respectively.

Fig. 3.4 shows the snapshot of the simulated source current for the present case of purely resistive load. We can see that the average demand is almost constant during the steady state operation.

Fig. 3.5 shows the simulated voltages of the two capacitors present in the switched-capacitor leg. Here, we can note from this figure that the voltage of upper and lower capacitors, C_1 and C_2 respectively, is almost the same for the steady state condition.

FFT analysis of the output line voltage from the converter is shown in Fig. 3.6. It can be seen that the used PWM modulation produces a strong fundamental harmonic wave of 50 Hz with the side

bands located around the multiples of switching frequency of 5100 Hz. The calculated total harmonic distortion (THD) for unfiltered output line voltage wave turns out to be 31.86%.

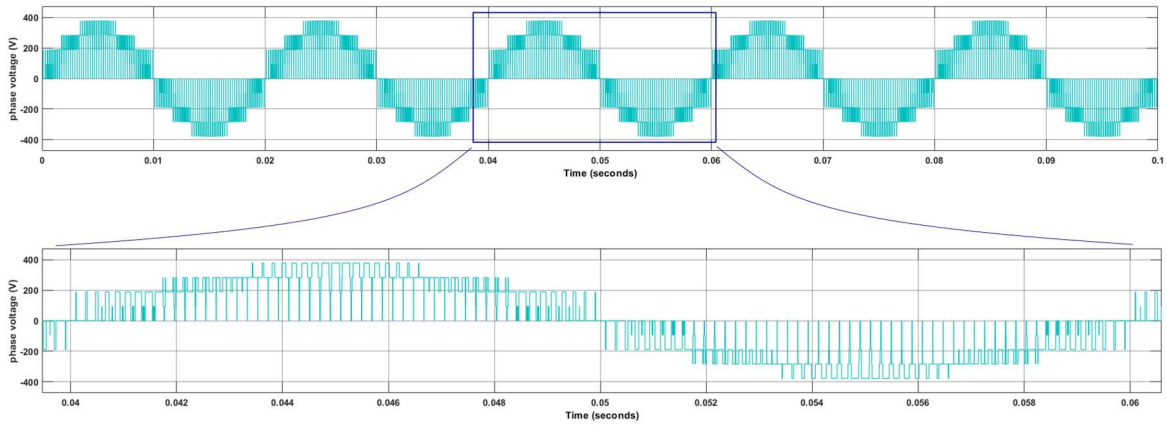

Fig. 3.1: snapshot of simulated steady-state phase voltage along with its zoomed snapshot for t = 0.04 to 0.06 seconds

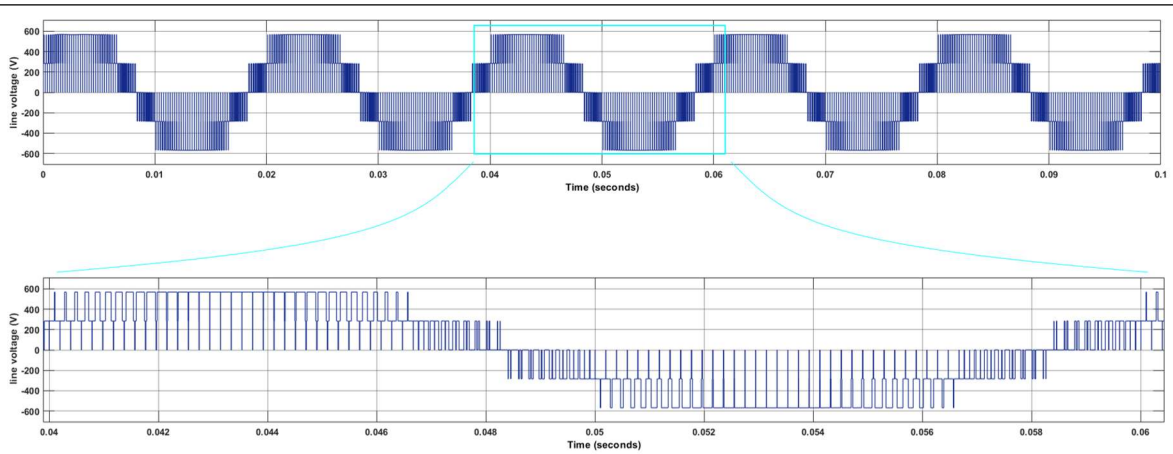

Fig. 3.2: snapshot of simulated steady-state l-l voltage along with its zoomed snapshot for t = 0.04 to 0.06 seconds

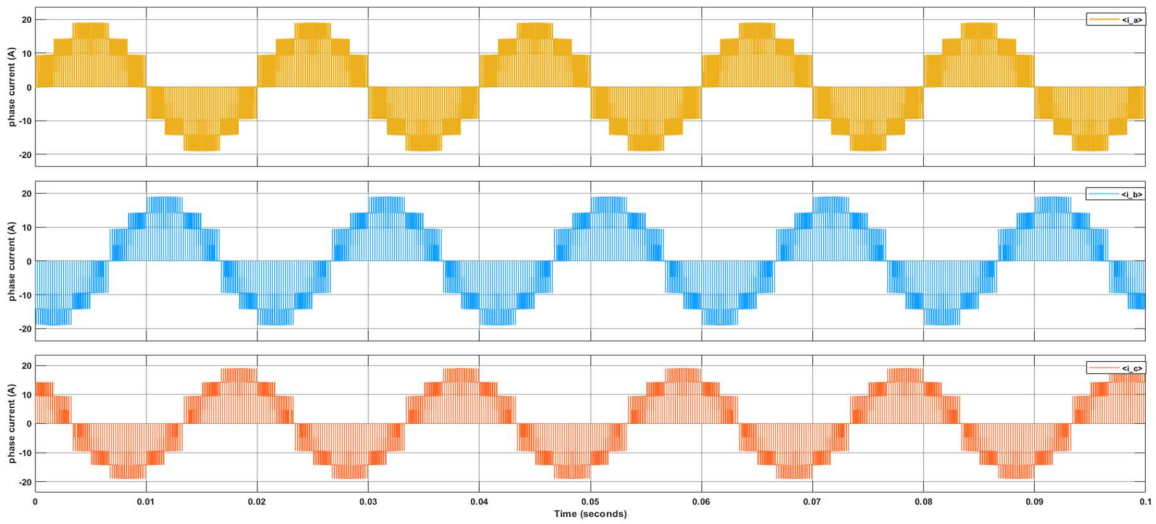

Fig. 3.3: snapshot of simulated steady-state phase current for phases a,b and c, respectively

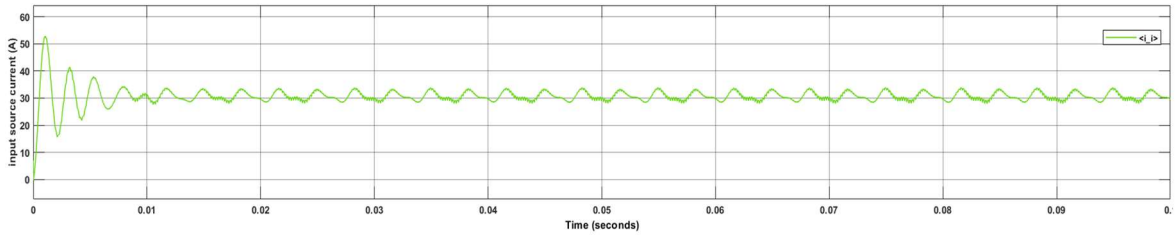

Fig. 3.4: snapshot of simulated steady-state value of input source current

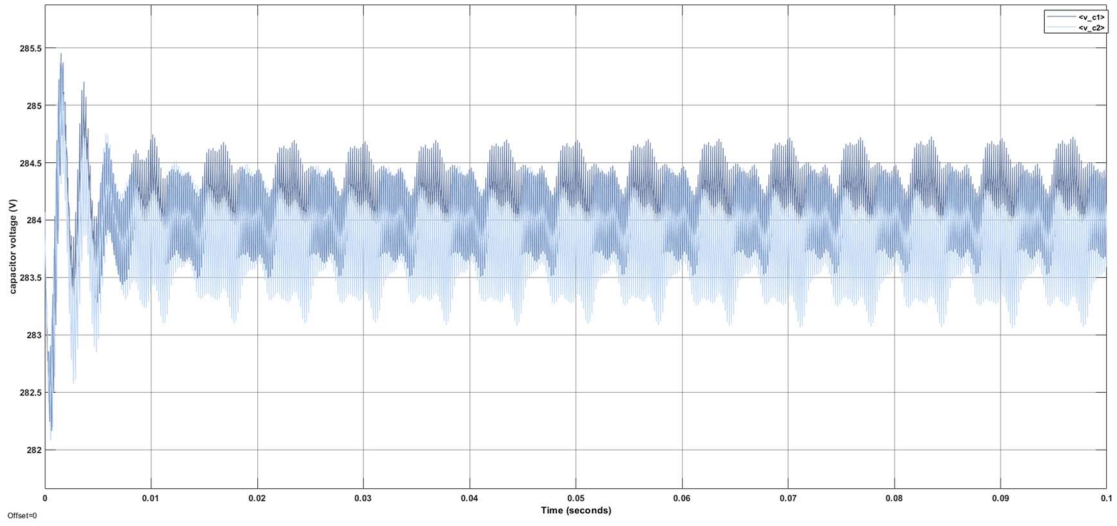

Fig. 3.5: snapshot of simulated steady-state capacitor voltages

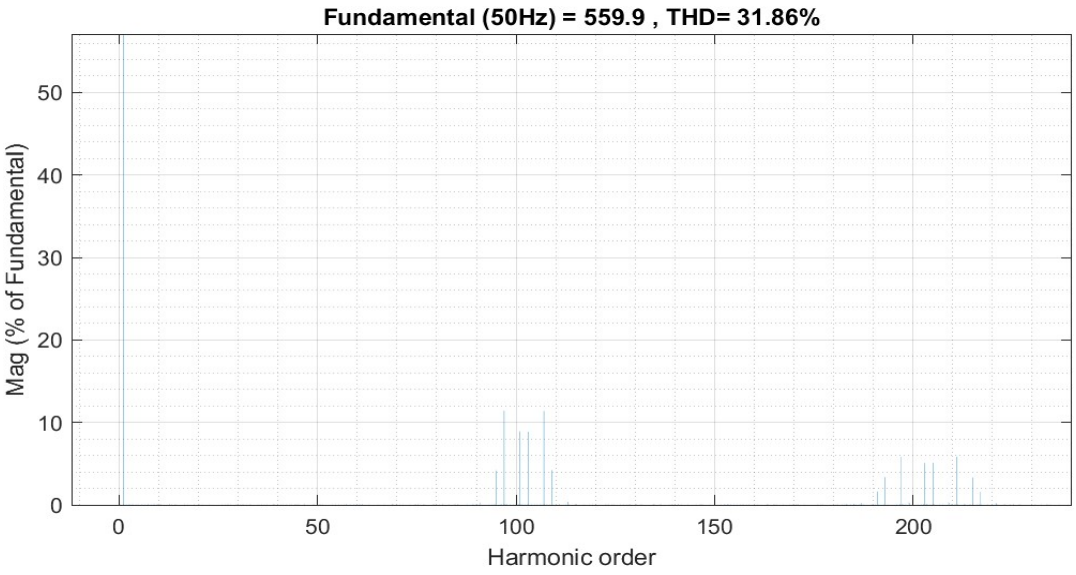

Fig. 3.6: FFT analysis window of line voltage

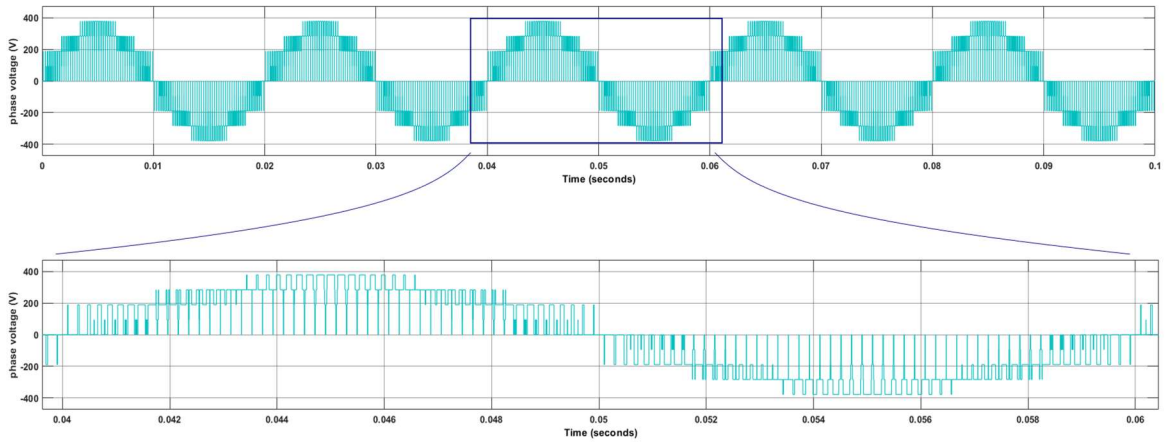

Fig. 3.7: snapshot of simulated steady-state phase voltage along with its zoomed snapshot for t = 0.04 to 0.05 seconds

3.1.2. CASE 2 : power factor = 0.85

This section presents the simulated response results of the converter for a load having a power factor = 0.85. Fig. 3.7 shows the steady-state phase voltage of phase a, v_{an}, and below it is shown zoomed view of the wave.

Fig. 3.8 shows the simulated line voltage between phases a and b. And Fig. 3.9 shows the phase currents of the three phases a,b and c respectively. We can clearly see that the now the current response is of sinusoidal form. This is because now the load is of inductive nature as the pf = 0.85.

Fig. 3.10 and Fig. 3.11 present the input source current and capacitor voltages, respectively. In Fig. 3.10, it can be observed that now the input source current has some ripple around its average value. Fig. 3.12 shows the FFT analysis window of the output line voltage. The calculated THD is almost of the same value of around 31% as which was the case when the pf was unity.

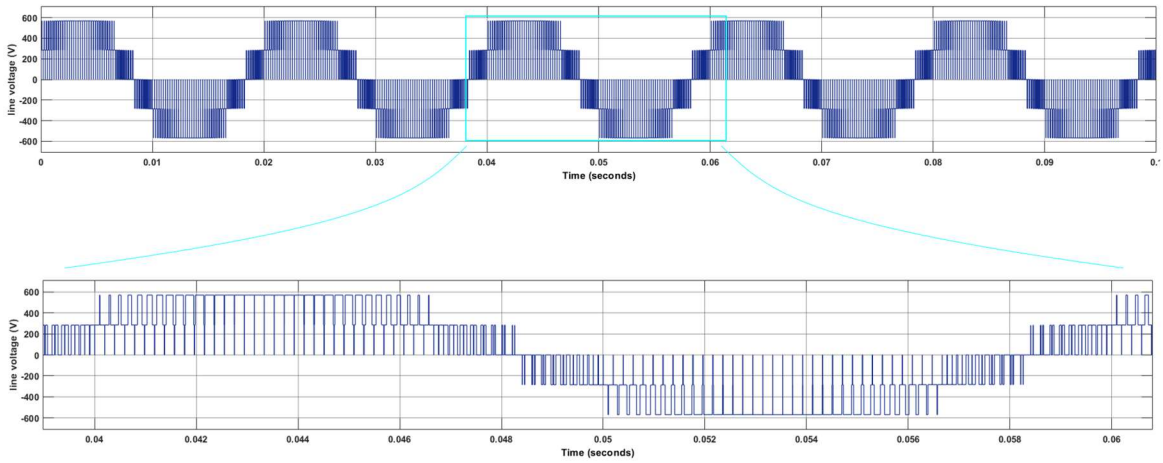

Fig. 3.8: snapshot of simulated steady-state l-l voltage along with its zoomed snapshot for t = 0.04 to 0.05 seconds

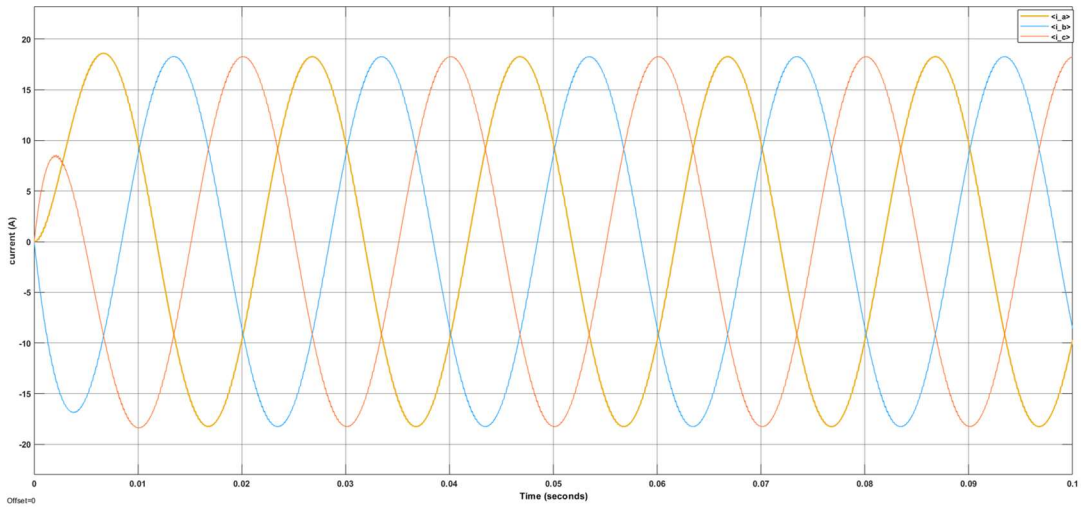

Fig. 3.9: snapshot of simulated steady-state phase current for phases a,b and c, respectively

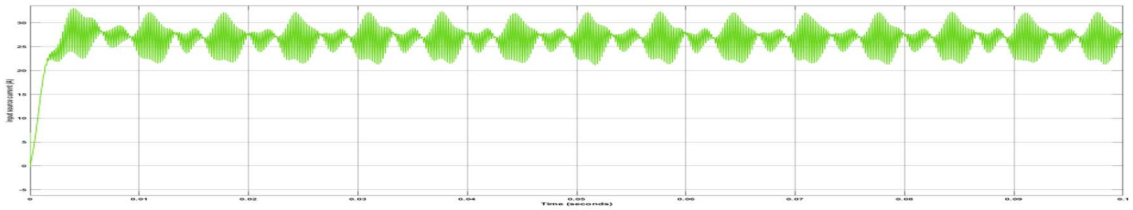

Fig. 3.10: snapshot of simulated steady-state value of input source current

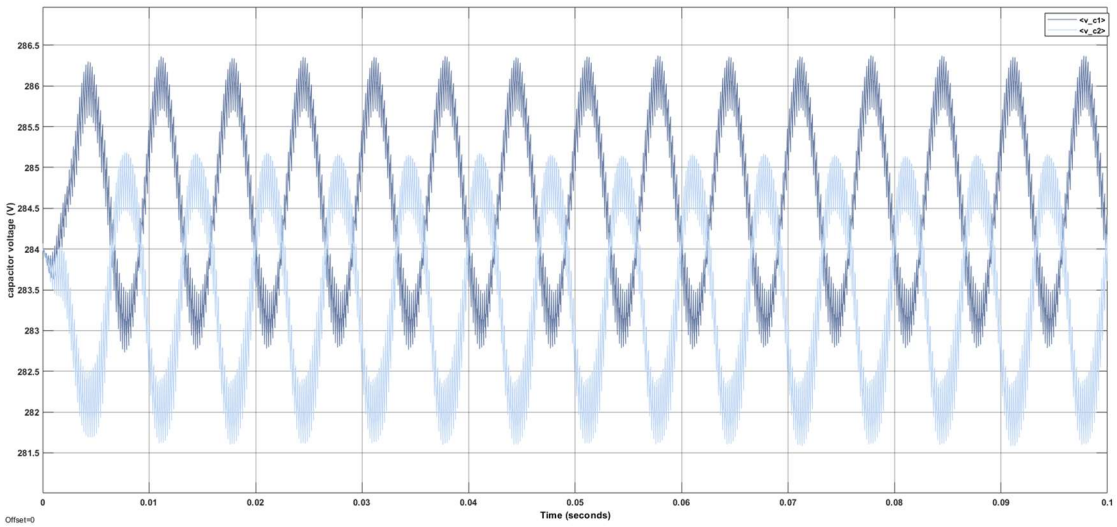

Fig. 3.11: snapshot of simulated steady-state value of capacitor voltages

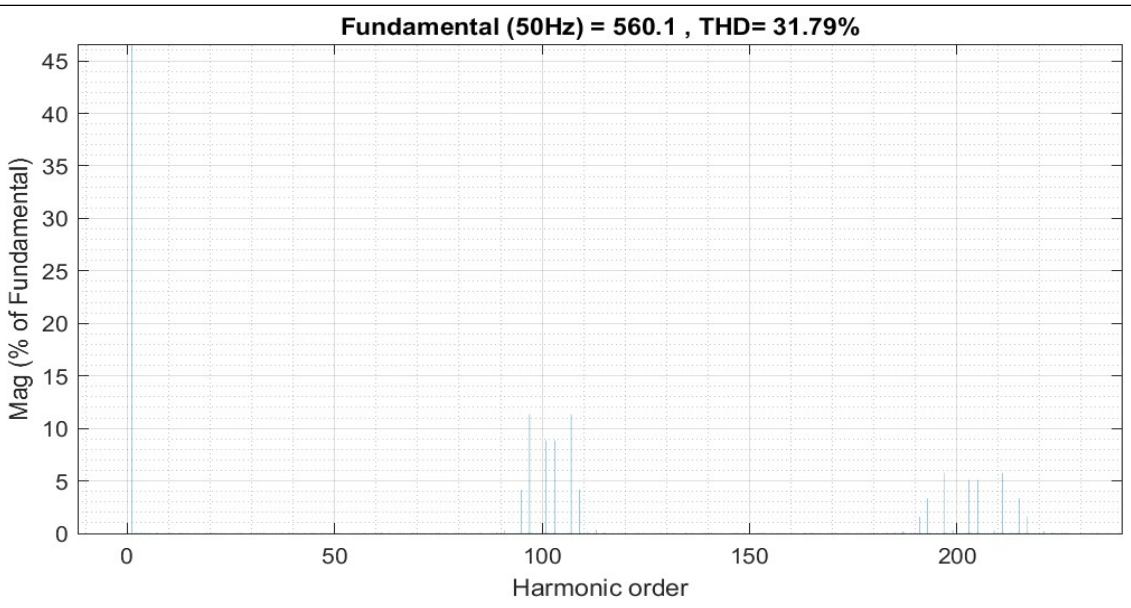

Fig. 3.12: : FFT analysis window of line voltage

3.2. SIMULATION USING PDLSPWM GATE DRIVER

This section will show and analyse the simulation results obtained from the proposed topological structure when Phase Disposition LSPWM (PDLSPWM) strategy is used for modulation of the converter model. These results are shown for similar cases as was done in section 3.1.

3.2.1. CASE 1 : unity power factor

This case is similar to the CASE-1 of the section 3.1 presenting the simulated response results for unity power factor load. Fig. 3.13 shows the steady-state phase voltage of phase a, v_{an}, and below it is shown zoomed view of the wave. Fig. 3.14 shows the simulated line voltage between phases a and b. The line voltage is a five level wave.

Fig. 3.15 shows the phase currents of the three phases a,b and c respectively. Fig. 3.16 shows the snapshot of the simulated source current for the present case of purely resistive load. Fig. 3.17 shows the simulated voltages of the two capacitors present in the switched-capacitor leg.

FFT analysis of the output line voltage from the converter is shown in Fig. 3.18. We can clearly see that the THD is 27.95 % and side bands are centered around frequency of 5100 Hz.

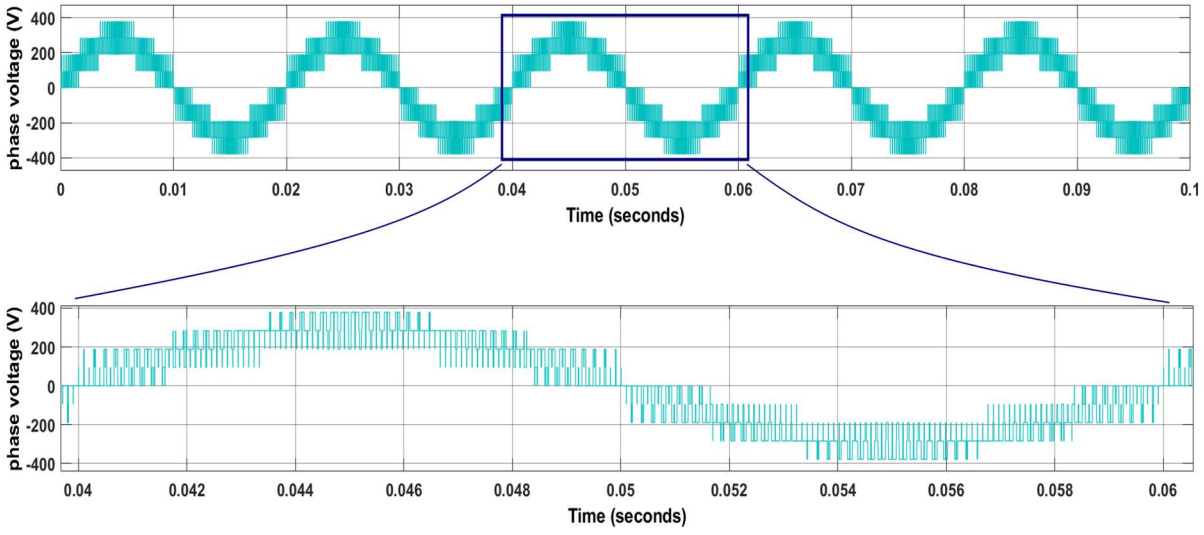

Fig. 3.13: snapshot of simulated steady-state phase voltage along with its zoomed snapshot for t = 0.04 to 0.05 seconds

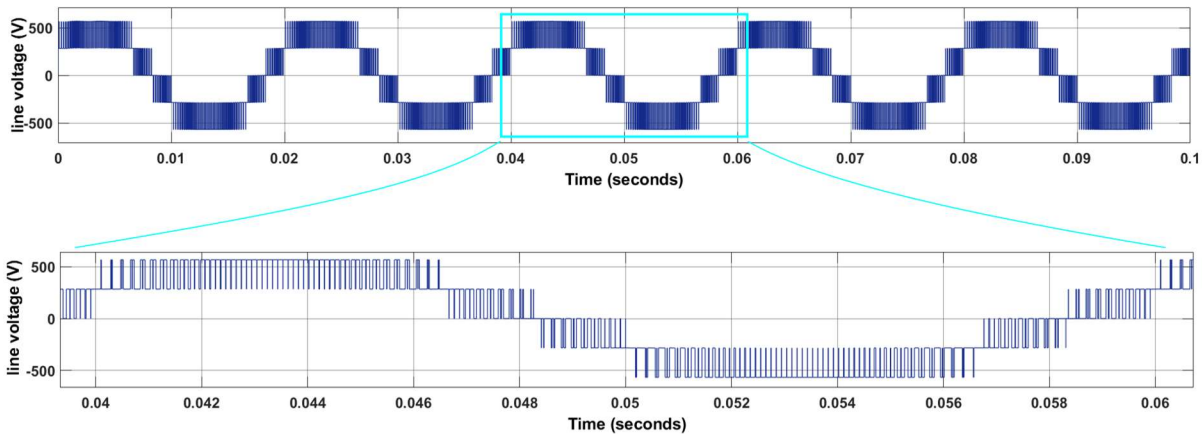

Fig. 3.14: snapshot of simulated steady-state l-l voltage along with its zoomed snapshot for t = 0.04 to 0.05 seconds

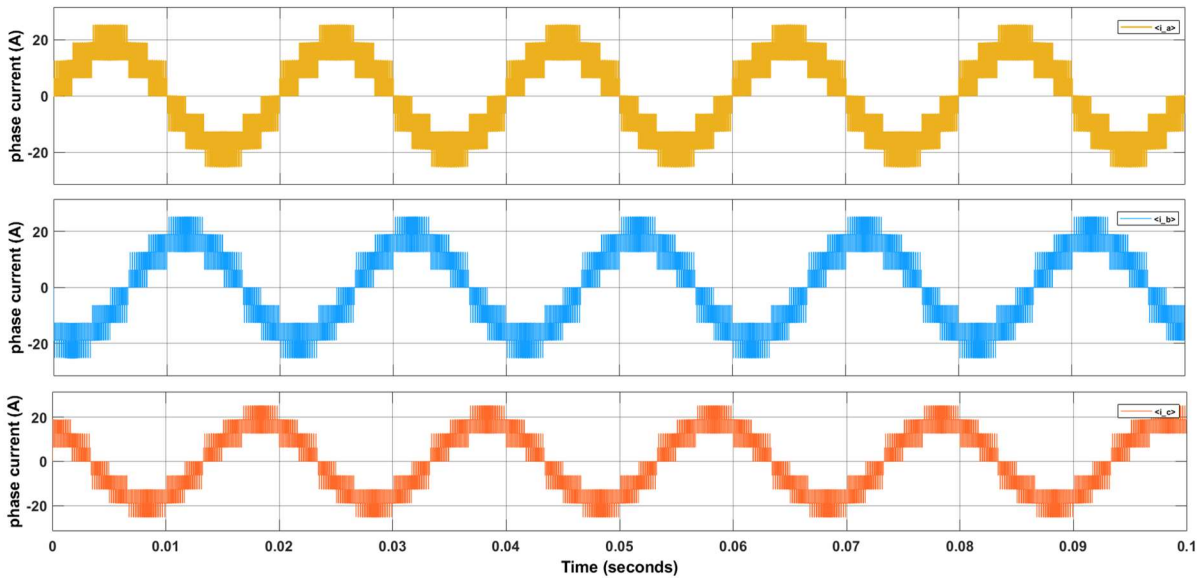

Fig. 3.15: snapshot of simulated steady-state phase current for phases a,b and c, respectively

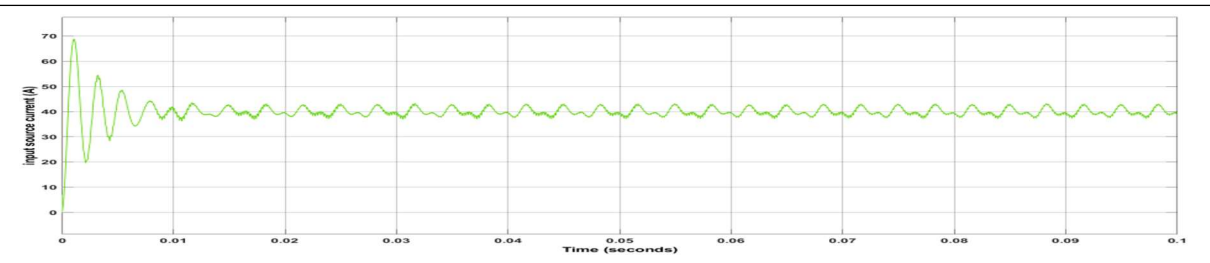

Fig. 3.16: snapshot of simulated steady-state value of input source current

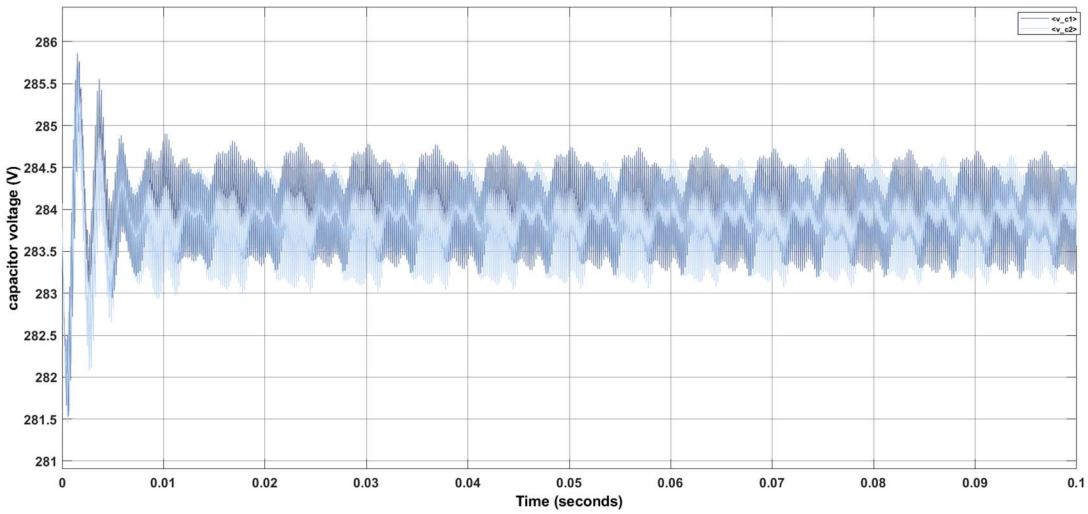

Fig. 3.17: snapshot of simulated steady-state value of capacitor voltages

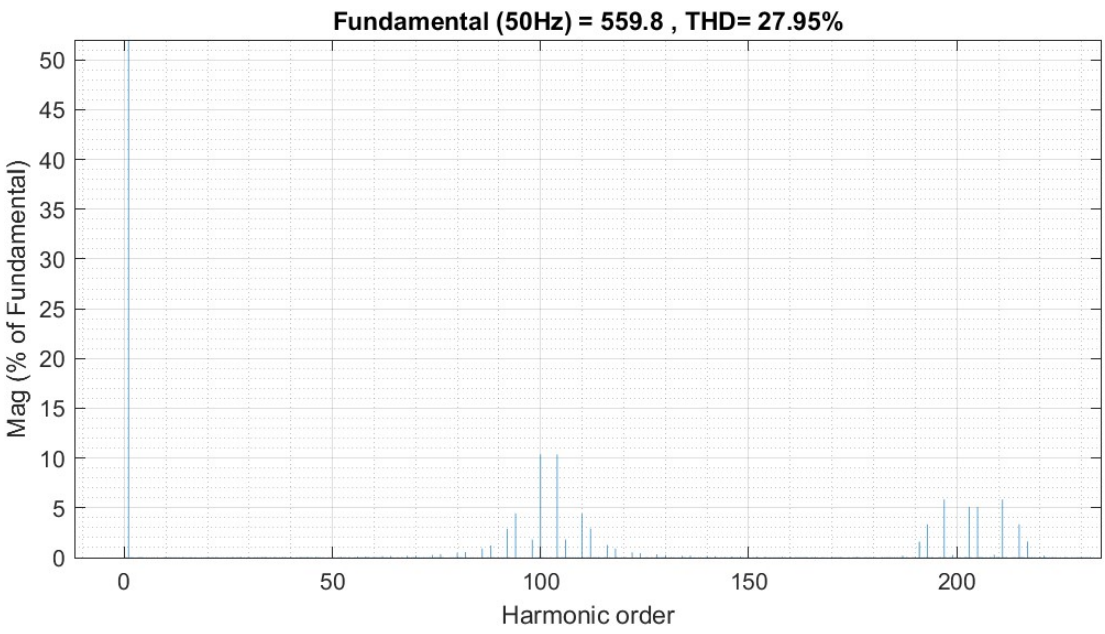

Fig. 3.18: FFT analysis window of line voltage

3.2.2. CASE 2 : power factor = 0.85

This case is similar to the CASE-2 of the section 3.1.2 presenting the simulated response results for pf = 0.85. Fig. 3.19 shows the steady-state phase voltage of phase a, v_{an}, and below it is shown zoomed view of the wave. And Fig. 3.20 shows the simulated line voltage between phases a and b. Similar to the case-1 in previous sub-section, the line voltage is a five level wave.

Fig. 3.21 shows the phase currents of the three phases a,b and c respectively. We can clearly see that the now the current response is of sinusoidal form. This is because now the load is of inductive nature as the pf = 0.85.

Fig. 3.22 and Fig. 3.23 present the input source current and capacitor voltages, respectively. In Fig. 3.22 it can be observed that now the input source current has some ripple around its average value.

Fig. 3.24 shows the FFT analysis window of the output line voltage. The calculated THD is almost of the same value of around 27.9 % which was the case when the pf was unity.

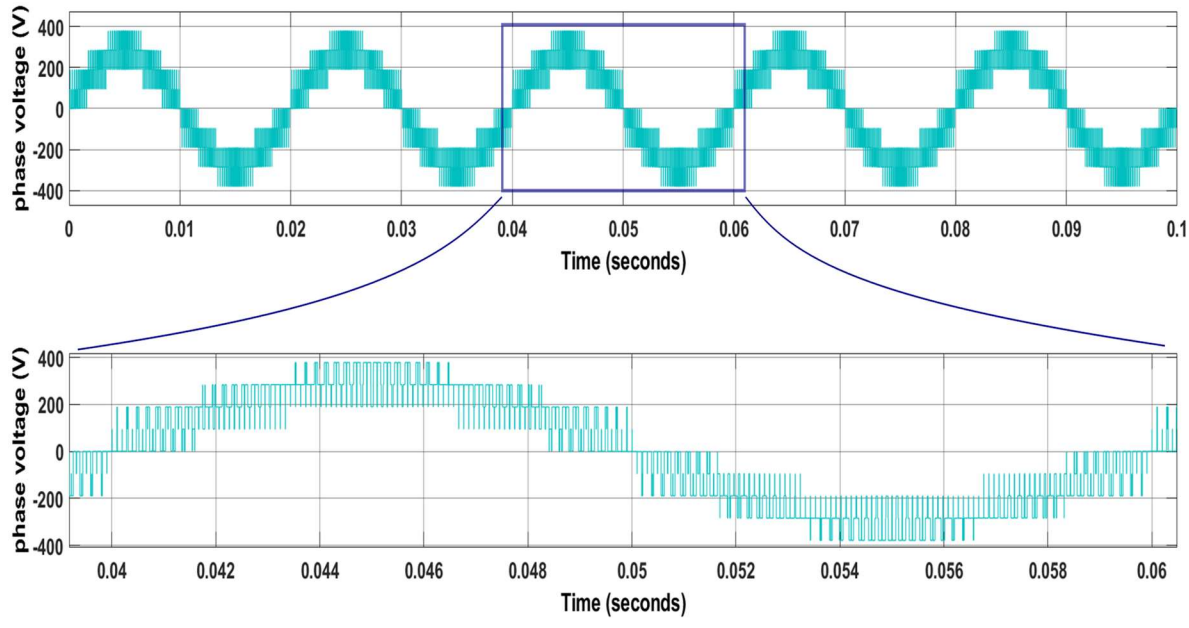

Fig. 3.19: snapshot of simulated steady-state phase voltage along with its zoomed snapshot for t = 0.04 to 0.05 seconds

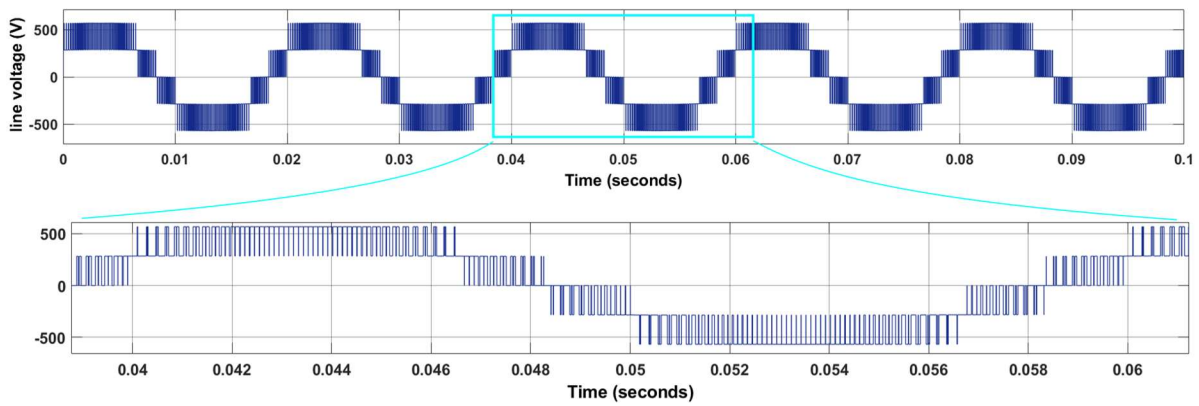

Fig. 3.20: snapshot of simulated steady-state l-l voltage along with its zoomed snapshot for t = 0.04 to 0.05 seconds

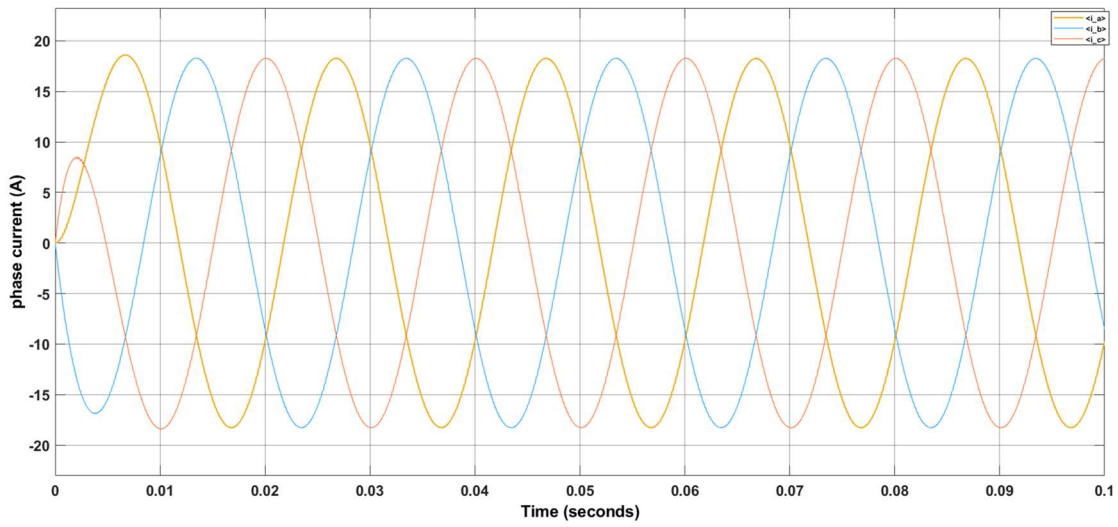

Fig. 3.21: snapshot of simulated steady-state phase current for phases a,b and c, respectively

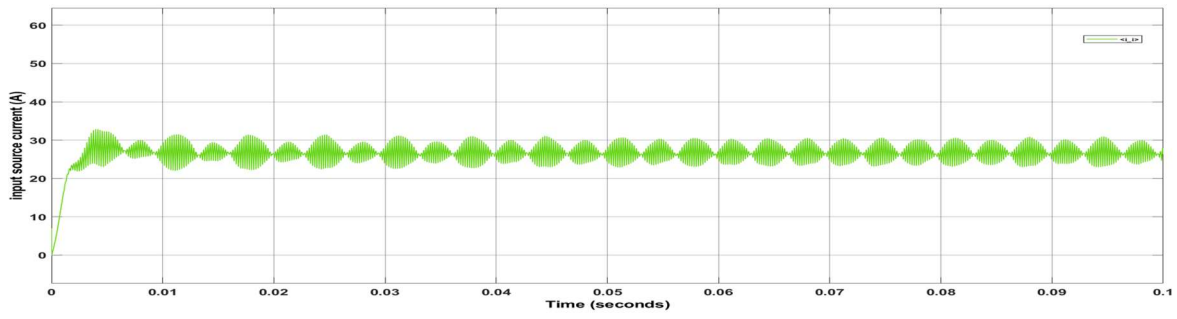

Fig. 3.22: snapshot of simulated steady-state value of input source current

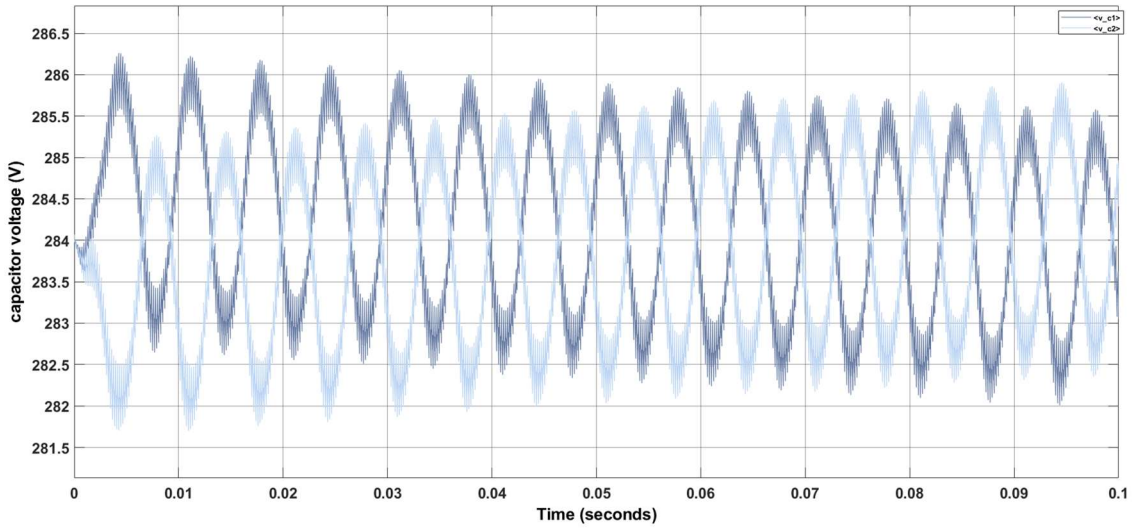

Fig. 3.23: snapshot of simulated steady-state value of capacitor voltages

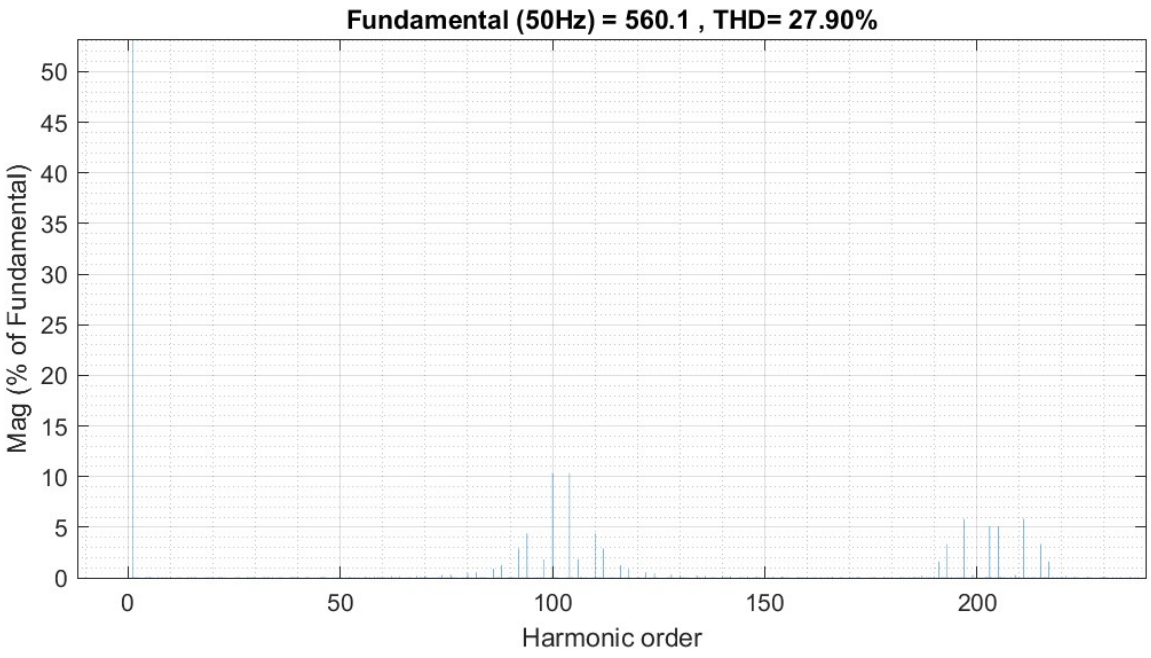

Fig. 3.24: FFT analysis window of line voltage

3.3. COMPARISON BETWEEN PD AND POD TYPE LSPWM

This section will highlight some of the distinct results obtained by employment of PD and POD type LSPWM algorithms in gate driver for modulation of proposed converter's simulation model. Here, differences between results for a pf = 0.85 are showed even though slight differences between other cases can also be observed.

3.3.1. Phase voltage and line voltage

Fig. 3.25 and Fig. 3.26 below show the comparison between the phase voltage and line voltage results obtained after simulating the converter model for one complete cycle. The upper and lower parts in both the shown figures show the results in case of POD and PD type schemes, respectively. In both figures, some part of both the positive and negative half cycles is highlighted since same stuff is happening in each case. And hence, we can focus our attention only towards positive half cycle.

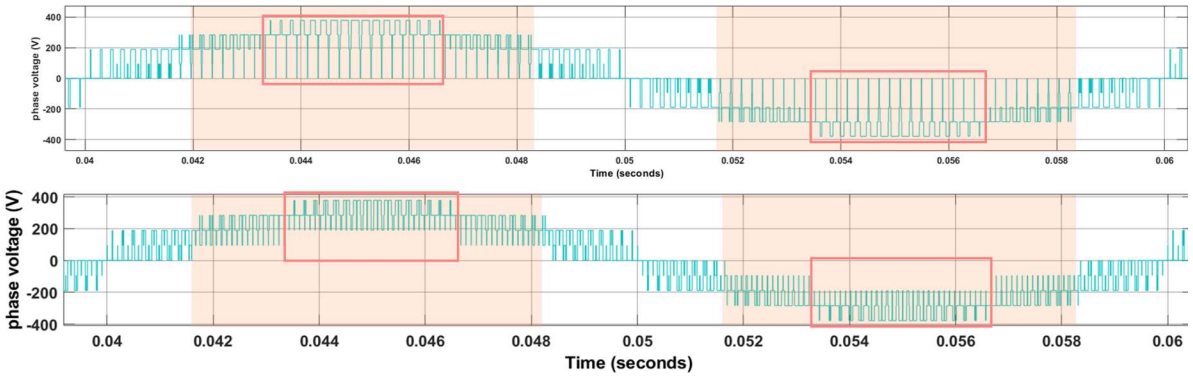

Fig. 3.25: phase voltage comparison between POD and PD type LSPWM modulation schemes

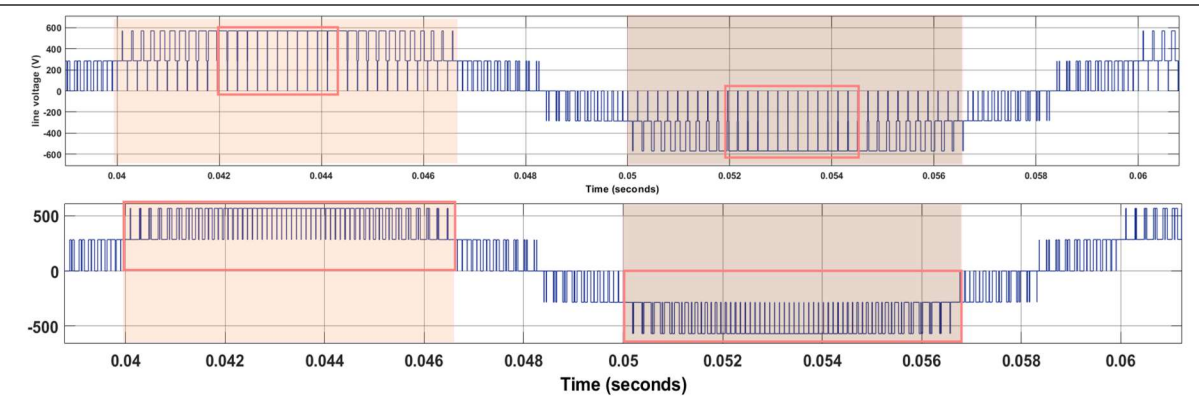

Fig. 3.26: line voltage comparison between POD and PD type LSPWM modulation schemes

In Fig. 3.25, we can see that during the positive half cycle in highlighted rectangular area, the voltage pulse is dropping from its value to zero in the upper part while the same does not happen in the lower part, thereby, dv/dt voltage stress has decreased. Moreover, the darker colour rectangular window inside the highlighted rectangular area shows the duration when this dv/dt voltage stress is the highest. Thus, this shows that in case of PD scheme, we could achieve lower dv/dt voltage stress.

In Fig. 3.26, the case is similar as in phase voltage case but there are slight differences. Even though the voltage drops similar as in phase voltage case for upper part's highlighted rectangalar area and has highest stress in the darker rectangular window, voltage does not drop to zero for the entire duration. Hence, in case of PD scheme, the dv/dt voltage stress for line voltage is halved.

3.3.2. Input source current

Fig. 3.27 shows the comparison in case of input source current and one complete cycle time period T = 0.02 sec (50 Hz) is highlighted in reactangular window. It can be seen that the steady-state wave shape in the lower part has smoothened and has lower peak-to-peak ripples. Thus, in case of PD type LSPWM scheme results in reduction of ripples and ultimately, input current harmonics.

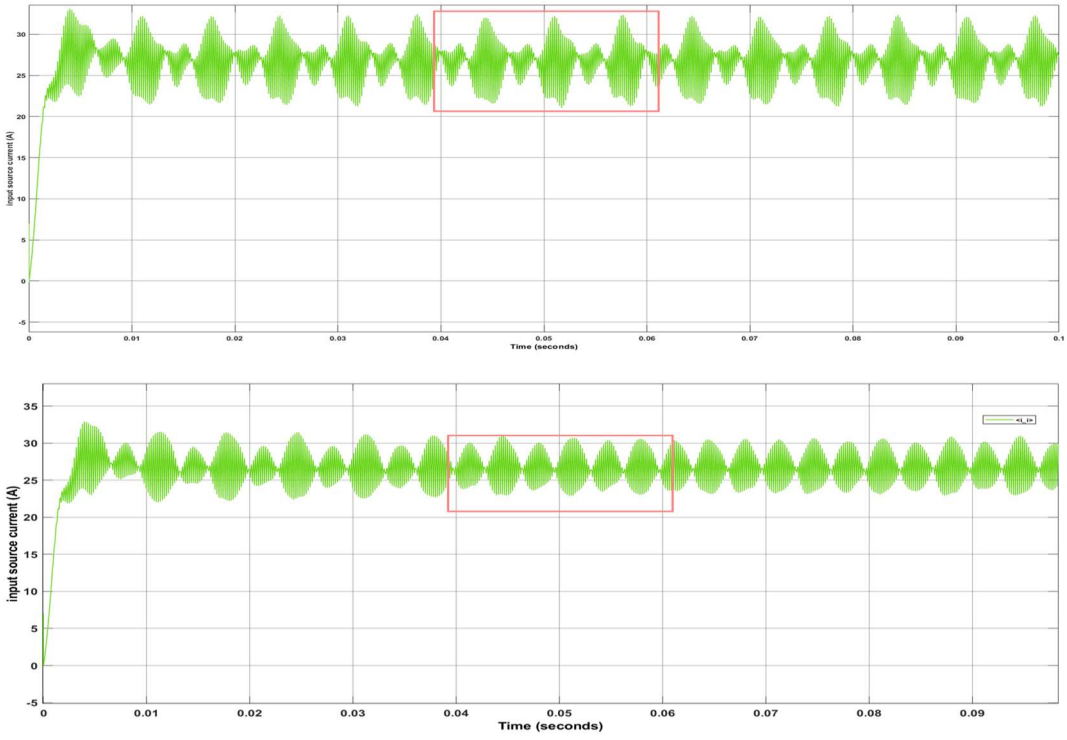

Fig. 3.27: input source current comparison for POD and PD type LSPWM schemes

3.3.3. Harmonic analysis of line voltage

Fig. 3.28 shows the FFT analysis comparison in case of POD and PD type LSPWM schemes. In both upper and lower parts frequency side bands are enveloped and differences are highlighted. We can observe that both schemes give a strong fundamental component of equal value along with the elimination of lower order harmonics. In case of first side band, there are slight differences; the envelope is of different shapes, reduced peak integral harmonic components in lower part around 10% and widened side band in case of lower part. This widened side band could result in slight decrease in cutoff frequency as well as slight increase in size of filter components. Further, we can see THD is highlighted on top in both the parts and can note that the use of PD type LSPWM has resulted in 3 % lower harmonic content which is a significant reduction.

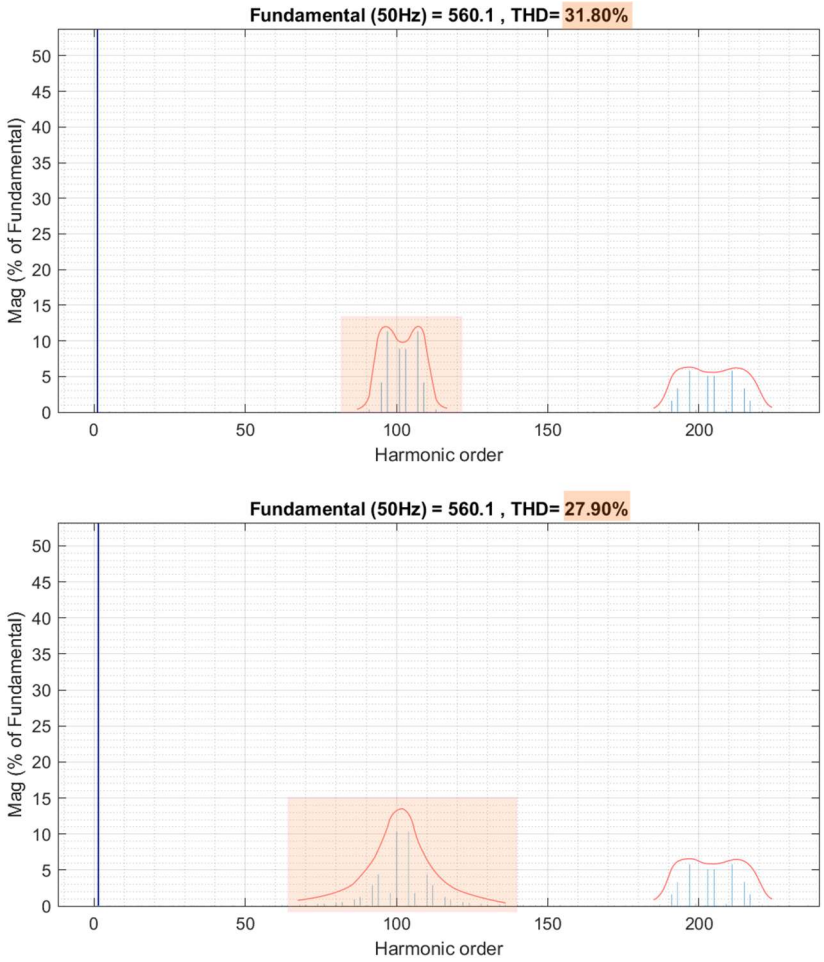

Fig. 3.28: FFT comparion in case POD and PD type LSPWM schemes

3.3.4. Results and Discussion

This section has compared the different aspects for the cases of Phase Opposition Disposition (POD) and Phase Disposition (PD) type LSPWM modulation schemes. Following were some of the obsered results of the comparison done:

- In case of both phase and line voltages, the use of PD scheme results in significant reduction in dv/dt voltage stresses. This is more pronounced in the case of line voltage.
- The use of PD scheme also results in smoothening of input source current wave as well as peak ripple reduction. Reduction of ripple results in reducing input current harmonics.
- Moreover, the use of PD results in reduction of harmonics and the THD reduces to 27.9 % from 31.80 % which is as significant reduction of 3%.
- Even though the PD scheme has resulted in harmonic reduction it has resulted in widened first side band which could slightly decrease the cutoff frequency as well slightly increase the filter component size if very good output wave is required.

Chapter-4
CONCLUSIONS AND FUTURE SCOPE

Following sections discuss the main conclusions of the present work and various aspects which could be worked upon in future studies making this work as its base.

4.1. CONCLUSIONS

This study has presented a novel switched-capacitor (SC) based topolgy. Further, the theory is presented showing the necessary aspects for understanding the different states and modulation of the topology. Also, following the theorectical analysis, simulations of the proposed converter structure were done and analysed. And these simulations were carried out in MATLAB/SIMULINK environment. This is where some of the parameters of the model especially the load and modulation scheme were varied. And the results were shown and later discussed. Finally, some conclusions and key takeaways are given below:

- A novel 3-phase switched-capacitor (SC) principle based T-type MLI topology is developed and presented.
- This topology has voltage boosting capabilities which means the ouptut voltage magnitude is greater than the input voltage magnitude, i.e., voltage gain is greater than 1.
- Moreover, a single dc voltage source is required for the 3-ϕ topology.
- The output line voltage is a 5-level PWM waveform which reduces harmonics and total harmonic distortion (THD).

4.2. FUTURE SCOPE

While this work has touched numerous aspects related to the proposed topology, there are still some areas which could be worked upon:

- First and foremost, the modulation part could be improved where the merits between use of sinusoidal pulsewidth modulation (SPWM) and space vector modulation (SVM) could be explored.

- Further, fault tolerance of the proposed topological structure could be explored and analysed.
- And finally, the use of the converter structure could be studied and applied to various relevant applications such electric vehicles (EV), Photovoltaics (PV), drives, etc.

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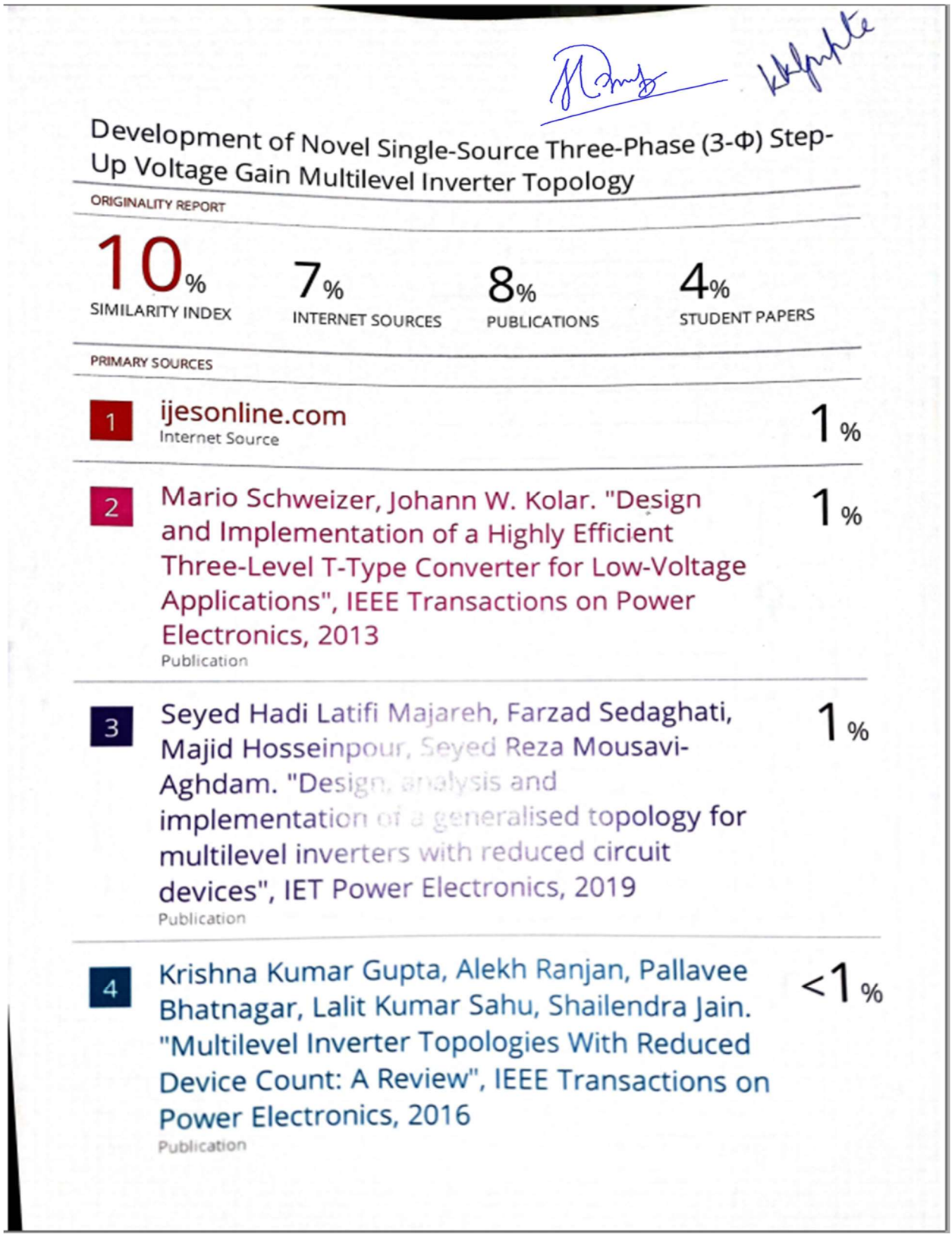

Development of Novel Single-Source Three-Phase (3-Φ) Step-Up Voltage Gain Multilevel Inverter Topology

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